

RIMINI

CPU : INTEL YONAH-ULV
Chip Set : INTEL 945GMS
Remarks : 1 Spindle

Model Name : RIMINI MAIN
With Docking / Without Docking
PCB Part No : BA41-00680A (TPT)
BA41-00683A (GCE)
Dev. Step : SR
Revision : 1.0
T.R. Date : 2006.05.11

DRAW	CHECK	APPROVAL
JULIO	HK PARK	JS EUH

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DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG
CHECK	HK, PARK	DEV. STEP	SR	MAIN		ELECTRONICS
APPROVAL	JS, EUR	REV	1.0	COVER		PART NO.
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	1	OF 50
						BA41-00680(3)A

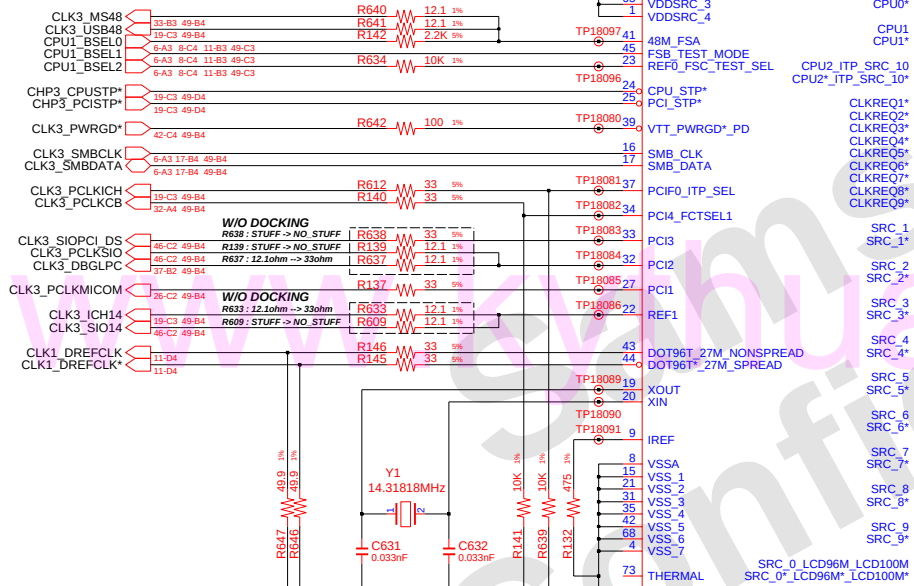
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CK410M+

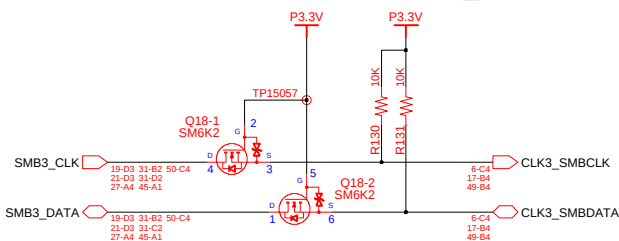
- FSB Frequency Select

CPU	FSB BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	0	266 MHz
0	0	1	1	333 MHz
0	1	0	0	200 MHz
0	1	1	1	400 MHz
1	0	0	0	133 MHz
1	0	1	1	100 MHz
1	1	0	0	166 MHz
1	1	1	1	RSVD



Trace Width *2
1205-002799 : SILEGO
1205-001801 : SILEGO
1205-002800 : CYPRESS
SMBUS Address "D2h"

CK-410M+	
w/ CLKREQ	ICS954305
w/ SS Clock	SL98LP455
	CY28447



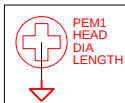
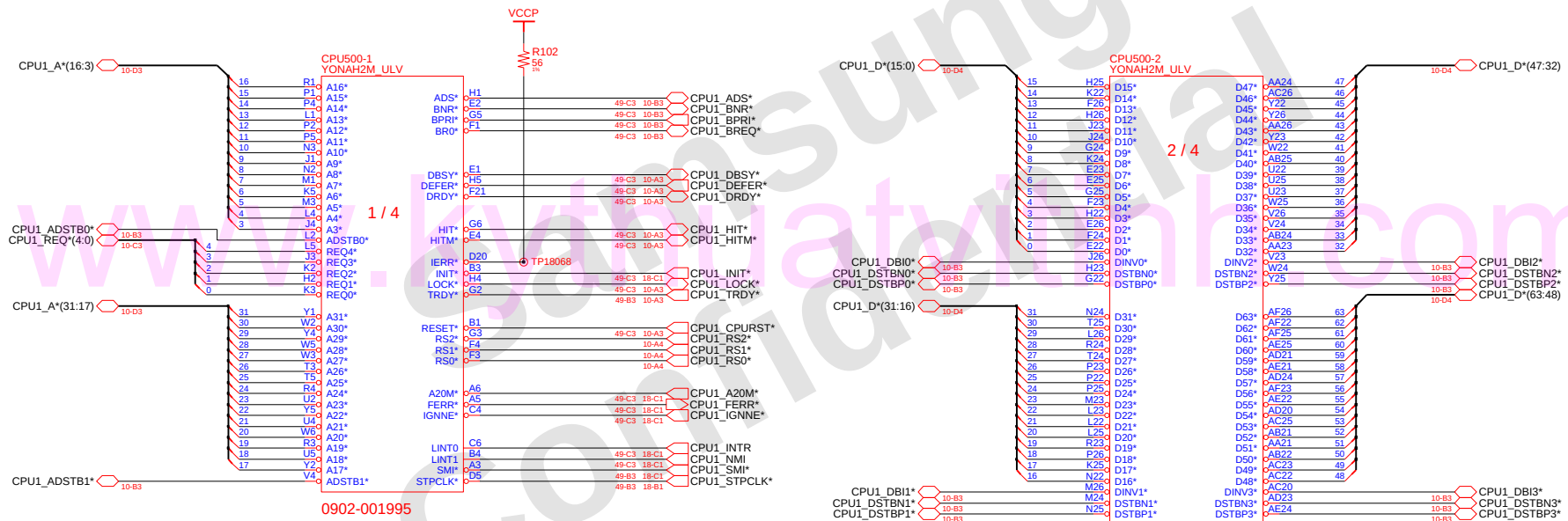
CPU1_BSEL0	6-C4 8-C4 11-B3 49-C3
CPU1_BSEL1	6-C4 8-C4 11-B3 49-C3
CPU1_BSEL2	6-C4 8-C4 11-B3 49-C3

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0			
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YONAH-ULV CPU (Single Core)

YONAH-ULV CPU S-SPEC			
1.2GHz	(C1)	QKGD	0902-001995
1.06GHz	(C1)	QKGE	0902-002031
933MHz	(C1)	Q5XY	

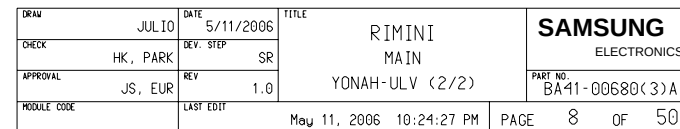


BA61-01090A[screw-gap130-41-h0250]

TOP : 5.5mm PAD
BOTTOM : 4.5mm PAD (SMT)
HOLE size : 2.95mm
Height : 1.5mm

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN YONAH-ULV (1/2)	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT				
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YONAH-ULV CPU (Single Core)



Place at the middle of CPU & GMCH

U505 W83L771W/G

1 VDD
2 DPLUS
3 DMINUS
4 T_CRIT_A*

5 SMBCLK
6 SMBDATA
7 ALERT*
8 GND

1209-001653
SMBus Address "5E"

CPU2_THERMDA 8-C4 49-B3

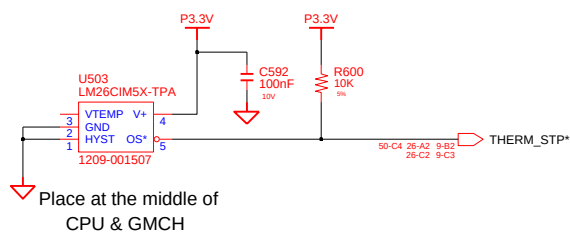
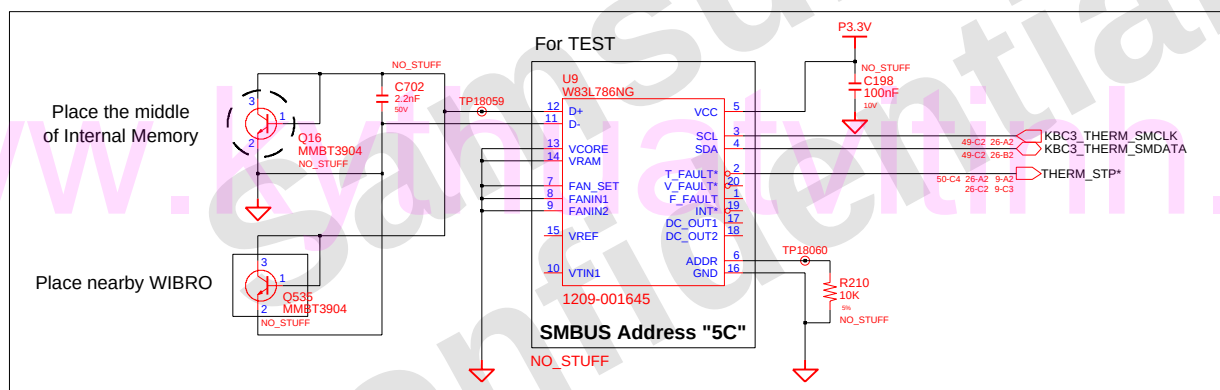
CPU2_THERMDC_THERM_STP+ 8-C4 49-B3
9-A2 26-A2 50-C4
9-B2 26-C2

R611 10K 5%
C612 2.2nF
R612 10K 5%
C611 100nF 10V
R604 10K 5%
R603 10K 5%

P3.3V
P3.3V
P3.3V

NO_STUFF
TP19005

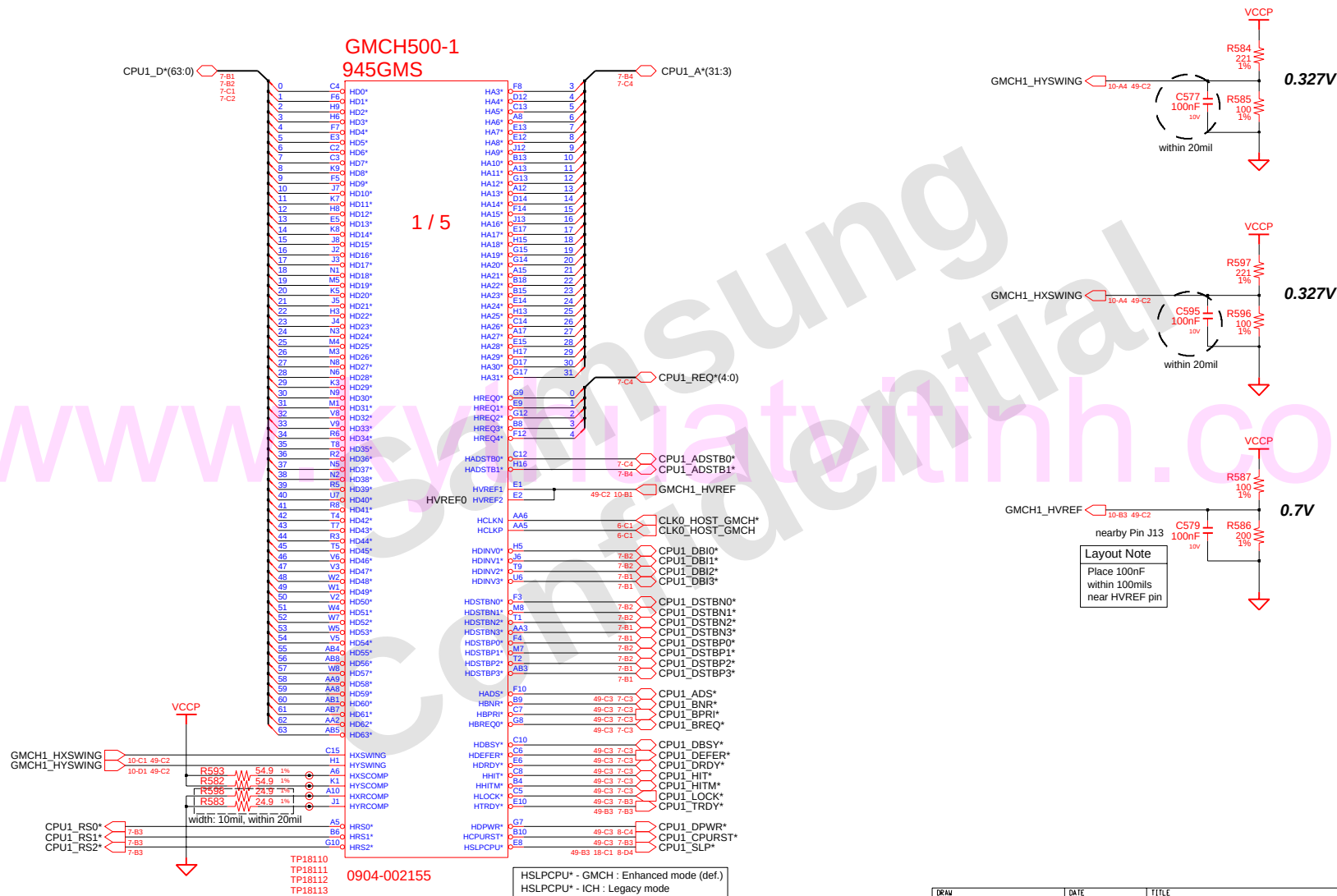
KBC3_THERM_SMCLK 49-C2 26-A2
KBC3_THERM_SMDATA 49-C2 26-B2
THERM_ALERT* 50-C4 18-C3
26-B4



DATE	JUL10	5/11/2006	TITLE	RIMINI MAIN THERMAL MONITOR			
CHECK	HK, PARK	DEV. STEP	SR			PART NO.	BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0				
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CALISTOGA-SFF

A3 Stepping : QK64



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CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0		CALISTOGA-SFF (1/4)	
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	10	OF 50



DATE	JULIO	5/11/2006	TITLE	RIMINI		SAMSUNG	
CHECK	HK, PARK	DEV. STEP	SR	MAIN		ELECTRONICS	
APPROVAL	JS, EUR	REV	1.0	CALISTOGA-SFF (2/4)		PART NO.	BA41-00680(3)A
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GMCH500-4
945GMS

CALISTOGA-SFF

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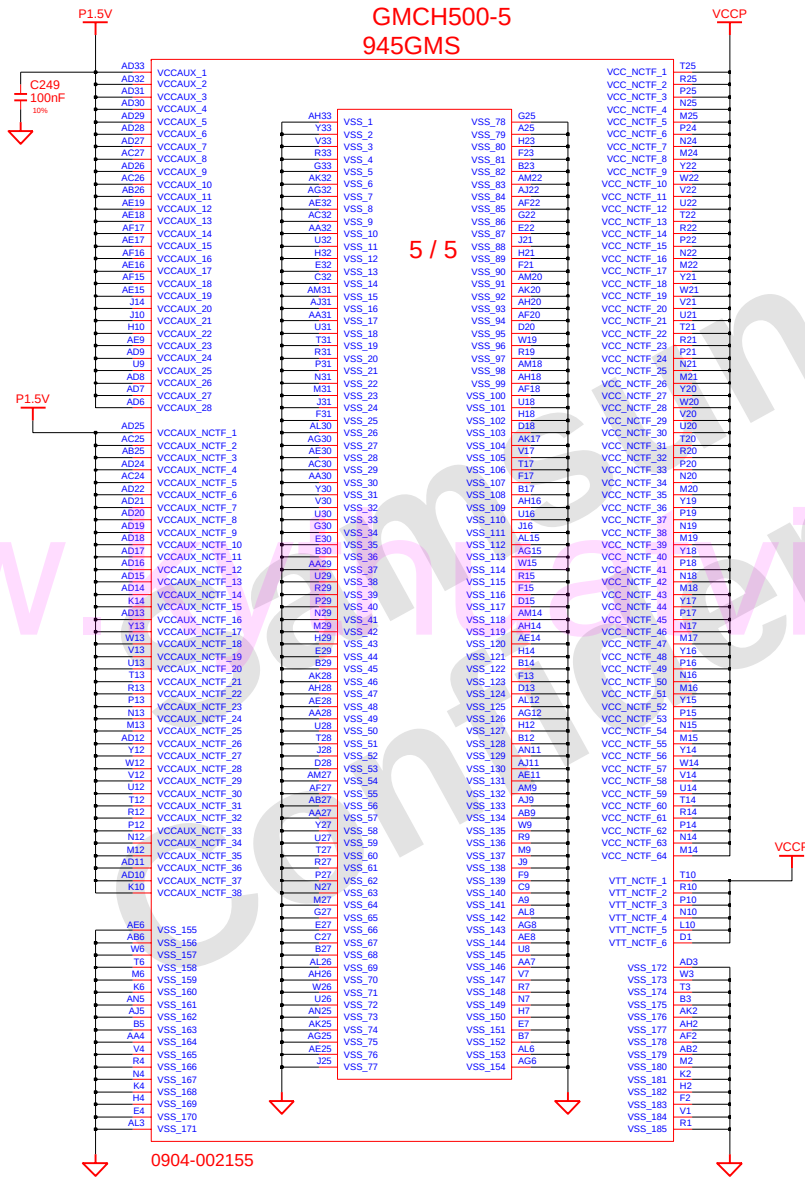
0904-002155

DRAW	JUL10	DATE	5/11/2006	TITLE	RIMINI MAIN CALISTOGA-SFF (3/4)	SAMSUNG ELECTRONICS
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CALISTOGA-SFF

GMCH500-5
945GMS



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CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0		CALISTOGA-SFF (4/4)	
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On Board MEMORY

1105-001680 : 512Mbit C-die

1105-001717 : 1Gbit C-die

DDR2 ON BOARD MEMORY

1. 512Mbit DDR2-533MHz x16 I/O

SAMSUNG: K4T51163QB-ZCD5

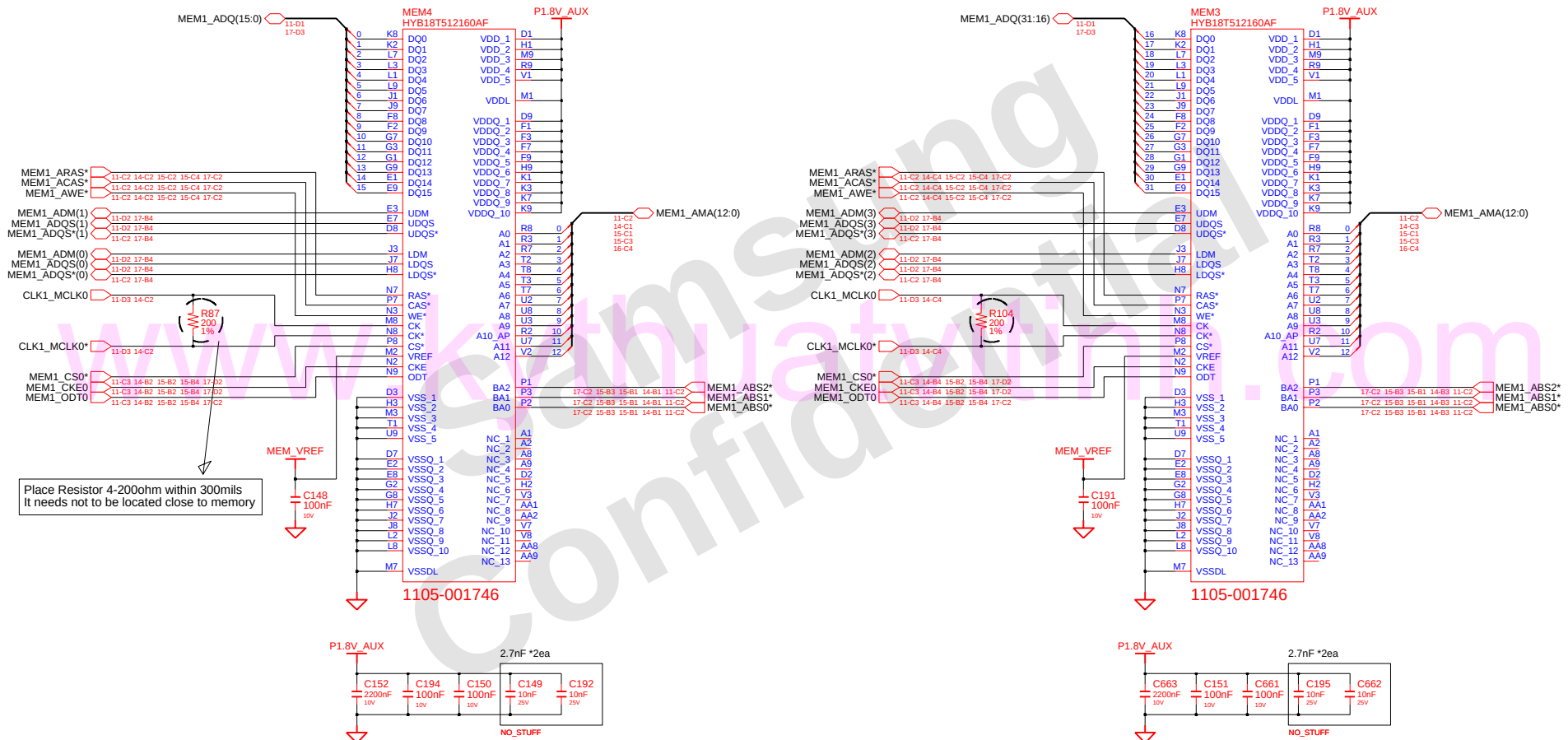
1105-001680

INFINEON: HYB18T512160AF-3.7

1105-001746

D0

D1



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG
CHECK	HK, PARK	DEV. STEP	SR	MAIN	MAIN	ELECTRONICS
APPROVAL	JS, EUR	REV	1.0	DDR2 ON BOARD (1/2)	PART NO.	BA41-00680(3)A
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM	PAGE	14 OF 50

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On Board MEMORY

1105-001680 : 512Mbit C-die

1105-001717 : 1Gbit C-die

DDR2 ON BOARD MEMORY

1. 512Mbit DDR2-533MHz x16 I/O

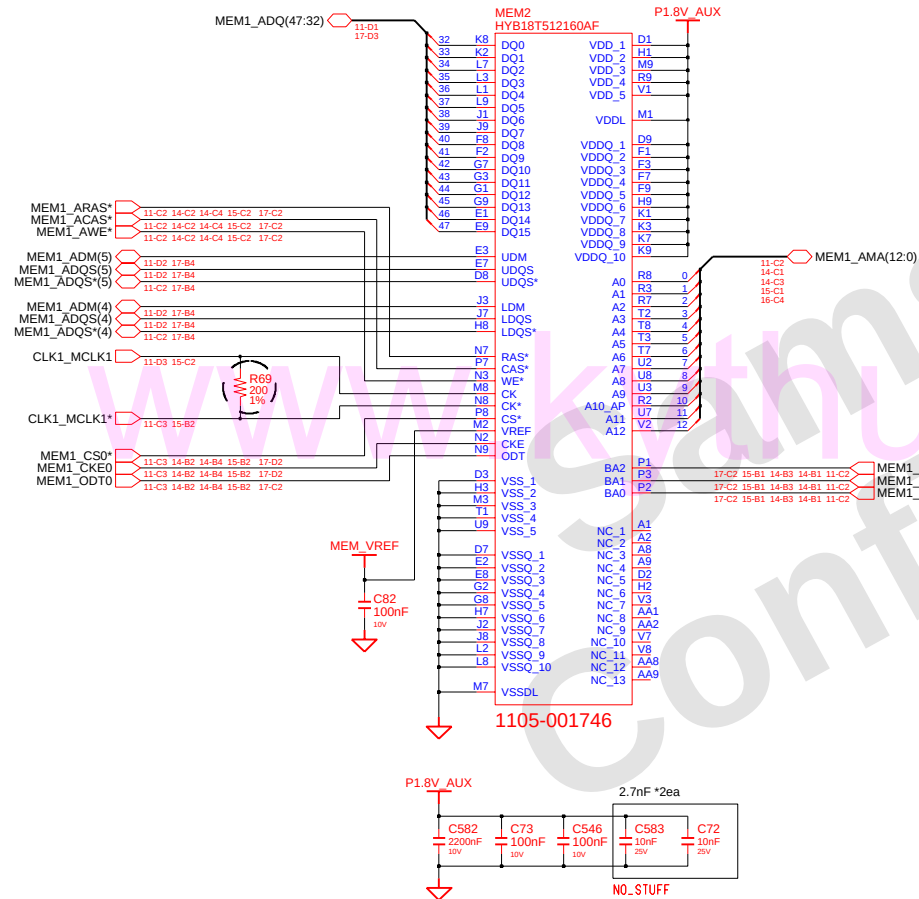
SAMSUNG: K4T51163QB-ZCD5

1105-001680

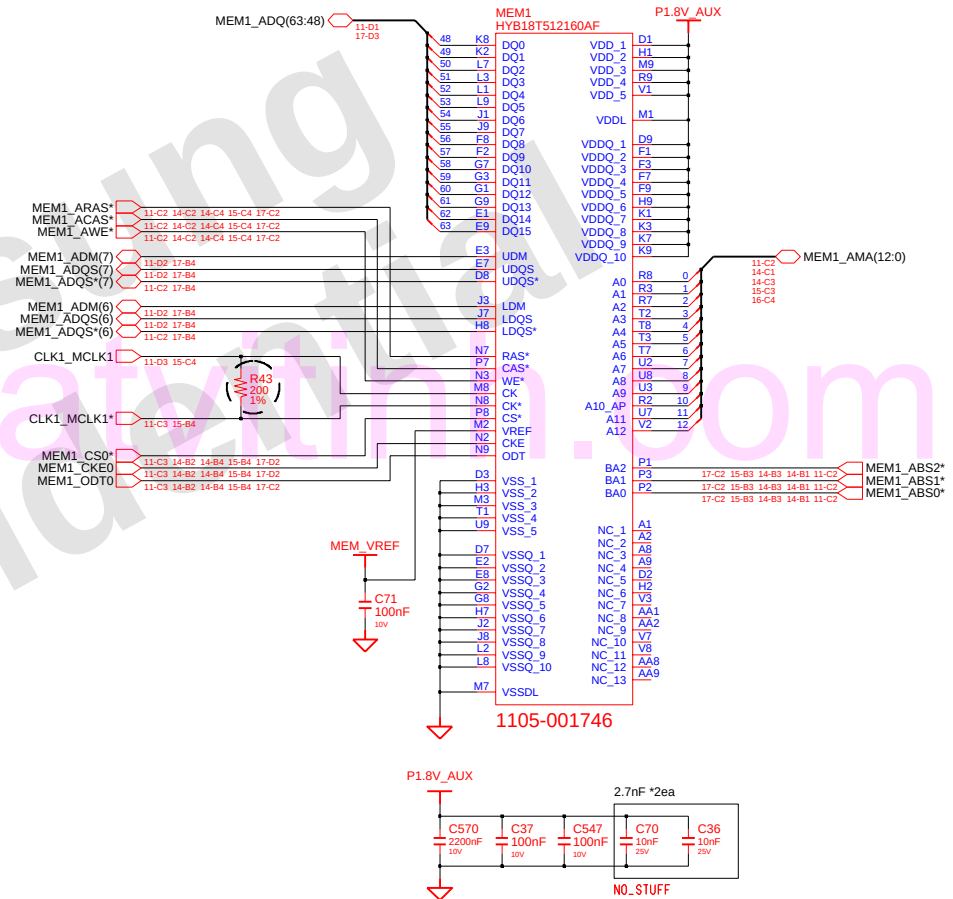
INFINEON: HYB18T512160AF-3.7

1105-001746

D2



D3



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG
CHECK	HK, PARK	DEV. STEP	SR	MAIN	MAIN	ELECTRONICS
APPROVAL	JS, EUR	REV	1.0	DDR2 ON BOARD (2/2)	PART NO.	BA41-00680(3)A
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM	PAGE	15 OF 50

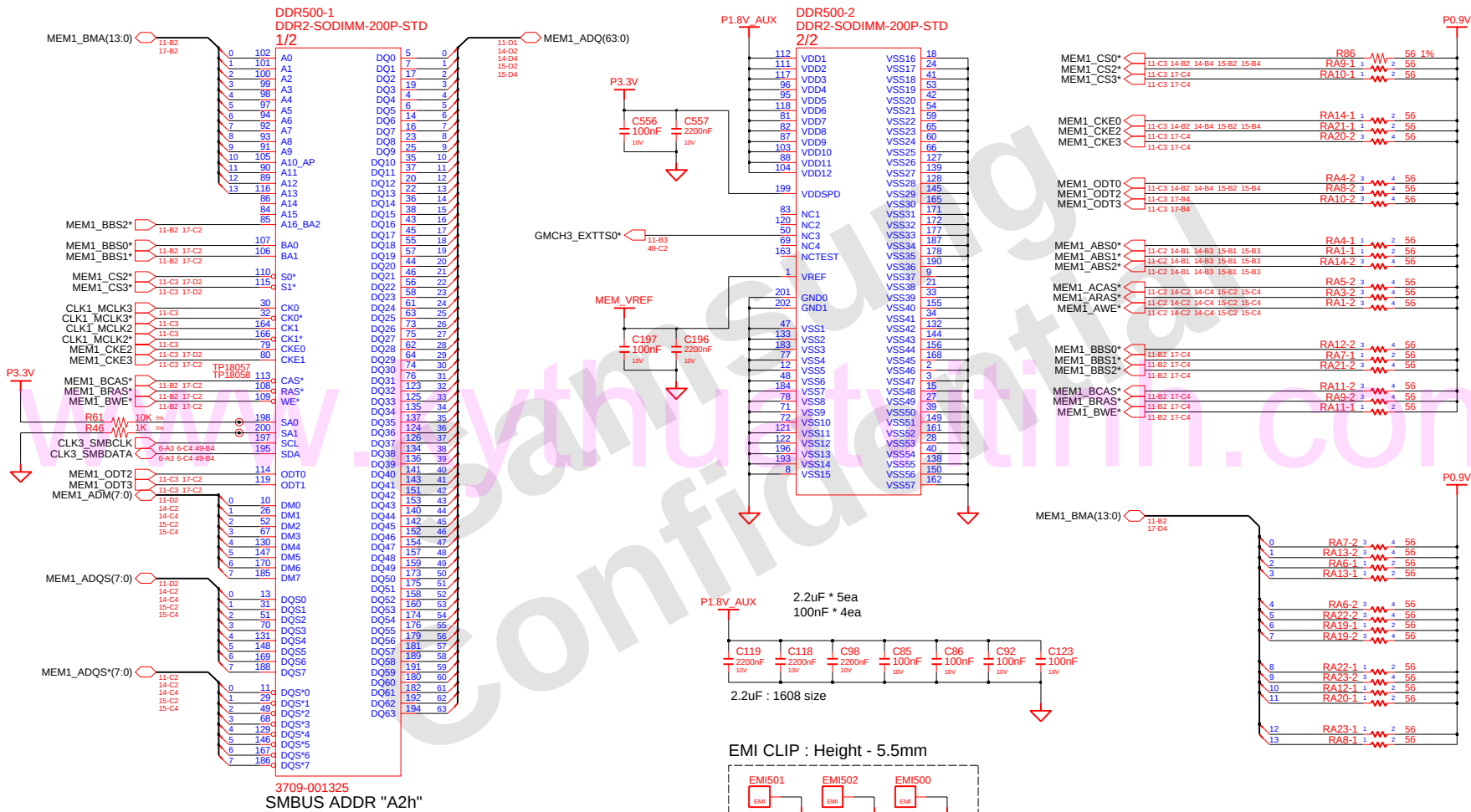
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DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0		DDR2 TERMINATION	PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	16	OF 50

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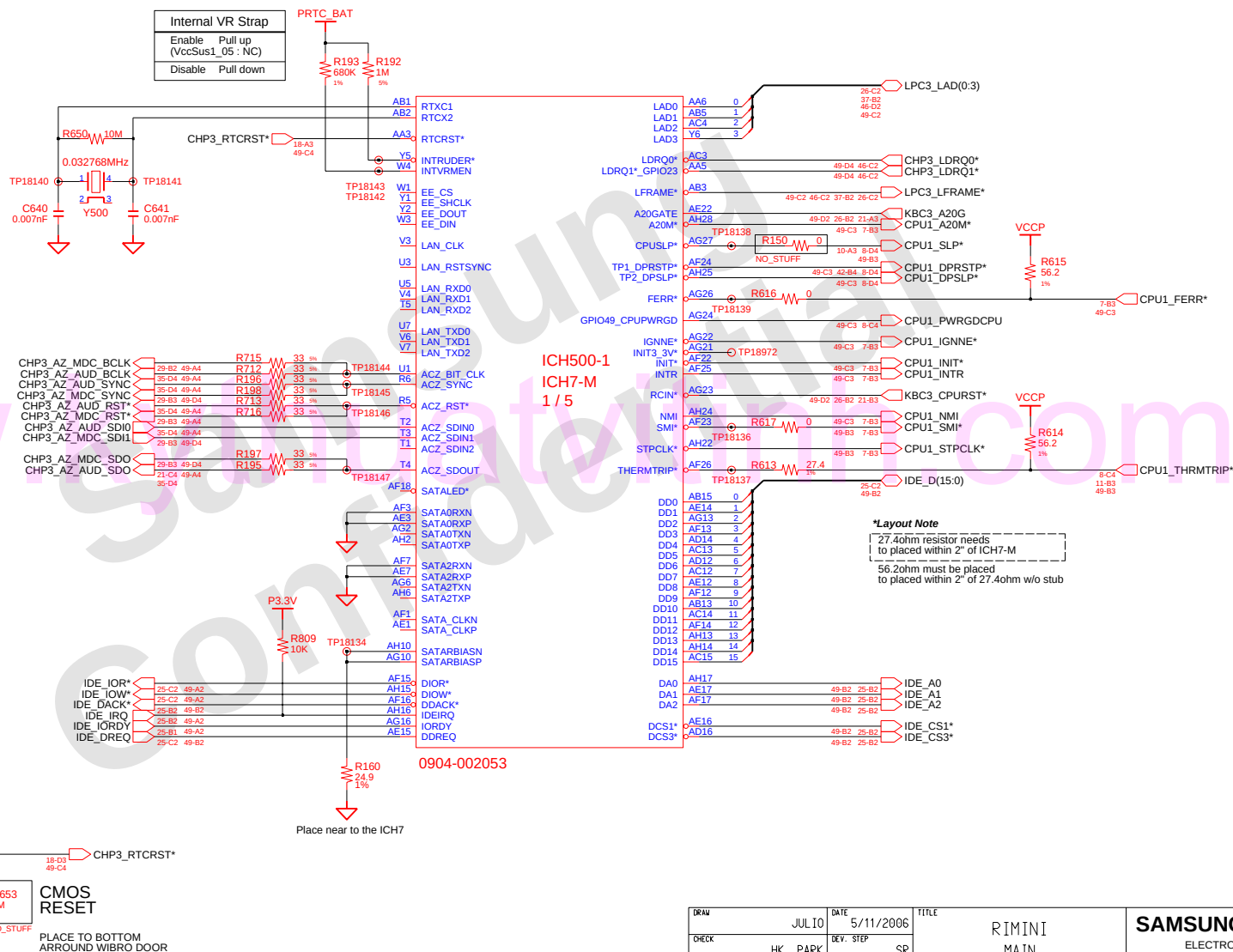
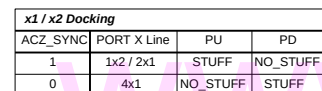
DDR2 Memory Socket



DRAM	JUL10	DATE	5/11/2006	TITLE	RIMINI MAIN DDR2 SODIMM	
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM			

ICH7-M **B0 Stepping : QK65**

Internal VR Strap	
Enable	Pull up (VccSus1_05 : NC)
Disable	Pull down



***Layout Note**

27.4ohm resistor needs
to be placed within 2" of ICH7-M

56.2ohm must be placed
to be placed within 2" of 27.4ohm w/o stub

0904-002053

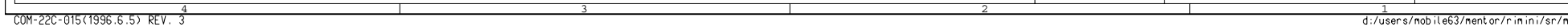
RTC Battery
BA39-00534A
BA39-00598A (New)

CMOS
RESET

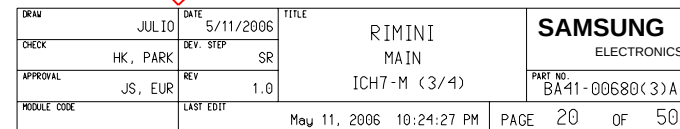
PLACE TO BOTTOM
ARROUND WIBRO DOOR

DATE	JUL10	5/11/2006	TITLE	RIMINI MAIN ICH7-M (1/4)				
CHECK	HK, PARK	DEV. STEP	SR			PART NO.	BA41-00680(3)A	
APPROVAL	JS, EUR	REV	1.0					
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM			PAGE	18 OF 50	

ICH500-3
ICH7-M
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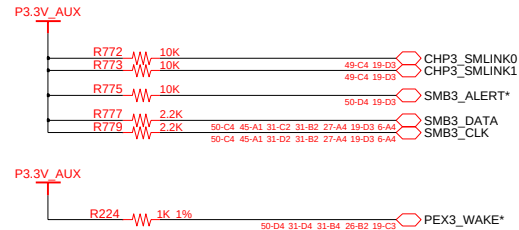
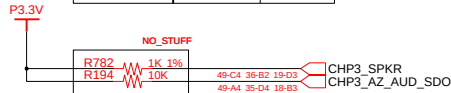
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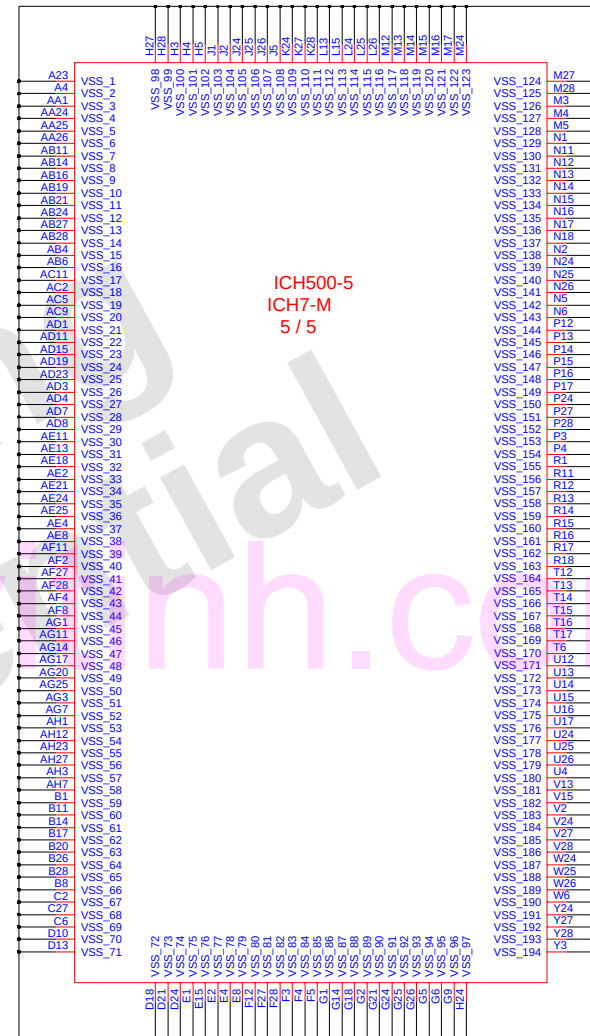
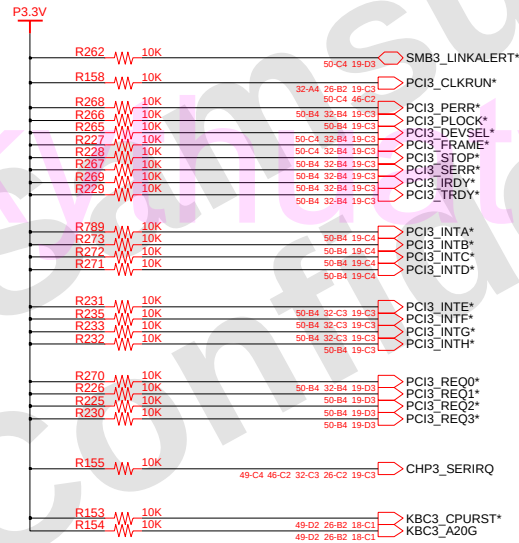
ICH7-M

ICH7-M Options

	Function	Default
CHP3_SPKR AC97_SDOOUT	No Reboot Safe Mode	No Stuff TBD



Wake on PCI-E, OD, Pull-up to ALWAYS power



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR		MAIN	
APPROVAL	JS, EUR	REV	1.0		ICH7-M (4/4)	
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	21 OF 50	

BIOS CODE

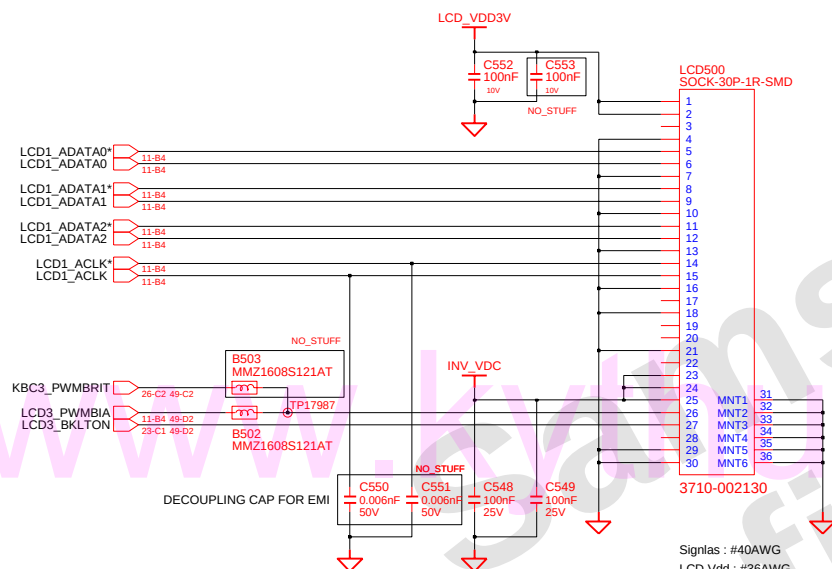
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I2O SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY " PRESS SETUP"	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN BIOS CODE	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	22	OF 50

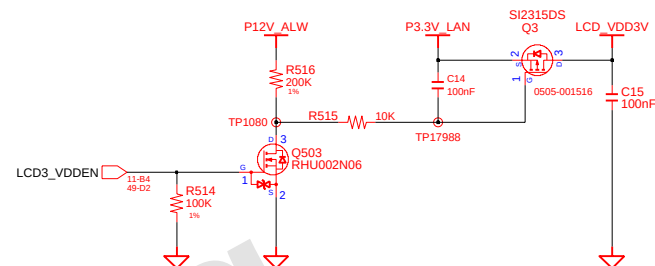
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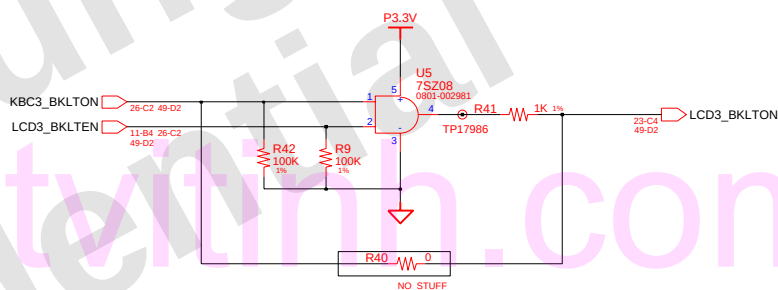
WXGA LCD CONNECTOR



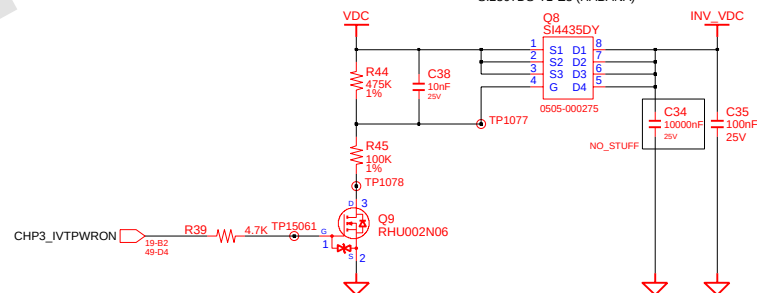
Signals : #40AWG
LCD Vdd : #36AWG
Inverter Vdd : #36AWG
GND : #36AWG



Remove AND Gate : MICOM Control



After DV, check Habana INV_VDC circuit.
SI2307DS-T1-E3 (HABANA)



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN LCD(LVDS) CONN.	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM	PAGE 23 OF 50	

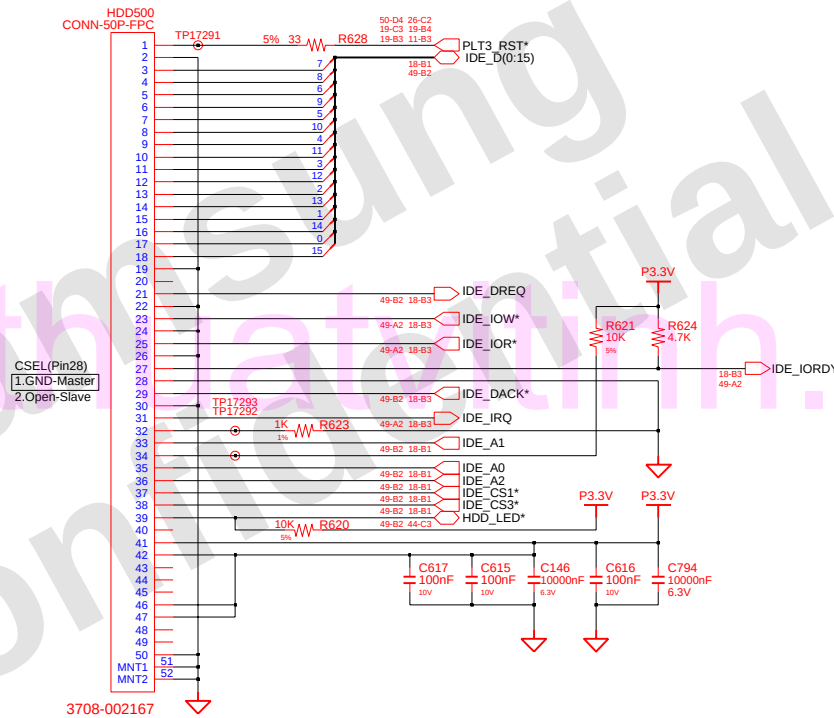
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DATE	JUL 10	5/11/2006	TITLE		RIMINI MAIN CRT CONN.			
CHECK	HK, PARK	SR						
APPROVAL	JS, EUR	REV 1.0						
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Main to HDD (Locking Type)

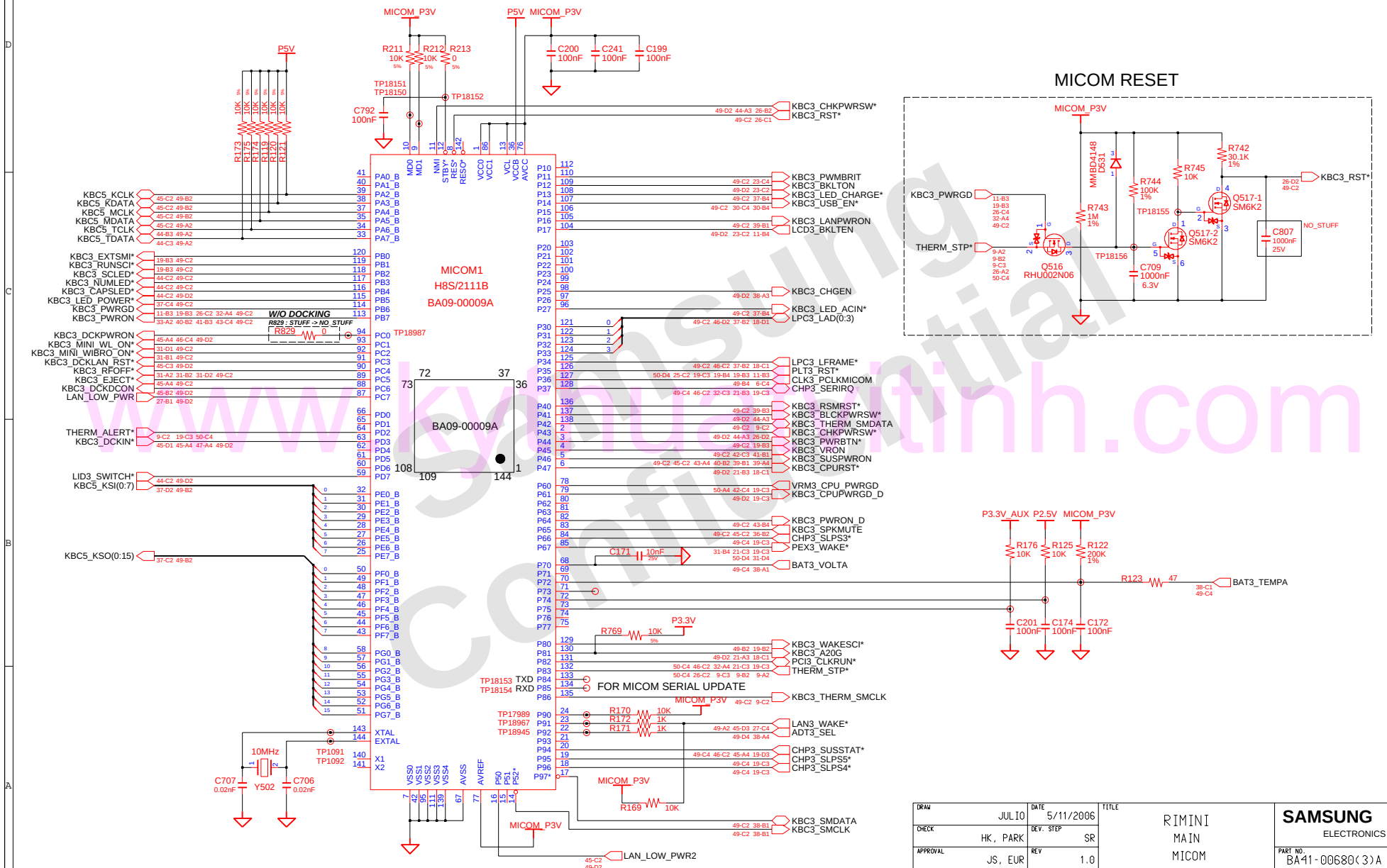
IDE Pin Assignment			
1.8 SFF HDD		Main Board	
SIGNALS	No.	No.	SIGNALS
RESERVED	1	-	N.C
RESERVED	2	-	N.C
RESET	3	1	RESET
GROUND	4	2	GROUND
DD7	5	3	DD7
DD8	6	4	DD8
DD6	7	5	DD6
DD9	8	6	DD9
DD5	9	7	DD5
DD10	10	8	DD10
DD4	11	9	DD4
DD11	12	10	DD11
DD3	13	11	DD3
DD12	14	12	DD12
DD2	15	13	DD2
DD13	16	14	DD13
DD1	17	15	DD1
DD14	18	16	DD14
DD0	19	17	DD0
DD15	20	18	DD15
GROUND	21	19	GROUND
DMARQ	22	21	IDE_DREQ
GROUND	23	22	GROUND
D1OW	24	23	D1OW
D1OR	25	25	D1OR
GROUND	26	26	GROUND
IORDY	27	27	IDE_IORDY
GROUND	28	28	GROUND (CSEL)
DMACK	29	29	IDE_DACK
INTRQ	30	31	IDE_IRQ
DA1	31	33	IDE_A1
PDIAG	32	34	PDIAG (Pull-Up)
DA0	33	35	IDE_A0
DA2	34	36	IDE_A2
CS0	35	37	IDE_CS1
CS1	36	38	IDE_CS3
DASP	37	39	IDE_LED
+3.3V	38	41,42	+3.3V
+3.3V	39	46,47	+3.3V
Reserved (Toshiba) DevAdri(HGST) - 0(open): Master - 1(PullUp): Slave	40	-	N.C



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MICOM P3V

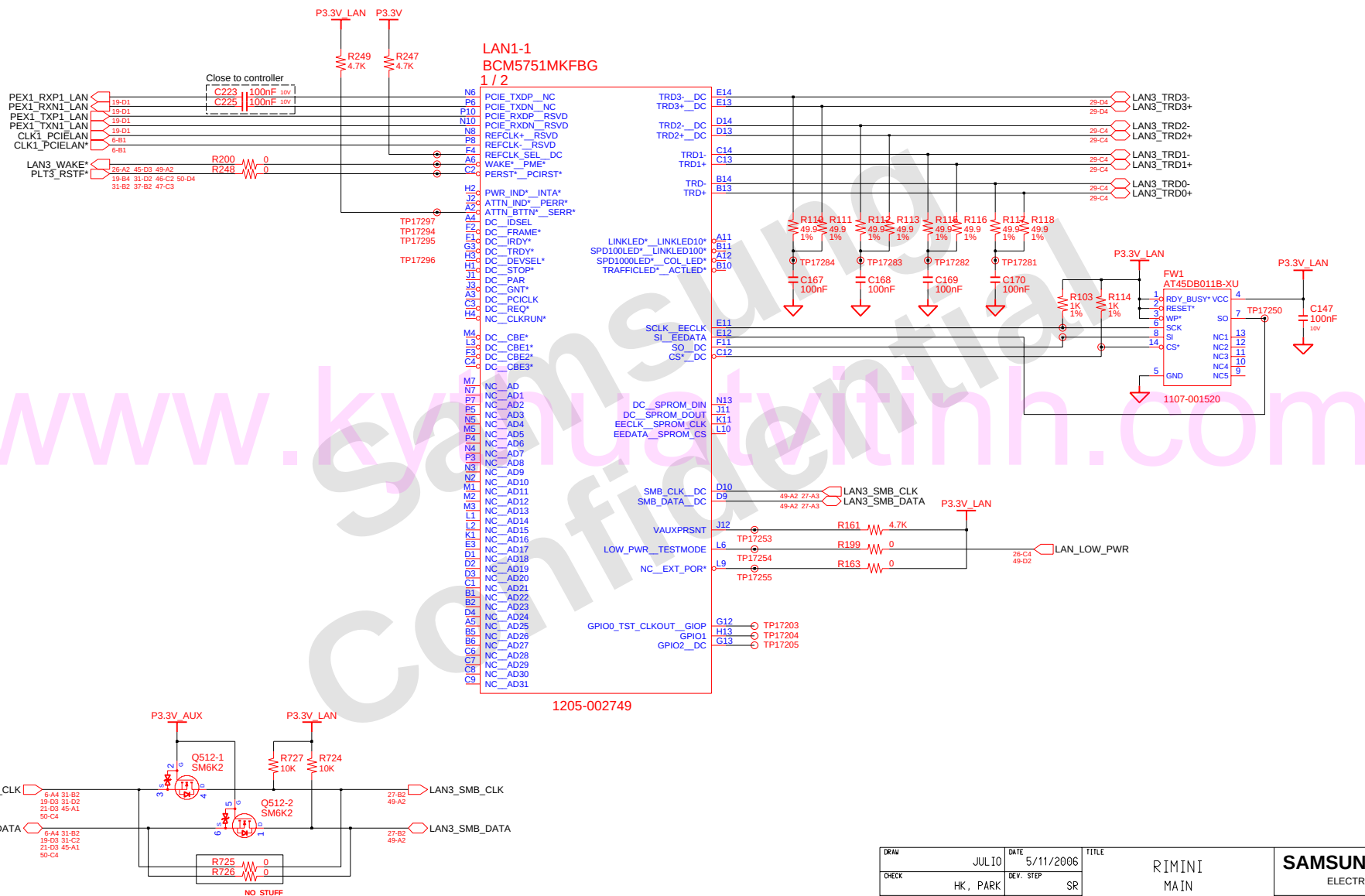
P5V MICOM P3V



DATE	JULIO	5/11/2006	TITLE	RIMINI		SAMSUNG	
CHECK	HK, PARK	DEV. STEP	SR	MAIN		ELECTRONICS	
APPROVAL	JS, EUR	REV	1.0	MICON		PART NO. BA41-00680(3)A	
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM		PAGE	26	OF 50

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LAN1-1
BCM5751MKFBG
1 / 2

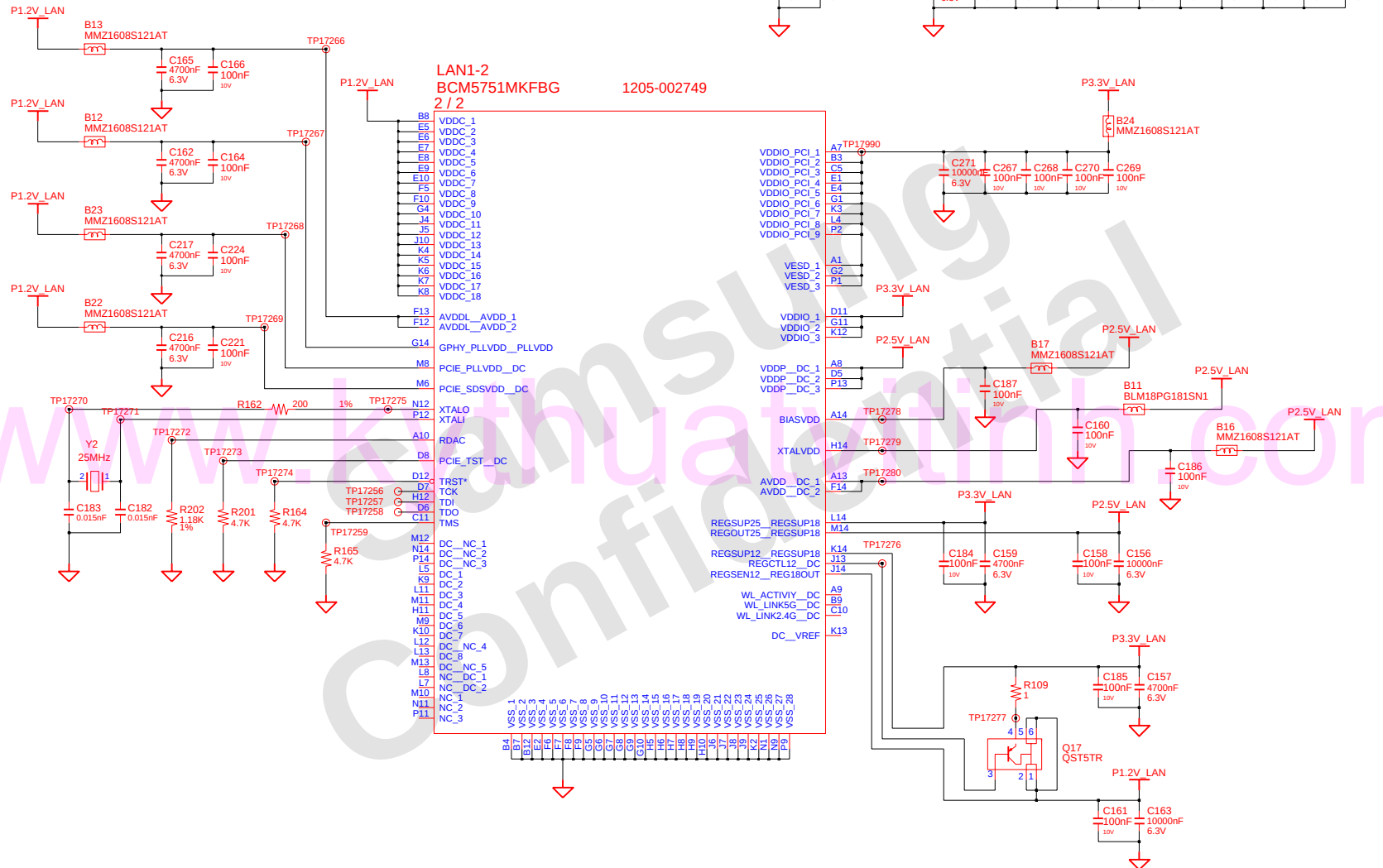


DATE	JUL 10	5/11/2006	TITLE	RIMINI MAIN LAN CONTROLLER (1/2)		SAMSUNG ELECTRONICS	
CHECK	HK, PARK	DEV. STEP	SR			PART NO.	BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0				
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM			PAGE	27 OF 50

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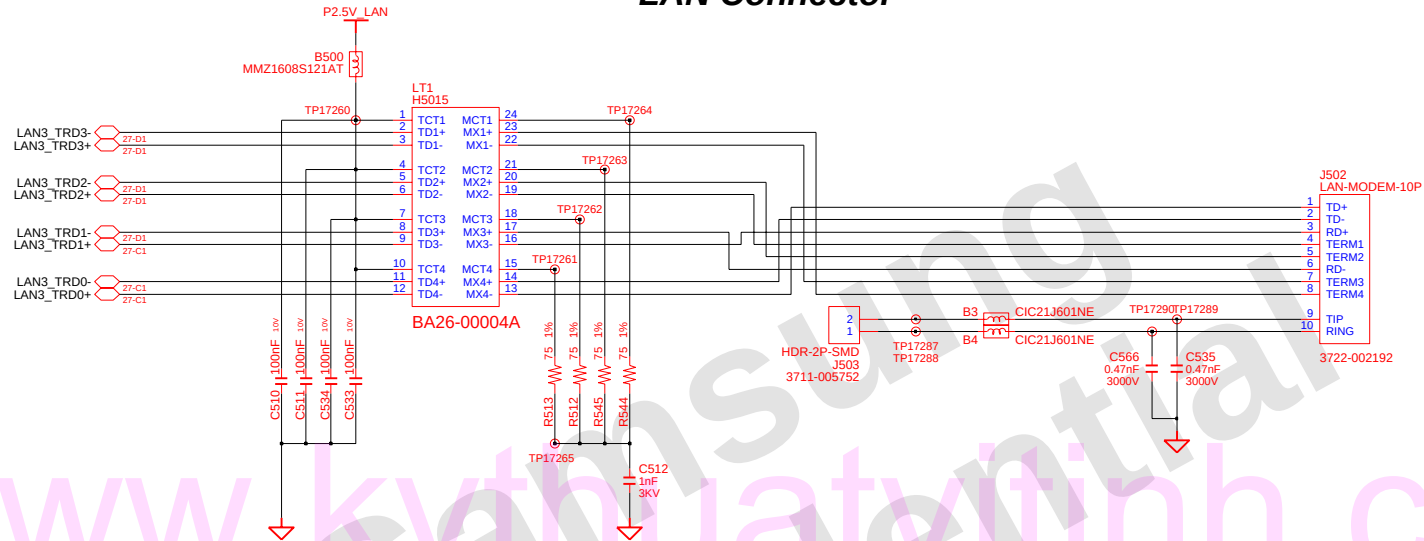
LAN Controller



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN LAN CONTROLLER (2/2)	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	28	OF 50

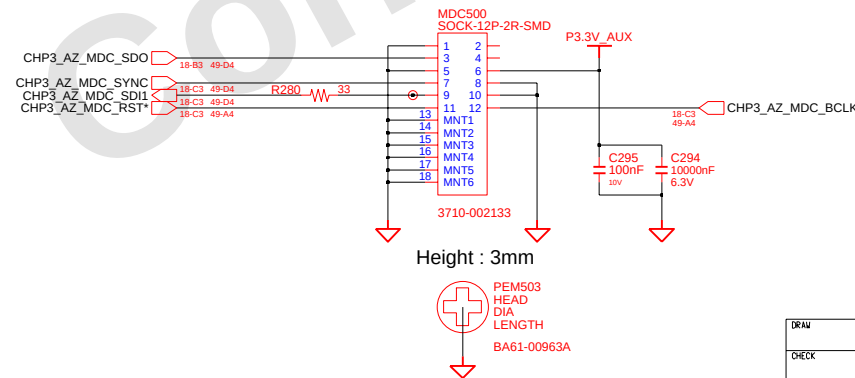
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LAN Connector



MDC Connector

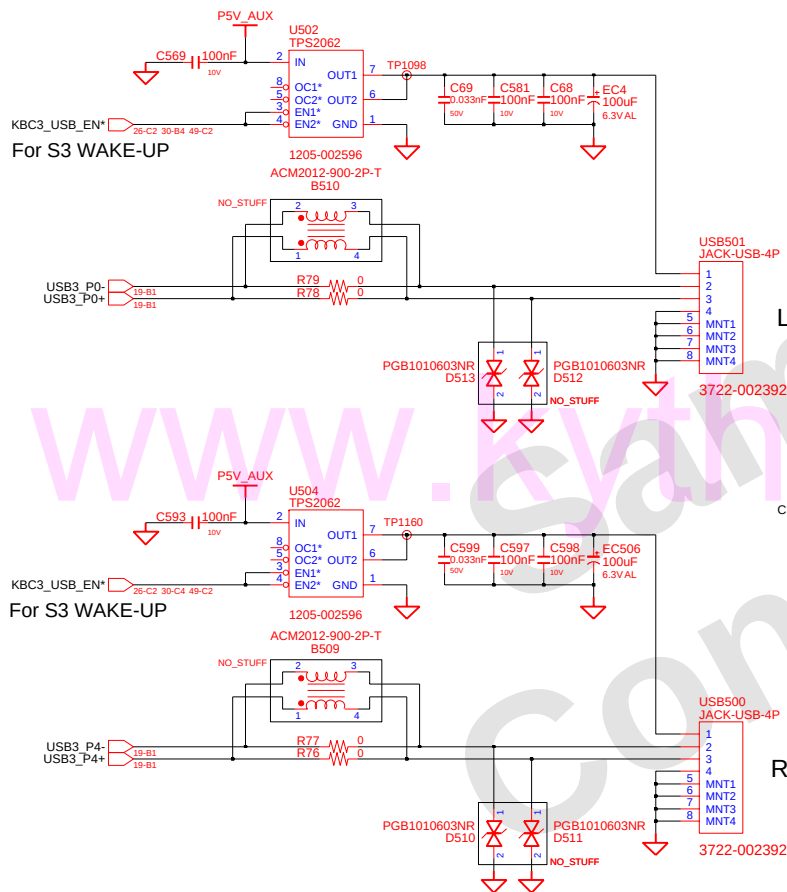
MDC Module : BA59-01272A



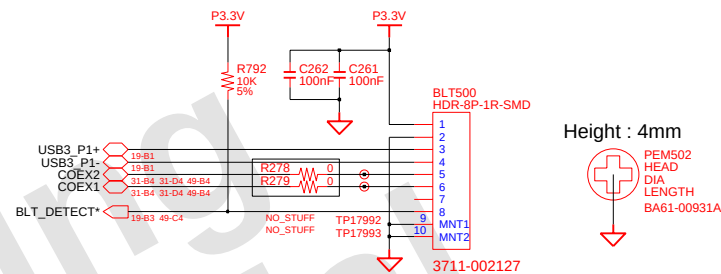
DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN MDC & COMBO JACK	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	29	OF 50

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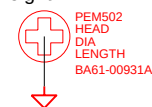
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USB Port**BLUETOOTH**

INTEL F/W : PIN5-COEX2
BROADCOM F/W : PIN7-COEX2

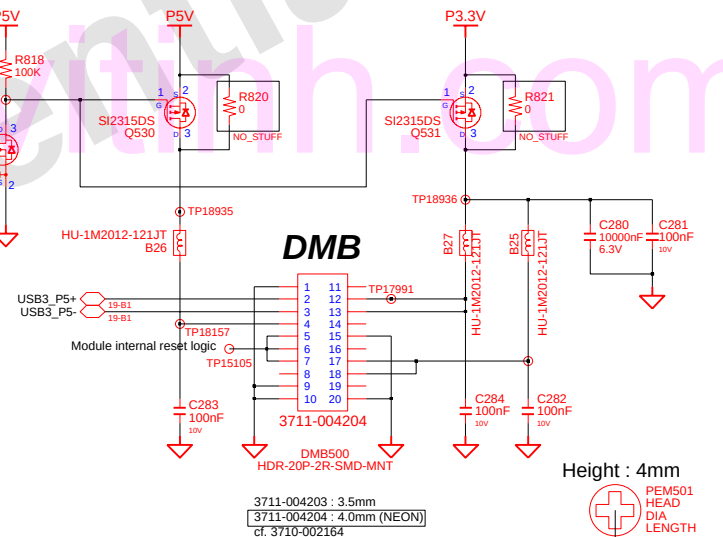


Height : 4mm



LEFT

RIGHT

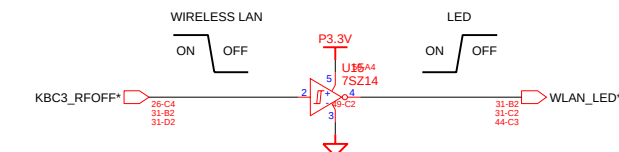
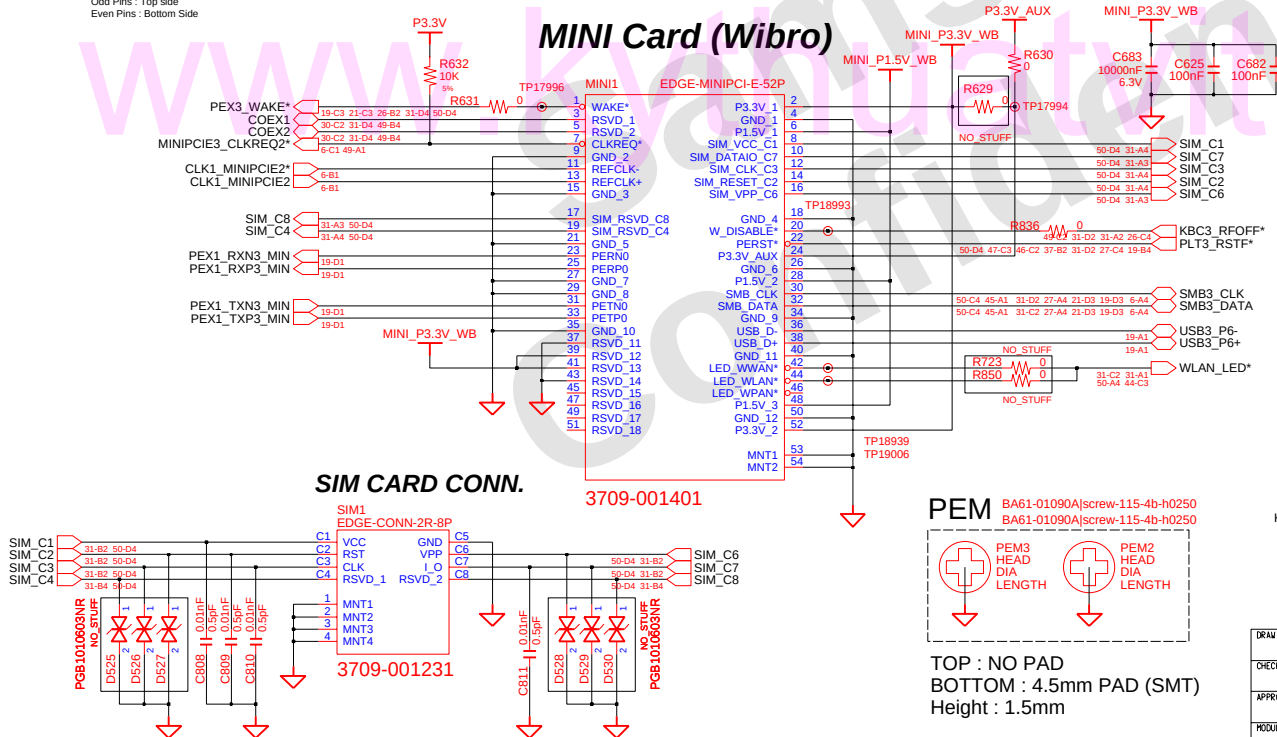
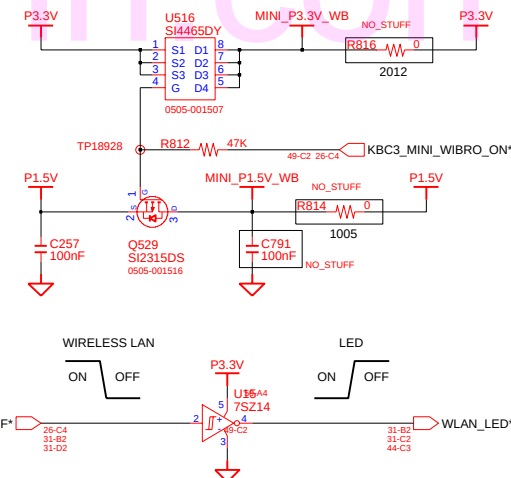
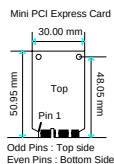
DMB

Height : 4mm



DMB Module : BA59-01869A

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0	USB, DMB & BLUETOOTH		PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	30	OF 50

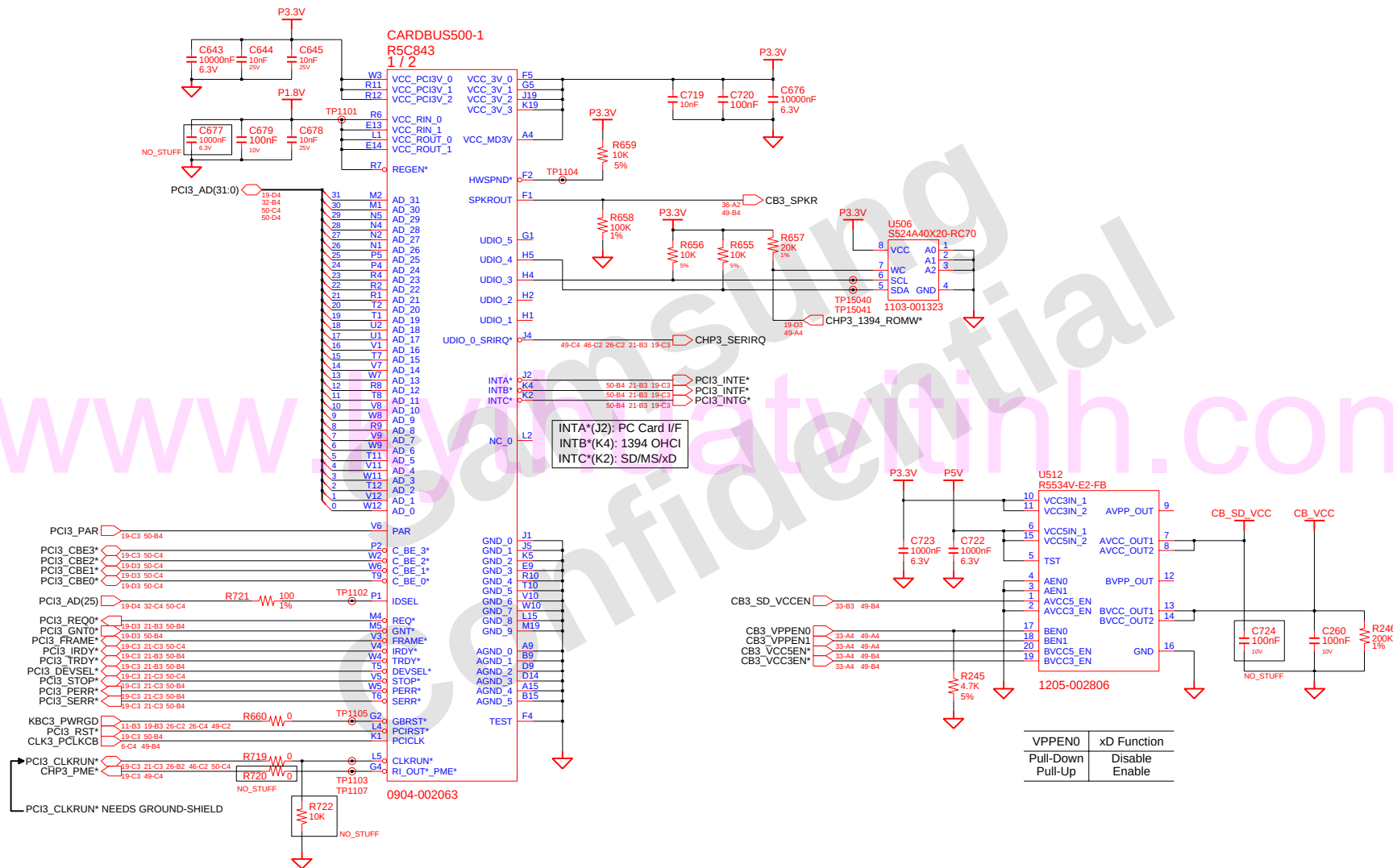


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN MINI CARD (GOLAN,WIBRO)	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE	LAST EDIT					
				May 11, 2006 10:24:27 PM	PAGE	31 OF 50

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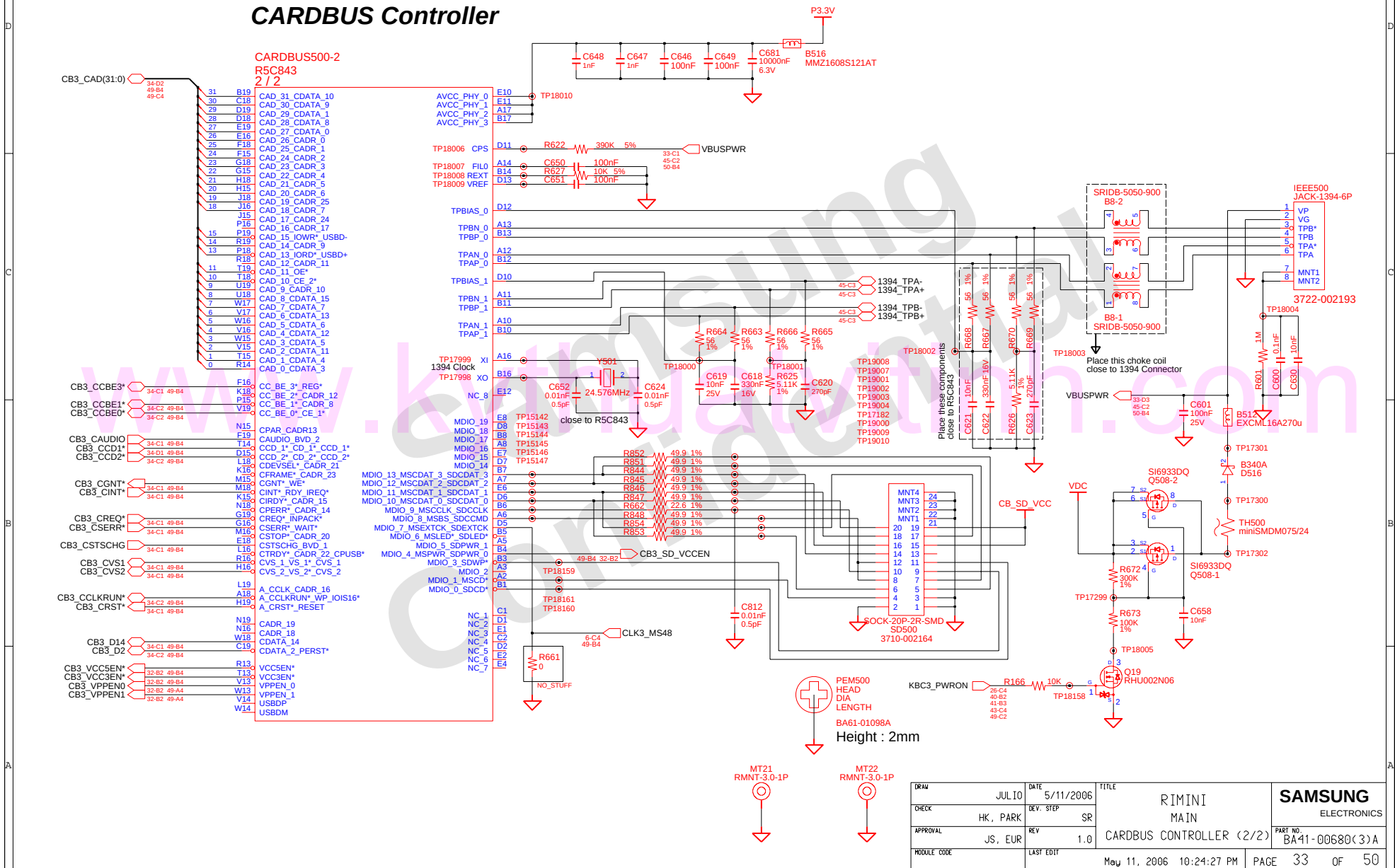
CARDBUS Controller



VPPEN0	xD Function
Pull-Down	Disable
Pull-Up	Enable

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG
CHECK	HK, PARK	DEV. STEP	SR	MAIN	MAIN	ELECTRONICS
APPROVAL	JS, EUR	REV	1.0	CARDBUS CONTROLLER (1/2)	PART NO.	BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	32	OF 50

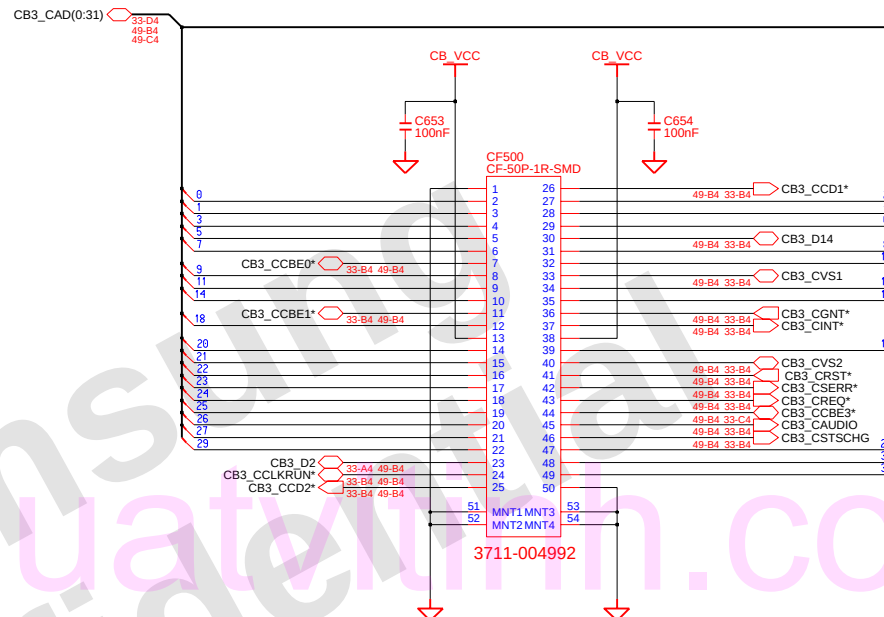
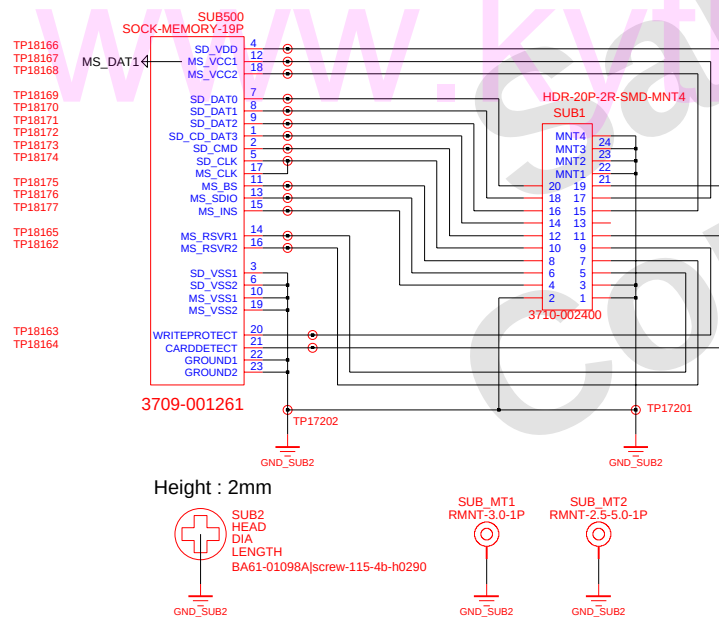
CARDBUS Controller



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CF CARD

3in1 Sub Board



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	MAIN		
APPROVAL	JS, EUR	REV	1.0	CF CARD & 3IN1 SUB B'D	PART NO.	BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	34	OF 50

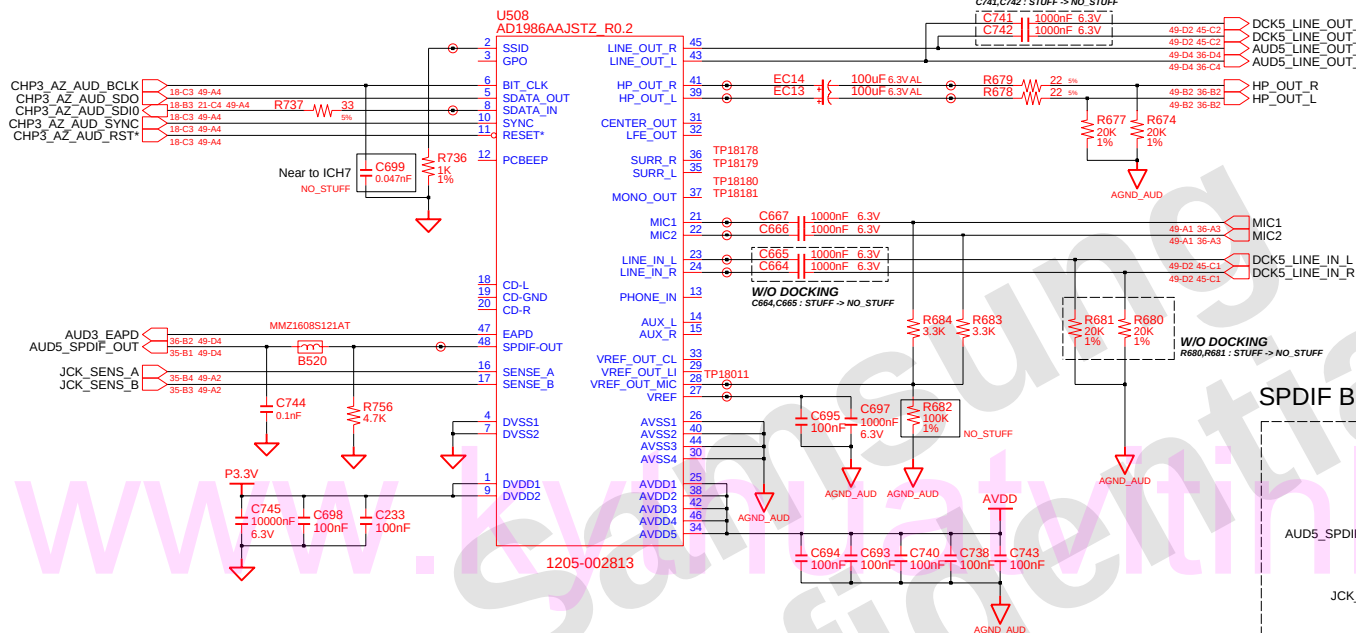
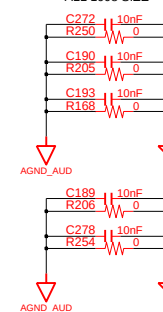
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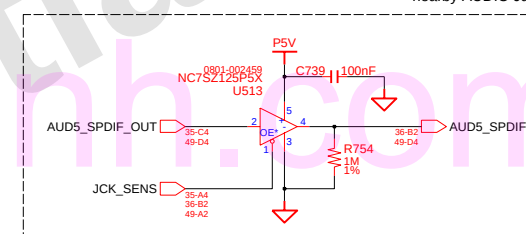
AUDIO CODEC

1.AGND_AUD	Audio Ground
2.GND	Digital Ground

ALL 1608 SIZE



SPDIF BUFFER

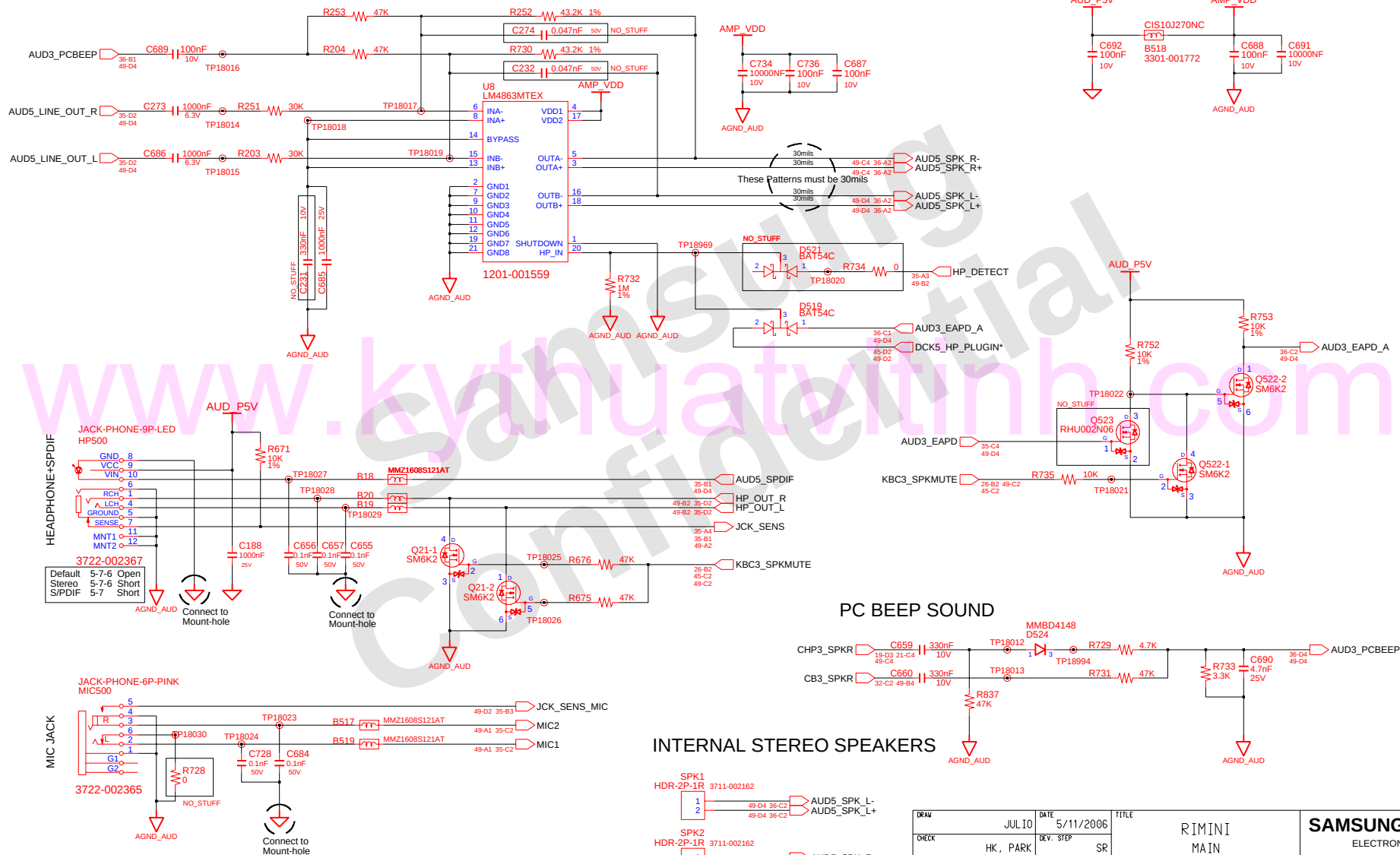


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AUDIO AMP

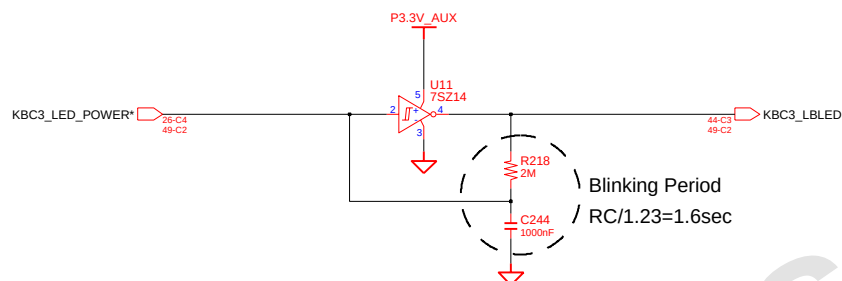
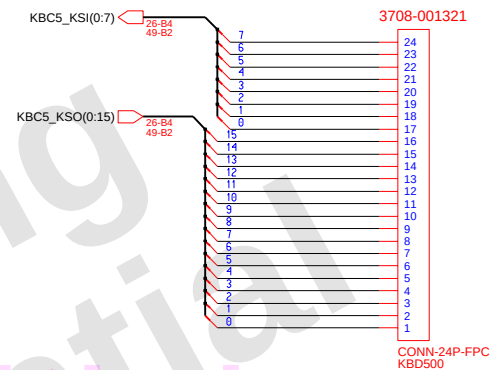
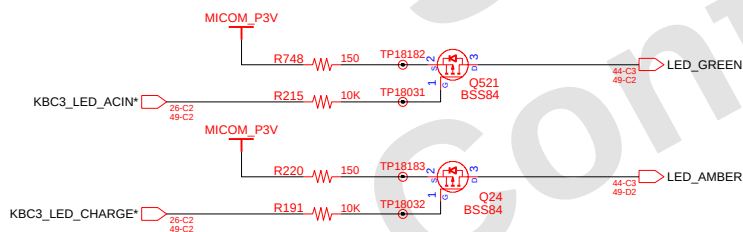
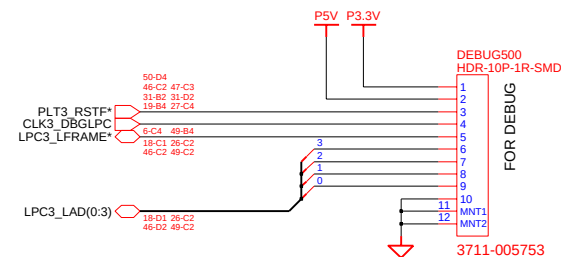
AMP_VDD



DATE	JULIO	5/11/2006	TITLE	RIMINI MAIN AUDIO AMP & JACK	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR		PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0		
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	36 OF 50

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POWER_ON / LB LED**KEYBOARD****ADAPTERIN/CHARGING LED****DEBUG PORT**

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN KBD CONN & DEBUG	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	37 OF 50	

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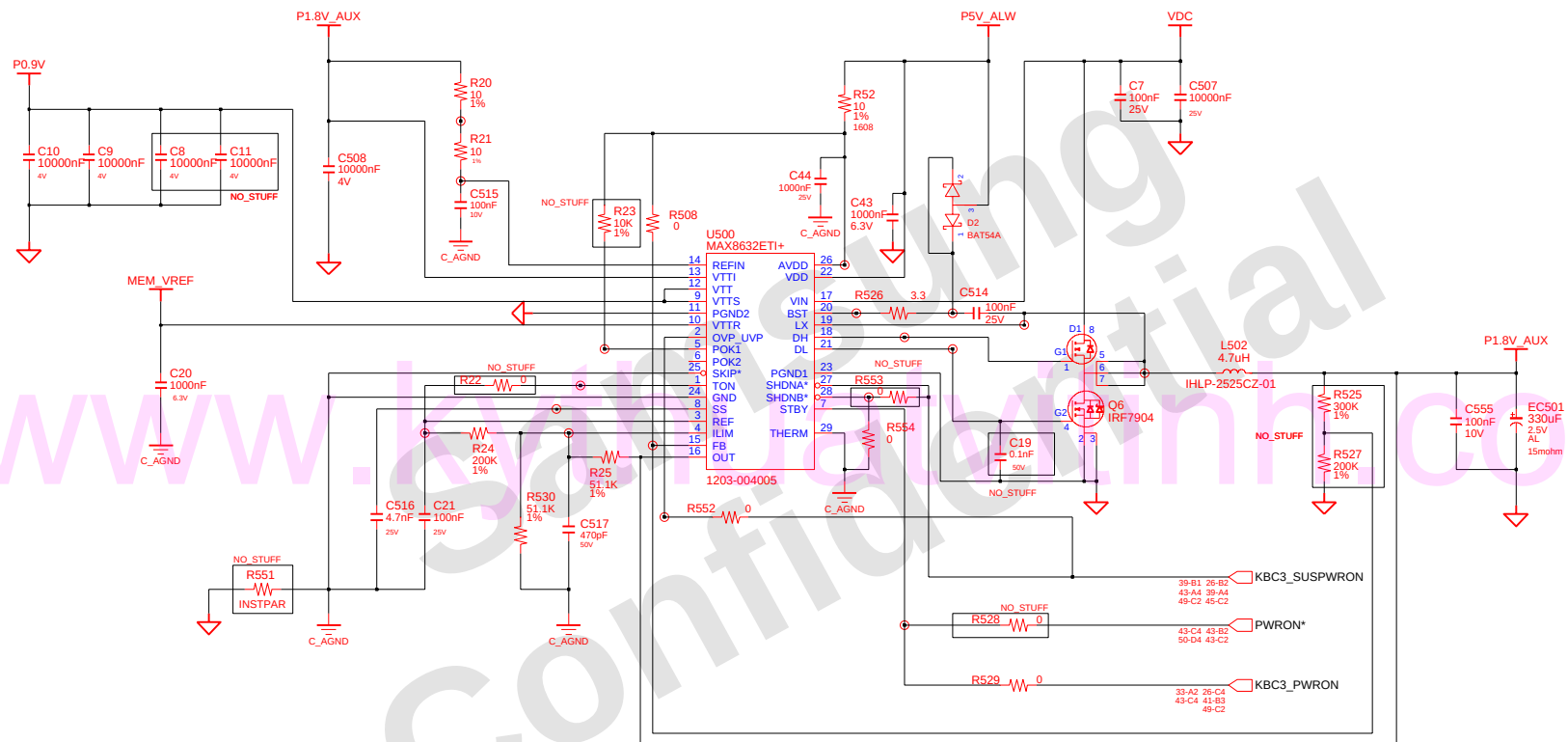
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CHECK	HK, PARK	DEV. STEP							SR
APPROVAL	JS, EUR	REV							1.0
MODULE CODE			LAST EDIT		May 11, 2006 10:24:27 PM		PAGE	38 OF 50	

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DRAW		JUL 10		DATE		5/11/2006		TITLE		RIMINI		SAMSUNG	
CHECK		HK, PARK		DEV. STEP		SR		MAIN				ELECTRONICS	
APPROVAL		JS, EUR		REV		1.0		P5V-AUX & P3.3V-LAN		PART NO.		BA41-00680(3)A	
MODULE CODE				LAST EDIT				May 11, 2006 10:24:27 PM		PAGE		39 OF 50	

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DDR2 POWER

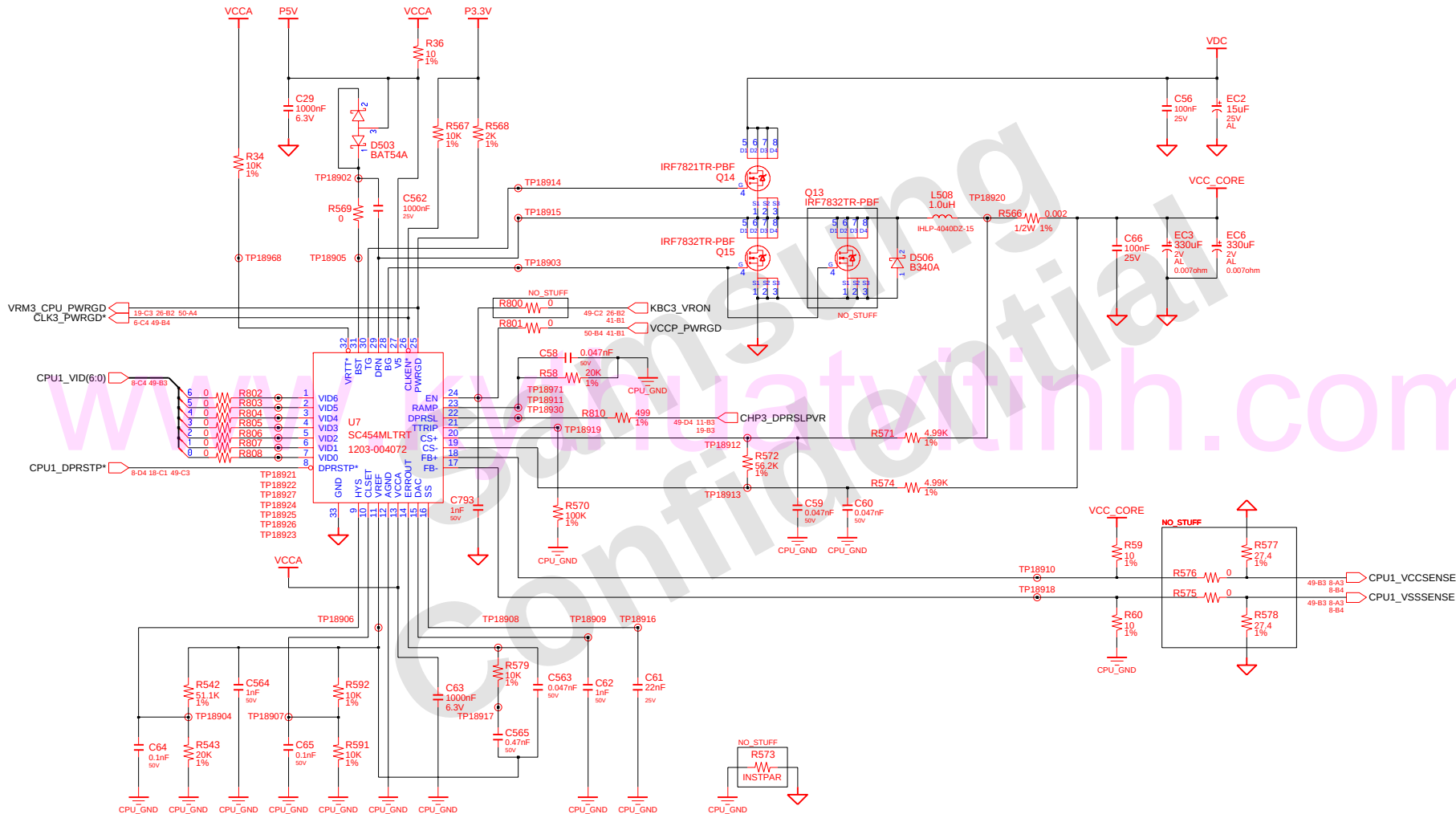
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CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	40	OF 50

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DATE	JUL10	5/11/2006	TITLE RIMINI MAIN P1.5V & VCCP		SAMSUNG ELECTRONICS		
CHECK	HK, PARK	DEV. STEP					SR
APPROVAL	JS, EUR	REV					1.0
MODULE CODE			LAST EDIT		PART NO. BA41-00680(3)A		
			May 11, 2006 10:24:27 PM		PAGE	41 OF 50	

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CPU VRM POWER

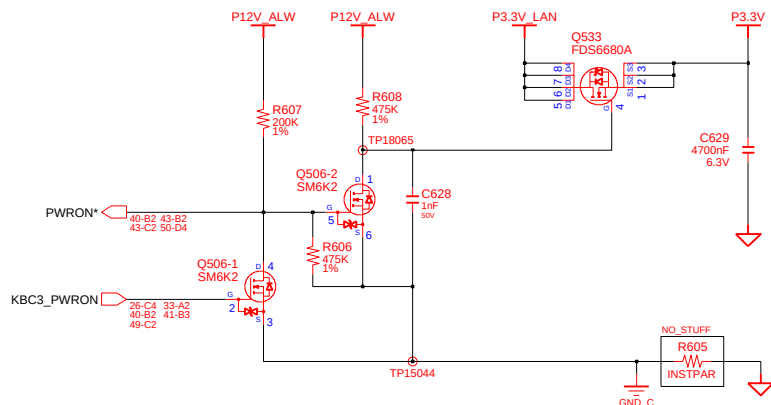


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN VCC_CORE	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM			
			PART NO.		BA41-00680(3)A	

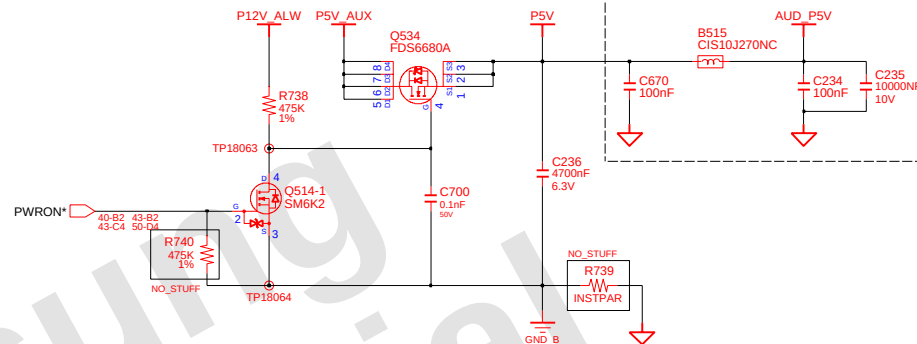
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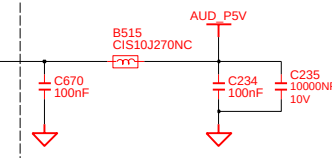
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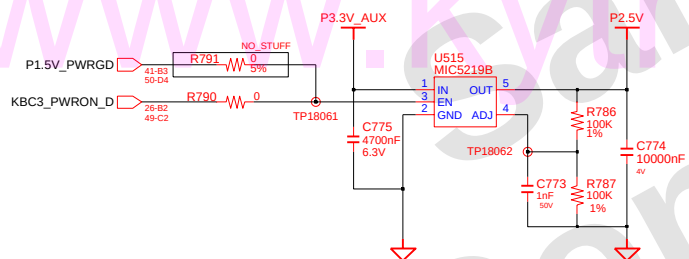
Switched Power On (P5V)



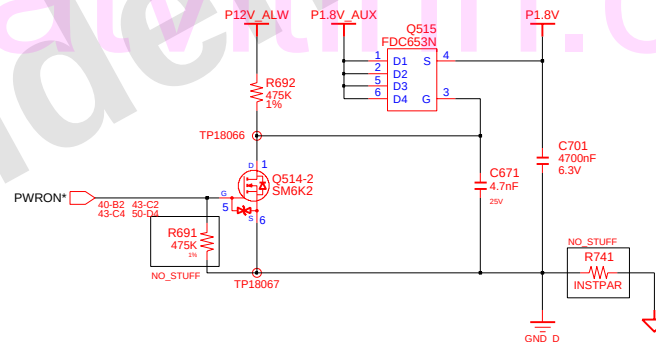
AUDIO_POWER



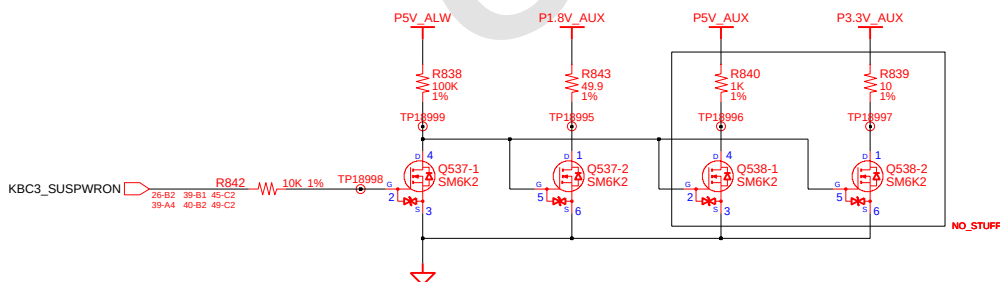
Switched Power On (P2.5V)



Switched Power On (P1.8V)



Discharge Circuit

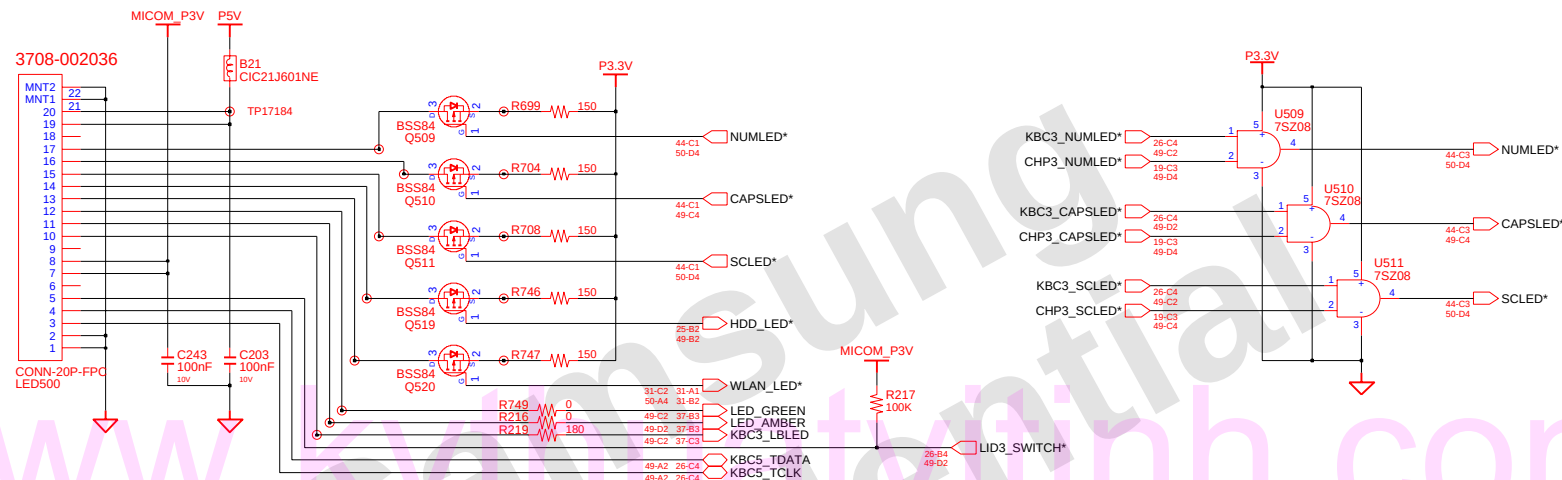


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	43	OF 50

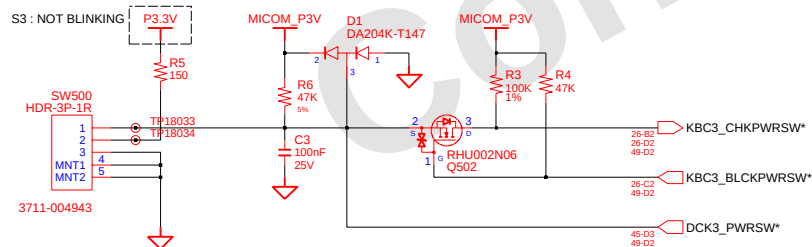
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LED & T/P FPC Conn.



Power Switch Connector



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0	LED, TP CONN & POWER SW		PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	44	OF 50

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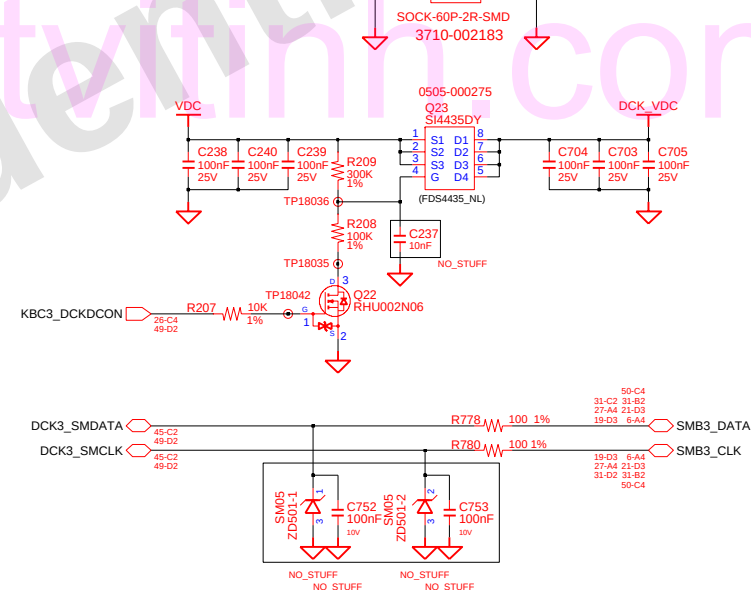
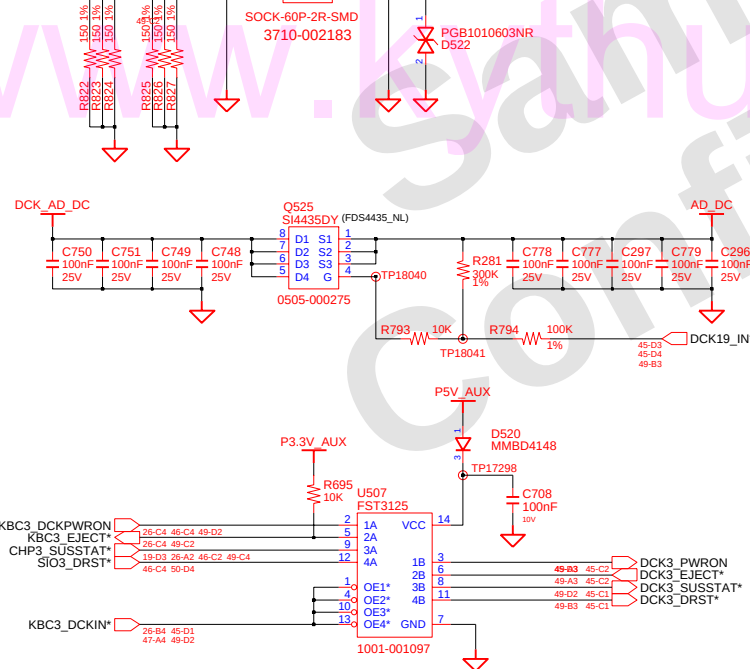
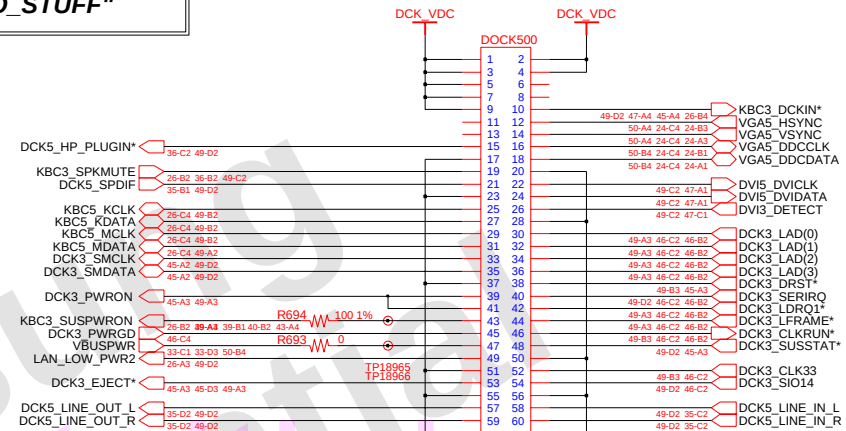
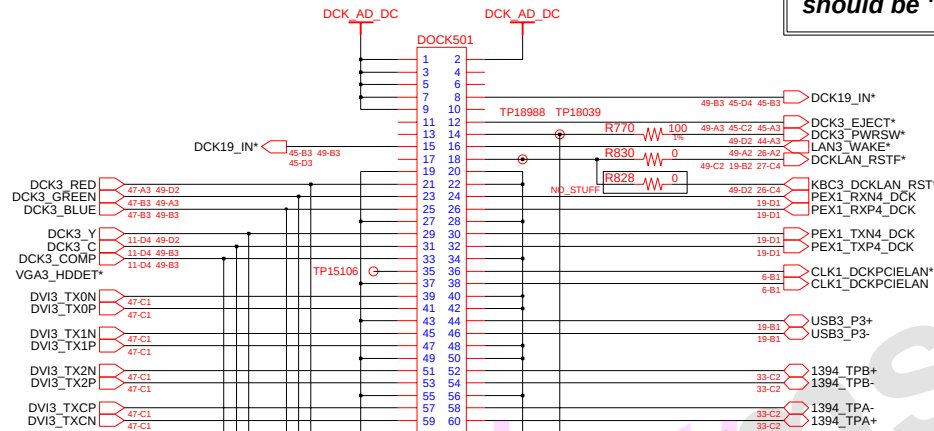
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DOCKING CONNECTOR (124PIN)

In "Without Docking Model"
 all components of this page
 should be "NO_STUFF"

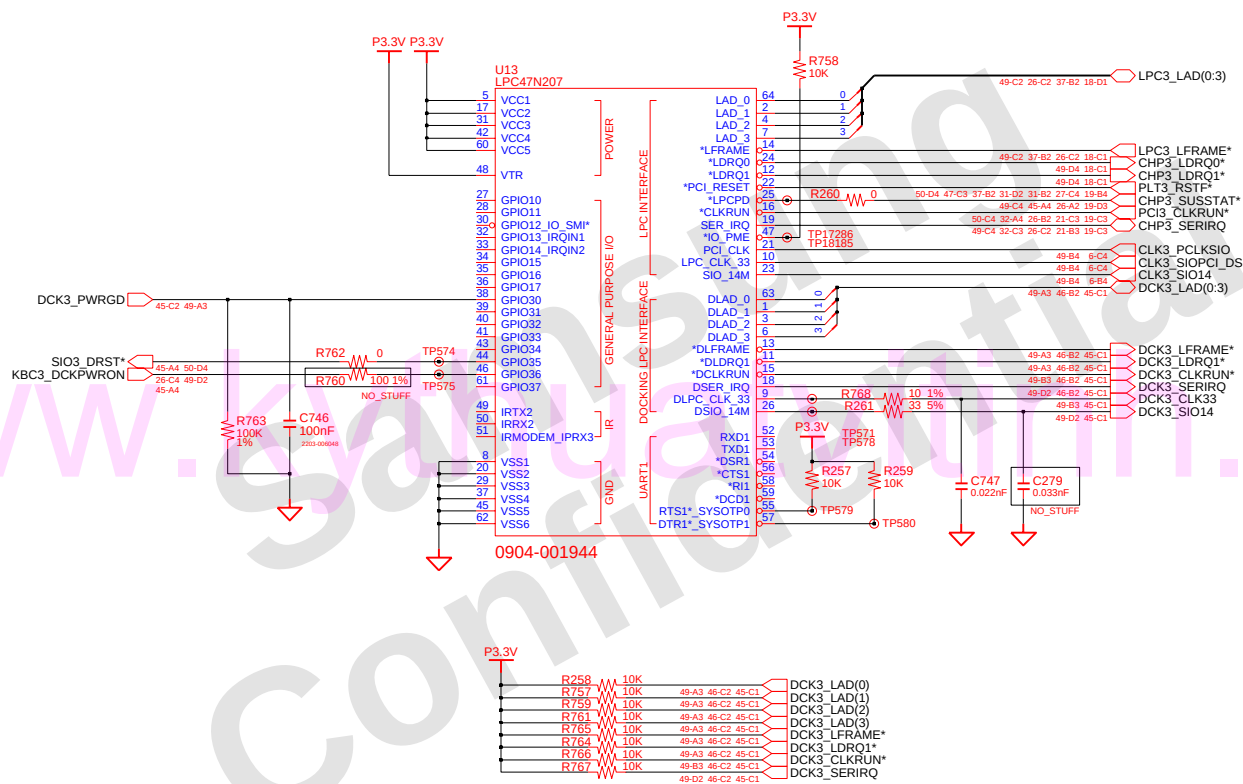
Docking Placement

PWR1	1	119	PWR4
Top View			
PWR3	2	120	PWR2



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN DOCKING CONN.	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			PART NO. BA11-00680(3)A
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	45	OF 50

***In "Without Docking Model"
all components of this page
should be "NO STUFF"***



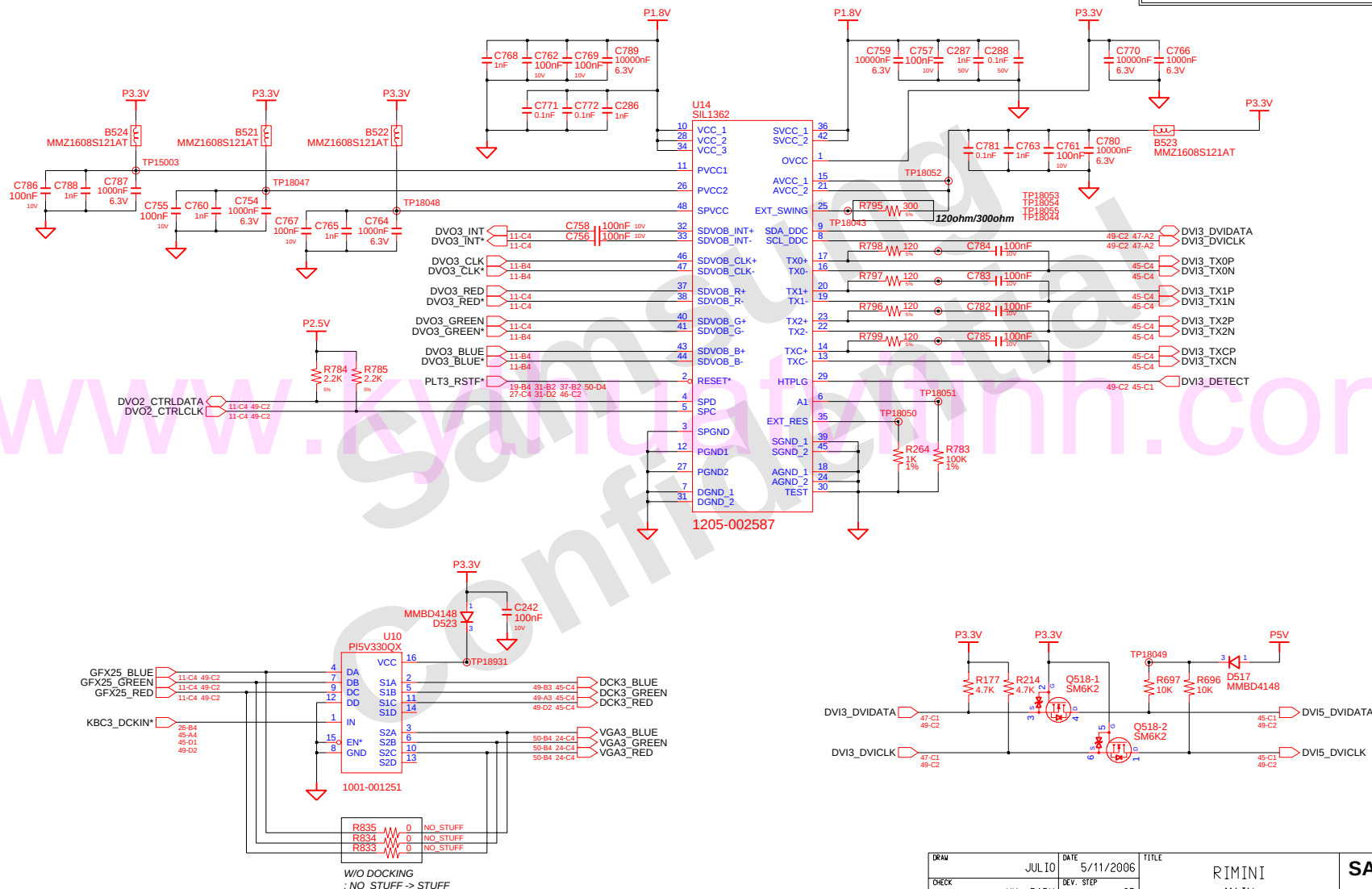
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CHECK	HK, PARK	DEV. STEP	SR						
APPROVAL	JS, EUR	REV	1.0						
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM		PAGE	46	OF	50

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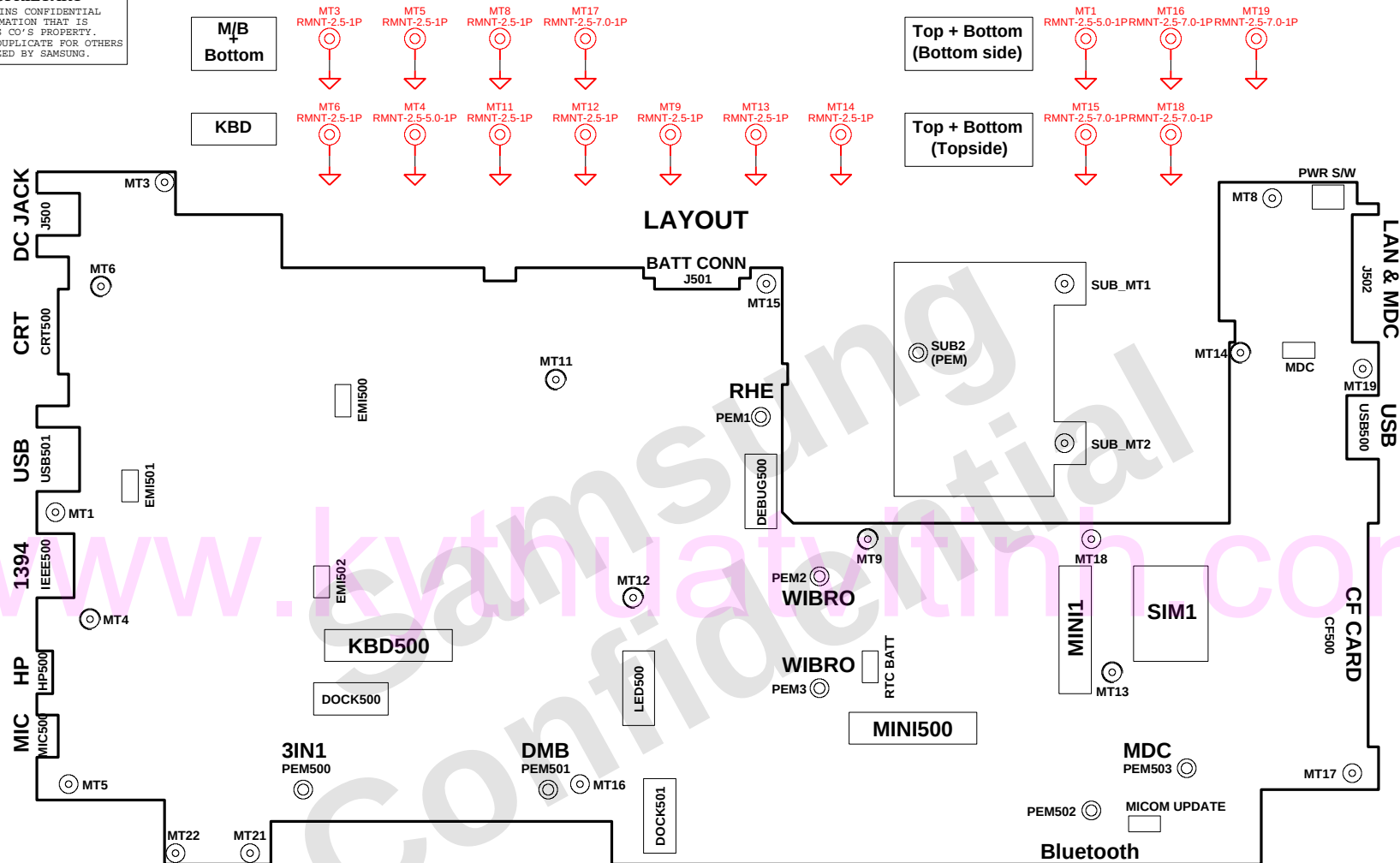
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DOCKING DVI

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all components of this page
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(Except R833, R834, R835)



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PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV500

1○

2○ ○3

TP18982 TP18983 TP18984 TP18985

C800 0.1nF C803 0.015nF C797 0.033nF C806 0.047nF

TP18986

NO_STUFF NO_STUFF NO_STUFF
NO_STUFF NO_STUFF NO_STUFF

DRAW		DATE		TITLE		SAMSUNG	
JULIO		5/11/2006		RIMINI		ELECTRONICS	
CHECK		REV. STEP		MAIN		PART NO.	
HK, PARK		SR		MOUNT HOLE		BA11-00680(3)A	
APPROVAL		REV					
JS, EUR		1.0					
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM		PAGE 48 OF 50	

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PT18237<AUD.3.APD
PT18238<AUD.3.CPBD
PT18239<AUD.5.SPD<OUT_L
PT18240<AUD.5.SPD<OUT_R
PT18241<AUD.5.SPD
PT18242<AUD.5.SPD<F.L
PT18243<AUD.5.SPD<L.L
PT18244<AUD.5.SPD<R.L
PT18245<AUD.5.SPD<R
PT18246<AUD.5.SPD<R-
PT18247<BA1.3.TEMPA
PT18248<BA1.3.TEMPB
PT18249<BL.1.7E.TC1
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PT18292<CR3.CCSTGCH
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PT18295<CR3.CVST3
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PT18299<CR3.VCC3EN*
PT18300<CR3.VCC4EN*
PT18301<CR3.VPPENO
PT18302<CR3.VPPENT
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PT18308<CHP.3.AZ.AUD.SYN
PT18309<CHP.3.AZ.AUD.SYN
PT18310<CHP.3.AZ.MDC.RST

TP183110 CHP3_4Z_MDC_SD11
TP183120 CHP3_AZ_MDC_SDO
TP183130 CHP3_AZ_MDC_SYNC
TP183140 CHP3_BIOS_TBL_*
TP183150 CHP3_BIOS_WP*
TP183160 CHP3_CAPS_LED_*
TP183170 CHP3_CPU_STP*
TP183180 CHP3_CPU_TEMP*
TP183190 CHP3_DPRS_LPVR
TP183190 CHP3_IVTP_WRON
TP183200 CHP3_LDR00_*
TP183210 CHP3_LDR01_*
TP183220 CHP3_NUMLED_*
TP183230 CHP3_PC1STP*
TP183240 CHP3_PC2STP*
TP183250 CHP3_PC1_TCRST_*
TP183260 CHP3_SLED_*
TP183270 CHP3_SERIRQ
TP183280 CHP3_SLP_S3*
TP183290 CHP3_SLP_S4*
TP183300 CHP3_SLP_S5*
TP183310 CHP3_SML_INKO
TP183320 CHP3_SML_INK1
TP183330 CHP3_SML_INK2
TP183340 CHP3_SUS_STAT*

TP18335 CLK3_DBLGPC
TP18336 CLK3_ICH14
TP18337 CLK3_MS48
TP18338 CLK3_PCLKCB

TP18340 CLK3_PCLKIC
TP18341 CLK3_PCLKMI
TP18342 CLK3_PCLKSI
TP18343 CLK3_PWRGD
TP18344 CLK3_SIO14
TP18345 CLK3_SIOPCI
TP18346 CLK3_SMBCLK
TP18347 CLK3_SMBDAT
TP18348 CLK3_USB48
TP18349 COEX1
TP18350 COEX2

TP18340 ○ CLK3_PCLKICH
TP18341 ○ CLK3_PCLKMIC0
TP18342 ○ CLK3_PCLKSI0
TP18343 ○ CLK3_PWRGD+
TP18344 ○ CLK3_SIO14
TP18345 ○ CLK3_SIOPC1_DS
TP18346 ○ CLK3_SMBCLK
TP18347 ○ CLK3_SMBDATA
TP18348 ○ CLK3_USB48
TP18349 ○ COEX1
TP18350 ○ COEX2

TP18351 CPU1_A20M*
TP18352 CPU1_ADS*

TP18353 CPU1_BNR*
TP18354 CPU1_BPR1*
TP18355 CPU1_BREQ*
TP18356 CPU1_BSEL0
TP18357 CPU1_BSEL1
TP18358 CPU1_BSEL2
TP18359 CPU1_CPURST*

TP18360 CPU1_DBSY•
TP18361 CPU1_DEFER•
TP18362 CPU1_DPRSPT•
TP18363 CPU1_DPSLP•
TP18364 CPU1_DPMR•
TP18365 CPU1_DRDY•

TP18366 CPU1_FERR•
TP18367 CPU1_HIT•
TP18368 CPU1_HITM•
TP18369 CPU1_ICNNE•
TP18370 CPU1_INIT•
TP18371 CPU1_INIR•
TP18372 CPU1_LOCK•
TP18373 CPU1_NMI•
TP18374 CPU1_PWTGDCPU

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T1P3875 CPU1, SLP
T1P3876 CPU1, SM1
T1P3877 CPU1, STRCL
T1P3878 CPU1, HTRMTRIP
T1P3879 CPU1, HTRMTRIP
T1P3880 CPU1, VCCSENSE
T1P3881 CPU1, VID(0)
T1P3882 CPU1, VID(1)
T1P3883 CPU1, VID(2)
T1P3884 CPU1, VID(3)
T1P3885 CPU1, VID(4)
T1P3886 CPU1, VID(5)
T1P3887 CPU1, VID(6)
T1P3888 CPU1, VID(7)
T1P3889 CPU2, THERM0
T1P3890 CPU2, THERMDC
T1P3911 DCK19, IN_
T1P3932 DCK3, BLUE
T1P3933 DCK3, BLUE
T1P3934 DCK3, CLK_33
T1P3935 DCK3, CLKRUN
T1P3936 DCK3, CMPR
T1P3937 DCK3, CMPR
T1P3938 DCK3, EJECT
T1P3939 DCK3, GREEN
T1P3940 DCK3, LAD(0)
T1P3941 DCK3, LAD(1)
T1P3942 DCK3, LAD(2)
T1P3943 DCK3, LAD(3)
T1P3944 DCK3, LDR01
T1P3945 DCK3, LFRAME
T1P3946 DCK3, LFRAME
T1P3947 DCK3, PIRON

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TP18091 CDCK3_PURS5*
 TP18040 CDCK3_RED
 TP18409 CDCK3_SERIRQ
 TP18410 CDCK3_S1014
 TP18411 CDCK3_SMC1K
 TP18412 CDCK3_SMDATA
 TP18413 CDCK3_SSUSTA*
 TP18414 CDCK3_Y
 TP18415 CDCK5_HP_PLUGIN*
 TP18416 CDCK5_LINE_IN_L
 TP18417 CDCK5_LINE_IN_R
 TP18418 CDCK5_LINE_OUT_L
 TP18419 CDCK5_LINE_OUT_R
 TP18420 CDCK5_SPDIF
 TP18421 CDCKLAN_RSTF*

 TP18730 CDV13_DETECT
 TP18733 CDV13_DV1CLK
 TP18734 CDV13_DV1DATA
 TP18707 CDV15_DV1CLK
 TP18708 CDV15_DV1DATA

 TP18422 CDV02_CTRL_CLK
 TP18423 CDV02_CTRLDATA

[illegible]

T184800(KBC_SENS_HS)
T184810(KBC_SENS_MIC)
T184820(KBC_A2L)
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TP18844 O LAN3_SMB_CLK
TP18847 O LAN3_SMB_DATA
TP18551 O LAN3_WAKE*
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TP18552OLAN_LOW_PWR
TP18553OLAN_LOW_PWR2

TP18845OLID3_SWITCH*

TP18841OLCD3_BKLTEN
TP18554OLCD3_BKLTION
TP18555OLCD3_PWMBIA
TP18556OLCD3_VDDEN
TP18557OLED_AMBER
TP18558OLED_GREEN
TP18559OLPC3_LAD(0)
TP18560OLPC3_LAD(1)
TP18561OLPC3_LAD(2)
TP18562OLPC3_LAD(3)
TP18563OLPC3_LFRAME*
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TP18564OMIC1
TP18565OMIC2
TP18566OMINIPCIE3-CLKREQ1*
TP18567OMINIPCIE3-CLKREQ2*

TP18564OMIC1

TP18565 ○ MIC2
TP18566 ○ MINIPCI E3_CLKREQ1*
TP18567 ○ MINIPCI E3_CLKREQ2*

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN TEST POINTS(1)	SAMSUNG ELECTRONICS		
CHECK	HK, PARK	DEV. STEP	SR					
APPROVAL	JS, EUR	REV	1.0					
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM				PAGE	49
						PART NO	BA41-00680(3)A	

4				3				2				1			
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