

HAINAN3_EXT

CPU : Intel Santarosa Merom
Chip Set : RS600&SB600&M64S
Remarks : Mobility Platform

Model Name : HAINAN3_EXT
PBA Name : MAIN
PCB Code : BA41-00809A GCE
BA41-00810A NANYA
Dev. Step : MP1.1
Revision : 1.0
T.R. Date : 2007.09.08

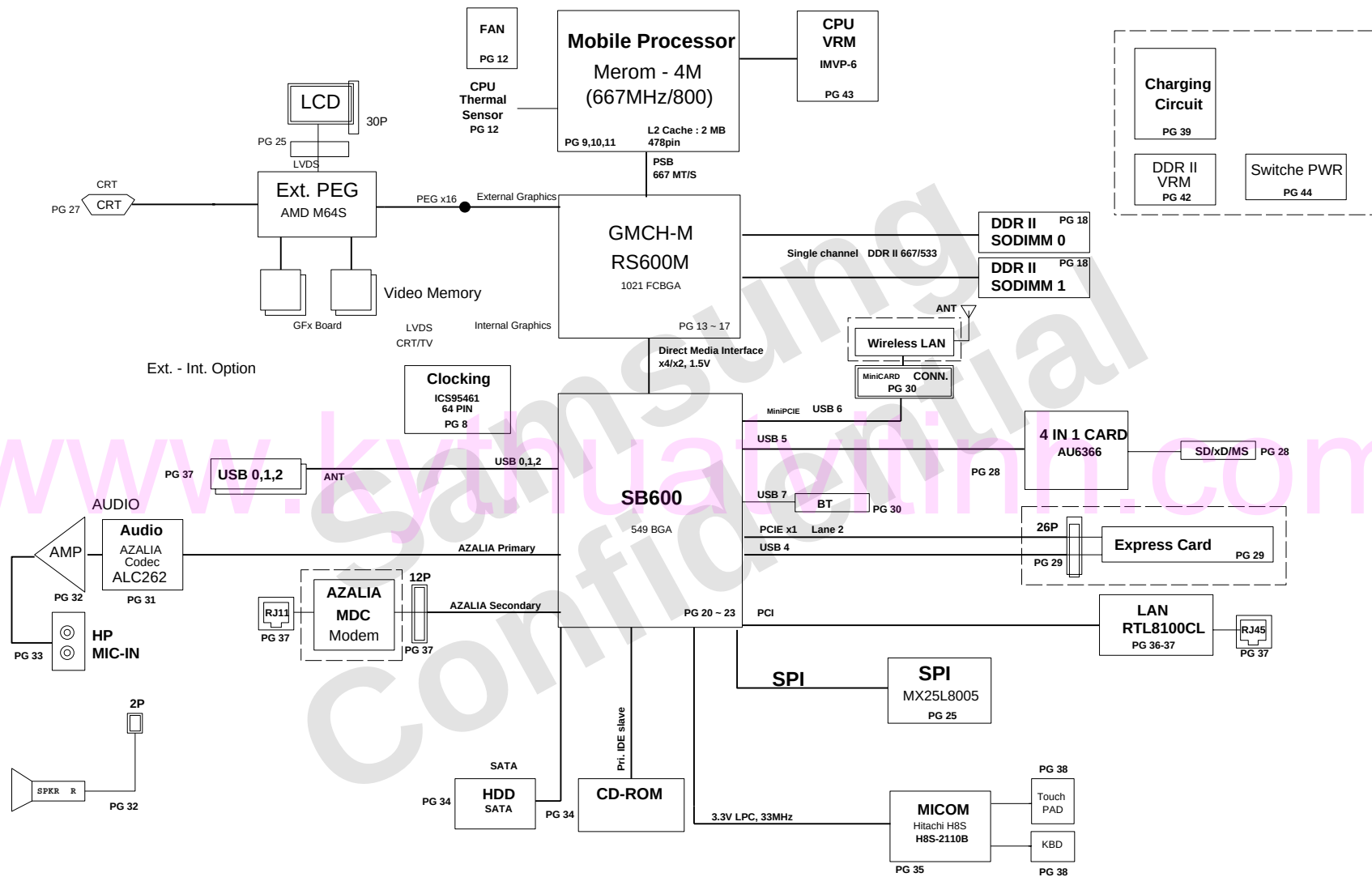
DRAW	CHECK	APPROVAL
ELLEN ZHANG	ROKY ZHENG	KEVIN LEE

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DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0			
				COVER		PART NO. BA41-00809/B10A
MODULE CODE	undefined	LAST EDIT		September 8, 2007 12:02:16 PM		PAGE 1 OF 53

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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	DIAGRAM		
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	2 OF 53	

Power Diagram

KBC3_SUSPWRON

KBC3_PWRON

KBC3_VRON

VCCP3_PWRGD

AC Adapter

Battery DC

VDC

P12.0V_ALWS

P5.0V_ALWS

P1.2V_ALWS

P3.3V_MICOM

P1.2V_ALWS

P1.8V_AUX

P1.5V

P1.8V

P1.2V

P0.9V

P5.0V_AUX

P5.0V

P3.3V_AUX

P3.3V

P2.5V_LAN

P1.05V
MEROM
NB
SB
(VCCP_CORE)

CPU_CORE
MEROM

Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

S5 / S4

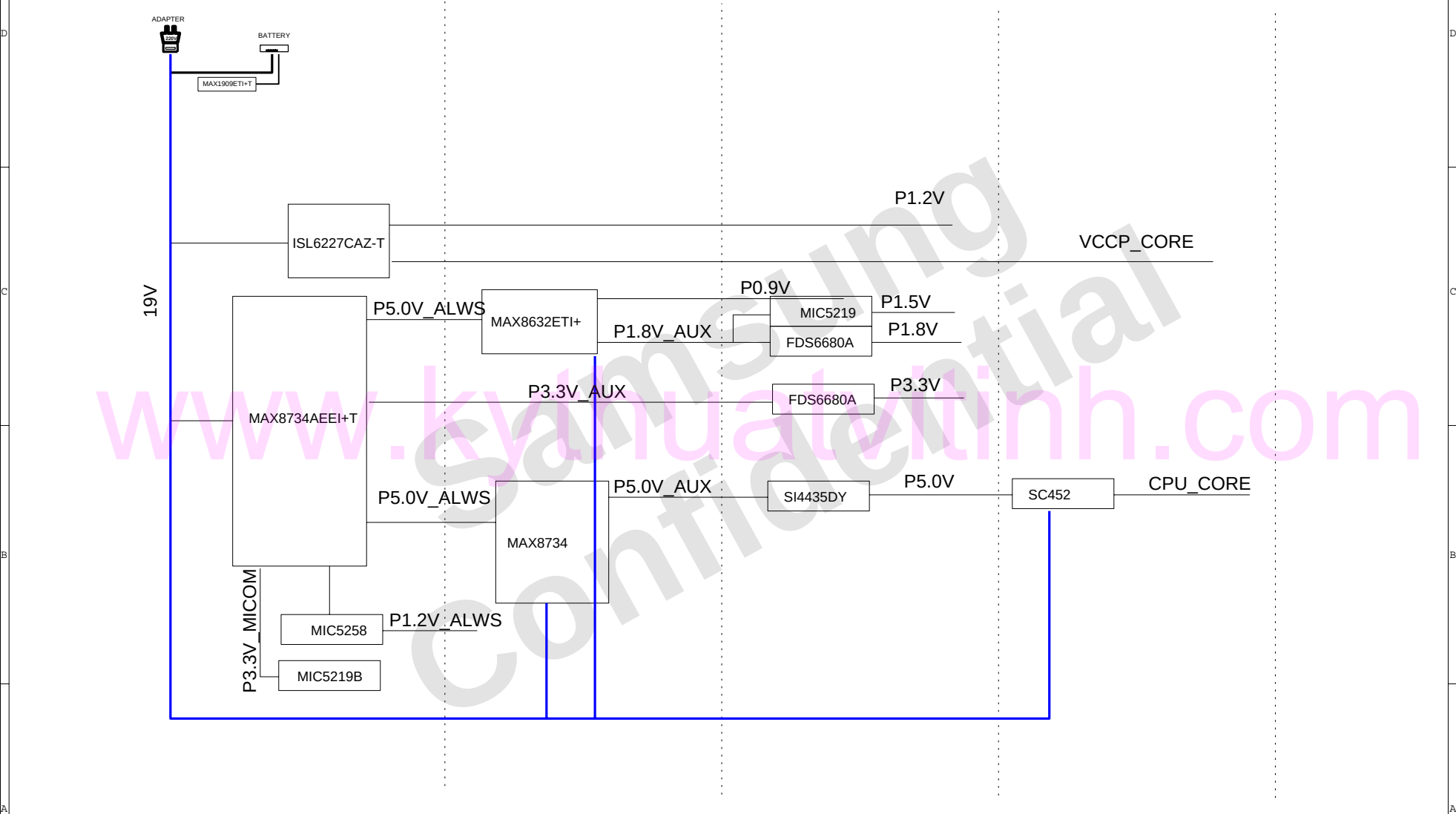
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S0

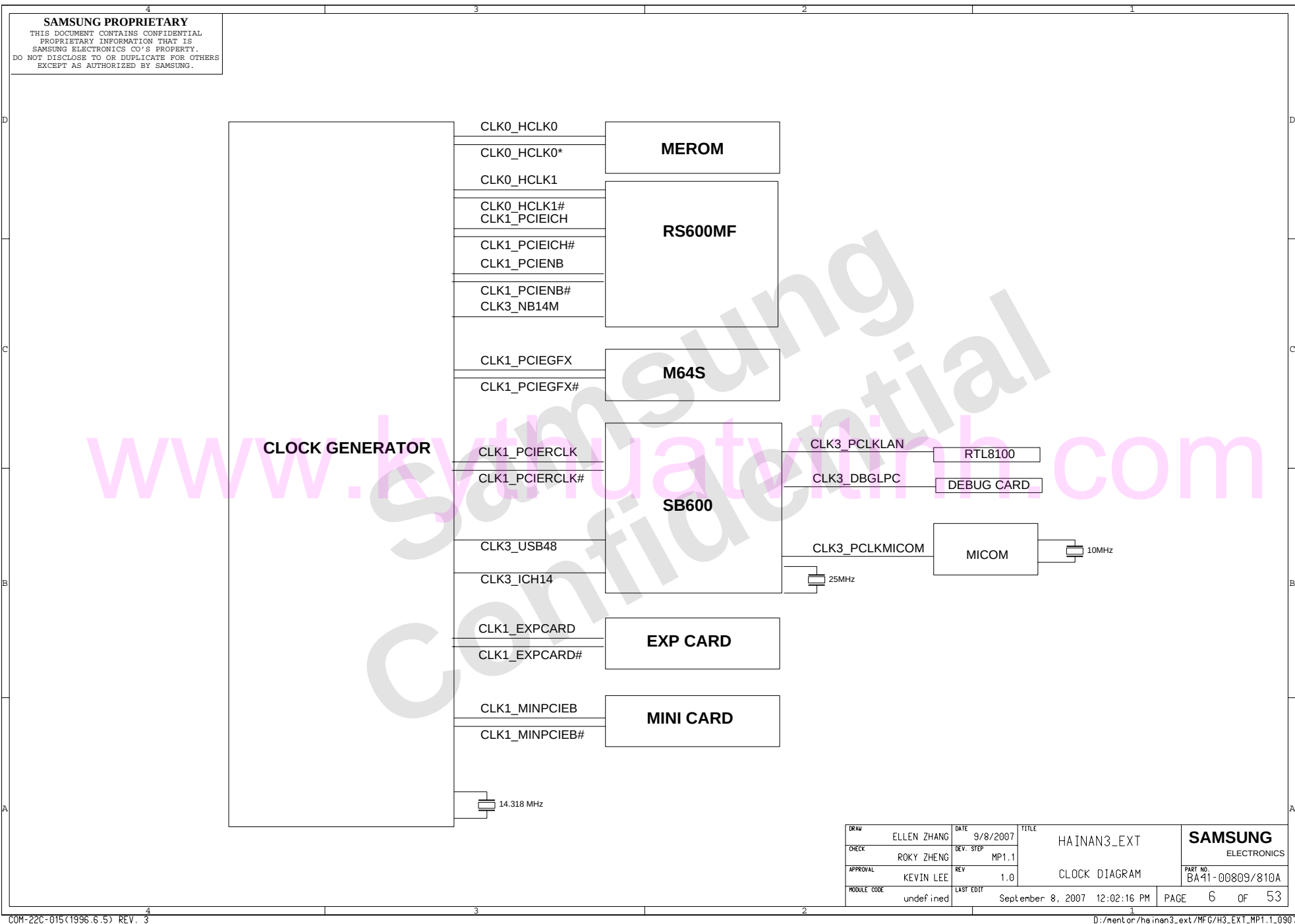
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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	POWER DIAGRAM		
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POWER RAILS ANALYSIS



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	POWER BLOCK		
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	5 OF 53	



PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
LAN	AD21	1	G
USB	AD30(internal)	-	-
			-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	-
Internal MAC	AD31(internal)	-	-
PCI 1			

Voltage Rails

CPU_CORE	CPU
VCCP_CORE	CPU RS600 SB600
P1.2V	RS600 SB600
P1.5V	CPU EXPCARD
P1.8V	RS600
P0.9V	DDR2
P5.0V	FAN THERMAL CRT SB600 AU6366 MINIPCI ALC262 HDD ODD MICOM USB TOUCH-PAD CPU_CORE
P3.3V	SYSTEM POWER
P2.5V_LAN	RTL8100
P1.8V_AUX	DDR2 P1.8V RS600
P5.0V_AUX	THERMAL LCD P1.2V P5.0V
P3.3V_AUX	MDC MICOM MINIPCI EXP-CARD SB600 THERMAL
P12.0V_ALWS	P1.5V P3.3V P1.8V
P5.0V_ALWS	P3.3V DDR2-PWR
P3.3V_MICOM	THERMAL SB600 MICOM LED P1.8V_ALWS
P1.2V_ALWS	SB600,P1.2V
VDC	Primary DC system power supply (7 to 21V)

2 I C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001x	A2h	-
ICS95411 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0,1	SYSTEM PORT A
2	SYSTEM PORT B
4	EXPRESS CARD
5	4 IN 1 CARD
6	MINI CARD
8	BT

System Power States

CHP3_SLPS1*	S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
CHP3_SLPS3*	S3, Suspend-to-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
CHP3_SLPA5*	S4, Suspend-to-Disk(STD) : The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. External power source same as S3, but may have different wake events.
CHP3_SLPS5*	S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	10MHz	MICOM	HD64F2110B
Crystal	14.318MHz	CLOCK-Generator	ICS95461
Crystal	12MHz	AU6366	4-IN 1 CARD
Crystal	25MHz	LAN	LOM

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 0	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 0	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 0 1 1	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 0	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 0 1	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	1 1 0 0 0 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	1 1 0 0 0 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	1 1 0 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	1 1 0 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	1 1 0 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	1 1 0 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	1 1 0 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	1 1 0 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	1 1 0 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	1 1 0 1 1 1 1	0.7125 V	1 1 0 0 1 1 1	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 1 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 0	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 1 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 1 0 0 0 0 1	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 1 0 0 0 0 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 1 0 0 0 1 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 1 0 0 0 1 0	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 1 0 0 0 1 1	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 1 0 0 0 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 1 0 0 1 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 1 0 0 1 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 1 0 0 1 0 1	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 1 0 0 1 0 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 1 0 0 1 1 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 1 0 0 1 1 0	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 1 0 0 1 1 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 1 0 0 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 1 0 0 1 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

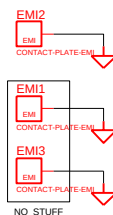
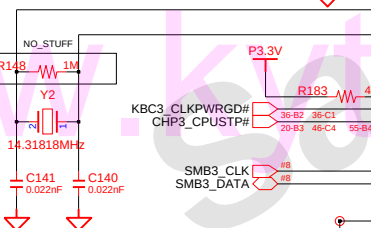
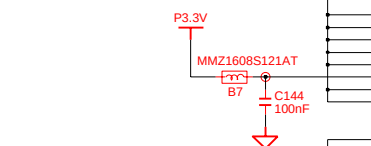
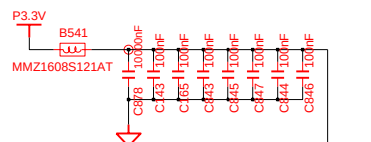
DATE	9/8/2007	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG		
APPROVAL	KEVIN LEE		
MODULE CODE	undef ined		
DEV. STEP	MP1.1	ANNOTATIONS	PART NO. BA41-00809/810A
REV	1.0		
LAST EDIT	September 8, 2007 12:02:16 PM		
		PAGE	7 OF 53

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CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	0	266 MHz
0	0	1	0	333 MHz
0	1	0	0	200 MHz
0	1	1	0	400 MHz
1	0	0	0	133 MHz
1	0	1	0	100 MHz
1	1	0	0	166 MHz
1	1	1	1	RSVD

Pt decoupling CAPS close to ICS951461 power pin



U6 ICS951461

VDDCPU
 VDD_SRC1
 VDD_SRC2
 VDD_SRC3
 VDD_SRC4
 VDD_48
 VDD_ATIG
 VDD_REF

GND_CPU
 GND_SRC1
 GND_SRC2
 GND_SRC3
 GND_SRC4
 GND_48
 GND_ATIG
 GND_REF

RESET_IN*
 VTPWRGD*_PD
 CPU_STOP*

SMBCLK
 SMBDAT

IREF
 48MHZ_1
 48MHZ_0

CLKREQ0A*
 FSLB_REF1
 FSLC_REF2

SRCLKT0
 SRCLKT1
 SRCLKT2
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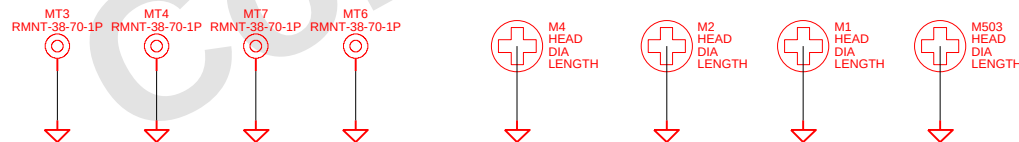
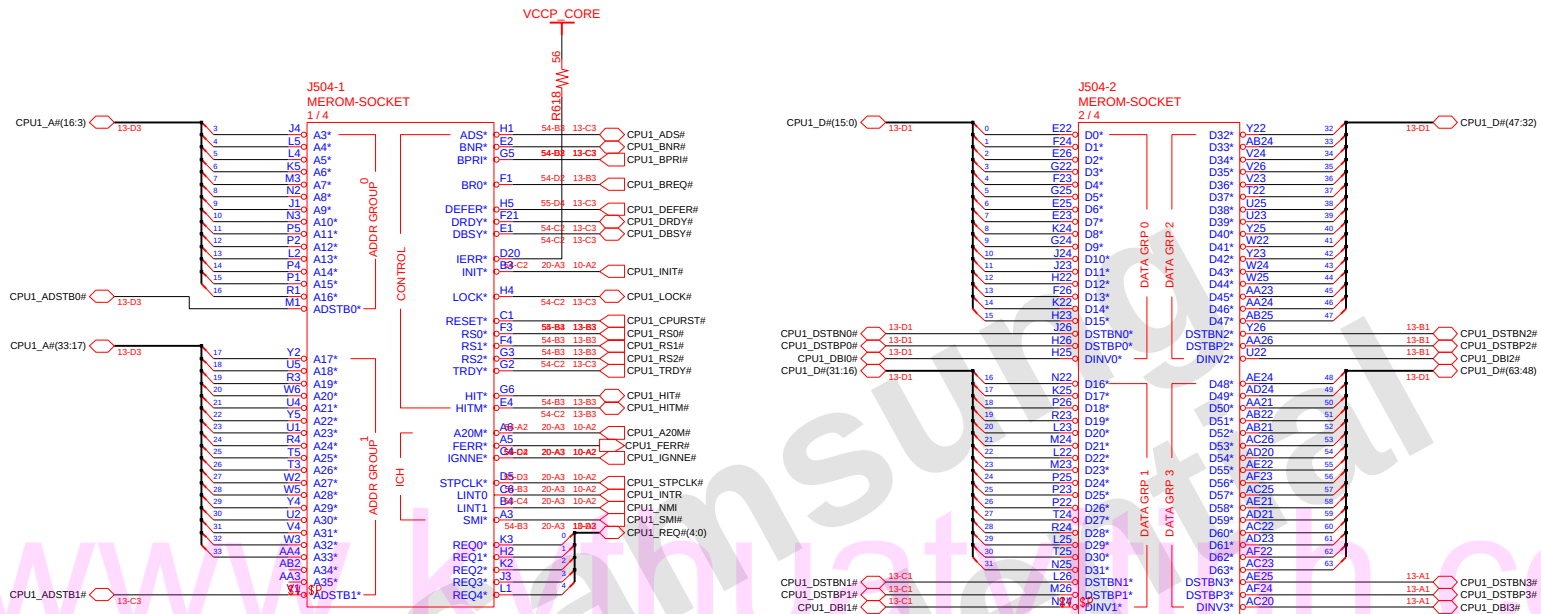
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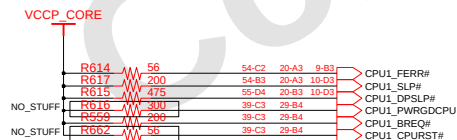
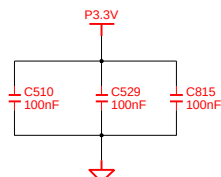
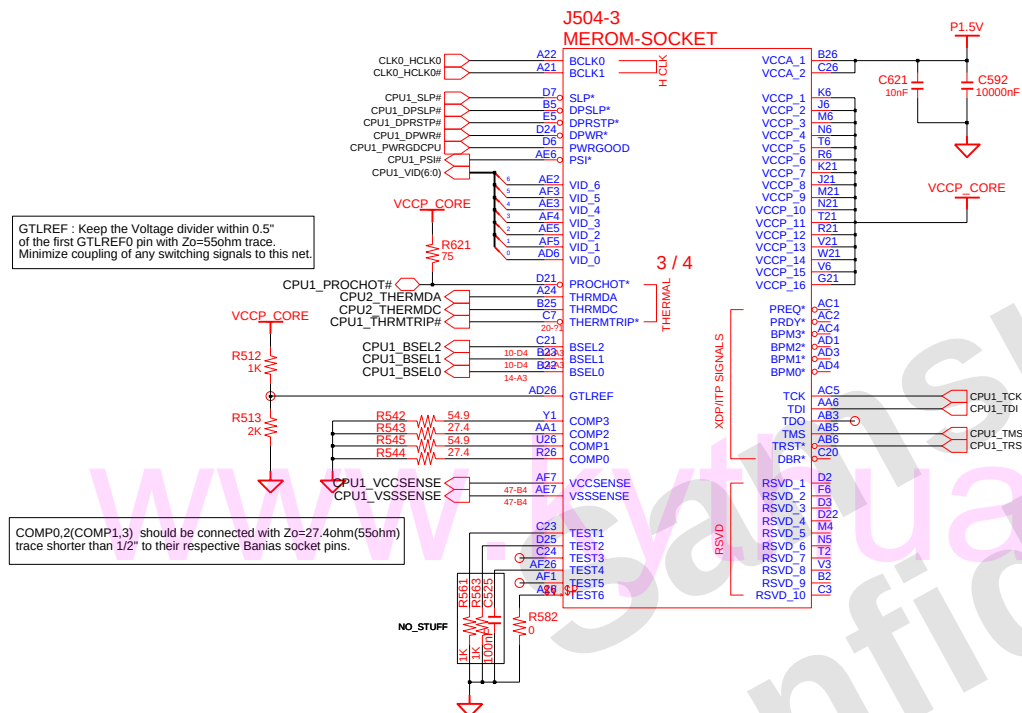
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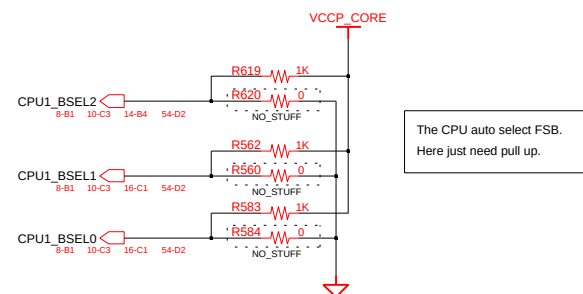
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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	MEROM(1/3)		
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	9 OF 53	



CPU Core Voltage Table IMVP-6

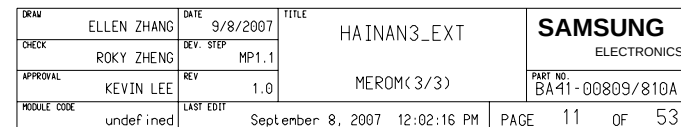
Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	15000 V	0 1 0 1 0 0 0	10000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	14875 V	0 1 0 1 0 0 1	0.9875 V	1 1 1 0 0 1 0	0.48625 V
0 0 0 0 0 1 0	14750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	14625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	14500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	14375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	14250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 1 0 0 1	0.4125 V
0 0 0 0 1 1 1	14125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	14000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	13875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	13750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	13625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	13500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	13375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	13250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	13125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	13000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	12875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	12750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	12625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	12500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	12375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	12250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	12125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 0 1 0 0	0.2000 V
0 0 1 1 0 0 0	12000 V	0 1 1 1 0 0 0	0.7000 V	1 1 0 1 0 0 0	0.1875 V
0 0 1 1 0 0 1	11875 V	1 0 0 0 0 0 0	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	11750 V	1 0 0 0 0 0 1	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	11625 V	1 0 0 0 0 1 0	0.6625 V	1 1 0 1 1 0 0	0.1500 V
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0 0 1 1 1 0 1	11375 V	1 0 0 0 1 0 0	0.6375 V	1 1 0 1 1 1 0	0.1250 V
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0 0 1 1 1 1 1	11125 V	1 0 0 0 1 1 0	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	11000 V	1 0 0 0 1 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	10875 V	1 0 0 0 1 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	10750 V	1 0 0 0 1 0 1	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	10625 V	1 0 0 0 1 1 0	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	10500 V	1 0 0 0 1 1 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	10375 V	1 0 0 0 1 1 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	10250 V	1 0 0 0 1 1 1	0.5250 V	1 1 1 1 0 0 0	0.0125 V
0 1 0 0 1 1 1	10125 V	1 0 0 0 1 1 1	0.5125 V	1 1 1 1 0 0 1	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 1 0	0.0000 V
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				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
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*Yonah Processor (2.33 GHz / 800 MHz : TBD)



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS	
CHECK	ROKY ZHENG	DEV. STEP	MP1.1				
APPROVAL	KEVIN LEE	REV	1.0				
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM				
				MEROM(2/3)		PART NO.	BA411-00809/810A

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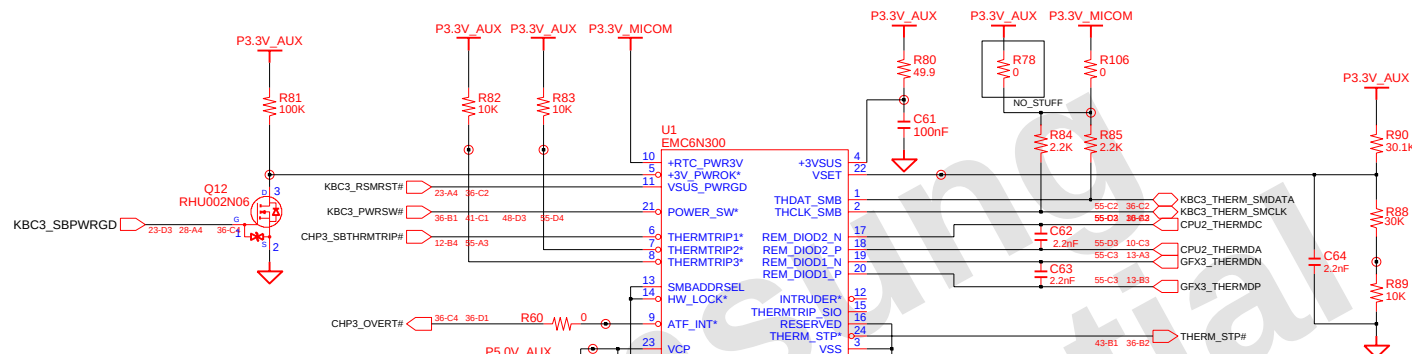
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CPU / RS600 Thermal Sensor

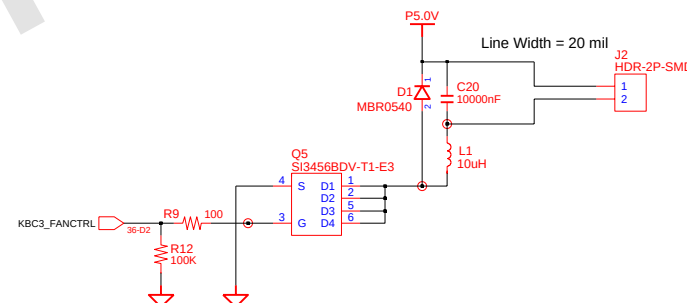
Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND



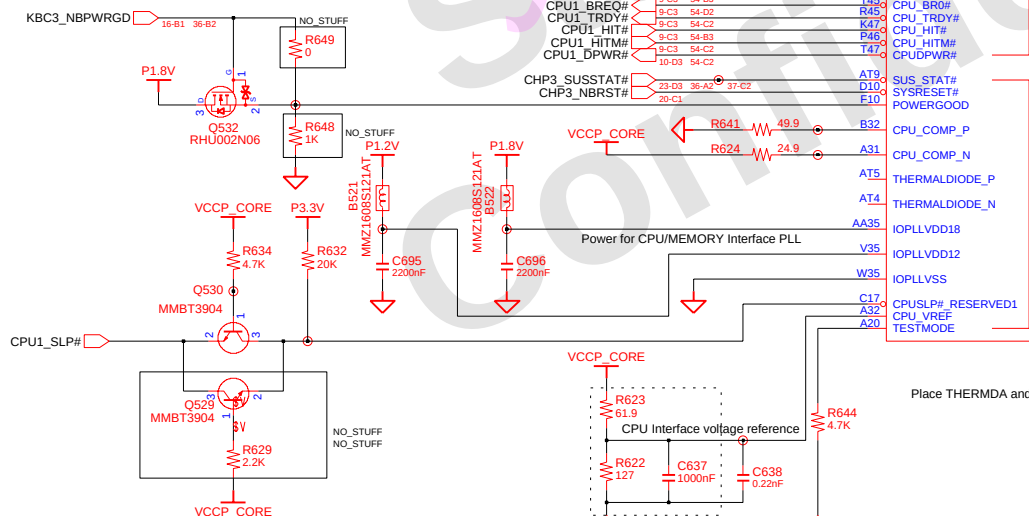
PLACE THIS AT THE OPPSITE SIDE OF CPU

Place between NB and CPU

FAN Control Logic

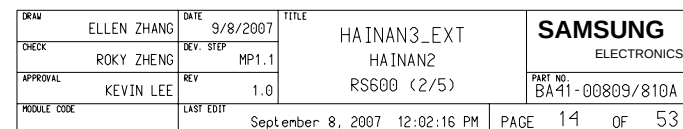
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APPROVAL	KEVIN LEE	REV	1.0	THERMAL & FAN		
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	12 OF 53	

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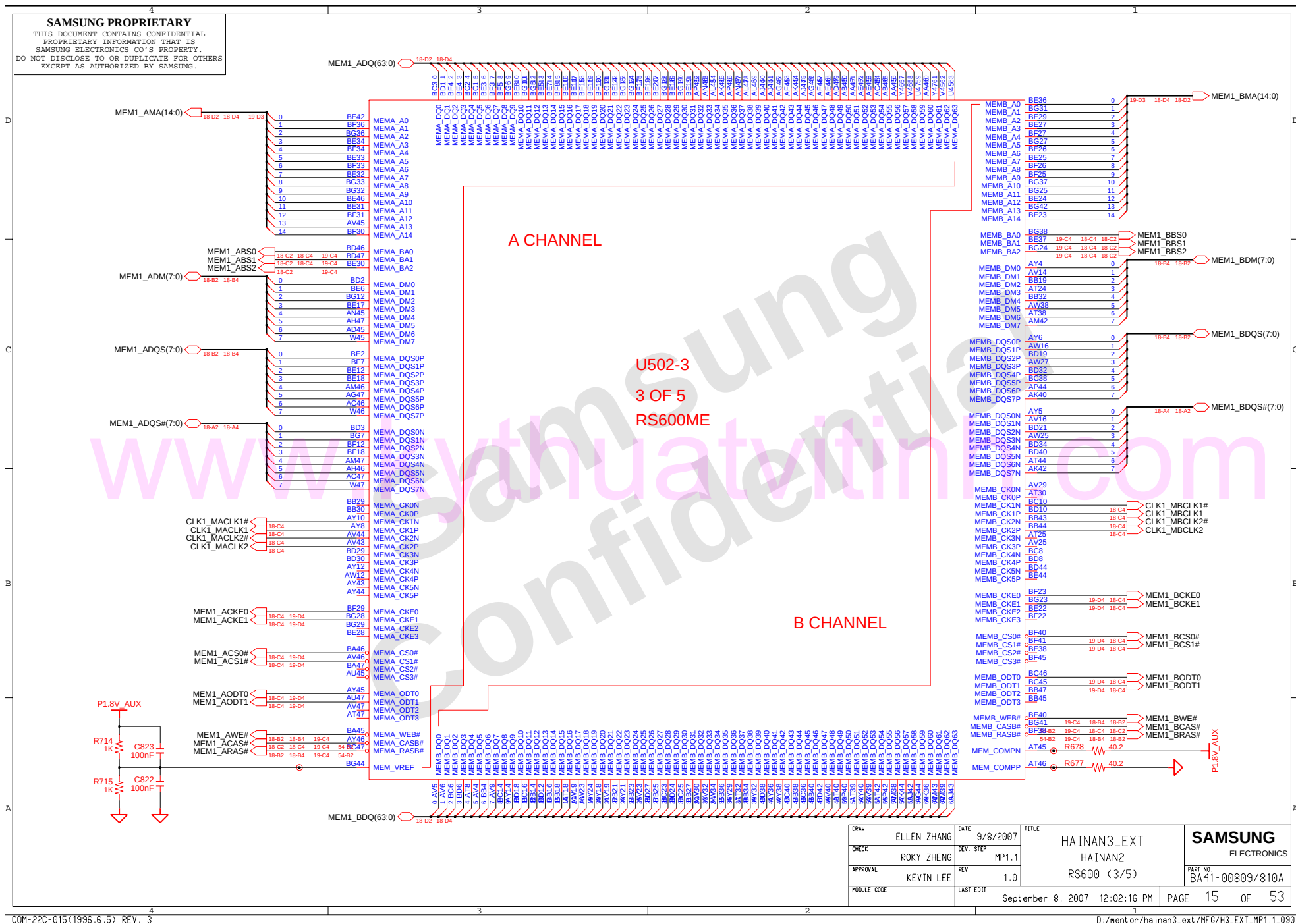


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CHECK	ROKY ZHENG	DEV. STEP	HAINAN2		ELECTRONICS	
APPROVAL	KEVIN LEE	REV	RS600 (1/5)		PART NO.	
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM		BA41-00809/810A	
					PAGE 13 OF 53	

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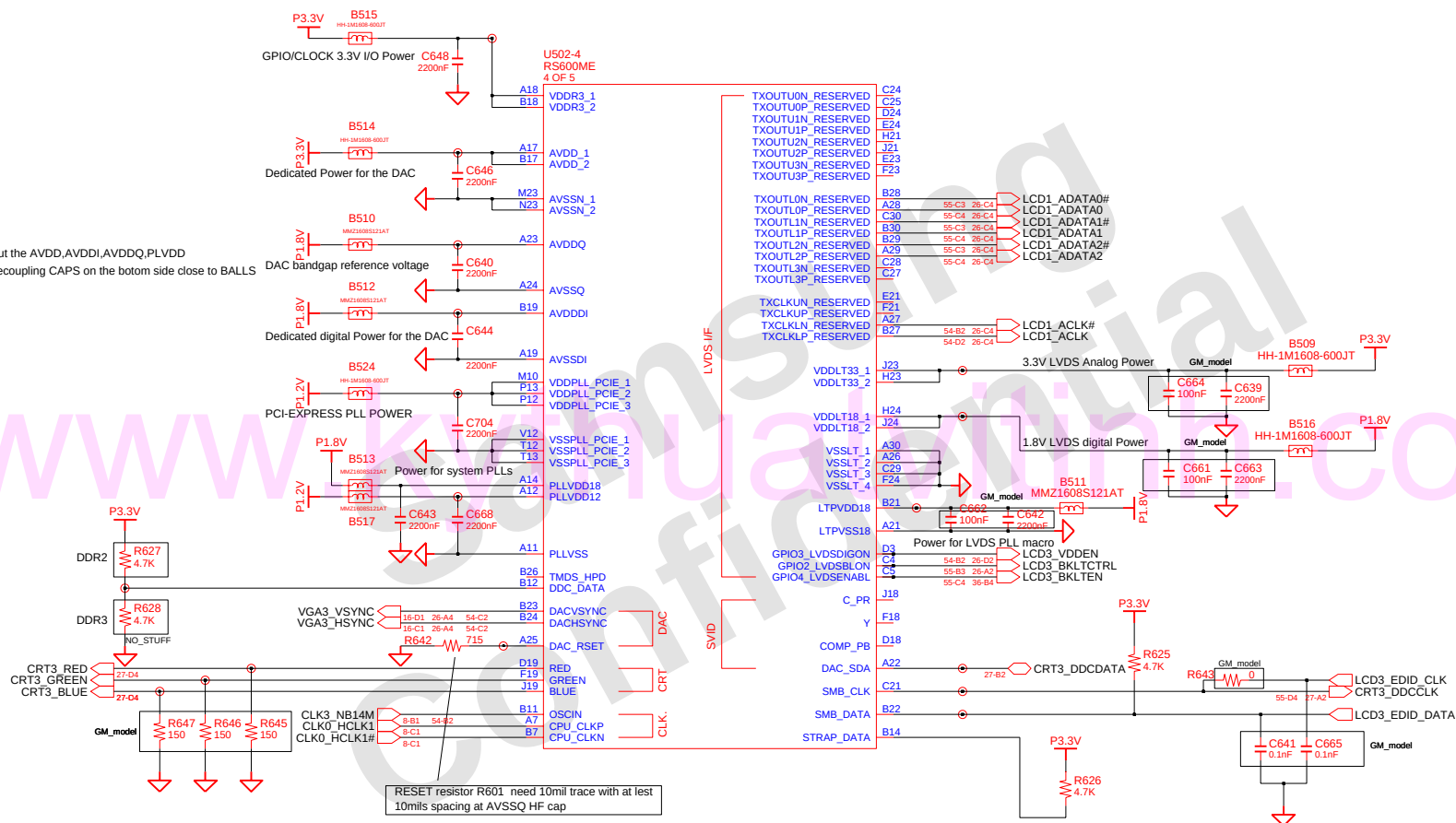
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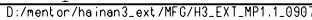
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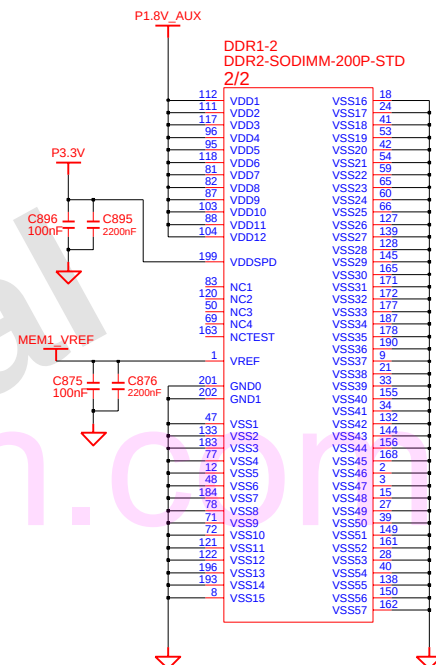
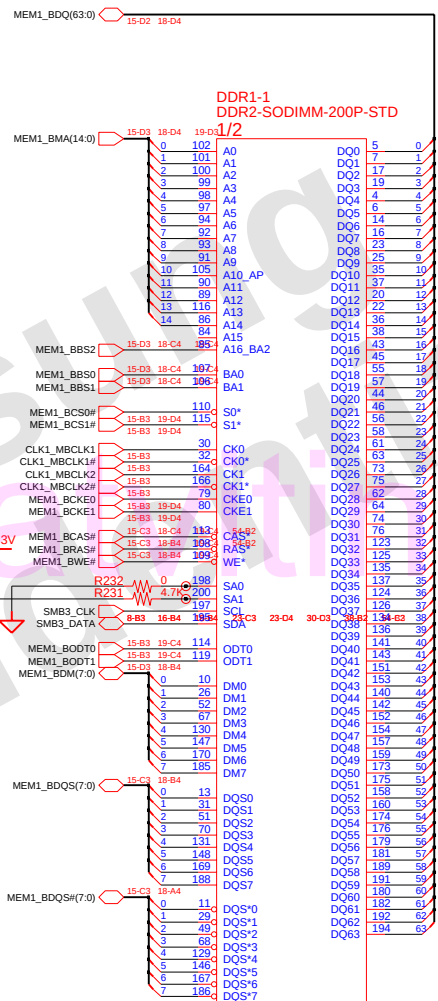
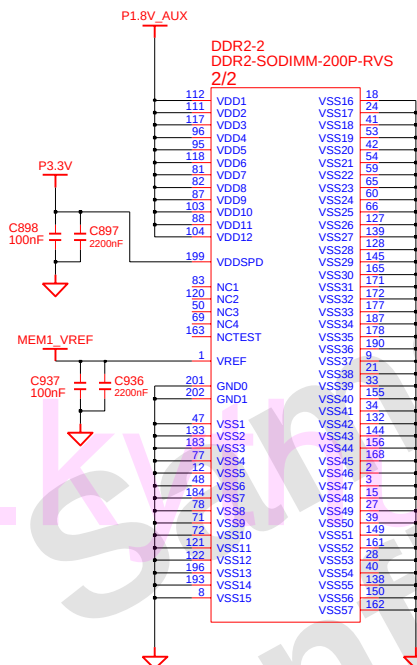
Put the AVDD,AVDDI,AVDDQ,PLVDD
 decoupling CAPS on the botom side close to BALLS



RESET resistor R601 need 10mil trace with at least
 10mils spacing at AVSSQ HF cap

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1		HAINAN2	
APPROVAL	KEVIN LEE	REV	1.0		RS600 (4/5)	
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	16 OF 53	



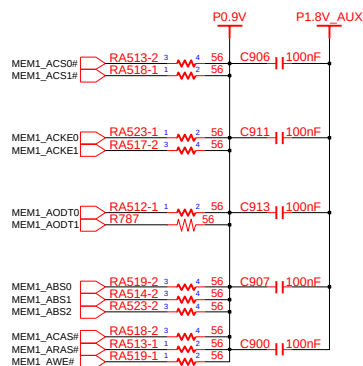


COM-22C-015(1996.6.5) REV. 3

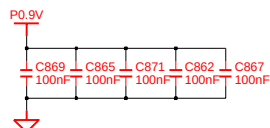
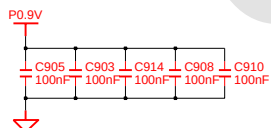
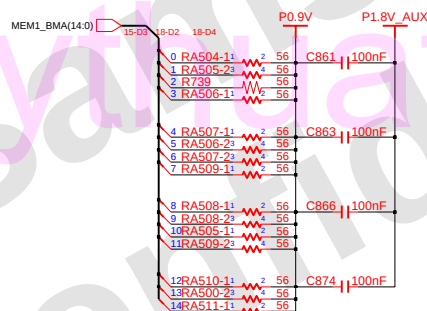
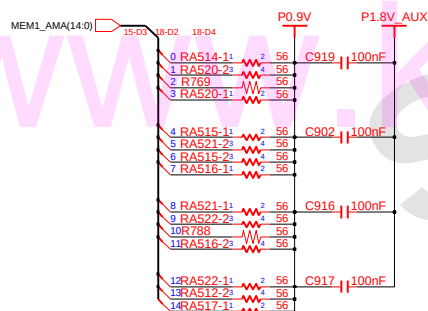
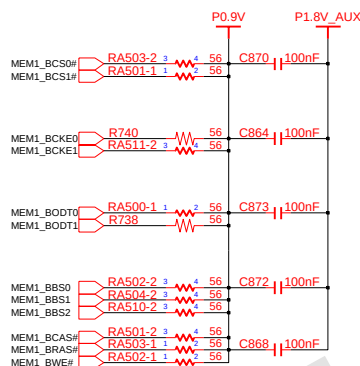
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Channel 1

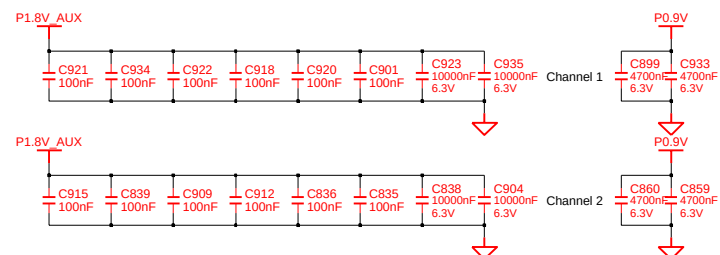
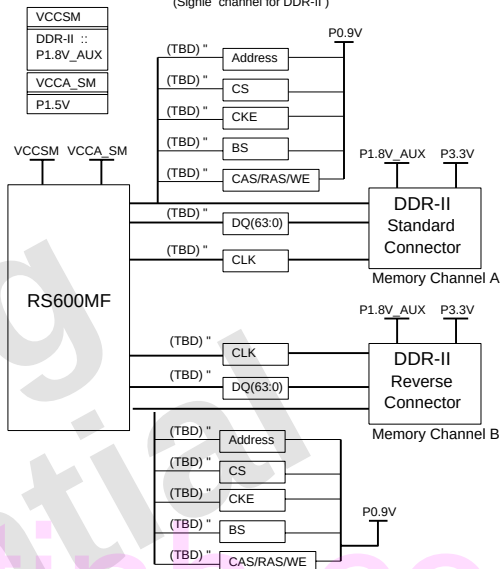


Channel 2



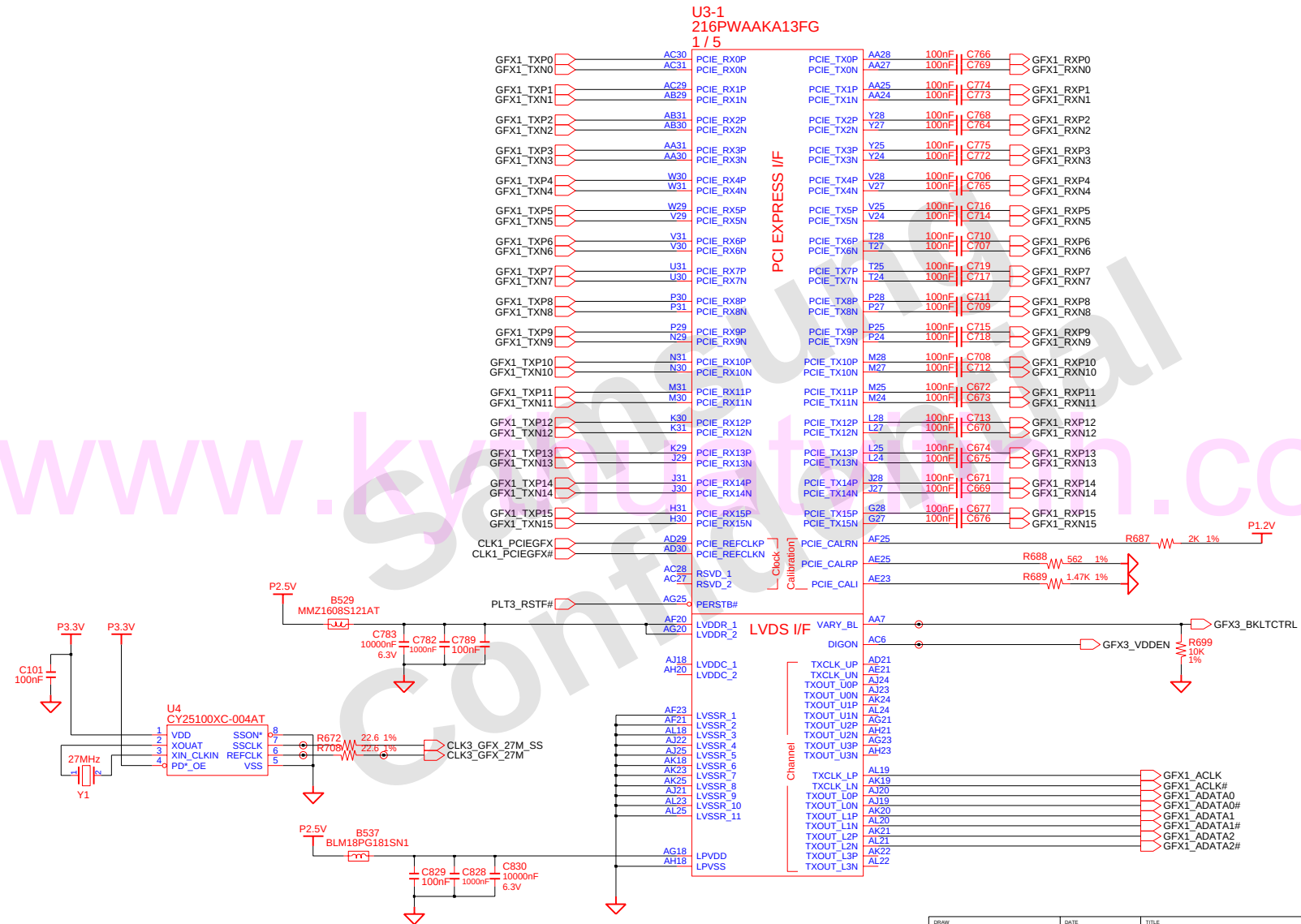
Memory Topology

(Single channel for DDR-II)



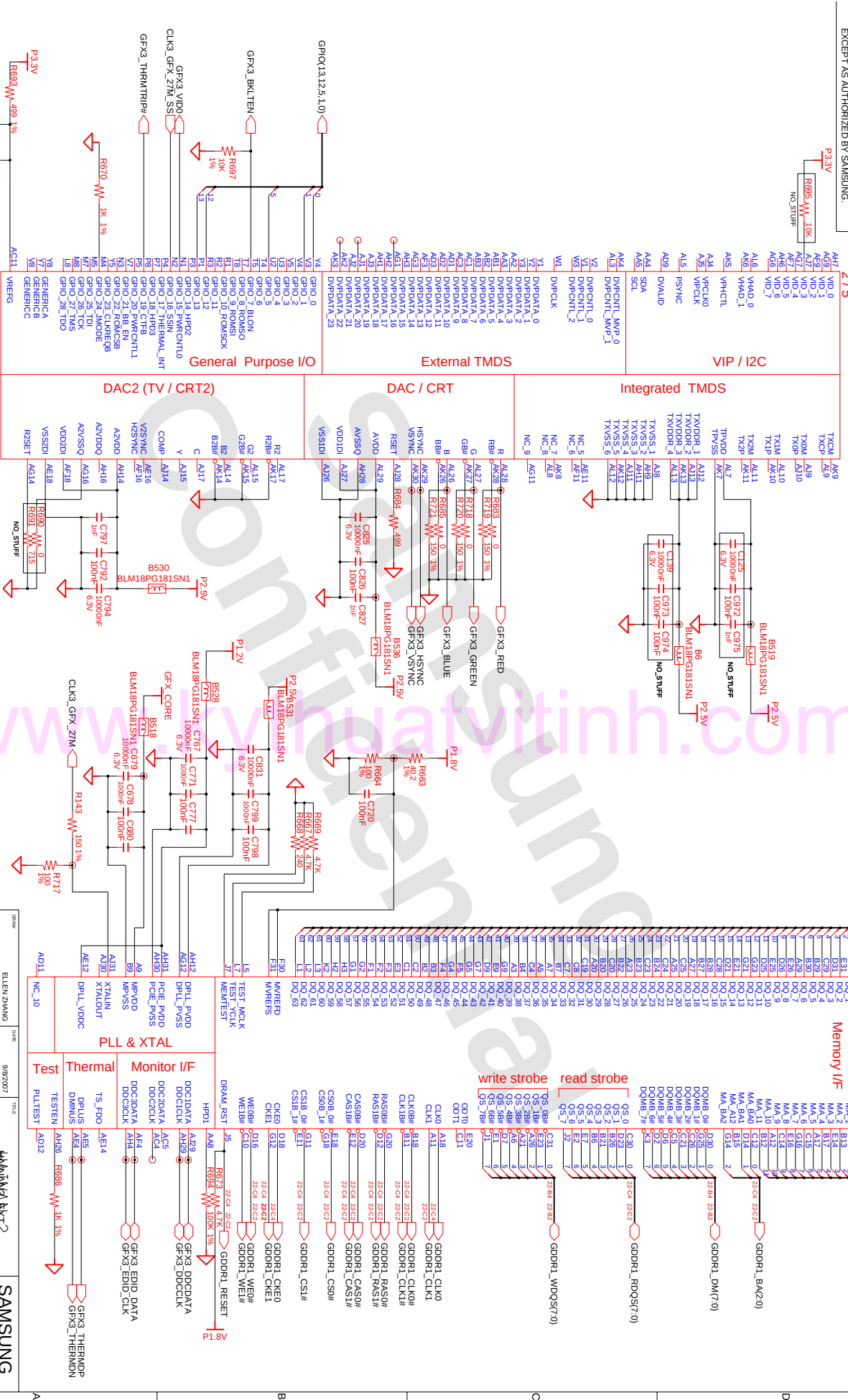
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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		DDR2 TERMINATION	
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	19 OF 53	

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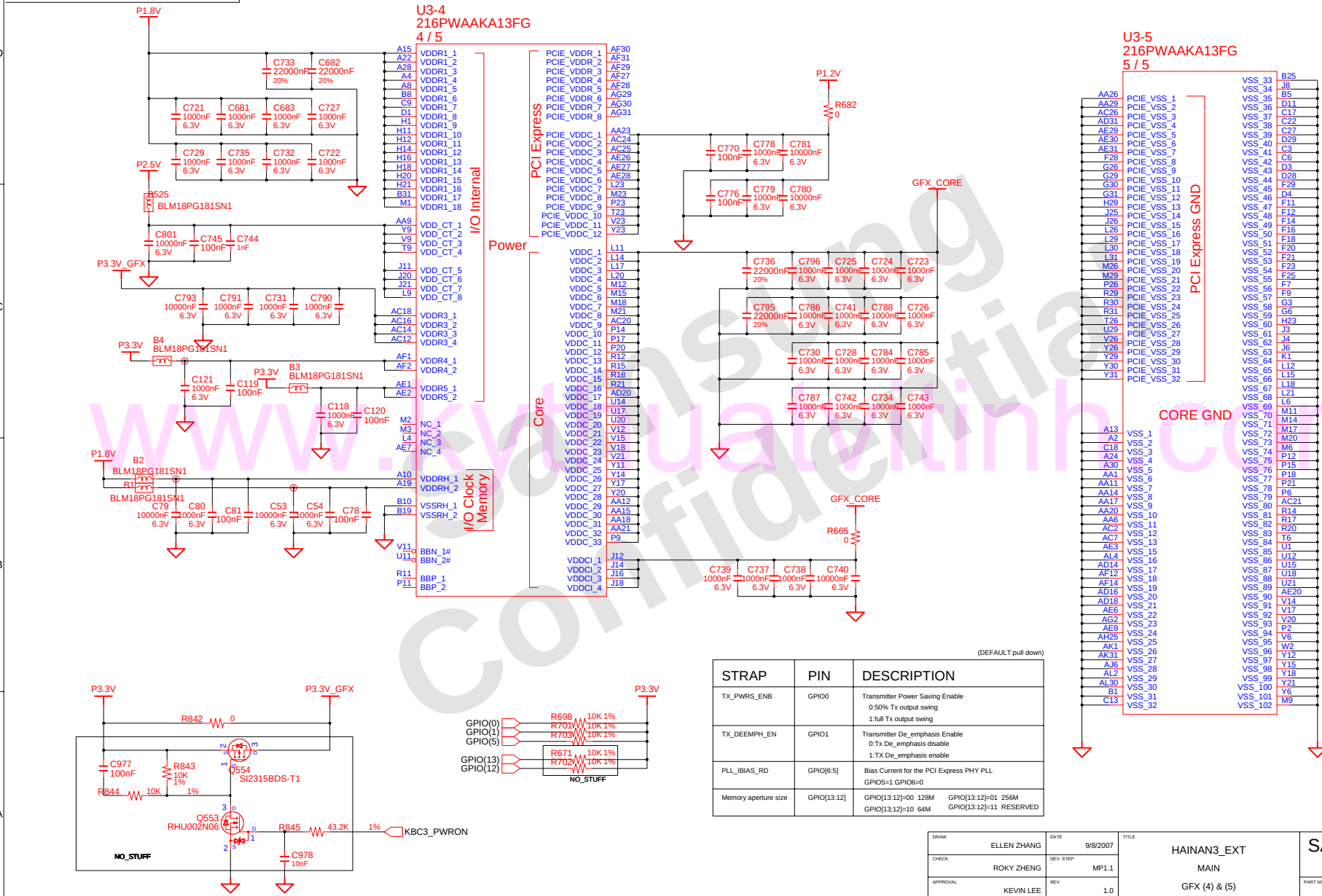


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG
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APPROVAL	KEVIN LEE	REV	1.0	GFX (1)		PART NO.
MODULE CODE		LAST EDIT				BA41-00809/810A
				September 8, 2007 12:02:16 PM	PAGE	20 OF 53

U3-2
216PWAKA13FG



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U13 K4J52324QC-BC14

U17 K4J52324QC-BC14

U13 Pin Connections:

- GDDR1_MA(11:0) to A0-A11
- GDDR1_CLK0 to CK
- GDDR1_CLK0# to CK*
- GDDR1_CKE0 to H4
- GDDR1_BA(2:0) to G4, G9, H10
- GDDR1_RESET to V4
- GDDR1_CS0# to F9
- GDDR1_RAS0# to H3
- GDDR1_CAS0# to H9
- GDDR1_WE0# to H9
- GDDR1_RDQS(3:0) to D3, D10, P10, P3
- GDDR1_WDQS(3:0) to D2, D11, P11, P2
- GDDR1_DM(3:0) to E3, E10, N10, N3
- GDDR1_VREF to H1, H12
- VSS 1 to VSS 14
- VSSA 1 to VSSA 14

U17 Pin Connections:

- GDDR1_MA(11:0) to A0-A11
- GDDR1_CLK1 to CK
- GDDR1_CLK1# to CK*
- GDDR1_CKE1 to H4
- GDDR1_BA(2:0) to G4, G9, H10
- GDDR1_RESET to V4
- GDDR1_CS1# to F9
- GDDR1_RAS1# to H3
- GDDR1_CAS1# to H9
- GDDR1_WE1# to H9
- GDDR1_RDQS(7:4) to D3, D10, P10, P3
- GDDR1_WDQS(7:4) to D2, D11, P11, P2
- GDDR1_DM(7:4) to E3, E10, N10, N3
- GDDR1_VREF to H1, H12
- VSS 1 to VSS 14
- VSSA 1 to VSSA 14

Component Values:

- C625: 100nF
- C687: 100nF
- C624: 220nF
- C684: 100nF
- C628: 100nF
- C746: 100nF
- C685: 100nF
- C627: 100nF
- C623: 100nF
- C747: 220nF
- C686: 100nF
- R61: 60.4 1%
- R62: 60.4 1%
- R97: 60.4 1%
- R109: 60.4 1%
- R94: 240 A4
- R68: 240 A4
- R650: 5.6K 1%
- R98: 5.6K
- R93: 121 1%
- R96: 121 1%
- R92: 121 1%
- R95: 121 1%

Legend:

- 0: G4
- 1: G9
- 2: H10
- 3: D3
- 4: D2
- 5: D11
- 6: P11
- 7: P10
- 8: P3
- 9: F9
- 10: H3
- 11: H9
- 12: H1
- 13: H12
- 14: VSS 1
- 15: VSS 2
- 16: VSS 3
- 17: VSS 4
- 18: VSS 5
- 19: VSS 6
- 20: VSS 7
- 21: VSS 8
- 22: VSS 9
- 23: VSS 10
- 24: VSS 11
- 25: VSS 12
- 26: VSS 13
- 27: VSS 14
- 28: VSSA 1
- 29: VSSA 2
- 30: VSSA 3
- 31: VSSA 4
- 32: VSSA 5
- 33: VSSA 6
- 34: VSSA 7
- 35: VSSA 8
- 36: VSSA 9
- 37: VSSA 10
- 38: VSSA 11
- 39: VSSA 12
- 40: VSSA 13
- 41: VSSA 14

Notes:

- All Instances on this Page should be NO_STUFF @ Int. Gfx.

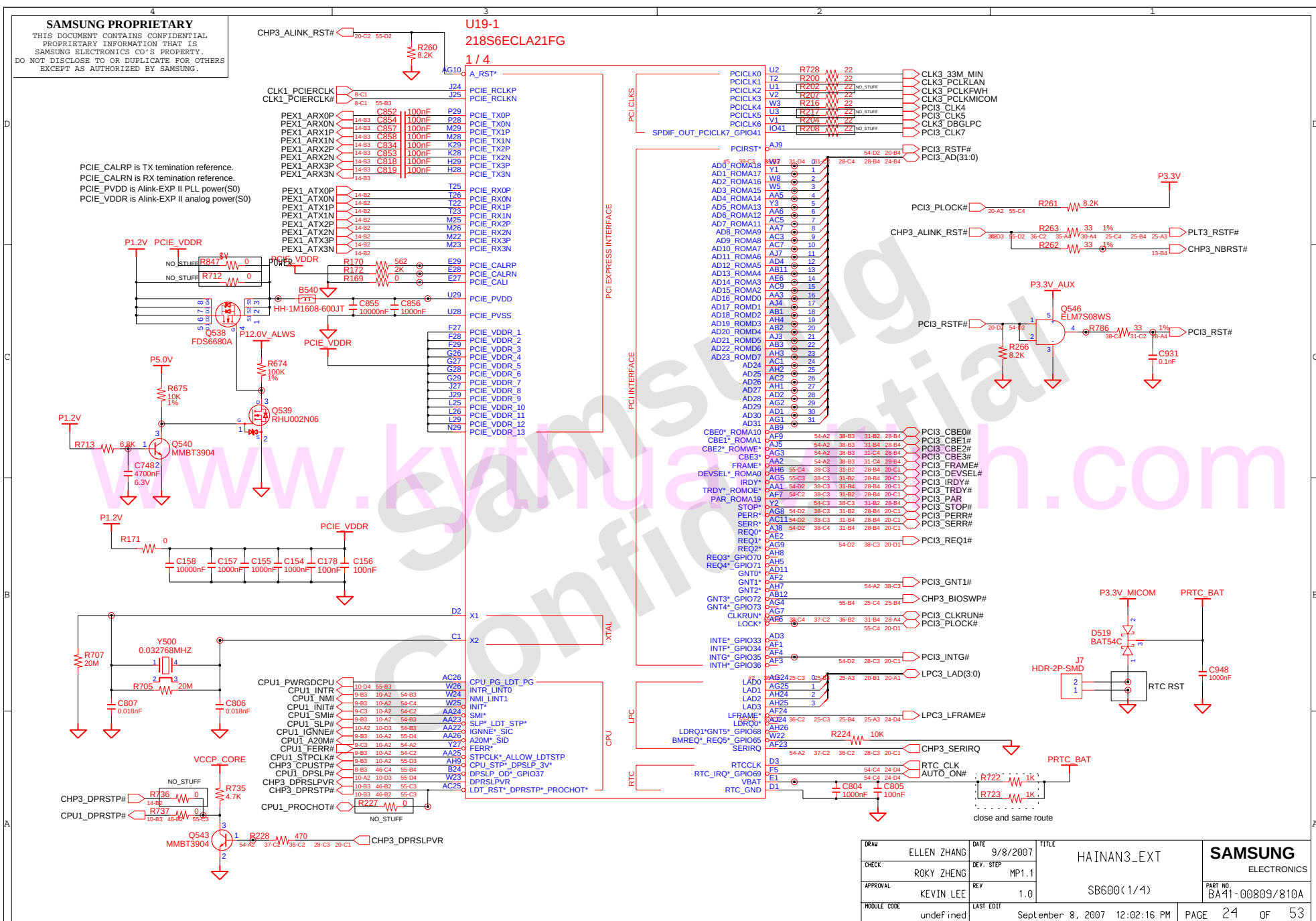
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MODULE CODE		LAST EDIT			

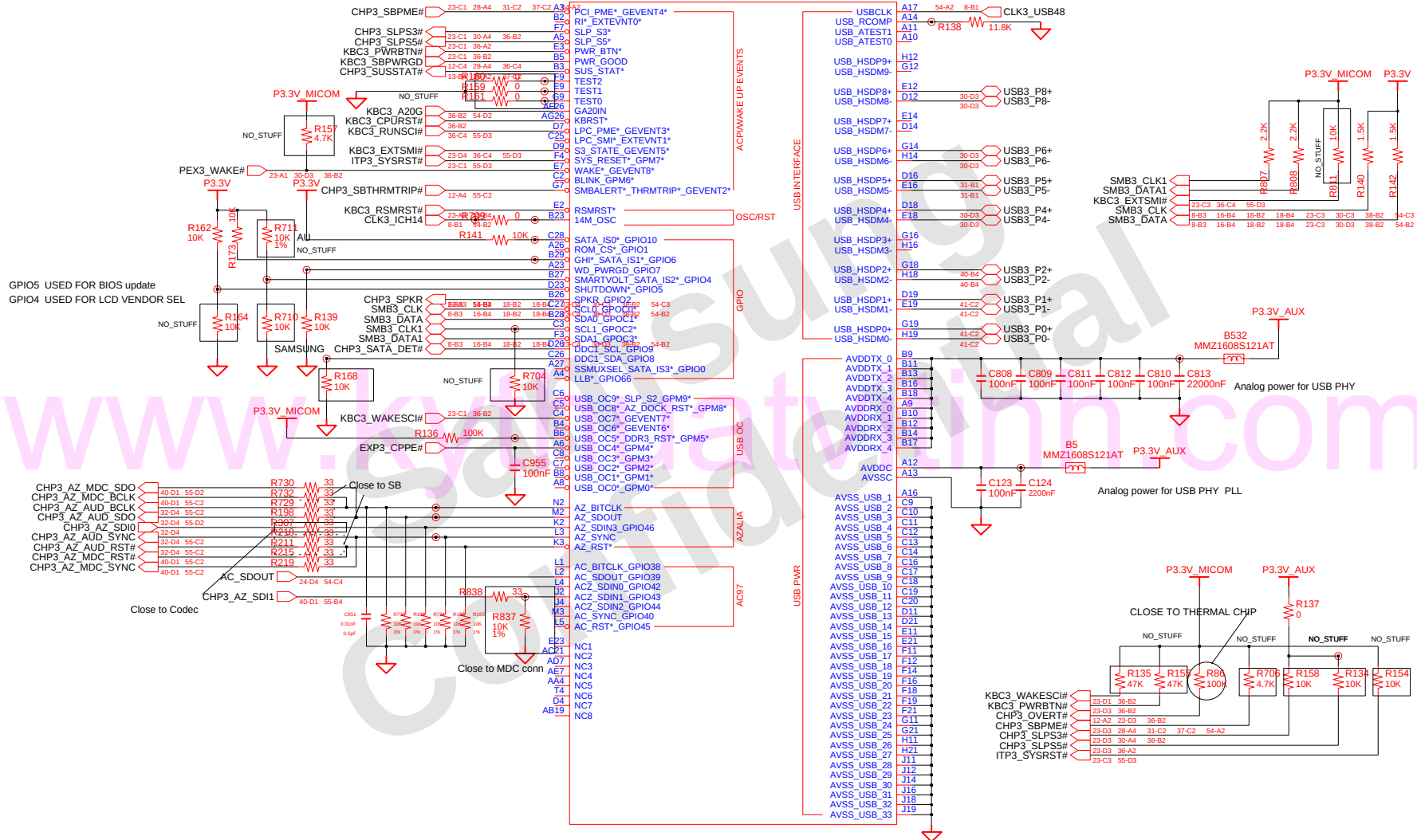
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September 8, 2007 12:02:16 PM
PAGE 23 OF 53

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U19-2
218S6ECLA21FG
2 / 4

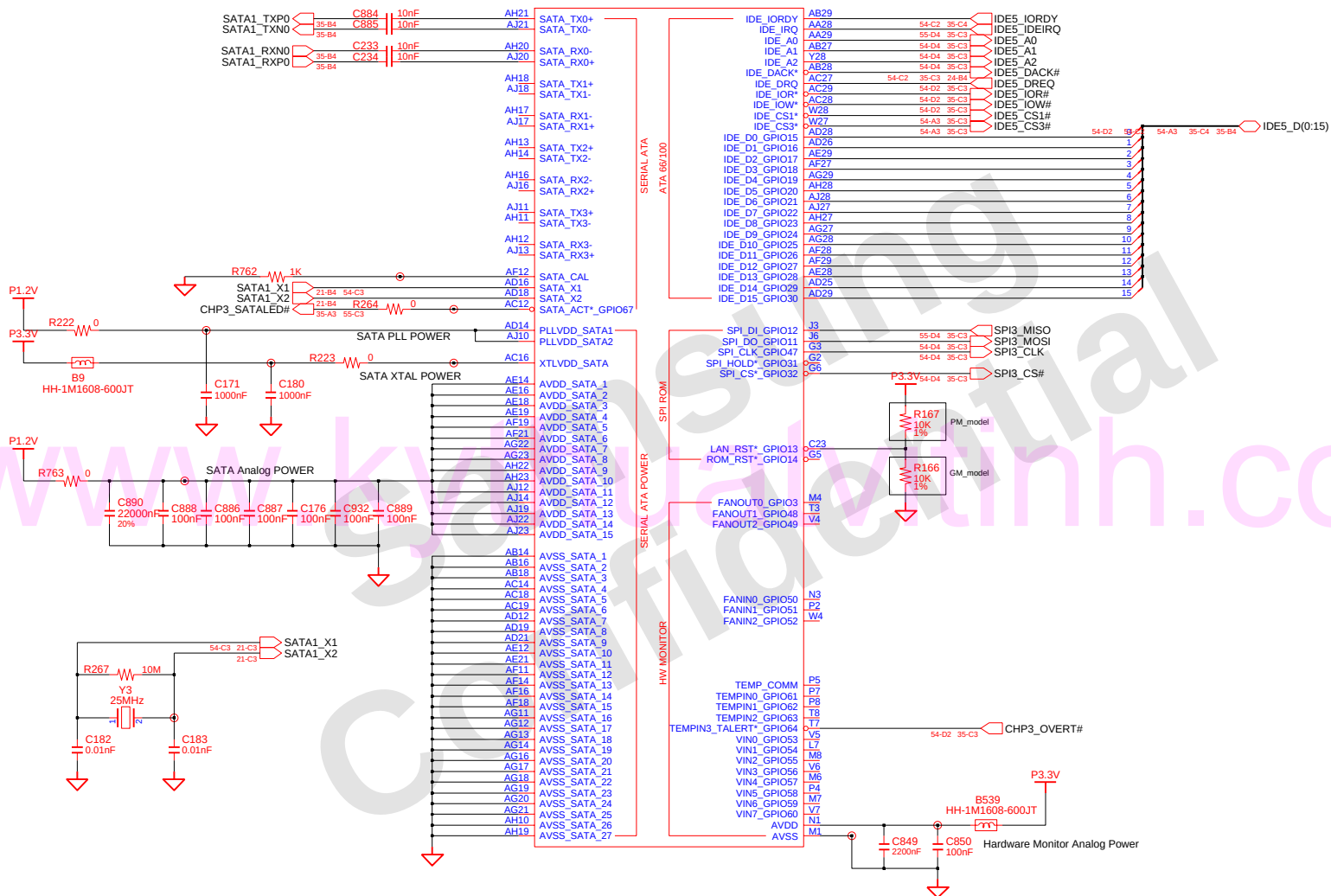


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	25 OF 53	

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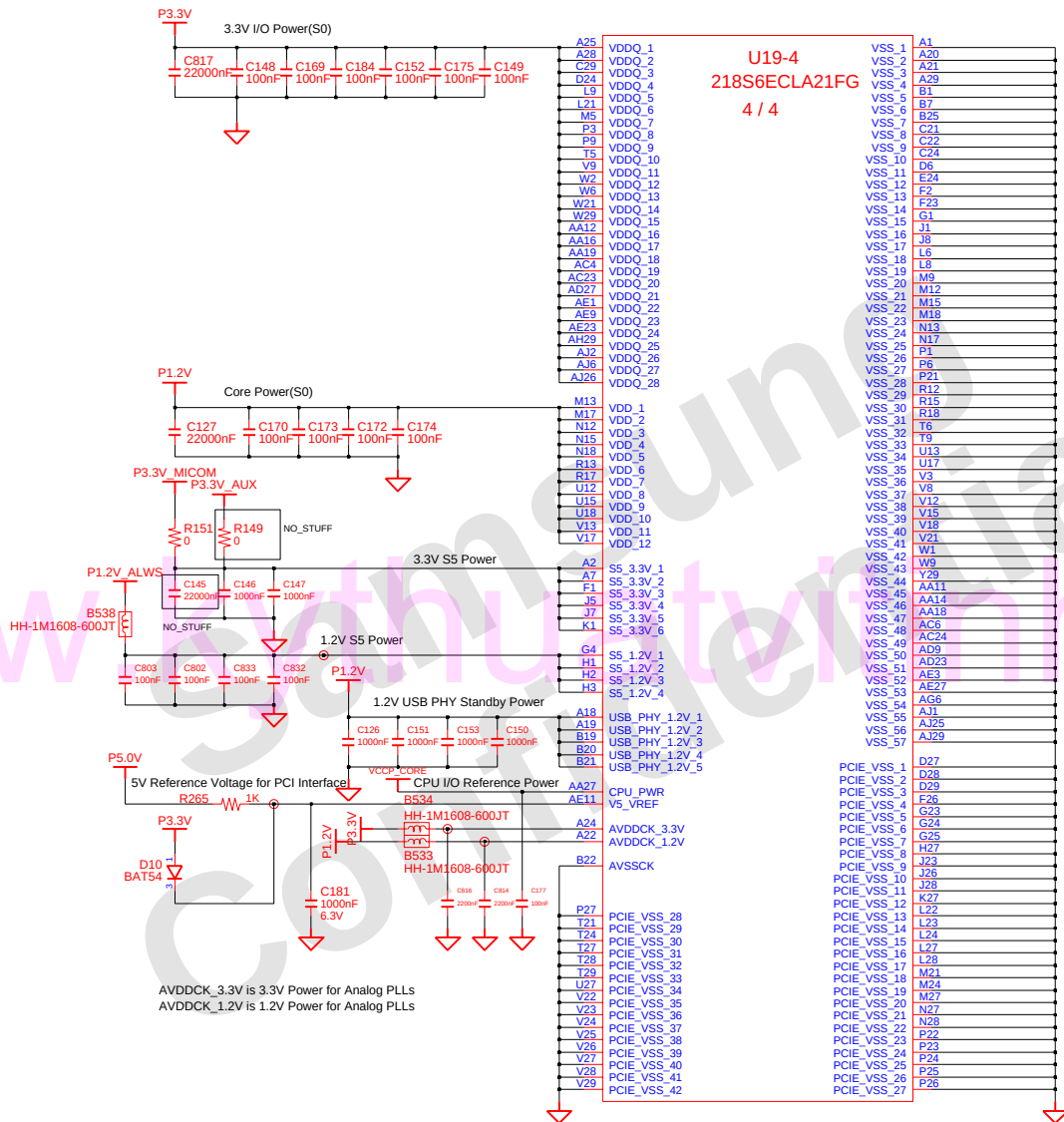
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U19-3
 218S6ECLA21FG
 3 / 4



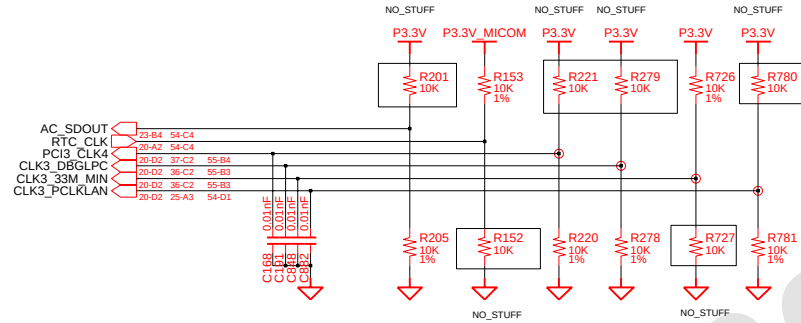
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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		SB600(3/4)	
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	26 OF 53	

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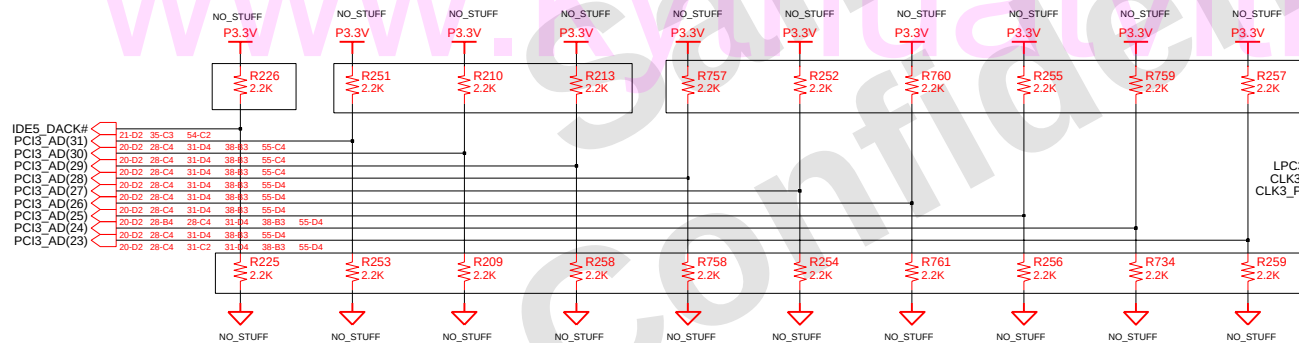
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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		SB600(4/4)	PART NO. BA41-00809/810A
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	27	OF 53

REQUIRED SYSTEM STRAPS



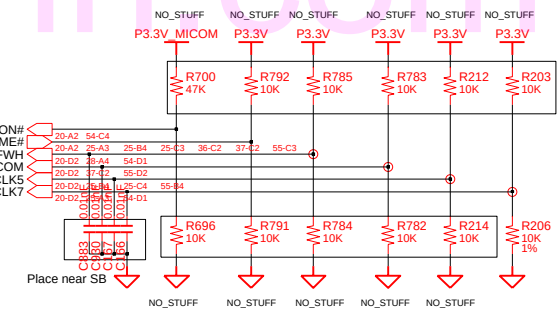
	AC_SDOUT	RTC_CLK	PCI3_CLK4	CLK3_DBG LPC	CLK3_33M_MIN, CLK3_PCLKLAN
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT PLL 48	CPU I/F = K8	ROM TYPE H.H = PCI ROM H.L = SPI ROM L.H = LPC ROM L.L = FWH ROM
STRAP LOW	IGNORE DEBUG STRAPS DEFAULT	EXRERNAL RTC	USE EXT 48MHZ DEFAULT	CPU I/F = P4 DEFAULT	

DEBUG STRAPS



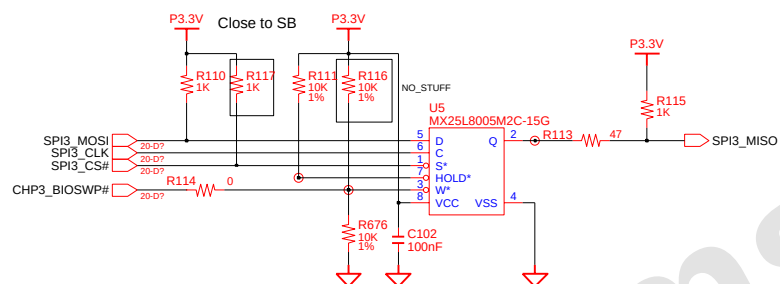
	IDE5_DACK*	PCI3_AD(31)	PCI3_AD(30)	PCI3_AD(29)	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	RESERVED	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTF ALL TIMER DISABLED DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	BOOTF ALL TIMER ENABLED

RESERVED PORT DEBUG

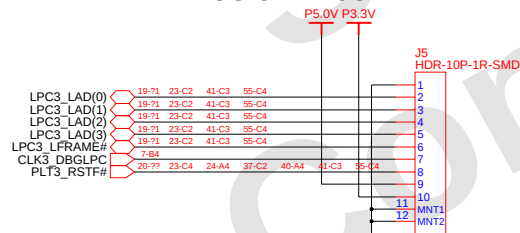


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DEBUG CARD CONN

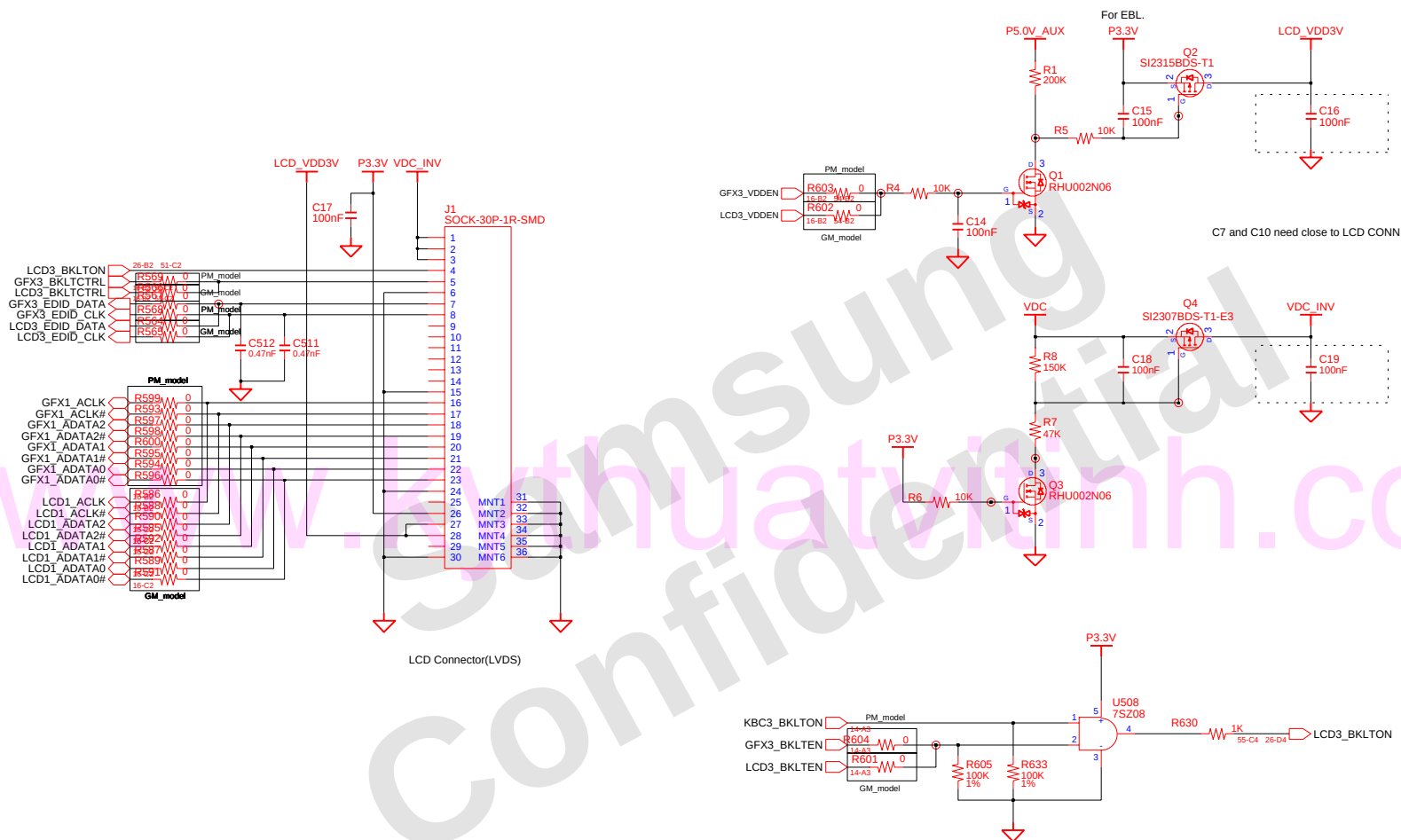


- | | |
|---------------------------------------|------------------------------------|
| 02 VERIFY REAL MODE | 66 CONFIGURE ADVANCE CACHE REG. |
| 03 DISABLE NMI | 6A DISPLAY EXTERNAL CACHE SIZE |
| 04 GET CPU TYPE | 6C DISPLAY SHADOW MESSAGE |
| 06 INIT. SYSTEM H/W | 6E DISPLAY NON-DISPOSABLE SEGMENT |
| 08 INIT. CHIPSET REG. | 70 DISPLAY ERROR MESSAGE |
| 09 SET IN POST FLAG | 72 CHECK FOR CONFIGURATION ERROR |
| 0A INIT CPU.REG | 74 TEST REAL-TIME CLOCK |
| 0B CPU CACHE ON | 76 CHECK FOR KEYBOARD ERROR |
| 0C INIT.CACHE TO POST | 7C SETUP HARDWARE INTERRUPT VECTOR |
| 0E INIT. I/O VALUE | 7E TEST COPROCESSER IF PRESENT |
| 0F ENABLE THE L-BUS IDE | 80 DISABLE ON-BOARD I/O PORT |
| 10 INIT. POWER MANAGER | 82 DETECT AND INSTALL EXT.RS232C |
| 11 LOAD ALTERNATE REG. | 84 DETECT AND INSTALL EXT.PARALLEL |
| 13 PCI BUS MASTER RESET | 86 RE-INIT. ON-BOARD I/O PORT |
| WITH INITIAL POST VALUE | 88 INIT. BIOS DATA ROM |
| 14 INIT. KEYBOARD CONTROLLER | 8A INIT.EXTENDED BIOS DATA AREA |
| 16 CHECK CHECKSUM | 8C INIT. FDD CONTROLLER |
| 18 8254 TIMER INIT. | 9A SHADOW OPTION ROMS |
| 1A 8237 DMA CONTROLLER INIT. | 9C SETUP POWER MANAGEMENT |
| 1C RESET INTERRUPT CONTROLLER | 9E ENABLE H/W INTERRUPT |
| 20 TEST DRAM REFRESH | A0 SET TIME OF DAY |
| 22 TEST 8742 KEYBOARD CONTROLLER | A4 INIT. TYPOMATIC RATE |
| 24 SET ES SEGMENT REG. TO 4GB | A8 ERASE F2 PROMPT |
| 26 ENABLE A20 | AA SCAN FOR F2 KEY STROKE |
| 28 AUTO SIZING DRAM | AC ENTER SETUP |
| 32 COMPUTE THE CPU SPEED | AE CLEAR IN POST FLAG |
| 34 TESET CMOS RAM | B0 CHECK FOR ERRORS |
| 38 SHADOW SYSTEM BIOS ROM | B2 POST DONE-PREPARE TO BOOT O/S |
| 3A AUTO SIZING CACHE | B4 ONE BEEP |
| 3C CONFIGURE ADVANCED CHIPSET REG. | B6 CHECK PASSWORD (OPTION) |
| 3D LOAD ALTER REG. WITH CMOS VALUE | B7 ACPI INIT |
| 42 INIT. INTERRUPT VECTOR | BA DMI INIT |
| 44 INIT. BIOS INTERRUPT | BE CLEAR SCREEN |
| 46 CHECK ROM COPYRIGHT NOTICE | C0 TRY BOOT WITH INT19 |
| 47 INIT. I20 SUPPORT IF INSTALLED | D0 INTERRUPT HANDLER ERROR |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS | D2 UNKNOWN INTERRUPT ERROR |
| 49 INIT. PCI BUS AND DEVICE | D4 PENDING INTERRUPT ERROR |
| 4A INIT. ALL VIDEO BIOS ROM | D6 SHUTDOWN 5 |
| 4C SHADOW VIDEO BIOS ROM | D8 SHUTDOWN ERROR |
| 50 DISPLAY CPU TYPE AND SPEED | DA EXTENDED BLOCK MOVE |
| 52 TEST KEYBOARD | DC SHUTDOWN 10 |
| 54 SET KEYCLICK IF ENABLED | E0 ENABLE NMI |
| 56 ENABLE KEYBOARD | 90 INIT. HDD CONTROLLER |
| 58 TEST FOR UNEXPECTED INTERRUPTS | 91 INIT. LOCAL BUS HDD CONTROLLER |
| 5A DISPLAY "PRESS SETUP" | 92 JUMP TO USER PATCH 2 |
| 5C TEST RAM BETWEEN 512K AND 640K | 94 DISABLE A20 ADDRESS LINE |
| 60 TEST EXTENDED MEMORY | 96 CLEAR HUGE ES SEGMENT REG. |
| 62 TEST EXTENDED MEMORY ADDRESS LINE | 98 SEARCH FOR OPTION ROMS |
| 64 JUMP TO USER PATCH 1 | |

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	FWH		PART NO.
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	29	BA41-00809/810A

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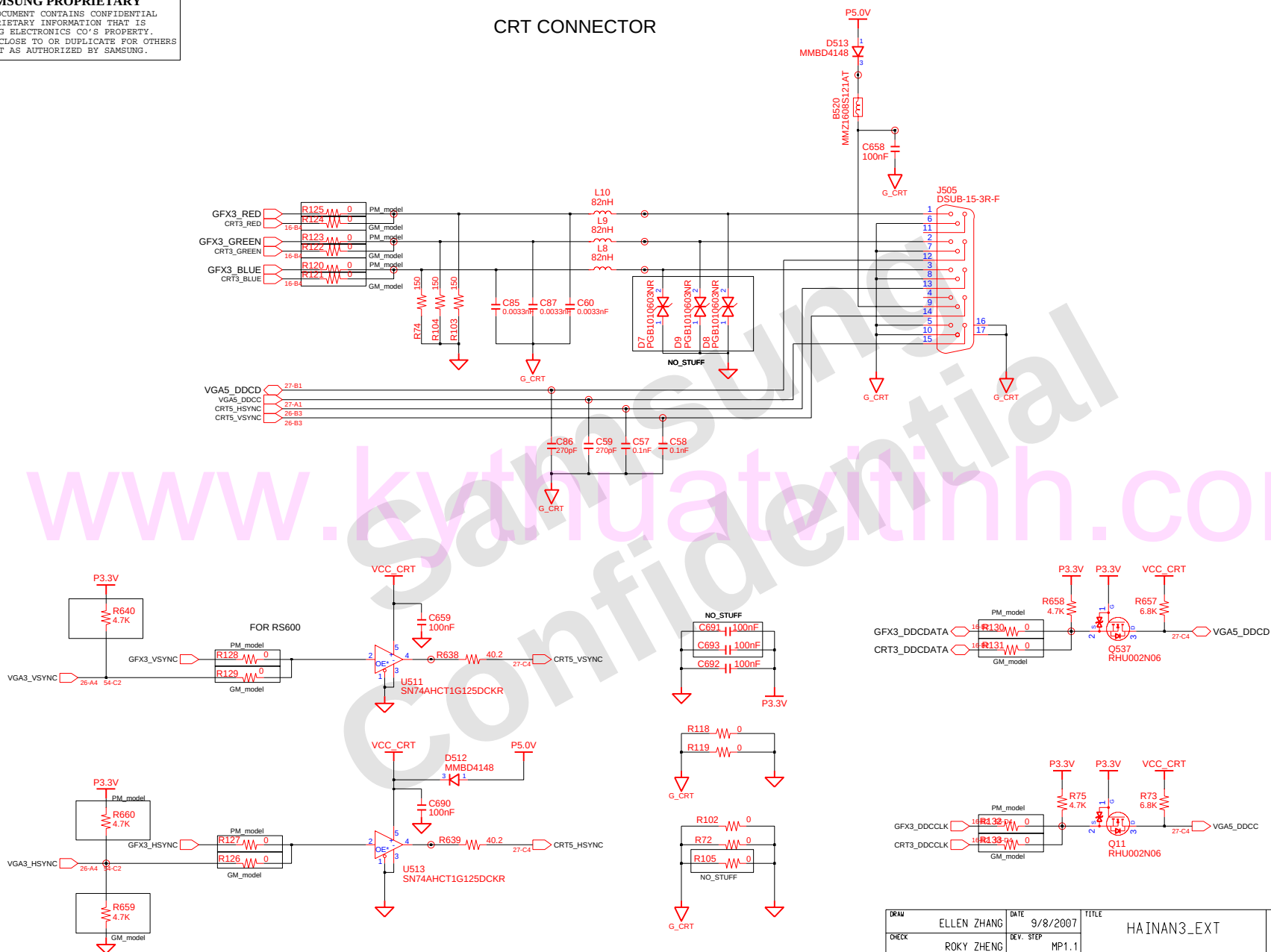


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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	LCD		
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	30 OF 53	

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CRT CONNECTOR



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		CRT	
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	31 OF 53	

[illegible]

DATE	9/8/2007	TITLE	HAINAN3_EXT		SAMSUNG ELECTRONICS	
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	4 IN 1 CARD	PART NO.	BA41-00809/810A
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM		PAGE	32 OF 53

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The schematic diagram illustrates the J511 Edge-Xpress-26P board's connections. It features a USB3 P4 connector (pins 23-C2, 23-C2, 30-A2, 55-D4, 8, 8, 23-A1, 23-C3, 30-A2, 55-D4, 30-A2, 54-C2, 9-B1, 9-B1, 14-B3, 14-B3, 14-B2, 14-B2) and a USB3 P+ connector (pins 23-C2, 23-C2, 30-A2, 55-D4, 8, 8, 23-A1, 23-C3, 30-A2, 55-D4, 30-A2, 54-C2, 9-B1, 9-B1, 14-B3, 14-B3, 14-B2, 14-B2). The board is powered by a 3.3V EXP and 1.5V EXP supply, with decoupling capacitors (C957, C954, C958, C956, C957, C954, C958, C956, C957, C954, C958, C956) connected to ground. The I2C interface is connected to the J511 connector (pins 23-C2, 23-C2, 30-A2, 55-D4, 8, 8, 23-A1, 23-C3, 30-A2, 55-D4, 30-A2, 54-C2, 9-B1, 9-B1, 14-B3, 14-B3, 14-B2, 14-B2) and the J511 connector (pins 23-C2, 23-C2, 30-A2, 55-D4, 8, 8, 23-A1, 23-C3, 30-A2, 55-D4, 30-A2, 54-C2, 9-B1, 9-B1, 14-B3, 14-B3, 14-B2, 14-B2). The I2C interface is connected to the J511 connector (pins 23-C2, 23-C2, 30-A2, 55-D4, 8, 8, 23-A1, 23-C3, 30-A2, 55-D4, 30-A2, 54-C2, 9-B1, 9-B1, 14-B3, 14-B3, 14-B2, 14-B2) and the J511 connector (pins 23-C2, 23-C2, 30-A2, 55-D4, 8, 8, 23-A1, 23-C3, 30-A2, 55-D4, 30-A2, 54-C2, 9-B1, 9-B1, 14-B3, 14-B3, 14-B2, 14-B2).

Type 1 module

Dimensions: 34.00 mm W, 75.00 mm L, 5.00 mm H.

Calculation:

$$\begin{array}{r} 34.00 \text{ mm W} \\ \times \\ 75.00 \text{ mm L} \\ \times \\ 5.00 \text{ mm H} \end{array}$$

Type 2 module

Dimensions: 54.00 mm W, 75.00 mm L, 5.00 mm H.

Calculation:

$$\begin{array}{r} 54.00 \text{ mm W} \\ \times \\ 75.00 \text{ mm L} \\ \times \\ 5.00 \text{ mm H} \end{array}$$

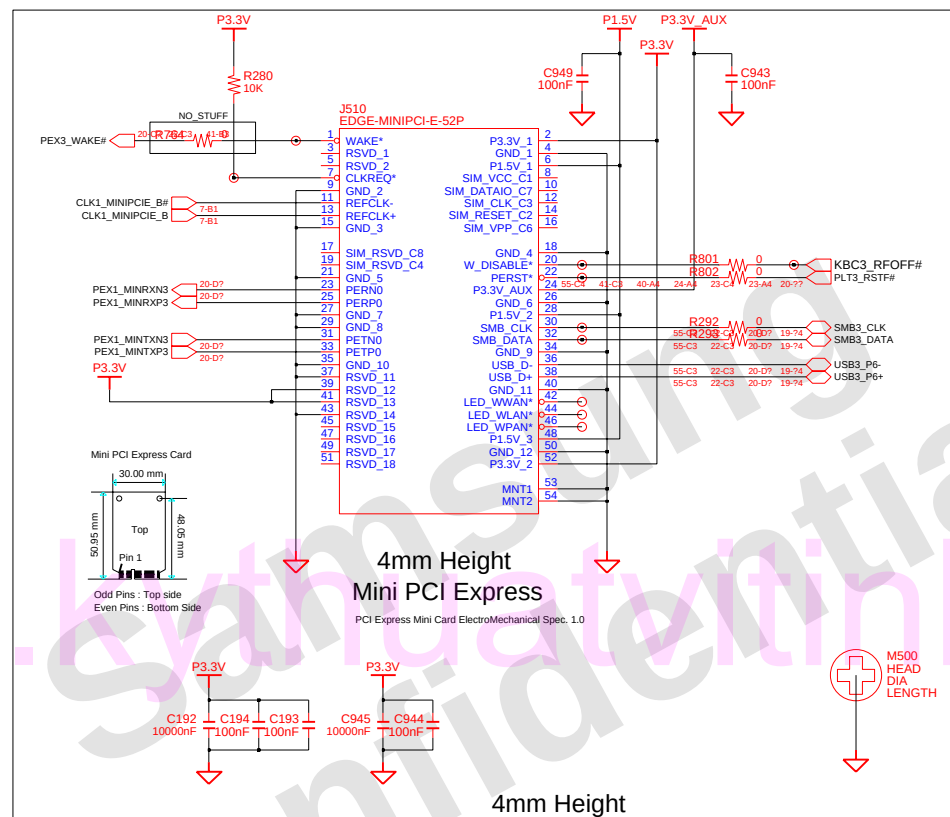
J6
EXPRESS-26P-FRAME

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS		
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APPROVAL	KEVIN LEE	REV	1.0					
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM				PAGE	33
				EXPRESS CARD	PART NO.	BA41-00809/810A		

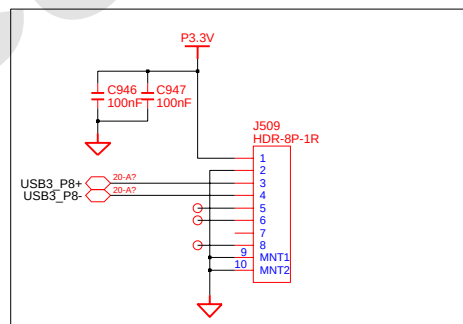
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MINI CARD



Bluetooth Interface



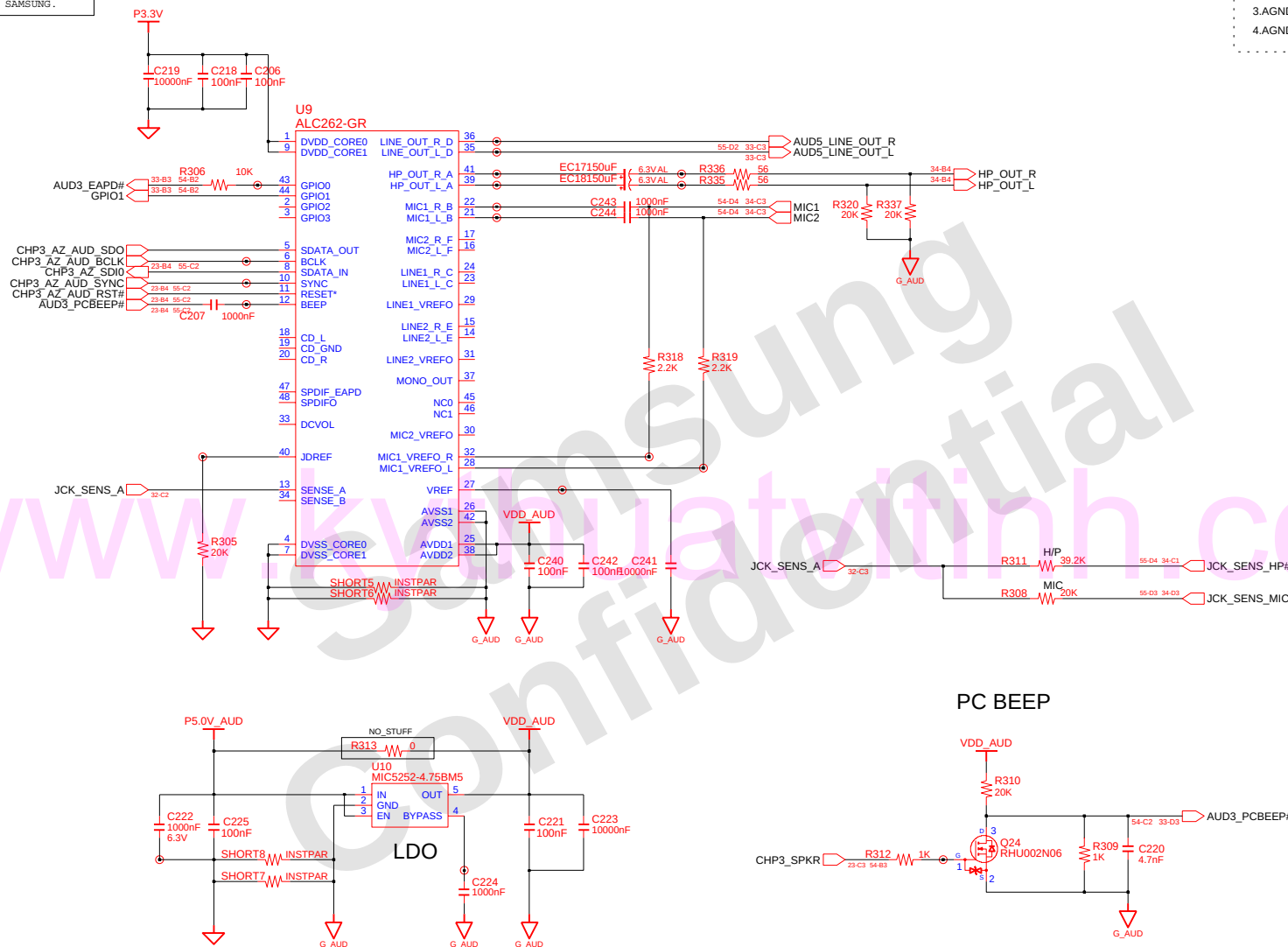
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APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	34	OF 53

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- 1.AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
- 3.AGND_MIC IS MIC GROUND
- 4.AGND_CHS IS CHASS GROUND

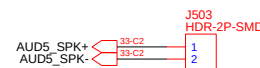
ALL TYPE IS 1608



PC BEEP

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		AUDIO(1/3)	
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	35 OF 53	

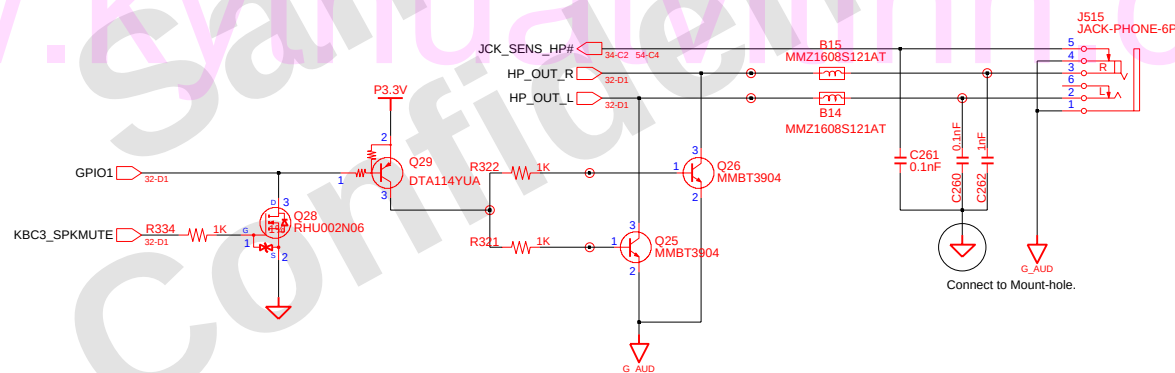
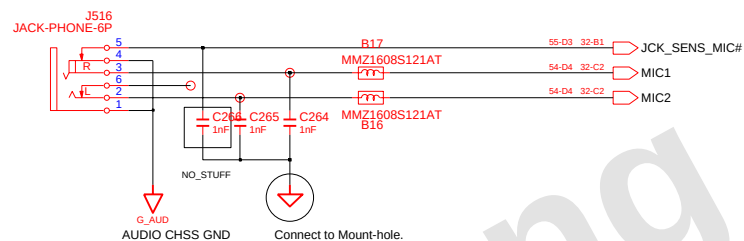
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DRWN	ELLEN ZHANG	DATE	9/8/2007	TITLE		HAINAN3_EXT		SAMSUNG ELECTRONICS	
CHECK	ROKY ZHENG	DEV. STEP	MP1.1						
APPROVAL	KEVIN LEE	REV	1.0	AUDIO(2/3)		PART NO.		BA41-00809/810A	
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM			PAGE	36	OF	53

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HEADPHONE



The traces led to Audio Jacks have the width over 10mil

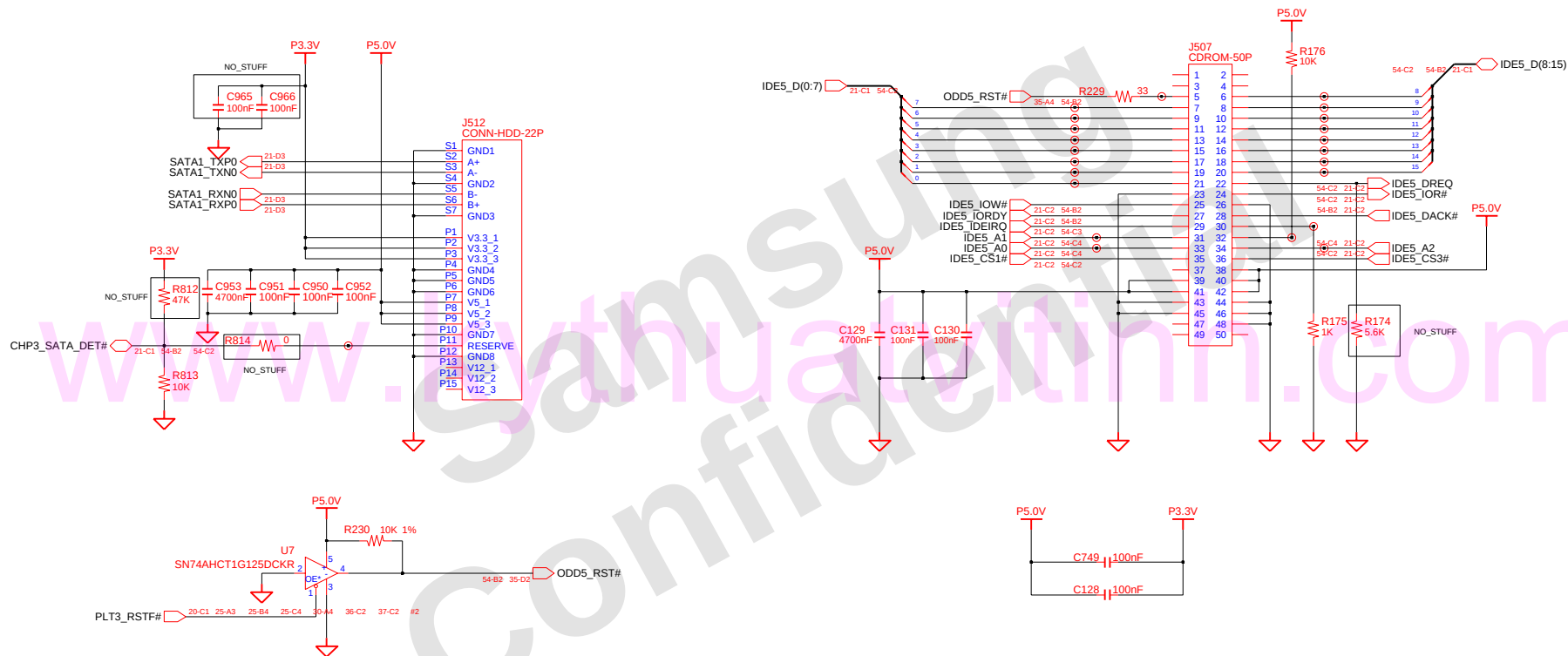
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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	AUDIO(3/3)	PART NO.	BA41-00809/810A
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM		PAGE	37 OF 53

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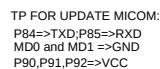
Main to HDD

Main to ODD



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	HDD & ODD		
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	38 OF 53	

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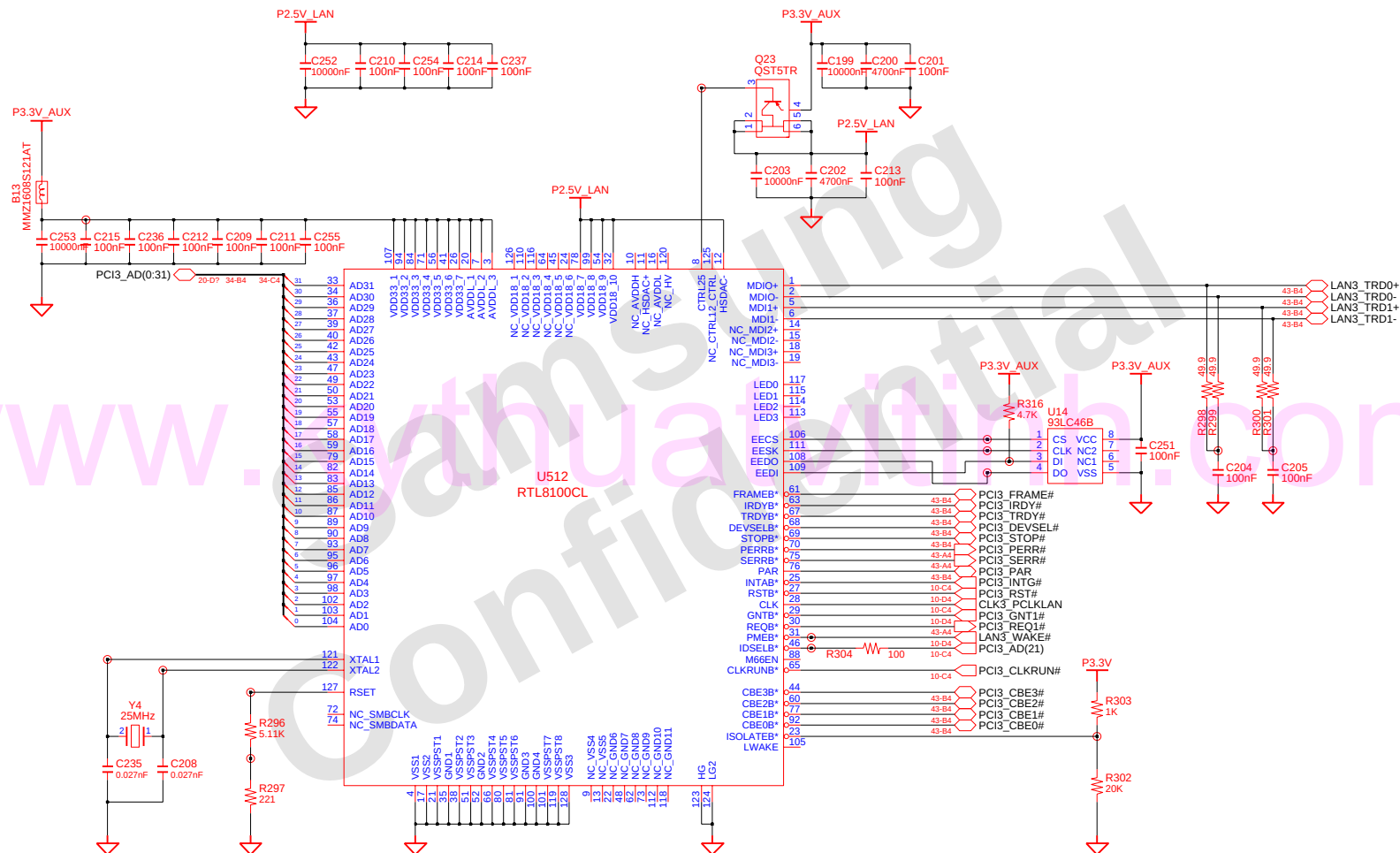


DATE	9/8/2007	TITLE	HAINAN3_EXT		SAMSUNG	
CHECK	ROKY ZHENG	DEV. STEP	MP1.1		ELECTRONICS	
APPROVAL	KEVIN LEE	REV	1.0		PART NO.	
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM		BA41-00809/810A	
			PAGE	39	OF 53	

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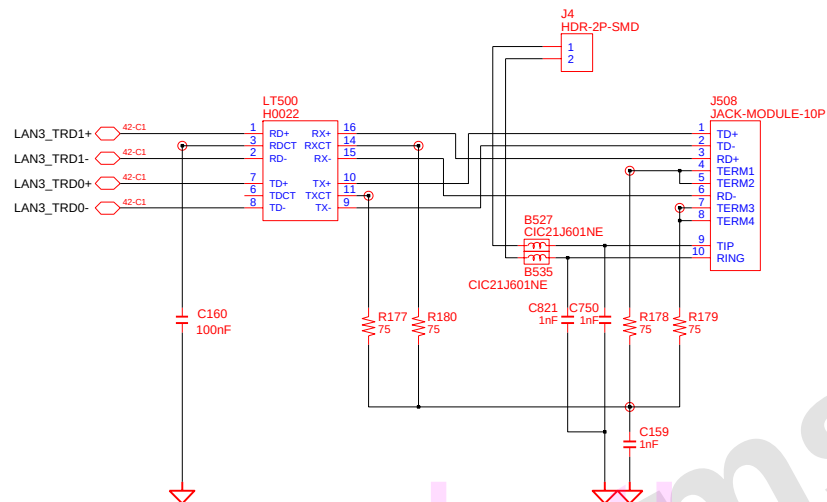
LAN Controller (Only 10/100M)



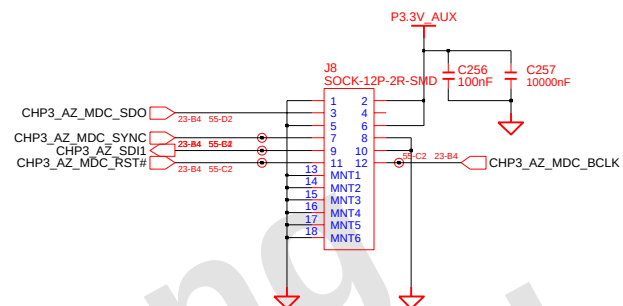
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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	LAN		PART NO. BA41-00809/810A
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	40	OF 53

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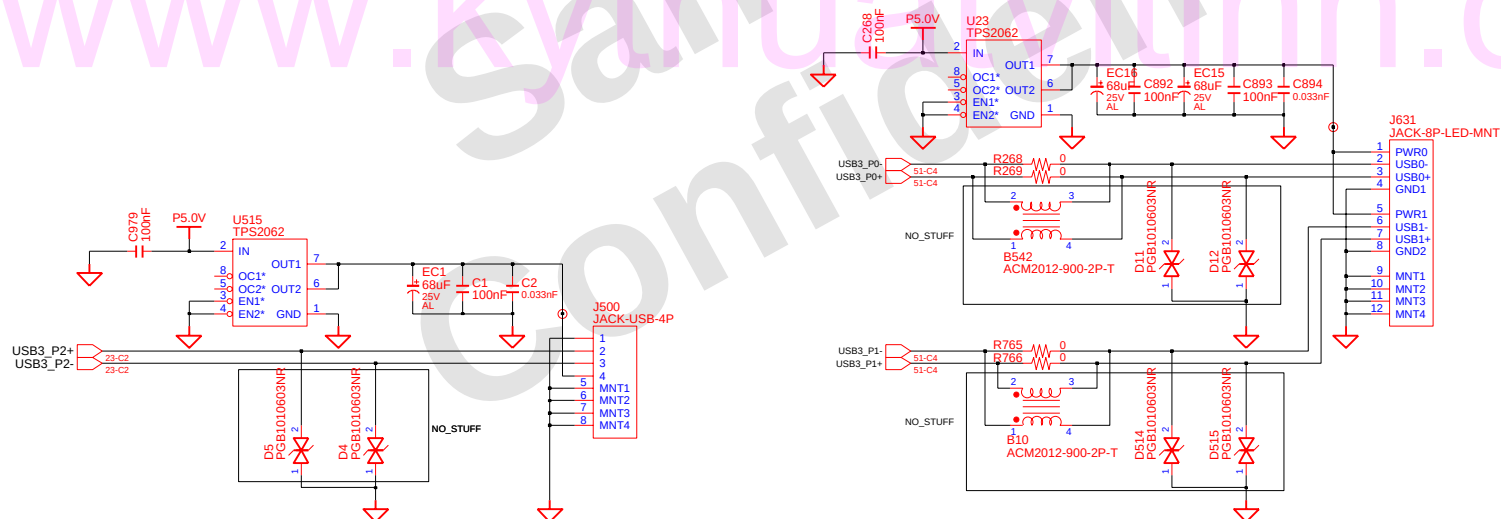
LAN Connector



MDC Connector



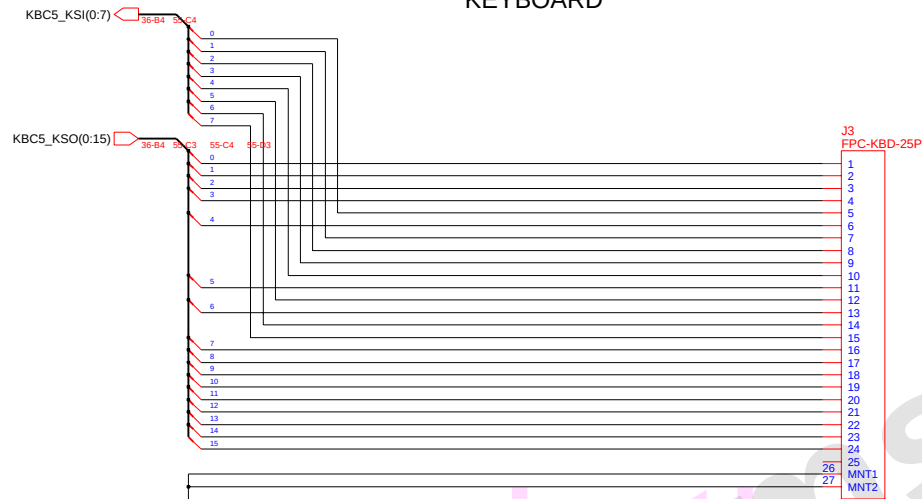
USB Connector



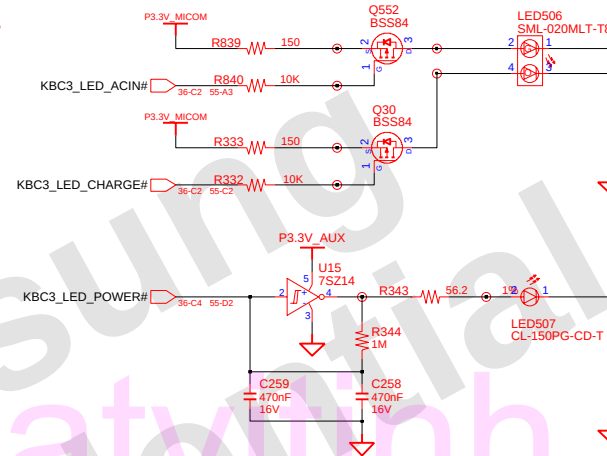
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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	LAN & MDC & USB		
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	41 OF 53	

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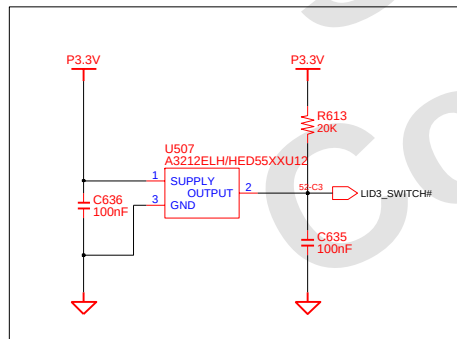
KEYBOARD



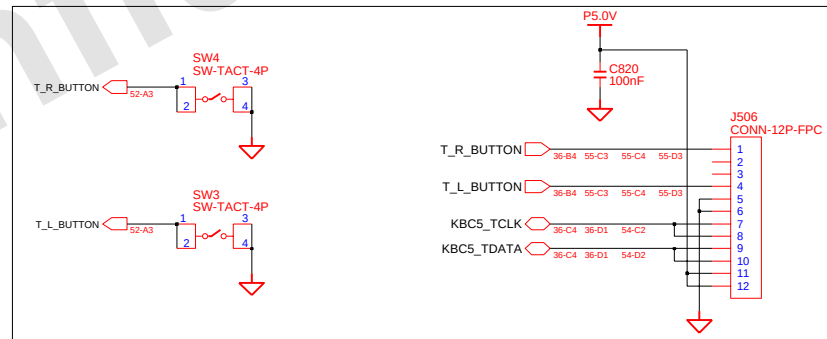
ADAPTERIN/CHARGING LED



LID SWITCH



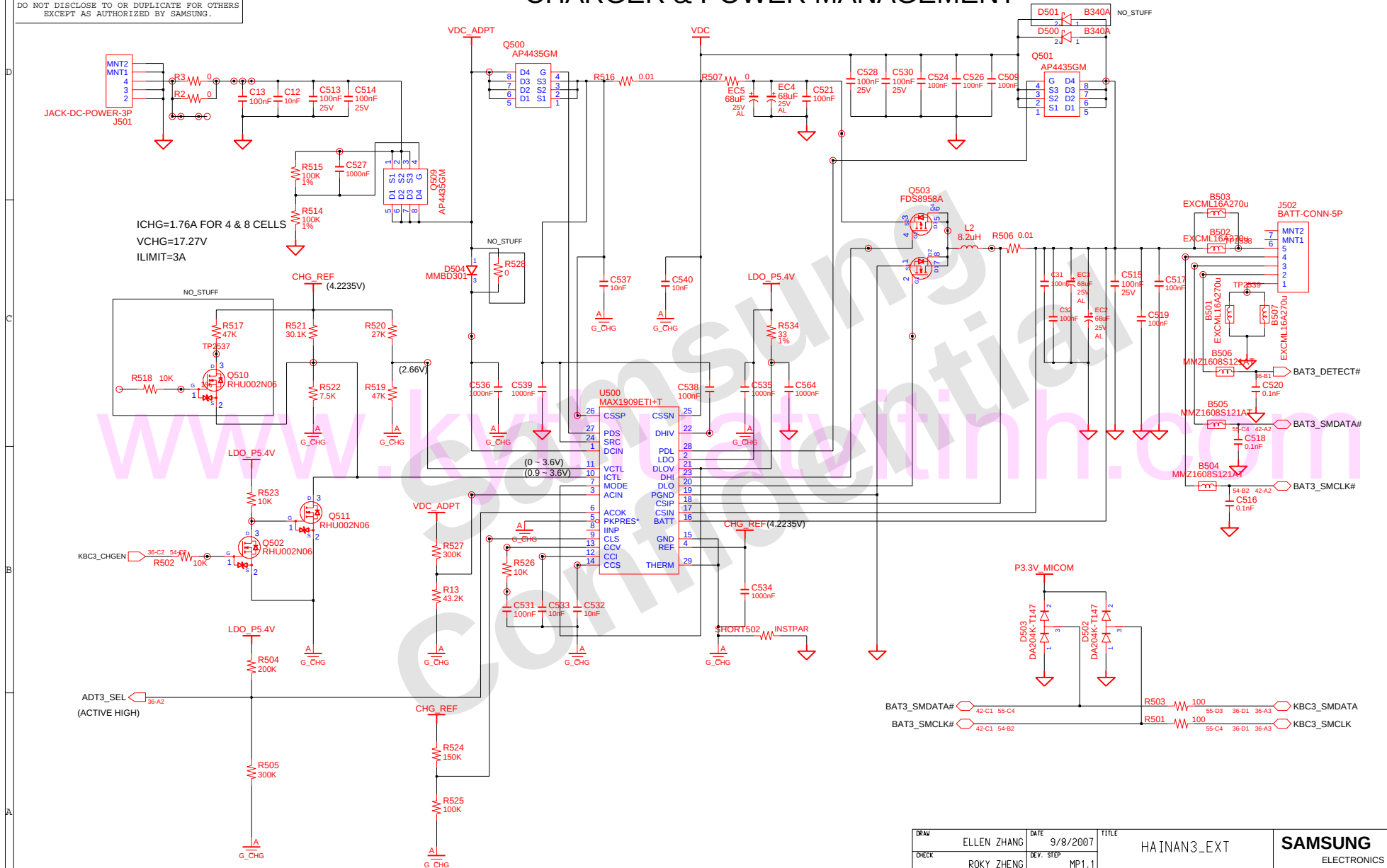
TOUCHPAD



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	BOARD CONN		
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	42 OF 53	

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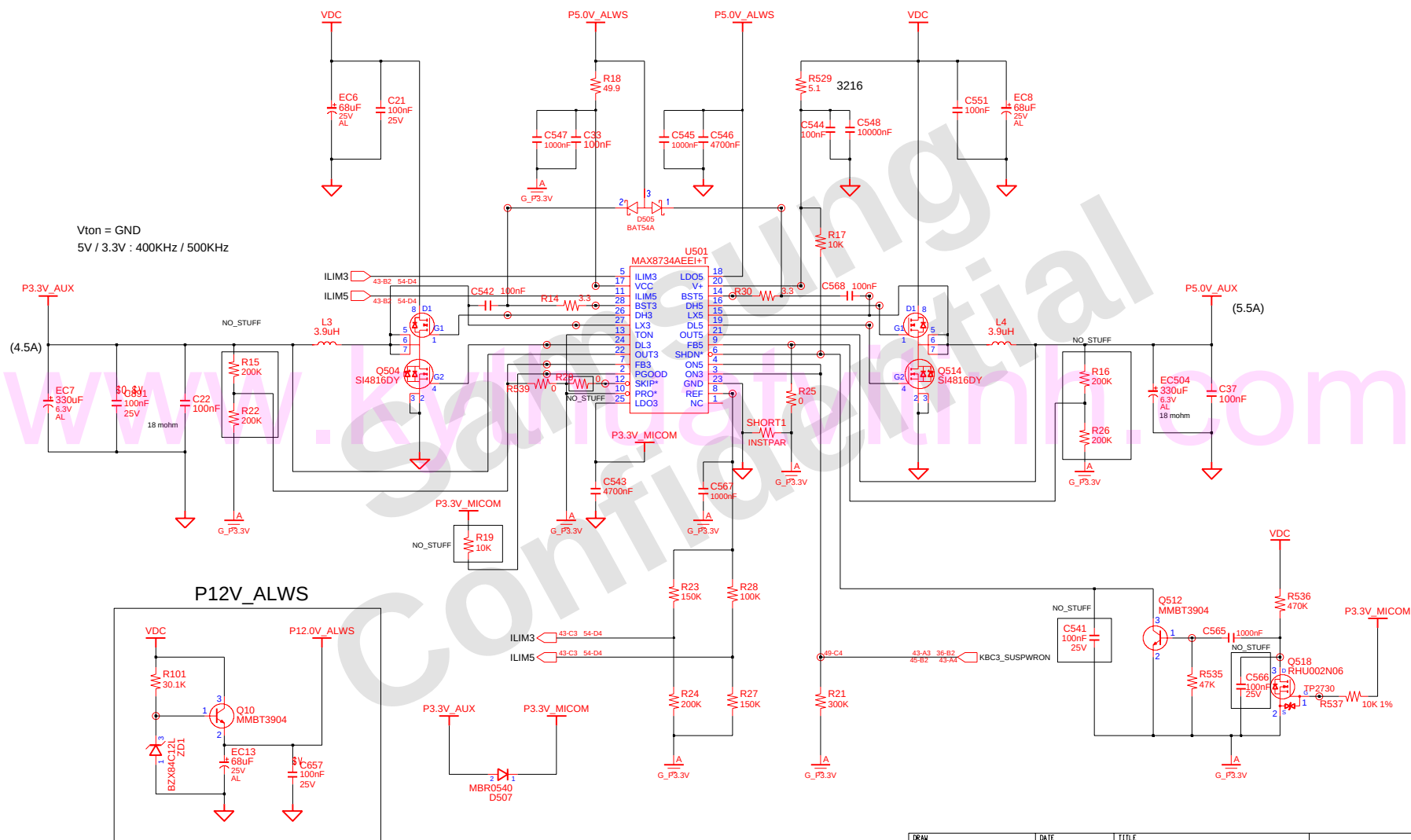
CHARGER & POWER MANAGEMENT



DATE	9/8/2007	HAINAN3_EXT	SAMSUNG ELECTRONICS		
CHECK	ROKY ZHENG			DEV. STEP	MP1.1
APPROVAL	KEVIN LEE			REV	1.0
MODULE CODE	undefined			LAST EDIT	September 8, 2007 12:02:16 PM
			PAGE 43 OF 53		

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P3.3V_AUX & P5V_AUX

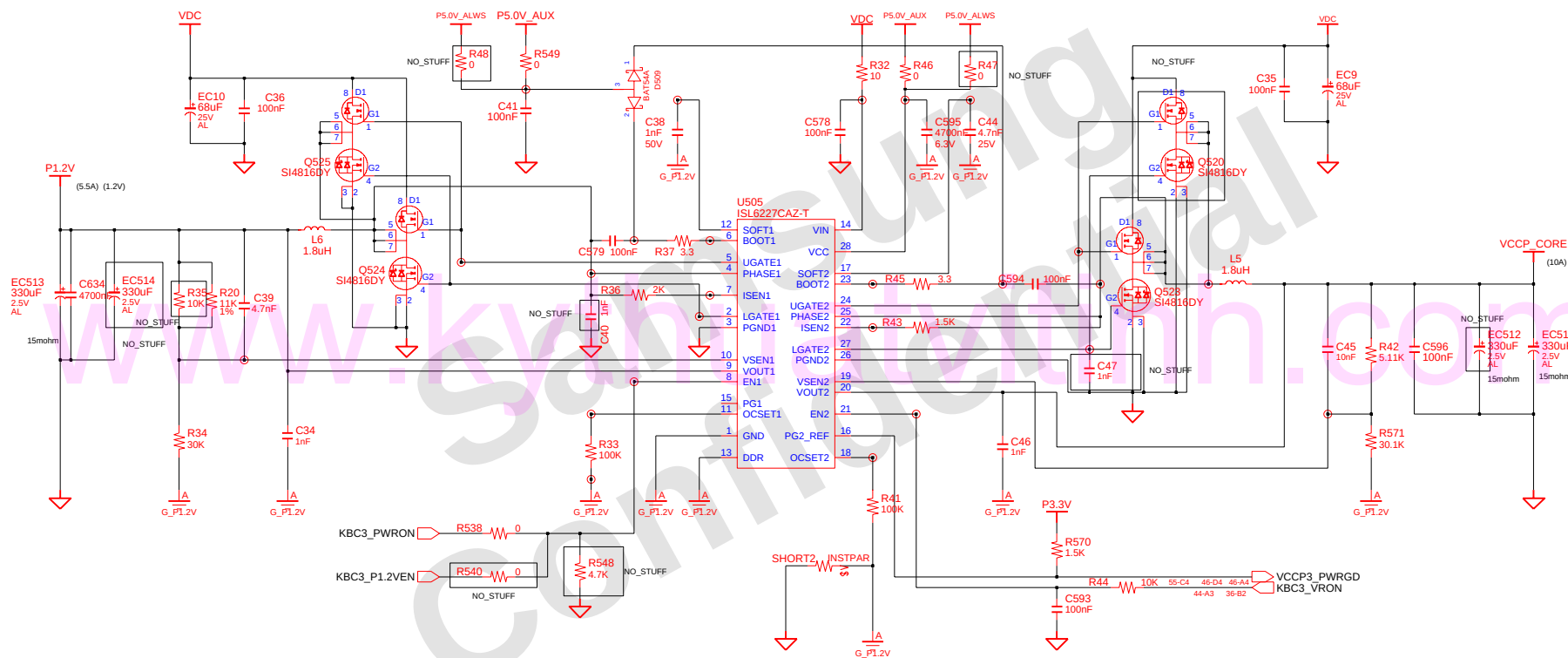


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG	
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			ELECTRONICS	
APPROVAL	KEVIN LEE	REV	1.0	P3.3V_AUX & P5V_AUX		PART NO.	BA41-00809/810A
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM			PAGE	44 OF 53

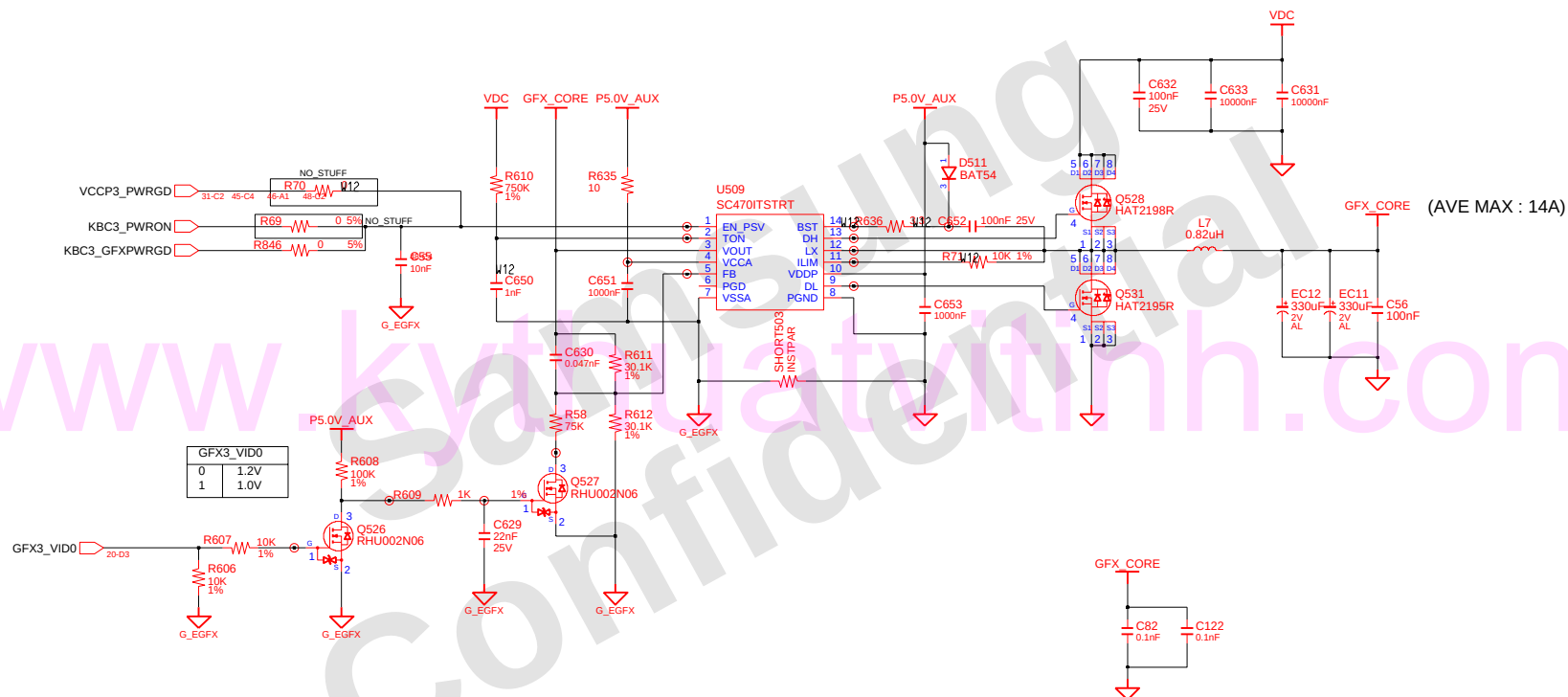
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P1.2V & VCCP_CORE(1.05V)



Graphic Core Power



DRAW	ELLEN ZHANG	DATE	9/8/2007	HAINAN3_EXT MAIN GFX_CORE	SAMSUNG ELECTRONICS					
CHECK	ROKY ZHENG	DEV. STEP	MP1.1							
APPROVAL	KEVIN LEE	REV	1.0		PART NO.	BA41-00809/810A				
MODULE CODE		LAST EDIT			September 8, 2007 12:02:16 PM		PAGE	46	OF	53

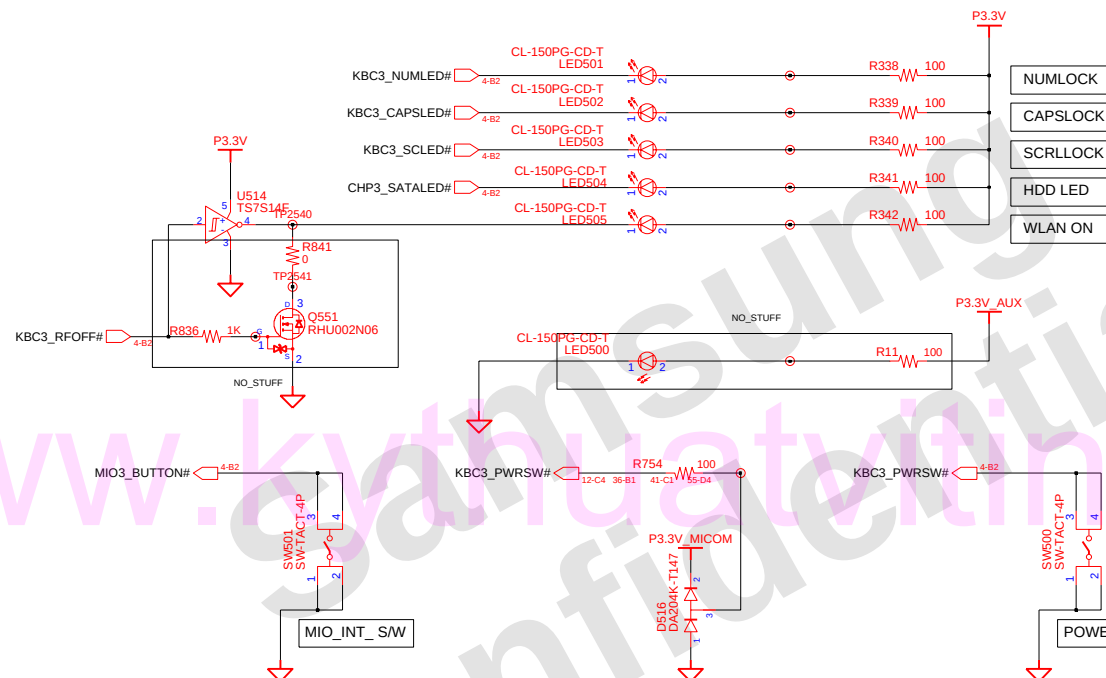
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DATE	9/8/2007	TITLE	HAINAN3_EXT		SAMSUNG ELECTRONICS	
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	DDR2 POWER	PART NO.	BA1A-00809/810A
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM		PAGE	47 OF 53

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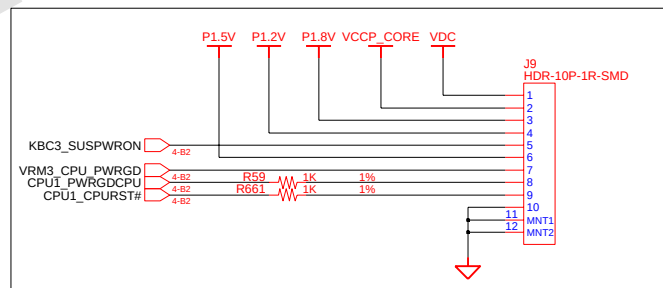
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LED 0801-002195



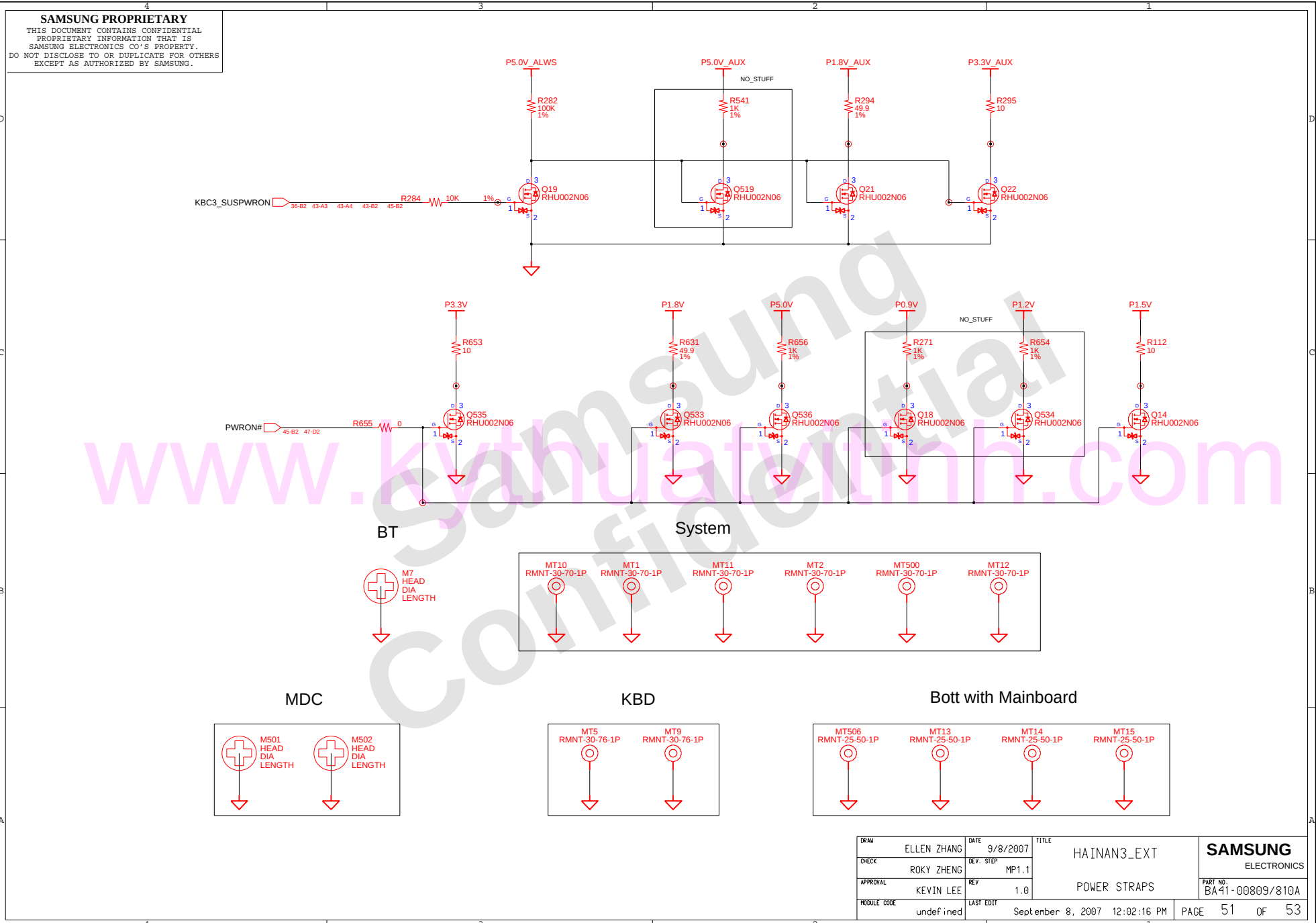
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TP2544	C501	0.01nF	TP2546
TP2545	C502	0.018nF	TP2547
TP2546	C503	0.022nF	TP2548
TP2547	C504	0.027nF	TP2549
TP2548	C505	0.033nF	TP2550
TP2549	C506	0.047nF	TP2551
TP2550	C508	0.068nF	TP2552
TP2551	C500	0.0033nF	TP2553

ICT



ICT/JIG

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	POWER SWITCH		PART NO.
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	50	BA41-00809/810A



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TP2027MIC1 TP2028MIC2 TP2029GPIO1 TP2030ILIM3 TP2031ILIM5	TP2020CPU1_TDI TP2021CPU1_TMS TP2022PCI3_PAR TP2023SATA1_X1 TP2024SMB3_CLK TP2025SPI3_CLK TP2026SPI3_CS#	TP1968CPU1_A20M#	TP1888KBC5_KSO(0) TP1889KBC5_KSO(1) TP1890KBC5_KSO(2) TP1891KBC5_KSO(3) TP1892KBC5_KSO(4) TP1893KBC5_KSO(5) TP1894KBC5_KSO(6) TP1895KBC5_KSO(7) TP1896KBC5_KSO(8) TP1897KBC5_KSO(9)																											
TP2637OSMB3_DATA1		TP1939PCI3_CBE0# TP1940PCI3_CBE1# TP1941PCI3_CBE2# TP1942PCI3_CBE3# TP1943PCI3_GNT1#																												
TP2638VGA3_HSYNC TP2639VGA3_VSYNC TP2640GFX_CORE TP2641GFX_CORE TP2642GFX_CORE TP2643GFX_CORE TP2644GFX_CORE TP2645GFX_CORE TP2646GFX_CORE TP2647GFX_CORE TP2648OP2_5V TP2649OP2_5V TP2650OP2_5V TP2651OP2_5V	TP2002CHP3_SPKR	TP1945PCI3_IRDY# TP1946PCI3_PERR# TP1947PCI3_REQ1# TP1914PCI3_RST# TP1915PCI3_SERR# TP1916PCI3_STOP# TP1917PCI3_TRDY#	TP1898LCD3_BKLTON TP1899LPC3_LAD(0) TP1900LPC3_LAD(1) TP1869LPC3_LAD(2) TP1870LPC3_LAD(3) TP1871MCD3_MSINS#																											
	TP2006CPU1_INTR TP2007CPU1_PSI#	TP1977CPU1_FERR# TP1979CPU1_INIT#																												
	TP2011CPU1_SLP# TP2012CPU1_SM# TP2013IDES_CS1# TP2014IDES_CS3#	TP1950CPU1_TRST# TP1951EXP3_CPPE#	TP1918PEX3_WAKE# TP1919PLT3_RST#																											
	TP1980IDES_DREQ TP1981IDES_IOR# TP1982IDES_IOW# TP1983KBC3_A20G TP1984KBC3_RST# TP1985KBC3_VRON TP1986KBC3_TCLK	TP1952IDES_DACK# TP1953IDES_IORDY TP1954JCK_SENS_A TP1955KBC3_CHGEN TP1956KBC3_SMCLK TP1957KBC3_TDATA	TP1920OT_L_BUTTON TP1921OT_R_BUTTON																											
TP2621MEM1_BRAS# TP2622MEM1_BWE#		TP1924BAT3_SMCLK# TP1925CHP3_OVERT# TP1910CHP3_SBPME# TP1911CHP3_SERIRQ TP1912CHP3_SLPS3# TP1913CHP3_SLPS5#																												
TP2633LCD3_BKLTCTRL TP2634LCD3_BKLTEN TP2635LCD3_EDIO_CLK TP2636LCD3_VDDEN	TP1996ODDS_RST#	TP1902CPU1_DPSLP# TP1903CPU1_IGNNE# TP1904CPU1_VID(0) TP1905CPU1_VID(1) TP1906CPU1_VID(2) TP1907CPU1_VID(3) TP1908CPU1_VID(4) TP1909CPU1_VID(5) TP1872CPU1_VID(6) TP1873EXP3_CPUSB# TP1874EXP3_PERST# TP1875IDES_IDEIRQ TP1876KBC3_L8VEN# TP1877KBC3_PWRSW# TP1878KBC3_SCLED# TP1879KBC3_SMDATA TP1880KBC5_KSI(0) TP1881KBC5_KSI(1) TP1882KBC5_KSI(2) TP1883KBC5_KSI(3) TP1884KBC5_KSI(4) TP1885KBC5_KSI(5) TP1886KBC5_KSI(6) TP1887KBC5_KSI(7)																												
TP2623GFX3_BKLTEN TP2624GFX3_THRMTRIP# TP2625GFX3_VID0																														
TP2629GPIO<13> TP2630GPIO<5> TP2631KBC3_BKLTEN TP2632KBC3_P1_2VEN	TP1997SMB3_DATA TP1998SPI3_MISO TP1999SPI3_MOSI TP2000AUD3_EAPD#																													
TP2015RTC_CLK TP2016AC_SDOUT TP2017AUTO_ON# TP2018CPU1_NMI TP2019CPU1_TCK	TP2001CLK3_NB14M																													
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DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS																								
CHECK	ROKY ZHENG	DEV. STEP	MP1.1																											
APPROVAL	KEVIN LEE	REV	1.0	TP		PART NO. BA41-00809/810A																								
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM		PAGE	52 OF 53																								

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TP2233○PCI3_FRAME#

TP2235○VCCP3_PWRGD
TP2236○AUD3_PCBEEP#
TP2237○BAT3_DETECT#
TP2238○BAT3_SMDATA#
TP2239○CHP3_AZ_SD0
TP2240○CHP3_BIOSWP#
TP2241○CHP3_CPUSTP#

TP2223○CPU1_STPCLK#

TP2225○ITP3_SYSRST#
TP2226○JCK_SENS_HP#
TP2227○KBC3_CPURST#
TP2228○KBC3_EXTSMI#
TP2229○KBC3_FANCTRL
TP2230○KBC3_NBPWRGD
TP2231○KBC3_NUMLED#
TP2232○KBC3_PWRBTN#
TP2207○KBC3_RSMRST#
TP2208○KBC3_RUNSC#
TP2209○KBC3_SBPWRGD
TP2210○KBC5_KSO(10)
TP2211○KBC5_KSO(11)
TP2212○KBC5_KSO(12)
TP2213○KBC5_KSO(13)
TP2214○KBC5_KSO(14)
TP2215○KBC5_KSO(15)

TP2216○LID3_SWITCH#
TP2217○LPC3_LFRAME#

TP2195○CHP3_DPRSPLVR
TP2196○CHP3_SATALED#

TP2197○CPU1_PROCHOT#
TP2198○CPU1_PWRGDOPU
TP2199○CPU1_VCCSENSE
TP2200○CPU1_VSSSENSE
TP2201○JCK_SENS_MCHP
TP2202○KBC3_CAPSLD#
TP2203○KBC3_WAKESC#

TP2180○CHP3_SATA_DET#

TP2181○CPU1_THRMTRIP#
TP2182○KBC3_CLKPWRGD#
TP2183○KBC3_LED_ACIN#
TP2184○KBC5_CAL_THRM#

TP2186○VRM3_CPU_PWRGD

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TP2189○CHP3_AZ_MDC_SD0

TP2192○KBC3_LED_POWER#

TP2158○CHP3_AZ_AUD_RST#

TP2159○CHP3_SBTHRMTRIP#

TP2162○KBC3_LED_CHARGE#
TP2163○KBC3_THERM_SMCLK

TP2164○KBC3_THERM_SMDATA

TP2193○PCI3_CLKRUN#
TP2194○PCI3_DEVSEL#

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TP2174○G_CHG
TP2175○G_CHG
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TP2178○G_CRT
TP2179○G_CRT

TP2126○G_CRT
TP2127○G_CRT
TP2128○G_DDR
TP2129○G_DDR
TP2130○G_DDR
TP2131○G_DDR
TP2132○G_P3.3V
TP2133○G_P3.3V
TP2134○G_P3.3V
TP2135○G_P3.3V
TP2136○LCD_VDD3V
TP2137○LCD_VDD3V

TP2142○LDO_P5.4V
TP2143○LDO_P5.4V

TP2146○MEM1_VREF
TP2147○MEM1_VREF

TP2148○P0.9V
TP2149○P0.9V
TP2150○P0.9V
TP2151○P0.9V
TP2152○P1.2V
TP2153○P1.2V
TP2154○P1.2V
TP2155○P1.2V
TP2156○P1.5V
TP2157○P1.5V
TP2084○P1.5V
TP2095○P1.5V
TP2096○P1.8V
TP2097○P1.8V
TP2098○P1.8V
TP2099○P1.8V

TP2103○PRTC_BAT

TP2109○P1.5V_EXP
TP2110○P1.5V_EXP
TP2111○P1.5V_EXP
TP2112○P1.8V_AUX
TP2113○P1.8V_AUX
TP2114○P1.8V_AUX
TP2115○P1.8V_AUX
TP2116○P2.5V_LAN
TP2117○P2.5V_LAN
TP2118○P2.5V_LAN
TP2119○P2.5V_LAN

TP2123○P2.5V_MCD
TP2124○P3.3V_AUX
TP2125○P3.3V_AUX
TP2062○P3.3V_AUX
TP2063○P3.3V_AUX

TP2065○P3.3V_EXP
TP2066○P3.3V_EXP

TP2068○P3.3V_MCD
TP2069○P3.3V_MCD
TP2070○P3.3V_MCD
TP2071○P3.3V_MCD
TP2072○P5.0V_AUD
TP2073○P5.0V_AUD
TP2074○P5.0V_AUD
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TP2076○P5.0V_AUD
TP2077○P5.0V_AUD

TP2078○P5.0V_AUX
TP2079○P5.0V_AUX
TP2080○PCIE_VDDR

TP2085○P12V_ALWS
TP2086○P12V_ALWS

TP2089○P5.0V_ALWS
TP2089○P5.0V_ALWS
TP2090○P5.0V_ALWS
TP2091○P5.0V_ALWS
TP2092○P12.0V_ALWS
TP2093○P12.0V_ALWS
TP2032○P12.0V_ALWS
TP2033○P12.0V_ALWS

TP2035○P3.3V_AUX_EXP

TP2037○P3.3V_AUX_EXP
TP2038○VDC
TP2039○VDC
TP2040○VDC
TP2041○VDC

TP2045○VCC_CRT
TP2046○VDC_INV
TP2047○VDC_INV

TP2050○VDD_AMP
TP2051○VDD_AMP
TP2052○VDD_AMP
TP2053○VDD_AMP
TP2054○VDD_AUD
TP2055○VDD_AUD
TP2056○VDD_AUD
TP2057○VDD_AUD
TP2058○VCCP_CORE
TP2059○VCCP_CORE
TP2060○VCCP_CORE
TP2061○VCCP_CORE

TP2656○GPI0(1)

TP2660○KBC3_BKLTON
TP2661○KBC3_P1.2VEN

TP2663○GFX_CORE
TP2664○GFX_CORE
TP2665○GFX_CORE
TP2666○GFX_CORE
TP2667○G_EGFX
TP2668○G_EGFX
TP2669○G_EGFX
TP2670○G_EGFX
TP2671○P2.5V
TP2672○P2.5V
TP2673○P2.5V
TP2674○P2.5V

PCB REVISION CONTROL (ICT)					
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP	
1	N.C.				
2	1-2				
3	2-3				
4	3-1				
5	1-2-3				
6	N.C.				
7	1-2				
8	2-3				
9	3-1				
10	1-2-3				

REV500
1○
2○ 03

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	TP		
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	53 OF 53	