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9. 회로도

9-1. External Graphic

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
	AD21	3	
MiniPCI SLOT1	AD23	2	D,E
USB	AD29(internal)	-	USB2.0 #0 : A
			USB2.0 #1 : D
			USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
		-	A,B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	Northwood-B
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	(Interposer B'd)
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
Highest Freq. 0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V	Lowest Freq.
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V	
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V	
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V	Deeper Sleep
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V	
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V)
	MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

I C / SMB Address

Devices	Address	Hex	Bus
ICH6	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO	
0	SYSTEM PORT A	
1,2	SYSTEM PORT B	
3	BLUETOOTH	OPTION
4	FINGER PRINT	OPTION

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

REVISION HISTORY

See rev notes in the changes file for more information.

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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		
APPROVAL: KIM, DW	REV: 1.0		PART NO. BA41-00451A
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM		PAGE 4 OF 49

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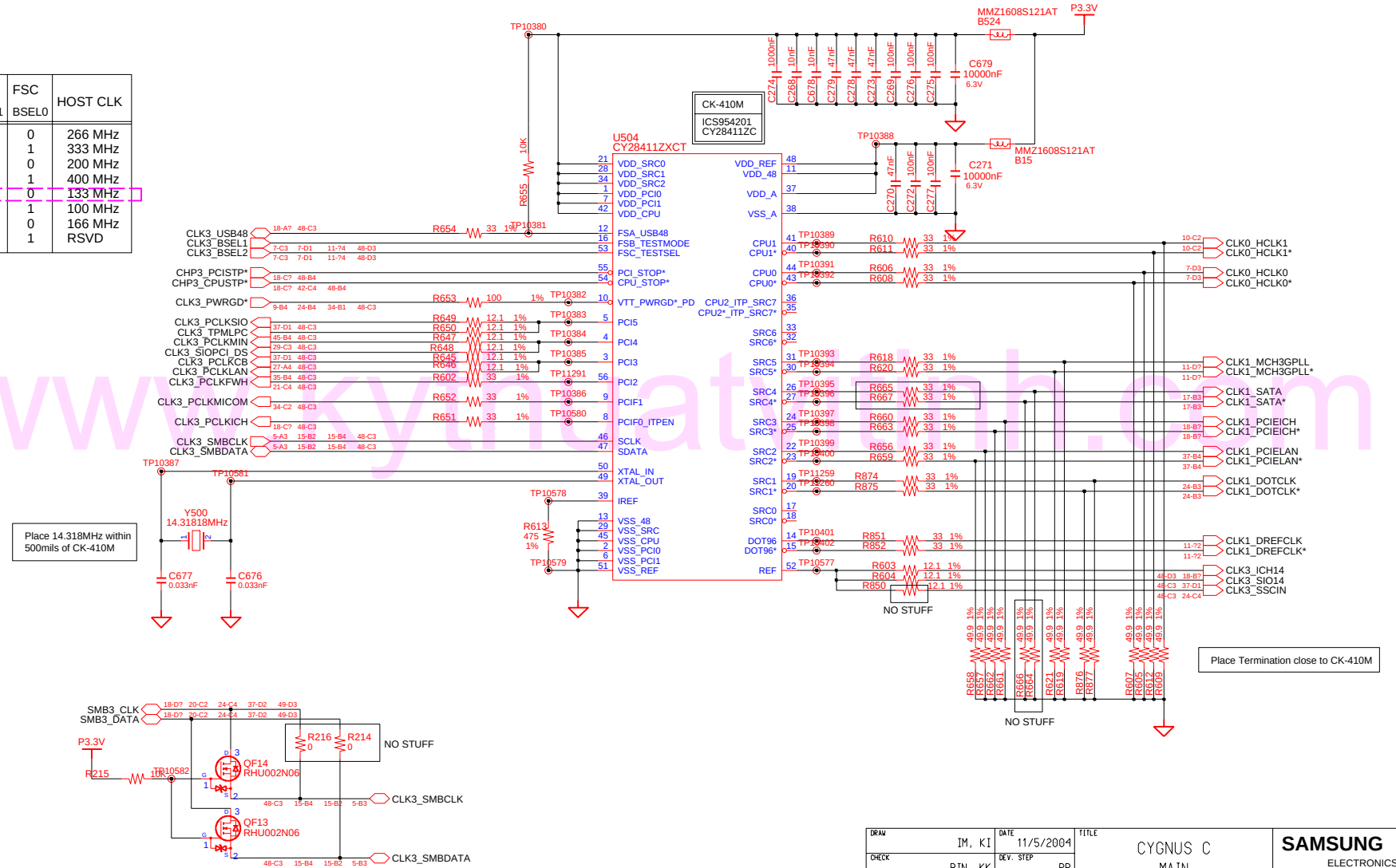
FSA BSEL2	FSB BSEL1	FSC BSEL0	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



DRAW	DATE	TITLE	SAMSUNG ELECTRONICS
IM, KI	11/5/2004	CYGNUS C MAIN CLOCK GENERATOR	
CHECK: BIN, KK	DEV. STEP: PR		
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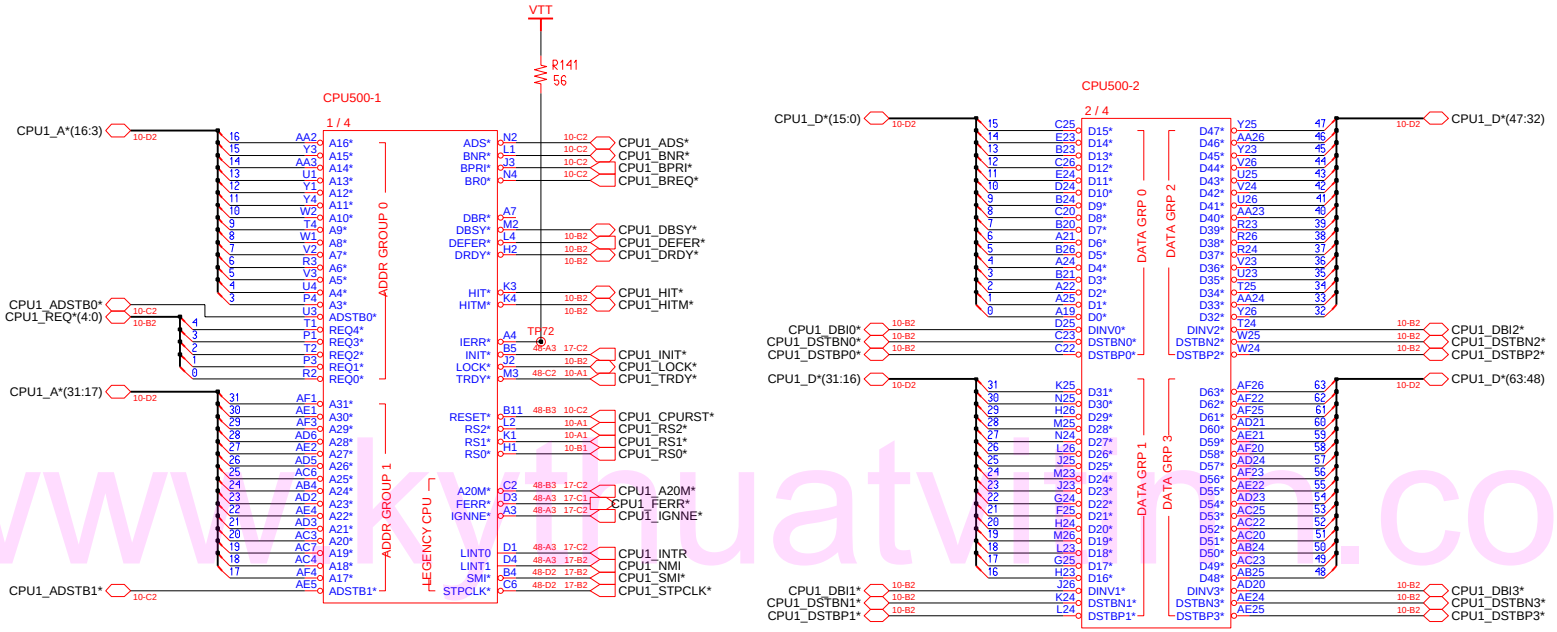

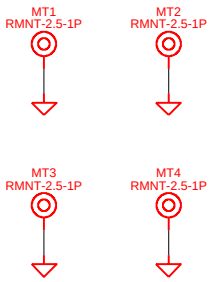

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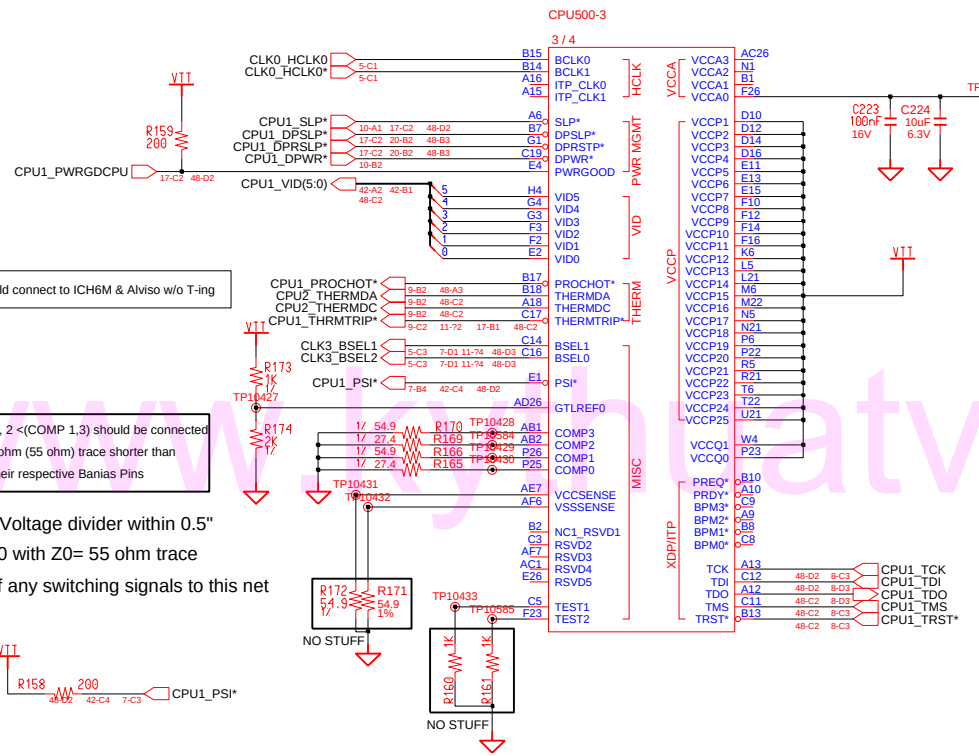
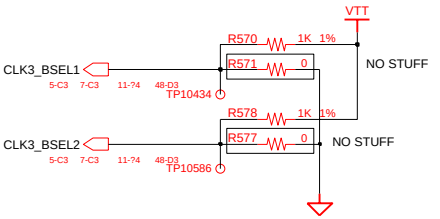


THERTRIP* should connect to ICH6M & Alviso w/o T-ing

COMP 0 , 2 <(COMP 1,3) should be connected Z0=27.4 ohm (55 ohm) trace shorter than 1/2 " to their respective Banias Pins

GTLREF : Keep the Voltage divider within 0.5" of the First GTLREF0 with Z0= 55 ohm trace

Minimize coupling of any switching signals to this net



CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage	
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V	
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V	
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V	
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V	
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V	
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V	
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V	
0 0 0 1 1 1	1.596 V	1 0 0 1 1 1	1.084 V	
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V	
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V	
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V	
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V	
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V	
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V	
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V	
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V	
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V	
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V	
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V	
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V	
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V	
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V	
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V	Lowest Freq.
0 1 0 1 1 1	1.340 V	1 1 0 1 1 1	0.828 V	
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V	
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V	
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V	
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V	
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V	Deeper Sleep
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V	
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V	
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V	

Highest Freq. of Dothan400(1.8GHz)
* Highest Freq. of Dothan533(?? GHz : TBD)

DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN DOTHAN CPU(2/3)	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		
APPROVAL: KIM, DW	REV: 1.0		PART NO. BA41-00451A
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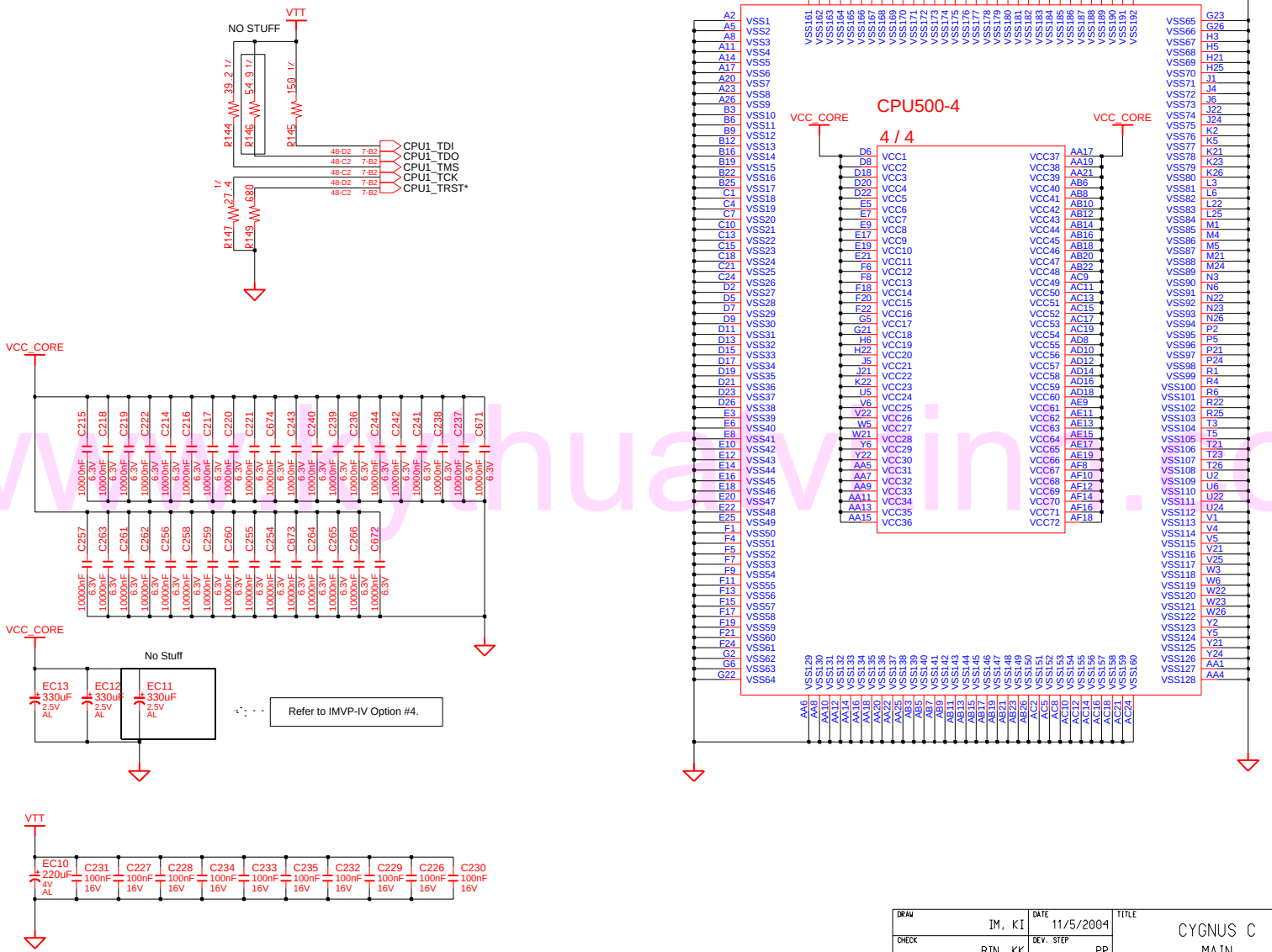
Refer to Sonoma Platform Design Guide(4.6.1.4)



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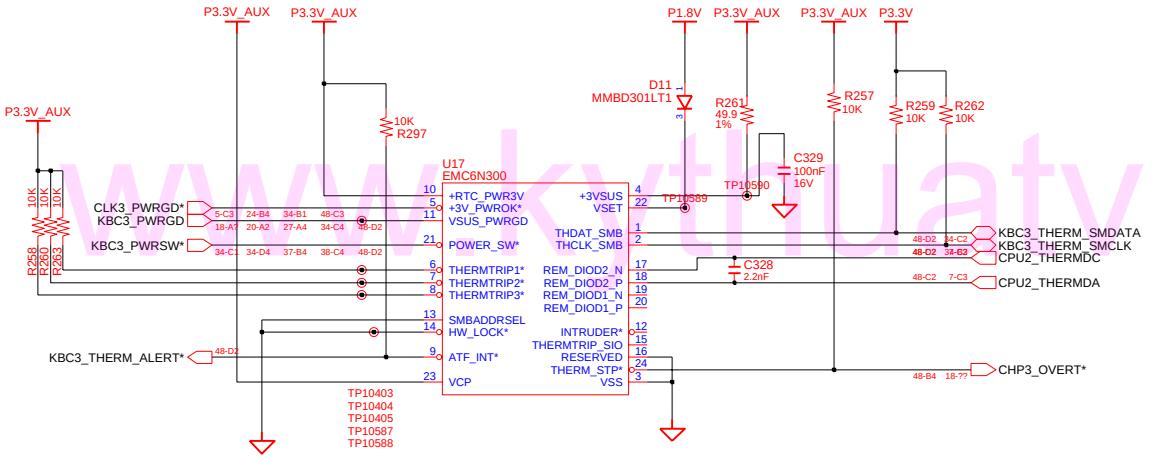
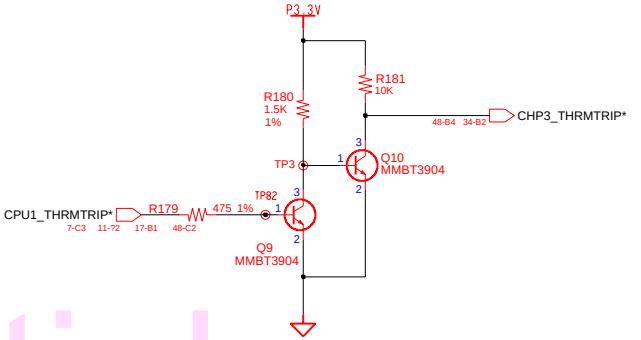
Refer To Thermal Sensor Layout Guidelines.

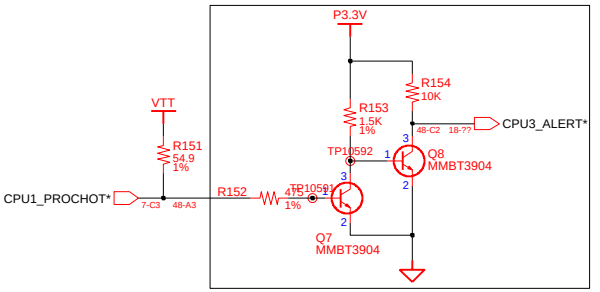
- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

CPU / DDR Thermal Sensor





NO STUFF



DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN THERMAL SENSOR/FAN CONTRL	SAMSUNG ELECTRONICS
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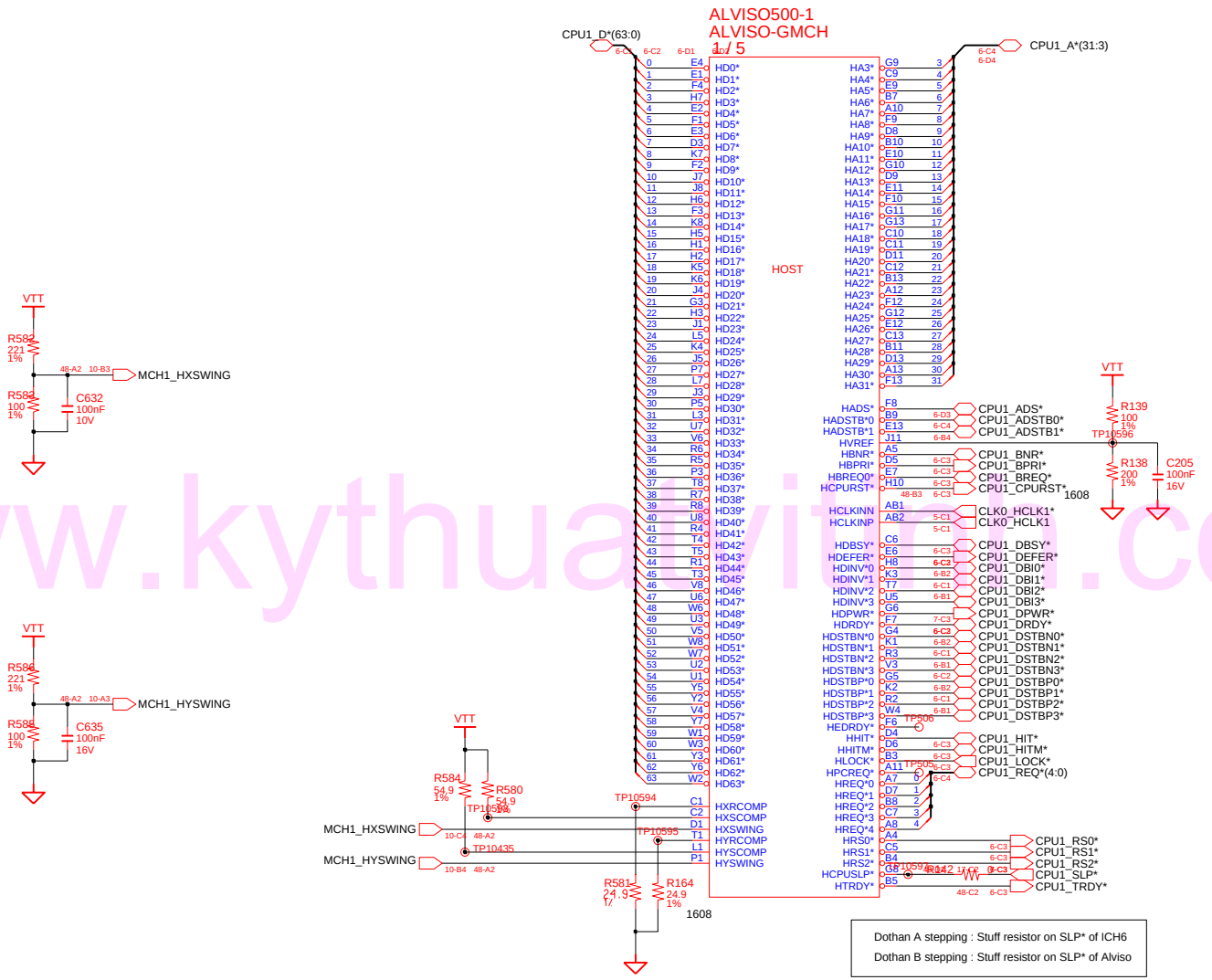

Dothan A stepping : Stuff resistor on SLP* of ICH6

Dothan B stepping : Stuff resistor on SLP* of Alviso

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APPROVAL: KIM, DW	REV: 1.0		
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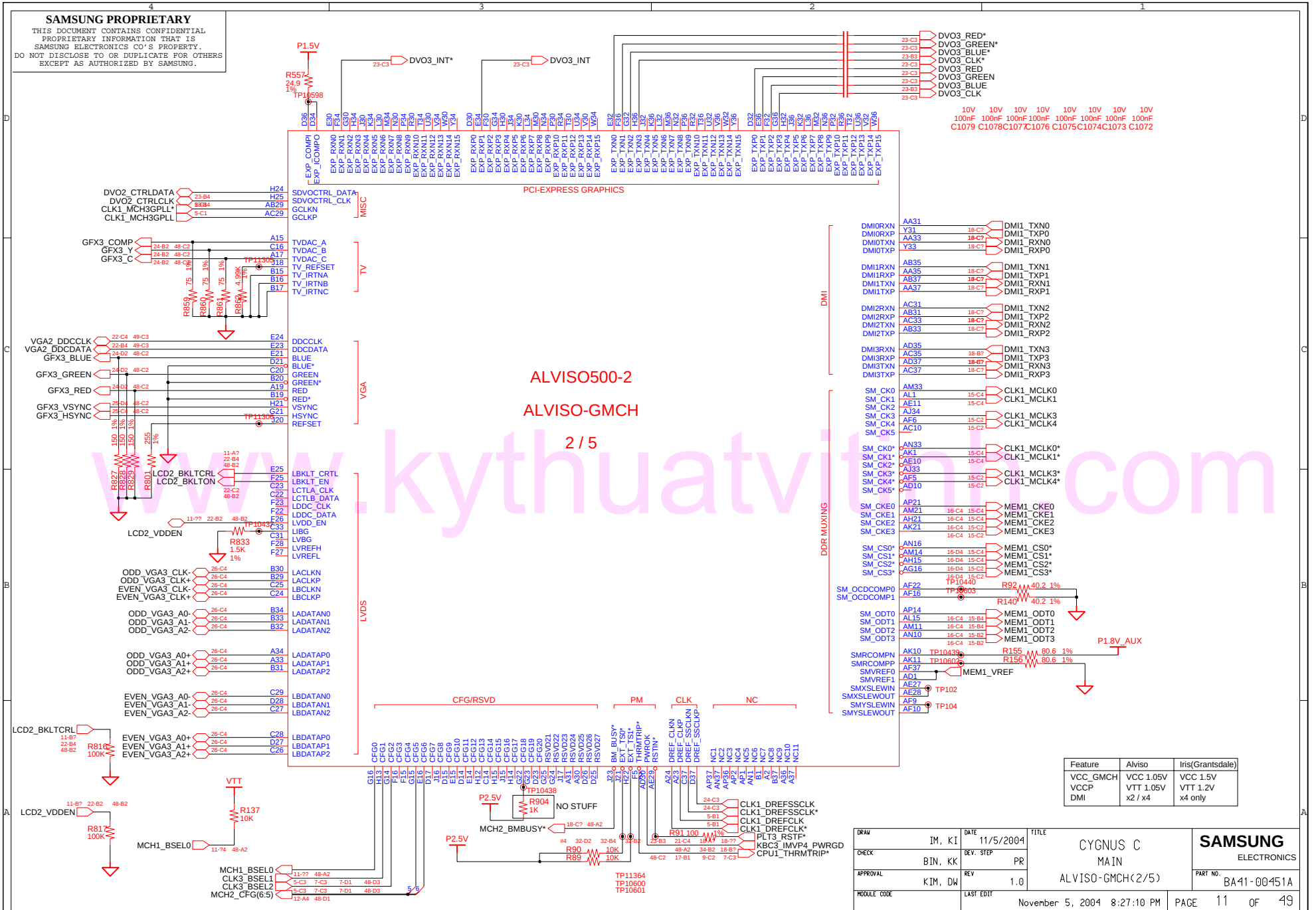

Feature	Alviso	Iris(Grantsdale)
VCC_GMCH	VCC 1.05V	VCC 1.5V
VCCP	VTT 1.05V	VTT 1.2V
DMI	x2 / x4	x4 only

DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN ALVISO-GMCH(2/5)	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
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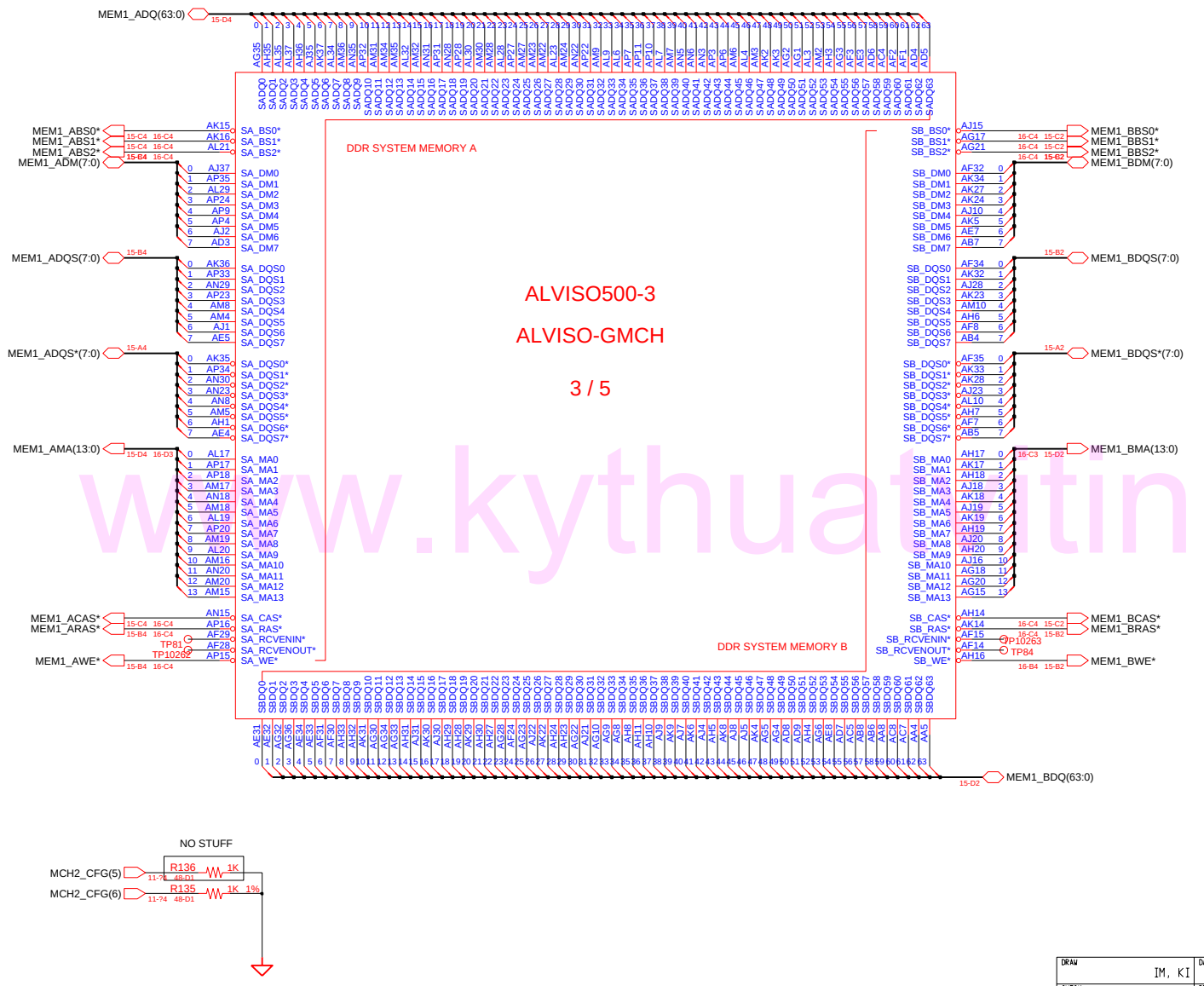

DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA	
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

def. : default Option

CFG#	Low	High
CFG(5)	DMIx2	DMIx4 (def.)
CFG(6)	DDR-2	DDR-1
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(10)	TBD	TBD
CFG(11)	TBD	TBD
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

NO STUFF

MCH2_CFG(5) — R136 1K
MCH2_CFG(6) — R135 1K 1%

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CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
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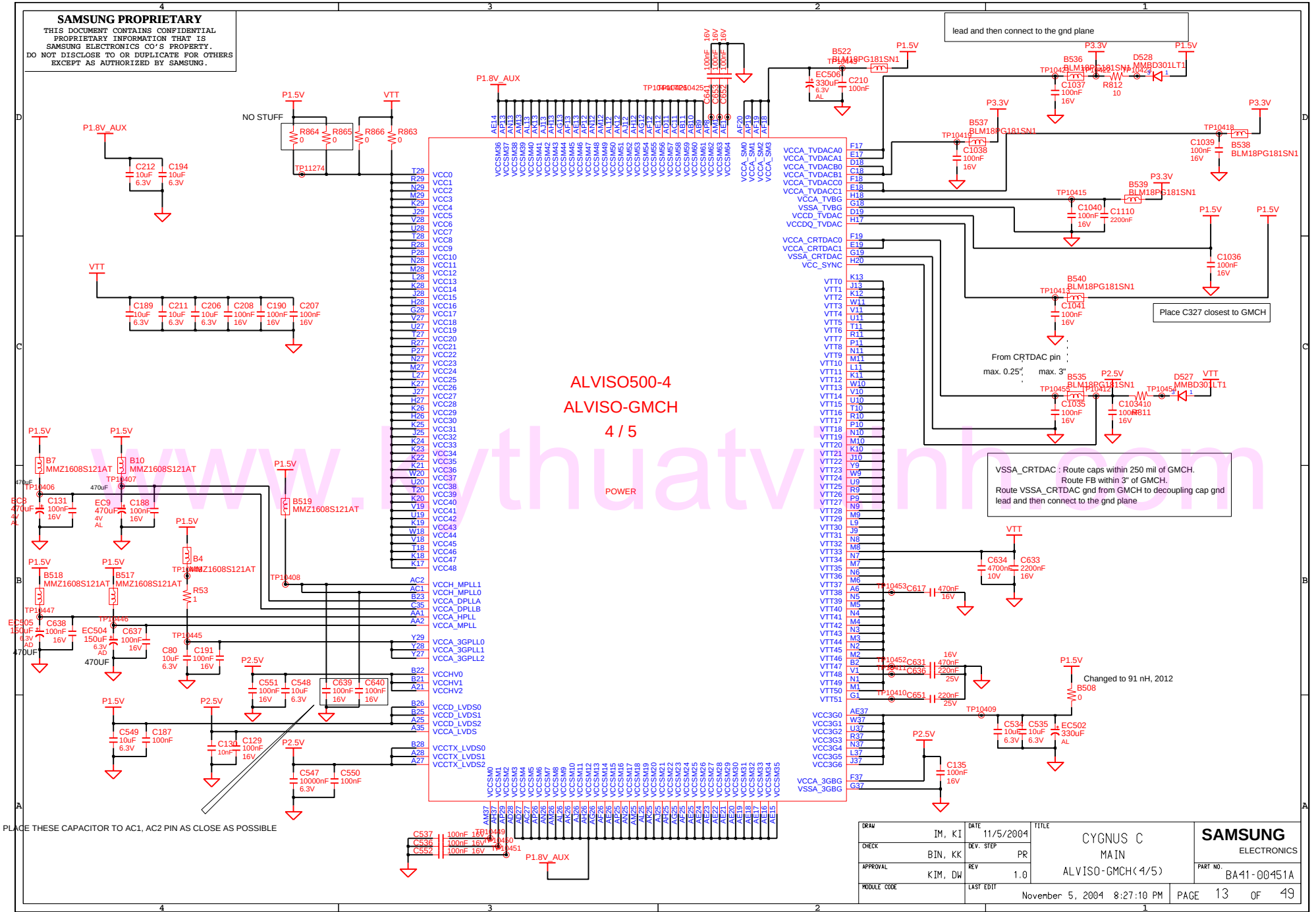

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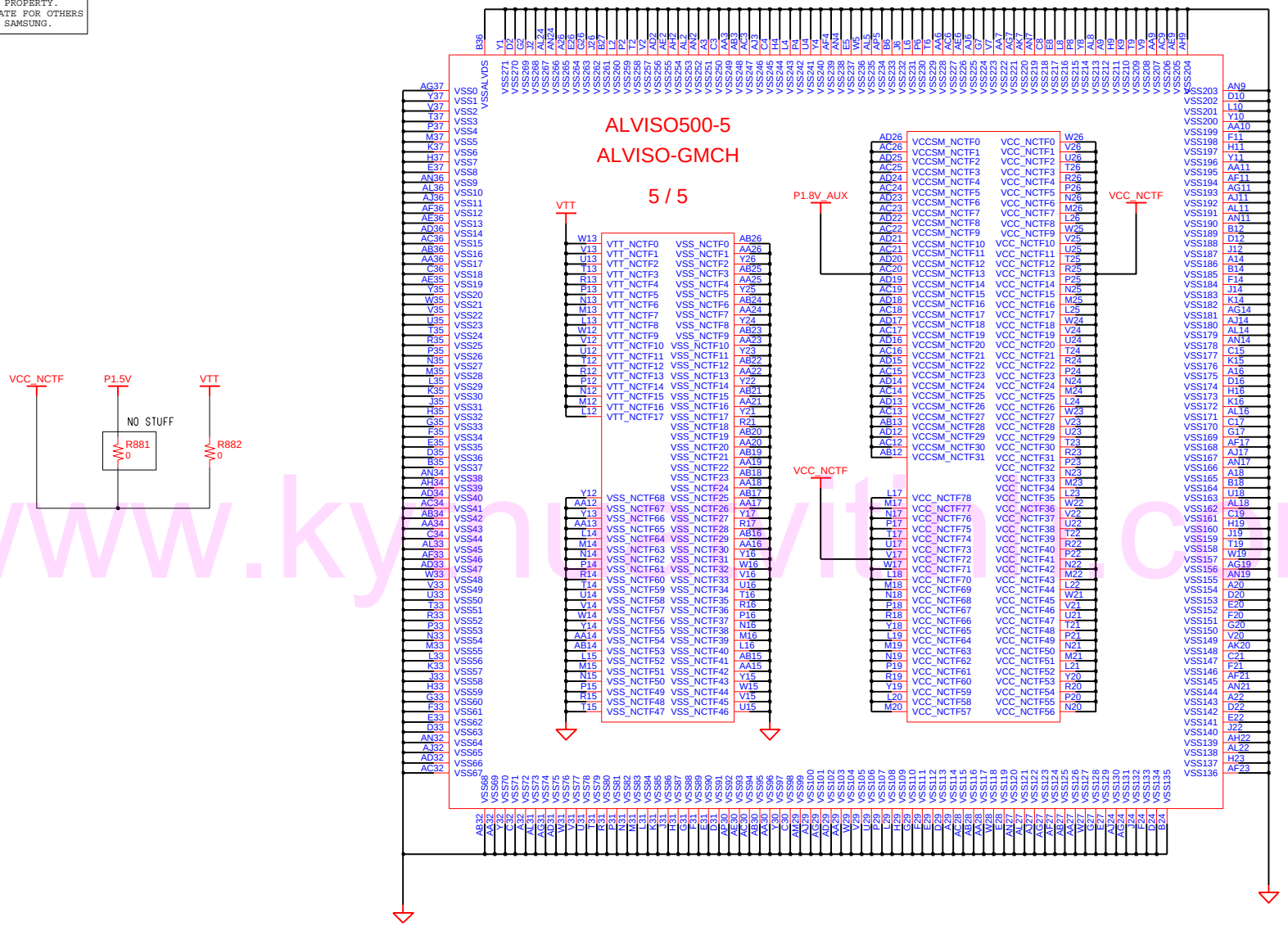

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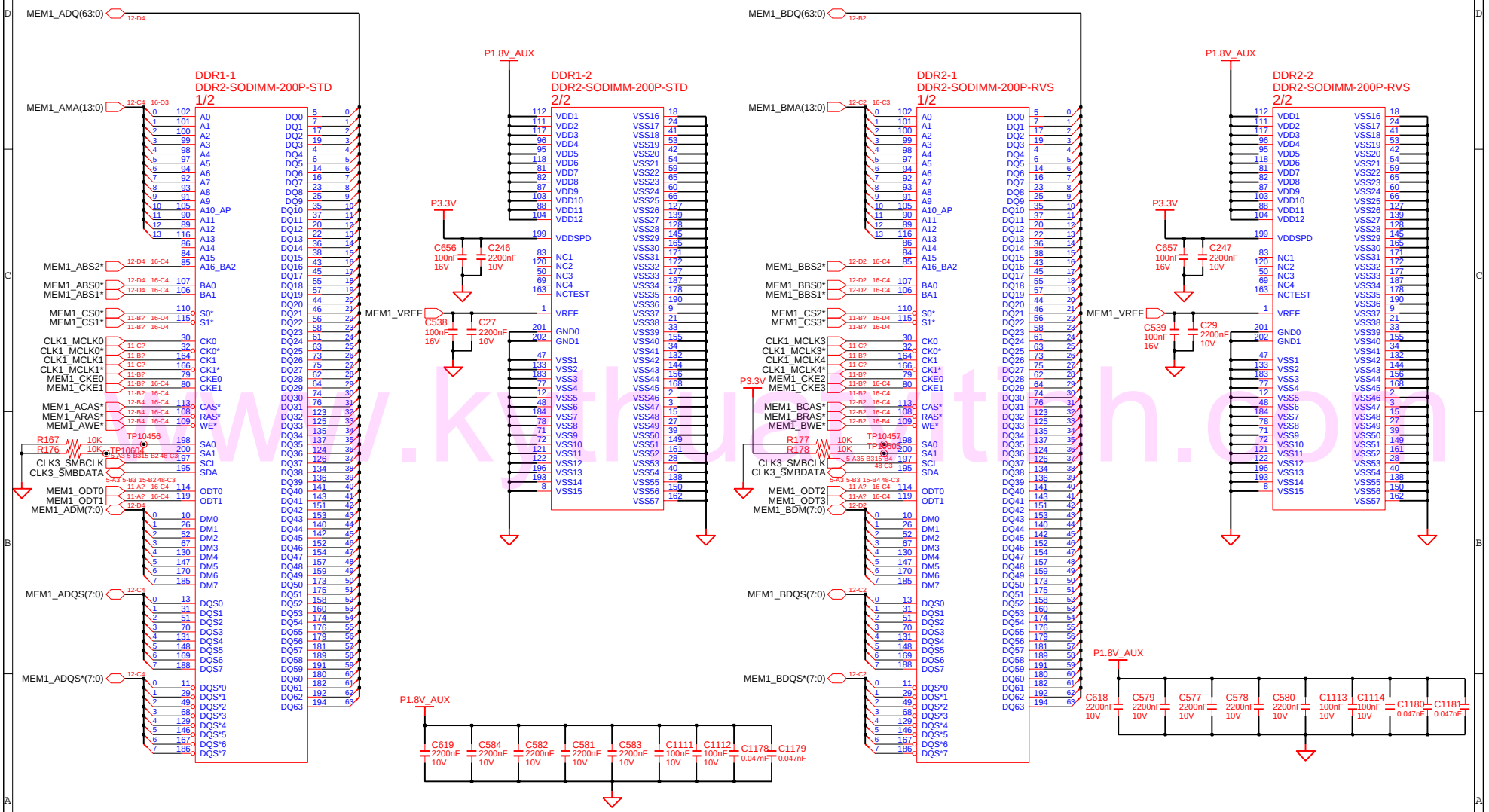

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CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
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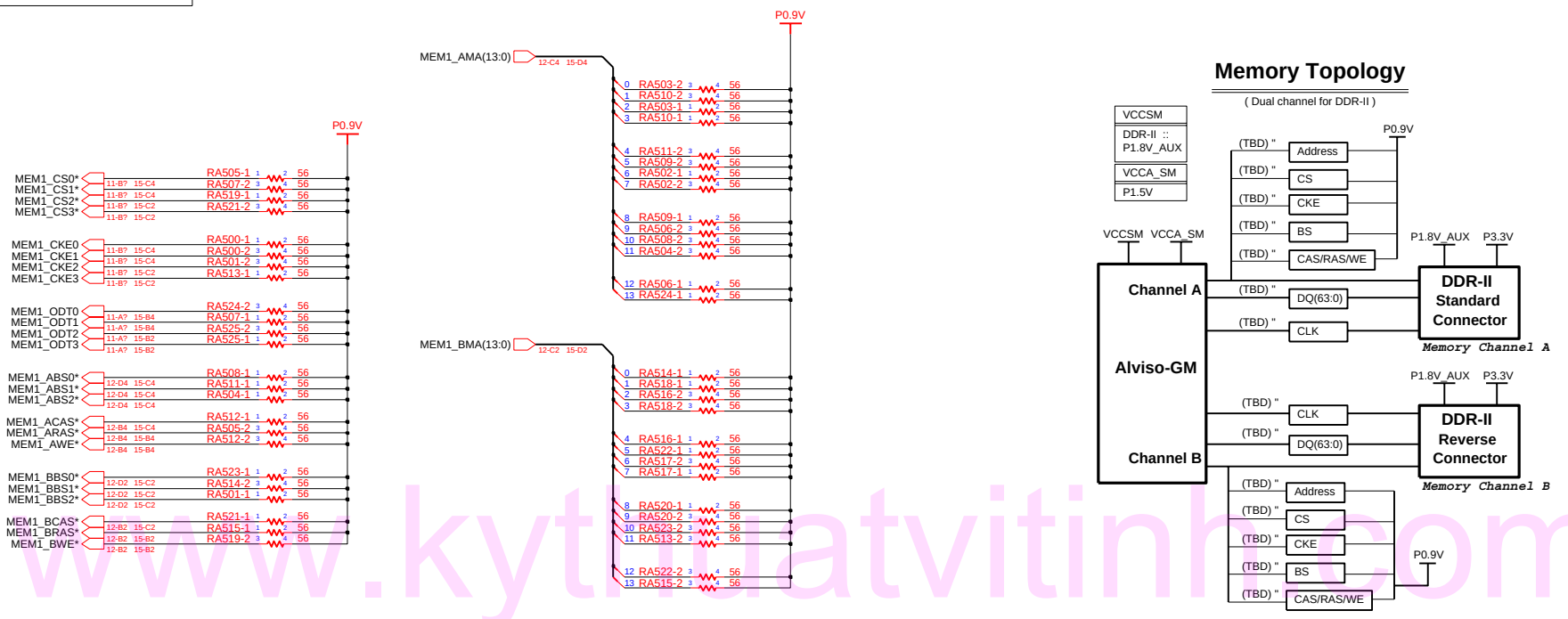

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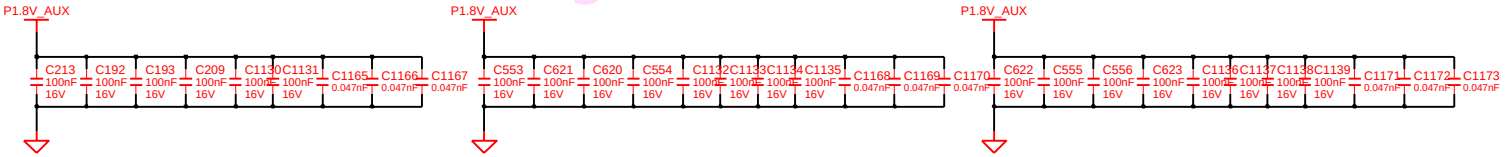
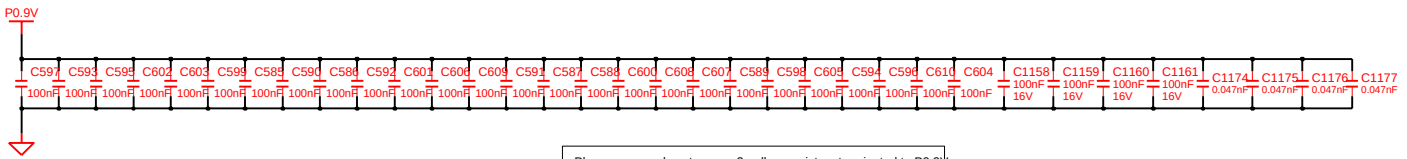


Place near GMCH

Place near SO-DIMM0

Place near SO-DIMM1



Place one cap close to every 2 pull-up resistors terminated to P0.9V

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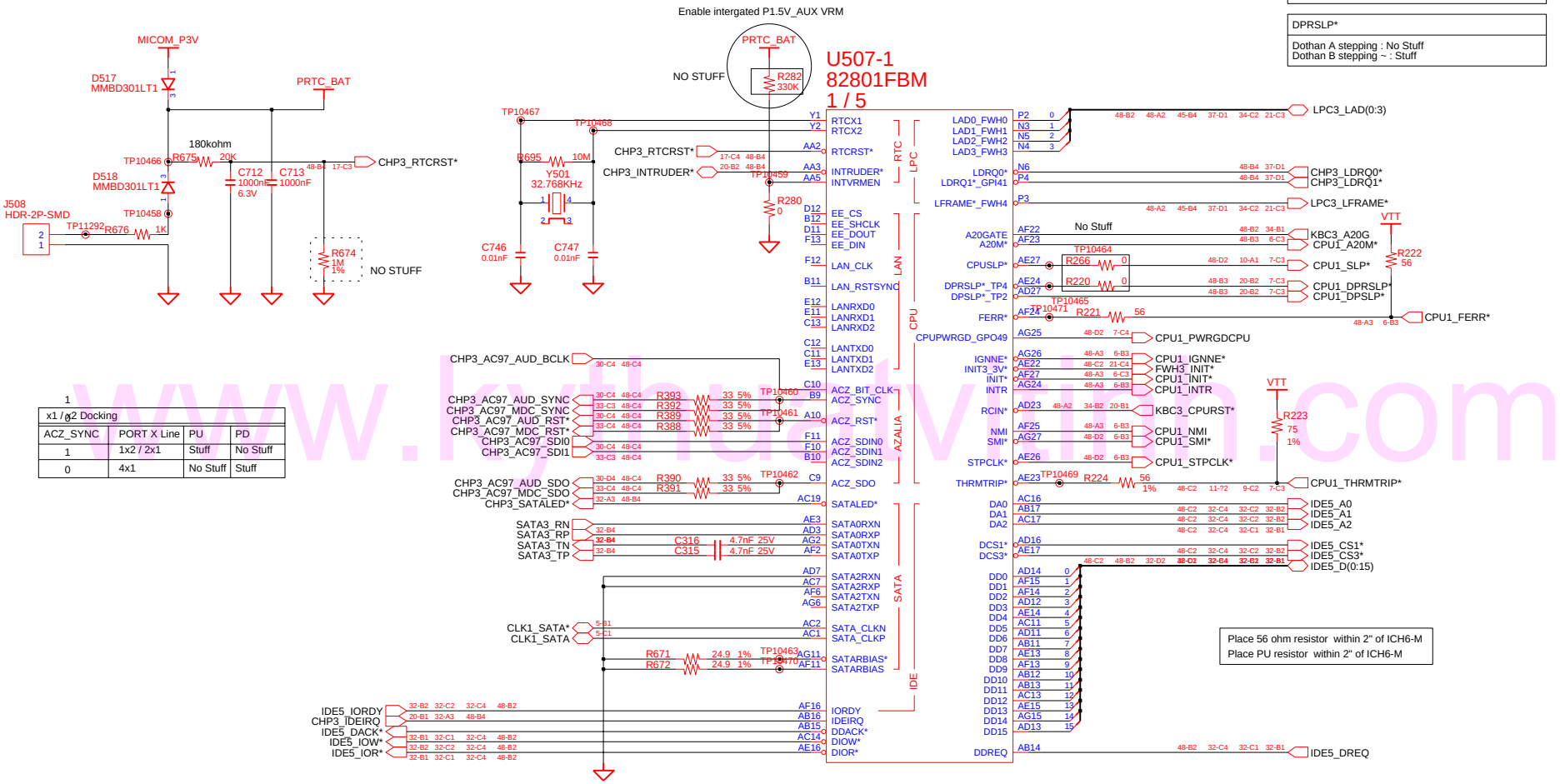
CPUSLP*
Dothan A stepping : Stuff resistor on SLP* of ICH6 Dothan B stepping ~ : Stuff resistor on SLP* of Alviso

DPRSLP*
Dothan A stepping : No Stuff Dothan B stepping ~ : Stuff



1

x1 / x2 Docking			
ACZ_SYNC	PORT X Line	PU	PD
1	1x2 / 2x1	Stuff	No Stuff
0	4x1	No Stuff	Stuff

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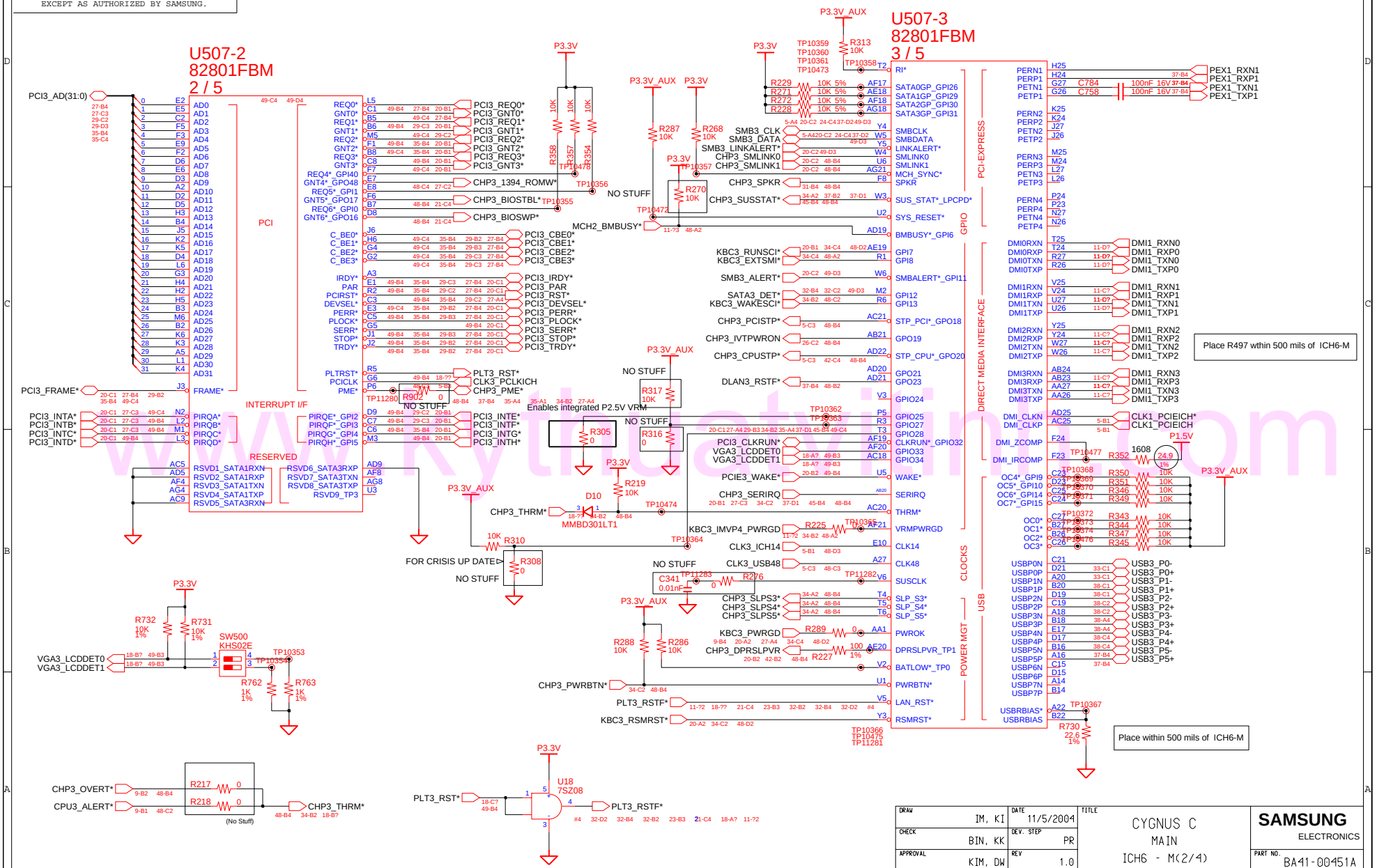

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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN ICH6 - M(2/4)	SAMSUNG ELECTRONICS
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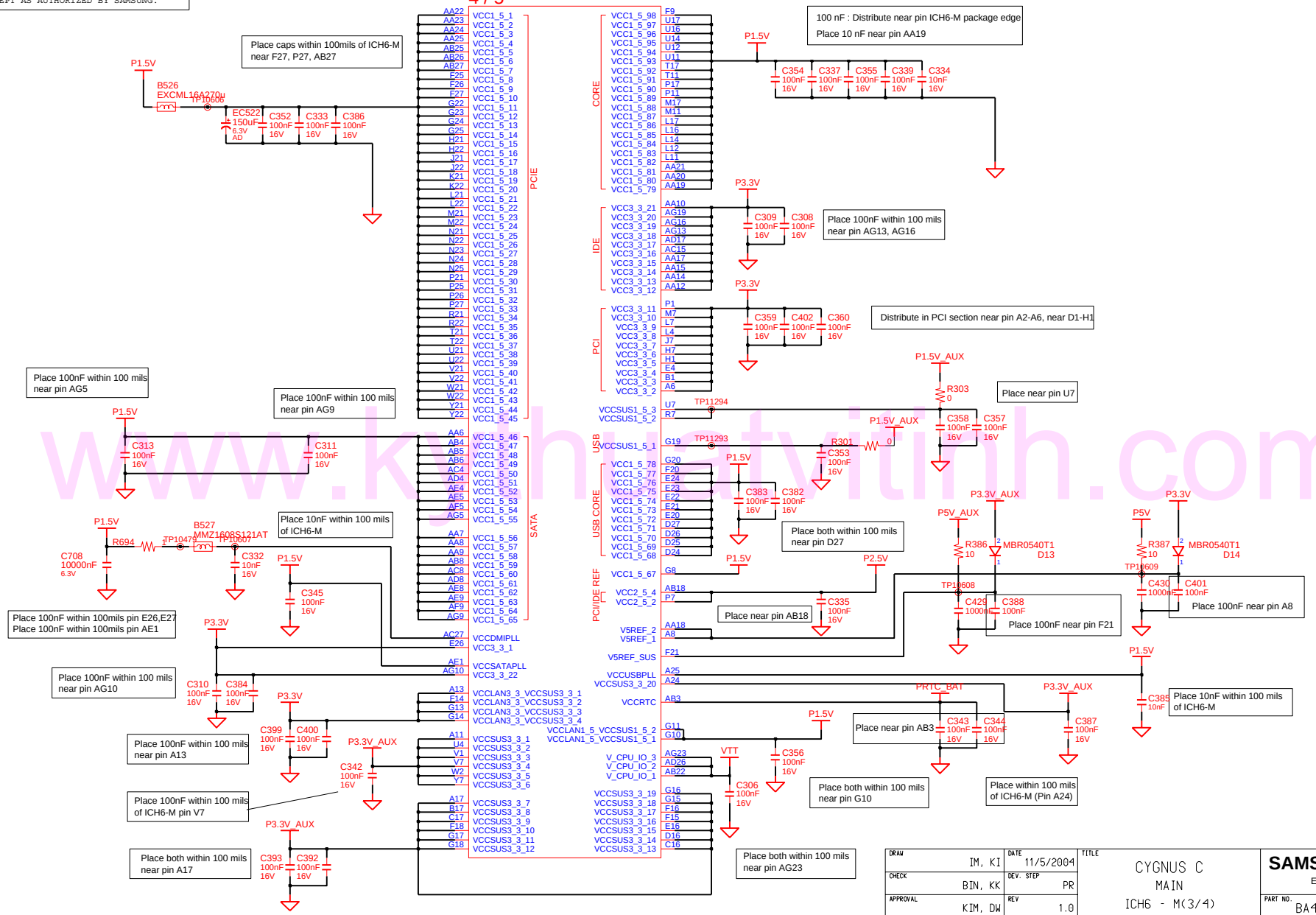

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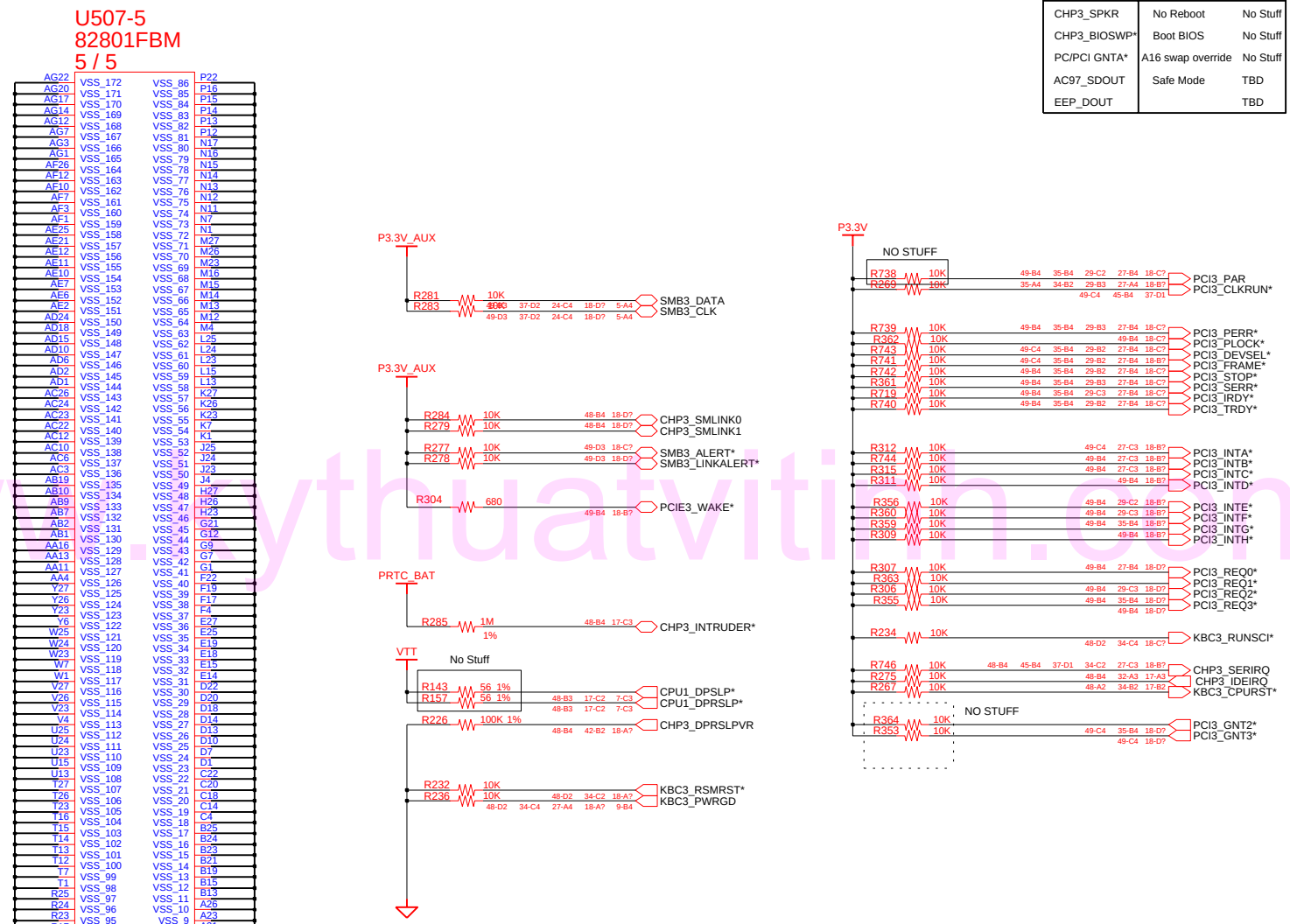
ICH6-m Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
EEP_DOUT		TBD



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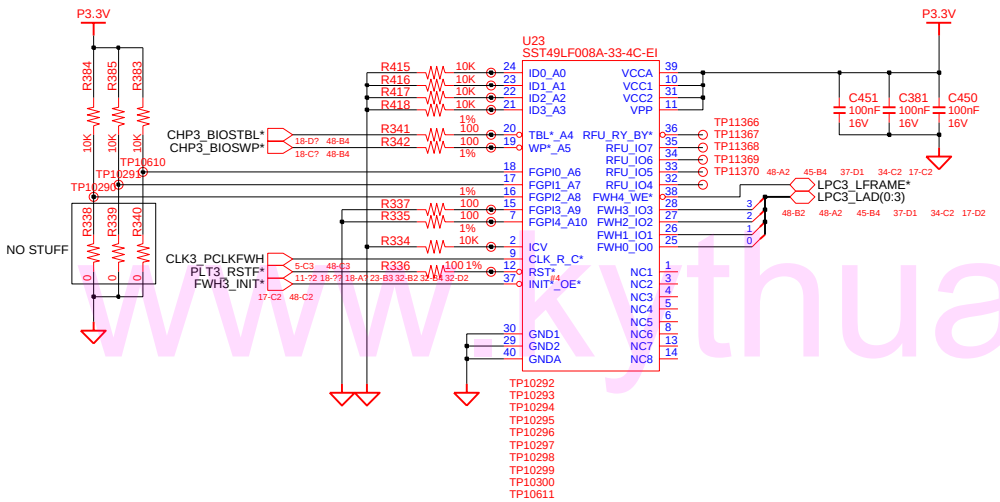

02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
OE	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUP CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY " PRESS ..... SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM GETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

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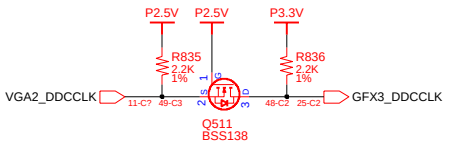
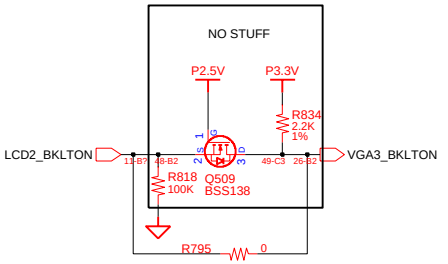
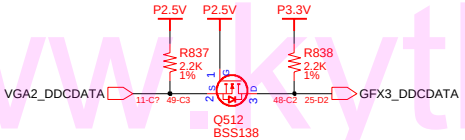
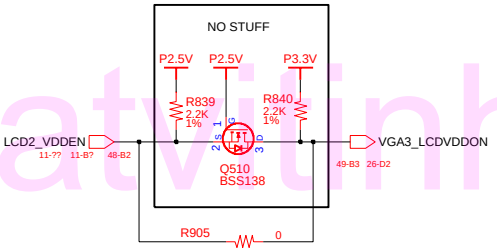
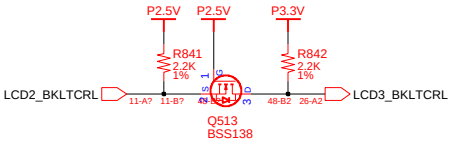
LVDS Voltage Translation Logic
(2.5V -> 3.3V)











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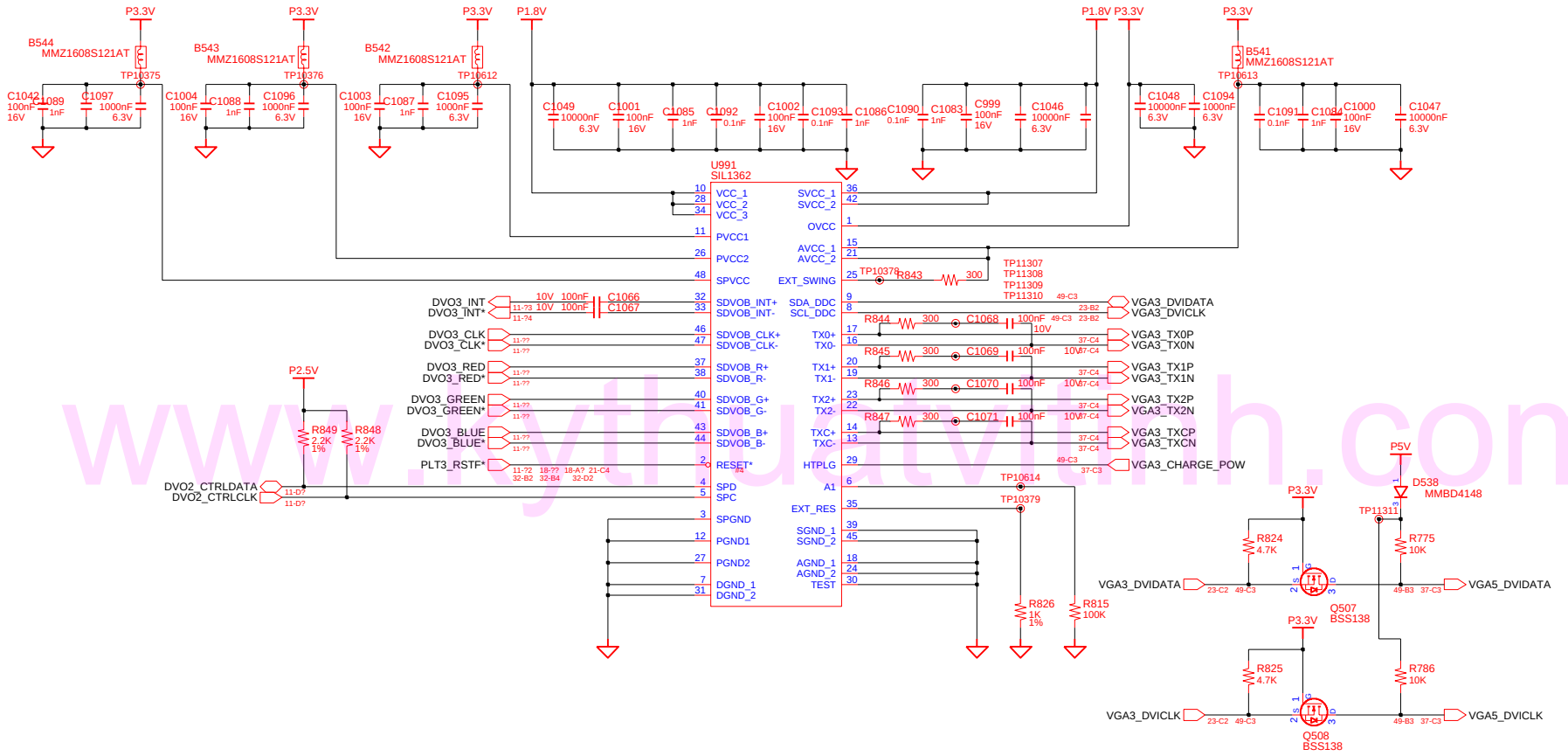

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CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
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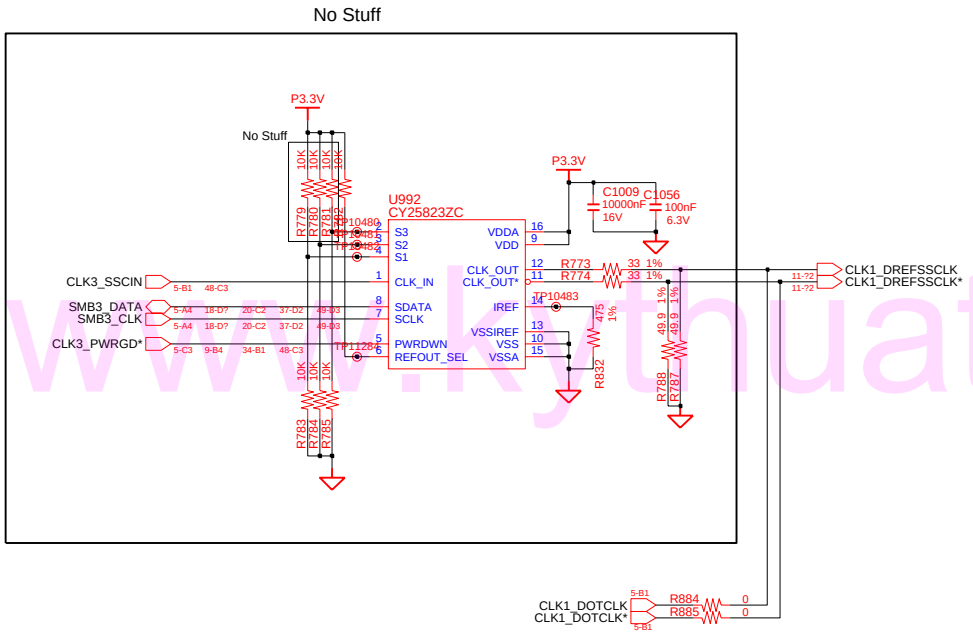

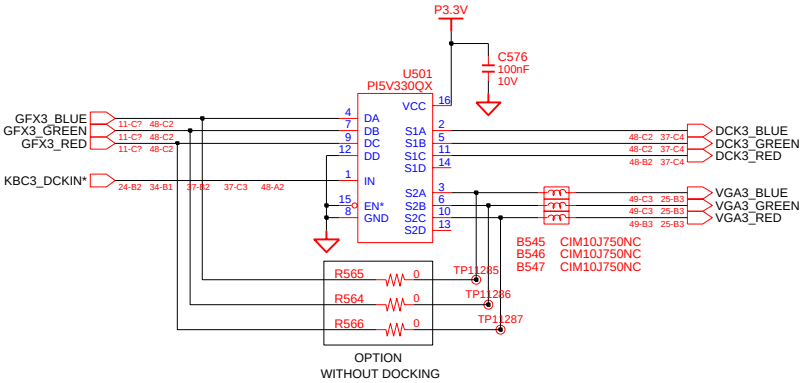

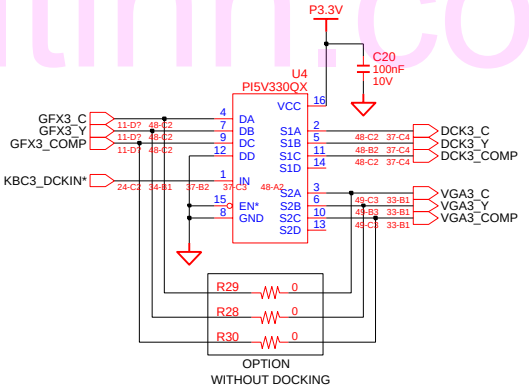

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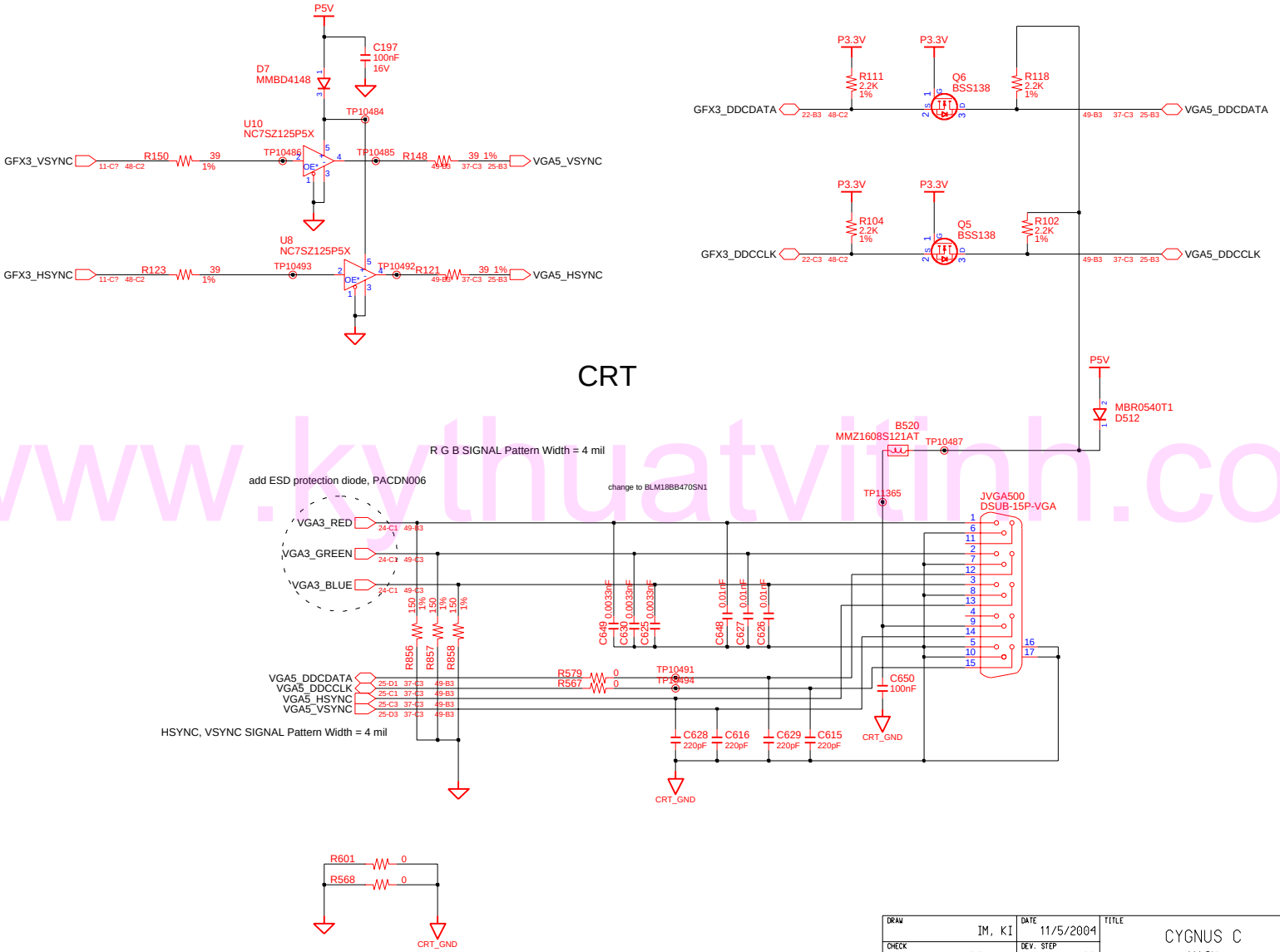

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Optional External Thermal Sensor

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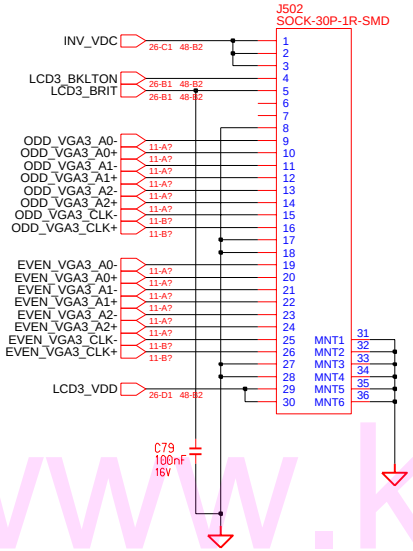
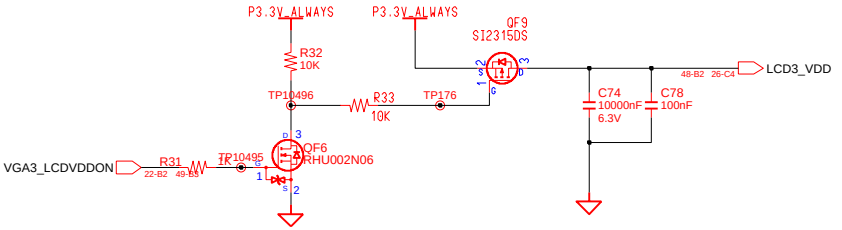
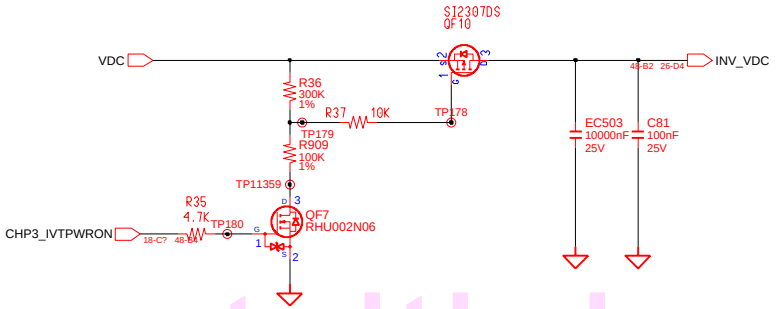
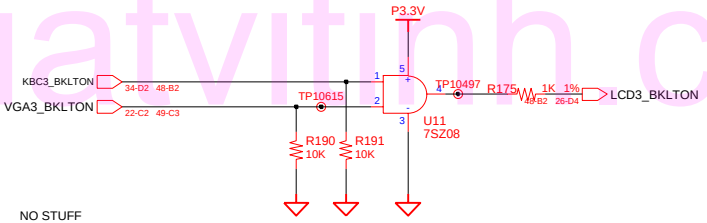
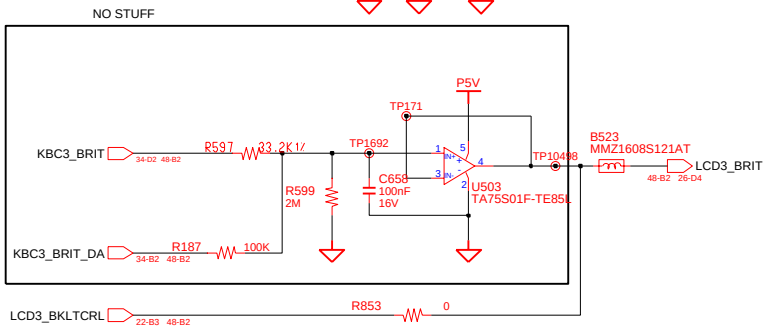
LCD CONNECTOR











DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN LCD_CONNECTOR / BKLT	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM		PAGE 26 OF 49

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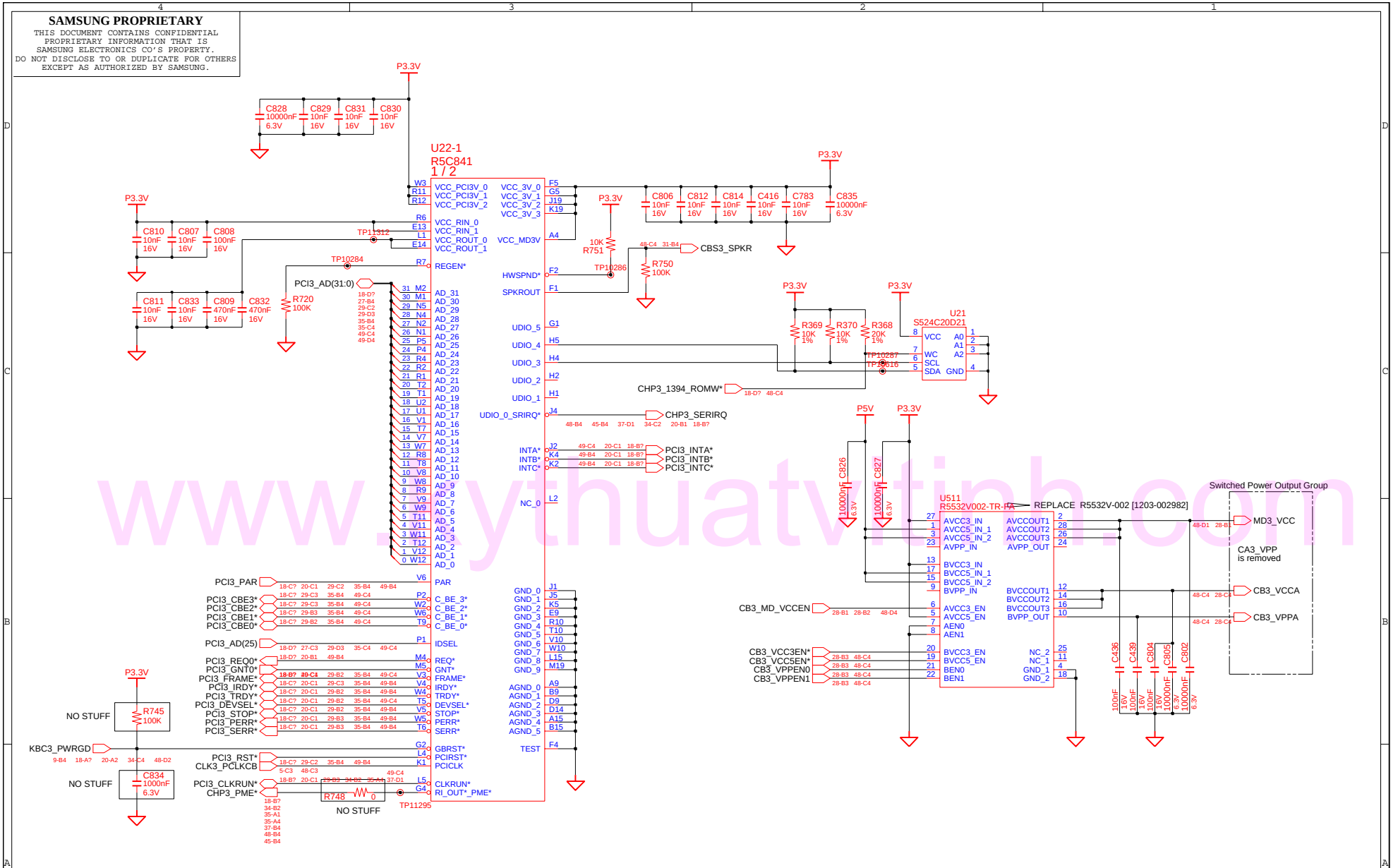

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CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM	PAGE 27 OF 49	

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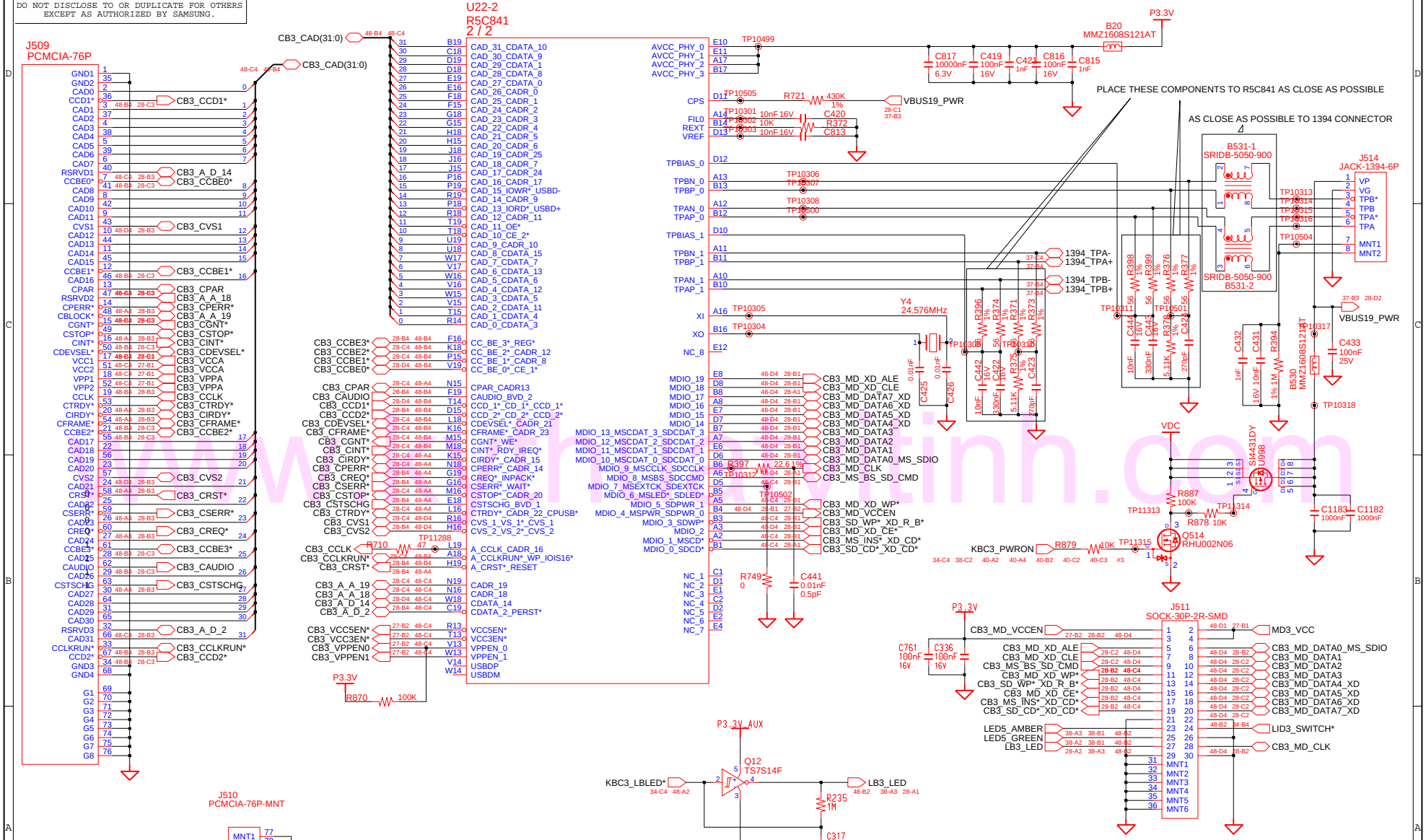

DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN CARDBUS SOCKET/MEDIA CARD	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM		PAGE 28 OF 49

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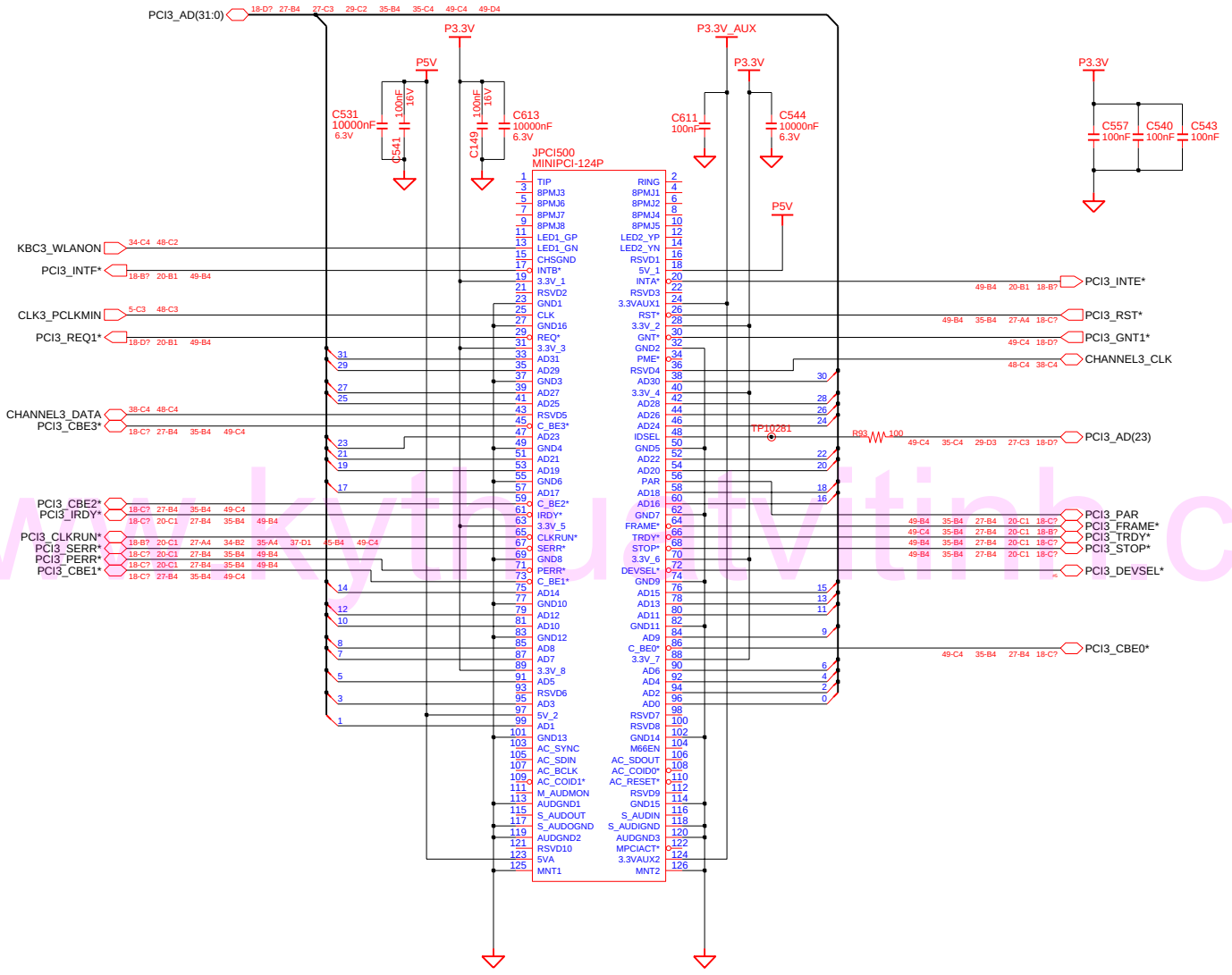

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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM		PAGE 29 OF 49

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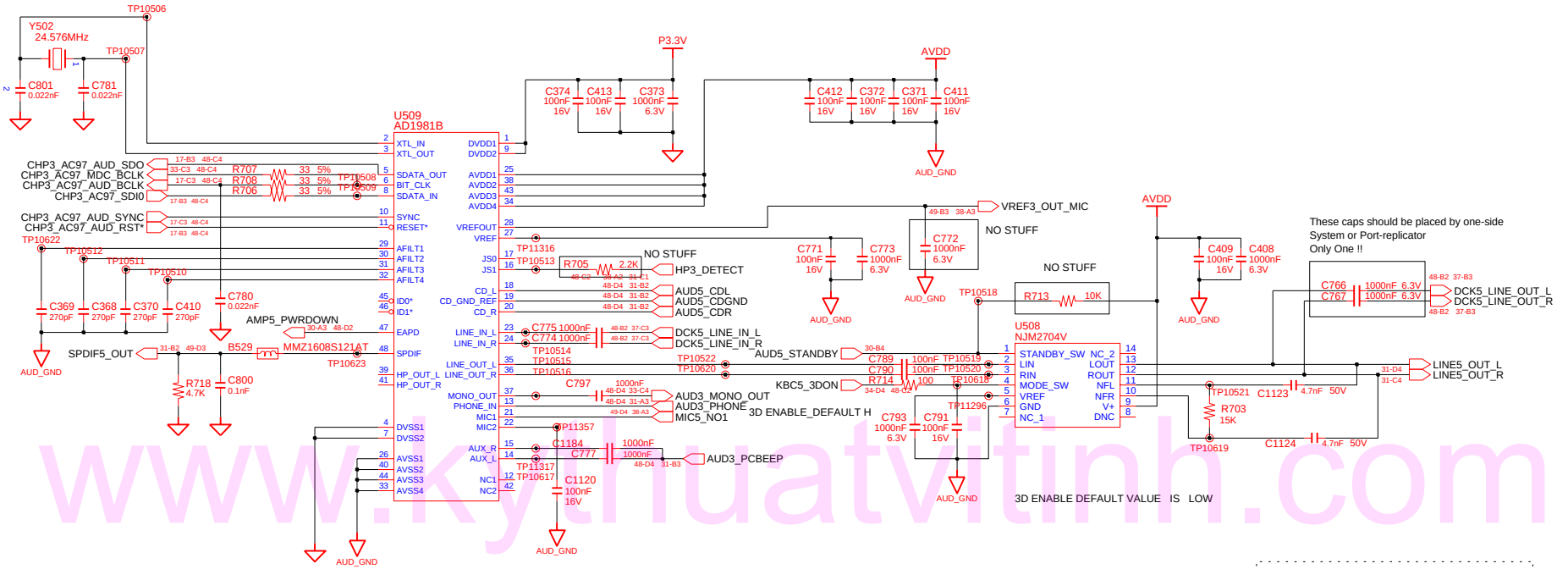
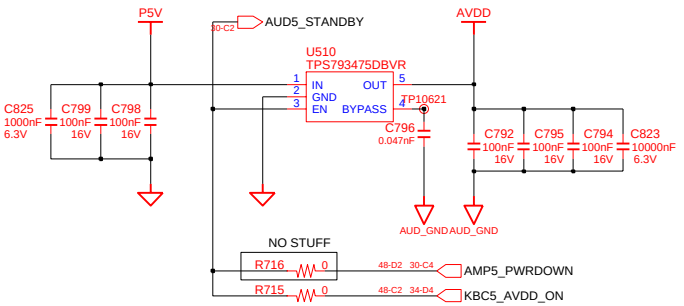


1. AUD_GND is Audio Ground
2. GND is Digital Ground
3. MGND is Mic_Ground
4. PR_LINE_OUT & PR_LINE_IN is for Port Replicator



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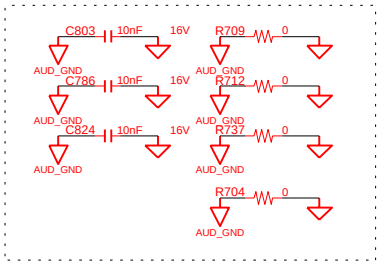

DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN AUDIO CODEC & AMP	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM	PAGE 30 OF 49	

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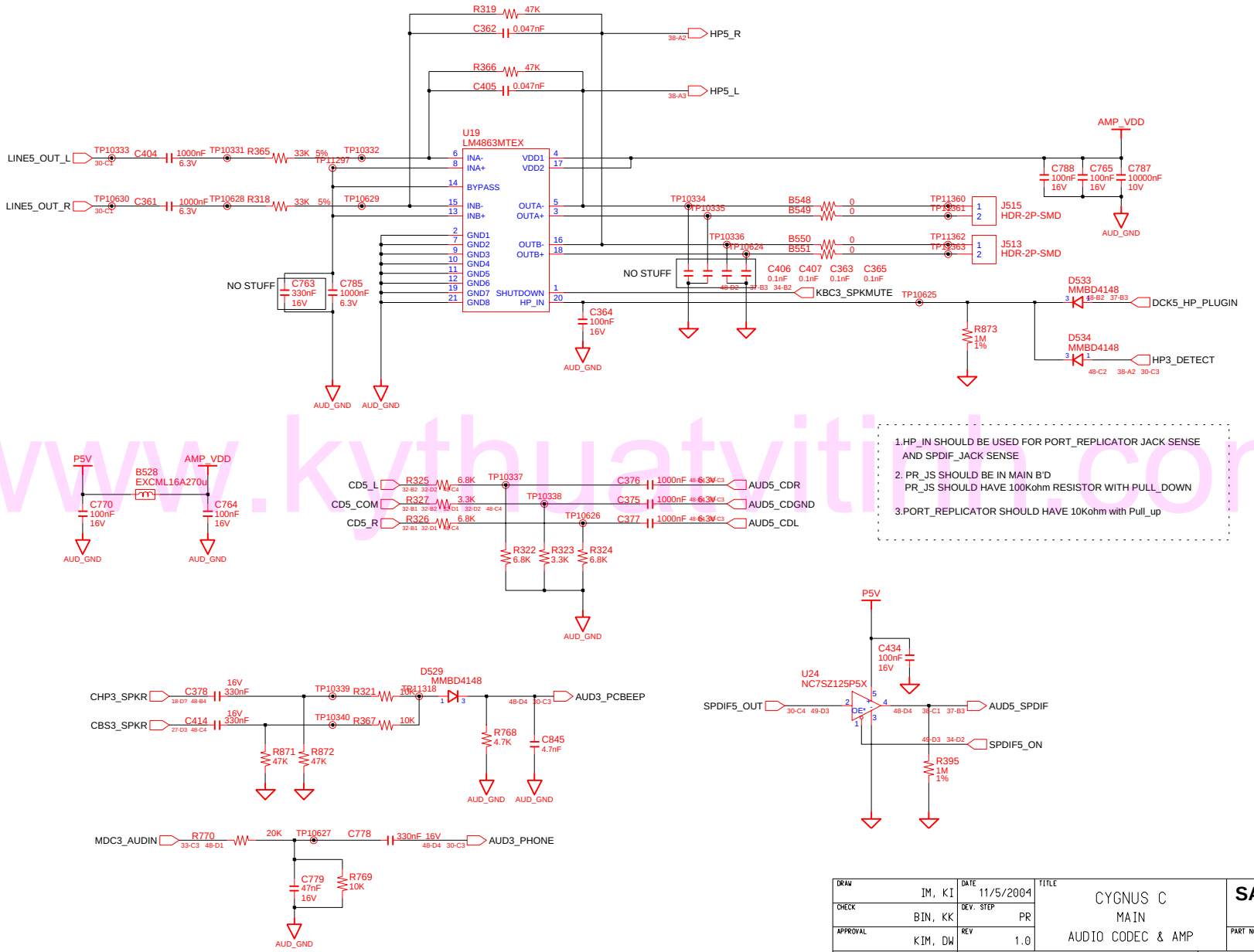

1.HP_IN SHOULD BE USED FOR PORT_REPLICATOR JACK SENSE AND SPDIF_JACK SENSE

2. PR_JS SHOULD BE IN MAIN B'D
PR_JS SHOULD HAVE 100Kohm RESISTOR WITH PULL_DOWN

3.PORT_REPLICATOR SHOULD HAVE 10Kohm with Pull_up

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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN AUDIO CODEC & AMP	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM		PAGE 31 OF 49

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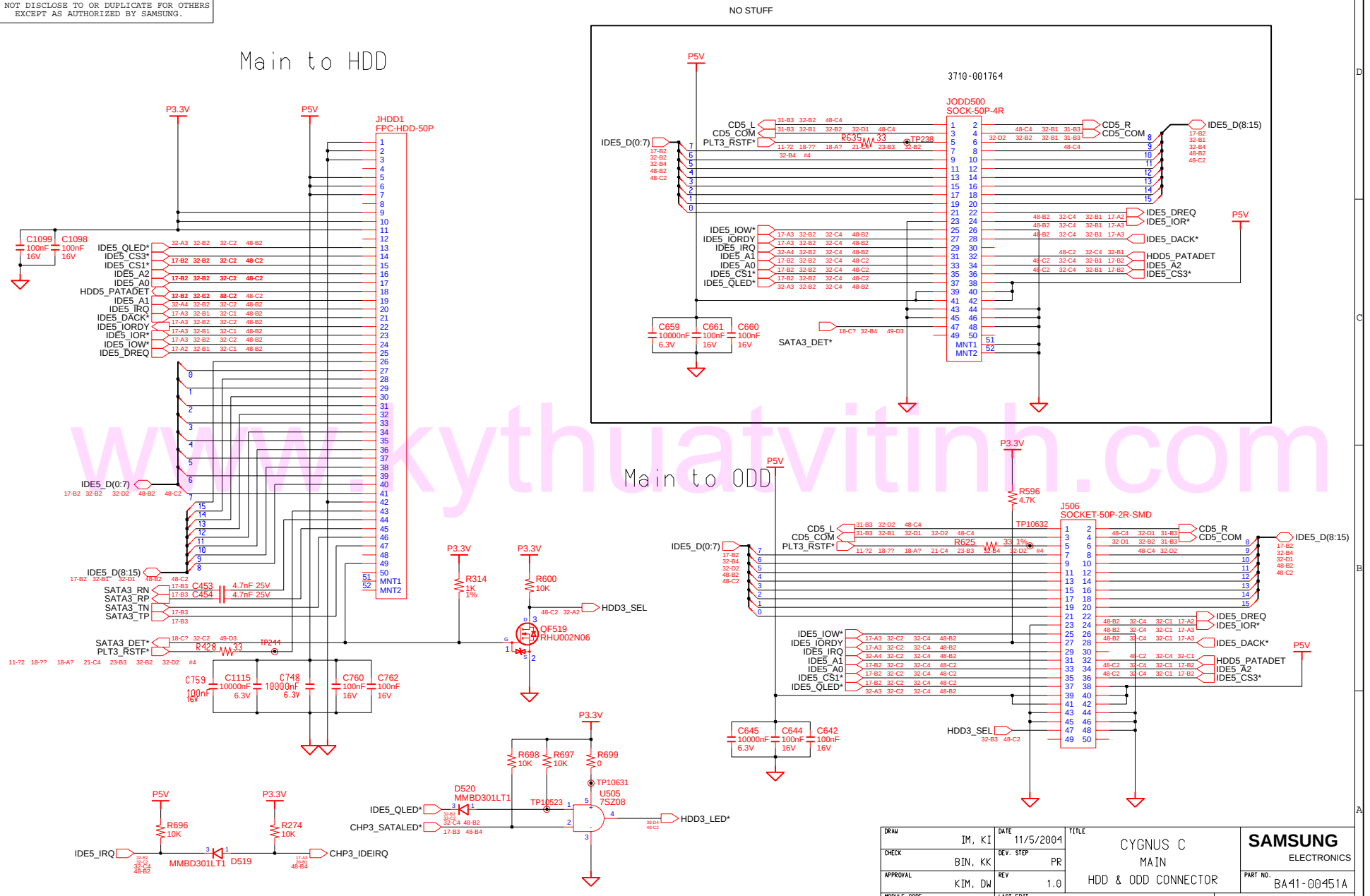

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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN HDD & ODD CONNECTOR	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM		PAGE 32 OF 49

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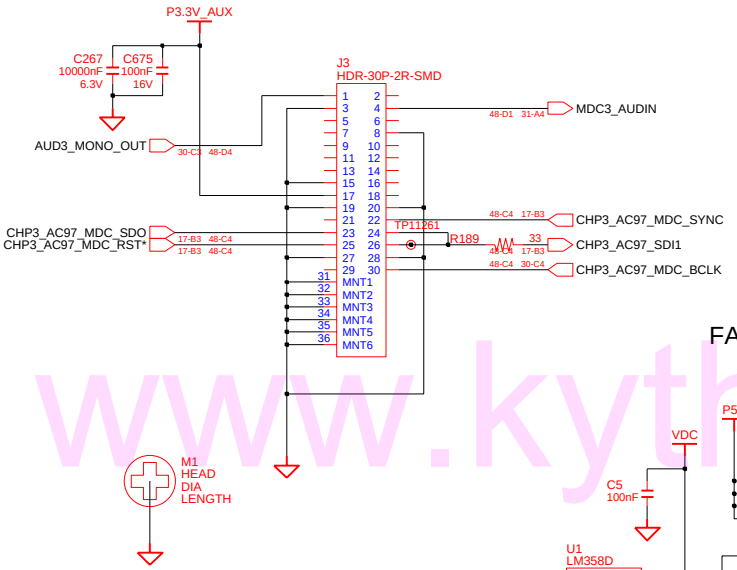
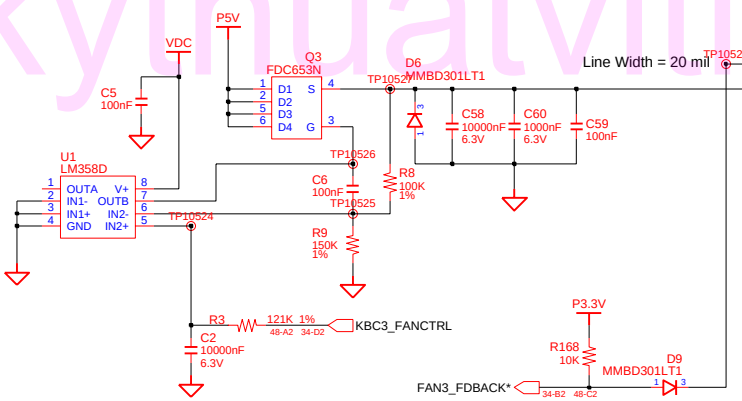
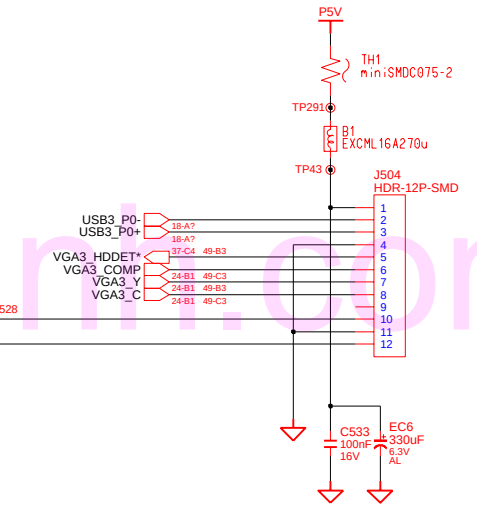
MDC Connecter



FAN Control Logic



TV-OUT(S-VHS)



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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR	MDC MODEM / TV-OUT(SVHS)	PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
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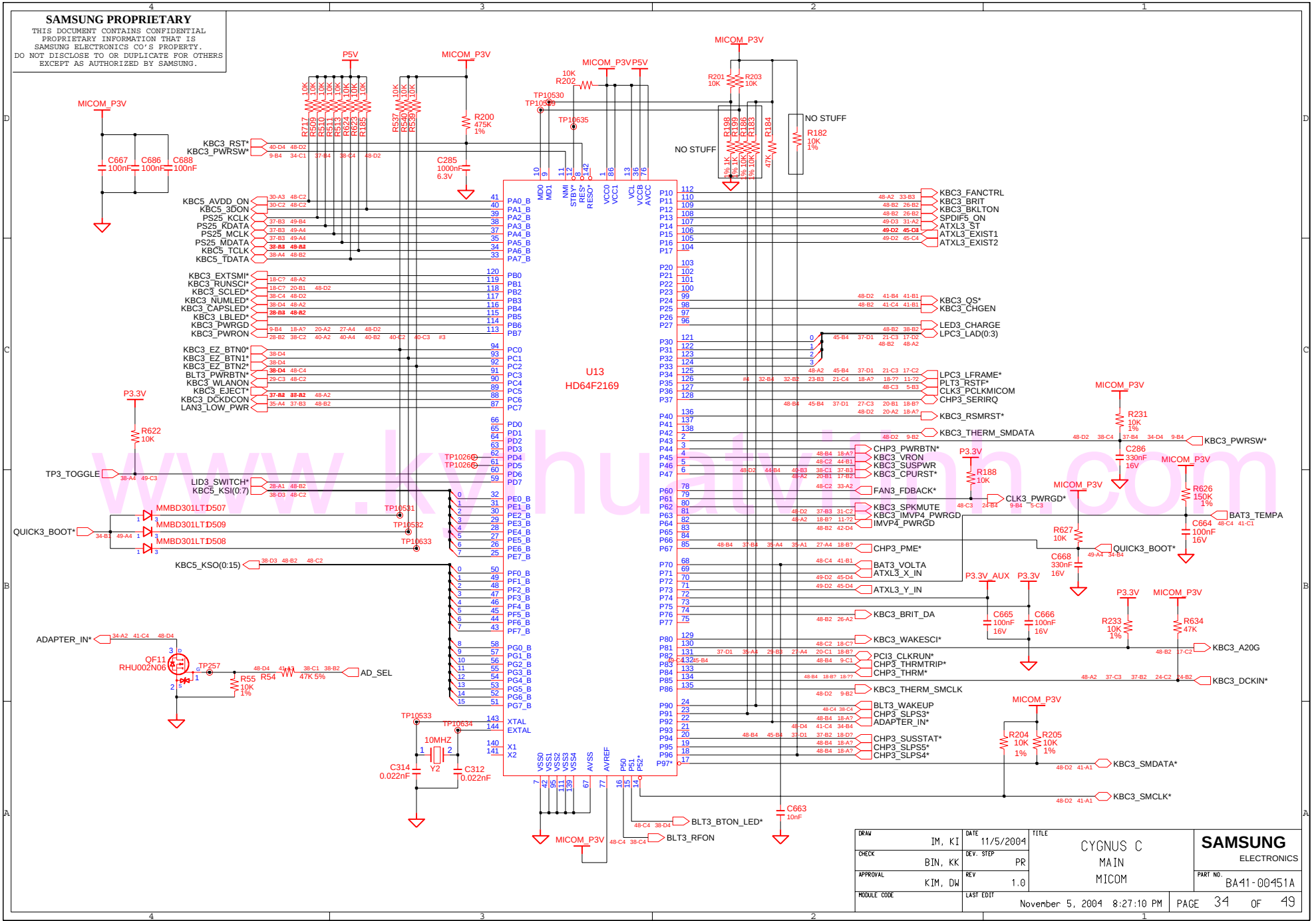

DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN MICOM	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM	PAGE 34 OF 49	

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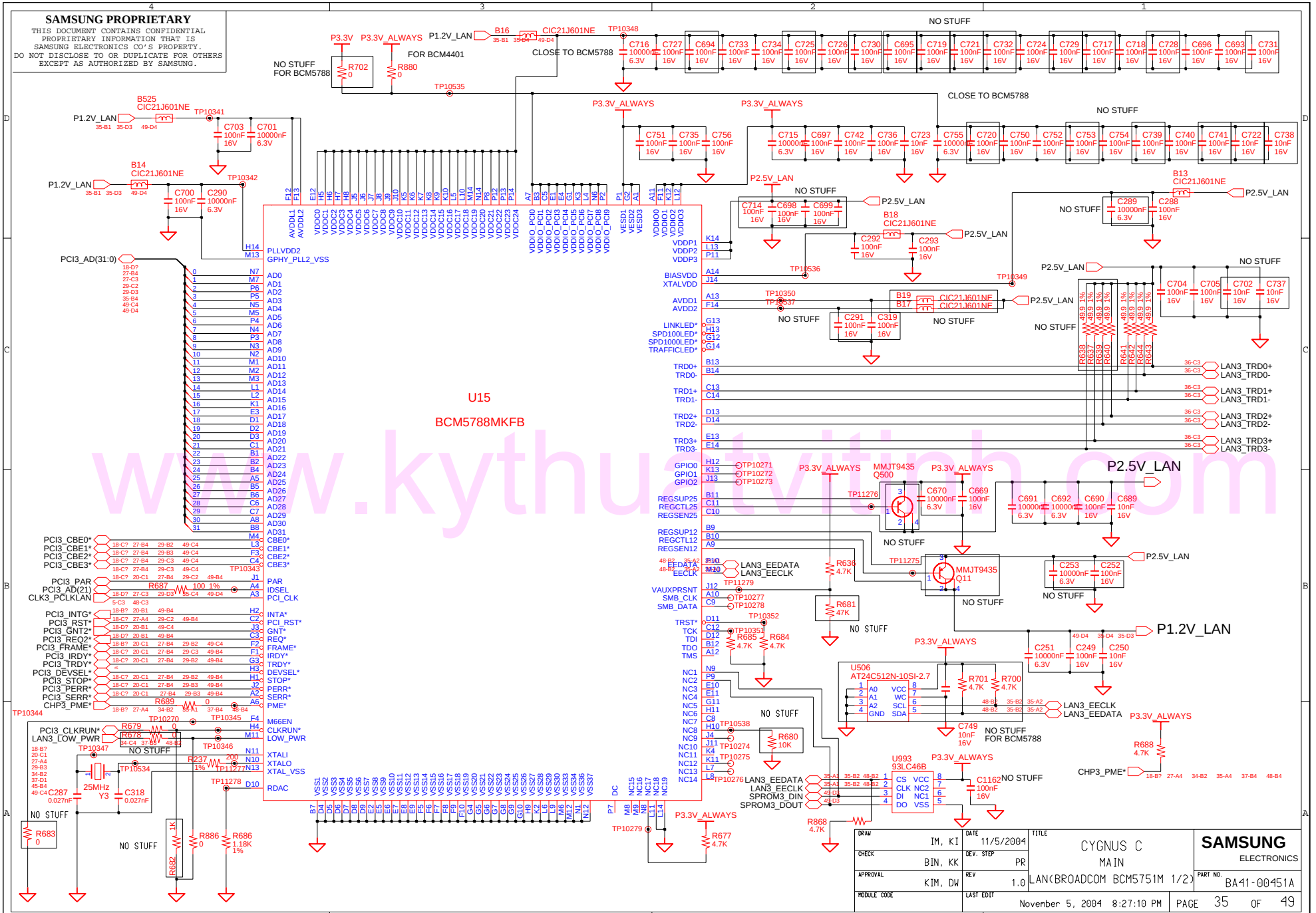

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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN LAN(BROADCOM BCM5751M 1/2)	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM	PAGE 35 OF 49	

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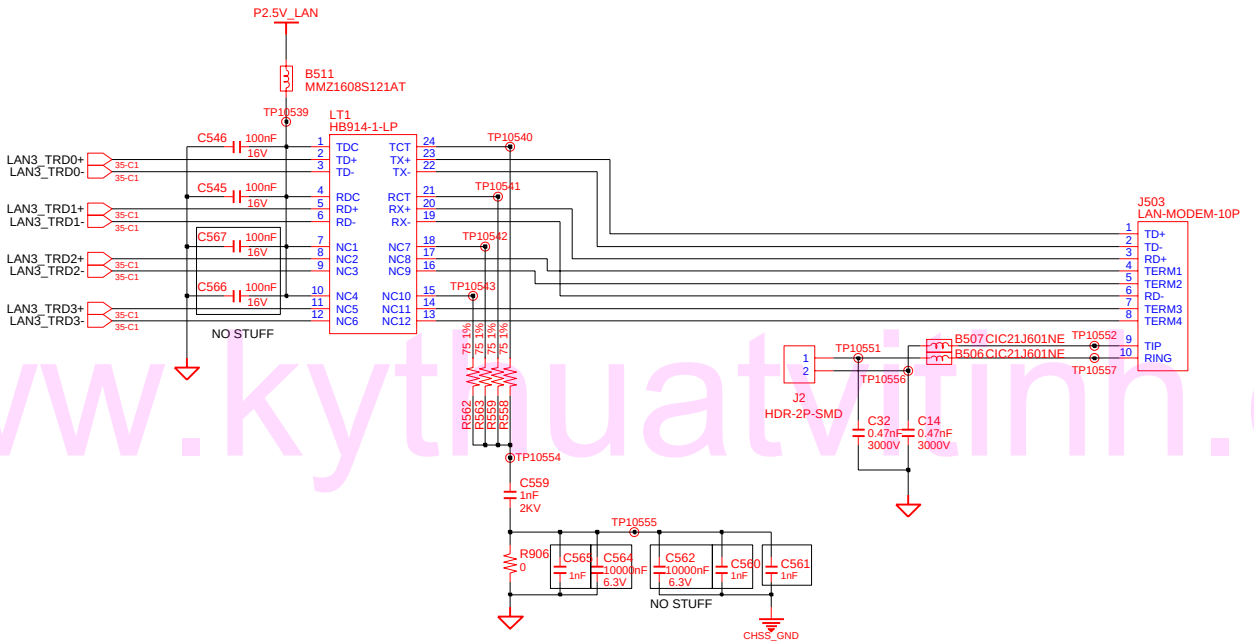

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DRAW IM, KI	DATE 11/5/2004	TITLE CYGNUS C MAIN LAN(BROADCOM BCM5751M 2/2)	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00451A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:27:10 PM	PAGE 36 OF 49	

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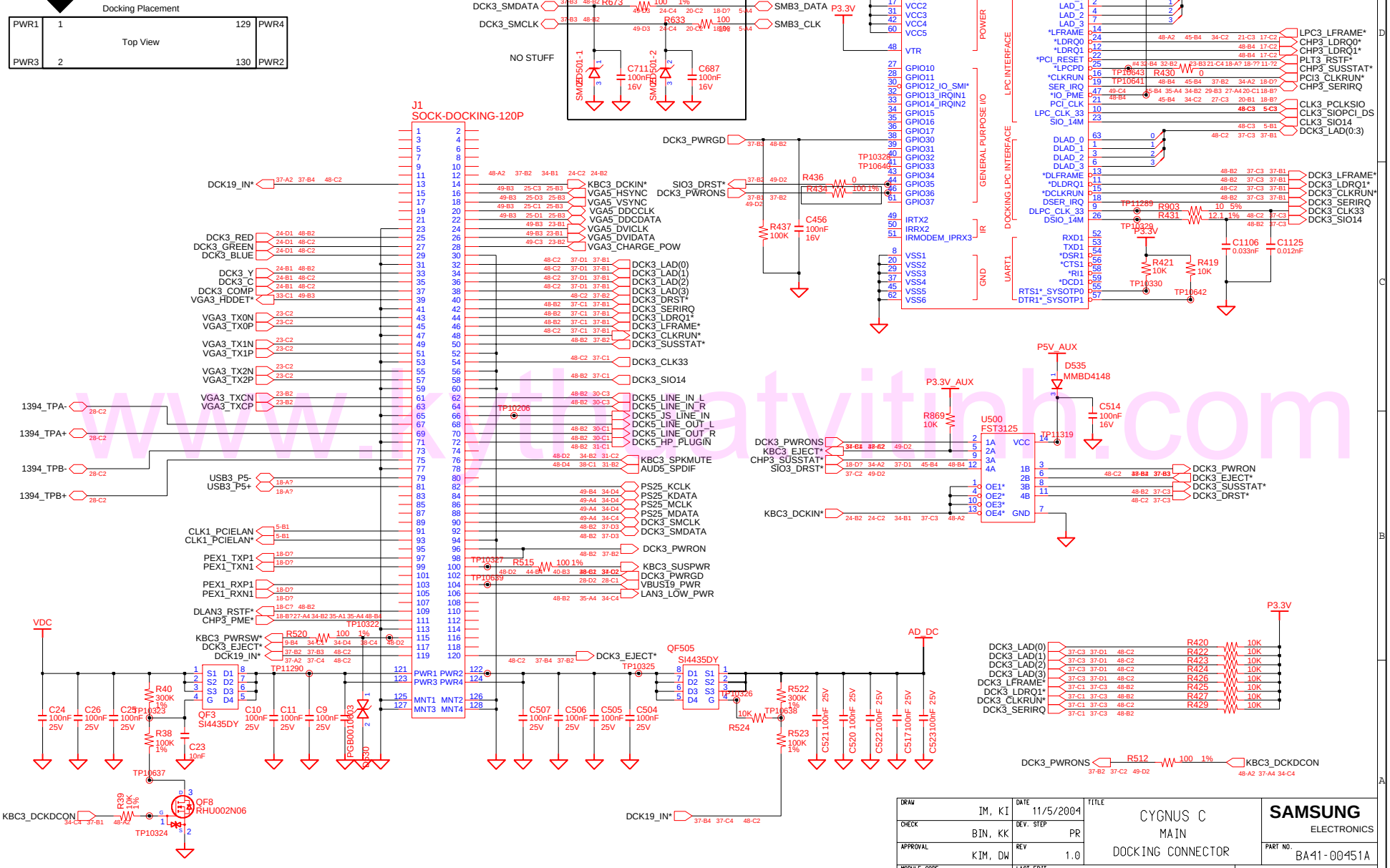
DOCKING CONNECTOR (130PIN)



DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN DOCKING CONNECTOR	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
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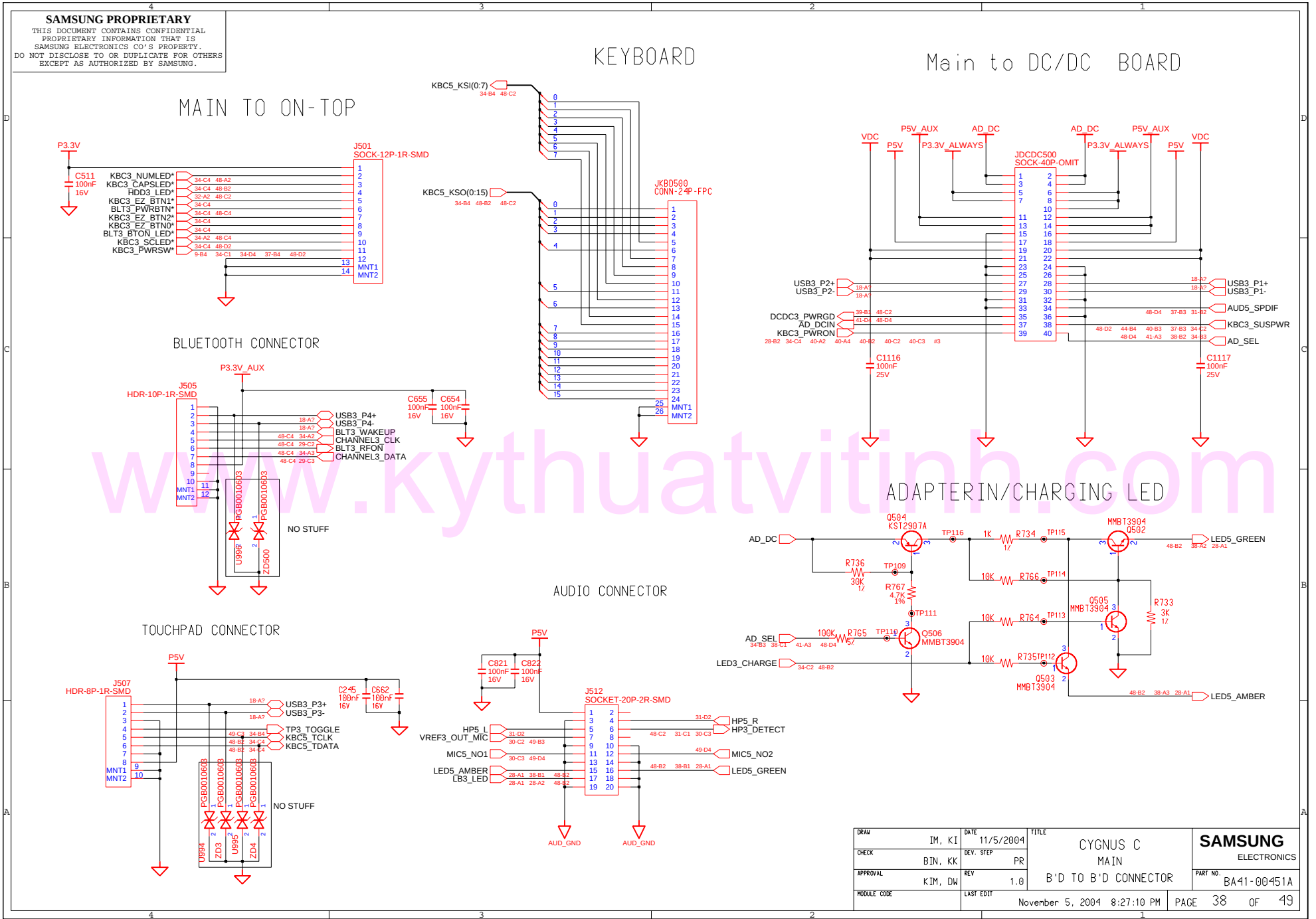

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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN B'D TO B'D CONNECTOR	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:27:10 PM		PAGE 38 OF 49

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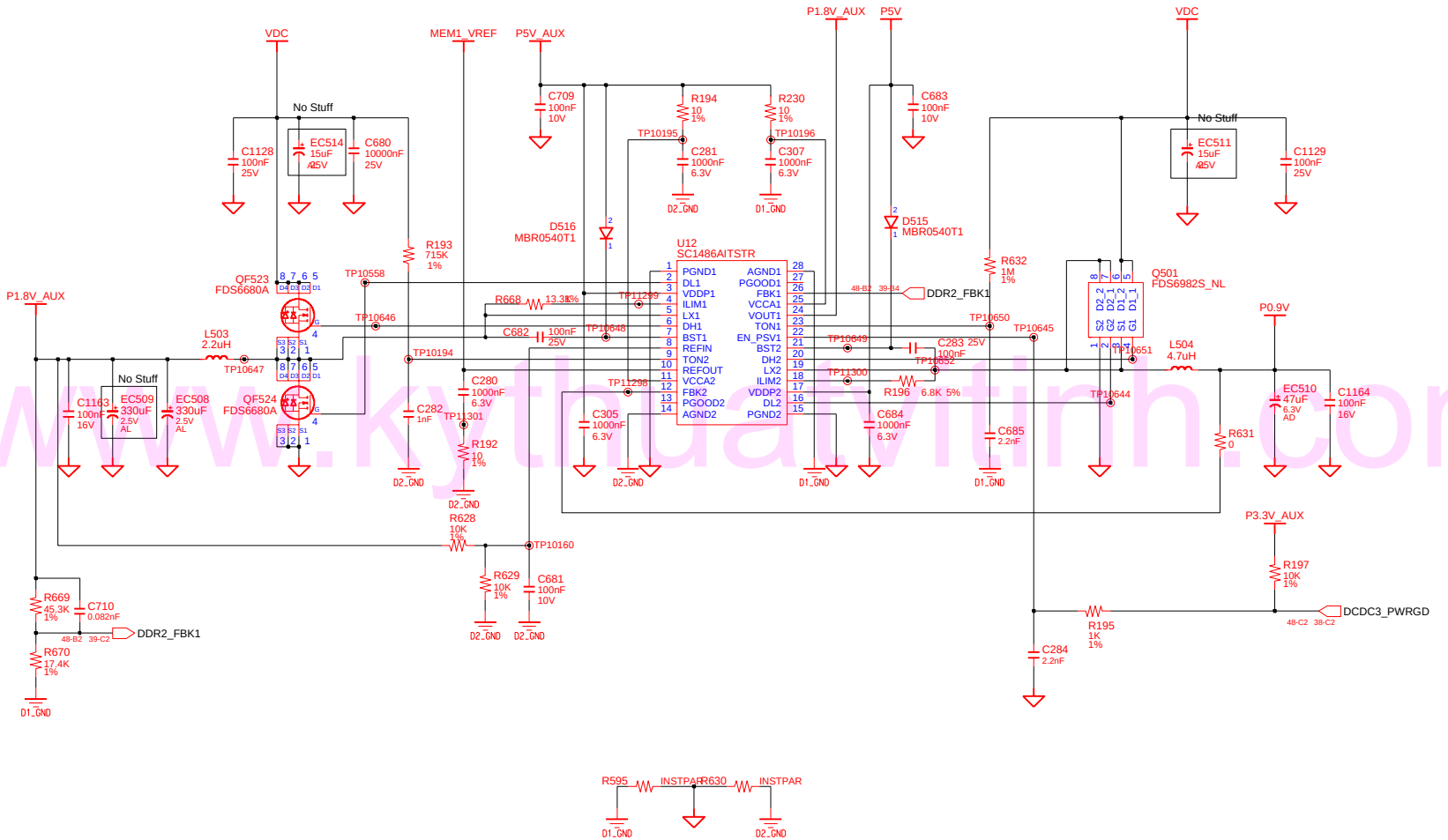
DDR Power



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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN DDR POWER	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
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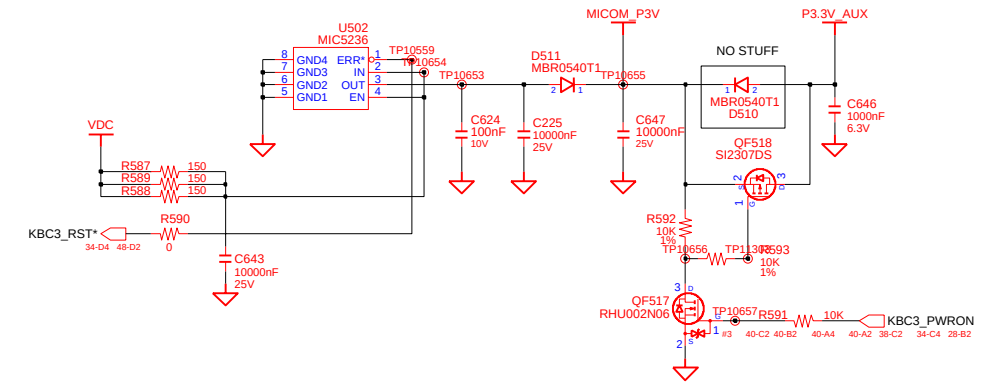
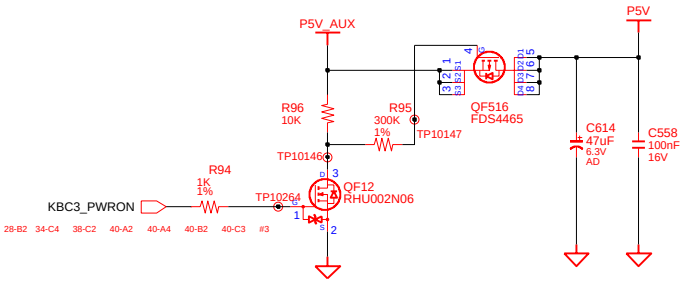
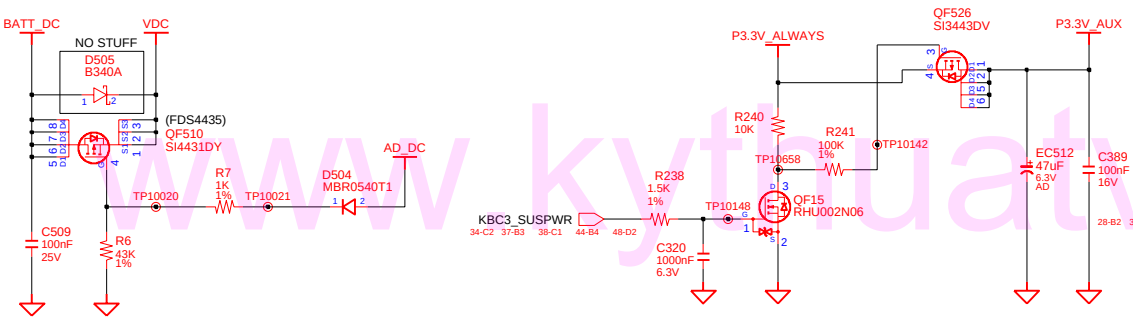
MICOM_P3V Power



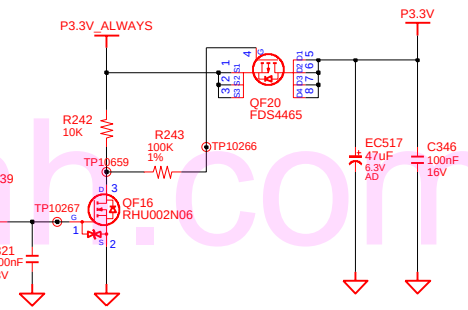
Switched Power On (P5V)



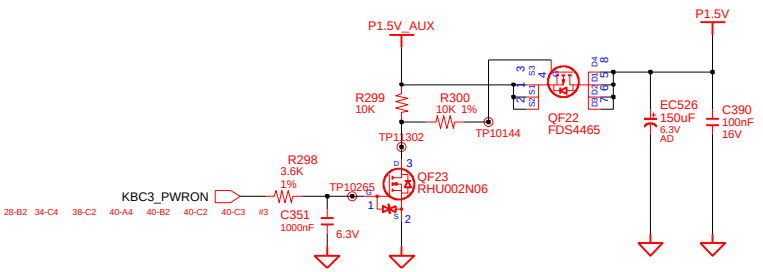
Switched Power On (P3.3V_AUX)



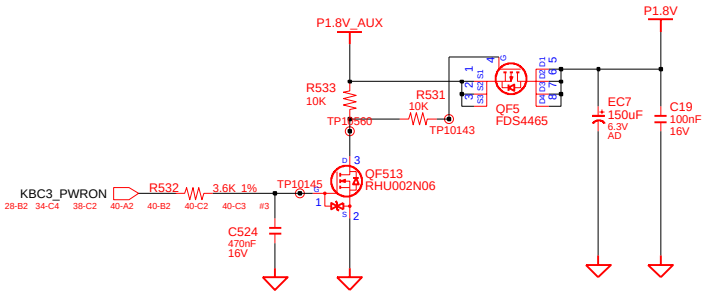
Switched Power On (P3.3V)



Switched Power On (P1.5V)



Switched Power On (P1.8V)



DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN MICOM & SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
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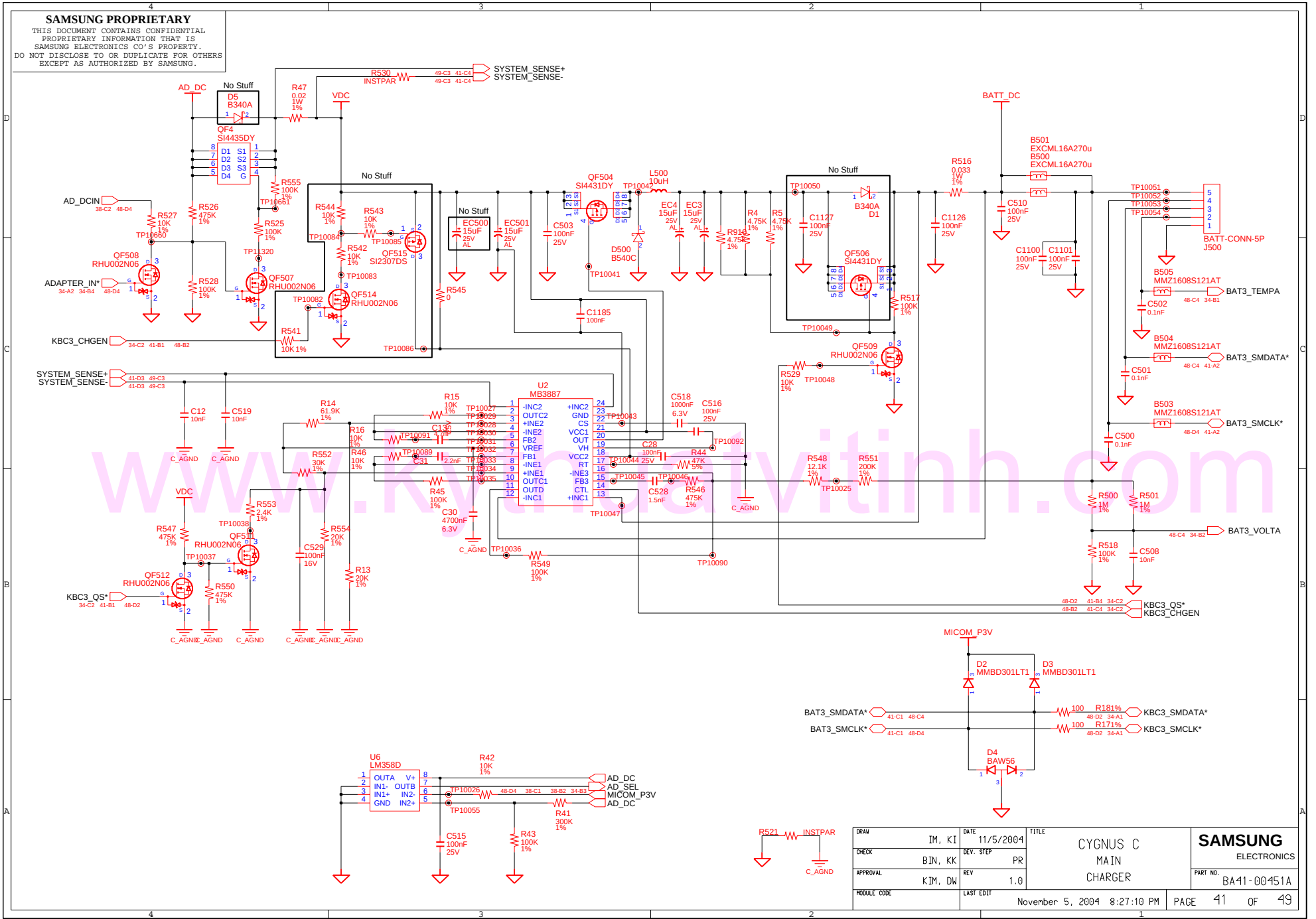

DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
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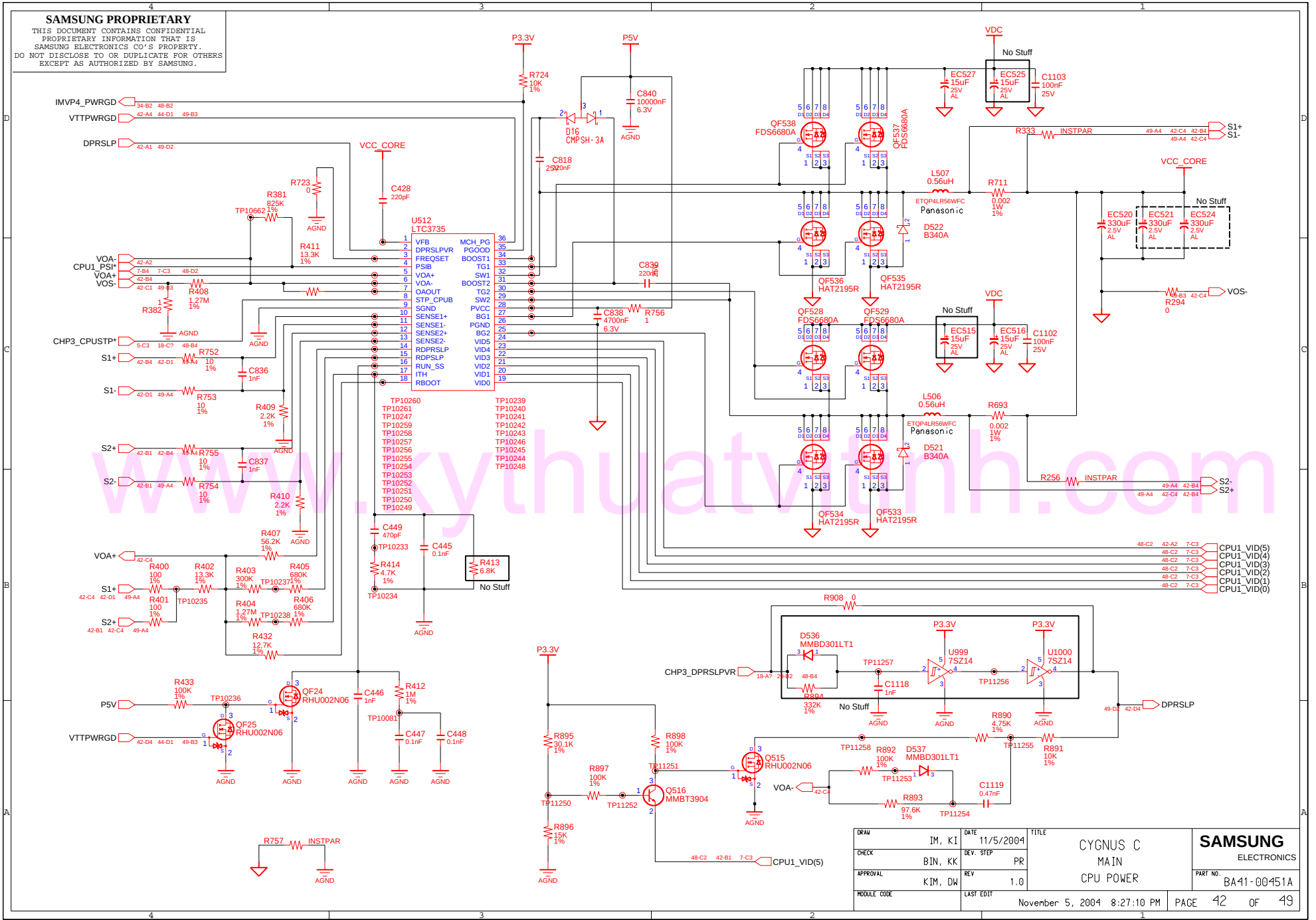

DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN CPU POWER	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
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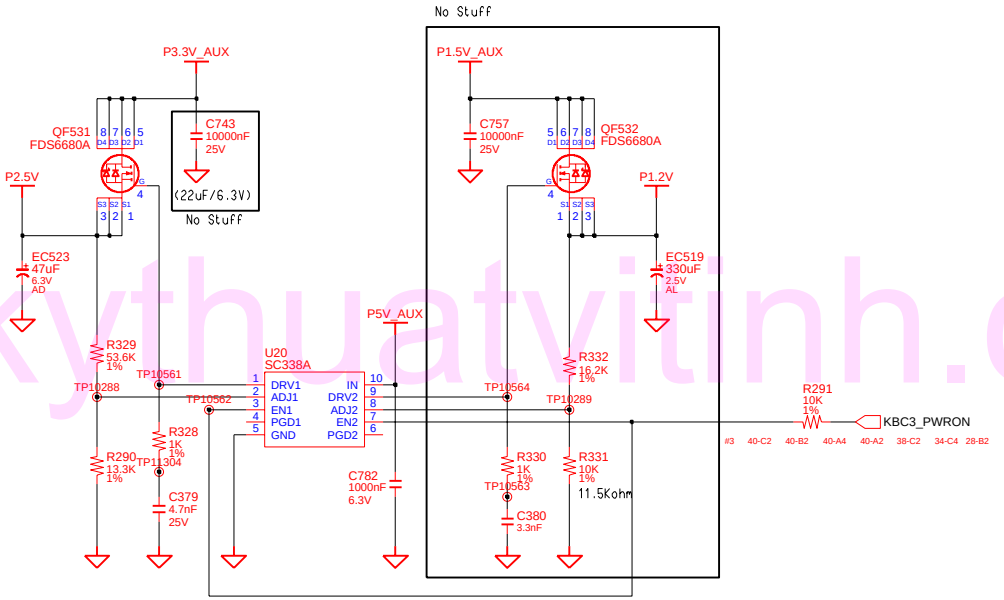
P2.5V&P1.2V



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DRAW: IM, KI	DATE: 11/5/2004	TITLE: CYGNUS C MAIN P2.5V & P1.2V	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
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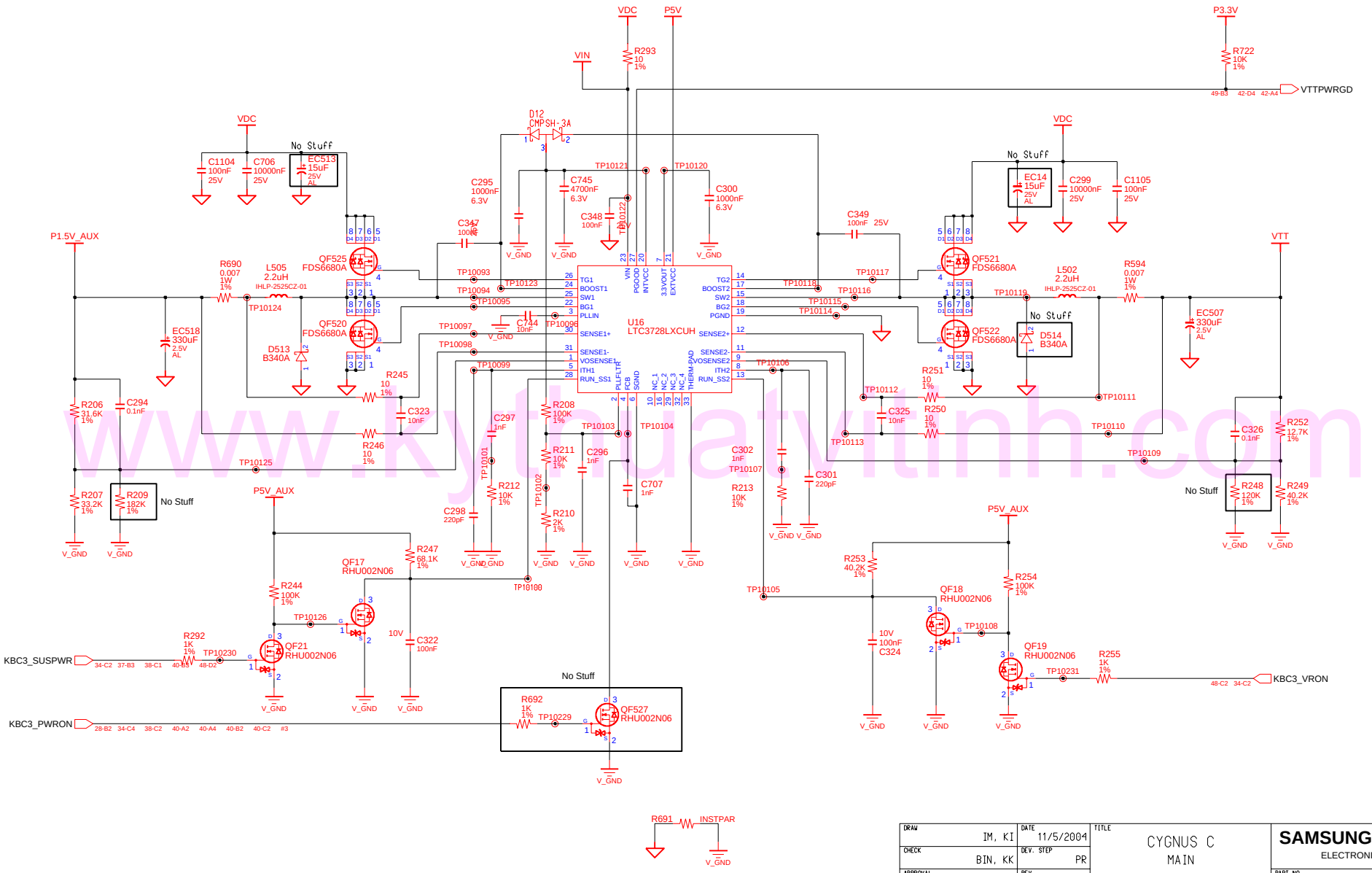

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CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00451A
APPROVAL: KIM, DW	REV: 1.0		
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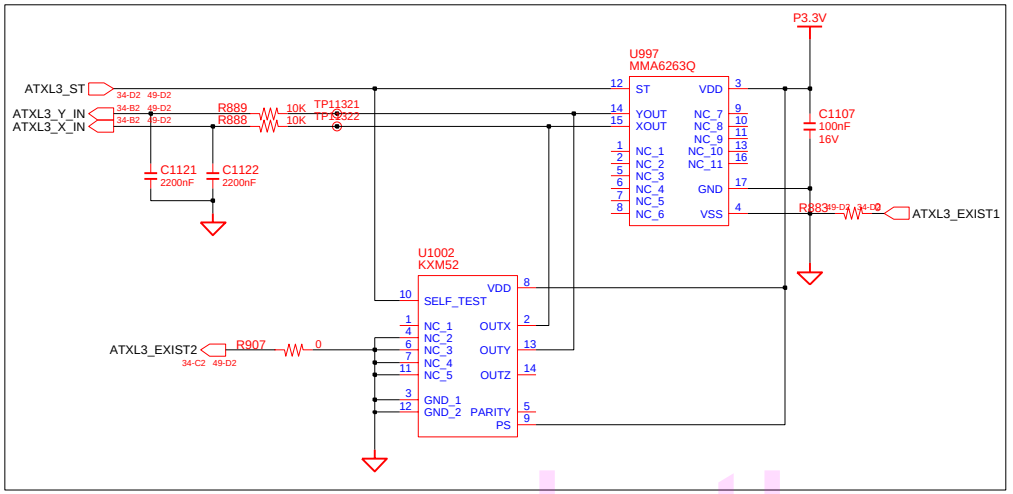
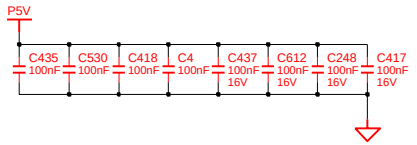
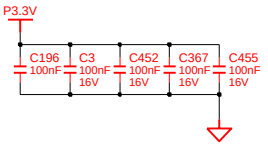
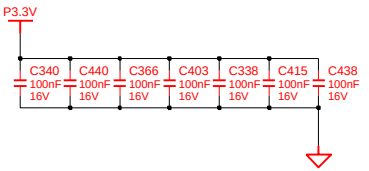
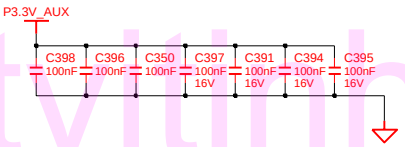
AIRBAG

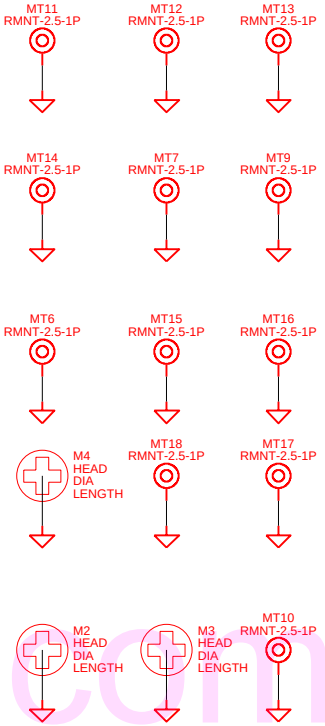












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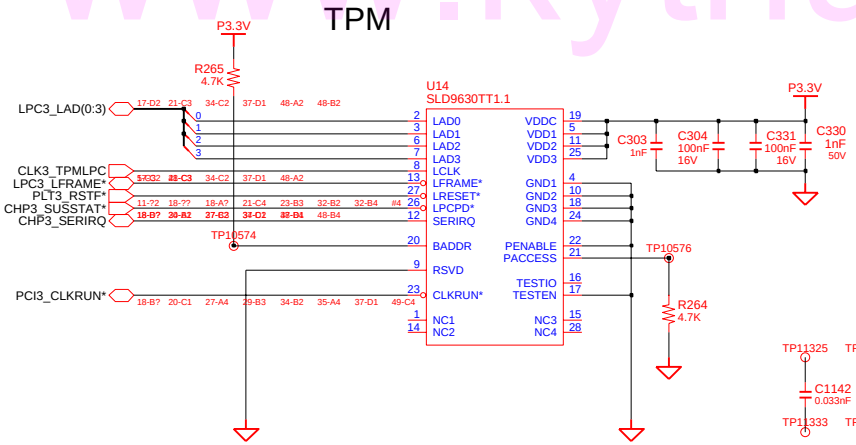
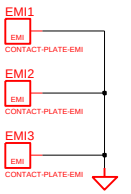
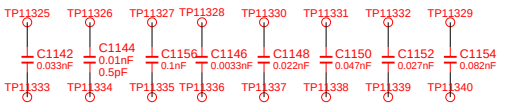
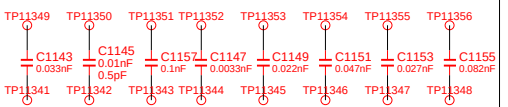
TPM



PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			







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CHECK	BIN, KK	DEV. STEP	PR		SAMSUNG ELECTRONICS
APPROVAL	KIM, DW	REV	1.0		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM		PAGE 45 OF 49

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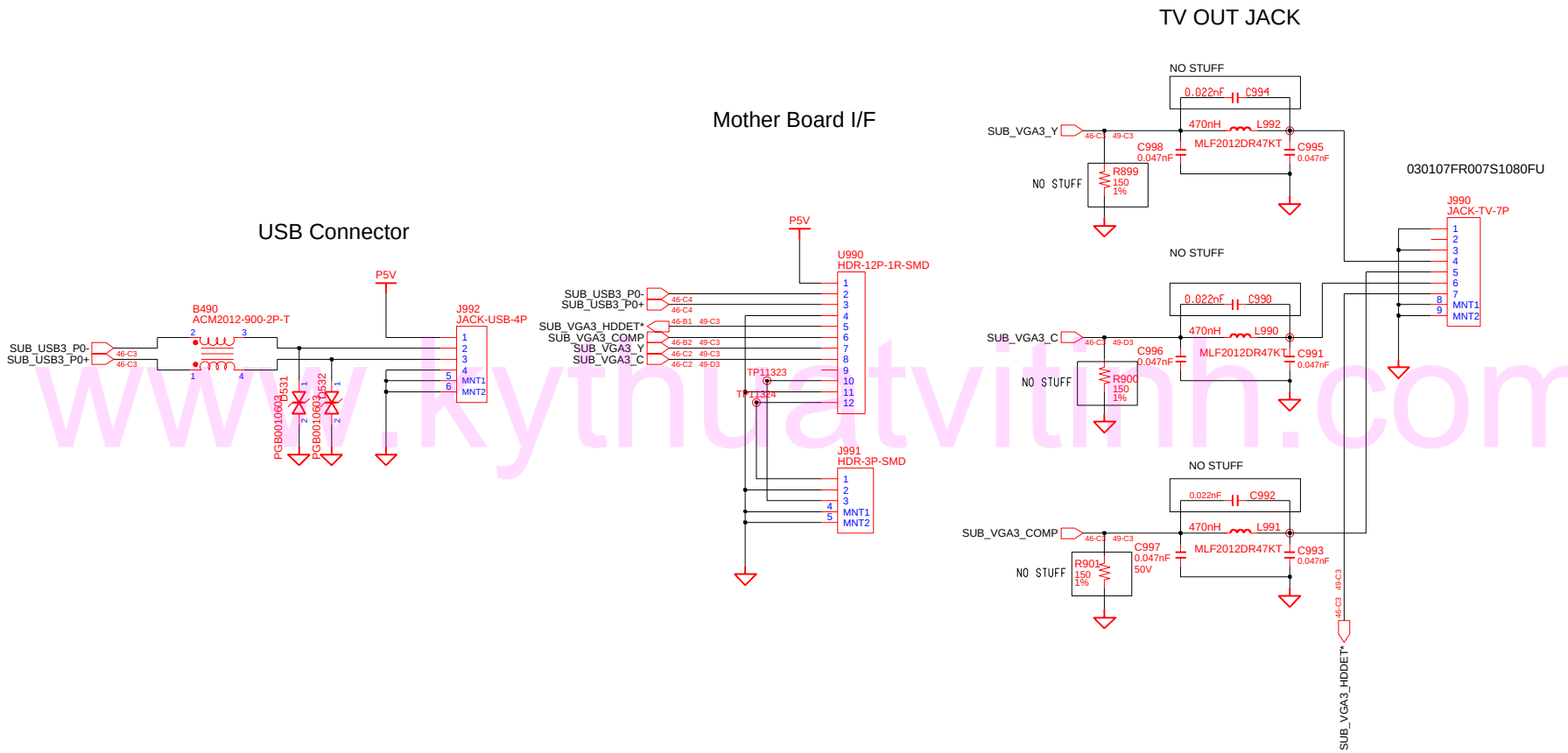
< USB BOARD >



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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
	AD21	3	
MiniPCI SLOT1	AD23	2	D,E
USB	AD29(internal)	-	USB2.0 #0 : A
			USB2.0 #1 : D
			USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
		-	A,B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	Northwood-B
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	(Interposer B'd)
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
Highest Freq. 0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V	Lowest Freq.
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V	
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V	
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V	Deeper Sleep
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V	
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V)
	MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

I C / SMB Address

Devices	Address	Hex	Bus
ICH6	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO	
0	SYSTEM PORT A	
1,2	SYSTEM PORT B	
3	BLUETOOTH	OPTION
4	FINGER PRINT	OPTION

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

REVISION HISTORY

See rev notes in the changes file for more information.

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DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		
APPROVAL: KIM, DW	REV: 1.0		PART NO. BA41-00450A
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 4 OF 51

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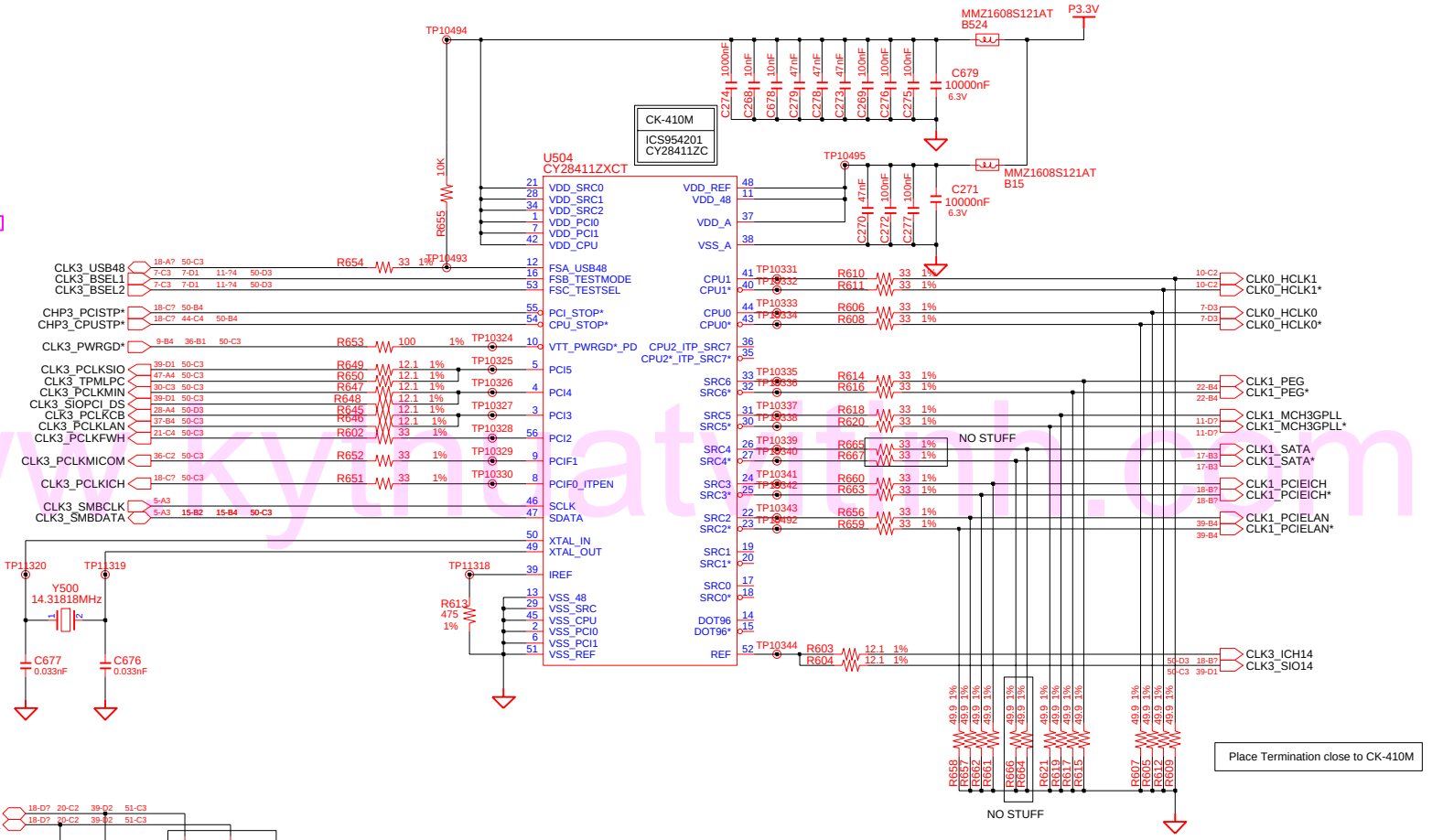
FSA BSEL2	FSB BSEL1	FSC BSEL0	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		
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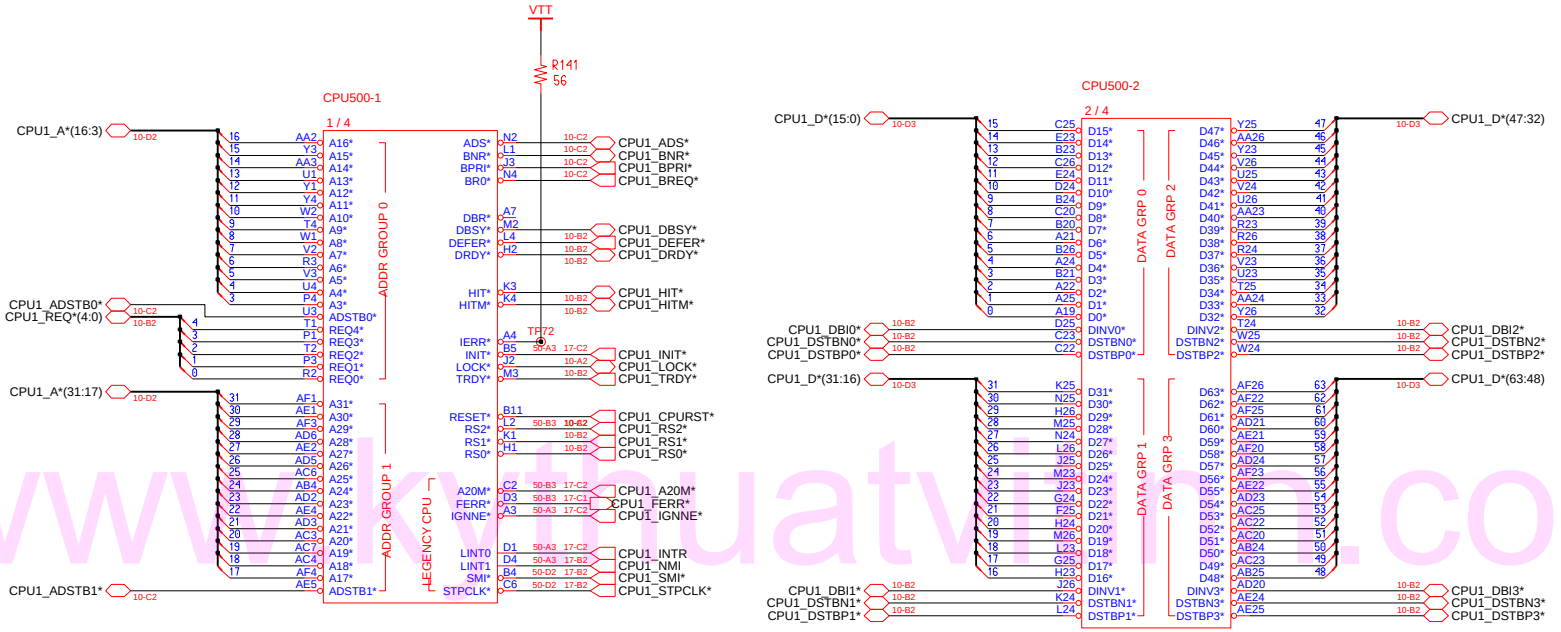

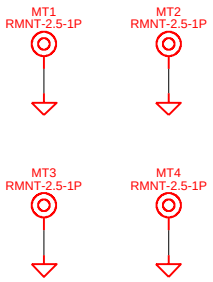

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CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
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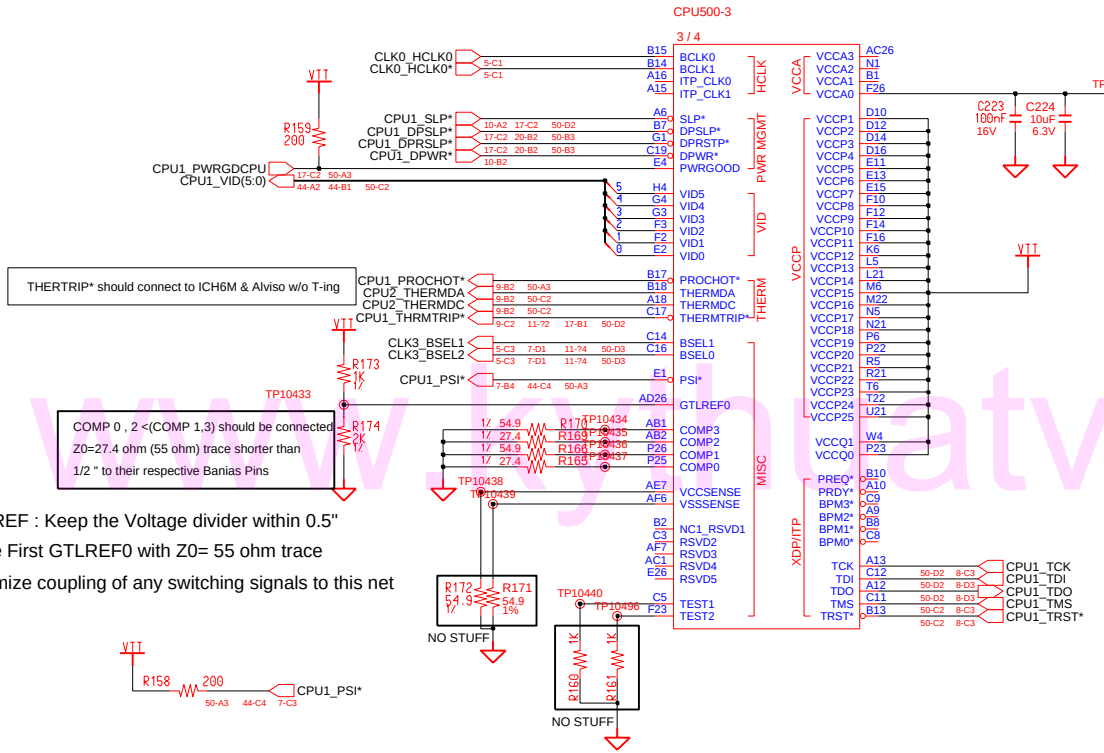
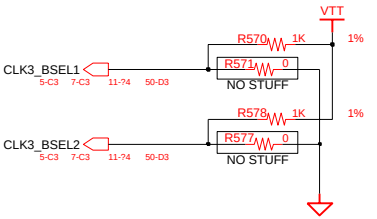


THERTRIP* should connect to ICH6M & Alviso w/o T-ing

COMP 0 , 2 <(COMP 1,3) should be connected
Z0=27.4 ohm (55 ohm) trace shorter than
1/2 " to their respective Banias Pins

GTLREF : Keep the Voltage divider within 0.5"
of the First GTLREF0 with Z0= 55 ohm trace
Minimize coupling of any switching signals to this net



	STUFF	NO STUFF
Dothan400 A-Step	R575 R578 R577 R582 R579 R580	R574 R581 R576 R583
Dothan533 A-Step	R576 R578 R577 R582 R579 R580	R574 R581 R575 R583
FutureDothan(B-Step*)	R574 R581 R578 R575 R577 R580 R579 R583	R576 R582

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 1 1	1.596 V	1 0 0 1 1 1	1.084 V
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V Lowest Freq.
0 1 0 1 1 1	1.340 V	1 1 0 1 1 1	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V Deeper Sleep
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

Highest Freq. of Dothan400(1.8GHz)
* Highest Freq. of Dothan533(?? GHz : TBD)

DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN DOTHAN CPU(2/3)	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		
APPROVAL: KIM, DW	REV: 1.0		PART NO. BA41-00450A
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 7 OF 51

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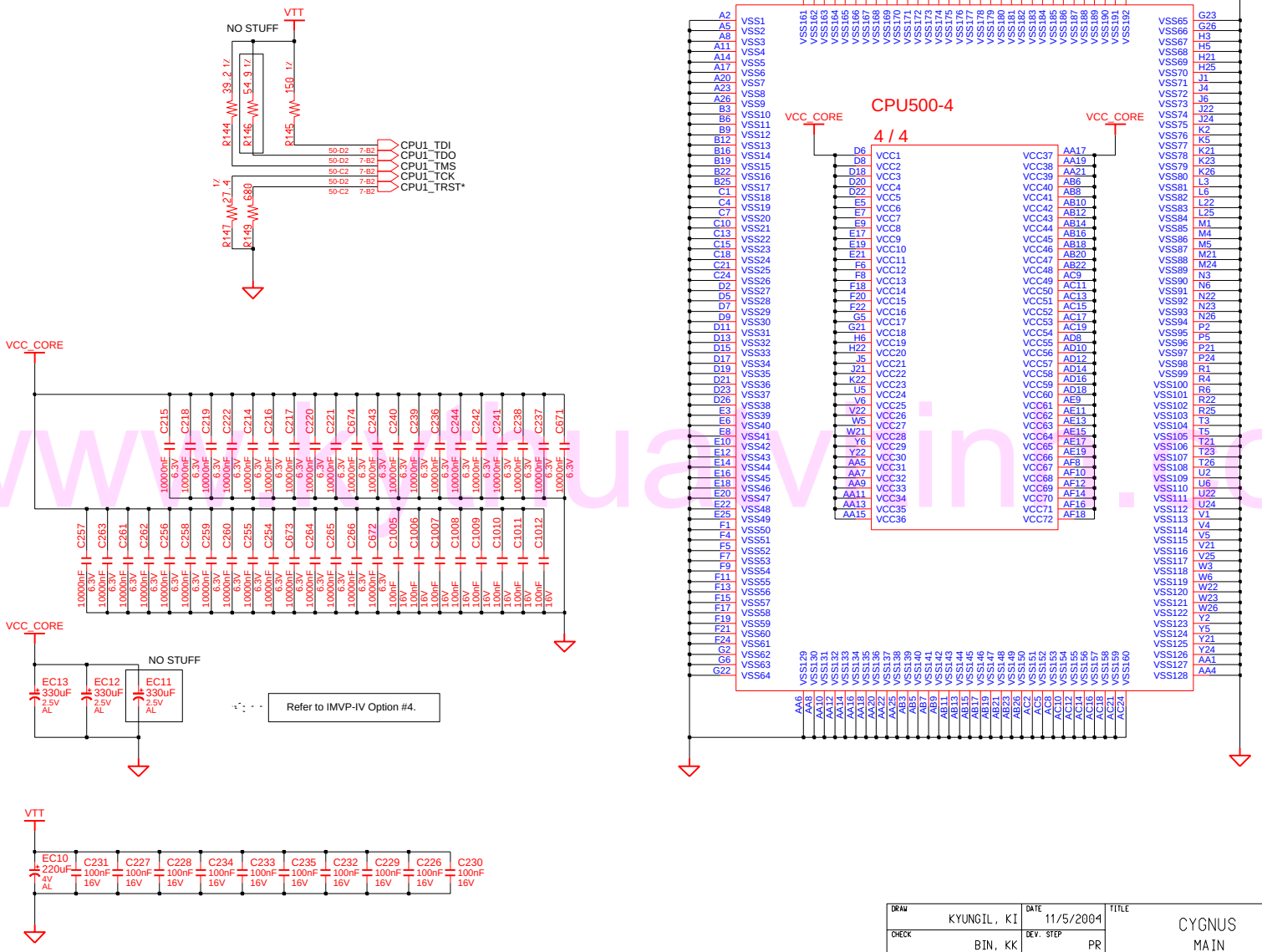
Refer to Sonoma Platform Design Guide(4.6.1.4)



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DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN DOTHAN CPU(3/3)	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
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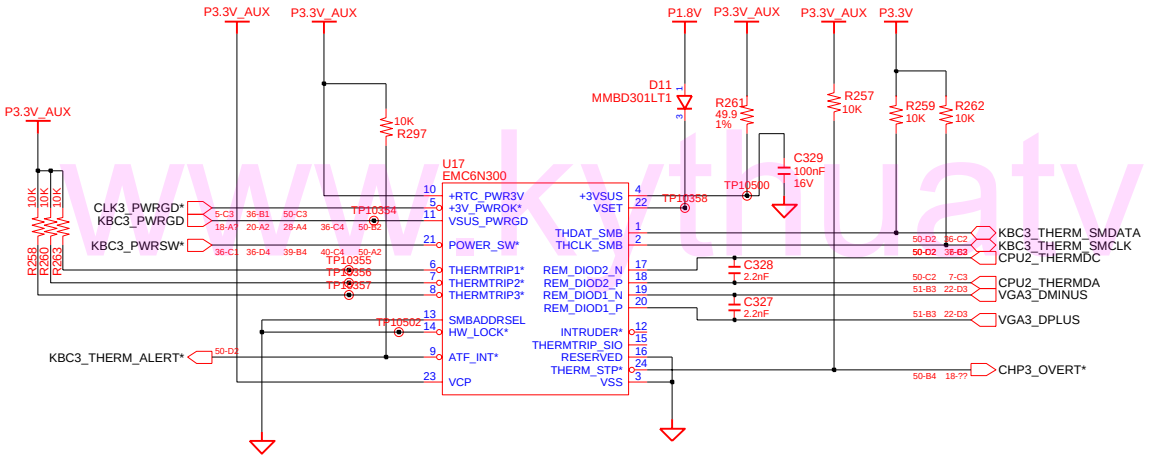
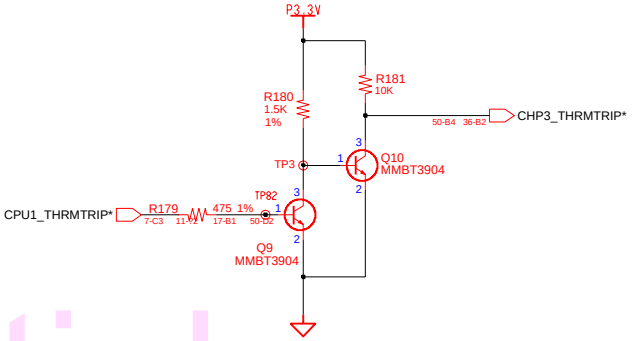
Refer To Thermal Sensor Layout Guidelines.

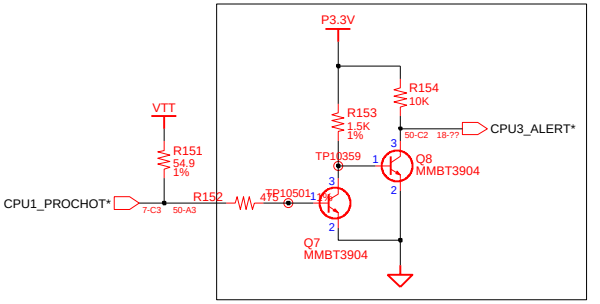
- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

CPU / DDR Thermal Sensor





NO STUFF



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DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN THERMAL SENSOR/FAN CONTRL	SAMSUNG ELECTRONICS
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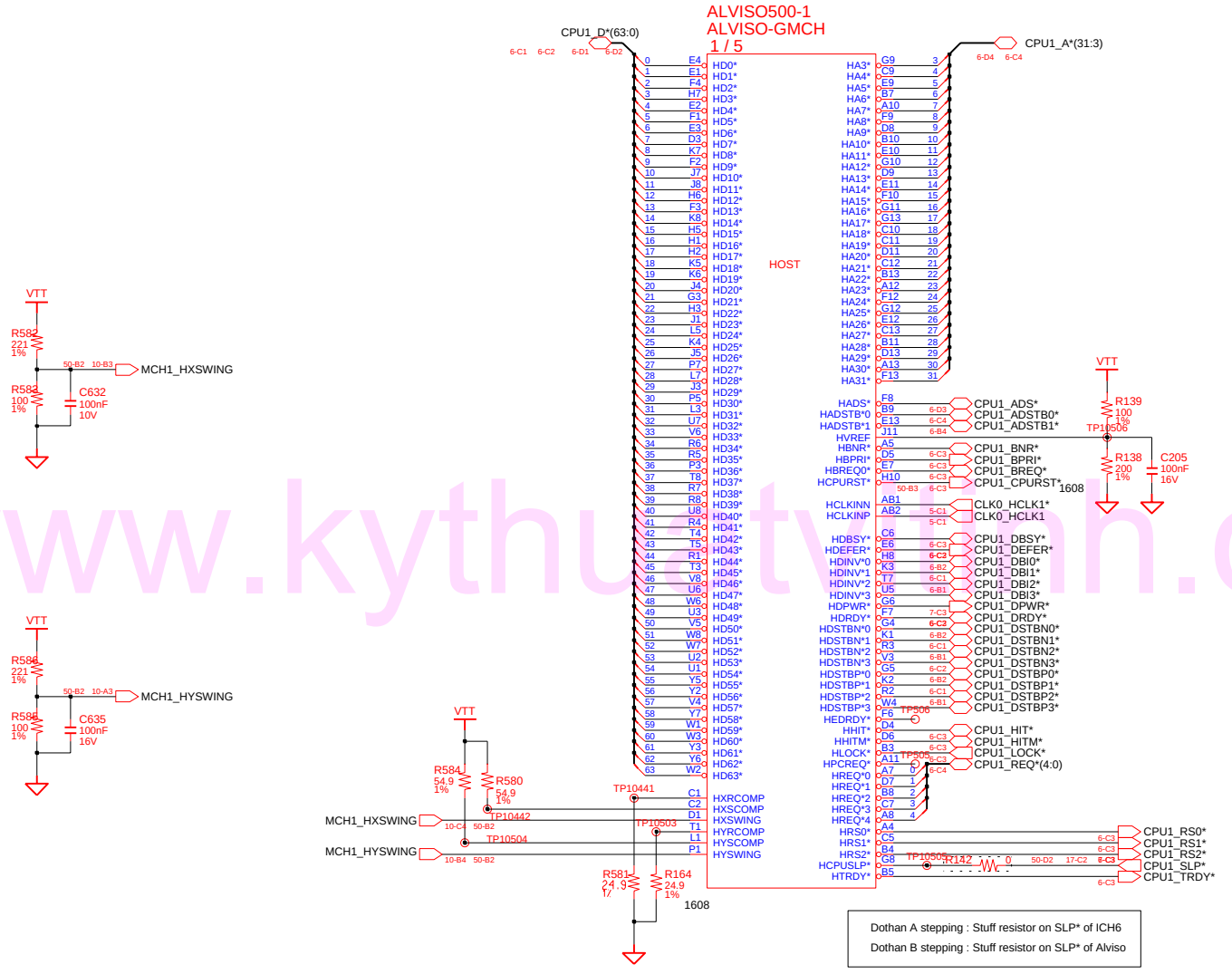

Dothan A stepping : Stuff resistor on SLP* of ICH6

Dothan B stepping : Stuff resistor on SLP* of Alviso

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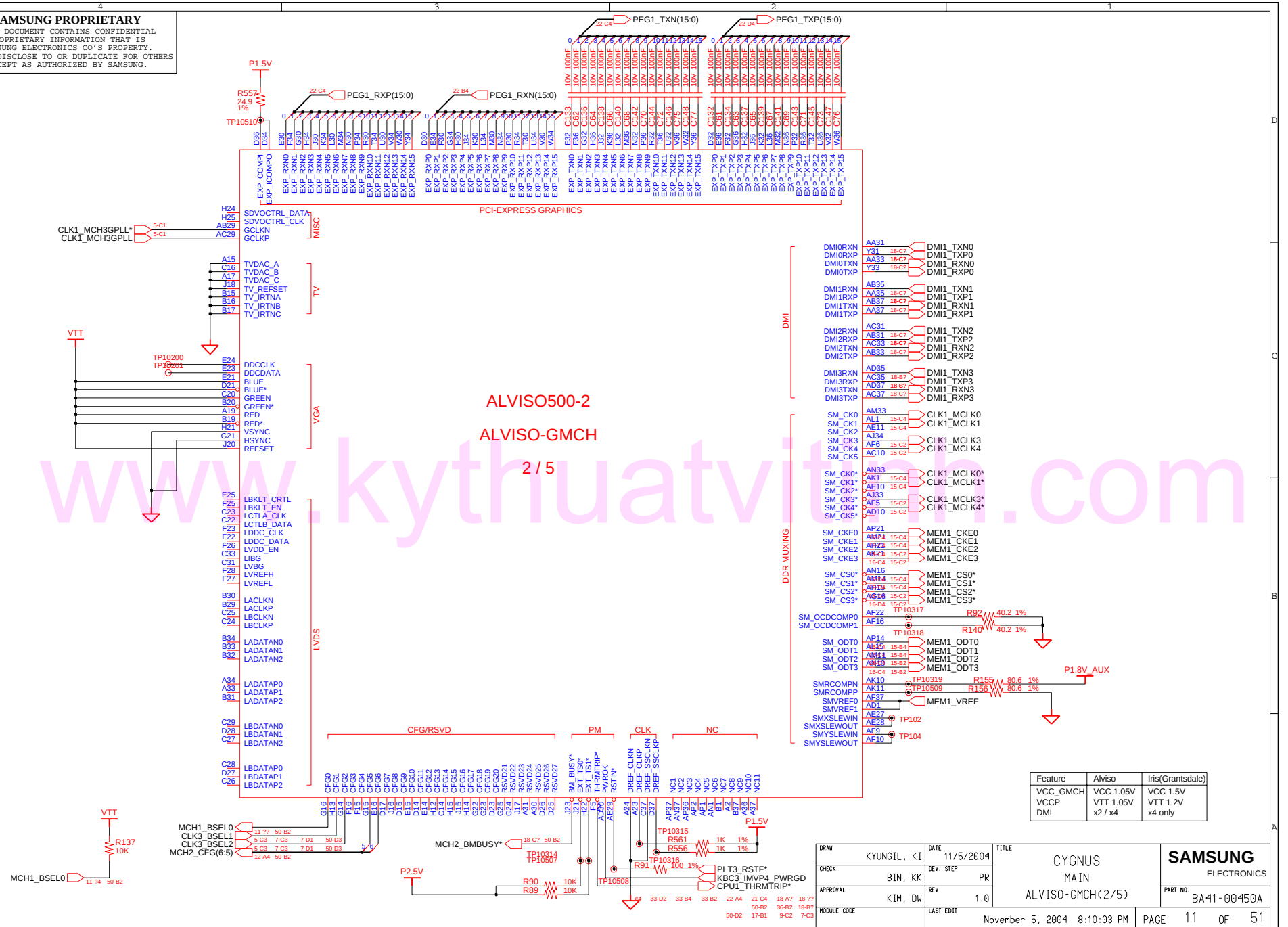

Feature	Alviso	Iris(Grantsdale)
VCC_GMCH	VCC 1.05V	VCC 1.5V
VCCP	VTT 1.05V	VTT 1.2V
DMI	x2 / x4	x4 only

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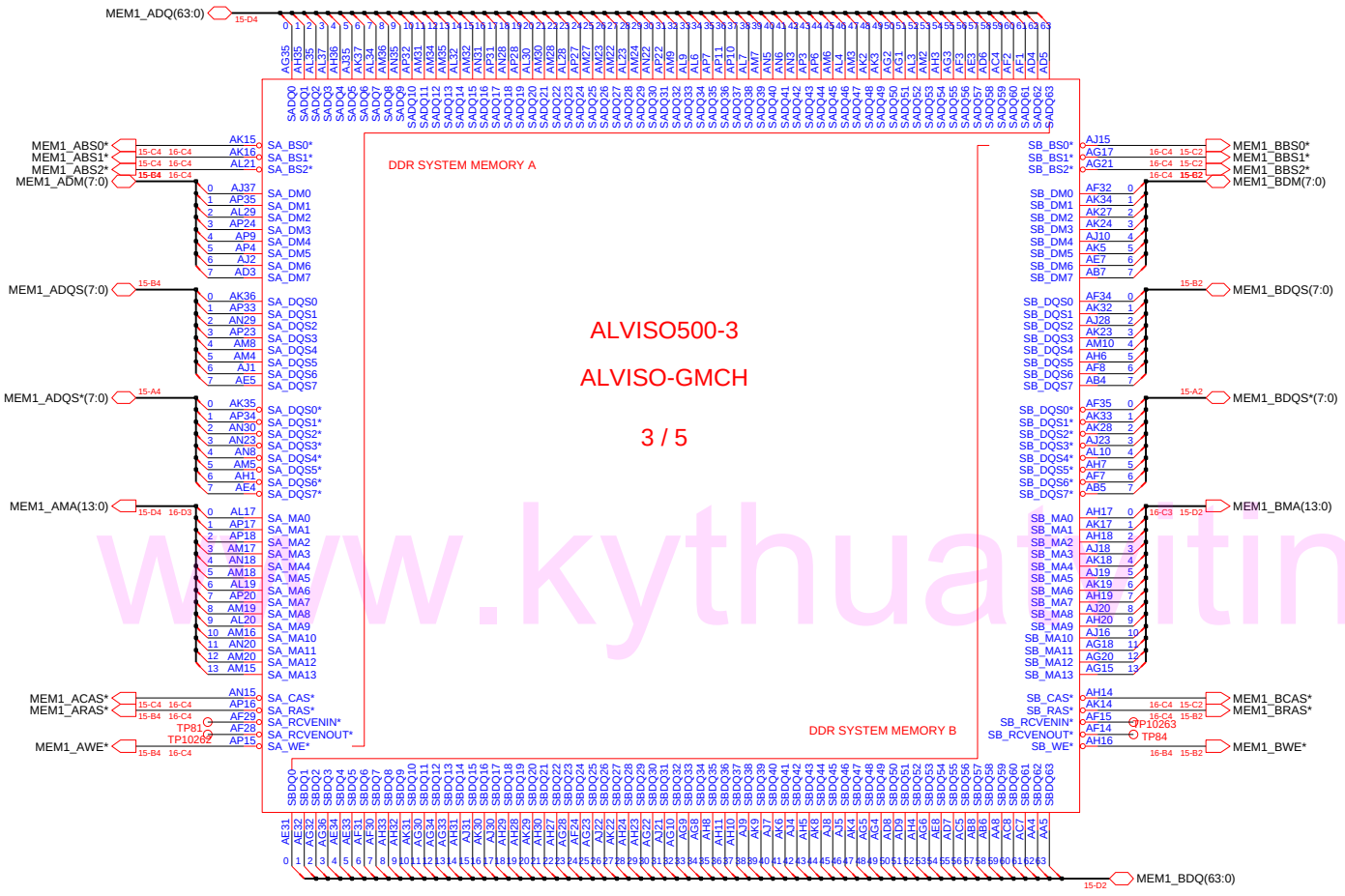

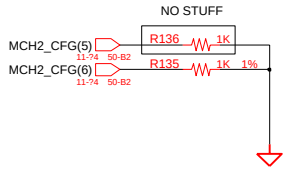

DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA	
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

def. : default Option

CFG#	Low	High
CFG(5)	DMIx2	DMIx4 (def.)
CFG(6)	DDR-2	DDR-1
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(10)	TBD	TBD
CFG(11)	TBD	TBD
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

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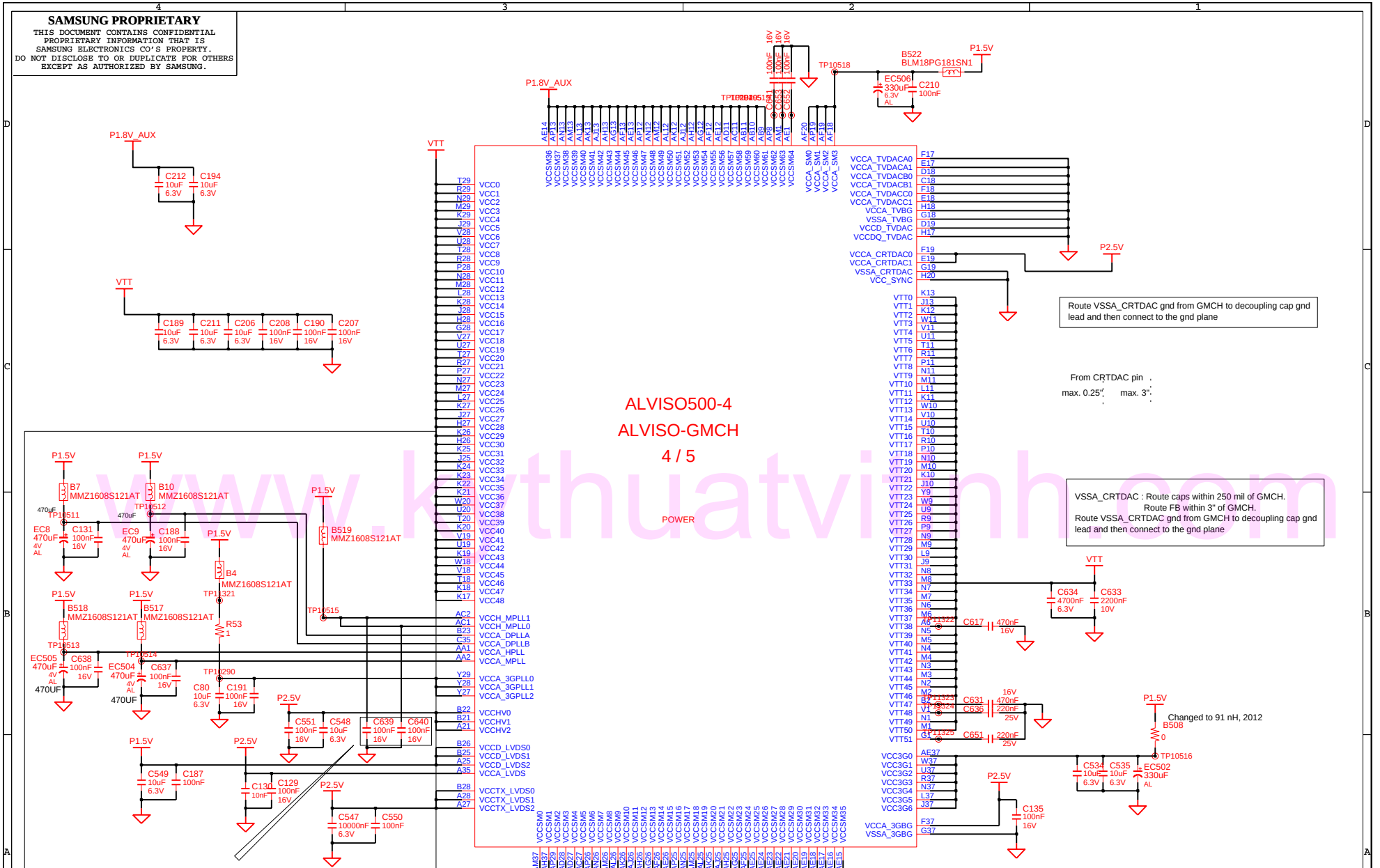

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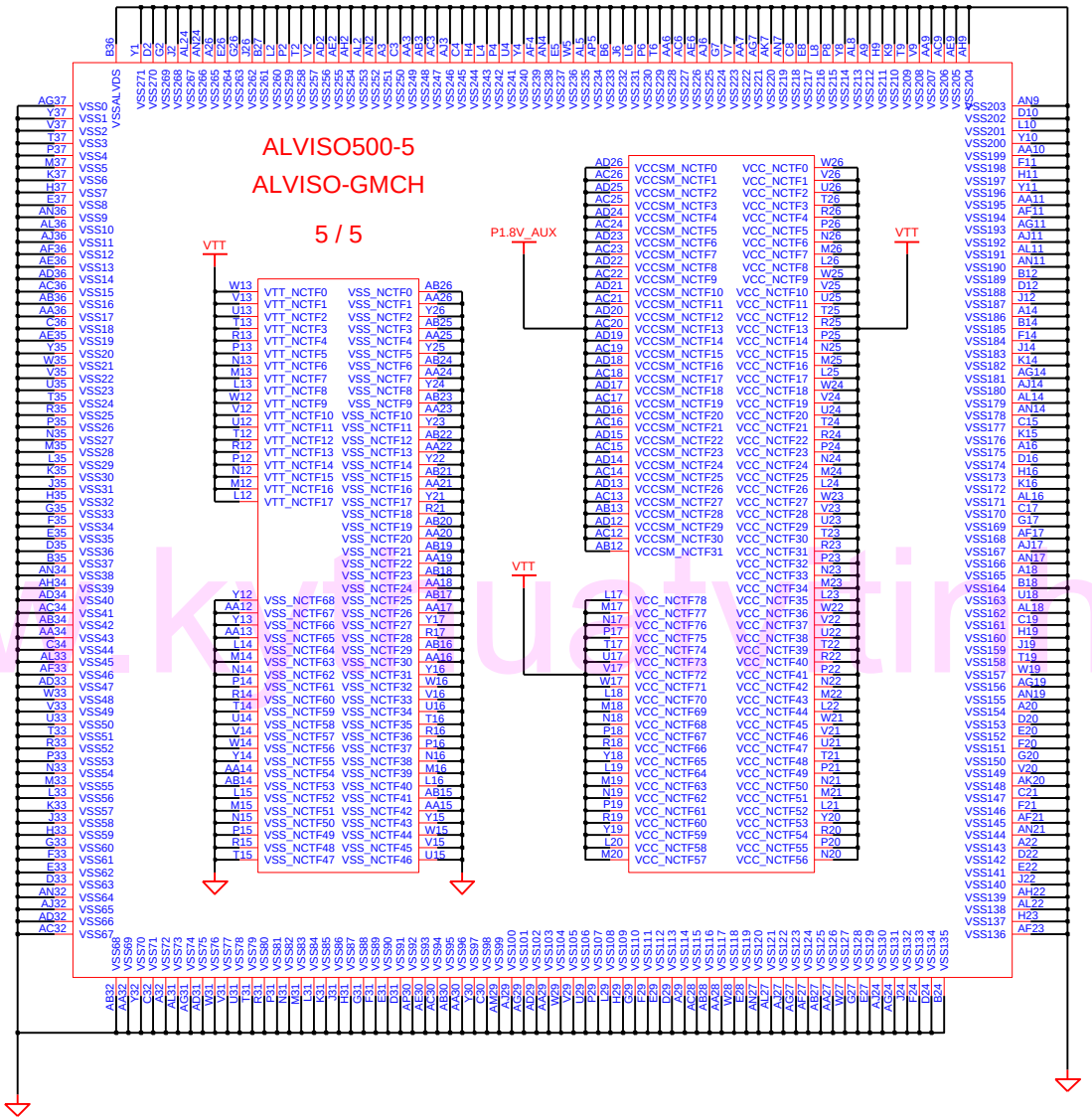

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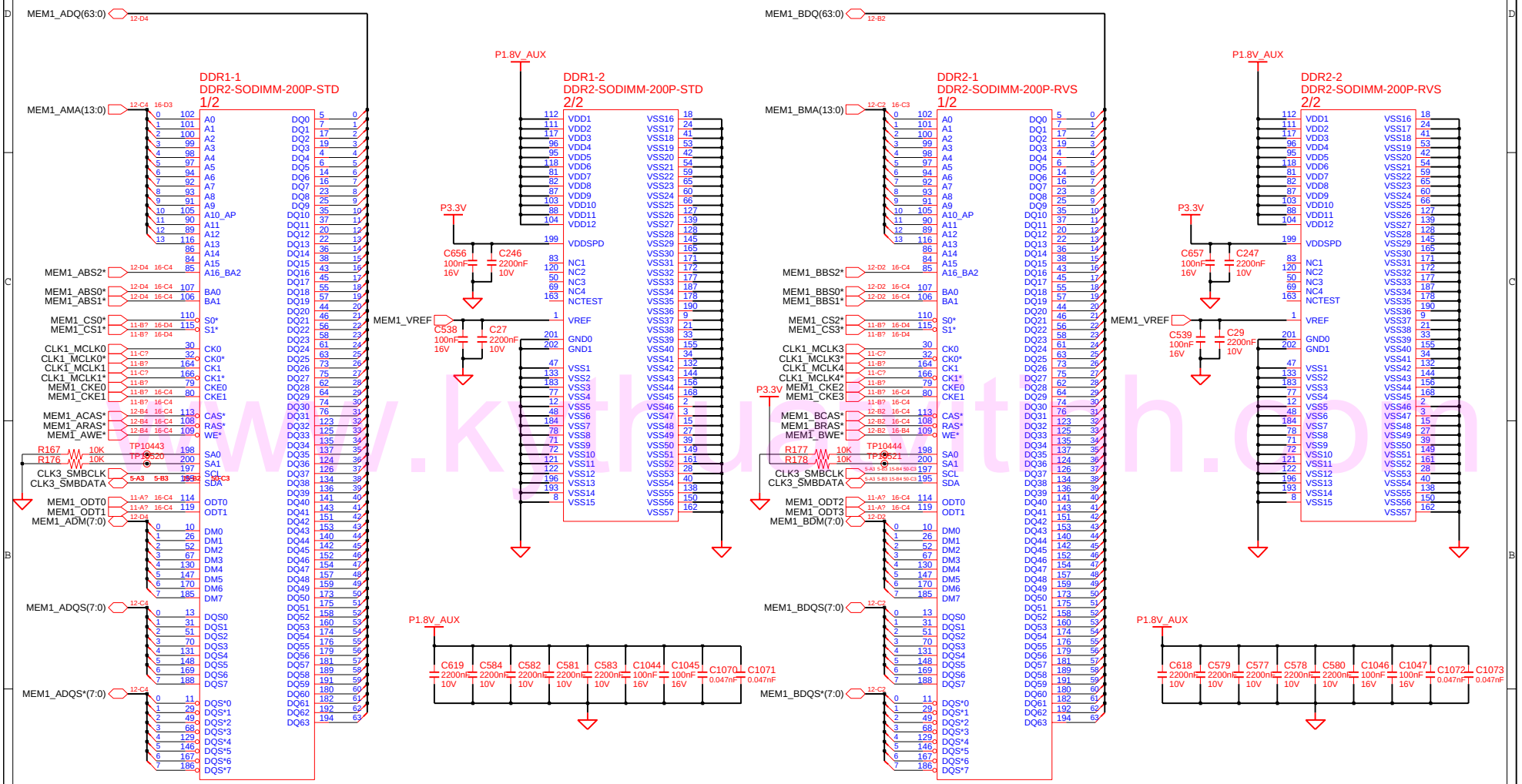

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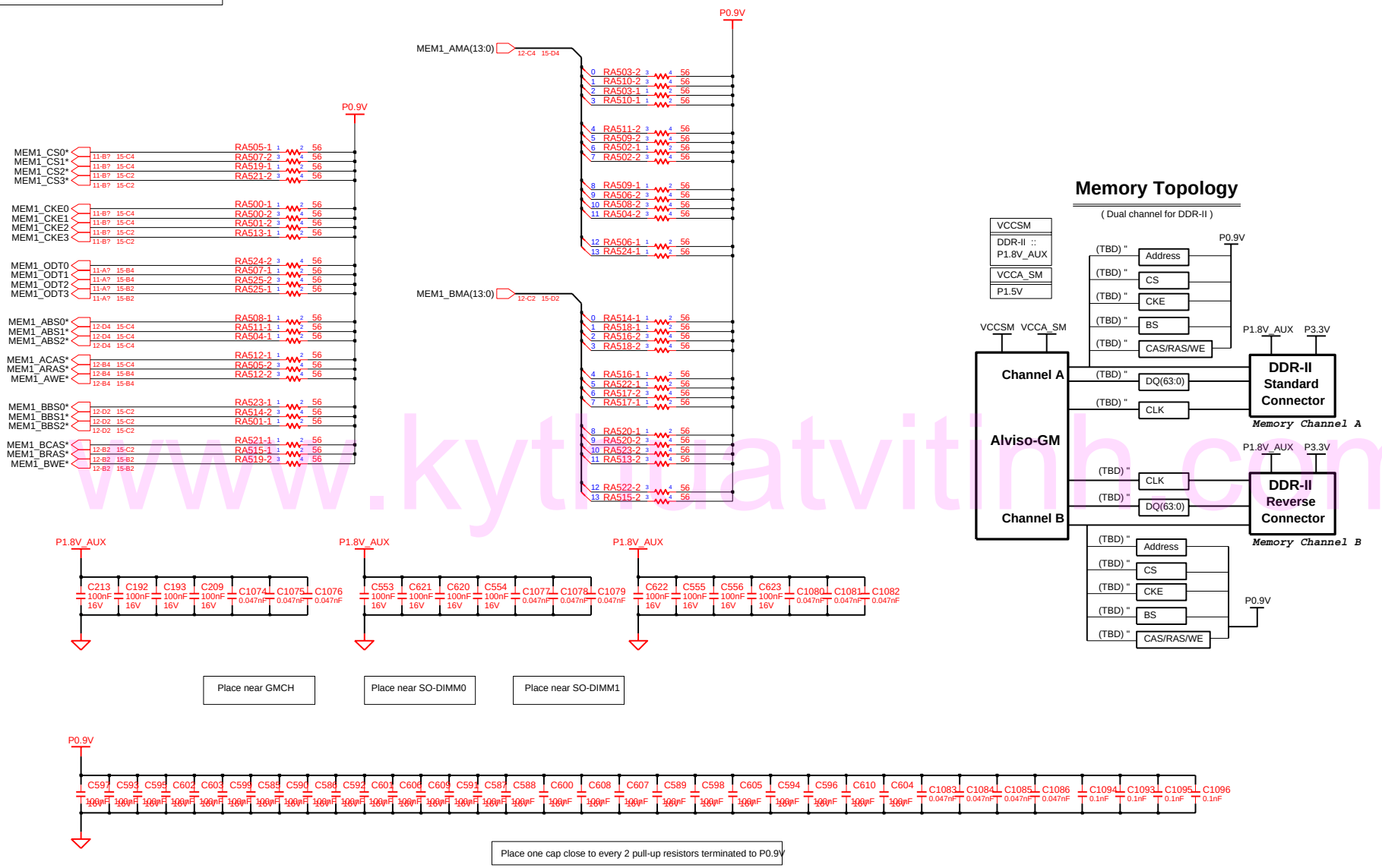

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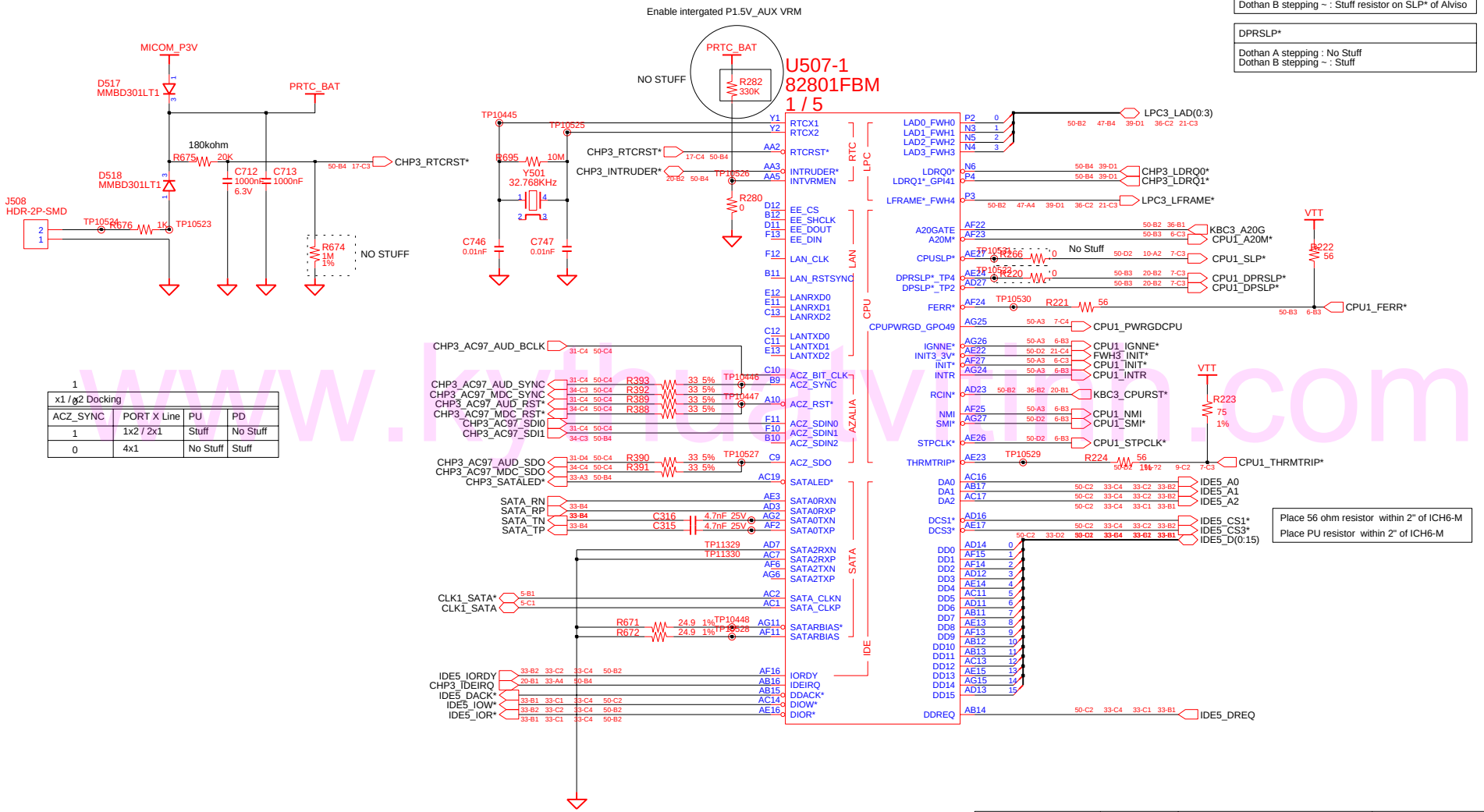
CPUSLP*
Dothan A stepping : Stuff resistor on SLP* of ICH6 Dothan B stepping ~ : Stuff resistor on SLP* of Alviso

DPRSLP*
Dothan A stepping : No Stuff Dothan B stepping ~ : Stuff



Place 56 ohm resistor within 2" of ICH6-M
Place PU resistor within 2" of ICH6-M

1

x1 / x2 Docking			
ACZ_SYNC	PORT X Line	PU	PD
1	1x2 / 2x1	Stuff	No Stuff
0	4x1	No Stuff	Stuff

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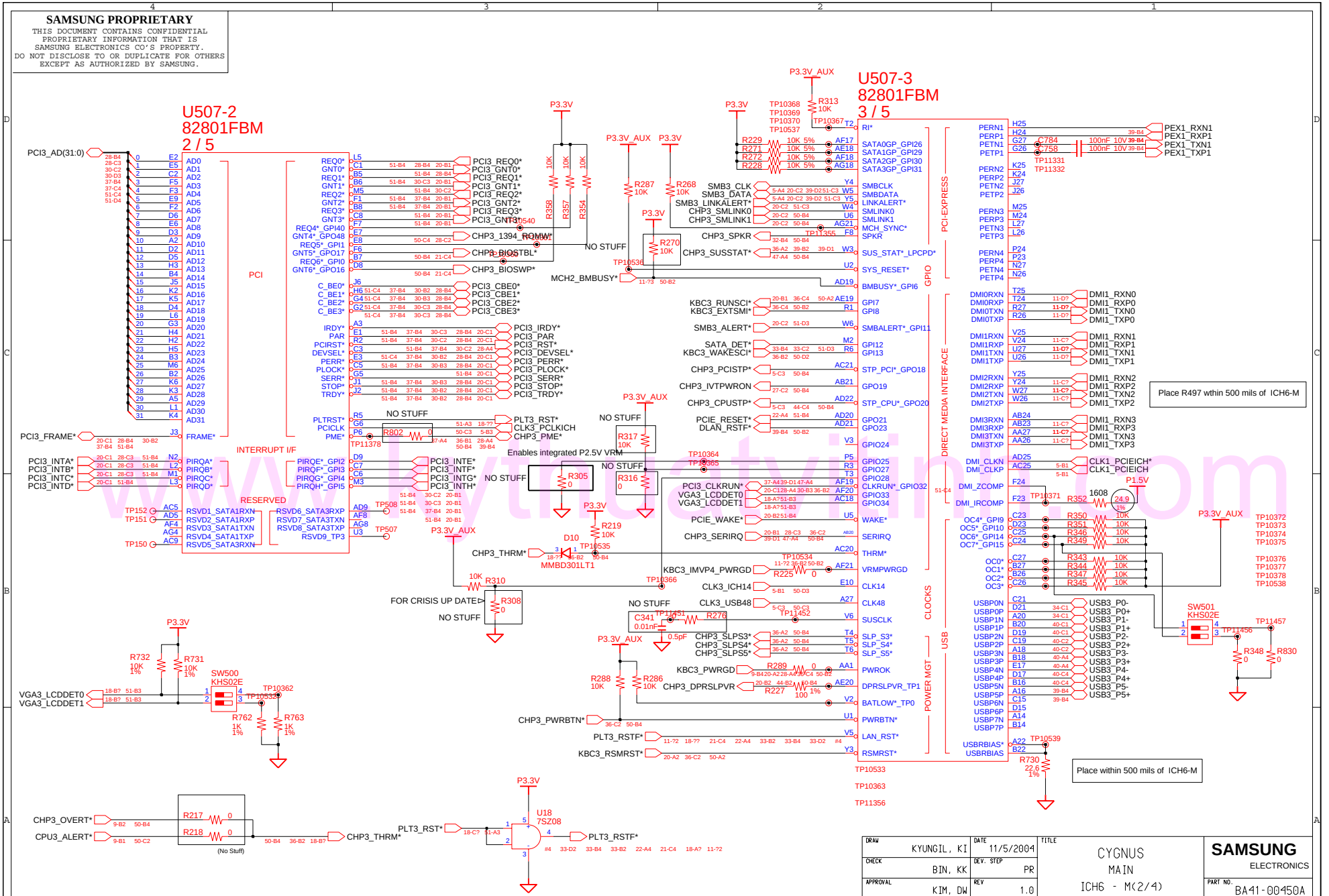

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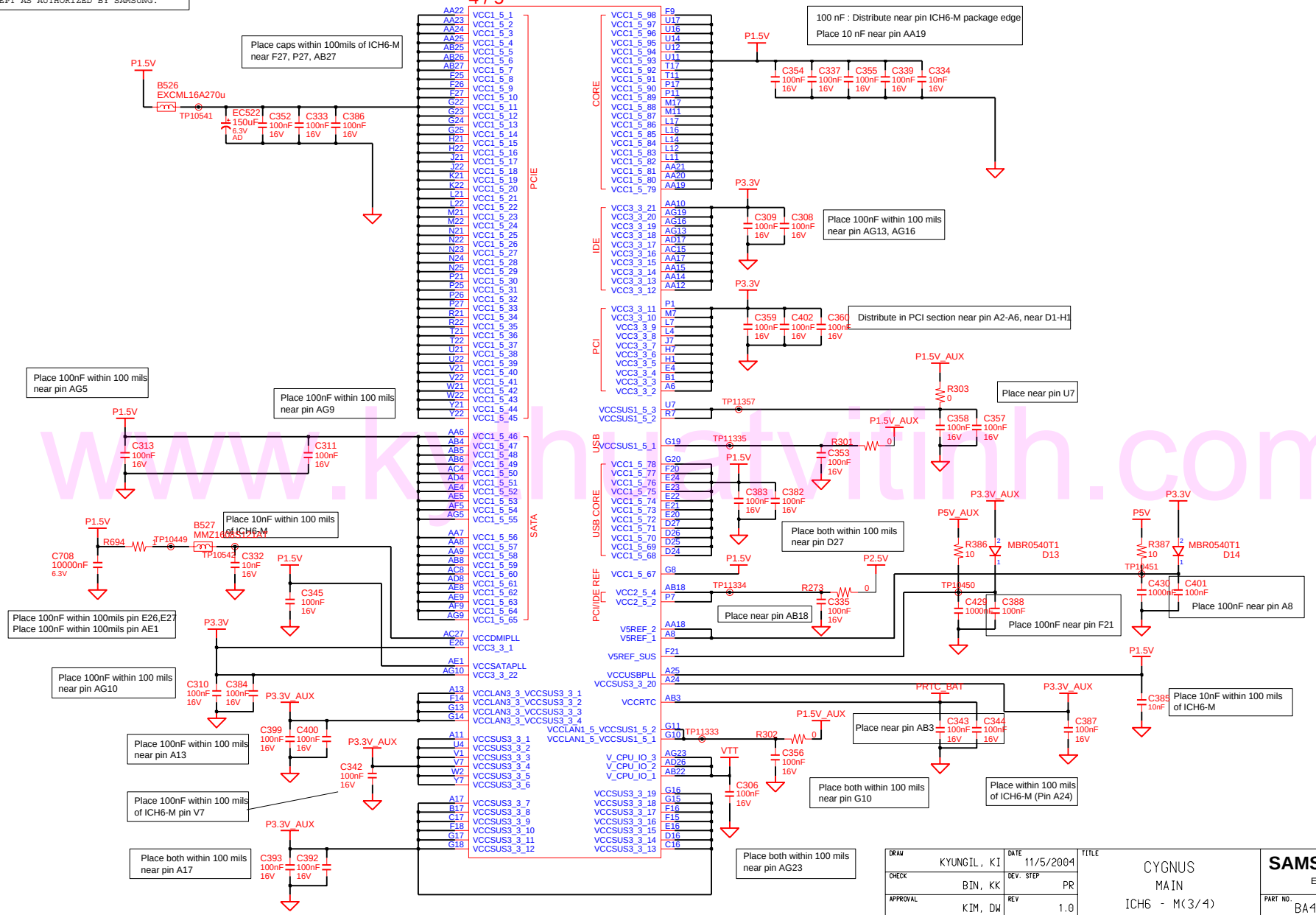

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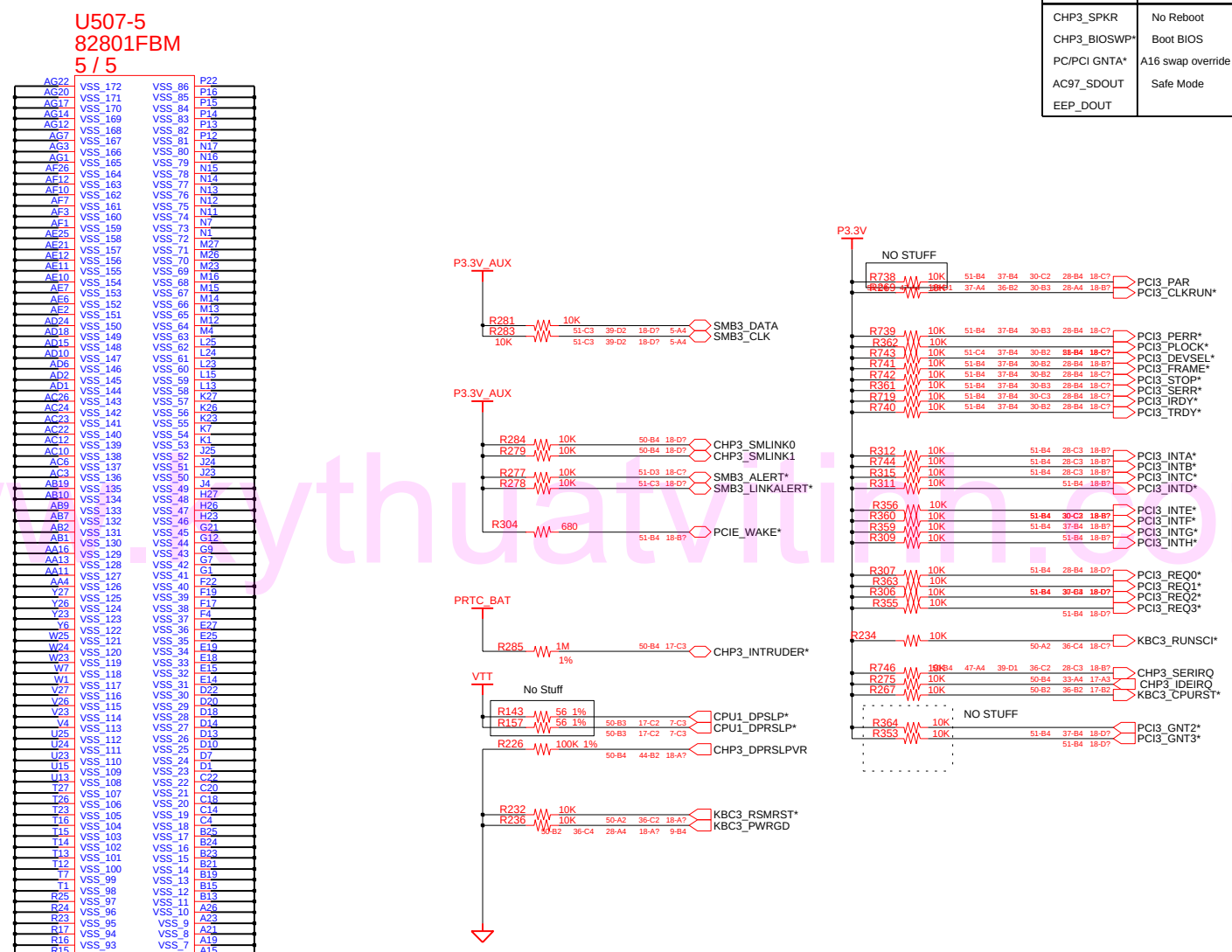
ICH6-m Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
EEP_DOUT		TBD



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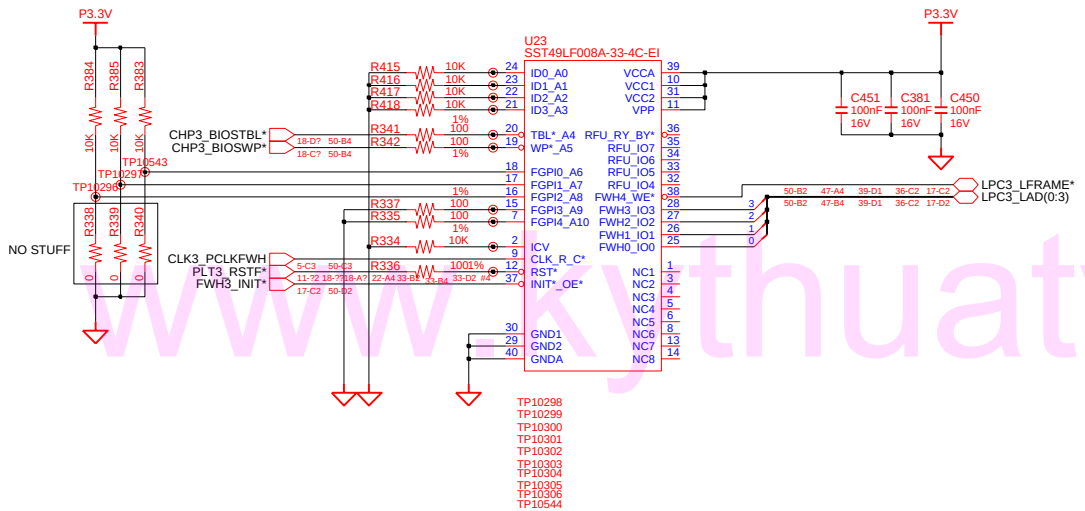

02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
OE	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUP CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY " PRESS ..... SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM GETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

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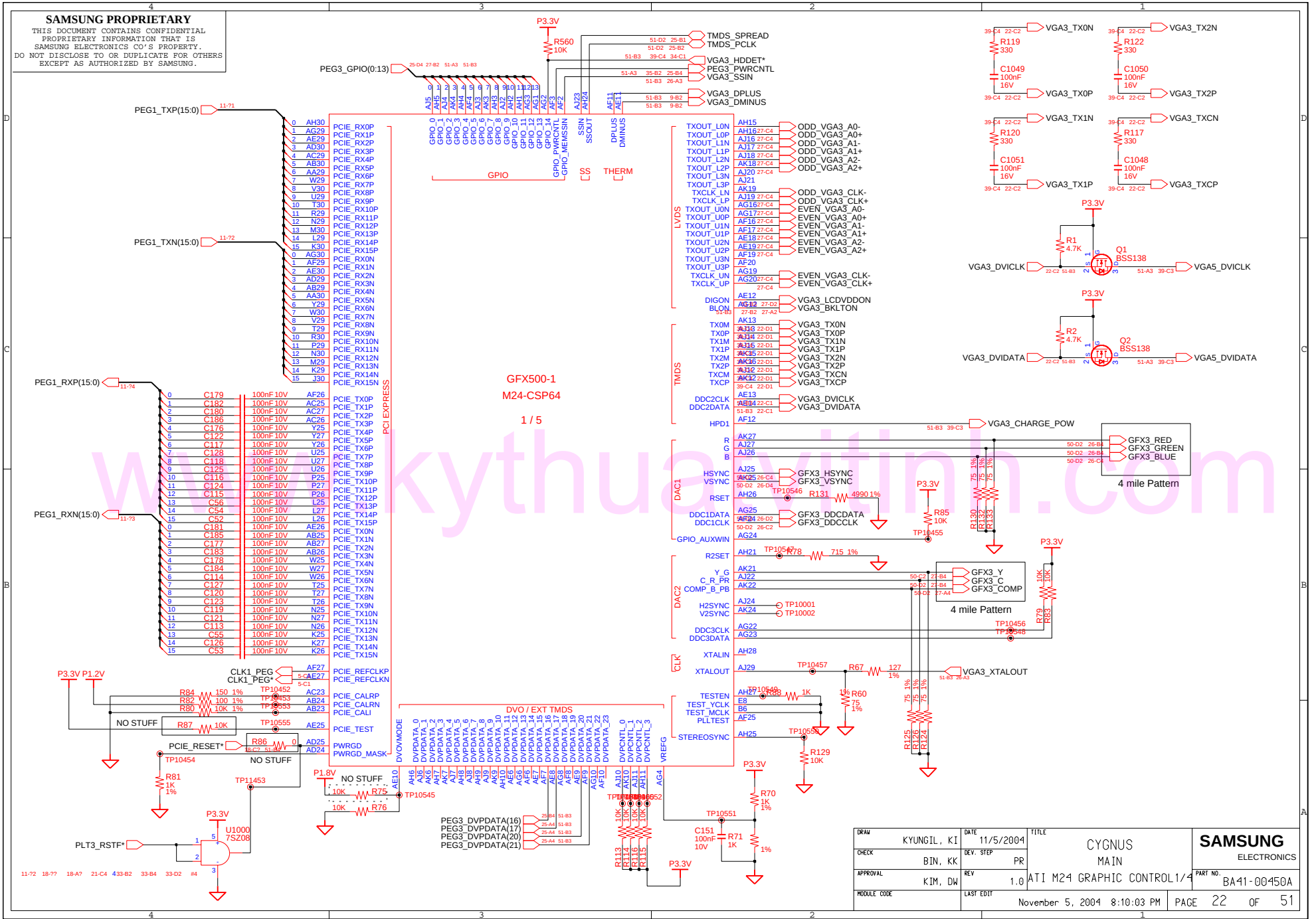

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APPROVAL: KIM, DW	REV: 1.0	ATI M24 GRAPHIC CONTROL1/4	PART NO. BA41-00450A
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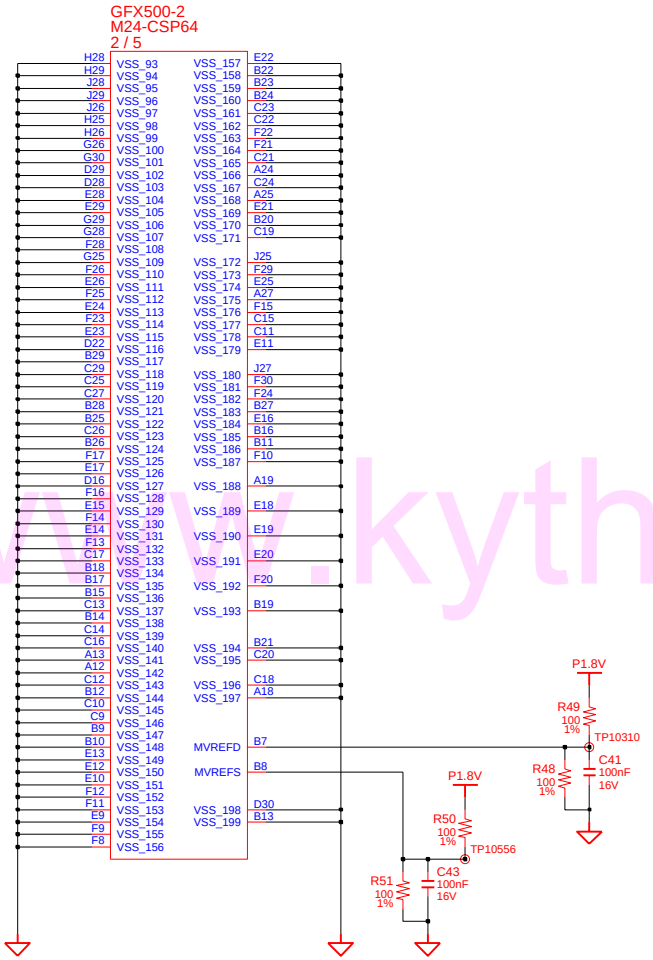

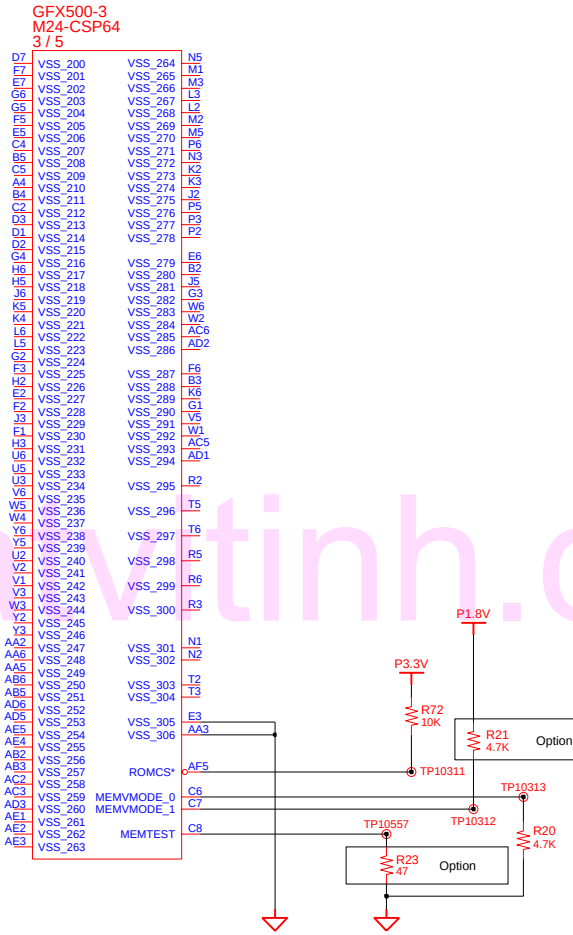

VDDR1	M24	M26
MEMVMODE	4.7K Pull Up	NC
MEMTEST	47 ohm	240 ohm

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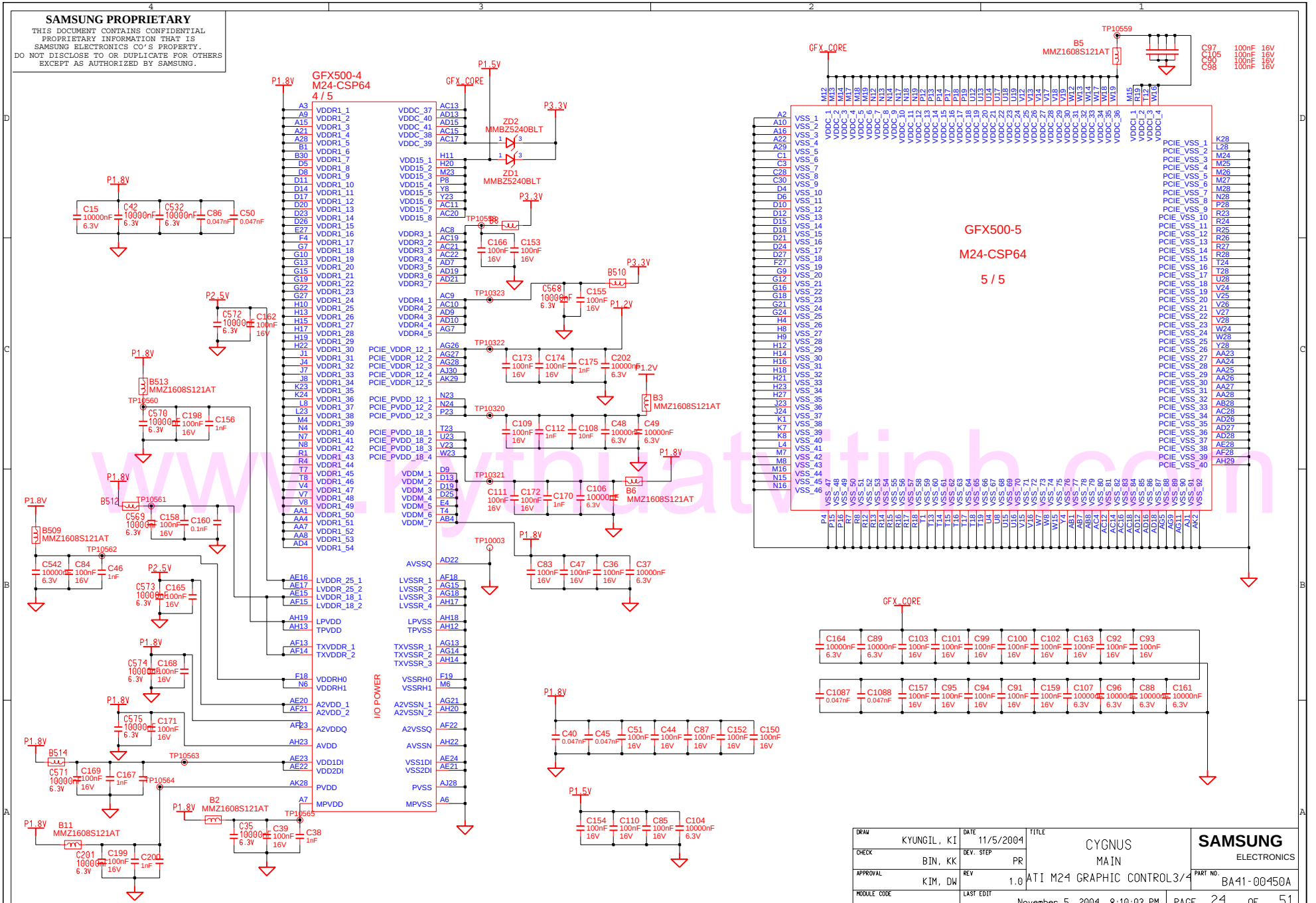

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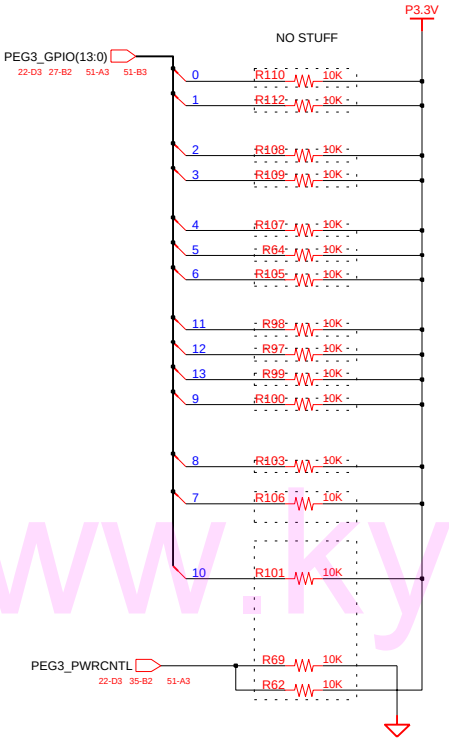
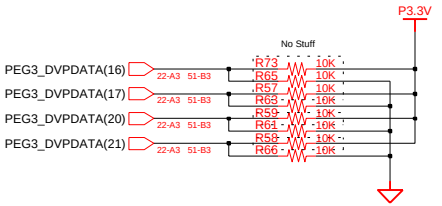
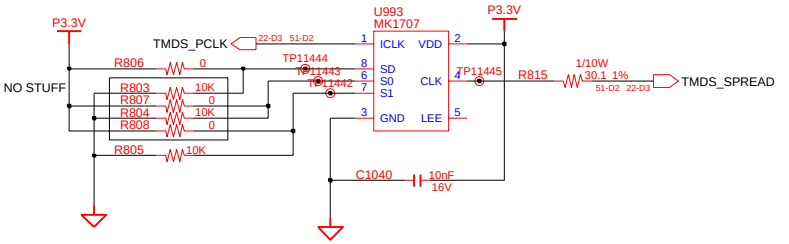


Straps	Pin Number	Descriptions
CAL_BG_BACKUP	GPIO0	PCI-Express Current Calibration Bandgap Backup 0 : use reference voltage from bandgap (Default) 1: use reference voltage from resistor divider
PLL_CAL_FORCE_EN	GPIO1	PCI-Express PLL Calibration Force Enable 0: Disable PLL force calibration (Default) 1 : Enable PLL force calibration
PCIE Mode(1:0)	GPIO(3:2)	PCI-Express Mode 00 : PCI Express 1.0A mode (Defalut) 01 : Reserved 10 : PCI Express 1.0 mode 11 : Reserved
CAL_OFF	GPIO4	Turn-Off PCI-Express Impedance / Strength Calibration 0 : Enalbe (Default) 1 : Disable Also, used to demux VCOREF / CALREF
BYPASS_PLL	GPIO5	Bypass PCI-Express PLL 0: - (Default) 1 : -
ICOMP	GPIO6	PCI-Express Transmitter Current Compensation 0 : Normal (Default) 1: Inject extra current for output buffer switching
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. 0000 : No ROM, CHG_ID = 0 0001 : No ROM, CHG_ID = 1 0100 : Reserved 0110 : Reserved Others : ROM (Third party vendors)
DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.





DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN REV. HISTORY	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM	PAGE 25 OF 51	

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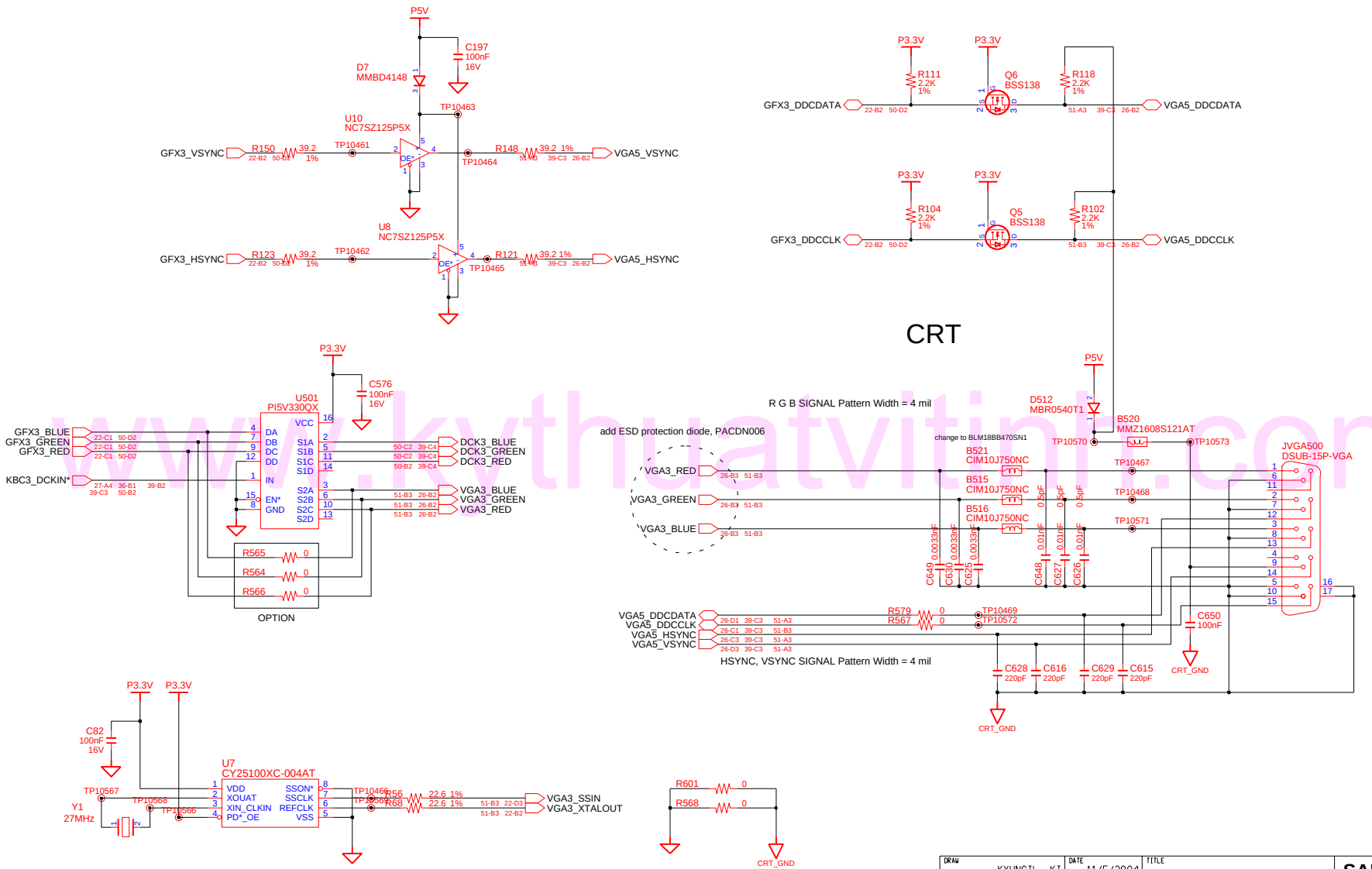

Optional External Thermal Sensor

DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN CRT PORT/SPREAD SPECTRUM	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		
APPROVAL: KIM, DW	REV: 1.0		PART NO. BA41-00450A
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 26 OF 51

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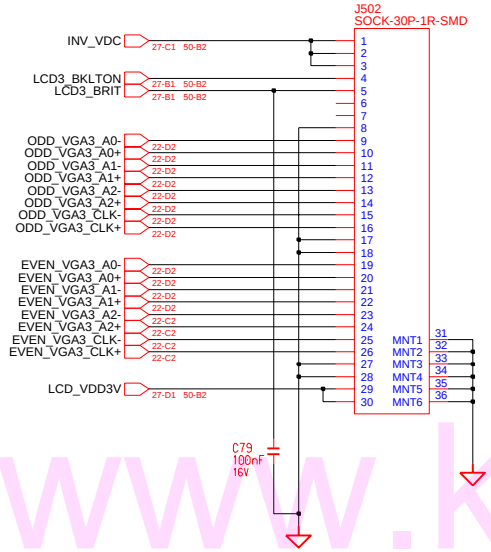
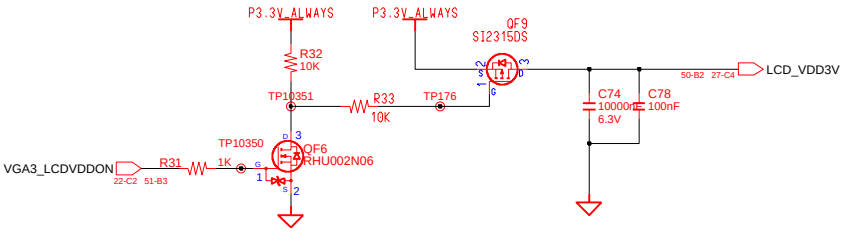
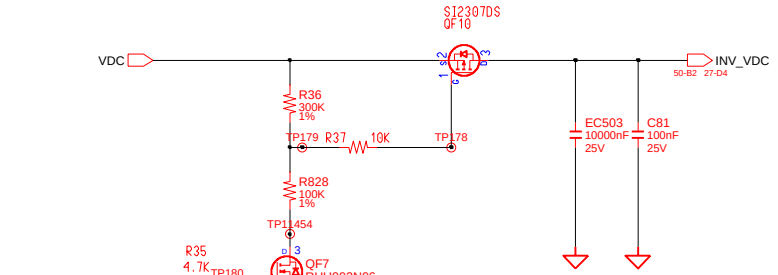
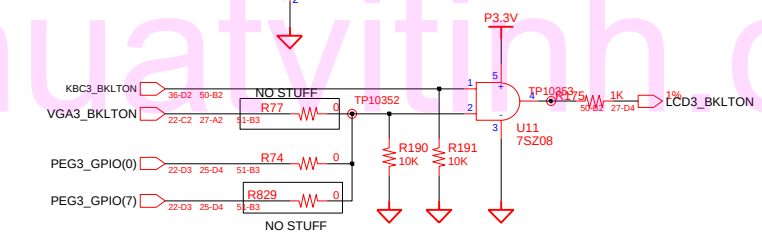
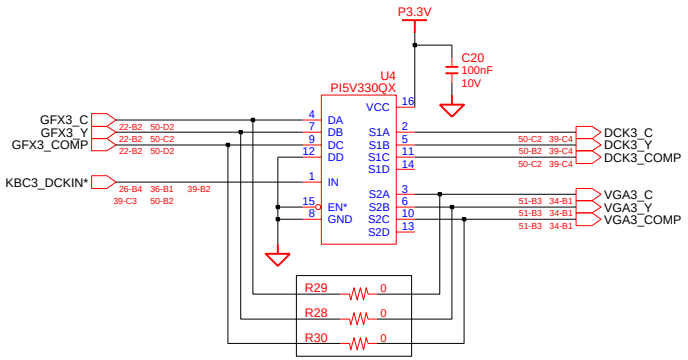
LCD CONNECTOR

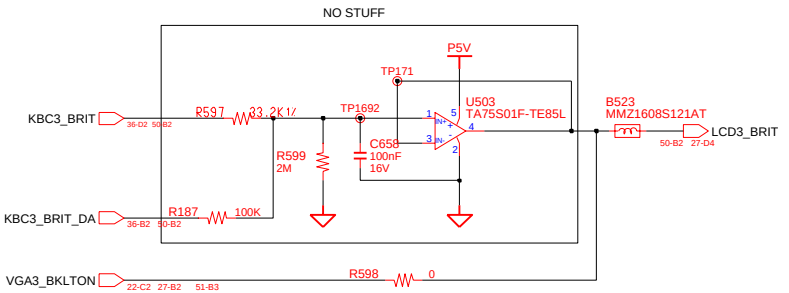












DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN LCD_CONNECTOR / BKLT	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM	PAGE 27 OF 51	

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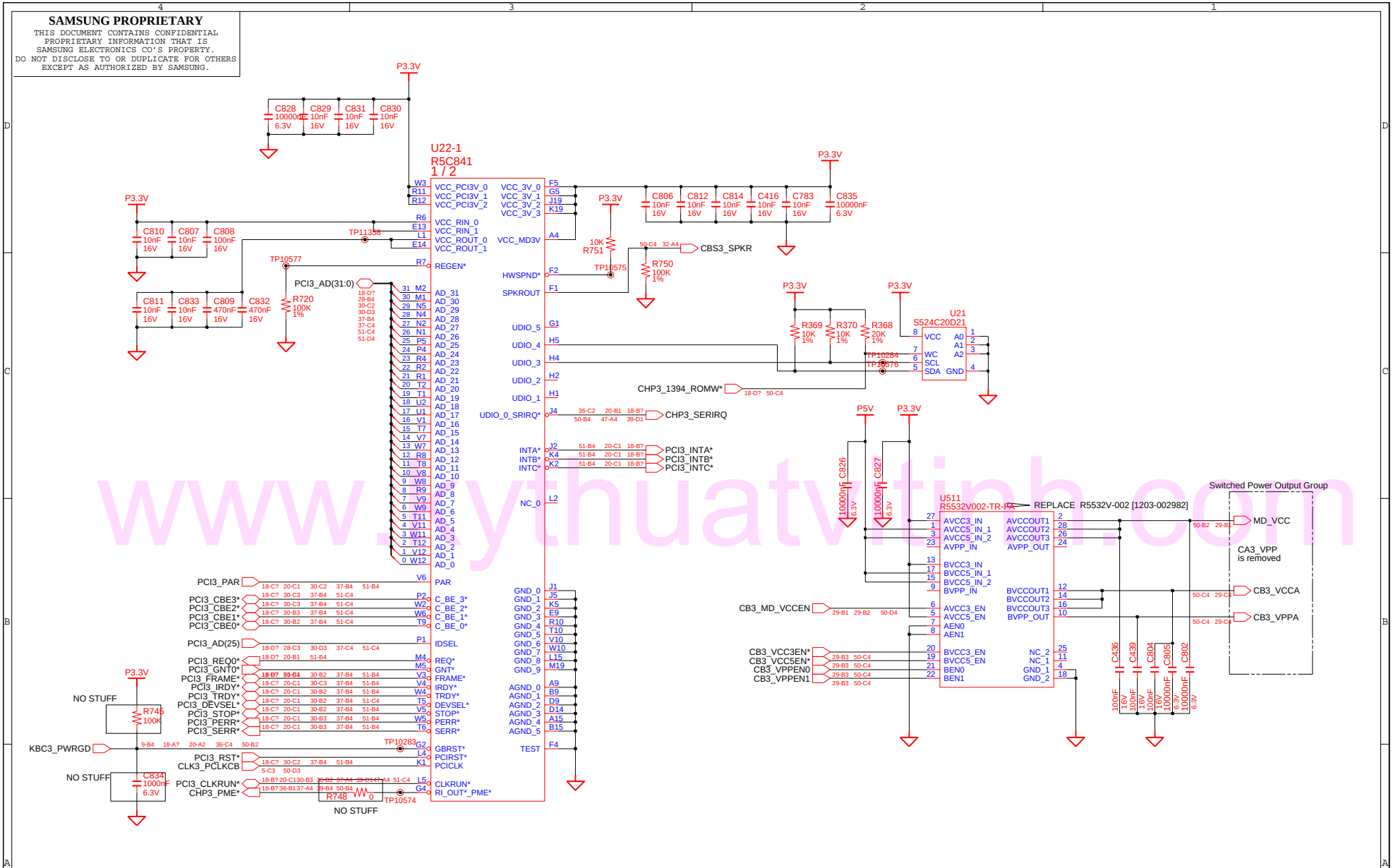

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DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN CARDBUS / 1394	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM		PAGE 28 OF 51

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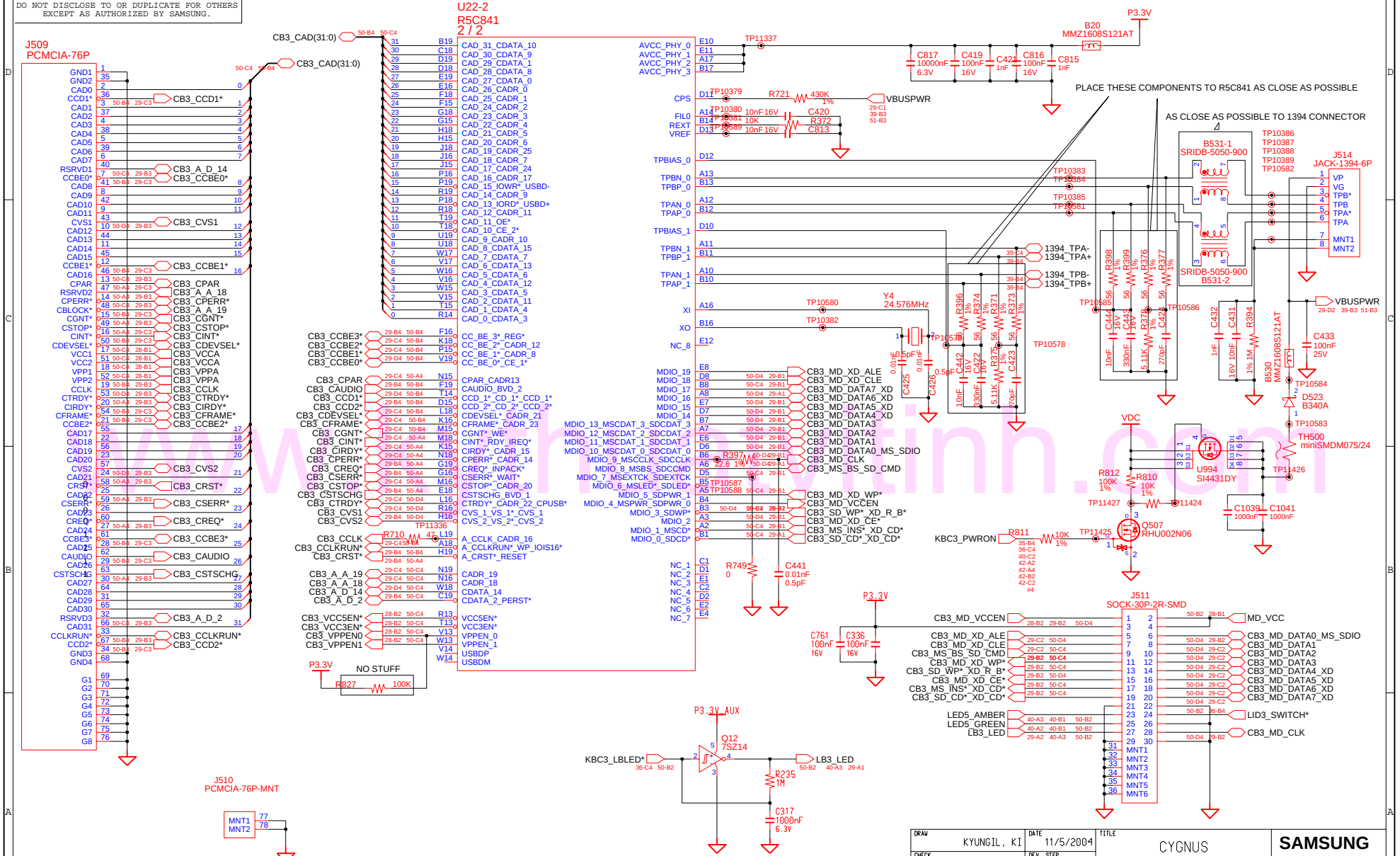

DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN CARDBUS SOCKET/MEDIA CARD	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
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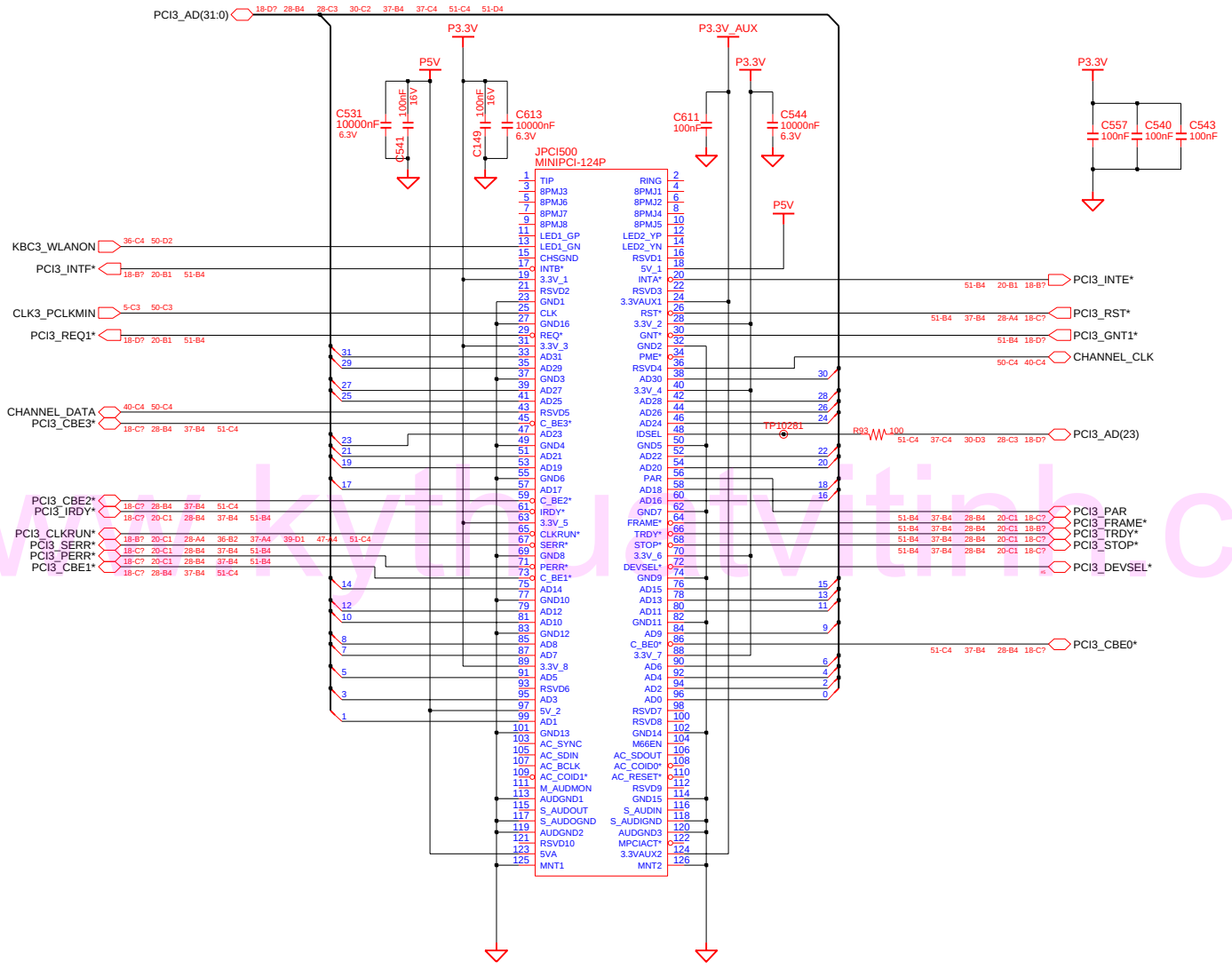

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DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 30 OF 51

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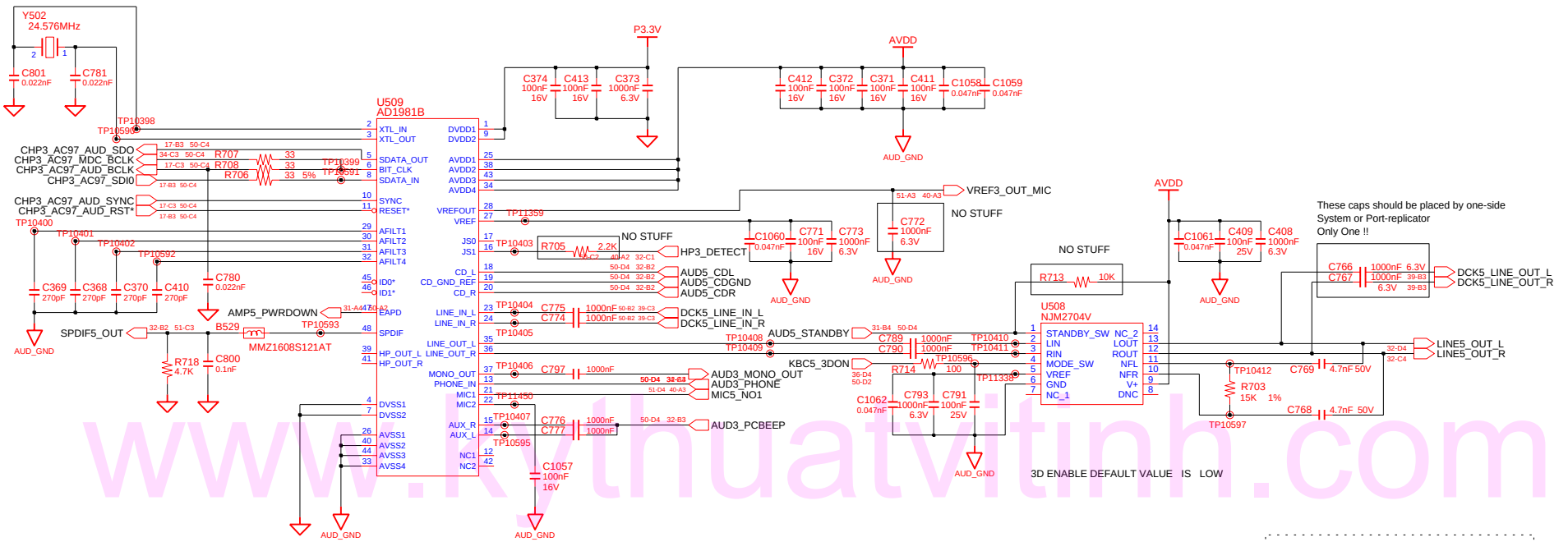
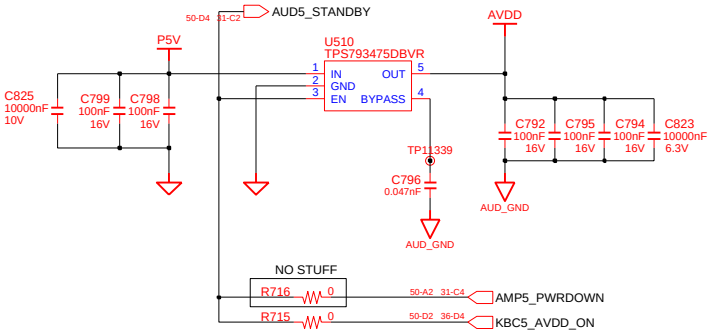


1. AUD_GND is Audio Ground
2. GND is Digital Ground
3. MGND is Mic_Ground
4. PR_LINE_OUT & PR_LINE_IN is for Port Replicator



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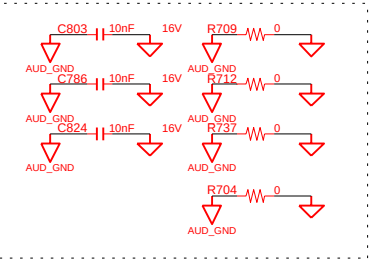

DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN AUDIO CODEC & AMP	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
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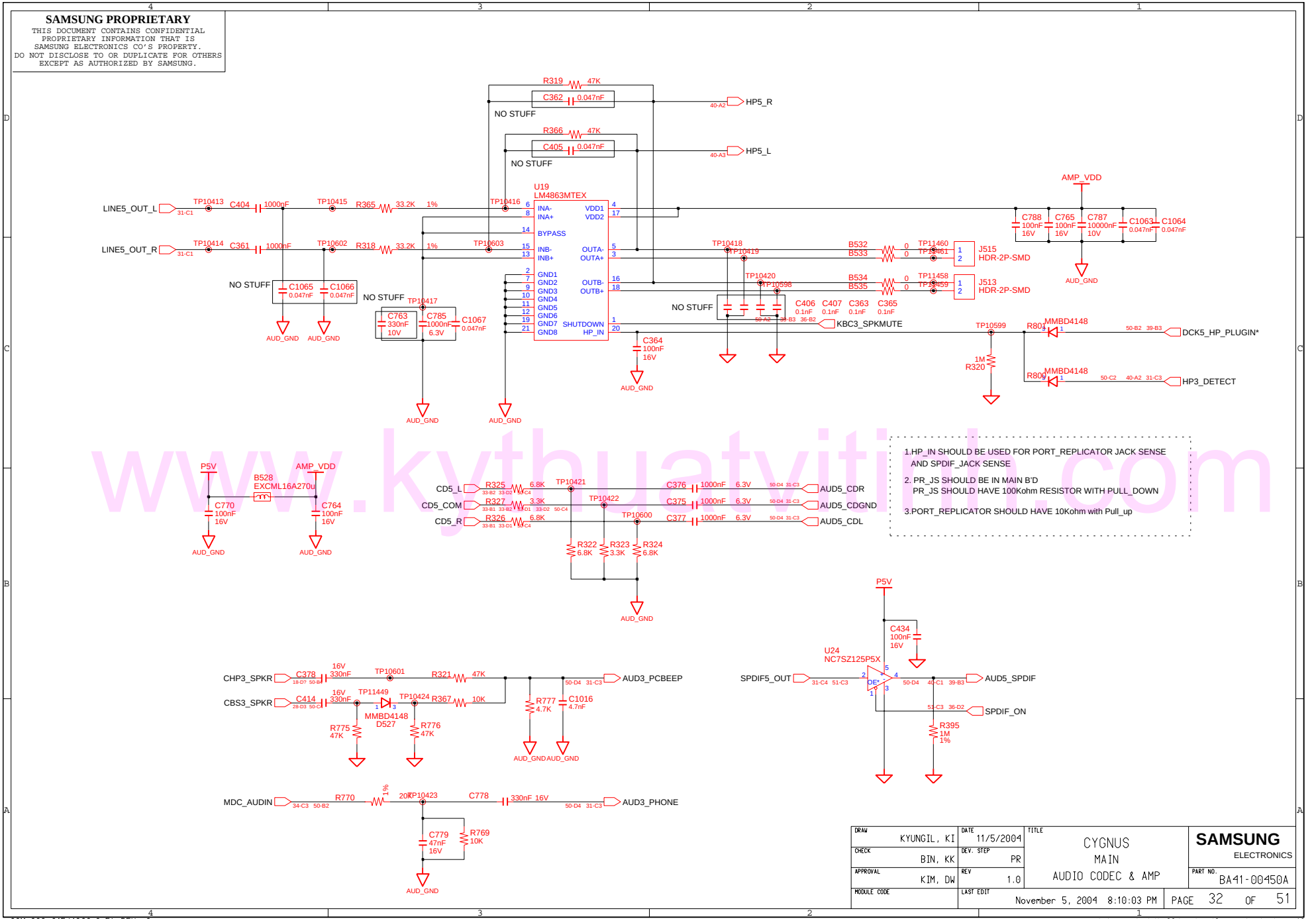

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DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN AUDIO CODEC & AMP	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM		PAGE 32 OF 51

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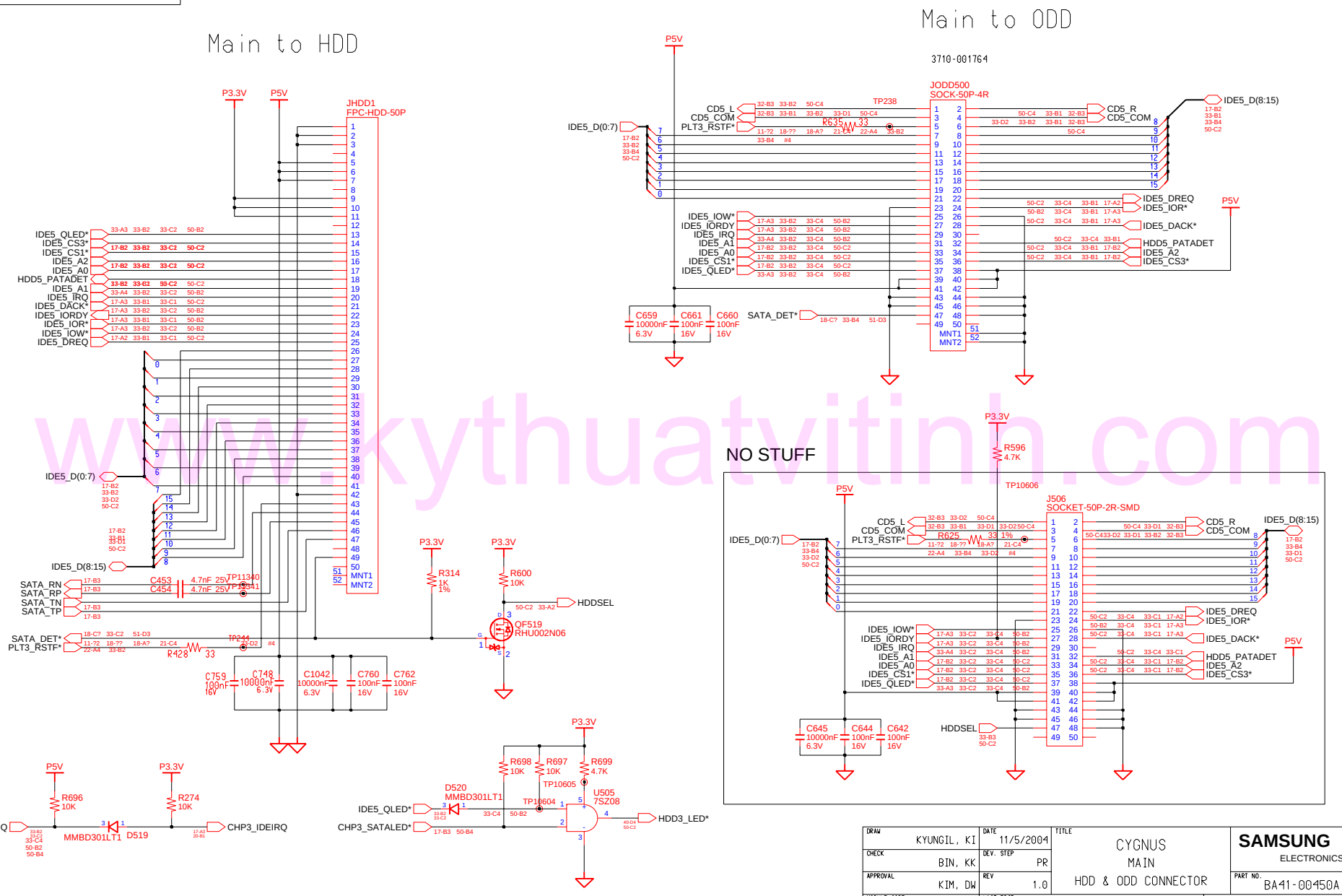

DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN HDD & ODD CONNECTOR	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
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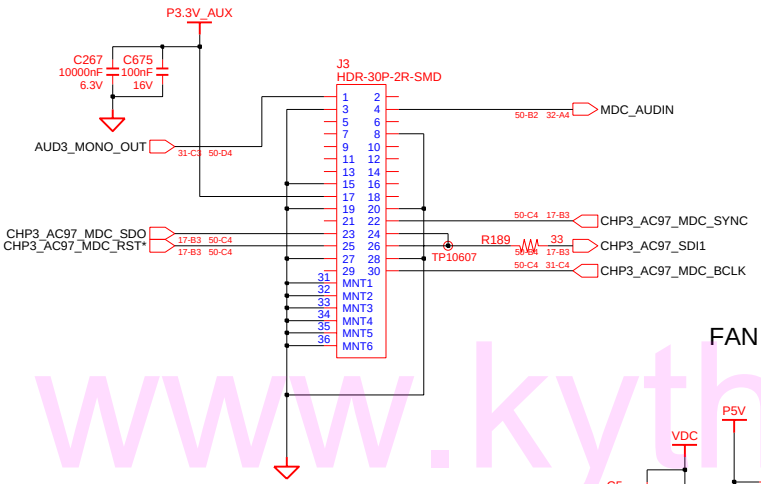
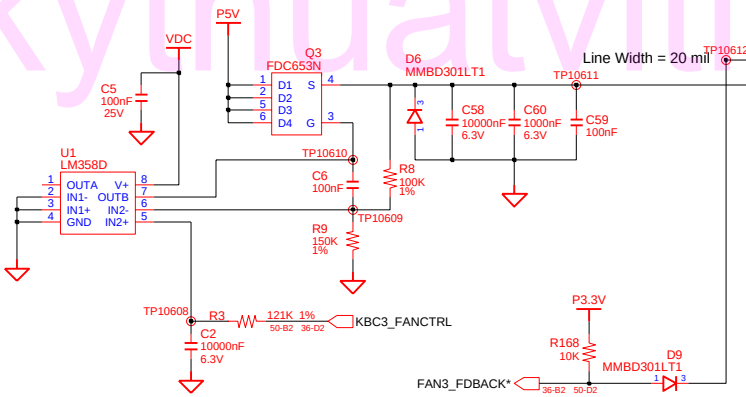
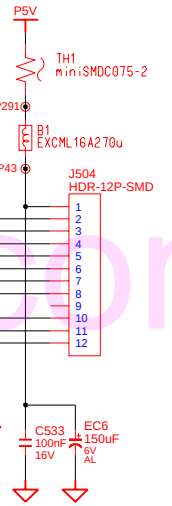
MDC Connecter



FAN Control Logic



TV-OUT(S-VHS)



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DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR	MDC MODEM / TV-OUT(SVHS)	PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM	PAGE 34 OF 51	

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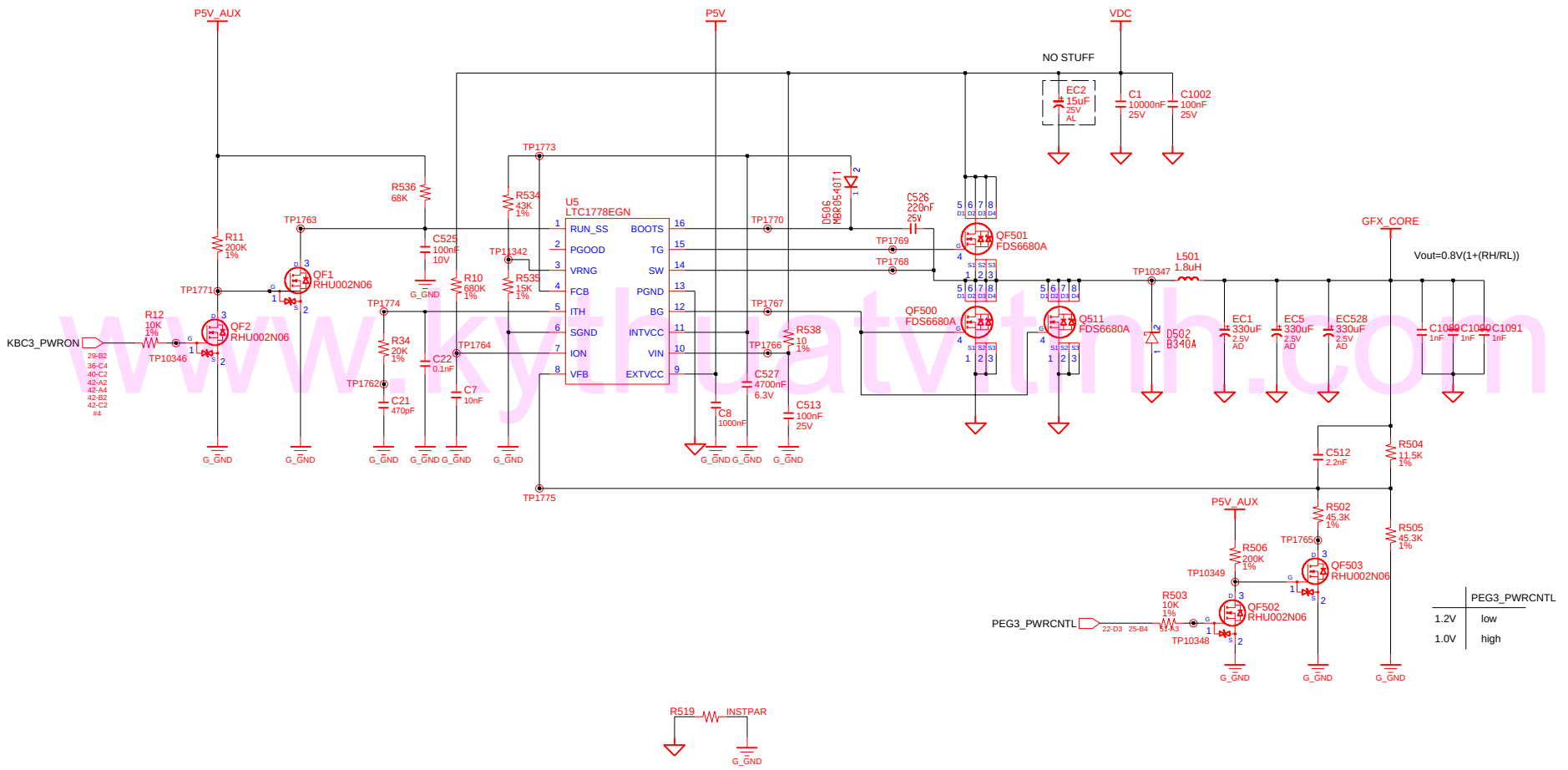
Graphic Core Power



PEG3_PWRCNTL	
1.2V	low
1.0V	high

DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN GRAPHIC CORE POWER	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 35 OF 51

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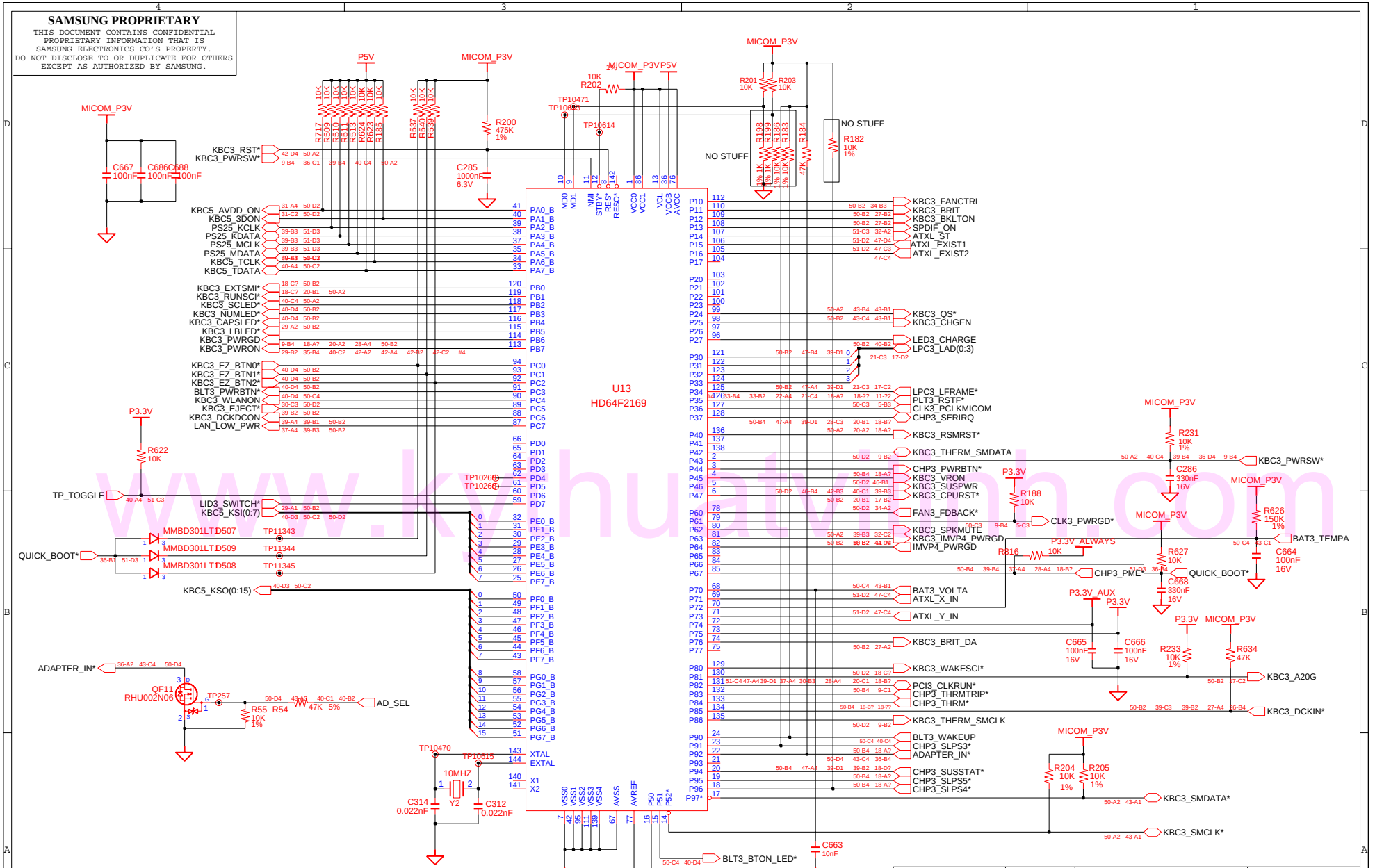

DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN MICOM	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM	PAGE 36 OF 51	

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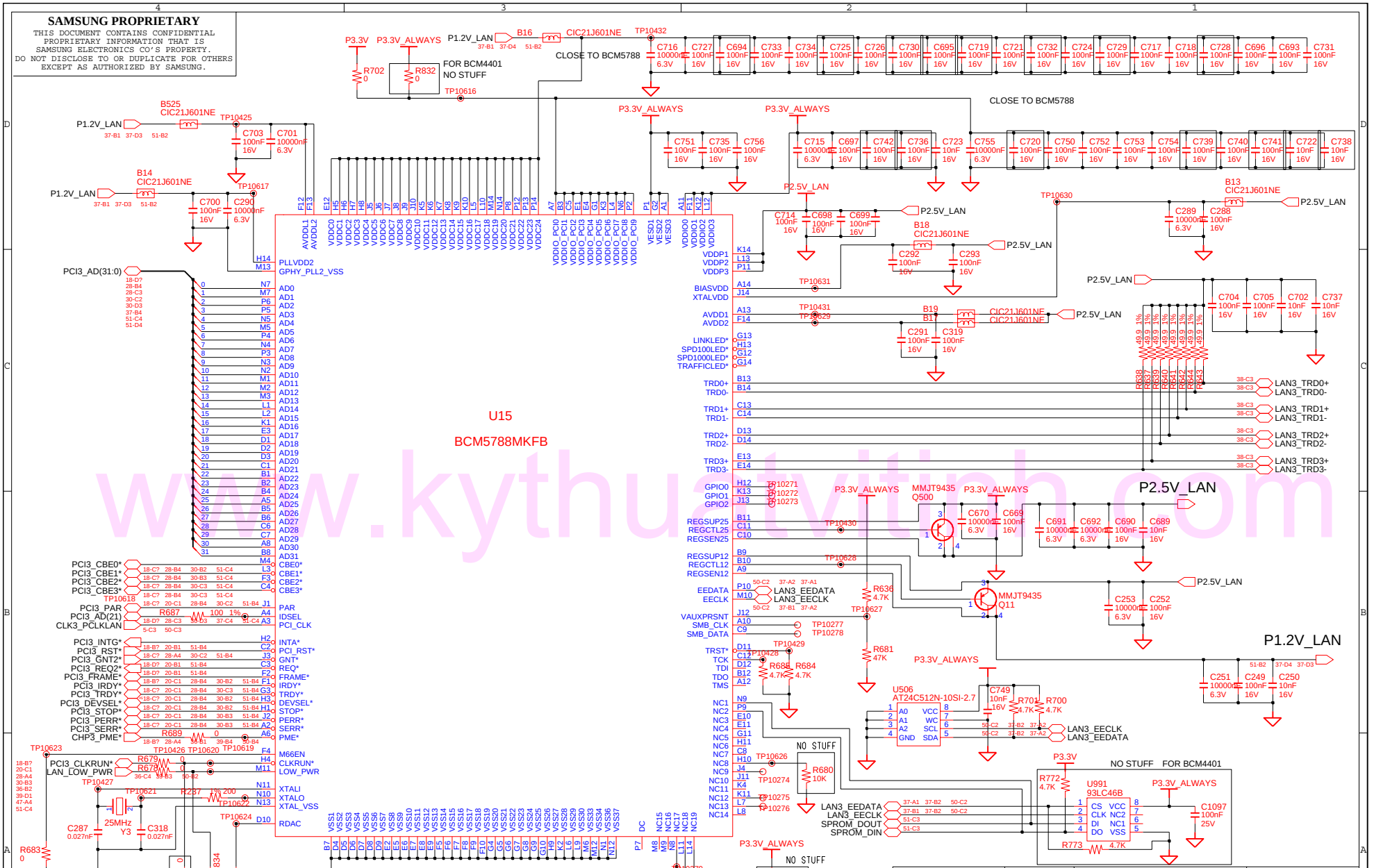

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DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN LAN(BROADCOM BCM5751M 1/2)	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 37 OF 51

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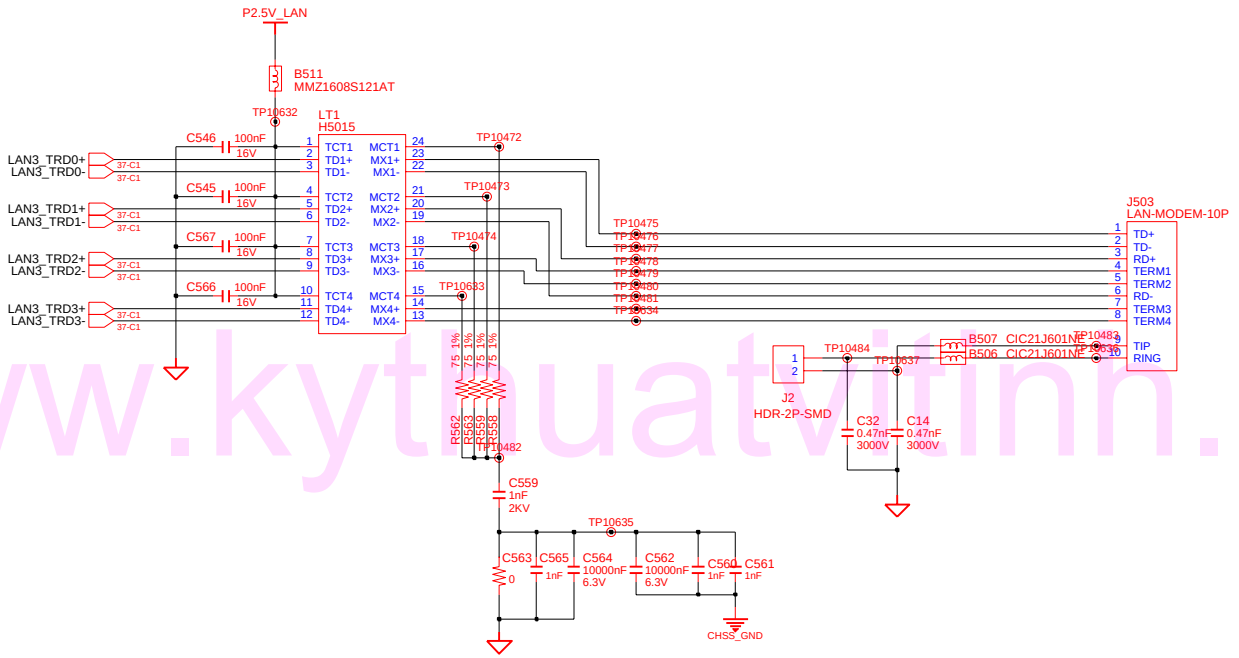

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DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN LAN(BROADCOM BCM5751M 2/2)	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		
APPROVAL KIM, DW	REV 1.0		PART NO. BA41-00450A
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM		PAGE 38 OF 51

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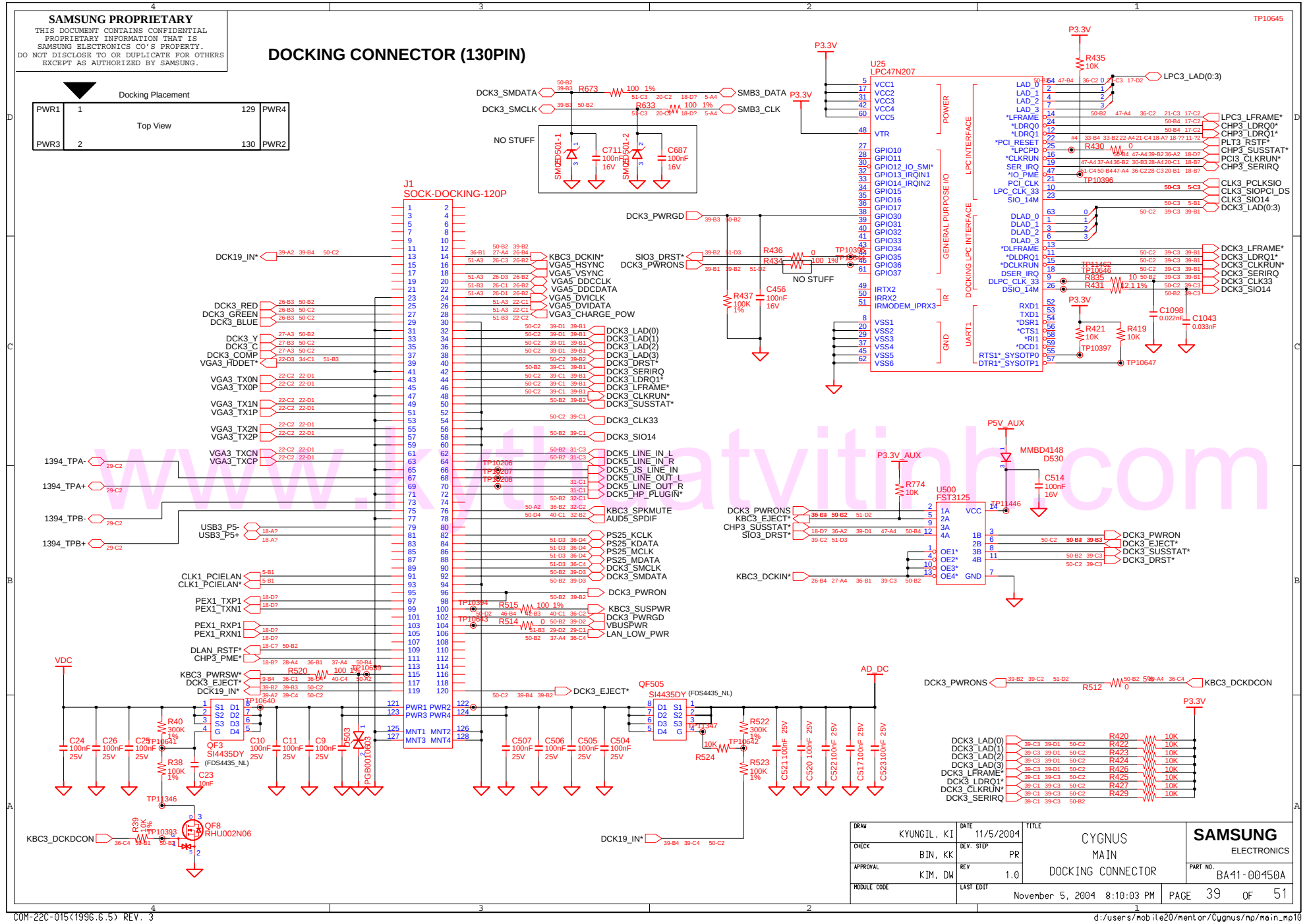
DOCKING CONNECTOR (130PIN)



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DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN DOCKING CONNECTOR	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 39 OF 51

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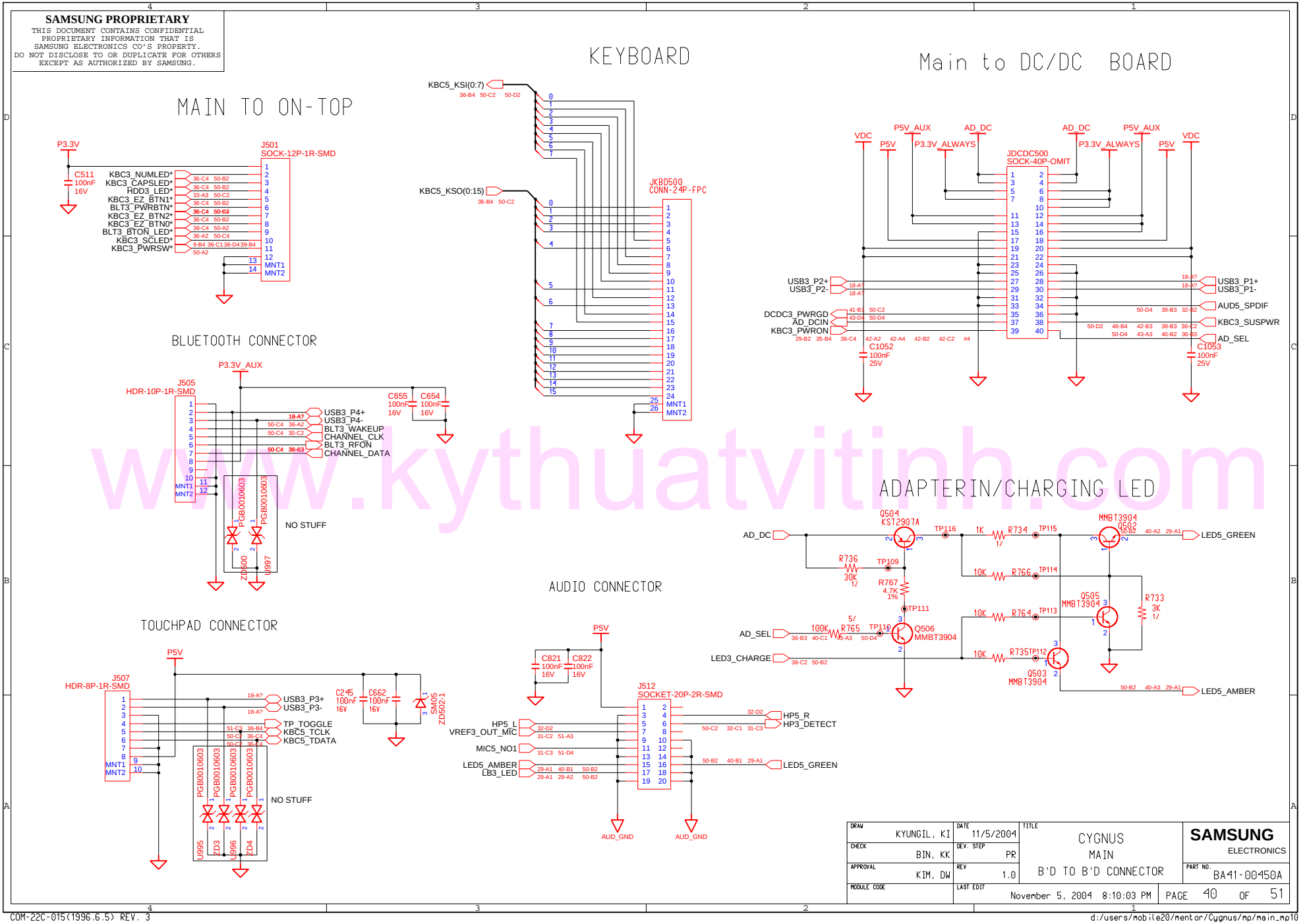

DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN B'D TO B'D CONNECTOR	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		
APPROVAL: KIM, DW	REV: 1.0		PART NO. BA41-00450A
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 40 OF 51

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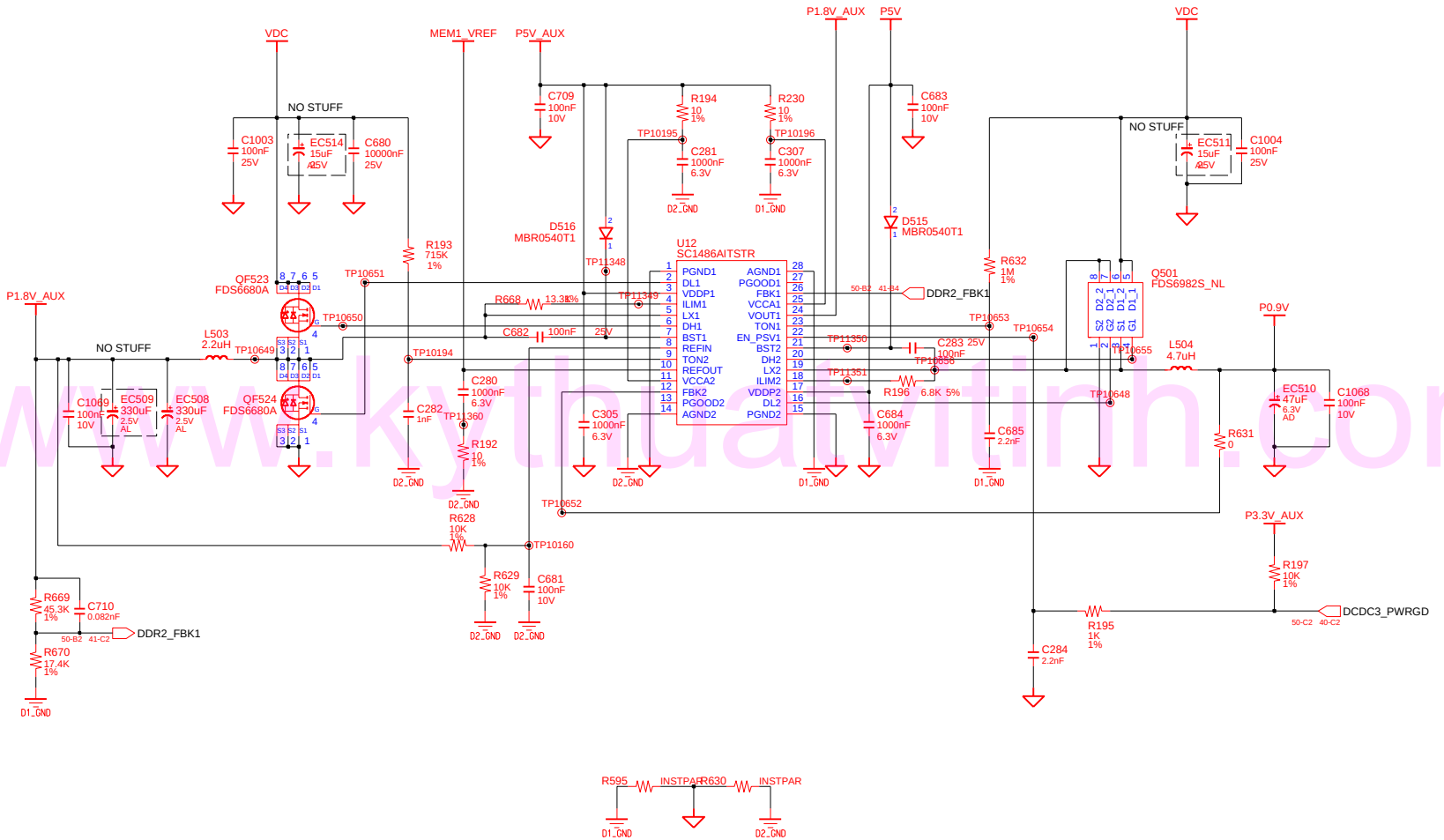
DDR Power



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DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN DDR POWER	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM		PAGE 41 OF 51

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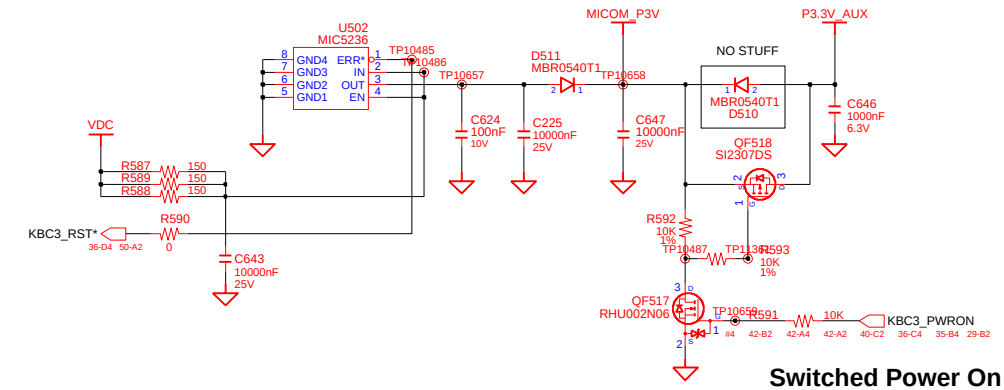
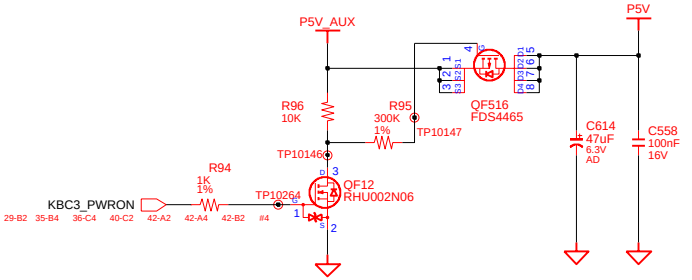
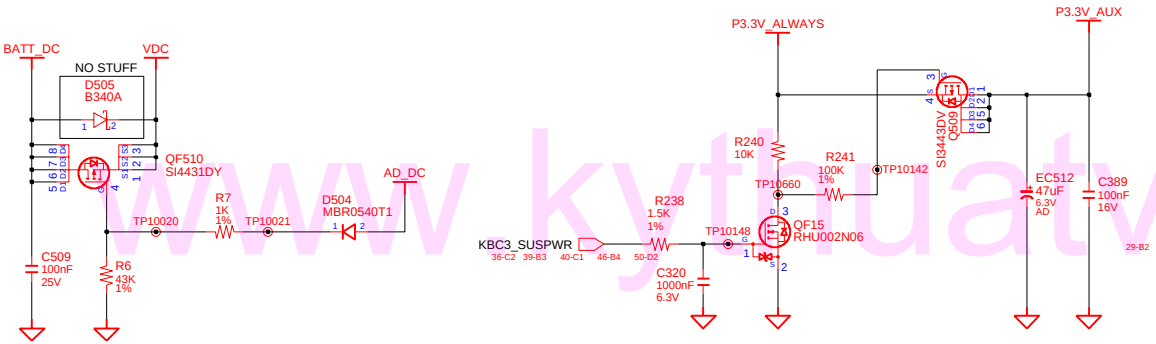
MICOM_P3V Power



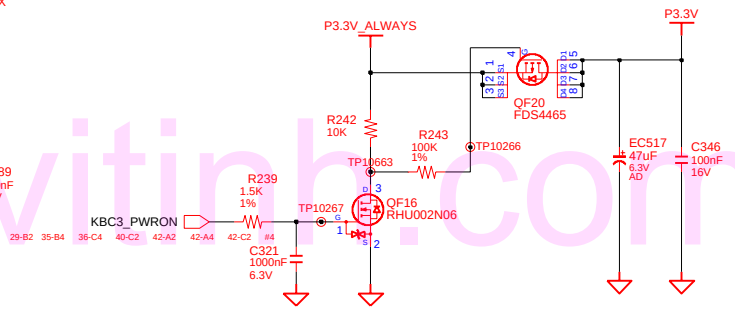
Switched Power On (P5V)



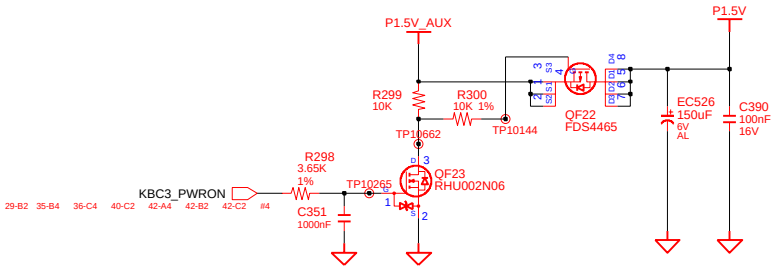
Switched Power On (P3.3V_AUX)



Switched Power On (P3.3V)



Switched Power On (P1.5V)



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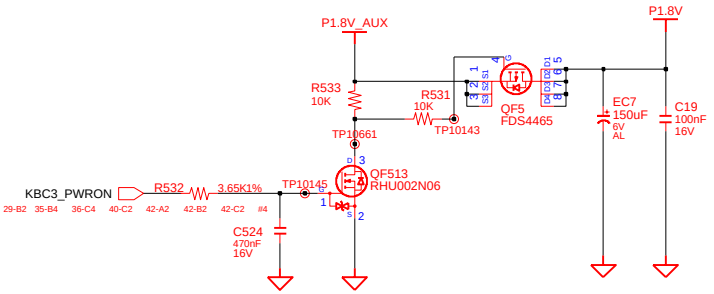

DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN MICOM & SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM	PAGE 42 OF 51	

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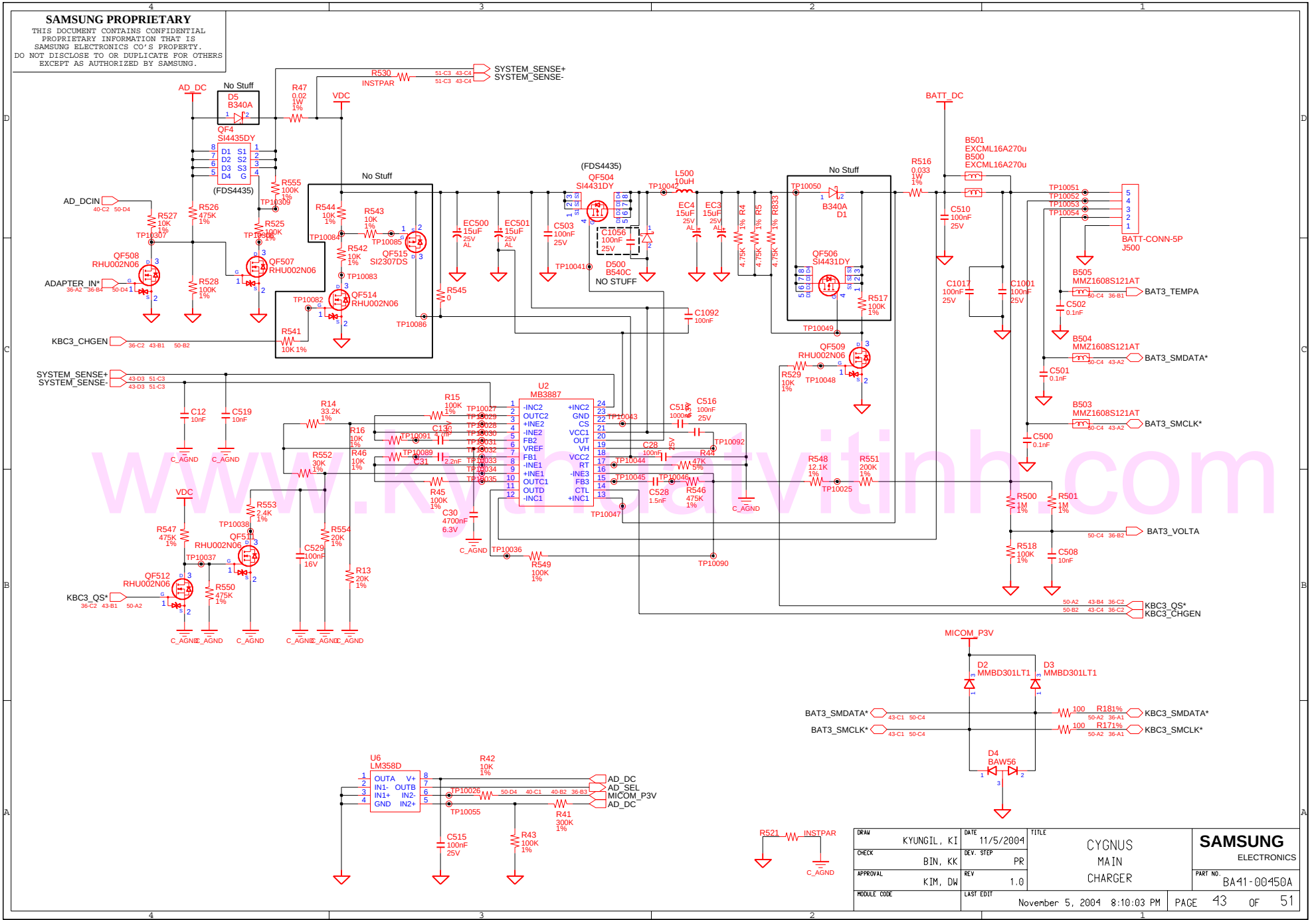

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CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 43 OF 51

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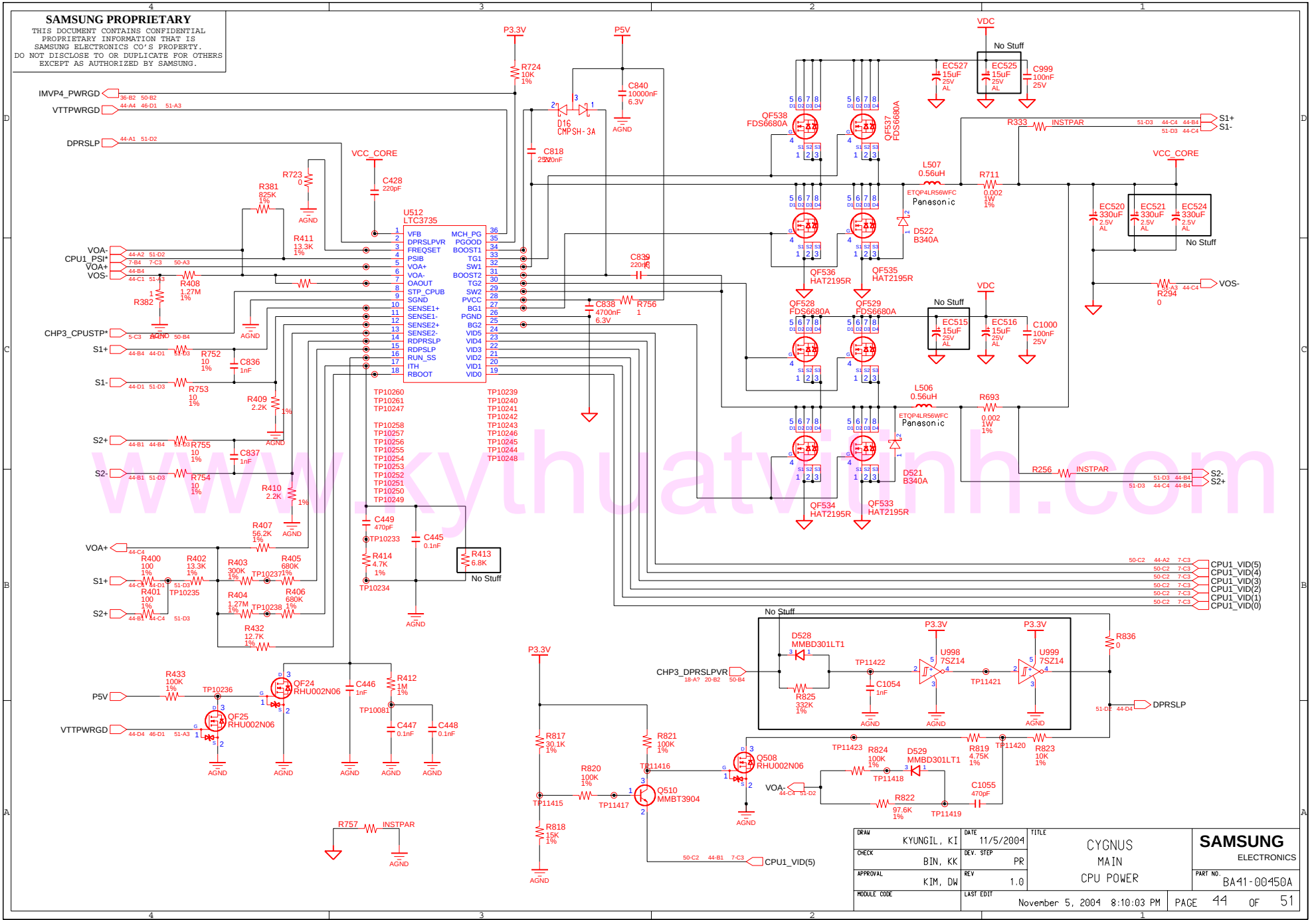

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DRAW: KYUNGIL, KI	DATE: 11/5/2004	TITLE: CYGNUS MAIN CPU POWER	SAMSUNG ELECTRONICS
CHECK: BIN, KK	DEV. STEP: PR		PART NO. BA41-00450A
APPROVAL: KIM, DW	REV: 1.0		
MODULE CODE	LAST EDIT: November 5, 2004 8:10:03 PM		PAGE 44 OF 51

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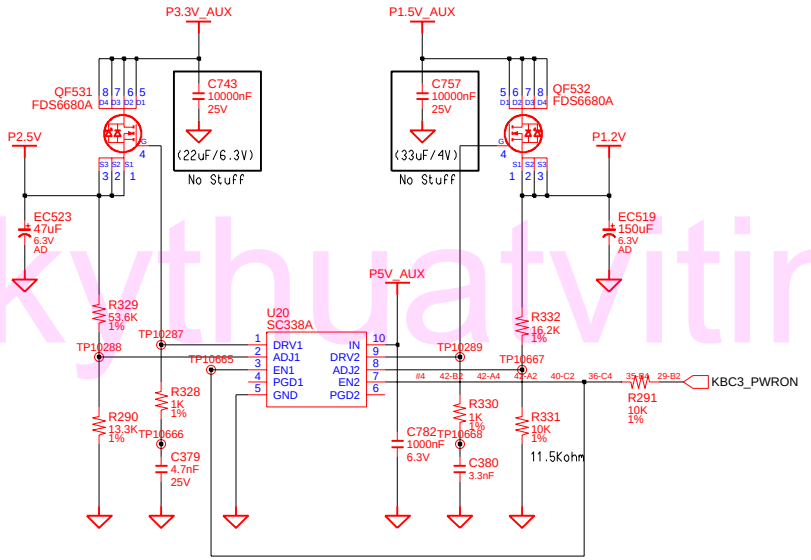
P2.5V&P1.2V



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DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN P2.5V & P1.2V	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM		PAGE 45 OF 51

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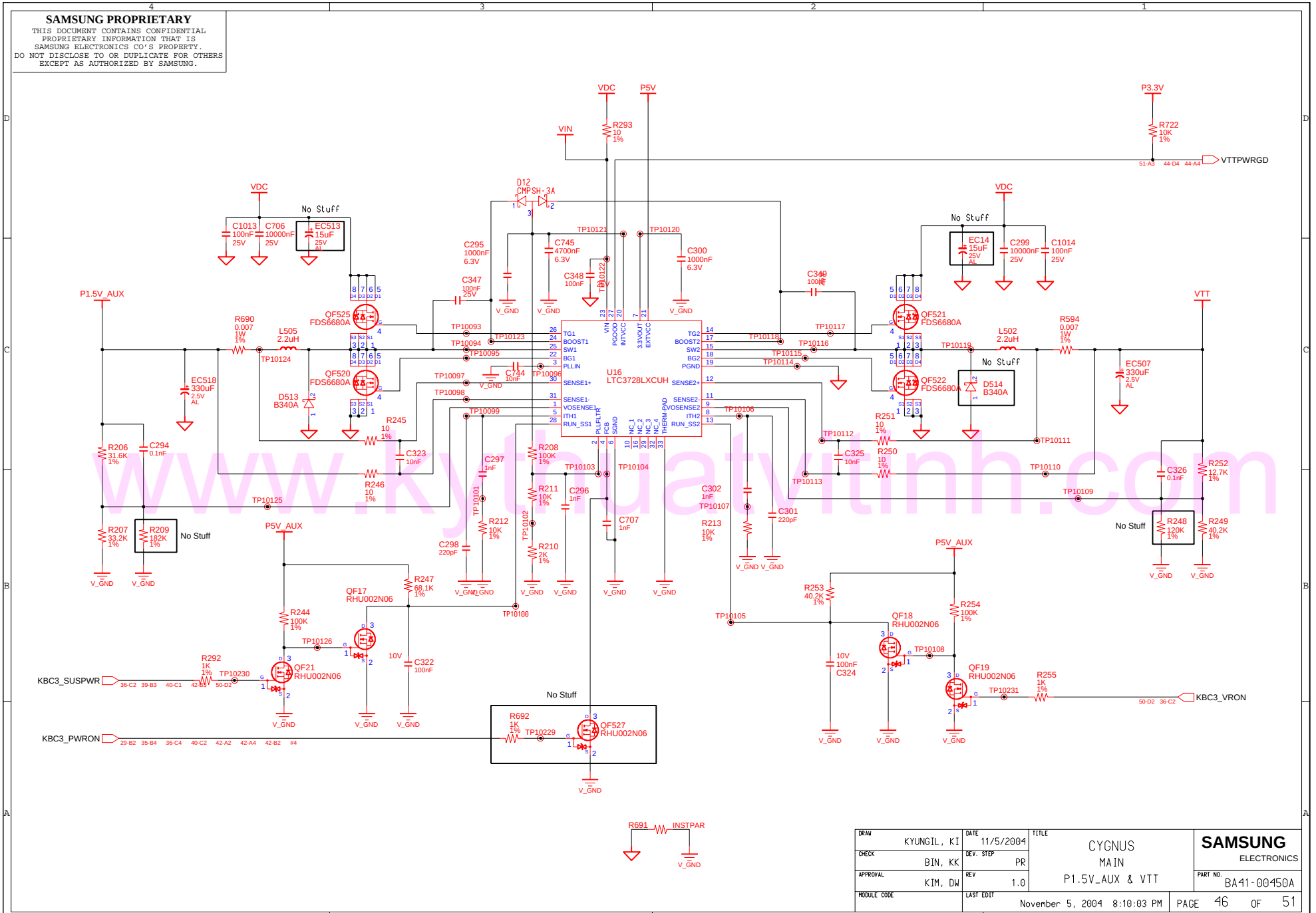

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CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM		PAGE 46 OF 51

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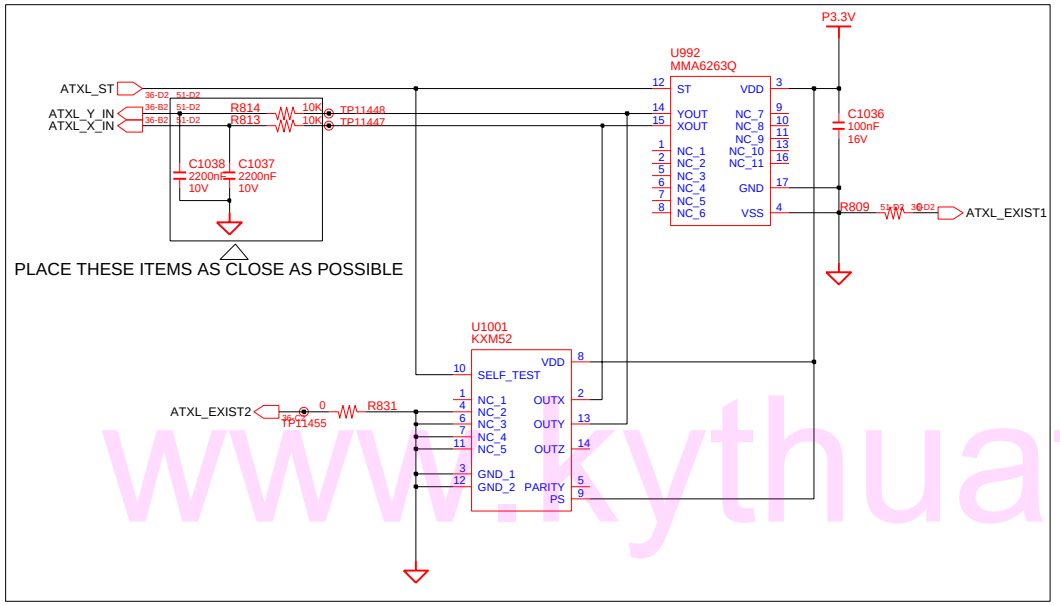
AIRBAG

NO STUFF



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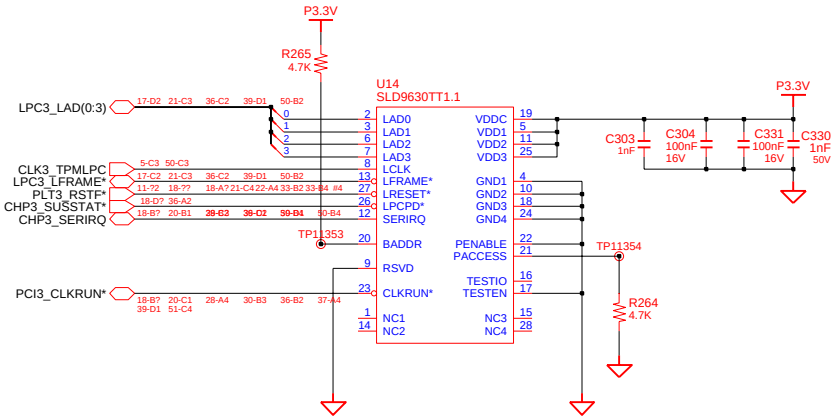

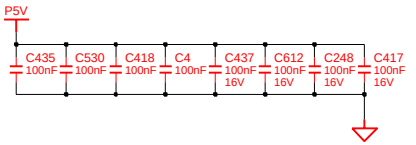

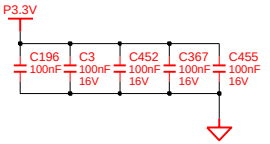

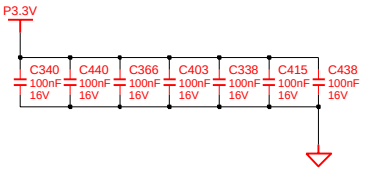

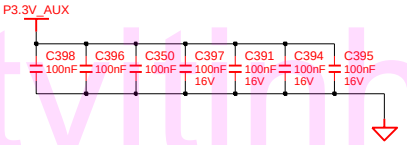

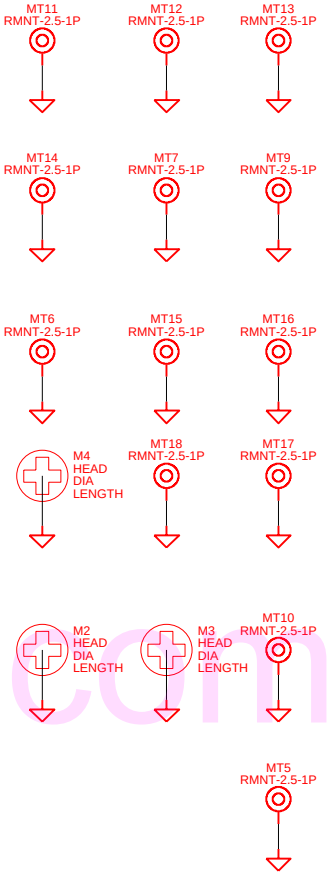

REV1

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAINBD AIRBAG & TPM	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM		PAGE 47 OF 51

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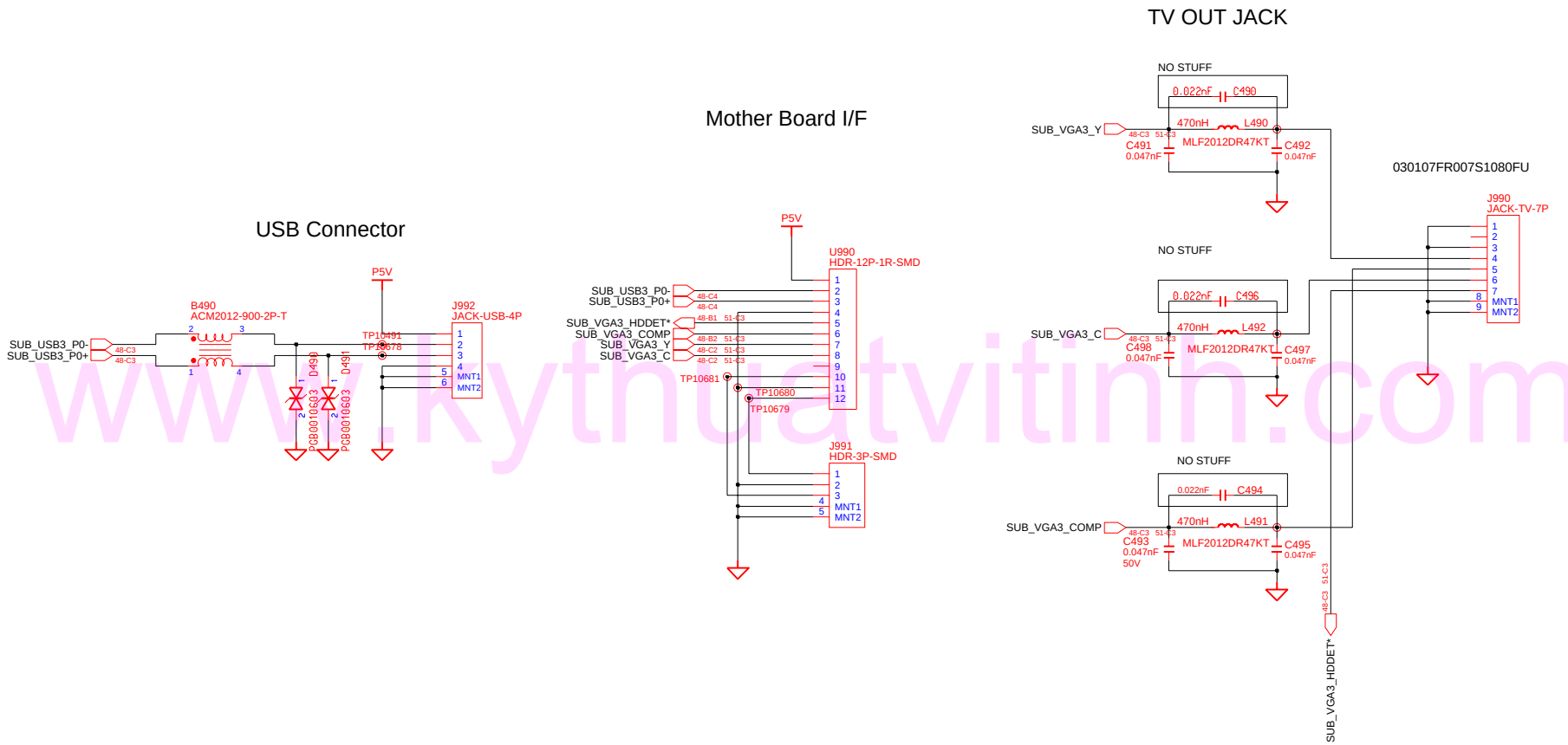

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DRAW KYUNGIL, KI	DATE 11/5/2004	TITLE CYGNUS MAIN MOUNT HOLE	SAMSUNG ELECTRONICS
CHECK BIN, KK	DEV. STEP PR		PART NO. BA41-00450A
APPROVAL KIM, DW	REV 1.0		
MODULE CODE	LAST EDIT November 5, 2004 8:10:03 PM		PAGE 48 OF 51

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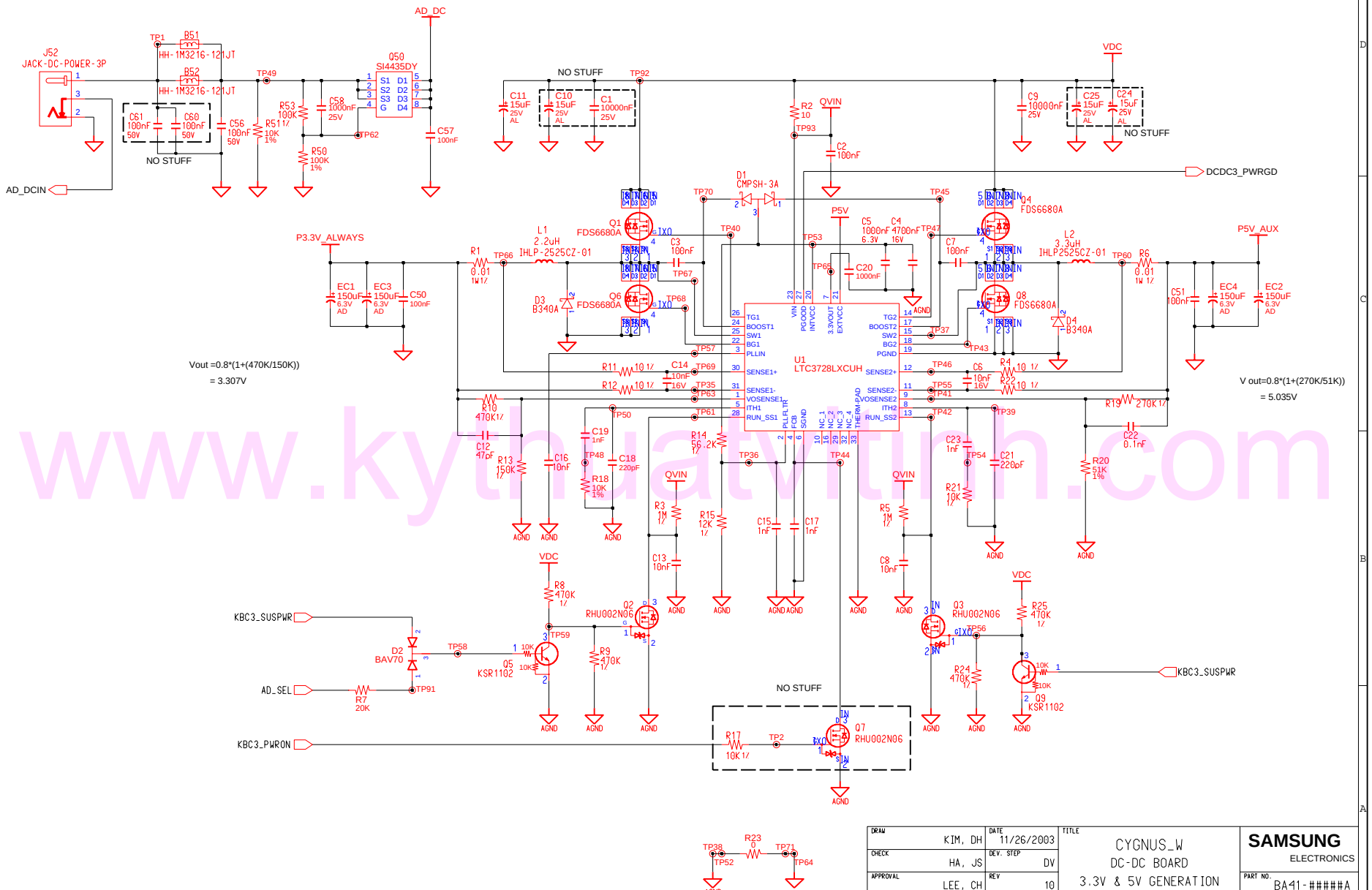

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DRAW: KIM, DH	DATE: 11/26/2003	TITLE: CYGNUS_W DC-DC BOARD 3.3V & 5V GENERATION	SAMSUNG ELECTRONICS
CHECK: HA, JS	DEV. STEP: DV		PART NO. BA41-#####A
APPROVAL: LEE, CH	REV: 10		
MODULE CODE	LAST EDIT: March, 9, 2002 4:21:54 PM	PAGE 1 OF 2	

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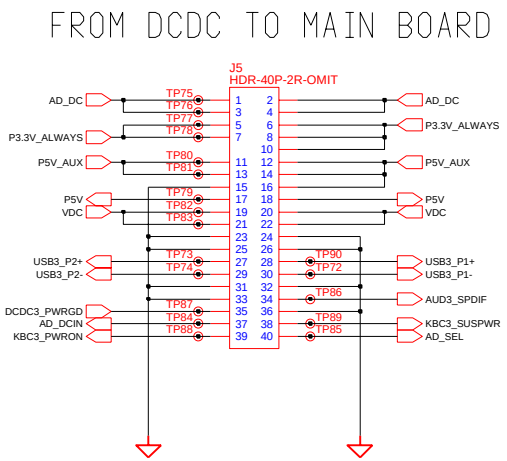
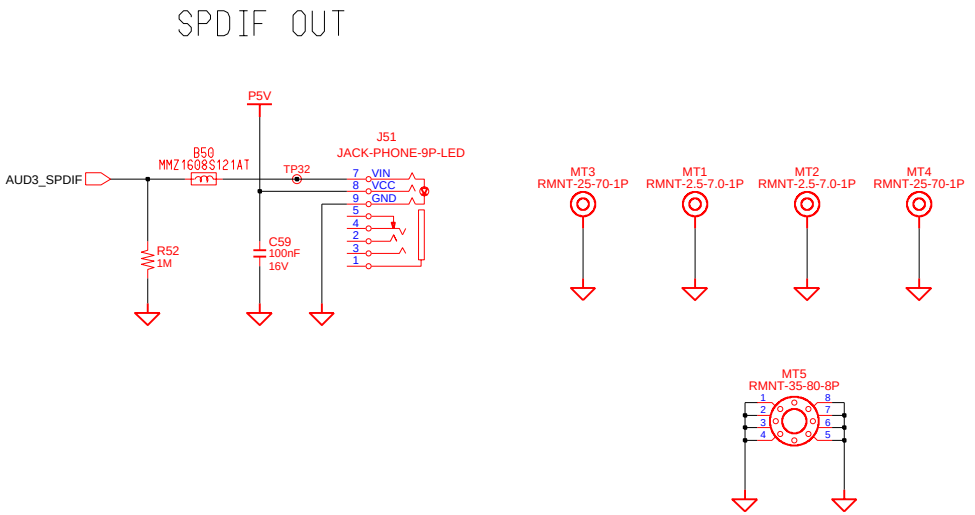
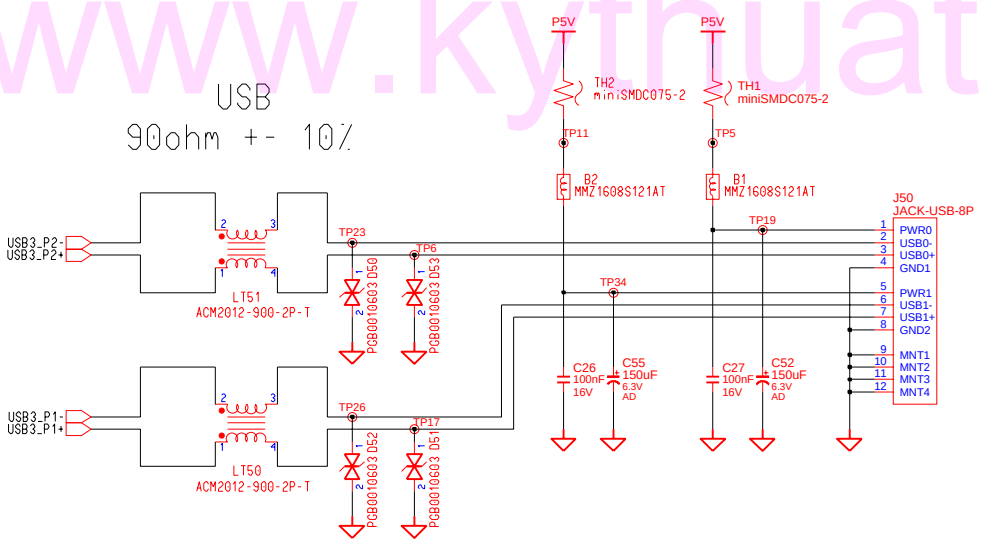
CHANGE THIS CONNECTOR TO HEADER < 12809A-40G5T>







REV1

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW KIM, DH	DATE 11/26/2003	TITLE CYGNUS_W DC-DC BOARD CONNECTOR & PORT	SAMSUNG ELECTRONICS
CHECK HA, JS	DEV. STEP DV		PART NO. BA41-#####A
APPROVAL LEE, CH	REV 10		
MODULE CODE	LAST EDIT March, 9, 2002 4:23:55 PM		PAGE 2 OF 2

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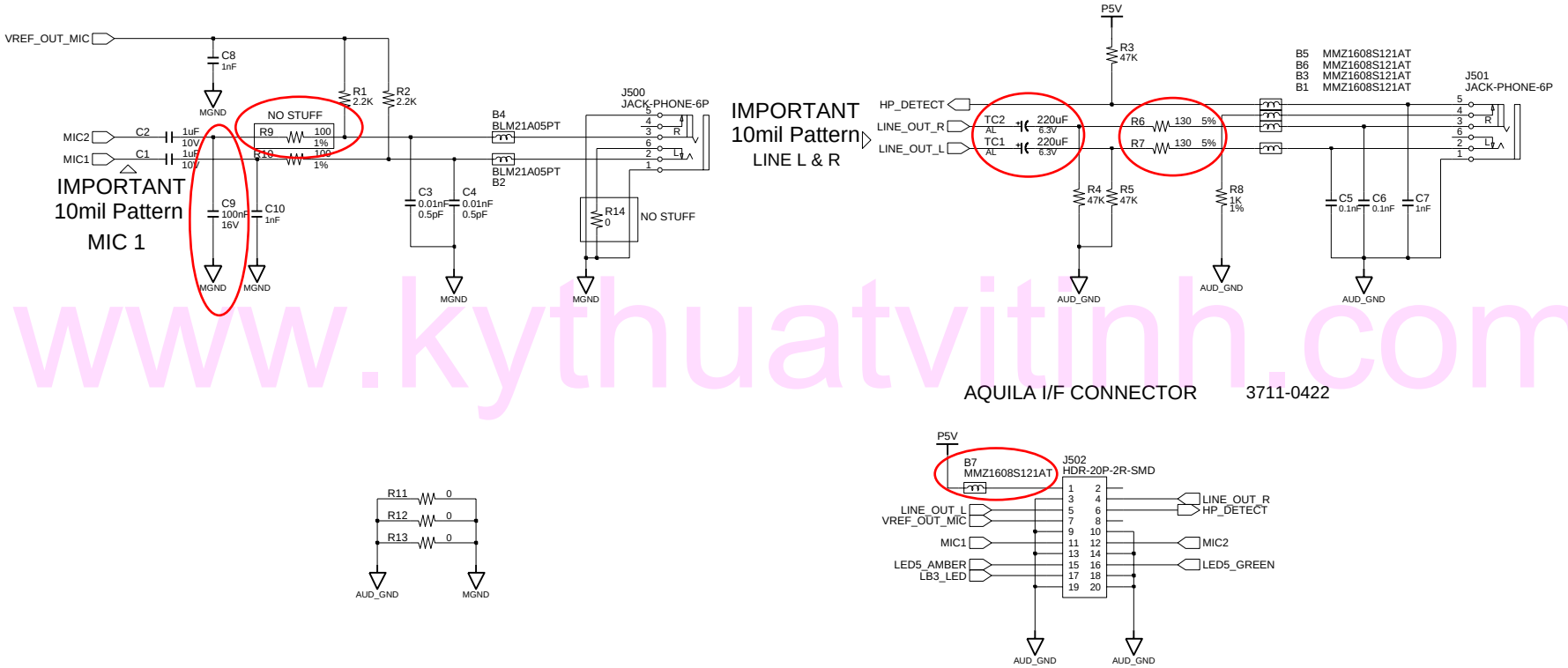
< AUDIO BOARD >



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AQUILA I/F CONNECTOR 3711-0422

DRAW	DATE 1/30/2004	TITLE Cygnus AUDIO JACK	SAMSUNG ELECTRONICS
CHECK	DEV. STEP		PART NO. BA41-
APPROVAL	REV		
MODULE CODE	LAST EDIT January, 30, 2004 9:34:17 AM		PAGE 1 OF

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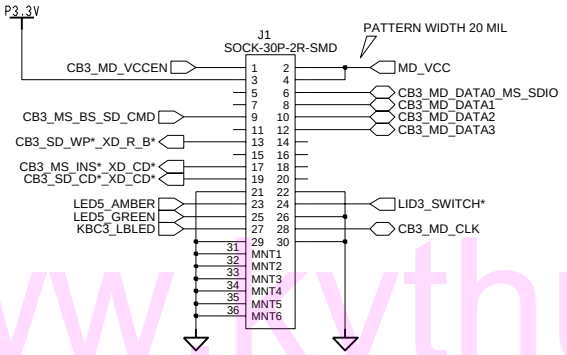
< 3 IN 1 BOARD >

MAIN BOARD I/F CONNECTOR



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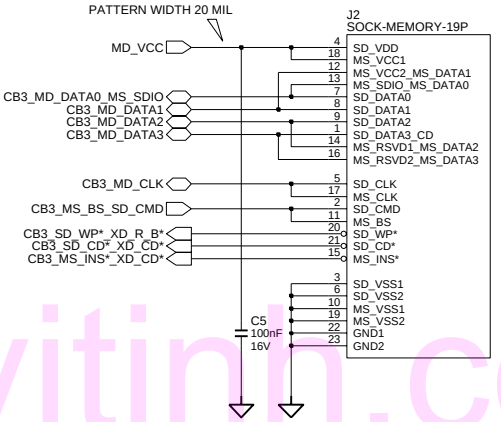

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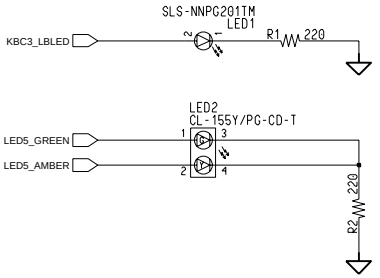
LED



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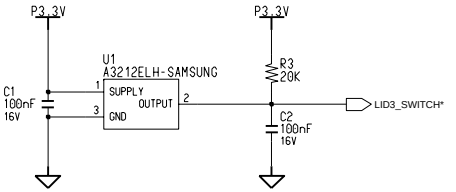

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CHECK	DEV. STEP		
APPROVAL	REV		PART NO. BA41-
MODULE CODE	LAST EDIT January, 11, 2004 2:16:04 PM		PAGE 1 OF

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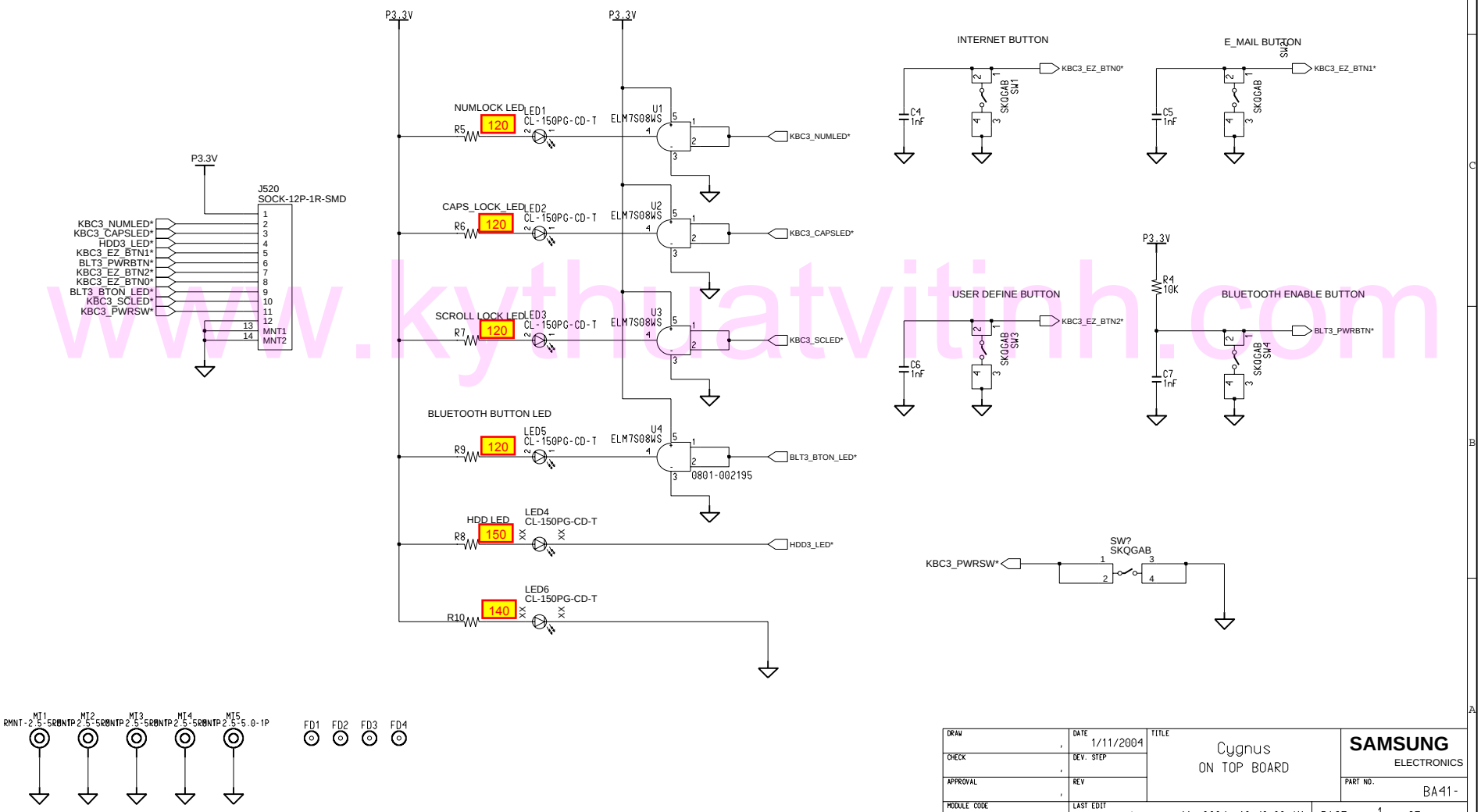
< ON TOP BOARD >



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DRAW	DATE 1/11/2004	TITLE Cygnus ON TOP BOARD	SAMSUNG ELECTRONICS
CHECK	DEV. STEP		PART NO. BA41-
APPROVAL	REV		
MODULE CODE	LAST EDIT January, 11, 2004 10:48:32 AM		PAGE 1 OF

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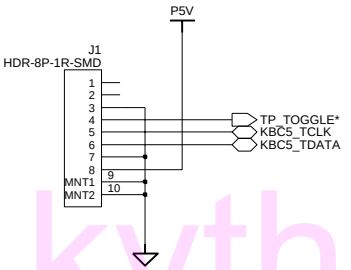
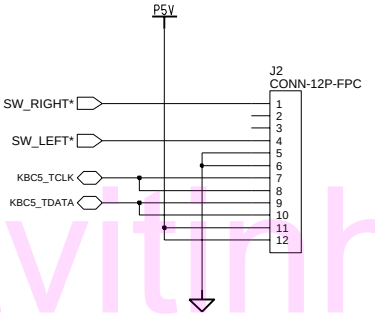
< TOUCHPAD BOARD >

MotherBoard I/F Connector



TouchPad Connector



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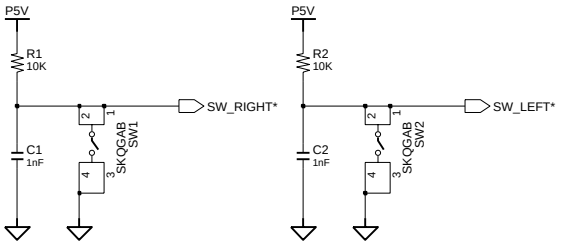

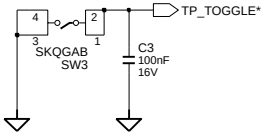

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CHECK ,	DEV. STEP		
APPROVAL ,	REV		PART NO. BA41-
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