

9. 회로도

9-1. External Graphic

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
	AD21	3	
MiniPCI SLOT1	AD23	2	D,E
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
		-	A,B
Internal MAC	AD24(internal)	-	E
AC Link		-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308-1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	1	1	0	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V
Highest Freq.	0	1	0	1	1	1.356 V	1	1	0	1	1	0	0.844 V
	0	1	0	1	1	1.340 V	1	1	0	1	1	1	0.828 V
	0	1	1	0	0	1.324 V	1	1	1	0	0	0	0.812 V
	0	1	1	0	1	1.308 V	1	1	1	0	0	1	0.796 V
	0	1	1	0	1	1.292 V	1	1	1	0	1	0	0.780 V
	0	1	1	0	1	1.276 V	1	1	1	0	1	1	0.764 V
	0	1	1	1	0	1.260 V	1	1	1	1	0	0	0.748 V
	0	1	1	1	0	1.244 V	1	1	1	1	0	1	0.732 V
	0	1	1	1	1	1.228 V	1	1	1	1	1	0	0.716 V
	0	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V

IC / SMB Address

Devices	Address	Hex	Bus
ICH6	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	BLUETOOTH
4	FINGER PRINT
	OPTION
	OPTION

System Power States

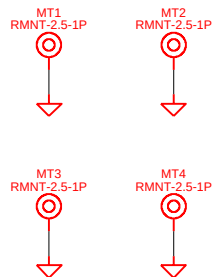
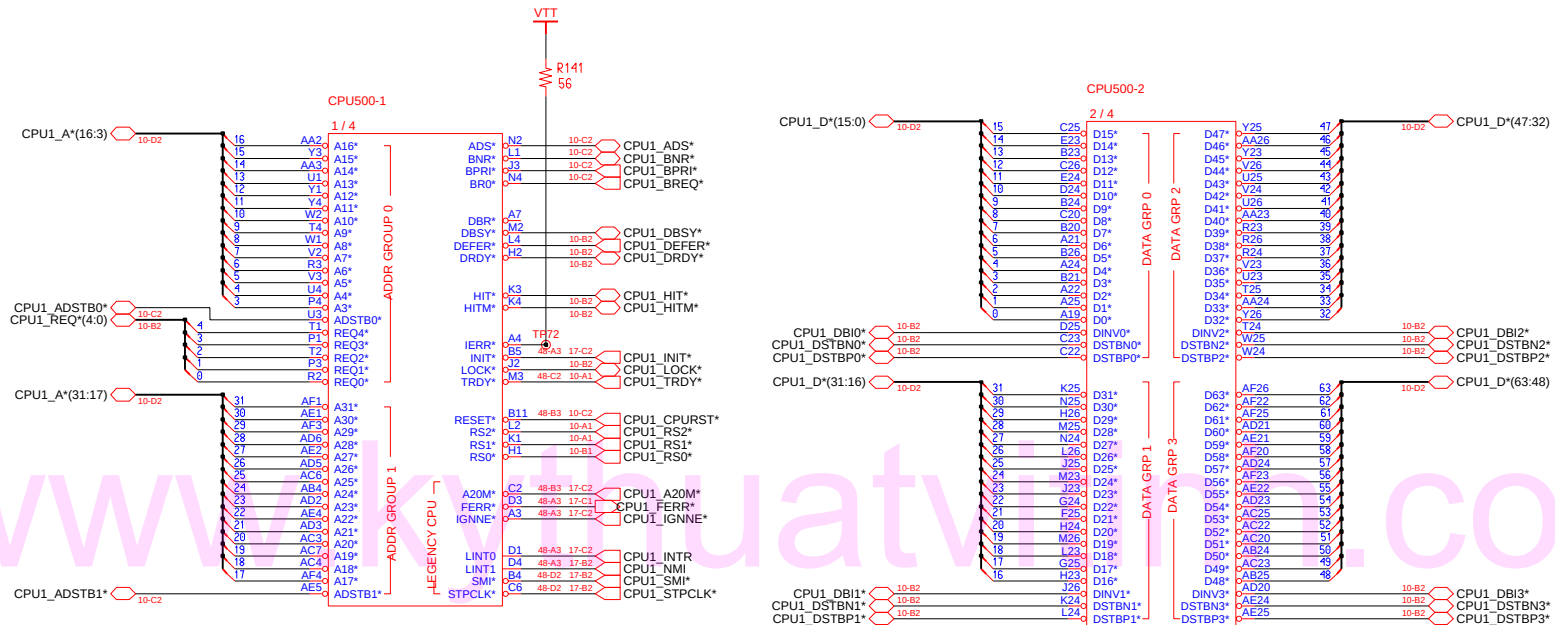
CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.
CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.
CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

REVISION HISTORY

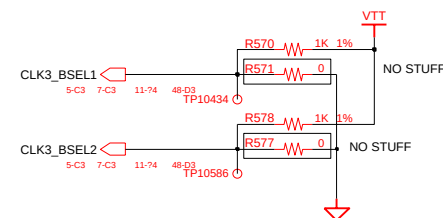
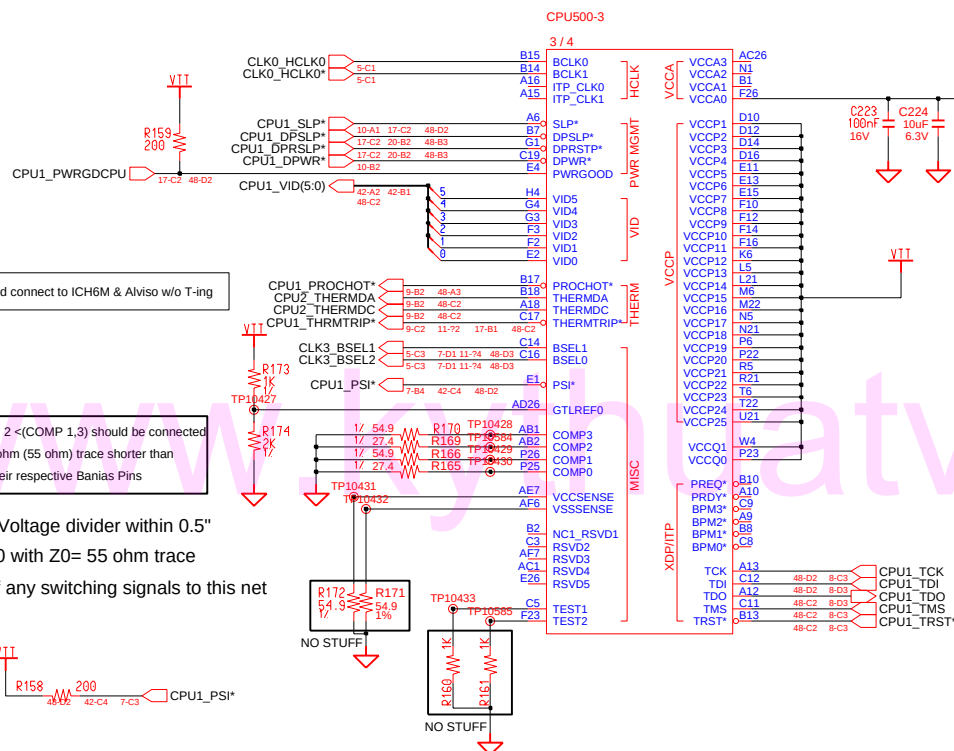
See rev notes in the changes file for more information.

DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG
CHECK	BIN, KK	DEV. STEP	PR		MAIN	ELECTRONICS
APPROVAL	KIM, DW	REV	1.0		BOARD INFORMATION	PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	4	OF 49

1	0	0	133 MHz
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DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN DOTHAN CPU (1/3)	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	6 OF 49	



CPU Core Voltage Table

VID(5.0)						Voltage	VID(5.0)						Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	1.196 V	
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1.180 V	
0	0	0	0	1	0	1.676 V	1	0	0	0	1	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	1.100 V	
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	0	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	0.860 V	
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0.844 V	
0	1	0	1	1	1	1.340 V	1	1	0	1	1	0.828 V	
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0.812 V	
0	1	1	0	0	1	1.308 V	1	1	1	0	0	0.796 V	
0	1	1	0	1	0	1.292 V	1	1	1	0	0	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	0	1	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0.748 V	
0	1	1	1	0	1	1.244 V	1	1	1	1	0	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	0	0.716 V	
0	1	1	1	1	1	1.212 V	1	1	1	1	1	0.700 V	

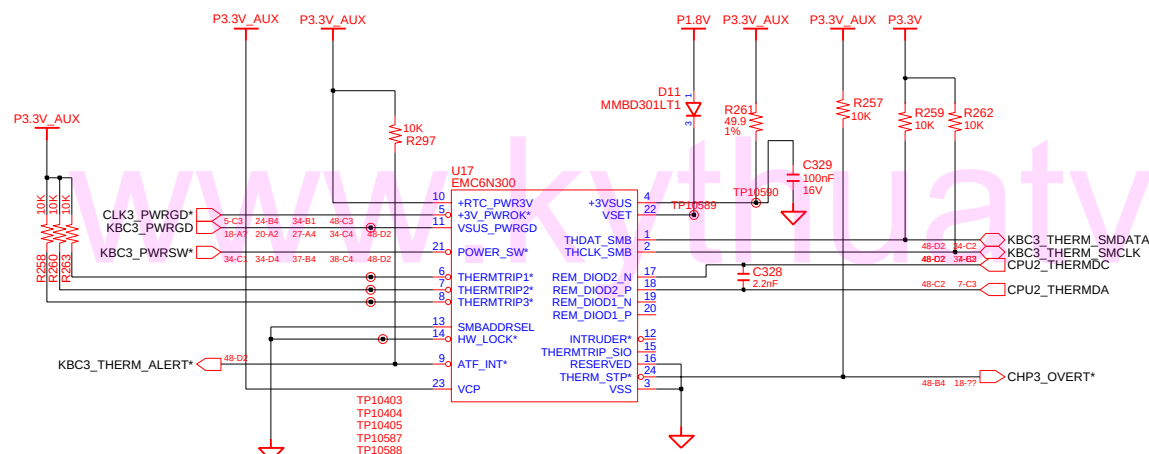
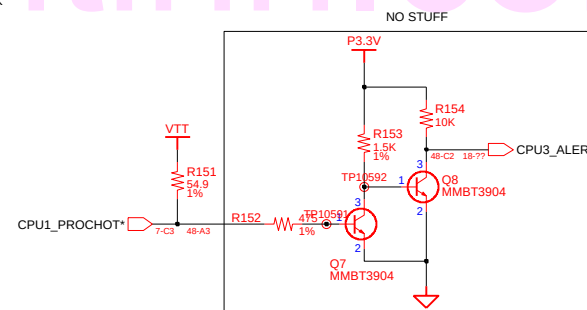
Highest Freq. of Dothan400(1.8GHz)

* Highest Freq. of Dothan533(?? GHz : TBD)

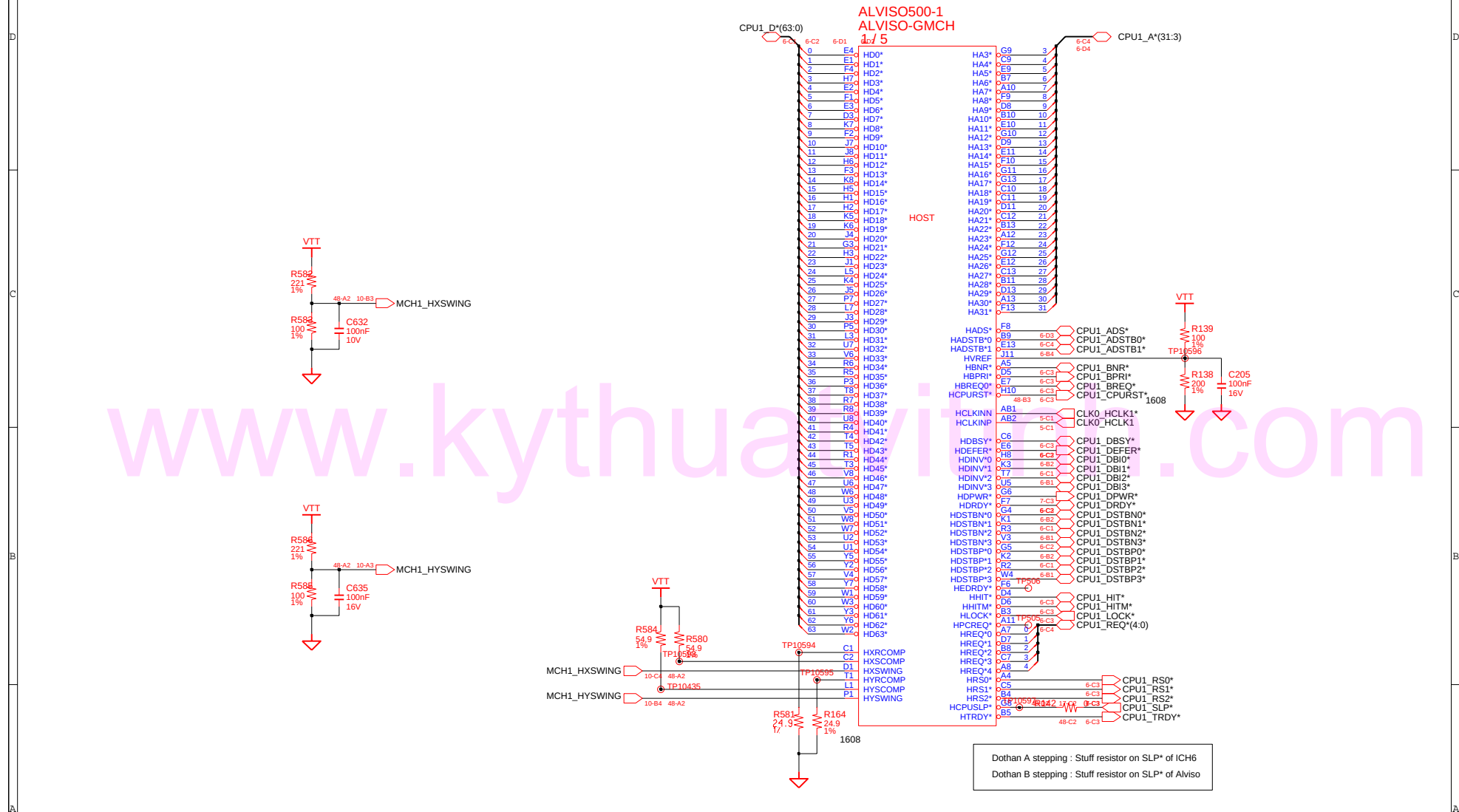
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CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE	LAST EDIT					
				PART NO.	BA41-00451A	

Refer To Thermal Sensor Layout Guidelines.

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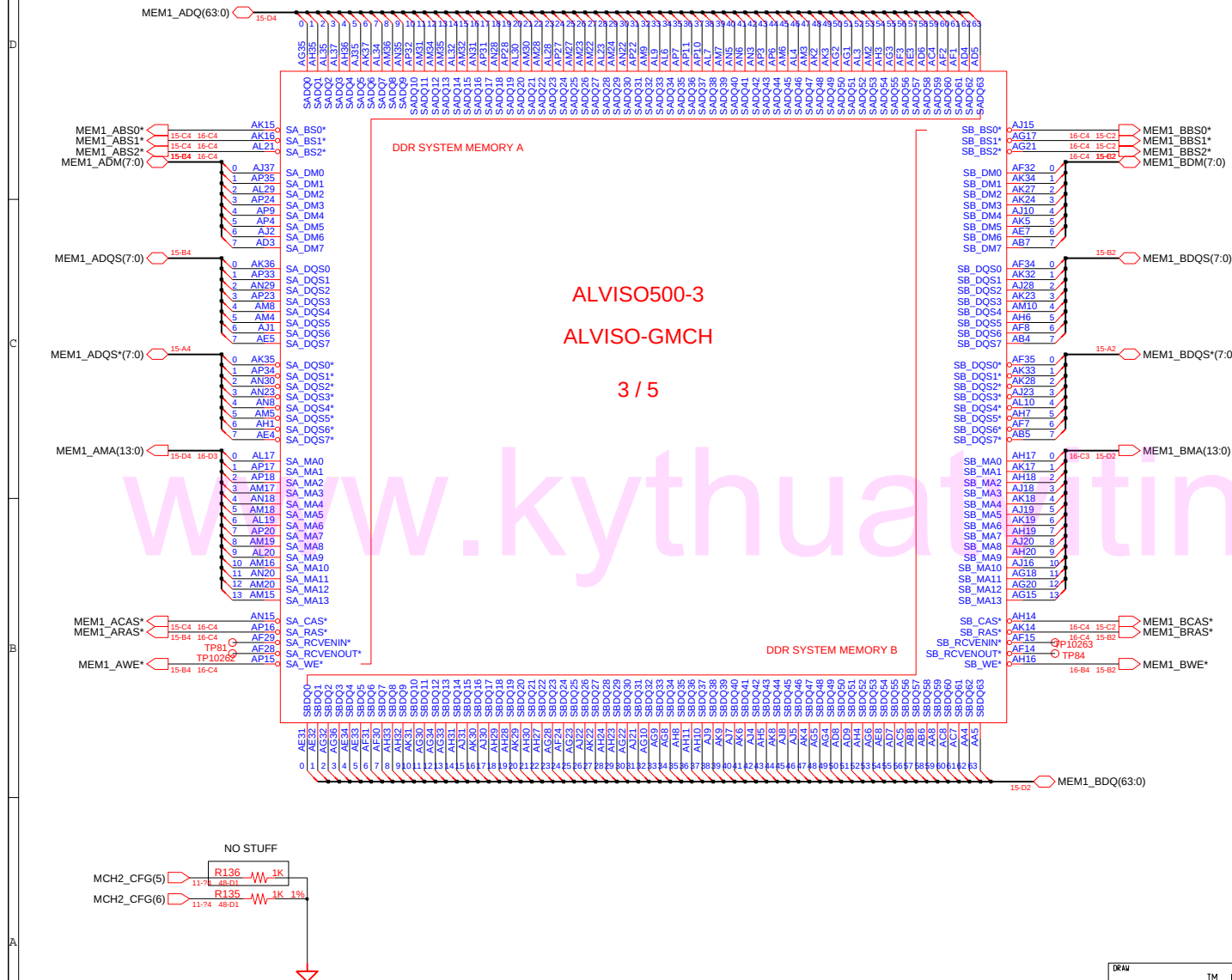


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CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	10	OF 49

Feature	Alviso	Iris(Grantsdale)
VCC_GMCH	VCC 1.05V	VCC 1.5V
VCCP	VTT 1.05V	VTT 1.2V
DMI	x2 / x4	x4 only

DESIGN	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN ALVISO-GMCH(2/5)	
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT		November 5, 2004 8:27:10 PM		PAGE 11 OF 49

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DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

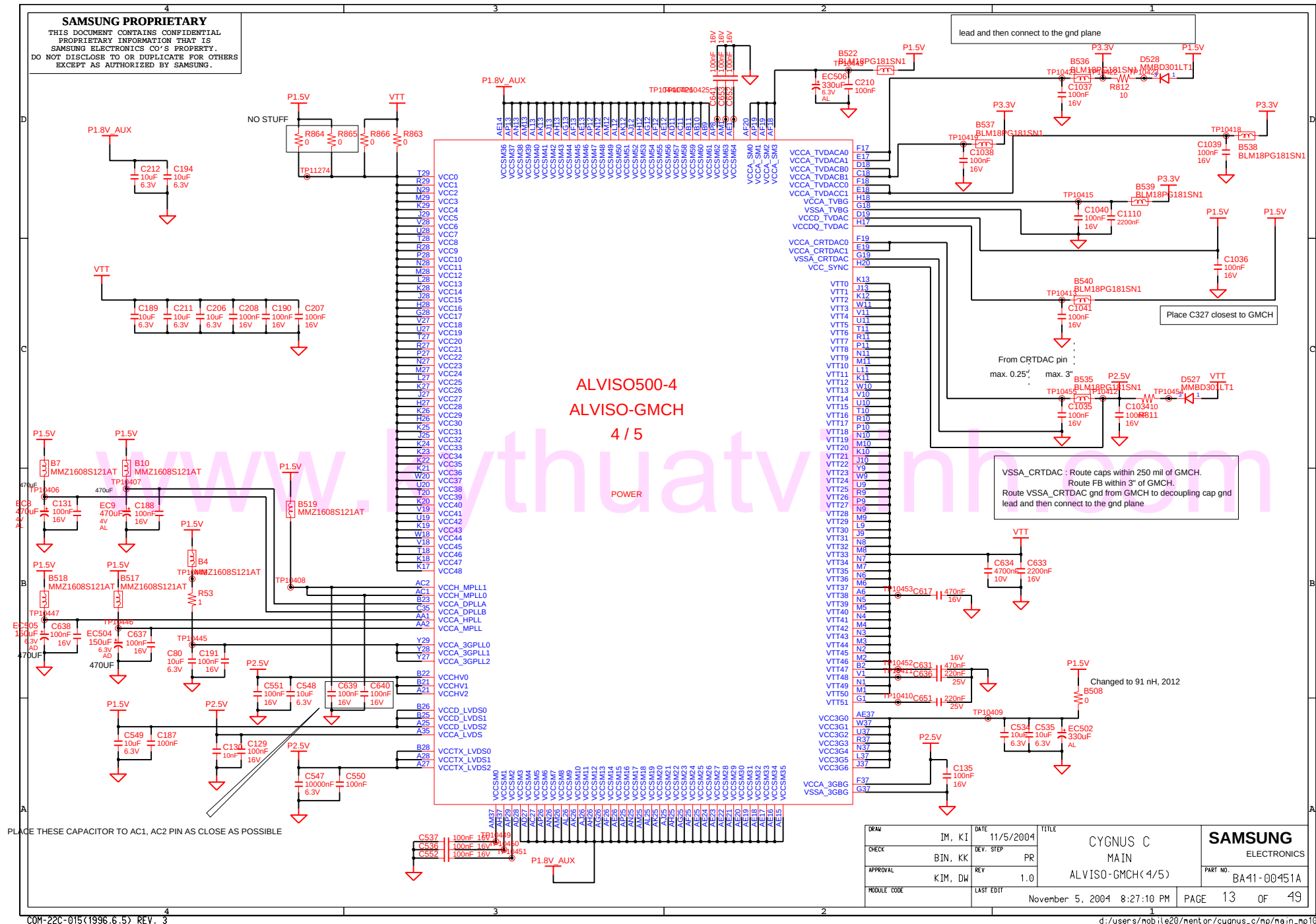
Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

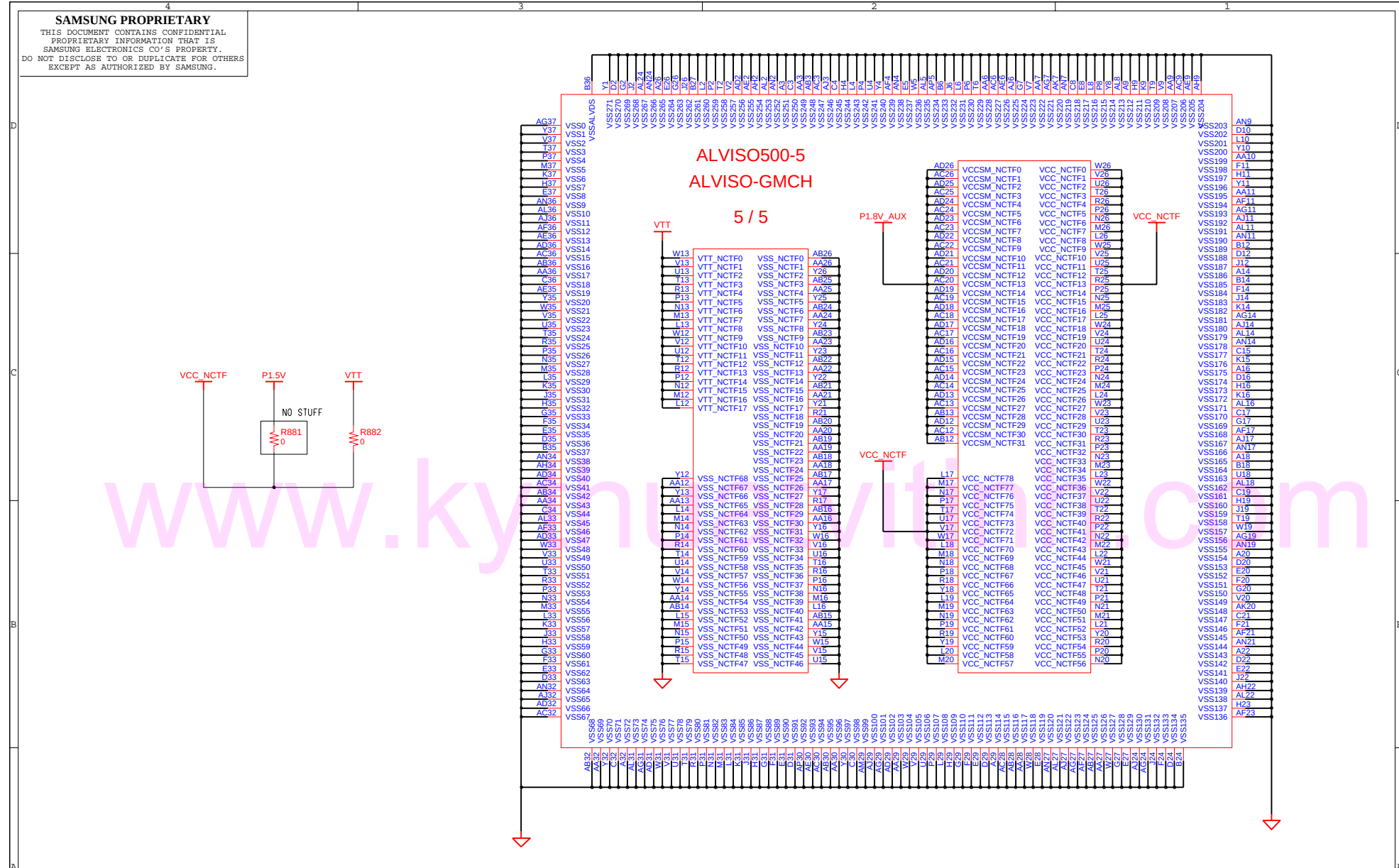
SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	EXP_TXP_4
SDVOC_RED	EXP_TXN_5
SDVOB_ALPHA	EXP_TXP_5
SDVOC_GREEN*	EXP_TXN_6
SDVOC_GREEN	EXP_TXP_6
SDVOC_BLUE*	EXP_TXN_7
SDVOC_BLUE	EXP_TXP_7
SDVOC_CLK*	EXP_TXN_8
SDVOC_CLK	EXP_TXP_8
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	DDR-2	DDR-1
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(10)	TBD	TBD
CFG(11)	TBD	TBD
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0		ALVISO-GMCH(3/5)	
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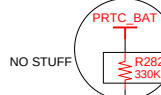




DRAM	IM, K1	DATE	11/5/2004	CYGNUS C MAIN ALVISO-GMCH(5/5)	SAMSUNG ELECTRONICS	
CHECK	BIN, KK	DEV. STEP	PR			
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Enable intergated P1.5V_AUX VRM



U507-1
82801FBM
1/5

CPUSLP*
Dothan A stepping : Stuff resistor on SLP* of ICH6 Dothan B stepping ~ : Stuff resistor on SLP* of Alviso
DPRSLLP*
Dothan A stepping : No Stuff Dothan B stepping ~ : Stuff

1	x1 / g2 Docking			
ACZ_SYNC	PORT X Line	PU	PD	
1	1x2 / 2x1	Stuff	No Stuff	
0	4x1	No Stuff	Stuff	

IDE5_IORDY 32-B2 32-C2 32-C4 48-B2
CHP3_IDEIRQ 20-B1 32-A3 48-B4
IDE5_DACK* 32-B1 32-C1 32-C4 48-B2
IDE5_IOW* 32-B2 32-C2 32-C4 48-B2
IDE5_IOR 32-B1 32-C1 32-C4 48-B2

CLK1_SATA* 5-B1
CLK1_SATA 5-C1

R671 24.9 1% TP10463 AG11
R672 24.9 1% TP10463 AF11

CHP3_AC97_AUD_SDO 30-D4 48-C4 R390 33 5% TP10462 C9
CHP3_AC97_MDC_SDO 33-C4 48-C4 R391 33 5%
CHP3_SATALED* 32-A3 48-B4 AC19

SATA3_RN 32-B4 AE3 SATA0RXN
SATA3_RP 32-B4 AD3 SATA0RXP
SATA3_TN 32-B4 AG2 SATA0TXN
SATA3_TP 32-B4 AF2 SATA0TXP

CHP3_AC97_AUD_BCLK 30-C4 48-C4
CHP3_AC97_AUD_SYNC 30-C4 48-C4 R393 33 5% TP10460 B9
CHP3_AC97_MDC_SYNC 33-C4 48-C4 R392 33 5%
CHP3_AC97_AUD_RST* 33-C4 48-C4 R389 33 5% TP10461 A10
CHP3_AC97_MDC_RST* 33-C4 48-C4 R388 33 5%
CHP3_AC97_SDI0 30-C4 48-C4
CHP3_AC97_SDI1 33-C3 48-C4

CHP3_RTCRST* 17-C4 48-B4
CHP3_INTRUDER* 20-B2 48-B4 TP10459
R695 10M Y501 32.768KHz
C746 0.01nF C747 0.01nF

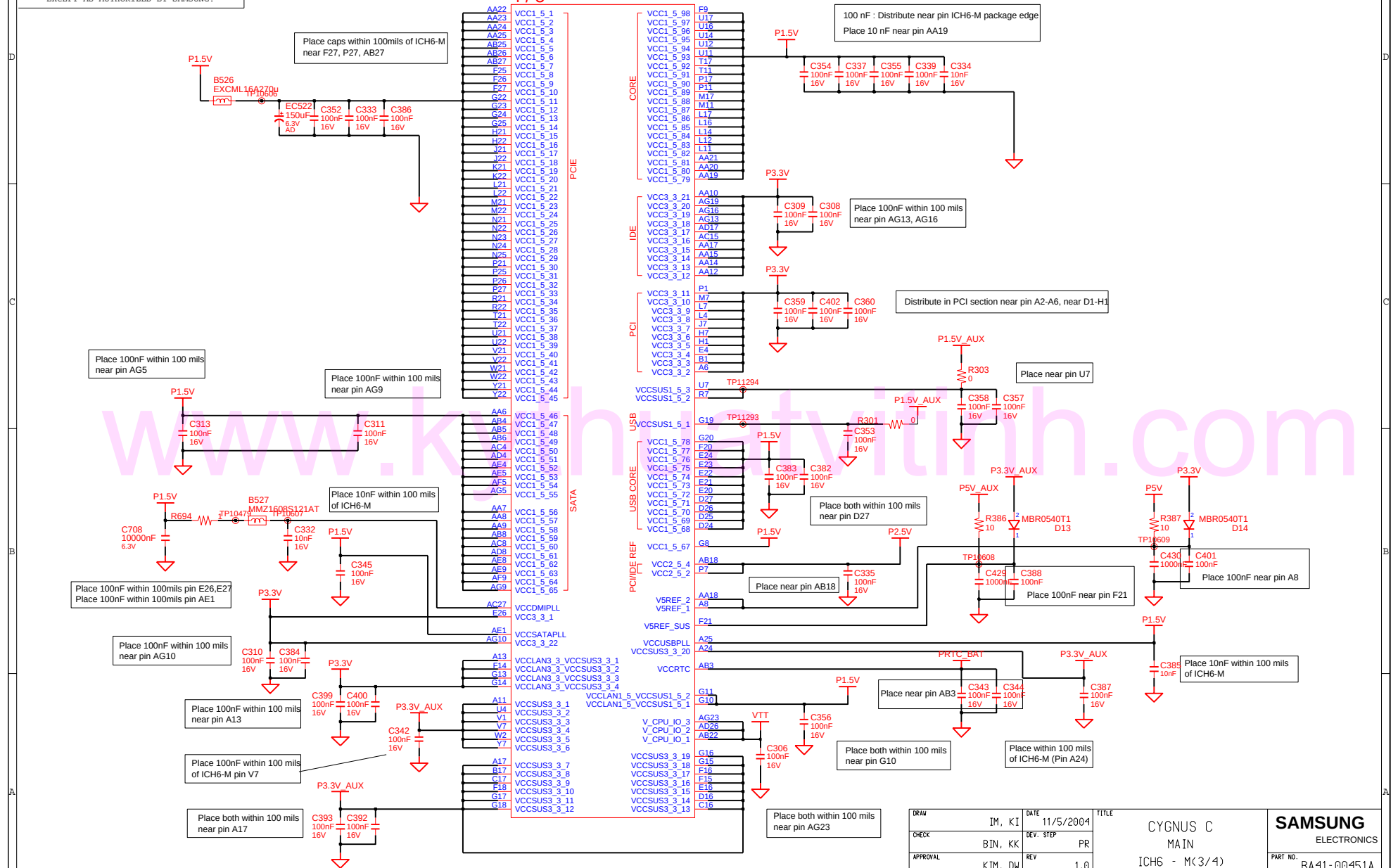
TP10467 TP10468
R675 20K C712 1000nF 6.3V C713 1000nF
TP10458 R674 1M 1% NO STUFF

LAD0_FWH0 P2 0
LAD1_FWH1 N3 1
LAD2_FWH2 N5 2
LAD3_FWH3 N4 3
LDRQ0* LDRQ1* GPI41 P4
LFRAME*_FWH4 N6
CPUSLP* AE27
DPRSLLP*_TP4 AD27
DPRSLLP*_TP2 AD27
FERR* AF24
CPUPWRGD_GPO49 AG25
IGNNE* AE26
INIT3_3V INIT* AE22
INTR* AG24
RCIN* AD23
NMI SMI* AF25
STPCLK* AE26
THRMTRIP* AE23
DA0 AC16
DA1 AB17
DA2 AC17
DCS1* AD16
DCS3* AE17
DD0 AD14
DD1 AF15
DD2 AF14
DD3 AD12
DD4 AE14
DD5 AC11
DD6 AD11
DD7 AB11
DD8 AE13
DD9 AF13
DD10 AB12
DD11 AC13
DD12 AE15
DD13 AF15
DD14 AG15
DD15 AD13
LPC3_LAD(0:3) 48-B2 48-A2 45-B4 37-D1 34-C2 21-C3
LPC3_LFRAME* 48-B2 48-A2 45-B4 37-D1 34-C2 21-C3
CHP3_LDRQ0* 48-B4 37-D1
CHP3_LDRQ1* 48-B4 37-D1
KBC3_A20G CPU1_A20M*
CPU1_SLP* 48-B2 10-A1 7-C3
CPU1_DPRSLLP* 48-B3 20-B2 7-C3
CPU1_DPRSLLP* 48-B3 20-B2 7-C3
CPU1_FERR* 48-A3 6-B3
CPU1_PWRGDCPU AG25
CPU1_IGNNE* AE26
CPU1_FWH3_INIT* AE22
CPU1_INIT* AE27
CPU1_INTR* AG24
KBC3_CPUREST* AD23
CPU1_NMI AF25
CPU1_SMI* AG27
CPU1_STPCLK* AE26
CPU1_THRMTRIP* AE23
IDE5_A0 48-C2 32-C4 32-C2 32-B2
IDE5_A1 48-C2 32-C4 32-C2 32-B2
IDE5_A2 48-C2 32-C4 32-C1 32-B1
IDE5_CS1* 48-C2 32-C4 32-C2 32-B2
IDE5_CS3* 48-C2 32-C4 32-C2 32-B2
IDE5_D(0:15) 48-C2 48-B2 32-D2 48-D2 32-B4 32-E2 32-B1
IDE5_DREQ 48-B2 32-C4 32-C1 32-B1

Place 56 ohm resistor within 2" of ICH6-M
Place PU resistor within 2" of ICH6-M

DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG
CHECK	BIN, KK	DEV. STEP	PR	MAIN		ELECTRONICS
APPROVAL	KIM, DW	REV	1.0	ICH6 - M(1/4)	PART NO.	BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	17	OF 49

U507-4
82801FBM
4 / 5



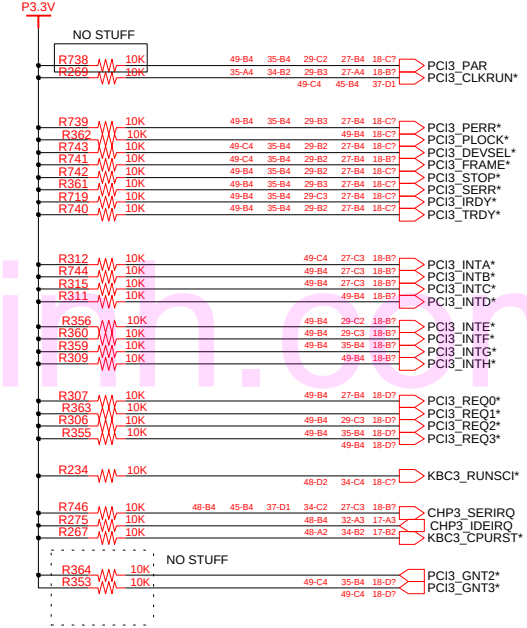
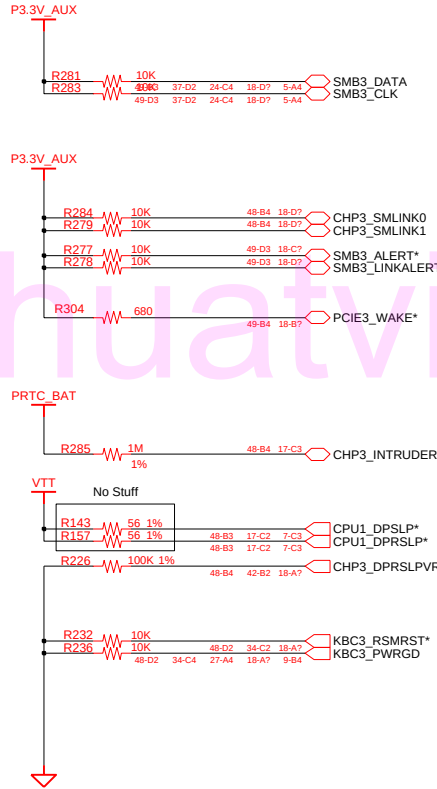
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CHECK		BIN, KK	DEV. STEP	PR		MAIN					
APPROVAL		KIM, DW	REV	1.0		ICHS - M(3/4)		PART NO.		BA11-00451A	
MODULE CODE			LAST EDIT			November 5, 2004 8:27:10 PM			PAGE 19 OF 49		

ICH6-m Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
EEP_DOUT		TBD

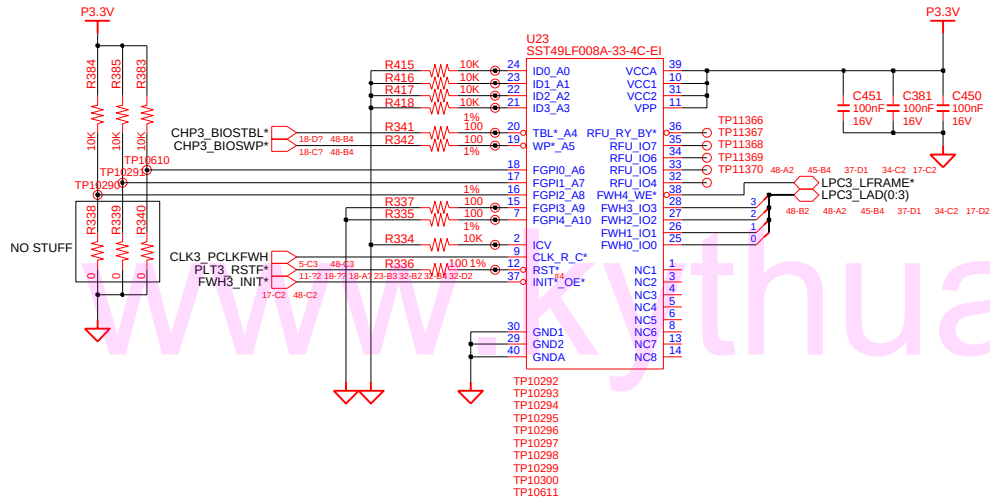
U507-5
82801FBM
5 / 5

AG22	VSS_172	VSS_86	P22
AG20	VSS_171	VSS_85	P16
AG17	VSS_170	VSS_84	P15
AG14	VSS_169	VSS_83	P14
AG12	VSS_168	VSS_82	P13
AG7	VSS_167	VSS_81	P12
AG3	VSS_166	VSS_80	N17
AG1	VSS_165	VSS_79	N16
AF26	VSS_164	VSS_78	N15
AF12	VSS_163	VSS_77	N14
AF10	VSS_162	VSS_76	N13
AF7	VSS_161	VSS_75	N12
AF3	VSS_160	VSS_74	N11
AF1	VSS_159	VSS_73	N7
AE25	VSS_158	VSS_72	N1
AE21	VSS_157	VSS_71	M27
AE12	VSS_156	VSS_70	M26
AE11	VSS_155	VSS_69	M25
AE10	VSS_154	VSS_68	M15
AE7	VSS_153	VSS_67	M14
AE6	VSS_152	VSS_66	M13
AE2	VSS_151	VSS_65	M12
AD24	VSS_150	VSS_64	M4
AD18	VSS_149	VSS_63	L25
AD15	VSS_148	VSS_62	L24
AD10	VSS_147	VSS_61	L23
AD6	VSS_146	VSS_60	L15
AD2	VSS_145	VSS_59	L13
AD1	VSS_144	VSS_58	K27
AC26	VSS_143	VSS_57	K26
AC24	VSS_142	VSS_56	K25
AC23	VSS_141	VSS_55	K7
AC22	VSS_140	VSS_54	K1
AC12	VSS_139	VSS_53	J25
AC10	VSS_138	VSS_52	J23
AC6	VSS_137	VSS_51	J22
AC3	VSS_136	VSS_50	J4
AB19	VSS_135	VSS_49	H27
AB10	VSS_134	VSS_48	H25
AB9	VSS_133	VSS_47	H23
AB7	VSS_132	VSS_46	G21
AB2	VSS_131	VSS_45	G12
AA16	VSS_129	VSS_43	G9
AA13	VSS_128	VSS_42	G1
AA11	VSS_127	VSS_41	F22
AA4	VSS_126	VSS_40	F19
Y27	VSS_125	VSS_39	F4
Y26	VSS_124	VSS_38	E27
Y23	VSS_123	VSS_37	E25
Y6	VSS_122	VSS_36	E13
W25	VSS_121	VSS_35	E12
W24	VSS_120	VSS_34	E11
W23	VSS_119	VSS_33	E14
W1	VSS_118	VSS_32	D22
W7	VSS_117	VSS_31	D20
V27	VSS_116	VSS_30	D19
V26	VSS_115	VSS_29	D18
V23	VSS_114	VSS_28	D17
V4	VSS_113	VSS_27	D13
U25	VSS_112	VSS_26	D10
U24	VSS_111	VSS_25	D7
U23	VSS_110	VSS_24	D1
U15	VSS_109	VSS_23	C22
U13	VSS_108	VSS_22	C20
U7	VSS_107	VSS_21	C18
T27	VSS_106	VSS_20	C14
T26	VSS_105	VSS_19	C4
T23	VSS_104	VSS_18	B25
T16	VSS_103	VSS_17	B24
T15	VSS_102	VSS_16	B23
T14	VSS_101	VSS_15	B21
T13	VSS_100	VSS_14	B19
T7	VSS_99	VSS_13	B15
T1	VSS_98	VSS_12	B13
R25	VSS_97	VSS_11	A26
R24	VSS_96	VSS_10	A23
R23	VSS_95	VSS_9	A21
R17	VSS_94	VSS_8	A19
R16	VSS_93	VSS_7	A15
R15	VSS_92	VSS_6	A12
R14	VSS_91	VSS_5	A9
R13	VSS_90	VSS_4	A7
R12	VSS_89	VSS_3	A4
R11	VSS_88	VSS_2	A1
R4	VSS_87	VSS_1	A1



DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0		ICH6 - M(4/4)	PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	20	OF 49

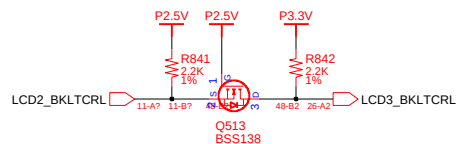
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- | | | | |
|----|--|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| OE | INIT. I/O VALUE | 7E | TEST COPROCESSOR IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 | RE-INIT. ON-BOARD I/O PORT |
| 16 | CHECK CHECKSUM | 88 | INIT. BIOS DATA ROM |
| 18 | 8254 TIMER INIT. | 8A | INIT.EXTENDED BIOS DATA AREA |
| 1A | 8237 DMA CONTROLLER INIT. | 8C | INIT. FDD CONTROLLER |
| 1C | RESET INTERRUPT CONTROLLER | 9A | SHADOW OPTION ROMS |
| 20 | TEST DRAM REFRESH | 9C | SETUP POWER MANAGEMENT |
| 22 | TEST 8742 KEYBOARD CONTROLLER | 9E | ENABLE H/W INTERRUPT |
| 24 | SET ES SEGMENT REG. TO 4GB | A0 | SET TIME OF DAY |
| 26 | ENABLE A20 | A4 | INIT. TYPOMATIC RATE |
| 28 | AUTO SIZING DRAM | A8 | ERASE F2 PROMPT |
| 32 | COMPUTE THE CPU SPEED | AA | SCAN FOR F2 KEY STROKE |
| 34 | TESET CMOS RAM | AC | ENTER SETUP |
| 38 | SHADOW SYSTEM BIOS ROM | AE | CLEAR IN POST FLAG |
| 3A | AUTO SIZING CACHE | B0 | CHECK FOR ERRORS |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B4 | ONE BEEP |
| 42 | INIT. INTERRUPT VECTOR | B6 | CHECK PASSWORD (OPTION) |
| 44 | INIT. BIOS INTERRUPT | B7 | ACPI INIT |
| 46 | CHECK ROM COPYRIGHT NOTICE | BA | DMI INIT |
| 47 | INIT. I20 SUPPORT IF INSTALLED | BE | CLEAR SCREEN |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | C0 | TRY BOOT WITH INT19 |
| 49 | INIT. PCI BUS AND DEVICE | D0 | INTERRUPT HANDLER ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D2 | UNKNOWN INTERRUPT ERROR |
| 4C | SHADOW VIDEO BIOS ROM | D4 | PENDING INTERRUPT ERROR |
| 50 | DISPLAY CPU TYPE AND SPEED | D6 | SHUTDOWN 5 |
| 52 | TEST KEYBOARD | D8 | SHUTDOWN ERROR |
| 54 | SET KEYCLICK IF ENABLED | DA | EXTENDED BLOCK MOVE |
| 56 | ENABLE KEYBOARD | DC | SHUTDOWN 10 |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 89 | ENABLE NMI |
| 5A | DISPLAY "PRESS SETUP" | 90 | INIT. HDD CONTROLLER |
| 5C | TEST RAM BETWEEN 512K AND 640K | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 60 | TEST EXTENDED MEMORY | 92 | JUMP TO USER PATCH 2 |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 94 | DISABLE A20 ADDRESS LINE |
| 64 | JUMP TO USER PATCH 1 | 96 | CLEAR HUGE ES SEGMENT REG. |
| | | 98 | SEARCH FOR OPTION ROMS |

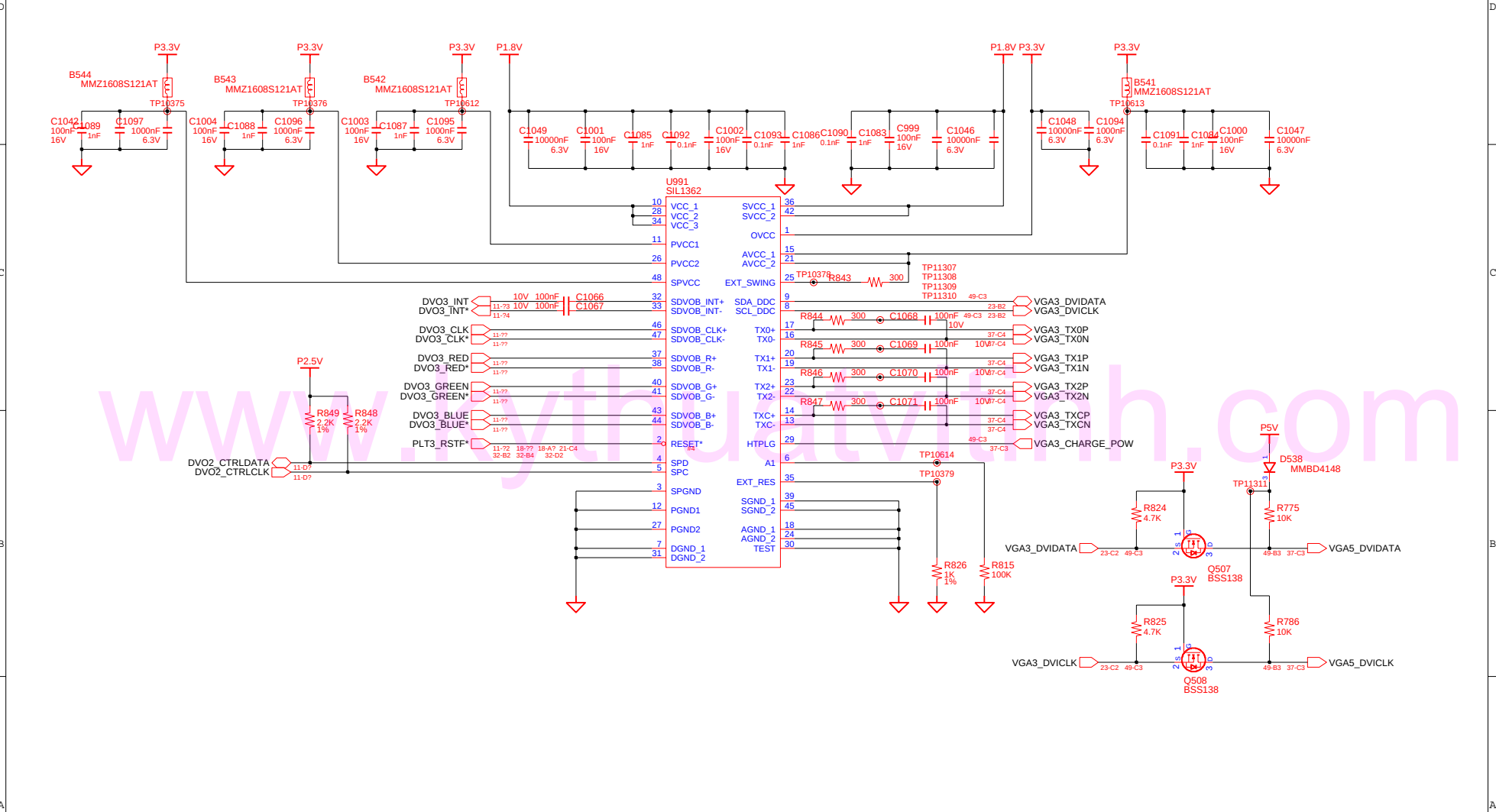
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CHECK	BIN, KK	DEV. STEP	PR		MAIN	ELECTRONICS
APPROVAL	KIM, DW	REV	1.0		FIRMWARE HUB	PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	21	OF 49

2



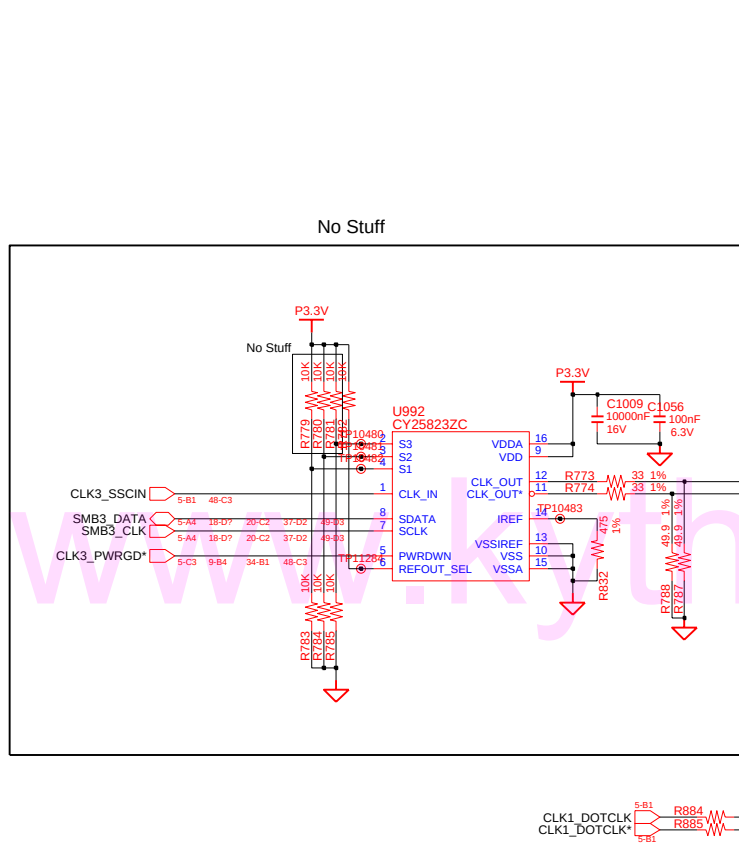
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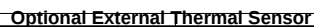


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CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	23	OF 49

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COM-22C-015(1996.6.5) REV. 3

A

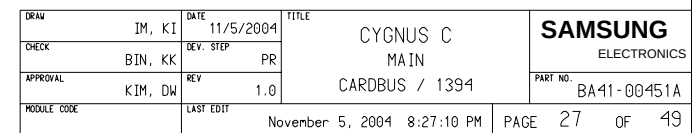
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C79
100nF
16V

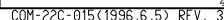


COM-22C-015(1996.6.5) REV. 3

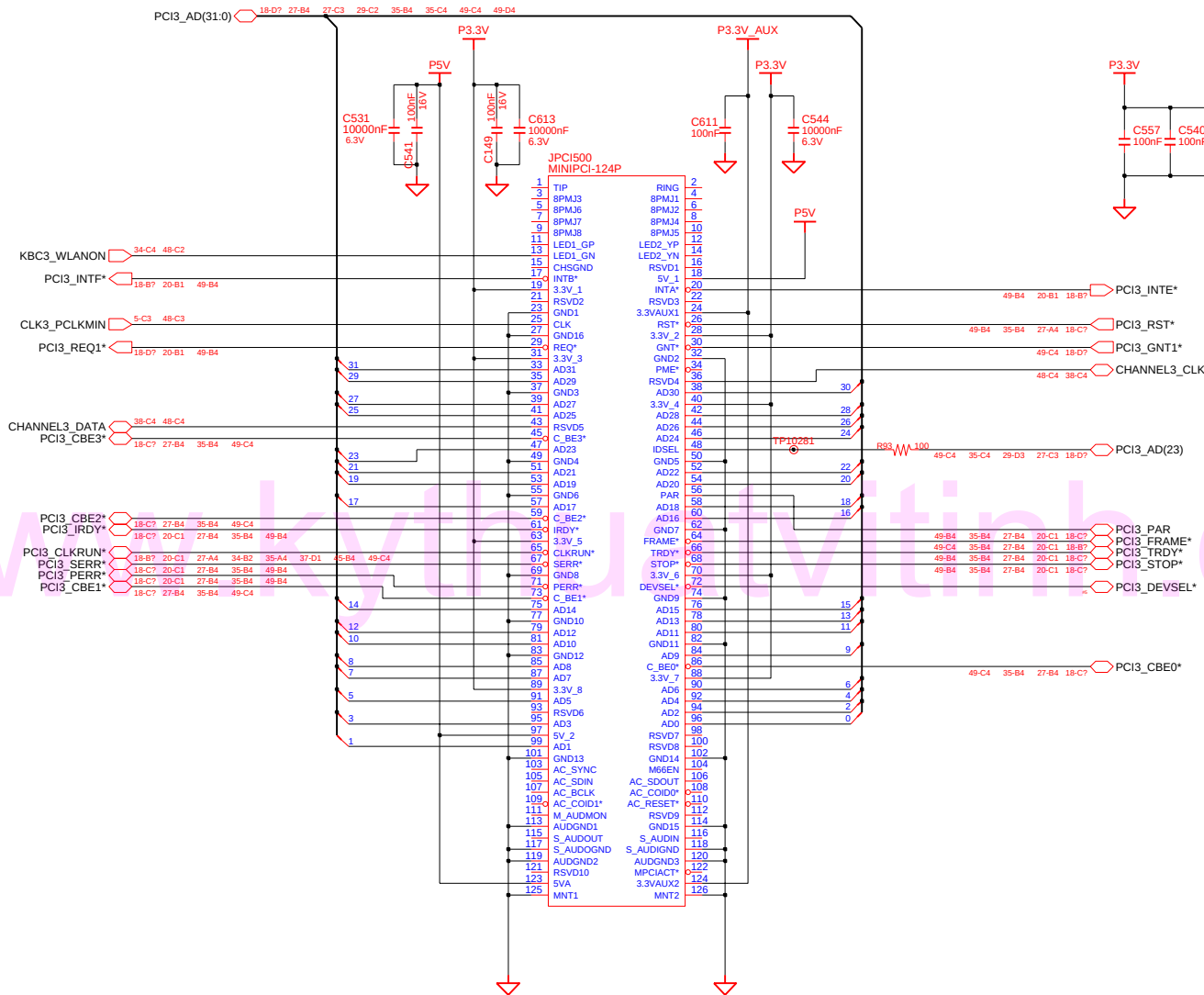
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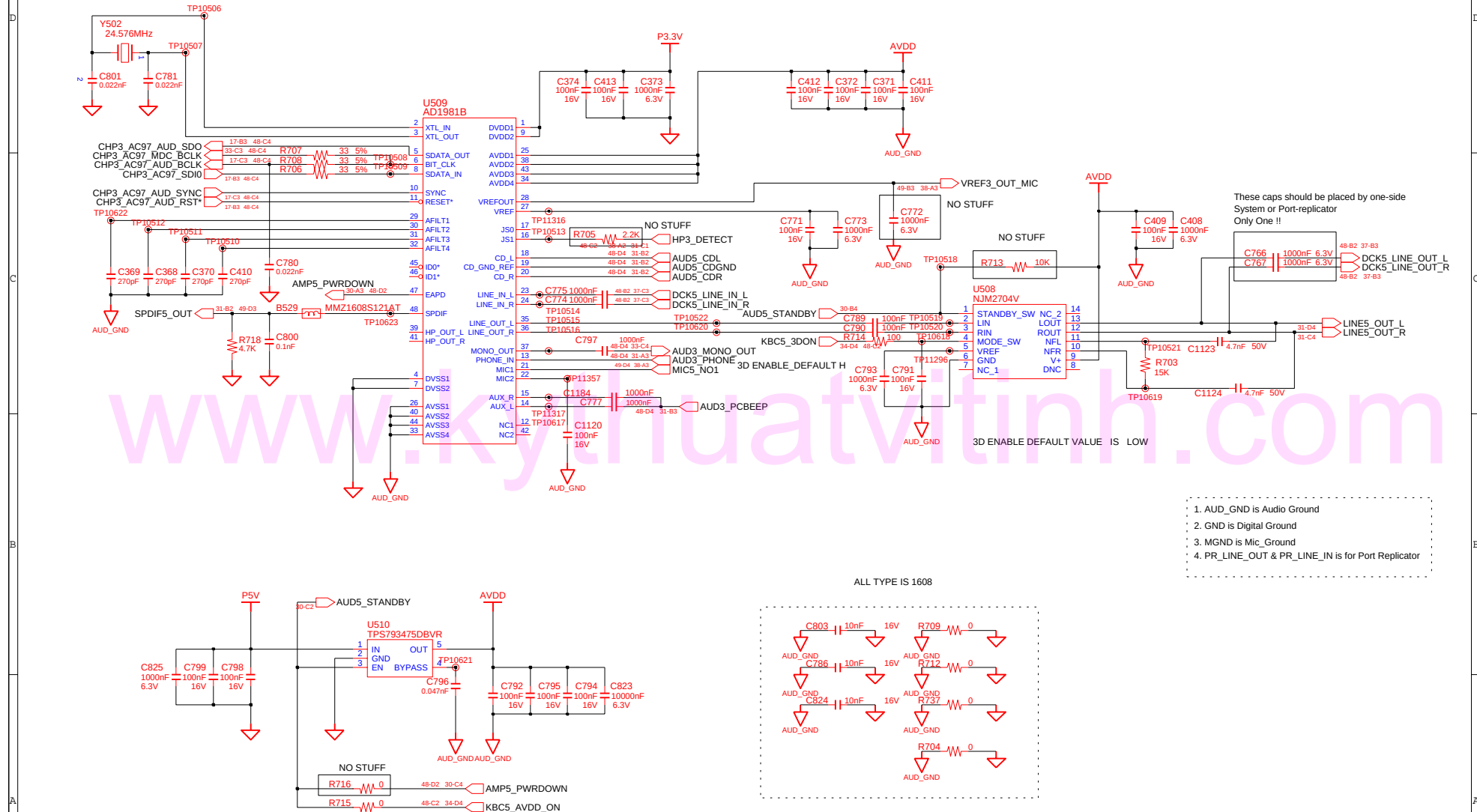


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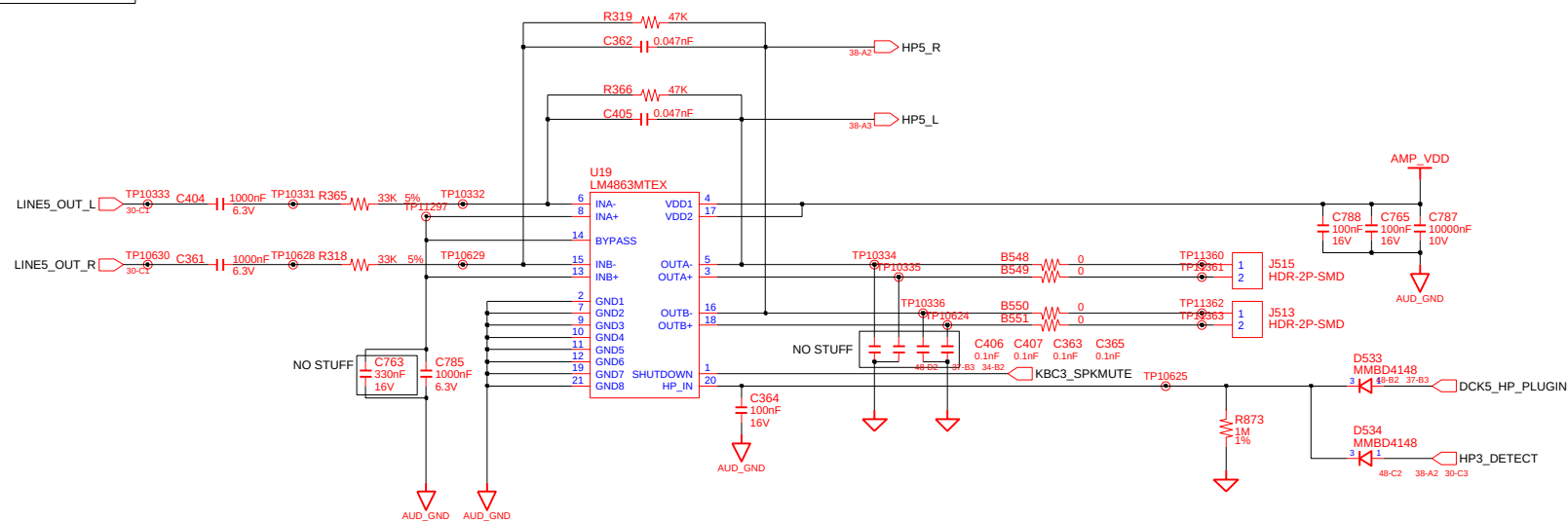


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CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	29	OF 49

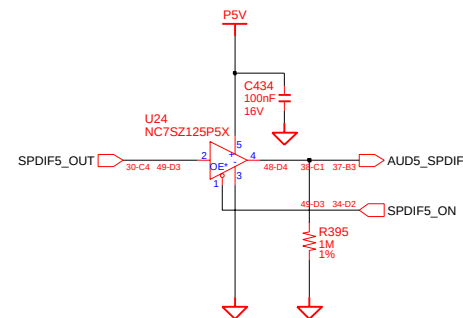
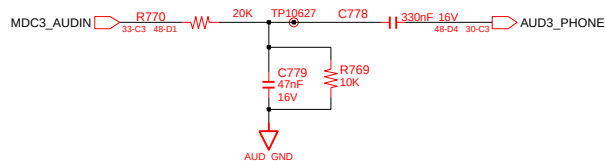
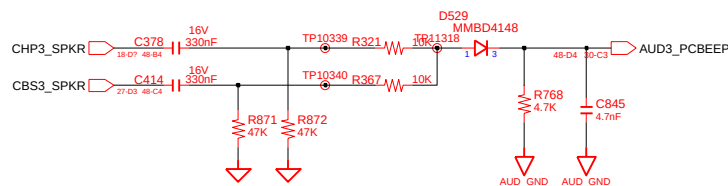
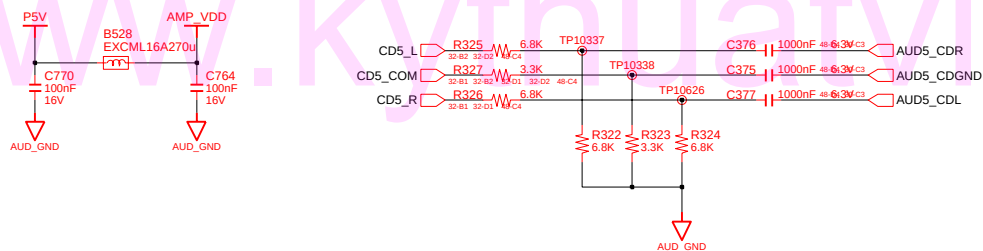
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DRAW	IM, KI	DATE	11/5/2004	TITLE CYGNUS C MAIN AUDIO CODEC & AMP		SAMSUNG ELECTRONICS		
CHECK	BIN, KK	DEV. STEP	PR					
APPROVAL	KIM, DW	REV	1.0					
MODULE CODE	LAST EDIT							
				November 5, 2004 8:27:10 PM	PAGE	30	OF	49



- 1.HP_IN SHOULD BE USED FOR PORT_REPLICATOR JACK SENSE AND SPDIF_JACK SENSE
2. PR_JS SHOULD BE IN MAIN B'D
PR_JS SHOULD HAVE 100Kohm RESISTOR WITH PULL_DOWN
- 3.PORT_REPLICATOR SHOULD HAVE 10Kohm with Pull_up

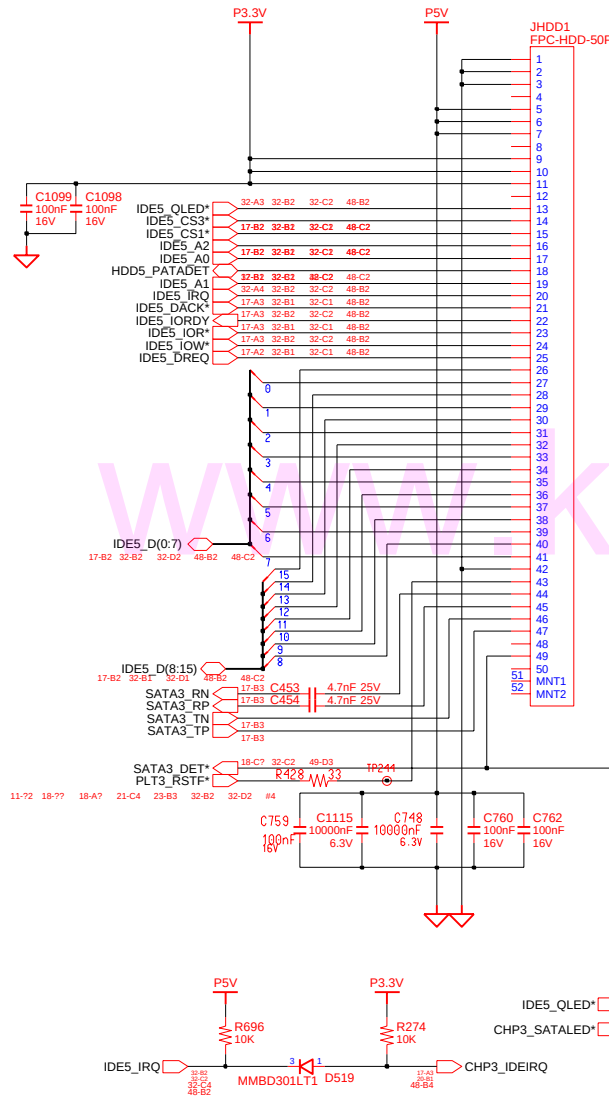


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CHECK	BIN, KK	DEV. STEP	PR		
APPROVAL	KIM, DW	REV	1.0		
MODULE CODE	LAST EDIT		November 5, 2004 8:27:10 PM		

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Main to HDD

NO STUFF

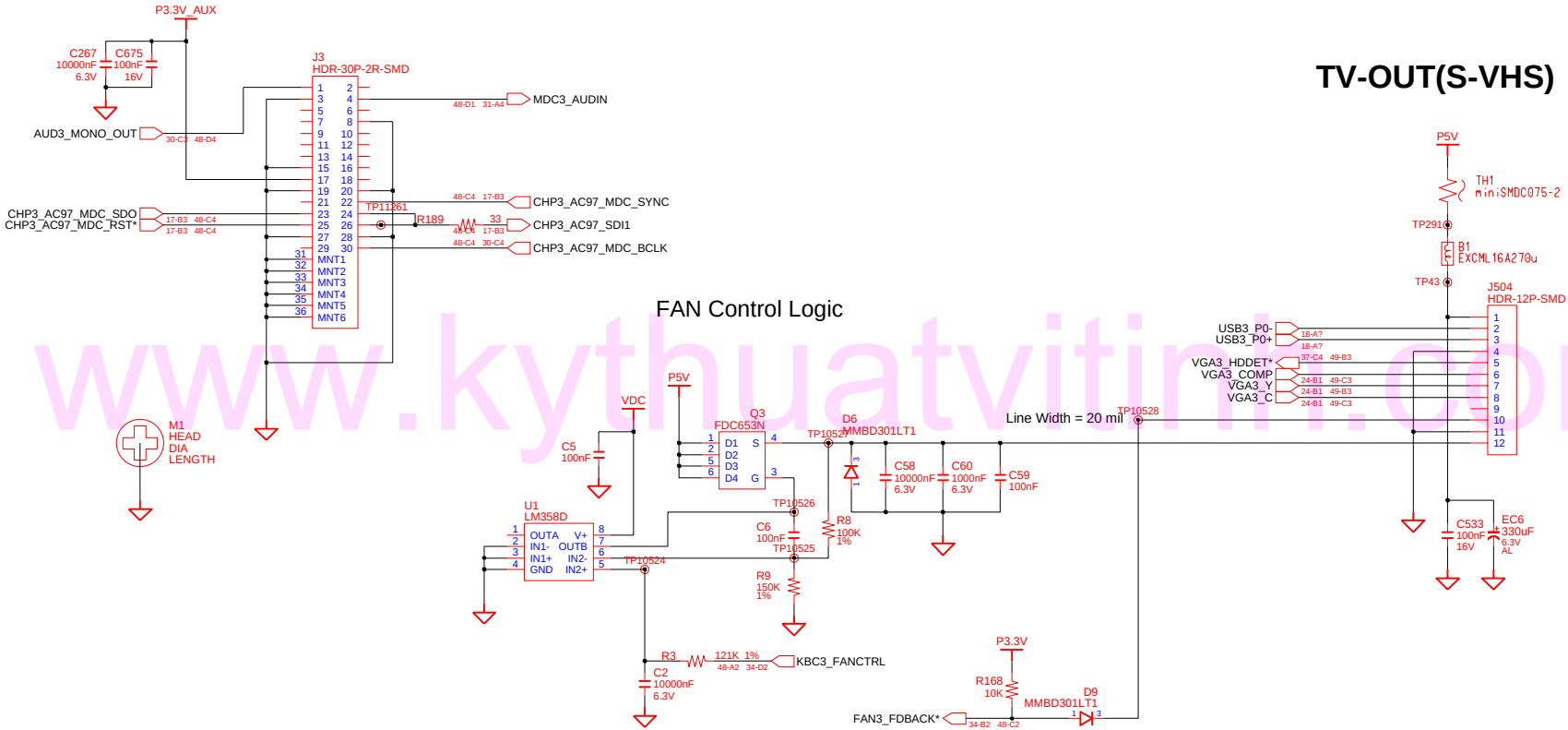


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MDC Connector

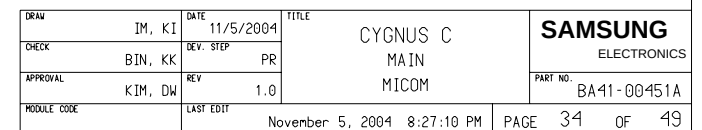
TV-OUT(S-VHS)

FAN Control Logic

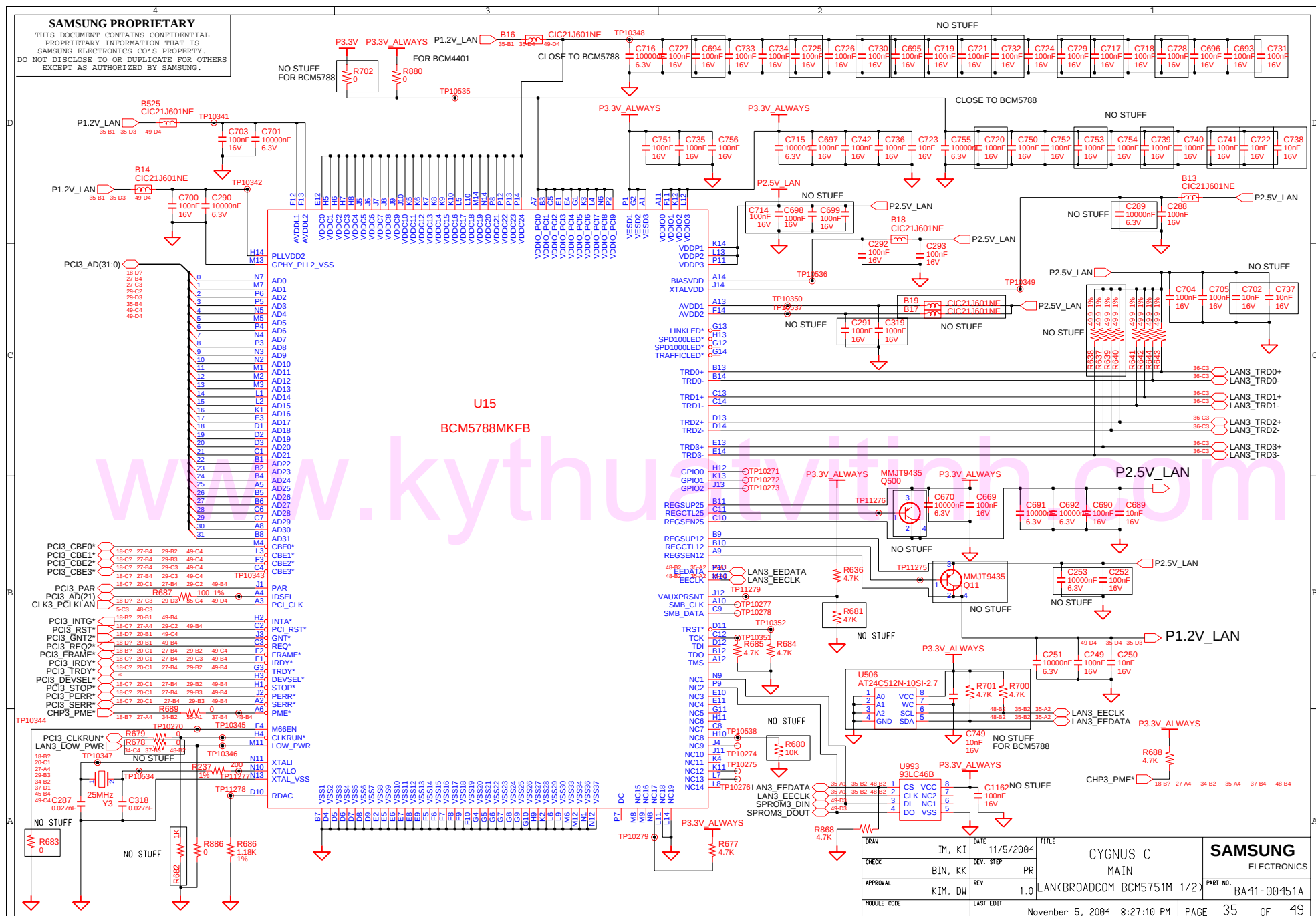


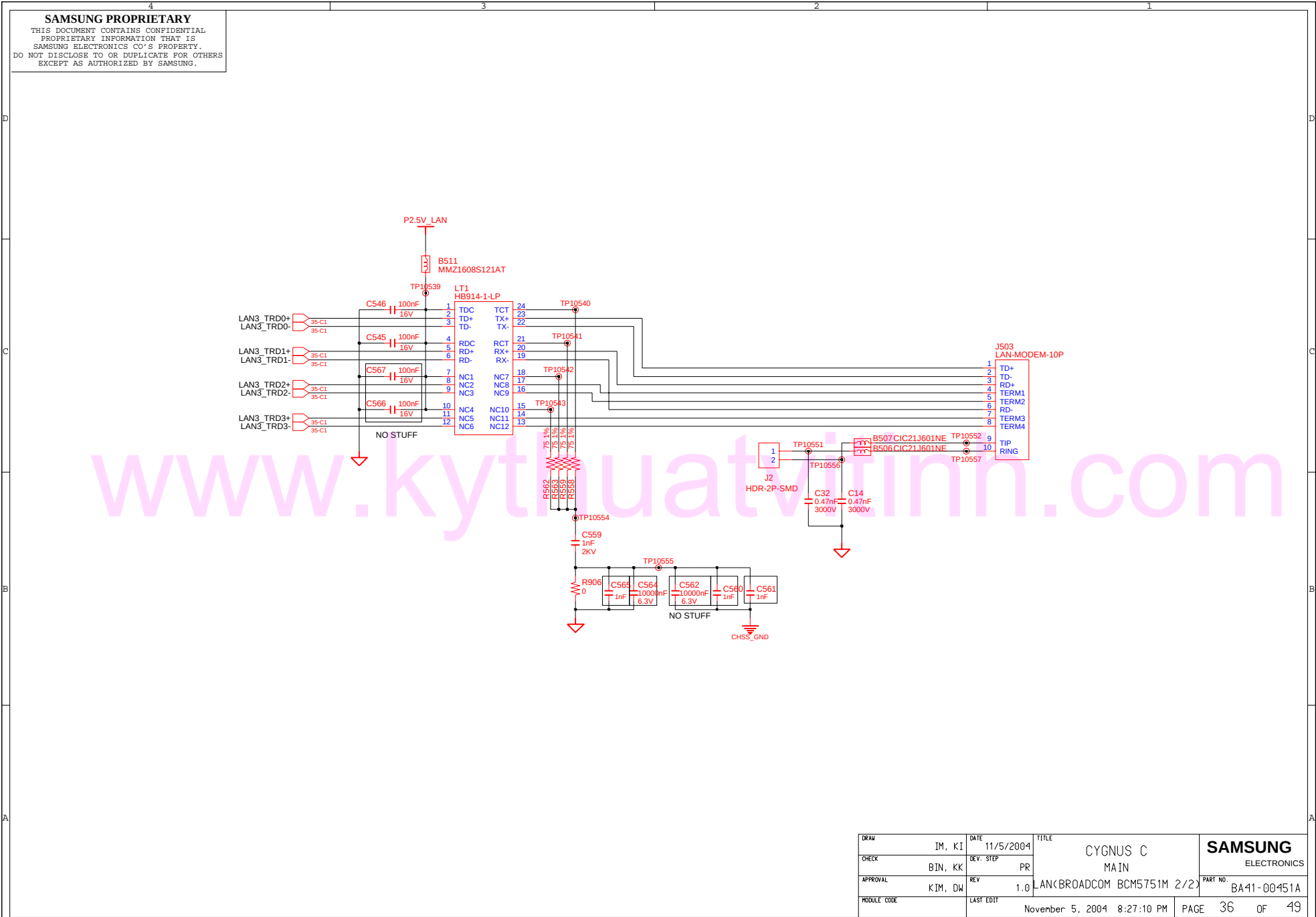
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CHECK	BIN, KK	DEV. STEP	PR	MAIN	MAIN	
APPROVAL	KIM, DW	REV	1.0	MDC MODEM / TV-OUT(SVHS)	PART NO.	BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	33	OF 49

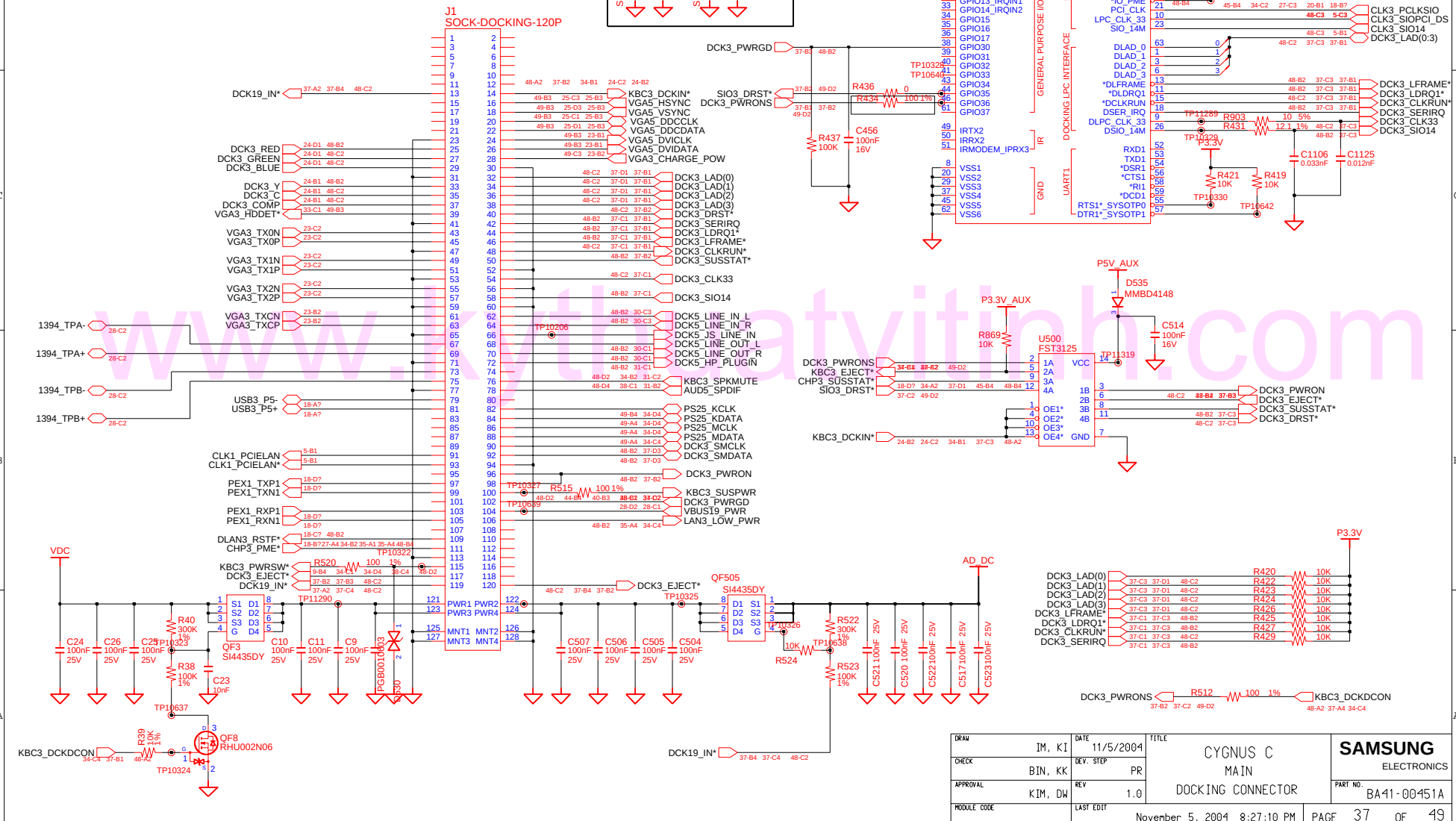
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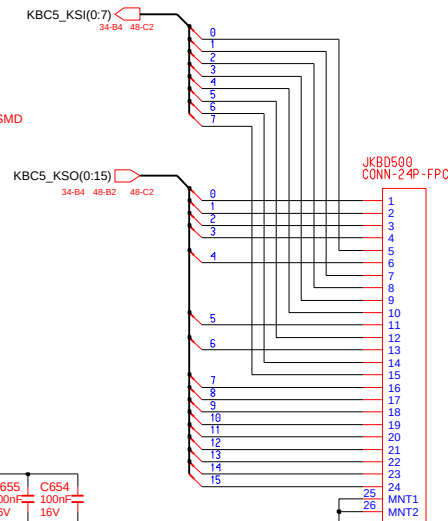
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CHECK	BIN, KK	DEV. STEP	PR						
APPROVAL	KIM, DW	REV	1.0					PART NO.	BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM					PAGE	37 OF 49

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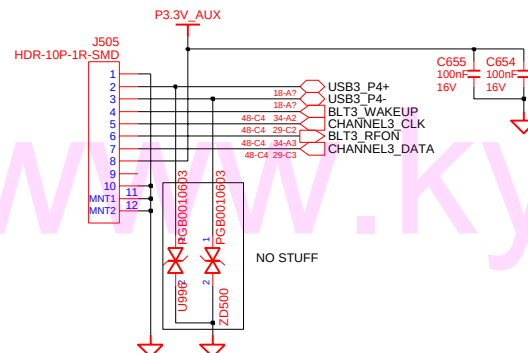
KEYBOARD

Main to DC/DC BOARD

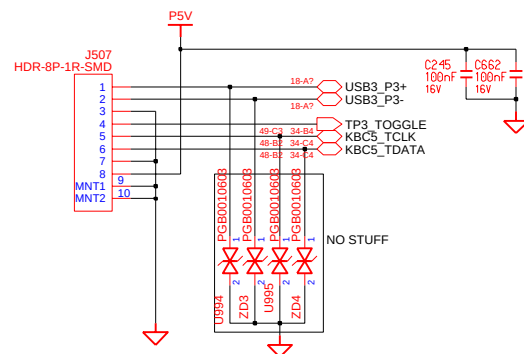
MAIN TO ON-TOP



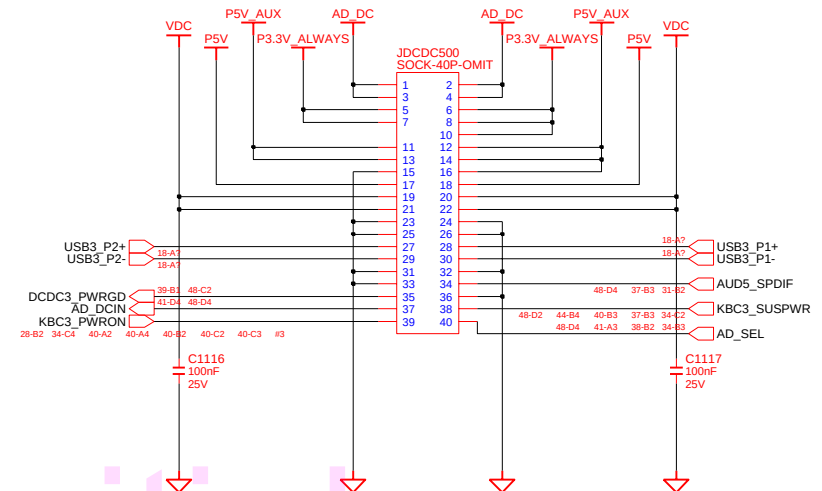
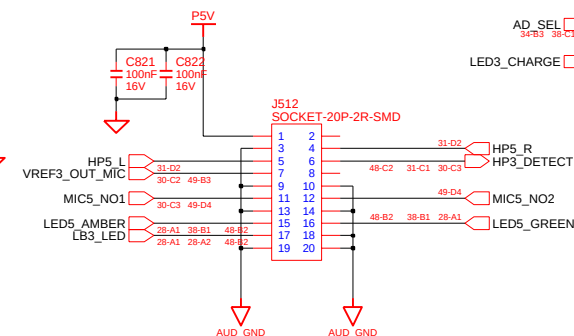
BLUETOOTH CONNECTOR



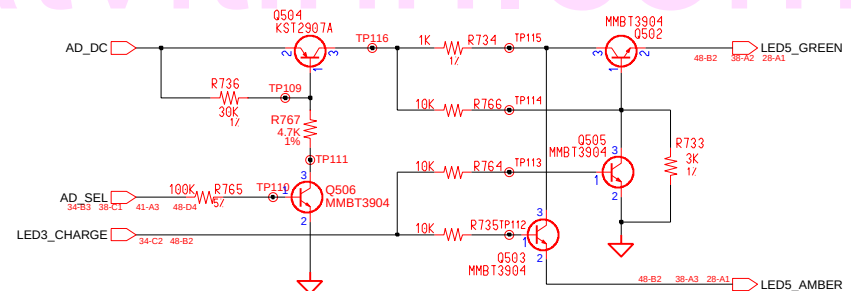
TOUCHPAD CONNECTOR



AUDIO CONNECTOR

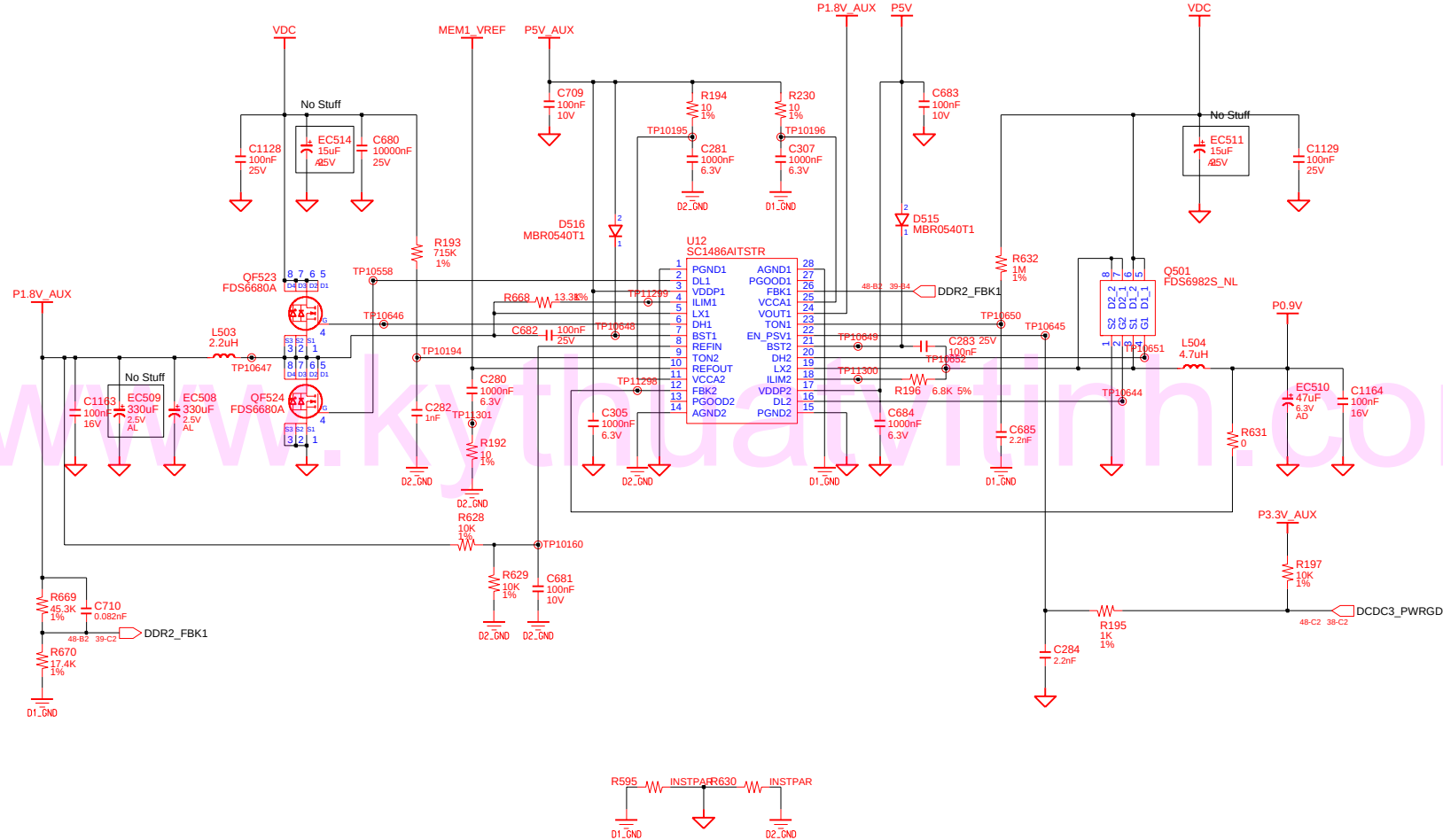


ADAPTER IN/CHARGING LED



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CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	38	OF 49

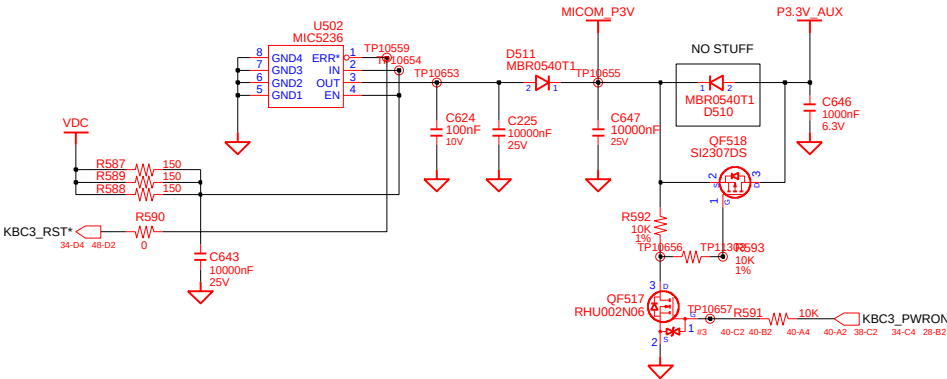
DDR Power



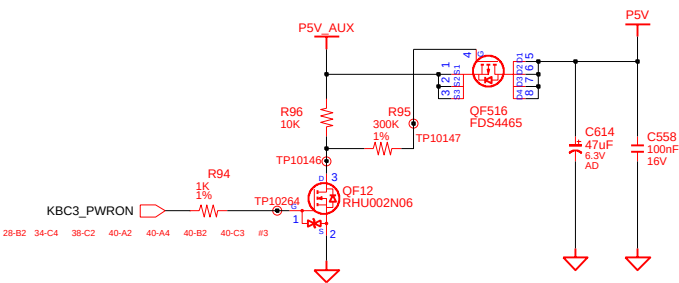
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CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	39	OF 49

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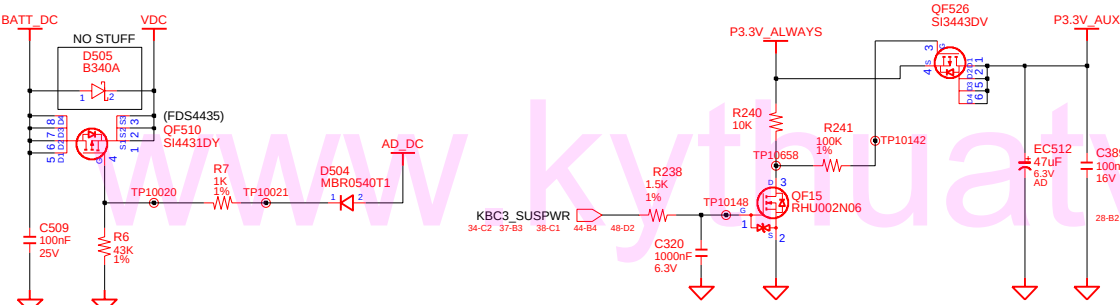
MICOM_P3V Power



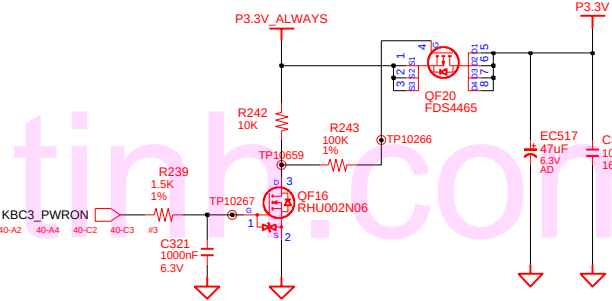
Switched Power On (P5V)



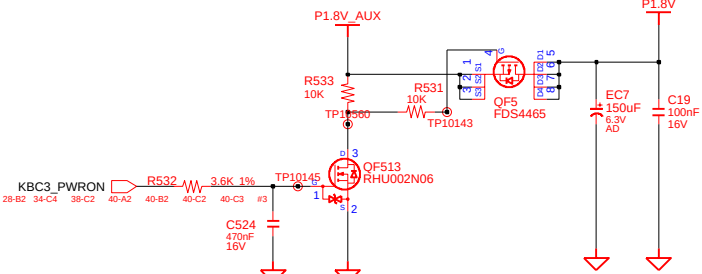
Switched Power On (P3.3V_AUX)



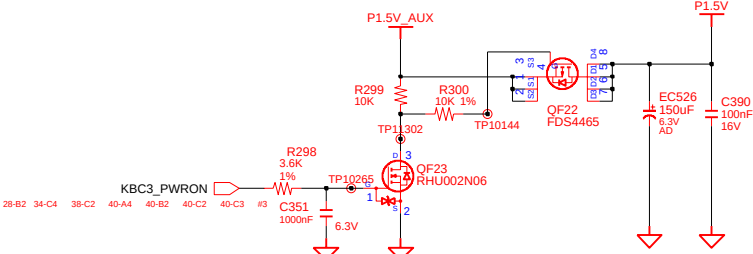
Switched Power On (P3.3V)



Switched Power On (P1.8V)

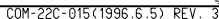


Switched Power On (P1.5V)



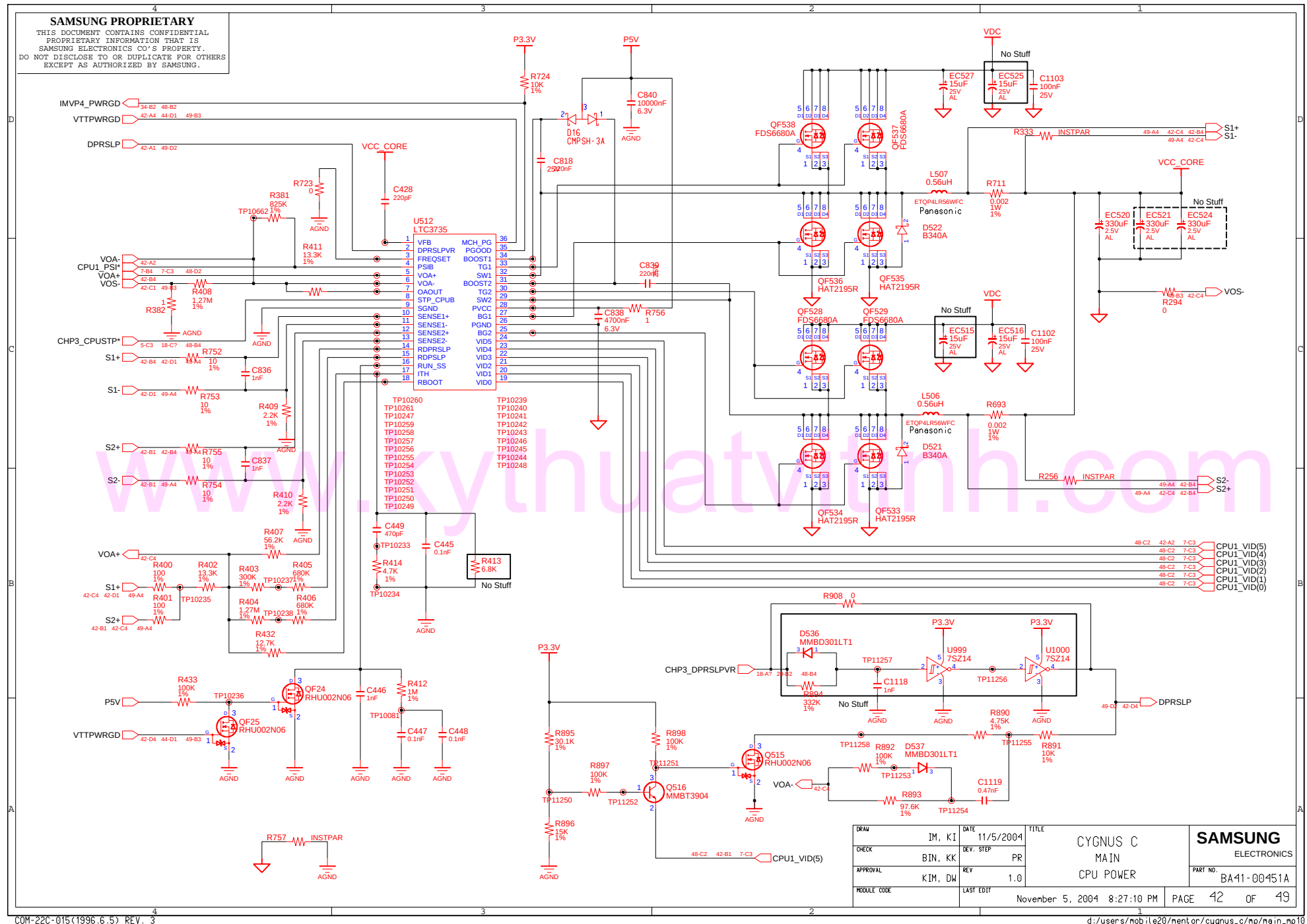
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CHECK	BIN, KK	DEV. STEP	PR	MAIN		ELECTRONICS
APPROVAL	KIM, DW	REV	1.0	MICOM & SWITCHED POWER	PART NO.	BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	40	OF 49

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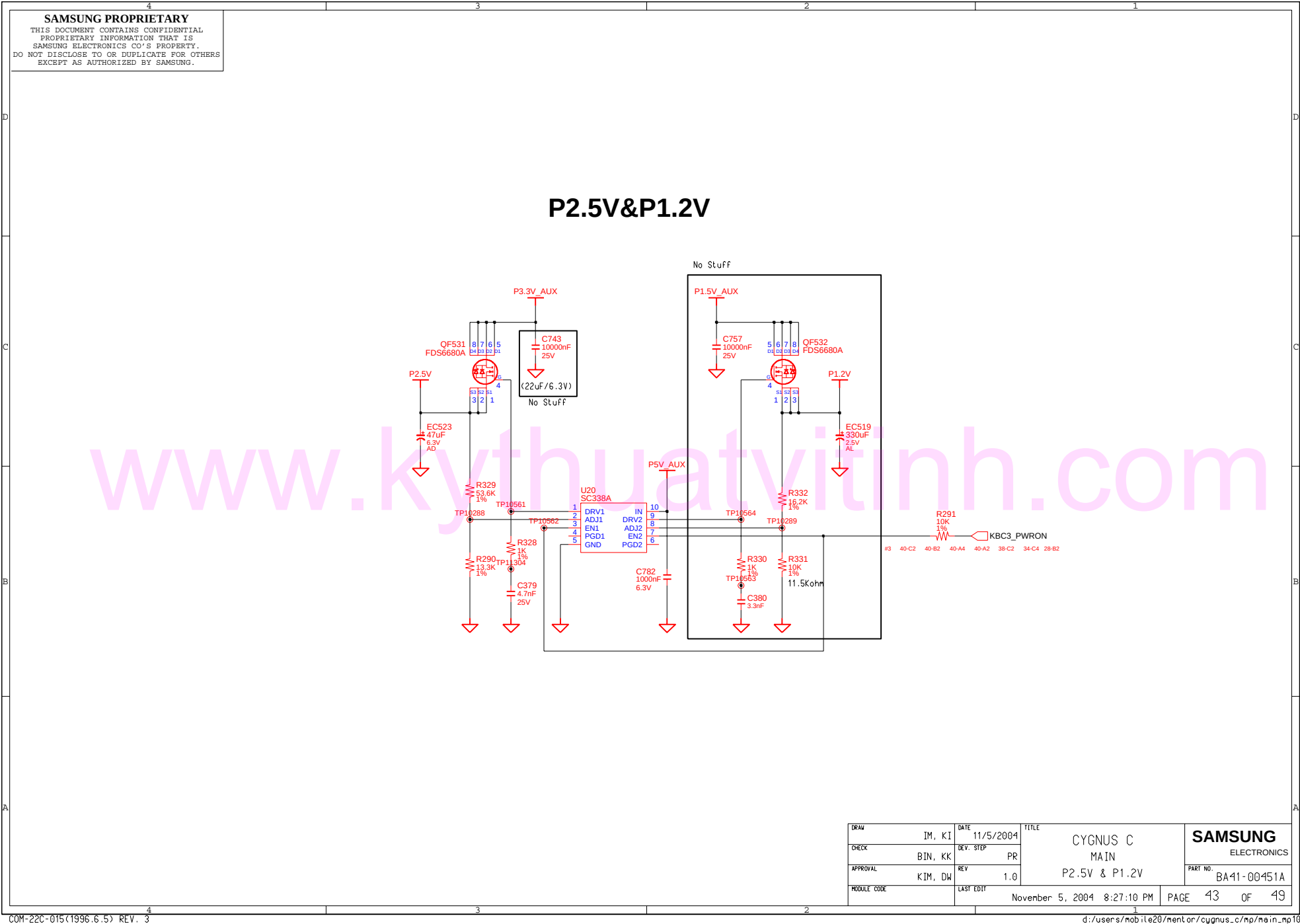


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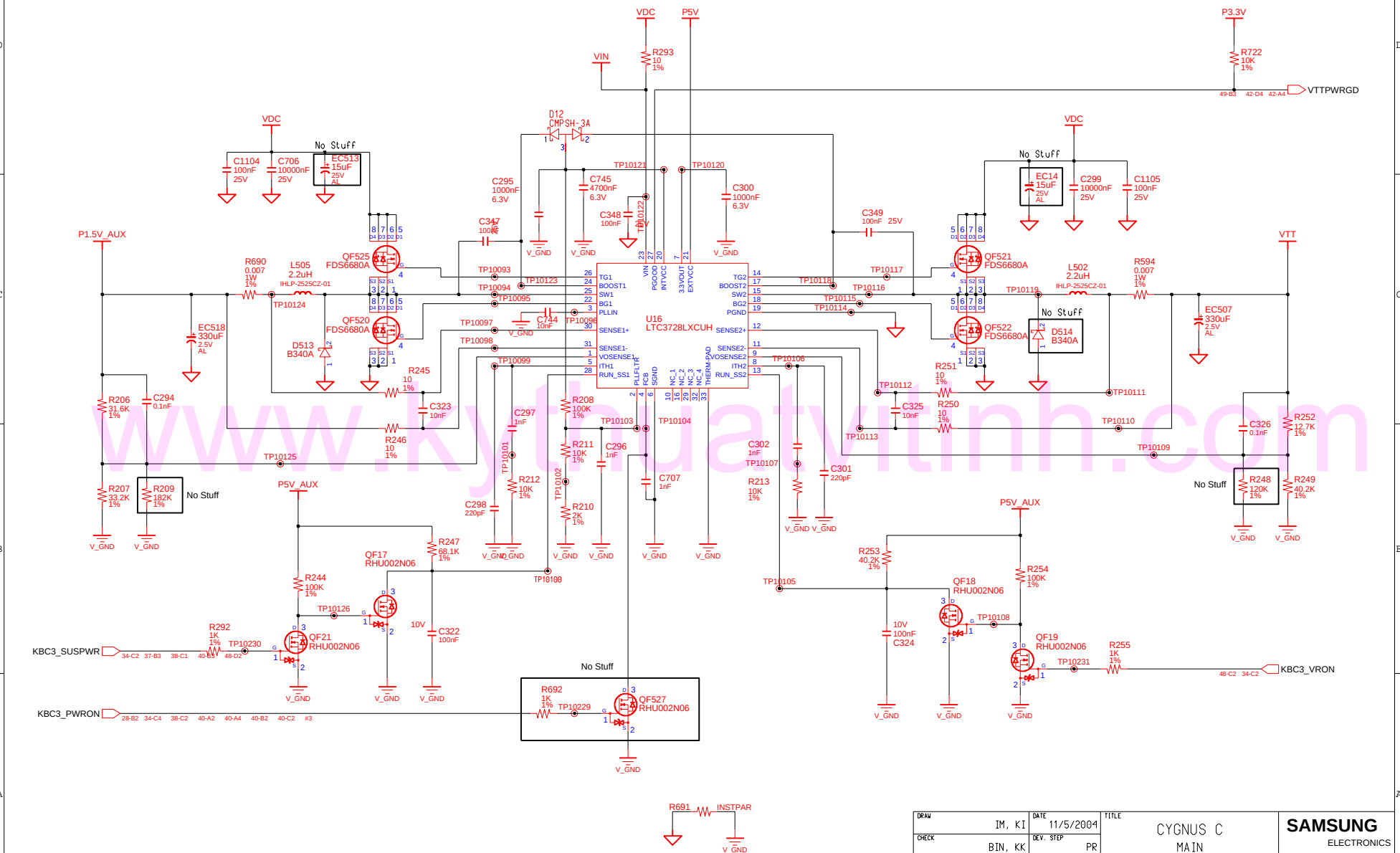
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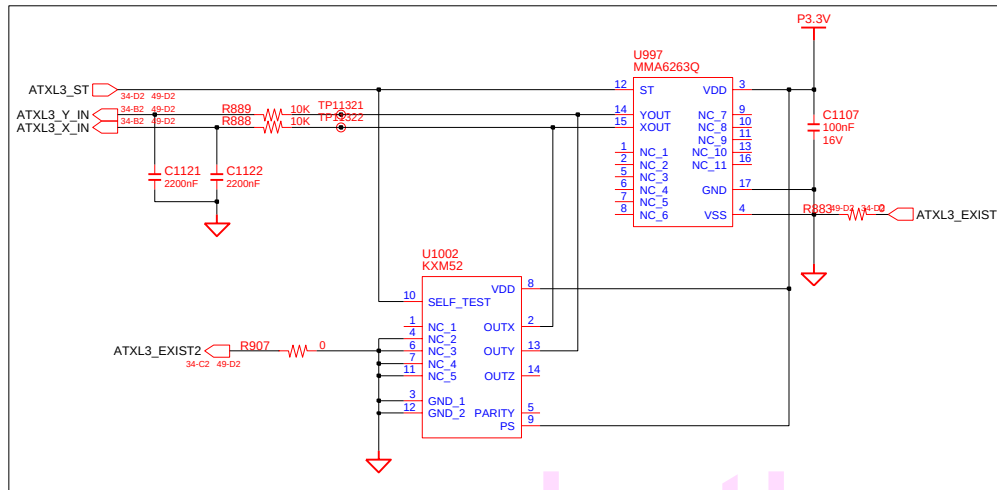
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CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	42	OF 49



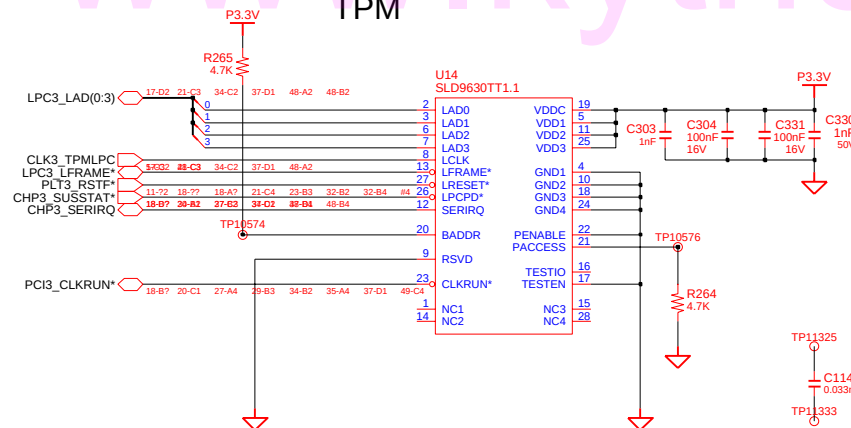
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AIRBAG

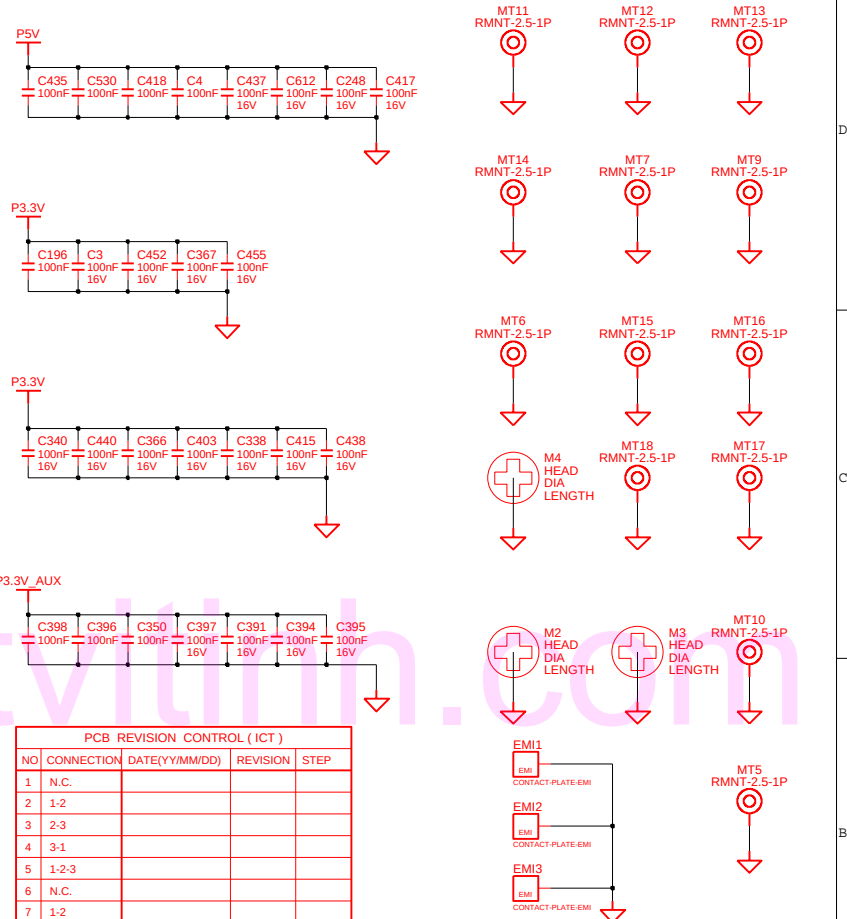
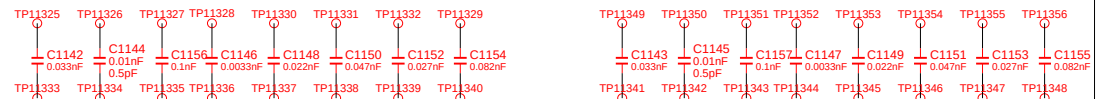


TPM



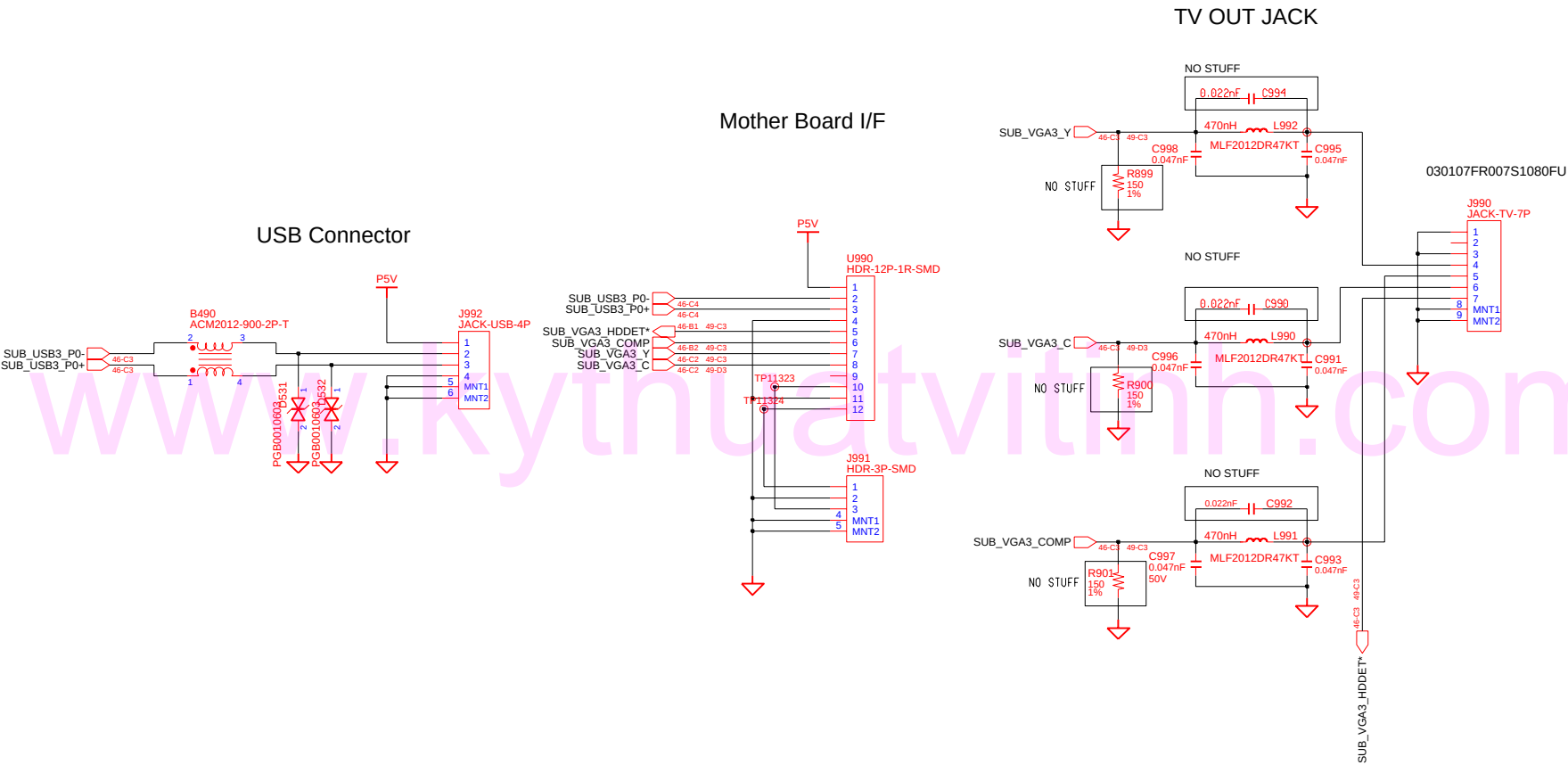
REV1
1
2 0 3

PCB REVISION CONTROL (ICT)					
NO	CONNECTION	DATE(Y/MM/DD)	REVISION	STEP	
1	N.C.				
2	1-2				
3	2-3				
4	3-1				
5	1-2-3				
6	N.C.				
7	1-2				
8	2-3				
9	3-1				
10	1-2-3				



DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAINBD AIRBAG & TPM	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	45	OF 49

< USB BOARD >



DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN MOUNT HOLE	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00451A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	46	OF 49

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
	AD21	3	
MiniPCI SLOT1	AD23	2	D,E
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
		-	A,B
Internal MAC	AD24(internal)	-	E
AC Link		-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	1	1	1	1	1	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	1	1	0	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V
Highest Freq.	0	1	0	1	1	1.356 V	1	1	0	1	1	0	0.844 V
	0	1	0	1	1	1.340 V	1	1	0	1	1	1	0.828 V
	0	1	1	0	0	1.324 V	1	1	1	0	0	0	0.812 V
	0	1	1	0	1	1.308 V	1	1	1	0	0	1	0.796 V
	0	1	1	0	1	1.292 V	1	1	1	0	1	0	0.780 V
	0	1	1	0	1	1.276 V	1	1	1	0	1	1	0.764 V
	0	1	1	1	0	1.260 V	1	1	1	1	0	0	0.748 V
	0	1	1	1	0	1.244 V	1	1	1	1	0	1	0.732 V
	0	1	1	1	1	1.228 V	1	1	1	1	1	0	0.716 V
	0	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V

IC / SMB Address

Devices	Address	Hex	Bus
ICH6	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	BLUETOOTH
4	FINGER PRINT
	OPTION
	OPTION

System Power States

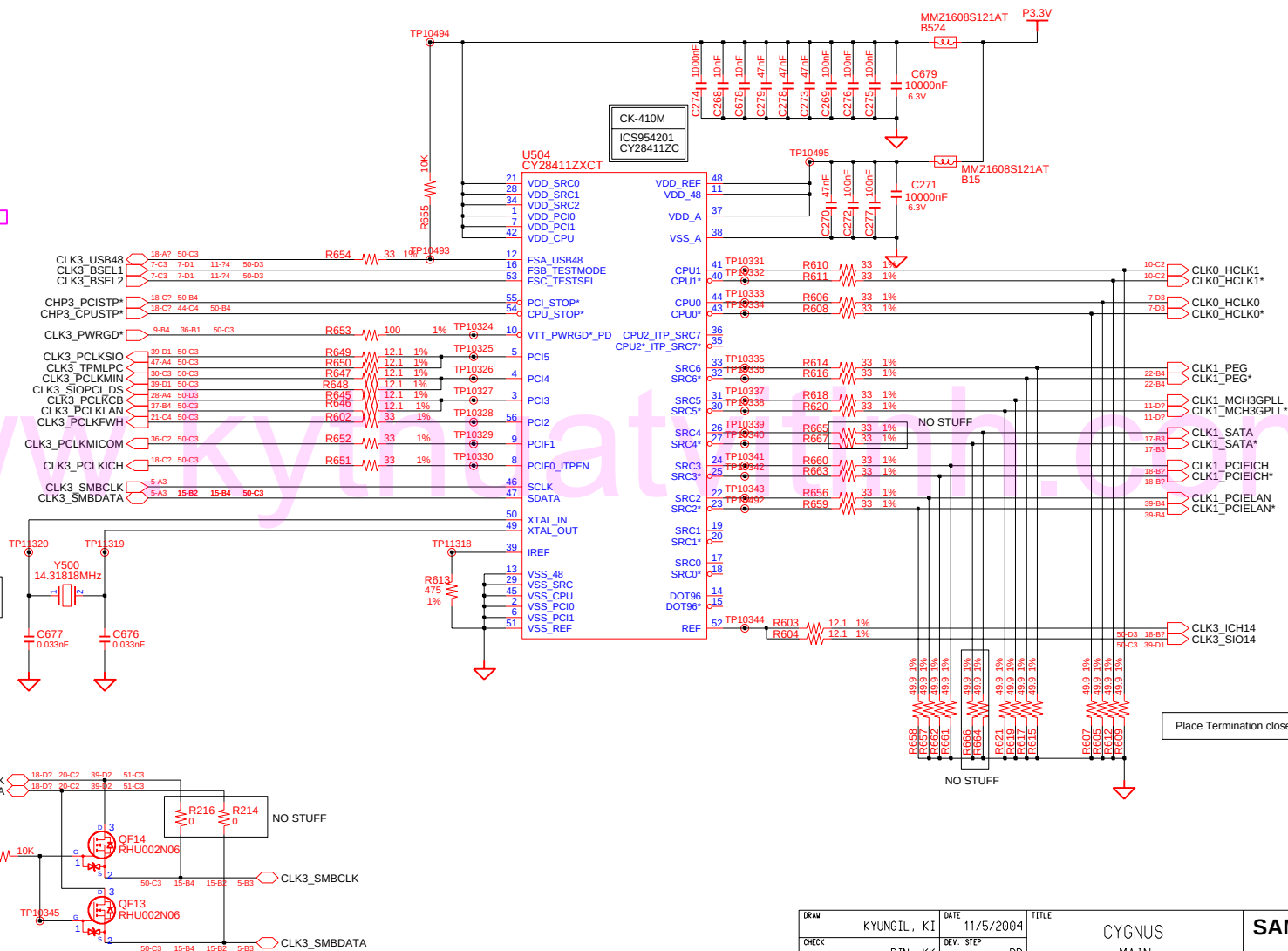
CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.
CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.
CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

REVISION HISTORY

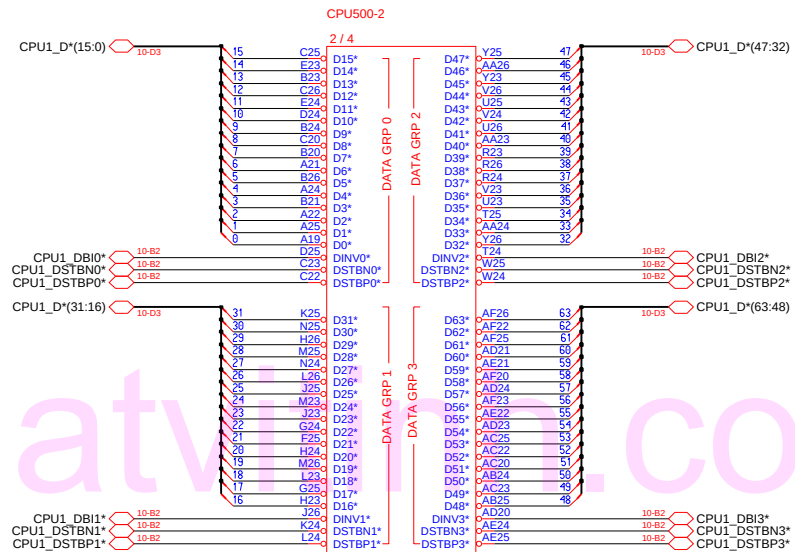
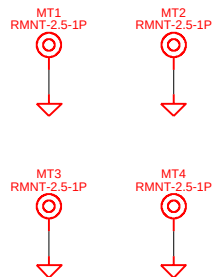
See rev notes in the changes file for more information.

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APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	4	OF 51

FSA BSEL2	FSB BSEL1	FSC BSEL0	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

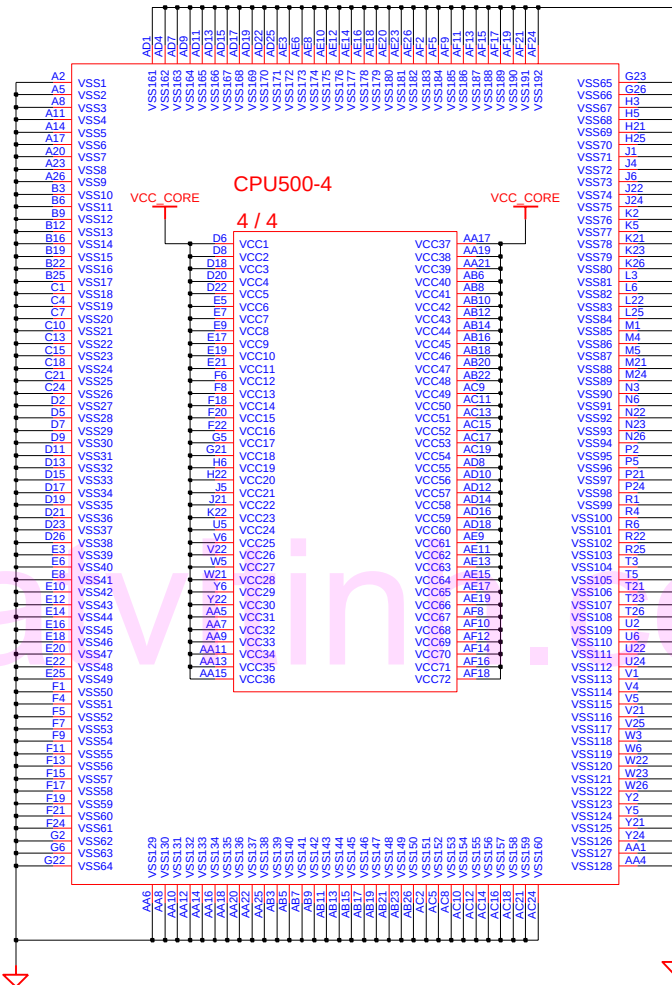
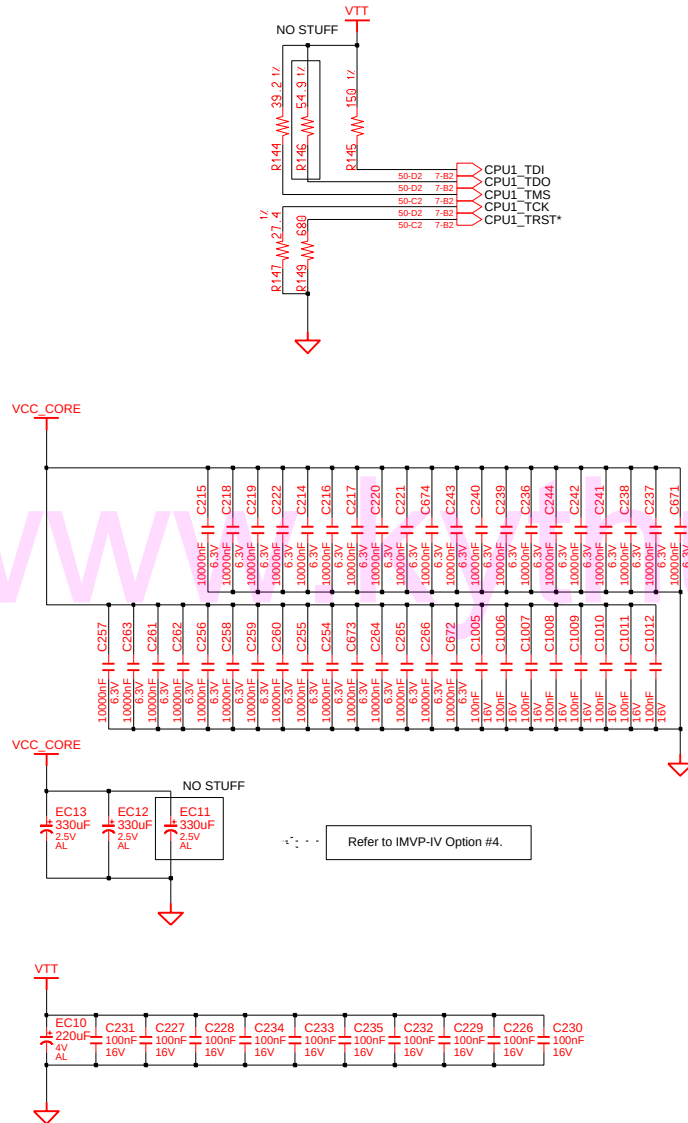


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DRAW	DATE	TITLE		SAMSUNG ELECTRONICS
KYUNGIL, K1	11/5/2004	CYGNUS MAIN		
CHECK	DEV. STEP	PR		
BIN, KK				
APPROVAL	REV	DOTHAN CPU (1/3)		PART NO.
KIM, DW	1.0			BA41-00450A
MODULE CODE	LAST EDIT	November 5, 2004 8:10:03 PM		PAGE 6 OF 51

Refer to Sonoma Platform Design Guide(4.6.1.4)



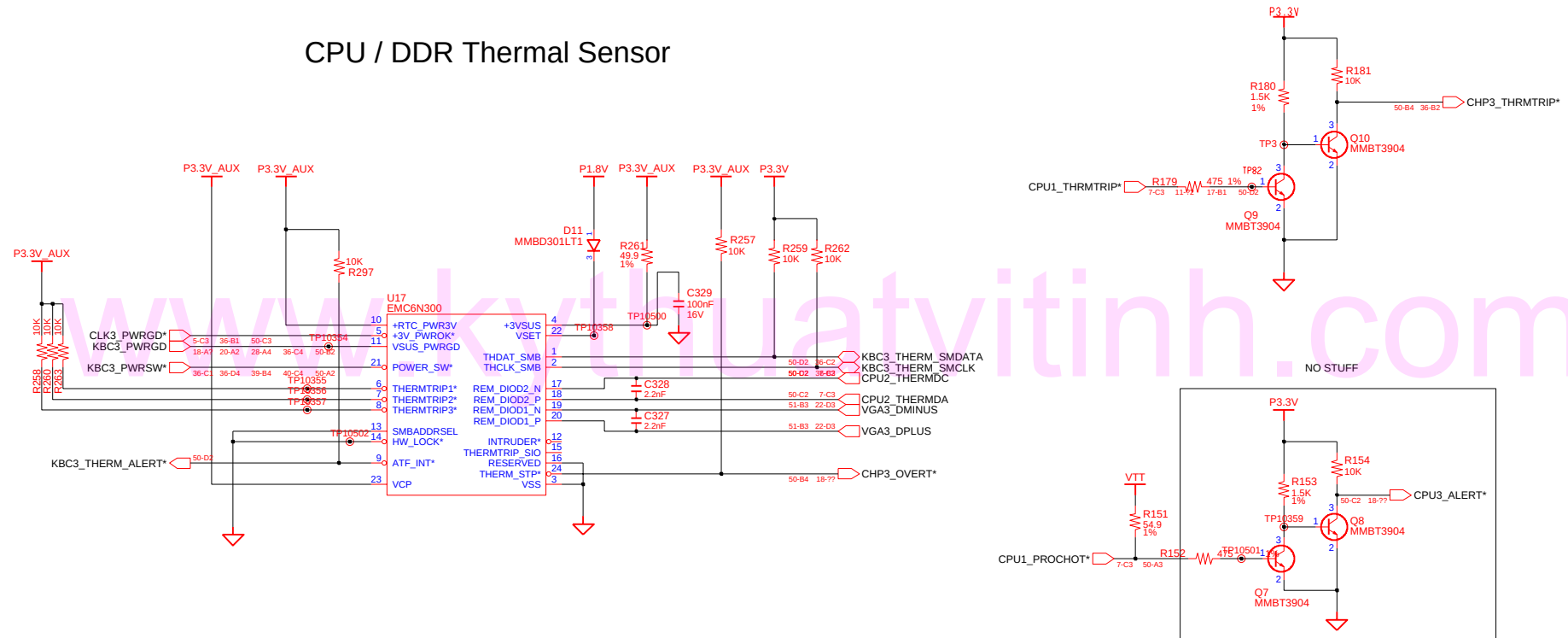
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CHECK	BIN, KK	DEV. STEP	PR	MAIN	
APPROVAL	KIM, DW	REV	1.0	DOTHAN CPU(3/3)	
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	8 OF 51

SAMSUNG	PART NO.
ELECTRONICS	BA41-00450A

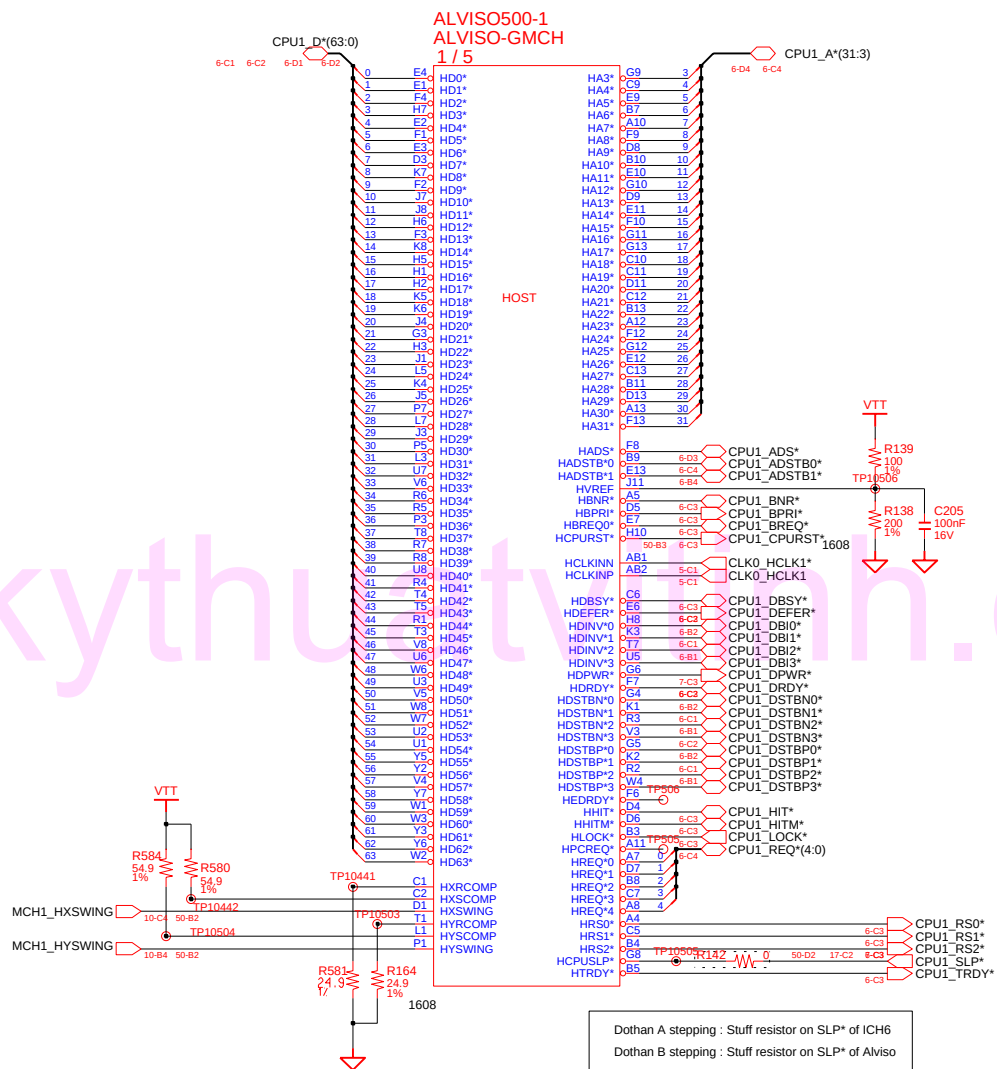
Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

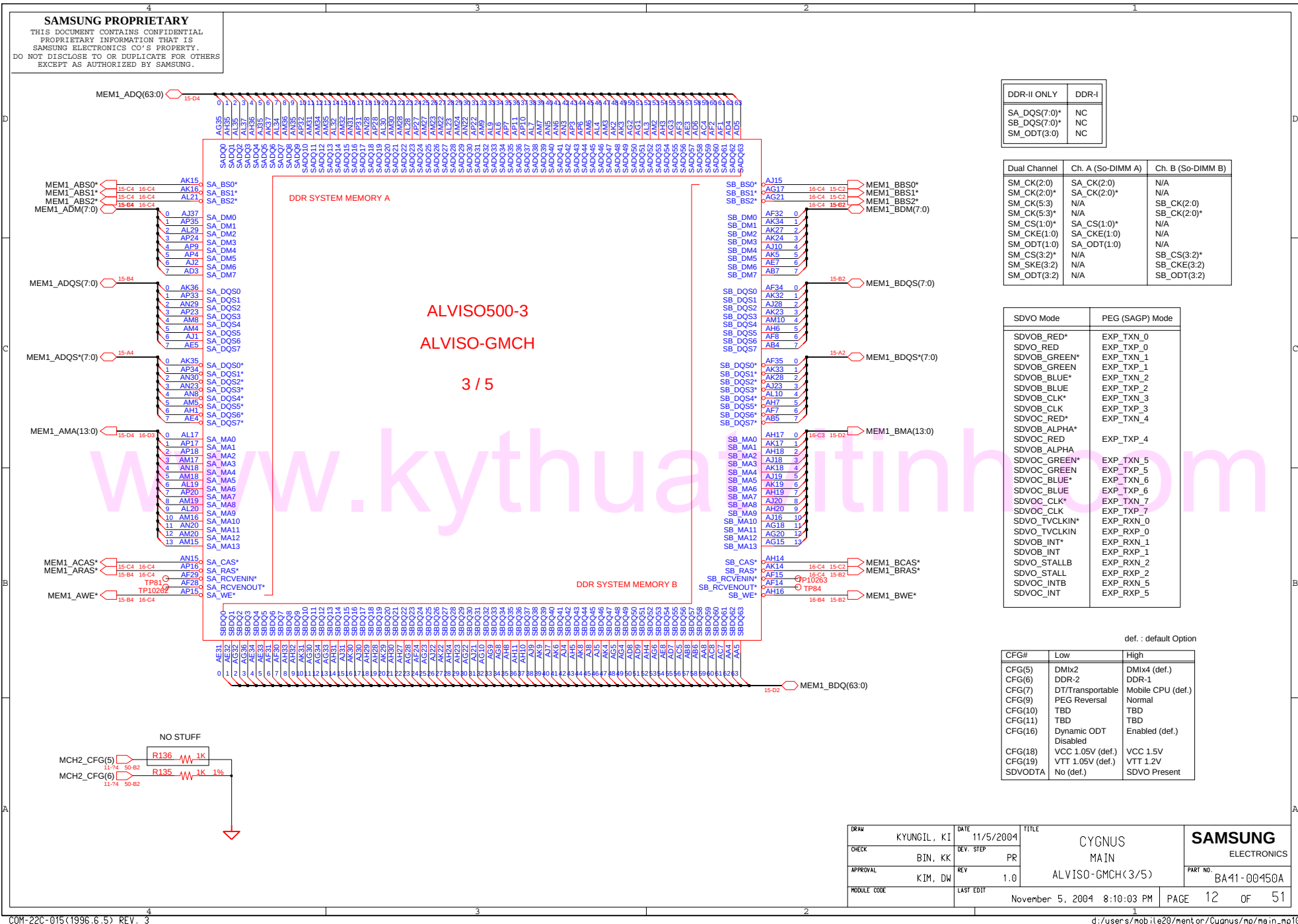
CPU / DDR Thermal Sensor



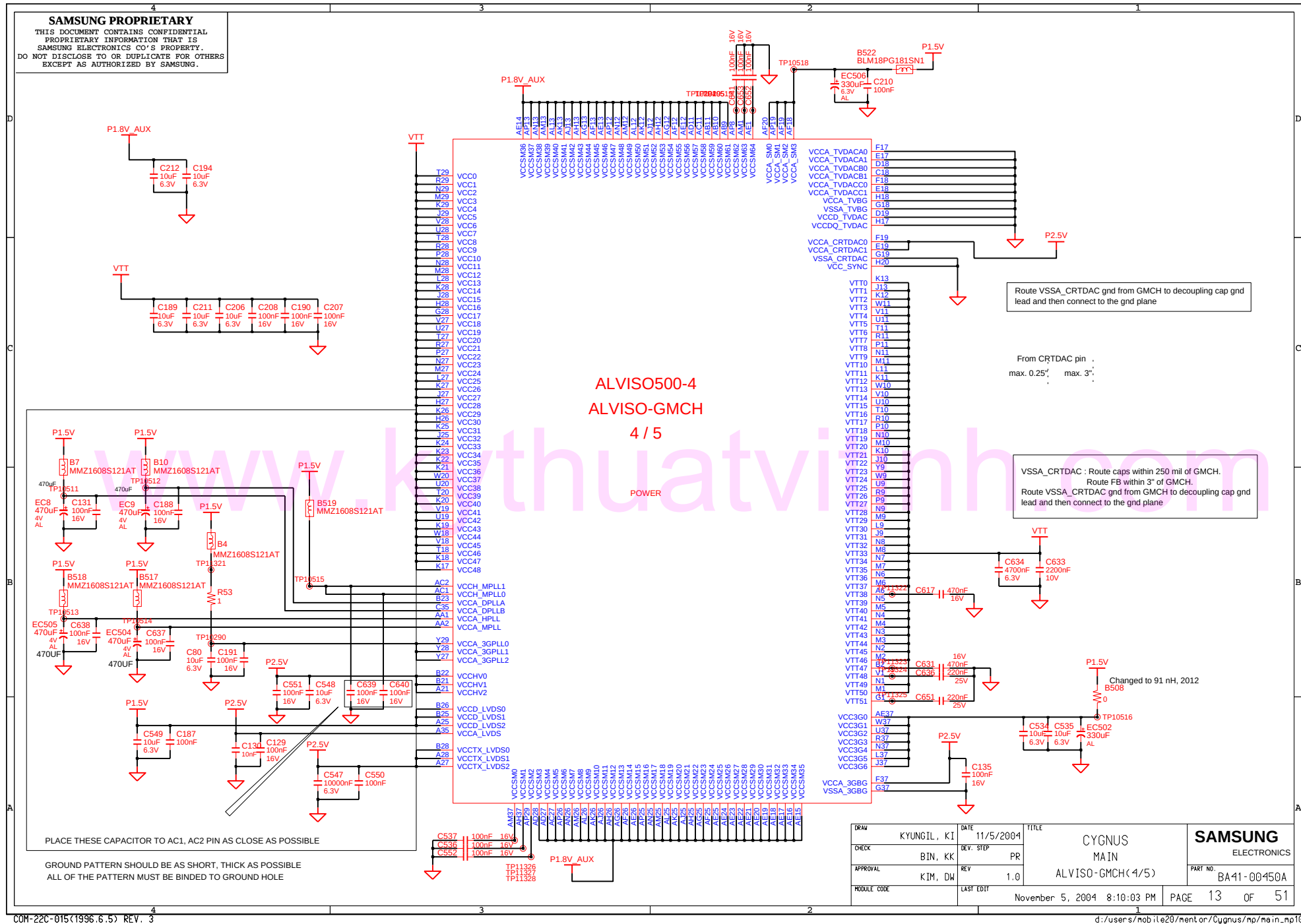
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CHECK	BIN, KK	REV. STEP	PR			PART NO. BA41-00450A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	9 OF 51	



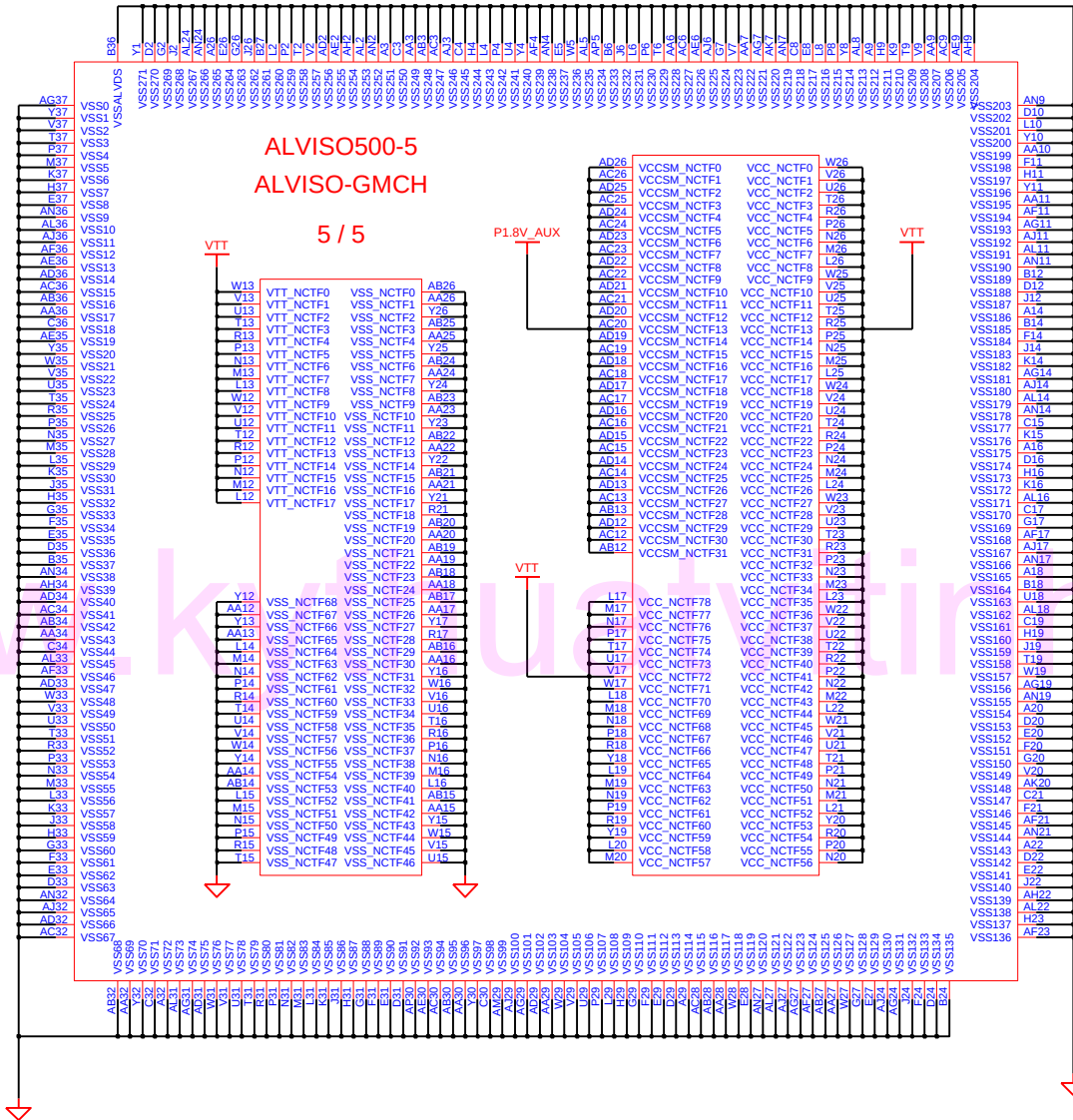
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CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE	LAST EDIT		November 5, 2004 8:10:03 PM		PAGE	10 OF 51



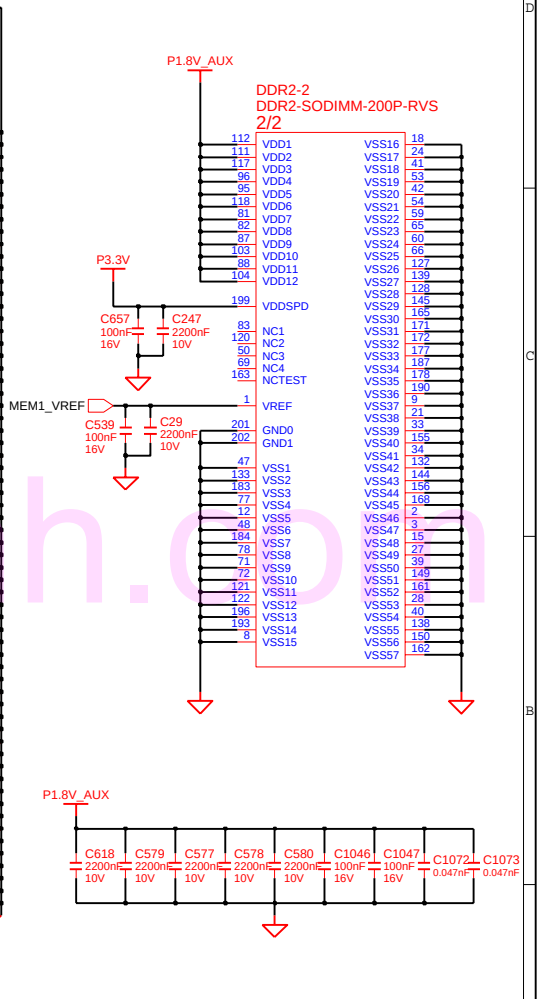
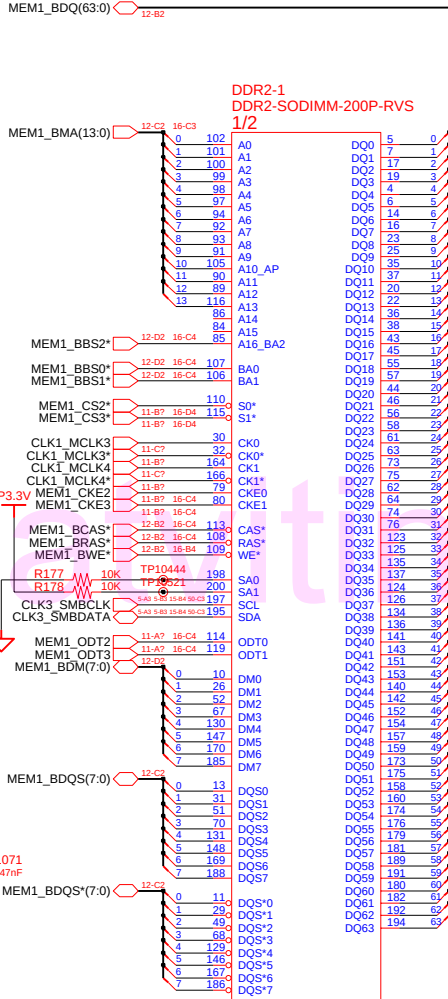
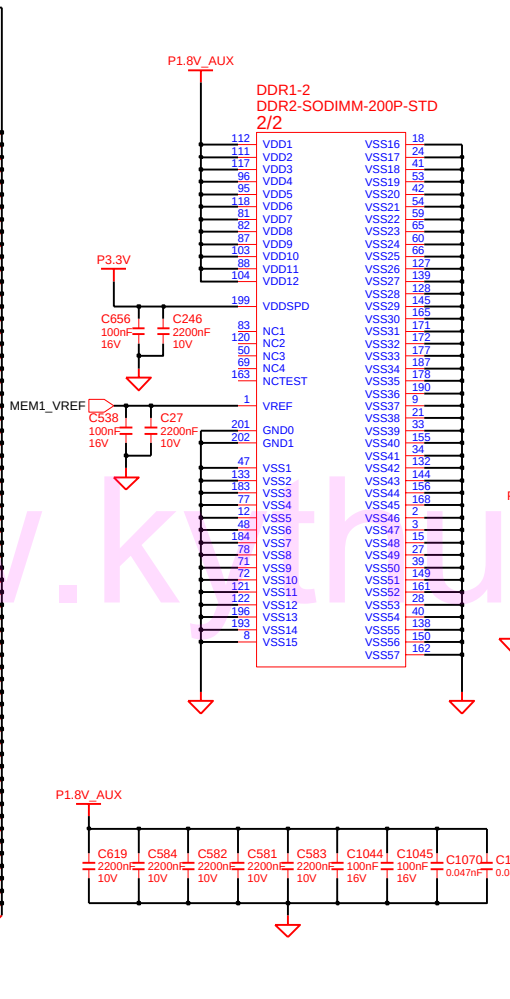
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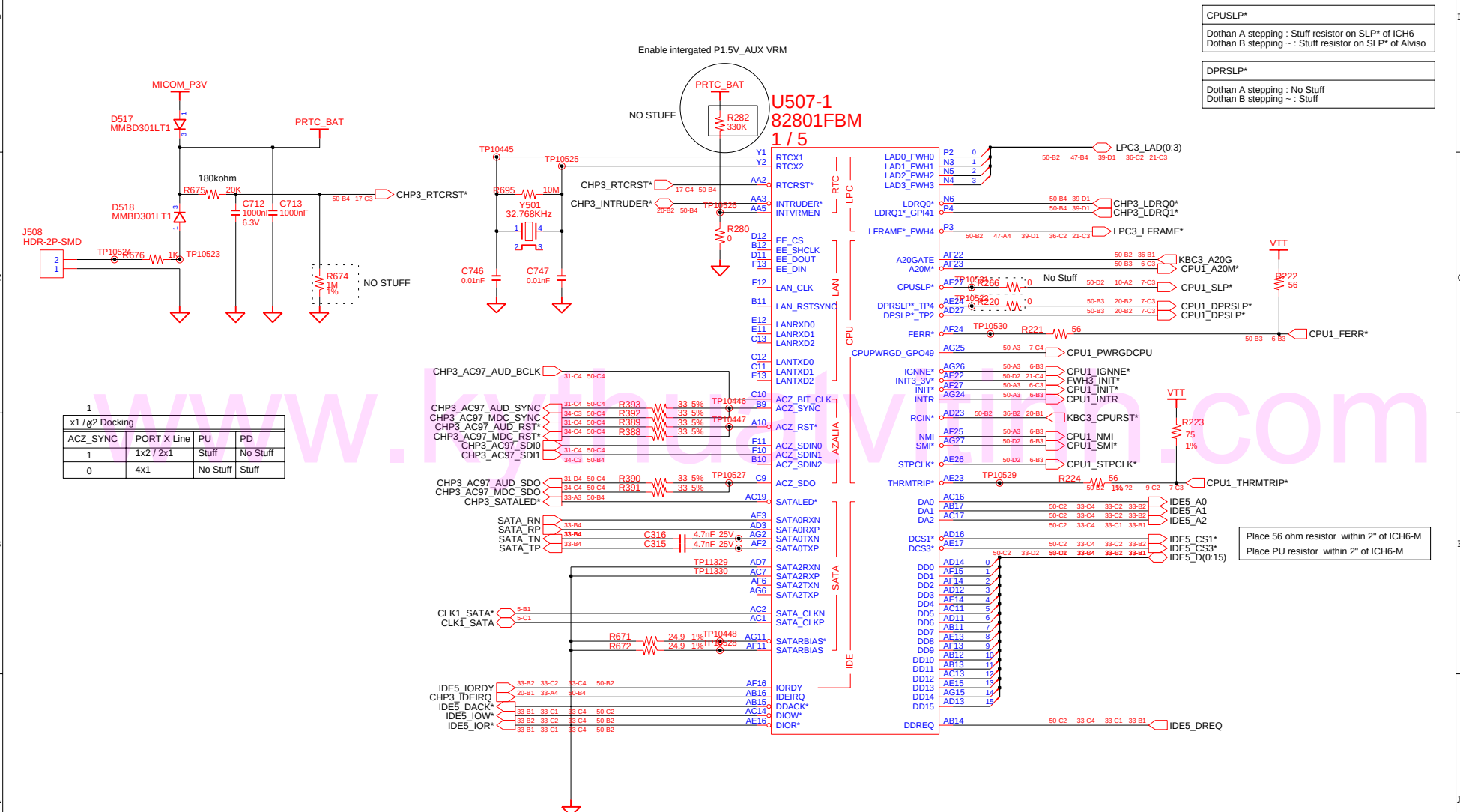
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CHECK	BIN, KK	REV. STEP	PR			PART NO. BA41-00450A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	14	OF 51



COM-22C-015(1996.6.5) REV. 3

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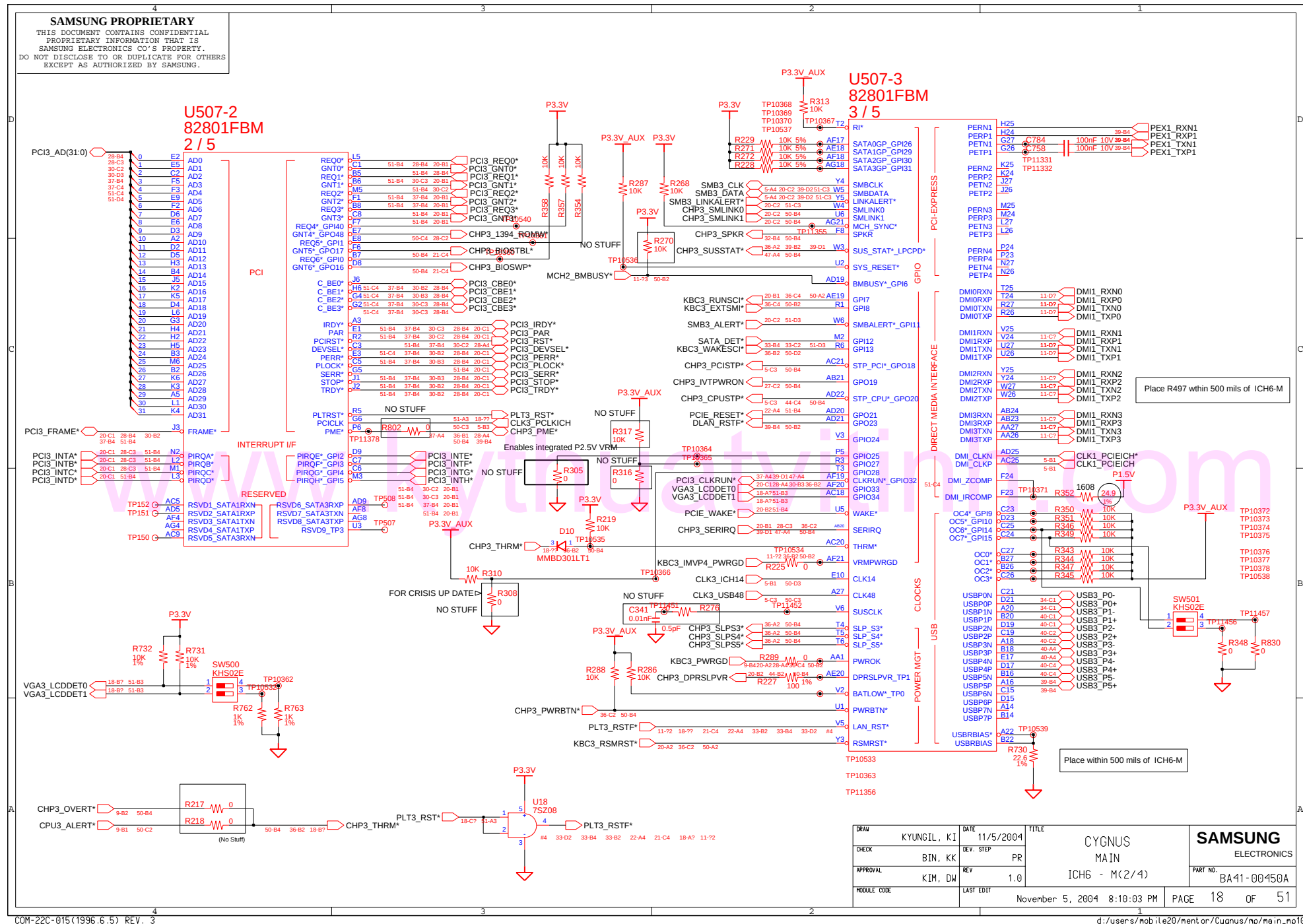
CPUSLP*
Dothan A stepping : Stuff resistor on SLP* of ICH6 Dothan B stepping ~ : Stuff resistor on SLP* of Alviso
DPRSLP*
Dothan A stepping : No Stuff Dothan B stepping ~ : Stuff

x1 / g2 Docking			
ACZ_SYNC	PORT X Line	PU	PD
1	1x2 / 2x1	Stuff	No Stuff
0	4x1	No Stuff	Stuff

Place 56 ohm resistor within 2" of ICH6-M
Place PU resistor within 2" of ICH6-M

DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0		ICH6 - M(1/4)	PART NO. BA41-00450A
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	17	OF 51

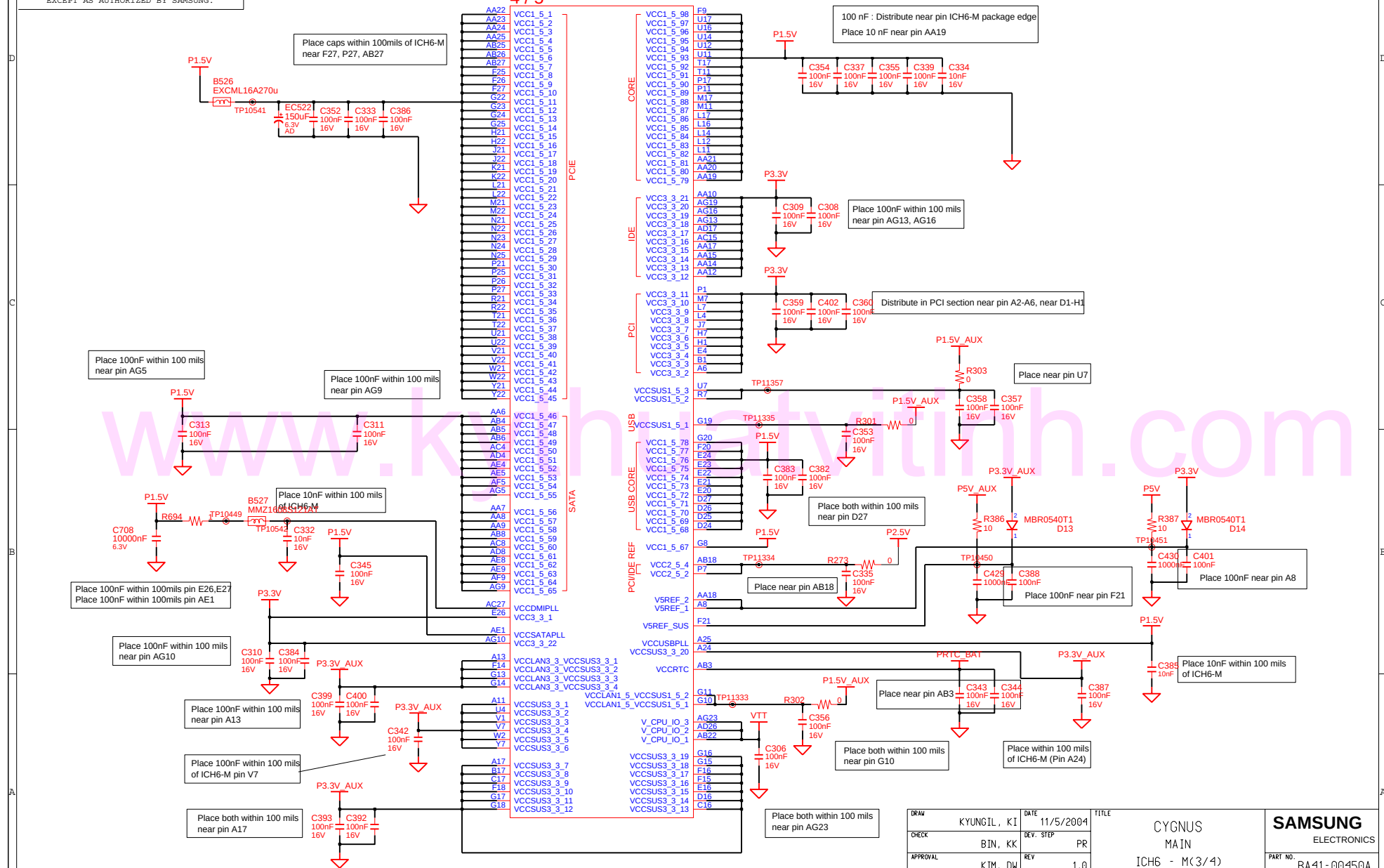
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DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN ICH6 - M(2/4)	SAMSUNG ELECTRONICS PART NO. BA14-00450A
CHECK	BIN, KK	REV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM			
			PAGE 18 OF 51			

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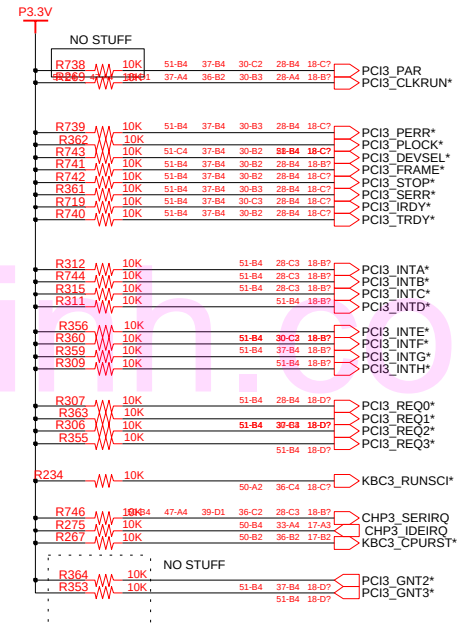
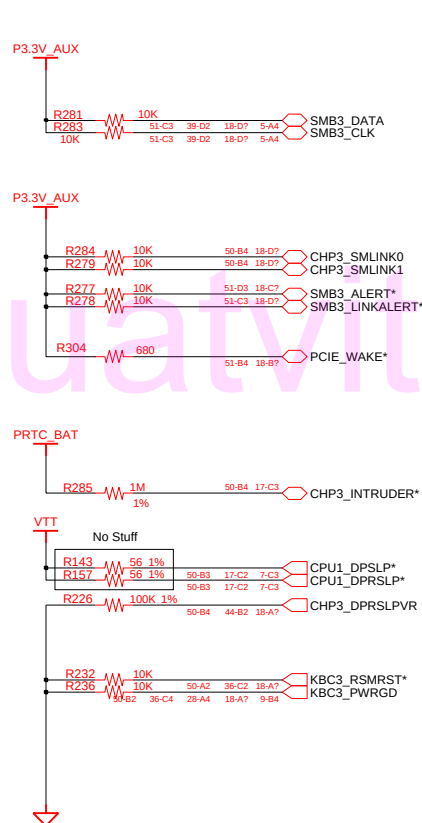
U507-4
82801FBM
4 / 5



DRWN	KYUNGIL, K	DATE	11/5/2004	TITLE		CYGNUS MAIN		SAMSUNG ELECTRONICS	
CHECK	BIN, KK	REV. STEP	PR	ICH6 - M(3/4)		PART NO.		BA41-00450A	
APPROVAL	KIM, DW	REV	1.0						
MODULE CODE	LAST EDIT		November 5, 2004 8:10:03 PM			PAGE	19	OF	51

U507-5
82801FBM
5 / 5

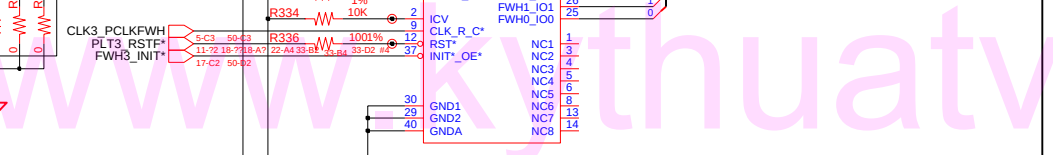
AG22	VSS_172	VSS_86	P22
AG20	VSS_171	VSS_85	P16
AG17	VSS_170	VSS_84	P15
AG14	VSS_169	VSS_83	P14
AG12	VSS_168	VSS_82	P13
AG7	VSS_167	VSS_81	P12
AG3	VSS_166	VSS_80	N17
AG1	VSS_165	VSS_79	N16
AF26	VSS_164	VSS_78	N15
AF12	VSS_163	VSS_77	N14
AF10	VSS_162	VSS_76	N13
AF7	VSS_161	VSS_75	N12
AF3	VSS_160	VSS_74	N11
AF1	VSS_159	VSS_73	N7
AE25	VSS_158	VSS_72	N1
AE21	VSS_157	VSS_71	M27
AE12	VSS_156	VSS_70	M26
AE10	VSS_155	VSS_69	M23
AE7	VSS_154	VSS_68	M15
AE6	VSS_153	VSS_67	M14
AE2	VSS_152	VSS_66	M13
AD24	VSS_151	VSS_65	M12
AD18	VSS_150	VSS_64	M4
AD15	VSS_149	VSS_63	L25
AD10	VSS_148	VSS_62	L24
AD6	VSS_147	VSS_61	L23
AD2	VSS_146	VSS_60	L15
AD1	VSS_145	VSS_59	L13
AC23	VSS_144	VSS_58	K23
AC26	VSS_143	VSS_57	K27
AC24	VSS_142	VSS_56	K26
AC22	VSS_141	VSS_55	K7
AC12	VSS_140	VSS_54	K1
AC10	VSS_139	VSS_53	K25
AC6	VSS_138	VSS_52	J25
AC3	VSS_137	VSS_51	J23
AB9	VSS_136	VSS_50	J4
AB19	VSS_135	VSS_49	H27
AB10	VSS_134	VSS_48	H26
AB7	VSS_133	VSS_47	H23
AB2	VSS_132	VSS_46	G21
AA13	VSS_131	VSS_45	G12
AA16	VSS_130	VSS_44	G9
AA11	VSS_129	VSS_43	G7
AA4	VSS_128	VSS_42	G1
Y26	VSS_127	VSS_41	F22
Y27	VSS_126	VSS_40	F19
Y26	VSS_125	VSS_39	F4
Y23	VSS_124	VSS_38	E27
Y6	VSS_123	VSS_37	E27
W25	VSS_122	VSS_36	E25
W24	VSS_121	VSS_35	E13
W23	VSS_120	VSS_34	E12
W7	VSS_119	VSS_33	E15
W1	VSS_118	VSS_32	E14
V27	VSS_117	VSS_31	D22
V26	VSS_116	VSS_30	D20
V23	VSS_115	VSS_29	D19
V4	VSS_114	VSS_28	D14
U25	VSS_113	VSS_27	D13
U24	VSS_112	VSS_26	D10
U23	VSS_111	VSS_25	D7
U15	VSS_110	VSS_24	D1
U13	VSS_109	VSS_23	C22
T27	VSS_108	VSS_22	C20
T26	VSS_107	VSS_21	C12
T23	VSS_106	VSS_20	C14
T16	VSS_105	VSS_19	C4
T15	VSS_104	VSS_18	B25
T14	VSS_103	VSS_17	B24
T13	VSS_102	VSS_16	B23
T12	VSS_101	VSS_15	B21
T7	VSS_100	VSS_14	B19
T1	VSS_99	VSS_13	B18
R25	VSS_98	VSS_12	B15
R24	VSS_97	VSS_11	B13
R23	VSS_96	VSS_10	A26
R17	VSS_95	VSS_9	A23
R16	VSS_94	VSS_8	A21
R15	VSS_93	VSS_7	A19
R14	VSS_92	VSS_6	A15
R13	VSS_91	VSS_5	A12
R12	VSS_90	VSS_4	A9
R11	VSS_89	VSS_3	A7
R4	VSS_88	VSS_2	A4
	VSS_87	VSS_1	A1



ICH6-m Strapping Options

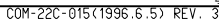
	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
EEP_DOUT		TBD

DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS	SAMSUNG
CHECK	BIN, KK	DEV. STEP	PR		MAIN	ELECTRONICS
APPROVAL	KIM, DW	REV	1.0		ICH6 - M(4/4)	PART NO. BA41-00450A
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM		PAGE 20	OF 51



d:/users/mobile20/mentor/Cognus/mo/main mo10

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DRAW	KYUNGIL, KI	DATE	11/5/2004	CYGNUS MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		
APPROVAL	KIM, DW	REV	1.0		
MODULE CODE		LAST EDIT			
				ATI M24 GRAPHIC CONTROL 1/4	PART NO. BA41-00450A
				November 5, 2004 8:10:03 PM	PAGE 22 OF 51

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**GFX500-2
M24-CSP64
2 / 5**

**GFX500-3
M24-CSP64
3 / 5**

Pin list for GFX500-2 (left):

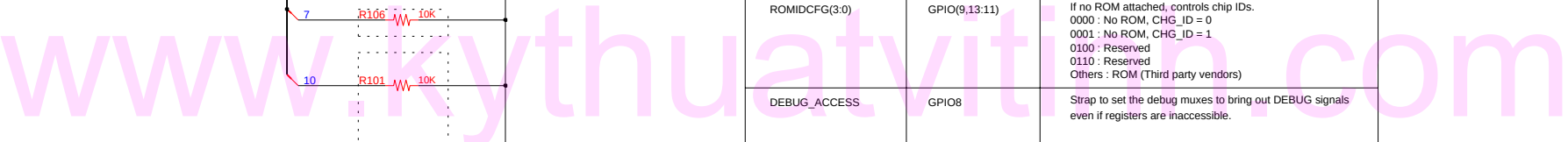
H28	VSS_93	VSS_157	E22
H29	VSS_94	VSS_158	B22
J28	VSS_95	VSS_159	B23
J29	VSS_96	VSS_160	B24
J26	VSS_97	VSS_161	C23
H25	VSS_98	VSS_162	C22
G28	VSS_99	VSS_163	F21
G30	VSS_100	VSS_164	F22
D29	VSS_101	VSS_165	C21
D28	VSS_102	VSS_166	A24
E28	VSS_103	VSS_167	C24
E29	VSS_104	VSS_168	A25
G29	VSS_105	VSS_169	E21
G28	VSS_106	VSS_170	B20
F28	VSS_107	VSS_171	C19
G25	VSS_108	VSS_172	J25
F26	VSS_109	VSS_173	F29
E26	VSS_110	VSS_174	E25
F25	VSS_111	VSS_175	A27
E24	VSS_112	VSS_176	F15
F23	VSS_113	VSS_177	C15
E23	VSS_114	VSS_178	C11
D22	VSS_115	VSS_179	E11
B29	VSS_116	VSS_180	J27
C29	VSS_117	VSS_181	F30
C25	VSS_118	VSS_182	F24
C27	VSS_119	VSS_183	B27
B28	VSS_120	VSS_184	E16
B25	VSS_121	VSS_185	B16
C26	VSS_122	VSS_186	B11
B26	VSS_123	VSS_187	F10
F17	VSS_124	VSS_188	A19
E17	VSS_125	VSS_189	E18
D16	VSS_126	VSS_190	E19
F16	VSS_127	VSS_191	E20
E15	VSS_128	VSS_192	F20
F14	VSS_129	VSS_193	B19
E14	VSS_130	VSS_194	B21
F13	VSS_131	VSS_195	C20
C17	VSS_132	VSS_196	C18
B18	VSS_133	VSS_197	A18
B17	VSS_134	VSS_198	B7
B15	VSS_135	VSS_199	B8
C13	VSS_136	VSS_200	D30
B14	VSS_137	VSS_201	B13
C14	VSS_138	VSS_202	
C16	VSS_139	VSS_203	
A13	VSS_140	VSS_204	
A12	VSS_141	VSS_205	
C12	VSS_142	VSS_206	
B12	VSS_143	VSS_207	
C10	VSS_144	VSS_208	
C9	VSS_145	VSS_209	
B9	VSS_146	VSS_210	
B10	VSS_147	VSS_211	
E13	VSS_148	VSS_212	
E12	VSS_149	VSS_213	
E11	VSS_150	VSS_214	
F9	VSS_151	VSS_215	
F8	VSS_152	VSS_216	
	VSS_153	VSS_217	
	VSS_154	VSS_218	
	VSS_155	VSS_219	
	VSS_156	VSS_220	

Pin list for GFX500-3 (right):

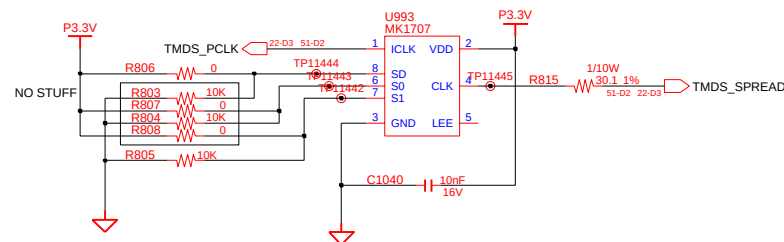
D7	VSS_200	VSS_264	N5
E7	VSS_201	VSS_265	M1
G6	VSS_202	VSS_266	M3
F5	VSS_203	VSS_267	L2
E5	VSS_204	VSS_268	M2
C4	VSS_205	VSS_269	M5
B5	VSS_206	VSS_270	P6
C5	VSS_207	VSS_271	N3
A4	VSS_208	VSS_272	K2
B4	VSS_209	VSS_273	K3
C2	VSS_210	VSS_274	J2
D1	VSS_211	VSS_275	P5
D2	VSS_212	VSS_276	P3
G4	VSS_213	VSS_277	P2
H5	VSS_214	VSS_278	E6
J6	VSS_215	VSS_279	B2
K5	VSS_216	VSS_280	J5
K4	VSS_217	VSS_281	G3
L5	VSS_218	VSS_282	W6
G2	VSS_219	VSS_283	W2
F3	VSS_220	VSS_284	AC6
E2	VSS_221	VSS_285	AD2
D1	VSS_222	VSS_286	F6
C2	VSS_223	VSS_287	B3
B2	VSS_224	VSS_288	K6
A2	VSS_225	VSS_289	G1
F2	VSS_226	VSS_290	V5
E2	VSS_227	VSS_291	W1
D2	VSS_228	VSS_292	AC5
C2	VSS_229	VSS_293	AD1
B2	VSS_230	VSS_294	R2
A2	VSS_231	VSS_295	T5
F2	VSS_232	VSS_296	T6
E2	VSS_233	VSS_297	R5
D2	VSS_234	VSS_298	R6
C2	VSS_235	VSS_299	R3
B2	VSS_236	VSS_300	N1
A2	VSS_237	VSS_301	N2
F2	VSS_238	VSS_302	T2
E2	VSS_239	VSS_303	T3
D2	VSS_240	VSS_304	E3
C2	VSS_241	VSS_305	AA3
B2	VSS_242	VSS_306	



d:/users/mobile20/mentor/Cygnus/mo/main.mo1

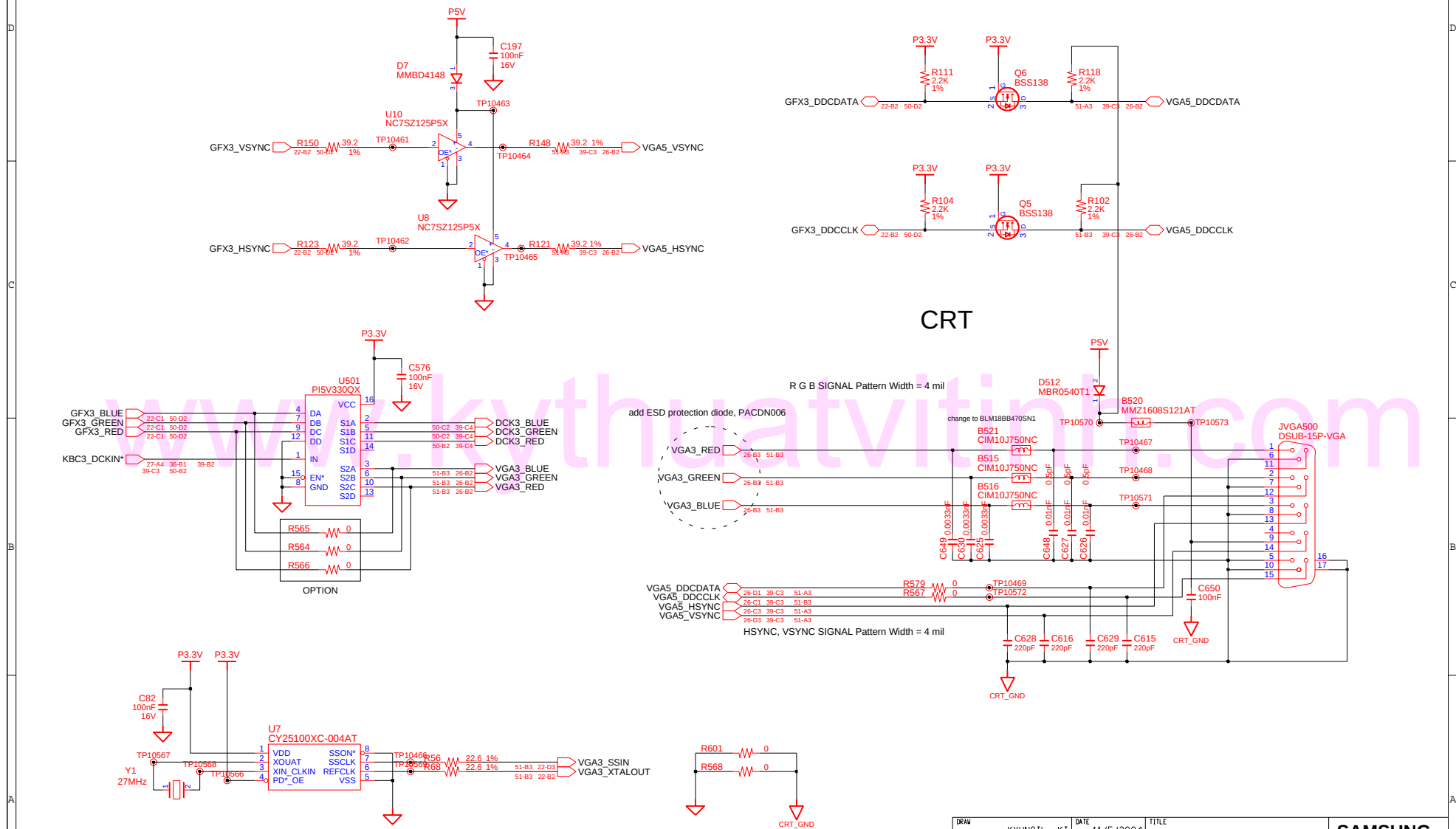


A



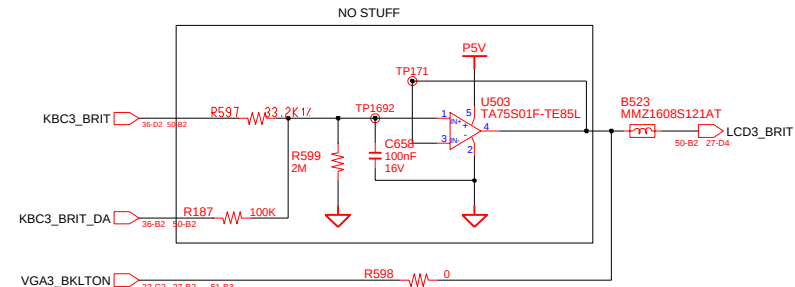
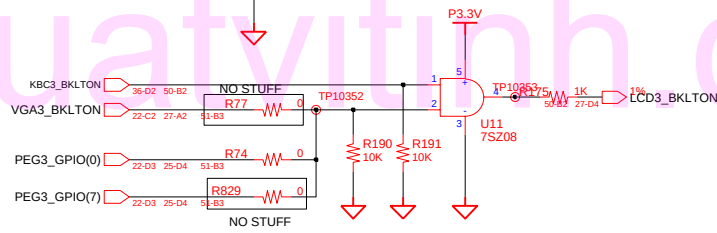
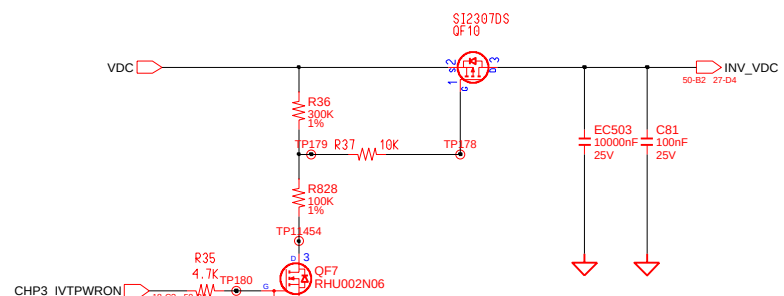
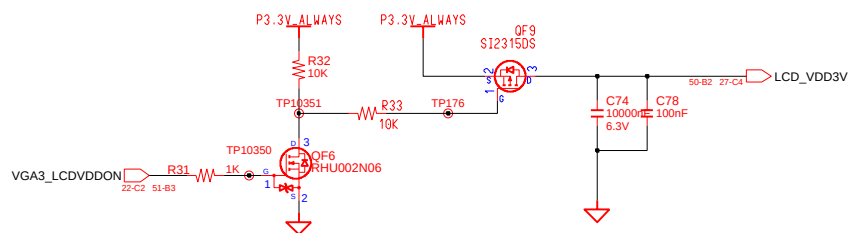
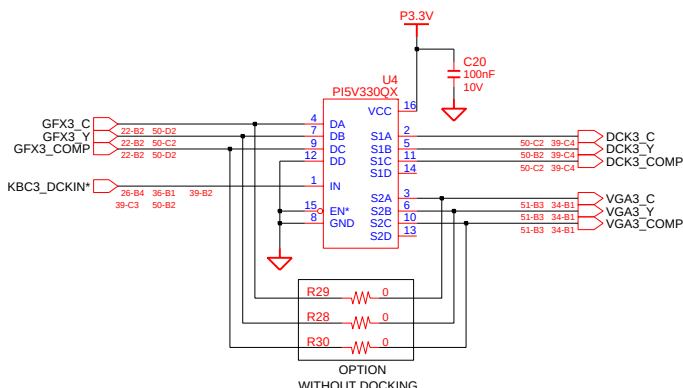
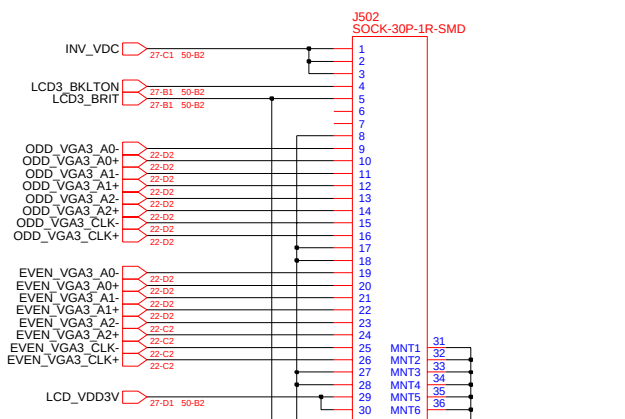
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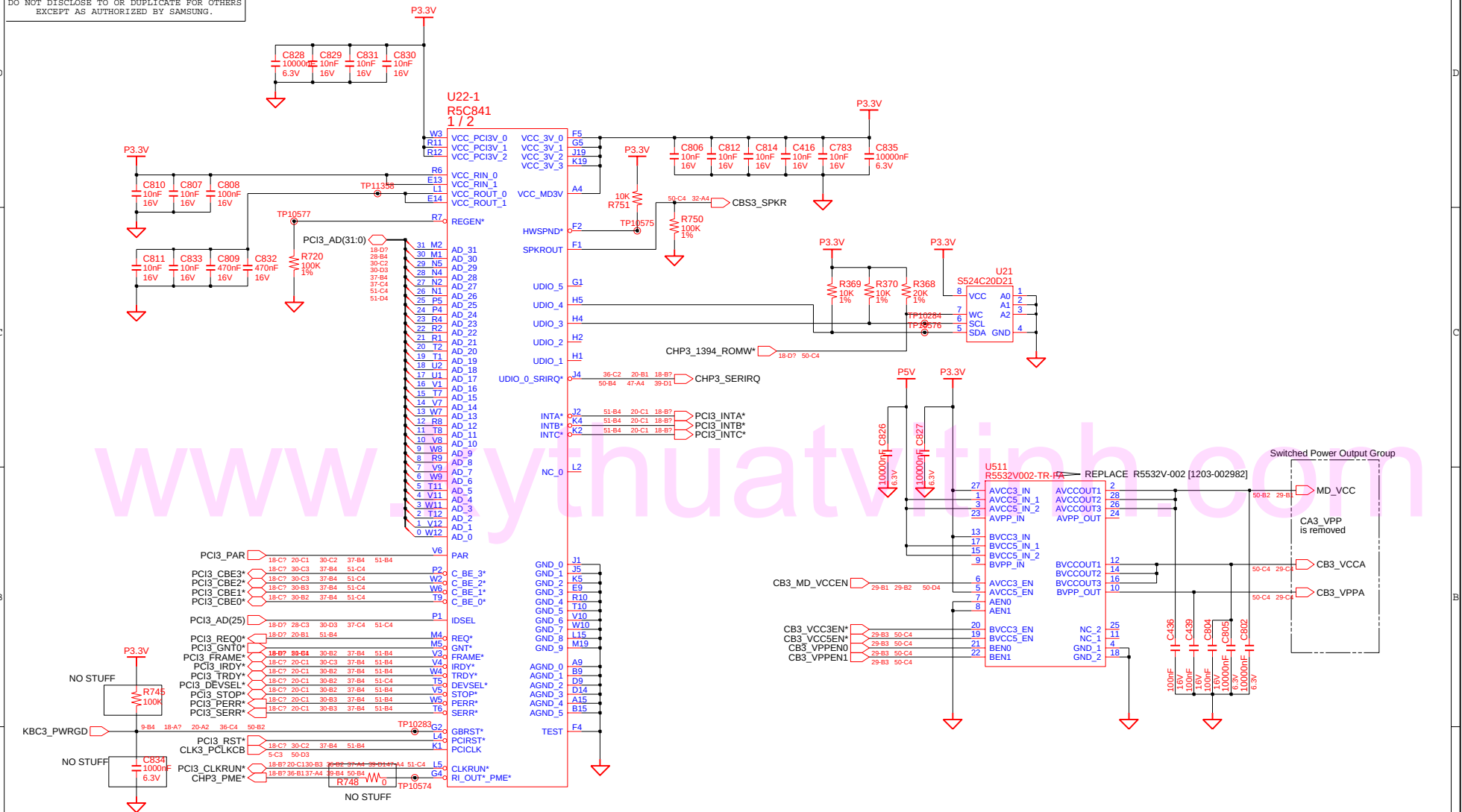
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LCD CONNECTOR



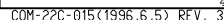
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CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00450A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	27 OF 51	

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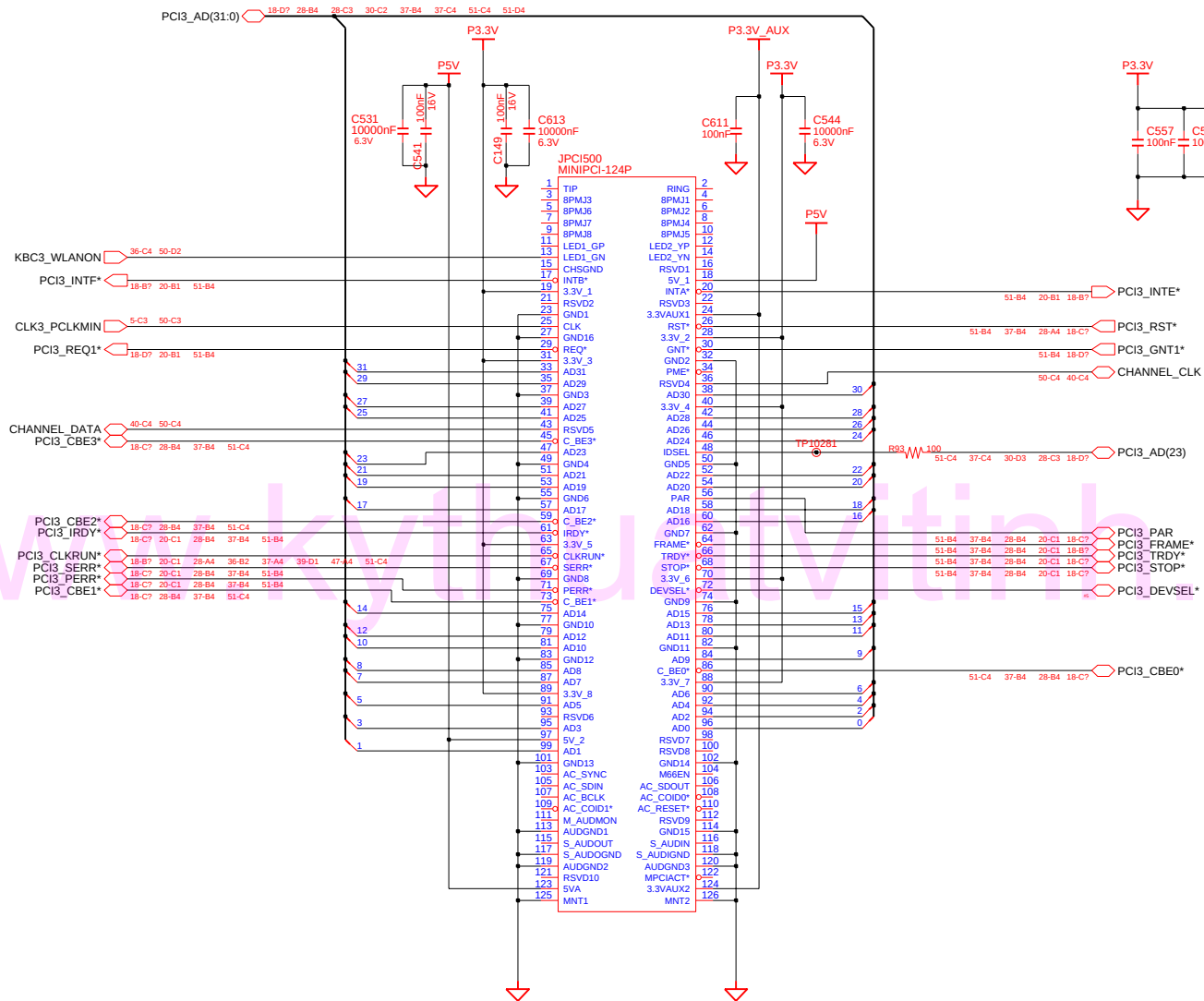
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CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00450A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	28	OF 51

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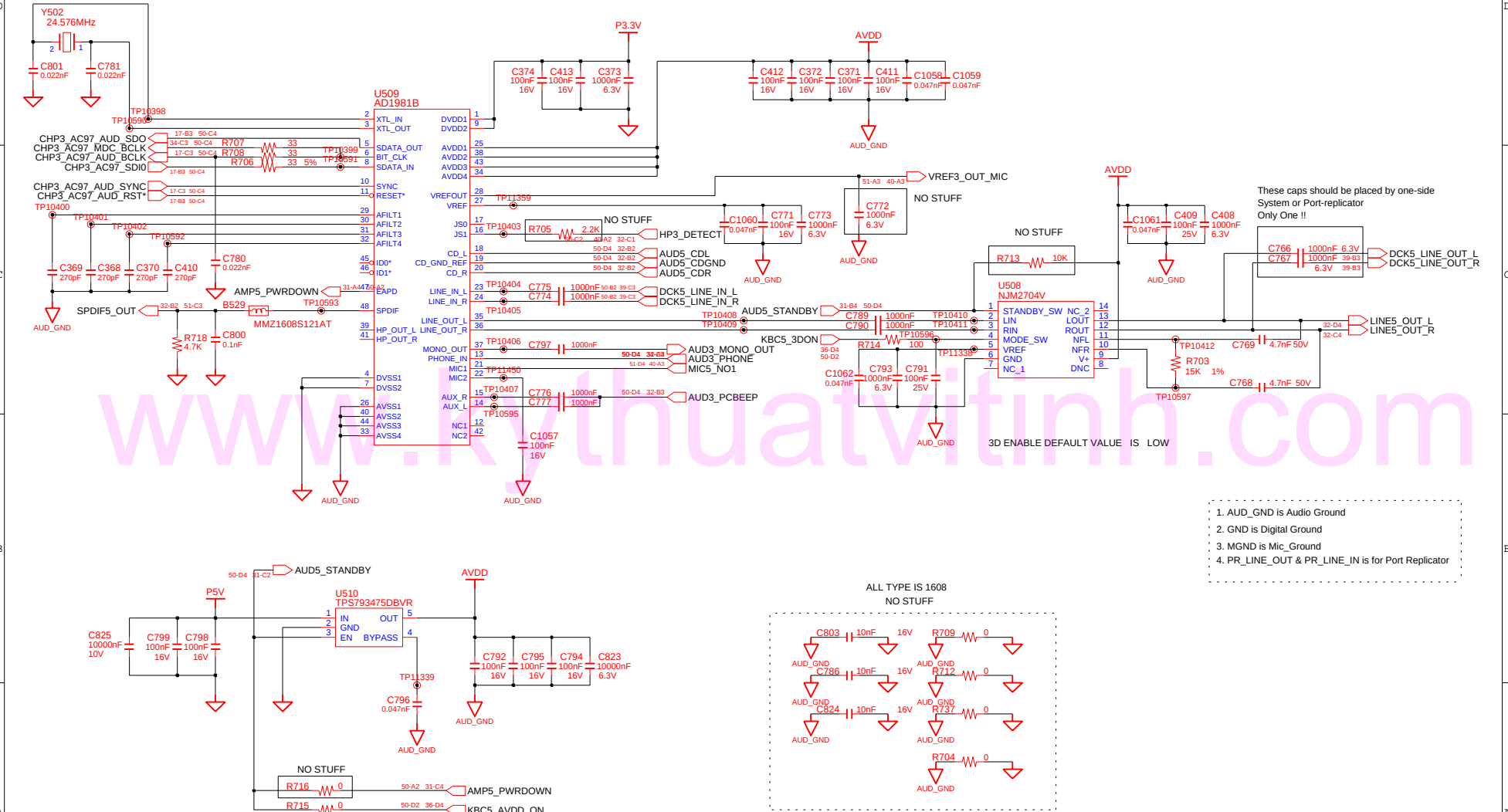
d:/users/mobile20/mentor/Cygnus/mo/main mo1

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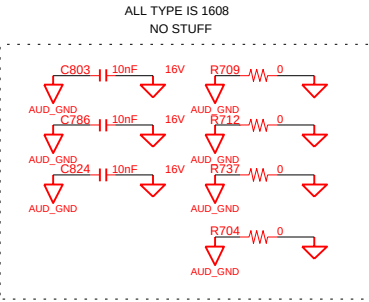


DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00450A
APPROVAL	KIM, DW	REV	1.0			PAGE 30 OF 51
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM			

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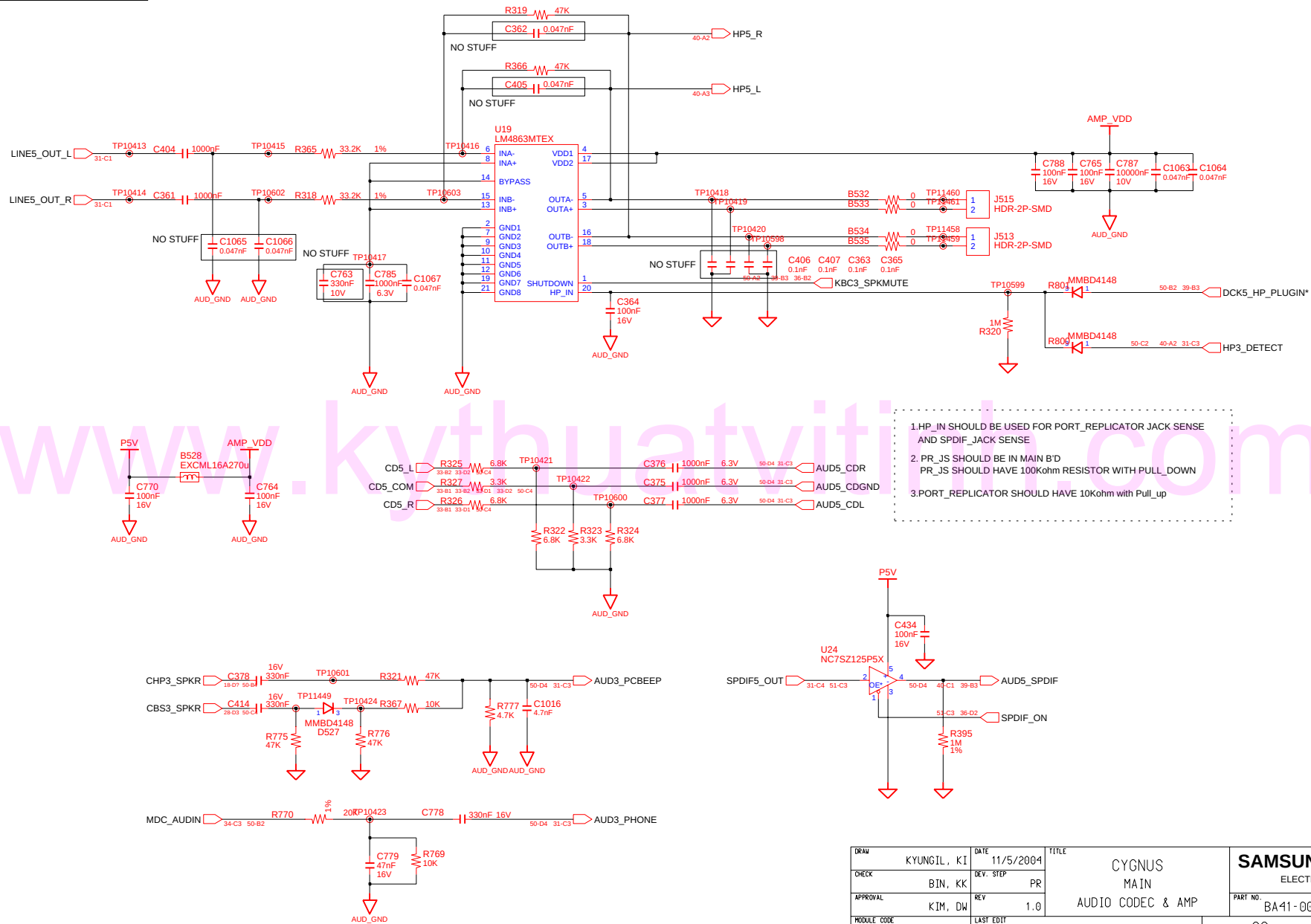


- 1. AUD_GND is Audio Ground
- 2. GND is Digital Ground
- 3. MGN is Mic_Ground
- 4. PR_LINE_OUT & PR_LINE_IN is for Port Replicator

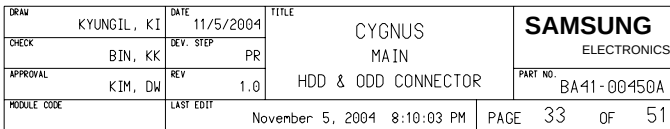


DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN AUDIO CODEC & AMP	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	REV	1.0	PART NO. BA41-00450A
APPROVAL	KIM, DW	LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	31	OF 51
MODULE CODE						

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DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN AUDIO CODEC & AMP	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00450A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	32	OF 51



33
HDR-30P-2R-SMD

1 2



P5V

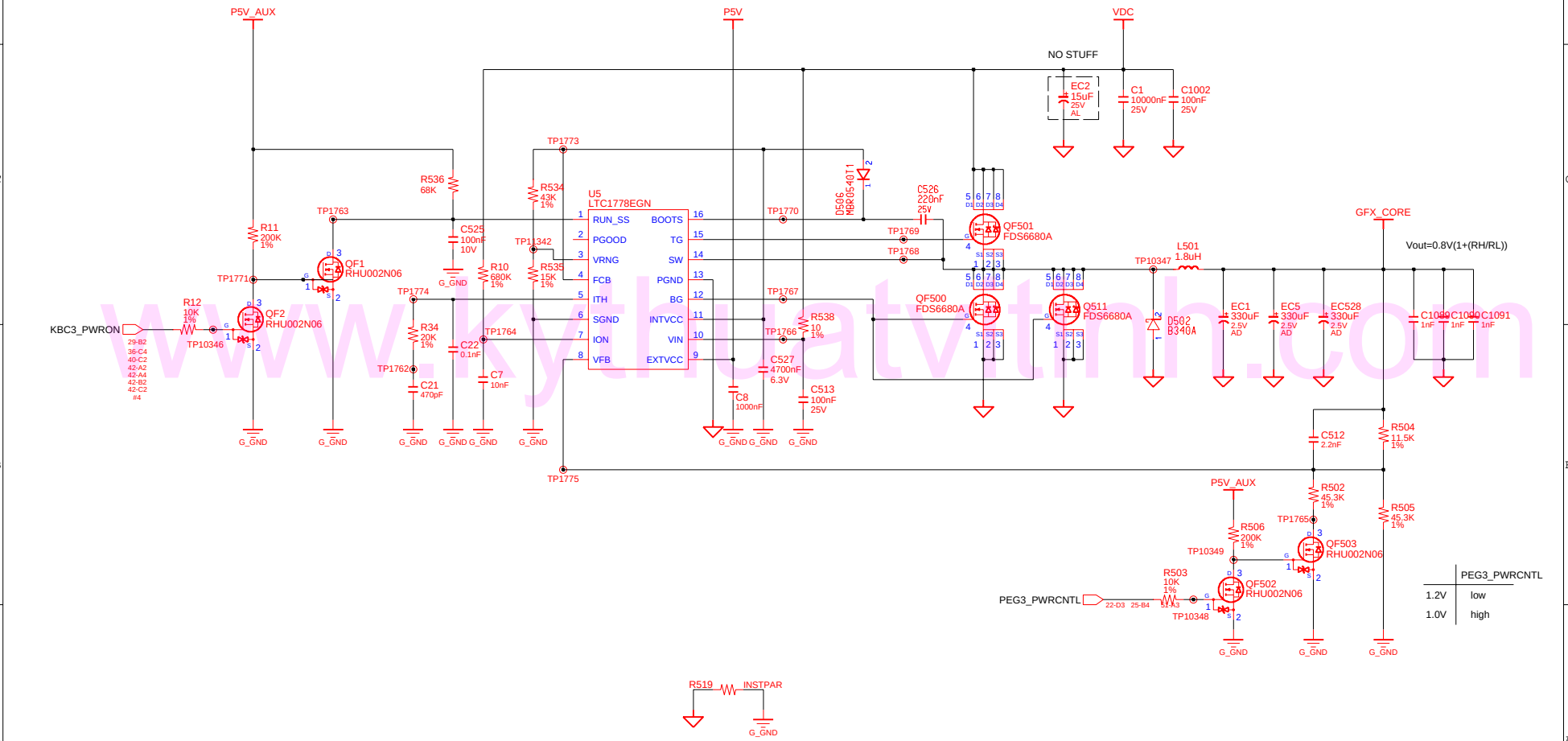


P5V

CHECK	DEV. STEP	STORNO	STORNO
BIN, KK	PR	MAIN	ELECTRONICS

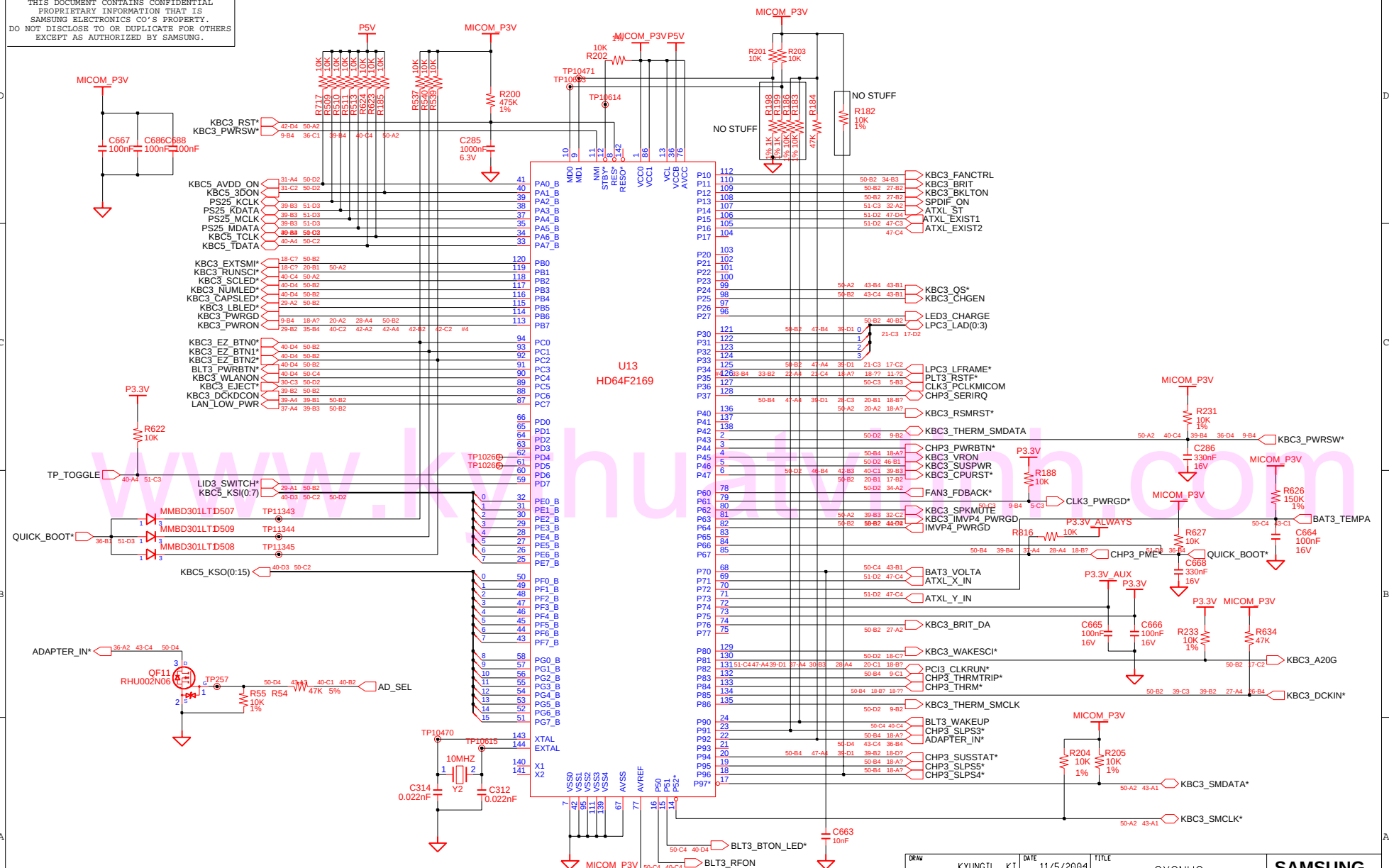
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Graphic Core Power



DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN GRAPHIC CORE POWER	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00450A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	35	OF 51

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U15
BCM5788MKFB

Table 1: Drawing and Revision Information

NO.	DATE	BY	CHK	APP	REV	DESCRIPTION
1	11/5/2004	KYUNGIL, KI	BIN, KK	KIM, DW	1.0	LAN(BROADCOM BCM5751M 1/2)

Table 2: Component Values

COMPONENT	VALUE
R683	0
C287	0.027nF
Y3	25MHz
C318	0.027nF
R682	0
R684	0
R686	1.24K 1%
R687	0
R688	0
R689	0
R690	0
R691	0
R692	0
R693	0
R694	0
R695	0
R696	0
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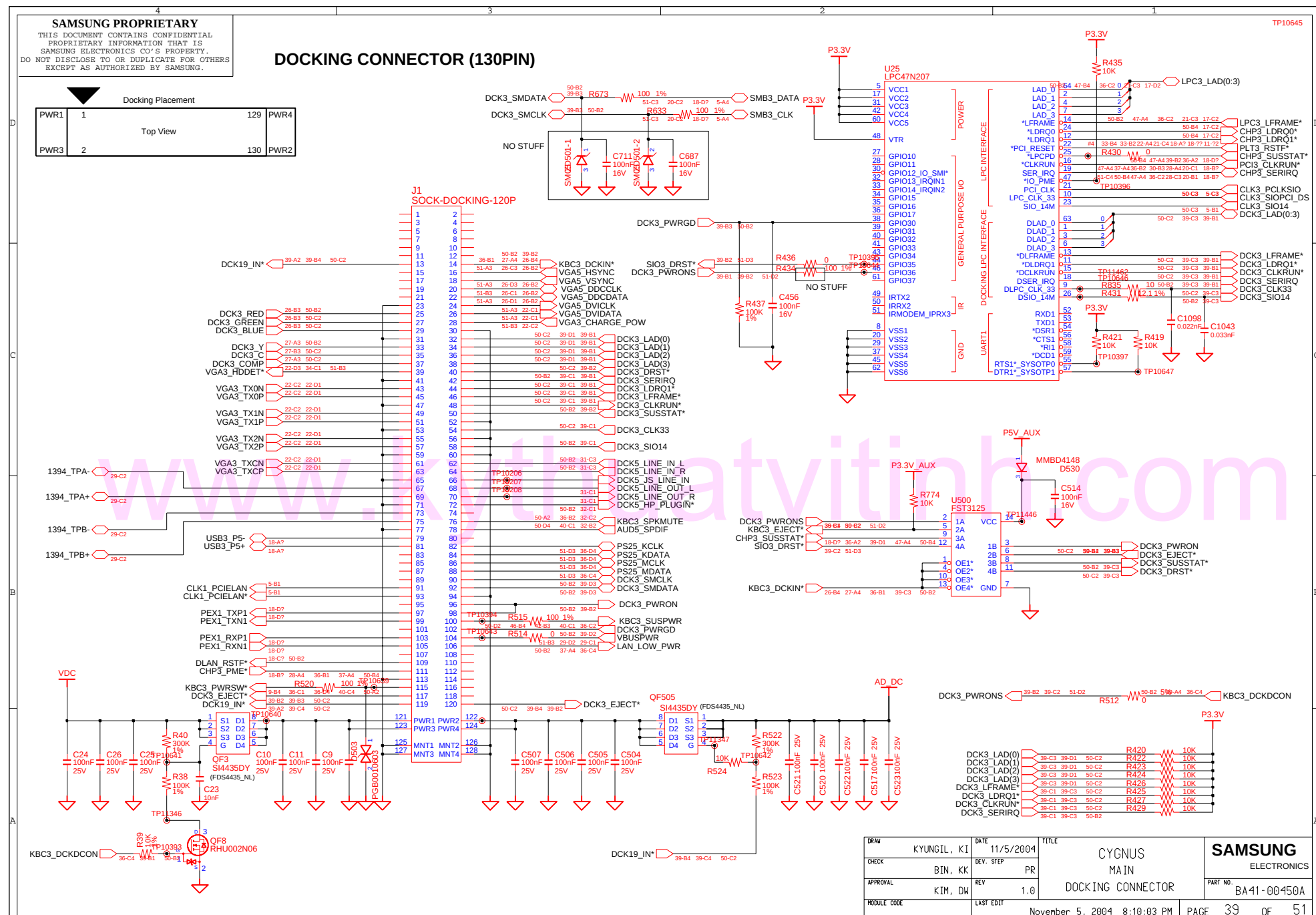
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d:/users/mobile20/mentor/Cognus/mp/main_mp10

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DOCKING CONNECTOR (130PIN)

PWR1	1	129	PWR4
Top View			
PWR3	2	130	PWR2

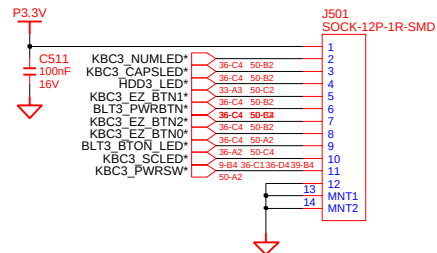


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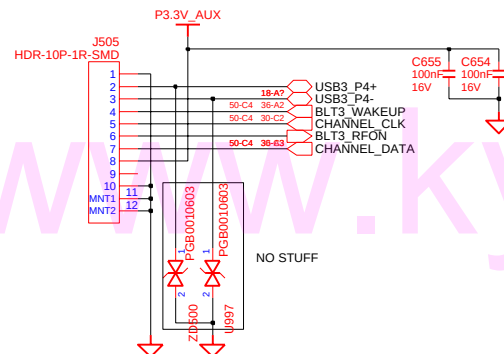
KEYBOARD

Main to DC/DC BOARD

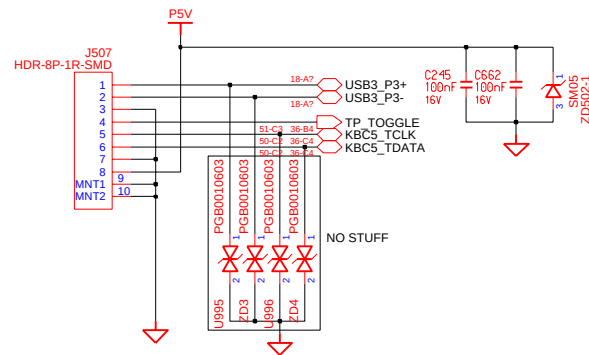
MAIN TO ON-TOP



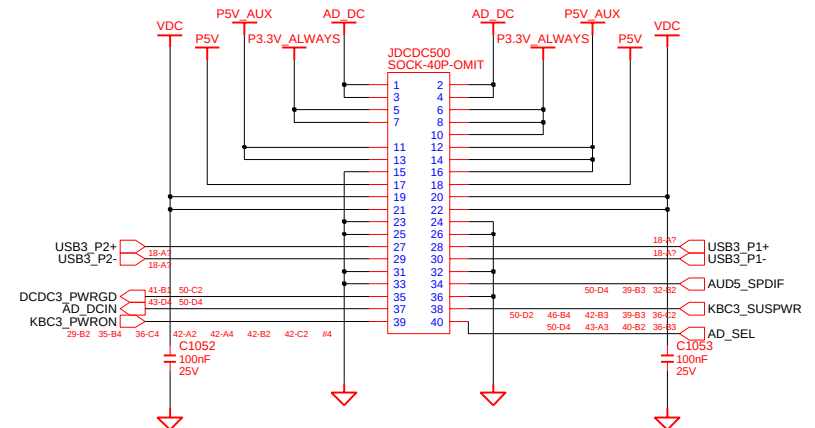
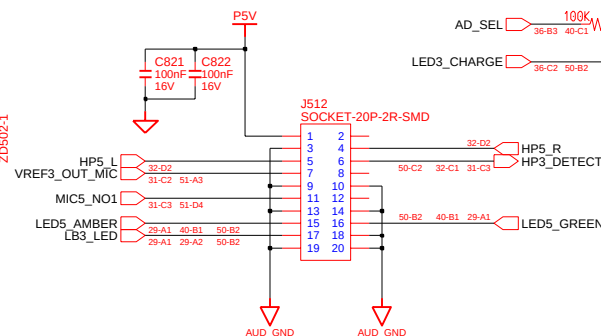
BLUETOOTH CONNECTOR



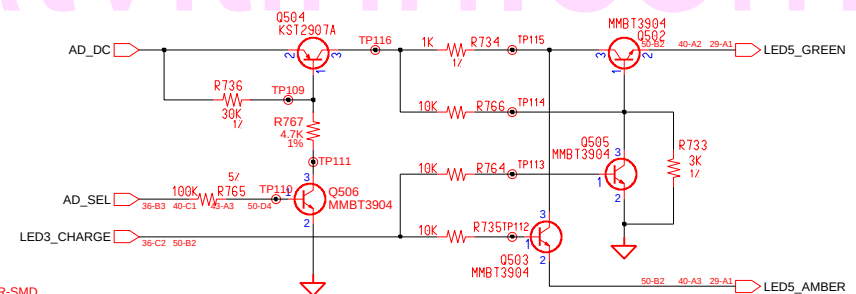
TOUCHPAD CONNECTOR



AUDIO CONNECTOR



ADAPTER IN/CHARGING LED

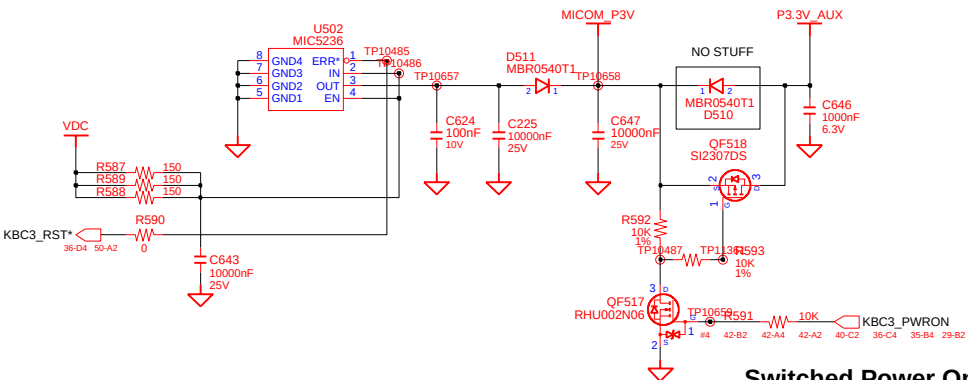


DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN B'D TO B'D CONNECTOR	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			PART NO.
APPROVAL	KIM, DW	REV	1.0			BA41-00450A
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	40	OF 51

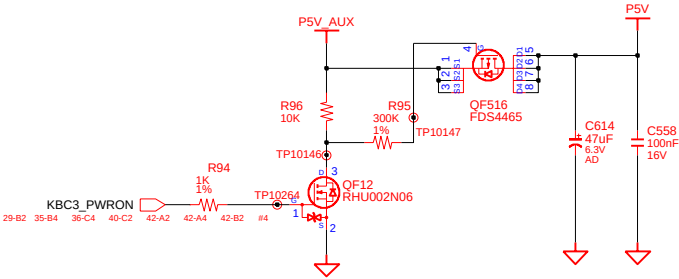
COM-22C-015(1996.6.5) REV. 3

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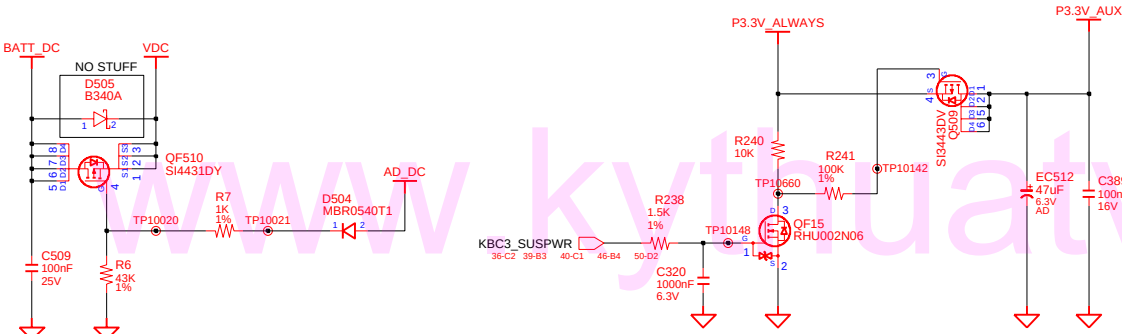
MICOM_P3V Power



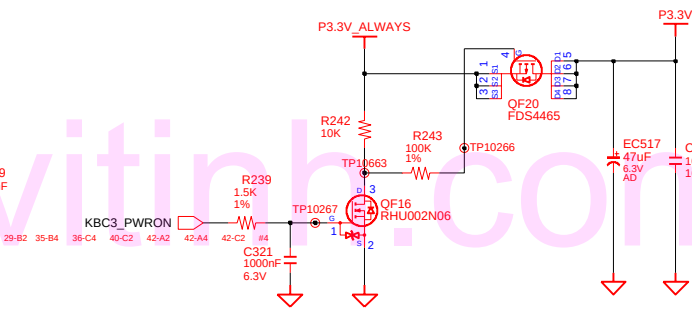
Switched Power On (P5V)



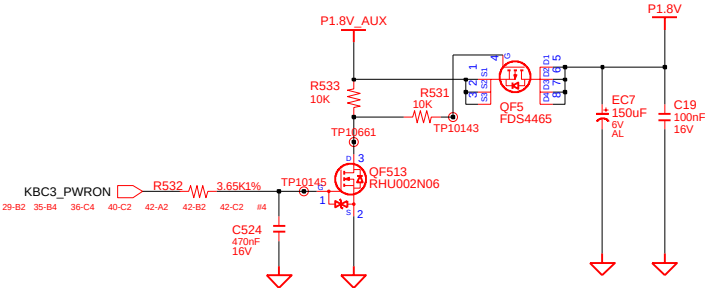
Switched Power On (P3.3V_AUX)



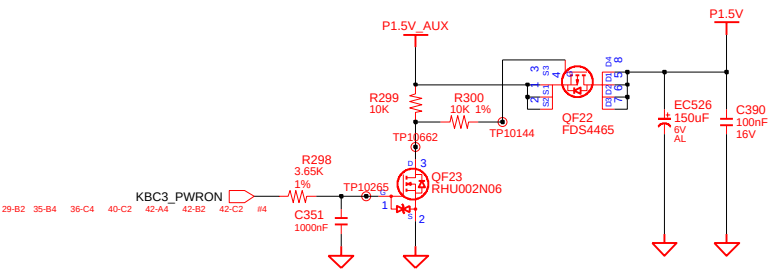
Switched Power On (P3.3V)



Switched Power On (P1.8V)



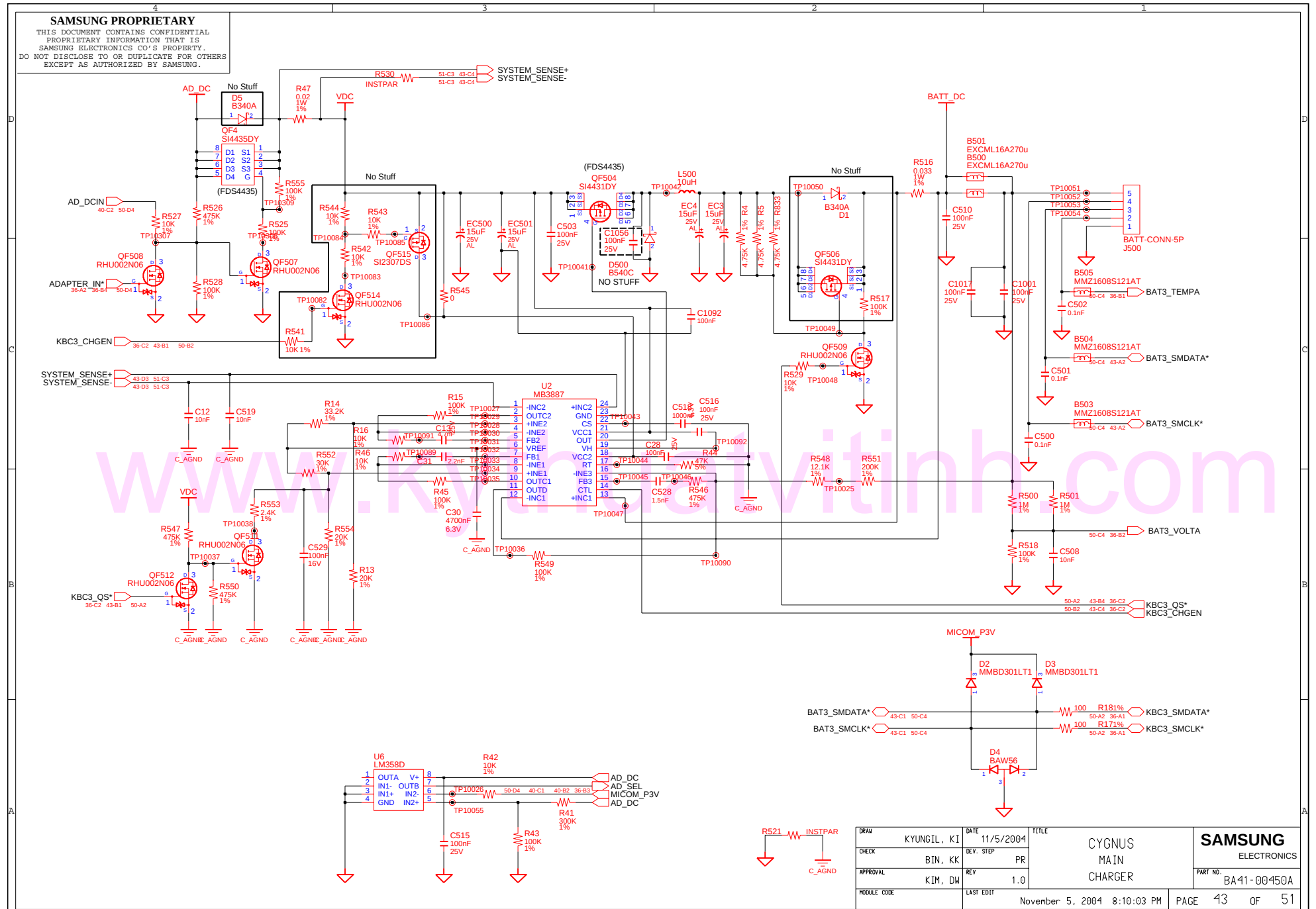
Switched Power On (P1.5V)



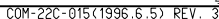
DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			PART NO. BA41-00450A
APPROVAL	KIM, DW	REV	1.0		MICOM & SWITCHED POWER	
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	42	OF 51

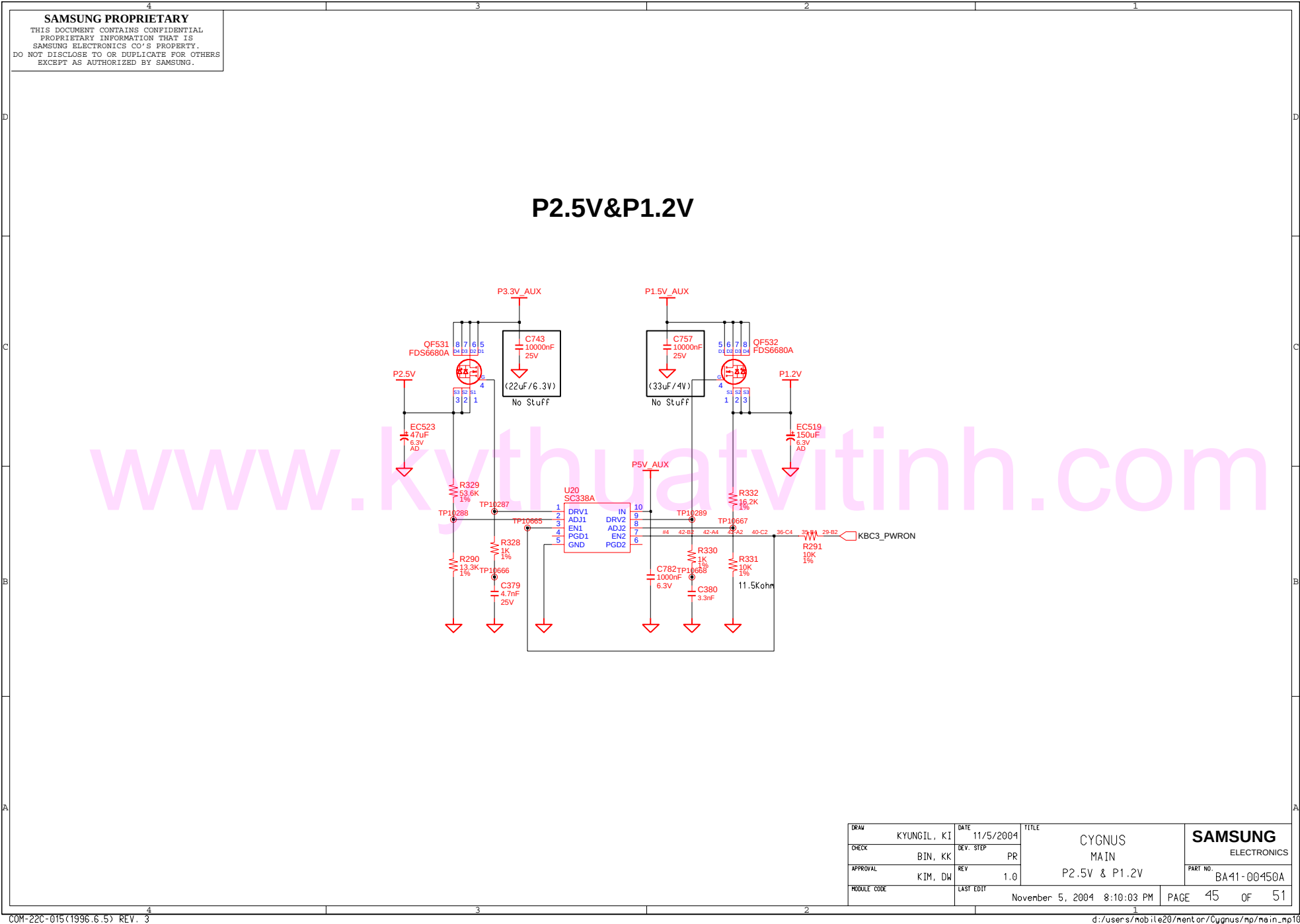
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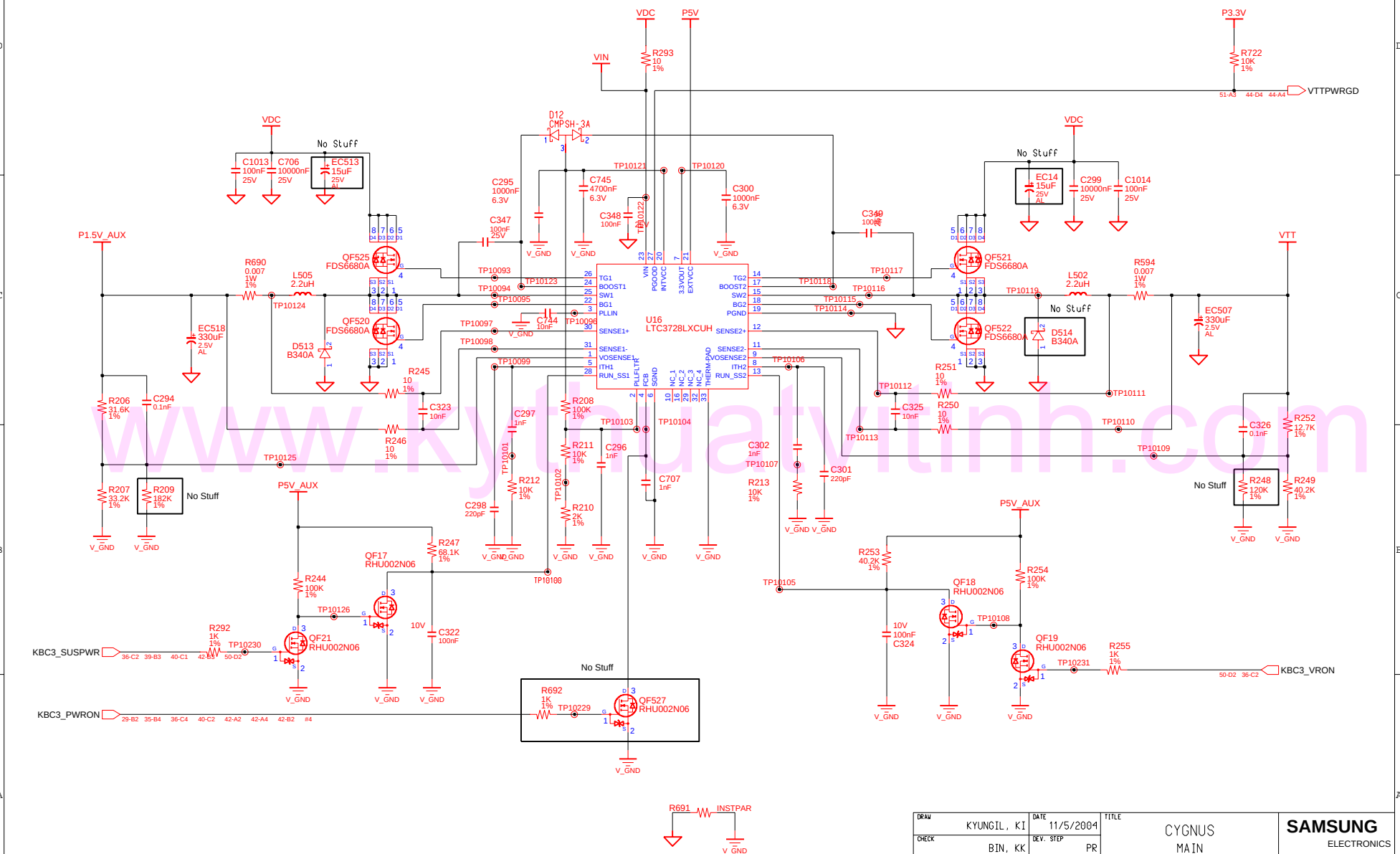


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DRAW KYUNGIL, KI		DATE 11/5/2004		TITLE CYGNUS MAIN			
CHECK BIN, KK		DEV. STEP PR		P1.5V_AUX & VTT		PART NO. BA41-00450A	
APPROVAL KIM, DW		REV 1.0		November 5, 2004 8:10:03 PM		PAGE 46 OF 51	
MODULE CODE		LAST EDIT					

NO STUFF



REV1
1_O
2_O _O3

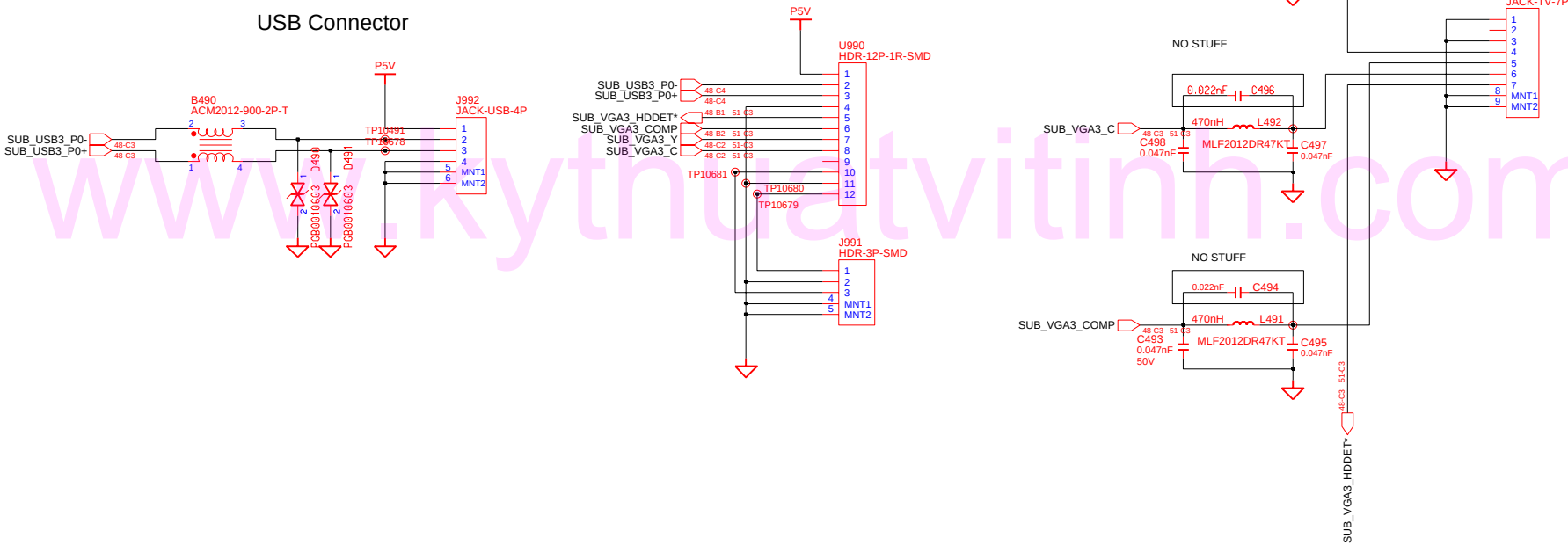
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< USB BOARD >

Mother Board I/F

USB Connector

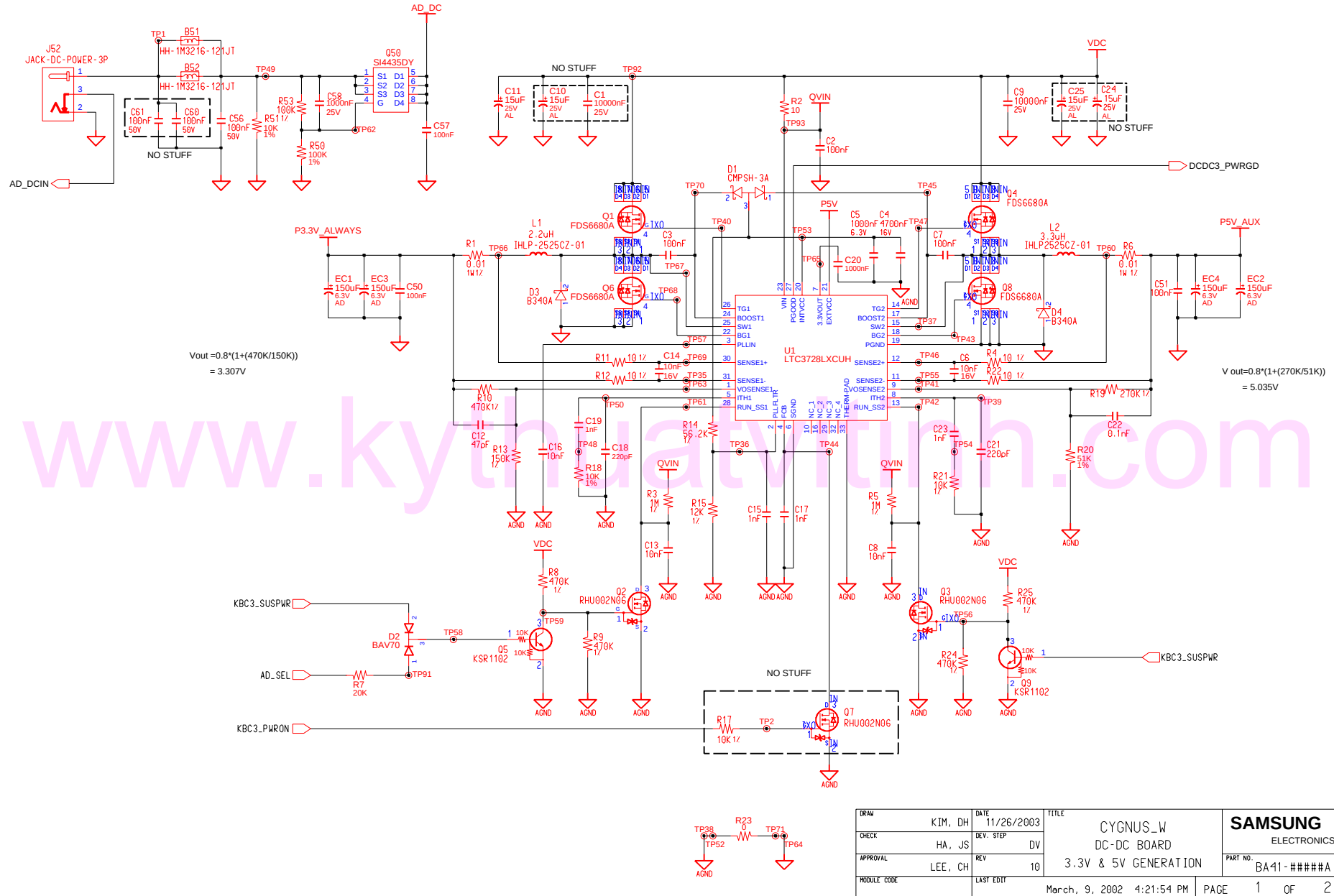
TV OUT JACK



DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN MOUNT HOLE	SAMSUNG ELECTRONICS
CHECK	BIN, KK	REV	PR			PART NO. BA41-00450A
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	48 OF 51	

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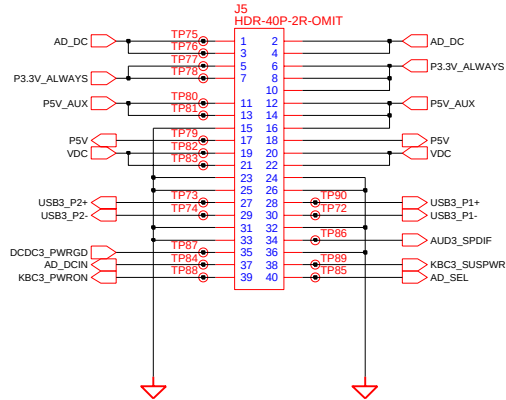


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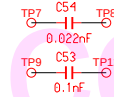
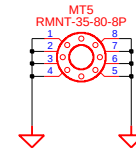
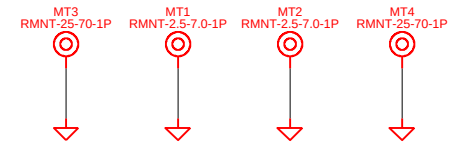
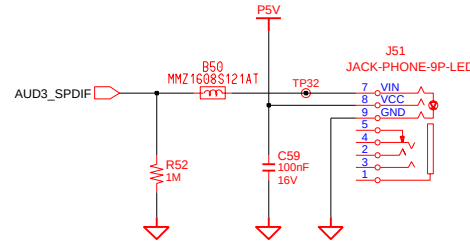
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CHANGE THIS CONNECTOR TO HEADER < 12809A-40G5T>

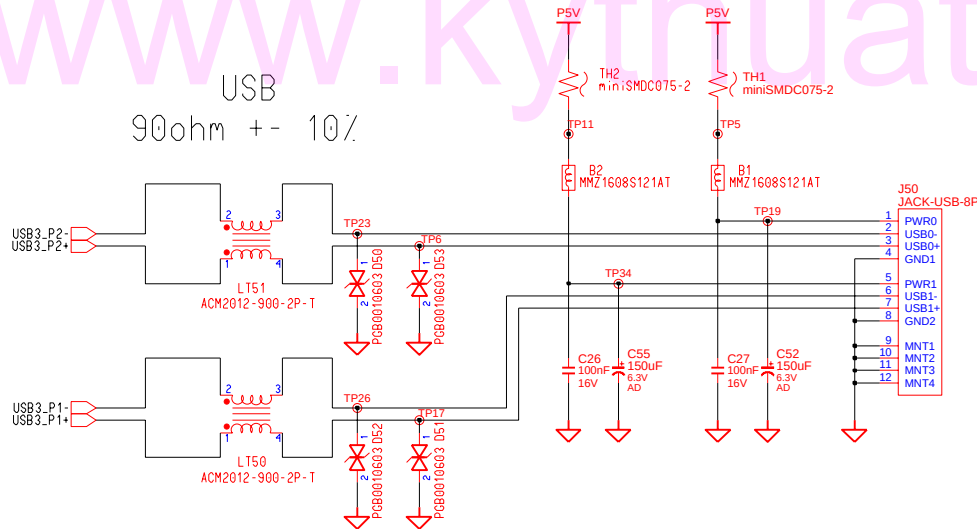
FROM DCDC TO MAIN BOARD



SPDIF OUT



USB
90ohm +- 10%

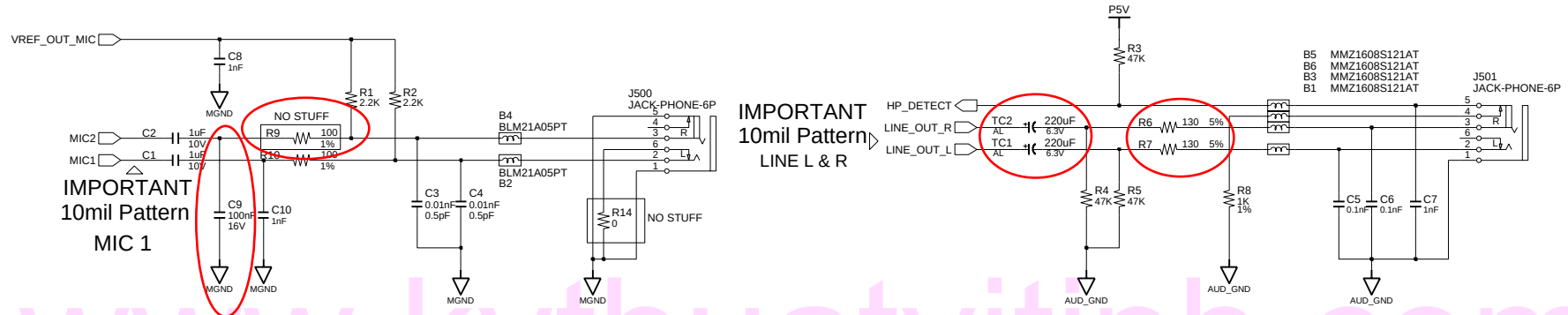


REV1
1 0
2 0 0 3

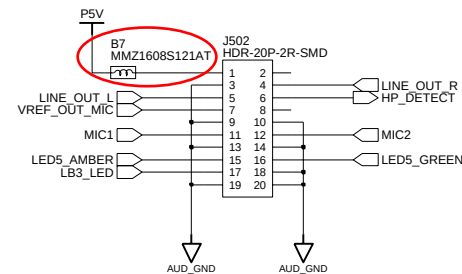
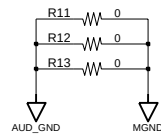
PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	KIM, DH	DATE	11/26/2003	TITLE	CYGNUS_W DC-DC BOARD CONNECTOR & PORT	SAMSUNG ELECTRONICS
CHECK	HA, JS	DEV. STEP	DV			PART NO. BA41-#####A
APPROVAL	LEE, CH	REV	10			
MODULE CODE		LAST EDIT	March, 9, 2002 4:23:55 PM	PAGE	2 OF 2	

< AUDIO BOARD >



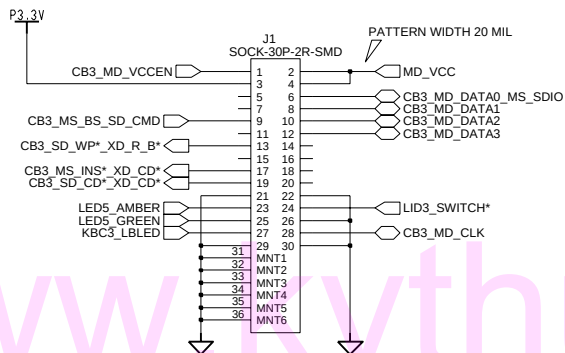
AQUILA I/F CONNECTOR 3711-0422



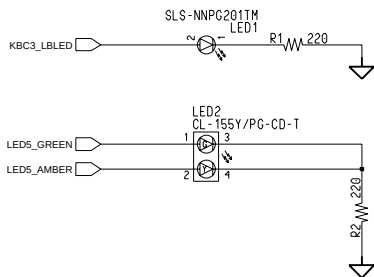
DRAW	DATE	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	DEV. STEP	Cygnus AUDIO JACK	
APPROVAL	REV		
MODULE CODE	LAST EDIT		
January, 30, 2004 9:34:17 AM			PAGE 1 OF

< 3 IN 1 BOARD >

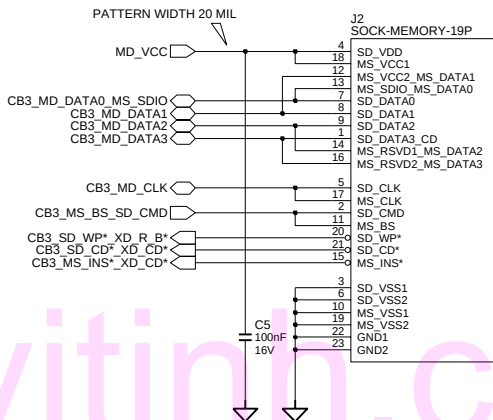
MAIN BOARD I/F CONNECTOR



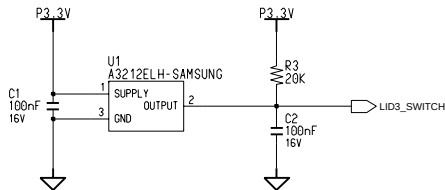
LED



Flash Media Socket



Lid Close Switch



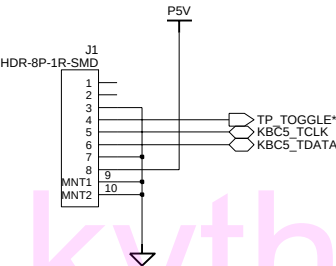
DRAW	DATE	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	DEV. STEP	CYGNUS MEMORY CARD	
APPROVAL	REV		
MODULE CODE	LAST EDIT		
January, 11, 2004 2:16:04 PM			PAGE 1 OF



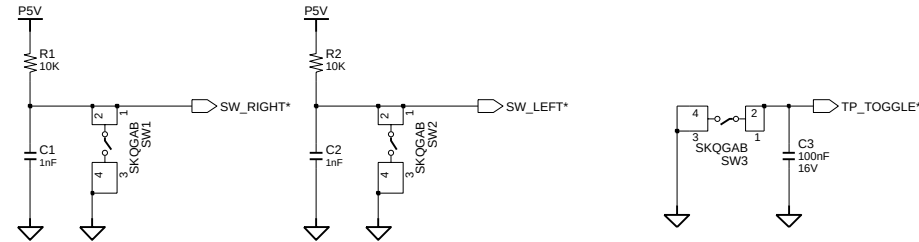
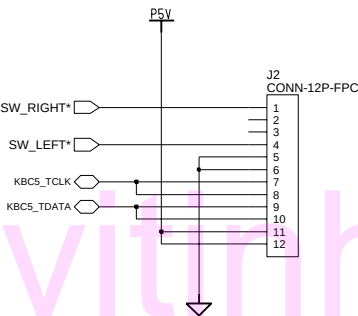
	4	3	2	1
COM-22C-015(1996.6.5) REV. 3				d:/users/mobile20/ment/or/Cygnus/ont

< TOUCHPAD BOARD >

MotherBoard I/F Connector



TouchPad Connector



DRAW	DATE	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	DEV. STEP	Cygnus TOUCHPAD	
APPROVAL	REV		
MODULE CODE	LAST EDIT		
undefined	January, 11, 2004 2:44:31 PM	PAGE 2 OF 3	