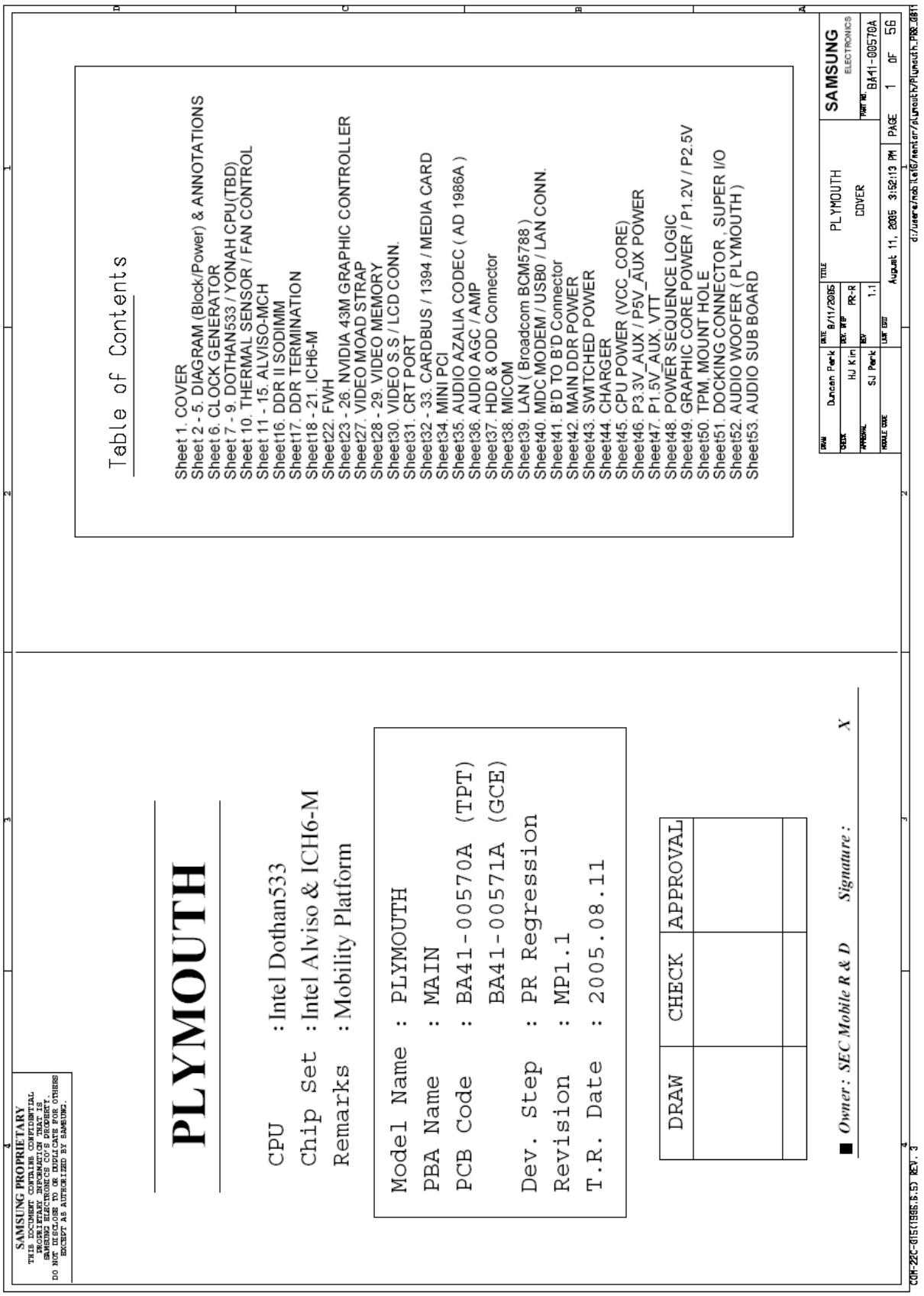
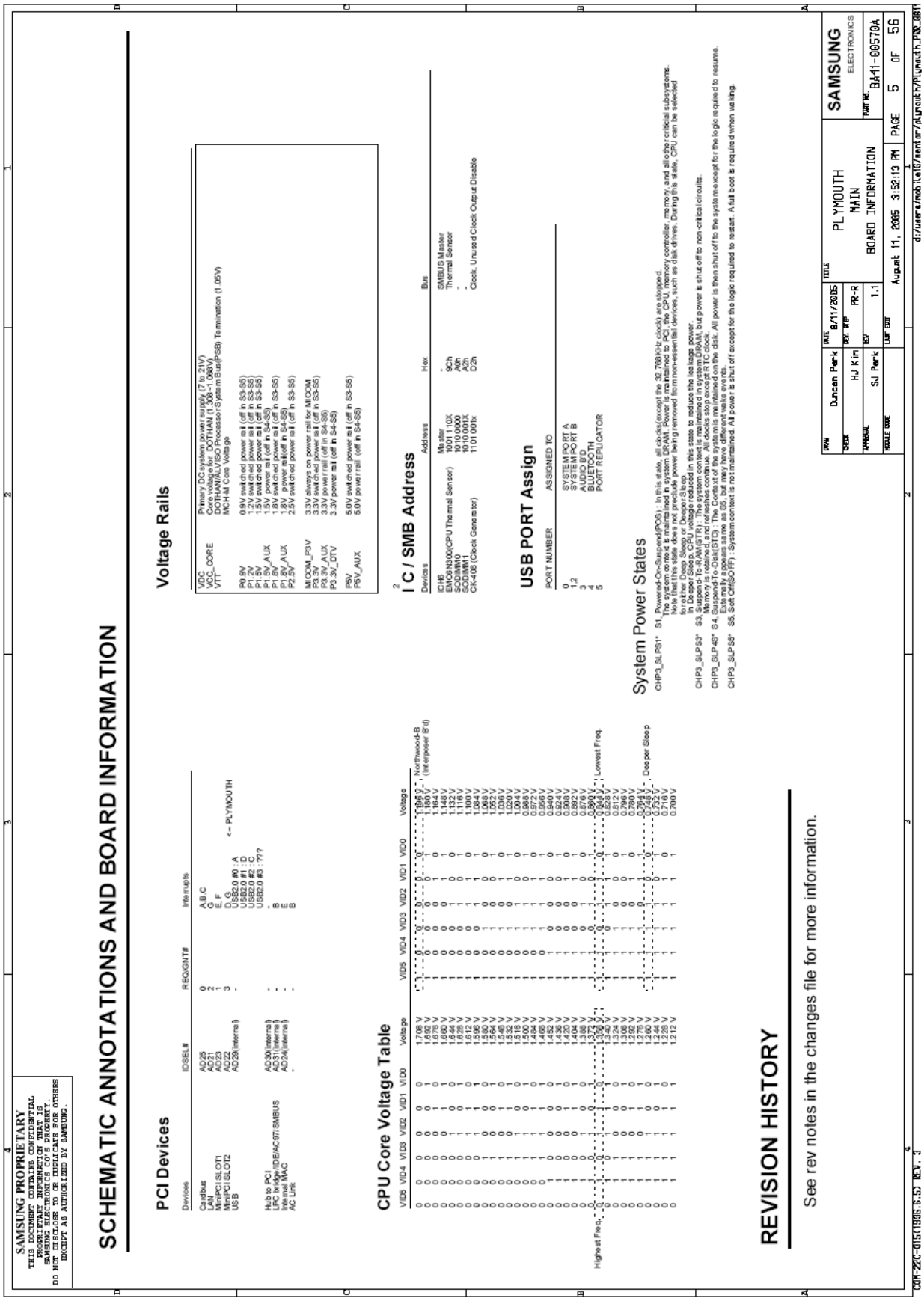
7. Schematic

1) System



7. Schematic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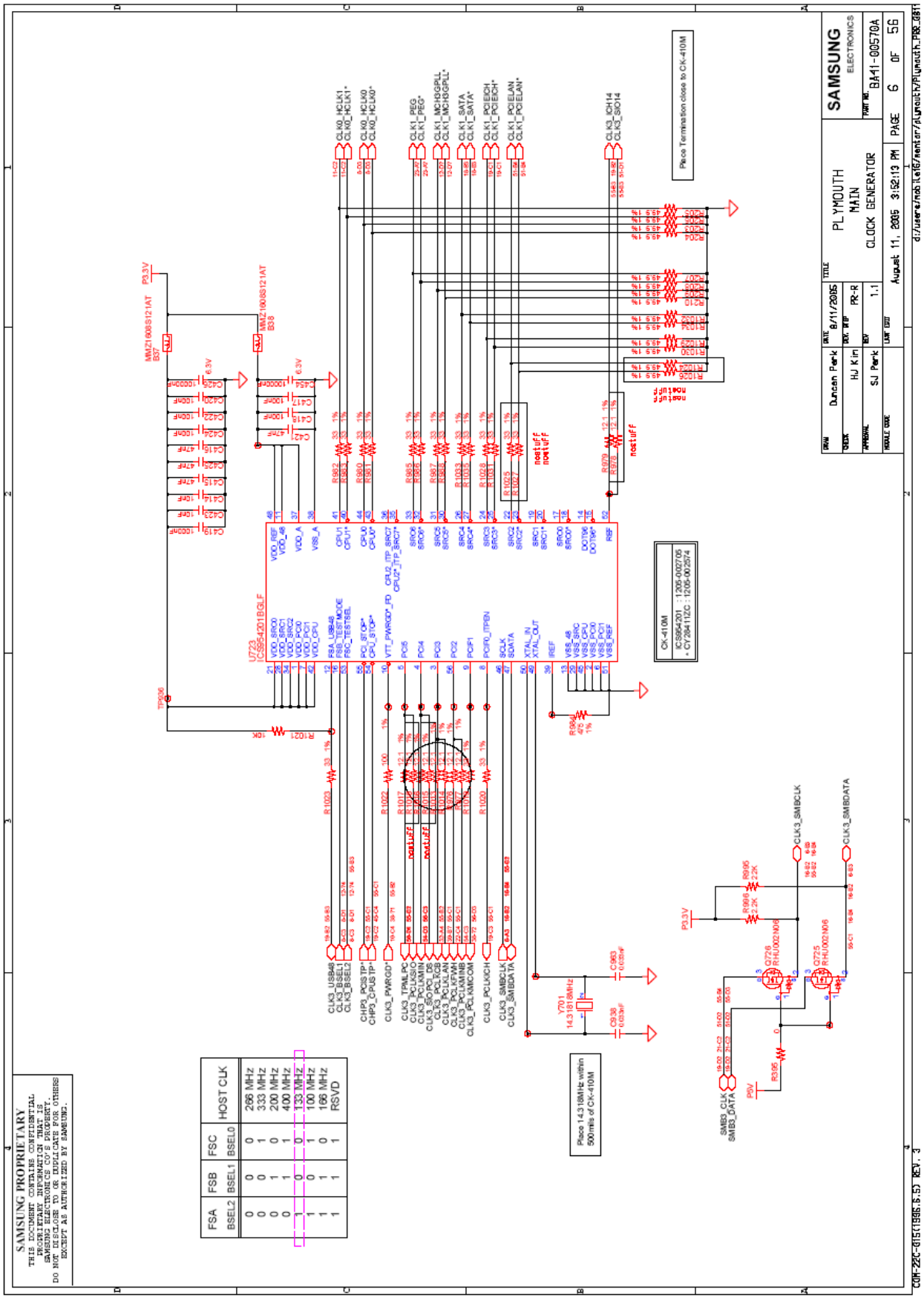
SCHEMATIC ANNOTATIONS AND BOARD INFORMATION
PCI Devices
Devices IDSEL# REQ/GNT# Interrupts
Cardbus AD25 0 A,B,C
LAN AD21 2 G
MiniPCI SLOT1 AD23 1 E,F
MiniPCI SLOT2 AD22 3 D,G
USB AD28(internal) - USB2.0 #0 : A <-- PLYMOUTH
USB2.0 #1 : D
USB2.0 #2 : C
USB2.0 #3 : ???
Hub to PCI - - B
LPC to Super IO/IDE/AC97/SMBUS AD30(internal) - - E
Internal MAC AD24(internal) - - B
AC Link - -
CPU Core Voltage Table
VID5 VID4 VID3 VID2 VID1 VID0 Voltage
1.708 V
1.692 V
1.676 V
1.660 V
1.644 V
1.628 V
1.612 V
1.596 V
1.580 V
1.564 V
1.548 V
1.532 V
1.516 V
1.500 V
1.484 V
1.468 V
1.452 V
1.436 V
1.420 V
1.404 V
1.388 V
1.372 V
1.356 V
1.340 V
1.324 V
1.308 V
1.292 V
1.276 V
1.260 V
1.244 V
1.228 V
1.212 V
Highest Freq.
Lowest Freq.
Northwood-B (Interposer Brd)
Deeper Sleep
Voltage Rails
VDC Primary DC system power supply (7 to 21V)
VCC_CORE Core voltage for DOTHAN (1.308~1.068V)
VTT DOTHAN/ALV/ISO Processor System Bus(FSB) Termination (1.05V)
MCH-M Core Voltage
P0.9V 0.9V switched power rail (off in S3-S5)
P1.2V 1.2V switched power rail (off in S3-S5)
P1.5V 1.5V switched power rail (off in S3-S5)
P1.8V_AUX 1.8V power rail (off in S3-S5)
P1.8V 1.8V switched power rail (off in S3-S5)
P1.8V_AUX 1.8V power rail(off in S4-S5)
P2.5V 2.5V switched power rail (off in S3-S5)
MCOM_P3V 3.3V always on power rail for MCOM
P3.3V 3.3V switched power rail (off in S3-S5)
P3.3V_AUX 3.3V power rail (off in S4-S5)
P3.3V_DTV 3.3V power rail (off in S4-S5)
P5V 5.0V switched power rail (off in S3-S5)
P5V_AUX 5.0V power rail (off in S4-S5)
I C / SMB Address
Devices Address Hex Bus
ICH9 Master -
EMC6N300(CPU Thermal Sensor) 1001 110X 9Ch SMBUS Master
SODIMM0 1010 0000 A0h Thermal Sensor
SODIMM1 1010 0010 A2h -
CK-408 (Clock Generator) 1101 001X D2h Clock, Unused Clock Output Disable
USB PORT Assign
PORT NUMBER ASSIGNED TO
0 SYSTEM PORT A
1,2 SYSTEM PORT B
3 AUDIO BD
4 BLUETOOTH
5 PORT REPLICATOR
System Power States
CHP3_SLPS1* S1 : Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768Khz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.
Non-critical subsystems may lose power (being removed from non-essential devices, such as disk drives. During this state, CPU can be selected
for either Deep Sleep or Deeper Sleep.
CHP3_SLPS3* S3 : Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is refreshed by the memory controller. Wakeup is accomplished via PCI or LAN or USB devices.
CHP3_SLP4S* S4 : Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.
CHP3_SLPS5* S5 : Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.
REVISION HISTORY
See rev notes in the changes file for more information.
DRAW Duncan Park DATE 8/11/2005 TITLE PLYMOUTH MAIN BOARD INFORMATION
DESK HJ Kim DOC WRP PR-R
APPROVAL SJ Park REV 1.1
MODULE CODE LAST EDIT August 11, 2005 3:52:13 PM
SAMSUNG ELECTRONICS
PART NO BA41-00570A
PAGE 5 OF 56
d:/users/hdkim/cells/mentor/plymouth/Plymouth.PRR.0811
COM-22C-01(1995.5.5) REV. 3

7. Schematic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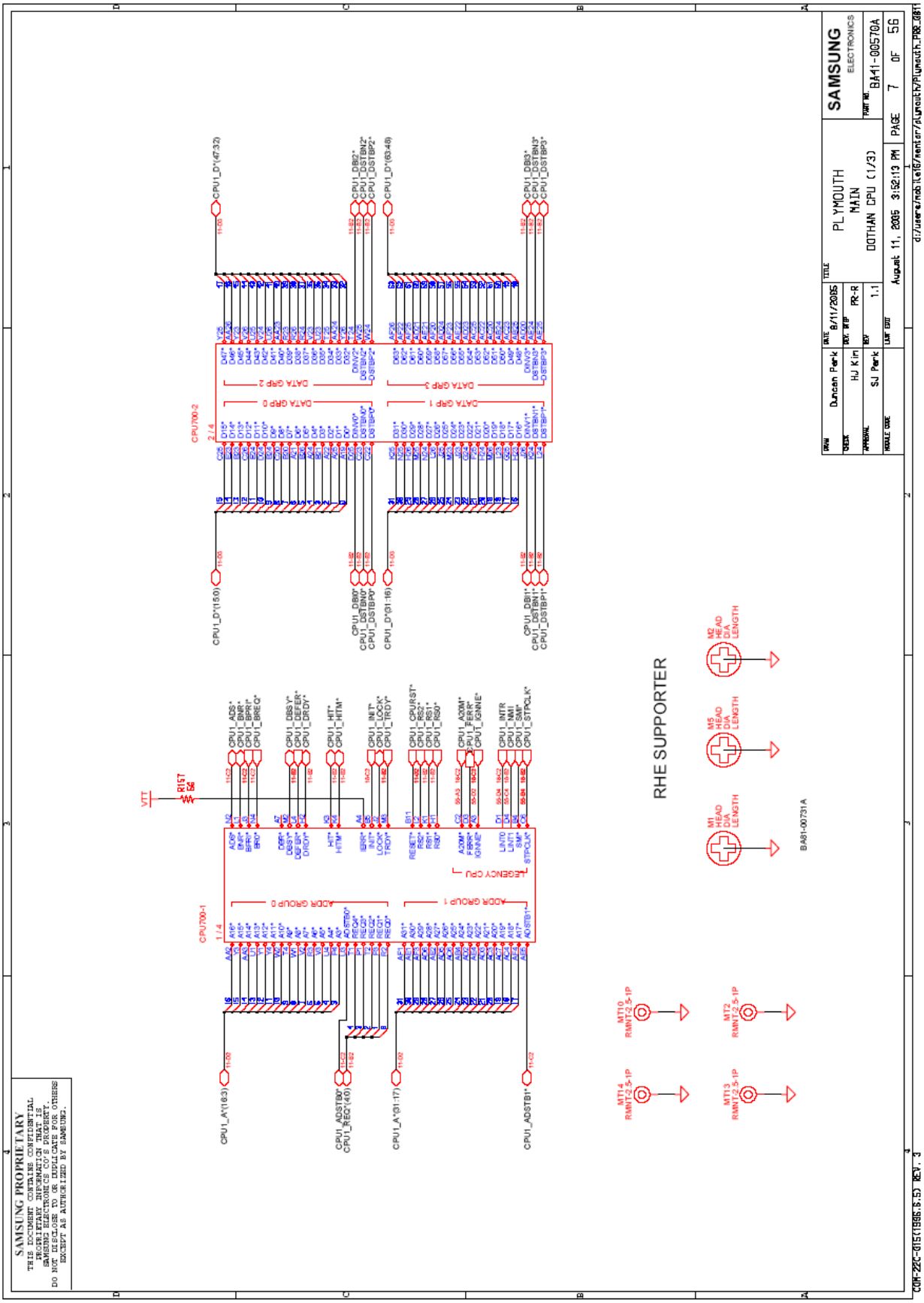
FSA BSEL2 FSB BSEL1 FSC BSEL0 HOST CLK
0 0 0 0 0 266 MHz
0 0 0 1 1 333 MHz
0 1 0 0 0 200 MHz
0 1 0 1 1 400 MHz
1 0 1 0 0 133 MHz
1 1 1 0 1 100 MHz
1 1 1 1 1 RSVD
SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
CLOCK GENERATOR
BA41-00570A
PAGE 6 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile6/mentor/plymouth/Plymouth_PRE_0811
COM-22C-011(1998.6.5) REV. 3

7. Schematic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SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
DOTHAN CPU (1/3)
BA41-00570A
PAGE 7 OF 56
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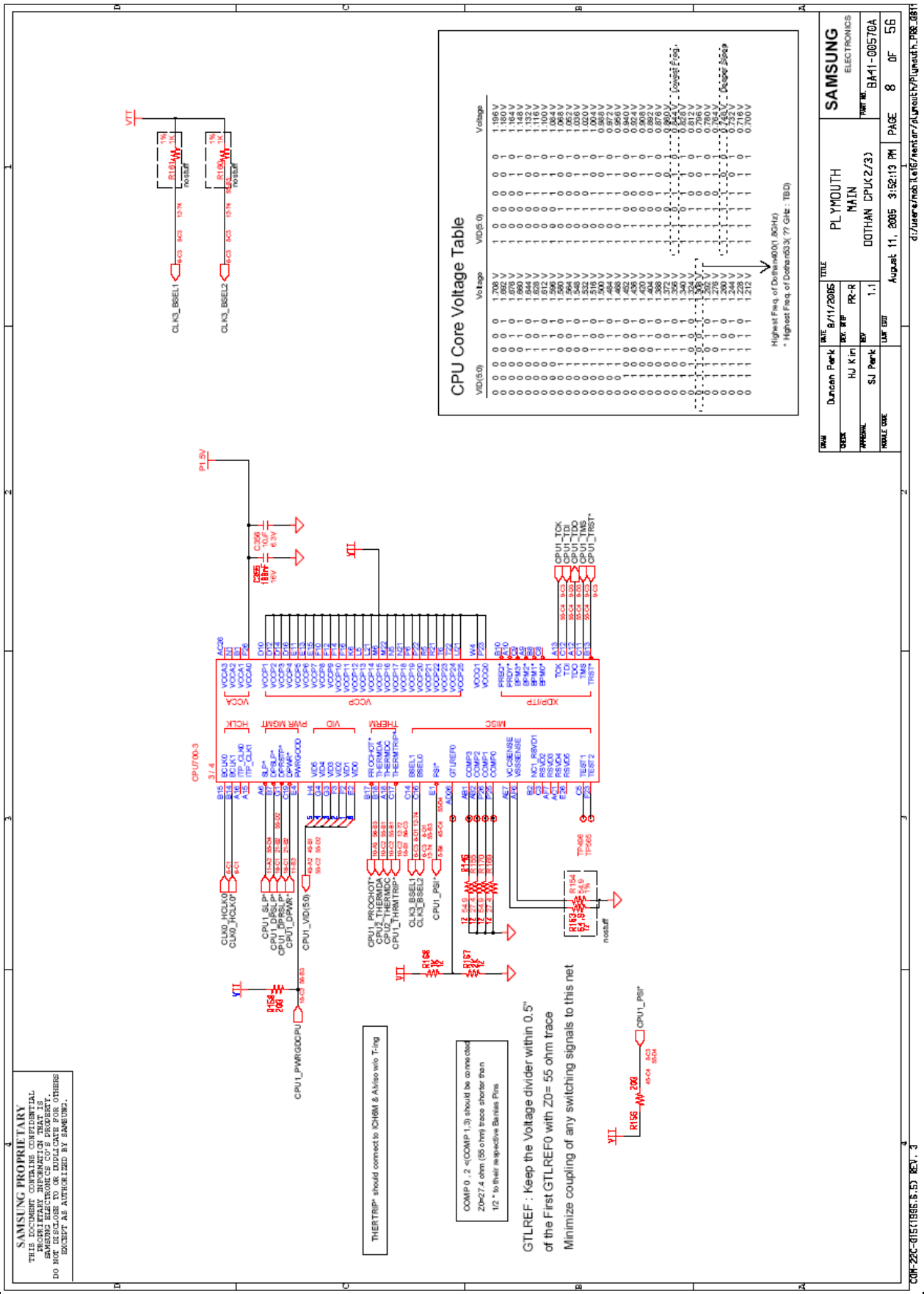
Duncan Park 8/11/2005
HJ Kim PR-R
SJ Park 1.1
CPU700-1
CPU700-2
RHE SUPPORTER
BA91-00731A

7. Schematic


CPU Core Voltage Table
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
DOTHAN CPUK2/33)
BA41-00570A
PAGE 8 OF 56
August 11, 2005 3:52:13 PM
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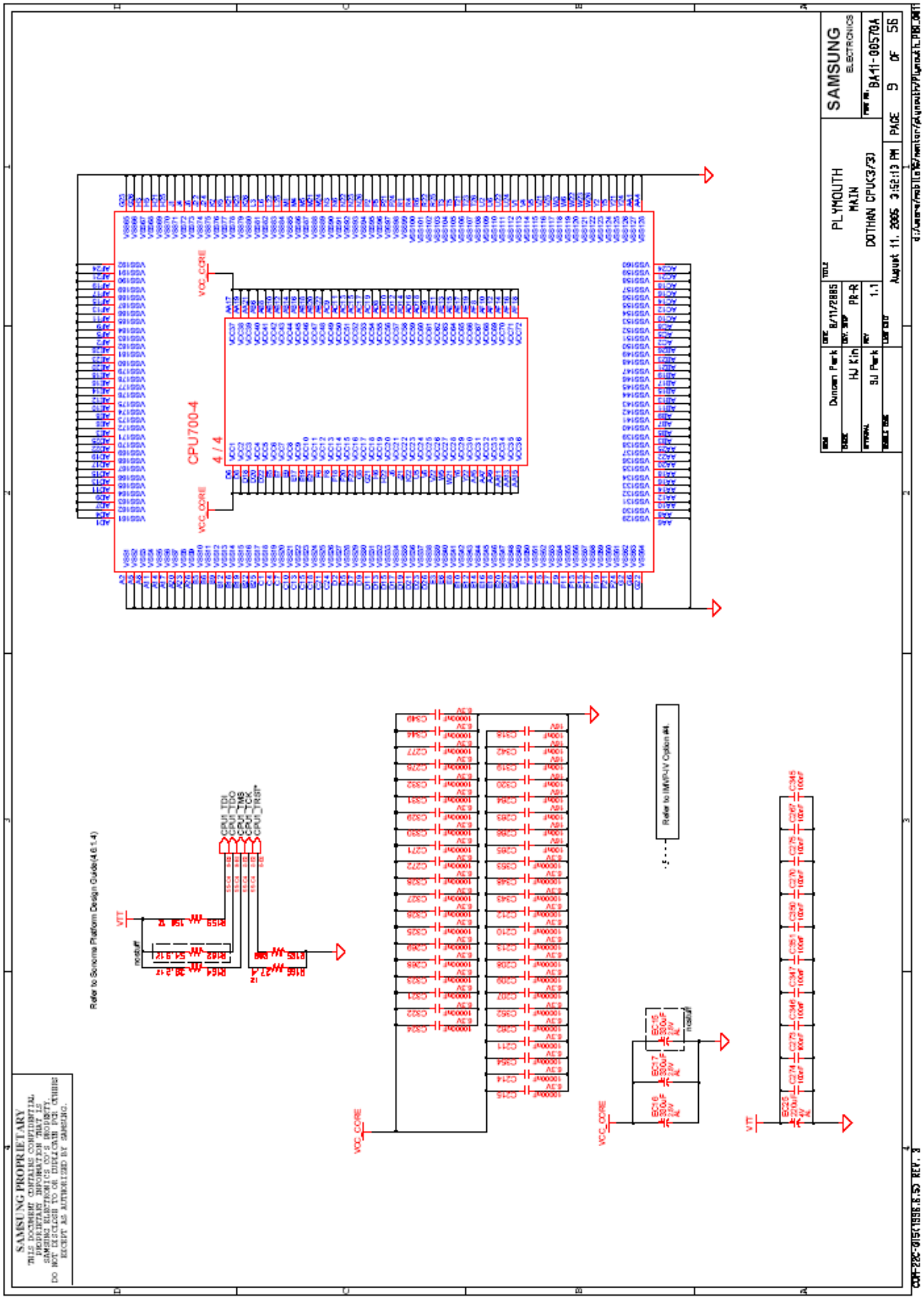
GTLREF : Keep the Voltage divider within 0.5"
of the First GTLREF0 with Z0= 55 ohm trace
Minimize coupling of any switching signals to this net

7. Schematic


CPU700-4
4 / 4
VCC_CORE
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
DOTHAN CPUC3/3M
August 11, 2005 3:52:13 PM
PAGE 9 OF 56
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SJ Park
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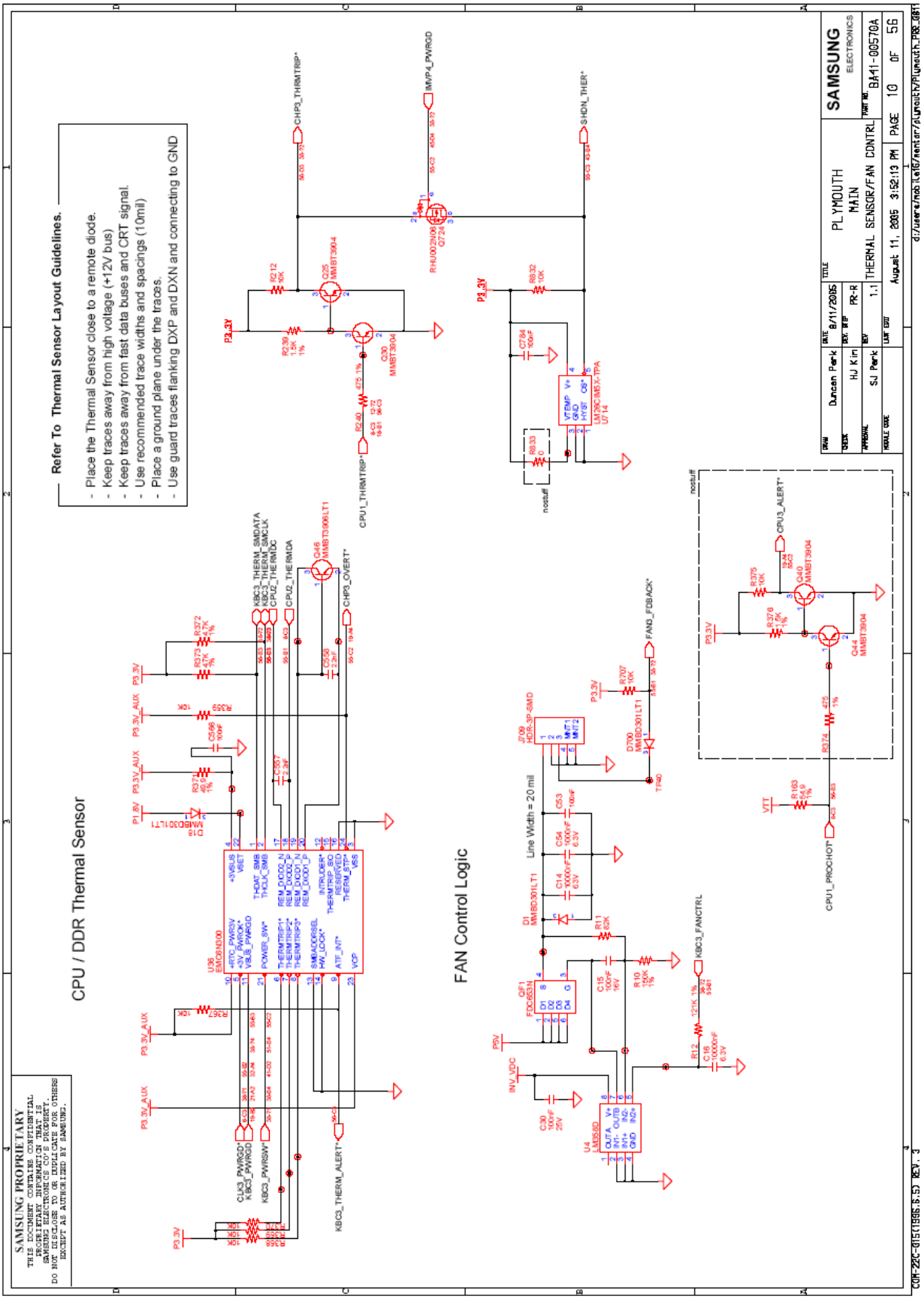
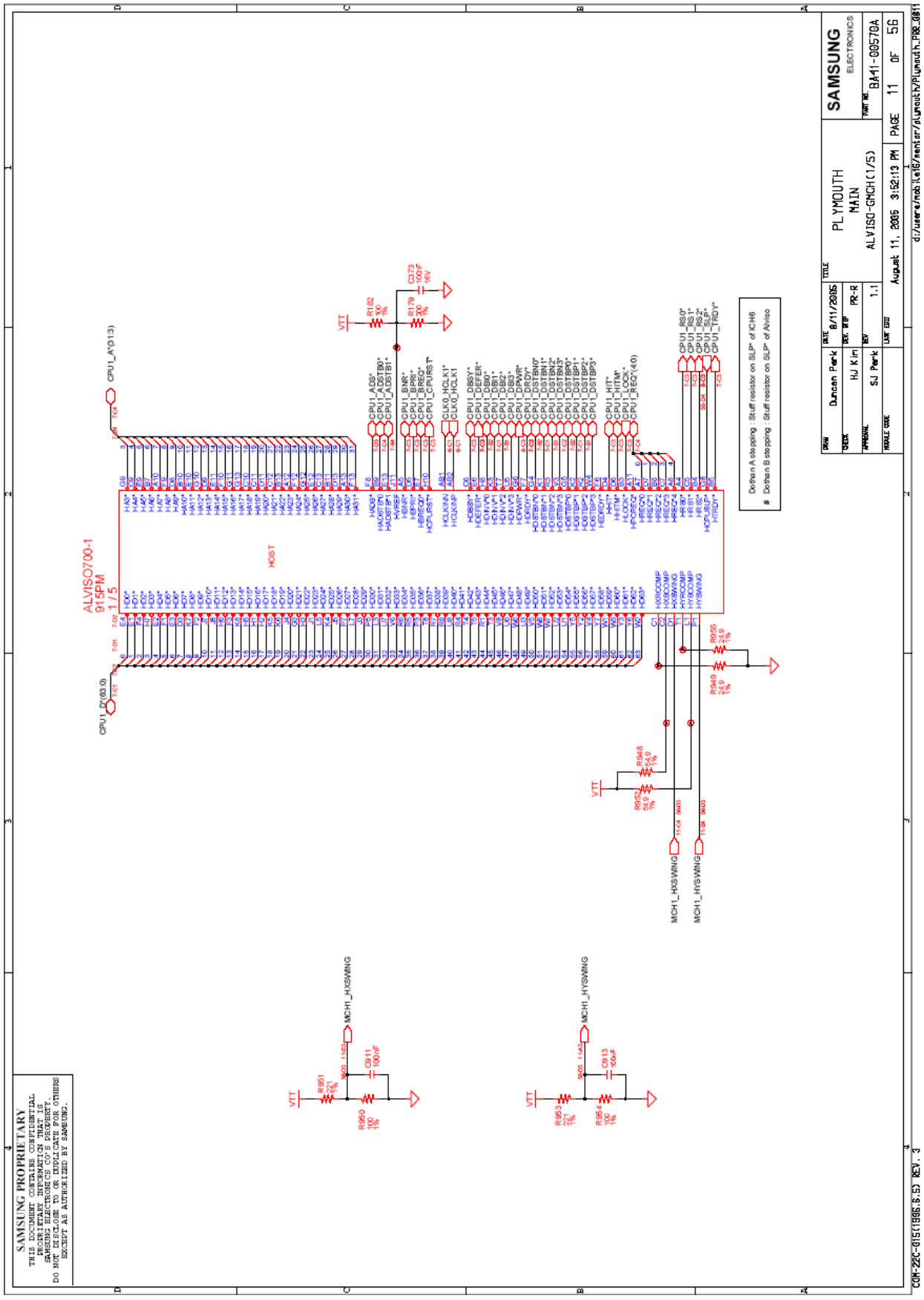
PR-R
1.1
SAMSUNG PROPRIETARY
Refer to Sonoma Platform Design Guide(4.6.1-4)
Refer to IMVP-IV Option #4
CPU_TDI
CPU_TDO
CPU_TMS
CPU_TCK
CPU_TRST*
VTT

7. Schematic


Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND
CPU / DDR Thermal Sensor
FAN Control Logic
SAMSUNG PROPRIETARY
SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
THERMAL SENSOR/FAN CONTRL
BA41-00570A
PAGE 10 OF 56
August 11, 2005 3:52:13 PM

7. Schematic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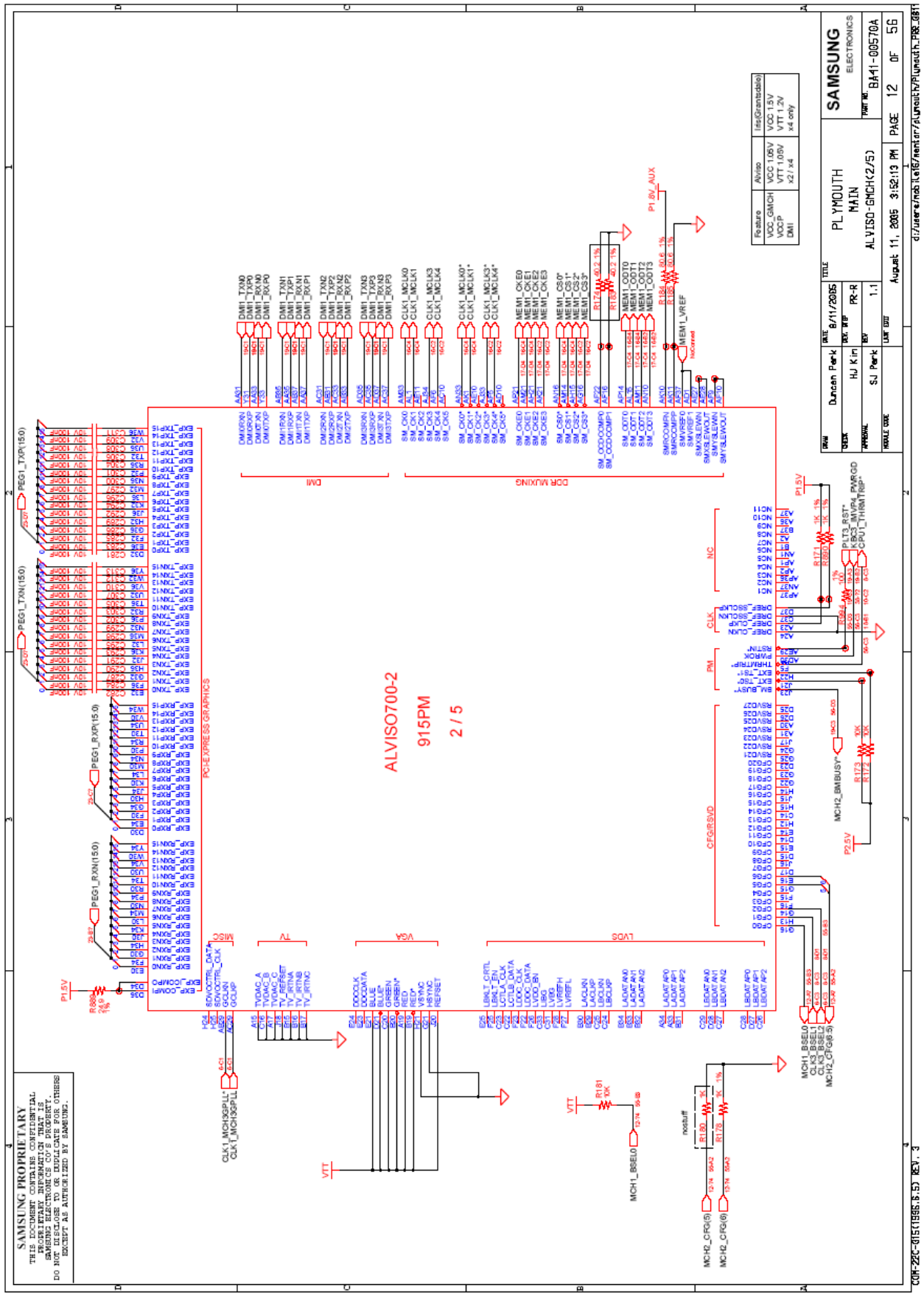
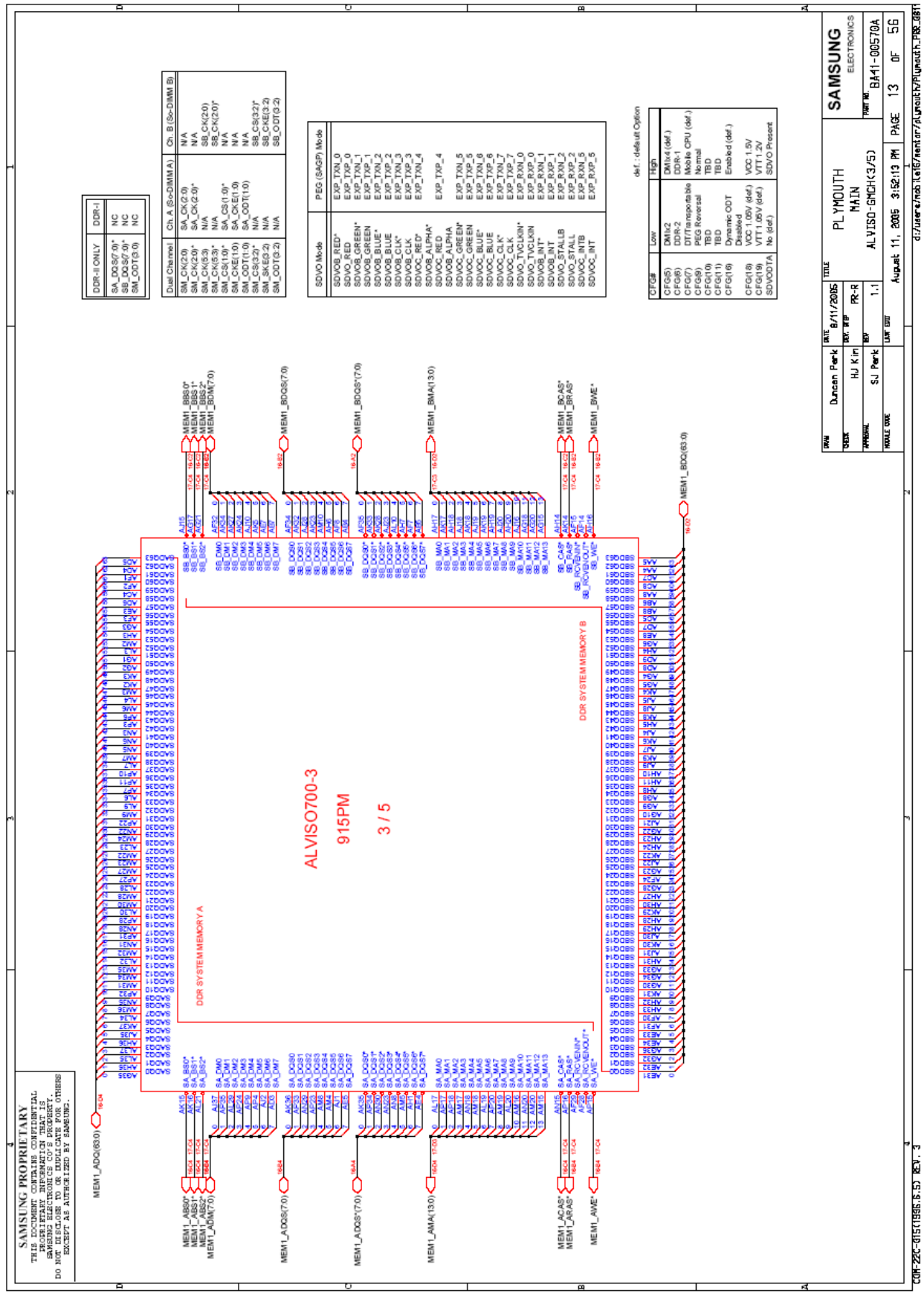
PLYMOUTH
MAIN
ALVISO-GMCH(1/5)
BA41-00570A
PAGE 11 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1:1
ALVISO700-1
915PM
1/5
HOST
CPU1_A*(31:3)
CPU1_D*(63:0)
VTT
MCH1_HXSWING
MCH1_HYSWING
Define A stepping : Stuff resistor on SLP* of ICH6
Define B stepping : Stuff resistor on SLP* of Alviso

7. Schematic


ALVISO700-2
915PM
2 / 5
PCI-EXPRESS GRAPHICS
DDR MUXING
DMI
VGA
TV
LVDS
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
ALVISO-GMCH(2/5)
BA41-00570A
PAGE 12 OF 56
August 11, 2005 3:52:13 PM

7. Schematic


ALVISO700-3
915PM
3 / 5
DDR SYSTEM MEMORY A
DDR SYSTEM MEMORY B
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
ALVISO-GMCH(3/5)
BA41-00570A
PAGE 13 OF 56
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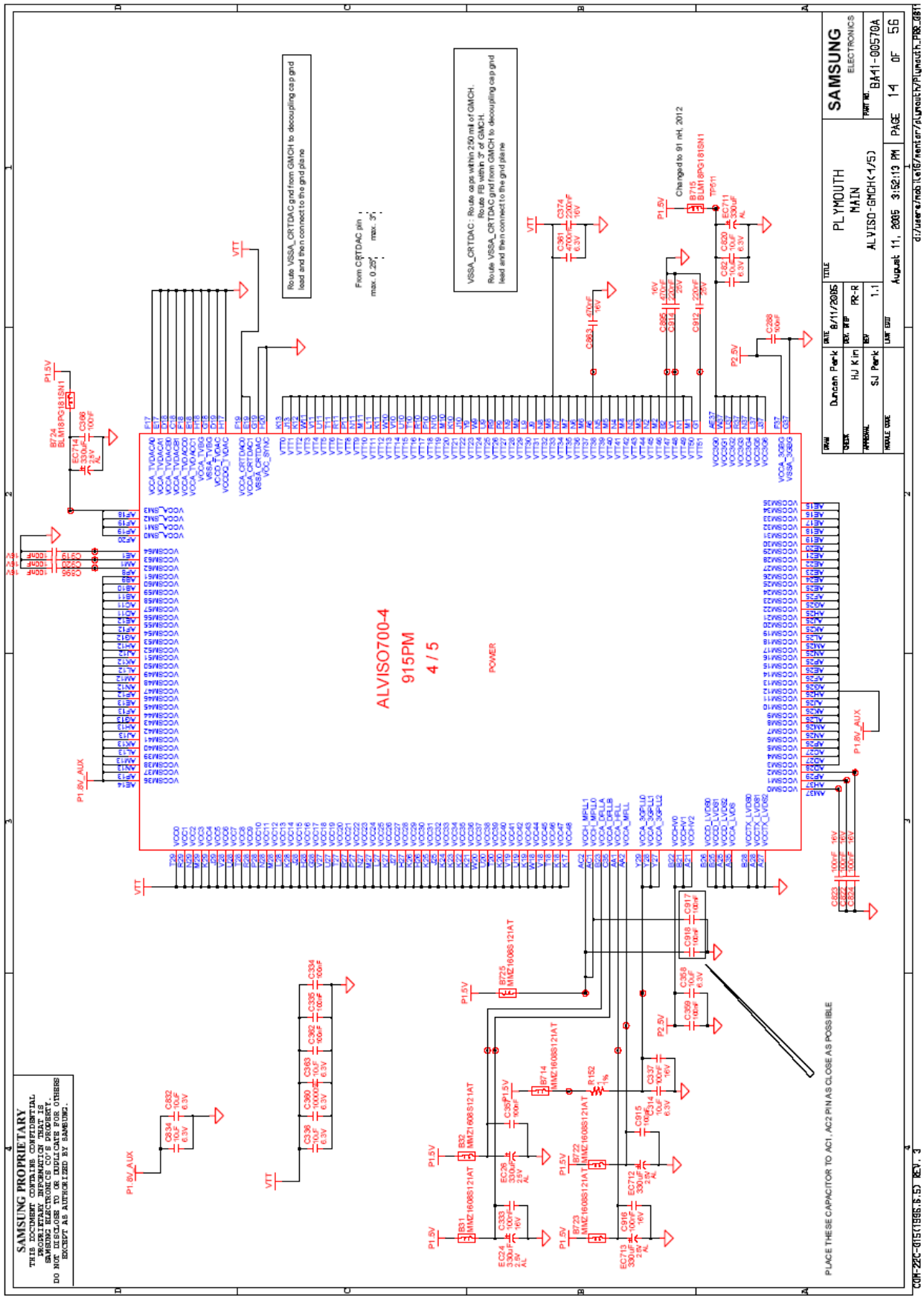
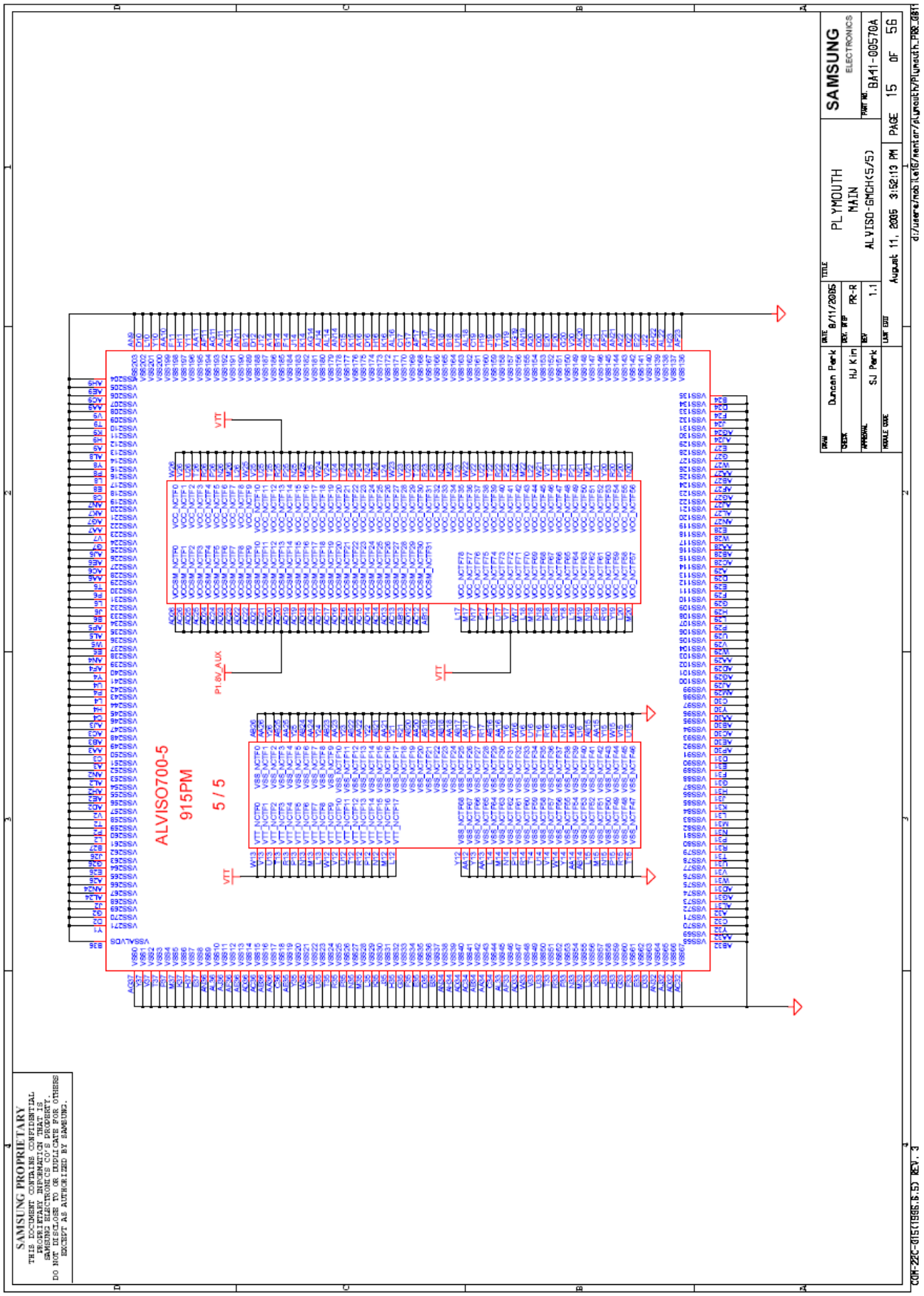
7. Schematic


SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
ALVISO-GMCH(4/5)
BA41-00570A
PAGE 14 OF 56
August 11, 2005 3:52:13 PM
ALVISO700-4
915PM
4 / 5
POWER
SAMSUNG PROPRIETARY
PLACE THESE CAPACITOR TO AC1 ,AC2 PIN AS CLOSE AS POSSIBLE
Route VSSA_CRTDAC grid from GMCH to decoupling cap grid lead and then connect to the grid plane
From CRTDAC pin : max. 0.25" ; max. 3" ;
VSSA_CRTDAC : Route caps within 250 mil of GMCH.
Route FB within 3" of GMCH.
Route VSSA_CRTDAC grid from GMCH to decoupling cap grid lead and then connect to the grid plane
Changed to 91 nH, 2012
P1.5V
P2.5V
P1.8V_AUX
VTT

7. Schematic


ALVISO700-5
915PM
5 / 5
VTT
P1.8V_AUX
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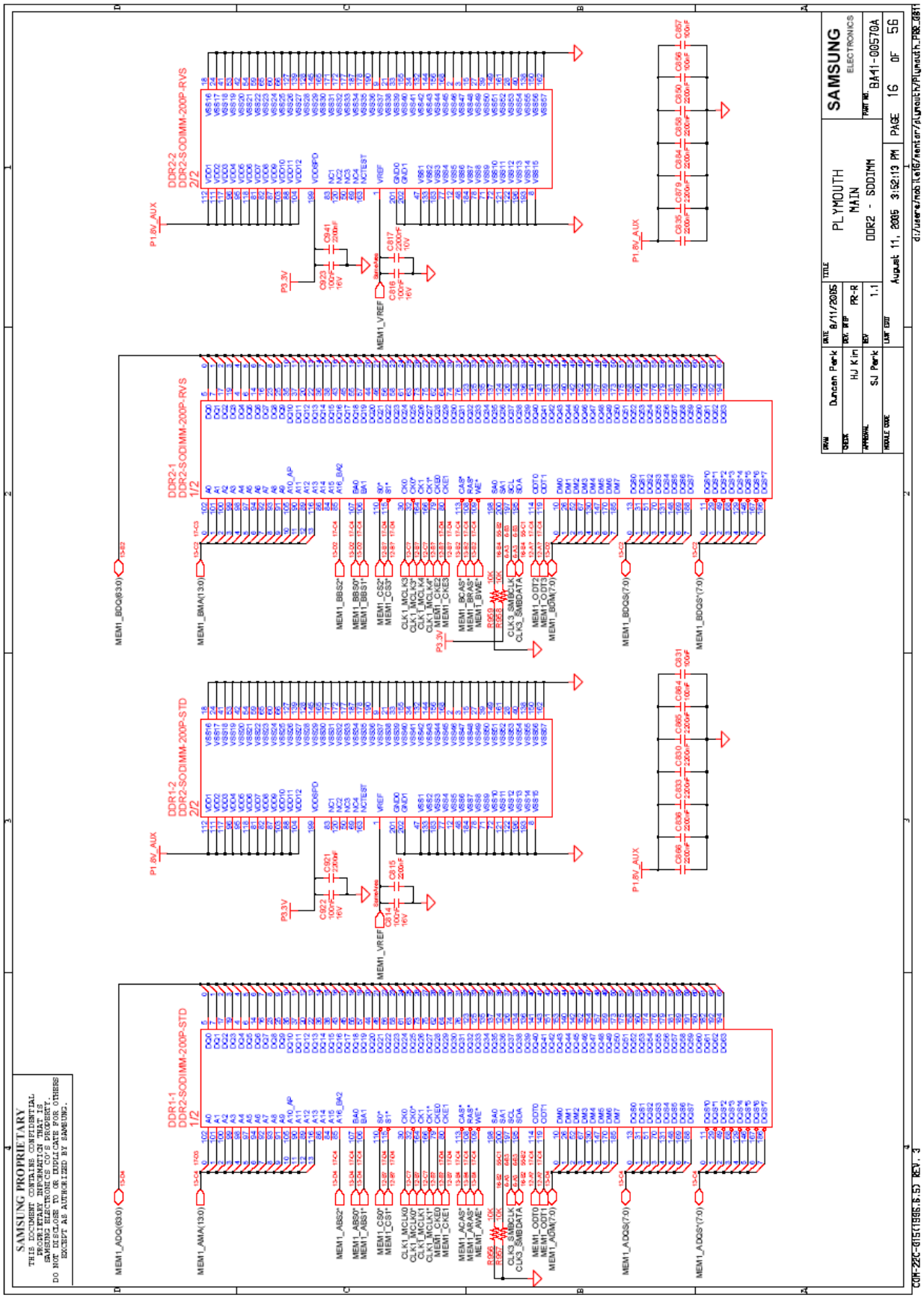
CHECK HJ Kim PR-R
APPROVAL SJ Park 1.1
MODULE CODE LAST EDIT August 11, 2005 3:52:13 PM
TITLE PLYMOUTH MAIN ALVISO-GMCH(5/5)
SAMSUNG ELECTRONICS
PART NO. BA41-00570A
PAGE 15 OF 56
d:/users/mobile6/rentar/plymouth/Plymouth.PRJ.dsn
COM-22C-015(1998.5.5) REV: 3

7. Schematic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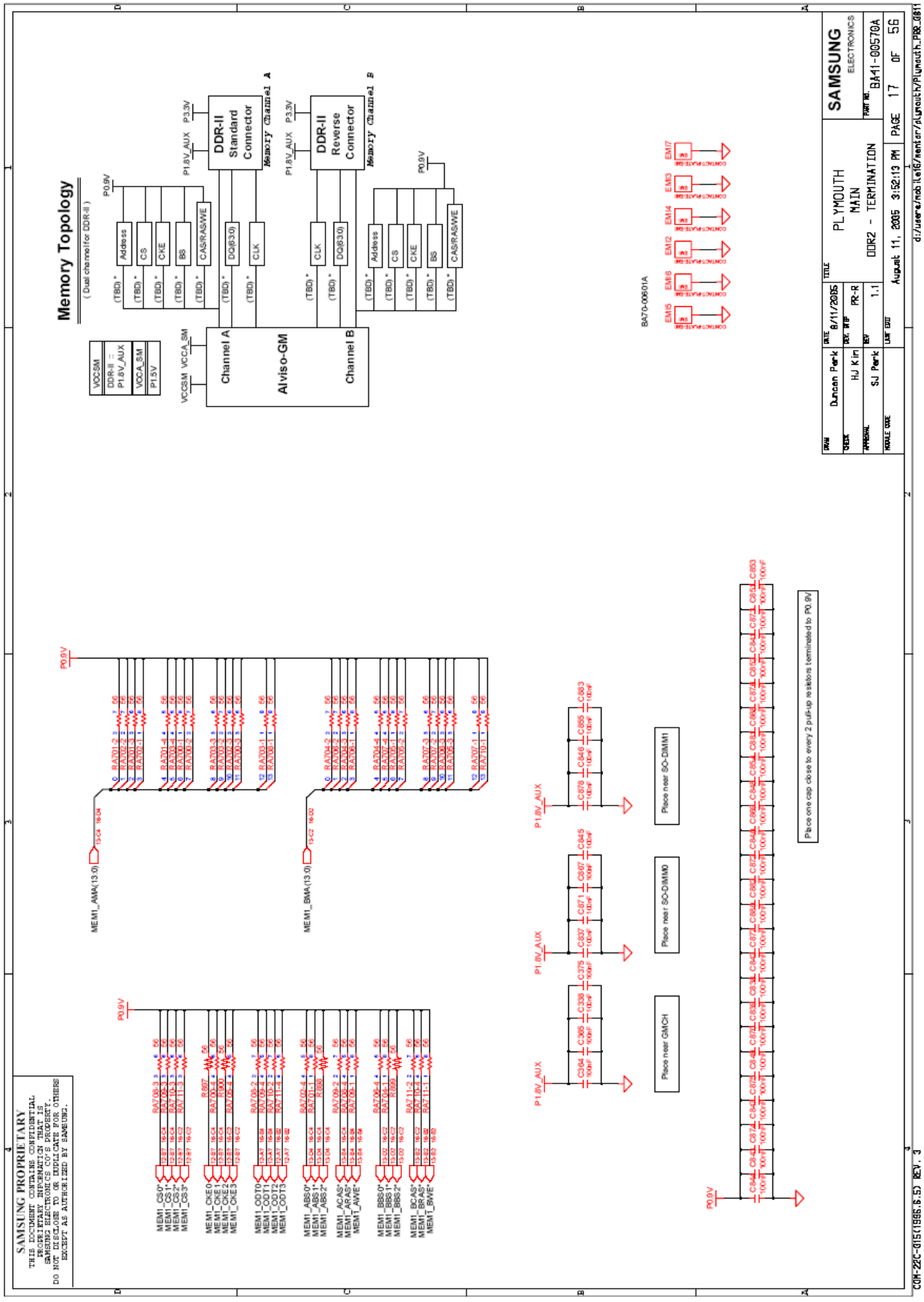
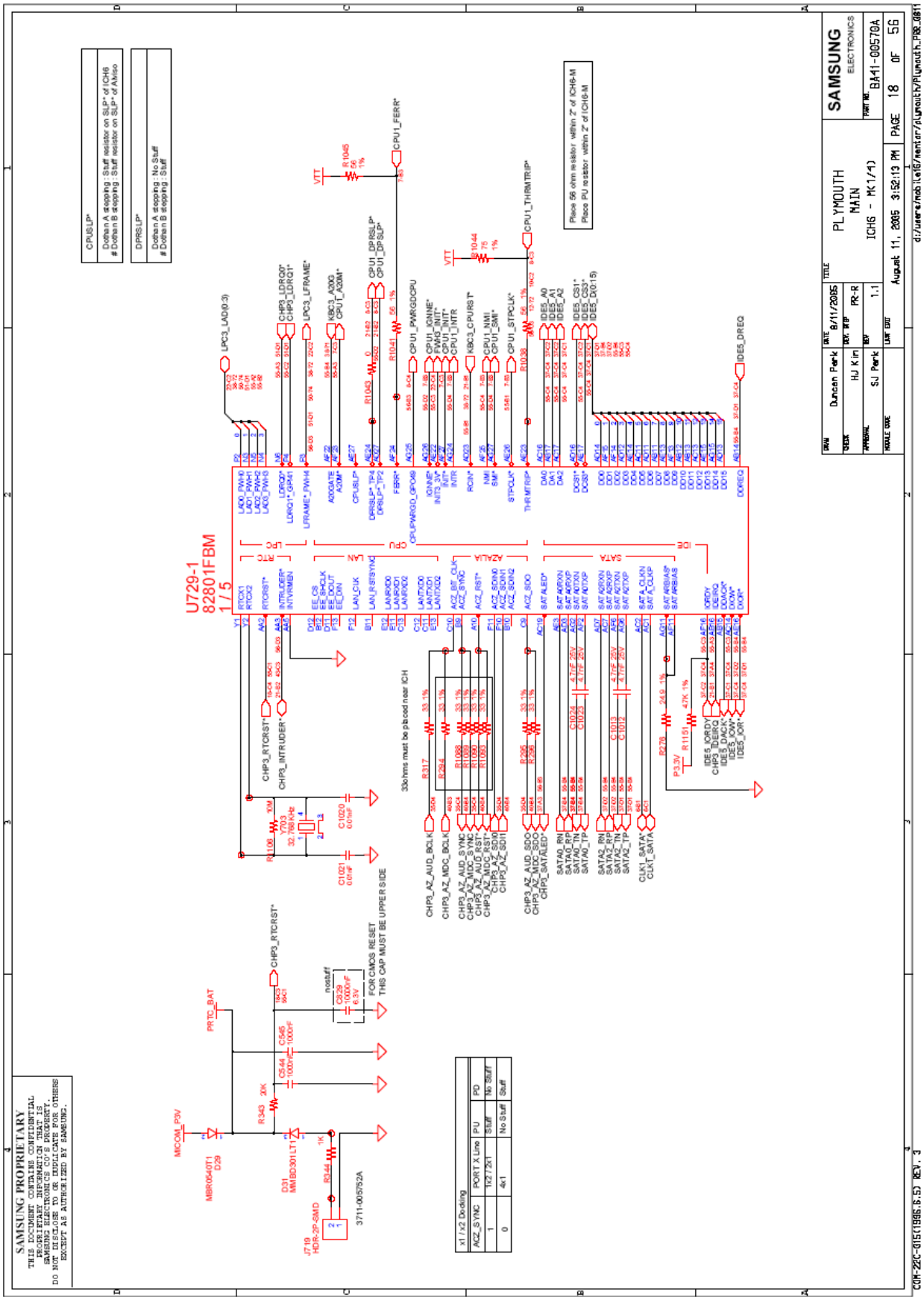
SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
DDR2 - SODIMM
BA41-00570A
PAGE 16 OF 56
August 11, 2005 3:52:13 PM
DDR1:1 DDR2-SODIMM-200P-STD 1/2
DDR1:2 DDR2-SODIMM-200P-STD 2/2
DDR2:1 DDR2-SODIMM-200P-RVS 1/2
DDR2:2 DDR2-SODIMM-200P-RVS 2/2
MEM1_ADQ(63:0)
MEM1_BDQ(63:0)
MEM1_AMA(13:0)
MEM1_BMA(13:0)
MEM1_ADQS(7:0)
MEM1_BDQS(7:0)
MEM1_VREF
P1.8V_AUX
P3.3V

7. Schematic


Memory Topology
(Dual channel for DDR-II)
DDR-II Standard Connector
DDR-II Reverse Connector
Memory Channel A
Memory Channel B
Channel A
Alviso-GM
Channel B
Address
CS
CKE
BS
CAS/RAS/WE
DQ(63:0)
CLK
SAMSUNG PROPRIETARY
PLYMOUTH
MAIN
DDR2 - TERMINATION
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 17 OF 56
Place near GMCH
Place near SO-DIMM0
Place near SO-DIMM1
Place one cap close to every 2 pull-up resistors terminated to P0.9V

7. Schematic


U729-1
82801FBM
1 / 5
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
ICH6 - M(1/4)
BA41-00570A
PAGE 18 OF 56
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SJ Park
8/11/2005
PR-R
1.1
CPUSLP*
DPRSLP*
Dothan A stepping : Stuff resistor on SLP* of ICH6
Dothan B stepping : Stuff resistor on SLP* of AMiso
Dothan A stepping : No Stuff
Dothan B stepping : Stuff
Place 56 ohm resistor within 2" of ICH6-M
Place PU resistor within 2" of ICH6-M
33ohms must be placed near ICH
FOR CMOS RESET
THIS CAP MUST BE UPPER SIDE
x1 / x2 Docking
ACZ_SYNC
PORT A Line
PU
PD
1x2 / 2x1
Stuff
No Stuff
4x1
No Stuff
Stuff
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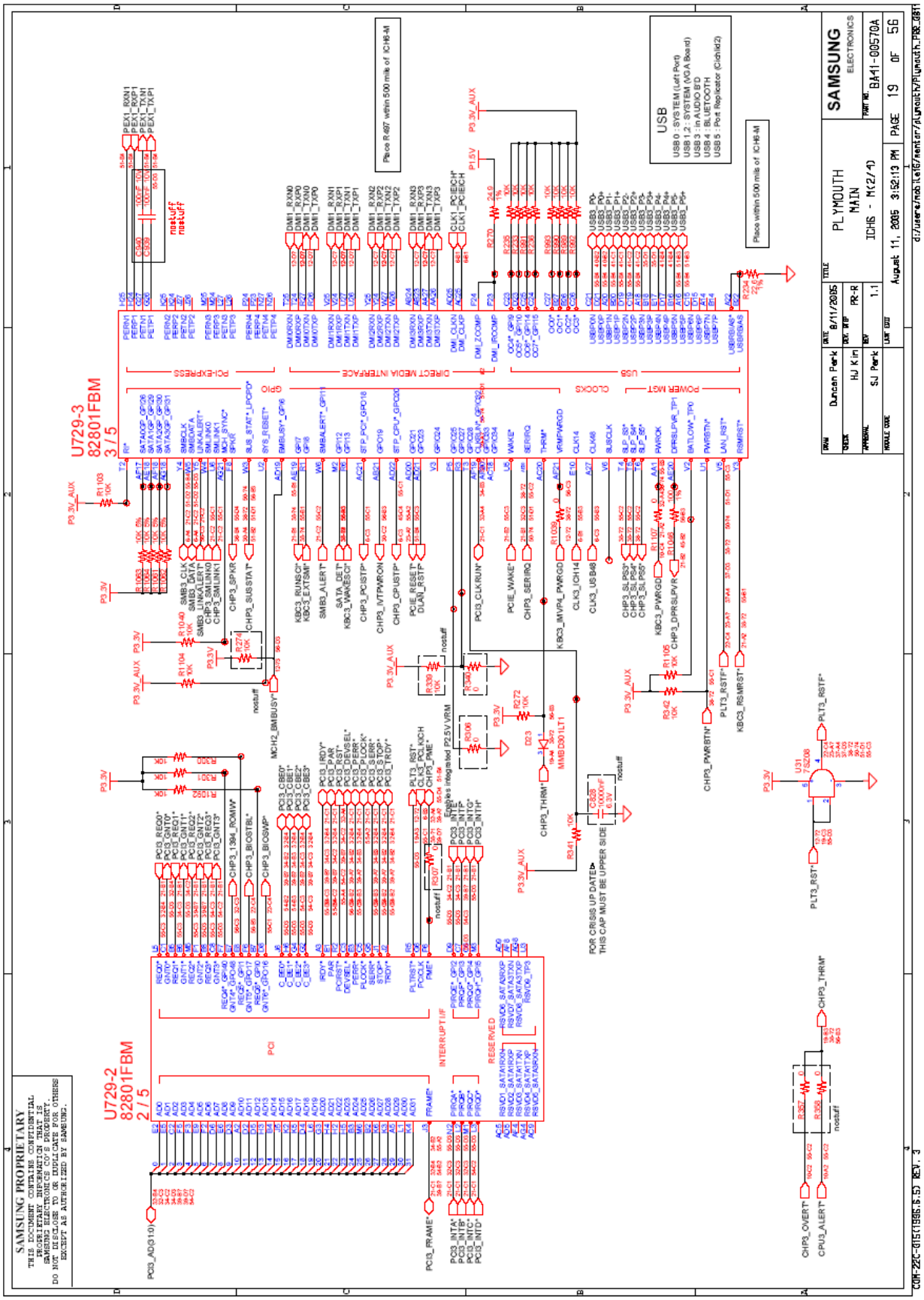
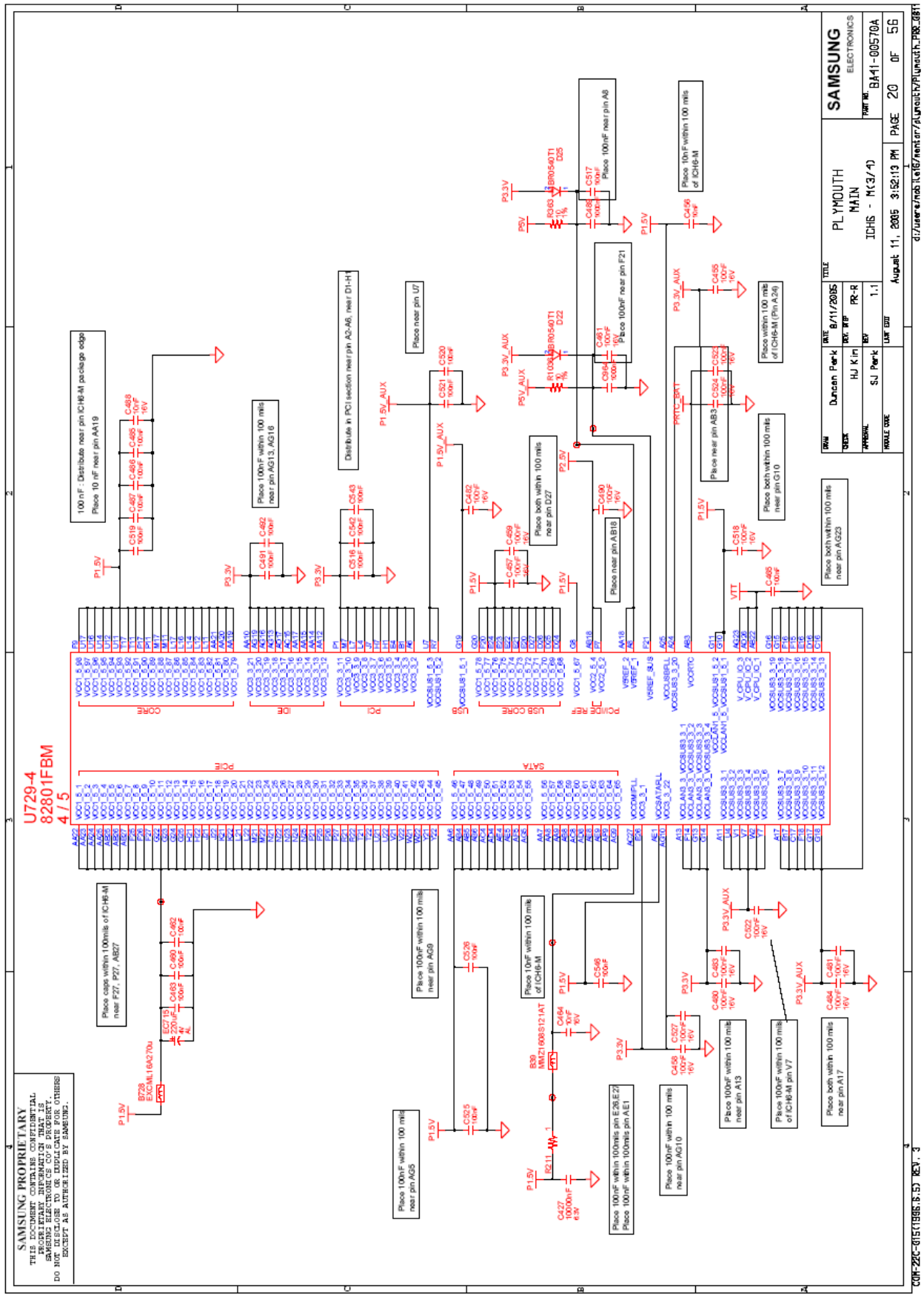
d:/users/mobile16/mentor/plymouth/Plymouth.PRR.1811

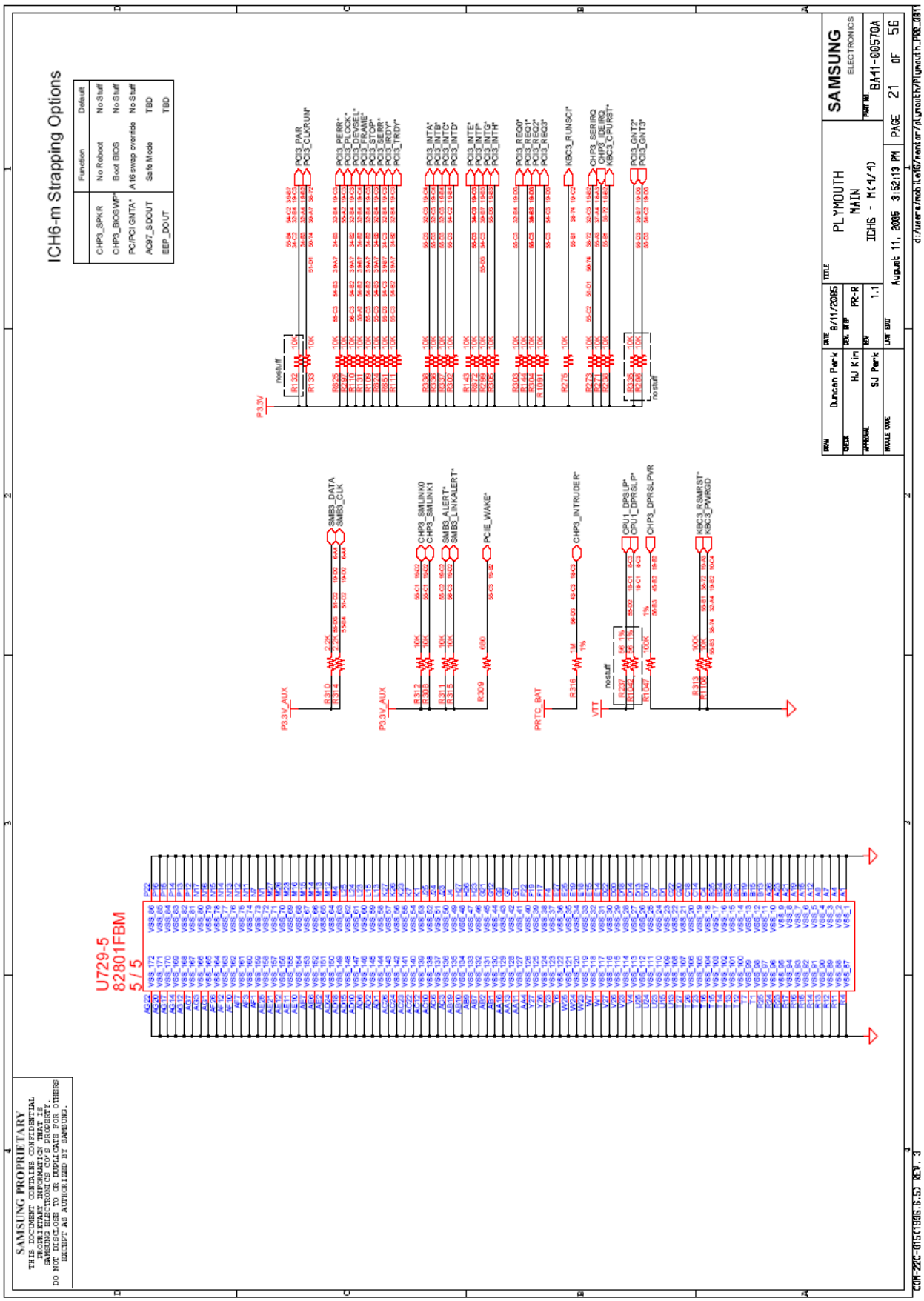
7. Schematic


U729-3
82801FBM
3/5
U729-2
82801FBM
2/5
SAMSUNG PROPRIETARY
PLYMOUTH
MAIN
SAMSUNG
ELECTRONICS
August 11, 2005 3:52:13 PM
PAGE 19 OF 56
BA41-00570A
USB
USB 0 : SYSTEM (Left Port)
USB 1,2 : SYSTEM (I/O A Board)
USB 3 : In AUDIO B'D
USB 4 : BLUETOOTH
USB 5 : Port Replicator (Cichlid2)
Place R497 within 500 mils of ICH6-M
Place within 500 mils of ICH6-M
PCI
INTERRUPT I/F
RESERVED
POWER MGT
CLOCKS
DIRECT MEDIA INTERFACE
PCI-EXPRESS
GPIO

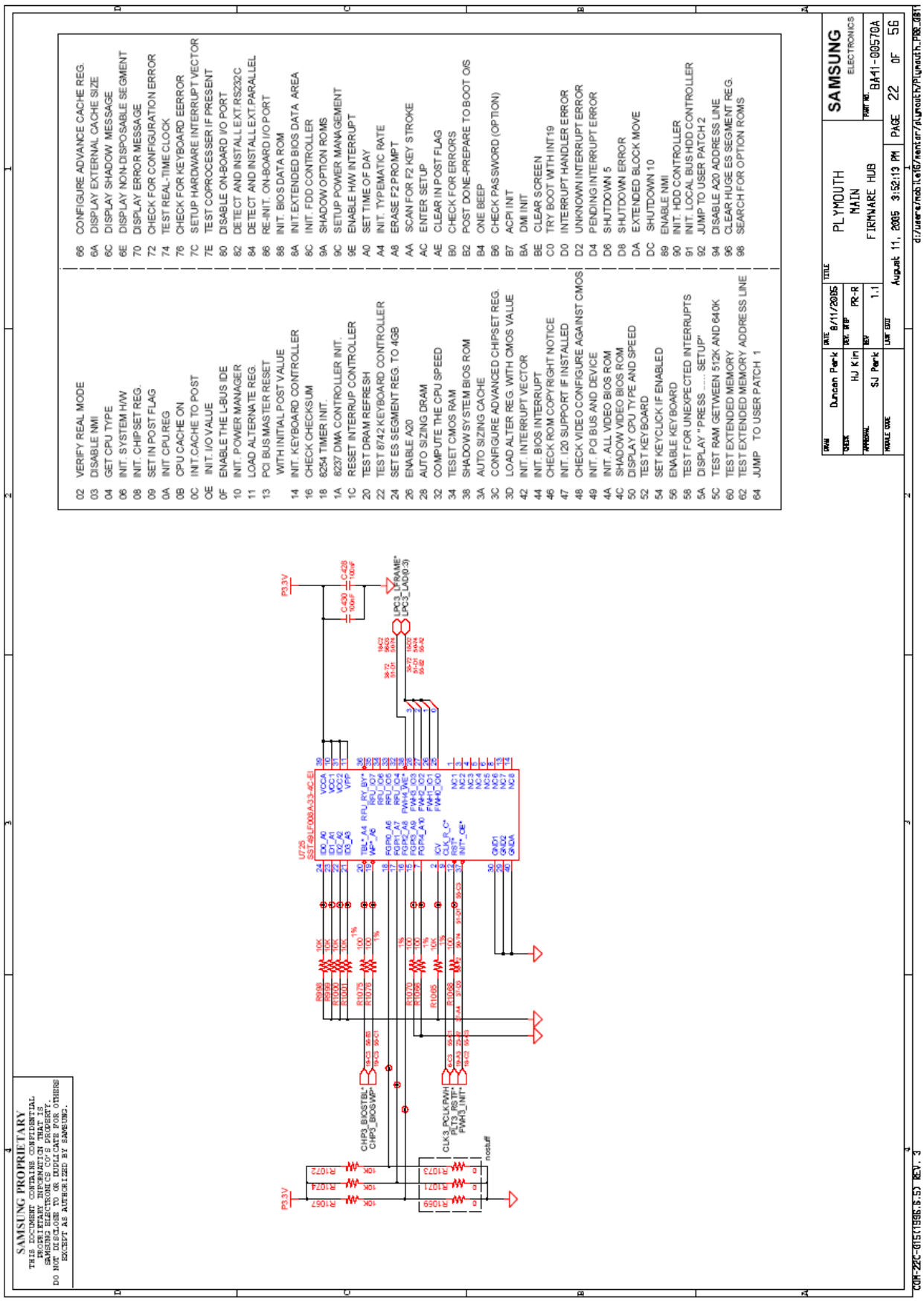
7. Schematic


U729-4
82801FBM
4/5
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
ICH6 - M(3/4)
BA41-00570A
PAGE 20 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
Place cap within 100mils of ICH6-M near F27, P27, AB27
Place 100nF within 100 mils near pin AG9
Place 100nF within 100 mils near pin AG5
Place 10nF within 100 mils of ICH6-M
Place 100nF within 100mils pin E26,E27 Place 100nF within 100mils pin AE1
Place 100nF within 100 mils near pin AG10
Place 100nF within 100 mils near pin A13
Place 100nF within 100 mils of ICH6-M pin V7
Place both within 100 mils near pin A17
Place both within 100 mils near pin A23
Place near pin AB3
Place near pin AB18
Place both within 100 mils near pin G10
Place within 100 mils of ICH6-M (Pin A24)
Place 10nF within 100 mils of ICH6-M
Place 100nF near pin A8
Place 100nF near pin F21
Place near pin U7
Distribute in PCI section near pin A2-A6, near D1-H1
Place 100nF within 100 mils near pin AG13, AG18
100 nF : Distribute near pin ICH6-M package edge
Place 10 nF near pin AA19
P1.5V
P3.3V
P5V
P3.3V_AUX
P5V_AUX
P1.5V_AUX
P2.5V
VTT
PRTC_BAT
CORE
IDE
PCI
USB
USB CORE
PCIMDE REF
PCIE
SATA

7. Schematic


ICH6-m Strapping Options
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
ICH6 - M(1/4)
August 11, 2005 3:52:13 PM
PAGE 21 OF 56
U729-5
82801FBM
5/5

7. Schematic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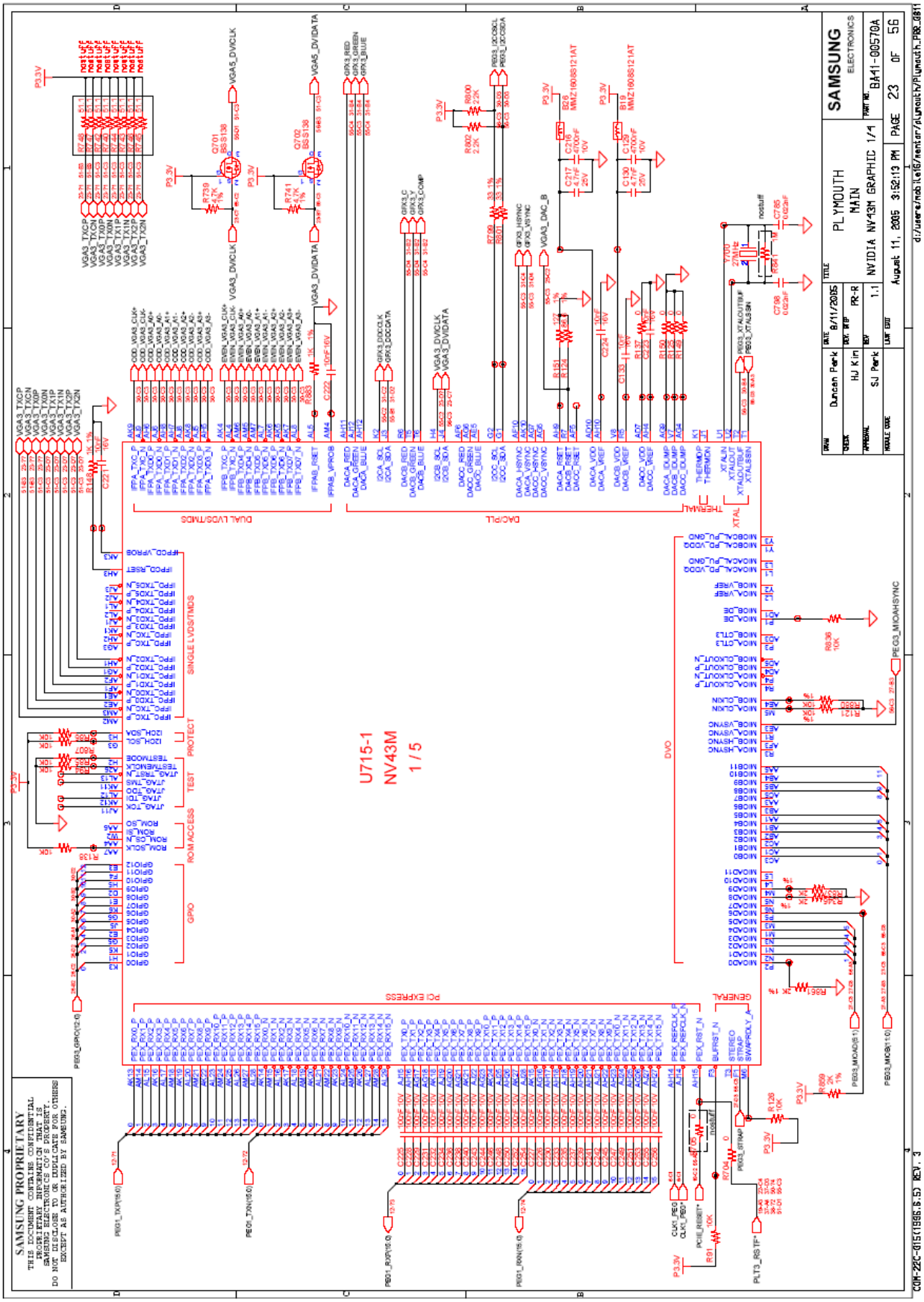
02 VERIFY REAL MODE
03 DISABLE NMI
04 GET CPU TYPE
06 INIT. SYSTEM H/W
08 INIT. CHIPSET REG.
09 SET IN POST FLAG
0A INIT CPU REG
0B CPU CACHE ON
0C INIT.CACHE TO POST
0E INIT. I/O VALUE
0F ENABLE THE L-BUS IDE
10 INIT. POWER MANAGER
11 LOAD ALTERNATE REG.
13 PCI BUS MASTER RESET
WITH INITIAL POST VALUE
14 INIT. KEYBOARD CONTROLLER
16 CHECK CHECKSUM
18 8254 TIMER INIT.
1A 8237 DMA CONTROLLER INIT.
1C RESET INTERRUP CONTROLLER
20 TEST DRAM REFRESH
22 TEST 8742 KEYBOARD CONTROLLER
24 SET ES SEGMENT REG. TO 4GB
26 ENABLE A20
28 AUTO SIZING DRAM
32 COMPUTE THE CPU SPEED
34 TESET CMOS RAM
38 SHADOW SYSTEM BIOS ROM
3A AUTO SIZING CACHE
3C CONFIGURE ADVANCED CHIPSET REG.
3D LOAD ALTER REG. WITH CMOS VALUE
42 INIT. INTERRUPT VECTOR
44 INIT. BIOS INTERRUPT.
46 CHECK ROM COPYRIGHT NOTICE
47 INIT. I20 SUPPORT IF INSTALLED
48 CHECK VIDEO CONFIGURE AGAINST CMOS
49 INIT. PCI BUS AND DEVICE
4A INIT. ALL VIDEO BIOS ROM
4C SHADOW VIDEO BIOS ROM
50 DISPLAY CPU TYPE AND SPEED
52 TEST KEYBOARD
54 SET KEYCLICK IF ENABLED
56 ENABLE KEYBOARD
58 TEST FOR UNEXPECTED INTERRUPTS
5A DISPLAY " PRESS ..... SETUP"
5C TEST RAM GETWEEN 512K AND 640K
60 TEST EXTENDED MEMORY
62 TEST EXTENDED MEMORY ADDRESS LINE
64 JUMP TO USER PATCH 1
66 CONFIGURE ADVANCE CACHE REG.
6A DISPLAY EXTERNAL CACHE SIZE
6C DISPLAY SHADOW MESSAGE
6E DISPLAY NON-DISPOSABLE SEGMENT
70 DISPLAY ERROR MESSAGE
72 CHECK FOR CONFIGURATION ERROR
74 TEST REAL-TIME CLOCK
76 CHECK FOR KEYBOARD EERROR
7C SETUP HARDWARE INTERRUPT VECTOR
7E TEST COPROCESSER IF PRESENT
80 DISABLE ON-BOARD I/O PORT
82 DETECT AND INSTALL EXT.RS232C
84 DETECT AND INSTALL EXT.PARALLEL
86 RE-INIT. ON-BOARD I/O PORT
88 INIT. BIOS DATA ROM
8A INIT.EXTENDED BIOS DATA AREA
8C INIT. FDD CONTROLLER
9A SHADOW OPTION ROMS
9C SETUP POWER MANAGEMENT
9E ENABLE H/W INTERRUPT
A0 SET TIME OF DAY
A4 INIT. TYPEMATIC RATE
A8 ERASE F2 PROMPT
AA SCAN FOR F2 KEY STROKE
AC ENTER SETUP
AE CLEAR IN POST FLAG
B0 CHECK FOR ERRORS
B2 POST DONE-PREPARE TO BOOT O/S
B4 ONE BEEP
B6 CHECK PASSWORD (OPTION)
B7 ACPI INIT
BA DMI INIT
BE CLEAR SCREEN
C0 TRY BOOT WITH INT19
D0 INTERRUPT HANDLER ERROR
D2 UNKNOWN INTERRUPT ERROR
D4 PENDING INTERRUPT ERROR
D6 SHUTDOWN 5
D8 SHUTDOWN ERROR
DA EXTENDED BLOCK MOVE
DC SHUTDOWN 10
89 ENABLE NMI
90 INIT. HDD CONTROLLER
91 INIT. LOCAL BUS HDD CONTROLLER
92 JUMP TO USER PATCH 2
94 DISABLE A20 ADDRESS LINE
96 CLEAR HUGE ES SEGMENT REG.
98 SEARCH FOR OPTION ROMS
DRAWN Duncan Park 8/11/2005
CHECK HJ Kim PR-R
APPROVAL SJ Park 1.1
MODULE CODE
TITLE PLYMOUTH MAIN FIRMWARE HUB
SAMSUNG ELECTRONICS
PART NO. BA41-00570A
PAGE 22 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile6/mentor/plymouth/Plymouth.PRJ.DBK
COM-22C-01501986.B.5D REV. 3

7. Schematic


SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
NVIDIA NV43M GRAPHIC 1/4
BA41-00570A
PAGE 23 OF 56
August 11, 2005 3:52:13 PM
U715-1
NV43M
1 / 5
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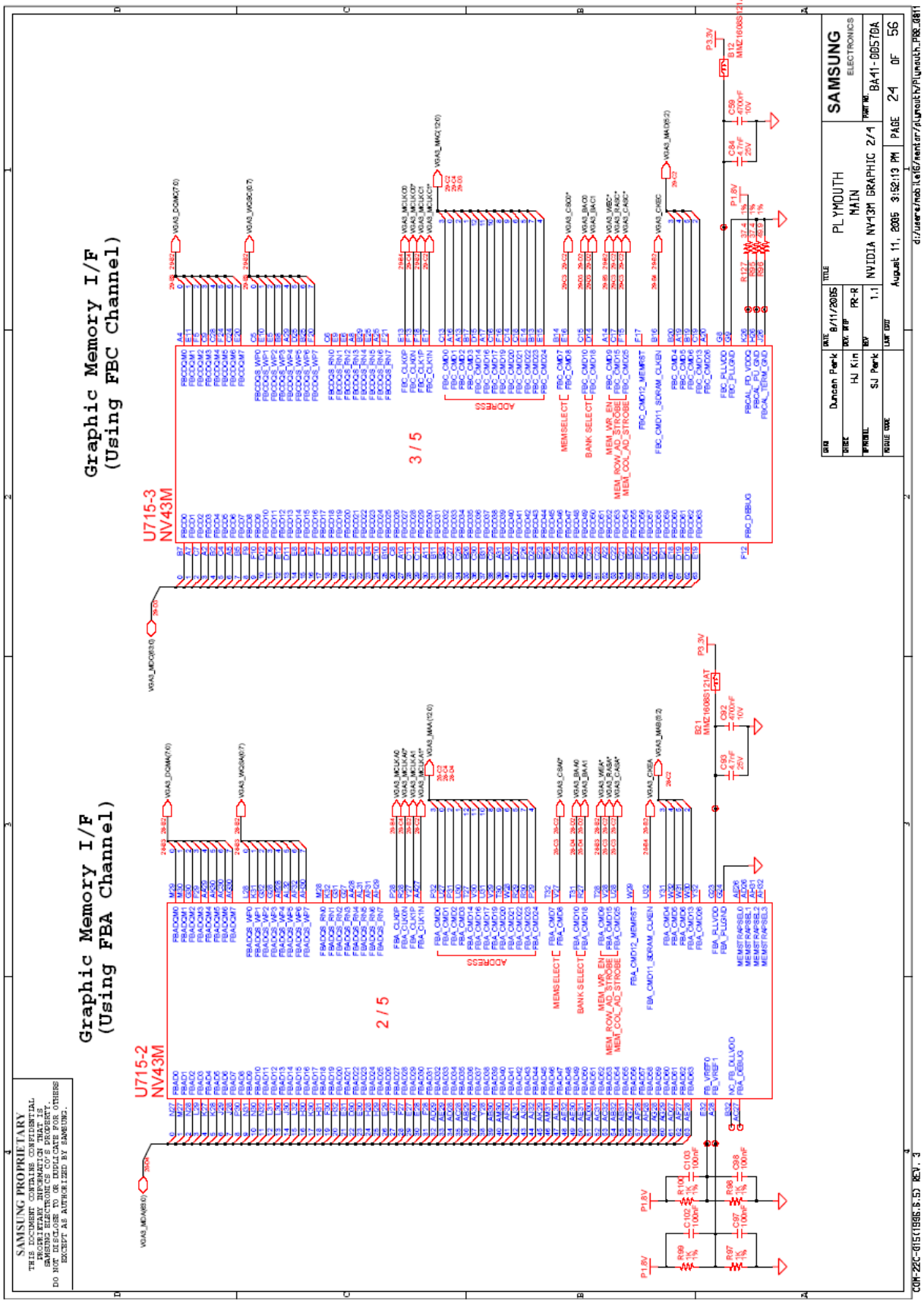
7. Schematic


Graphic Memory I/F
(Using FBA Channel)
U715-2
NV43M
2 / 5
Graphic Memory I/F
(Using FBC Channel)
U715-3
NV43M
3 / 5
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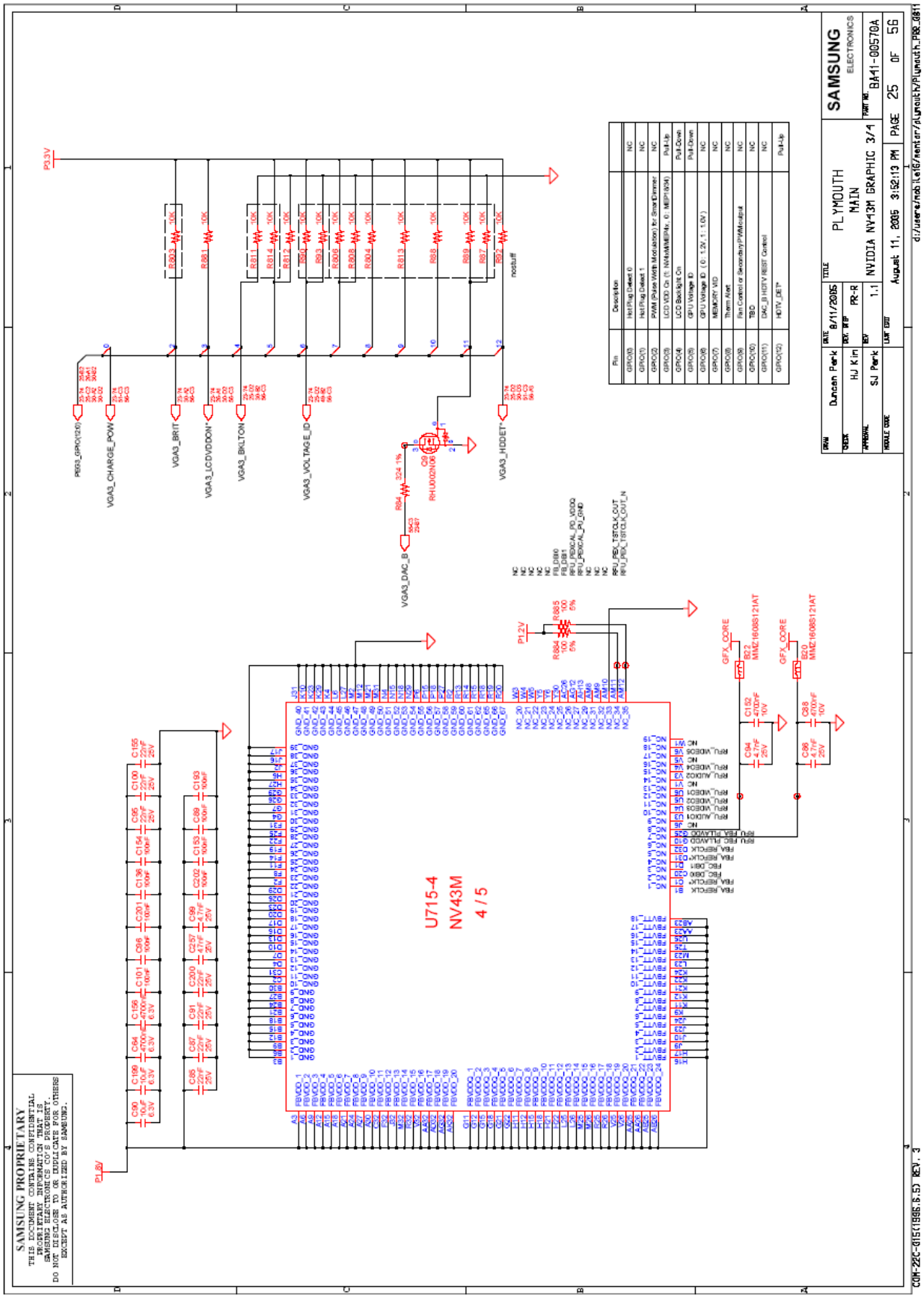
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
NVIDIA NV43M GRAPHIC 2/4
BA41-00570A
PAGE 24 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1

7. Schematic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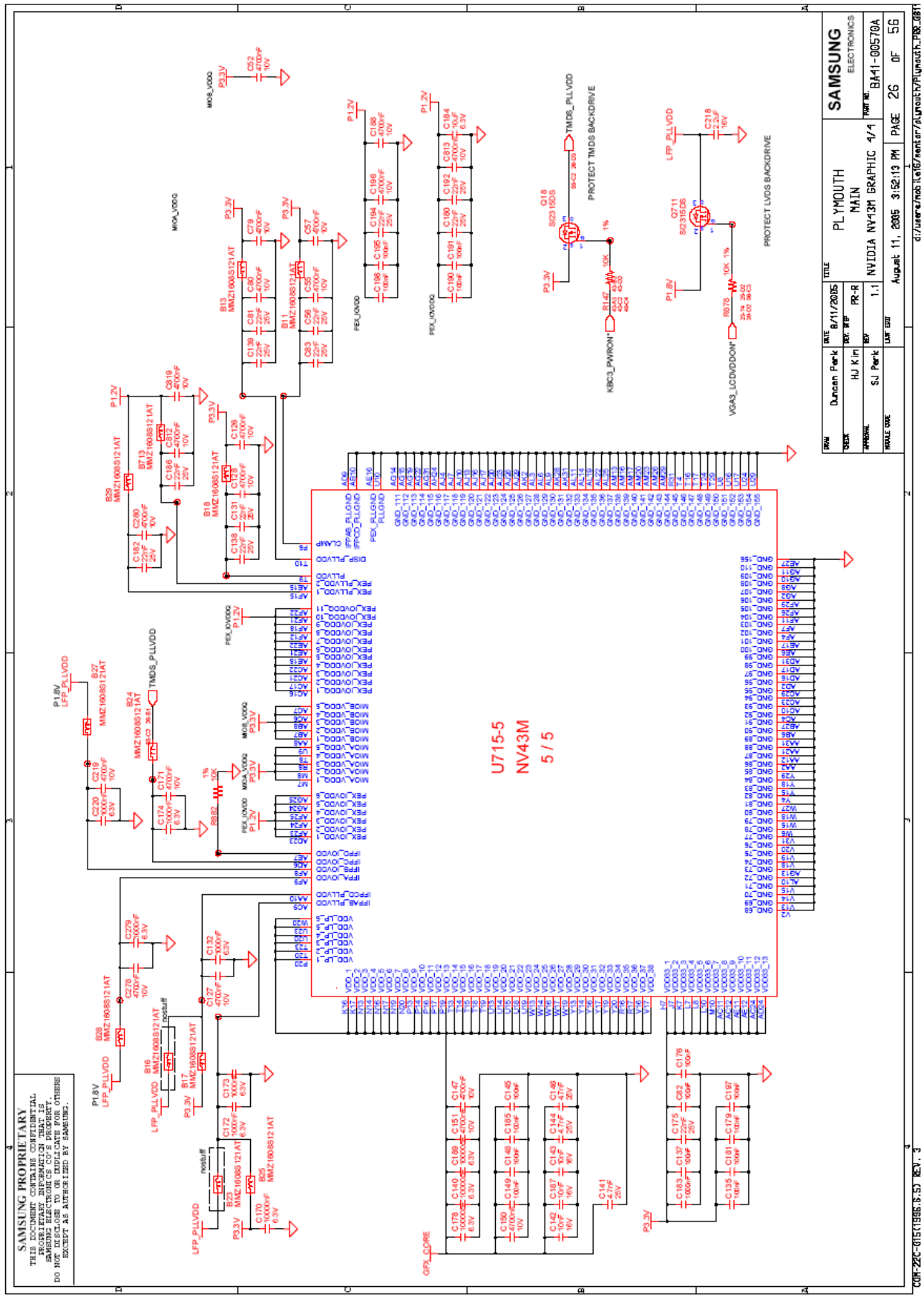
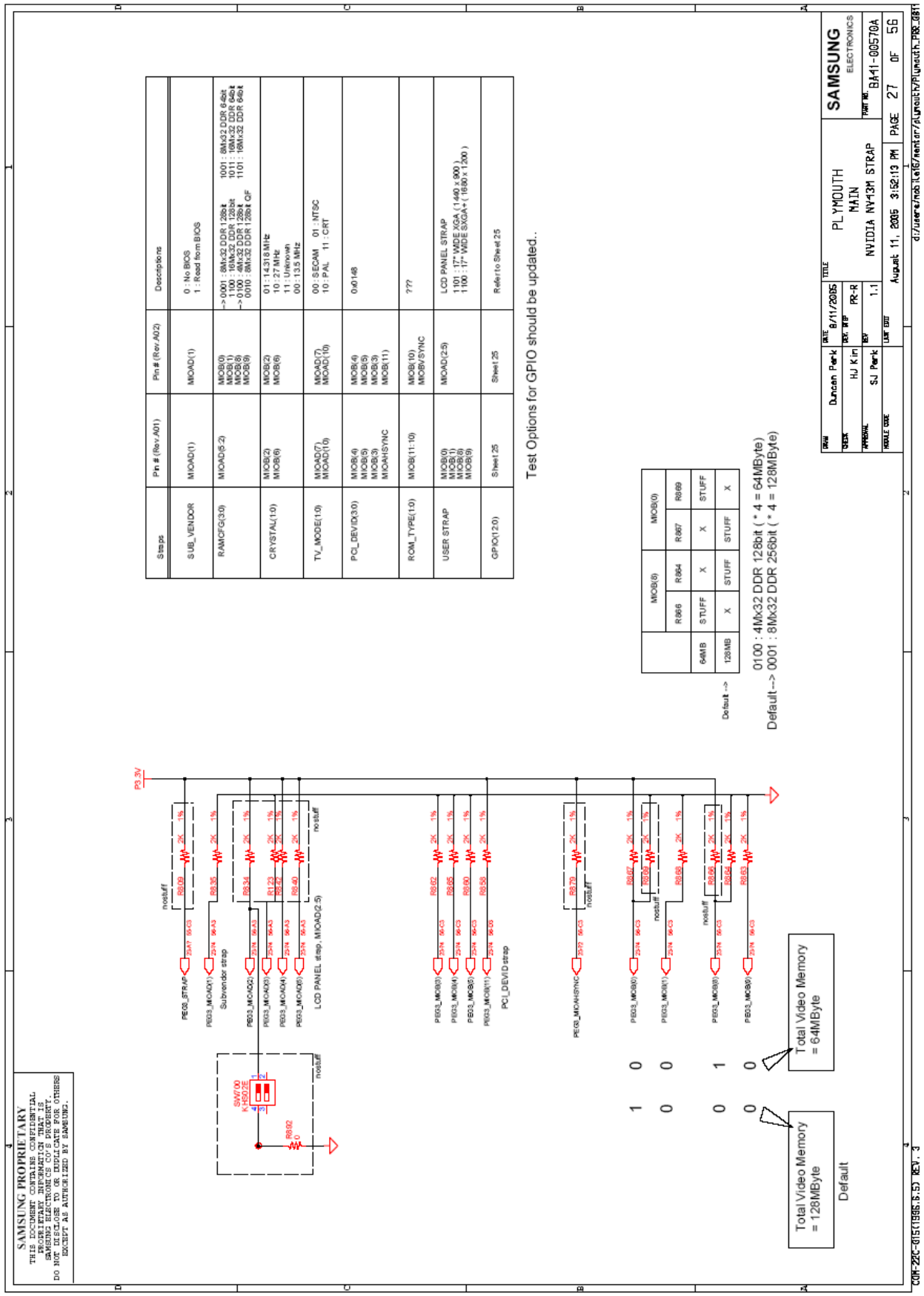
U715-4
NV43M
4 / 5
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
NVIDIA NV43M GRAPHIC 3/4
BA41-00570A
PAGE 25 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile6/kentaro/Plymouth/Plymouth_PRR_2811
Duncan Park 8/11/2005
HJ Kim PR-R
SJ Park 1.1
VGA3_CHARGE_POW
VGA3_BRIT
VGA3_LCDVDDON*
VGA3_BKLTON
VGA3_VOLTAGE_ID
VGA3_HDDET*
VGA3_DAC_B
GFX_CORE
GFX_CORE
P3.3V
P1.8V
P1.2V

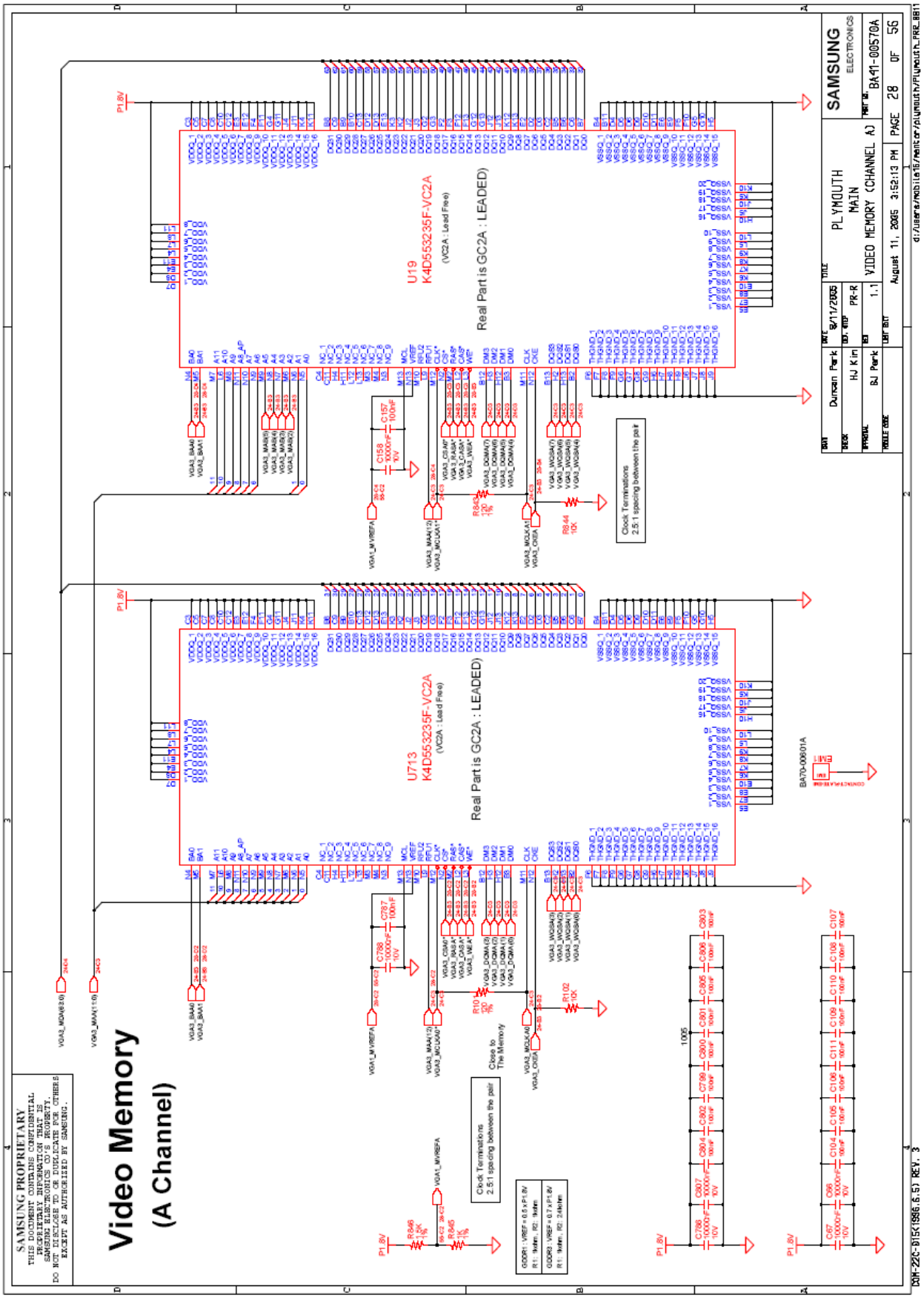
7. Schematic


U715-5
NV43M
5 / 5
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
NVIDIA NV43M GRAPHIC 4/4
BA41-00570A
PAGE 26 OF 56
August 11, 2005 3:52:13 PM
SAMSUNG PROPRIETARY
PROTECT TMDS BACKDRIVE
PROTECT LVDS BACKDRIVE

7. Schematic


Test Options for GPIO should be updated..
Default --> 0001 : 8Mx32 DDR 256bit (* 4 = 128MByte)
0100 : 4Mx32 DDR 128bit (* 4 = 64MByte)
Total Video Memory = 64MByte
Total Video Memory = 128MByte
Default
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
NVIDIA NV43M STRAP
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 27 OF 56

7. Schematic


Video Memory
(A Channel)
U19
K4D553235F-VC2A
(VC2A : Lead Free)
Real Part is GC2A : LEADED)
U713
K4D553235F-VC2A
(VC2A : Lead Free)
Real Part is GC2A : LEADED)
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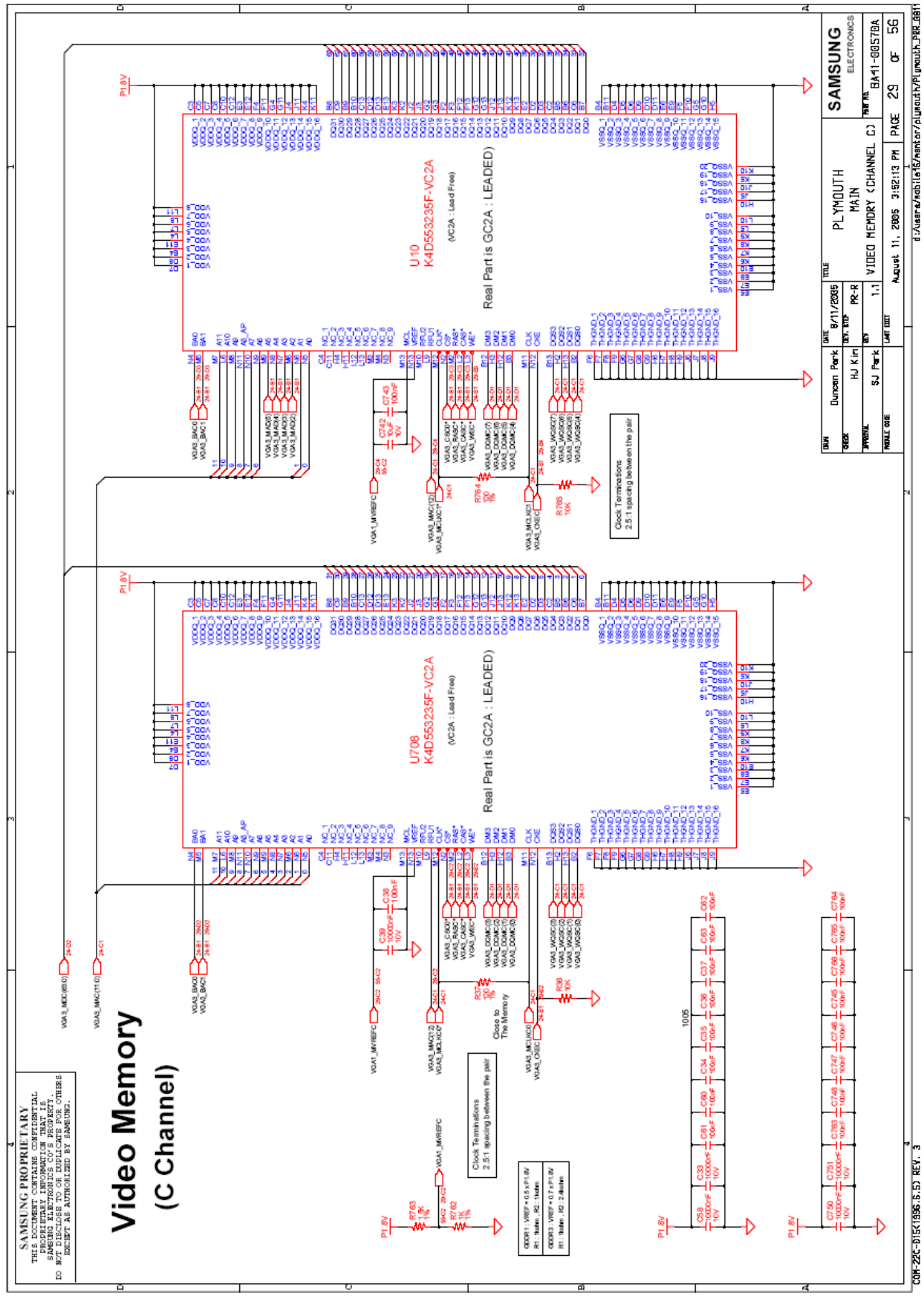
Clock Terminations
2.5:1 spacing between the pair
Close to
The Memory
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
VIDEO MEMORY (CHANNEL A)
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 28 OF 56

7. Schematic


Video Memory
(C Channel)
U10
K4D553235F-VC2A
(VC2A : Lead Free)
Real Part is GC2A : LEADED
U708
K4D553235F-VC2A
(VC2A : Lead Free)
Real Part is GC2A : LEADED
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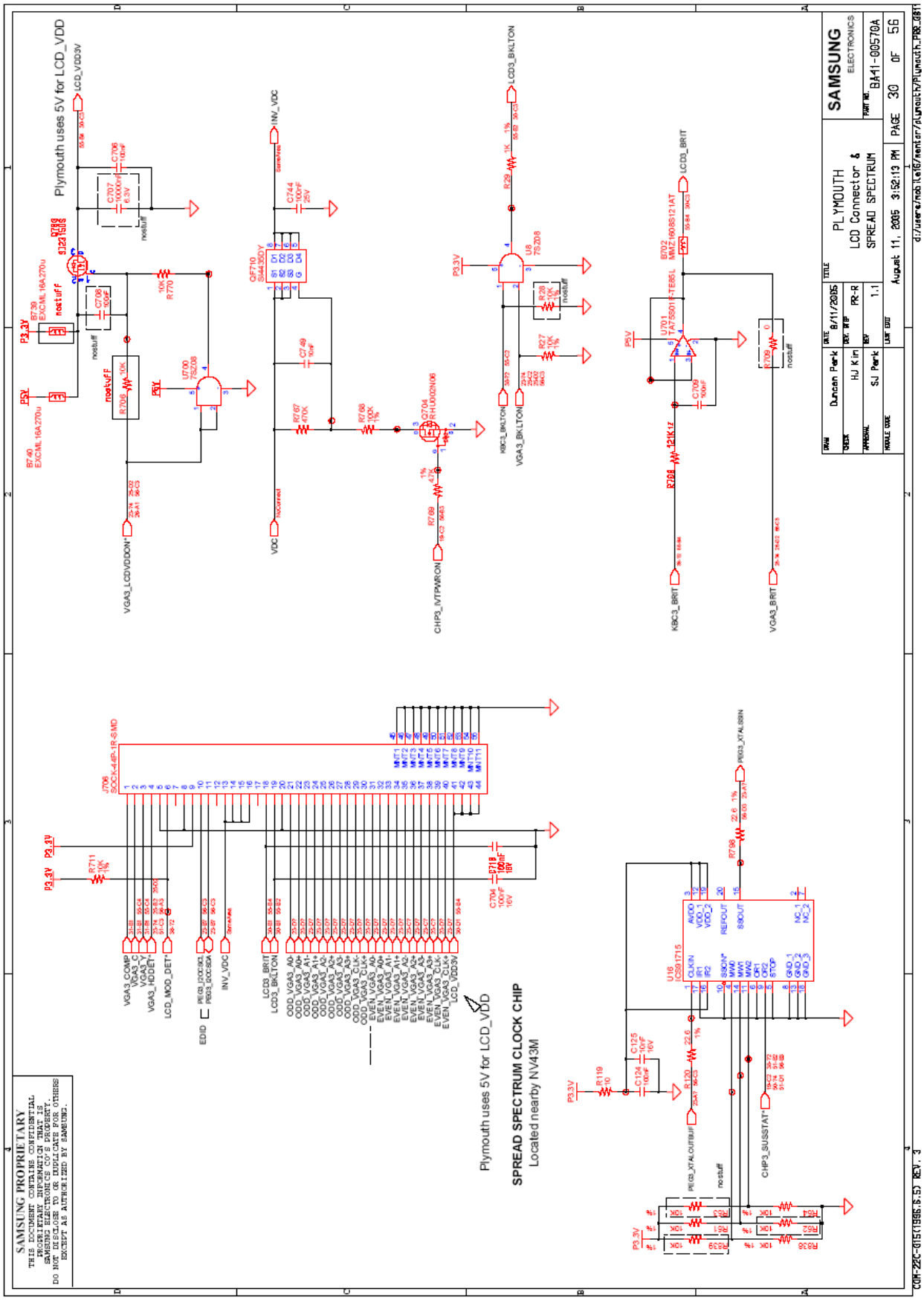
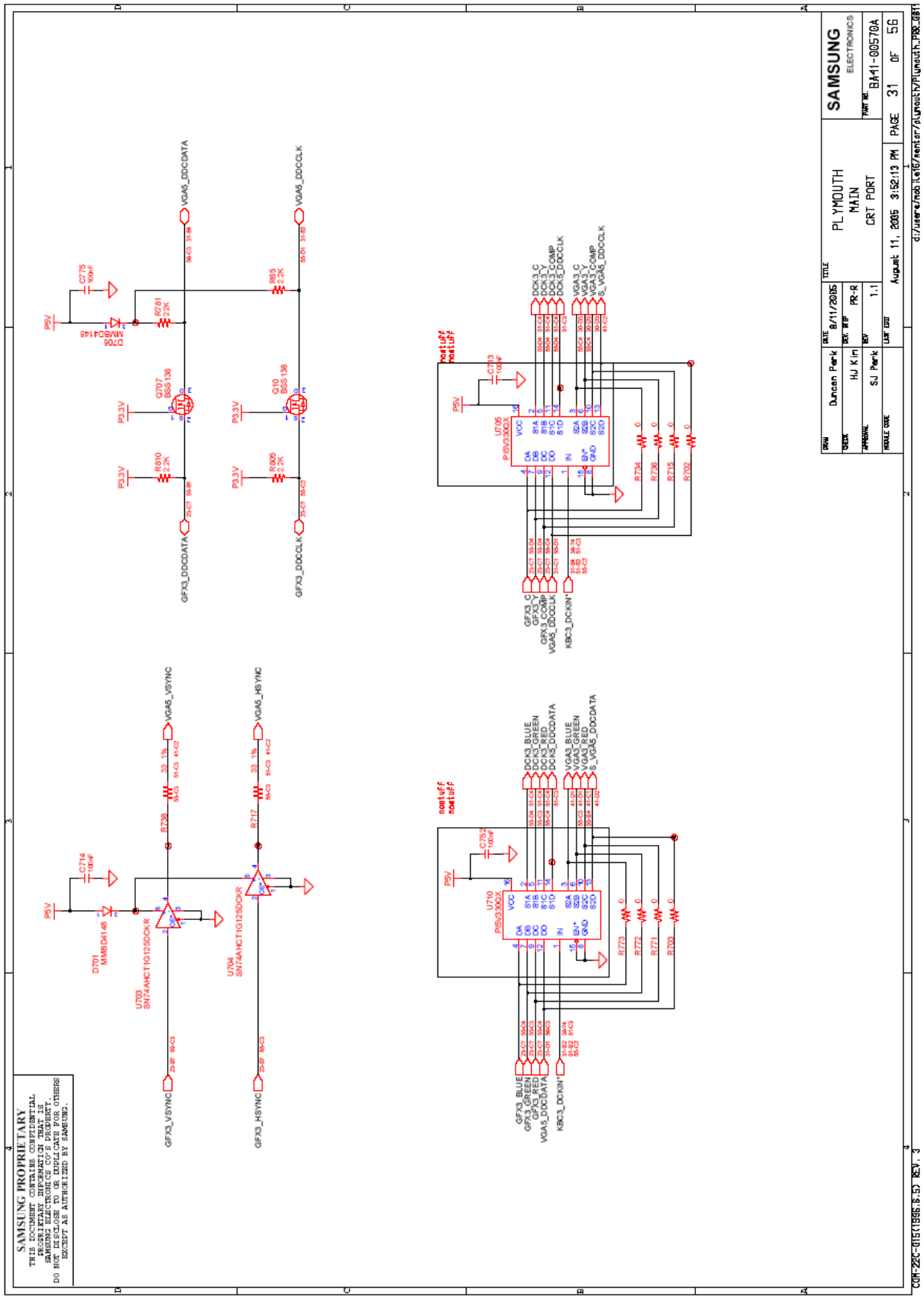
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
VIDEO MEMORY (CHANNEL C)
BA41-00857DA
PAGE 29 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
Clock Terminations
2.5:1 spacing between the pair
Close to
The Memory
Clock Terminations
2.5:1 spacing between the pair

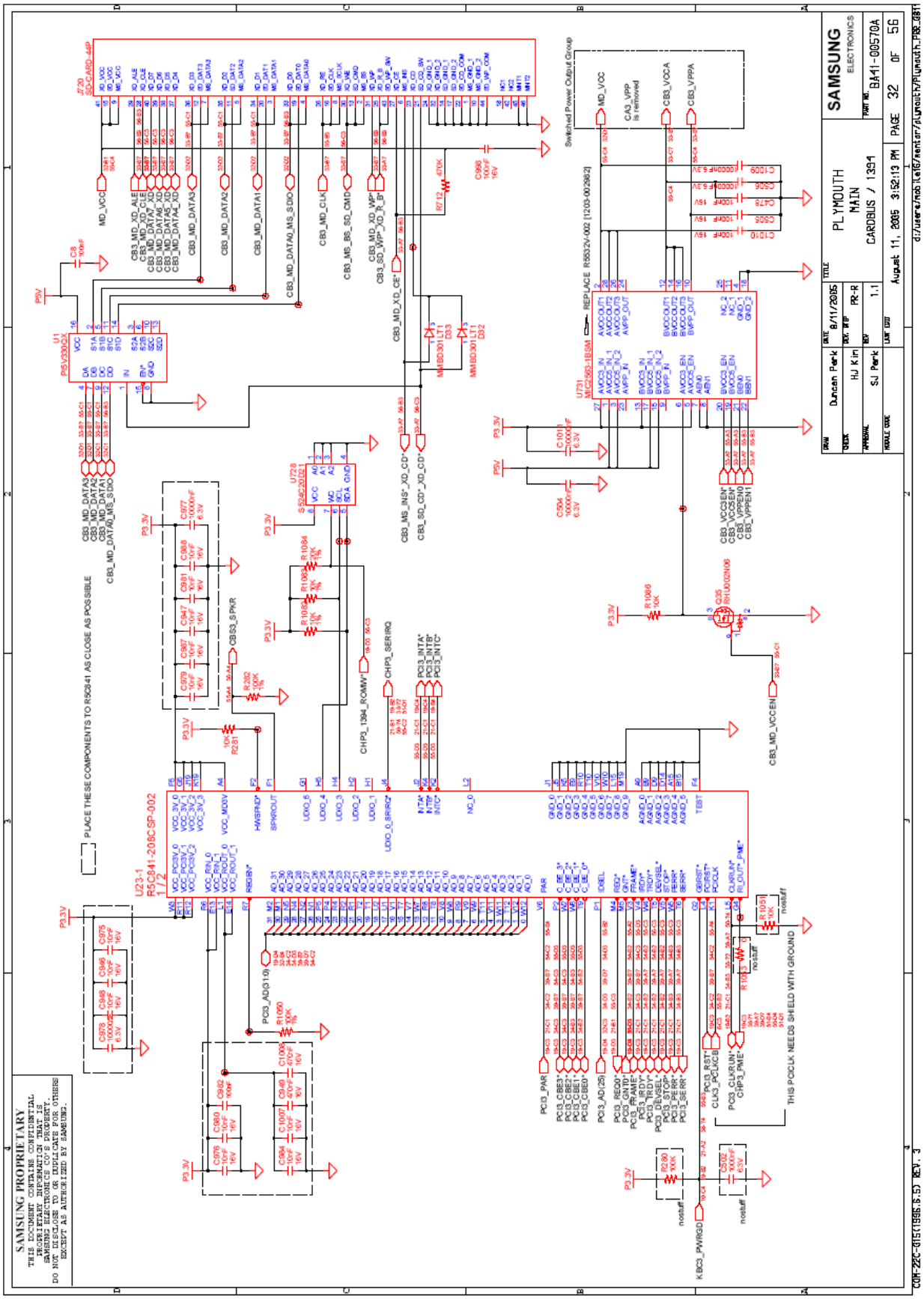
7. Schematic


Plymouth uses 5V for LCD_VDD
SPREAD SPECTRUM CLOCK CHIP
Located nearby NV43M
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
LCD Connector &
SPREAD SPECTRUM
August 11, 2005 3:52:13 PM
PAGE 30 OF 56

7. Schematic


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
CRT PORT
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 31 OF 56

7. Schematic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PLYMOUTH MAIN CARDBUS / 1394
PART NO. BA41-00570A
PAGE 32 OF 56
DRAW Duncan Park 8/11/2005
CHECK HJ Kim FR-R
APPROVAL SJ Park 1.1
August 11, 2005 3:52:13 PM
d:/users/mobile6/mentor/plymouth/PLYmouth.PRJ
PLACE THESE COMPONENTS TO R5C841 AS CLOSE AS POSSIBLE
U23-1 R5C841-206CSP-002 1/2
Switched Power Output Group
REPLACE R5632V-002 [1203-002982]
THIS PCICLK NEEDS SHIELD WITH GROUND

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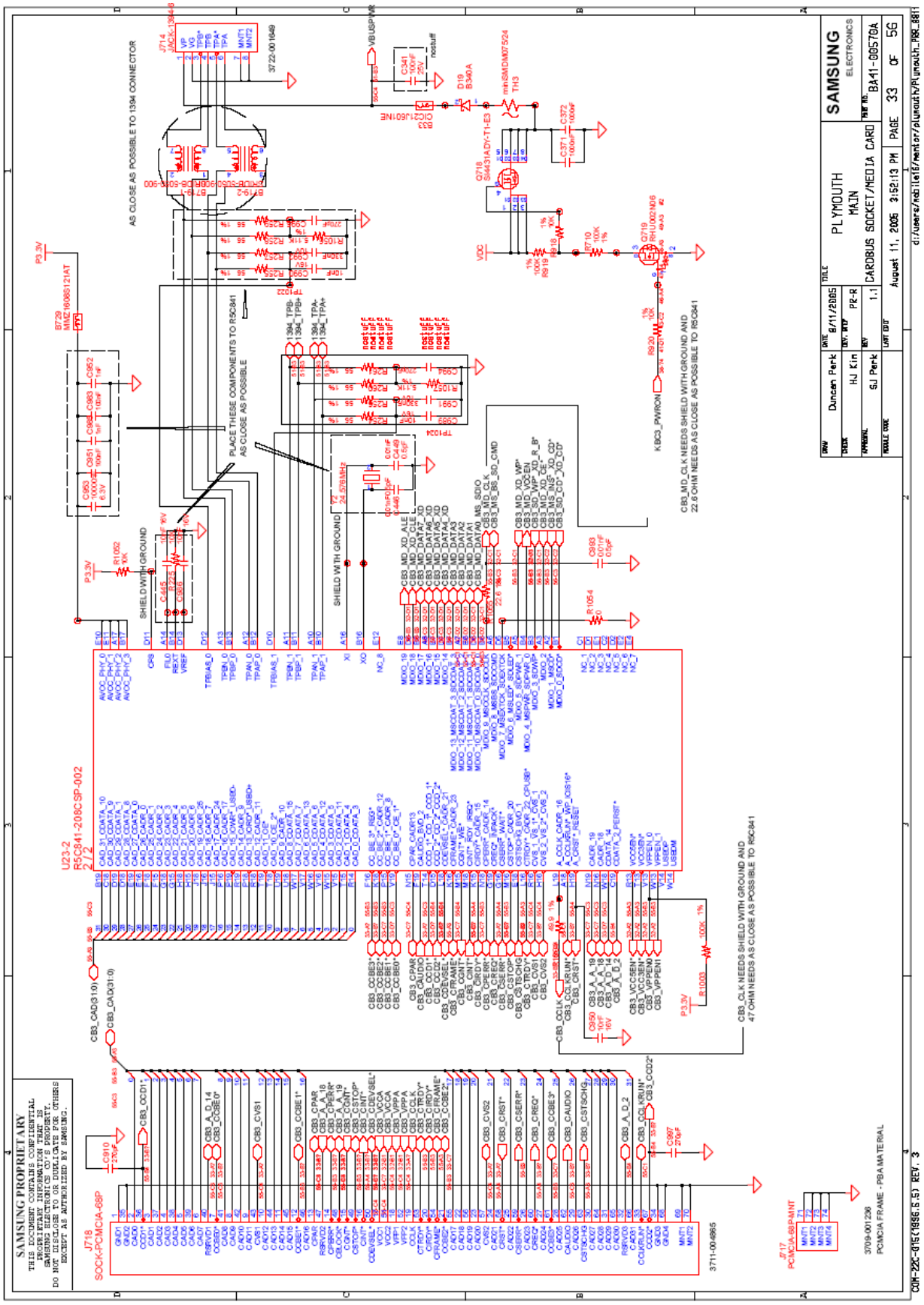
7. Schematic



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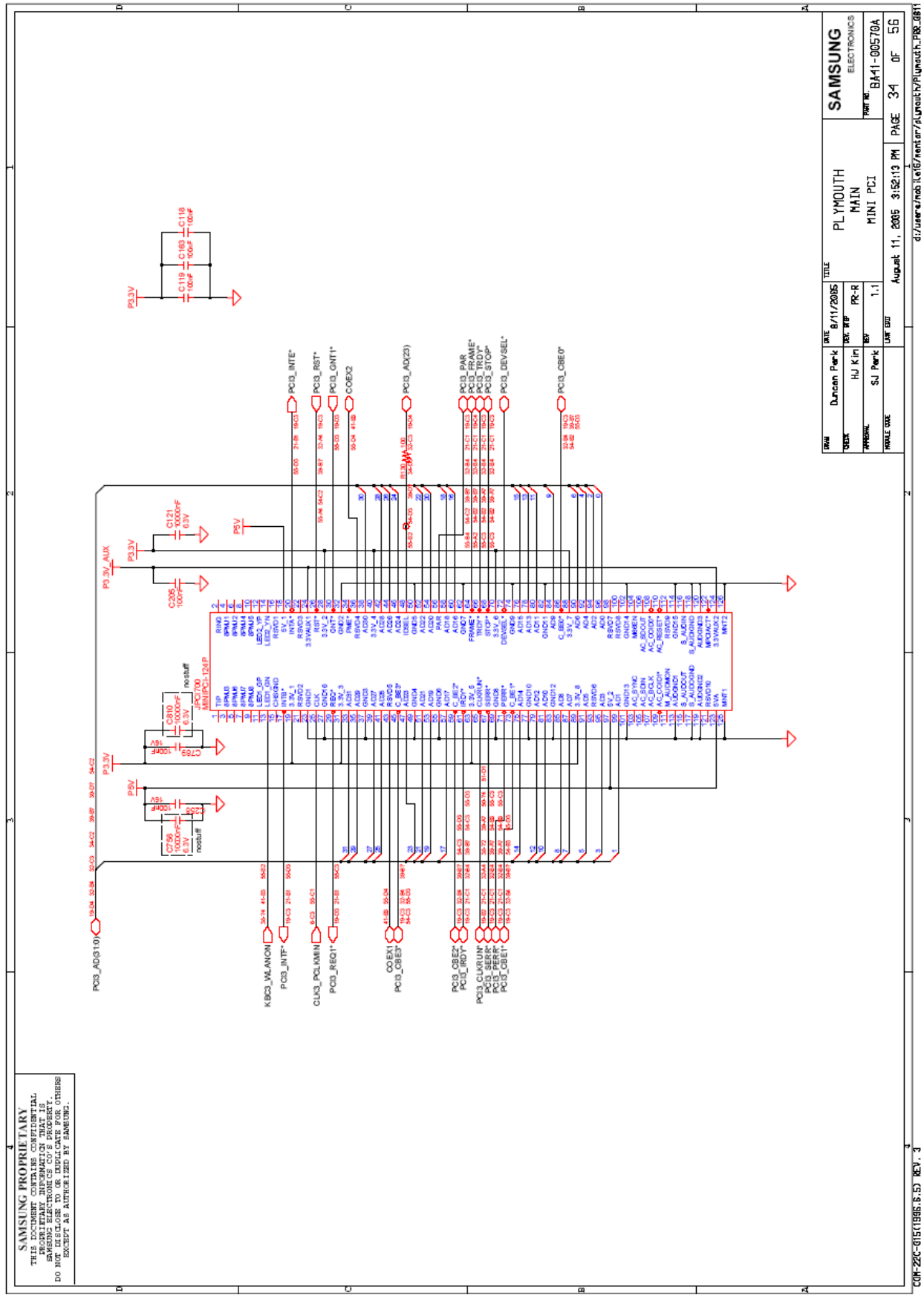
7. Schematic



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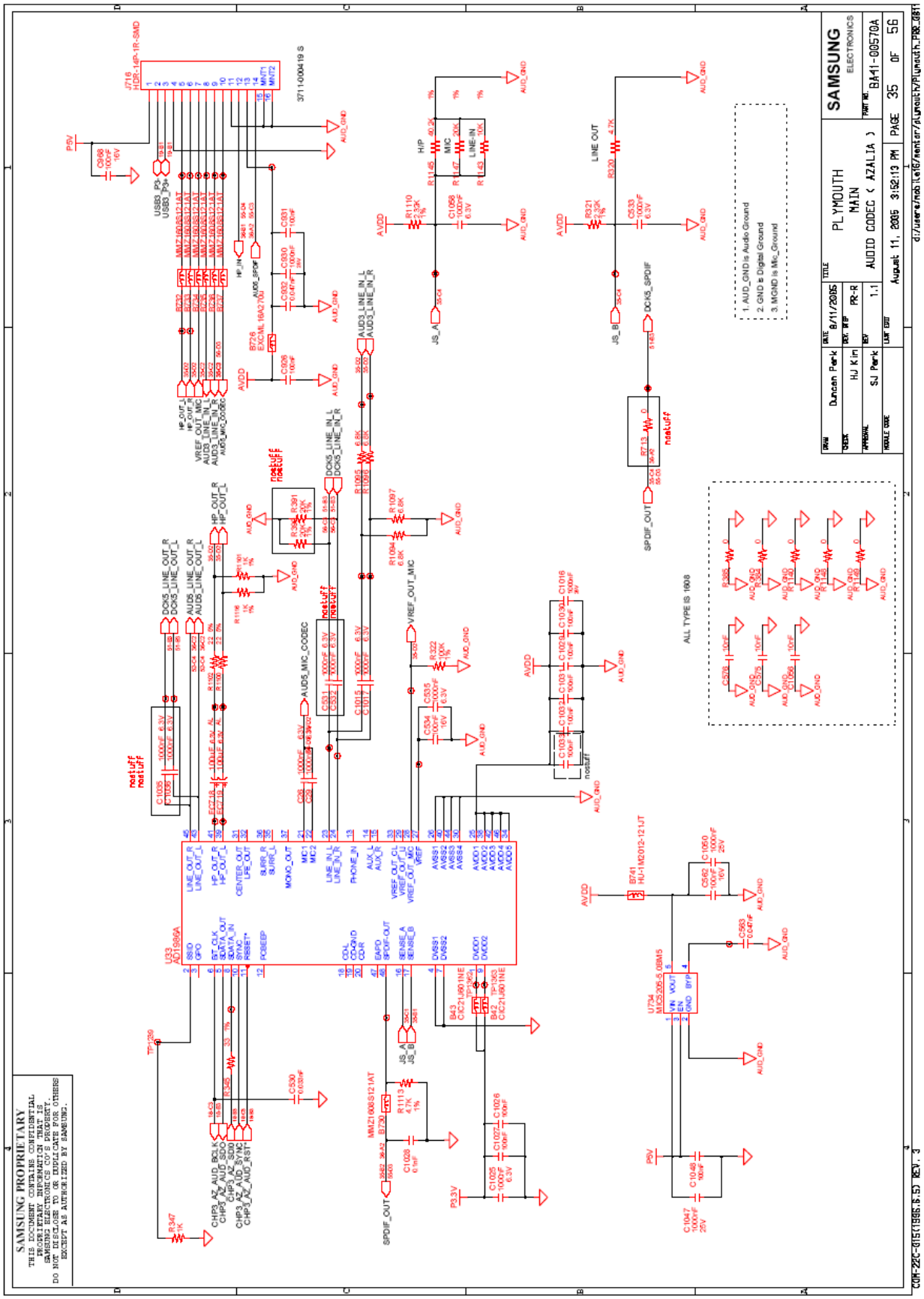
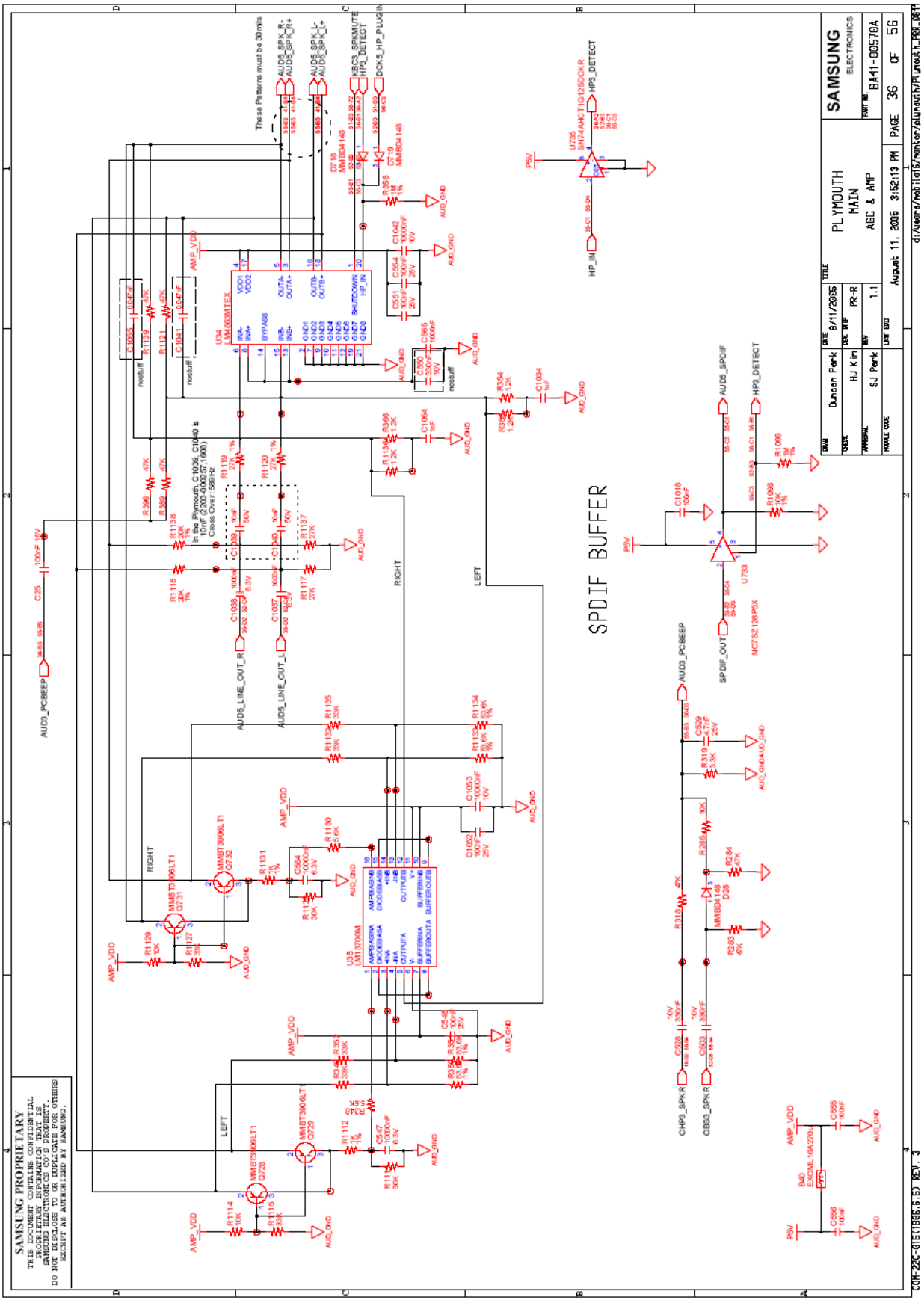
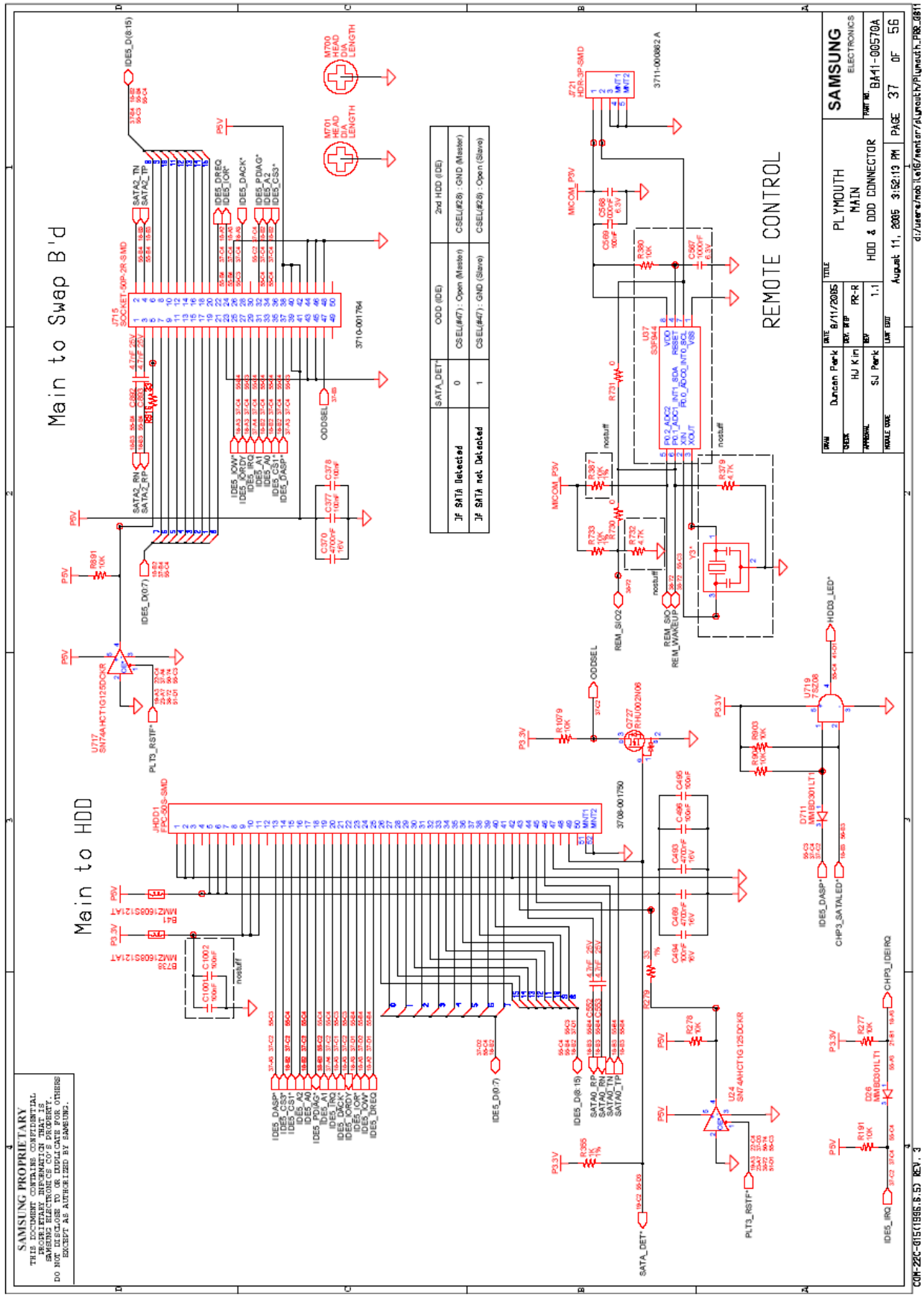
7. Schematic



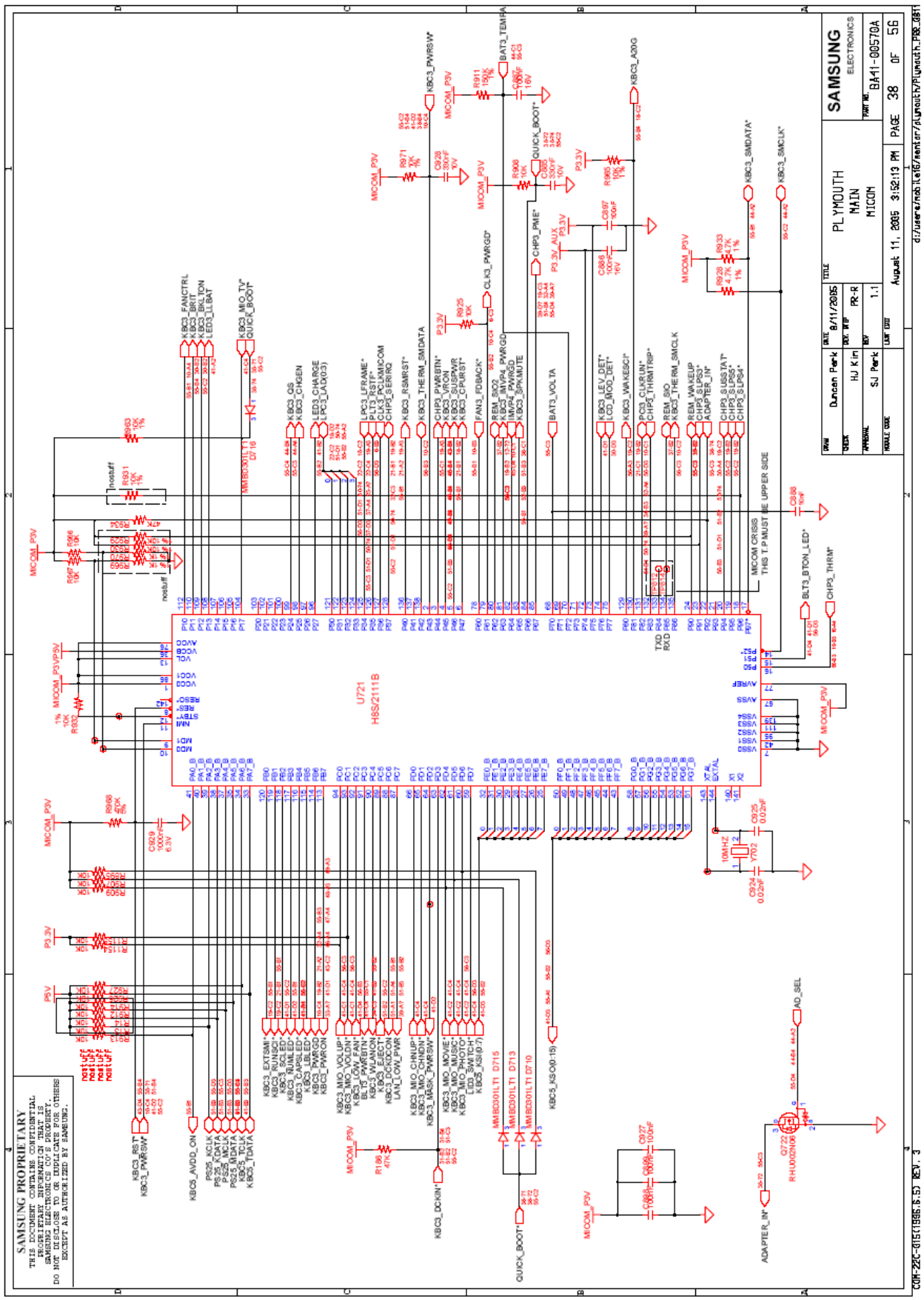
7. Schematic


SPDIF BUFFER
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
AGC & AMP
August 11, 2005 3:52:13 PM
PAGE 36 OF 56

7. Schematic


Main to Swap B'd
Main to HDD
REMOTE CONTROL
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
HDD & ODD CONNECTOR
BA41-00570A
PAGE 37 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
FR-R
1.1
SATA_DET*
ODD (IDE)
2nd HDD (IDE)
JF SATA Detected
JF SATA not Detected
CSEL(#47) : Open (Master)
CSEL(#47) : GND (Slave)
CSEL(#28) : GND (Master)
CSEL(#28) : Open (Slave)

7. Schematic


SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
MICOM
BA41-00570A
PAGE 38 OF 56
August 11, 2005 3:52:13 PM
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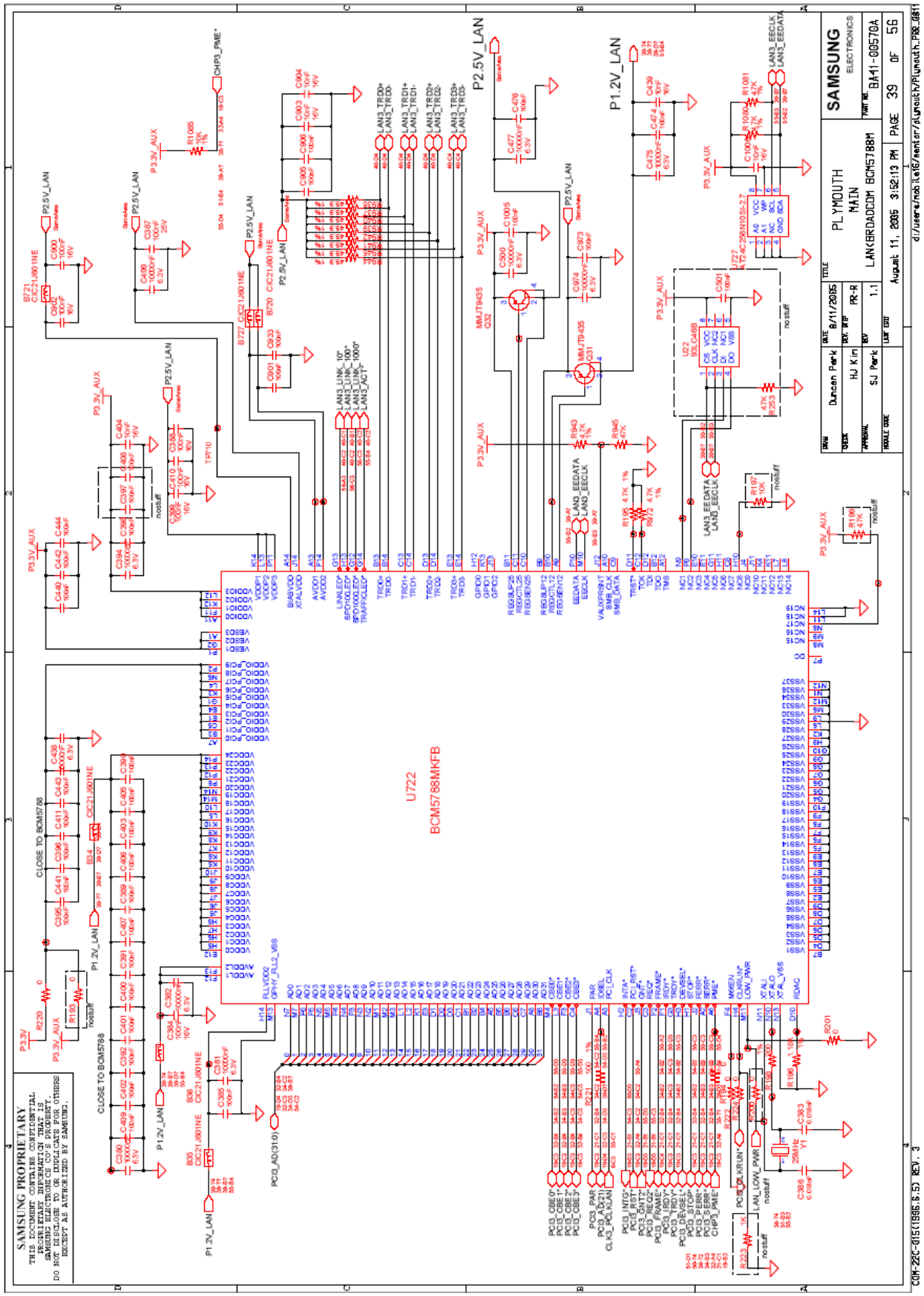
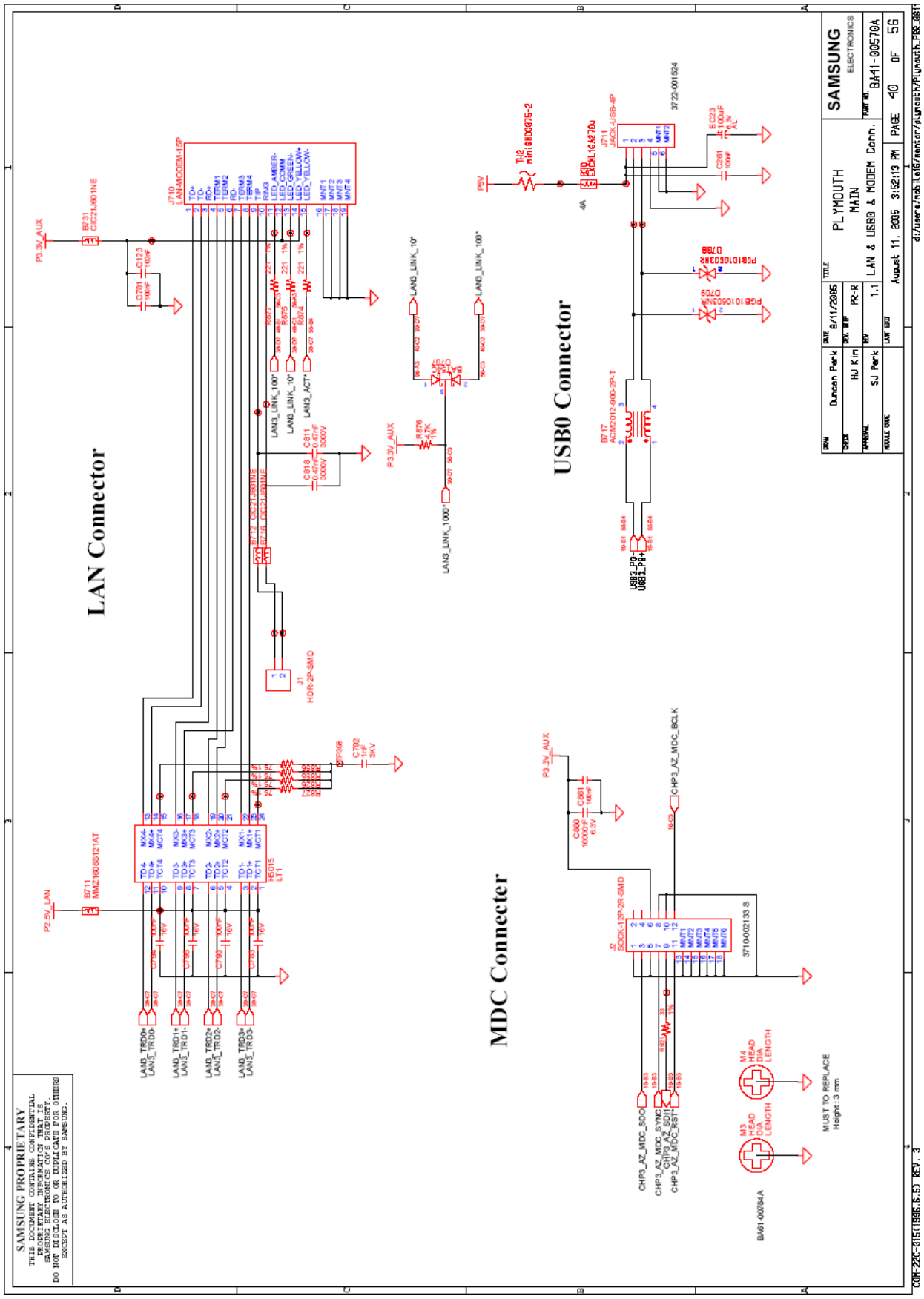
U721
H8S/2111B
MICOM CRSIS
THIS T.P MUST BE UPPER SIDE

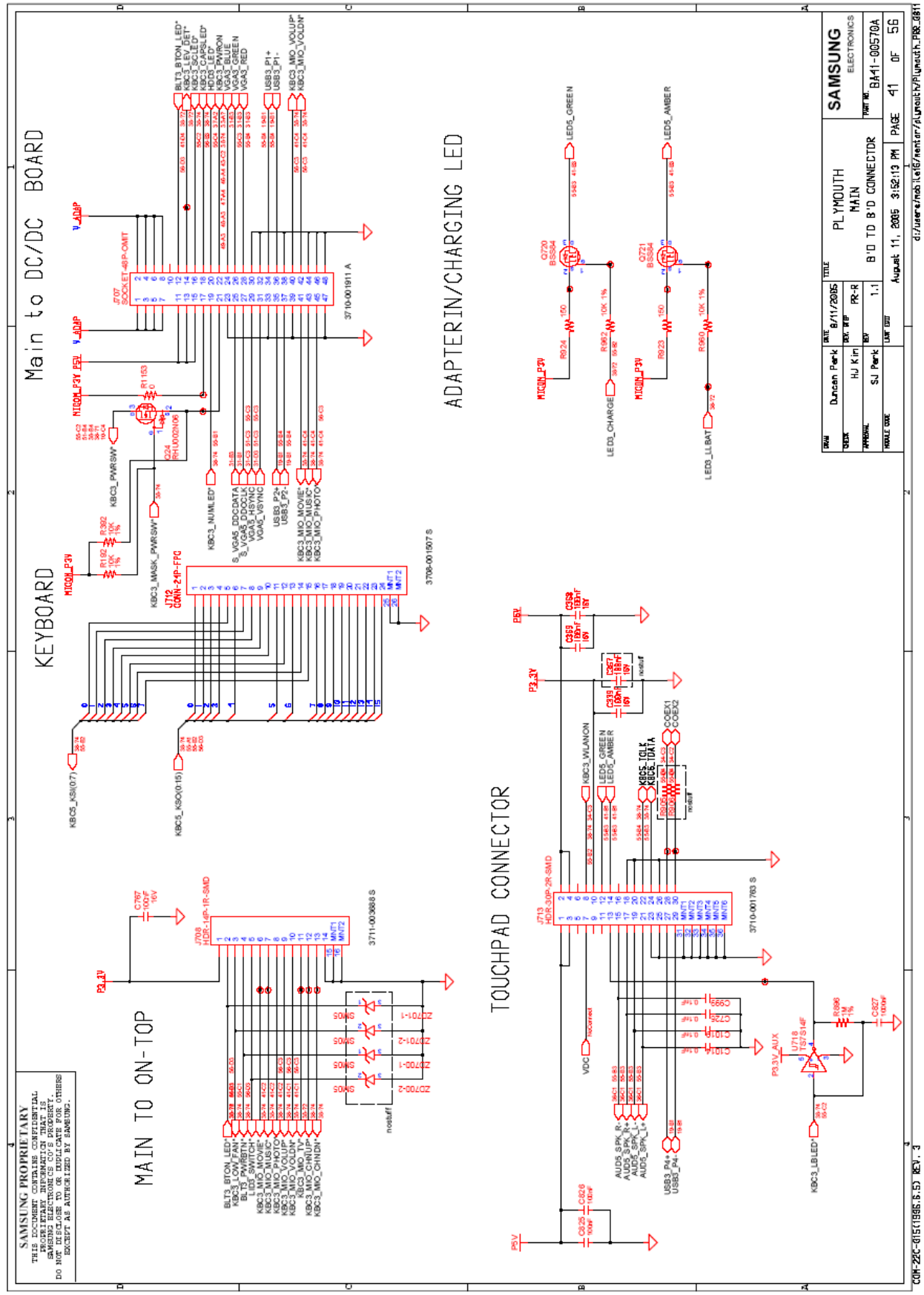
7. Schematic



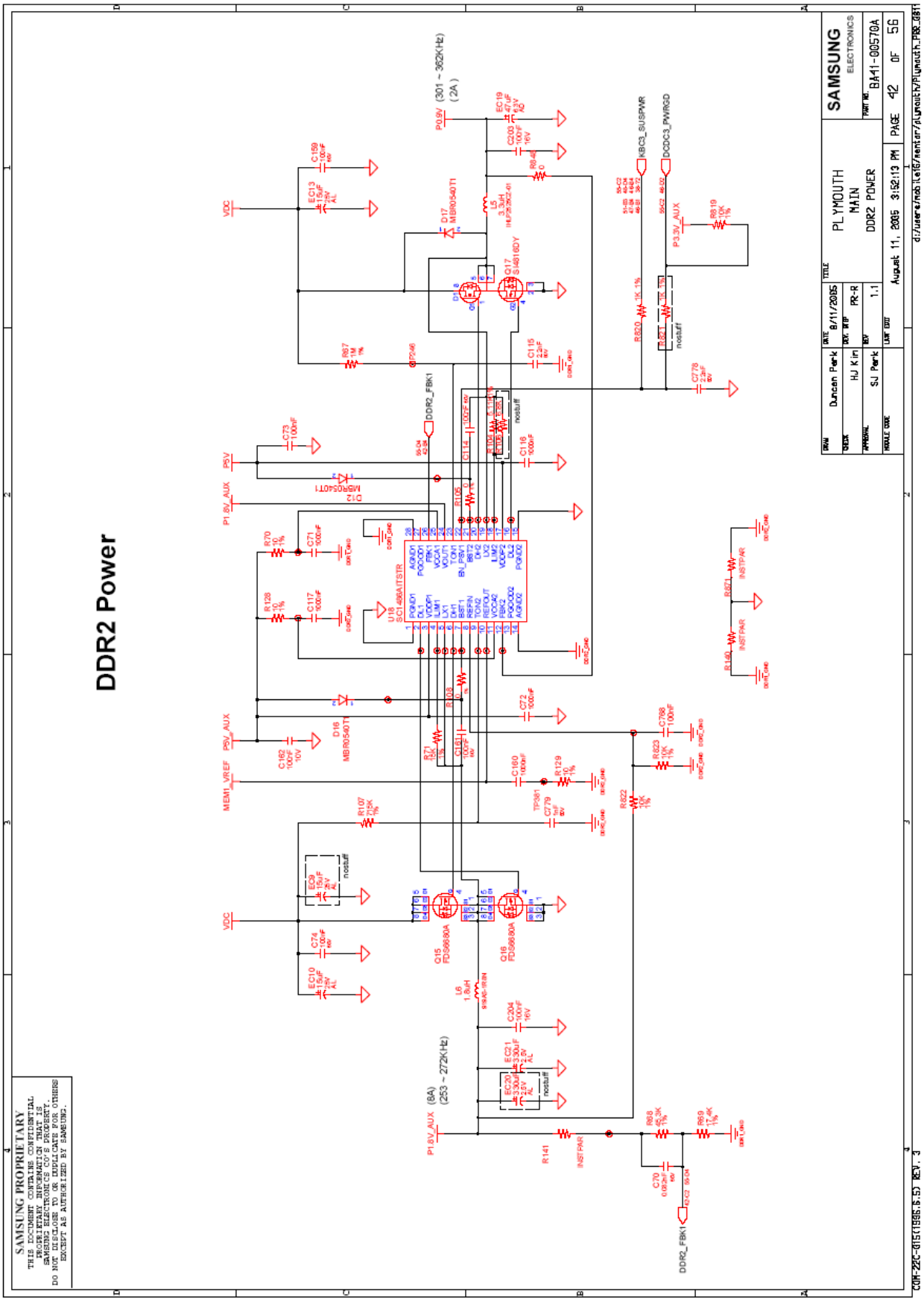
7. Schematic


LAN Connector
USB0 Connector
MDC Connecter
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
LAN & USB0 & MODEM Conn.
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 40 OF 56
MUST TO REPLACE
Height : 3 mm

7. Schematic


Main to DC/DC BOARD
KEYBOARD
ADAPTERIN/CHARGING LED
MAIN TO ON-TOP
TOUCHPAD CONNECTOR
SAMSUNG PROPRIETARY
SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
B'D TO B'D CONNECTOR
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 41 OF 56

7. Schematic


DDR2 Power
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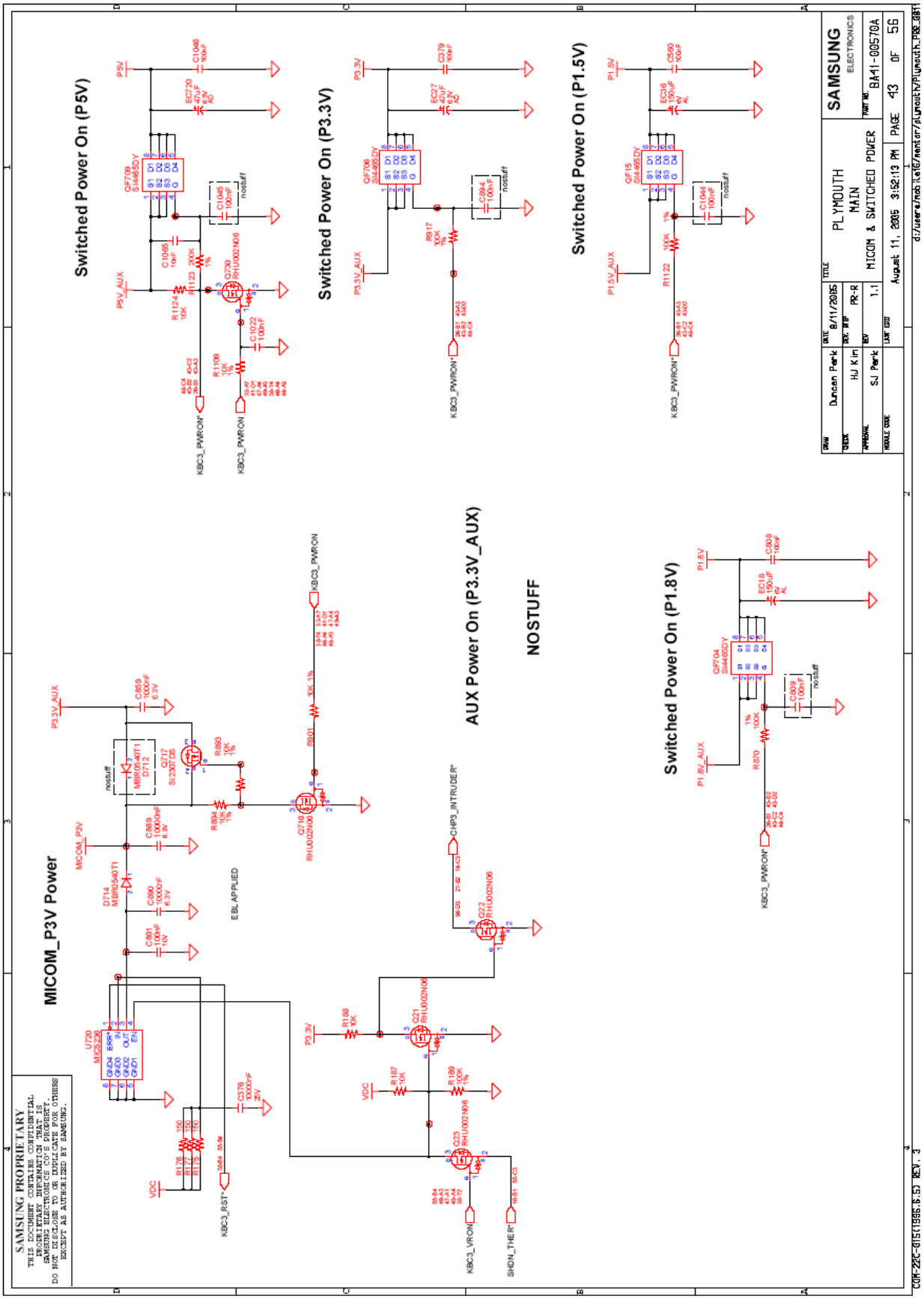
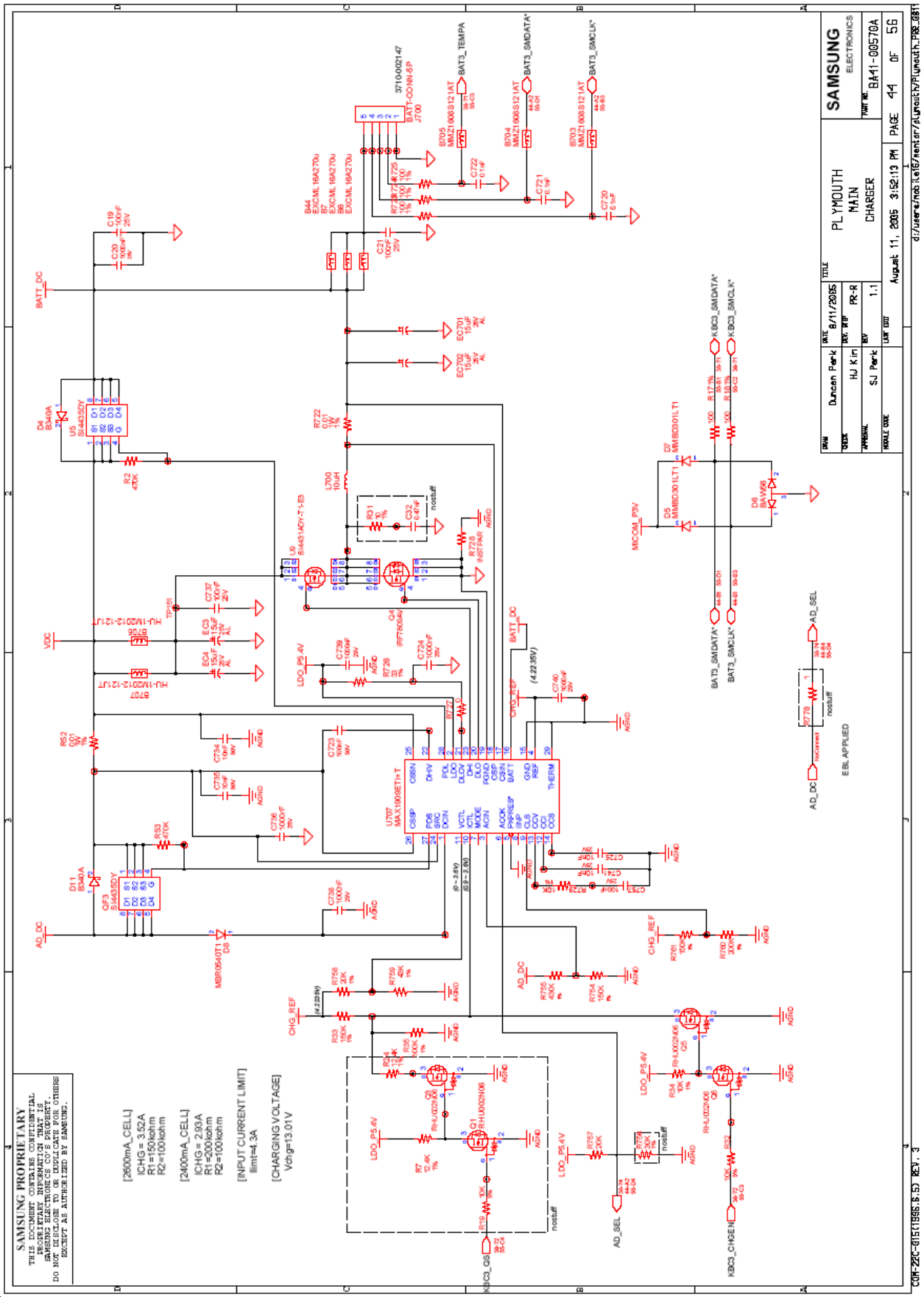
SAMSUNG ELECTRONICS
PLYMOUTH
MAIN
DDR2 POWER
BA41-00570A
PAGE 42 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile16/kentar/plymouth/Plymouth_PBR.dsn
Duncan Park 8/11/2005
HJ Kim PR-R
SJ Park 1.1
P0.9V (301 ~ 362KHz) (2A)
P1.8V_AUX (8A) (253 ~ 272KHz)
P5V
P3.3V_AUX
P5V_AUX
VDC
MEM1_VREF
DDR2_FBK1
KBC3_SUSPWR
DCDC3_PWRGD

7. Schematic


Switched Power On (P5V)
Switched Power On (P3.3V)
Switched Power On (P1.5V)
Switched Power On (P1.8V)
MICOM_P3V Power
AUX Power On (P3.3V_AUX)
NOSTUFF
EBL APPLIED
SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
MICOM & SWITCHED POWER
BA41-00570A
PAGE 43 OF 56
August 11, 2005 3:52:13 PM

7. Schematic


SAMSUNG
ELECTRONICS
PLYMOUTH
MAIN
CHARGER
BA41-00570A
PAGE 44 OF 56
August 11, 2005 3:52:13 PM
SAMSUNG PROPRIETARY
[2600mA_CELL]
ICHG = 3.52A
R1=150kohm
R2=100kohm
[2400mA_CELL]
ICHG = 2.93A
R1=200kohm
R2=100kohm
[INPUT CURRENT LIMIT]
Ilimit=4.3A
[CHARGING VOLTAGE]
Vchg=13.01V

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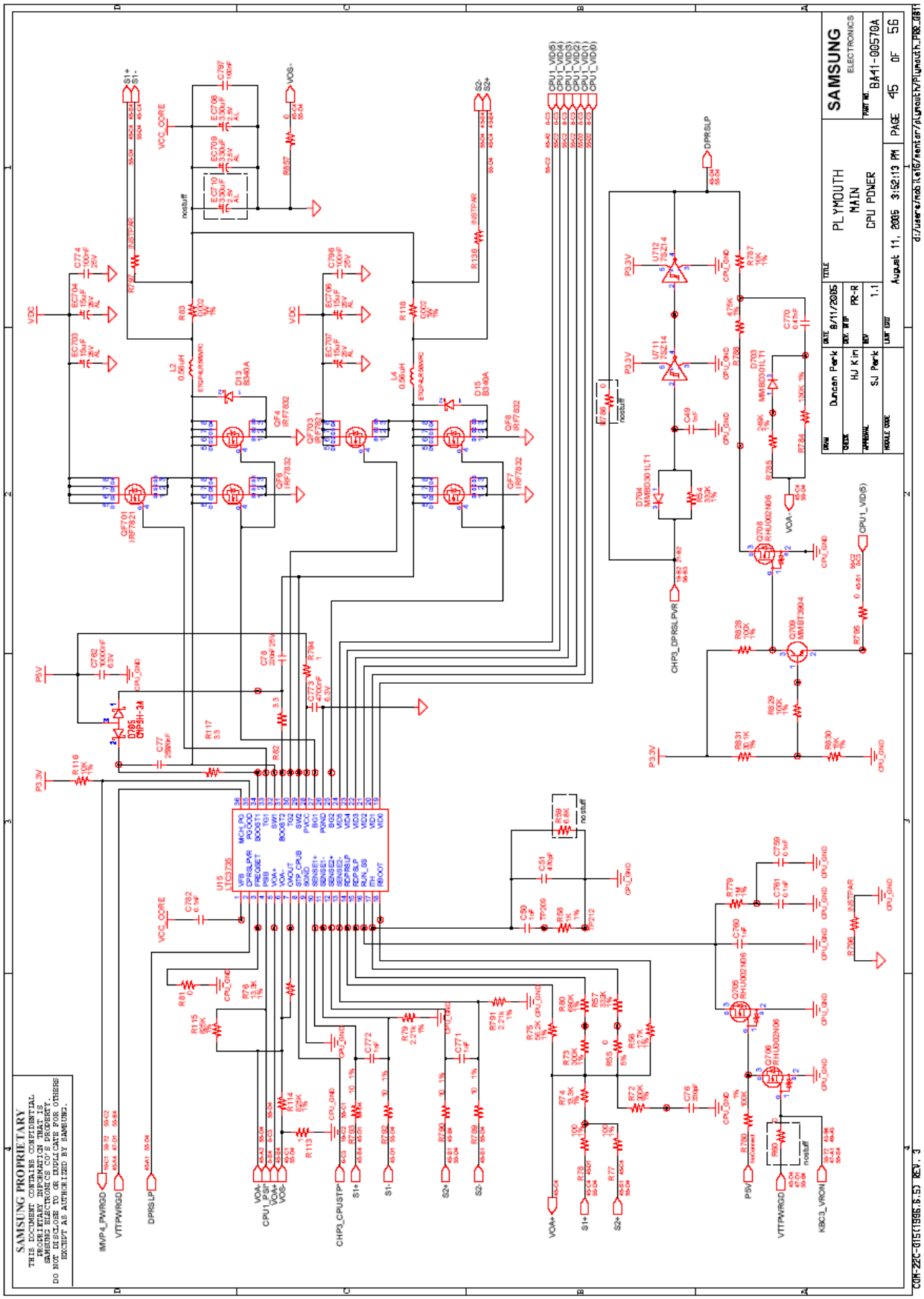
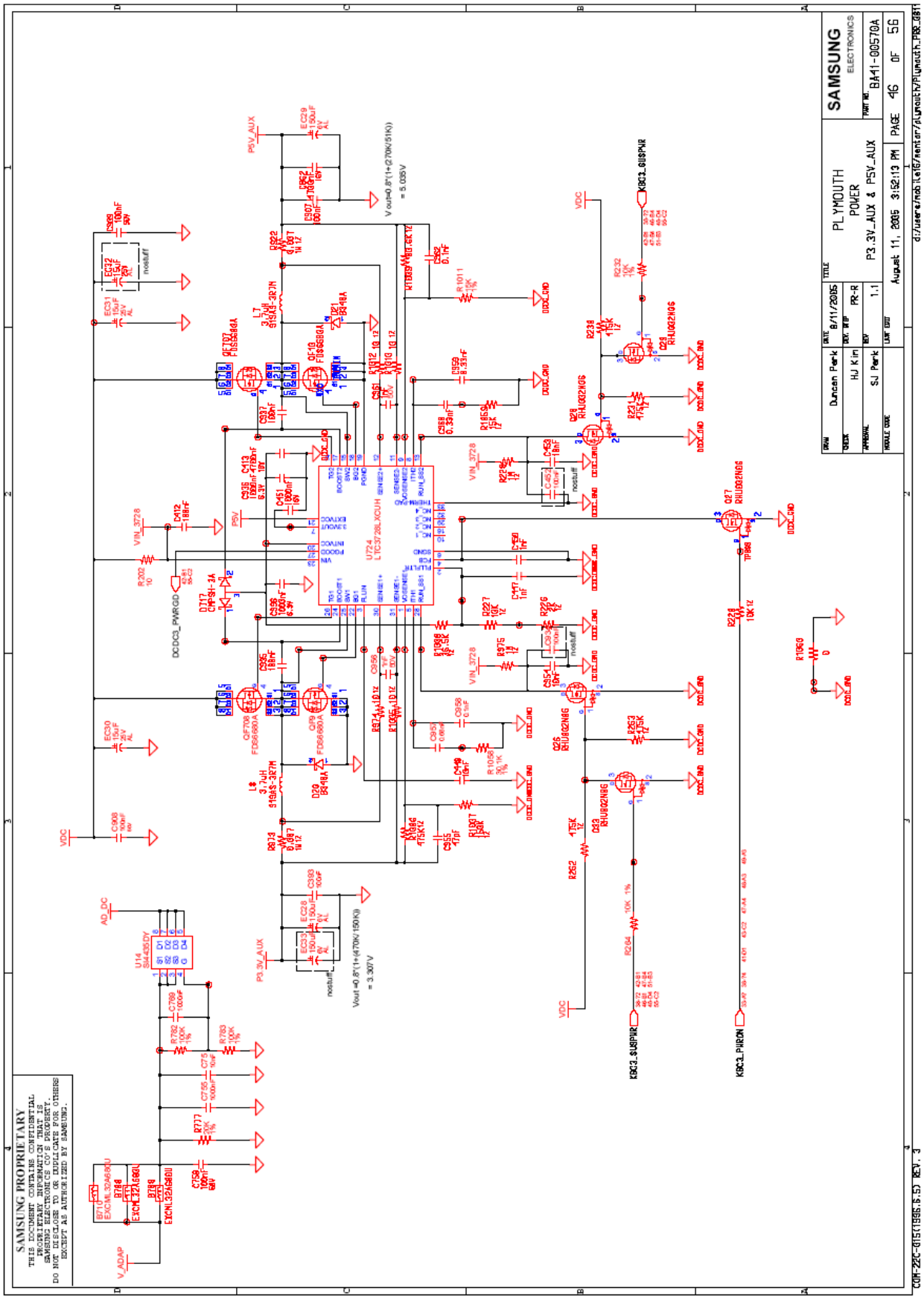
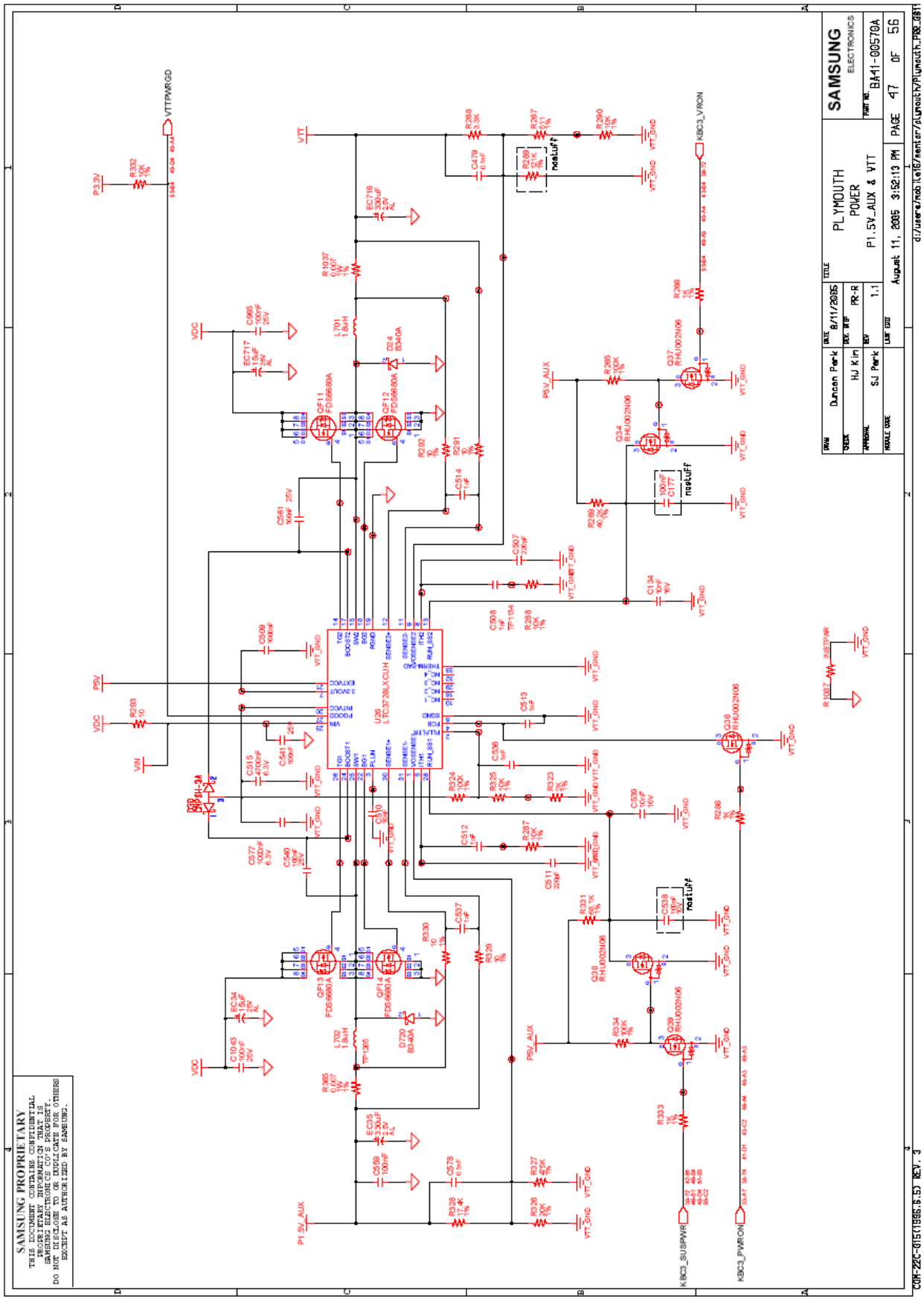
7. Schematic



7. Schematic


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH
POWER
P3.3V_AUX & PSV_AUX
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 46 OF 56
Duncan Park
HJ Kim
SJ Park
8/11/2005
FR-R
1.1
P3V_AUX
PSV_AUX
VIN_3728
VDC
V_ADAP
DCDCG_PWRGD
K8G3_6U8PWR
K8G3_SU8PWR
K8G3_PWRON

7. Schematic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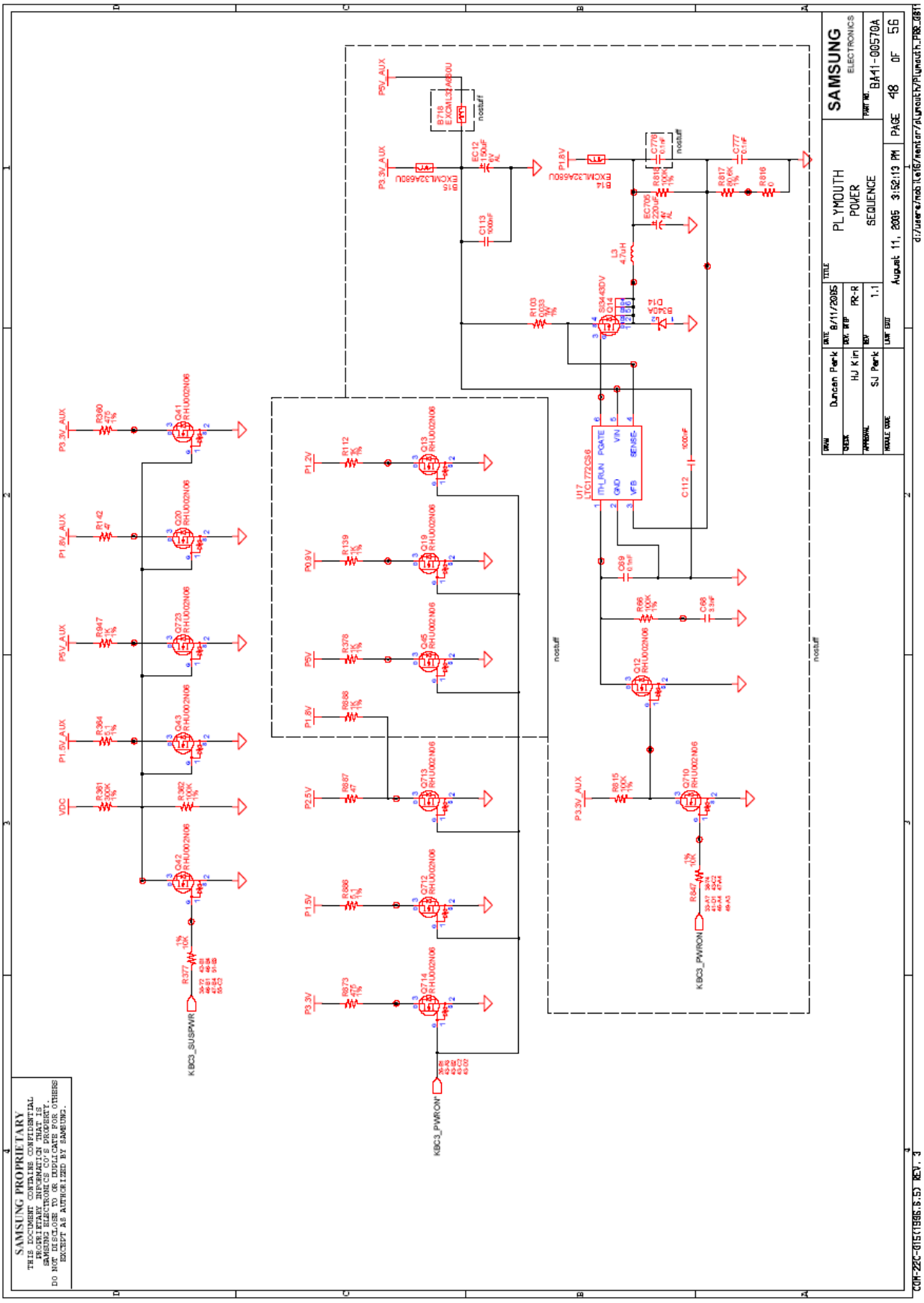
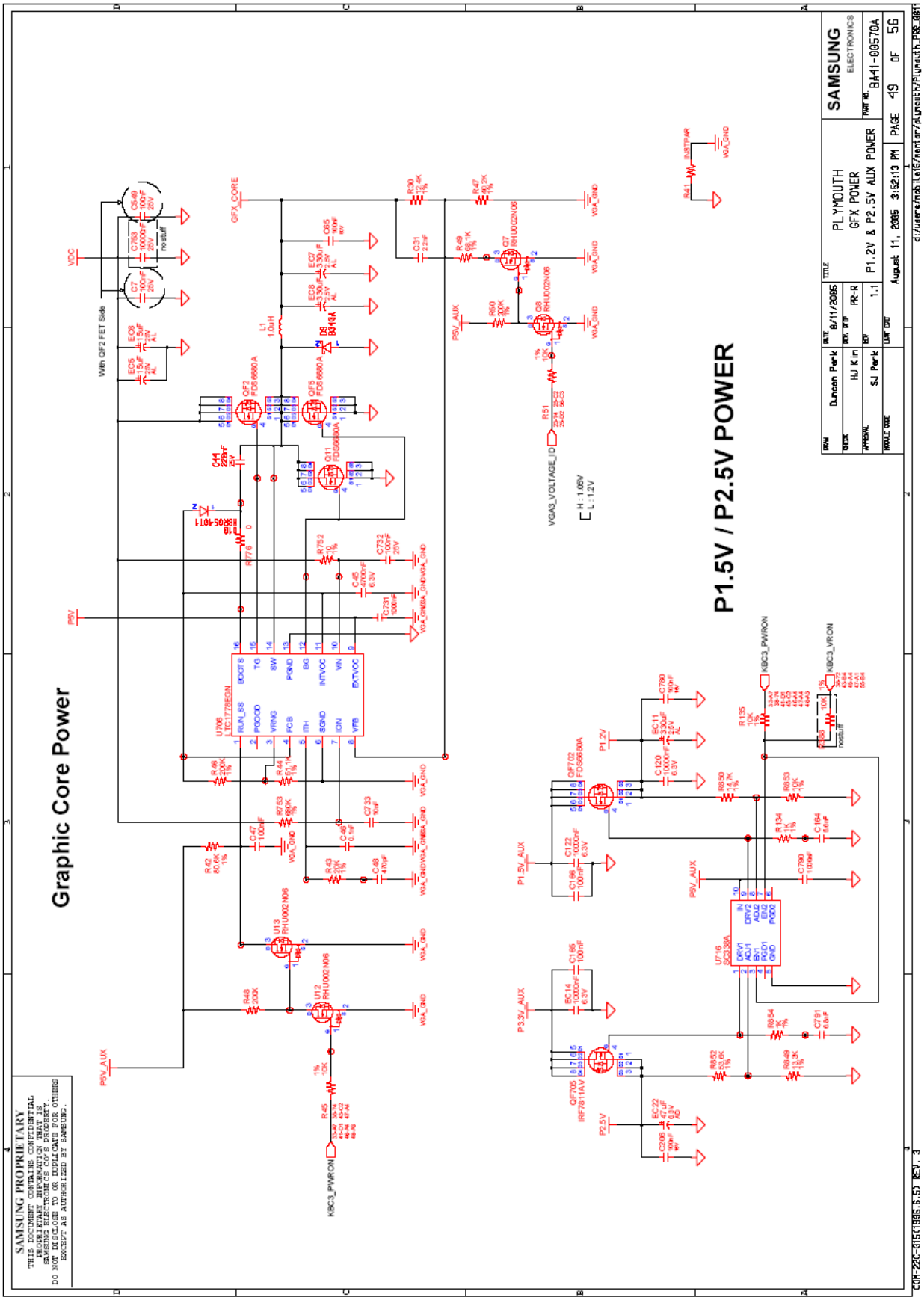
SAMSUNG ELECTRONICS
PLYMOUTH
POWER
P1.5V_AUX & VTT
BA41-00570A
PAGE 47 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile16/mentor/plymouth/Plymouth_PWR.dsn
Duncan Park 8/11/2005
HJ Kim PR-R
SJ Park 1.1
VTT
P5V_AUX
P1.5V_AUX
P3.3V
P5V
VDC
VIN
VTTPWRGD
KBC3_VRON
KBC3_SUSPWR
KBC3_PWRON
U26 LTC3728LXCUH
Q34 RHU002N06
Q35 RHU002N06
Q36 RHU002N06
Q37 RHU002N06
Q38 RHU002N06
Q39 RHU002N06
QF11 FDS6680A
QF12 FDS6680A
QF13 FDS6680A
QF14 FDS6680A
D24 B340A
D29 B340A
L701 1.8uH
L702 1.8uH
notstuff

7. Schematic


SAMSUNG
ELECTRONICS
PLYMOUTH
POWER
SEQUENCE
BA41-00570A
PAGE 48 OF 56
August 11, 2005 3:52:13 PM
SAMSUNG PROPRIETARY
P5V_AUX
P3.3V_AUX
P1.8V
P1.2V
P0.9V
P5V
P2.5V
P1.5V
P3.3V
VDC
P1.8V_AUX
P1.5V_AUX
KBC3_SUSPWR
KBC3_PWRON
U17
LTC1772CS6
Q41
Q20
Q723
Q43
Q42
Q19
Q45
Q713
Q712
Q714
Q12
Q710

7. Schematic


P1.5V / P2.5V POWER
Graphic Core Power
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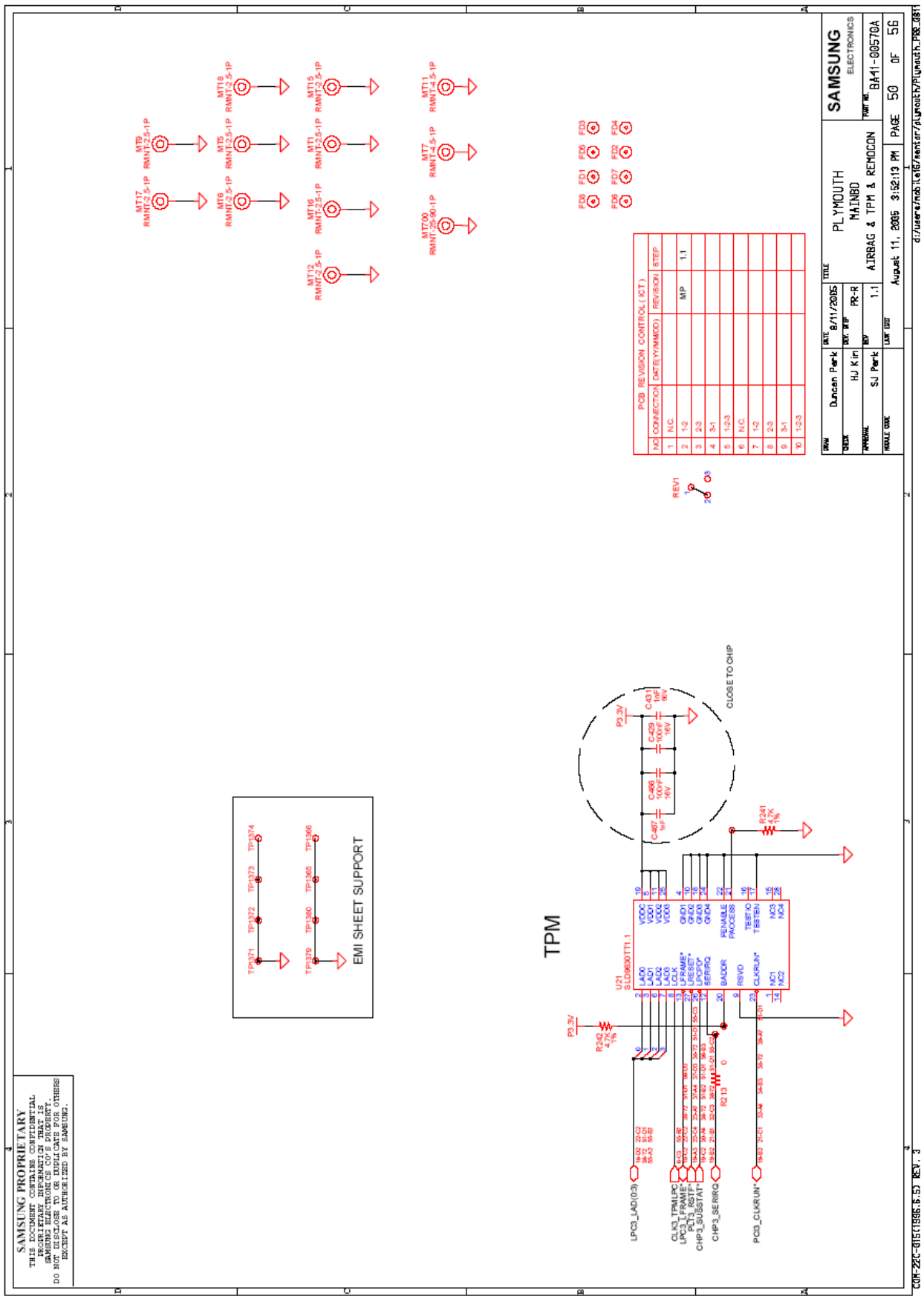
SAMSUNG ELECTRONICS
PLYMOUTH
GFX POWER
P1.2V & P2.5V AUX POWER
BA41-00570A
PAGE 49 OF 56
August 11, 2005 3:52:13 PM
d:/users/nobikes/mentor/plymouth/Plymouth.PRJ

7. Schematic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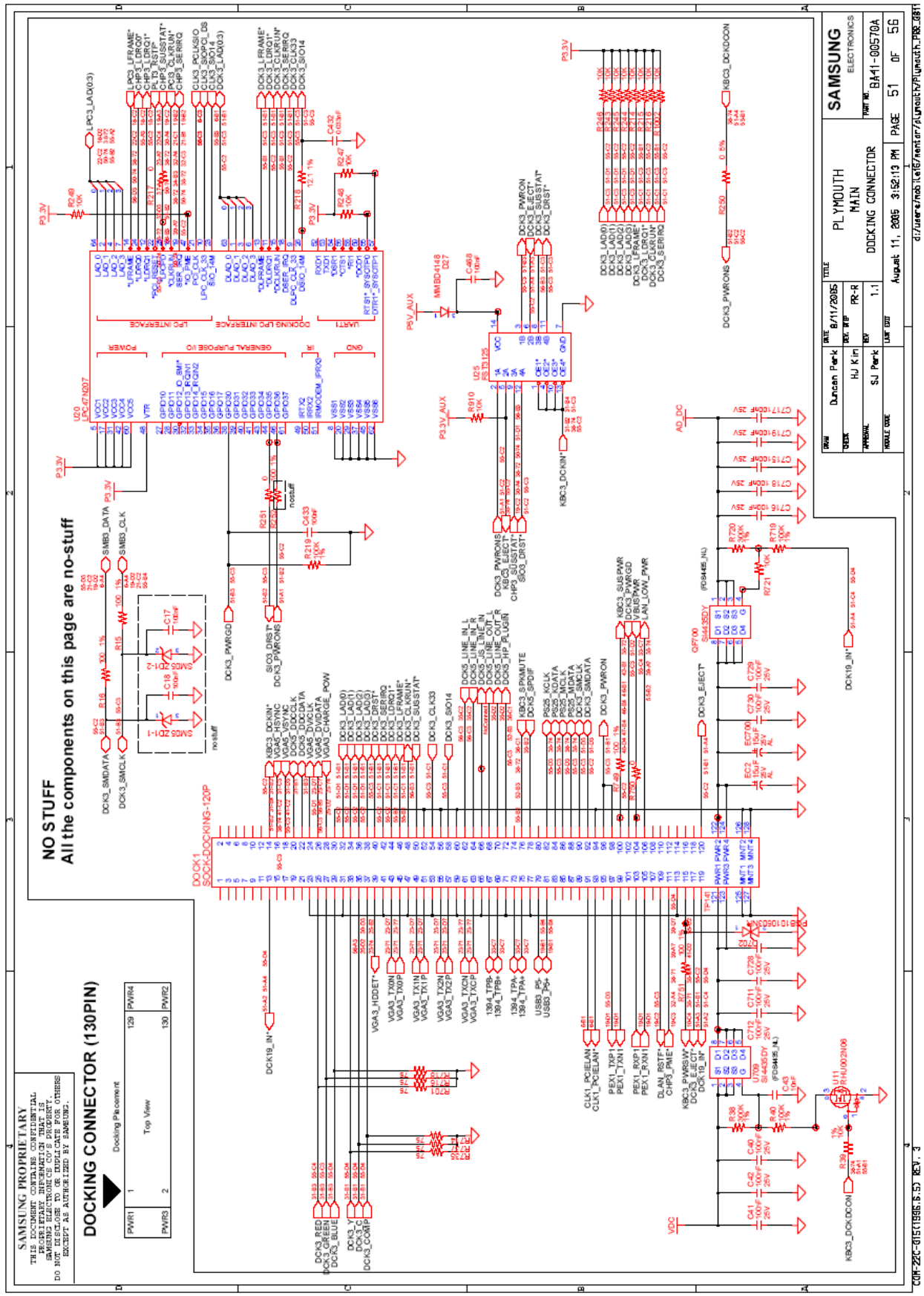
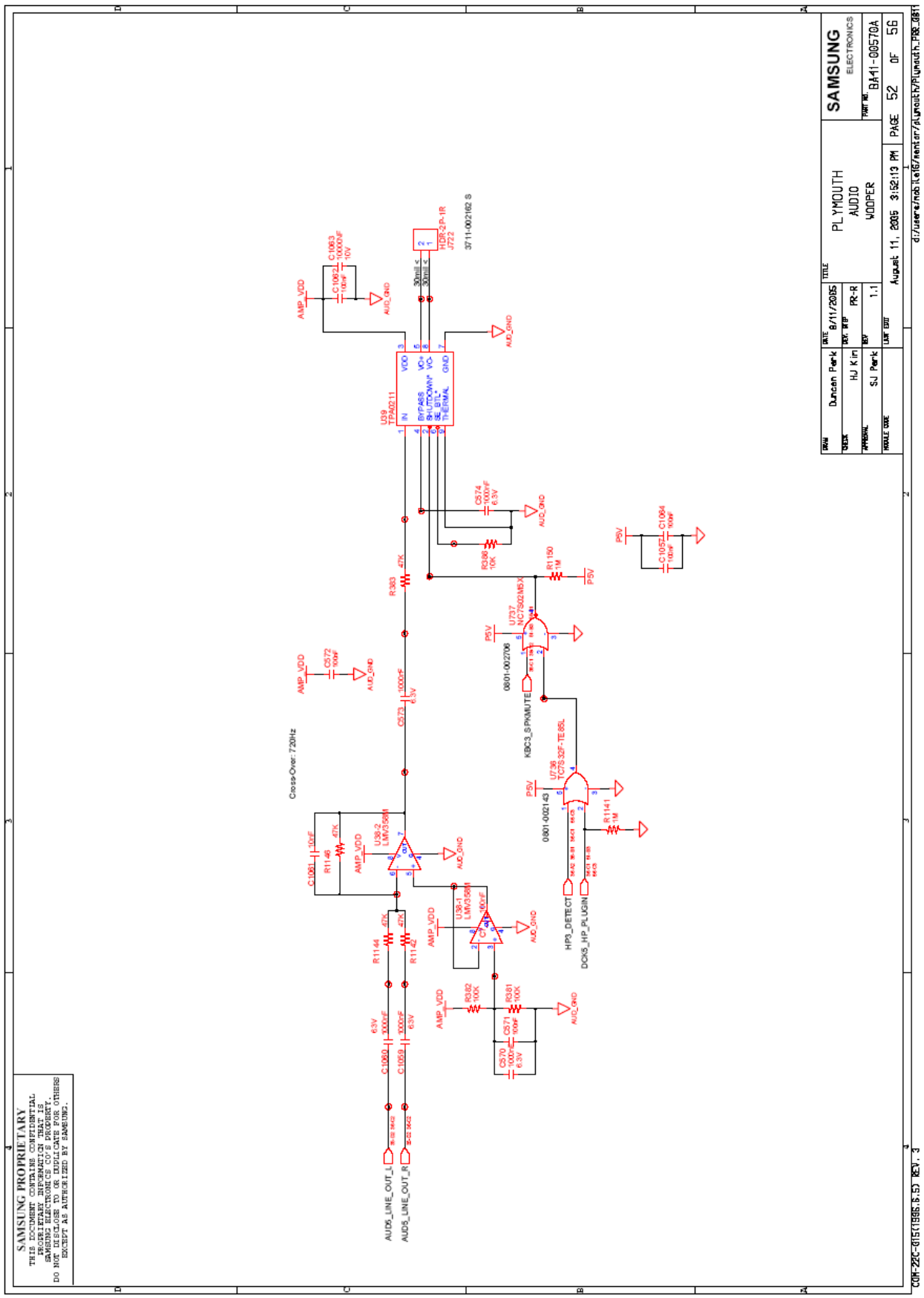
EMI SHEET SUPPORT
TPM
CLOSE TO CHIP
PCB REVISION CONTROL (ICT)
NO | CONNECTION | DATE(YY/MM/DD) | REVISION | STEP
SAMSUNG ELECTRONICS
PLYMOUTH MAINBD
AIRBAG & TPM & REMOCON
BA41-00570A
PAGE 50 OF 56
August 11, 2005 3:52:13 PM
d:/users/mobile6/mentor/plymouth/Plymouth_PBR.dsn
COM-22C-015(1986.6.5) REV. 3

7. Schematic


NO STUFF
All the components on this page are no-stuff
DOCKING CONNECTOR (130PIN)
SAMSUNG PROPRIETARY
SAMSUNG
PLYMOUTH
MAIN
DOCKING CONNECTOR
BA41-00570A
August 11, 2005 3:52:13 PM
PAGE 51 OF 56

7. Schematic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SAMSUNG ELECTRONICS
PLYMOUTH
AUDIO
WOOPER
BA41-00570A
PAGE 52 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
Cross-Over: 720Hz
AMP_VDD
AUD_GND
P5V
U39 TPA6211
U38-2 LM7358M
U38-1 LM7358M
U37 NC7SZ02M5X
U36 TC7S32F-TE85L
AUD5_LINE_OUT_L
AUD5_LINE_OUT_R
HP3_DETECT
DOK5_HP_PLUGIN
KBC3_SPKMUTE
COM-22C-01501986.6.5D REV. 3

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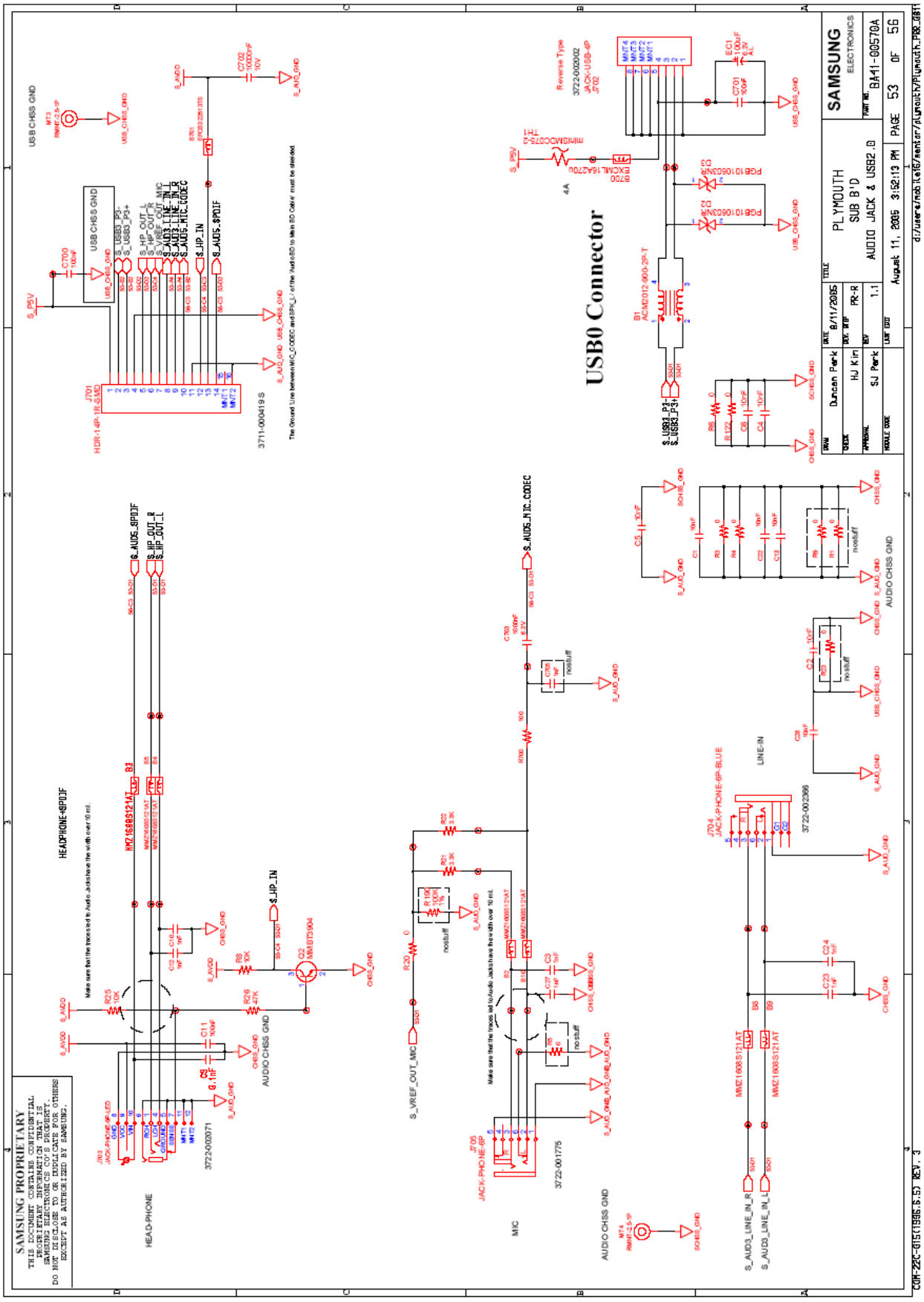
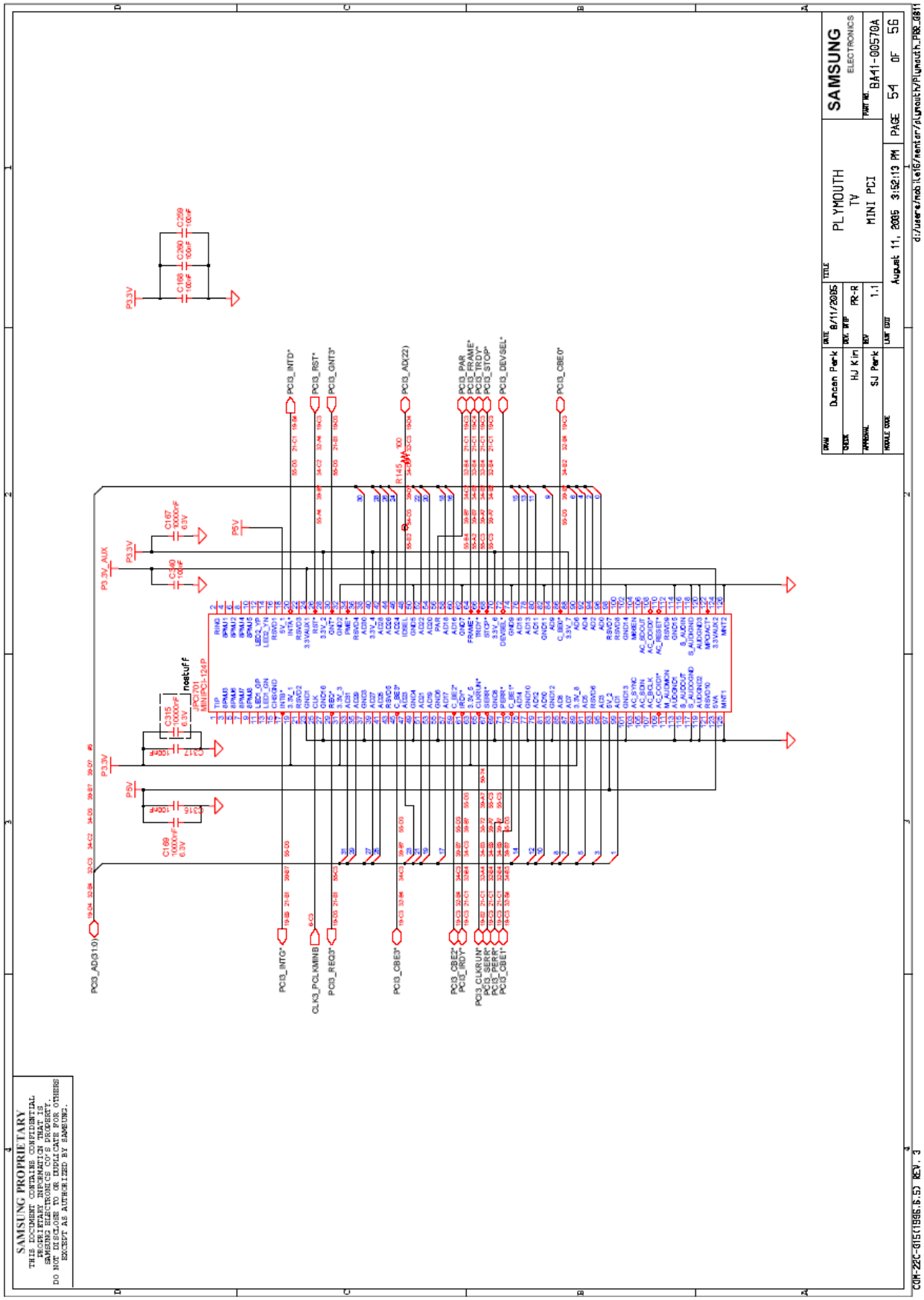
7. Schematic



7. Schematic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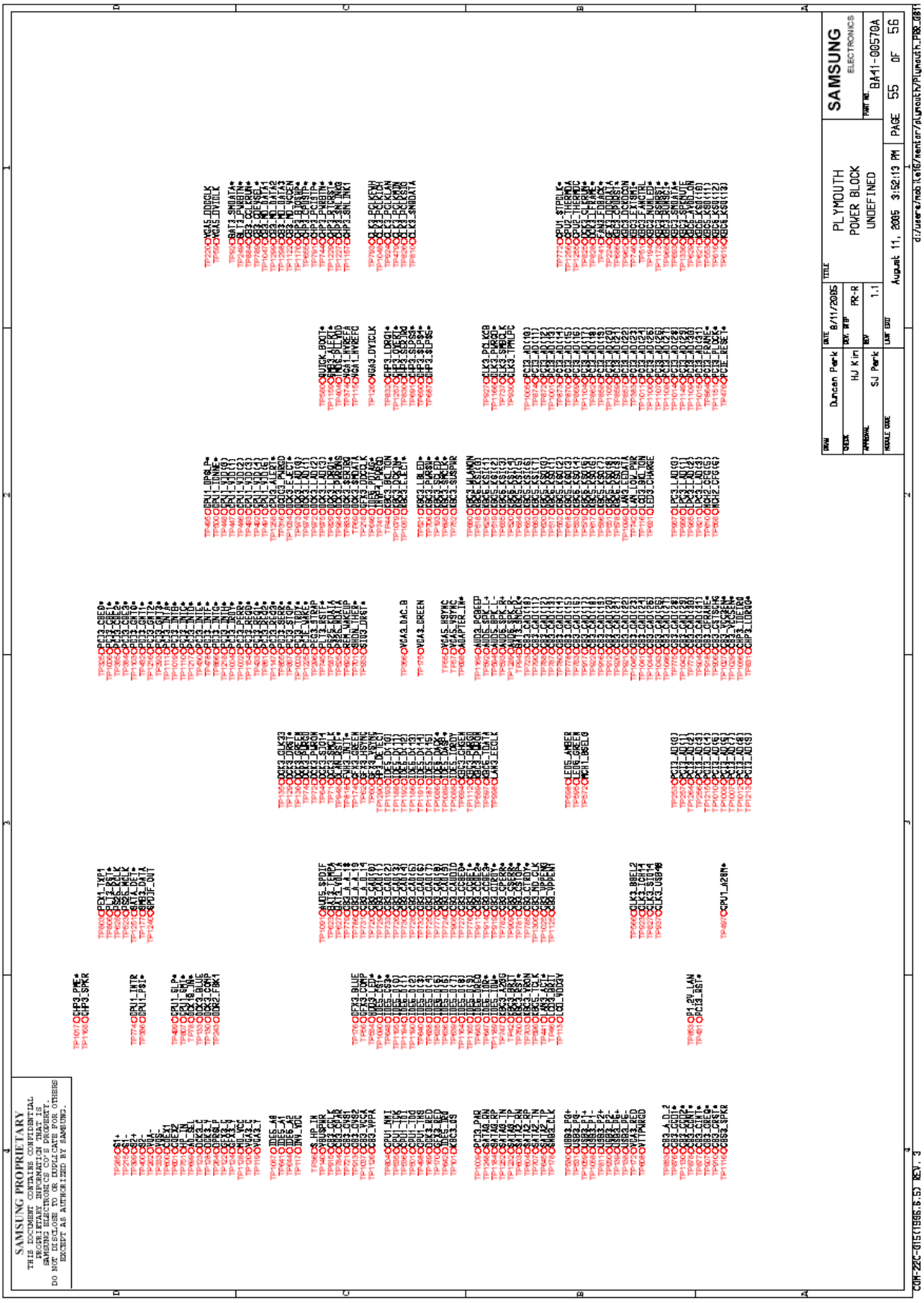
SAMSUNG ELECTRONICS
PLYMOUTH TV
MINI PCI
BA41-00570A
PAGE 54 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
P3.3V
P5V
P3.3V_AUX
PCI3_INTD*
PCI3_RST*
PCI3_GNT3*
PCI3_AD(22)
PCI3_PAR
PCI3_FRAME*
PCI3_TRDY*
PCI3_STOP*
PCI3_DEVSEL*
PCI3_CBE0*
PCI3_AD(31:0)
PCI3_INTG*
CLK3_PCLKMINB
PCI3_REQ3*
PCI3_CBE3*
PCI3_CBE2*
PCI3_IRDY*
PCI3_CLKRUN*
PCI3_SERR*
PCI3_PERR*
PCI3_CBE1*
mostuff
MINIPCI-124P

7. Schematic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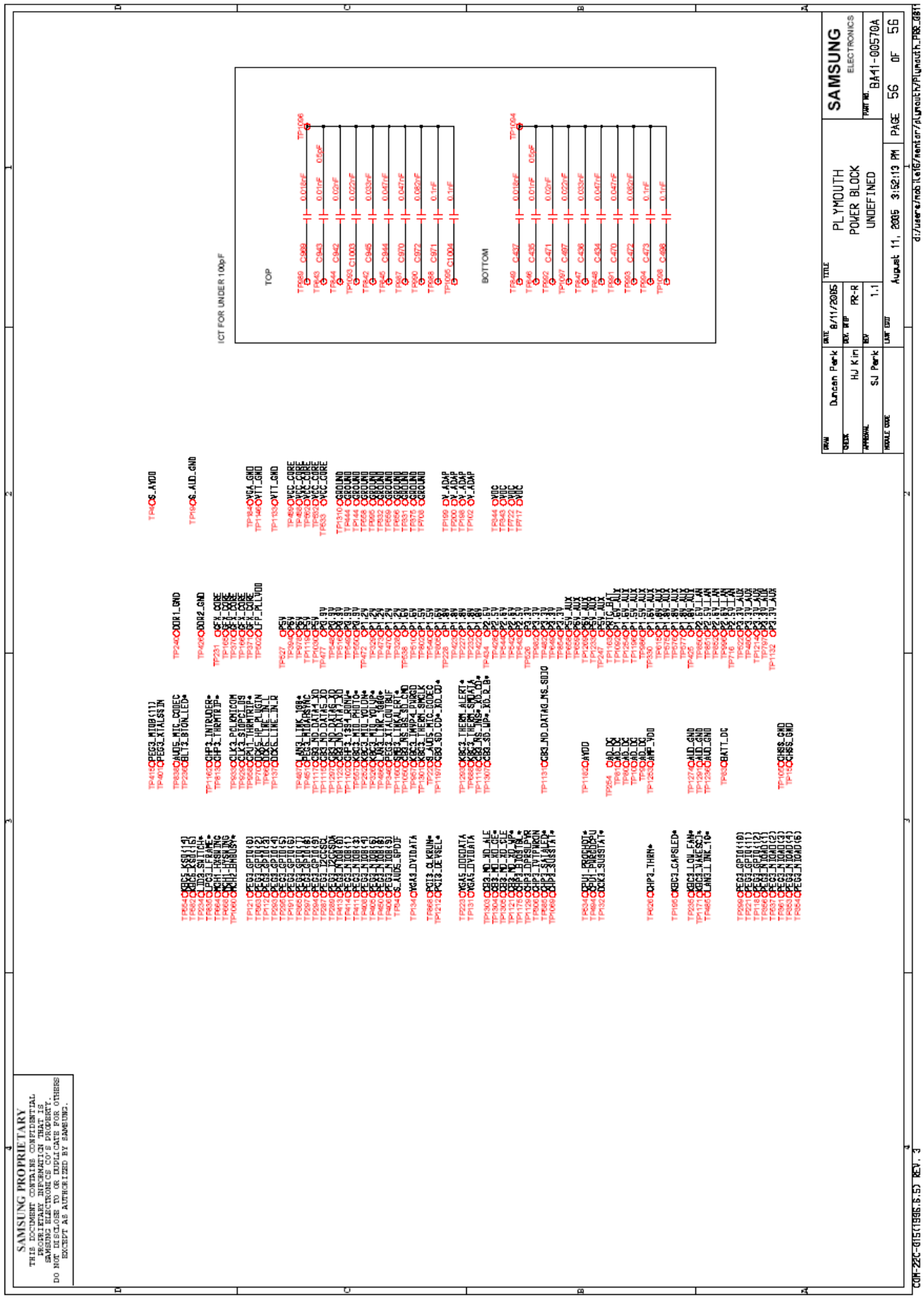
SAMSUNG ELECTRONICS
PLYMOUTH
POWER BLOCK
UNDEFINED
BA41-00570A
PAGE 55 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1.1
d:/users/models/mentor/plymouth/Plymouth_PBR.dbf

7. Schematic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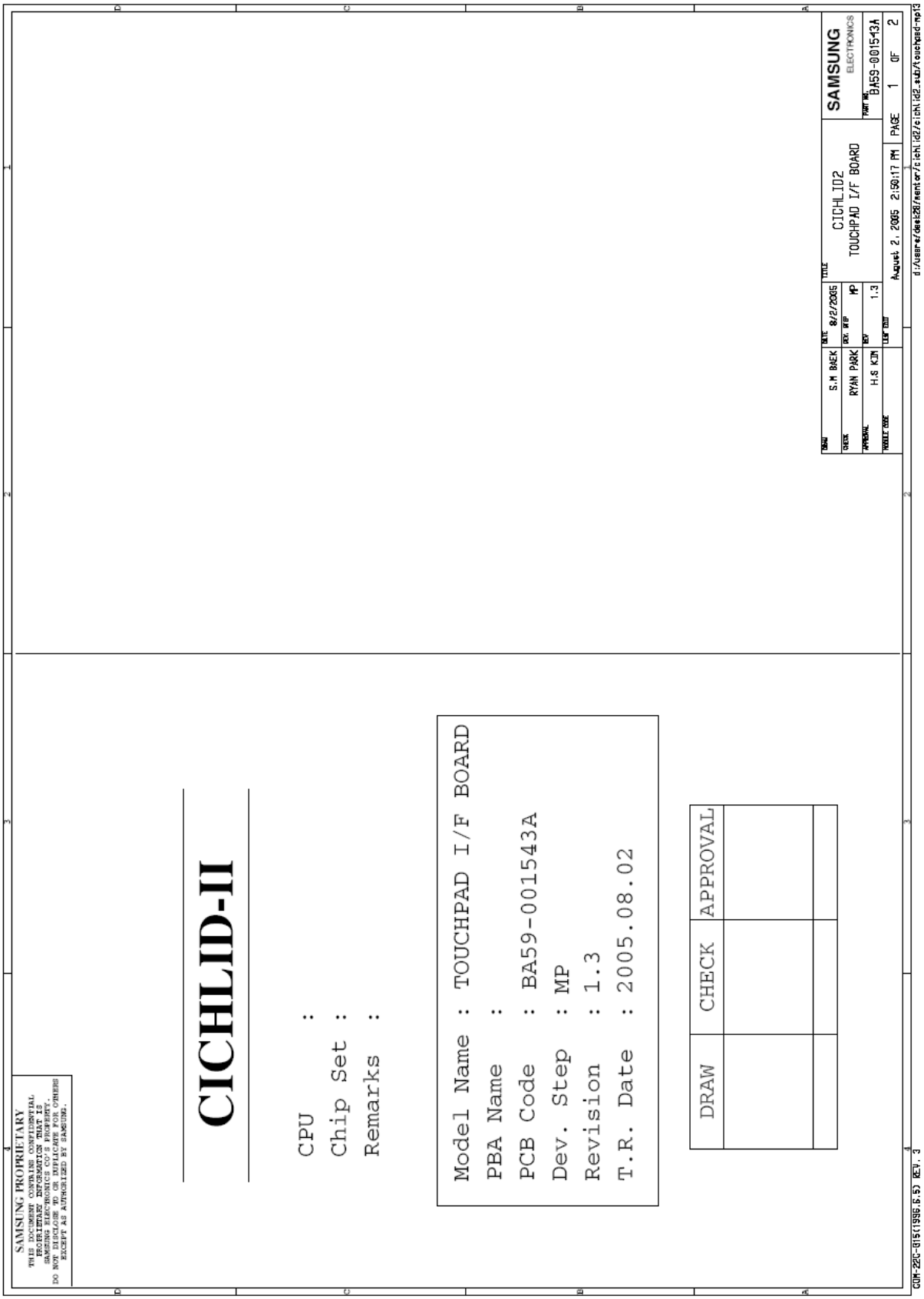
ICT FOR UNDER 100pF
TOP
BOTTOM
SAMSUNG
ELECTRONICS
PLYMOUTH
POWER BLOCK
UNDEFINED
BA41-00570A
PAGE 56 OF 56
August 11, 2005 3:52:13 PM
Duncan Park
HJ Kim
SJ Park
8/11/2005
PR-R
1:1

7. Schematic

2) Touchpad I/F Board



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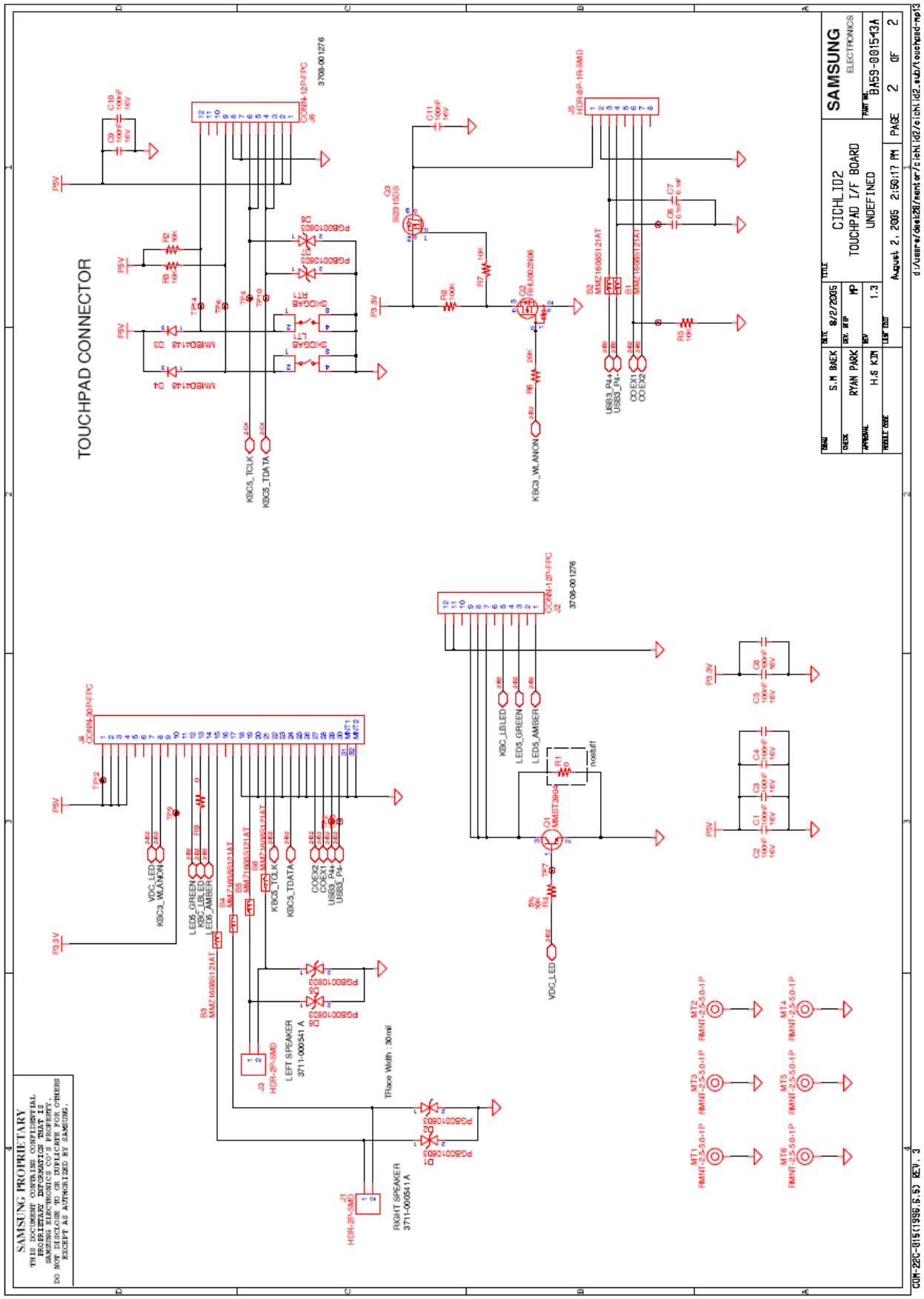
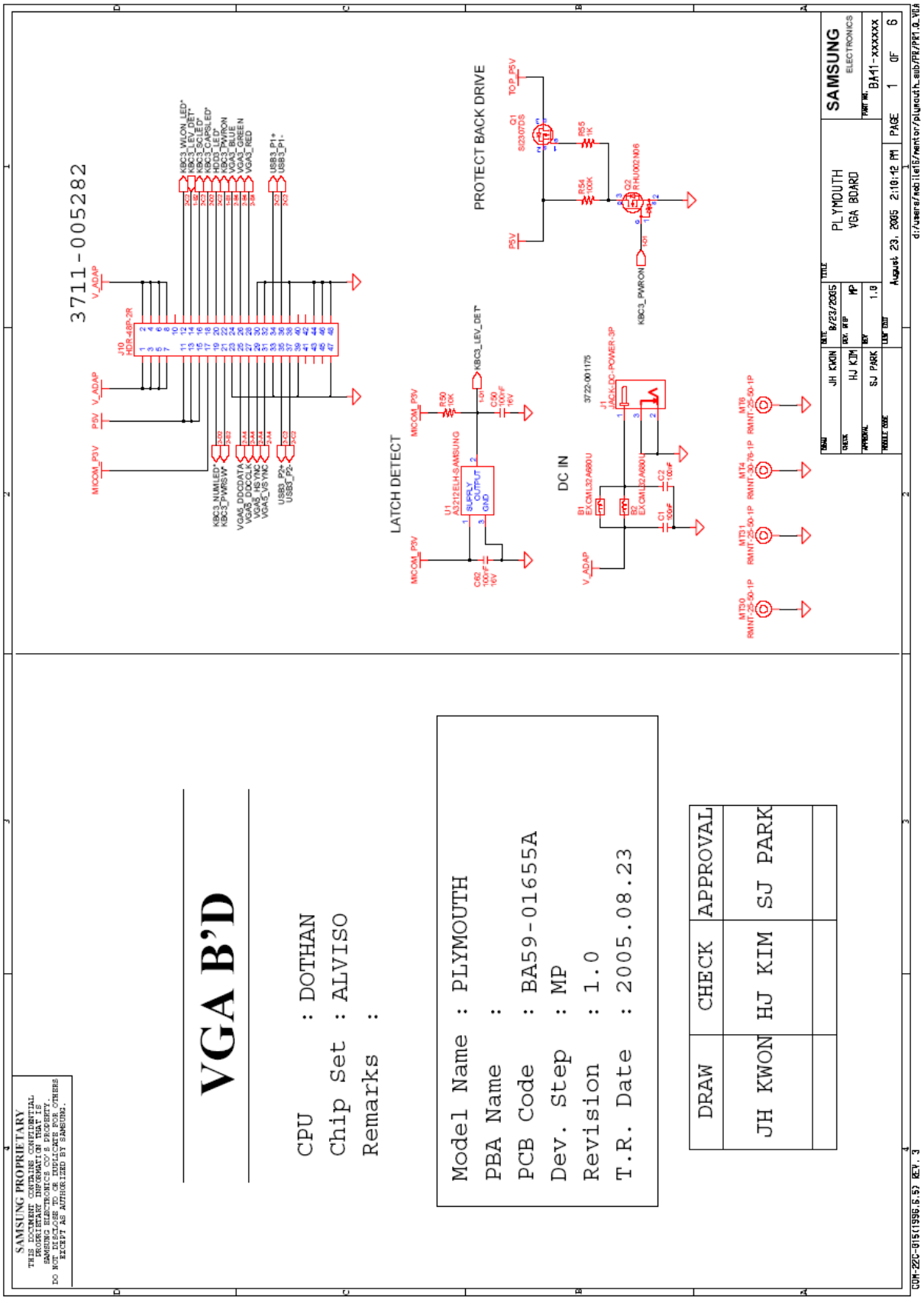
7. Schematic

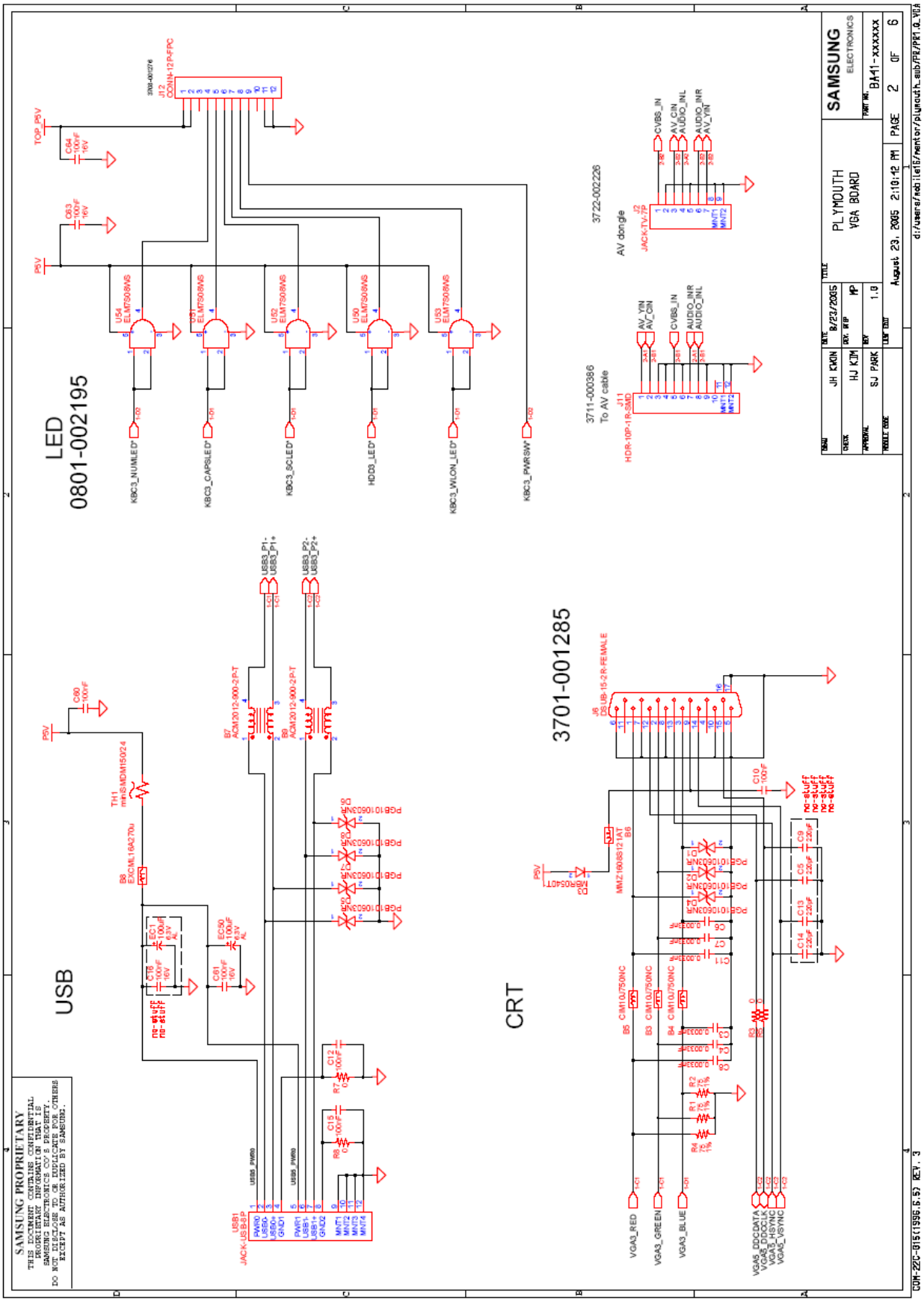


7. Schematic

3) VGA Board

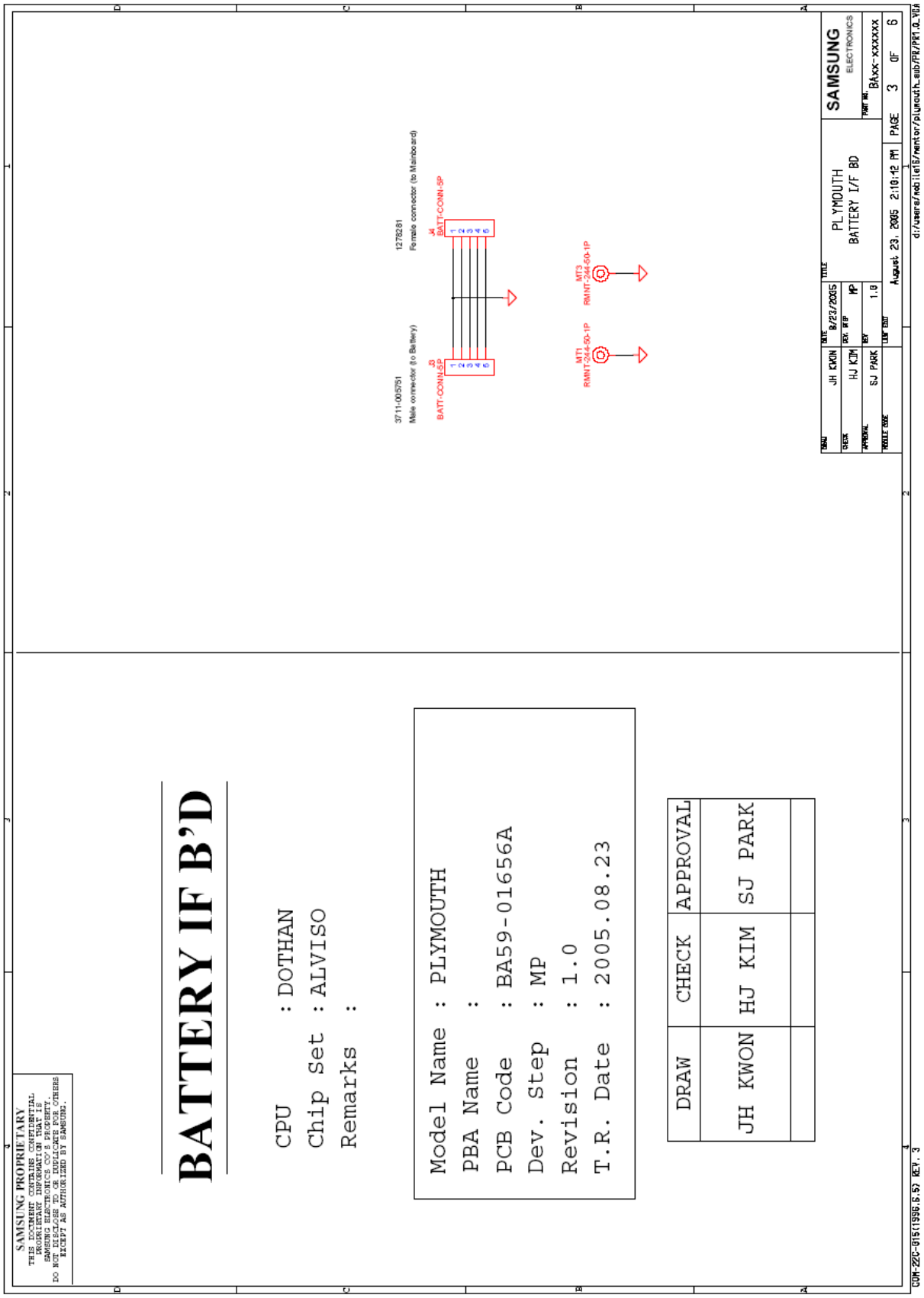


7. Schematic


LED
0801-002195
USB
CRT
3701-001285
3722-002226
AV dongle
3711-000386
To AV cable
PLYMOUTH
VGA BOARD
SAMSUNG
ELECTRONICS
BA41-xxxxxx
August 23, 2005 2:10:12 PM
SAMSUNG PROPRIETARY

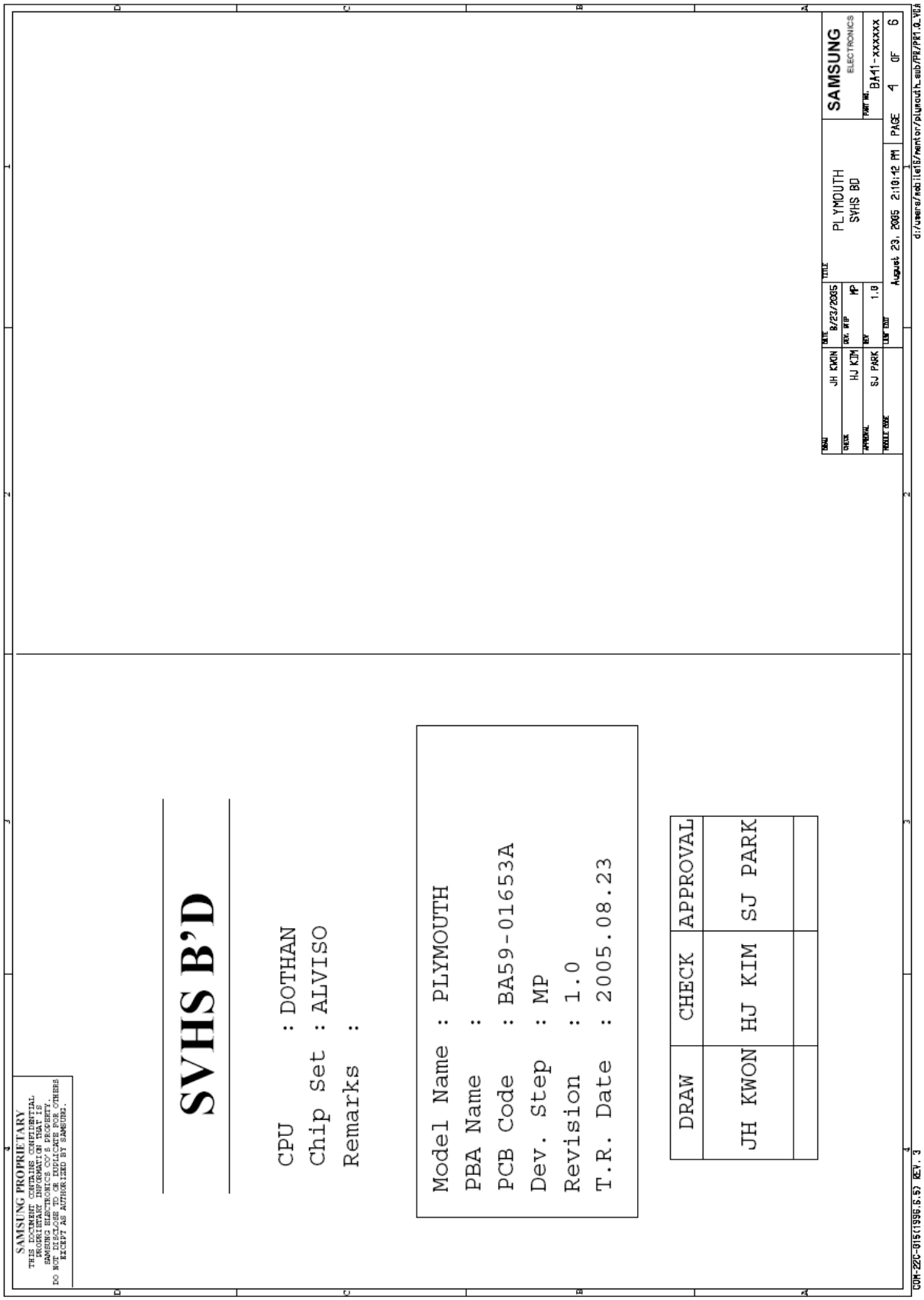
7. Schematic

4) Battery I/F Board

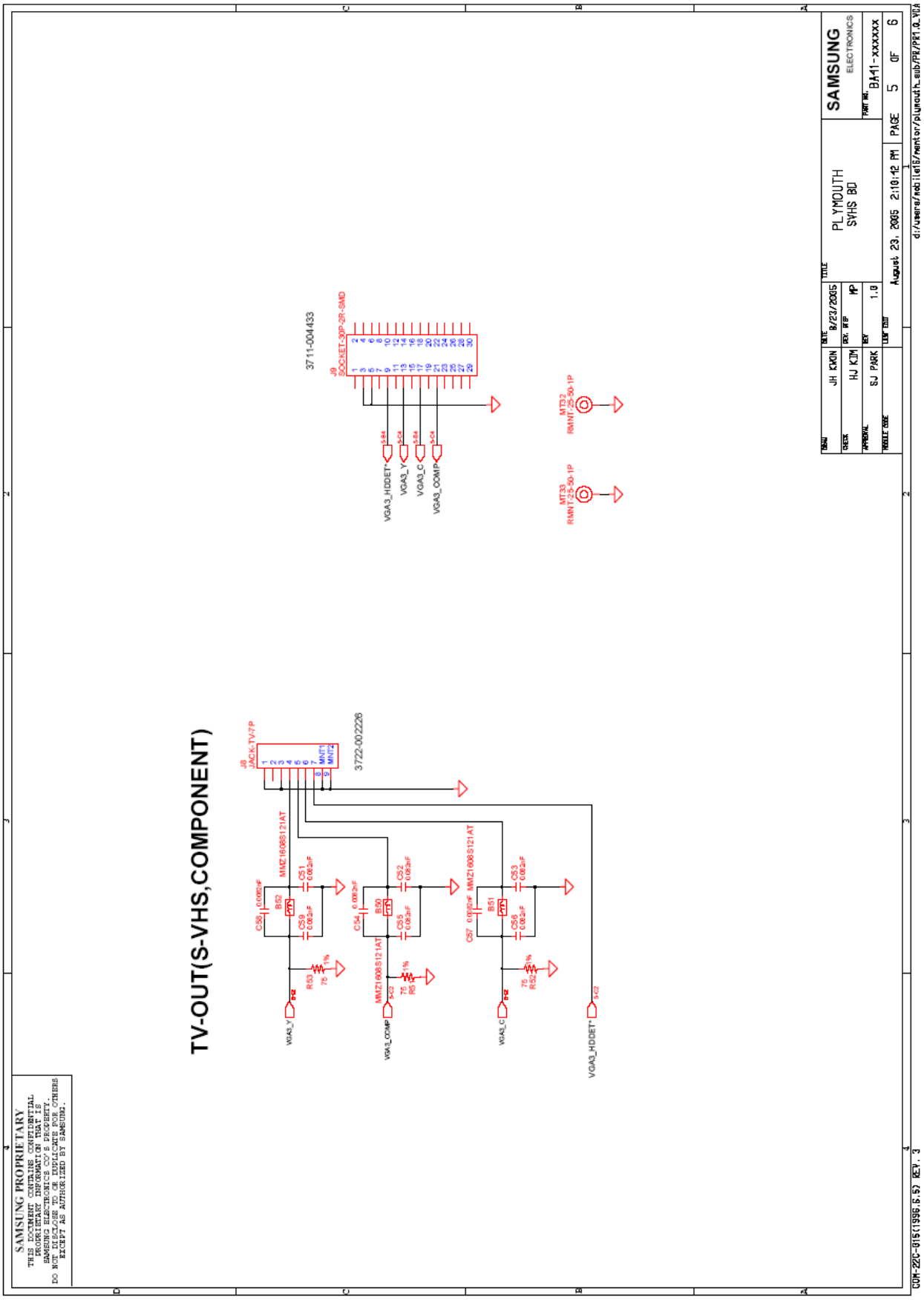


7. Schematic

5) SVHS Board

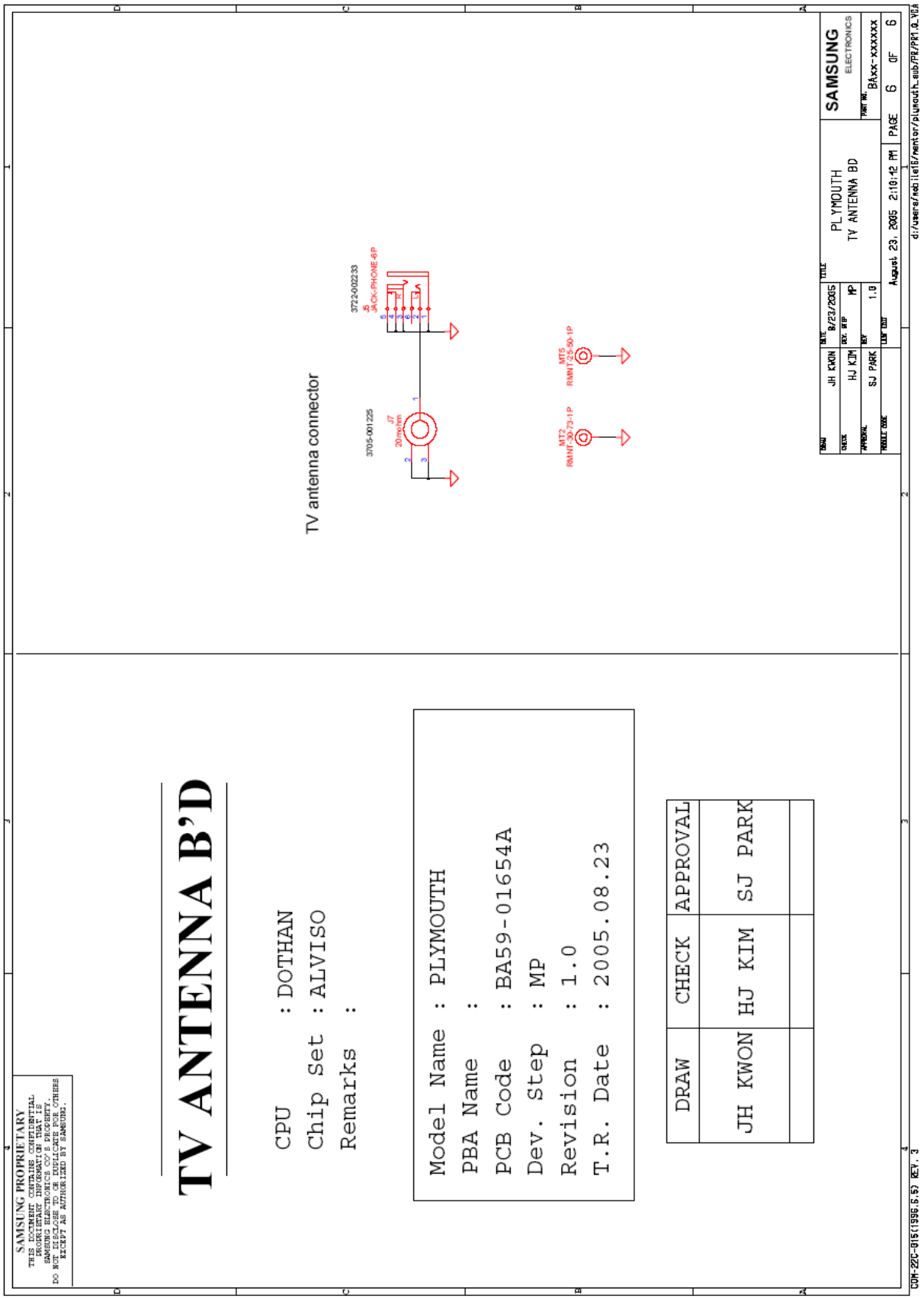


7. Schematic


TV-OUT(S-VHS,COMPONENT)
SAMSUNG PROPRIETARY
PLYMOUTH
SVHS BD
SAMSUNG
ELECTRONICS
BA41-xxxxxx
PAGE 5 OF 6
August 23, 2005 2:10:42 PM
d:/users/mobile15/mentor/plymouth_sub/PB/PB1.0_VGA
3722-002226
3711-004433
VGA3_HDDET*
VGA3_Y
VGA3_C
VGA3_COMP

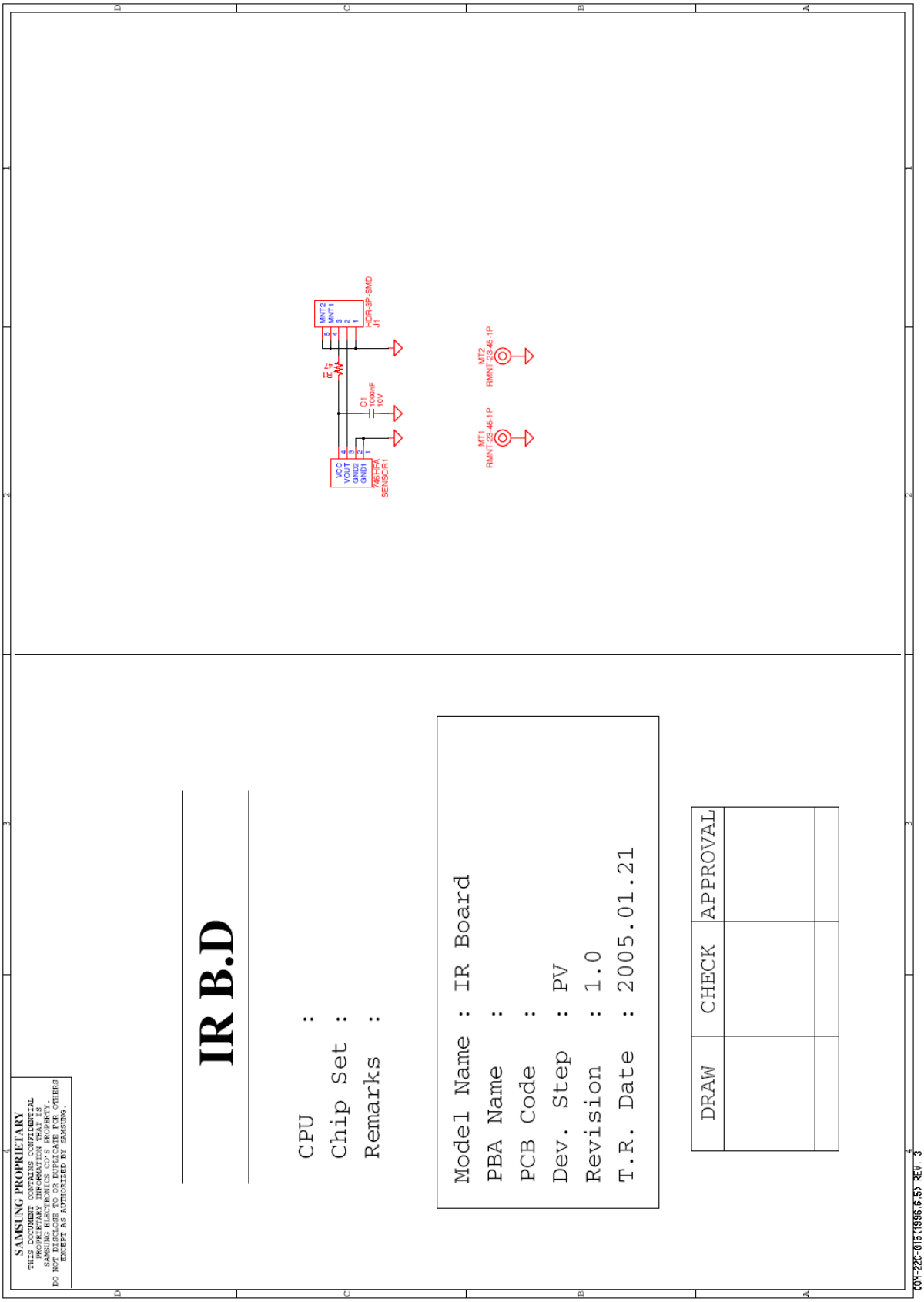
7. Schematic

6) TV Antenna Board



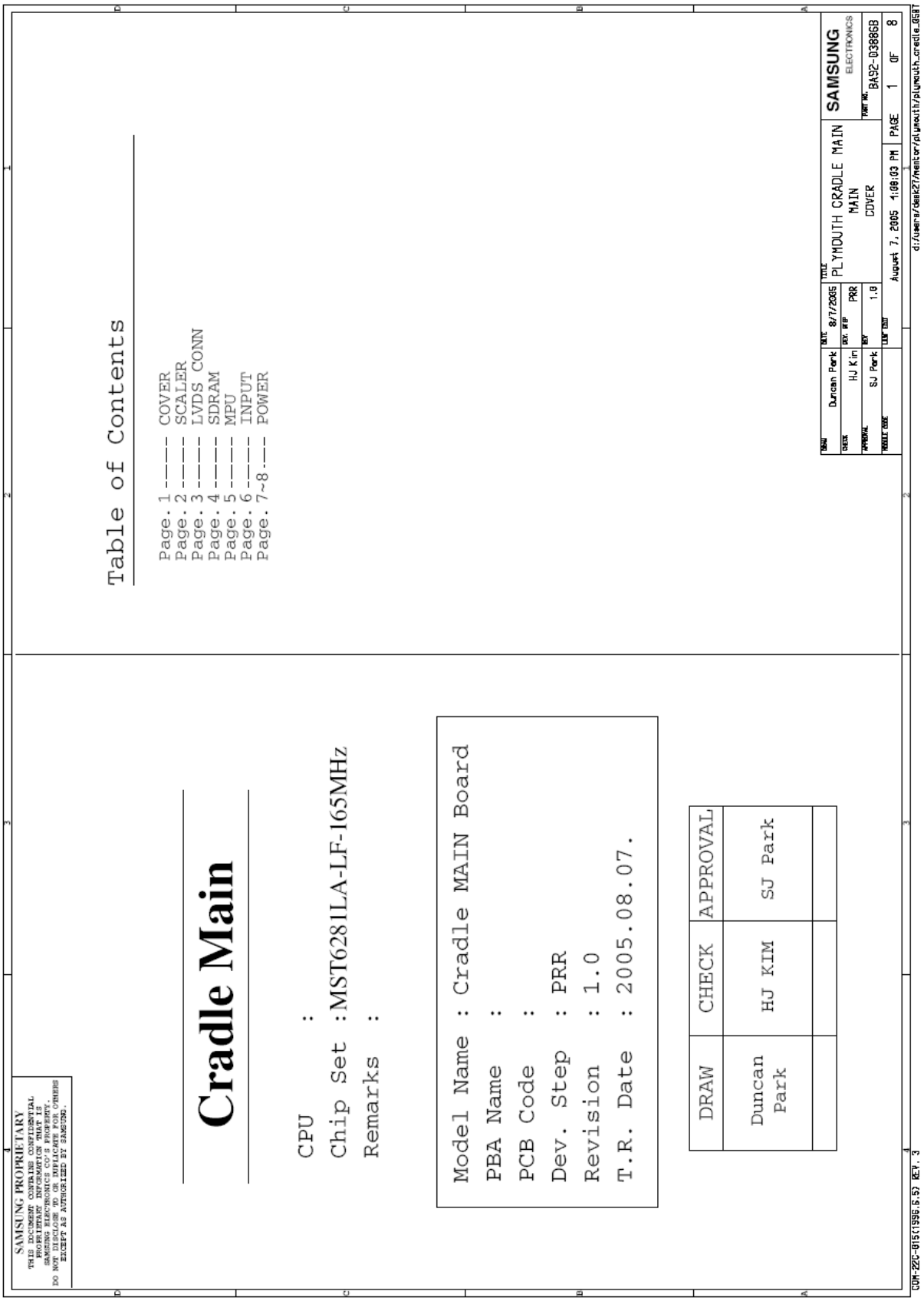
7. Schematic

7) IR Board



7. Schematic

8) Cradle Main Board



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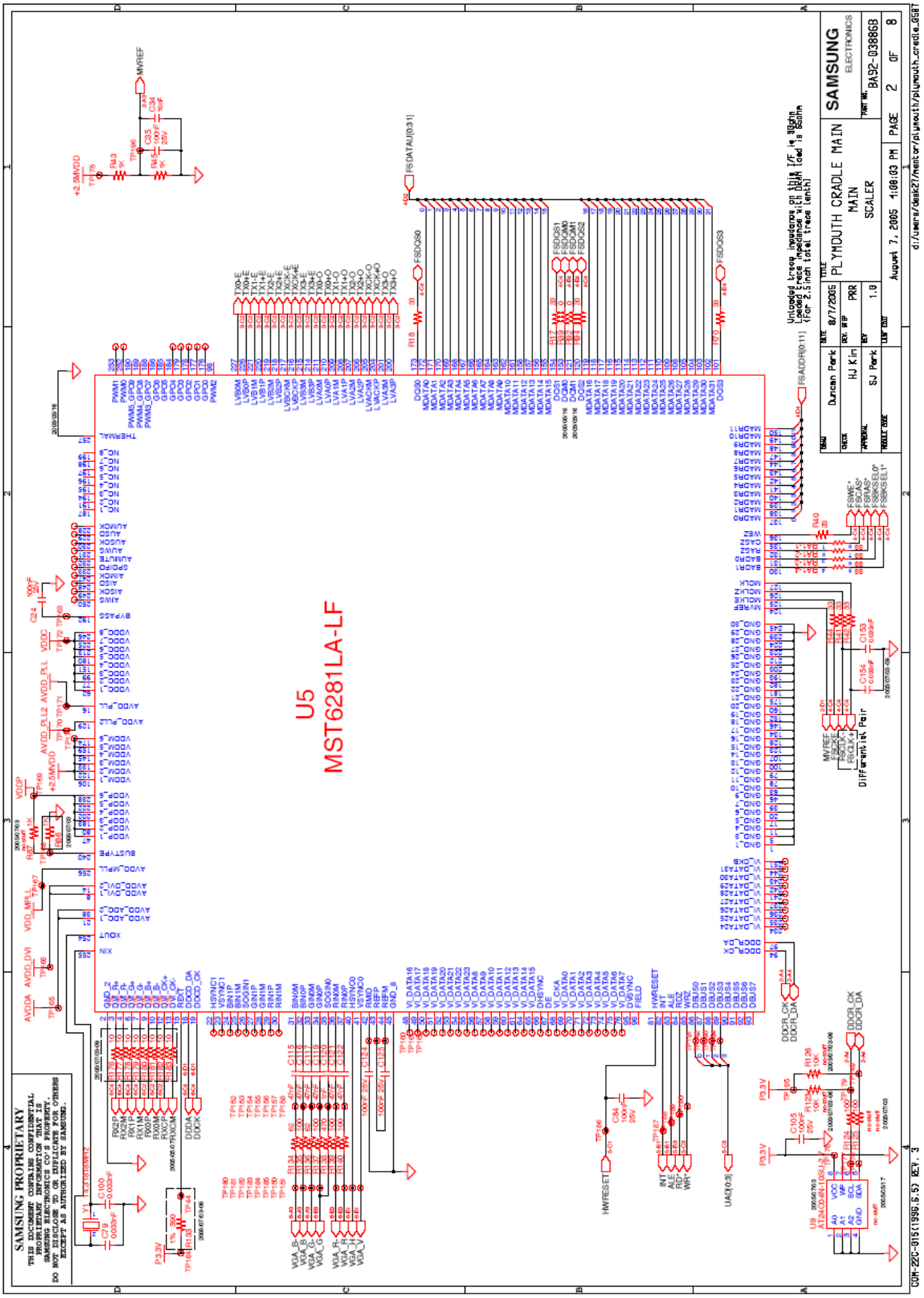
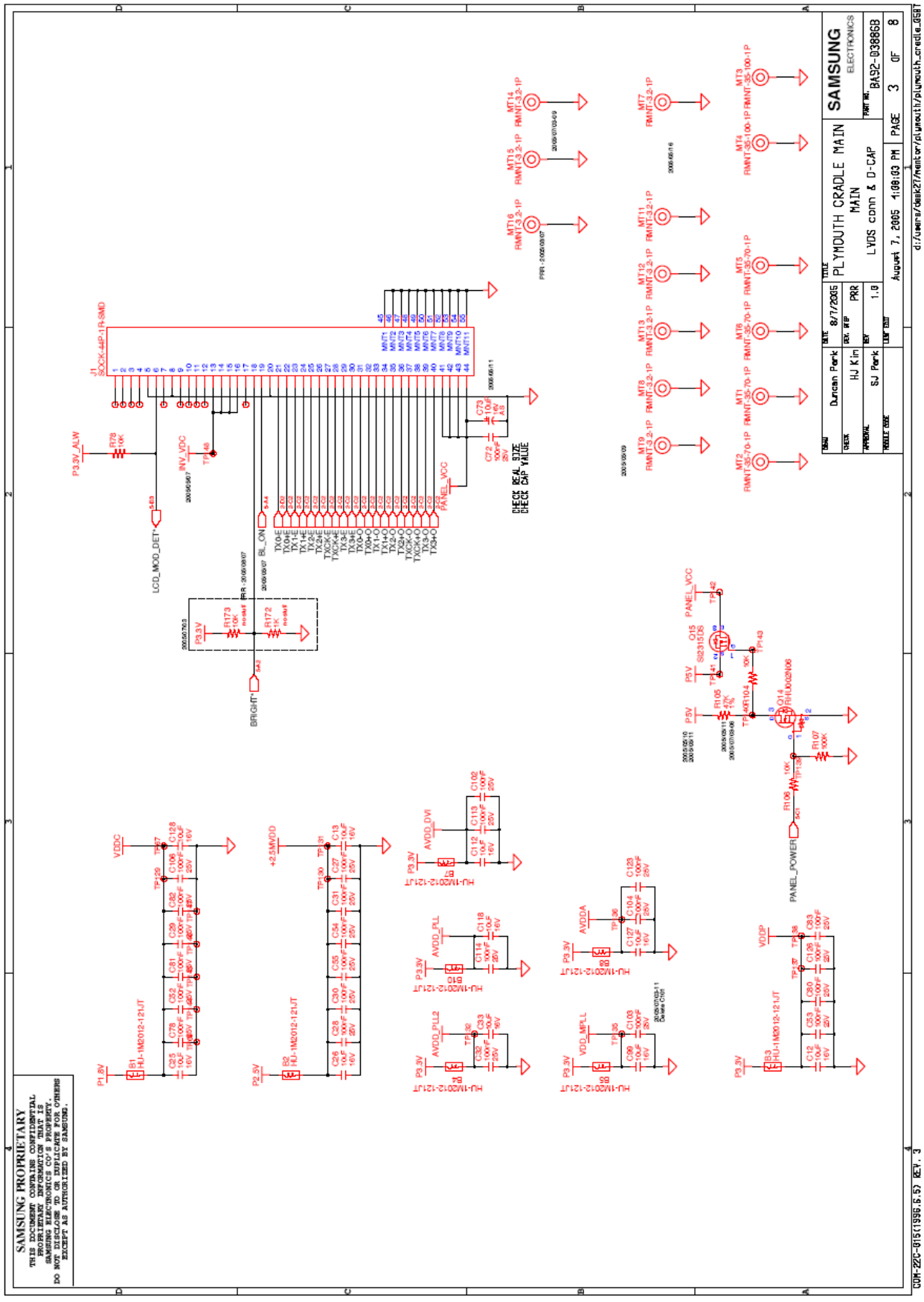
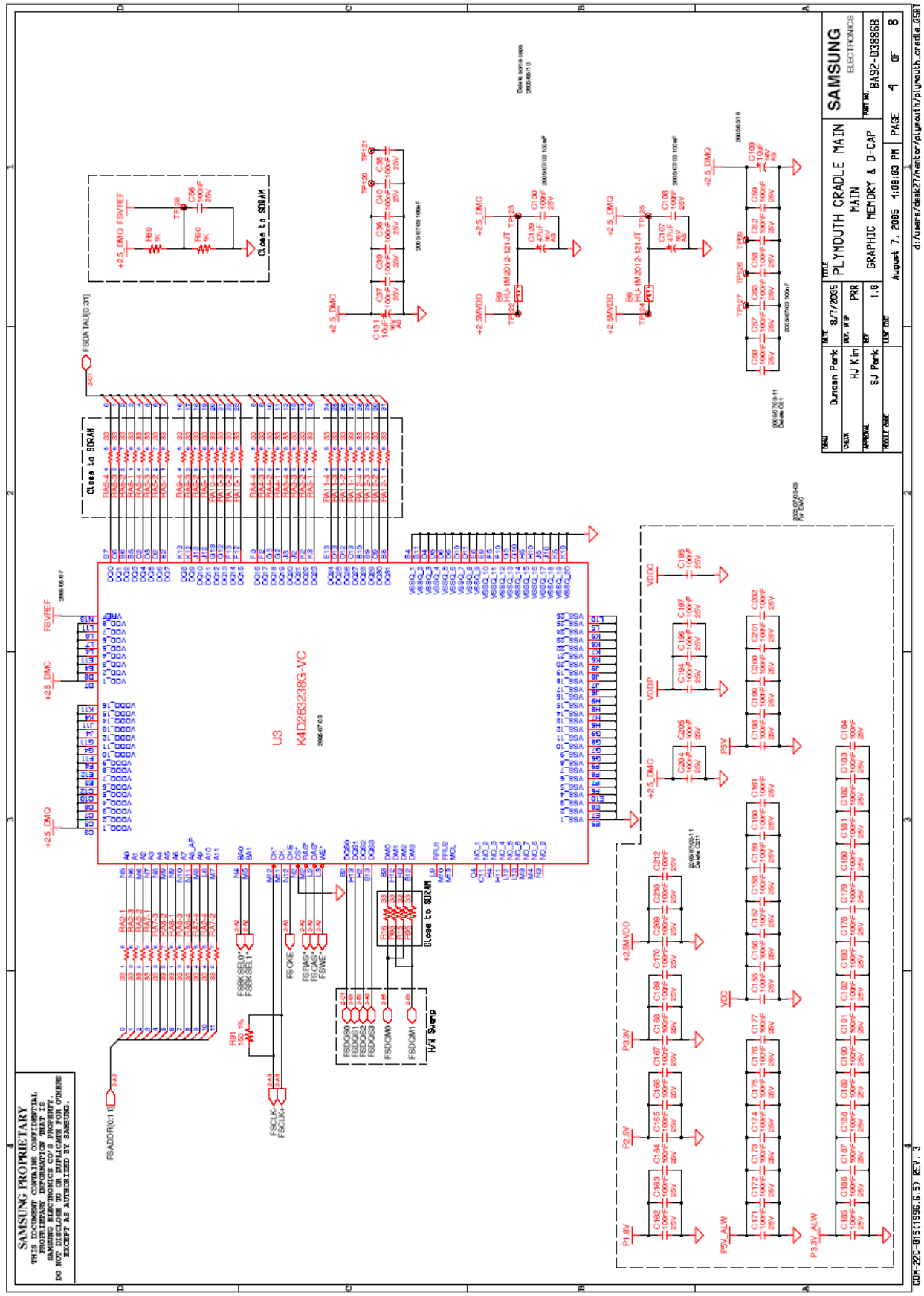
7. Schematic



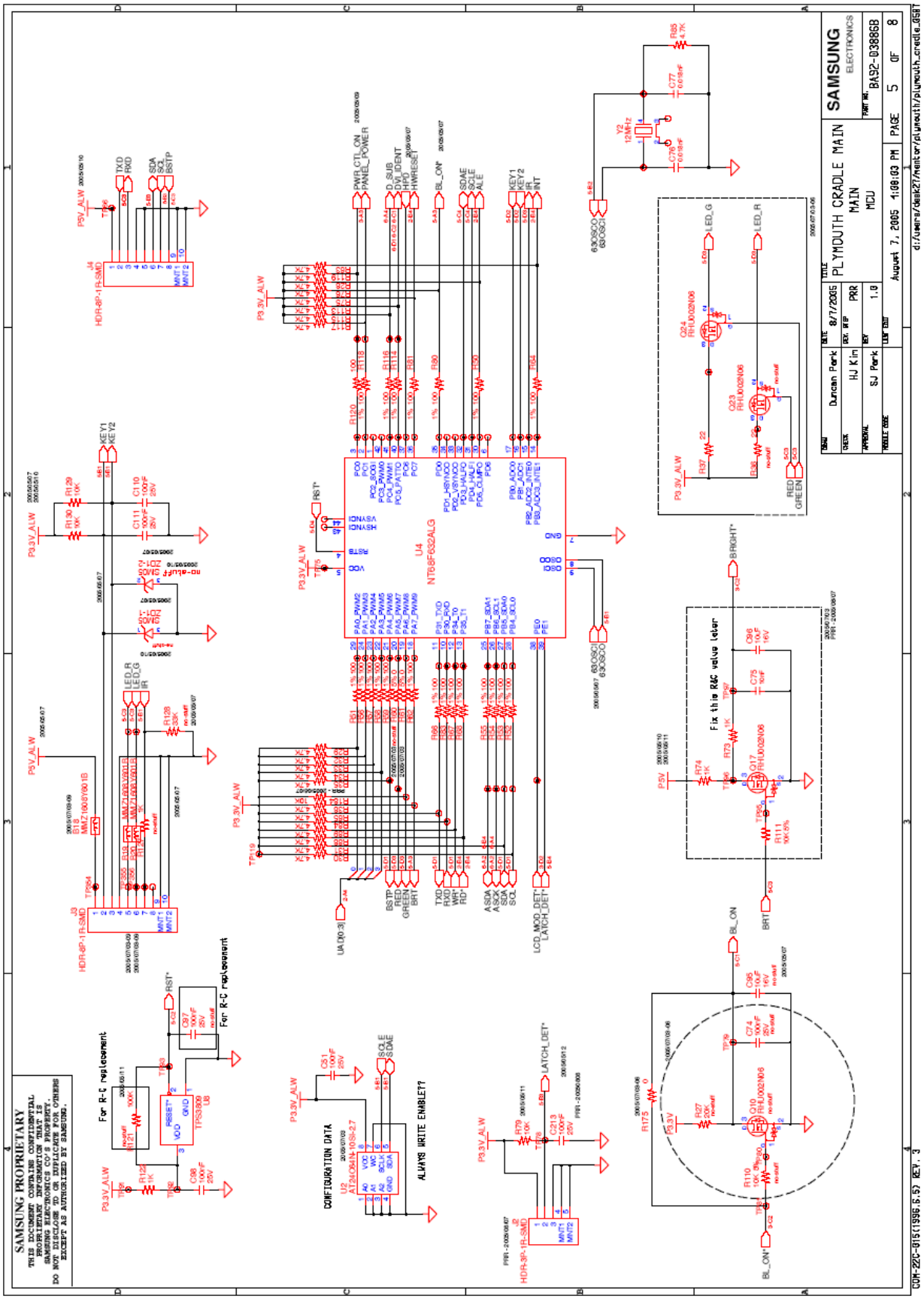
7. Schematic


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
LVDS conn & D-CAP
BA32-03886B
PAGE 3 OF 8
August 7, 2005 4:08:03 PM
d:/users/desk27/mentor/plymouth/plymouth_cradle.dsn
COM-22C-015(996.6.5) REV. 3

7. Schematic


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
GRAPHIC MEMORY & D-CAP
BA32-03886B
August 7, 2005 4:08:03 PM
PAGE 4 OF 8
d:/users/desk27/mentor/plymouth/plymouth_cradle.dsn
U3
K4D263238G-VC
FSADDR[0:11]
FSDATA[0:31]
FSCKE
FSRAS*
FSCAS*
FSWE*
FSDQM0
FSDQM1
FSDQM2
FSDQM3
FSCLK-
FSCLK+
FSVREF
+2.5_DMC
+2.5_DMO
+2.5MVDD
P1.8V
P2.5V
P3.3V
P3.3V_ALW
P5V
P5V_ALW
VDDC
VDDP
Close to SDRAM
H/I Swamp

7. Schematic


SAMSUNG
ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
MCU
BA92-03886B
August 7, 2005 1:08:03 PM
PAGE 5 OF 8
Duncan Park 8/7/2005
HJ Kim PRR
SJ Park 1.0
d:/users/deak27/mentor/plymouth/plymouth_cradle.dsbt
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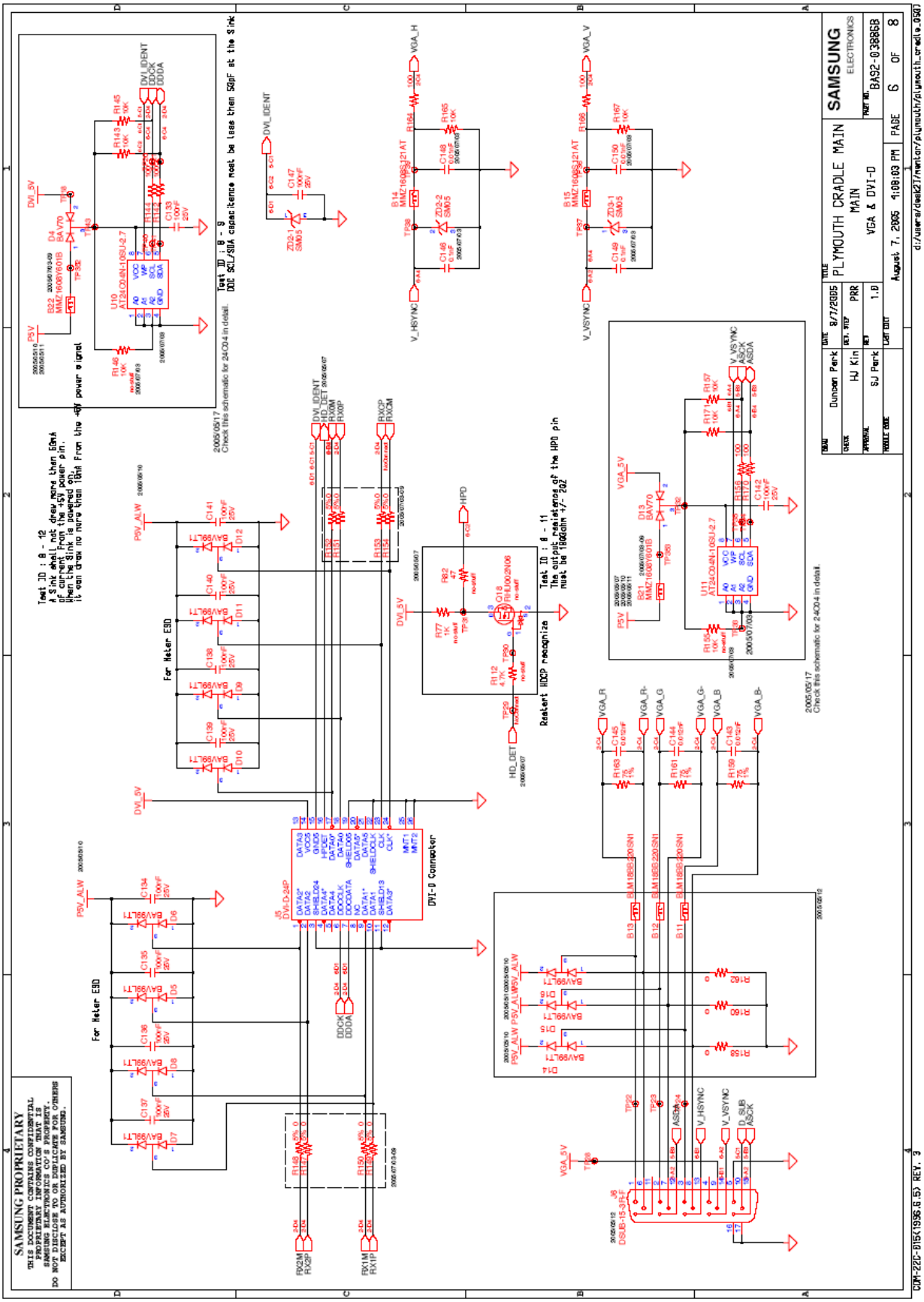
U4
NT68F632ALG
U2
AT24C64A-10SE-2.7
CONFIGURATION DATA
ALWAYS WRITE ENABLE??
For R-C replacement
For R-C replacement
Fix this R&C value later
U8
TPS3809
U6
HDR-8P-1R-SMD
HDR-3P-1R-SMD
J4
J3
J2
PWR_CTL_ON
PANEL_POWER
D_SUB
DVI_IDENT
HPD
HWRESET
BL_ON*
SDAE
SCLE
ALE
KEY1
KEY2
INT
RST*
TXD
RXD
SDA
SCL
BSTP
BRT
LED_R
LED_G
IR
LCD_MOD_DET*
LATCH_DET*
BL_ON
P5V_ALW
P3.3V_ALW
P3.3V
Y2
12MHz
RED
GREEN

7. Schematic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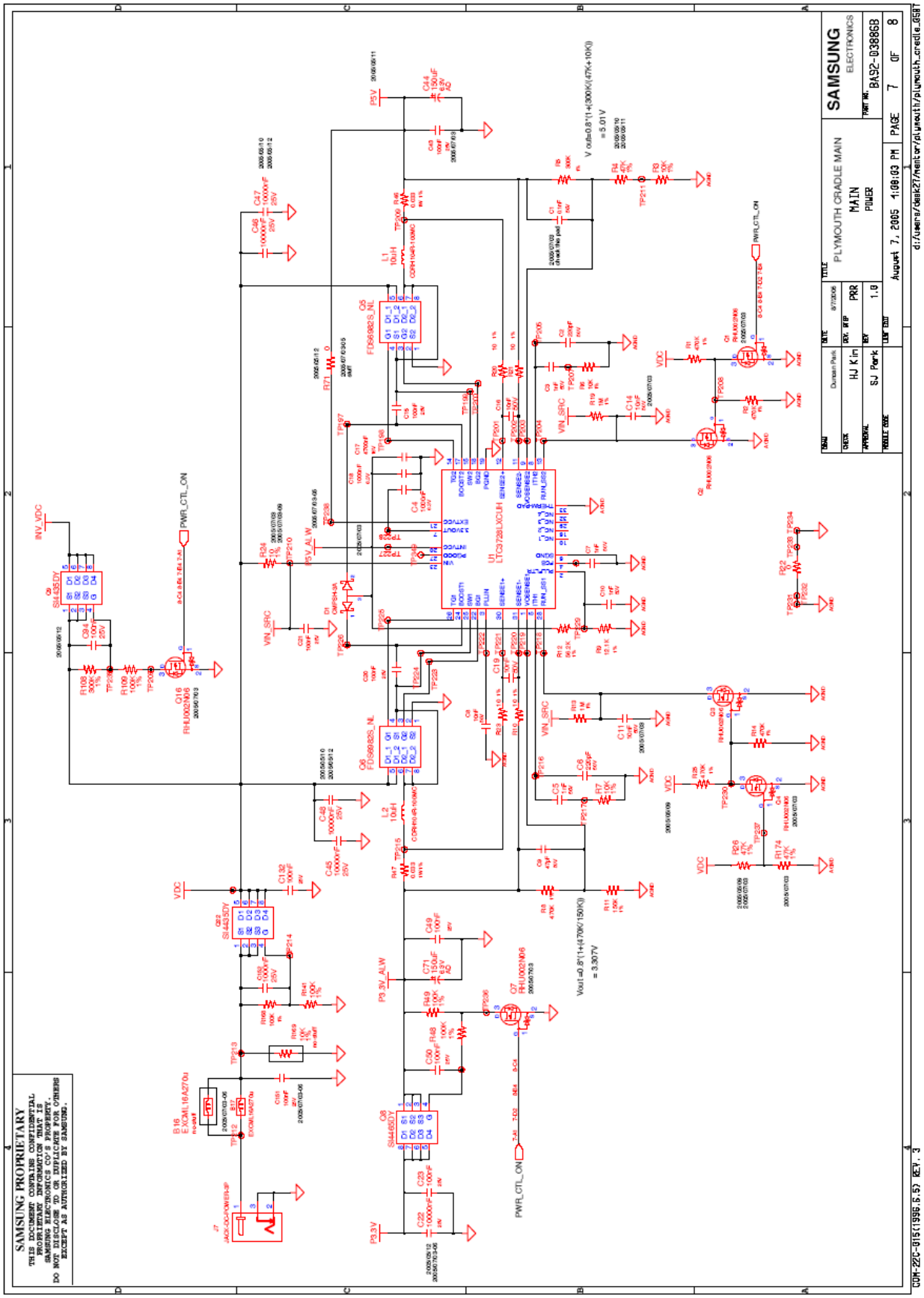
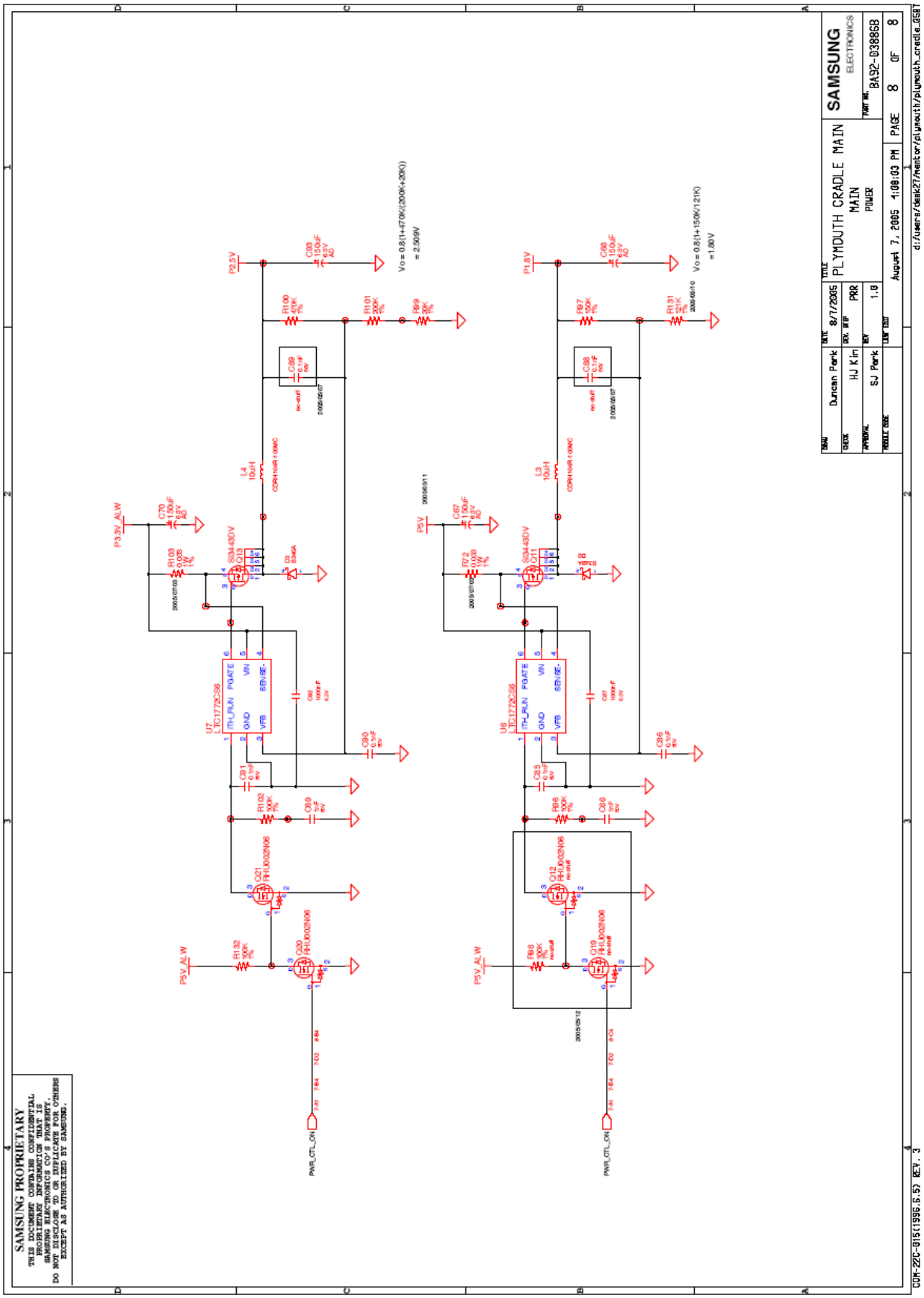
SAMSUNG ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
VGA & DVI-D
PART NO. BA92-03868B
PAGE 6 OF 8
DRAW Dunsan Park 8/17/2005
CHECK HJ Kim REV. STEP PRR
APPROVAL SJ Park REV 1.0
MODEL CODE LAST EDIT August 7, 2005 1:08:03 PM
d:/users/desk27/monitor/plymouth/plymouth_crad1e.dsn
For Meter ESD
DVI-D 24P
DDC SCL/SDA capacitance must be less then 50pF at the Sink
Restart HDCP recognize
Test ID : 8 - 11
The output resistance of the HPD pin must be 1800ohm +/- 20%
Test ID : 8 - 12
A Sink shall not draw more than 50mA of current from the +5V power pin.
When the Sink is powered on, it can draw no more than 10mA from the +5V power signal.
Test ID : 8 - 9
DDC SCL/SDA capacitance must be less then 50pF at the Sink
2005/05/17
Check this schematic for 24C04 in detail.

7. Schematic


SAMSUNG PROPRIETARY
SAMSUNG
ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
POWER
BA92-03886B
August 7, 2005 1:08:03 PM
PAGE 7 OF 8
HJ Kim
SJ Park
PRR
1.0
d:/users/desk27/mentor/plymouth/plymouth_cradle.dsn
INV_VDC
PWR_CTL_ON
VIN_SRC
P3V_ALW
P3.3V
VDC
PSV
PSV_ALW
Vout=0.8*(1+(470K/150K))
= 3.307V
V out=0.8*(1+(300K)/(47K+10K))
= 5.01 V

7. Schematic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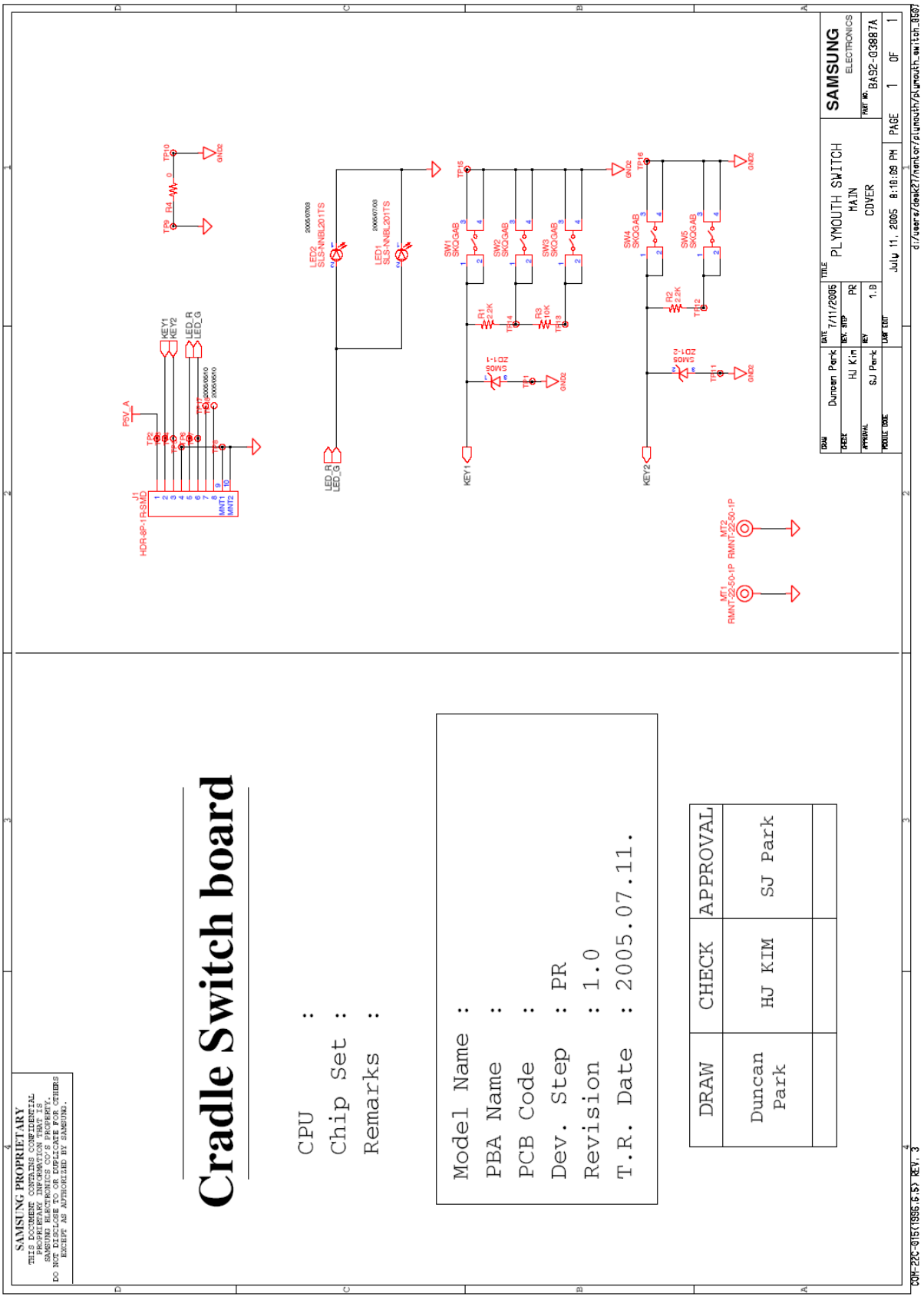
SAMSUNG ELECTRONICS
PLYMOUTH CRADLE MAIN
MAIN
POWER
BA92-03886B
August 7, 2005 4:08:03 PM
PAGE 8 OF 8
Duncan Park 8/7/2005 PRR
HJ Kim
SJ Park 1.0
d:/users/desk27/mentor/plymouth/plymouth_cradle.dsn
COM-22C-015(1996.5.5) REV. 3

7. Schematic

9) Cradle Switch Board