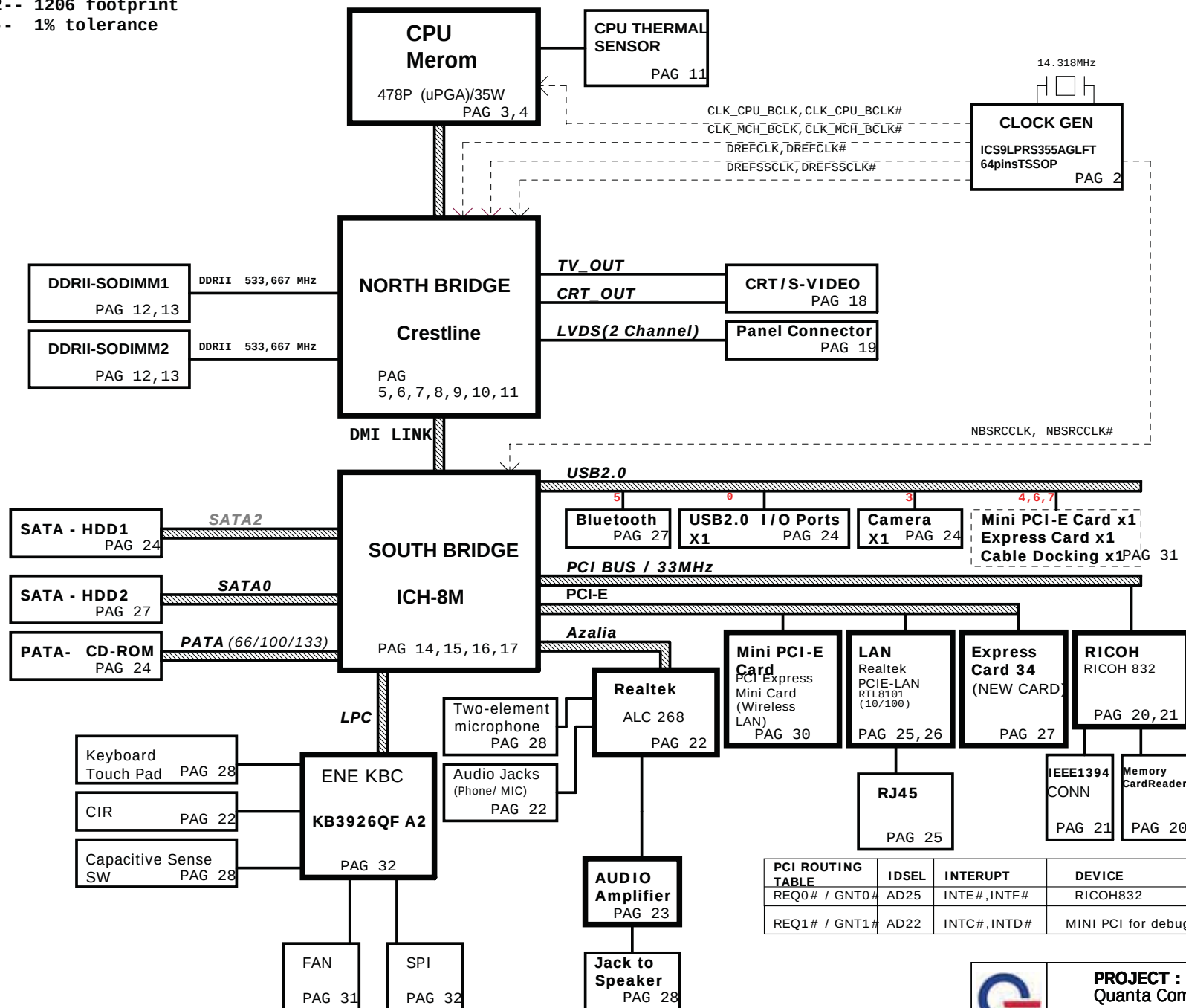


PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

```
04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance
```

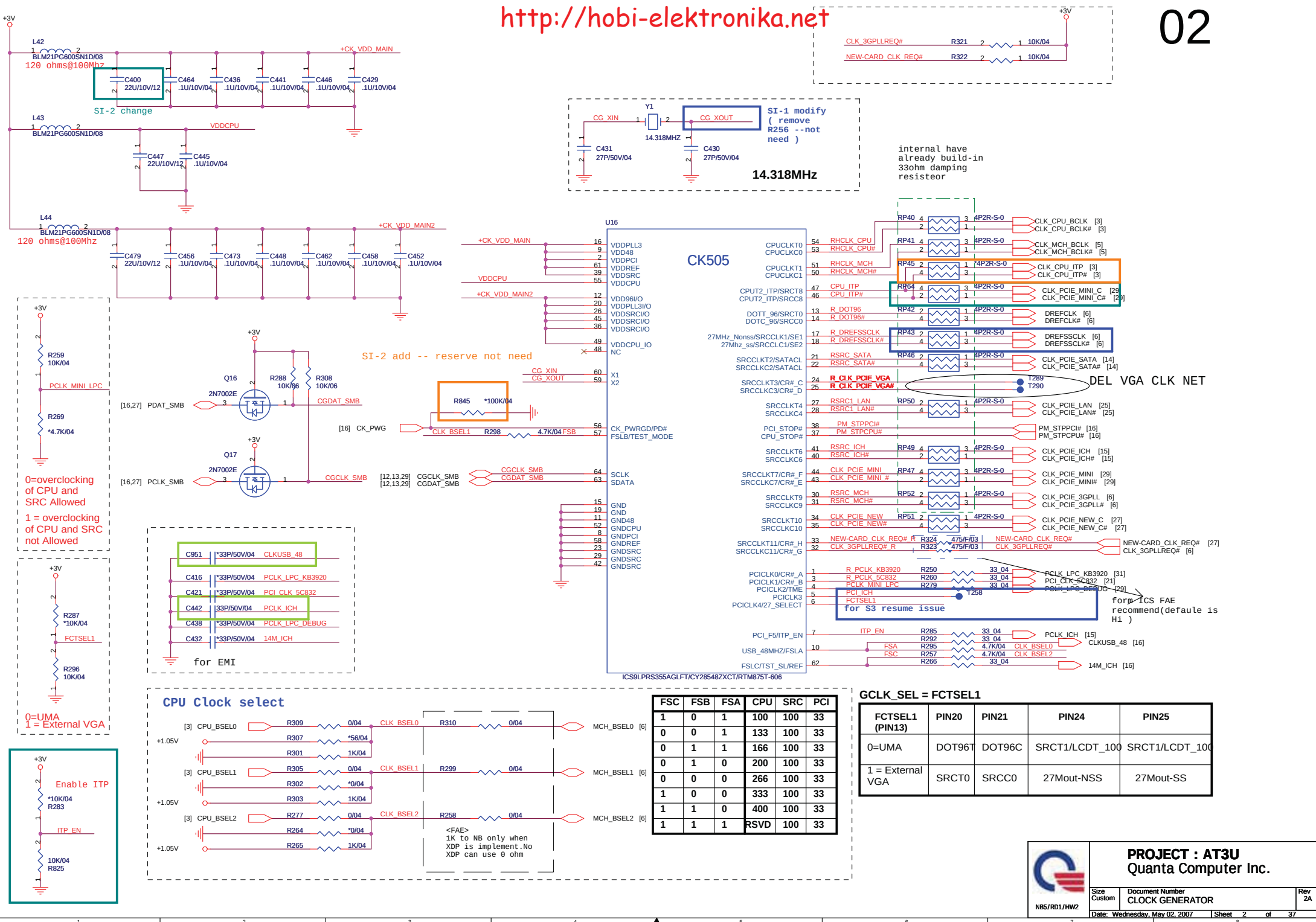


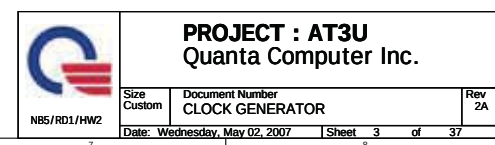
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

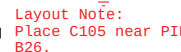
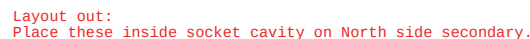


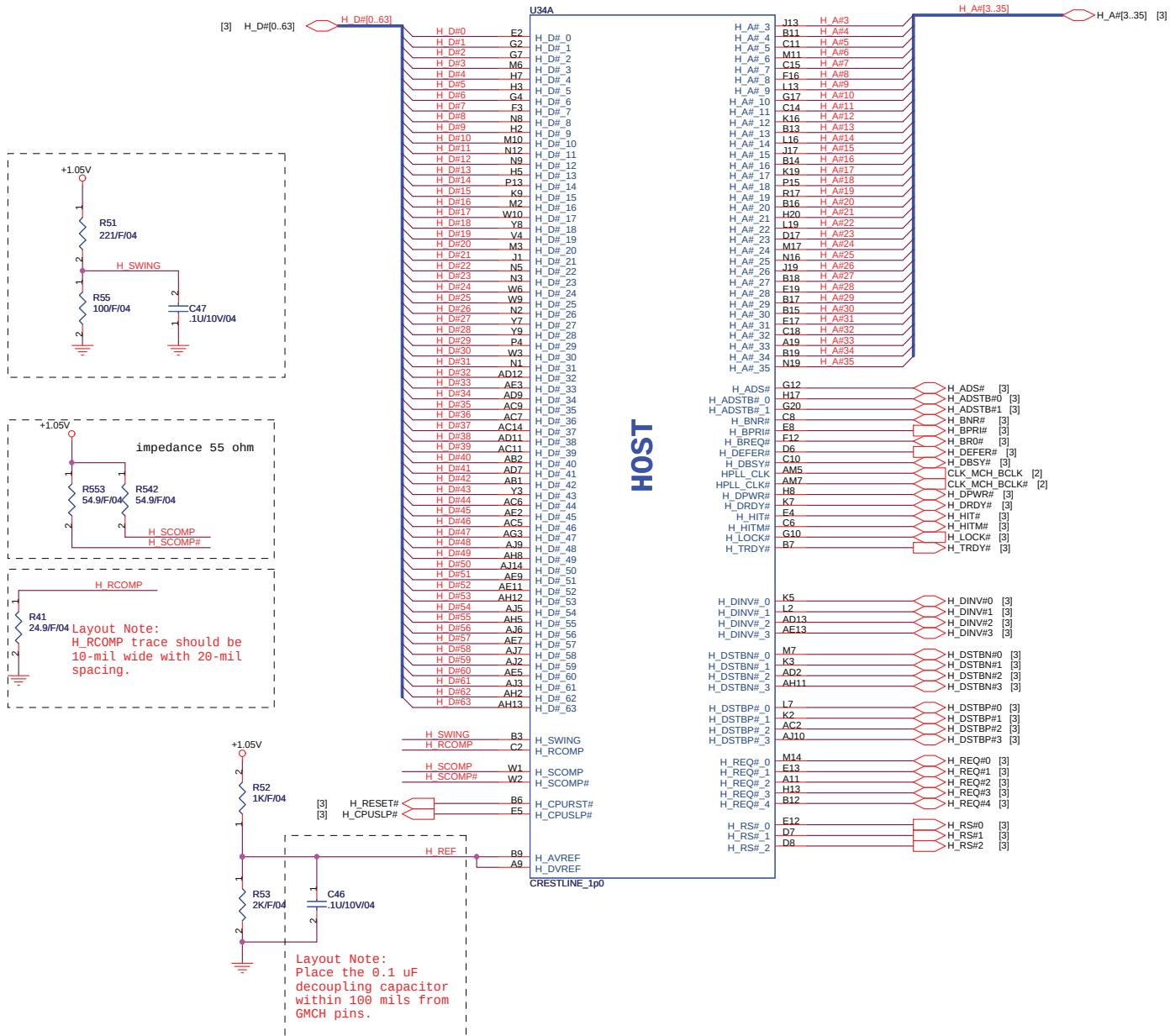
PROJECT : AT3U
Quanta Computer Inc.

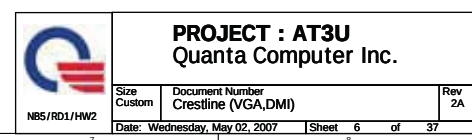
Size Custom	Document Number BLOCK DIAGRAM	Rev 2A
Date: Monday, April 30, 2007		Sheet 1 of 37

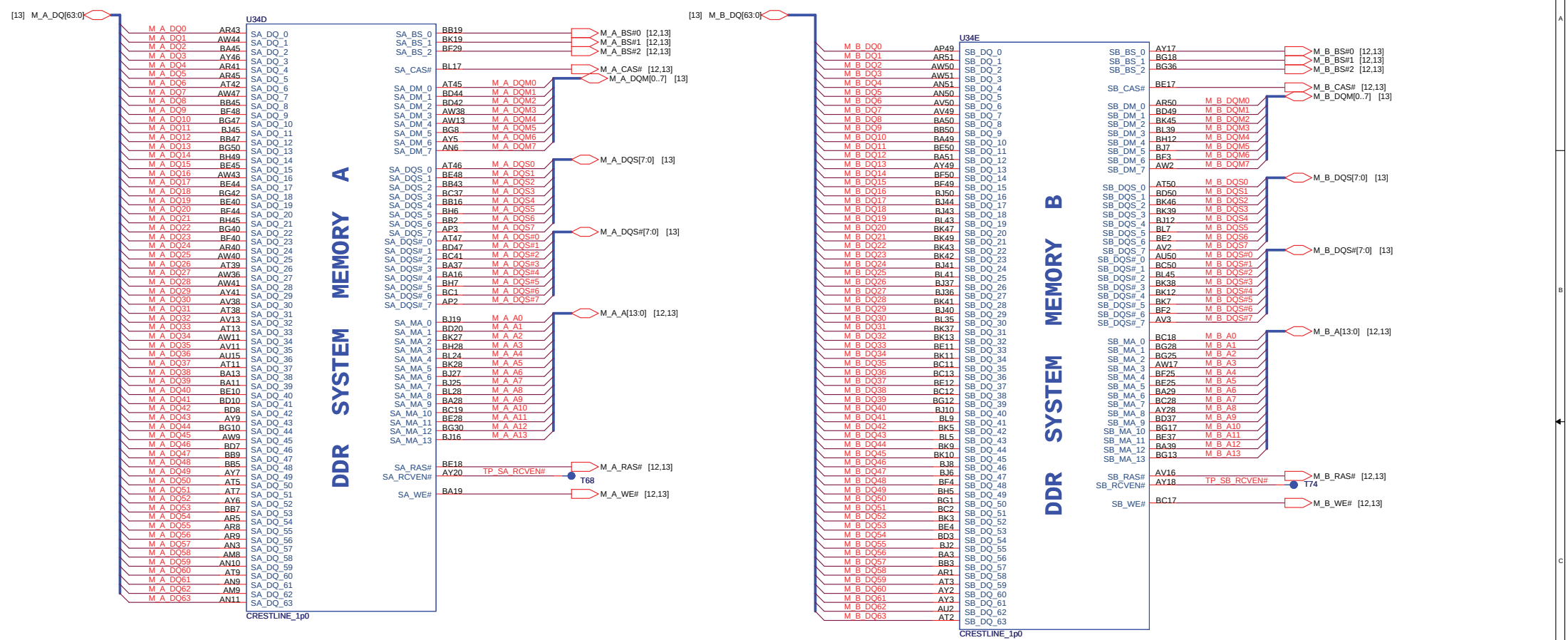






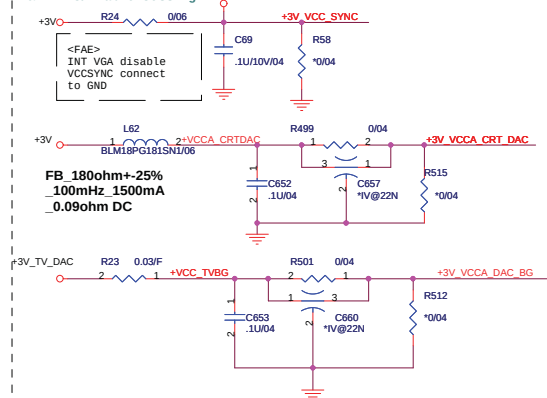




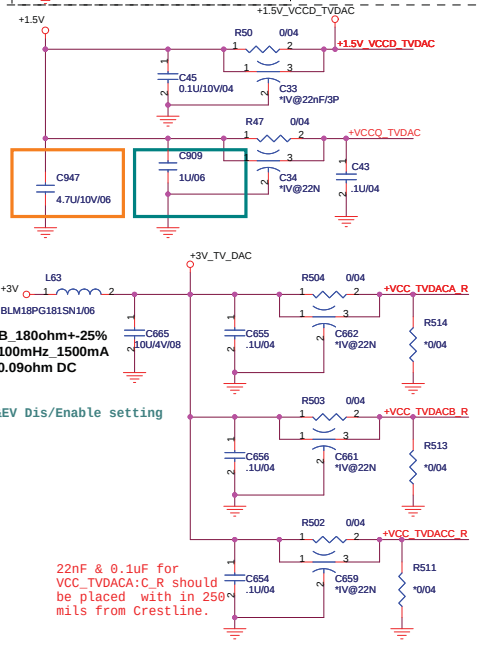
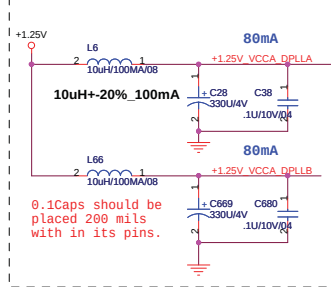
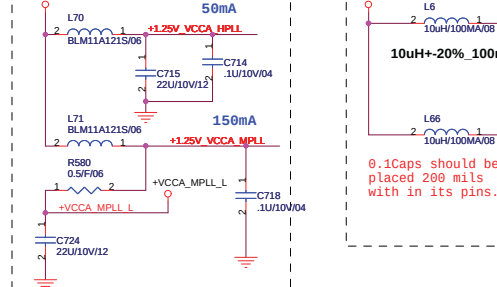




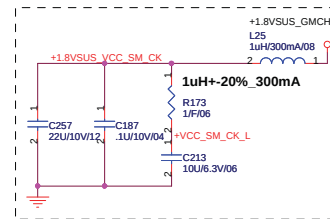
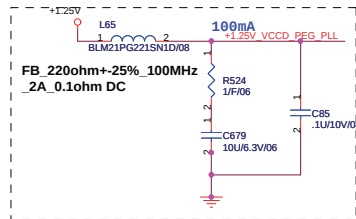
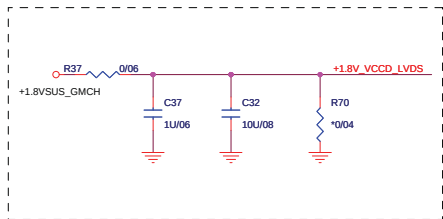
IV&EV Dis/Enable setting +3V_VCCSYN



FB_120ohm+-25%_100mHz		
+1.25V_200mA_0.2ohm DC		+1.25V



22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.



CRT/TV Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

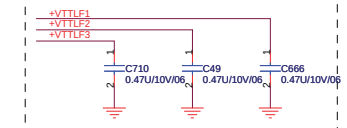
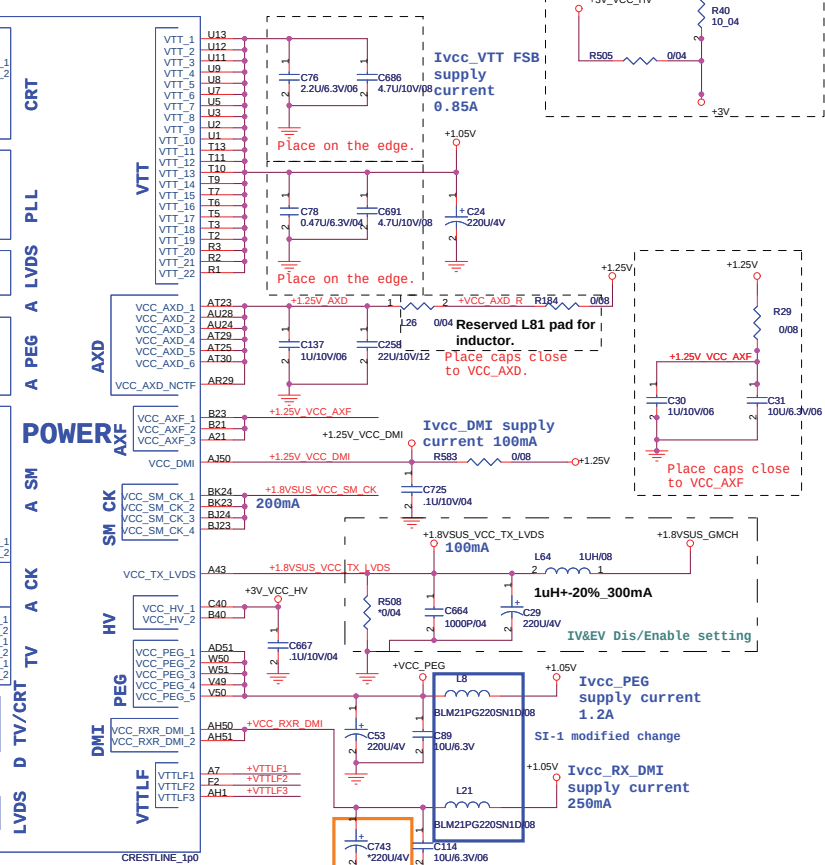
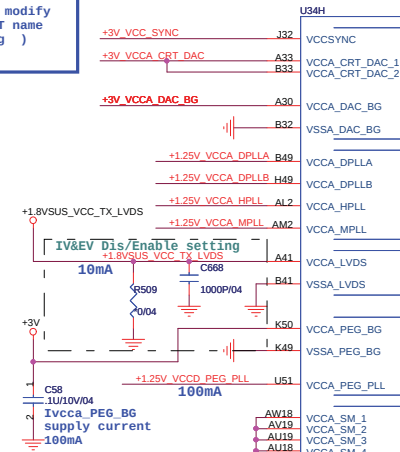
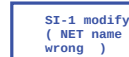
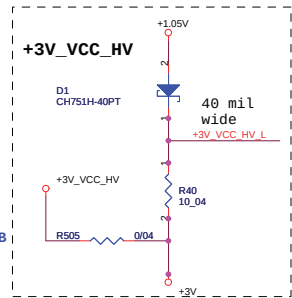
Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

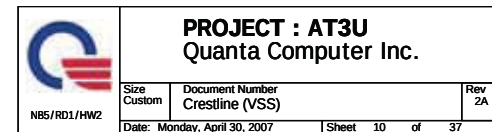
Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

9



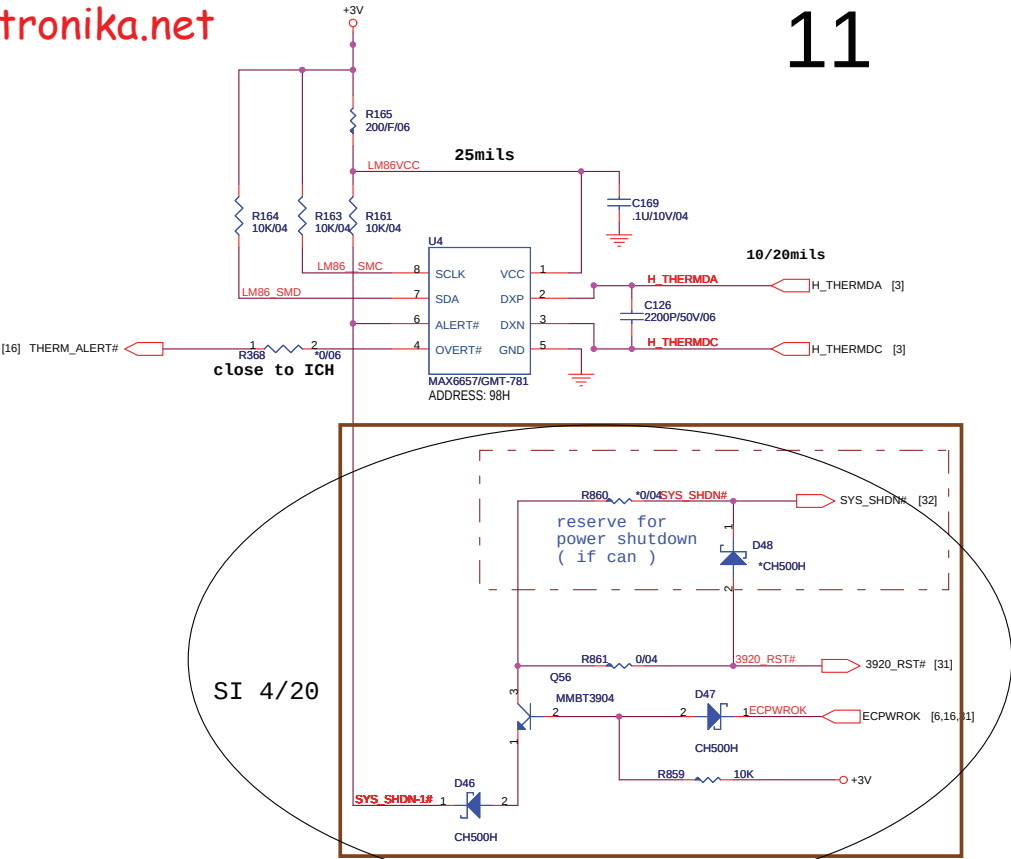
PROJECT : AT3U
Quanta Computer Inc.

Size Custom	Document Number Crestline (POWER)	Rev 2A
Date: Monday, April 30, 2007		Sheet 9 of 37



All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMI X4(Default)
-----------	--



FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--



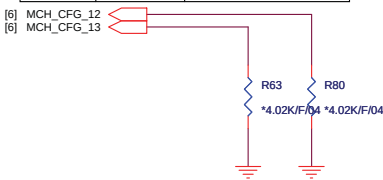
SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
------------	---



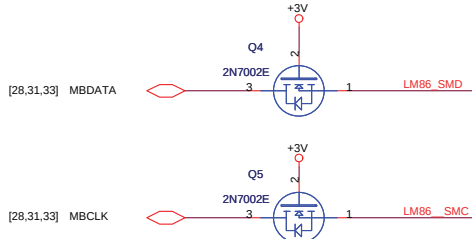
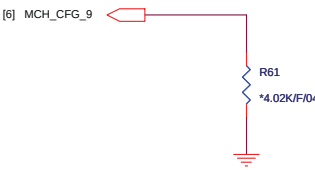
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

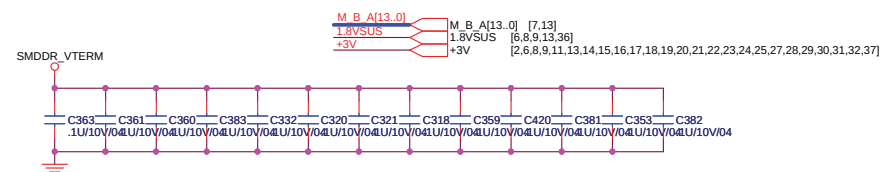
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--



SDVO Present

Strap define at External DVI control page

DDRII B CHANNEL



[6.13] M_A_ODT0

M A ODT0	RP21	1	2	56X2
M A A13		3	4	
M A A8	RP13	1	2	56X2
M A A5		3	4	
M A A3	RP14	1	2	56X2
M A A1		3	4	

SMDRR_VTERM

[6.13] M_A_CKE1

M A CKE1	RP23	1	2	56X2
M A A11		3	4	
M A A10	RP15	1	2	56X2
M A BS#0		3	4	

[7.13] M_A_BS#0

M A BS#0	RP24	1	2	56X2
M A A7		3	4	
M A A6		1	2	
M A A2	RP18	1	2	56X2
M A A4		3	4	

SMDRR_VTERM

[7.13] M_A_RAS#

M A RAS#	RP20	1	2	56X2
M A BS#1		3	4	
M A A9	RP22	1	2	56X2
M A A12		3	4	

[7.13] M_A_WE#

M A WE#	RP16	1	2	56X2
M A CAS#		3	4	

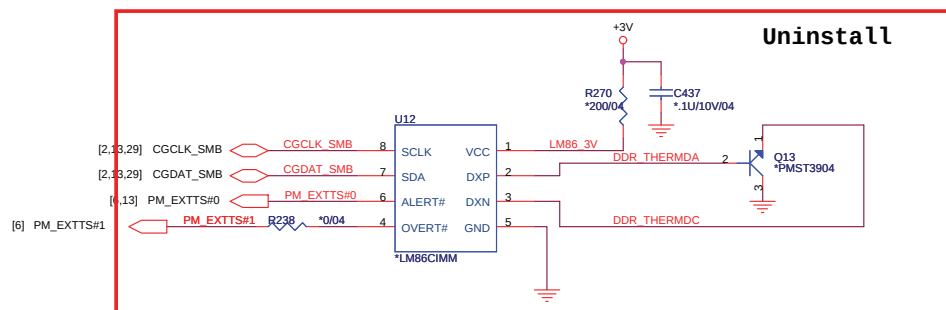
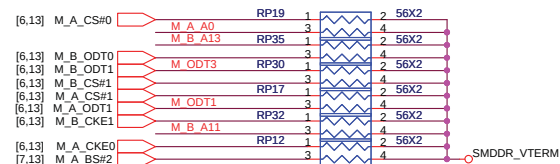
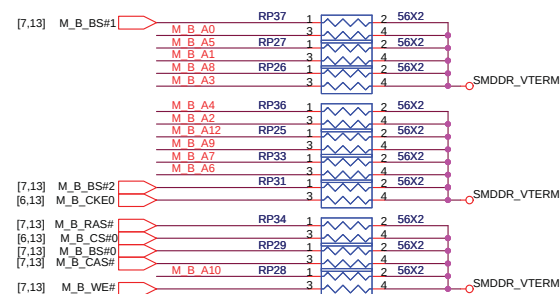
SMDRR_VTERM

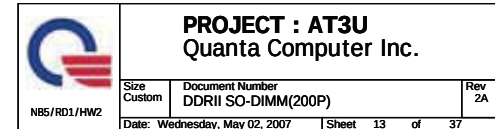
[6.13] SA_MA14

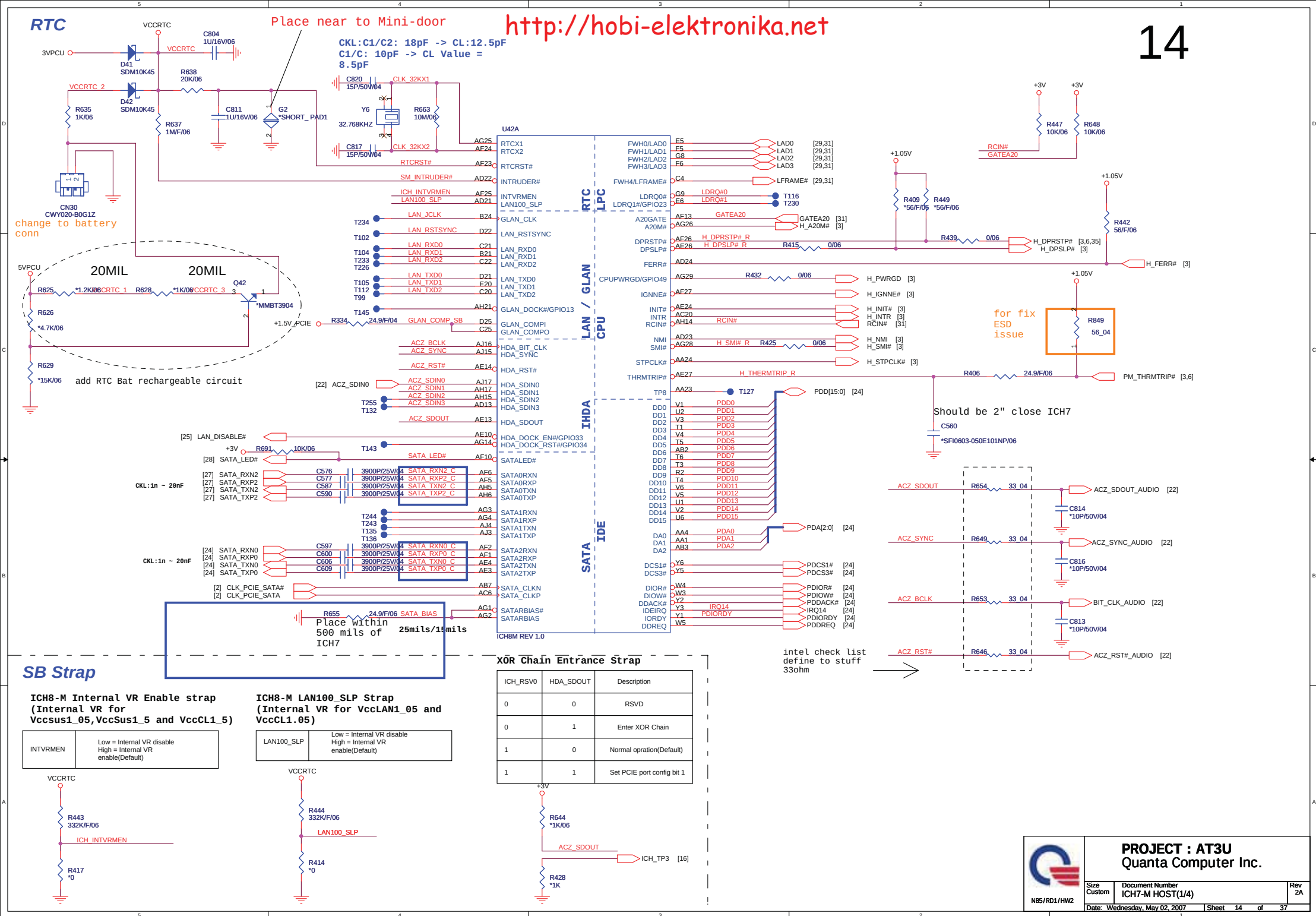
[6.13] SB_MA14

	R742	56_04
	R743	56_04

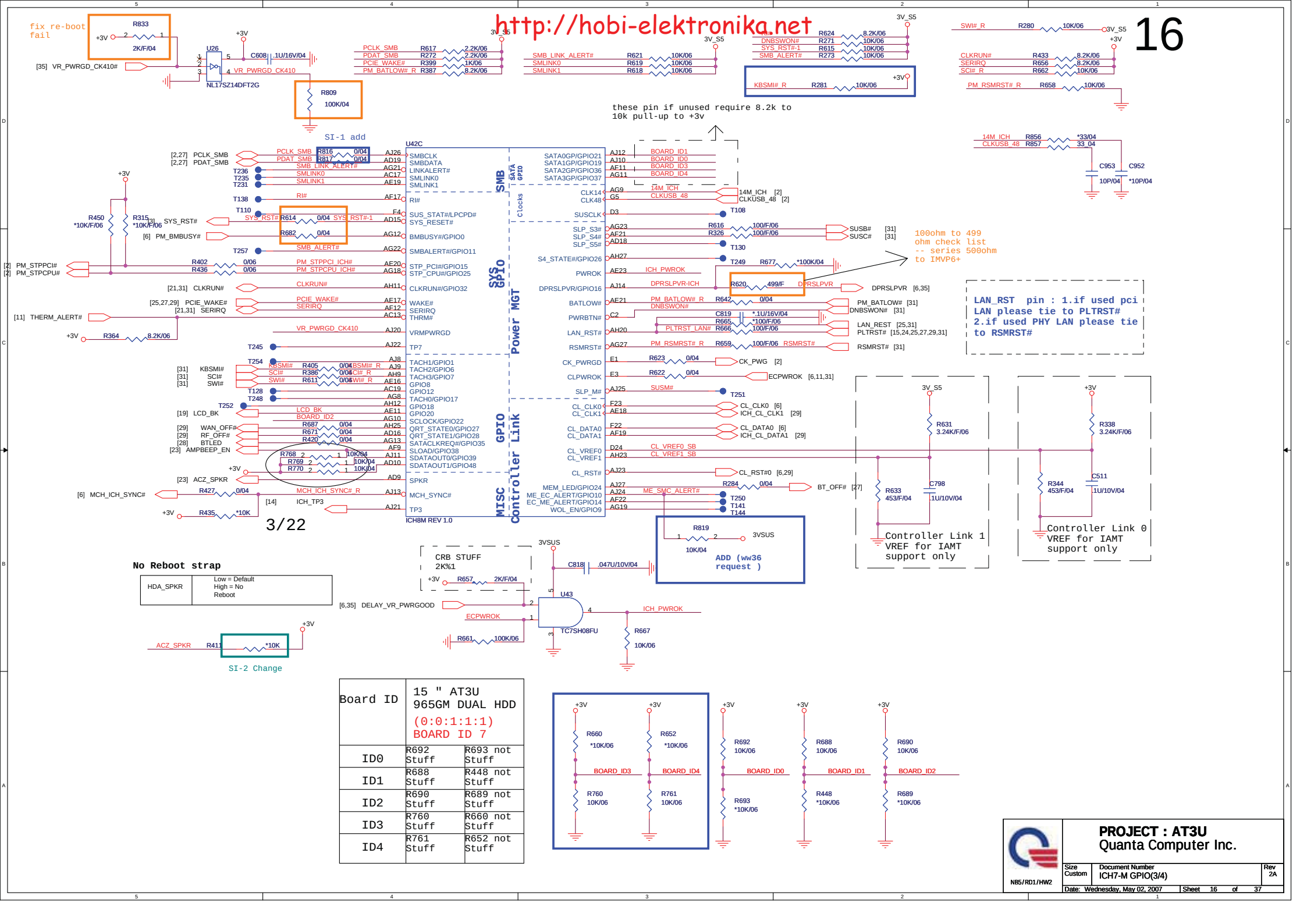
add terminator resistor

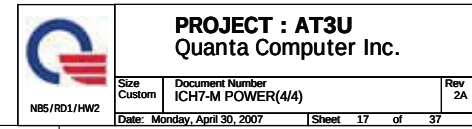




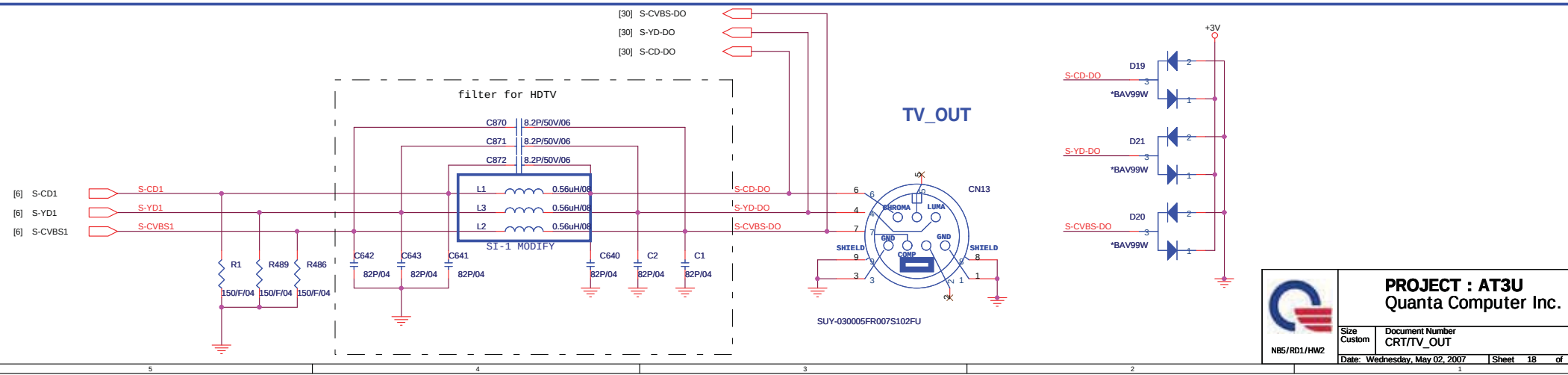
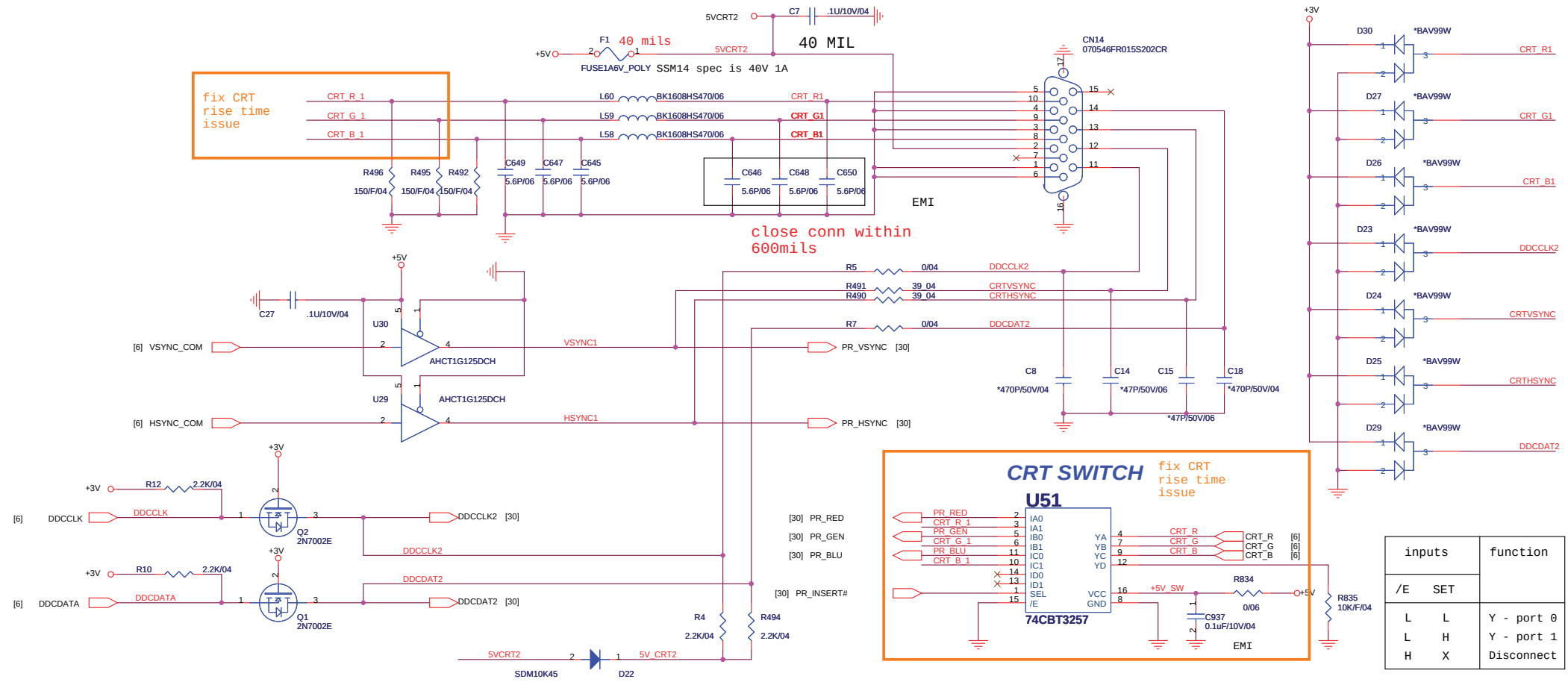


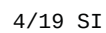
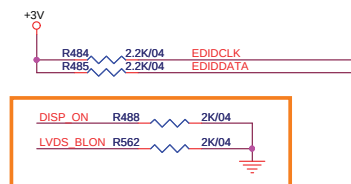
Size Custom	Document Number ICH7-M M PCI E(2/4)	Rev 2A
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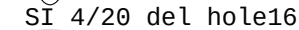
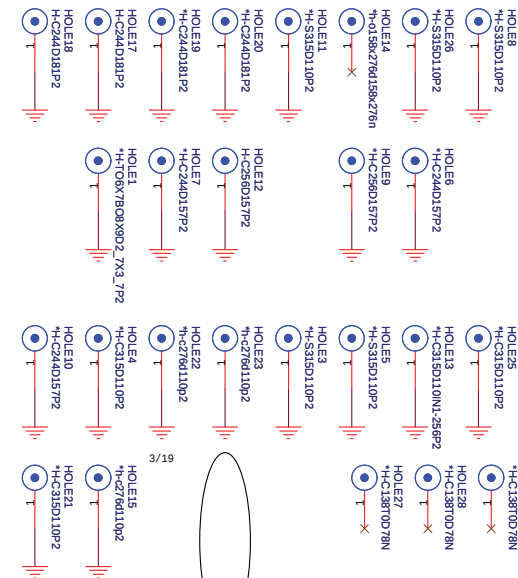




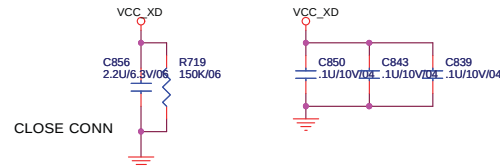
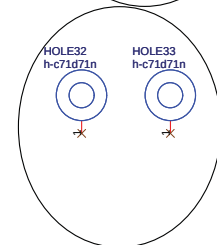
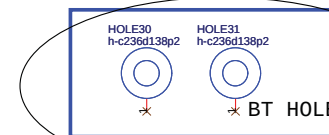
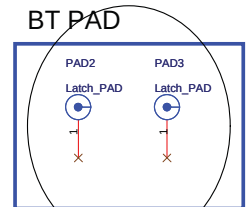
fix CRT
rise time
issue

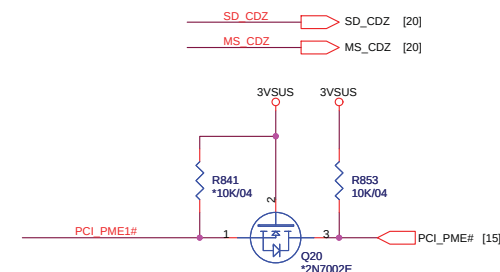
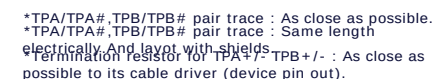
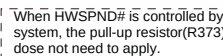






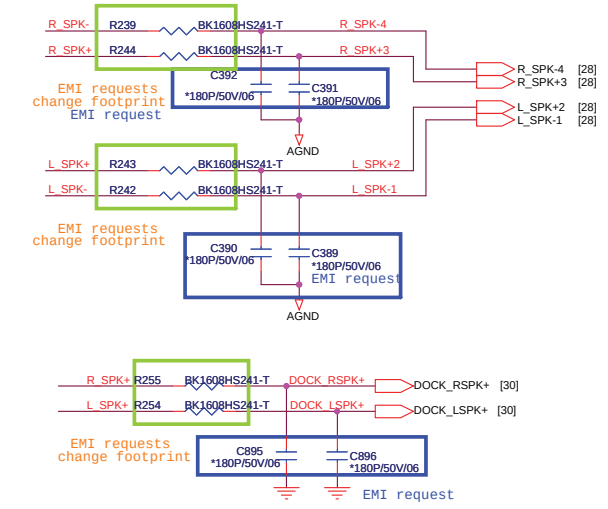
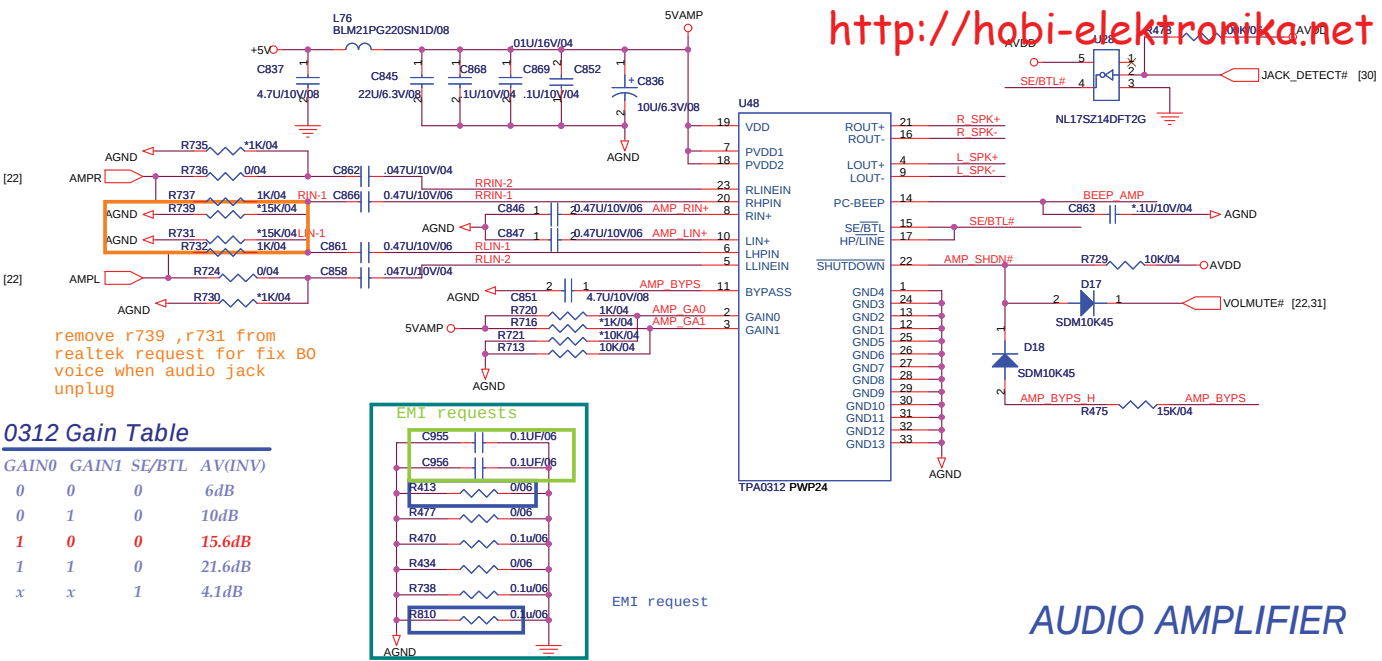
SI 4/30 del PAD1,9,10,13,16



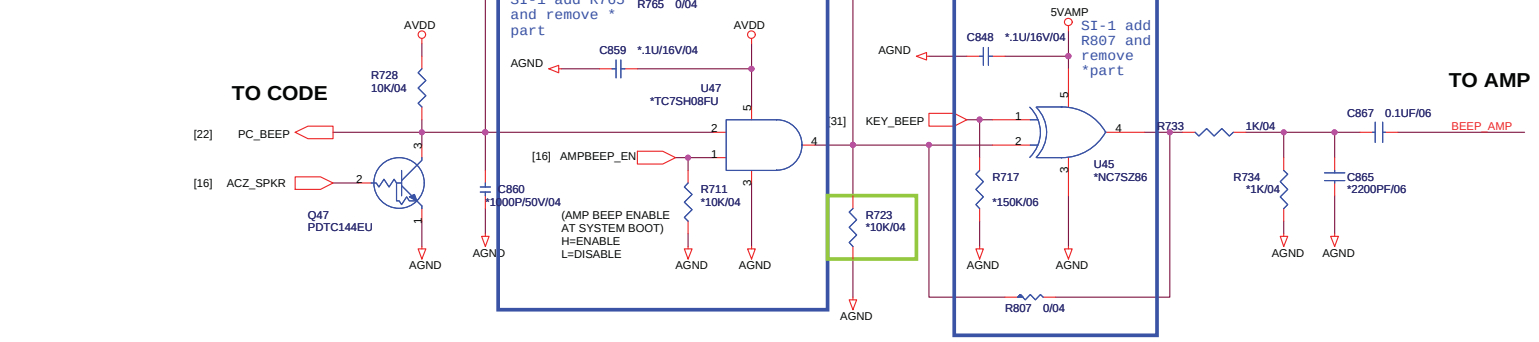


Size Custom	Document Number RICOH832 Controller	Rev 2A
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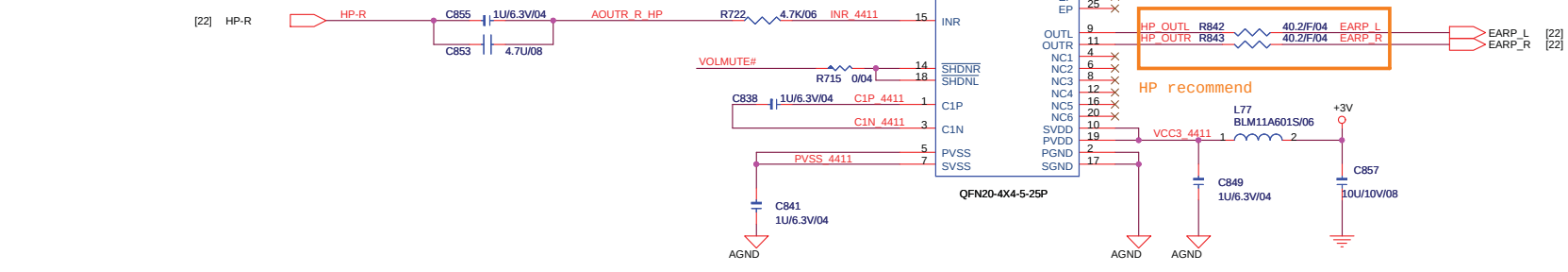


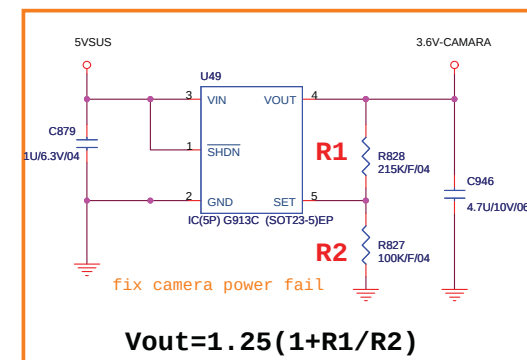


PCSPK BEEP

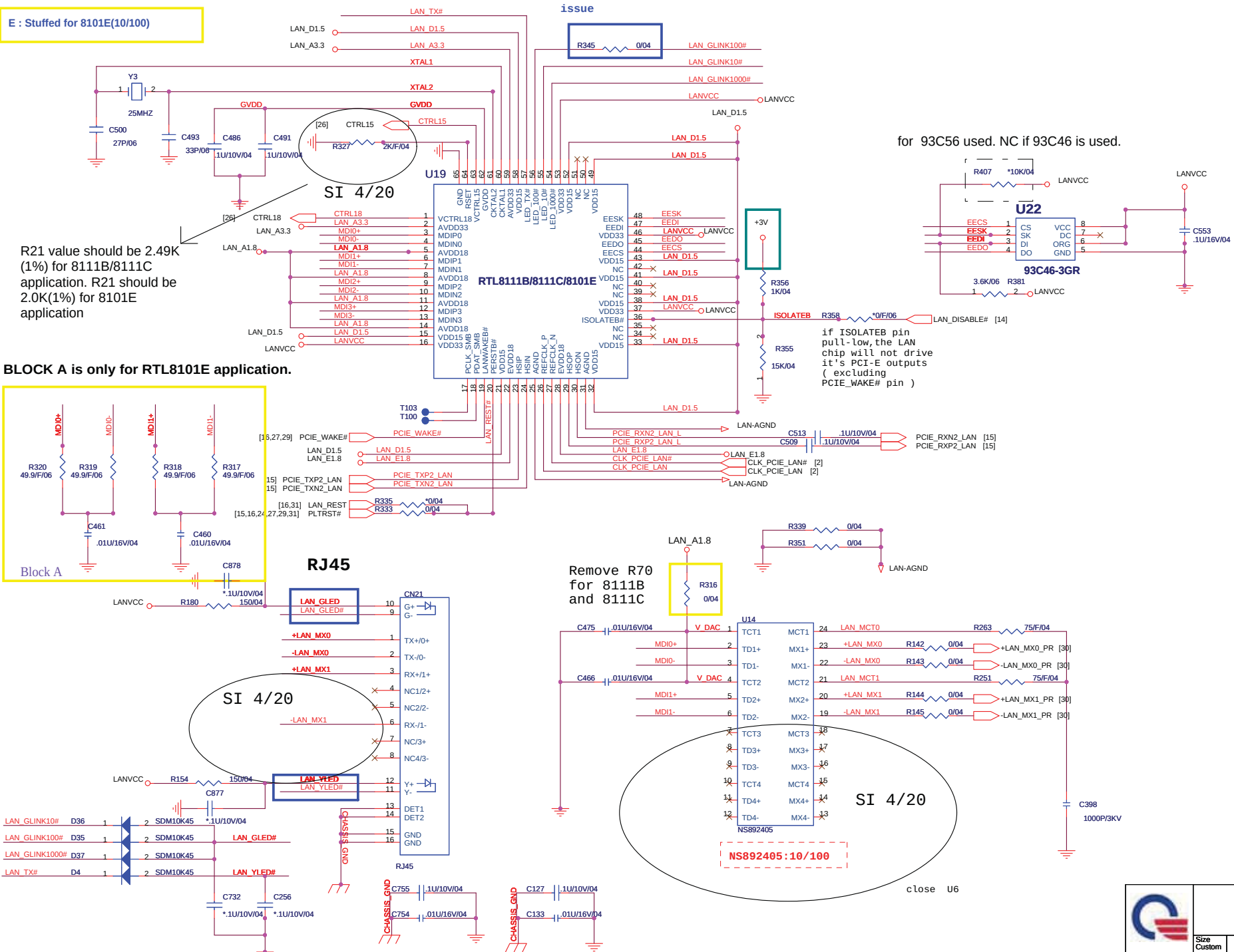


LINE OUT Amplifier

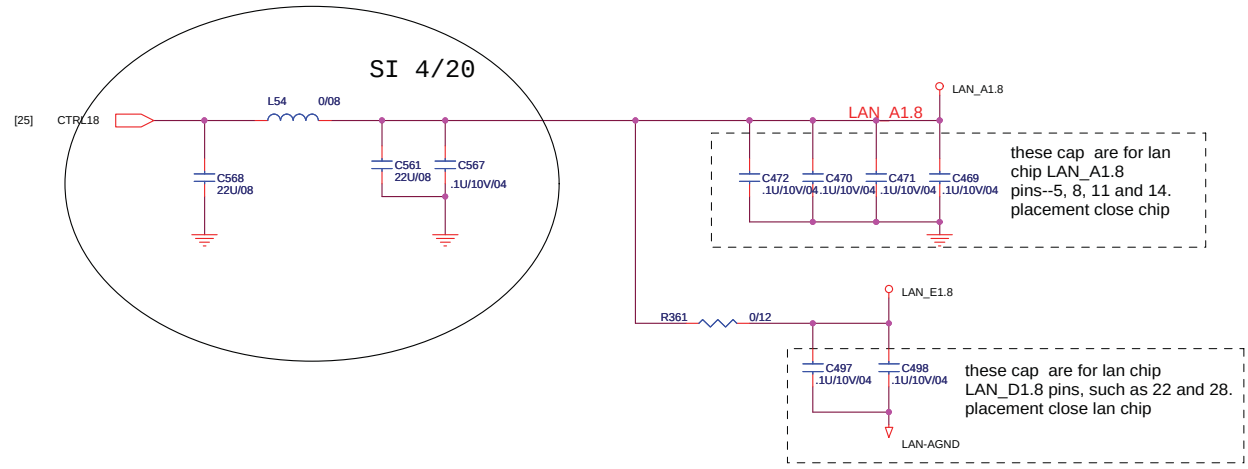
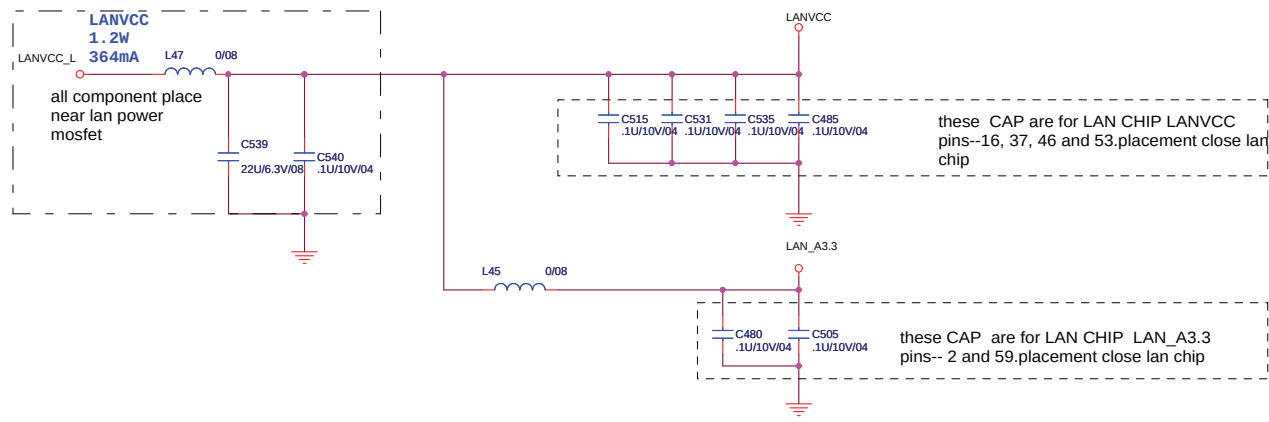




E : Stuffed for 8101E(10/100)



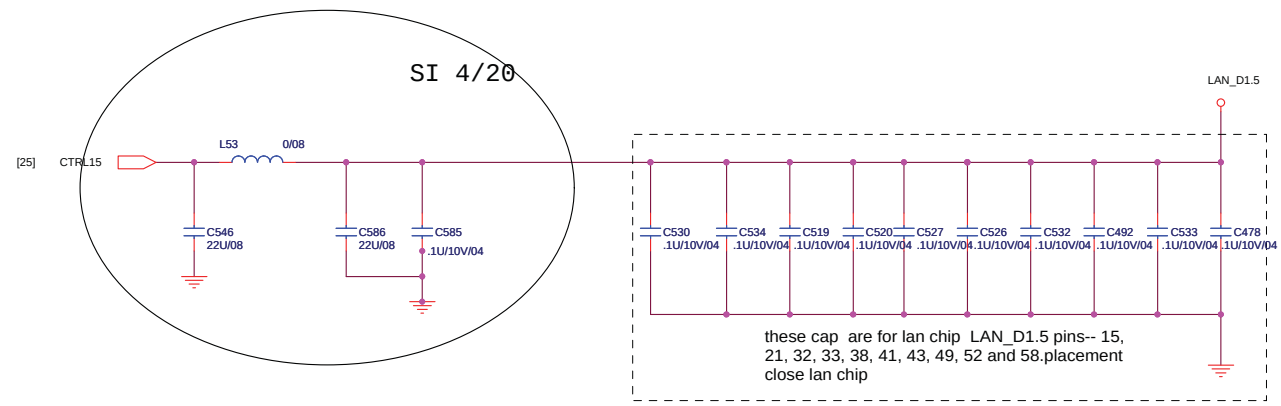
E : Stuffed for 8101E(10/100)



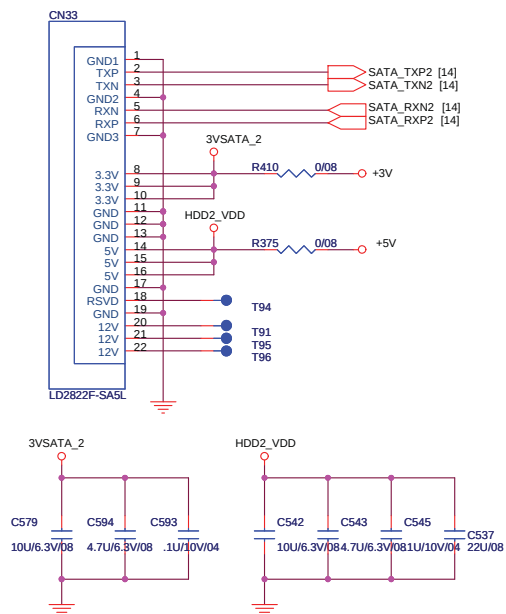
Power domain chart

	RTL8111B / RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

	Q19	Q21
RTL8111B	Need	Need
RTL8101E	N/A	N/A



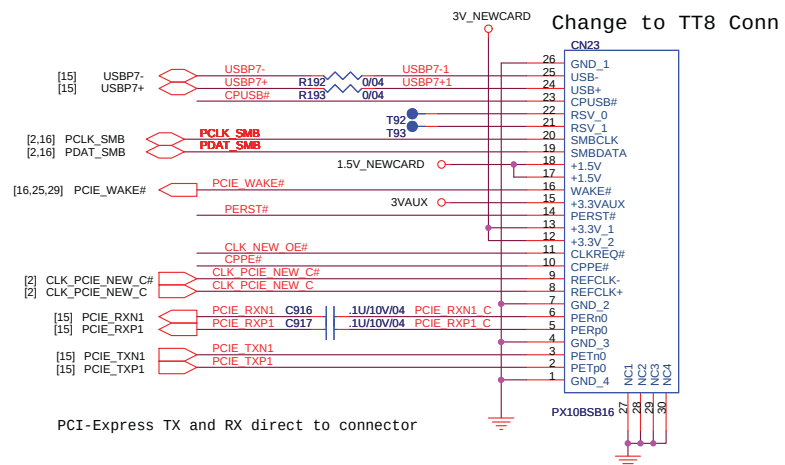
SATA_1 CONNECTOR



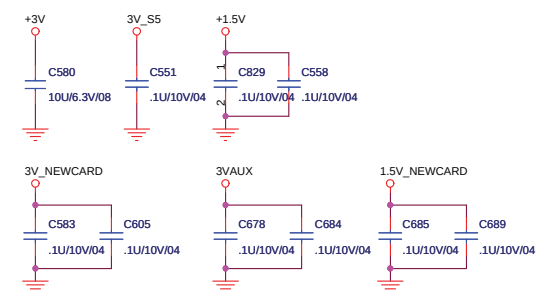
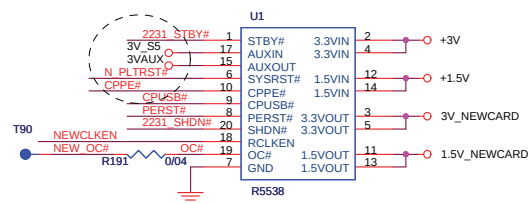
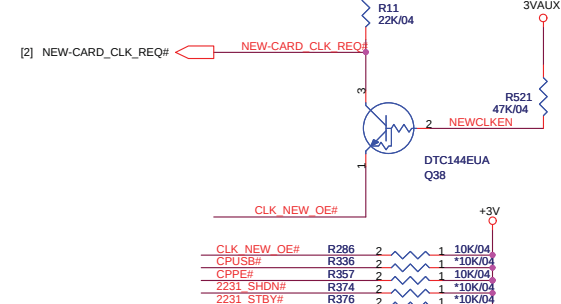
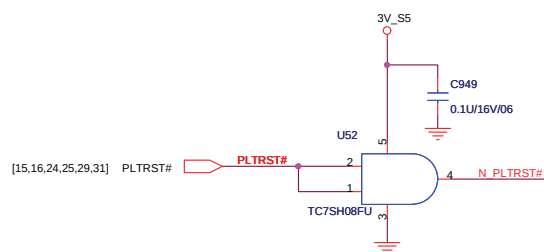
<http://hobi-elektronika.net>

NEWCARD

27



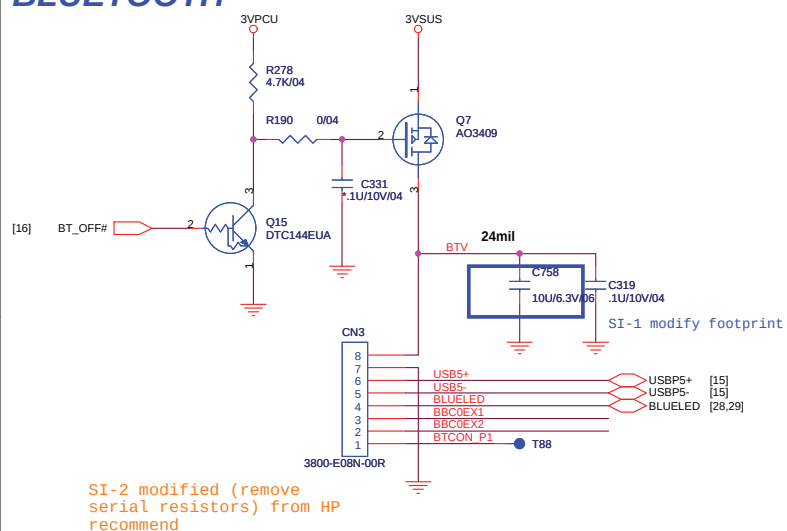
PCI-Express TX and RX direct to connector



PROJECT : AT3U
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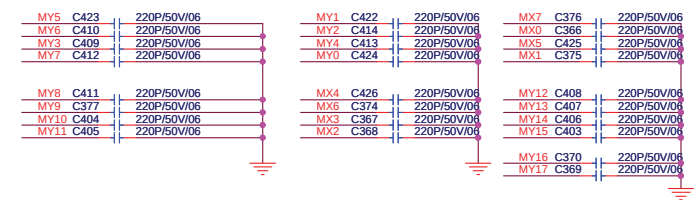
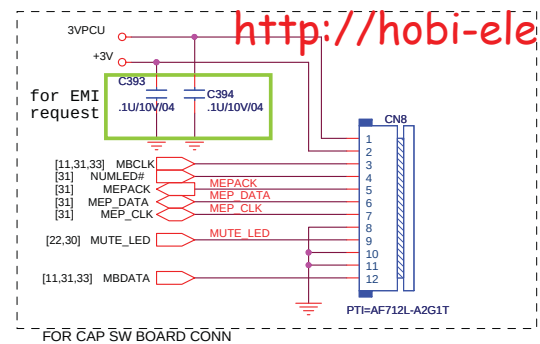
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BLUETOOTH

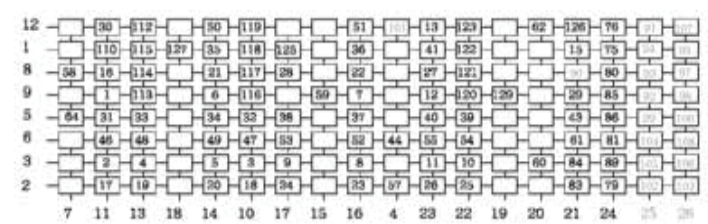
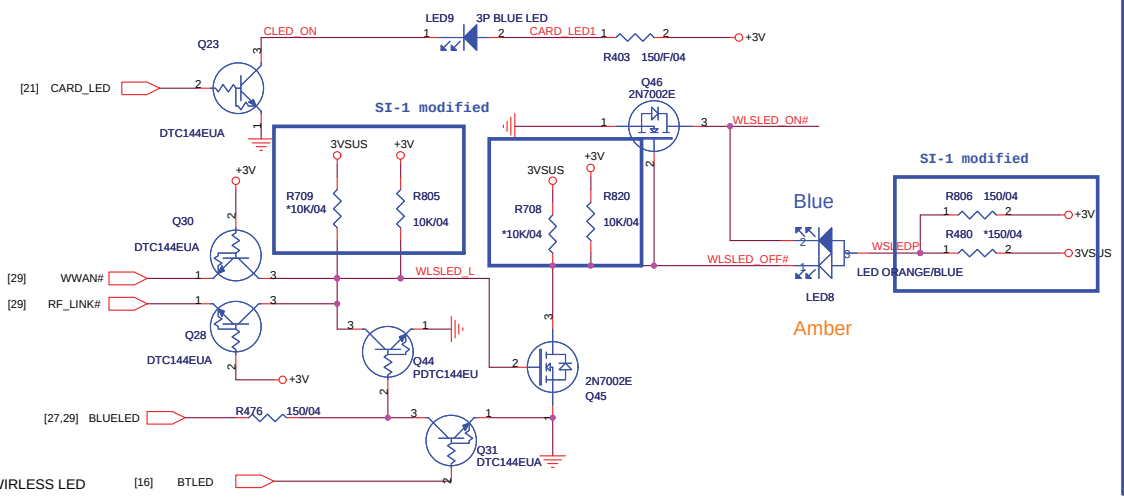
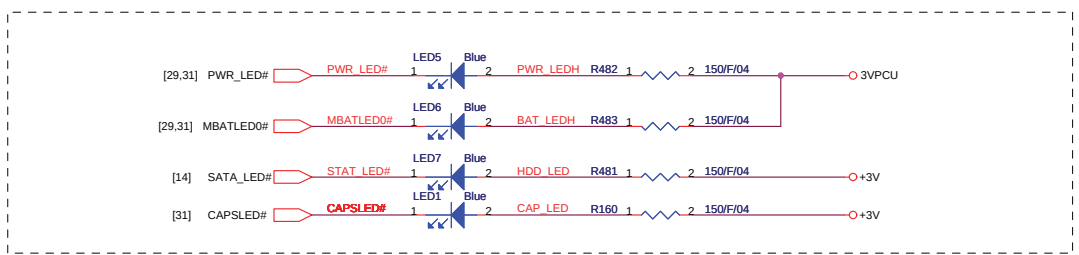
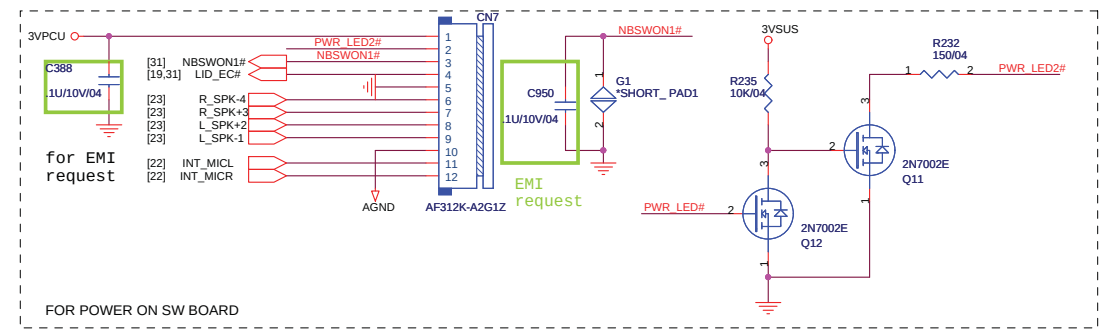
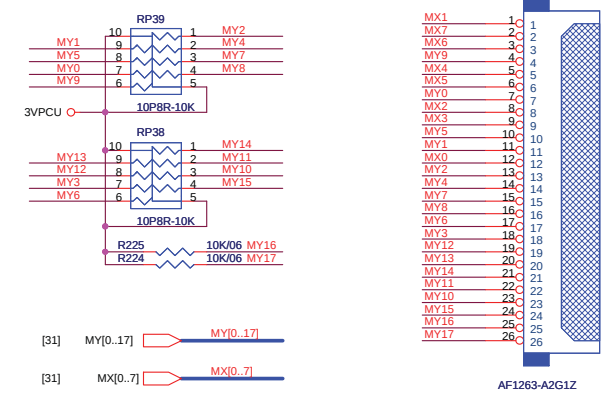


SI-2 modified (remove serial resistors) from HP recommend

BBC0EX1 [29]
BBC0EX2 [29]



KEYBOARD PULL-UP



INTEL WLAN
CARD PIN 20
W_DISABLE#
have
internal
pull-up 110k
ohm

[16,25,27] PCIE_WAKE#

MINICAR PME#

Q43 *PDTC144EU

 NBS/RD1/HW2	PROJECT : AT3U Quanta Computer Inc.		
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support docking
SPIDF

1.5V

R522 33_04

C883 .1u/10V/04

SPDIF V

Q37 MMBT3904

SPDIF

R531 510/F/04

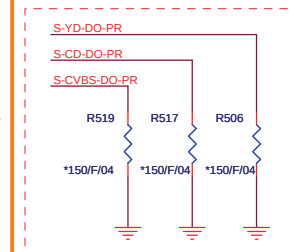
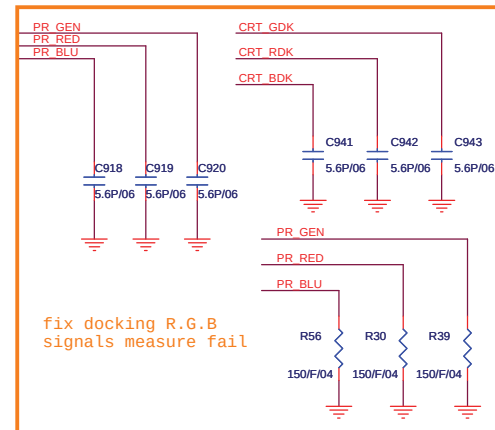
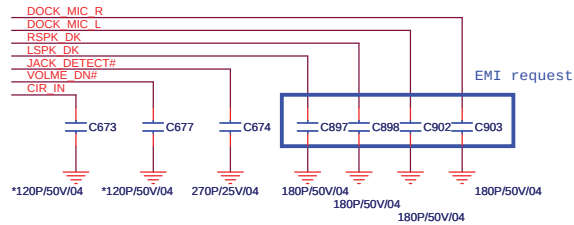
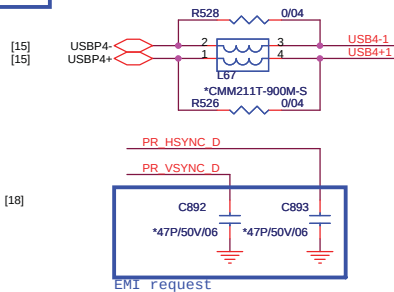
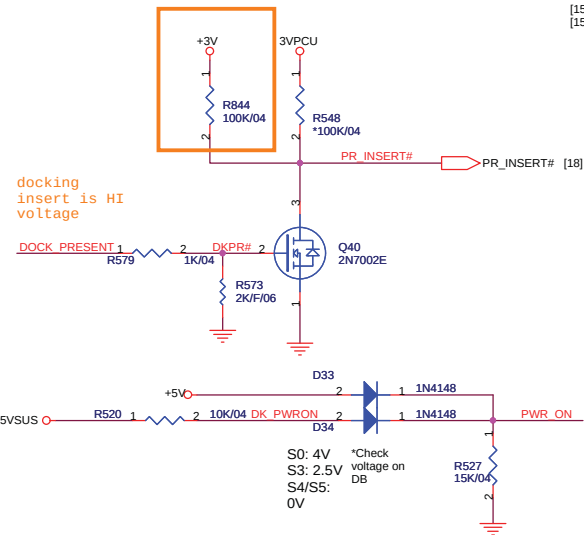
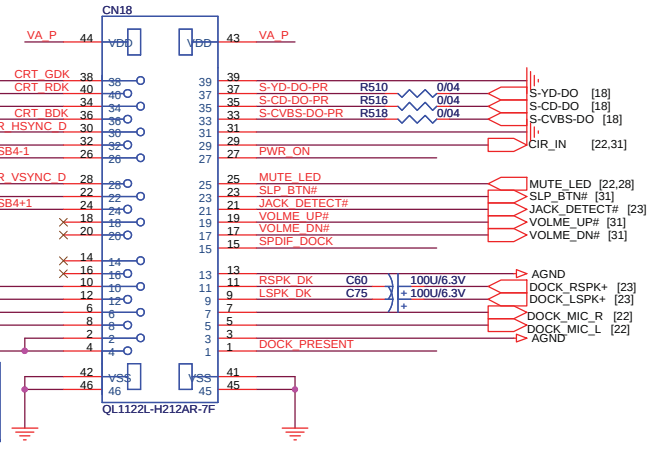
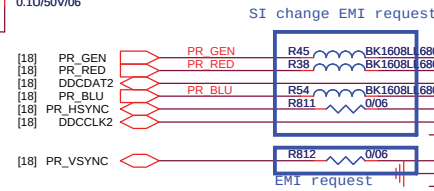
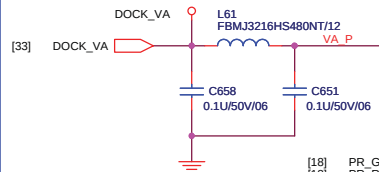
SPIDF_DK 2

R525 510/F/04

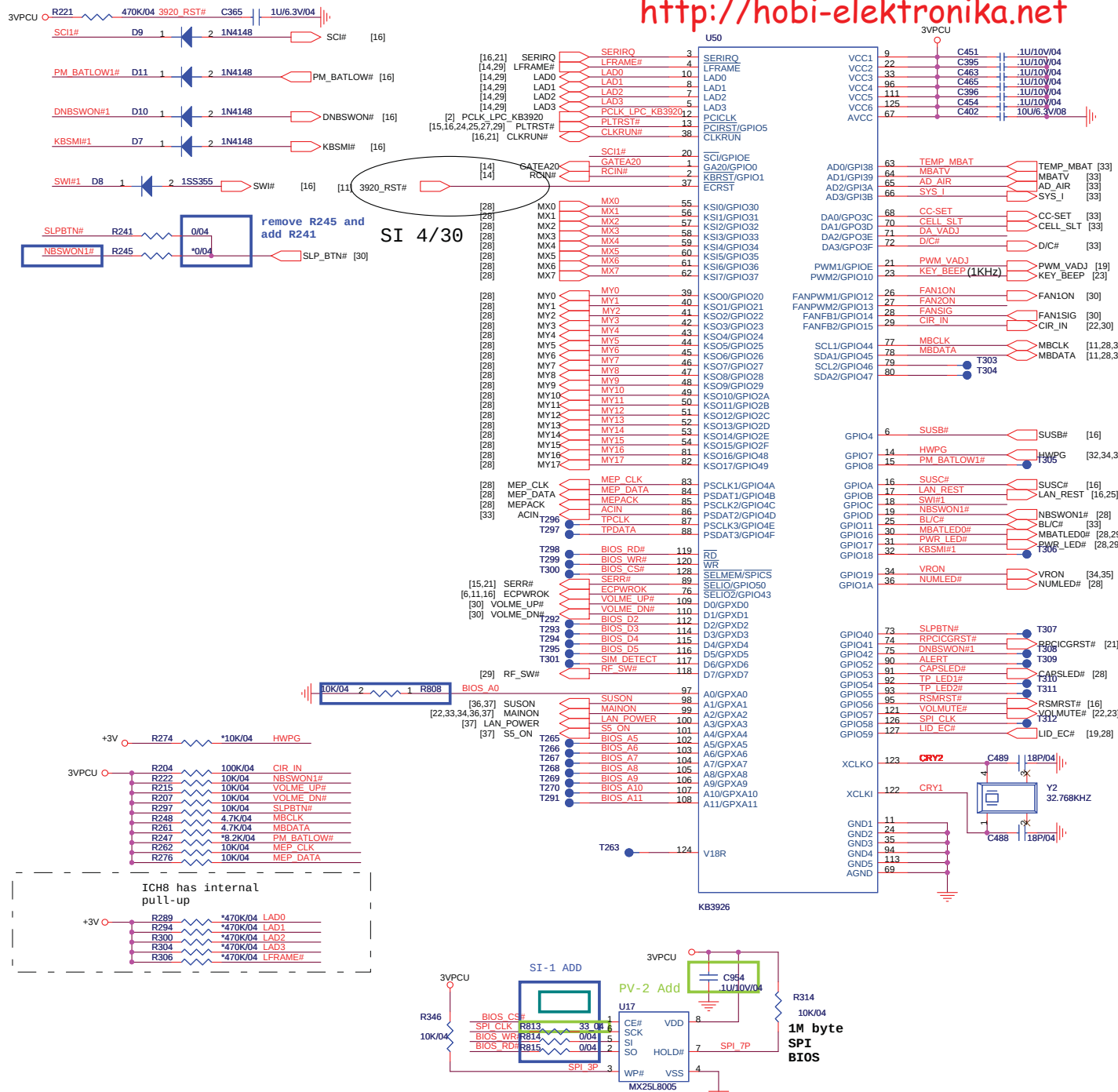
C681 68P/50V/04

L68 0/06

SPD_DK SPDIF_DOCK

[illegible]

 NBS / RD1 / HW2	PROJECT : AT3U Quanta Computer Inc.		
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STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

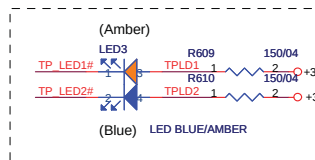
DEL R209, R210, R218, R219, R220



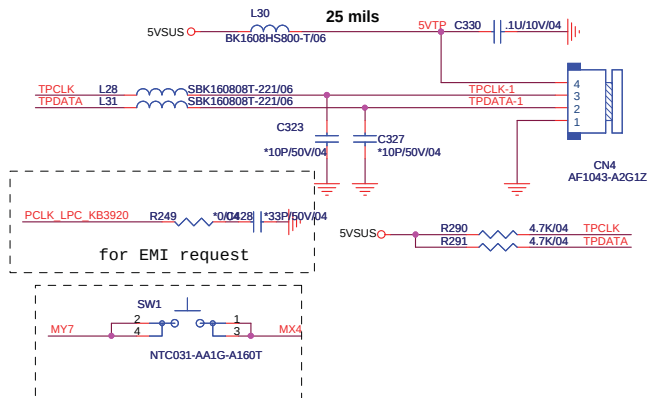
All hardware straps default internal pull-up, so don't need pull-up outside. A TEST need try --andrew ????

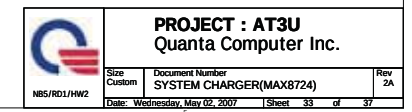
SELECT KBC TPYE

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808



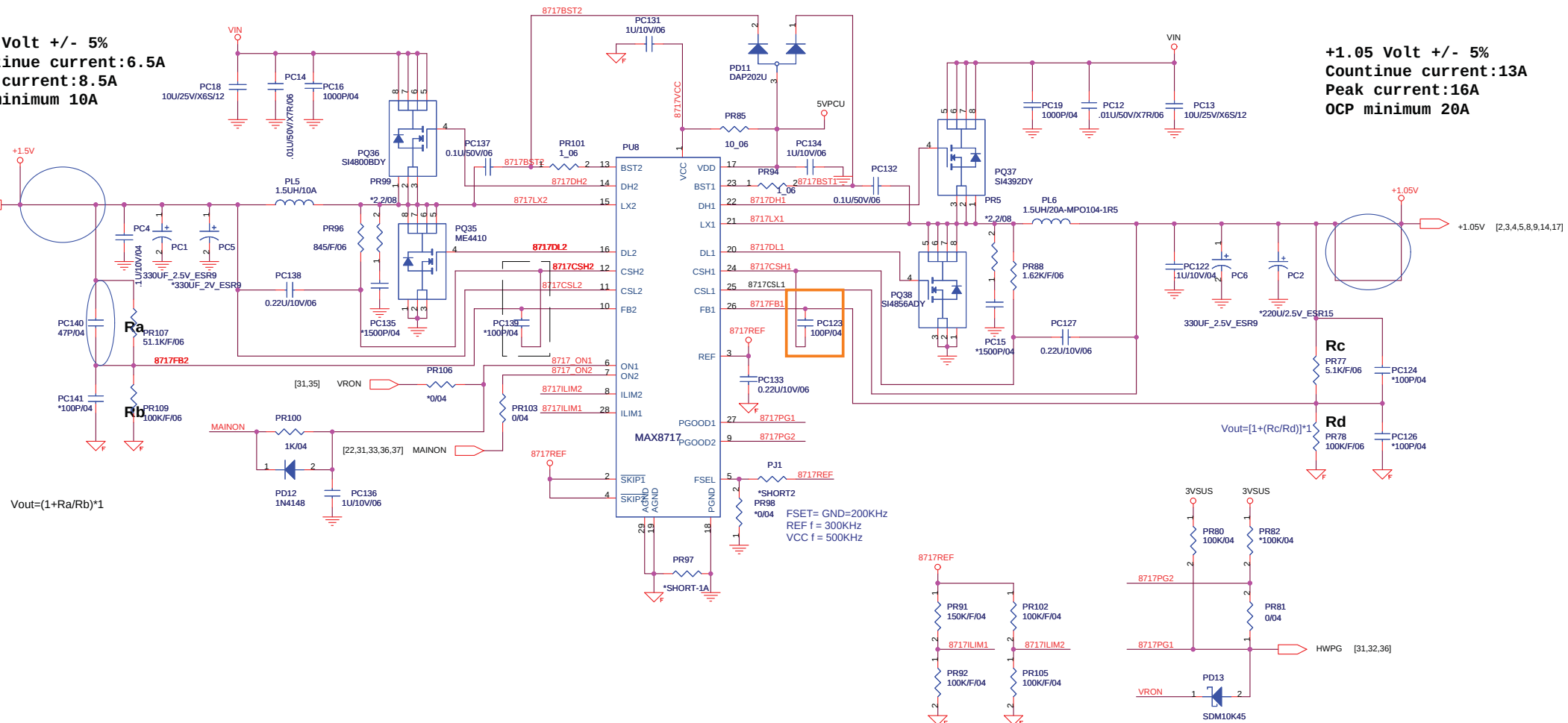
TOUCH PAD CONNECTOR

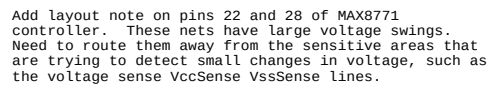


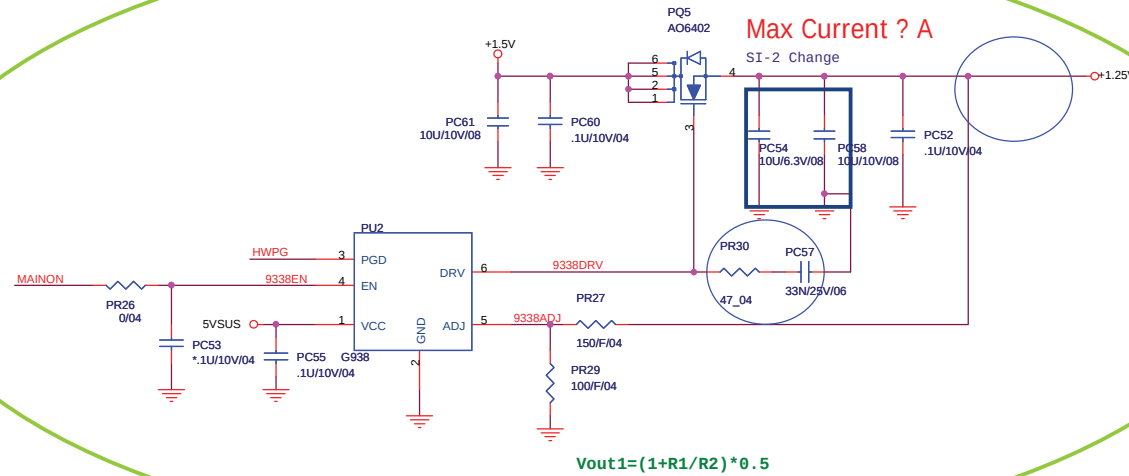
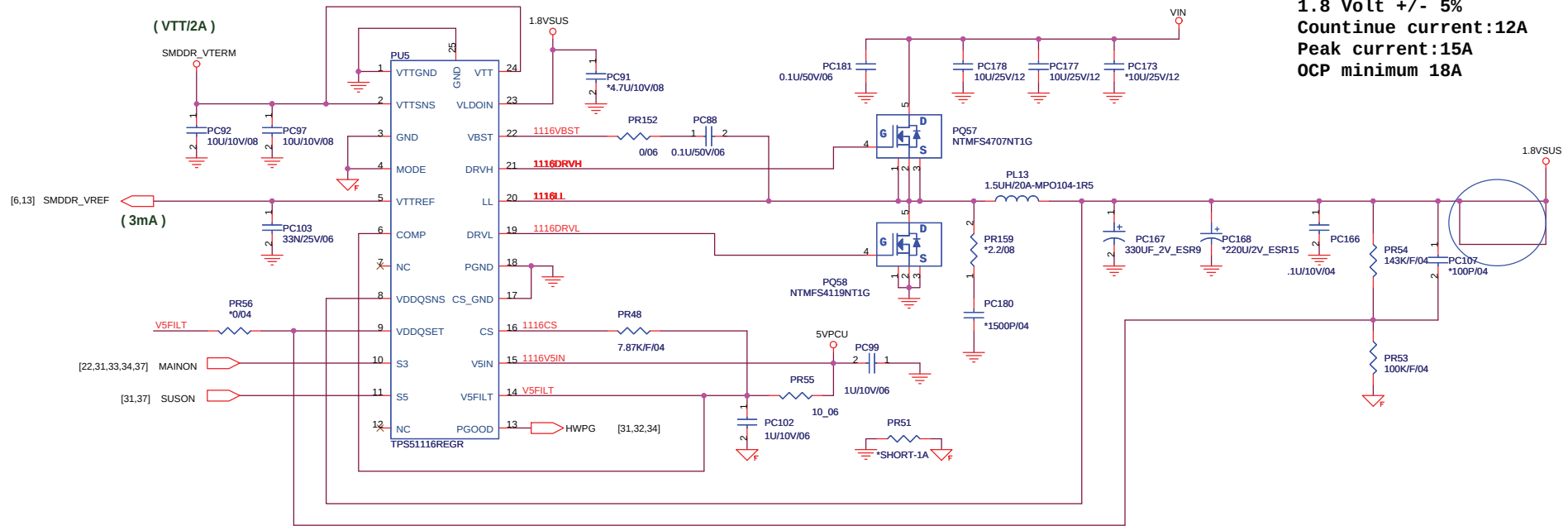


+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A

+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A







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