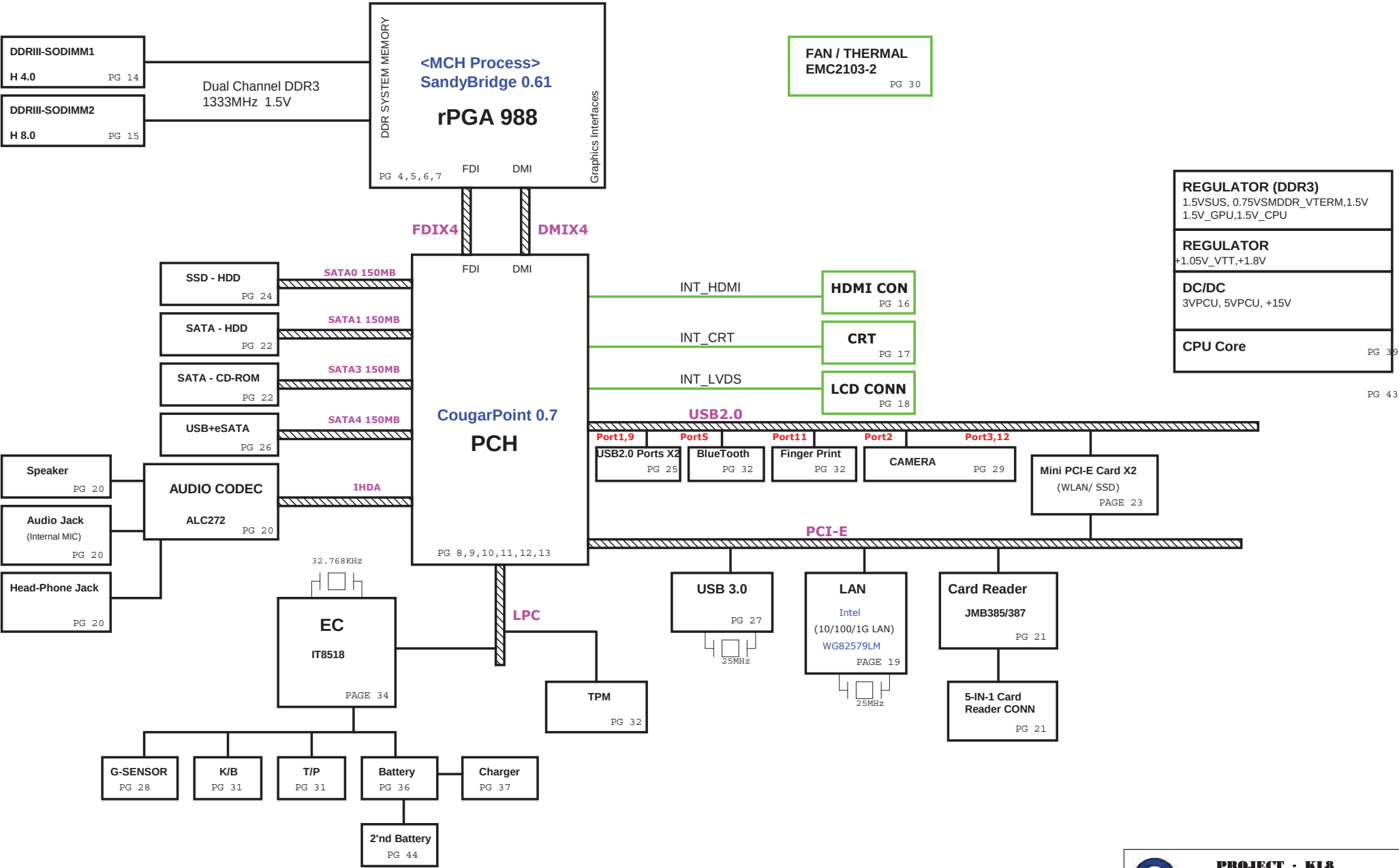
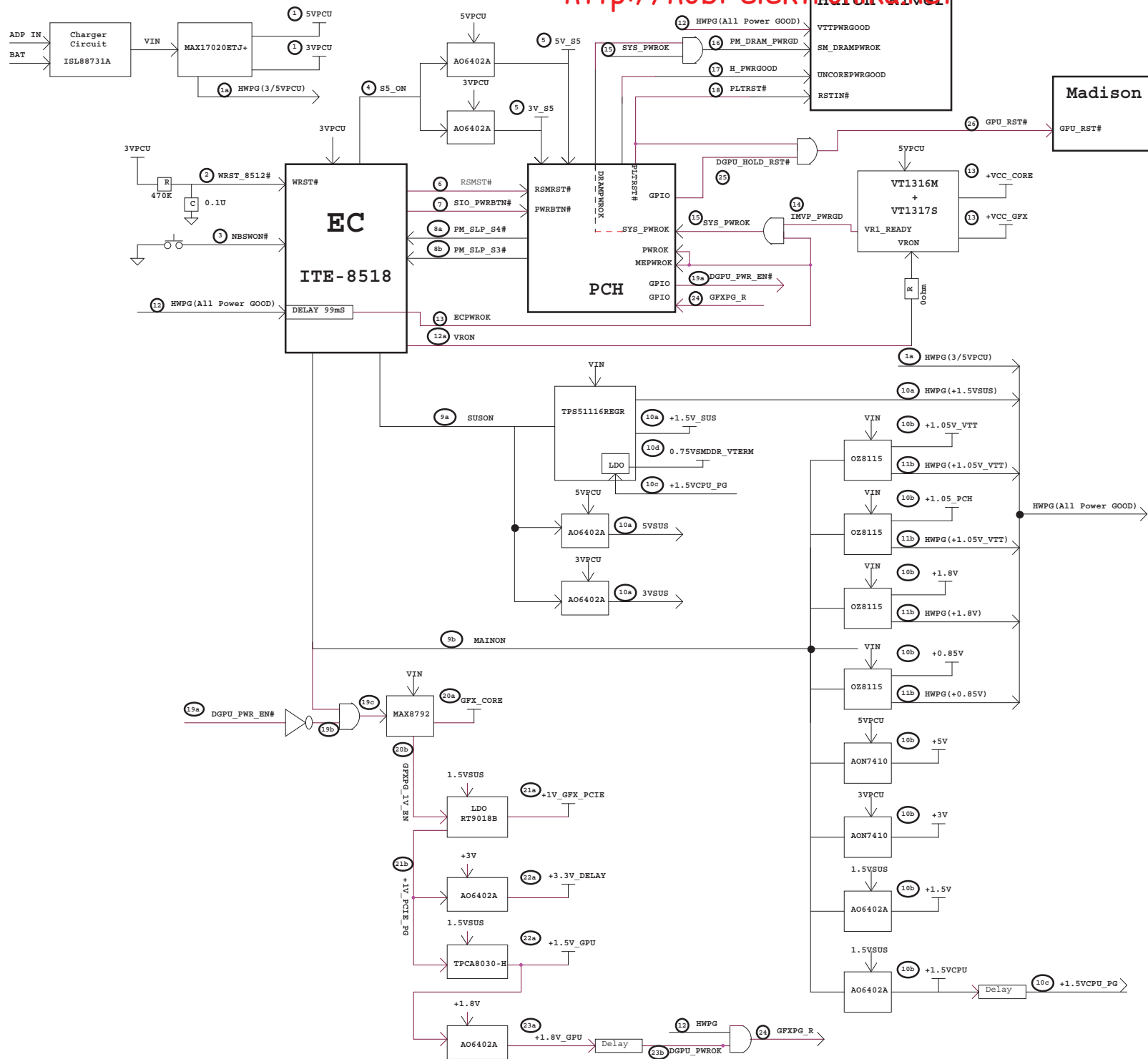






02/20 DEL for Pre-ES1

CPU_CLK select(CLK)

02/20 DEL for Pre-ES1

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

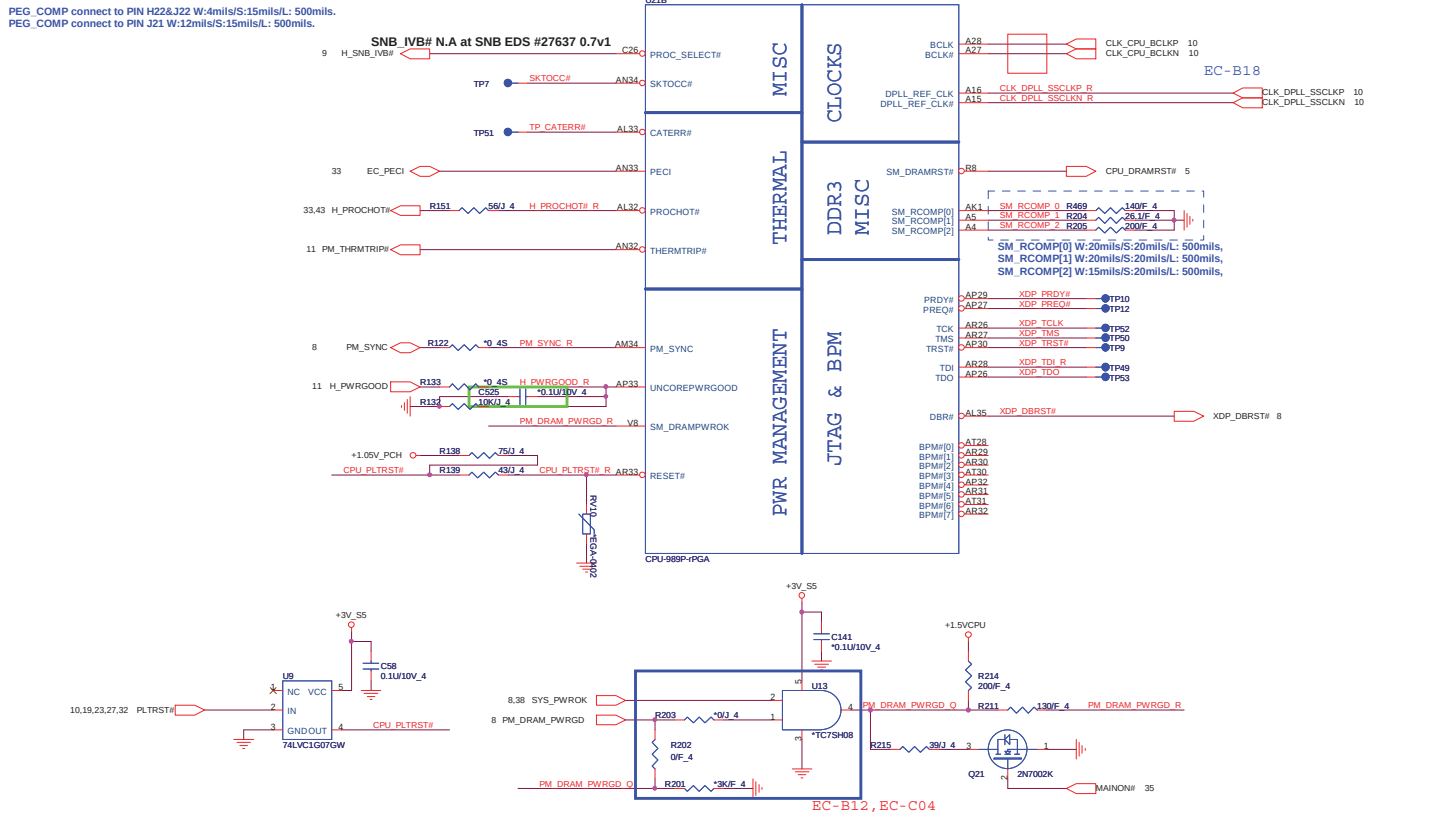
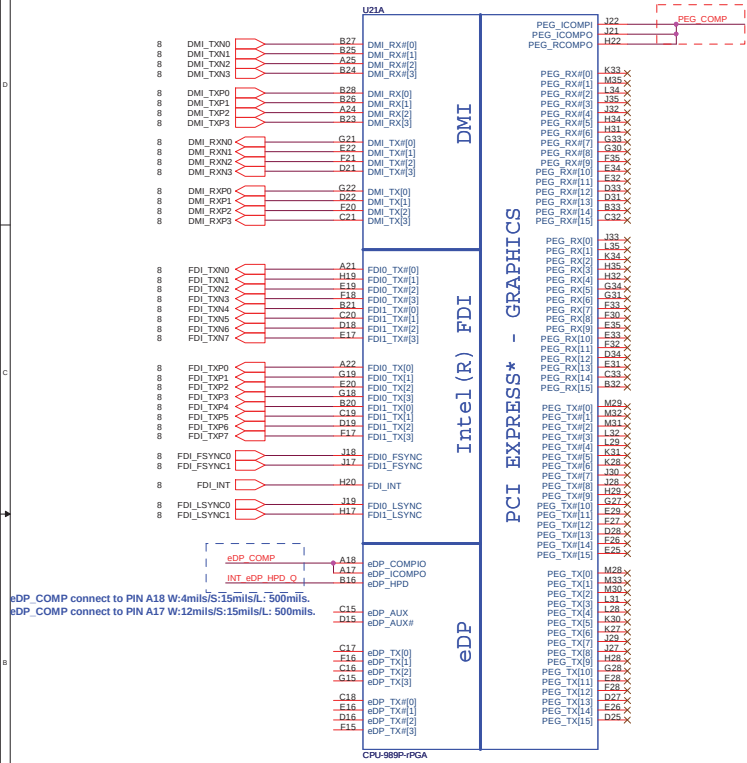


PROJECT : K13
Quanta Computer Inc.

Size	Document Number	Clock Generator	RevA
Date: Tuesday, January 04, 2011		Sheet 3	of 44

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)



FDI Disable

PEG x16 (UMA Non-stuff)

08/11 Del PEG trace

DP & PEG Compensation

PEG_ICOMPI and RCOMP signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 4.5 mohms

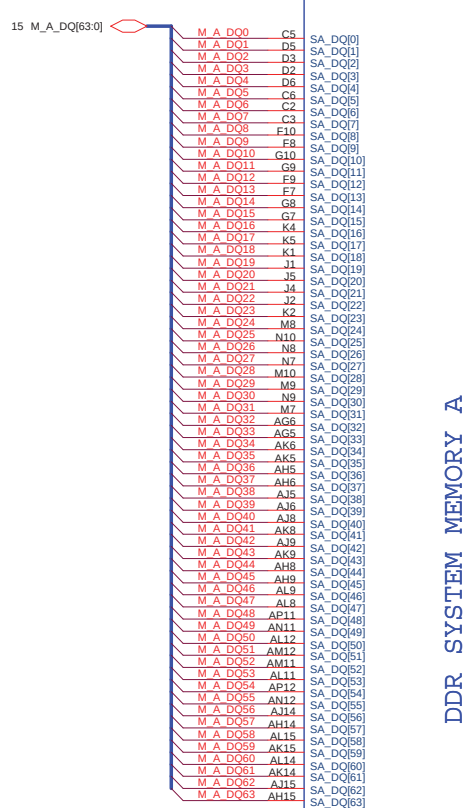
eDP_COMPO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)

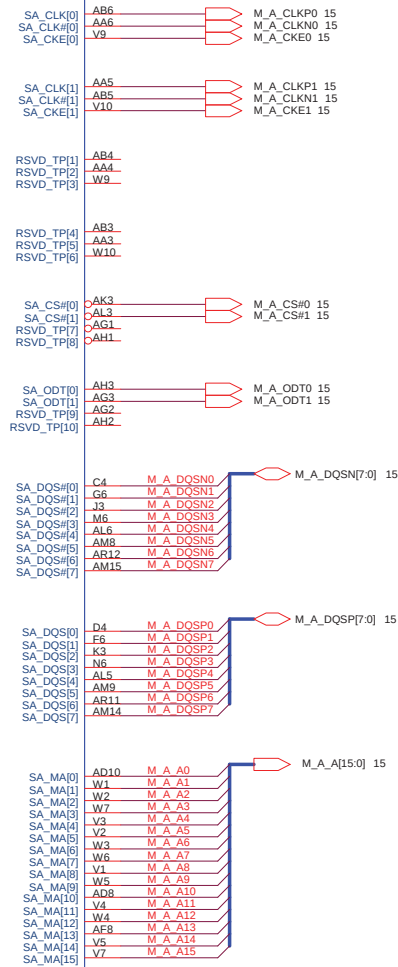
PROJECT : KLB
Quanta Computer Inc.

Size Document Number
Tuesday, January 04, 2011
Sandy Bridge 1/4
Date: Sheet 4 of 44

U21C

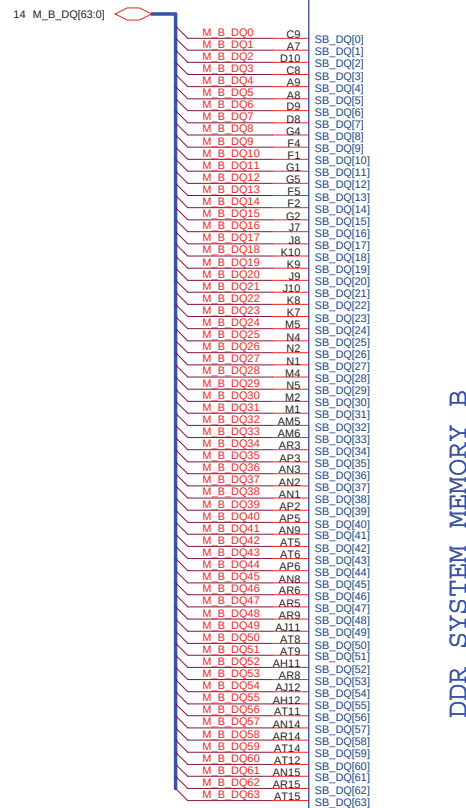


DDR SYSTEM MEMORY A

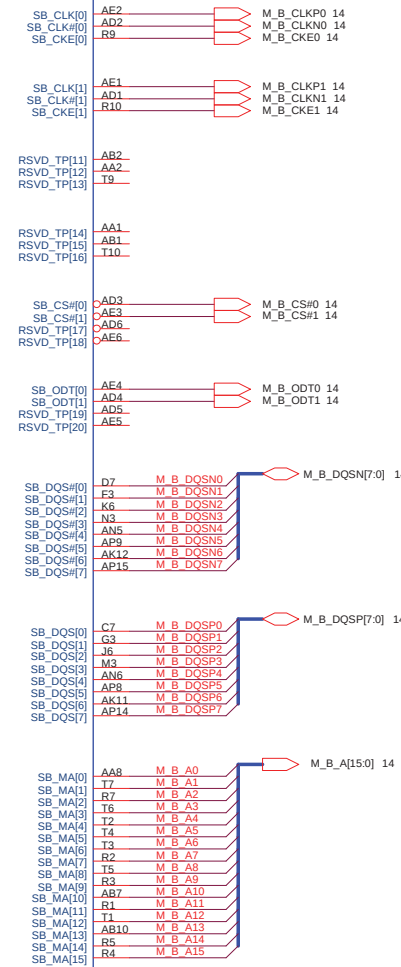


CPU-989P-rPGA

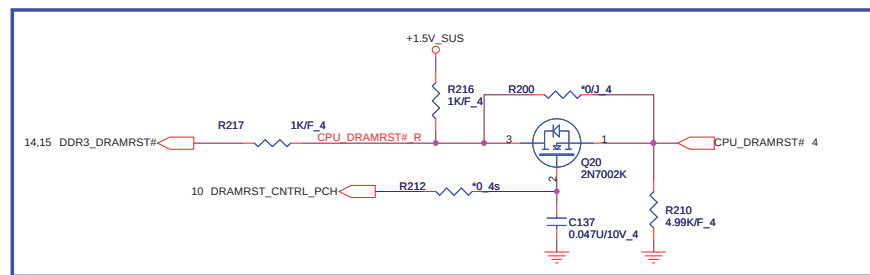
U21D



DDR SYSTEM MEMORY B

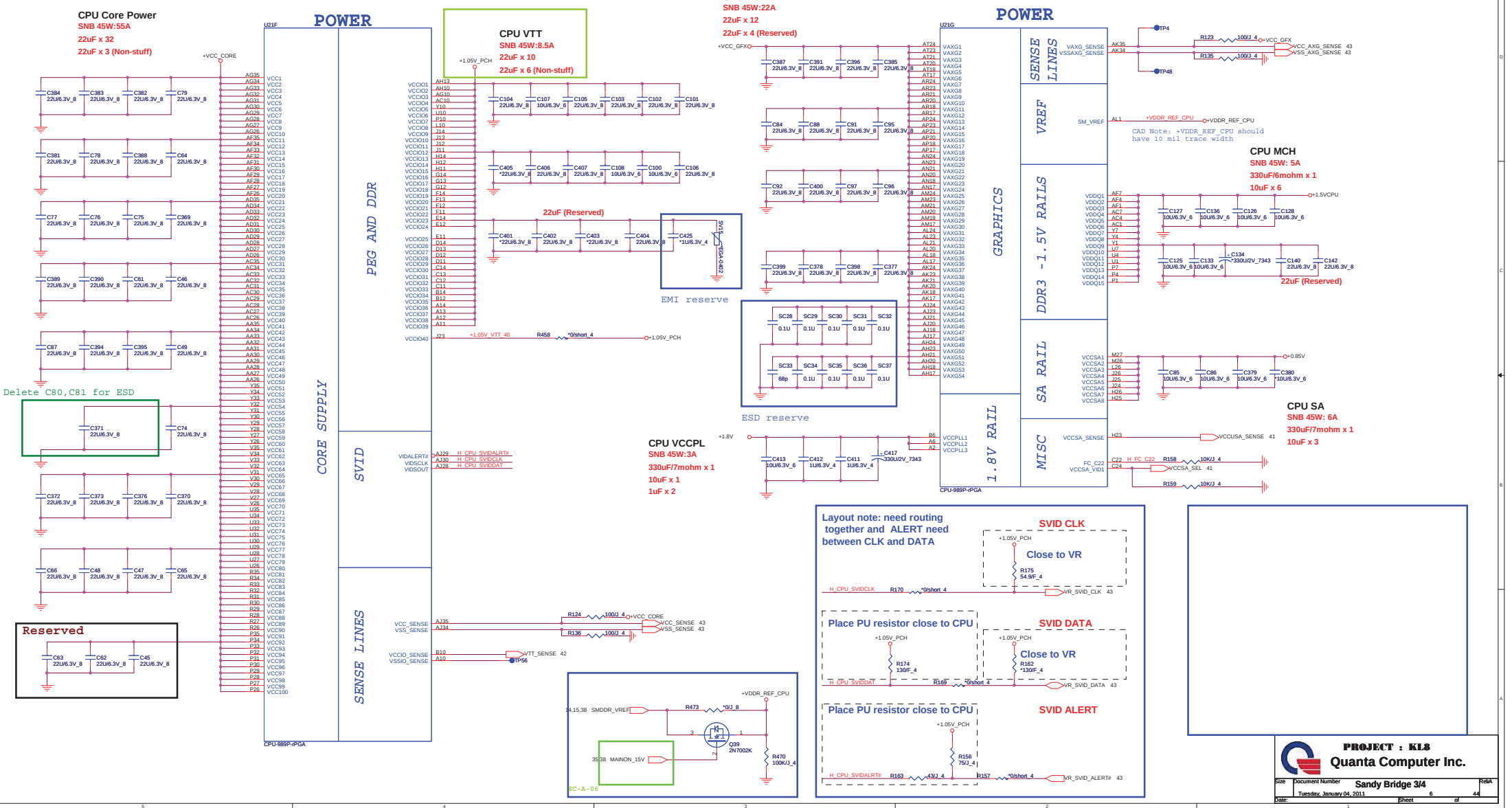


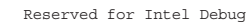
CPU-989P-rPGA



Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)





For rPGA socket, RSVD59 pin should be left NC

The CFG signals have a default value of '1' if not terminated on the board.

CFG2 R167 1K/F 4

CFG4 R173 *1K/F 4

CFG7 R146 *1K/F 4



```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```



Size	Document Number	Sandy Bridge 4/4	RelA
Date:	Tuesday, January 04, 2011	7	44
		Sheet	of

U8C



Follow PDG eDP disable guide

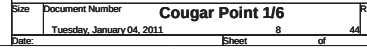
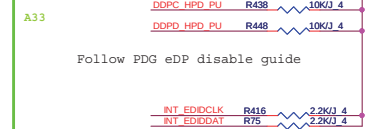
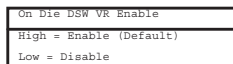


Figure 10 shows the ACZ pin connections. The left diagram is a pinout table for the ACZ signals, and the right diagram is a schematic of the ACZ_SYNC_CODEC signal connection.

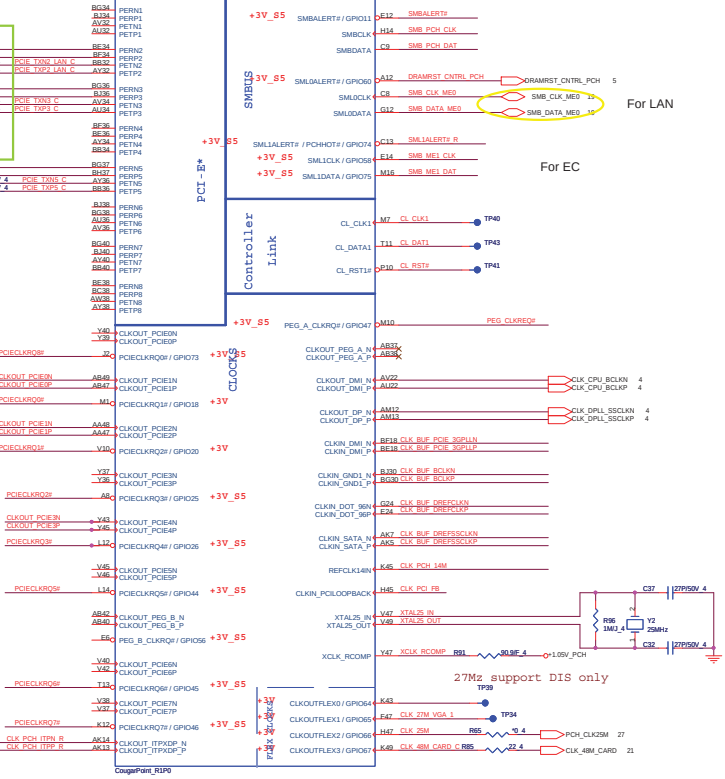
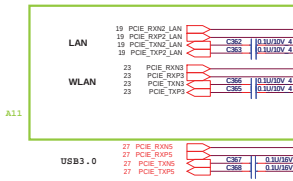
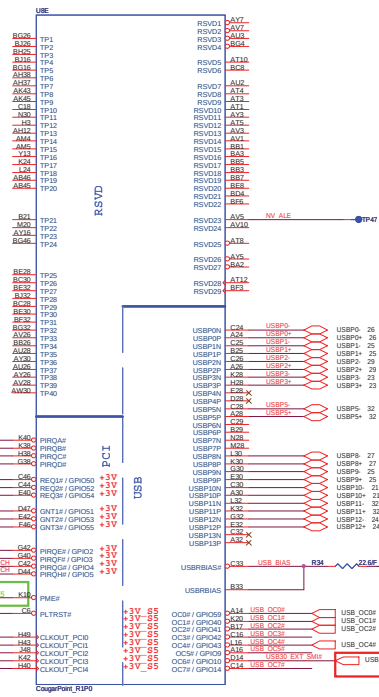
Signal	Pin	Component	Destination
ACZ_BITCLK	R352	33U1	ACZ_BITCLK_R
ACZ_SYNC	R22	33U1	ACZ_SYNC_CODEC
ACZ_RST#	R363	33U1	ACZ_RST#_R
ACZ_SDOUT	R335	33U1	ACZ_SDOUT_R

The right diagram shows the ACZ_SYNC_CODEC signal connected to pin 1 of a 2N7002 MOSFET. The MOSFET is also connected to a 900 Ohm resistor and a 1M Ohm resistor to ground.

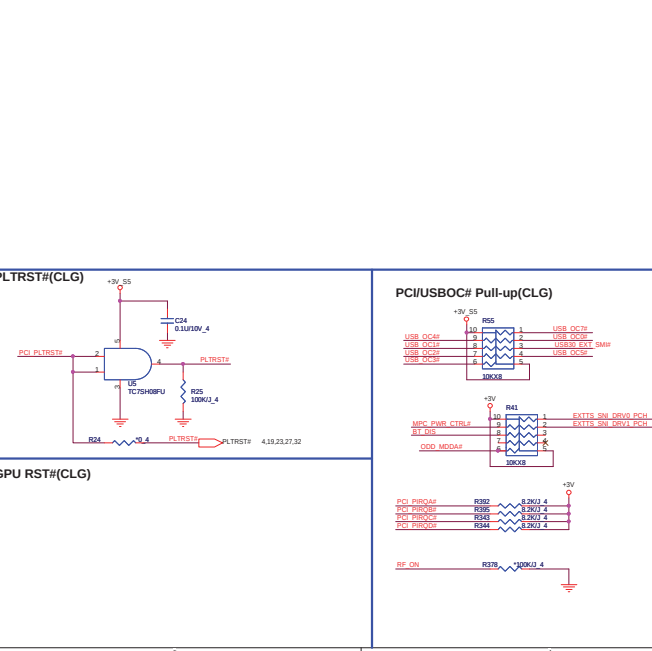
EC-B25

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO5	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI *</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)										
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)										

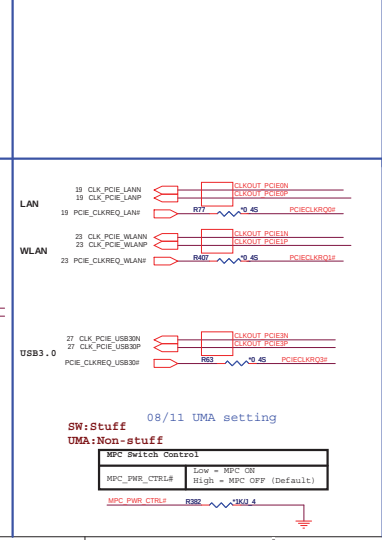
Cougar Point-M (PCI,USB,NVRAM)



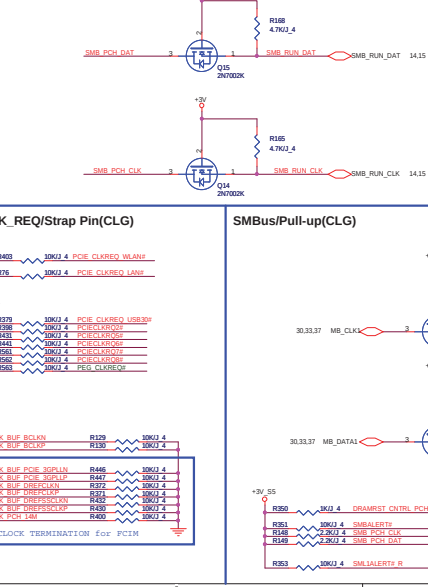
DGPU Power ON



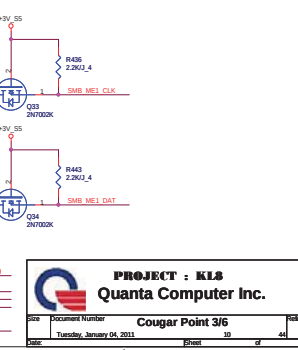
PEG CLK detect



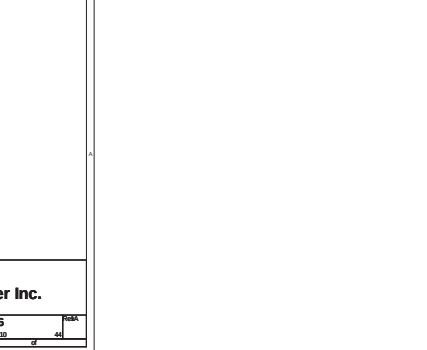
SMBus(CLK)

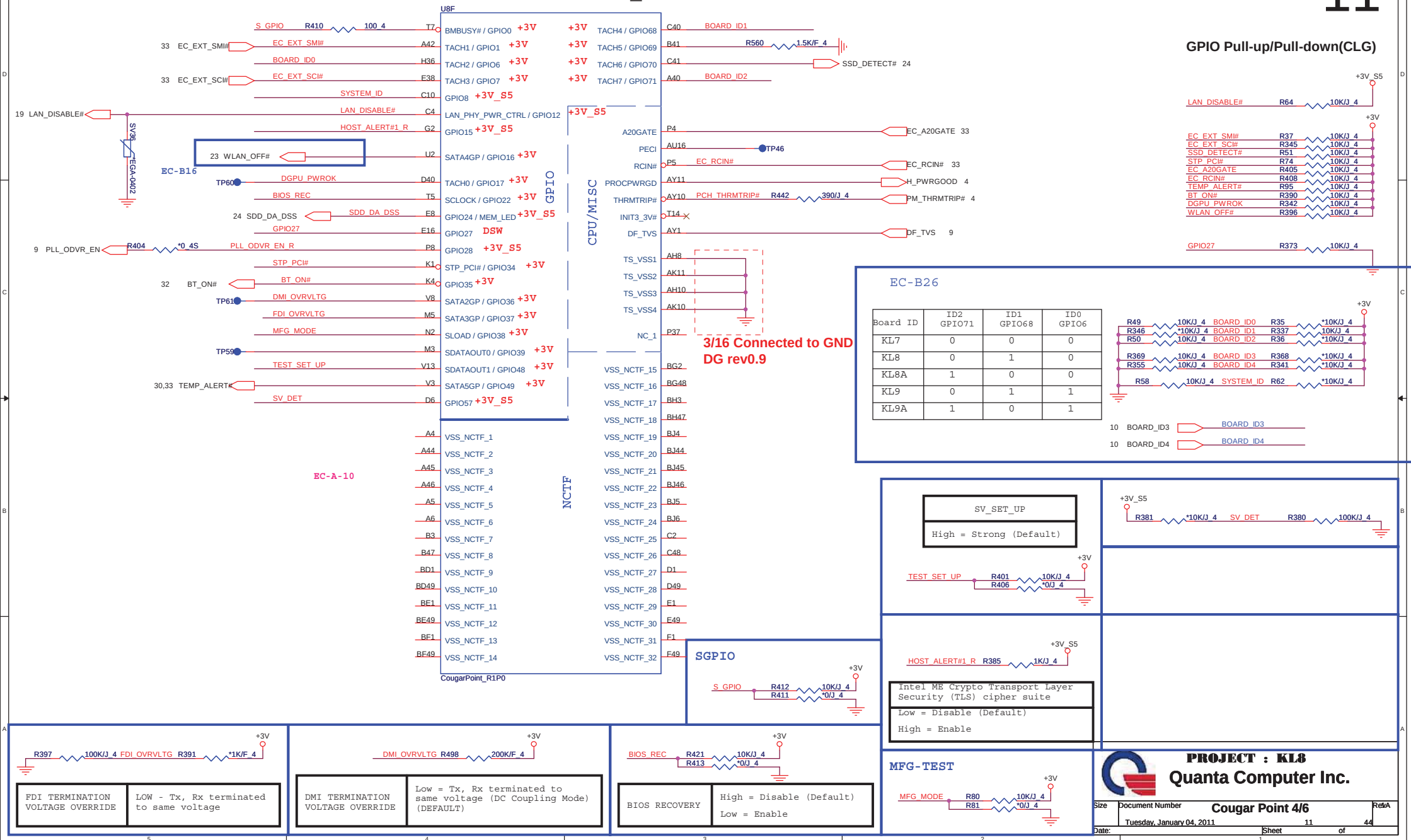


CLK_REQ/Strap Pin(CLG)

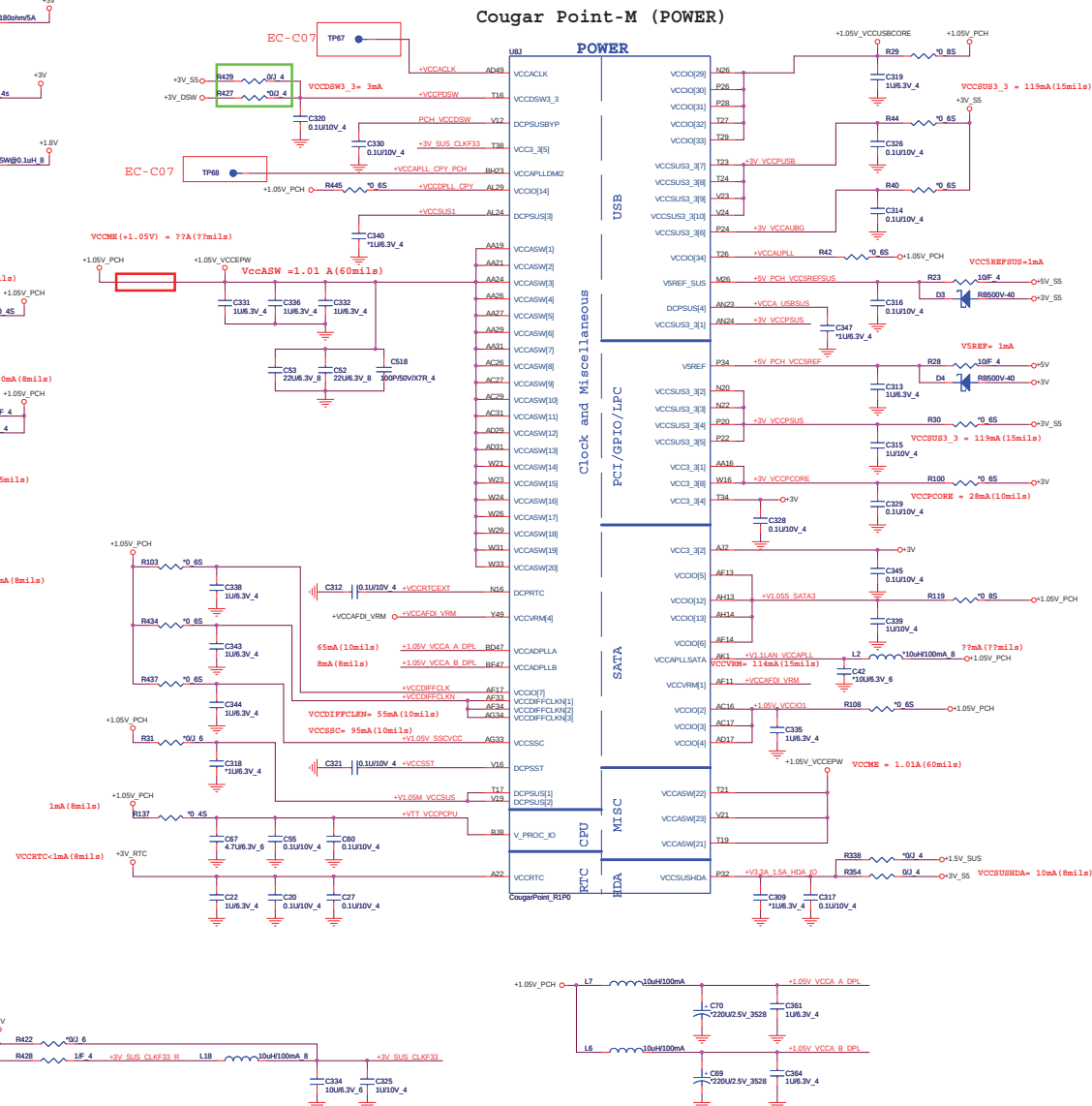


SMBus/Pull-up(CLG)

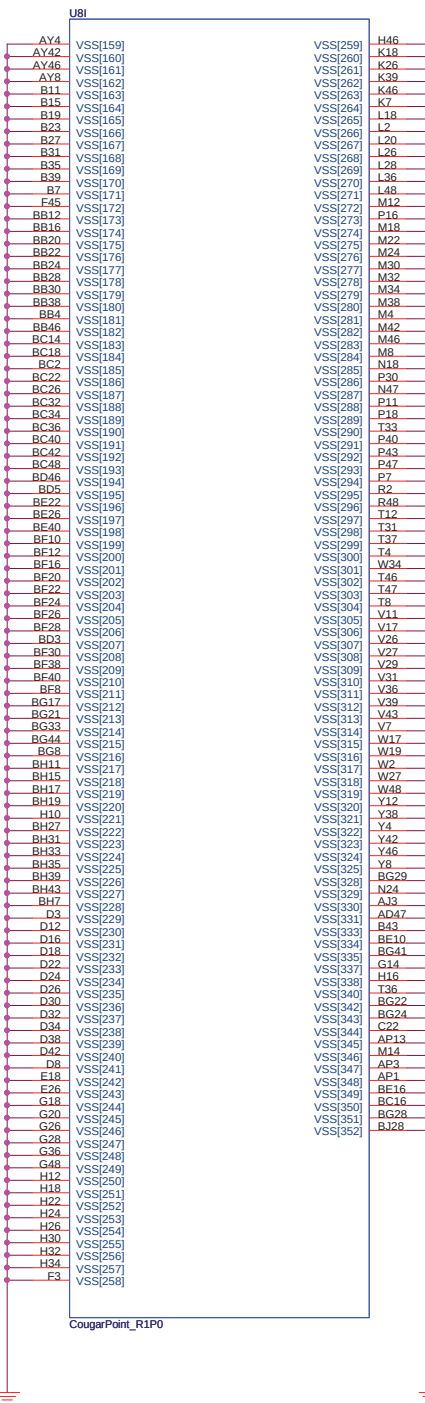
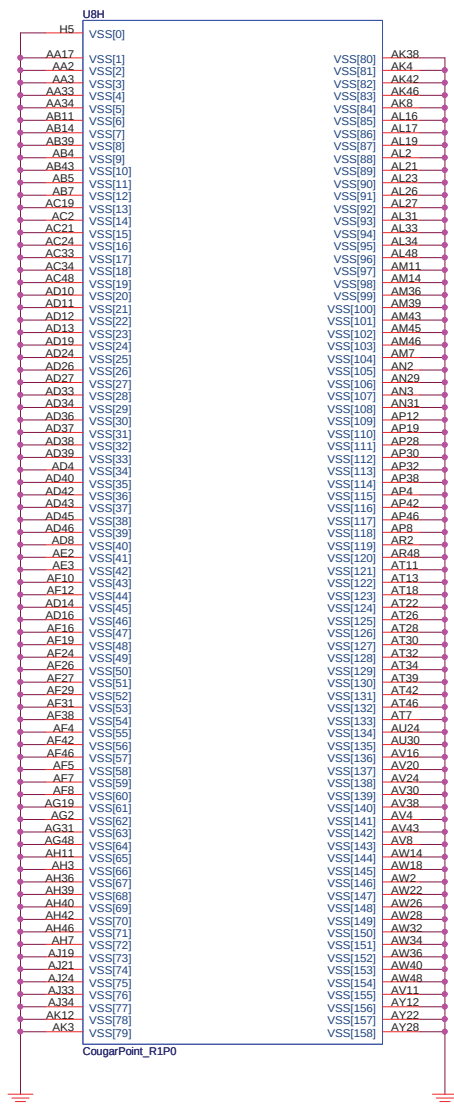


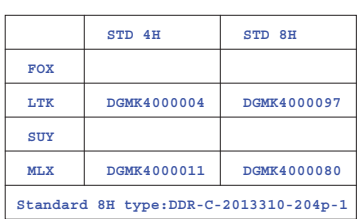
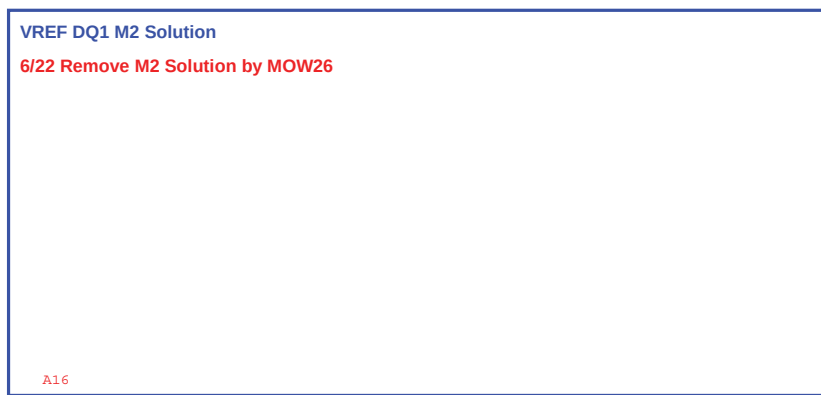
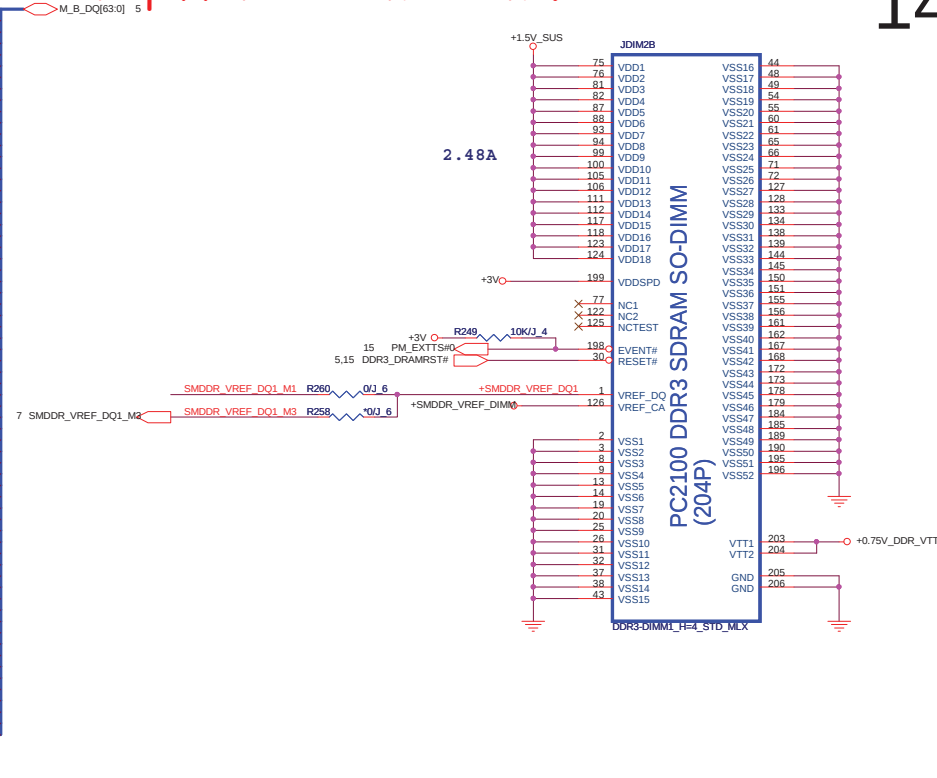


Cougar Point-M (POWER)



IBEX PEAK-M (GND)

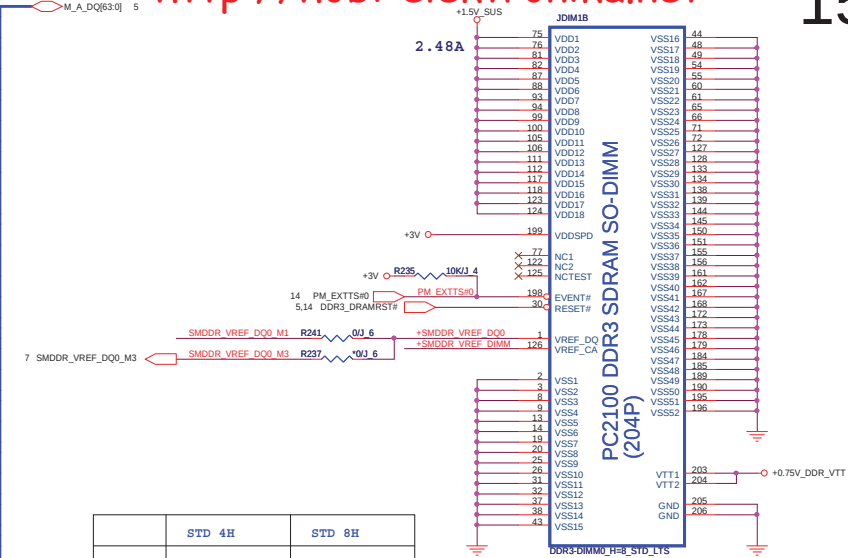
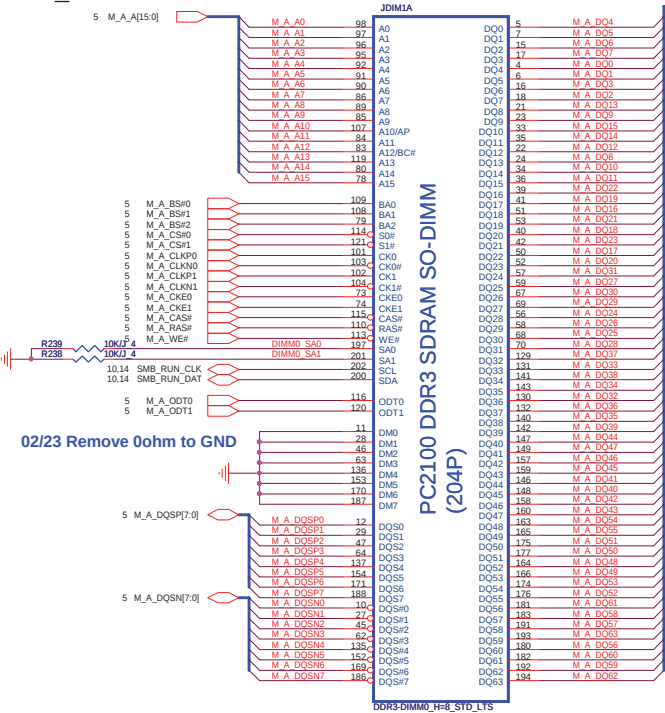




DDR_RVS (DDR)

<http://hobi-elektronika.net>

15



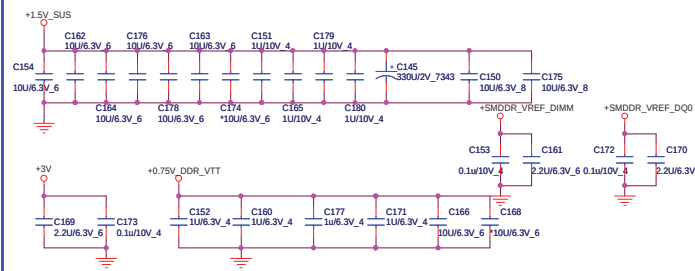
	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

VREF DQ0 M2 Solution

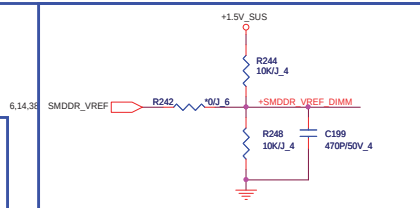
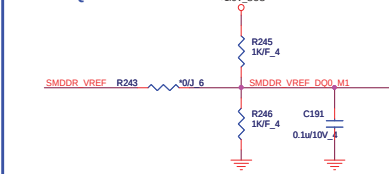
6/22 Remove M2 Solution by MOW26

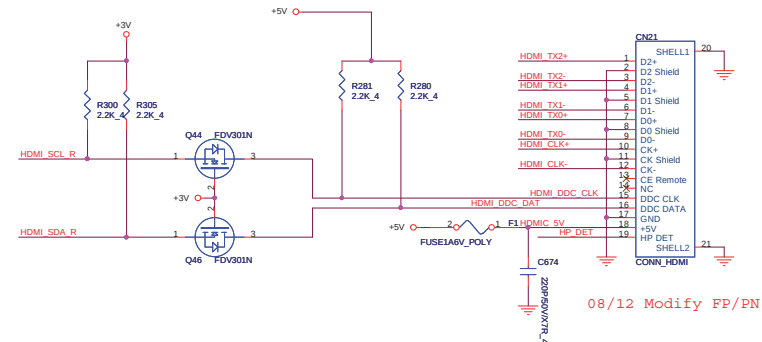
A16

Place these Caps near So-Dimm0.

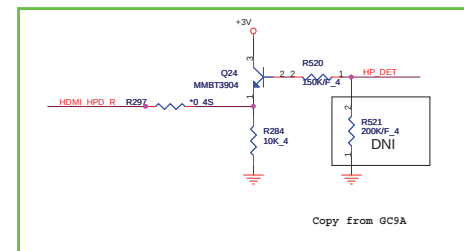


VREF DQ0 M1 Solution

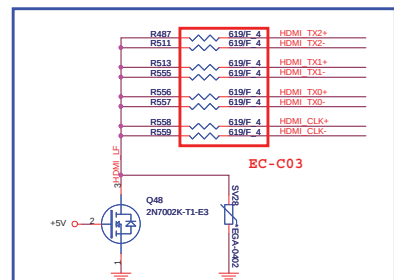
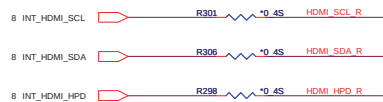
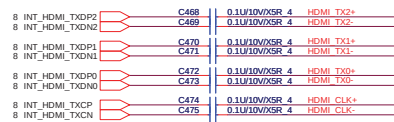




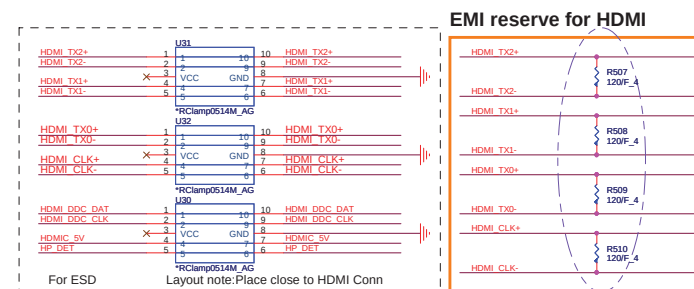
HDMI Hot-PLUG to EC and GPU

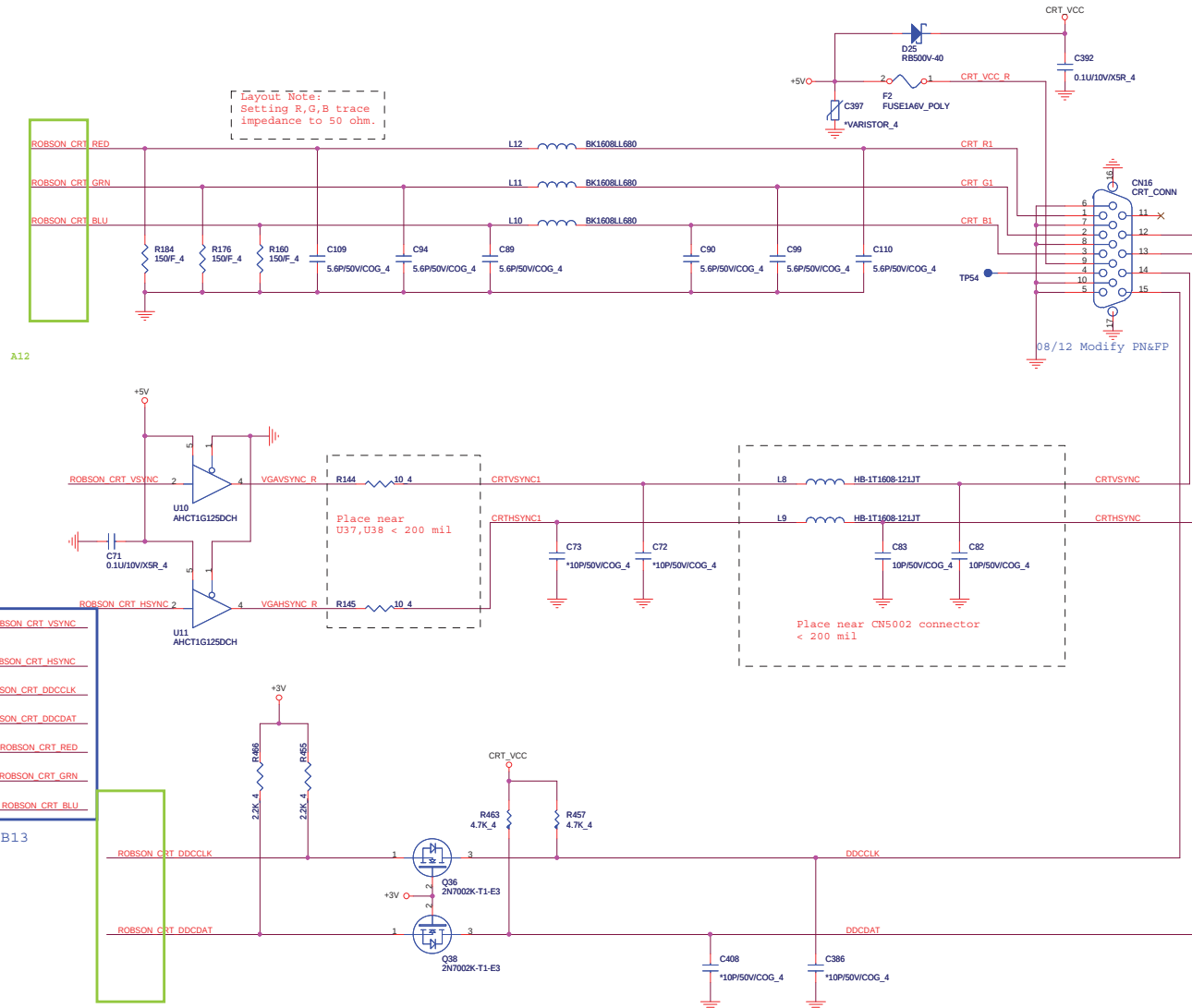
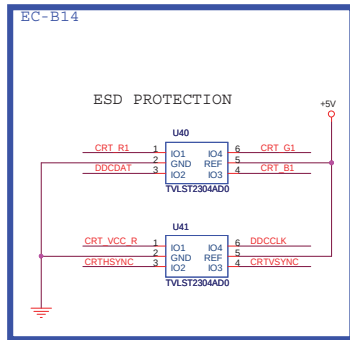


UMA Only

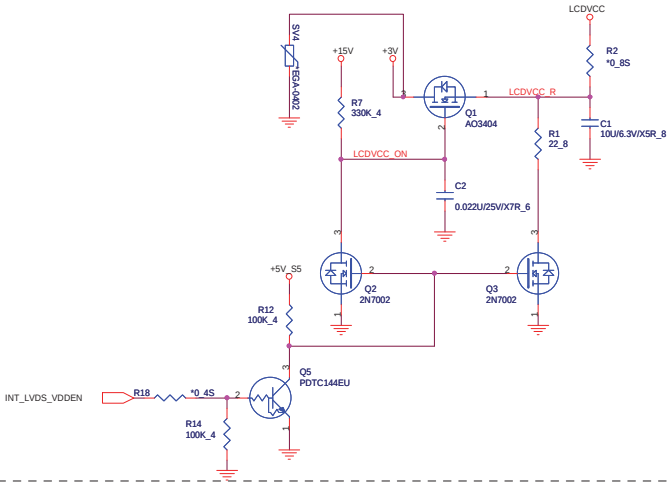


EC-B22

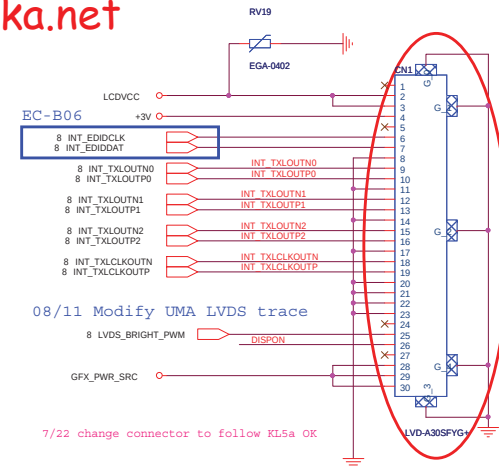
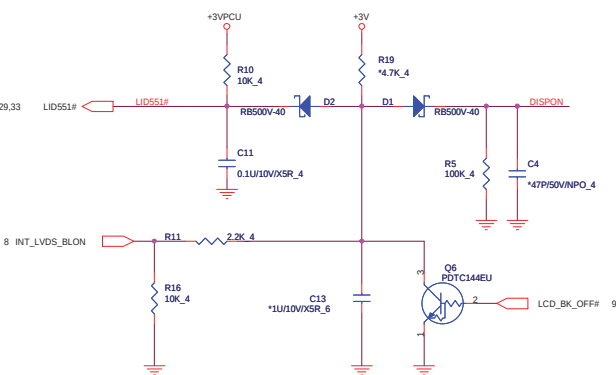




LCDVCC

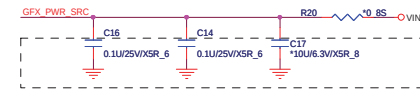


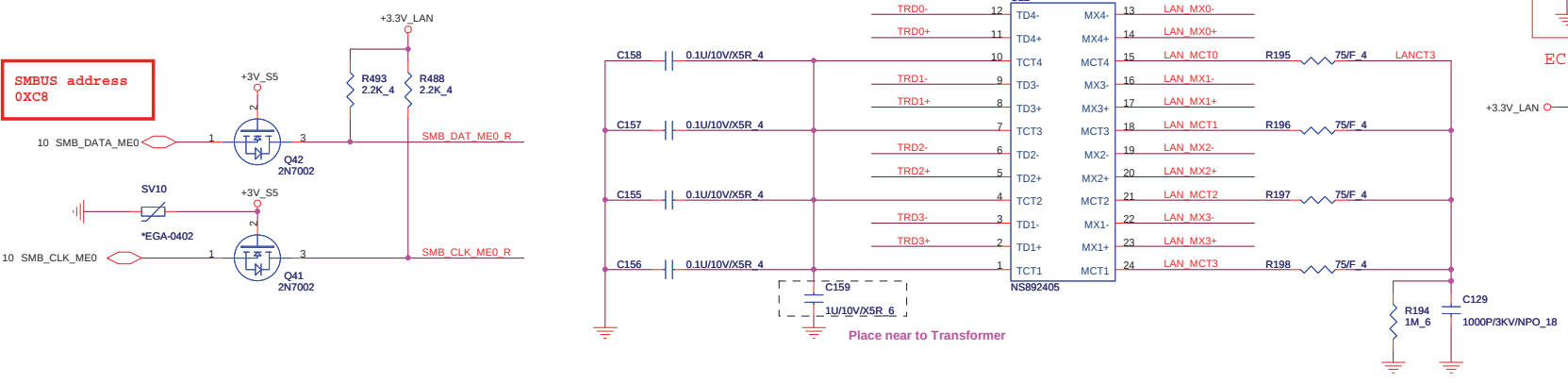
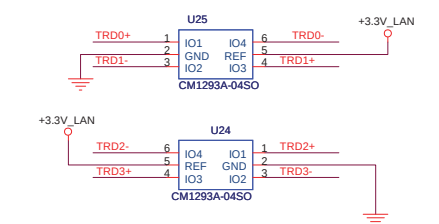
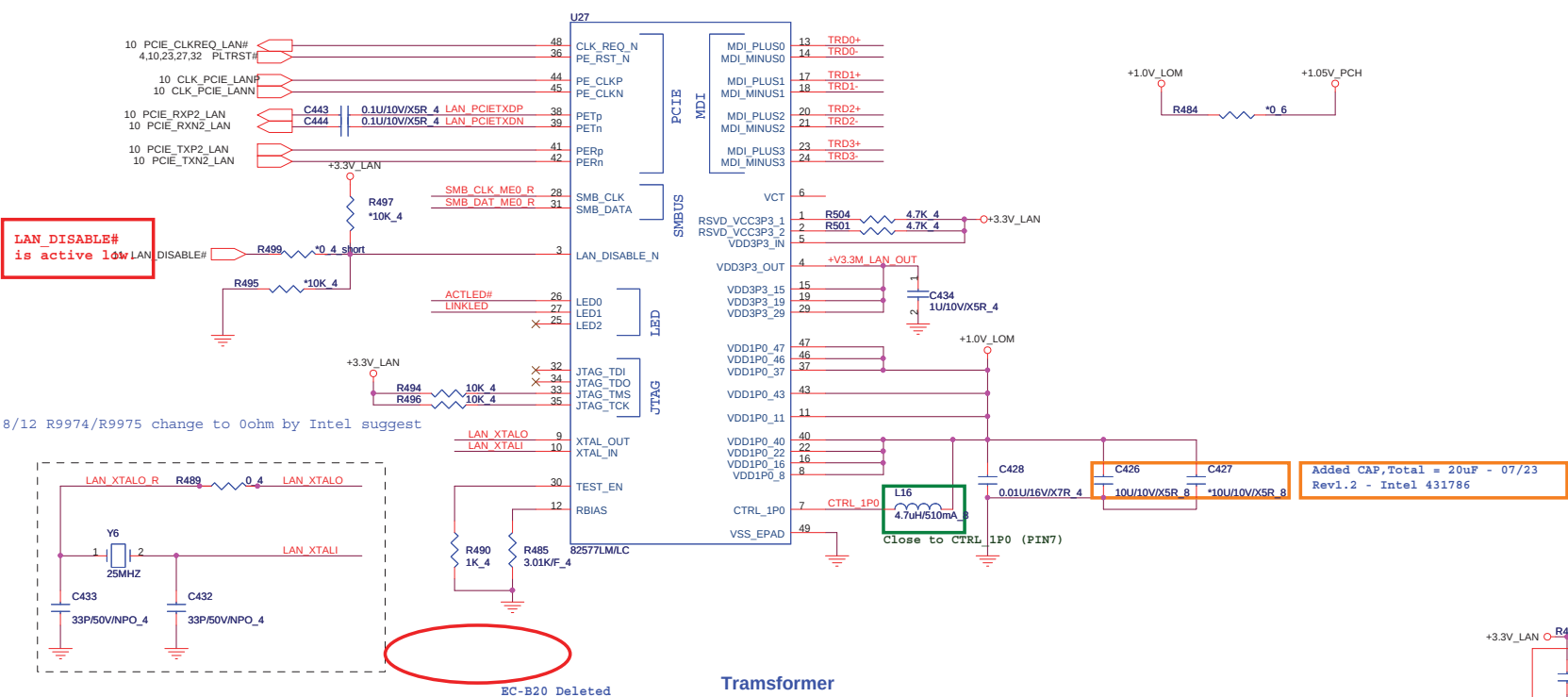
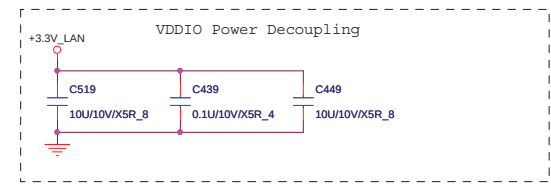
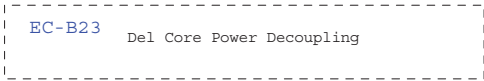
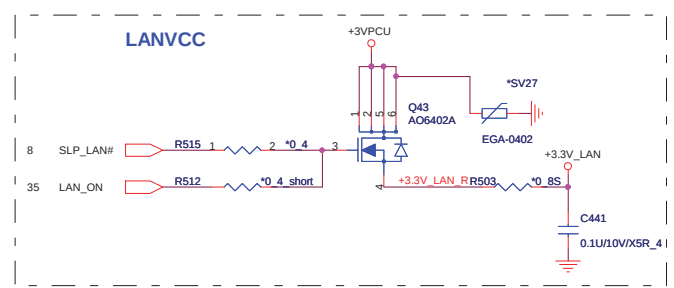
back light



08/11 Modify UMA LVDS trace

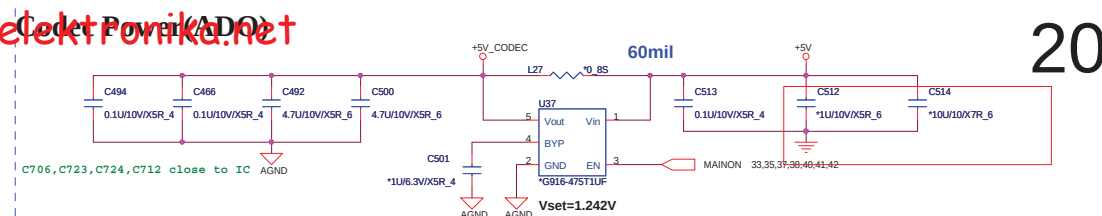
7/22 change connector to follow KL5a OK





Close to CODEC

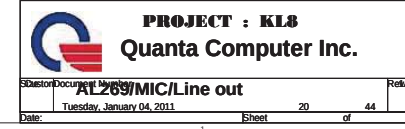
20

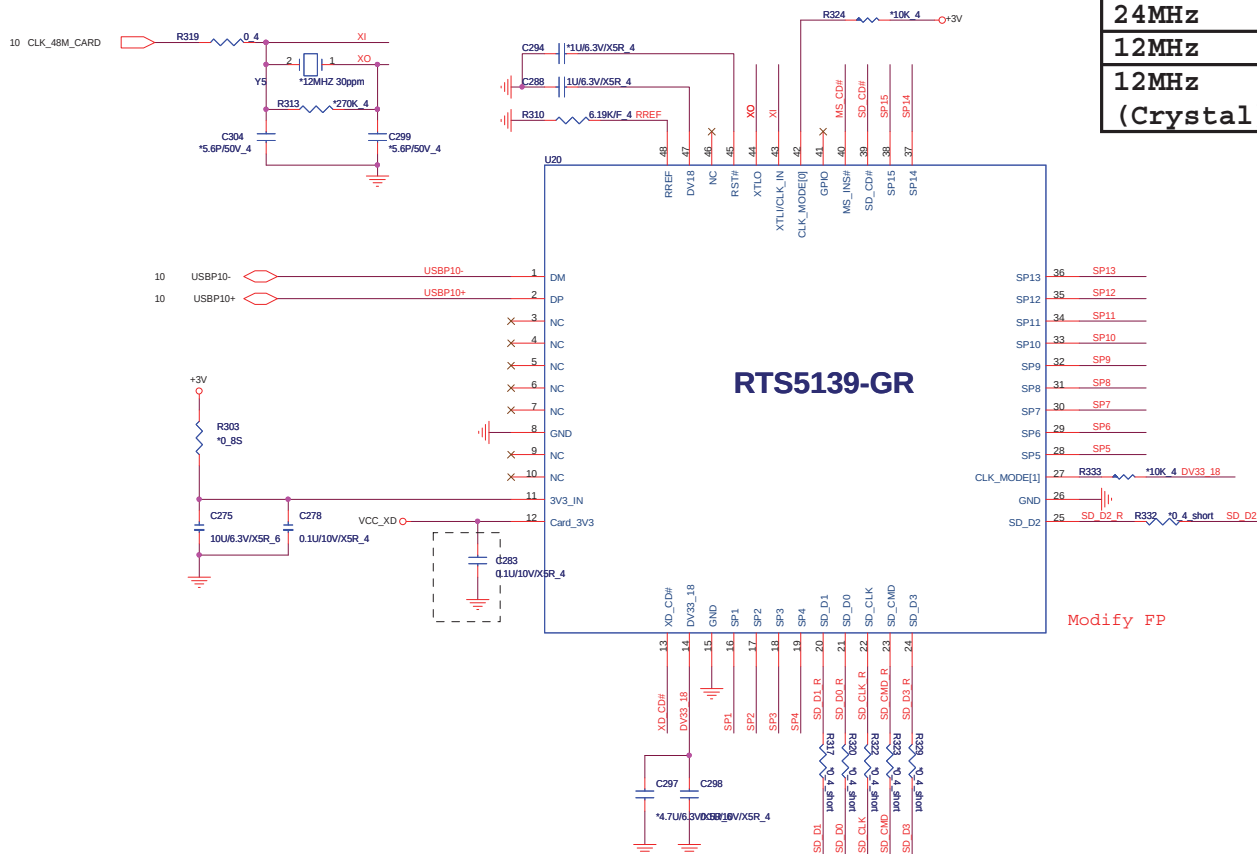


HDA Power(ADO)



Modify FP&PN
Modify Orcad Symbol



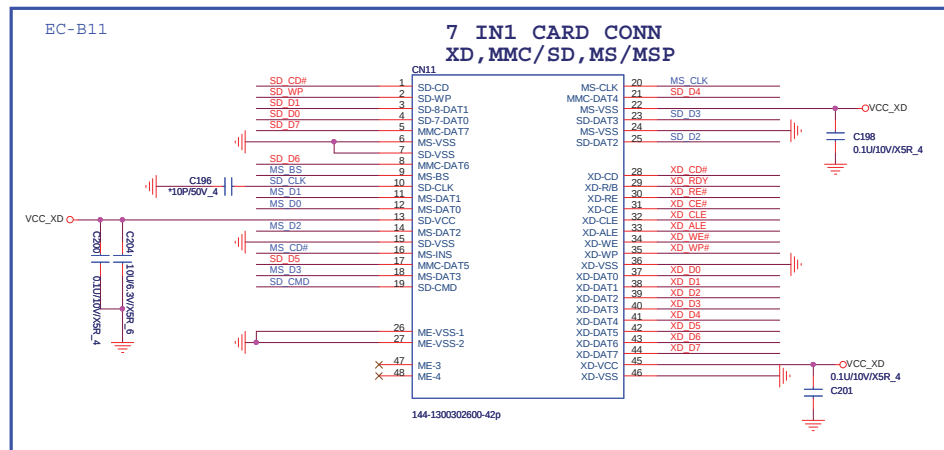


Clock Mode strap	R9287	R9307
48MHz	X	X
24MHz	X	O
12MHz	O	X
12MHz (Crystal)	O	O

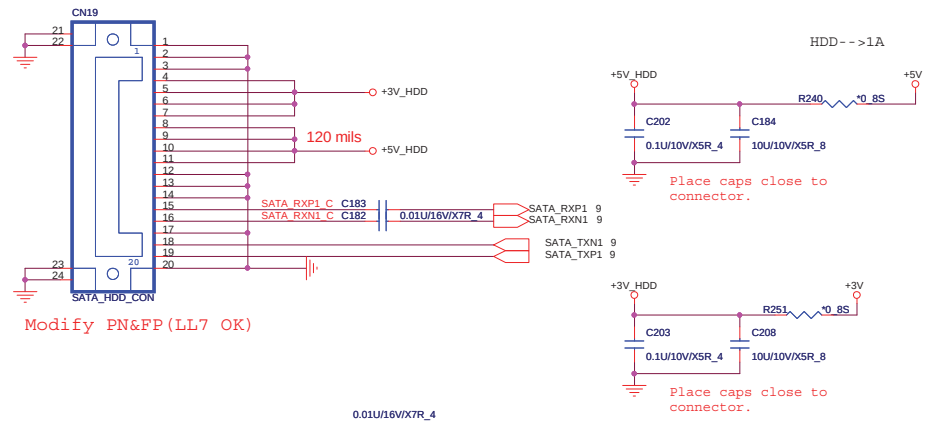
Note:

SD/MMC	MS	XD
SP1	SD D7	XD RDY
SP2	SD D6	XD RE#
SP3	SD D5	XD CE#
SP4	SD D4	XD WE#
SP5	MS BS	XD CLE
SP6	MS D5	XD ALE
SP7	MS D4	XD WP#
SP8	MS D3	XD D0
SP9	MS D2	XD D1
SP10	MS D1	XD D2
SP11	MS D0	XD D3
SP12	MS D3	XD D4
SP13	MS D7	XD D5
SP14	MS CLK	XD D6
SP15	SD_WP	XD D7

For RTS5139

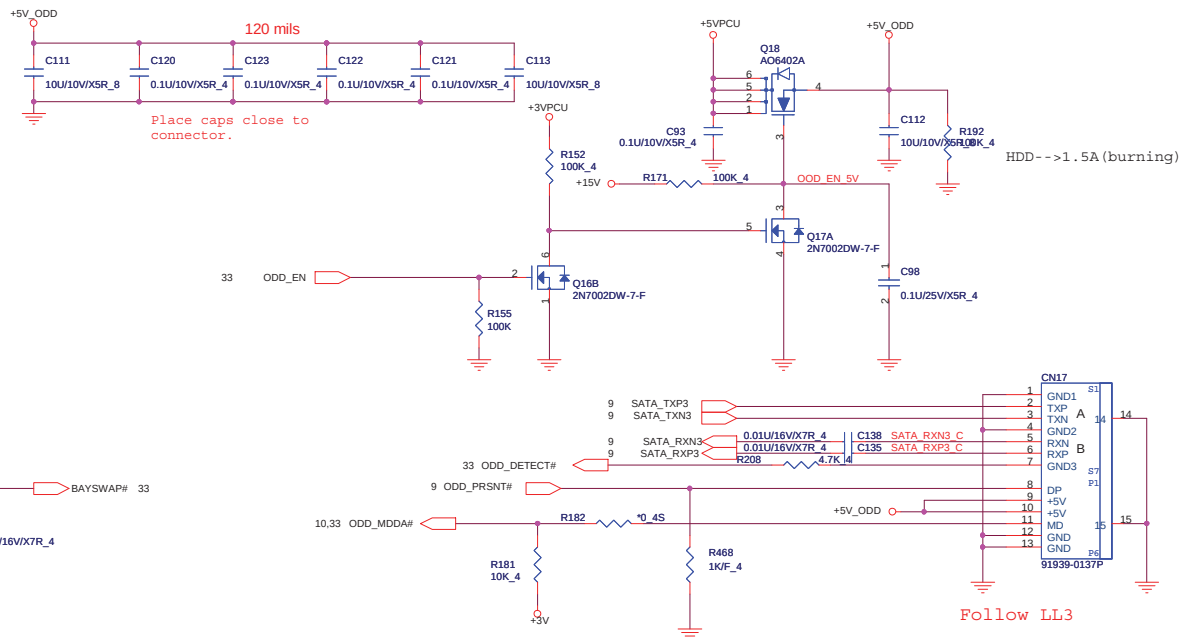


SATA HDD Connector.

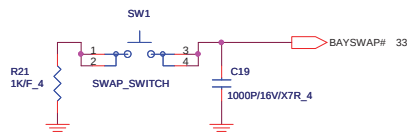


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

SATA ODD Connector.

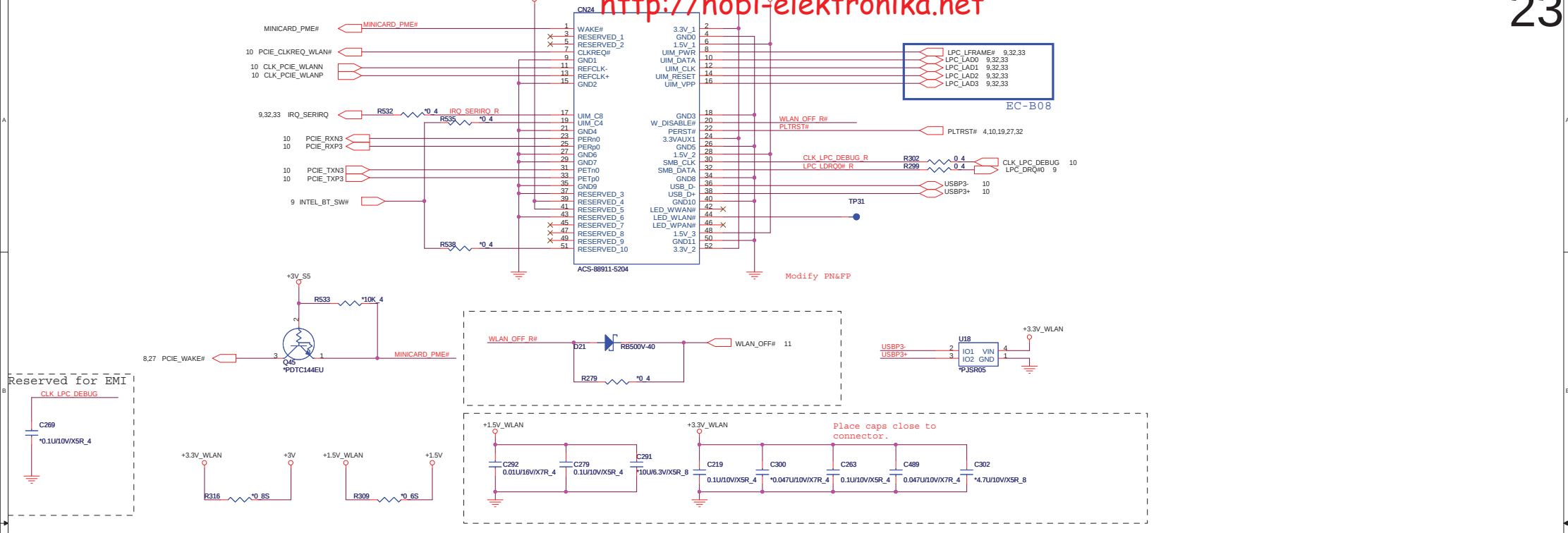


SATA ODD SW



MiniCard WLAN connector

<http://hobi-elektronika.net>



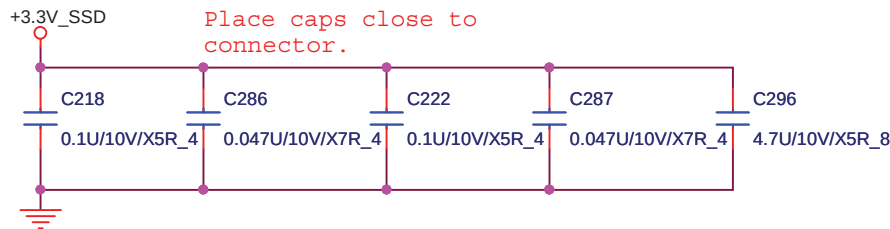
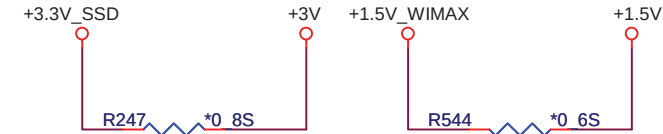
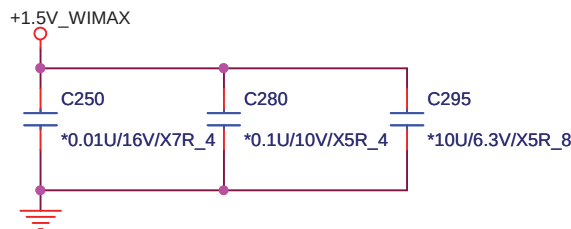
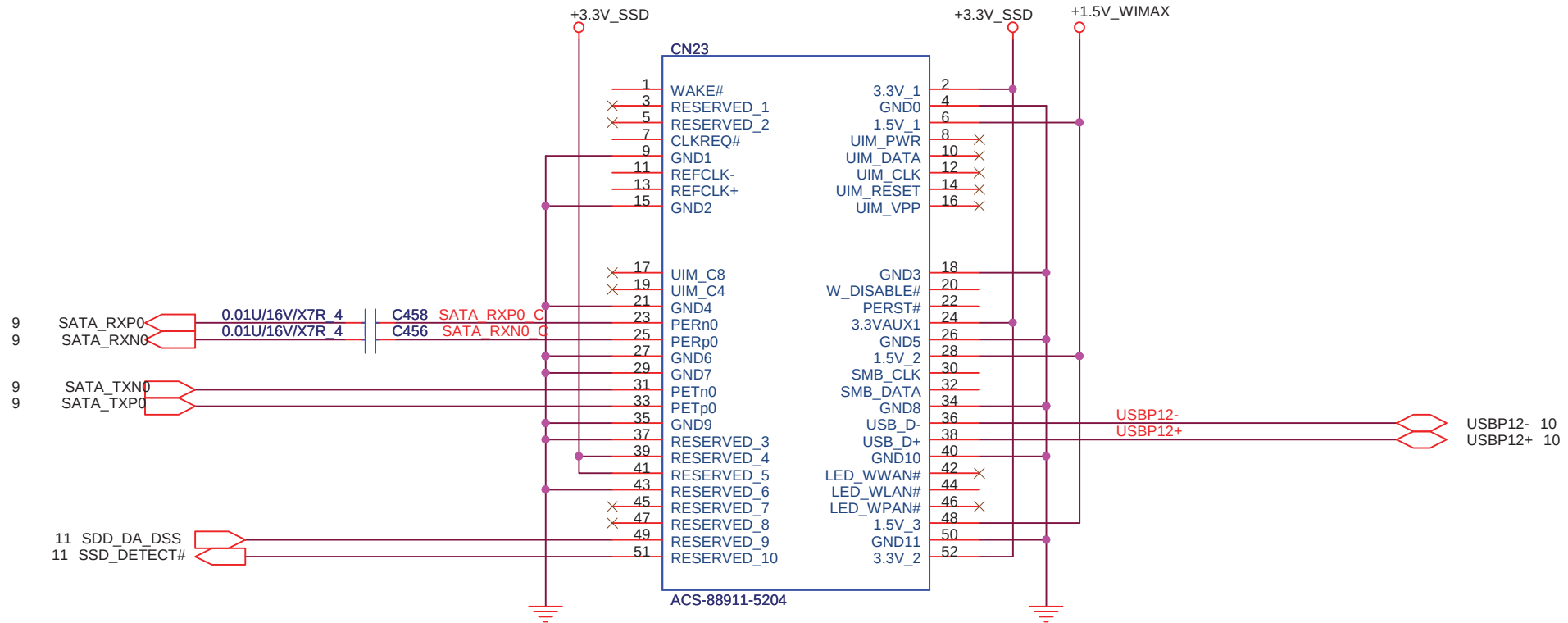
MiniCard WWAN (Reserved for KL9)

Mini PCI-E Card 2 SSD

<http://hobi-elektronika.net>

12,23,26,35,38 +1.5V
8,9,10,11,12,14,15,16,17,18,20,21,22,23,26,27,29,30,32,33,34,35,37,41,42,43 +3V

24

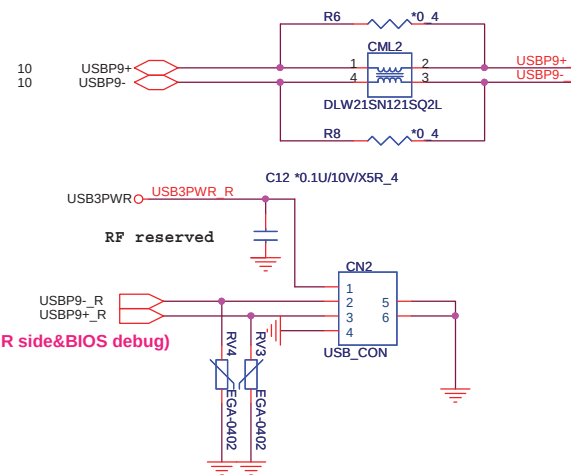
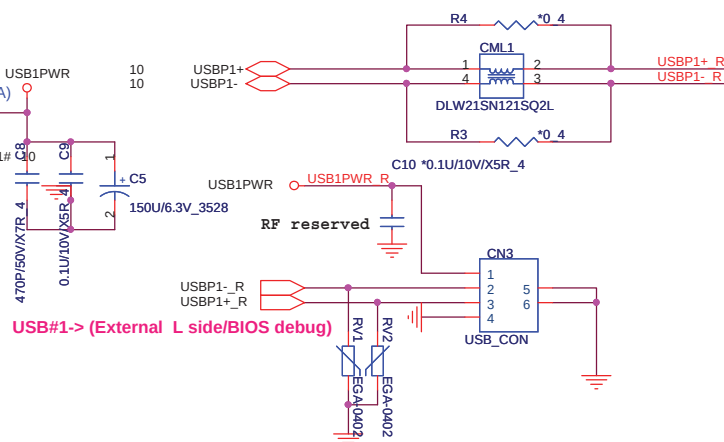


EC-B19

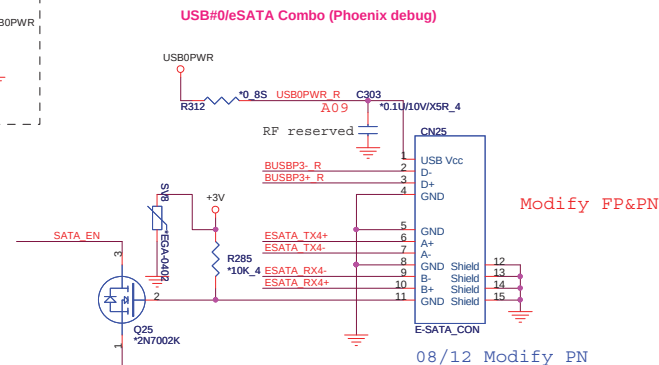
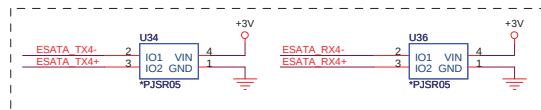
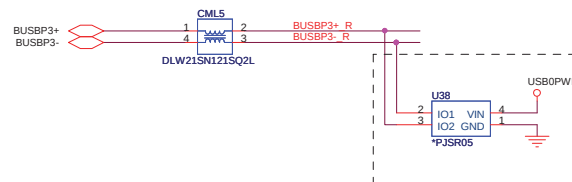
PROJECT : KL8

Quanta Computer Inc.

Size: 1	Document Number: MINI Card (SSD)	Rev: E
Tuesday, January 04, 2011		
Date:	Sheet 24 of 44	

[illegible][illegible]

PROJECT : KL8
Quanta Computer Inc.



Layout: Locate this IC near to conn 2~3 inch, and it can away PCH above 10 inch.

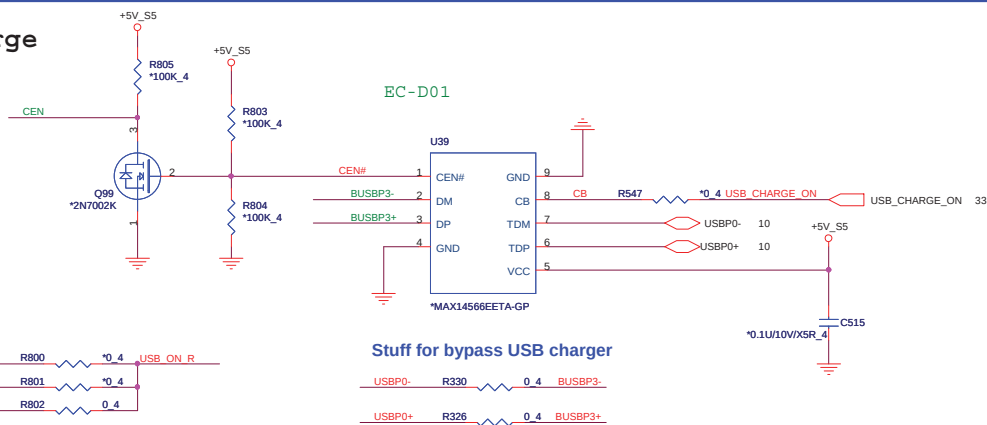
Straps notice:

1. SATA 3G-->600mV ; 0/1 BST#-->H
2. If input length is over 7 inch ; 0/1EQ-->H

Int.PH(150Kohm) : EN, 0/1 BST#

```
Int.PL(150Kohm) : AUTO EN,0/1EQ,0/1 PRE
```

USB Discharge



USB Charge Function					
	R326	R330	R800	R802	State
Enable	X	X	V	X	
Disable	V	V	X	V	Default

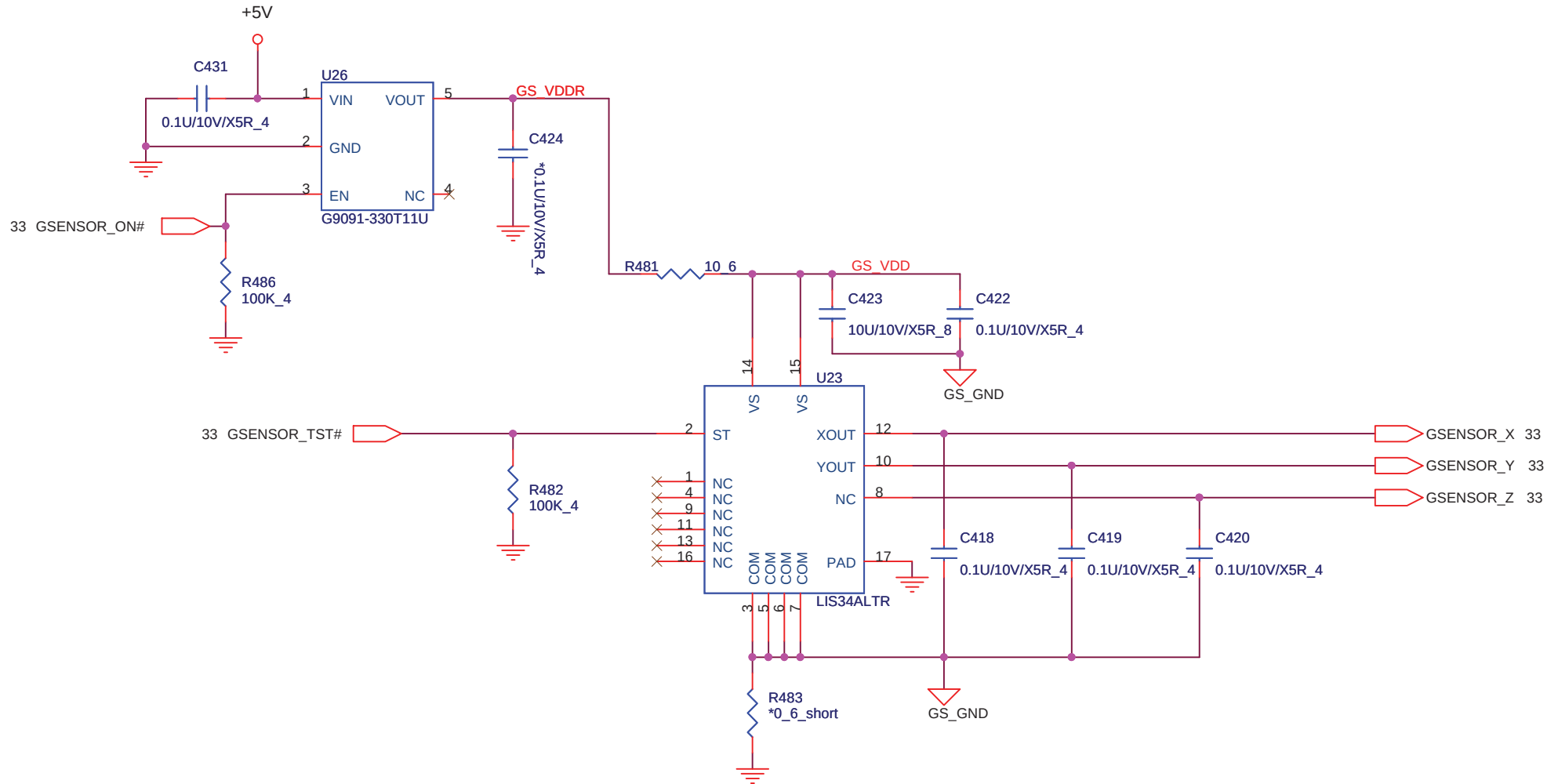
G-SENSOR (3-Axial)

<http://hobi-elektronika.net>

8,9,10,11,12,14,15,16,17,18,20,21,22,23,24,26,27,29,30,32,33,34,35,37,41,42,43 +3V
18,22,27,29,32,35,38,39 +15V



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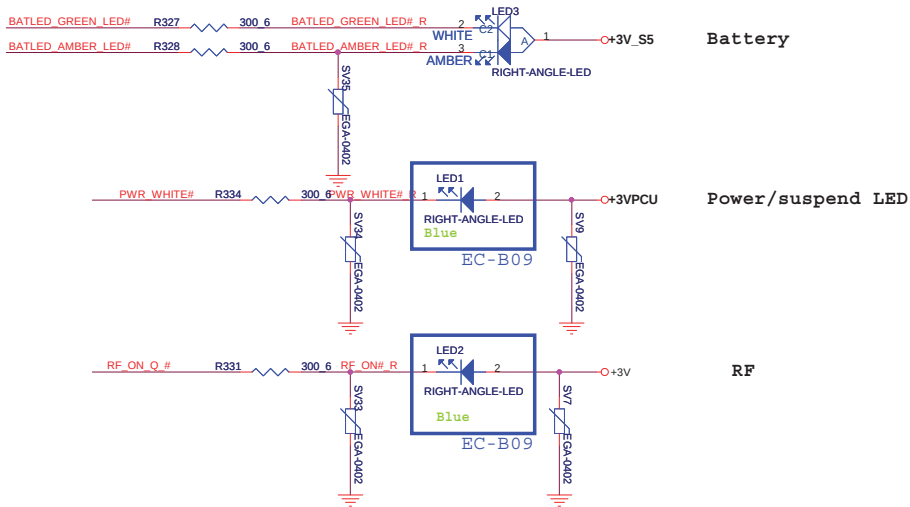
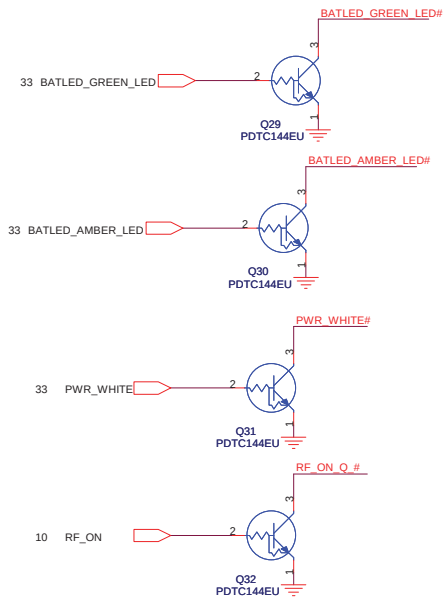




PROJECT : KL8

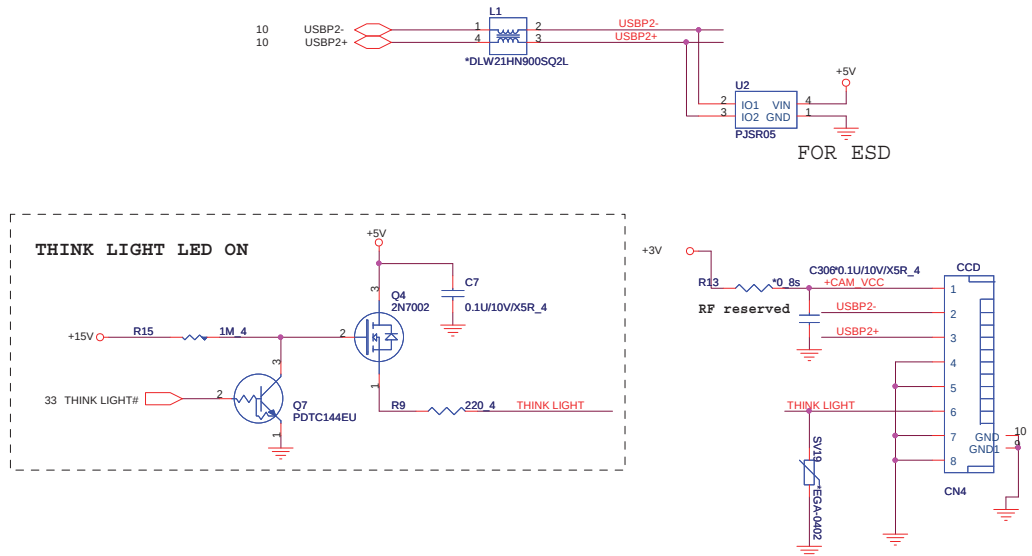
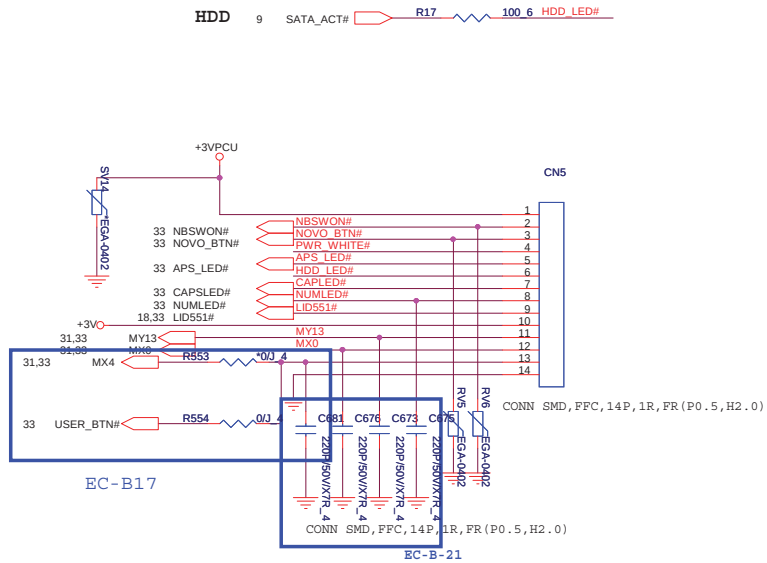
Quanta Computer Inc.

Size	Document Number	G-SENSOR	Rev
	Tuesday, January 04, 2011	28	44
Date:	Sheet	of	
		8	

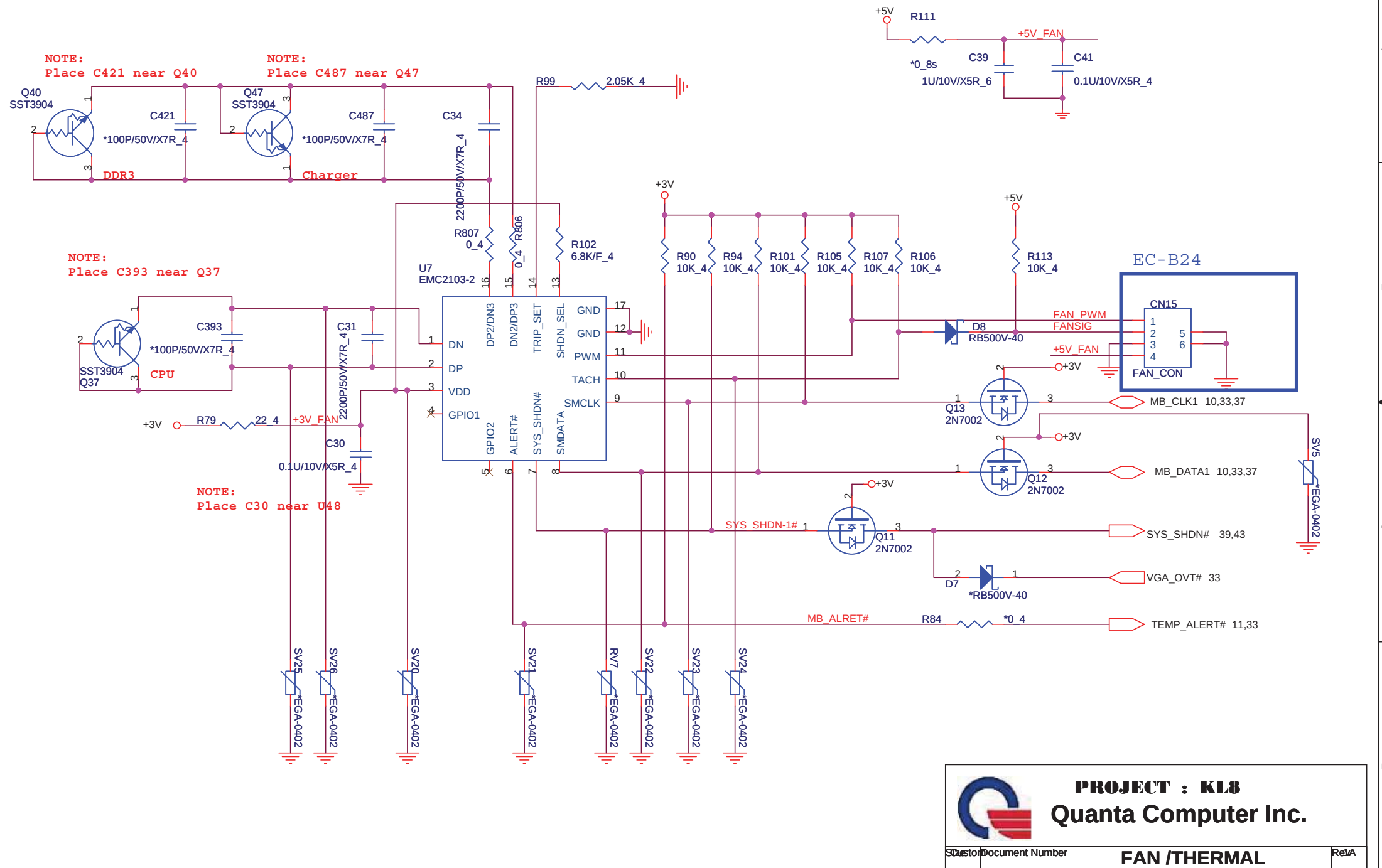


B to B connector

CAMERA & Keyboard light



FAN CONTROL

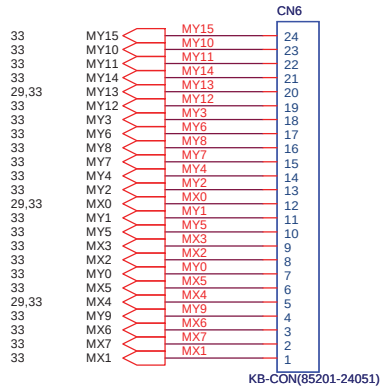




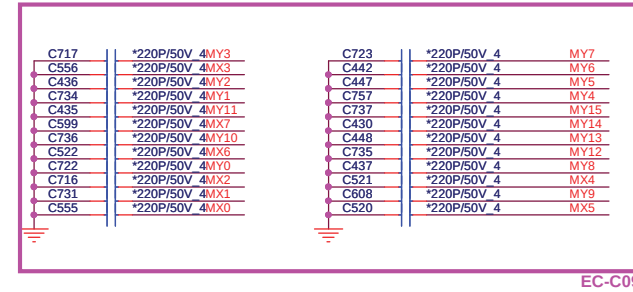
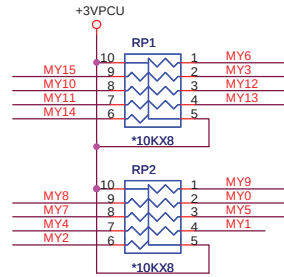
PROJECT : KL8
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Customer Document Number	FAN /THERMAL	Rev A
Date: Tuesday, January 04, 2011	30	44
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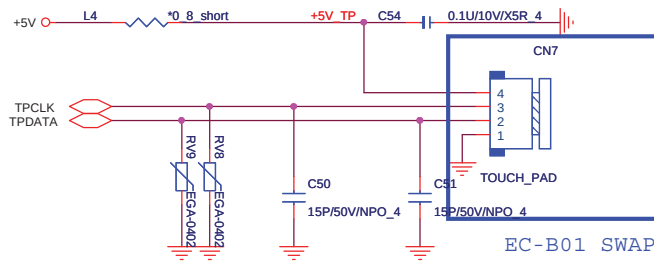
KEYBOARD



Follow LL3 KB



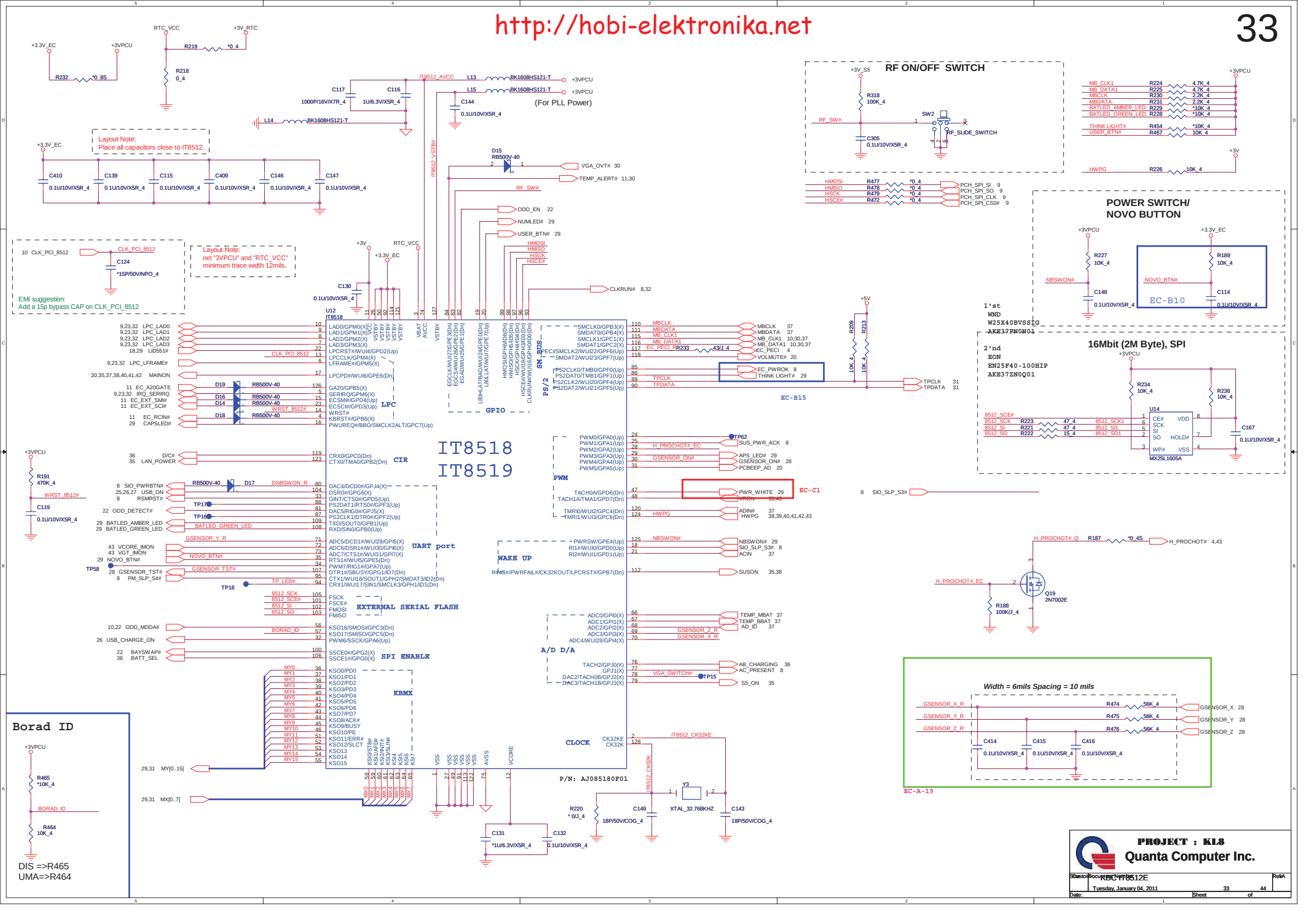
Touch pad

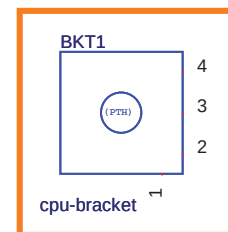


EC-B01 SWAP pin define

Modify PN&FP as ME request.

Follow LL3 Touch Pad

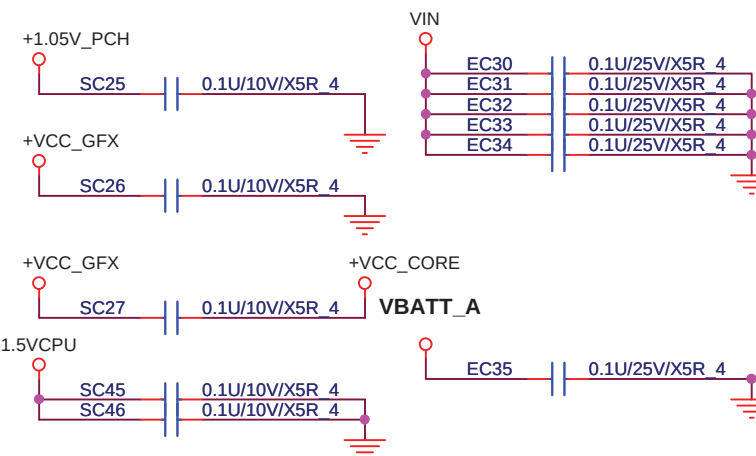
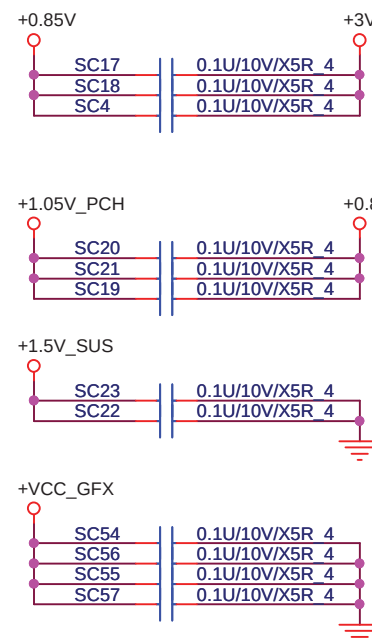
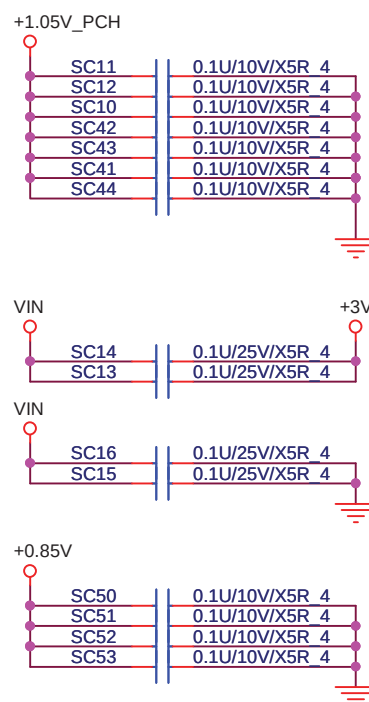




The schematic diagram illustrates the power supply network for the device. It is organized into three main sections, each with a common rail and a specific voltage source.

- Top Section (+VIN_VCC_CORE and +3V):** This section includes three capacitors (SC1, SC2, SC3) connected to a common rail. Each capacitor has a value of 0.1U/10V/X5R 4. The rail is connected to the +3V source.
- Middle Section (+VCC_CORE and +3V):** This section includes five capacitors (SC5, SC6, SC24, SC38, SC39, SC40) connected to a common rail. Each capacitor has a value of 0.1U/10V/X5R 4. The rail is connected to the +3V source.
- Bottom Section (+1.8V):** This section includes three capacitors (SC8, SC9, SC7) connected to a common rail. Each capacitor has a value of 0.1U/10V/X5R 4. The rail is connected to the +1.8V source.

All capacitors are connected to ground, as indicated by the ground symbols at the bottom of each section.

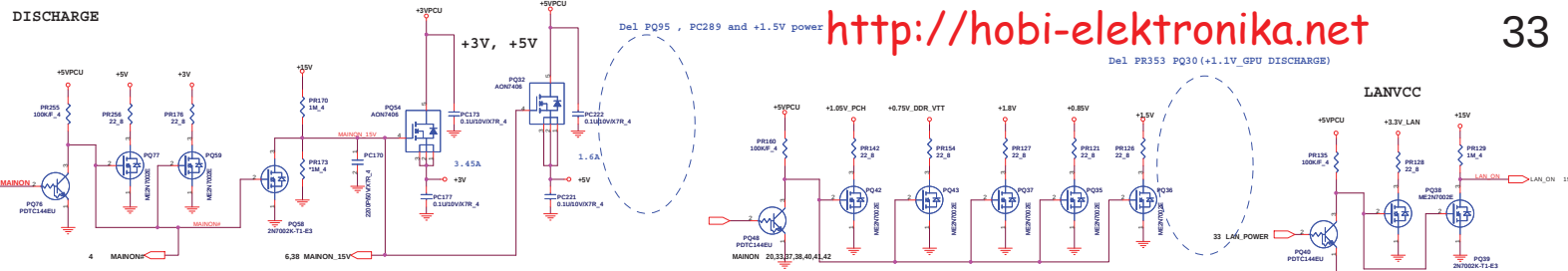


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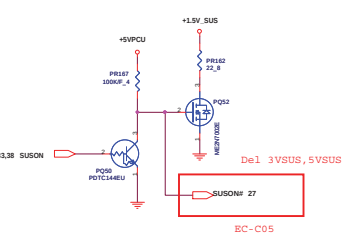
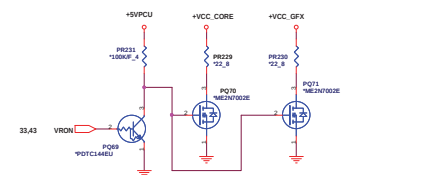
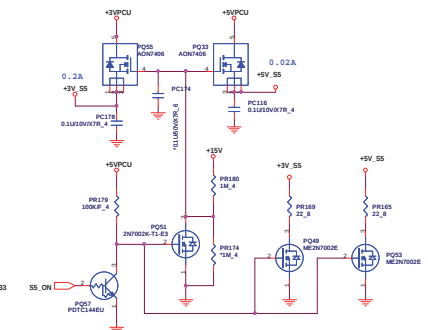
DISCHARGE

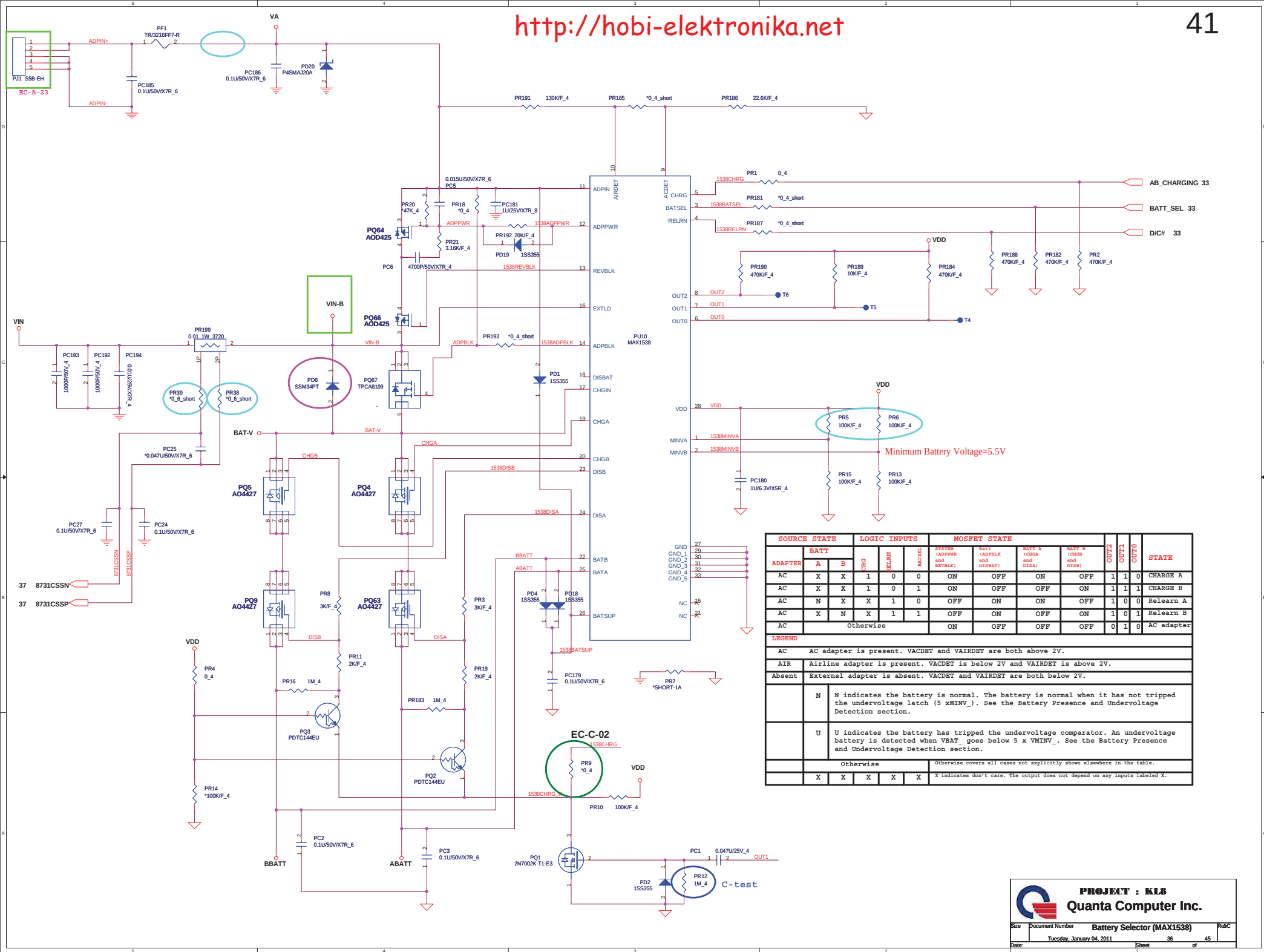
<http://hobi-elektronika.net>

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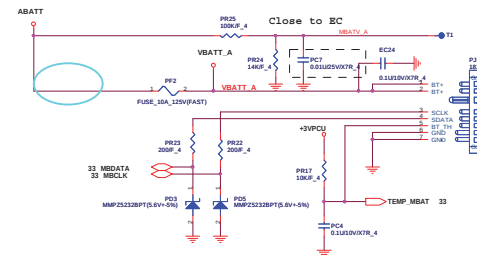
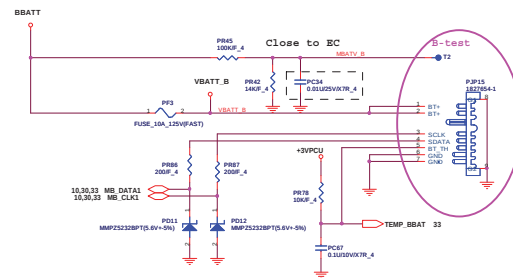
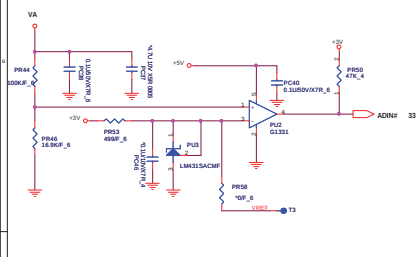
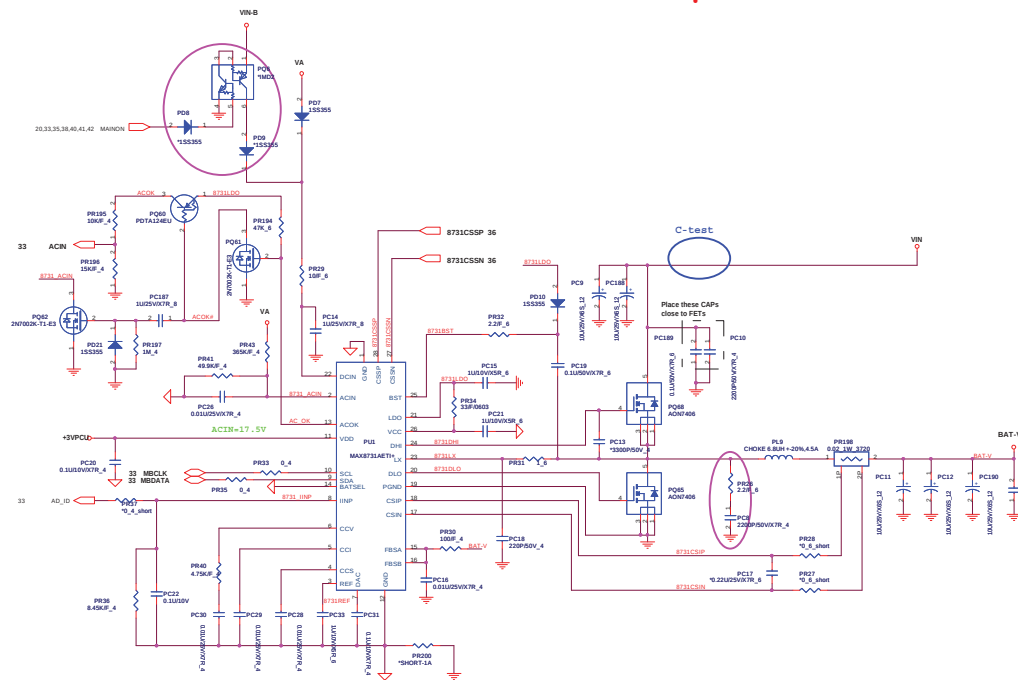


3V_S5, 5V_S5





SOURCE STATE			LOGIC INPUTS				MOSFET STATE							STATE
BATT														
ADAPTER	A	B	DIS	SELN	BATSEL	BATTERY (ADPPWR and REVBLK)	BATT (ADPBLK and DISBAT)	BATT A (CHGA and DISA)	BATT B (CHGB and DISB)	OUT2	OUT1	OUT0		
AC	X	X	1	0	0	ON	OFF	ON	OFF	1	1	0	CHARGE A	
AC	X	X	1	0	1	ON	OFF	OFF	ON	1	1	1	CHARGE B	
AC	N	X	X	1	0	OFF	ON	ON	OFF	1	0	0	Relearn A	
AC	X	N	X	1	1	OFF	ON	OFF	ON	1	0	1	Relearn B	
Otherwise						ON	OFF	OFF	OFF	0	1	0	AC adapter	
LEGEND														
AC		AC adapter is present. VACDET and VAIRDET are both above 2V.												
AIR		Airline adapter is present. VACDET is below 2V and VAIRDET is above 2V.												
Absent		External adapter is absent. VACDET and VAIRDET are both below 2V.												
		N	N indicates the battery is normal. The battery is normal when it has not tripped the undervoltage latch (5 x MINV_). See the Battery Presence and Undervoltage Detection section.											
		U	U indicates the battery has tripped the undervoltage comparator. An undervoltage battery is detected when VBAT goes below 5 x VMINV_. See the Battery Presence and Undervoltage Detection section.											
Otherwise						Otherwise covers all cases not explicitly shown elsewhere in the table.								
		X	X	X	X	X	X indicates don't care. The output does not depend on any inputs labeled X.							

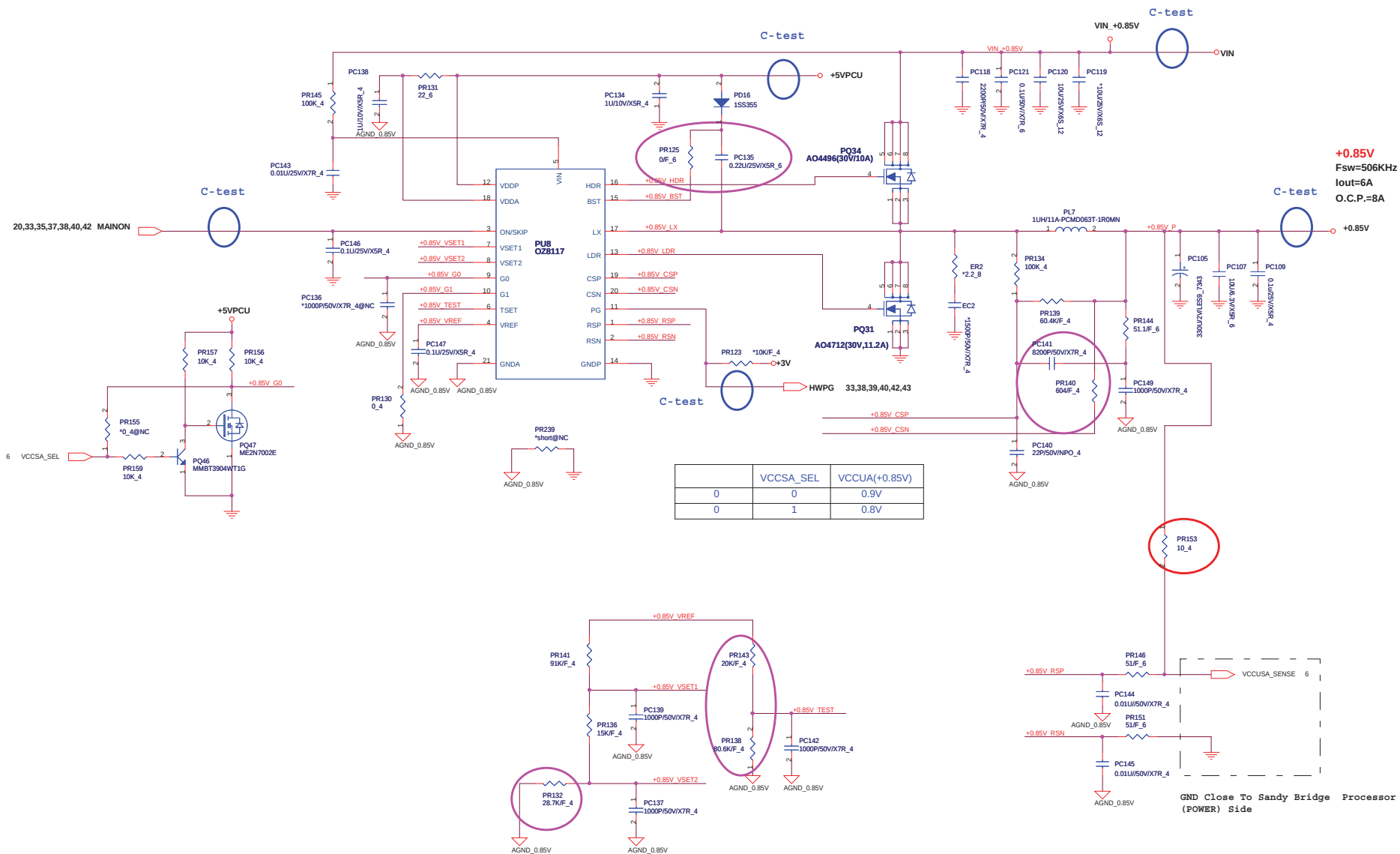




Change to +1.5V_SUS



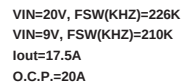




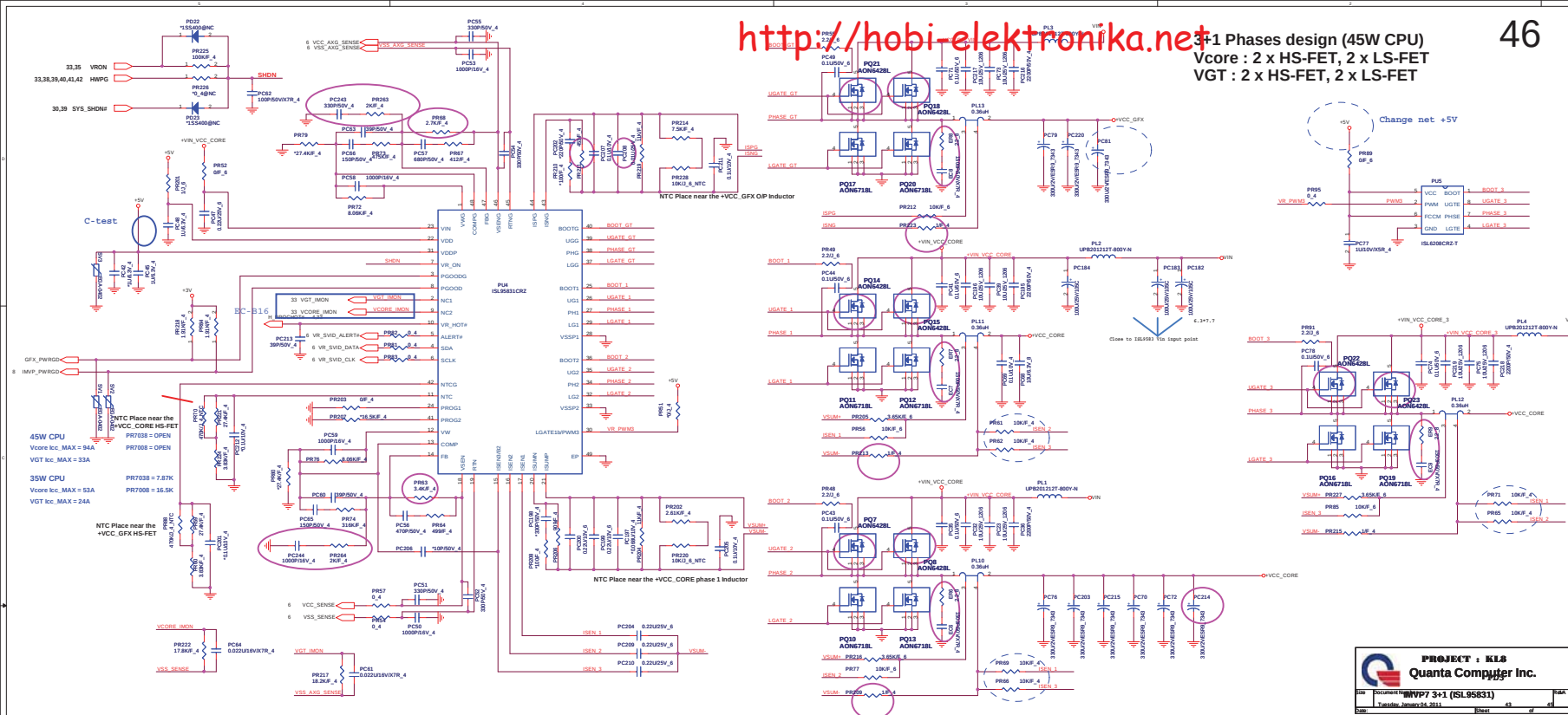
- ▶ NVVDD $\leq$ VDD33+0.5 V
- ▶ FBVDDQ $\leq$ VDD33+0.5 V

C-test

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Del +1.5V SW



EC #	Page	Description	Part Affected
B01	31	Swap touch pad pin define	
B02	20	Change D23 to diode	
B03	20	Add audio jack normal open circuit	
B04	26	Swap Esata RX pin	
B05	26	Charge IC F/P change	
B06	18	Swap LCD SMBUS	
B07	32	Add 0ohm on F/P	
B08	23	LPC L0~L3 swap	
B09	29	Change LED F/P	
B10	33	Novo_BTN# pull high 10k	
B11	21	Add SD3.0 circuit	
B12	04	Change U13 P/N	
B13	17	Del CRT 0ohm	
B14	17	Modify CRT ESD protection	
B15	11	Change PCH GPIO define for same as KL7/8/9	
B16	23	Add WLAN_off#	
B17	29	Change USER_BTN# to EC GPIO	
B18	04	Del SW reserve 0ohm	
B19	24	Modify SSD circuit	
B20	27	Change 25M CLK from LAN to USB3.0	
B21	29	Add cap for EMI reserve	
B22	16	Add HDMI Res for level shift	
B23	19	Del Lan decoupling cap	
B24	30	Modify Fan conn pin define	
B25	09	Del JTAG circuit	
B26	11	Modify Board ID	



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EC #	Page	Description	Part Affected
C01		Del R162	
C02		Change R487,R511,R513,R555,R556,R557,R558,R559 to CS16802FB09 for HDMI solution	
C03		Del R203,U13,C141; Add R202(0ohm) for cost down	
C04		Add Q60, R693, Q59, C824, R382, R384, R388	
C05		Add C440	
C06		Change R377 to 100k ohm	
C07		Add C399, C378, C398	
C08		Del R180,R110,R104,R433,C514,C512, R378, R535, R538 for cost down	
C09		Add CYAVL5M0B00 on SV1~15 and SV16~24; Add CYAVLC18B02 on SV27~37	
C10		Del R122,R133,R212,R157,R169,R170,R365, R386,R360,R376,R366,R357,R38,R359,R77,R407,R63,R404,R435,R137,R301,R306,R298,R297,R18,R499,R182,R187 for 0402 0	
C11		Del R114, R419,R44,R40,R42,R30,R100,R108,R103,R434,R437,R445,R309,R121,R544 for 0603 0ohm cost down	
C12		Del R29,R119,R449,R120,R115,R2,R20,R503,L2,L23,R303,R240,R251,R247,R316,R312,L4,R232 for 0805 0ohm cost down	
C13		Change R118,R141,R125 from CS+0026F203 to CS00006J248	



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