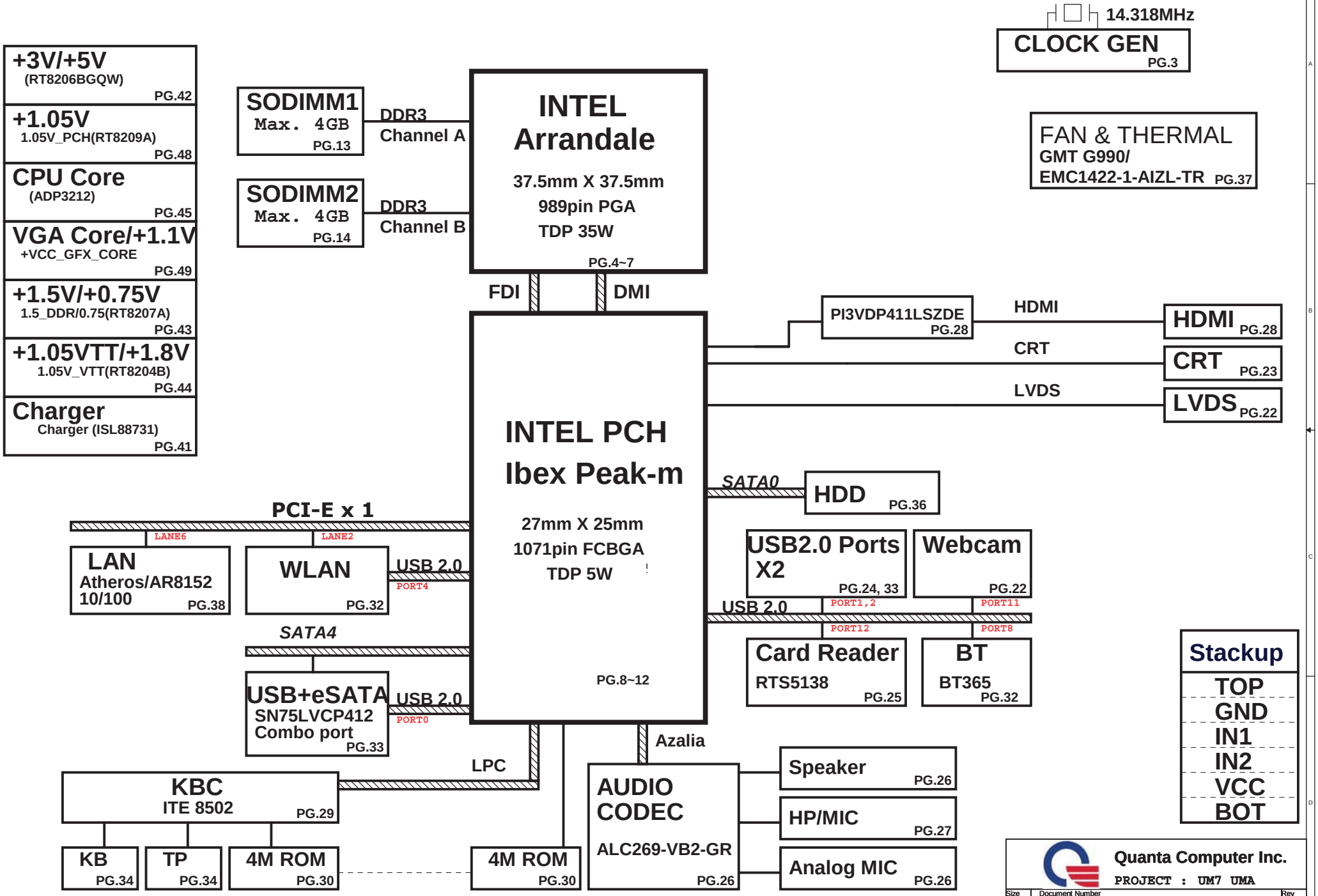
UM7 UMA SYSTEM DIAGRAM



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Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

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23	CRT CONN
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26	Azalia (ALC269)
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47	DCin & Batt
48	1.05V_PCH(RT8209A)
49	GFX_VCORE (ADP3211)
50	Power Block Diagram
51	Power sequence Block

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	23,42,43,44,45,46,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	09,12,30,31	RTC		S0~S5
+5V_ALW	+5V	37,43,44,47,48	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	30,31,37,42,43,45,47,48	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	12,25,34,37,43,44,45,46,47,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	03,08,09,10,11,12,23,35,37,39,41,46,47,50	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	04,06,14,15,44,47	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	14,15,44	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	08,12,23,24,27,28,29,35,36,3738,47	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,4,8,9,10,11,12,14,15,23,24,26,27,28,29,30 ,31,33,34,36,37,38,39,41,47	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	6,12,45	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	4,6,11,12,45,46	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	12,33,47	PCH/Min Card	RUN_ON	
+1.05V_PCH	+1.05V	3,8,9,10,12,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	6,46	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	23	LCD Power	LCDVCC_TST_EN & ENVDD	

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

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	BLOCK DIAGRAM	1A

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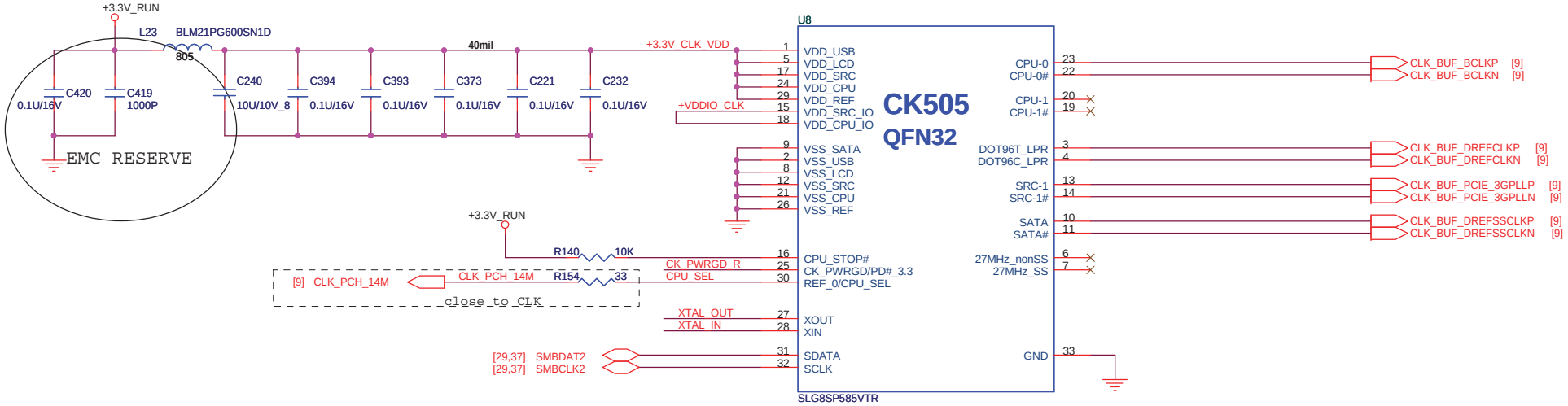

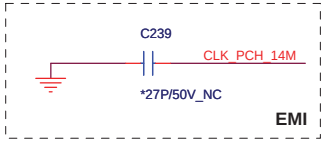

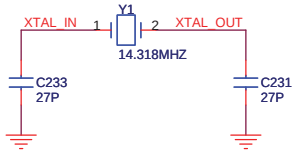

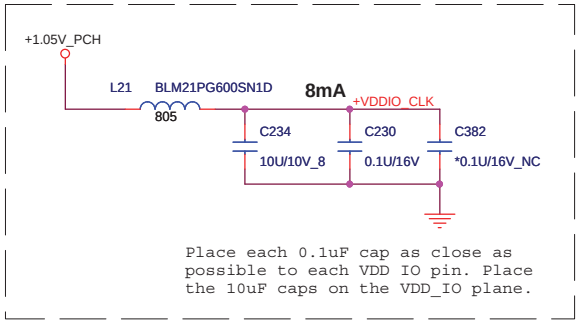

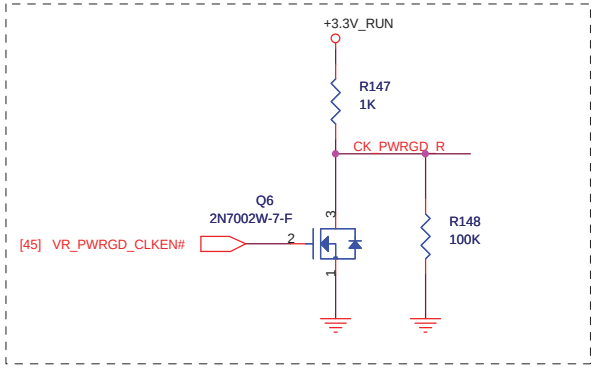

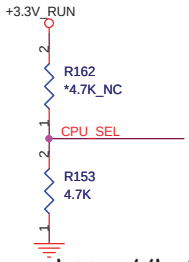

PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

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PROJECT : UM7 UMA

Size	Document Number	Rev
	Clock Generator	1A

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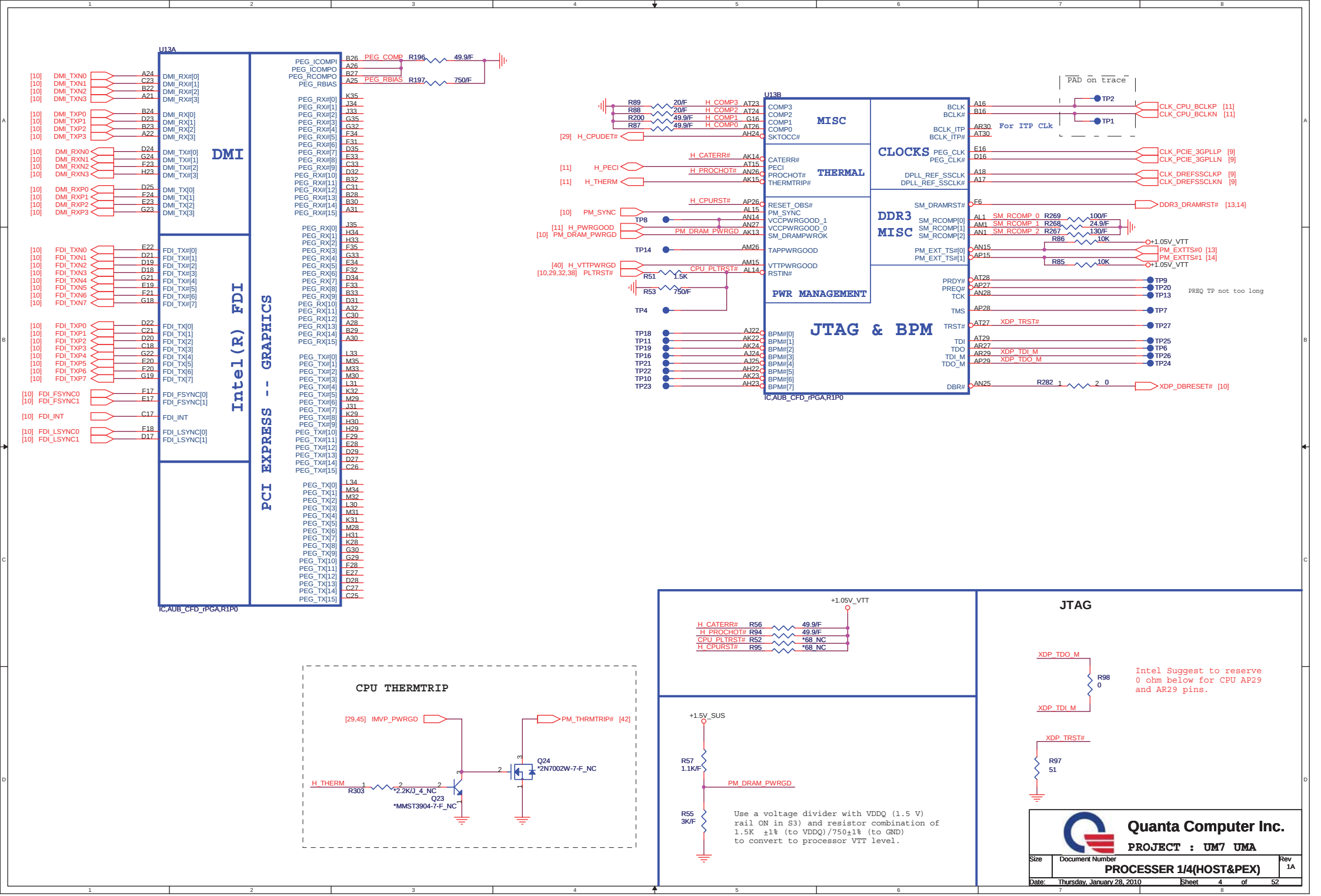

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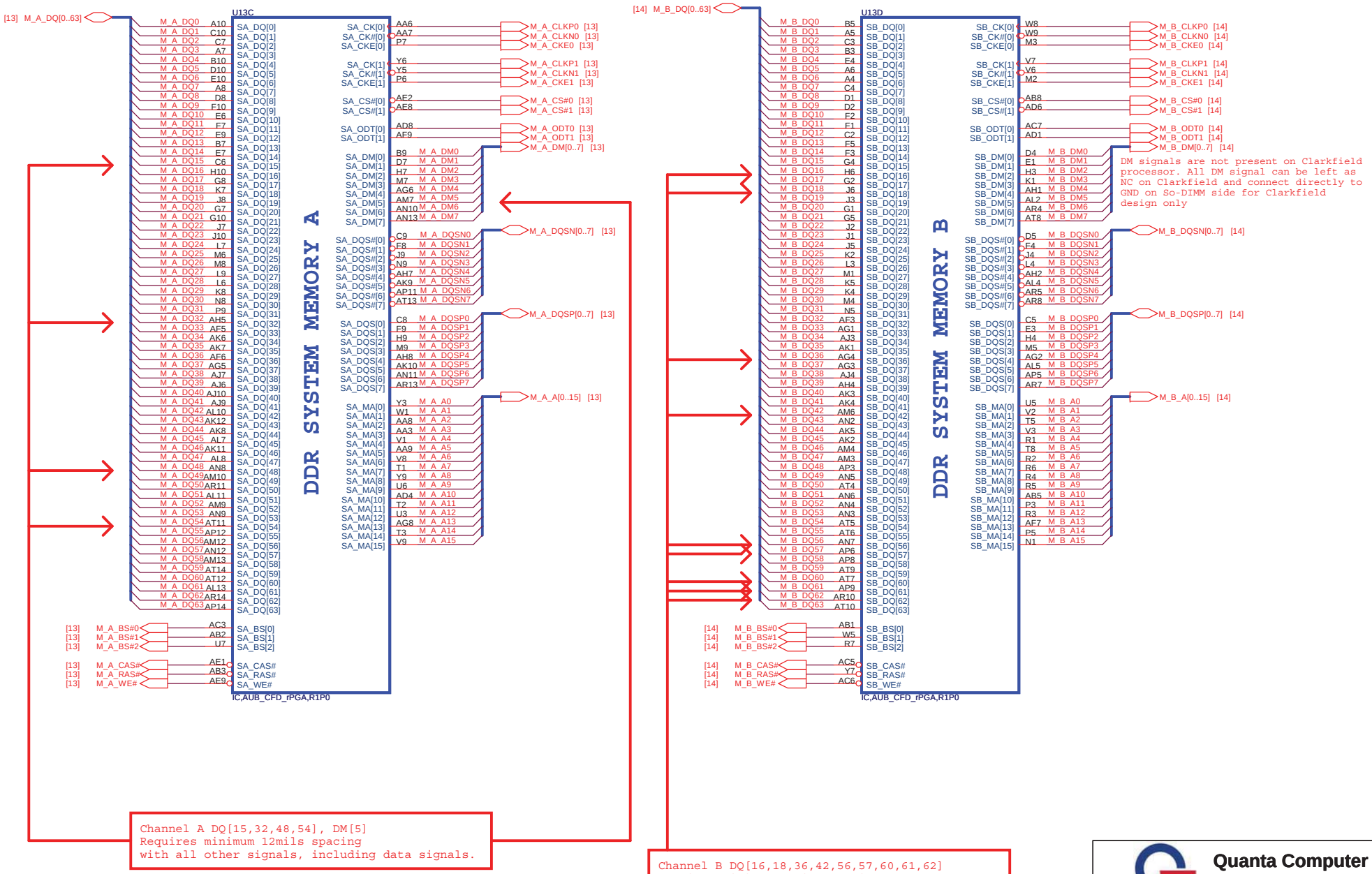
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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PROJECT : UM7 UMA

Size	Document Number	Rev
	PROCESSER 2/4(DDR)	1A

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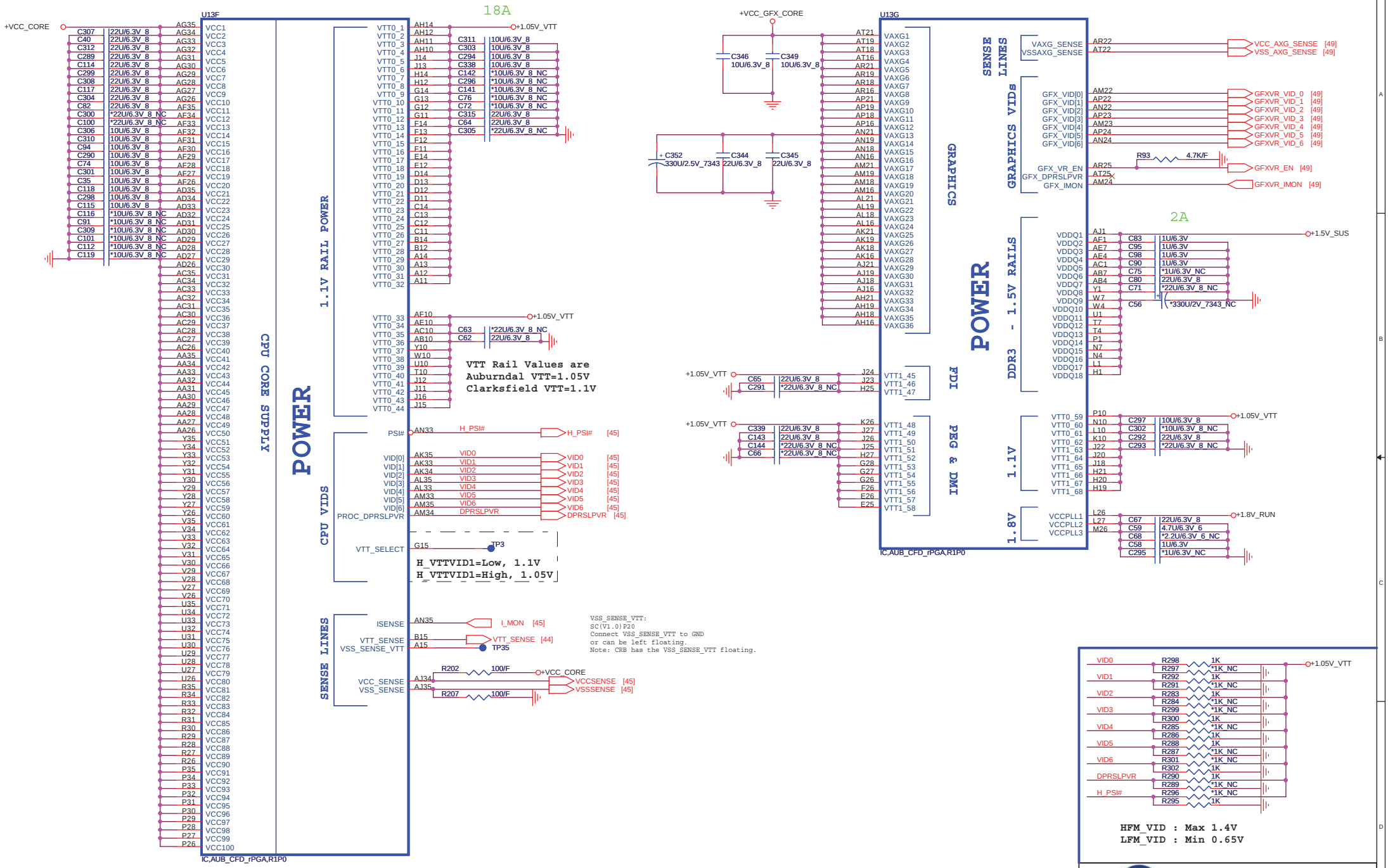
Please note that +VCC_GFX_CORE
should be 1.05V in Auburndale



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PROJECT : UM7 UMA

Size	Document Number	Rev
	PROCESSER 3/4(POWER)	1A

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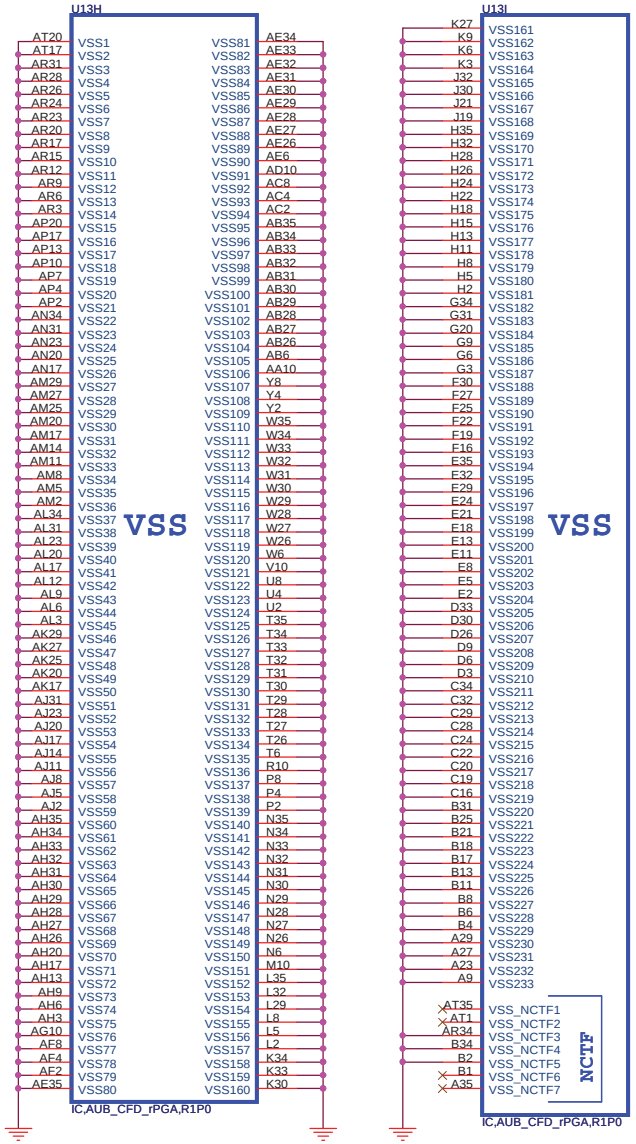
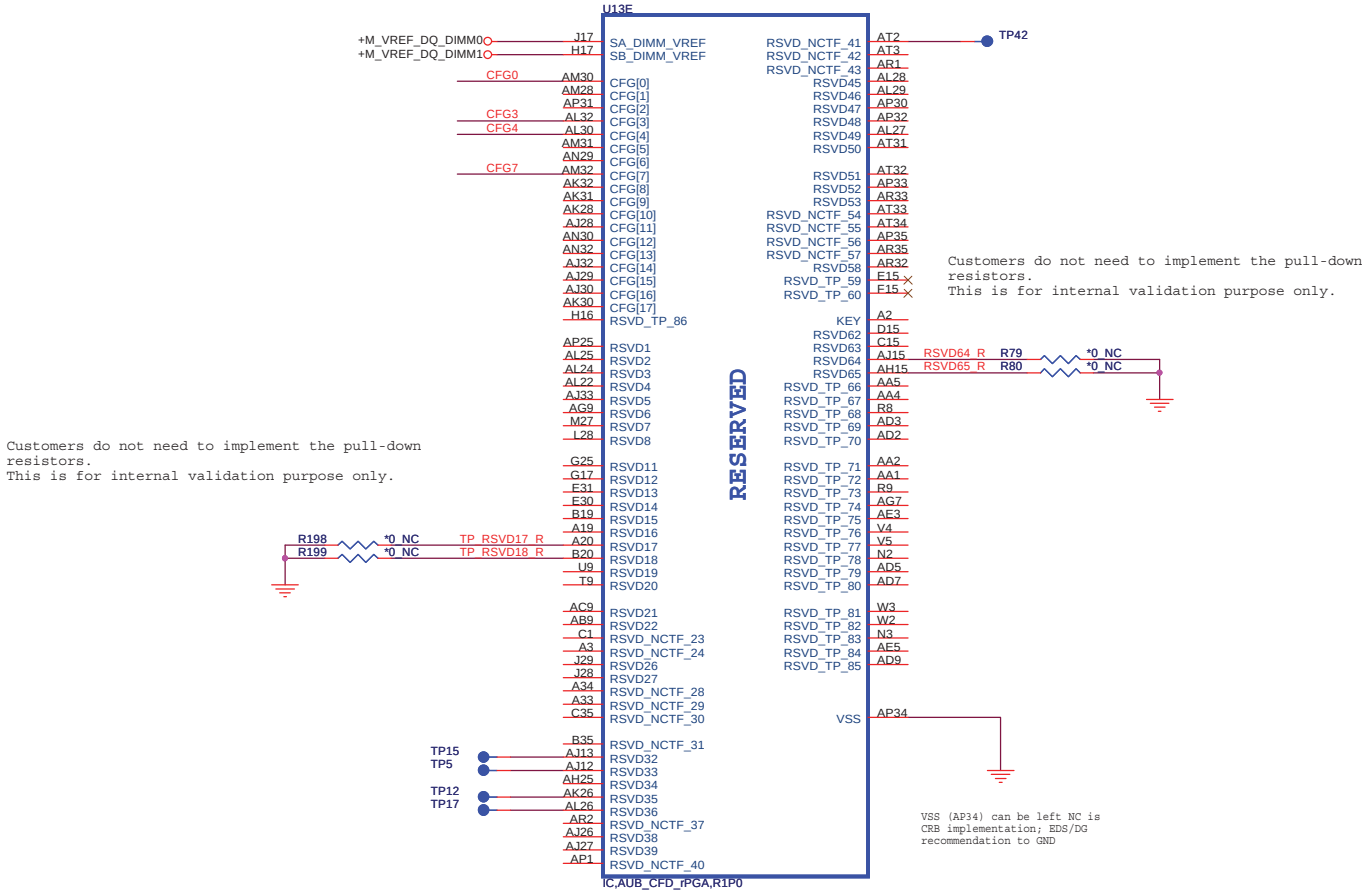
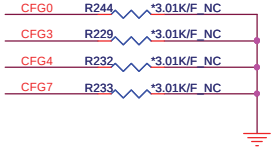
Arrandale PROCESSOR (GND)



Arrandale PROCESSOR(RESERVED, CFG)



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

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Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U17A

Ibex-M 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN

LPC: FWH0 / LAD0, FWH1 / LAD1, FWH2 / LAD2, FWH3 / LAD3, FWH4 / LFRAME#, LDRQ0#, (+3V) LDRQ1# / GPIO23, SERIRQ

IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN# / GPIO33 (+3V), HDA_DOCK_RST# / GPIO13 (+3V_S5)

JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#

SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

SATA: SATA0RXN, SATA0RXP, SATA0TXN, SATA0TXP, SATA1RXN, SATA1RXP, SATA1TXN, SATA1TXP, SATA2RXN, SATA2RXP, SATA2TXN, SATA2TXP, SATA3RXN, SATA3RXP, SATA3TXN, SATA3TXP, SATA4RXN, SATA4RXP, SATA4TXN, SATA4TXP, SATA5RXN, SATA5RXP, SATA5TXN, SATA5TXP, SATAICOMPO, SATAICOMPI, SATALED#, (+3V) SATA0GP / GPIO21, (+3V_S5) SATA1GP / GPIO19

HM57_MP

C348 18P/50V, Y3 32.768KHZ, R304 10M, C347 18P/50V

RTC_X1 B13, RTC_X2 D13

TP44 RTC_RST# C14, TP45 SRTC_RST# D17, SM_INTRUDER# A16

+RTC_CELL R309 330K_6 A14, TP46

ACZ_BITCLK A30, ACZ_SYNC D29, ACZ_SPKR P1, ACZ_RST# C30, ACZ_SDOUT B29

[26] ACZ_SPKR, [26] ACZ_SDIN0 G30, F30, E32, F32

[29] PCH_MELOCK H32, J30, R126 *1K/J_4_NC

TP37 PCH_JTAG_TCK_BUF M3, TP39 PCH_JTAG_TMS K3, TP40 PCH_JTAG_TDI K1, TP38 PCH_JTAG_TDO J2, TP41 PCH_JTAG_RST# J4

[30] SPI_CLK BA2, [30] SPI_CS0# AV3, TP43 AY3, [30] SPI_SI AY1, [30] SPI_SO AV1

SPI_SI

HDD: SATA_RXN0 [35], SATA_RXP0 [35], SATA_TXN0 [35], SATA_TXP0 [35]

SATA_TXN0_C C153 0.01U/16V, SATA_TXP0_C C152 0.01U/16V

ESATA: SATA_RXN4 [33], SATA_RXP4 [33], SATA_TXN4 [33], SATA_TXP4 [33]

SATA_TXN4_C C131 0.01U/16V, SATA_TXP4_C C130 0.01U/16V

SATA_COMP R112 37.4/F +1.05V_PCH

SATA_LED# [36]

10K R240 +3.3V_RUN

10K R73, 10K R242 +3.3V_RUN

LAD0 [29,32], LAD1 [29,32], LAD2 [29,32], LAD3 [29,32], LFRAME# [29,32], SERIRQ [29]

PANEL_BKEN R137 100K, ENVDD R136 100K

IBEX PEAK-M (LVDS,DDI)

U17D

Ibex-M 4 OF 10

Digital Display Interface

SDVO: SDVO_TVCLKINN BJ46, SDVO_TVCLKINP BG46, SDVO_STALLN BJ48, SDVO_STALLP BG48, SDVO_INTN BF45, SDVO_INTP BH45, SDVO_CTRLCLK T51, SDVO_CTRLDATA T53

HDMI_SCL [28], HDMI_SDA [28]

DISPLAY PORT B: DDPB_AUXN BG44, DDPB_AUXP BJ44, DDPB_HPD AU38, DDPB_0N BD42, DDPB_0P BC42, DDPB_1N BJ42, DDPB_1P BG42, DDPB_2N BB40, DDPB_2P BA40, DDPB_3N AW38, DDPB_3P BA38

R327 *1K_NC, R321 *1K_NC +1.05V_PCH, INT_HDMI_HPD [28]

INT_HDMI_TXDN0, INT_HDMI_TXDP0, INT_HDMI_TXDN1, INT_HDMI_TXDP1, INT_HDMI_TXDN2, INT_HDMI_TXDP2, INT_HDMI_TXCN, INT_HDMI_TXCP

DISPLAY PORT C: DDPC_CTRLCLK Y49, DDPC_CTRLDATA AB49, DDPC_AUXN BE44, DDPC_AUXP BD44, DDPC_HPD AV40, DDPC_0N BE40, DDPC_0P BD40, DDPC_1N BF41, DDPC_1P BH41, DDPC_2N BD38, DDPC_2P BC38, DDPC_3N BB36, DDPC_3P BA36

DISPLAY PORT D: DDPD_CTRLCLK U50, DDPD_CTRLDATA U52, DDPD_AUXN BC46, DDPD_AUXP BD46, DDPD_HPD AT38, DDPD_0N BJ40, DDPD_0P BG40, DDPD_1N BJ38, DDPD_1P BG38, DDPD_2N BF37, DDPD_2P BH37, DDPD_3N BE36, DDPD_3P BD36

VGA_BLU R349 150/F C647 22P, VGA_GRN R350 150/F C648 22P, VGA_RED R351 150/F C649 22P

Close BGA ball

LVDS--A: L_BKLTEN T48, L_VDD_EN T47, L_BKLTCTL Y48, L_DDC_CLK AB48, L_DDC_DATA Y45, L_CTRL_CLK AB46, L_CTRL_DATA V48, LVD_IBG AP39, LVD_VBG AP41, LVD_VREFH AT43, LVD_VREFL AT42

LVDSA_CLK# AV53, LVDSA_CLK AV51, LVDSA_DATA#0 BB47, LVDSA_DATA#1 BA52, LVDSA_DATA#2 AY48, LVDSA_DATA#3 AV47, LVDSA_DATA0 BB48, LVDSA_DATA1 BA50, LVDSA_DATA2 AY49, LVDSA_DATA3 AV48

LVDS--B: LVDSB_CLK# AP48, LVDSB_CLK AP47, LVDSB_DATA#0 AY53, LVDSB_DATA#1 AT49, LVDSB_DATA#2 AU52, LVDSB_DATA#3 AT53, LVDSB_DATA0 AY51, LVDSB_DATA1 AT48, LVDSB_DATA2 AU50, LVDSB_DATA3 AT51

CRT: CRT_BLUE AA52, CRT_GREEN AB53, CRT_RED AD53, CRT_DDC_CLK V51, CRT_DDC_DATA V53, CRT_HSYNC Y53, CRT_VSYNC Y51, DAC_IREF AD48, CRT_IRTN AB51

HM57_MP

[22,29] PANEL_BKEN, [22] ENVDD, [22] BIA_PWM, [22] LCD_DDCCLK, [22] LCD_DDCDAT, +3.3V_RUN R151 10K, R346 10K, R121 2.37K/F LVDS_VBG, T6 PAD

[22] LCD_ACLK-, [22] LCD_ACLK+, [22] LCD_A0-, [22] LCD_A1-, [22] LCD_A2-, T4 PAD

[22] LCD_A0+, [22] LCD_A1+, [22] LCD_A2+, T2 PAD

T20 PAD, T19 PAD

[23] VGA_BLU, [23] VGA_GRN, [23] VGA_RED, [23] DDCCLK, [23] DDCDATA

[23] VGAHSYNC R347 33, [23] VGAVSYNC R348 33

R152 1K/D different DIS

LCD_DDCCLK R150 2.2K, LCD_DDCDAT R149 2.2K, HDMI_SCL R345 2.2K, HDMI_SDA R344 2.2K

+3.3V_RUN

iTPM ENABLE/DISABLE

+3.3V_RUN R248 *1K_NC SPI_SI

TPM Function	
Enable	Mount
Disable	NC (Default)

R238 *51_NC PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

For AUDIO

[26,29] ACZ_RST#_AUDIO R318 33 ACZ_RST#

[26] ACZ_SDOUT_AUDIO R315 33 ACZ_SDOUT

[26] ACZ_SYNC_AUDIO R314 33 ACZ_SYNC

[26] ACZ_BITCLK_AUDIO R316 33 ACZ_BITCLK, C356 10P/50V

+3.3V_RUN R257 *1K/F_NC ACZ_SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot

RTC 1mA

+RTC_CELL

R305 20K/F RTC_RST# C350 1U/6.3V

R308 20K/F SRTC_RST# C353 1U/6.3V

R307 1M SM_INTRUDER#

Res. of TDI near PCH

+3.3V_SUS

R237 *200_NC, R236 *200_NC, R235 *200_NC, R219 *20K_NC

PCH_JTAG_TMS, PCH_JTAG_TDI, PCH_JTAG_TDO, PCH_JTAG_RST#

R255 *100_NC, R254 *100_NC, R253 *100_NC, R228 *10K_NC

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

For UMA HDMI Function

INT_HDMI_TXDN0 C334 0.1U/16V, INT_HDMI_TXDP0 C337 0.1U/16V — INT_HDMI_TXDN2_C [28], INT_HDMI_TXDP2_C [28]

INT_HDMI_TXDN1 C329 0.1U/16V, INT_HDMI_TXDP1 C331 0.1U/16V — INT_HDMI_TXDN1_C [28], INT_HDMI_TXDP1_C [28]

INT_HDMI_TXDN2 C324 0.1U/16V, INT_HDMI_TXDP2 C327 0.1U/16V — INT_HDMI_TXDN0_C [28], INT_HDMI_TXDP0_C [28]

INT_HDMI_TXCN C320 0.1U/16V, INT_HDMI_TXCP C323 0.1U/16V — INT_HDMI_TXCN_C [28], INT_HDMI_TXCP_C [28]

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Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1A

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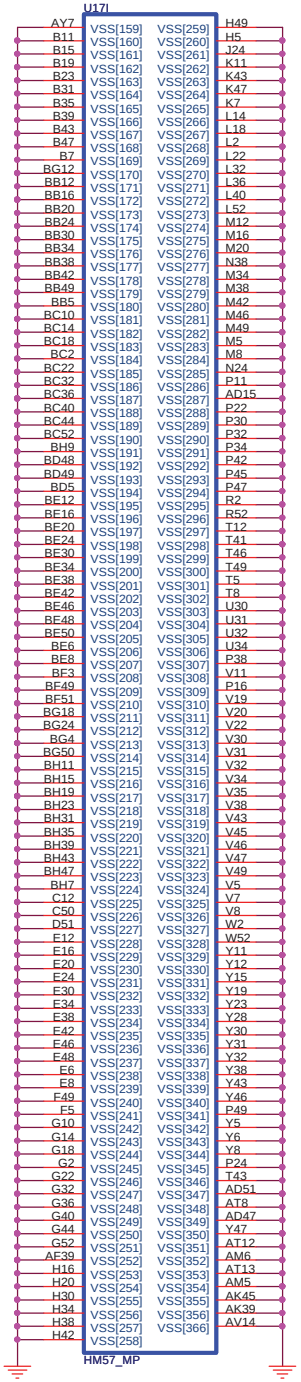
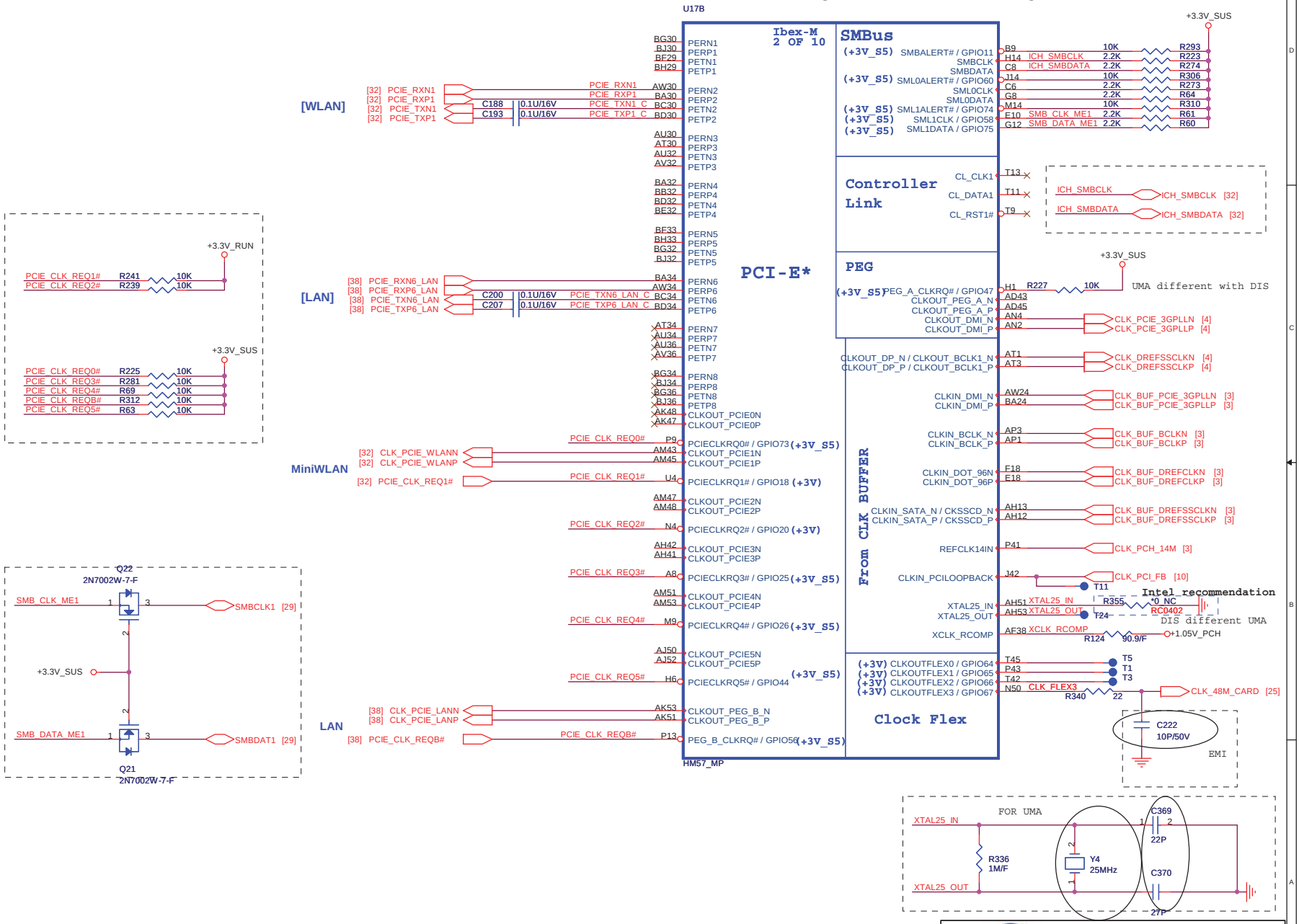
IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)



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Size	Document Number	Rev
	PCH 2/5 (PCIE, SMBUS, CK)	1A

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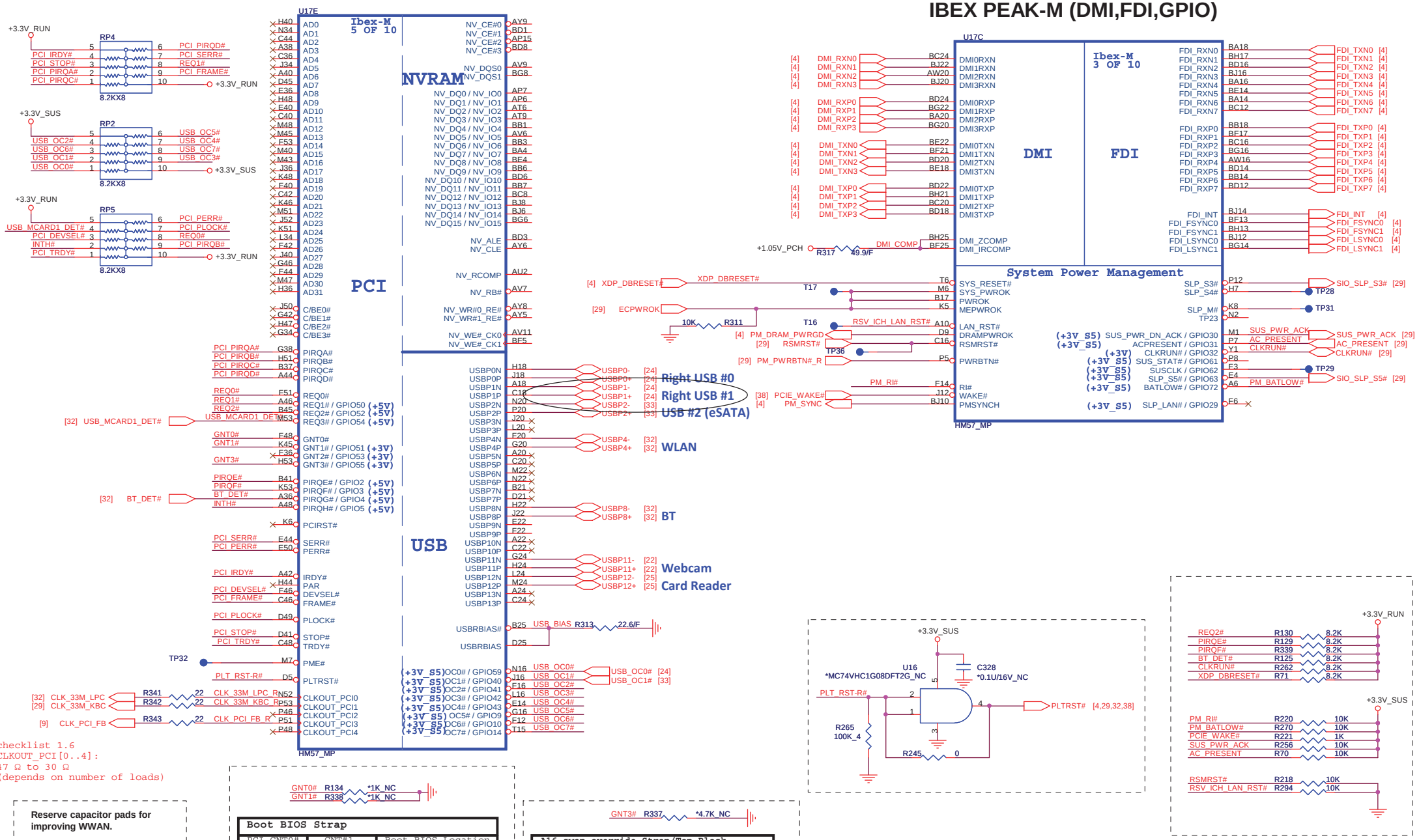
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)



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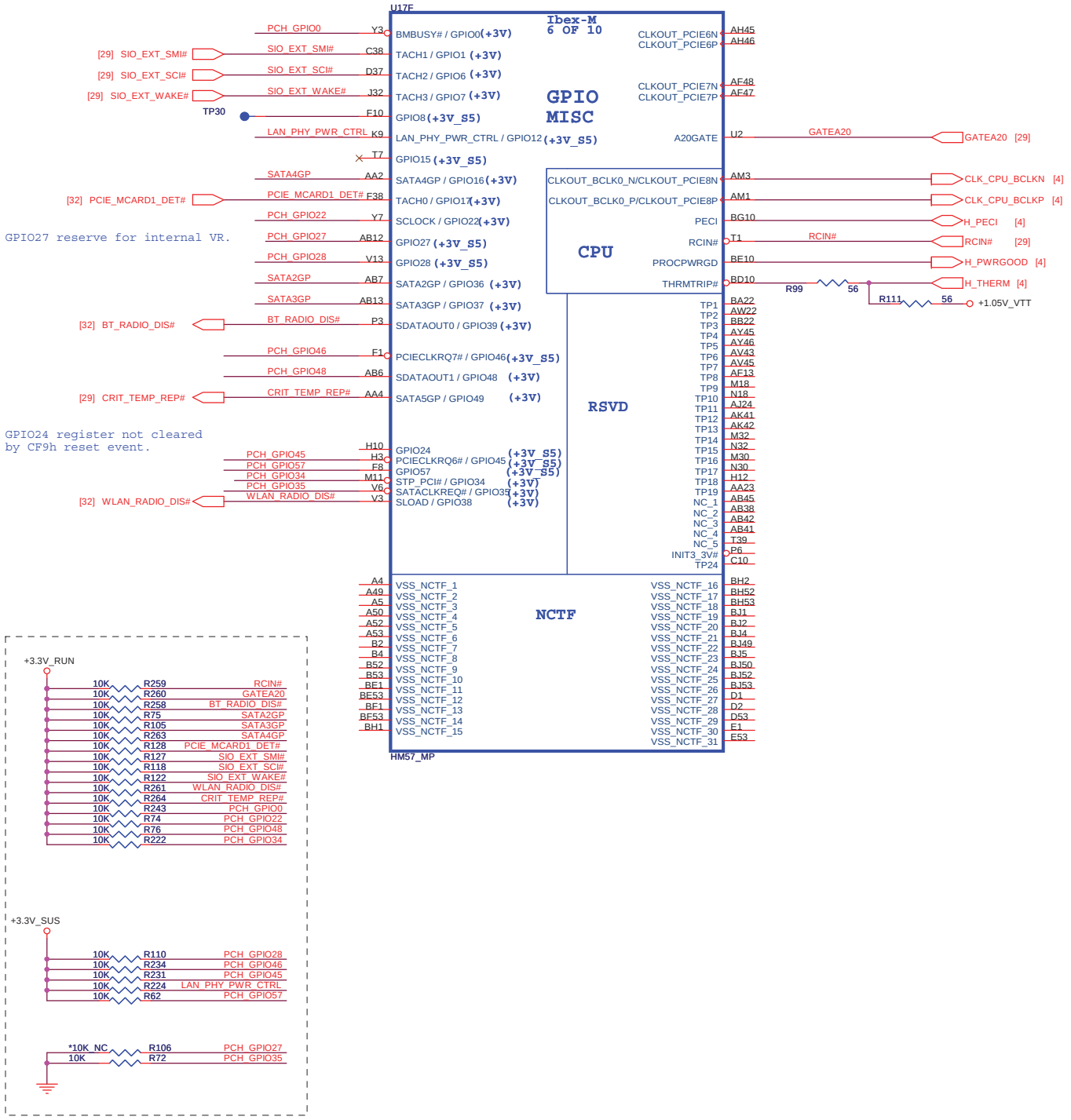
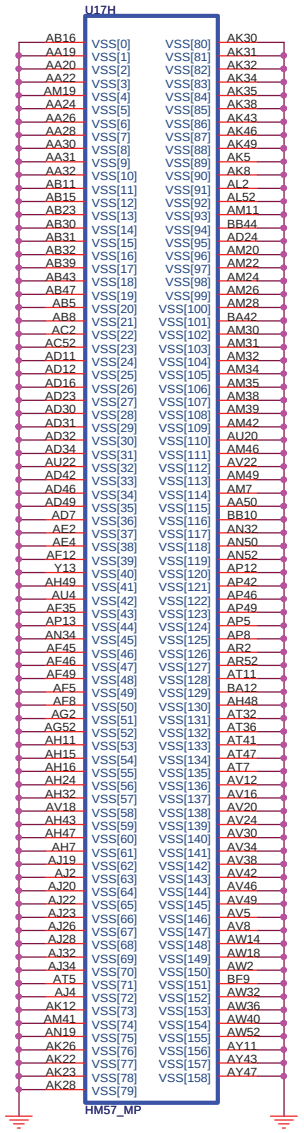
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



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Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	1A

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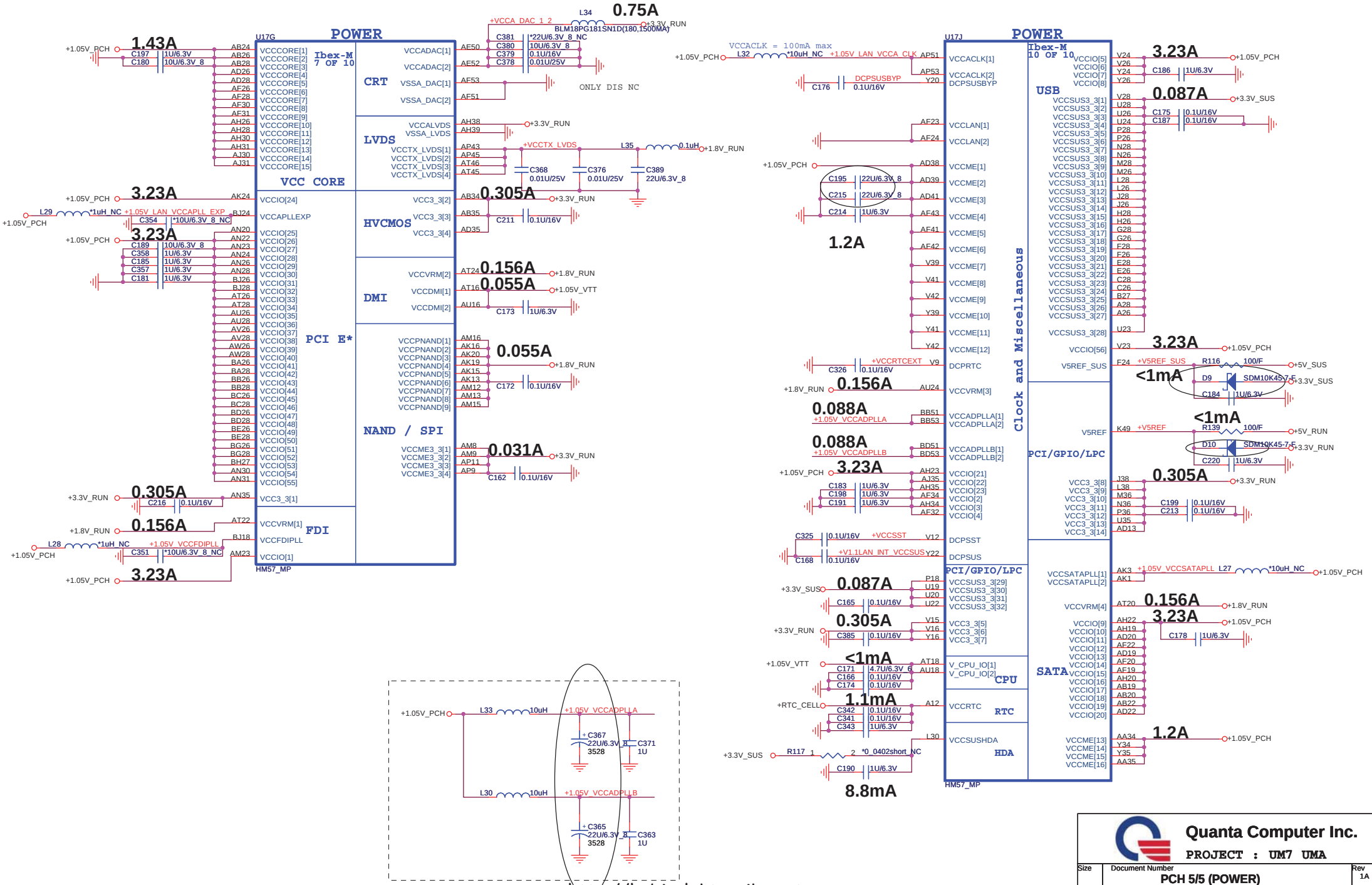
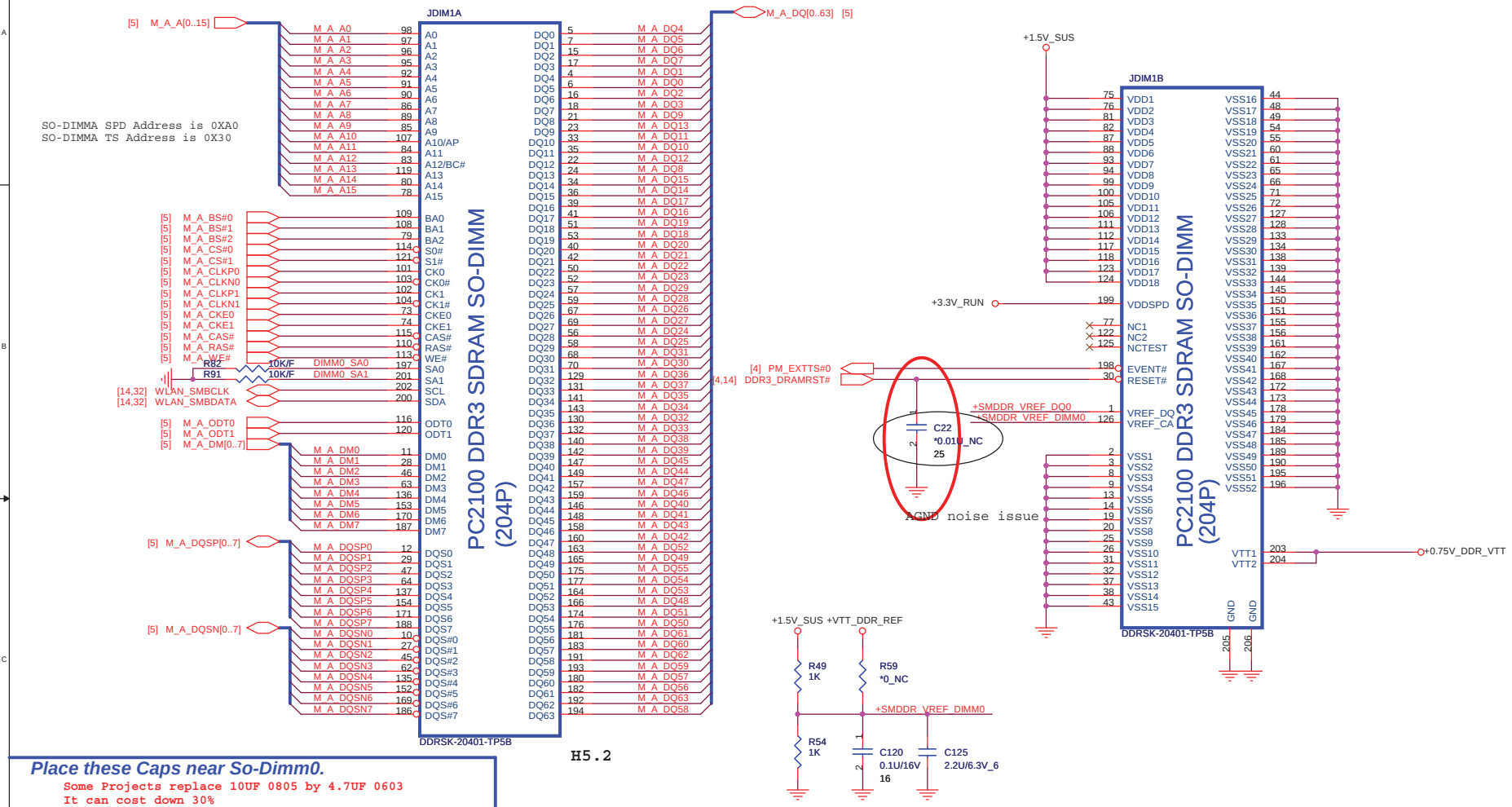

POWER
U17G
Ibex-M 7 OF 10
VCC CORE
PCI E*
FDI
CRT
LVDS
HVCMOS
DMI
NAND / SPI
HM57_MP
1.43A
3.23A
0.305A
0.156A
0.75A
0.305A
0.156A
0.055A
0.031A
ONLY DIS NC
POWER
U17J
Ibex-M 10 OF 10
Clock and Miscellaneous
PCI/GPIO/LPC
CPU
RTC
HDA
USB
SATA
VCCACLK = 100mA max
3.23A
0.087A
3.23A
<1mA
<1mA
0.305A
3.23A
1.2A
0.156A
0.088A
0.088A
3.23A
0.087A
0.305A
<1mA
1.1mA
8.8mA
HM57_MP
L33 10uH +1.05V_VCCADPLLA
C367 22U/6.3V_8 3528
C371 1U
L30 10uH +1.05V_VCCADPLLB
C365 22U/6.3V_8 3528
C363 1U
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : UM7 UMA
Size
Document Number
PCH 5/5 (POWER)
Rev 1A
Date: Friday, January 08, 2010
Sheet 12 of 52



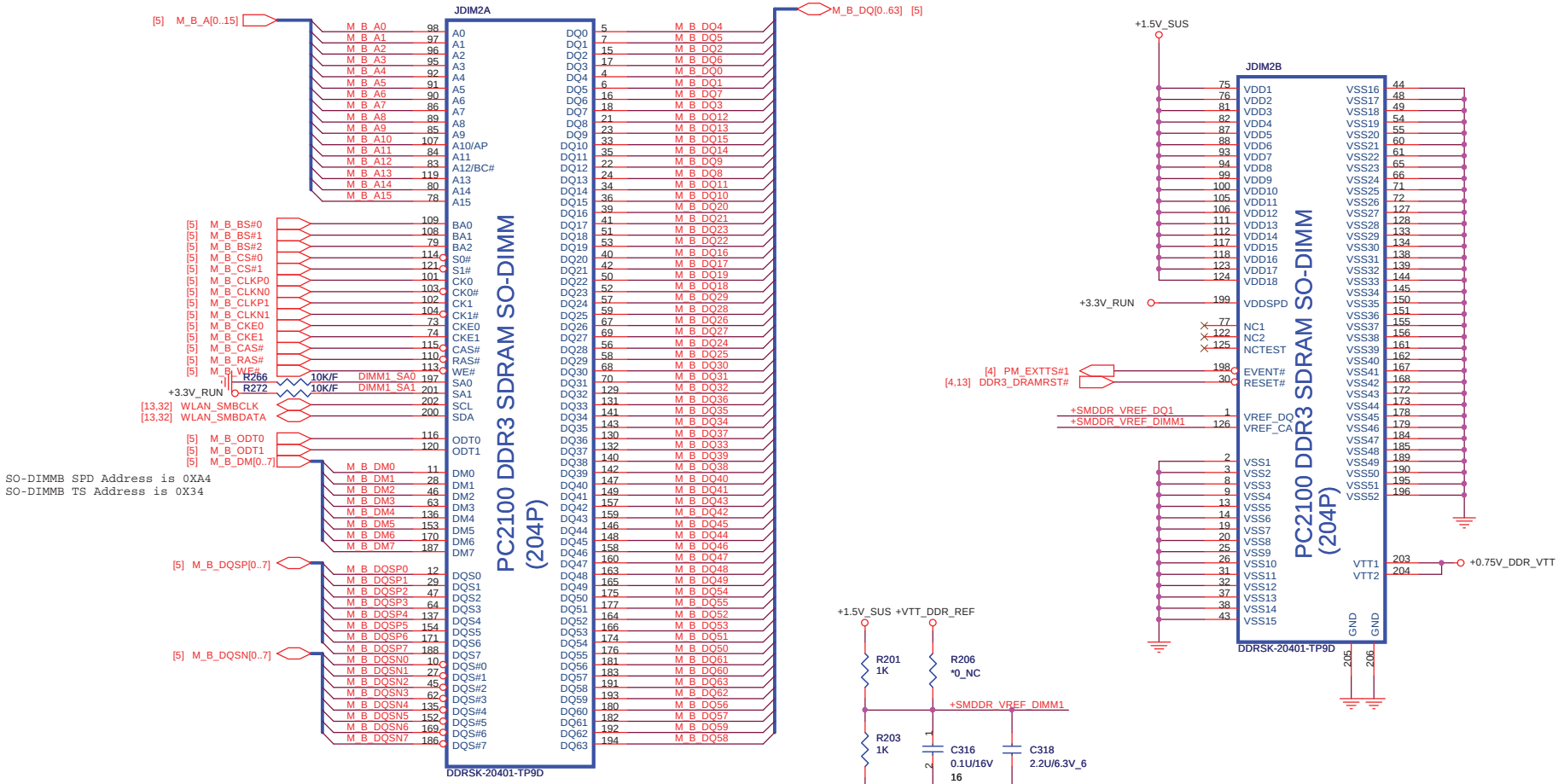
Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	DDR3 DIMM-0	1A

Date: Tuesday, January 19, 2010 Sheet 13 of 52

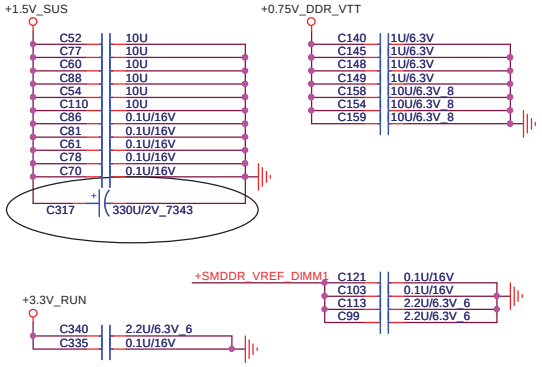
http://hobi-elektronika.net

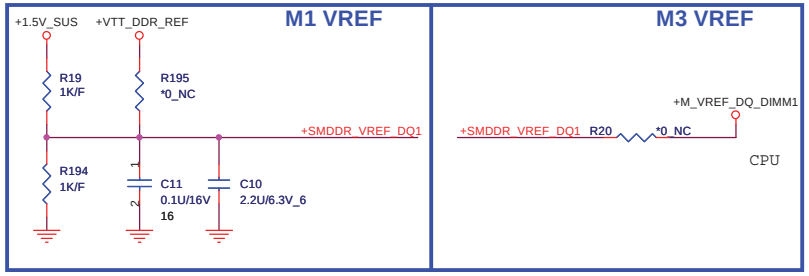


H9.2

Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





http://hobi-elektronika.net

Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: DDR3 DIMM-1	Rev 1A
Date: Tuesday, January 19, 2010	Sheet 14 of 52	

BLANK PAGE FOR PAGE NUMBER SAME AS DISCRETE

Quanta Computer Inc.			
PROJECT : UM7 UMA			
Size	Document Number Blank		Rev 1A
Date: Thursday, November 19, 2009		Sheet 15 of 52	

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Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	Blank	1A

Date: Thursday, November 19, 2009 Sheet 16 of 52

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Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	Blank	1A

Date: Thursday, November 19, 2009 Sheet 17 of 52

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Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	Blank	1A

Date: Thursday, November 19, 2009 Sheet 18 of 52

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Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	Blank	1A

Date: Thursday, November 19, 2009 Sheet 19 of 52

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Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	Blank	1A

Date: Thursday, November 19, 2009 Sheet 20 of 52

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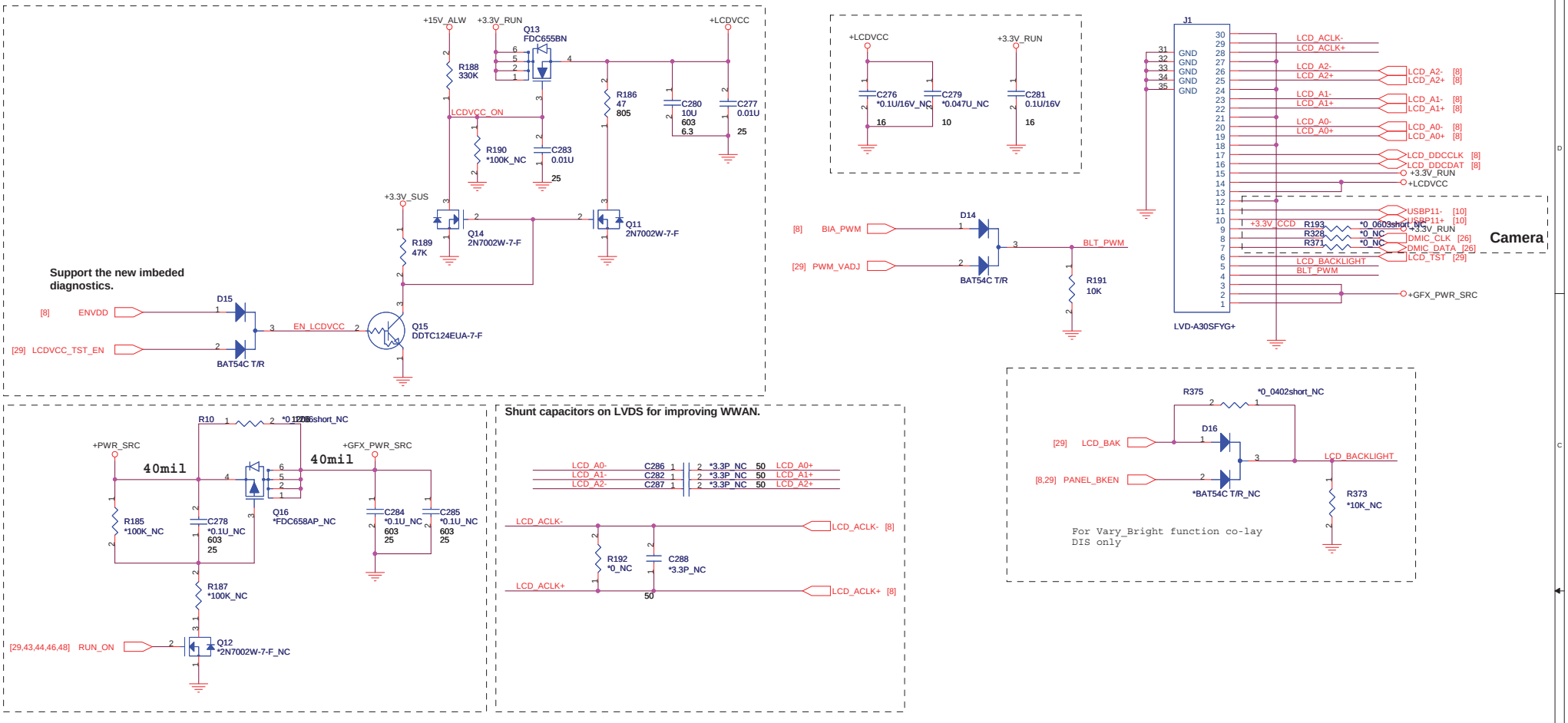
Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	Blank	1A

Date: Thursday, November 19, 2009 Sheet 21 of 52

http://hobi-elektronika.net



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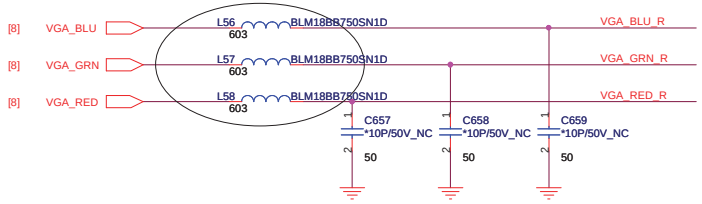
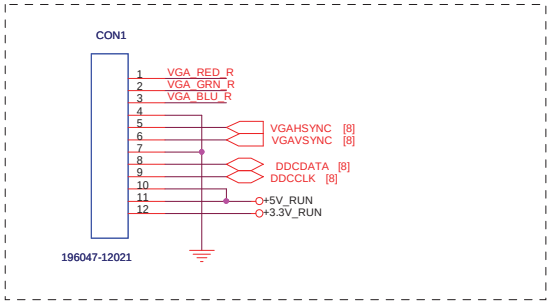
Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	LCD CONN / HDMI CONN	1A

Date: Tuesday, February 02, 2010 Sheet 22 of 52





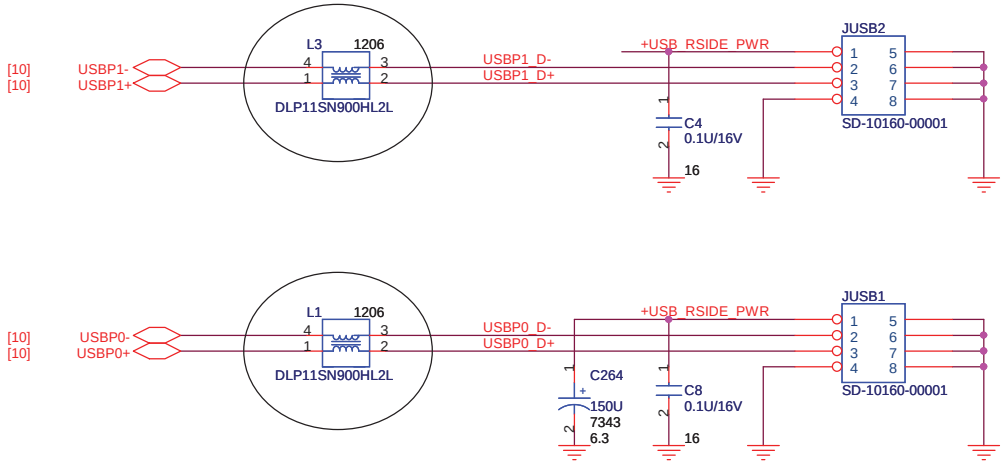
Quanta Computer Inc.

PROJECT : UM7 UMA

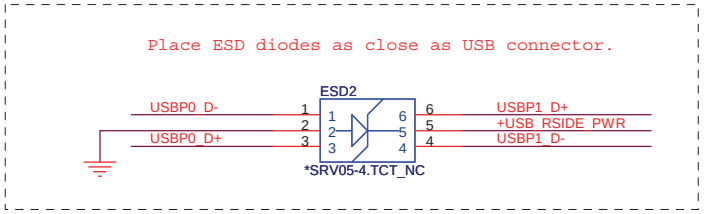
Size	Document Number	Rev
	CRT CONN	1A

Date: Tuesday, January 19, 2010 Sheet 23 of 52

http://hobi-elektronika.net

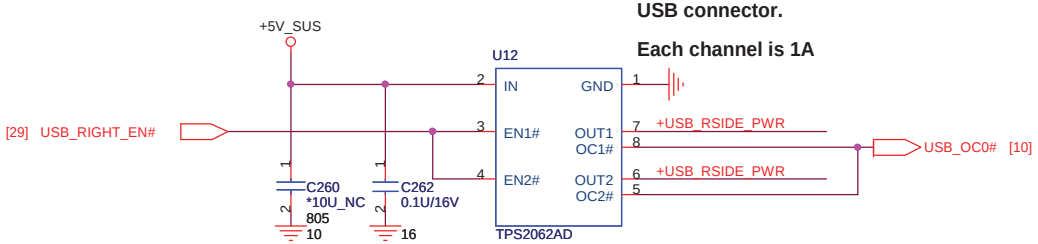


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



Place one 150uF cap by each USB connector.

Each channel is 1A



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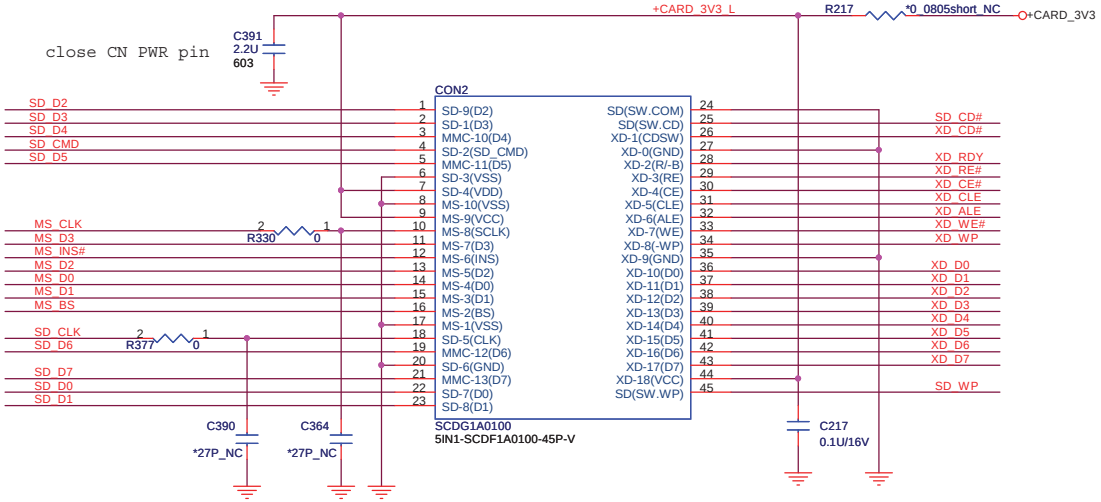
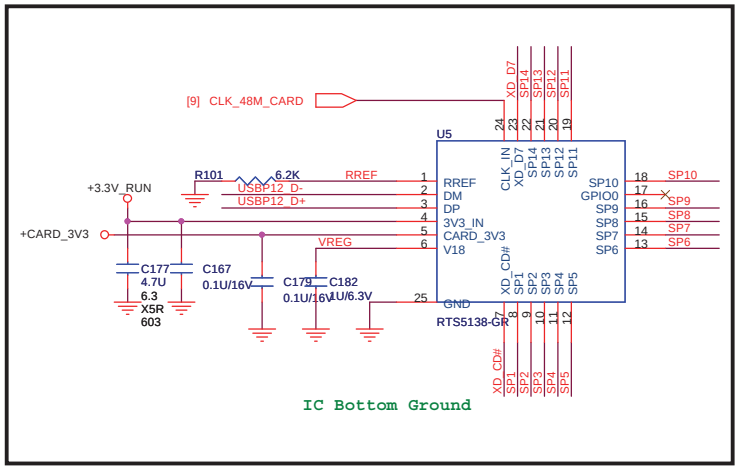
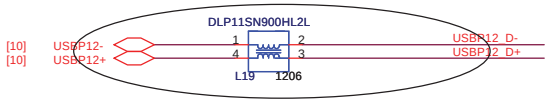
Quanta Computer Inc.		
PROJECT : UM7 UMA		
Size	Document Number: **Right USB**	Rev 1A
Date: Tuesday, February 02, 2010	Sheet 24 of 52	





RTS5138-QFN24



SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

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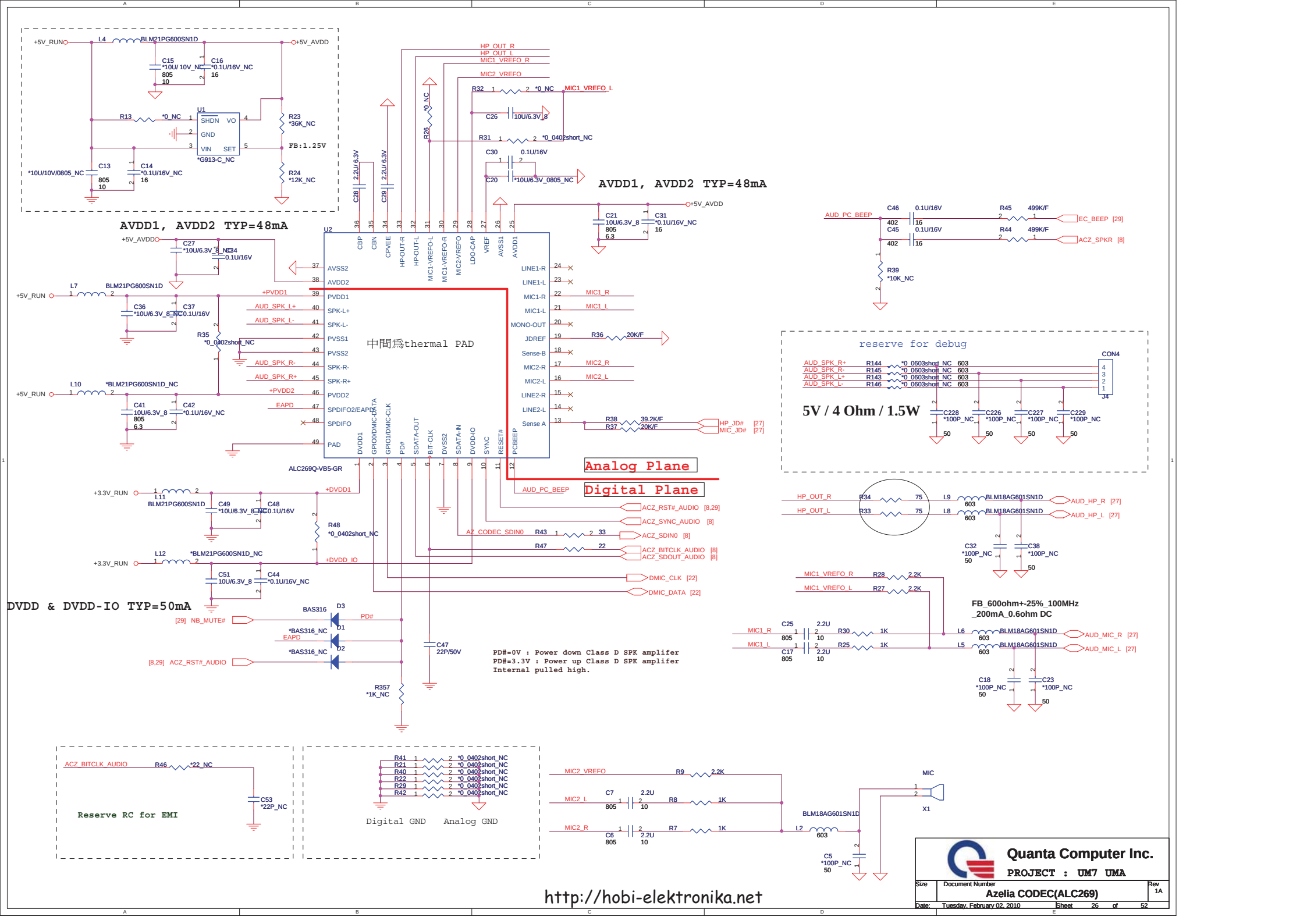
Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	Card Reader(RST5138)	1A

Date: Tuesday, February 02, 2010 Sheet 25 of 52


AVDD1, AVDD2 TYP=48mA
AVDD1, AVDD2 TYP=48mA
DVDD & DVDD-IO TYP=50mA
ALC269Q-VB5-GR
中間爲thermal PAD
Analog Plane
Digital Plane
5V / 4 Ohm / 1.5W
reserve for debug
FB_600ohm+-25%_100MHz
_200mA_0.6ohm DC
PD#=0V : Power down Class D SPK amplifer
PD#=3.3V : Power up Class D SPK amplifer
Internal pulled high.
Reserve RC for EMI
Digital GND
Analog GND
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : UM7 UMA
Azelia CODEC(ALC269)
Size
Document Number
Rev
1A
Date: Tuesday, February 02, 2010
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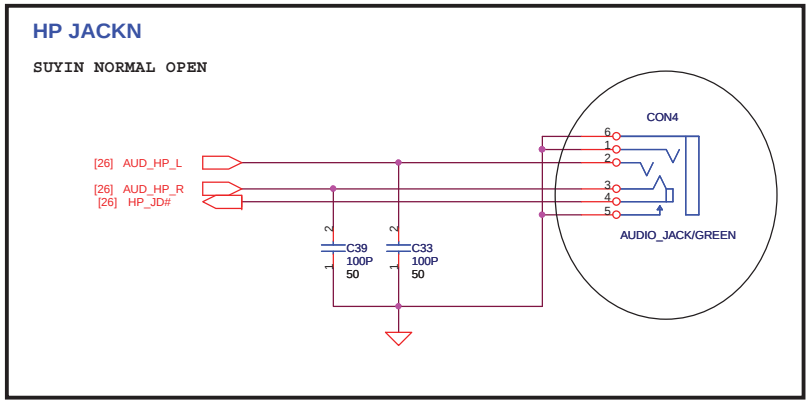

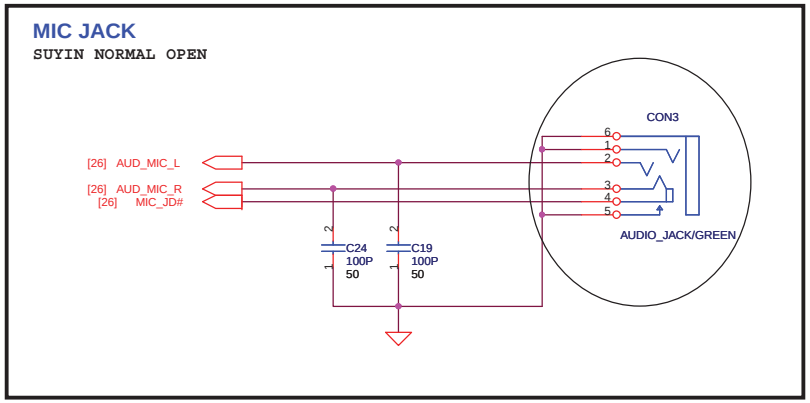

Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	AUDIO CONN	1A

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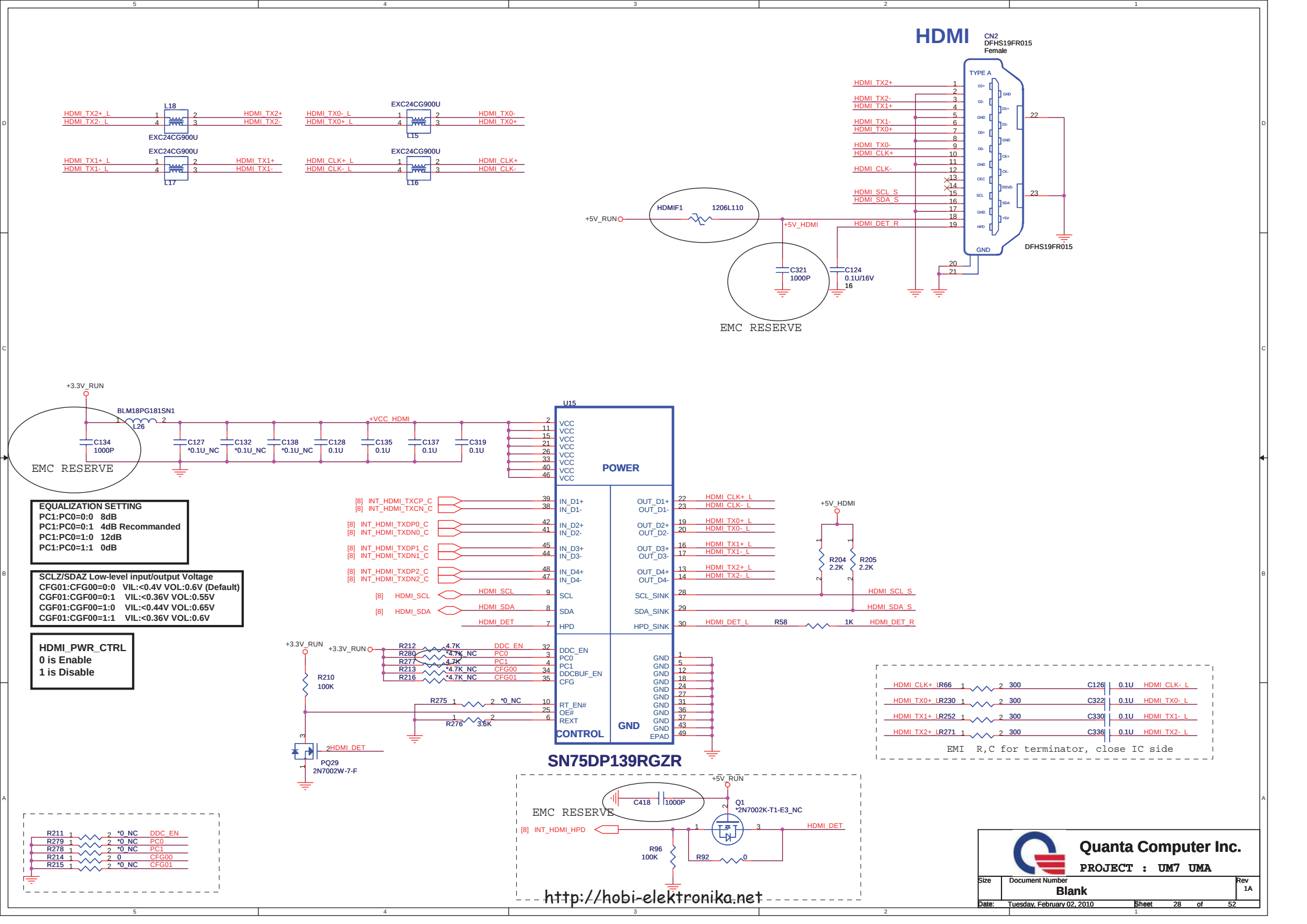
HDMI
CN2
DFHS19FR015
Female
TYPE A
DFHS19FR015
HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_CLK+
HDMI_CLK-
HDMI_SCL_S
HDMI_SDA_S
HDMI_DET_R
+5V_RUN
HDMIF1
1206L110
+5V_HDMI
C321
1000P
C124
0.1U/16V
16
EMC RESERVE
L18
EXC24CG900U
L17
L15
L16
HDMI_TX2+_L
HDMI_TX2-_L
HDMI_TX0-_L
HDMI_TX0+_L
HDMI_TX1+_L
HDMI_TX1-_L
HDMI_CLK+_L
HDMI_CLK-_L
+3.3V_RUN
BLM18PG181SN1
L26
C134
1000P
C127
*0.1U_NC
C132
*0.1U_NC
C138
*0.1U_NC
C128
0.1U
C135
0.1U
C137
0.1U
C319
0.1U
+VCC_HDMI
U15
POWER
VCC
IN_D1+
IN_D1-
IN_D2+
IN_D2-
IN_D3+
IN_D3-
IN_D4+
IN_D4-
SCL
SDA
HPD
OUT_D1+
OUT_D1-
OUT_D2+
OUT_D2-
OUT_D3+
OUT_D3-
OUT_D4+
OUT_D4-
SCL_SINK
SDA_SINK
HPD_SINK
DDC_EN
PC0
PC1
DDCBUF_EN
CFG
RT_EN#
OE#
REXT
CONTROL
GND
EPAD
SN75DP139RGZR
[8] INT_HDMI_TXCP_C
[8] INT_HDMI_TXCN_C
[8] INT_HDMI_TXDP0_C
[8] INT_HDMI_TXDN0_C
[8] INT_HDMI_TXDP1_C
[8] INT_HDMI_TXDN1_C
[8] INT_HDMI_TXDP2_C
[8] INT_HDMI_TXDN2_C
[8] HDMI_SCL
[8] HDMI_SDA
HDMI_DET
HDMI_CLK+_L
HDMI_CLK-_L
HDMI_TX0+_L
HDMI_TX0-_L
HDMI_TX1+_L
HDMI_TX1-_L
HDMI_TX2+_L
HDMI_TX2-_L
R204
2.2K
R205
2.2K
R58
1K
R212
4.7K
R280
*4.7K_NC
R277
4.7K
R213
*4.7K_NC
R216
*4.7K_NC
DDC_EN
PC0
PC1
CFG00
CFG01
R210
100K
R275
*0_NC
R276
3.6K
PQ29
2N7002W-7-F
R66
300
R230
300
R252
300
R271
300
C126
0.1U
C322
0.1U
C330
0.1U
C336
0.1U
EMI R,C for terminator, close IC side
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB
SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V
HDMI_PWR_CTRL
0 is Enable
1 is Disable
R211
R279
R278
R214
R215
*0_NC
0
C418
1000P
Q1
*2N7002K-T1-E3_NC
[8] INT_HDMI_HPD
R96
100K
R92
0
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : UM7 UMA
Size
Document Number
Blank
Rev
1A
Date: Tuesday, February 02, 2010
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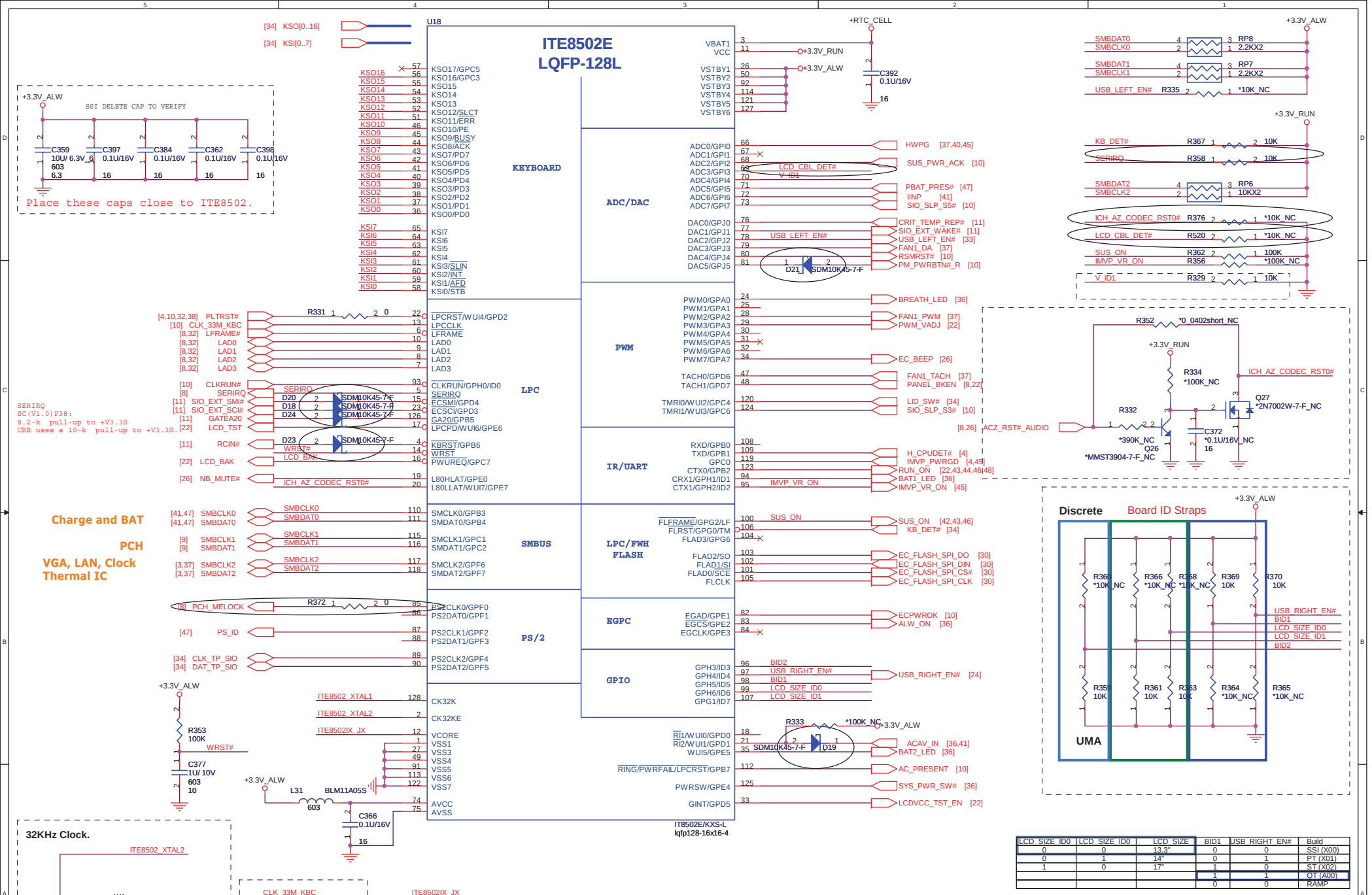

LCD_SIZE_ID0	LCD_SIZE_ID0	LCD_SIZE	BID1	USB_RIGHT_EN#	Build
0	0	13.3"	0	0	SSI (X00)
0	1	14"	0	1	PT (X01)
1	0	17"	1	0	ST (X02)
			1	1	QT (A00)
			0	0	RAMP

Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	SIO ITE8502	1A

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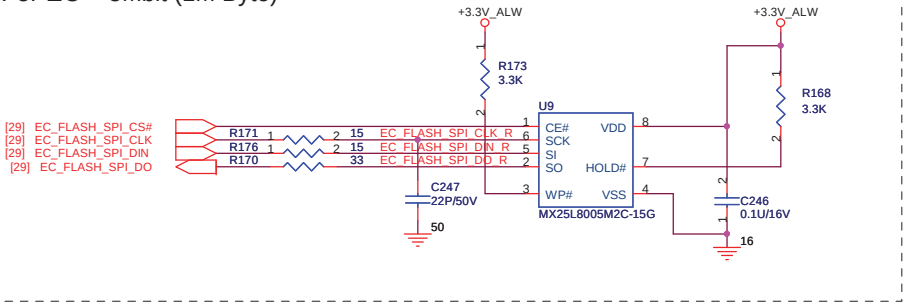
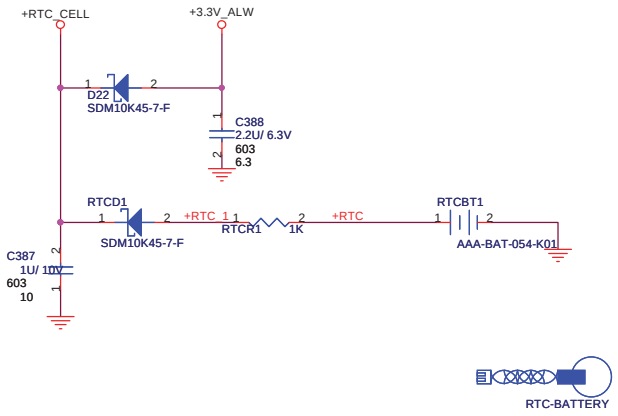
For EC 8Mbit (1M Byte)



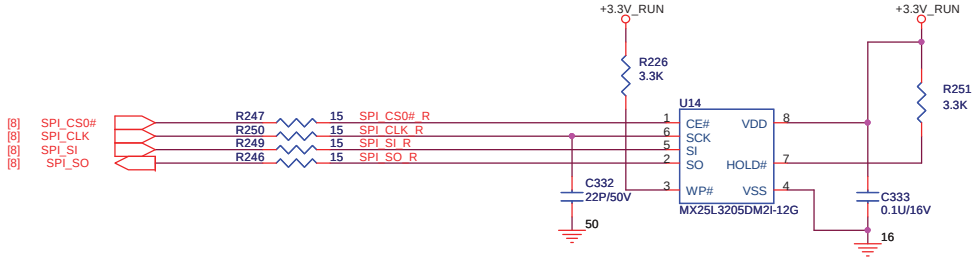
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



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Quanta Computer Inc.			
PROJECT : UM7 UMA			
Size	Document Number		Rev
	FLASH/RTC		1A
Date: Tuesday, February 02, 2010	Sheet 30 of 52		

Quanta Computer Inc.

PROJECT : UM7 UMA

Size	Document Number	Rev
	MINI-Card WWAN	1A

Date: Thursday, November 19, 2009 Sheet 31 of 52

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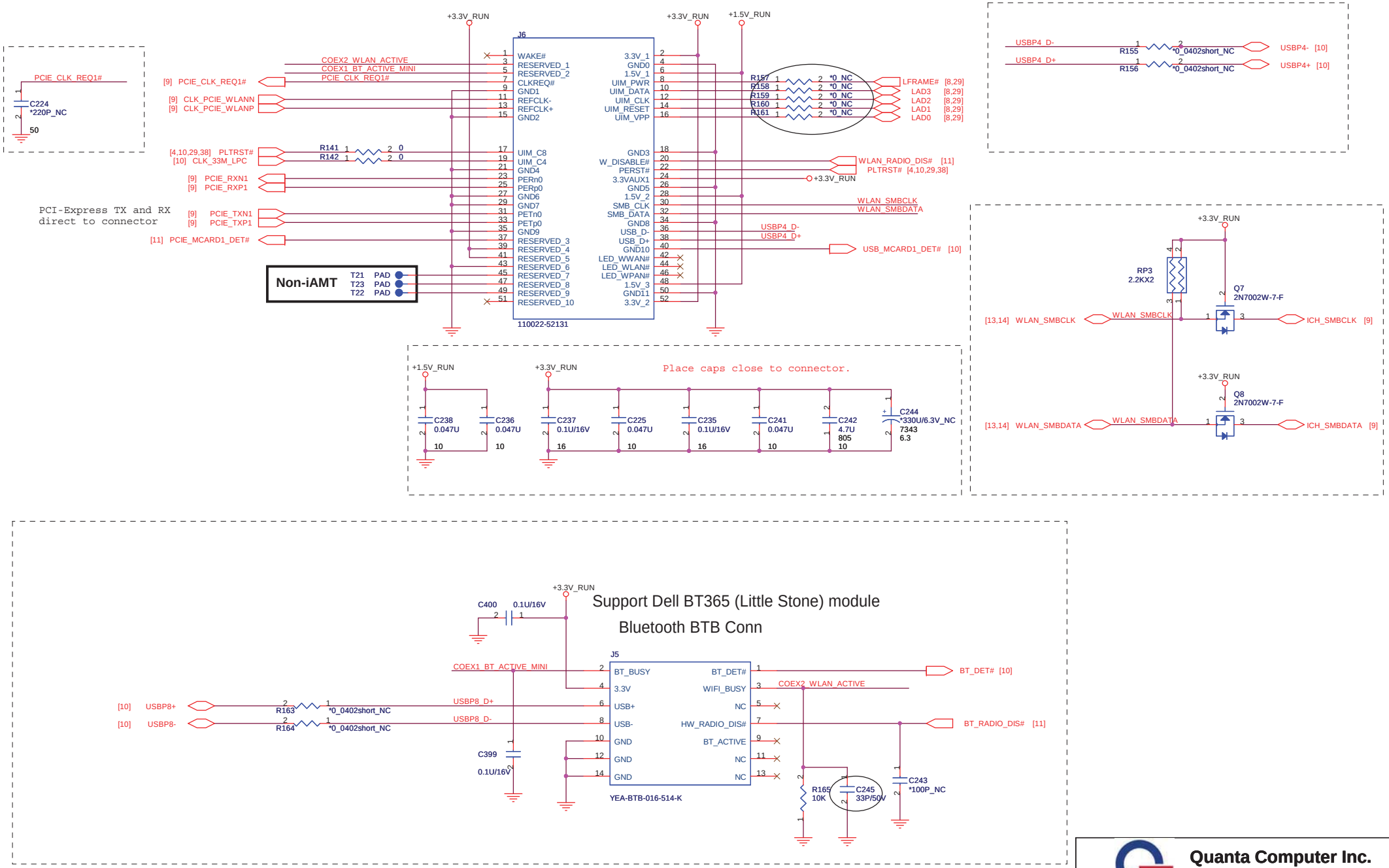
MiniCard WLAN connector



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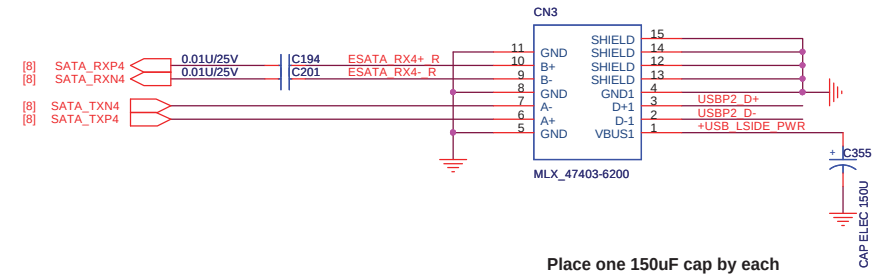
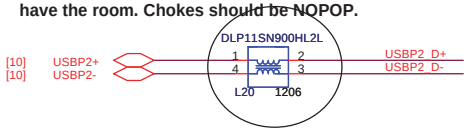
Quanta Computer Inc.		
PROJECT : UM7 UMA		
Size	Document Number: MINI-Card WLAN / BT	Rev 1A
Date: Tuesday, February 02, 2010	Sheet 32 of 52	

USB and eSATA Conn.

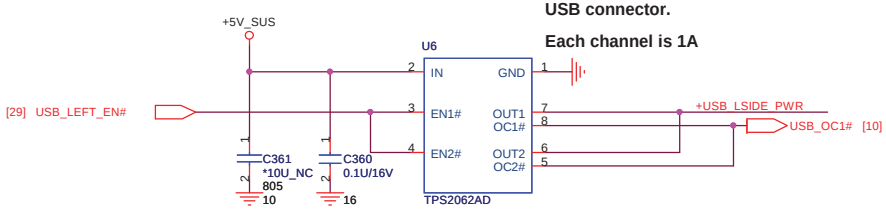


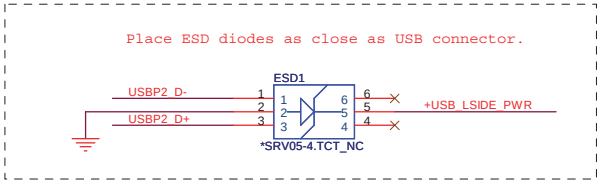
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



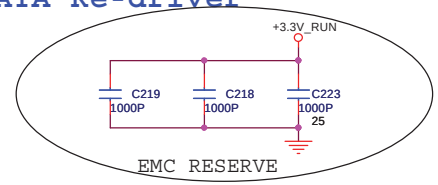
Place one 150uF cap by each USB connector.

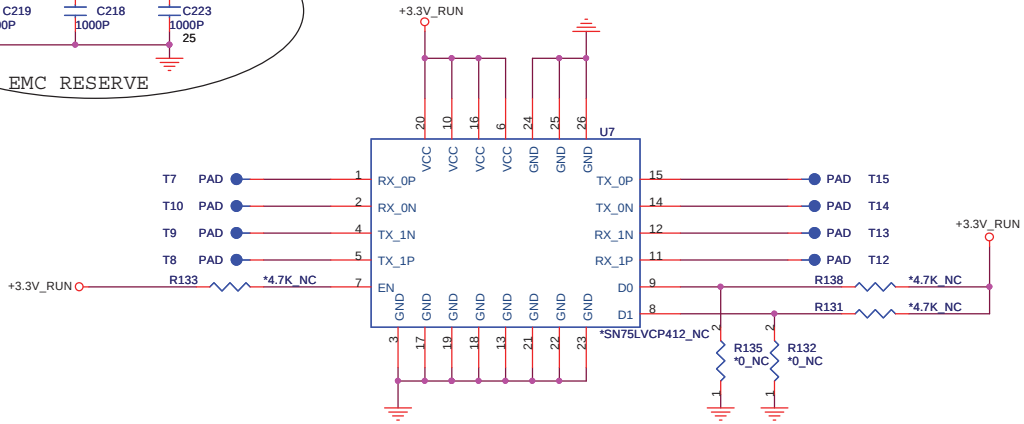
Each channel is 1A





E-SATA Re-driver





Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

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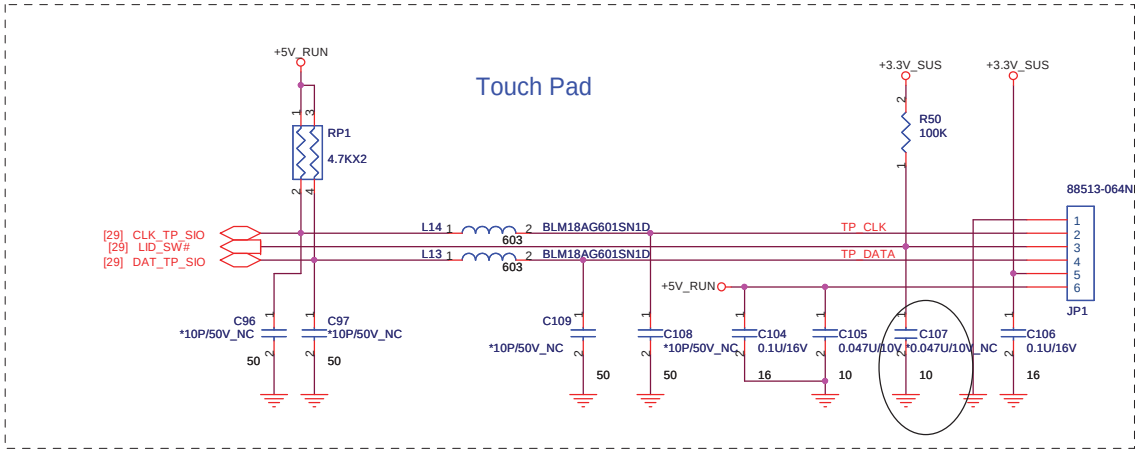
Quanta Computer Inc.

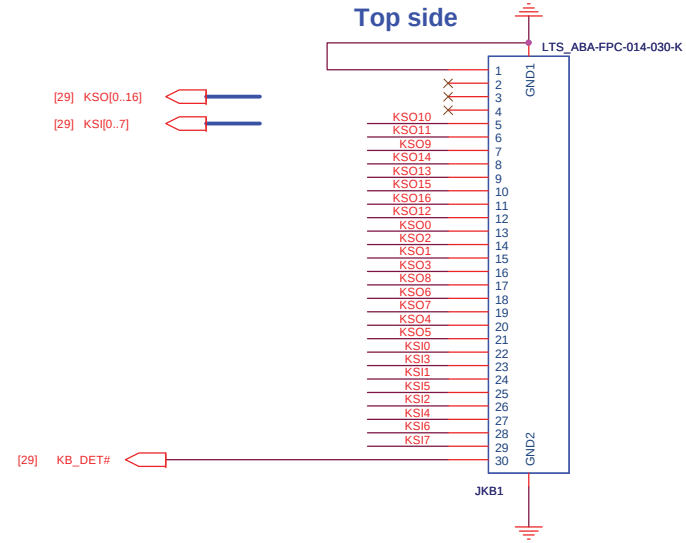
PROJECT : UM7 UMA

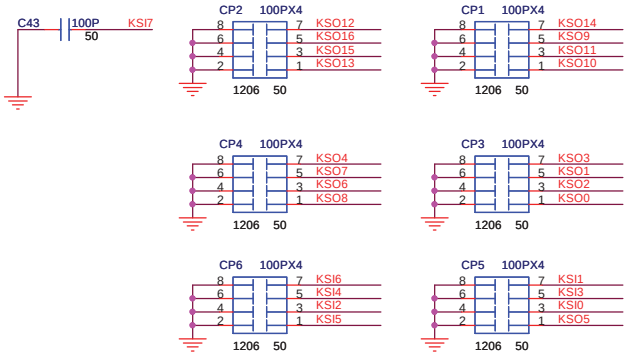
Size	Document Number	Rev
	eSATA & Right USB	1A

Date: Tuesday, February 02, 2010 Sheet 33 of 52



KEYBOARD CONNECTOR





100P CAPS CLOSE TO JKB1

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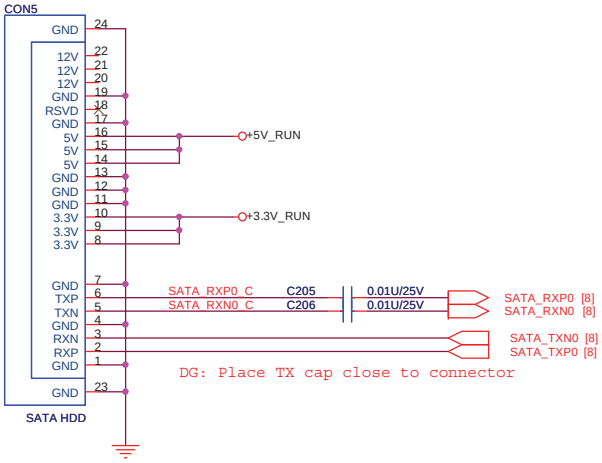
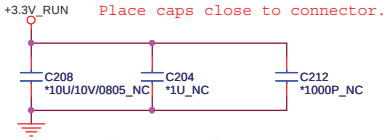
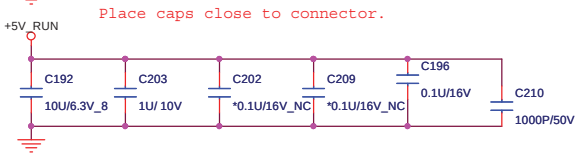
SATA Connector.







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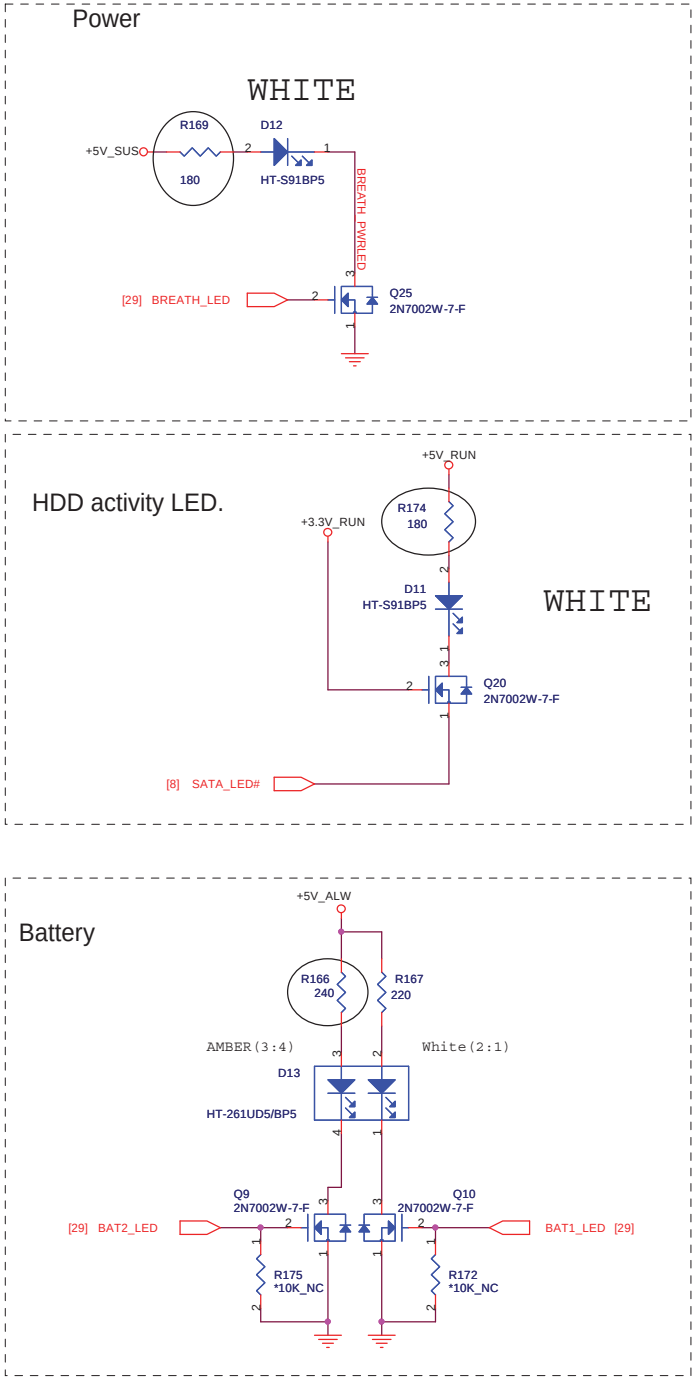
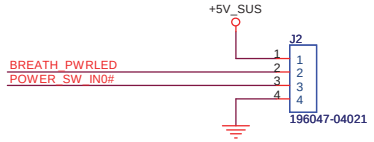
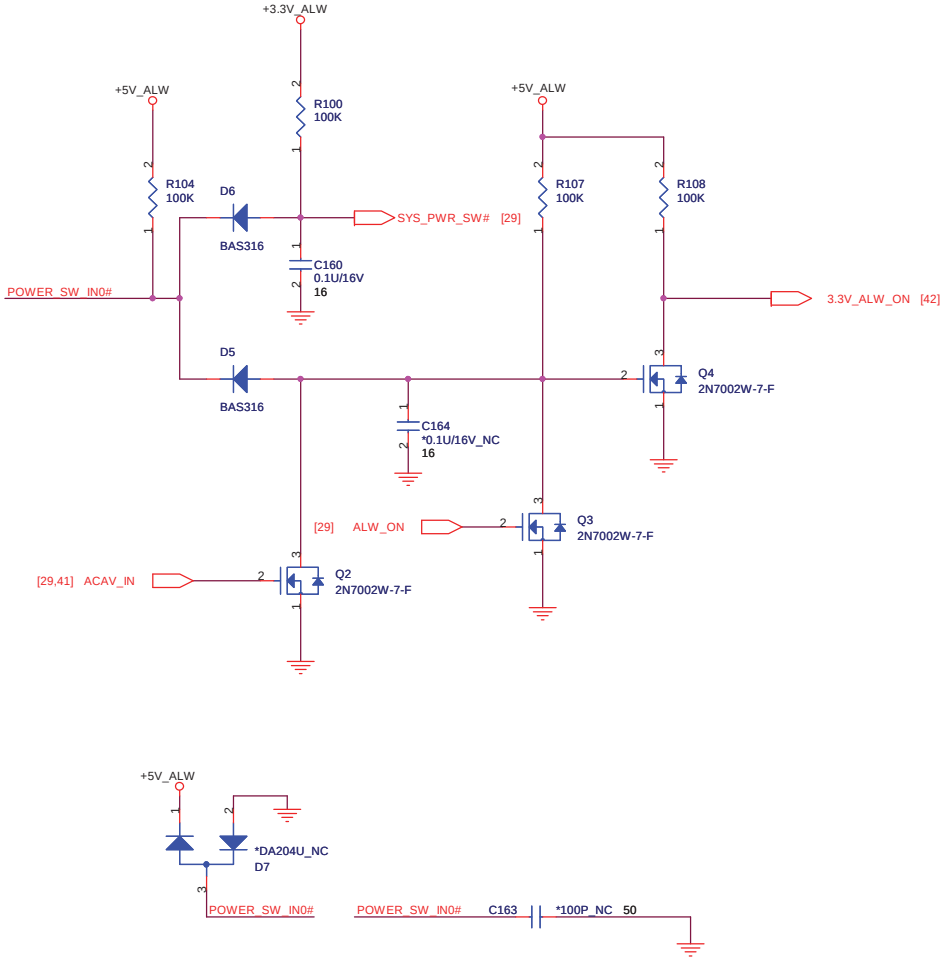


Power button Cable



3VALW ON POWER LOGIC



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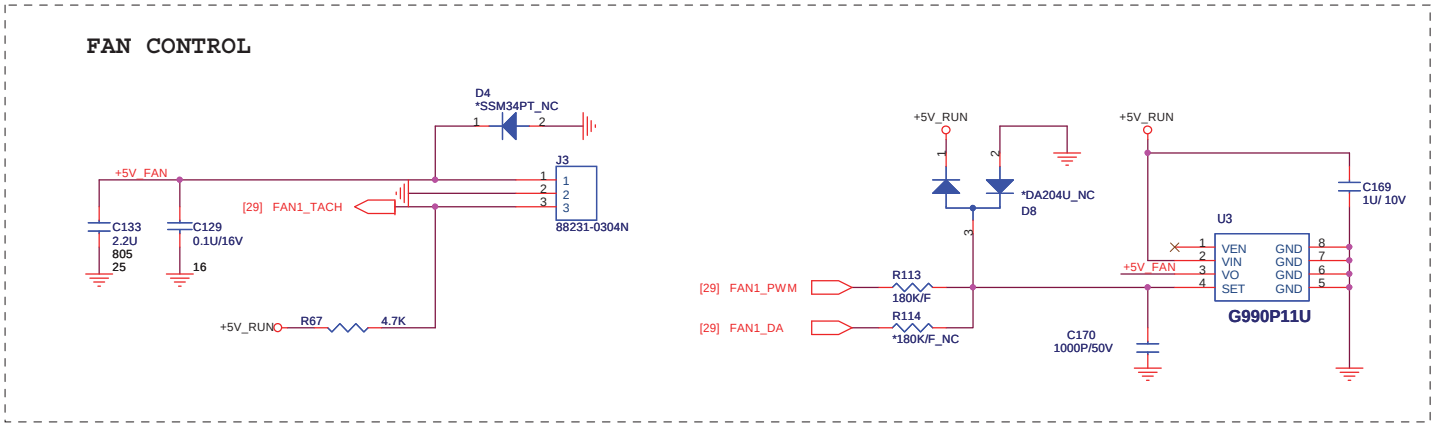

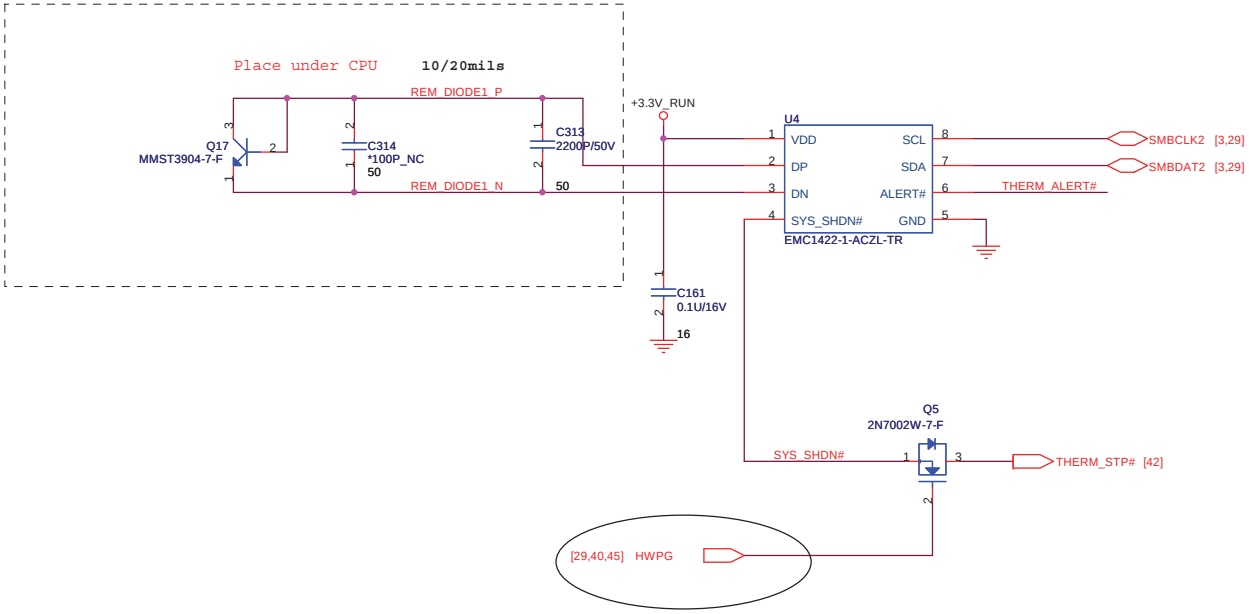

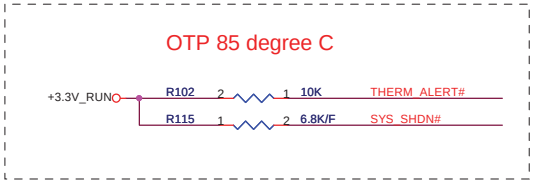

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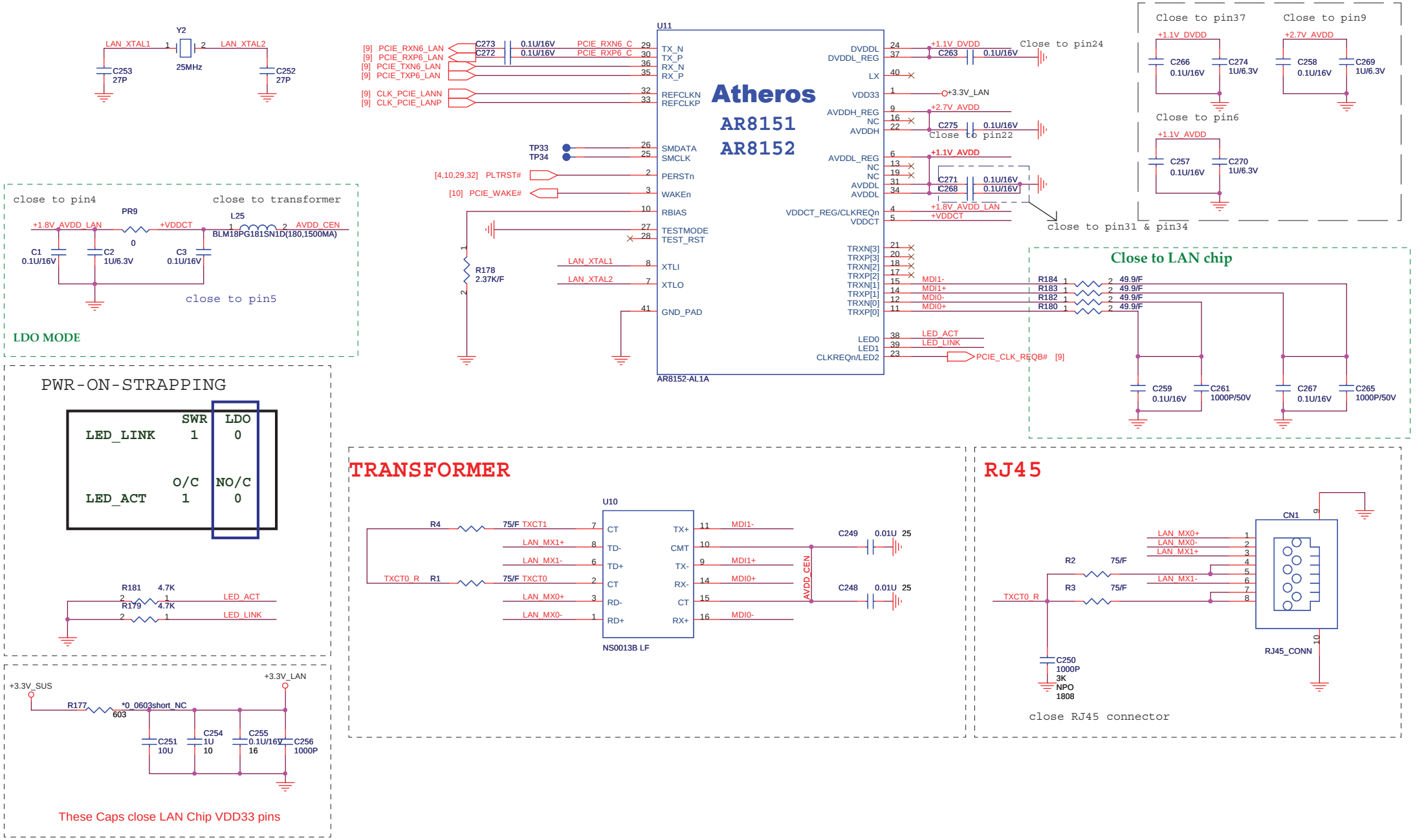

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Size	Document Number	Rev
	BTB CONN	1A

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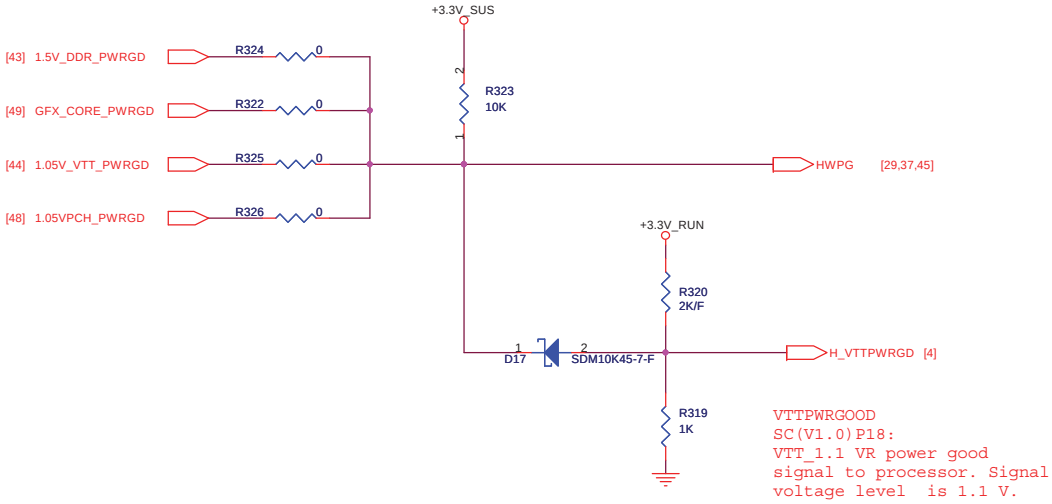

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	System Reset Circuit	1A

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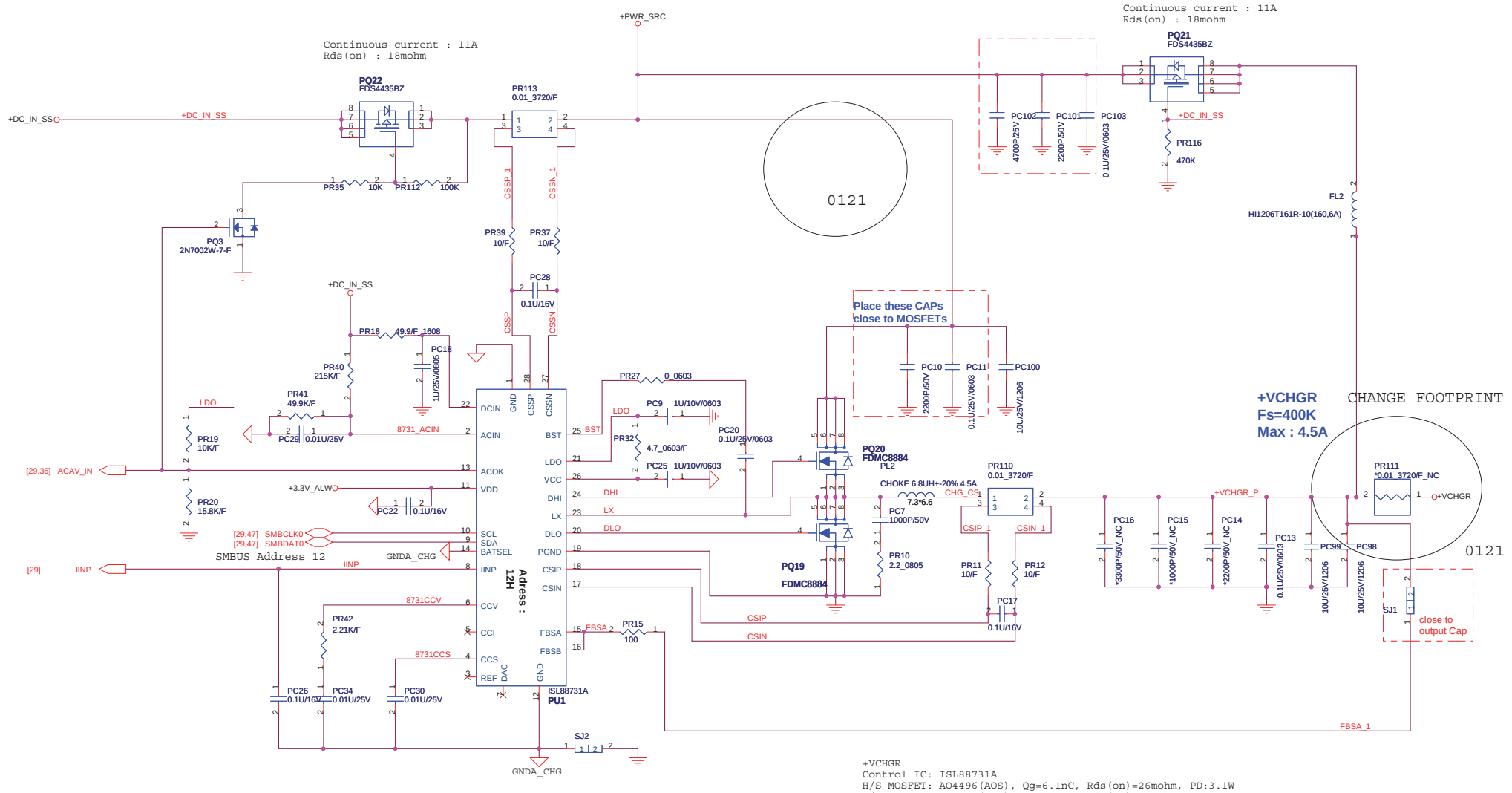

+VCHGR
Control IC: ISL88731A
H/S MOSFET: AO4496(AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496(AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
Inductor: 5.8UH +-30% 5.5A SDSL10D40F-5R8Y(TTA), DCR=21mohm
Output Cap: 2*10U 25V(+-10%,X6S,1206)

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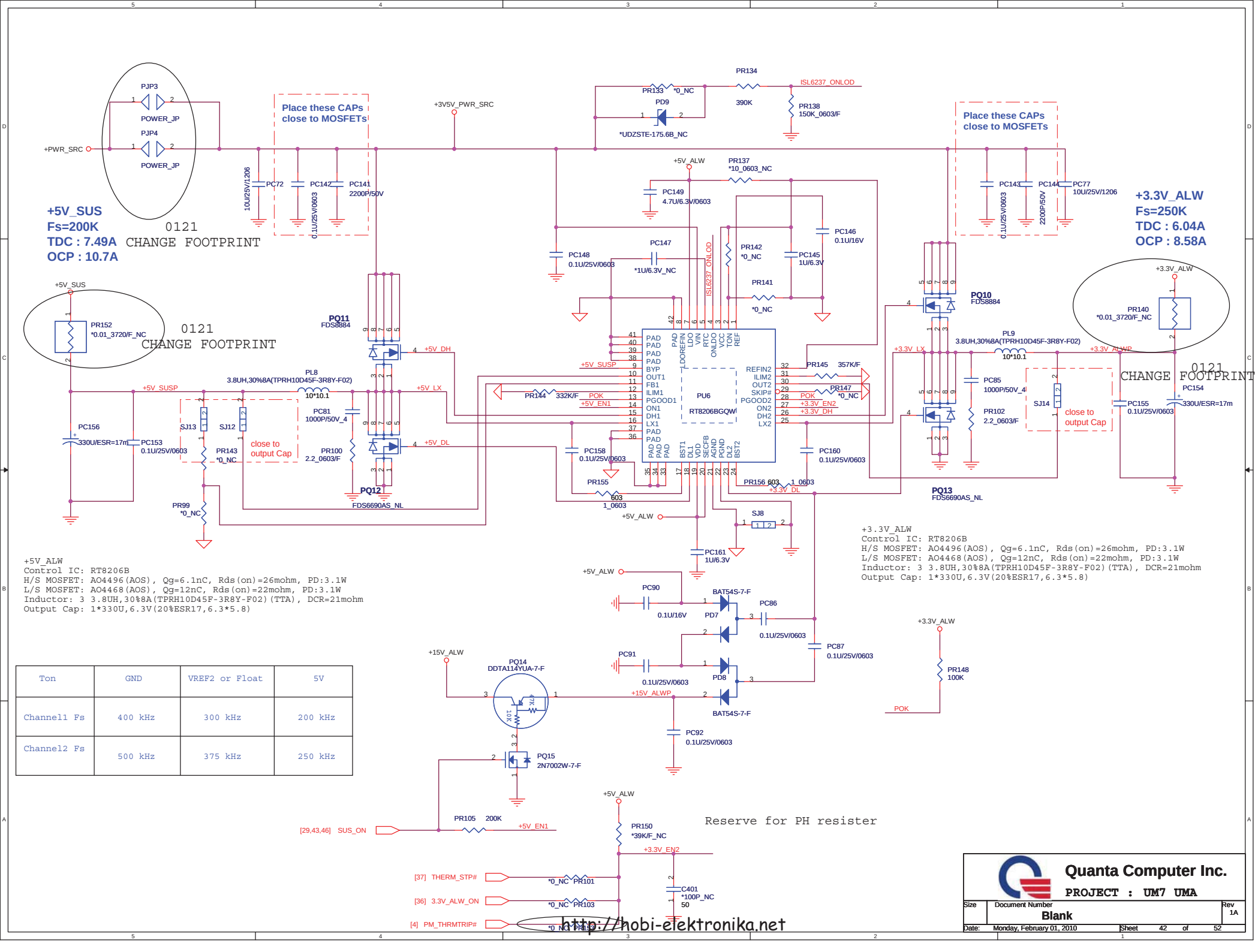
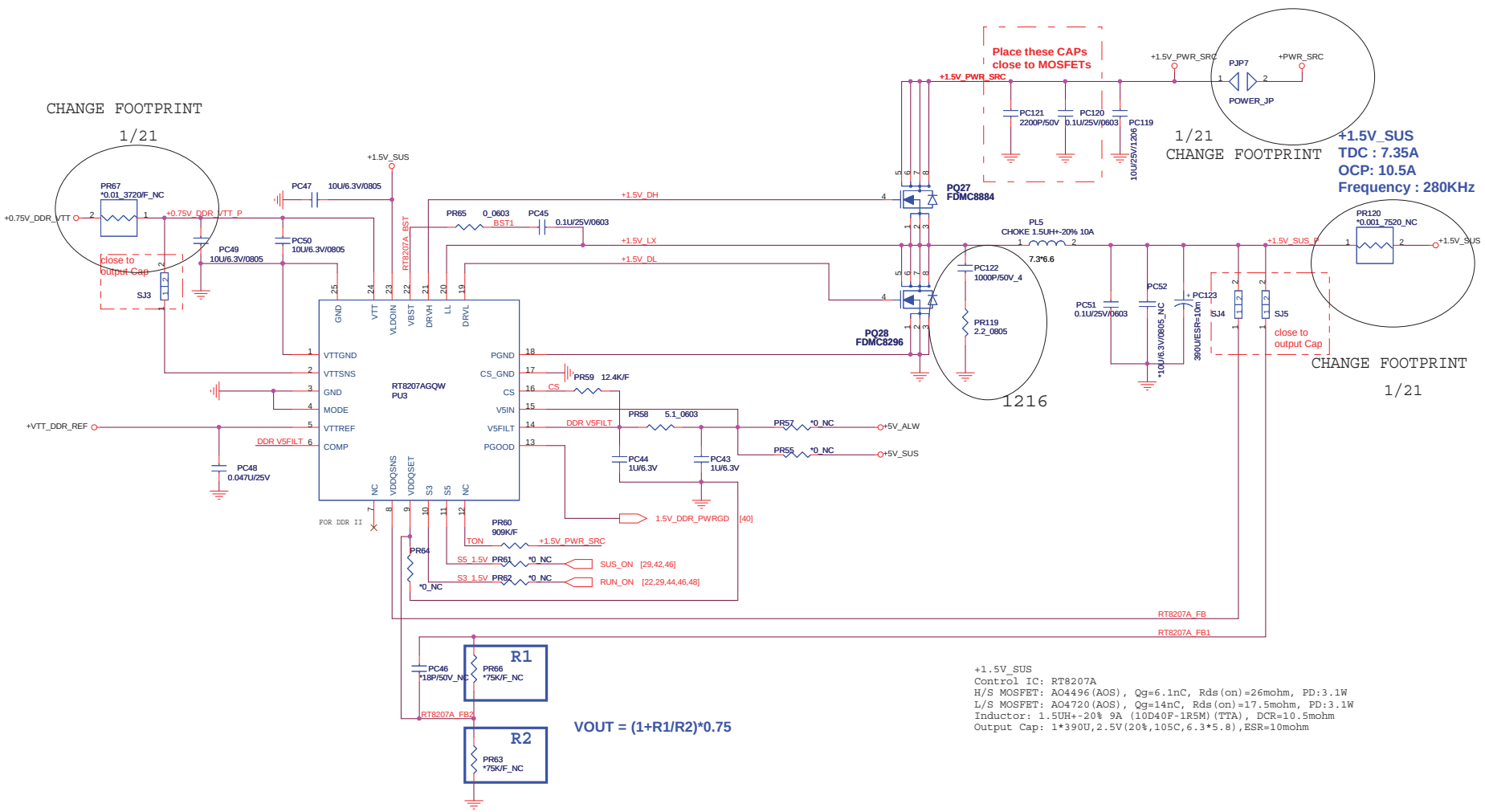


Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz



+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: AO4496(AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4720(AOS), Qg=14nC, Rds(on)=17.5mohm, PD:3.1W
Inductor: 1.5UH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

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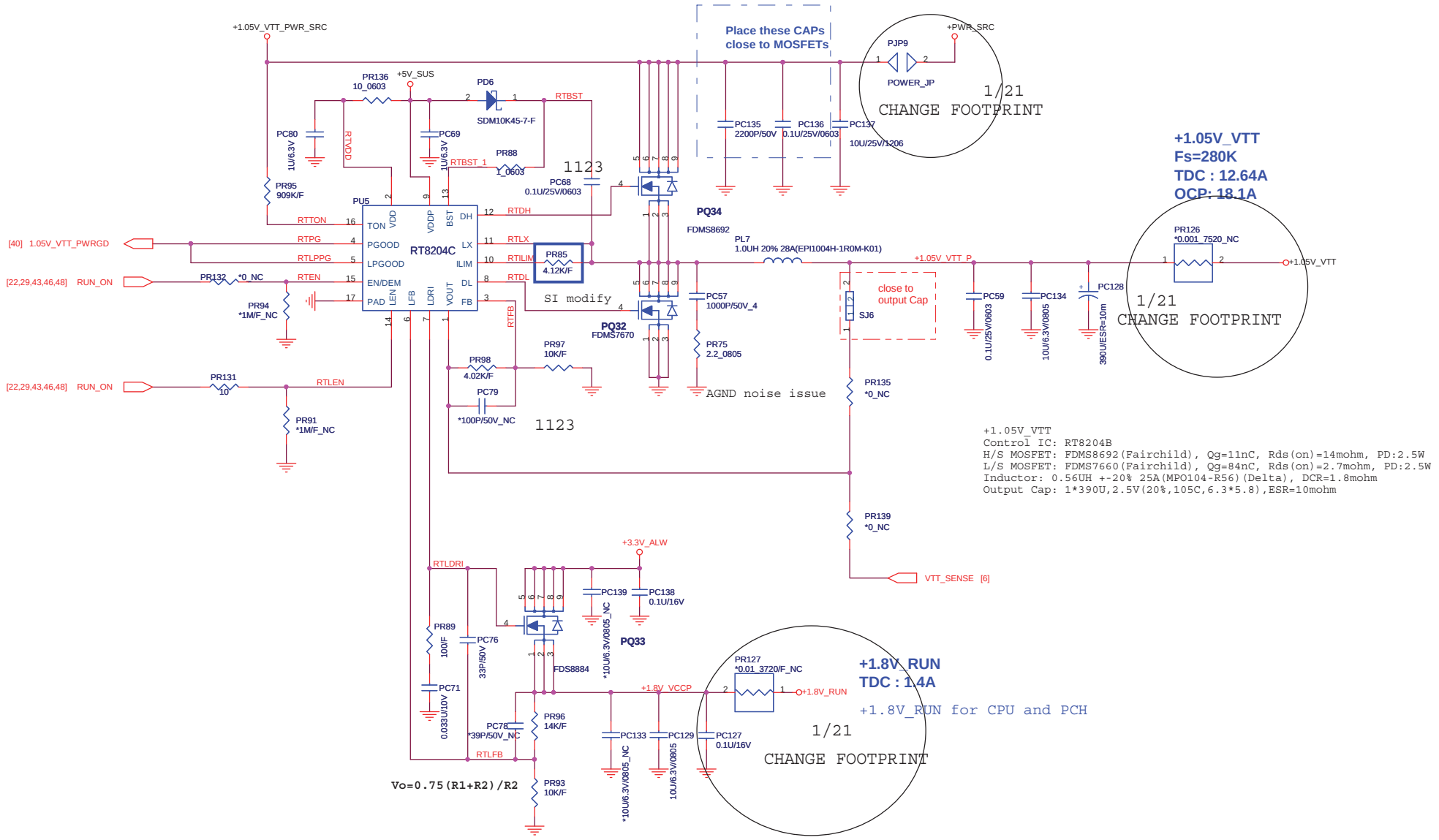

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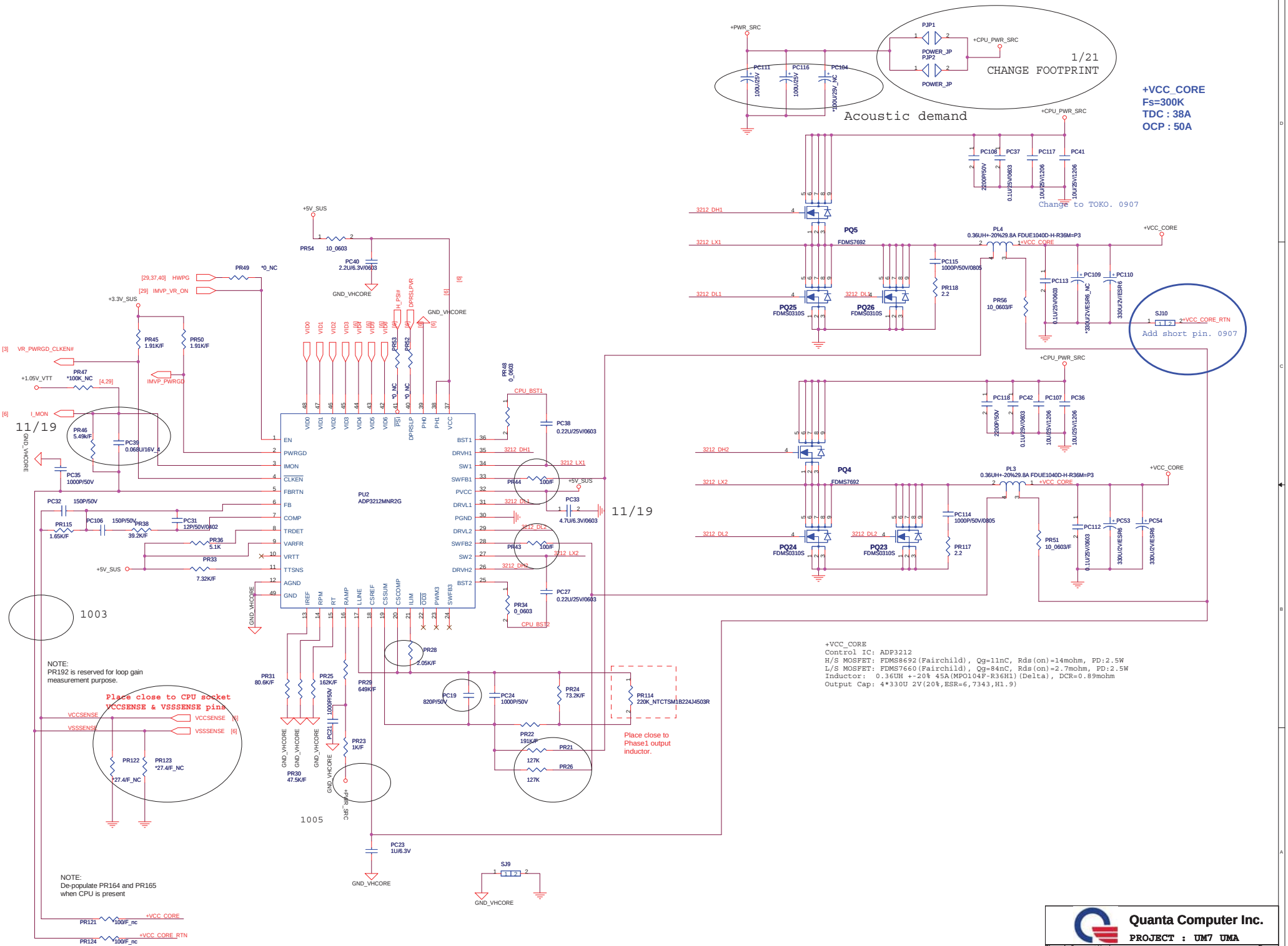
+VCC_CORE
Fs=300K
TDC : 38A
OCP : 50A
1/21
CHANGE FOOTPRINT
Acoustic demand
Change to TOKO. 0907
Add short pin. 0907
11/19
1003
1005
PU2
ADP3212MNR2G
PQ5
FDMS7692
PQ25
FDMS0310S
PQ26
FDMS0310S
PQ4
FDMS7692
PQ24
FDMS0310S
PQ23
FDMS0310S
PL4
0.36UH+-20%29.8A FDUE1040D-H-R36M=P3
PL3
0.36UH+-20%29.8A FDUE1040D-H-R36M=P3
+VCC_CORE
Control IC: ADP3212
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7660(Fairchild), Qg=84nC, Rds(on)=2.7mohm, PD:2.5W
Inductor: 0.36UH +-20% 45A(MPO104F-R36H1)(Delta), DCR=0.89mohm
Output Cap: 4*330U 2V(20%,ESR=6,7343,H1.9)
NOTE:
PR192 is reserved for loop gain measurement purpose.
Place close to CPU socket VCCSENSE & VSSSENSE pins
NOTE:
De-populate PR164 and PR165 when CPU is present
Place close to Phase1 output inductor.
Place close to PC98 +VCC_CORE & +VCC_CORE RTN pins
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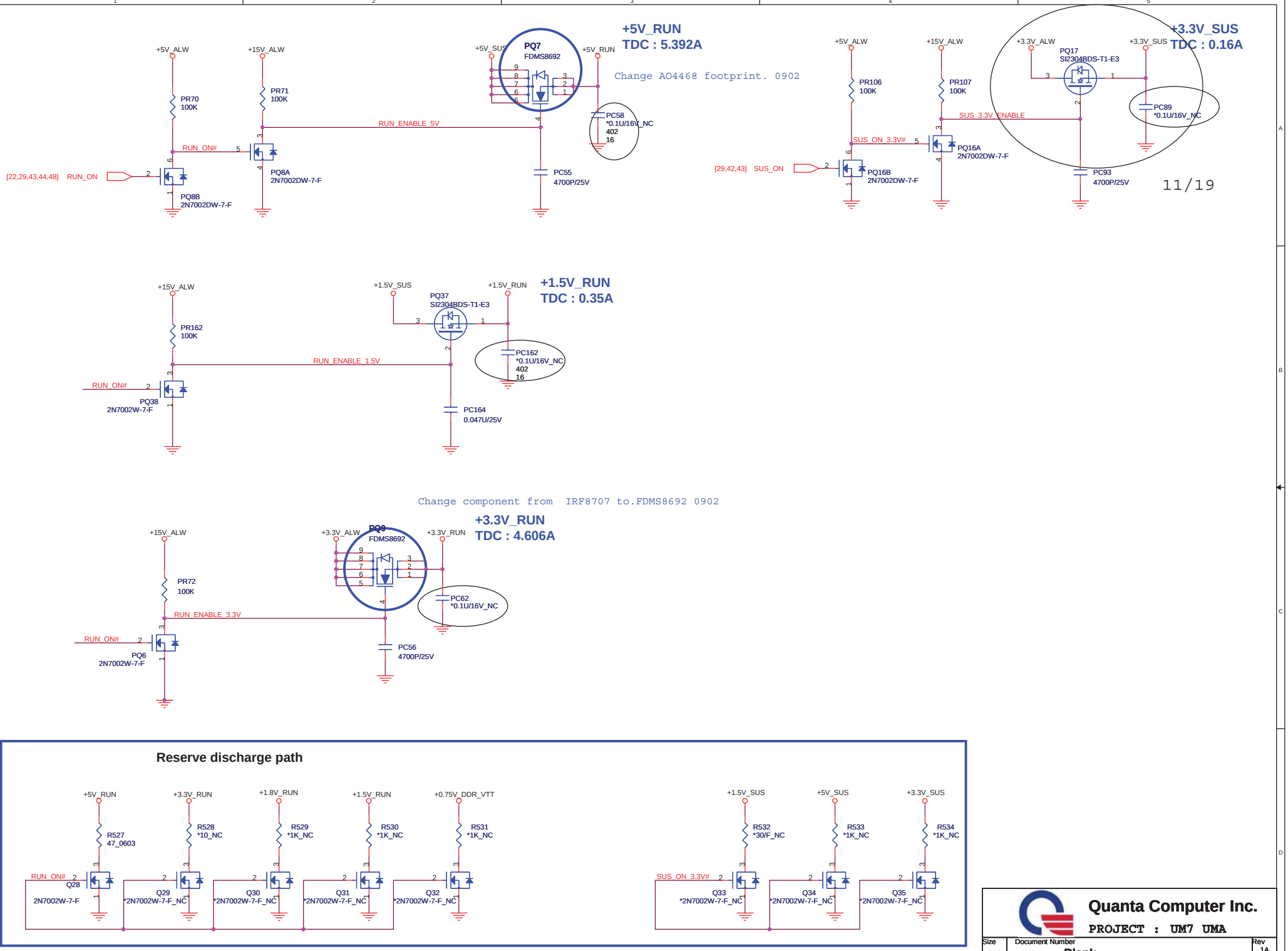

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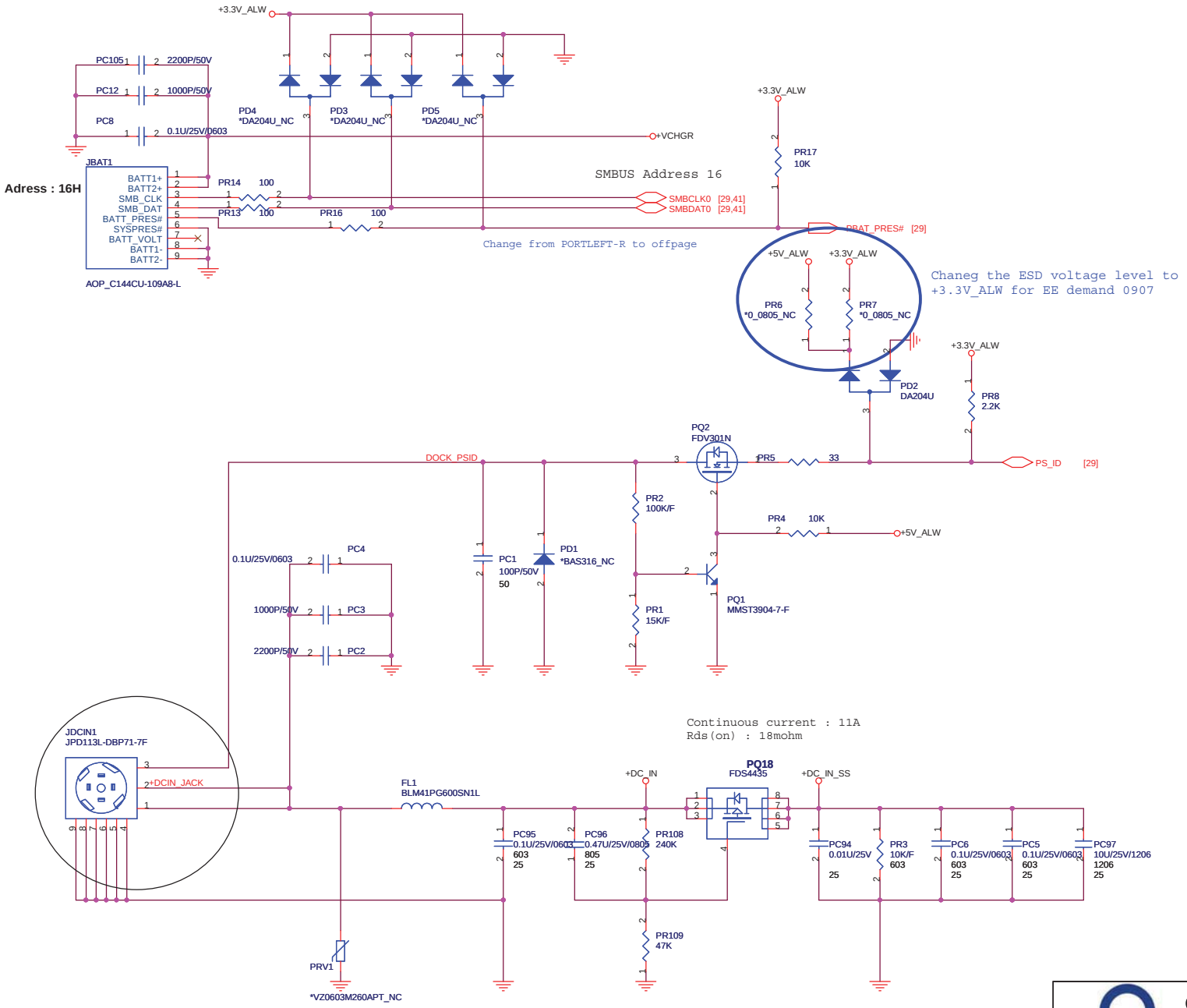

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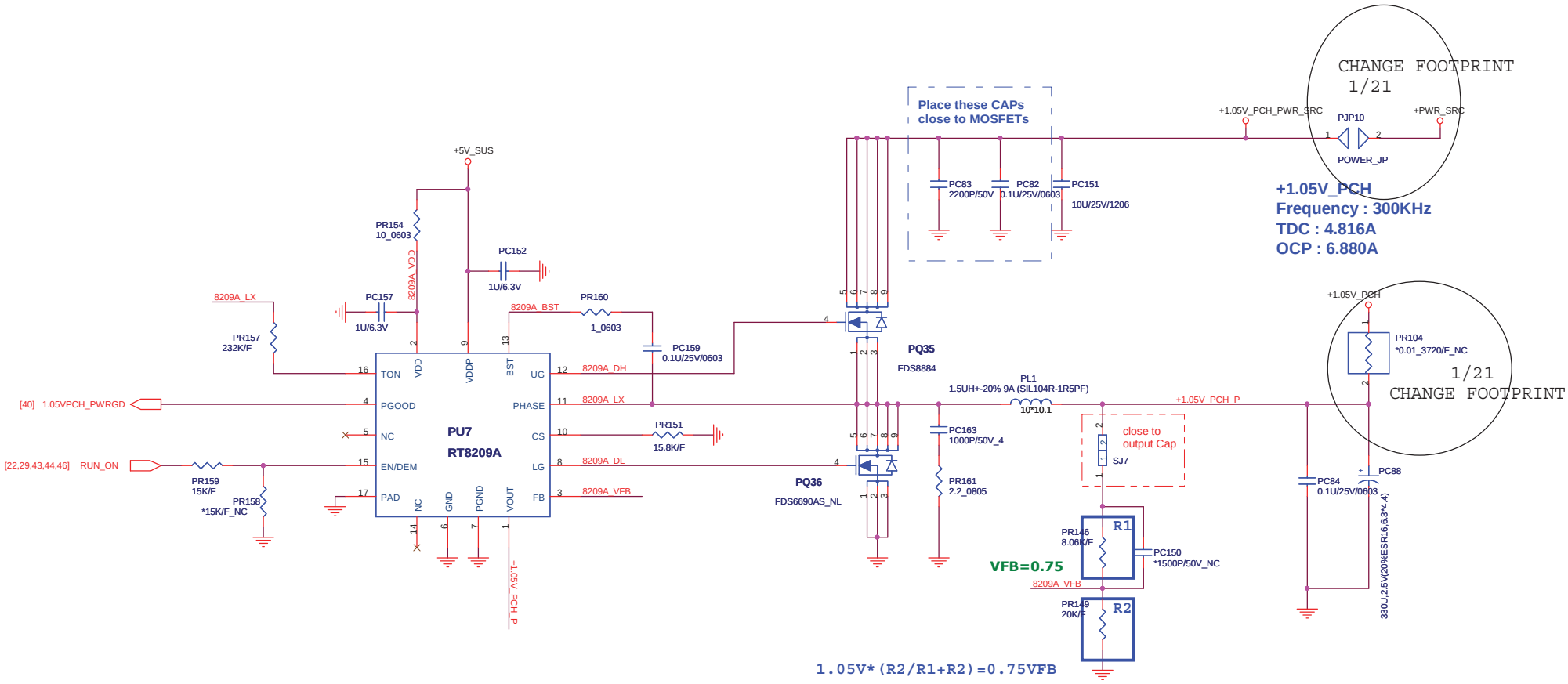

+1.05V_PCH
Control IC: RT8209A
H/S MOSFET: AO4496(AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4468(AOS), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 1.5UH+-20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

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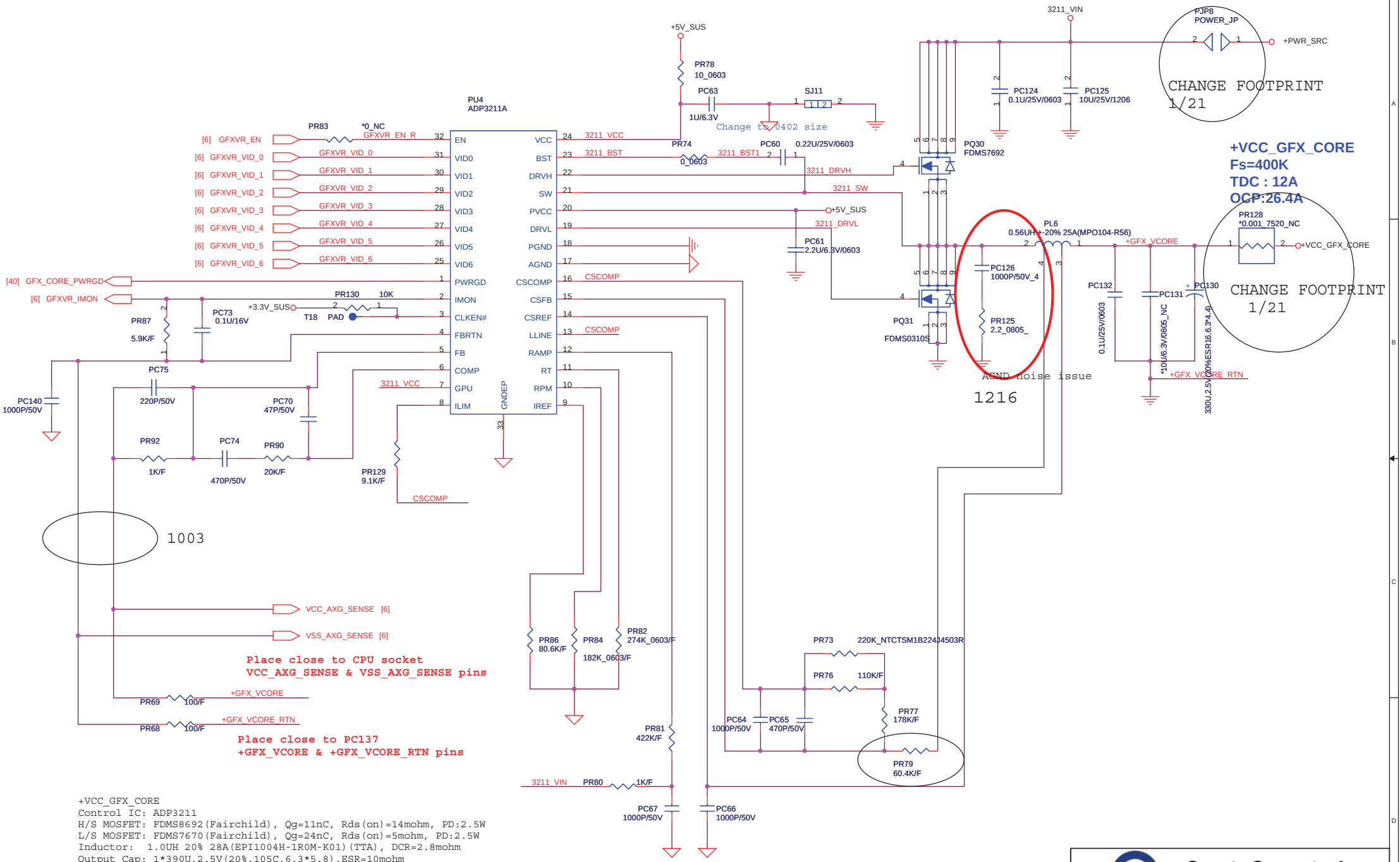

+VCC_GFX_CORE
Control IC: ADP3211
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*390U,2.5V(20%,105C,6.3*5.8),ESR=10mohm

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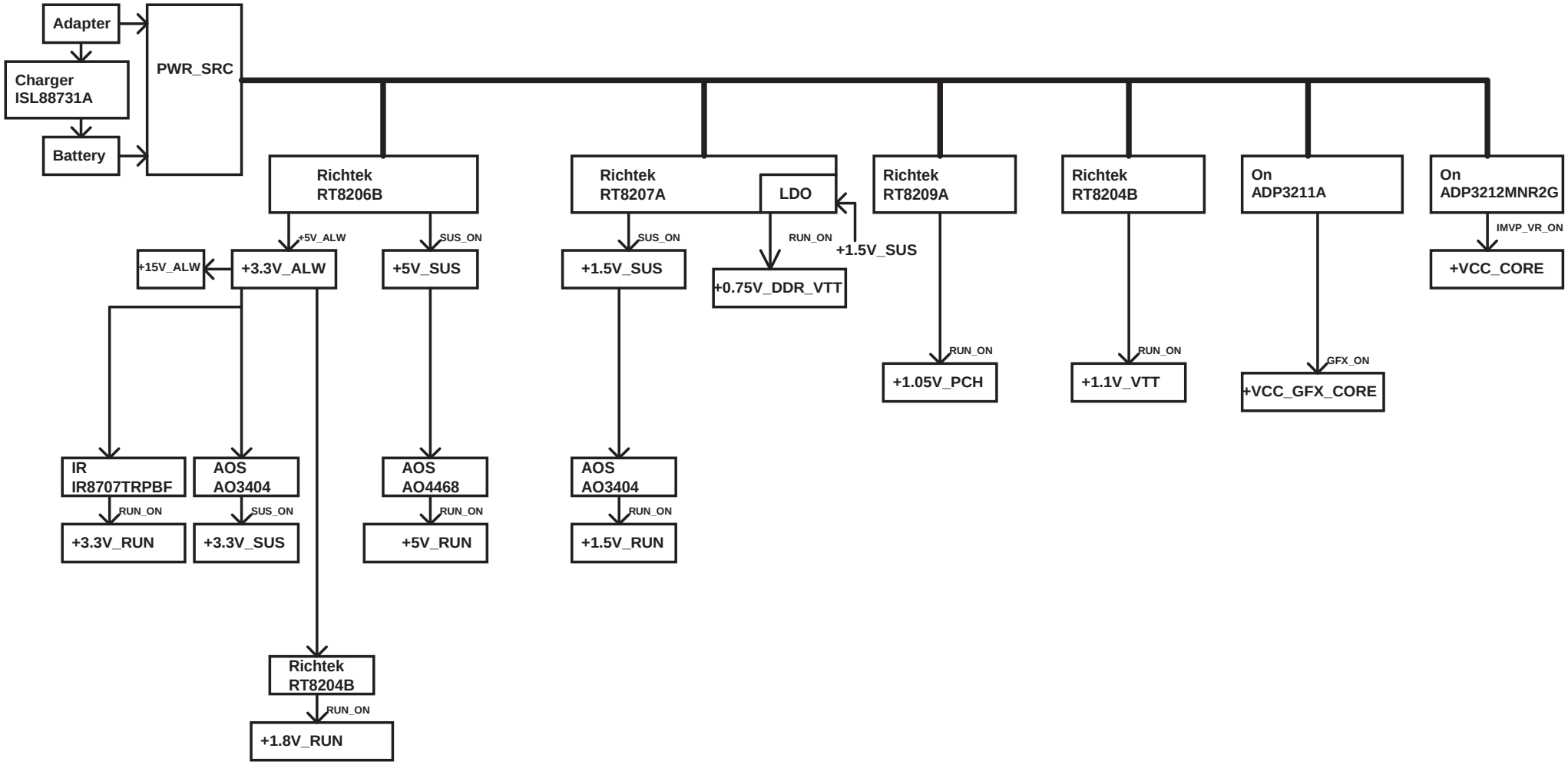

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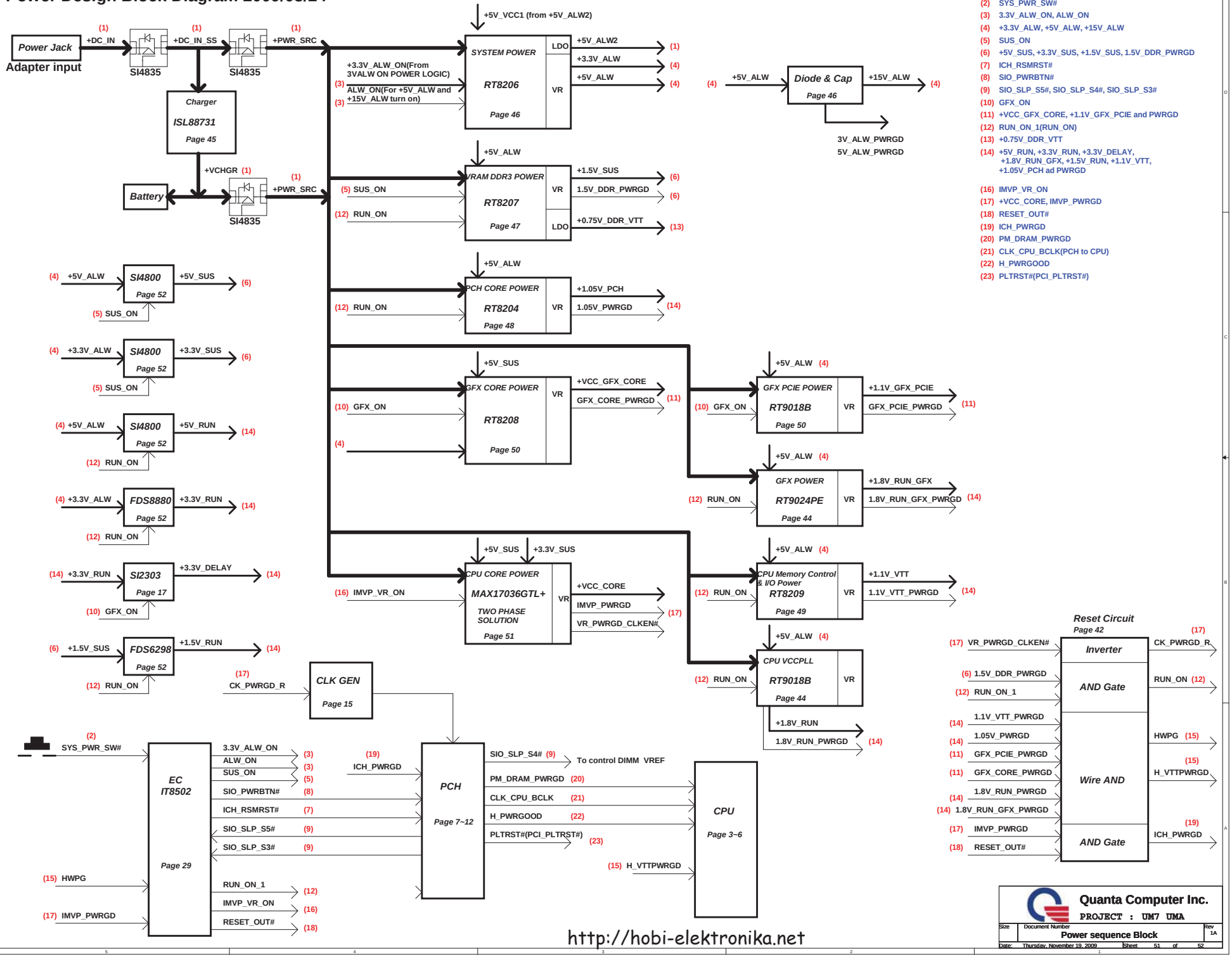
Power Design Block Diagram 2009/08/24



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

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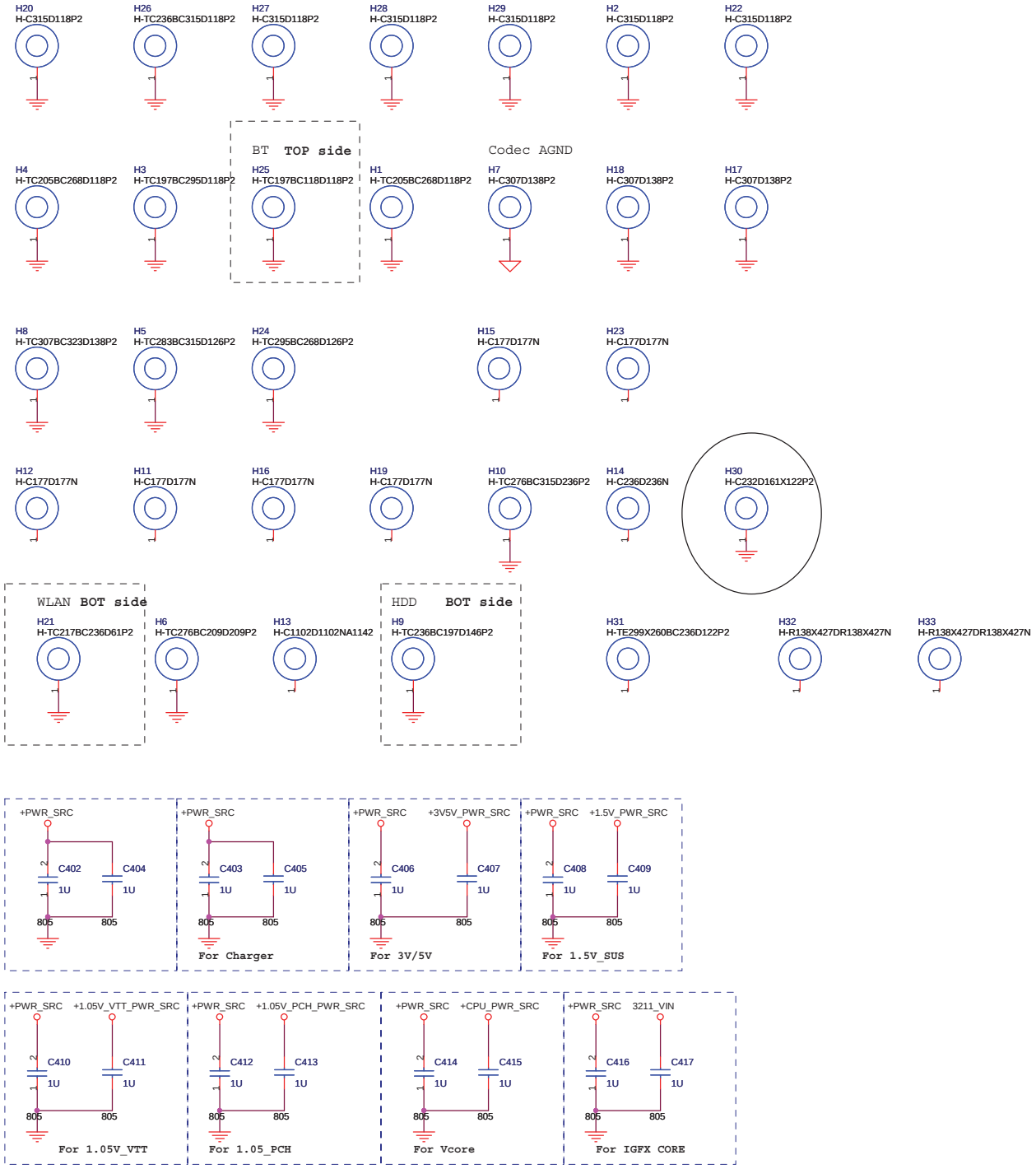

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