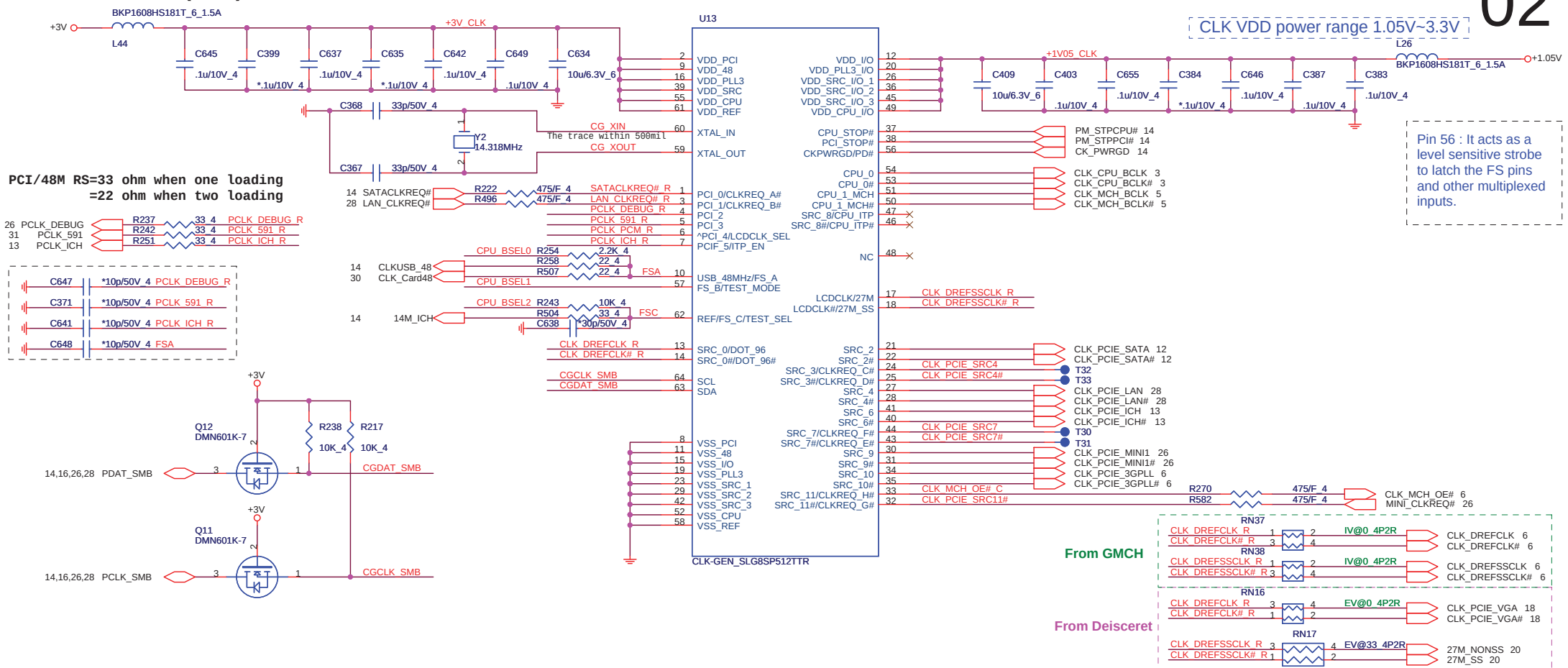
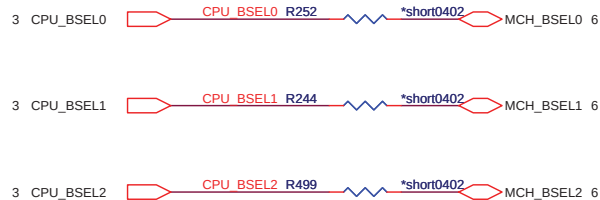


Clock Generator (CLK)



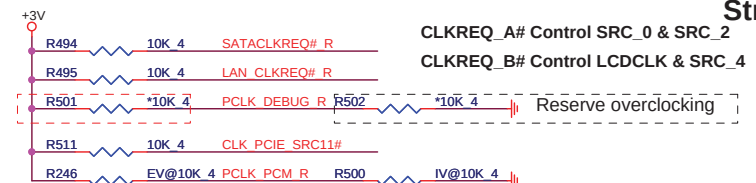
CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection



BSEL Frequency Select Table

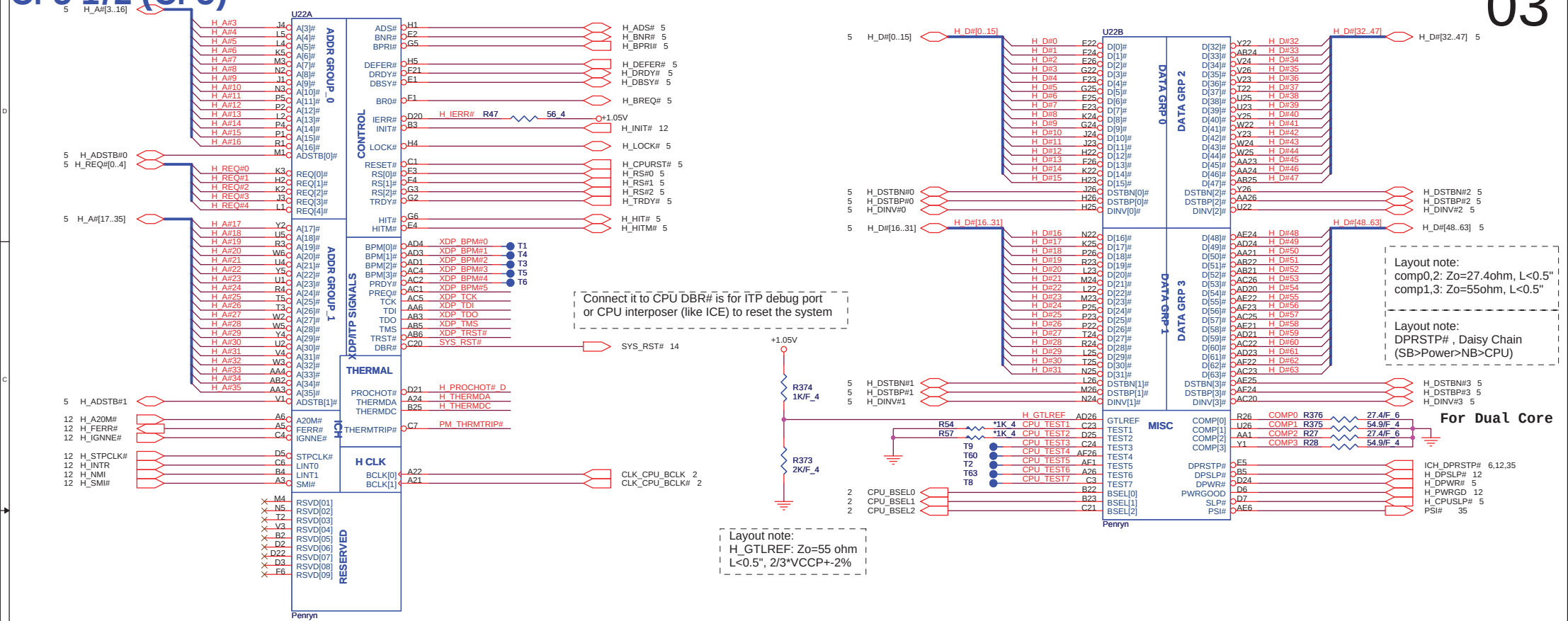
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



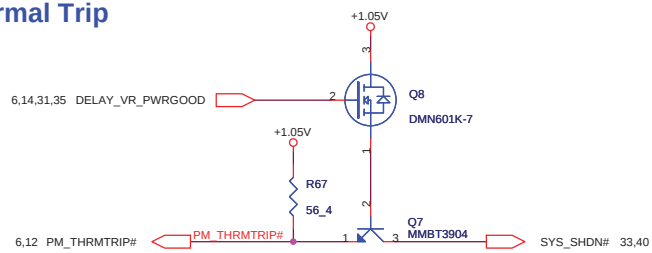
Pin 6 : For Pin 13/14 and 17/18 selection
 0 = LCDCLK & DOT96 for internal graphic controller support
 1 = 27M & 27M_SS & SRC_0 for external graphic controller support

Pin 7 : For Pin 46/47 selection
 1 = CPU_ITP
 0 = SRC_8

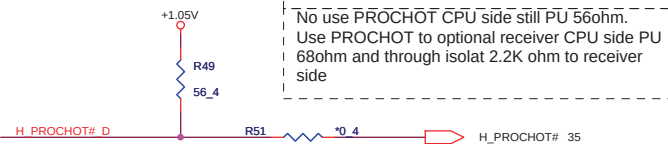




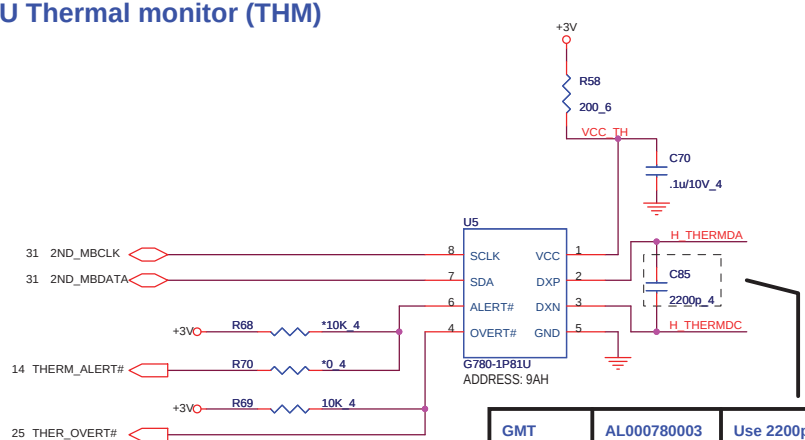
Thermal Trip



Processor hot

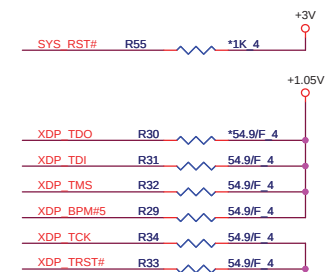


CPU Thermal monitor (THM)



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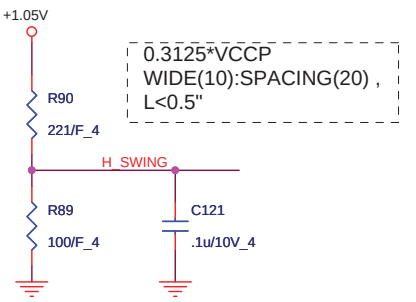
XDP PU/PD



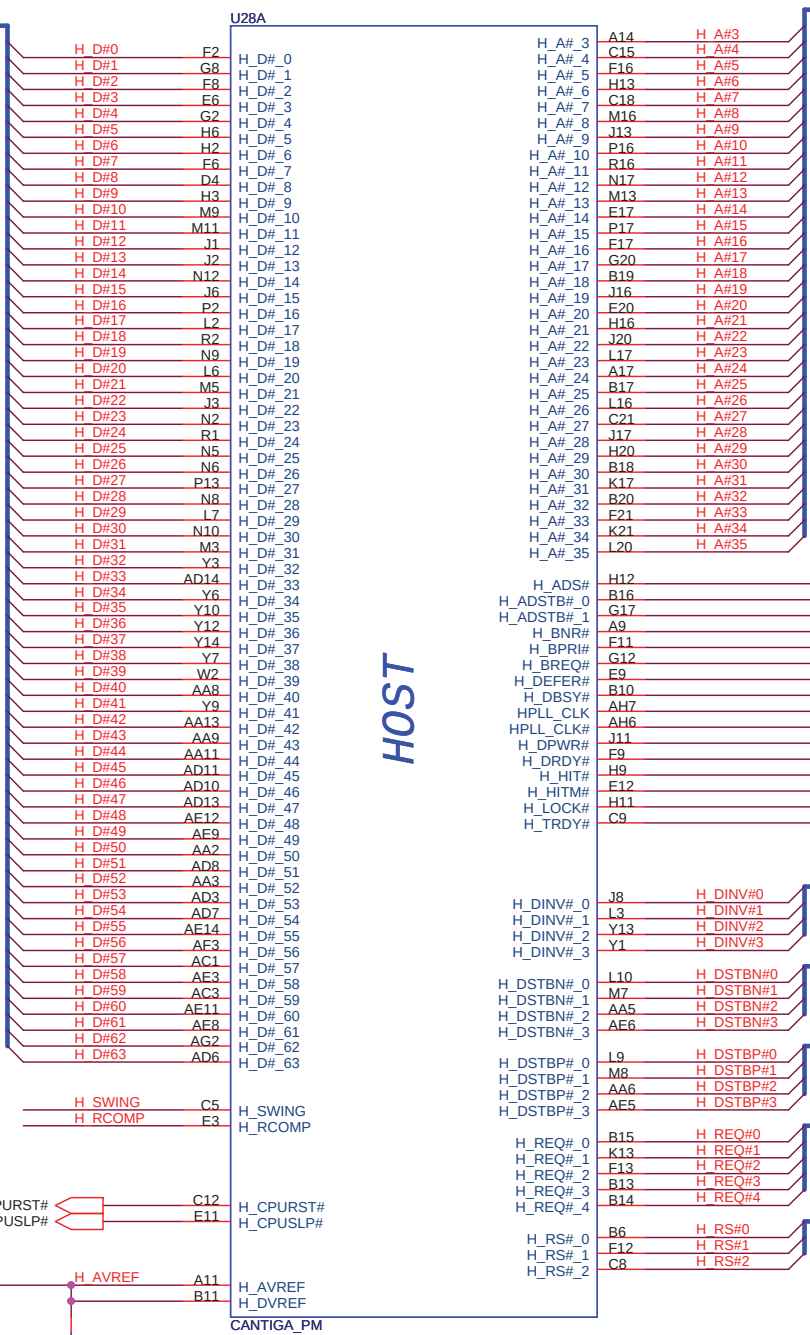
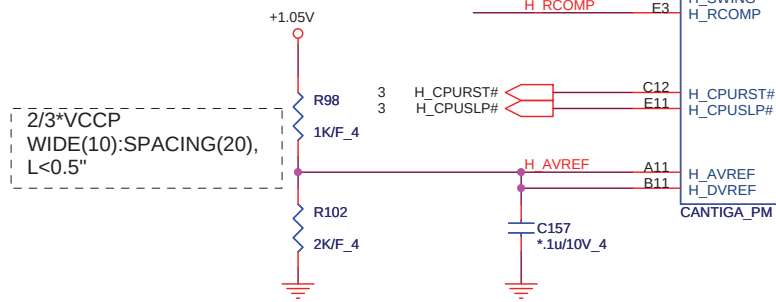
```
| XDP_DBRESET# and XDP_TDO |
| reserve for XDP           |
```


GMCH-CANTIGA(CLG)

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



Layout Note:
WIDE(10):SPACING(20),
L<0.5"





Quanta Computer Inc.

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GMCH HOST

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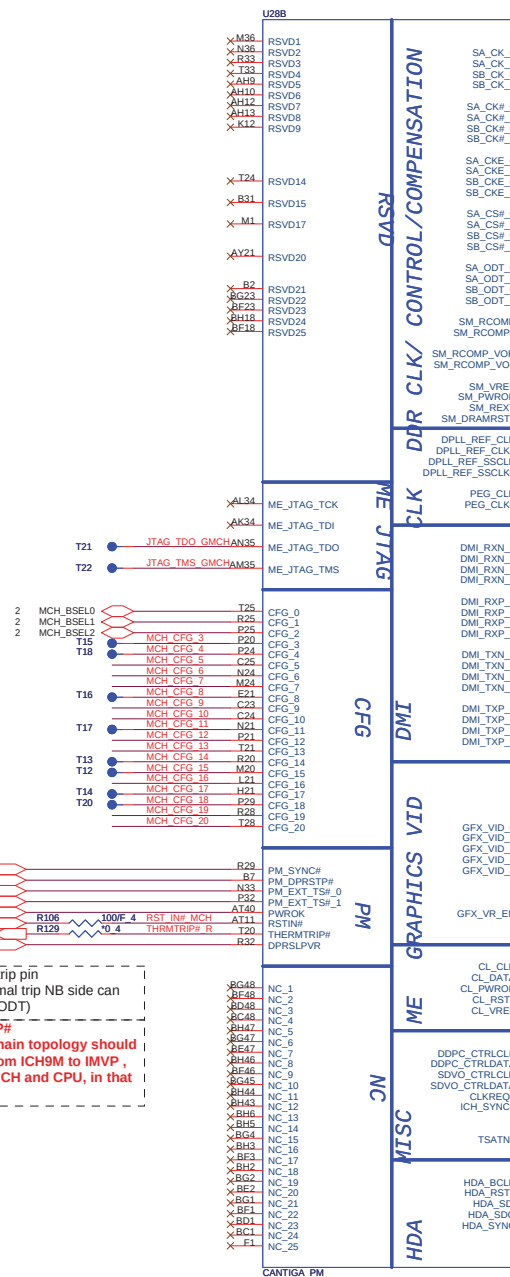
GMCH-CANTIGA(CLG)

IV@
EV@

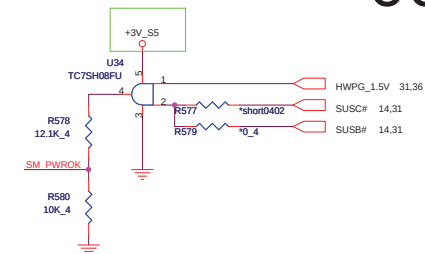
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) and Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

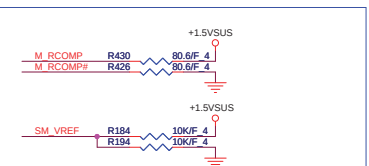
Strap pin



CANTIGA_PM

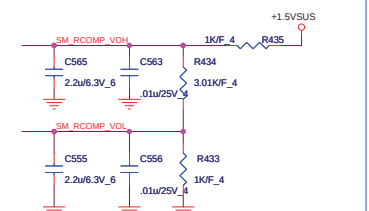
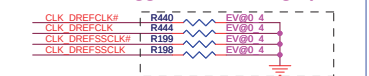


SM_VREF=0.5*VCC_SM
SM_PWROK only for DDR3(DDR2 PD only)
SM_DRAMRST# only for DDR3(DDR2-NC)

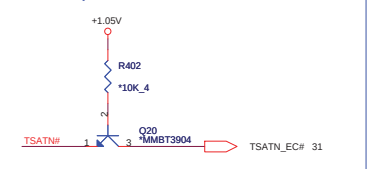


SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics



NB Thermaltrip



DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

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09

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GMCH VCC,NCTF		
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10

STUFF 5.6 onm

1210 10UH, 10%
0.45A DCR max = 0.39



VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

POWER

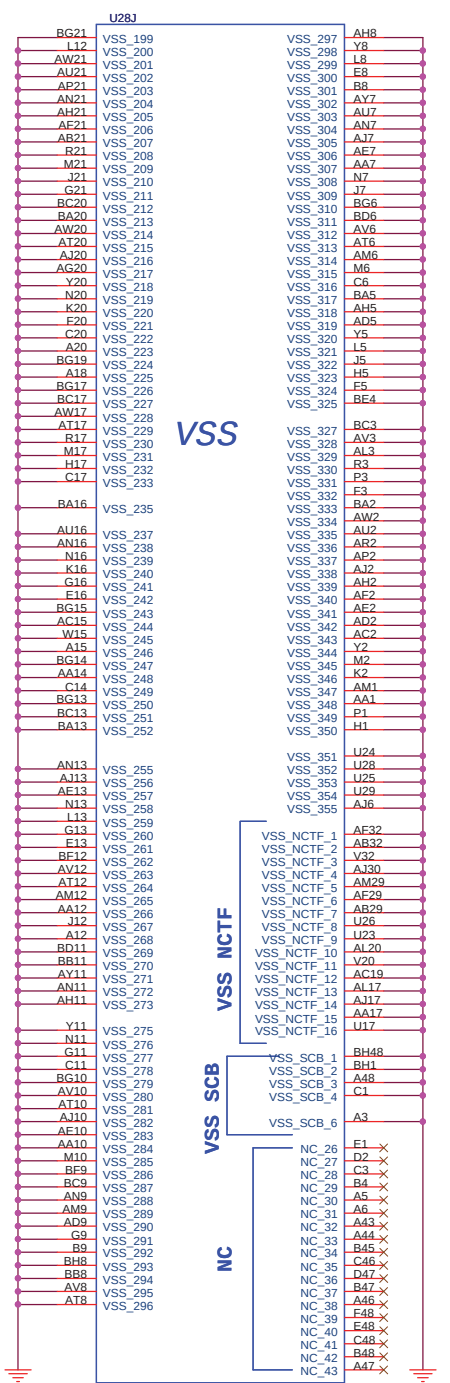
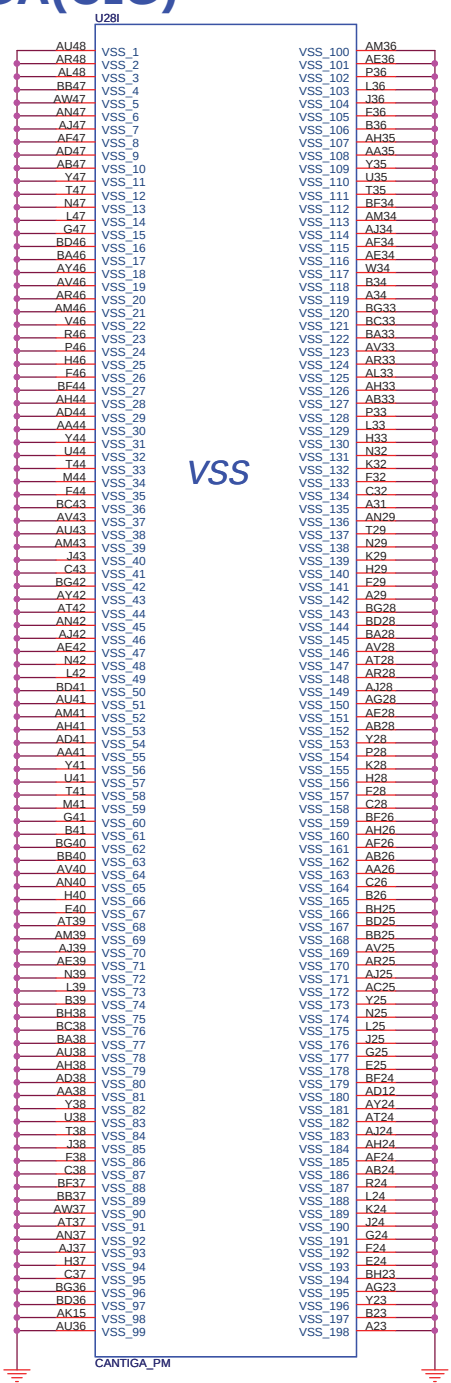
Power Net Name	Cantiga(V)
VCC_A06_#	1.05V
VCC_A06_NCTF_#	
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLL	1.05V
VCCA_SK_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SK_CR_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_A06_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

0 Ohm SP@1u/10V/4

VCC_AXF_#	1.05V
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GMCH-CANTIGA(CLG)



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Quanta Computer Inc.

PROJECT : ZR6

Size

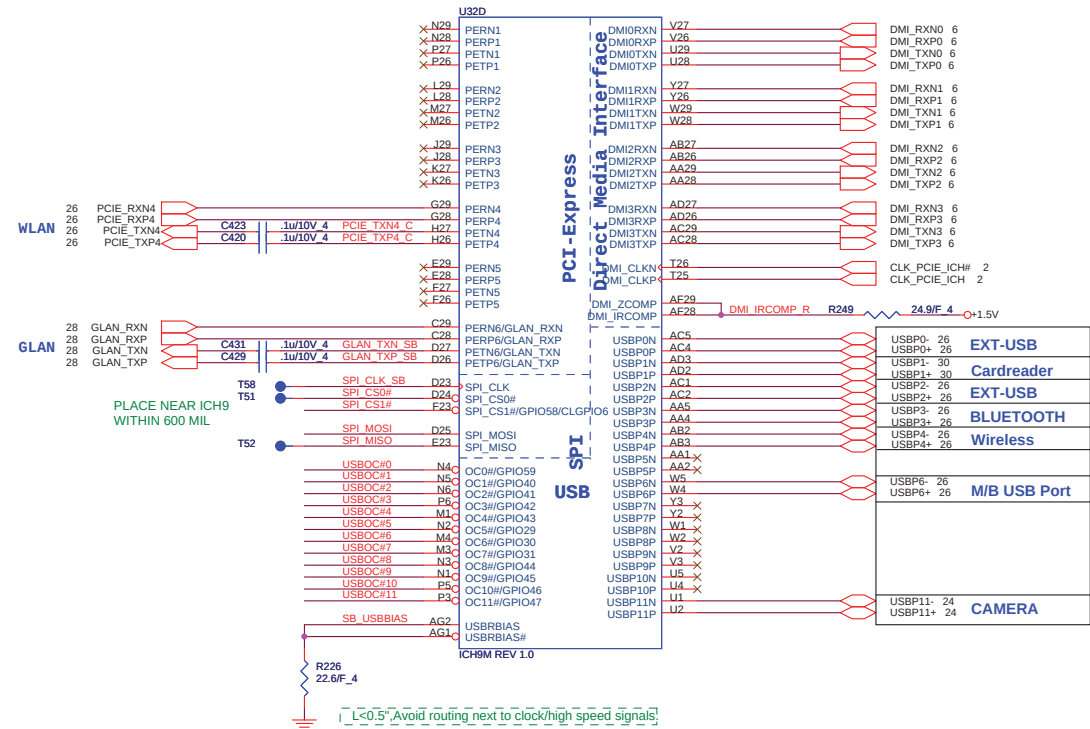
Document Number

Rev 1A

GMCH VSS

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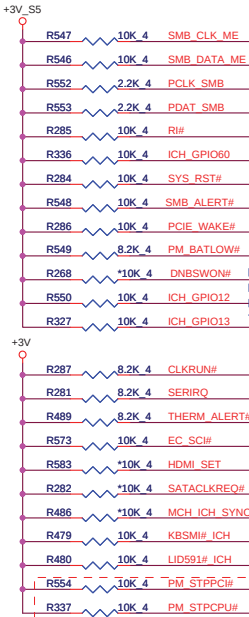


Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC(Default)	

ICH9M(CLG)

D3A:(1/31) ASF issue:when iAMT is not implemented,
ICH9M SMBus and SMLink should be connected together to support slave mode
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

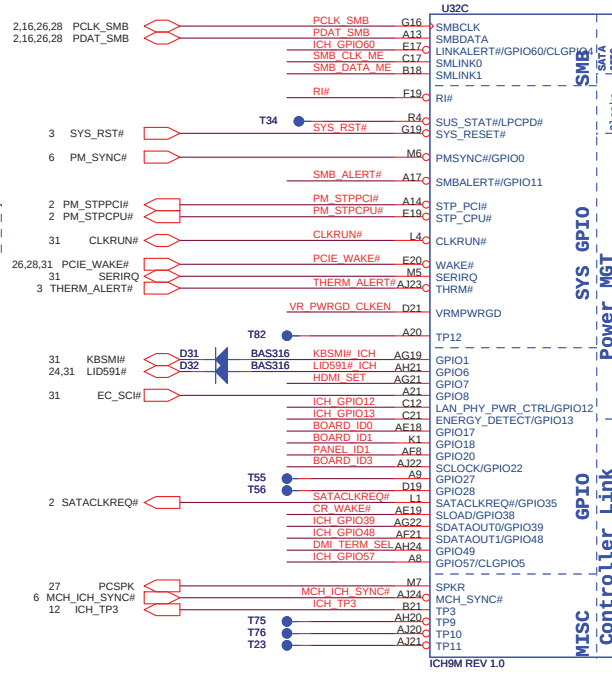
SATA[x]GP pins if unused may be
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground



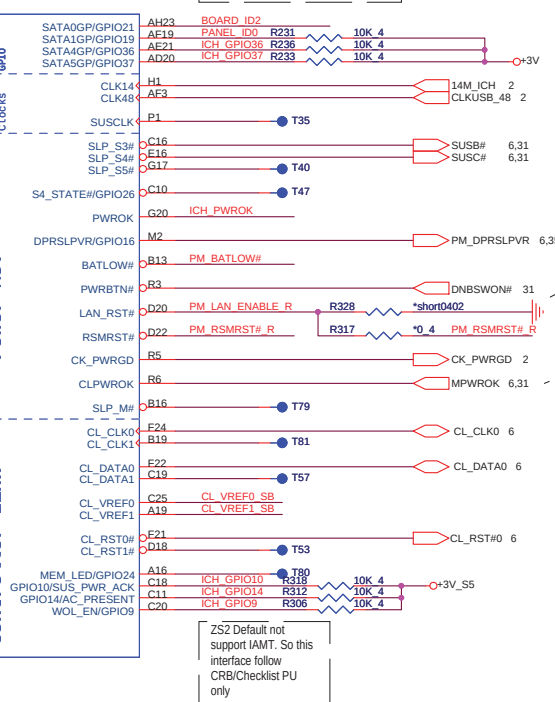
PWRBTN : 16 ms of internal debounce
logic on this pin and internal PU 24K

TPM Physical
Presence for
ITPM.

Stuff	HDMI SET
R583	HDMI
R315	No HDMI



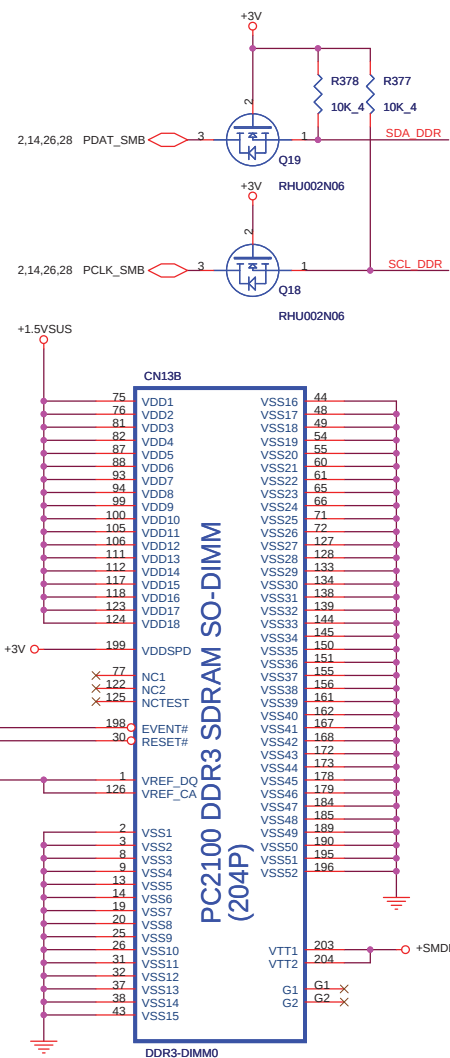
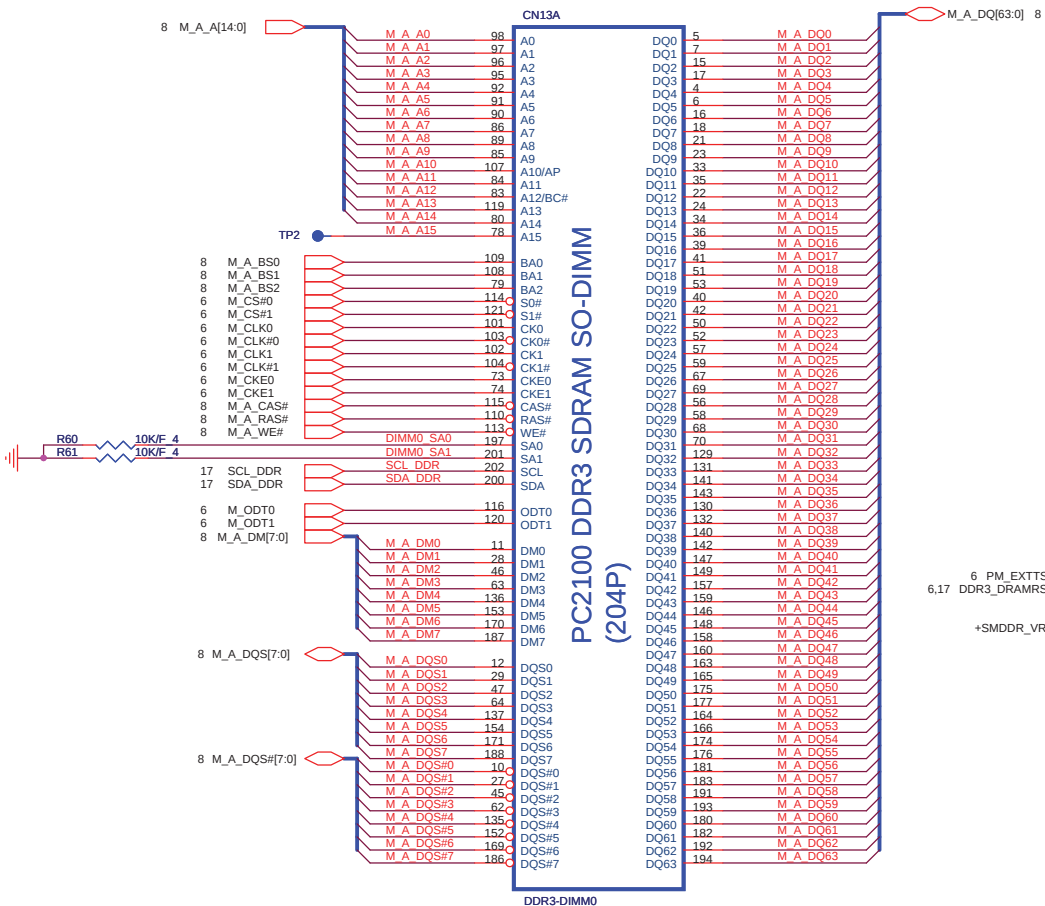
ICH9M REV 1.0



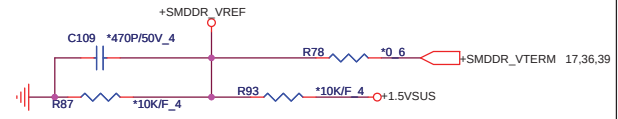
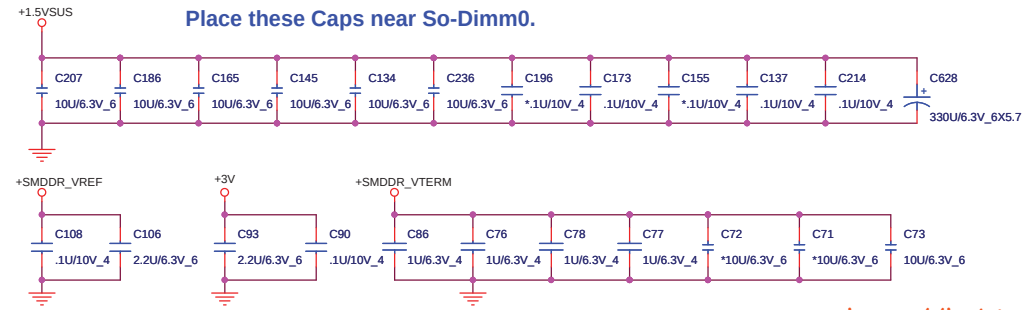
8

DDR3 (DDR)

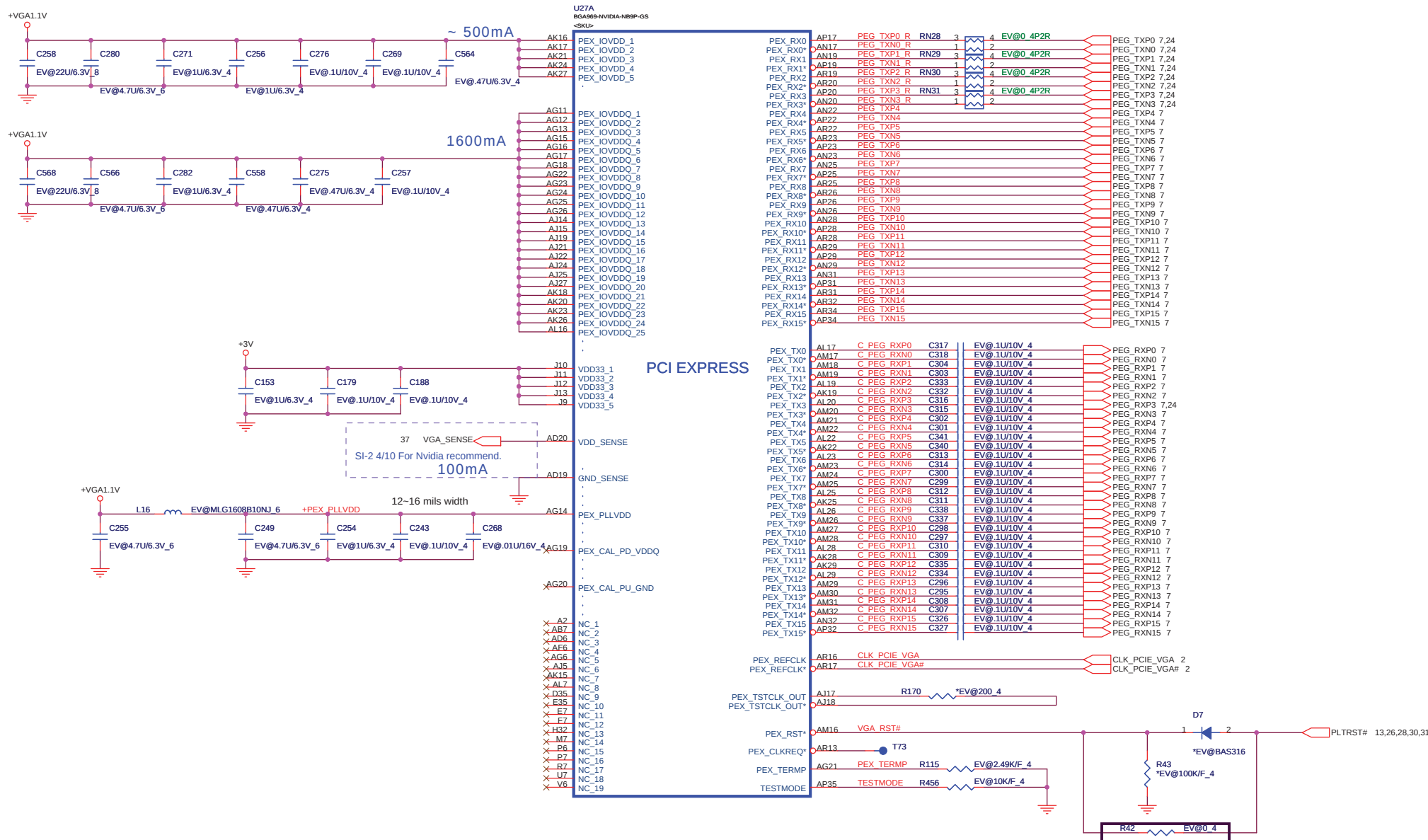
16

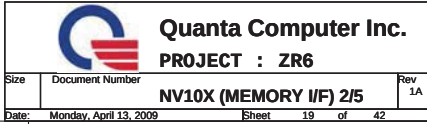


Place these Caps near So-Dimm0.

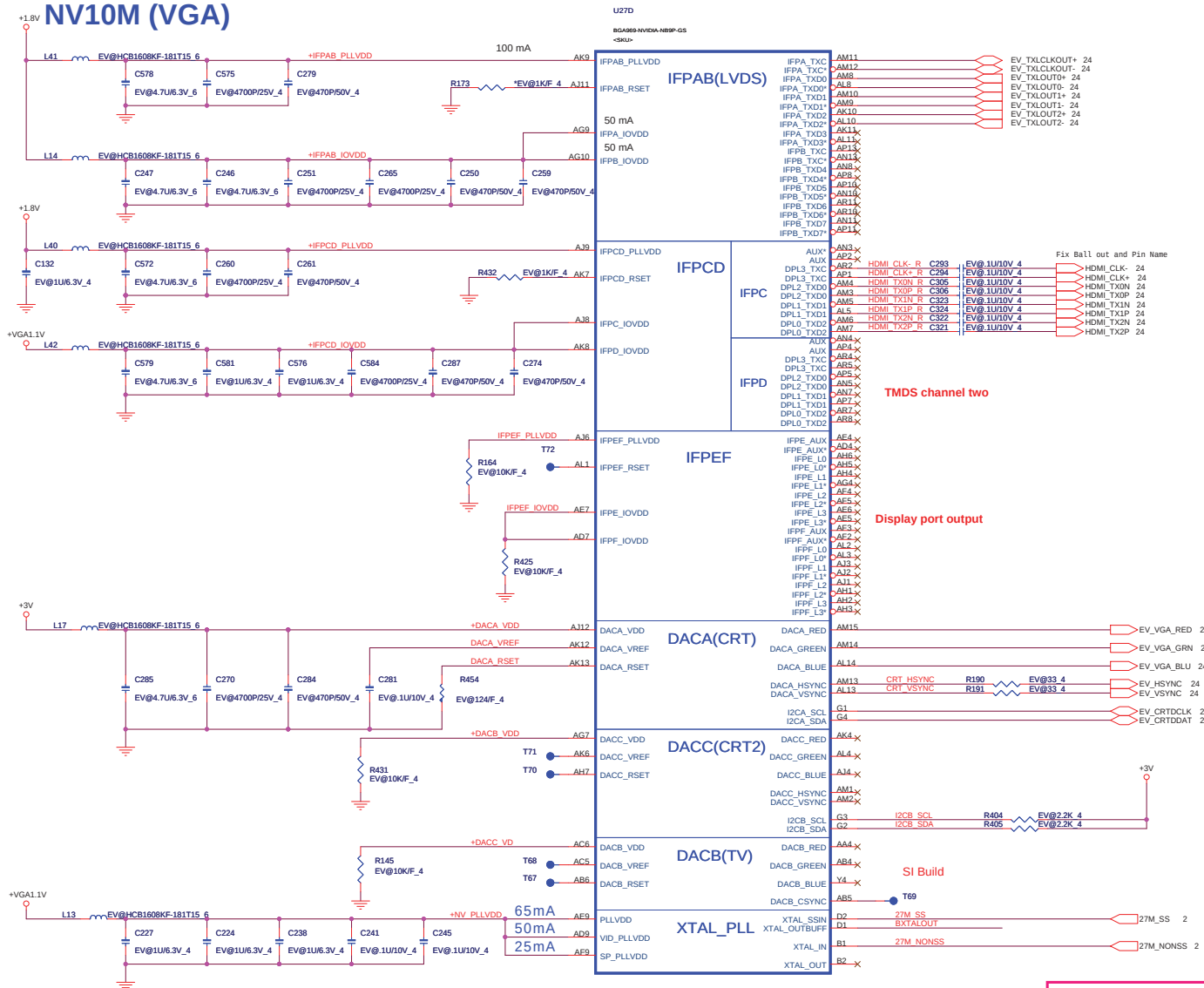


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NV10M (VGA)



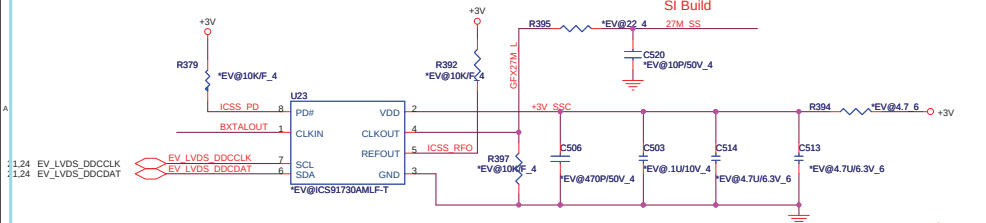
TMDs channel two

Display port output

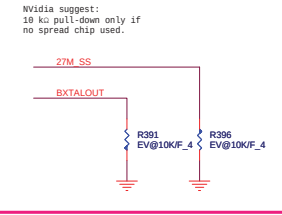
SI Build



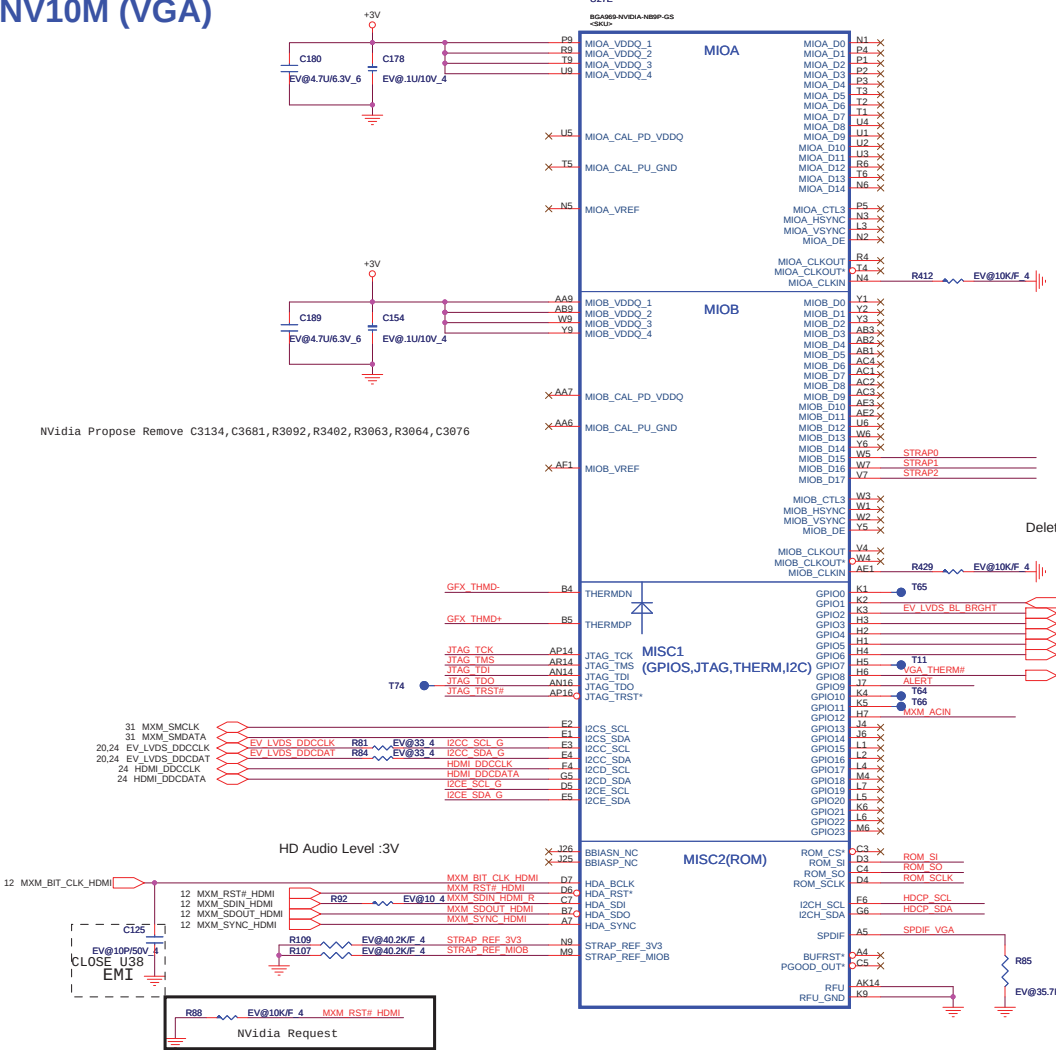
SPREAD SPECTRUM



I2C ADDRESS: 0xD4H

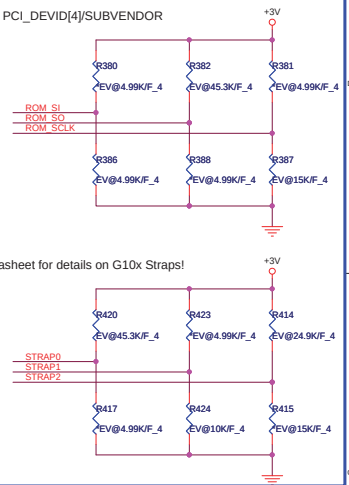
<http://hobi-elektronika.net>

NV10M (VGA)



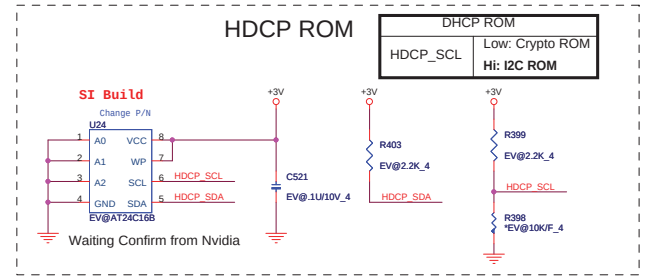
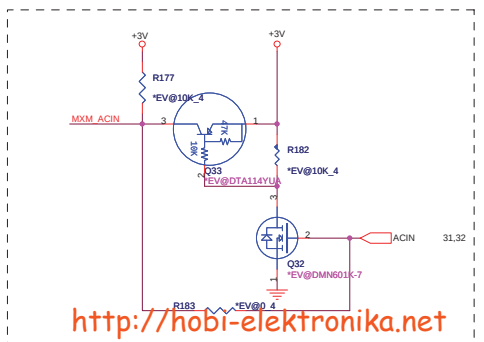
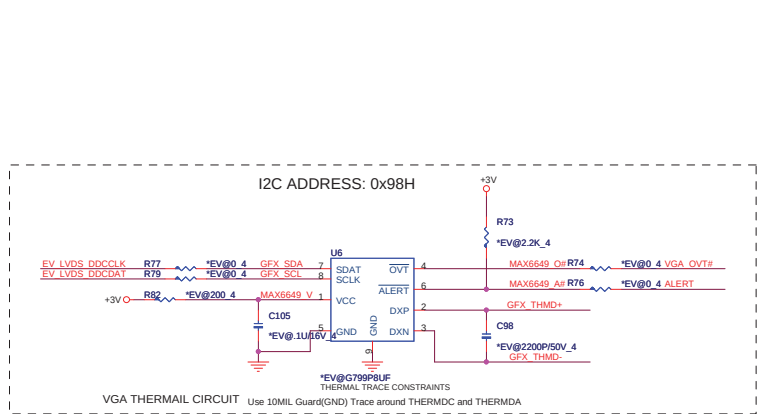
N10P-GE1 (G96) Straps N10M-GE1 (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

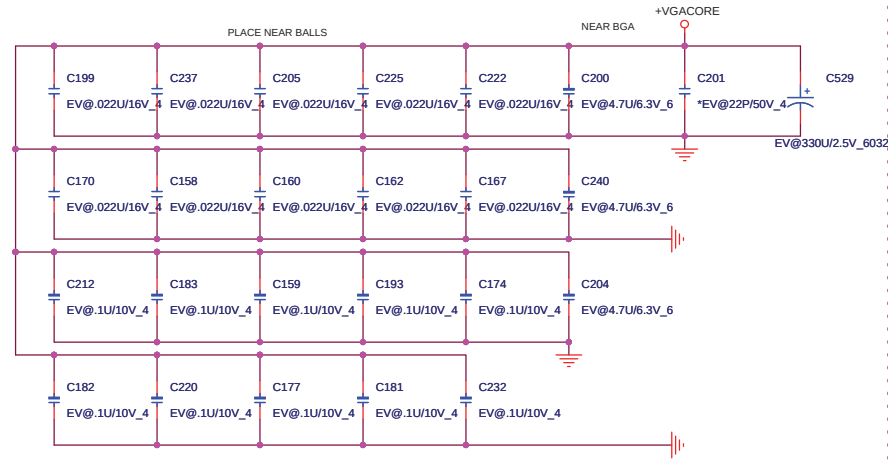
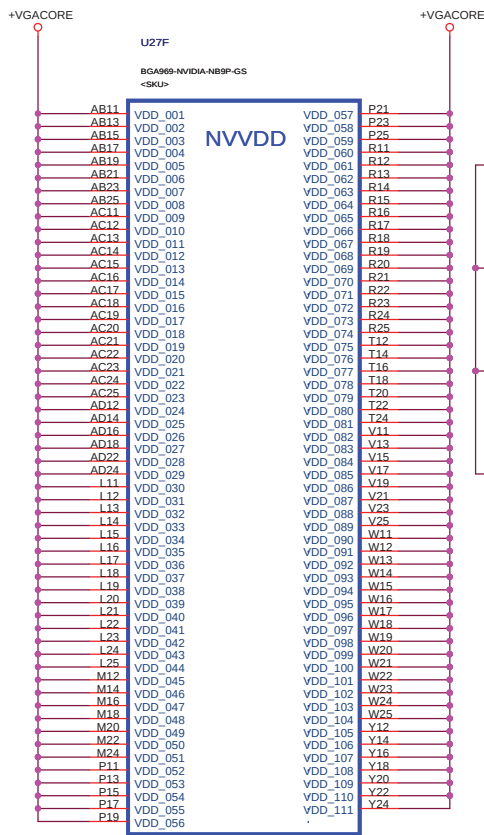


Logical Strap Bit Mapping			
	R414	PU-VDD	PD
NB9M-GE 0x06E 8	1000	5K	1000 0000
NB9M-GS 0x06E 9	1001	10K	1001 0001
NB9P-GE2 0x064 8	1000	15K	1010 0010
NB9P-GS 0x064 9	1001	20K	1011 0011
N10P-GE1 0x065 2	0010	25K	1100 0100
N10M-GE1 0x06E C	1100 default	30K	1101 0101
		35K	1110 0110
		45K	1111 0111

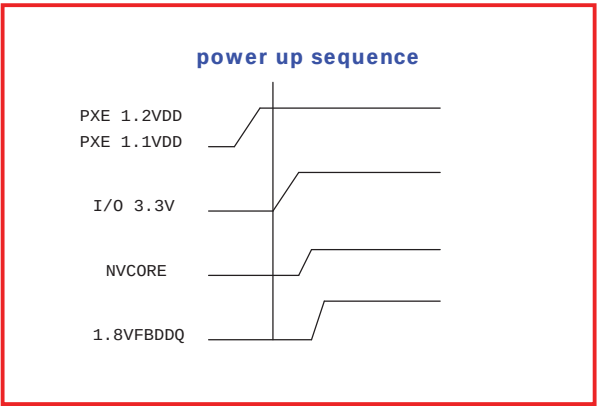
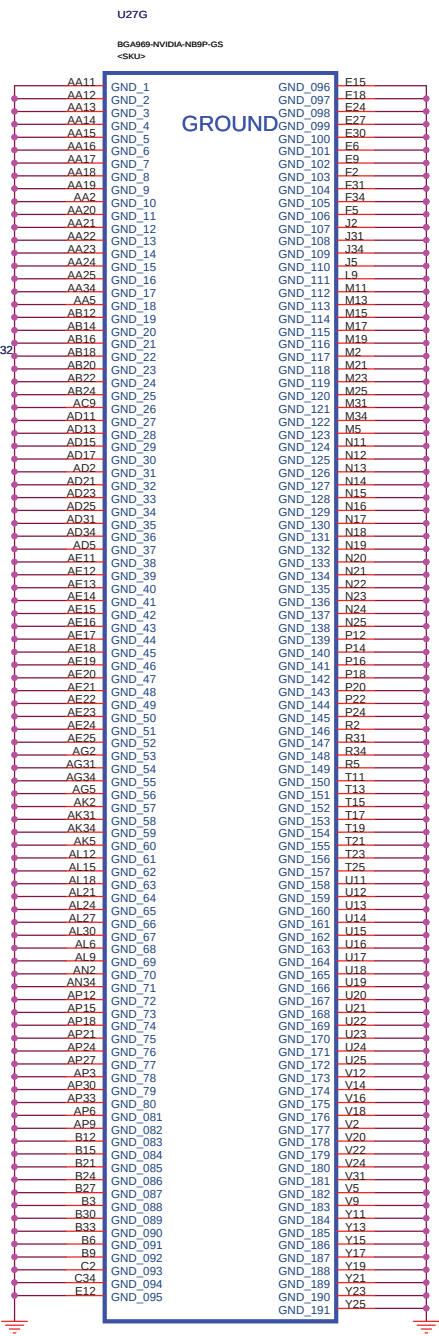
R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E



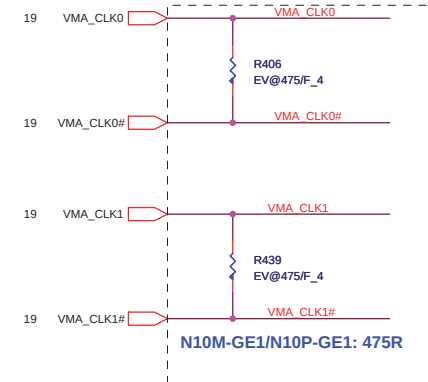
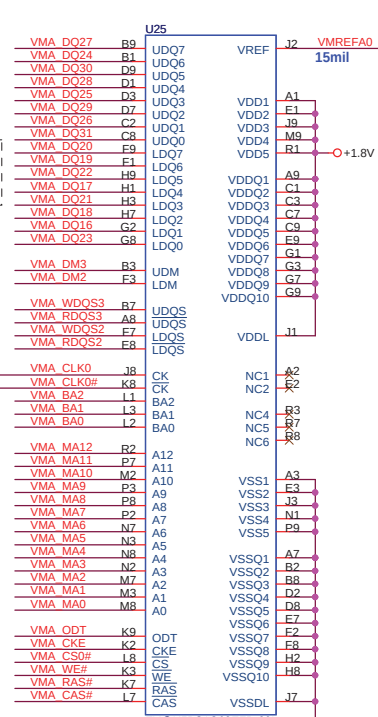
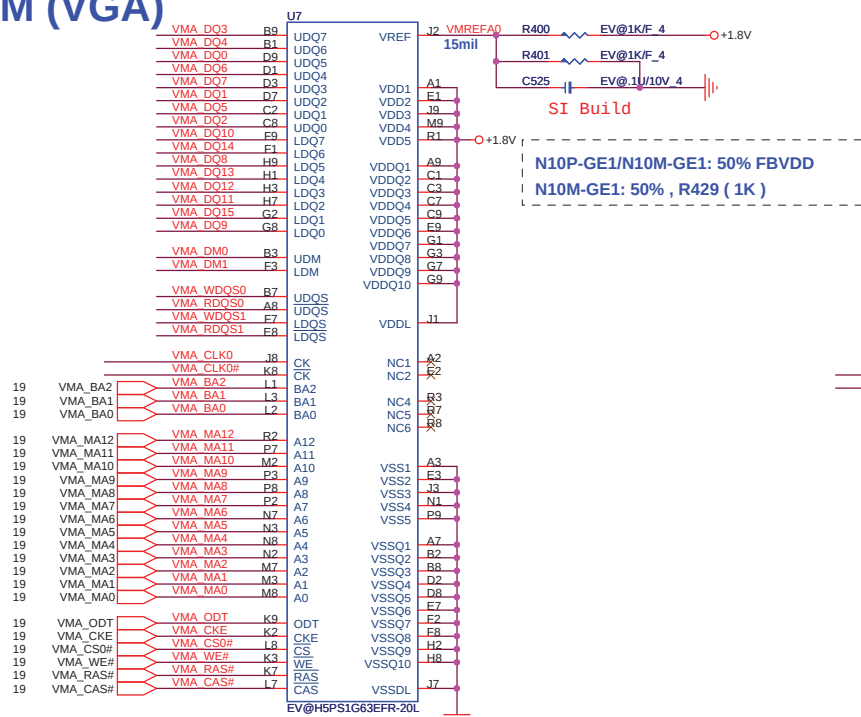
NVVDD Decoupling



Follow Design Guide DG-03276-001 4.7uFx3 and 0.22x10 uF instead of 0.1uF x10

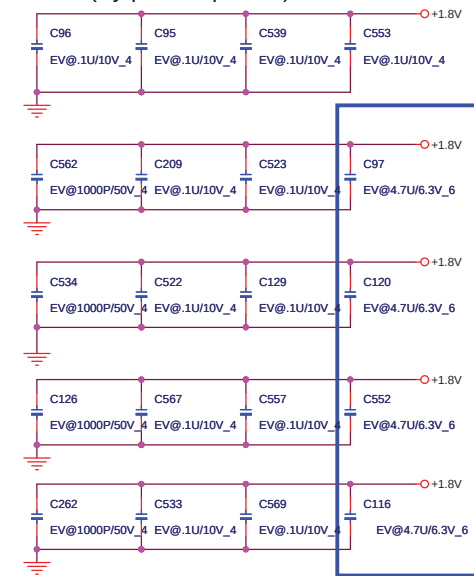


NV10M (VGA)

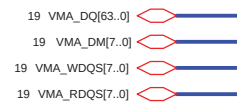


CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

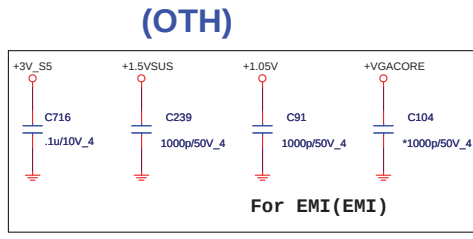
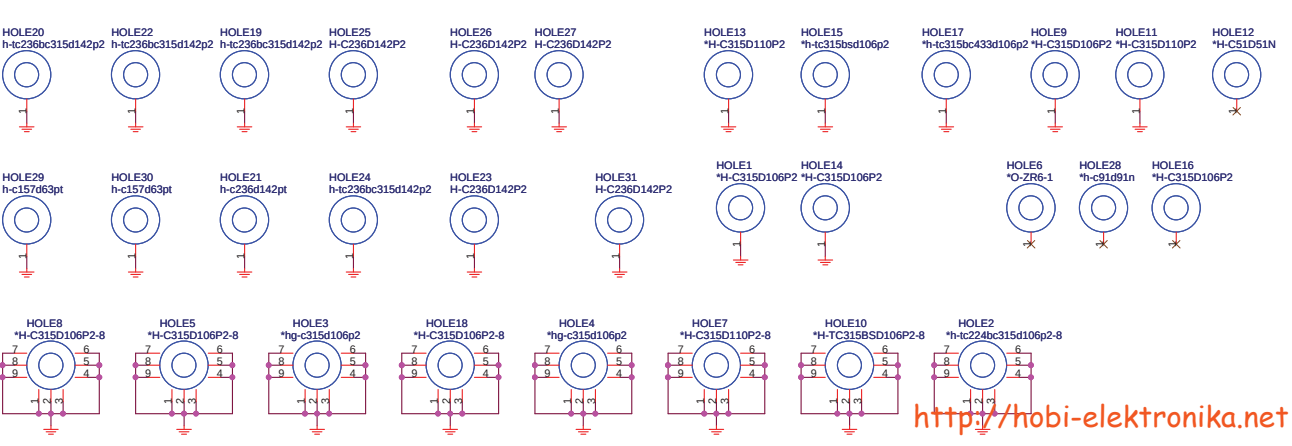
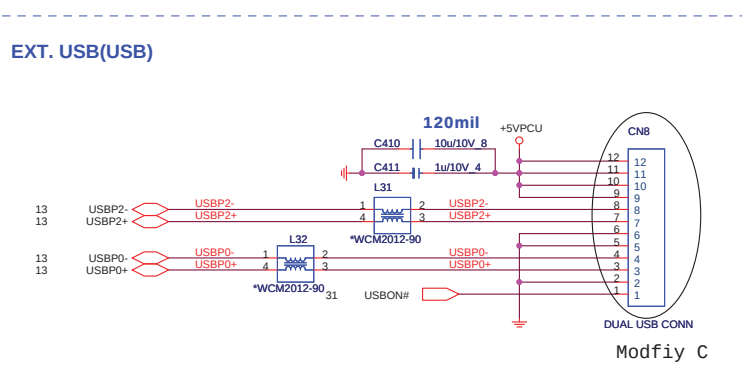
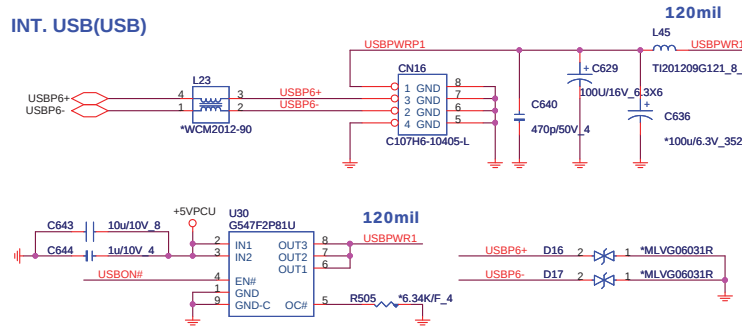
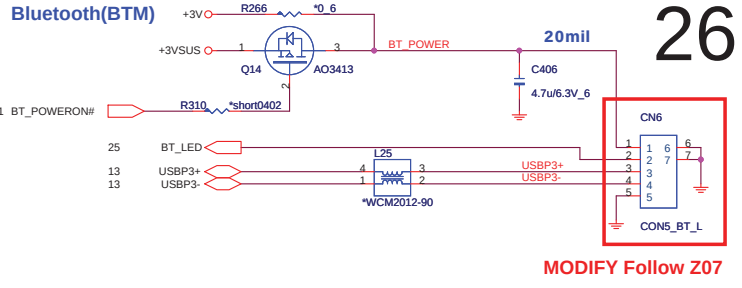
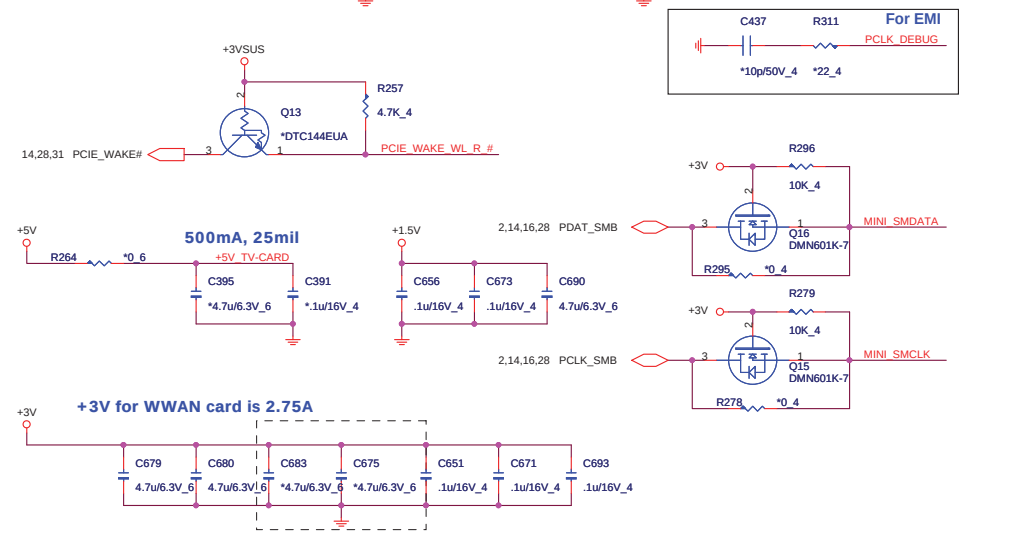
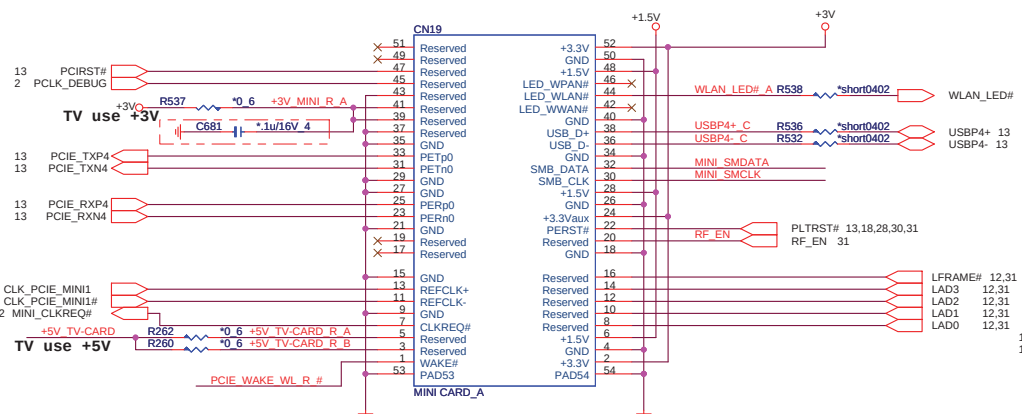
(By pass capacitor)



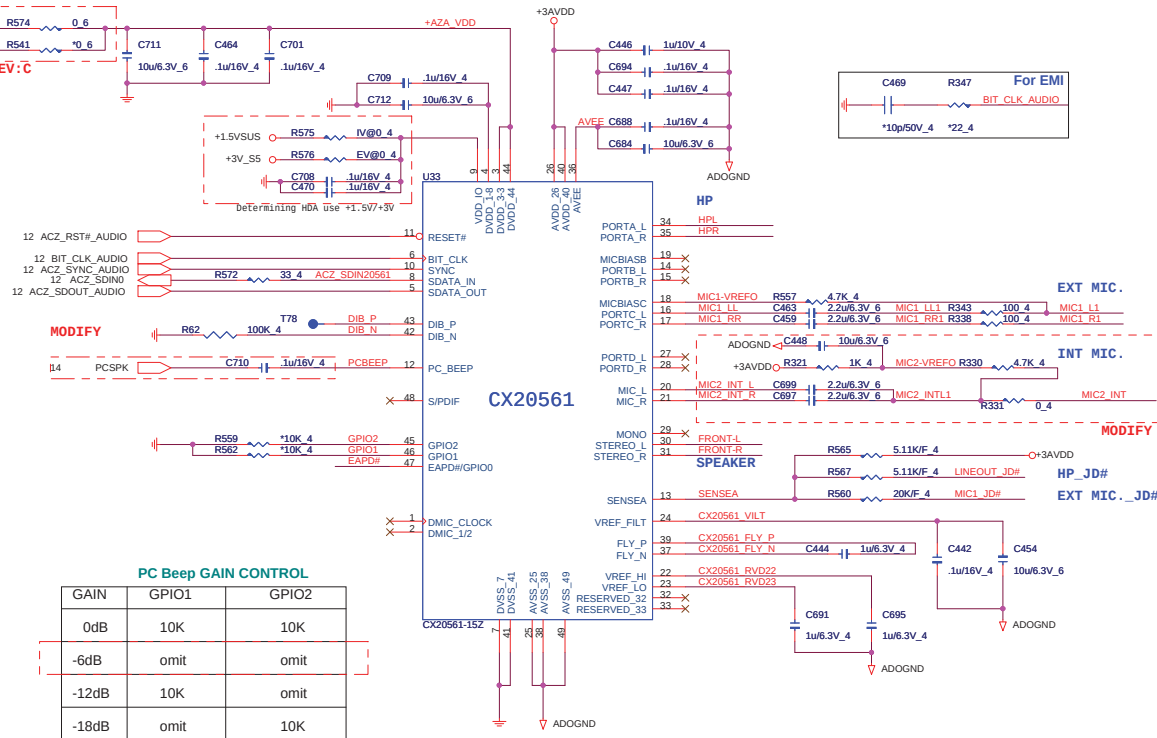
For DB:
 N10P/N10M : AKD5LG-T510(Samsung,64M*16)
 AKD5LG-TW02(Hynix,64M*16)


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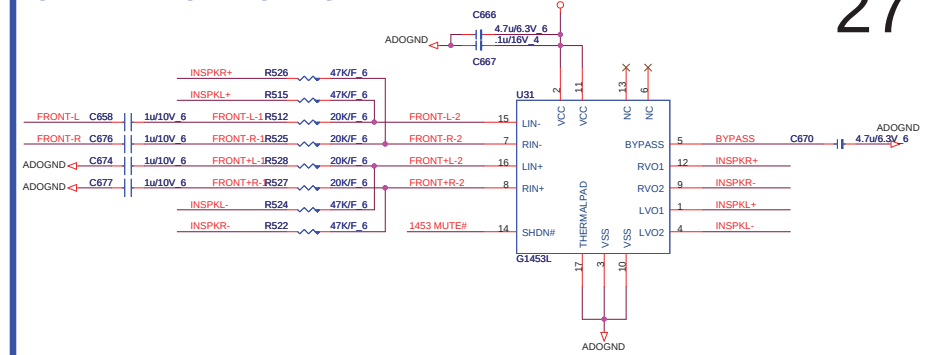
MINI-CARD(MPC)



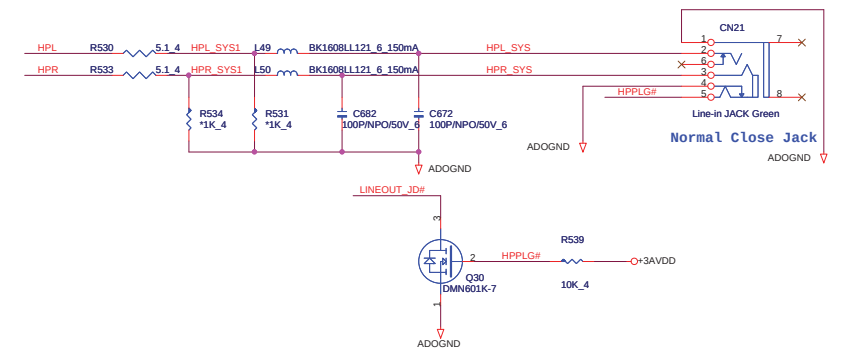
Codec CX20561-15Z (ADO) QFN



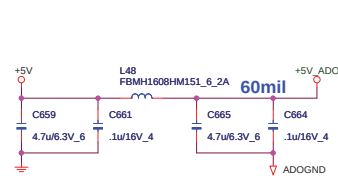
Speaker Amplifier(AMP)



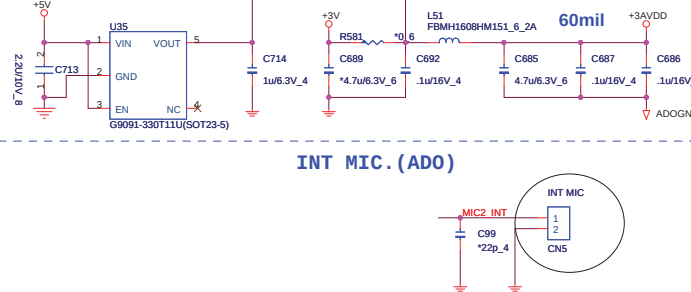
LINE OUT(AMP)



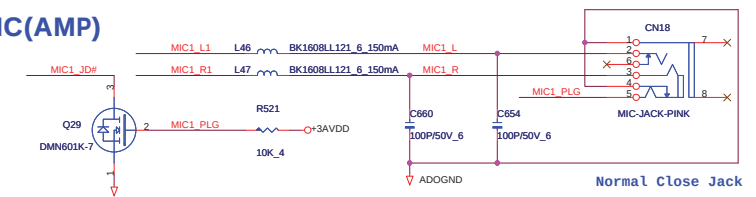
AMP Power(AMP)



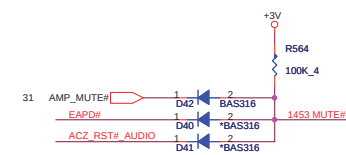
CODER Power(ADO)



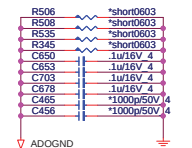
MIC(AMP)



MUTE(AMP)



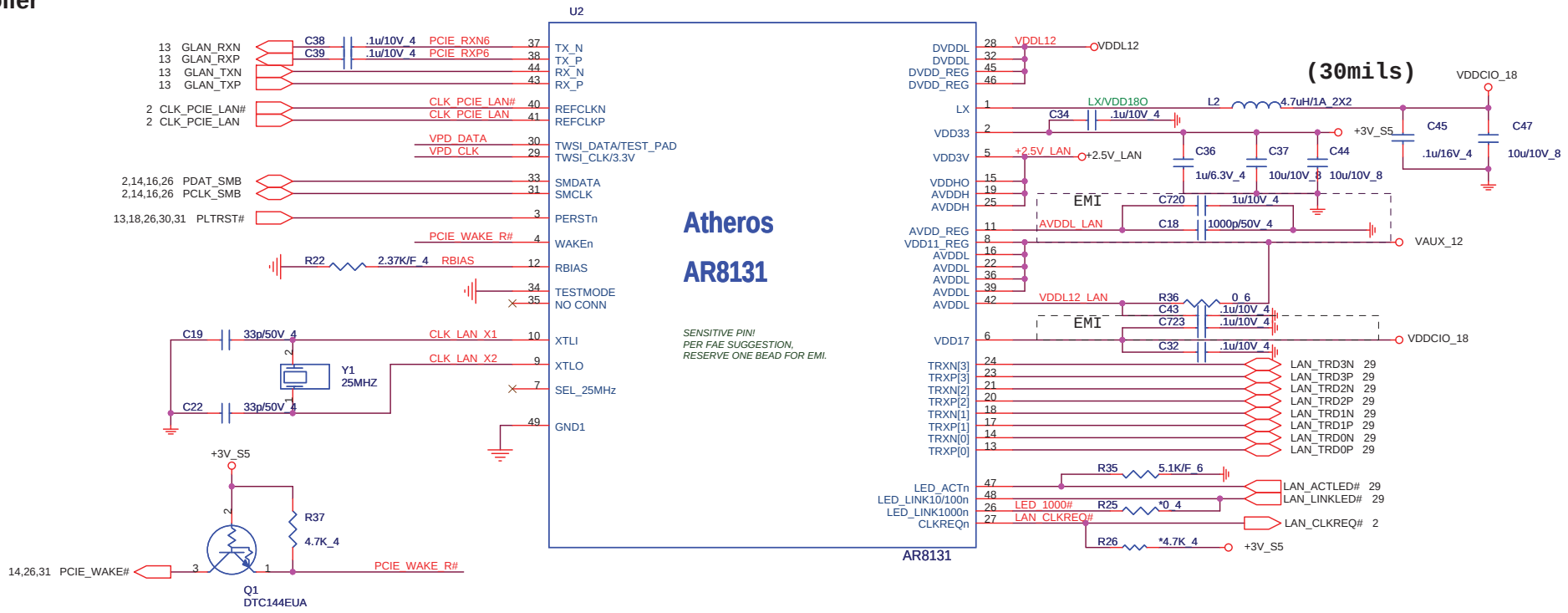
(ADO)



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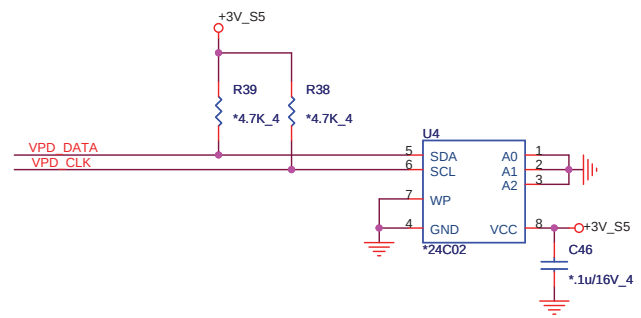
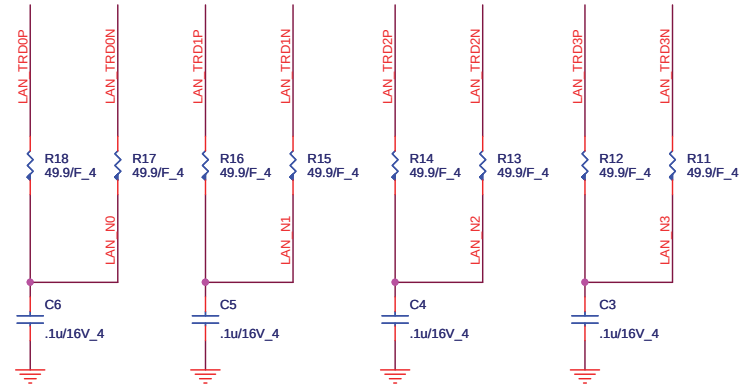
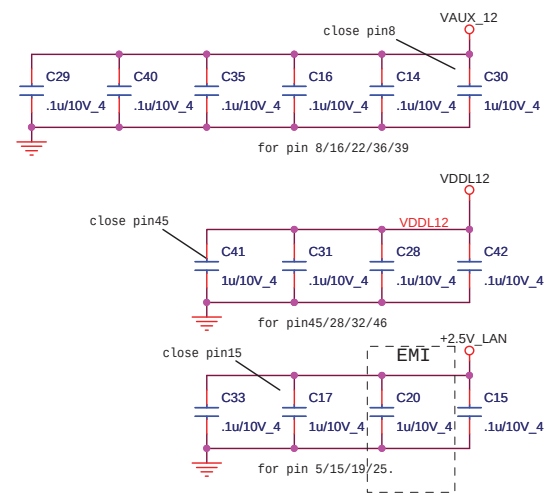
LAN Controller



Decoupling CAP

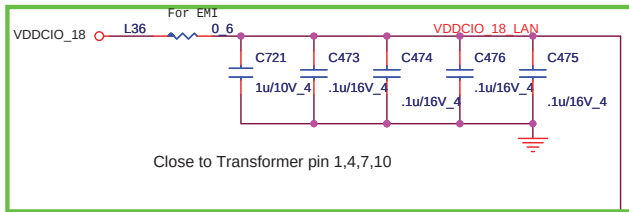
PLACE NEAR IC SIDE

EEPROM

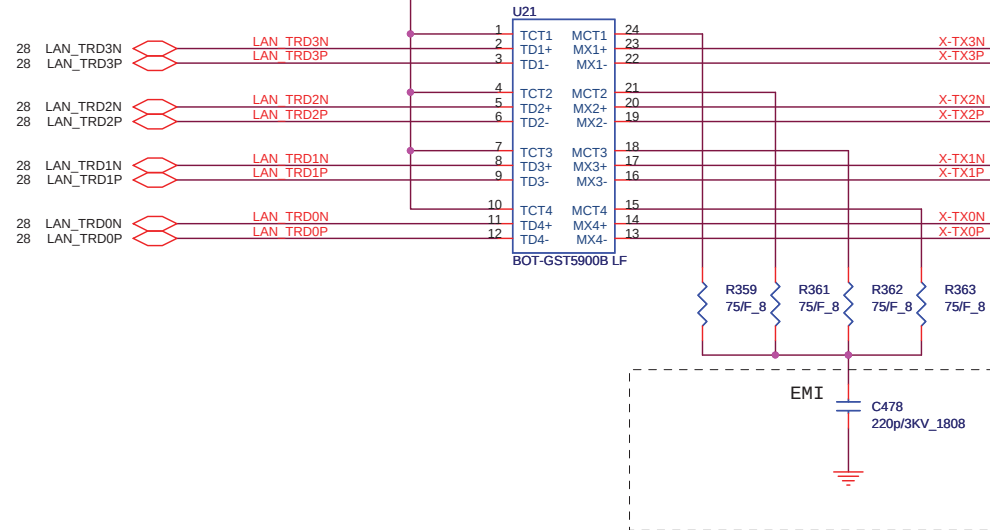


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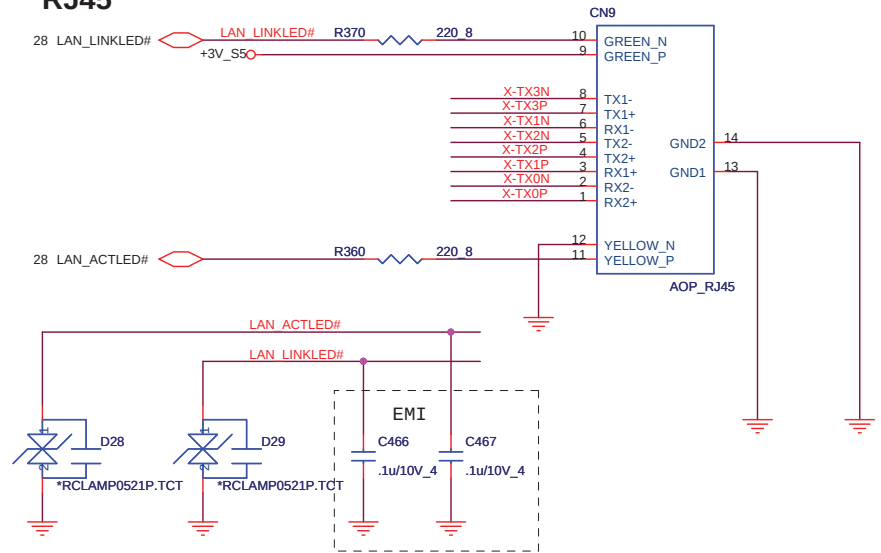
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		1A
AR8131 GLAN		
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TRANSFORMER



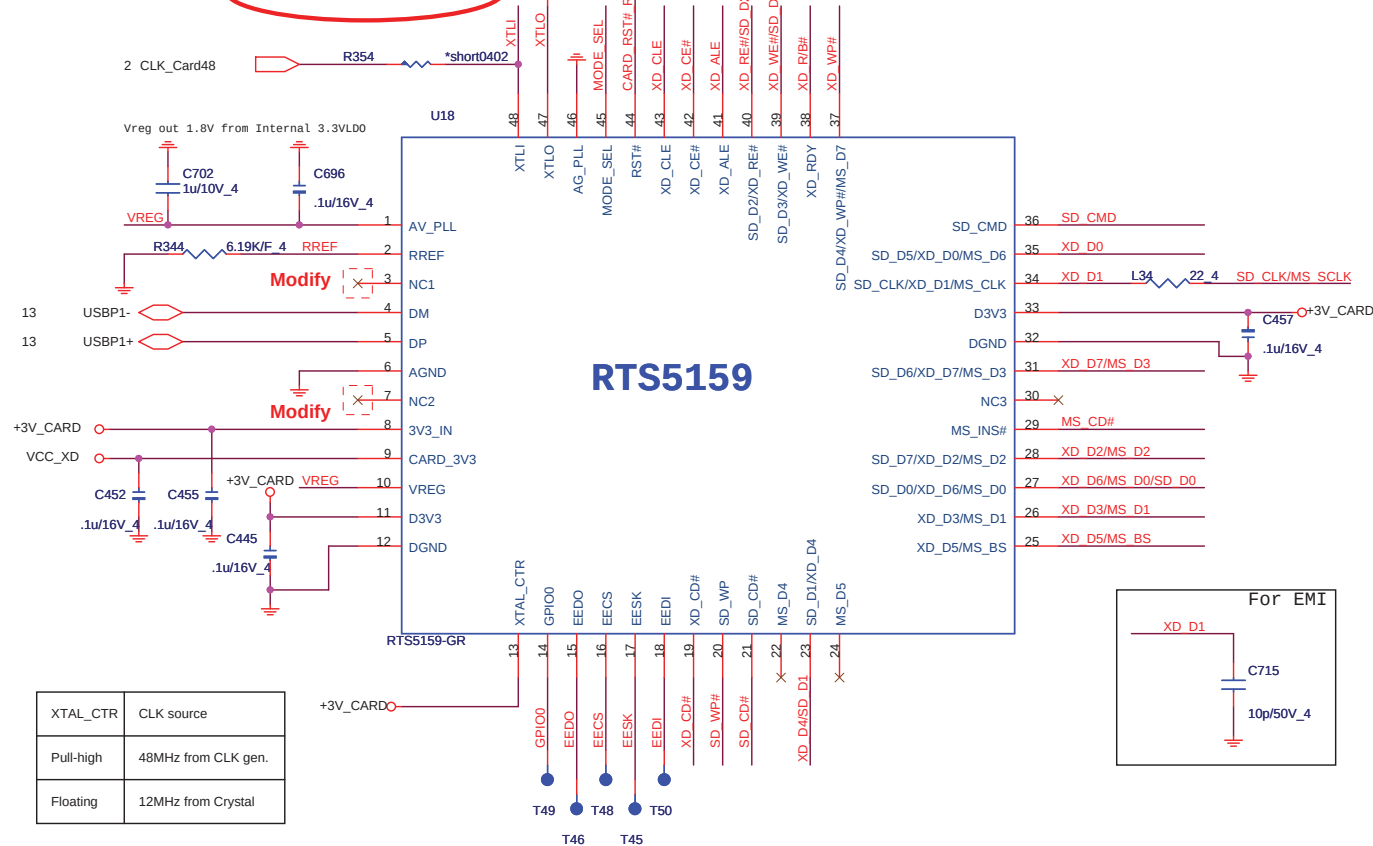
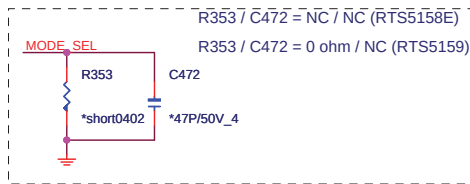
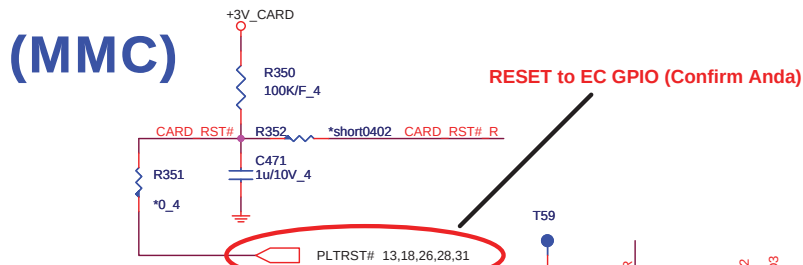
RJ45



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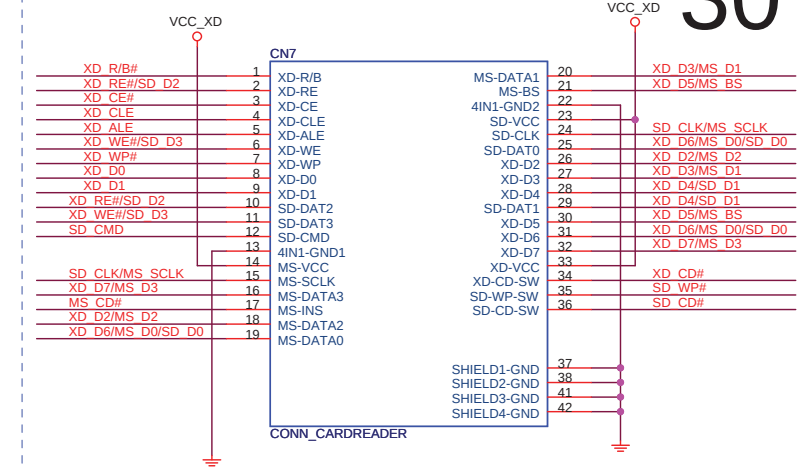
Size	Document Number	Rev
	LAN Transformer and RJ45/BT	1A
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(MMC)

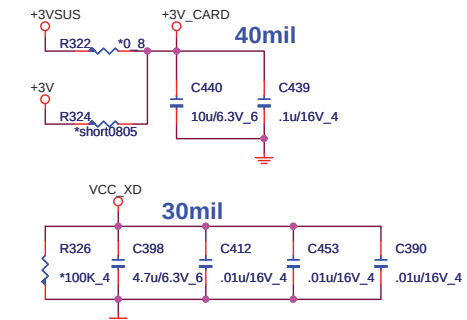


XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

4 IN 1 CARD READER



CARDREADER POWER

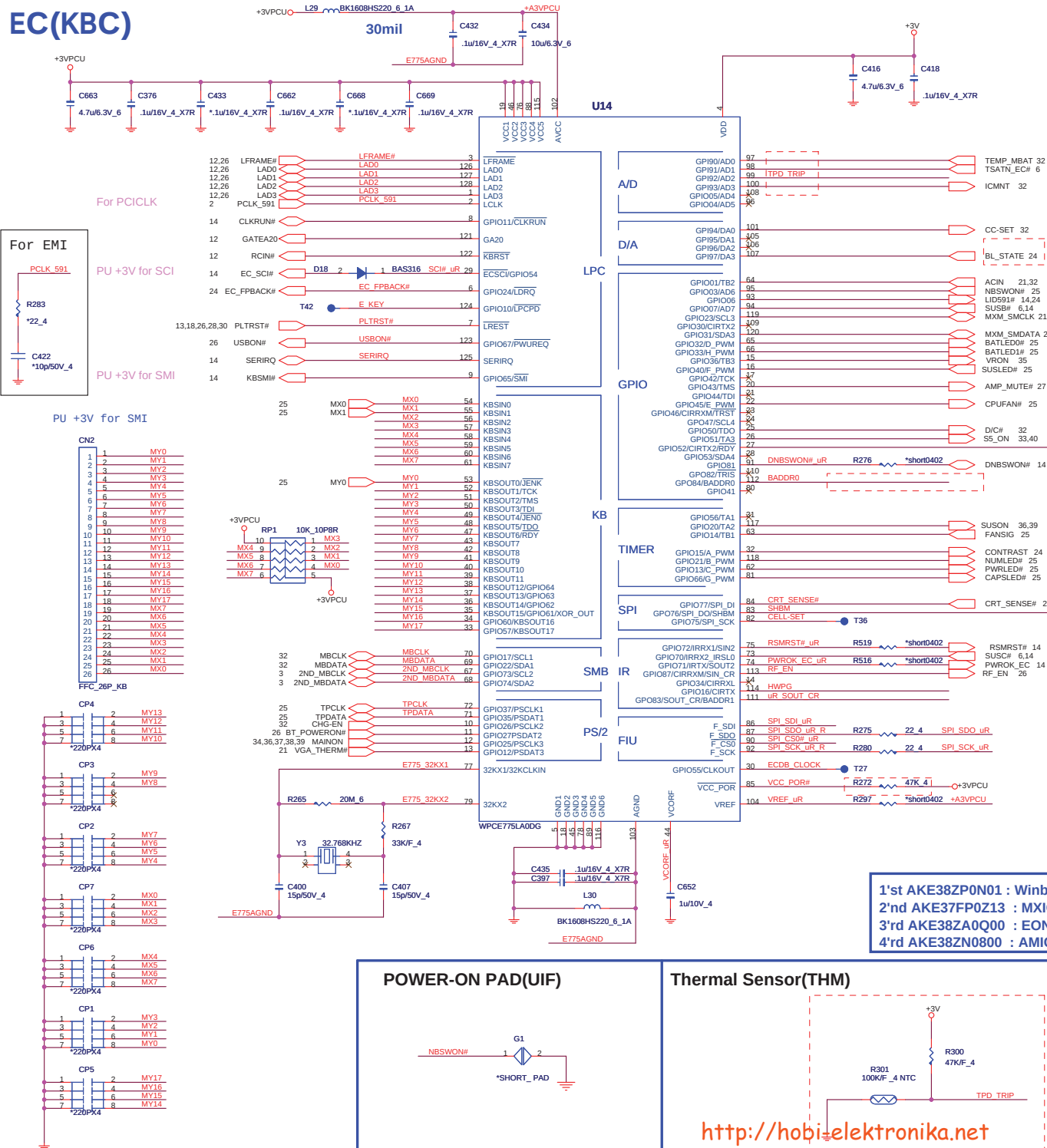




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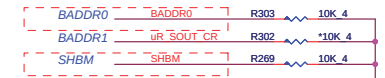
Size	Document Number	Rev
	CARD READER RTS5159	1A
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I/O ADDRESS SETTING

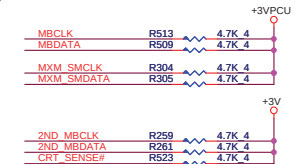
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

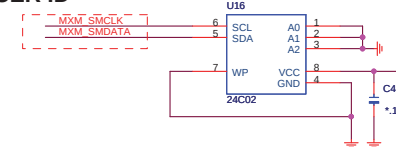


1/13 Confirm by vendor mail :
 Disabled (*) if using FW device on LPC.
 Enabled (0) if using SPI flash for both system BIOS and EC firmware

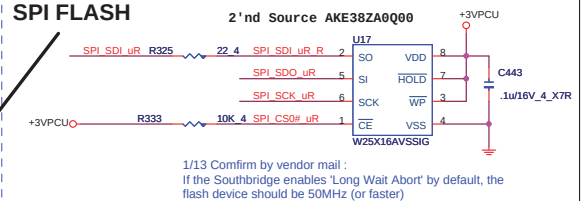
SM BUS PU



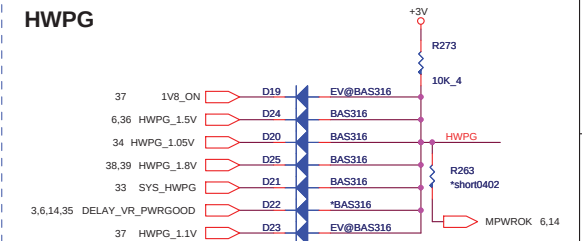
ACER ID



SPI FLASH



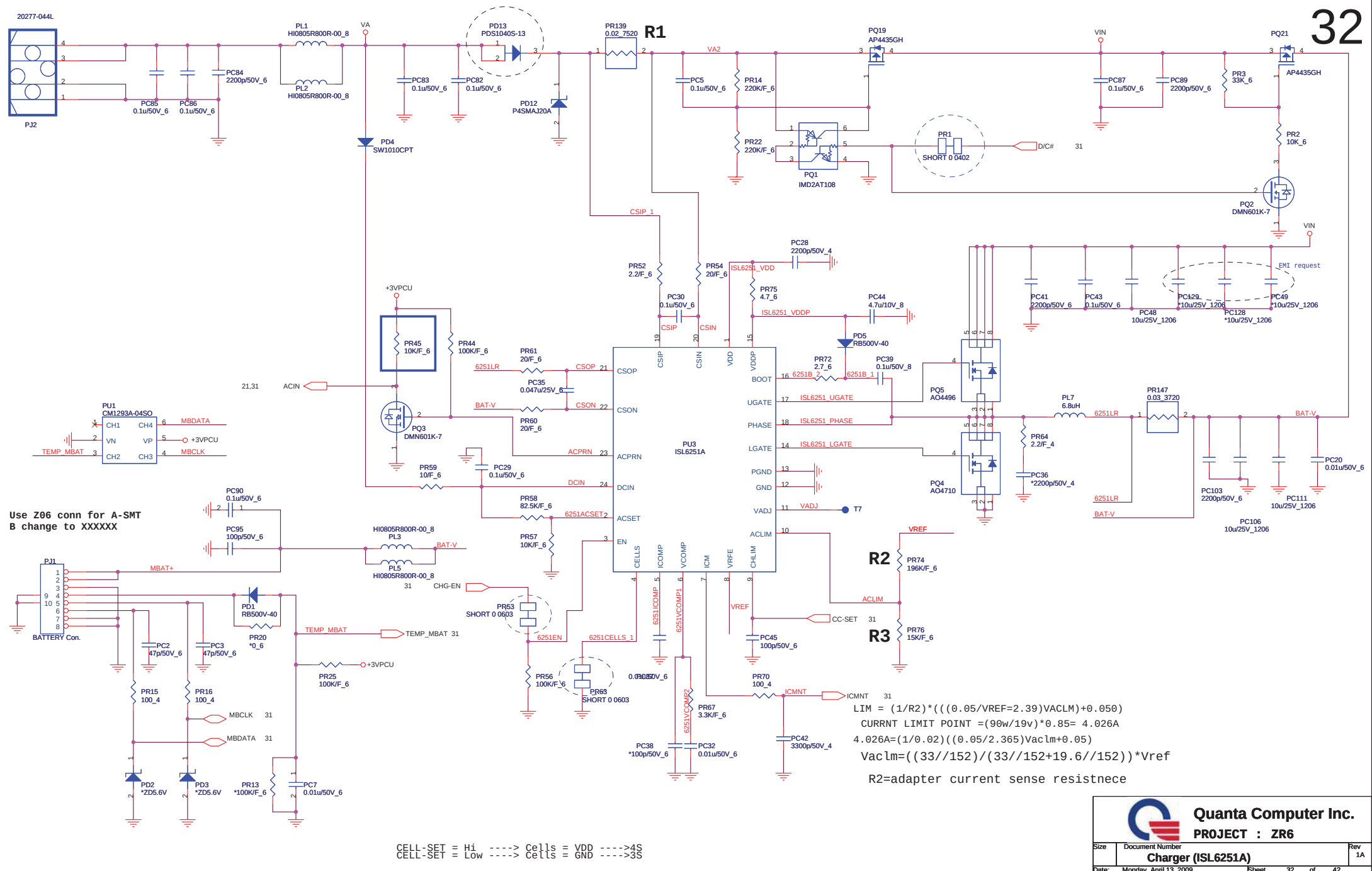
HWPG



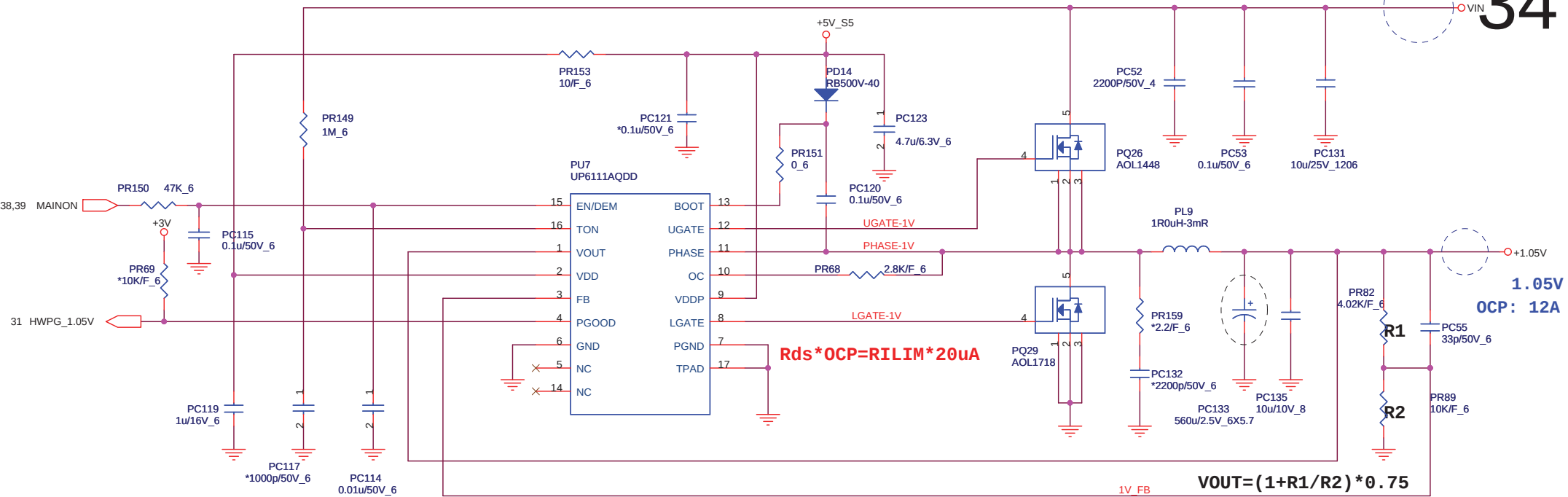
1'st AKE382P0N01 : Winbond W25X16AVSSIG
 2'nd AKE37FP0Z13 : MXIC MX25L1605AM2C-15G
 3'rd AKE382A0Q00 : EON EN25F16-100HIP
 4'rd AKE382N0800 : AMIC A25L016

INTERNAL KEYBOARD STRIP SET









$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

$$AOL1412 \quad R_{ds(on)} = 4.6m\Omega$$

$$OCP = 16 - 0.8A$$

$$L(\text{ripple current}) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \\ \sim 3.646A$$

$$4.6m * 12 = RILIM * 20uA$$

$$RILIM = 2.76K \text{ --- } 2.8K$$



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	VCCP 1.05V(UP6111A)	1A

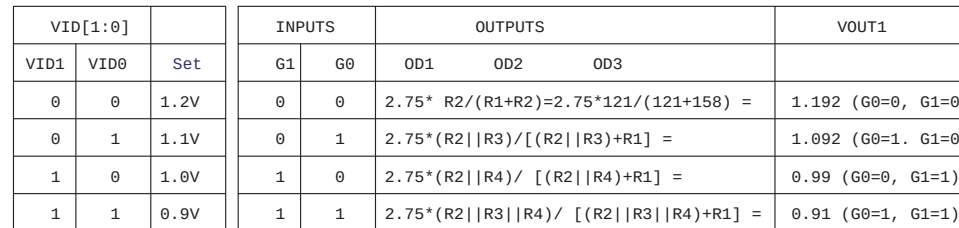
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$$OCP = 15.5 + 0.5A$$

4.6m*16=RILIM*10uA

RILIM=5.06K~5.1K

$$(10u \cdot PR154) / Rdson + \Delta I / 2 = I_{ocp}$$

38

OCP: 4A

2.73A

$$V_{OUT} = (1 + R1/R2) * 0.75$$

$$R_{ds} * OCP = R_{ILIM} * 20\mu A$$

$$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * T_{ON})$$

$$T_{ON} = 3.85p * 1M * 1 / (V_{in} - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

A04932 $R_{ds} = 15.6 \sim 19.6m\Omega$

OCP = 16 - 0.8A

$$L(\text{ripple current}) = (19 - 1.8) * 1.8 / (2.5u * 272k * 19) \sim 2.14A$$

$$19.6m * 4 = R_{ILIM} * 20\mu A$$

$$R_{ILIM} = 3.92K$$

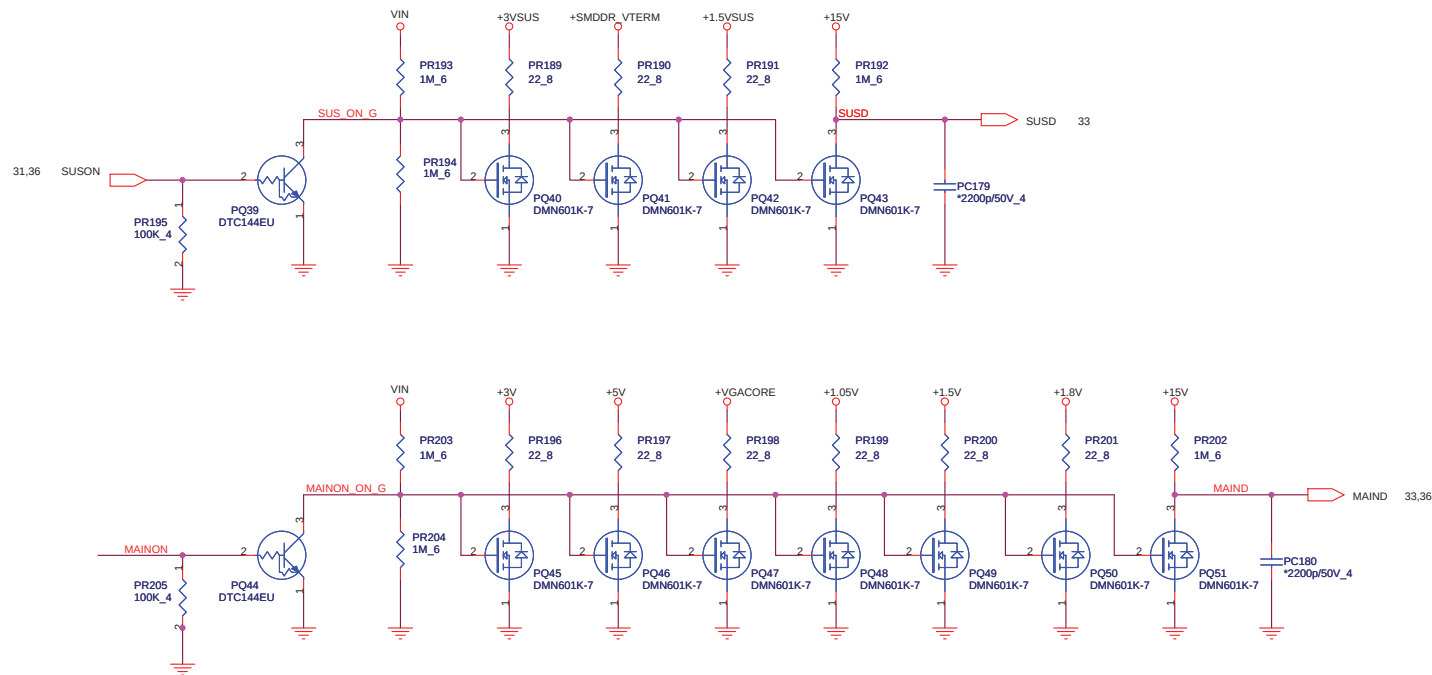
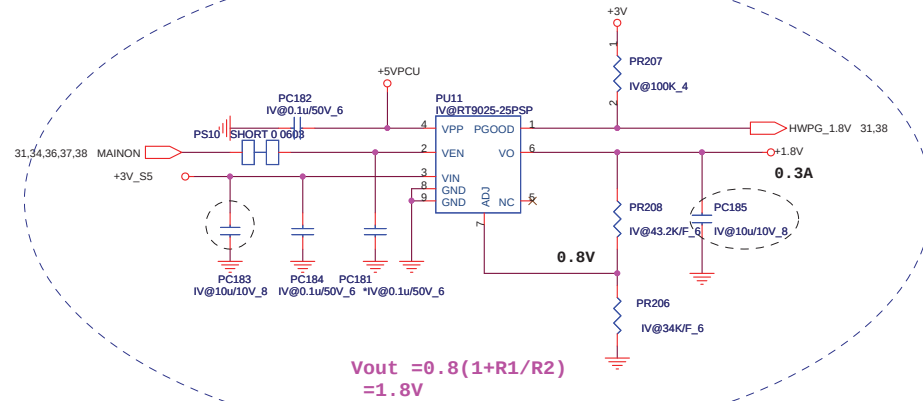


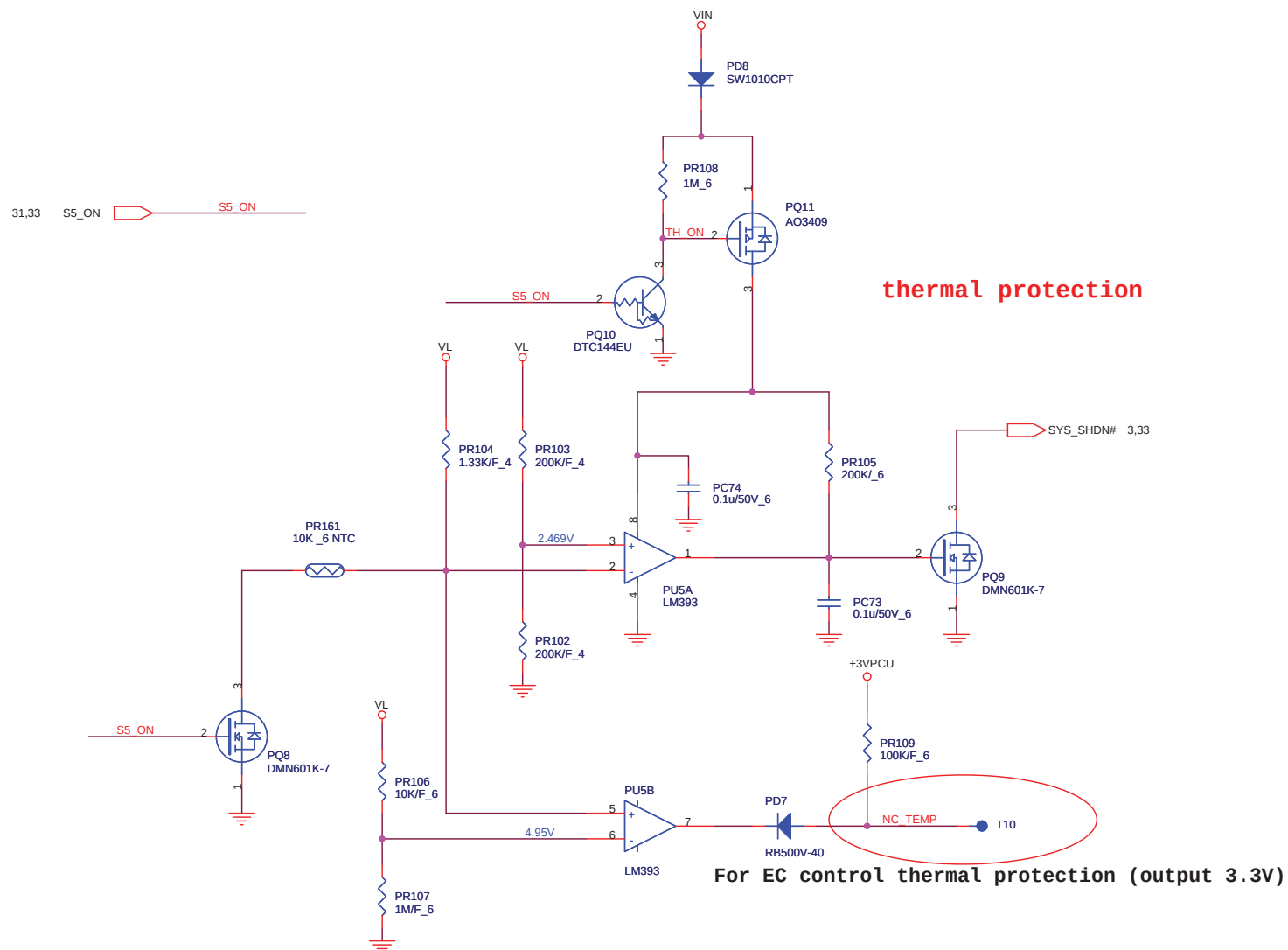
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	VCCP 1.8V(UP6111A)	1A

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		1A
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MODEL: REV		CHANGE LIST		MODEL	
				PAGE	ZR6 MB
				FROM	TO
ZR6 MB	A	First release			
	B	Page23:Change C209,C522,C567,C533 from CH31003MB14 to CH41002KB93			
	Page10:change net name +1.8VSUS_TXLVDS-->+1.5VSUS_TXLVDS,+1.8VSUS_VCC_SM_CK-->+1.5VSUS_VCC_SM_CK				
	Page24:change R174 from 100k to 470K,Del R177 to solve Hall sensor issue				
	Page25:U12 No stuff and Del R248 to no stuff				
	Page12:Change R543,R542,Q31 to no stuff,because ZR6 battery can't charging				
	Page21:VGA ID pin R387 stuff 15k,R382 stuff 45.3K,R414 stuff 25K,R381/R415 no stuff				
	Page14:MB ID pinR298 Value change to EV@,R308 Valule change to IV@				
	Page26:change L25 layout and del RN19 and change L23 layout and del RN14				
	Page24:change L1 layout and del RN1				
	Page24:Change LCD connector(OT2)				
	Page33:Mirror the PJ2 connector				
	Page26:change CN19 footprint to mipci800055fb052g100pl-52p-ldv as ZG5 and Del debug card 0 ohm R518,R517,R514,R511,R510,R315,R310				
	Page6:Change DD3 power OK circuit as ZK6				
	Page26:Del R520,R529 and change R538,R536,R532 footprint to short pad				
	Page24:U11 add pin 49 to thermal pad gnd				
	Page25:Change CN3 footprint to af712l-a2git-12p-l-zr6				
	Page32:Change CN2 footprint to 88502-260N-26P-L-ZR6				
	Page29:Change U21 footprint to trf-10-1-24p-zr6				
	Page27:Change U33 footprint to tqfn48-7x7-5-49p-zr6				
	Page26:Change CN8 footprint to bl123-10r-10p-l-zr6				
	Page25:Change D1、D2、D3 footprint to led-ht-110nb5-3p-zr6				
	Page27:Change CN18 Part Number to DFTJ06FR212 and Change CN21 Part Number to DFTJ06FR211				
	Page33:Change PJ1 Part Number to DFHD08MR064 for ZR6				
	Page17:Change C502 to no stuff for cost down				
	Page26:Change CN8 footprint to bl123-10r-10p-l-zr6& Partumber change to DFFC10FR017				
	Page2:Del RN15,RN36,RN18,RN22,RN20,RN24,RN23 for cost down &Change R252,R244,R499 to short pad				
	Page4:Change C58 to No stuff				
	Page29:change R366,R367,R357,R358 to short pad for cost down				
	Page27:change R506,R508,R535,R345 to short pad for cost down				
	Page24:Del R346,R7 for cost down				
	Page25:Del R218,R407 for cost down				
	Page26:change C683,C675 to no stuff				
	Page31:Add C715 for EMI				
	Page31:Del C466,C467,L35 for cost down				
	Page24:Add CN1 Pin33,Pin34 to GND ,Add R248,R218 for HDMI and Add L52,L53,L54,L55 for EMI				
	Page10:change L38 to R037				
	Page2:Add R511 for Mini_CLKREQ# pull up				
	Page40:change +3VSUS to +3V_S5,HWPG_1.5V to HWPG_1.8V				
	Page24:1.Del R248,R218,2.L19,L21 change to R218,R234,3.change D14,D15,R196,R197,R203,R200 vaule to stuff				
Page12:Change C450,C451 to 18P					
Page28:Change C19,C22 to 33P					
Page21:Add MXM ACIN circuit,R177R182,Q33,Q32,R183					
Page27:change R574 to no stuff and R541 to stuff					
Page24:Add D44 and Del R410					
Page28:change R39,R38,U4,C46 to no stuff					
Page18-23:change T65,T74,T11,T69,T68,T64,T67,T70,T73,T66,T72,T71 footprint to T3050					
Page26:Change C629 to 100uf and C636 to no stuff					
Page6:change R175 and R181 to 47K for HDMI vender request					
Page24:Change R197,R200 to EV@					
MB Assy' P/N: 31ZR6MB0000/10/20/30/40/50/60/70		Project ZR6 MB		Document No. :	
Approved by : Johnny_0		Drawing by :Andy Chen		DATE: 2009/03/04	



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MODEL: REV		CHANGE LIST	MODEL		
			ZR6 MB		
PAGE			FROM	TO	
ZR6 MB	B	Page6:change R175 and R181 to 4.7K for HDMI vender request	1	1A	
	C	Page10:change net name +1.5VSUS_TXLVDS--> +1.8V_TXLVDS	2	1A	
		Page3:Del Q5,Q6,R62,R63	3	1A	
		Page3:change Par Number from AL000780000 to AL000780003 for thermal sensor address change to 9AH	4	1A	
		Page21:Del Q10,Q9,R96,R86	5	2A	
		Page27:R574 stuff and R541 no stuff	6	1A	
		Page31:R300,R301 stuff thermal sensor	7	1A	
		Page37:change PC65,PC67 to 150pF	8	1A	
		Page28:change U2 PartNumber from AL008131001 to AL008131002(LAN chip)	9	3A	
		Page27:change R530,R533 from 10 ohm to 5.1 ohm for headphone	10	3A	
		Page27:change CN8 (usb) 12 pin board to board	11	1A	
		Page26:Change CN5 footprint to cwy027-b0g1z-2p-1,CN16(USB)footprint change to usb-c107h6-10405-1-4p-r-v-nb4	12	1A	
		Page30:Change CN7 footprint to 4IN1-R015-212-LM-42P-H-nb4	13	1A	
		Page32:PJ1 footprint change to bat-btj-08qn0b-8p-r-v-nb4	14	3A	
		Page32:Del R510,change Hole15 footprint from h-tc315bc433d106p2 to h-tc315bsd106p2	15	2A	
		Page04:change C493 to no stuff	16	1A	
		Page27:Del T77 and Add R62	17	3A	
		Page26:change Hole21 footprint to h-c236d142pt-8	18	2A	
		Page24:Change D1、D2、D3 footprint to led-ht-110nb5-3p	19	3A	
		Page24:Change R218,R234 to shortpad	20	1A	
		Page26:Change R310 to shortpad	21	3A	
		Page10:Change R91,R307,R418,R466,R469 to shortpad	22	1A	
		Page29:Add C466,C467 for EMI,Add R358,R357,R366,R367 and change DGND to LAN GND	23	3A	
		Page26:Add C716 for EMI	24	3A	
		Page30:Change L34 to 0 ohm and C715 to 10P,Change R512,R525,R528,R527 to 20K 1% and Change R526,R515,R524,R522 to 47K 1%	25	2A	
		Page25:Change R1,R4,R10,R365,R369,R368 to 221 ohm and Change D1,D2,D3 part number	26	3A	
		Page14:Change R282 to no stuff	27	2A	
		Page28:Change R26 to no stuff	28	3A	
		Page26:Change Hole29 part number to MBZR6005010	29	3A	
		Page29:Del net name LAN_LNK_LED_PWR	30	1A	
		D	Page14:Add R583 and R315 at GPIO7 for HDMI option,change R583 to no stuff and R315 to stuff	31	3A
			Page24:change HDMI item to no stuff(remove this function)	32	2A
			Page12:change R225,R216,R241,R220,R219,R215,R213,R214,R228,R227 to no stuff for remove HDMI Audio	33	2A
			Page26:Change Hole 16 footprint as hole1	34	2A
				35	2A
				36	2A
				37	2A
		E	Page37:change PR97,PR98 to short-pad ,change PU4 0Z8116 change to 0Z8111 for cost issue ,Del PC62	38	2A
			Page27:C670 change value from 1U to 4.7U (CH5471M9907)	39	3A
			Page29:change c478 from 1000p to 220p.(CH122GK1I10)	40	3B
			Page28:change C18 from 0.1u to 1000p (CH21006JB10),change C20 from 0.1u to 1u (CH5102K9B06) ,ADD C723 0.1u (CH41002KB93) ,ADD C720 1u (CH5102K9B06)		
	Page25:change DHP00DA1G03->DHPTME53201				
	Page24:add C722 (CH6101M9905) to solve ISN issue				
	Page27:the PC beep will change Gain from -6db to -18 db , so R559 needs stuff 10k on all BOM.				
	Page34:change PC133 from CC7560JMZ15 to CC7560JMZ02 for cost down				
	Page36:change PC139 from CC7560JMZ15 to CC7560JMZ02 for cost down				
	Page38:change PC156 from CC7560JMZ15 to CC7560JMZ02 for cost down				
	Page33:change PC158,PC162 from CC73301MZB2 to CC73301MZ04 for cost down				
	Page37:change PQ6,PQ7 from BAM700200F6 to BAM601K0003 for cost down				
	MB Assy' P/N: 31ZR6MB0000/10/20/30/40/50/60/70		Project :ZR6 MB	Document No.:	
Approved by : Johnny_0		Drawing by :Andy Chen	DATE: 2009/03/04		



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