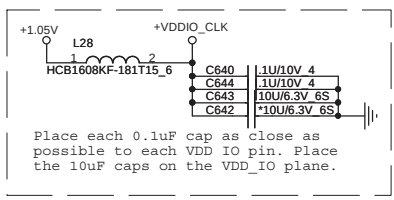
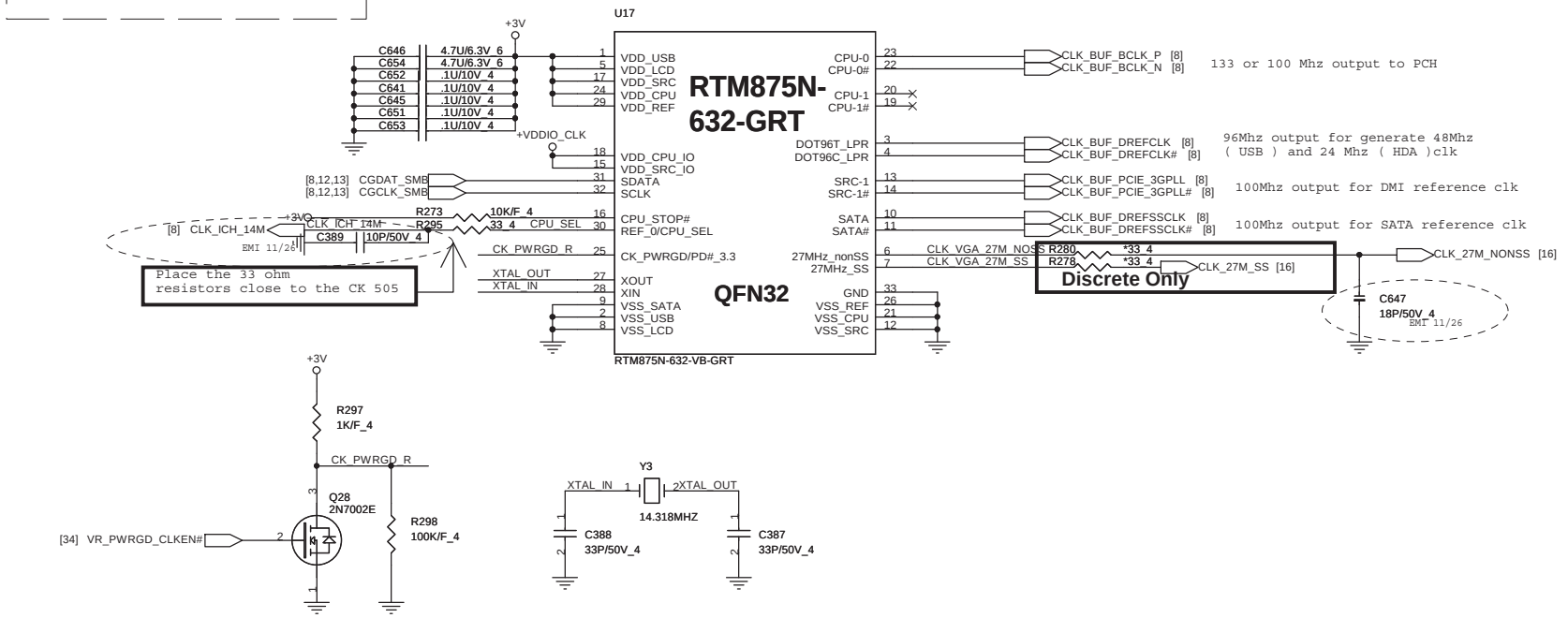


	PROJECT : SW9 Quanta Computer Inc.		
	Size Custom	Document Number Block Diagram	Rev 1A
	Date: Wednesday, December 02, 2009 Sheet 1 of 44		

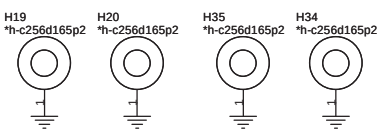


CLOCK GENERATOR

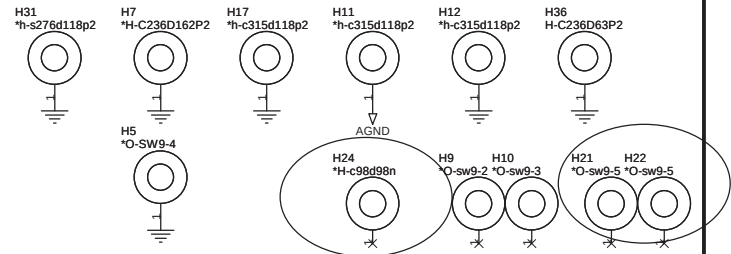


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

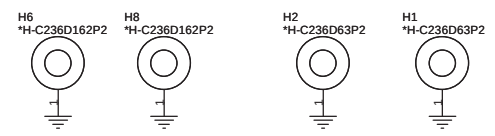
CPU bracket Hole.



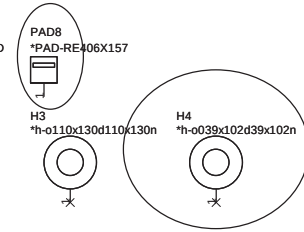
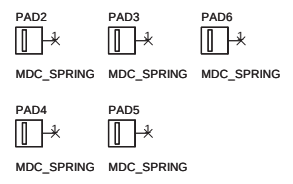
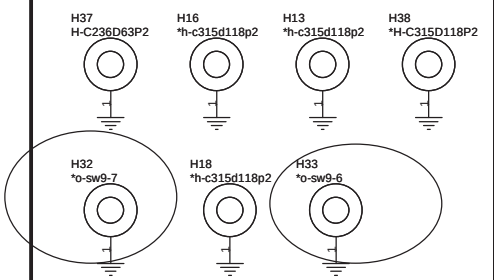
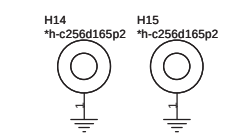
PAD and HOLE



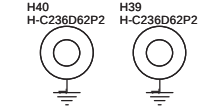
MINI CARD Hole.



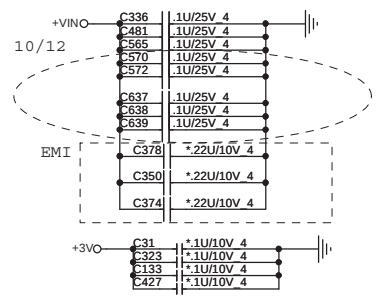
VGA bracket Hole.



MDC Hole.



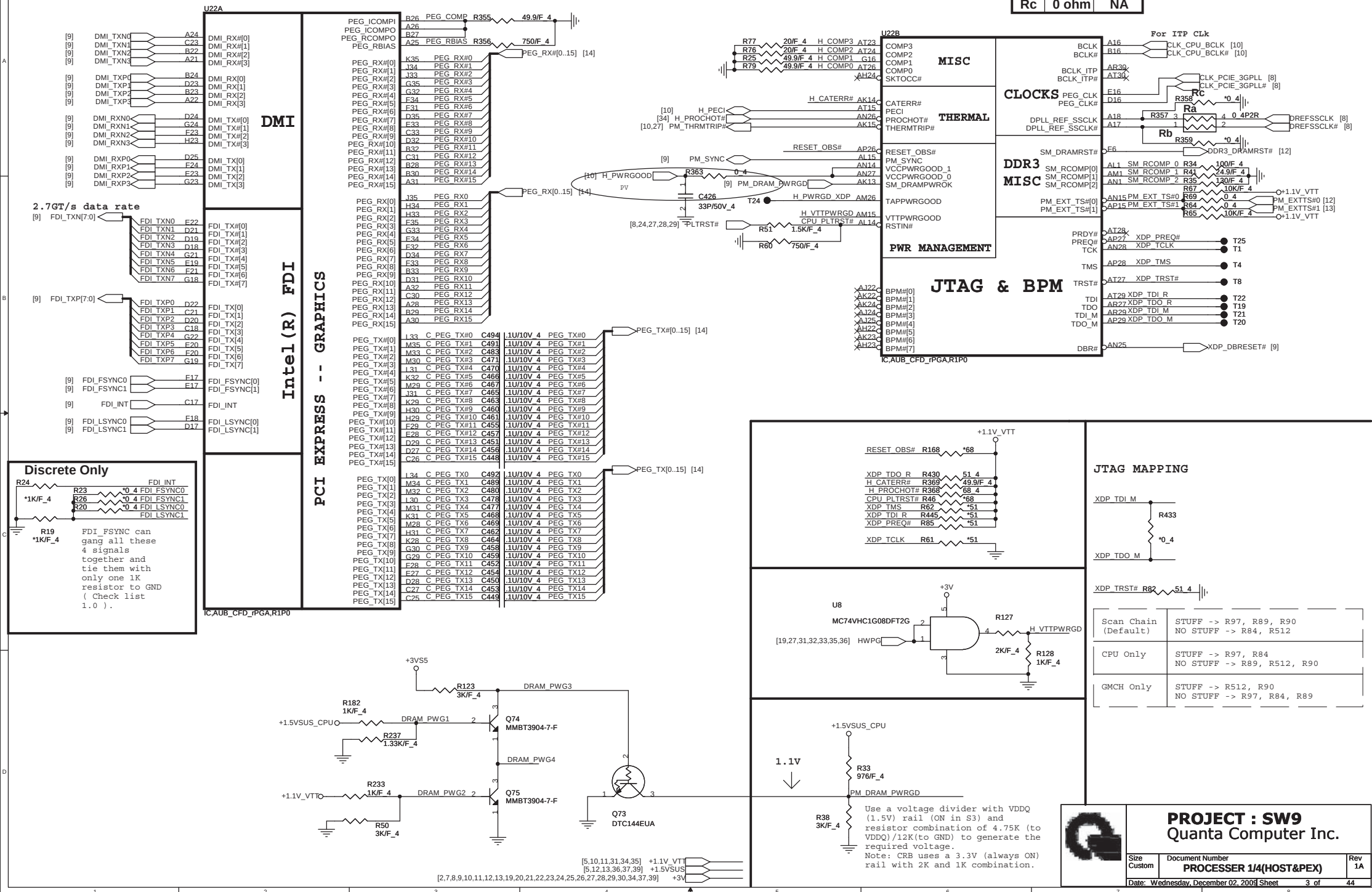
EMI capacitive



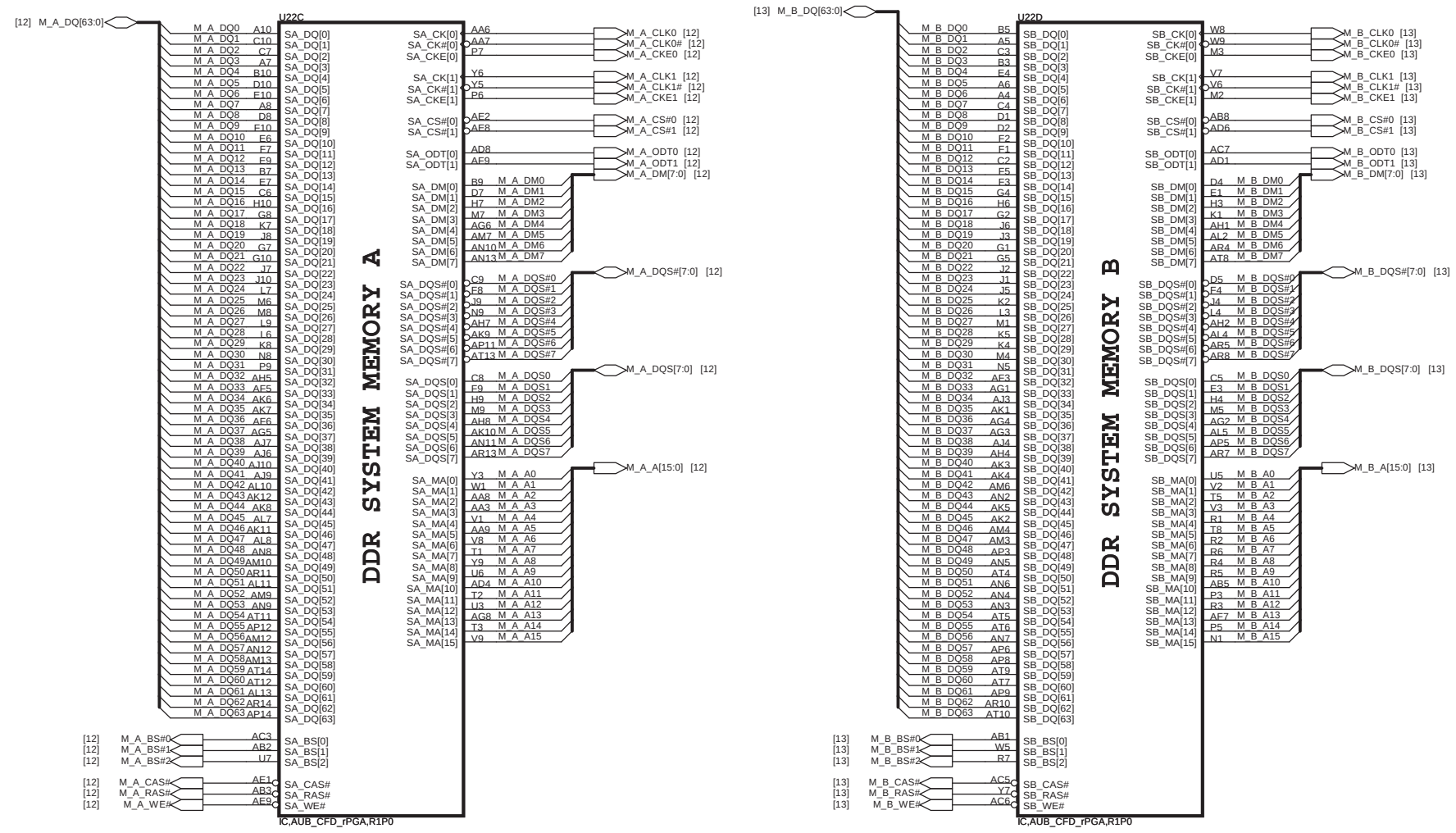
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK & Screw Holes	1A
Date: Wednesday, December 02, 2009 Sheet		2 of 44

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



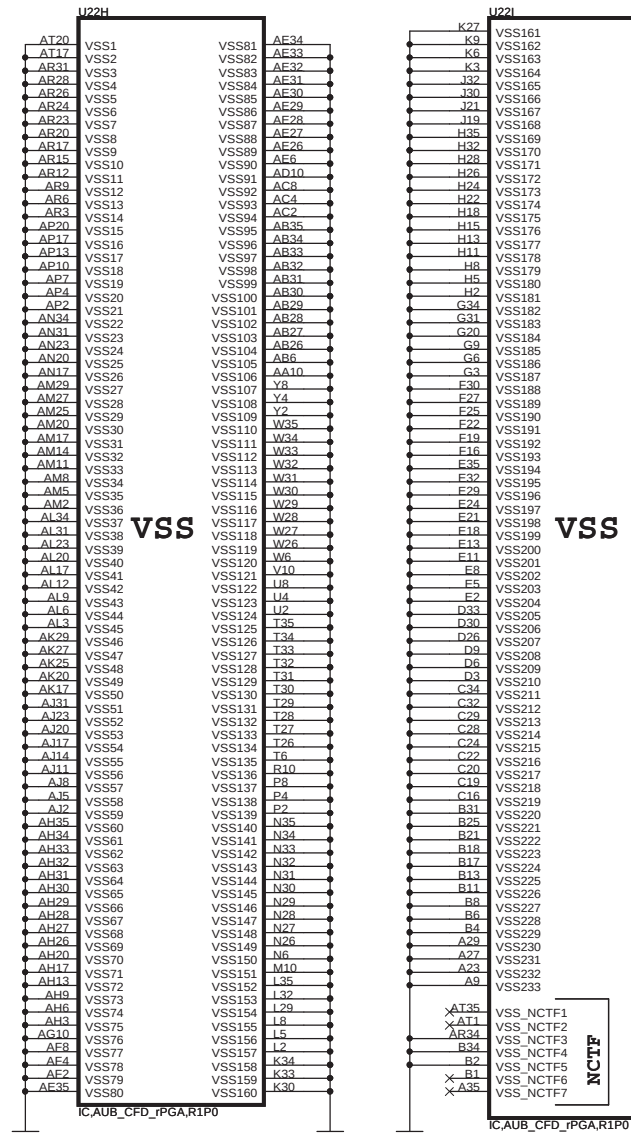


PROJECT : SW9
Quanta Computer Inc.

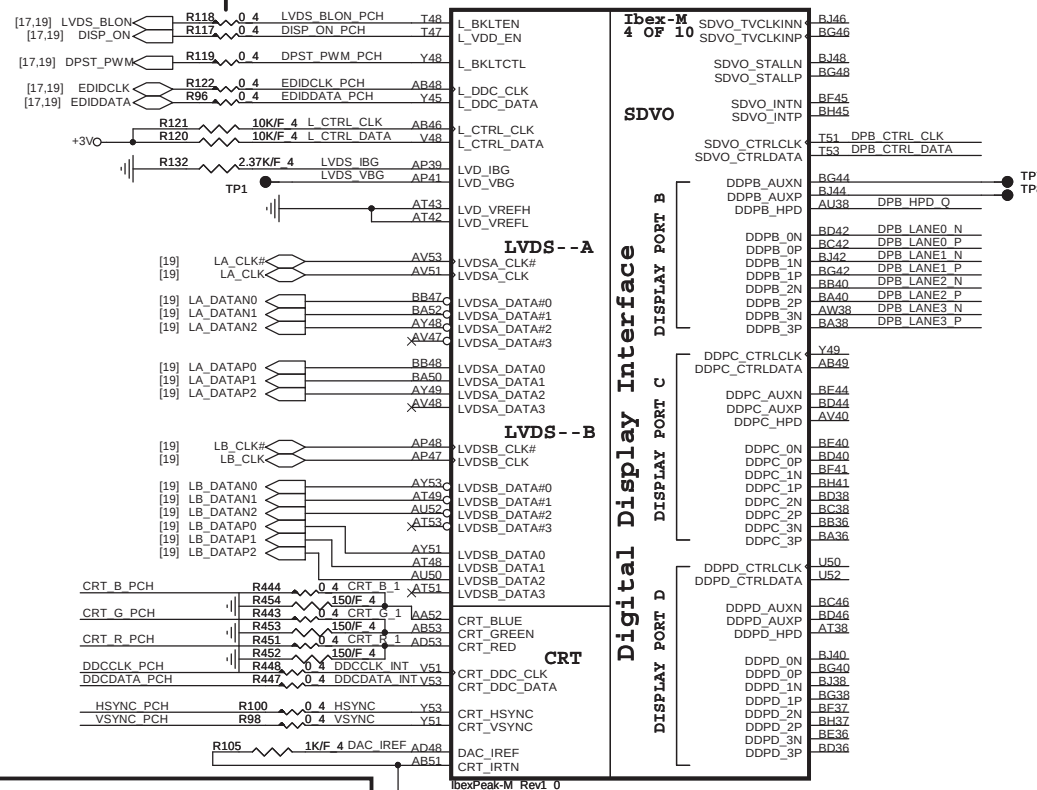
Size Custom	Document Number PROCESSER 3/4(POWER)	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 5 of 44		

AUBURNDAL/CLARKSFIELD PROCESSOR (GND)

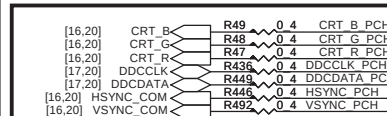
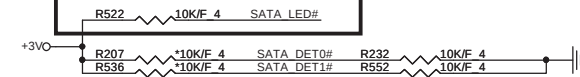
AUBURNDAL/CLARKSFIELD PROCESSOR(RESERVED, CFG)



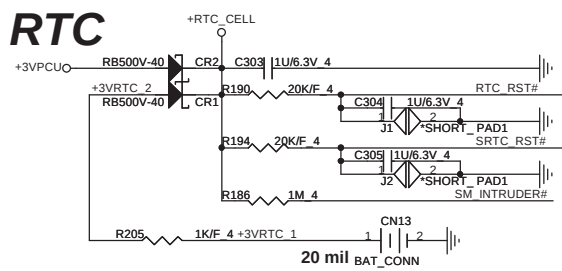
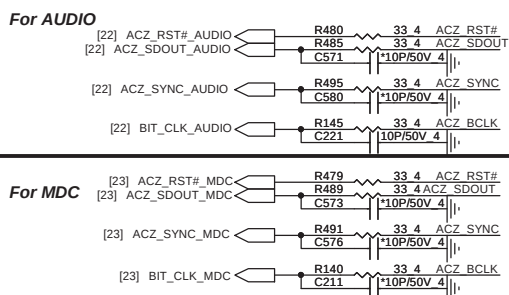
IBEX PEAK-M (LVDS,DDI)



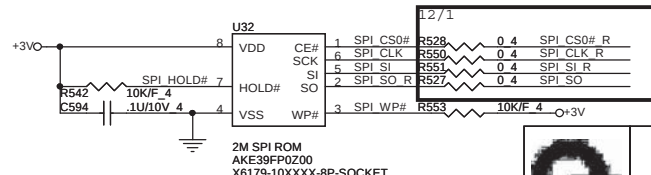
1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.



UMA only



2M byte SPI ROM for ME



4M byte SPI ROM for ME
MXIC AKE39FP0Z00

2M byte SPI ROM for ME
MXIC: AKE38FP0Z00

WINBOND: AKE38FP0N0
AIT: AKE38ZN0800

SPI ROM Socket
DG008000031

PROJECT - SW

PROJECT : SW

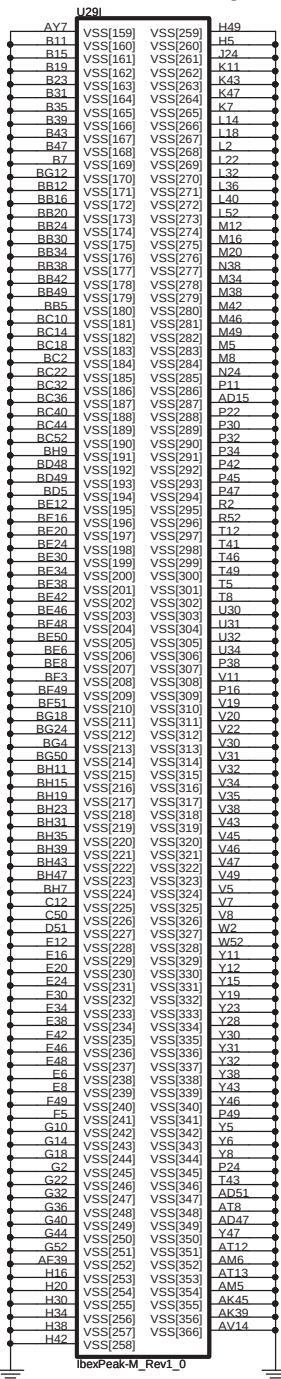
Quanta Comput

Document Number

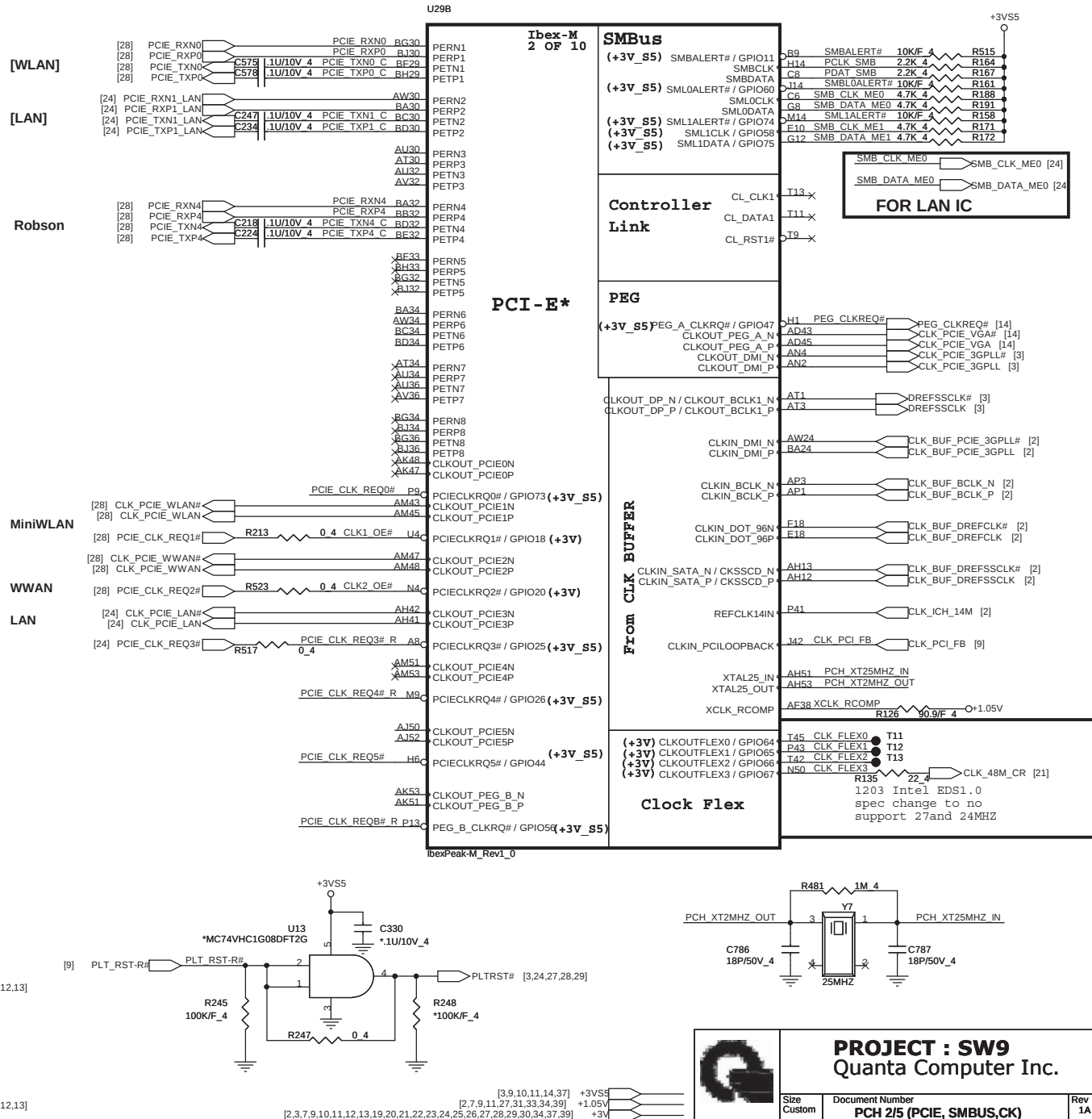
PCH 1/5 (SATA,HDA,LP	
----------------------	--

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		8

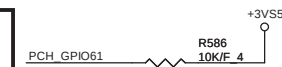
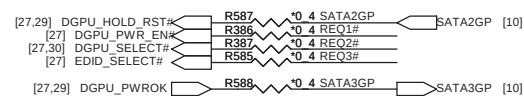
IBEX PEAK-M (GND)



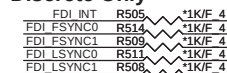
IBEX PEAK-M (PCI-E, SMBUS, CLK)



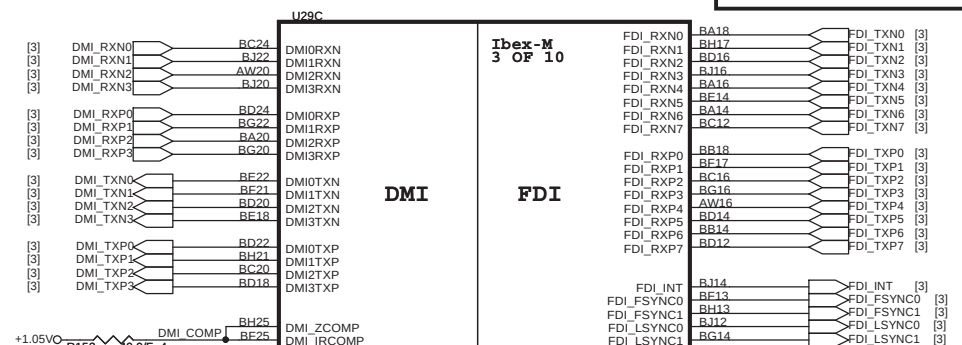
For Switchable only



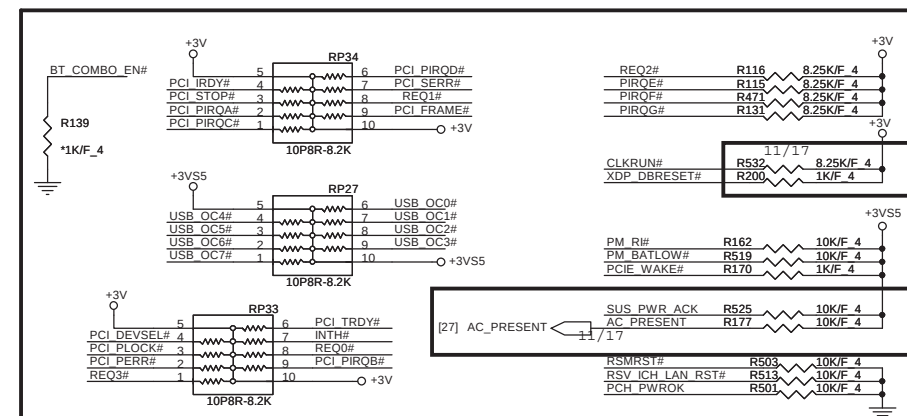
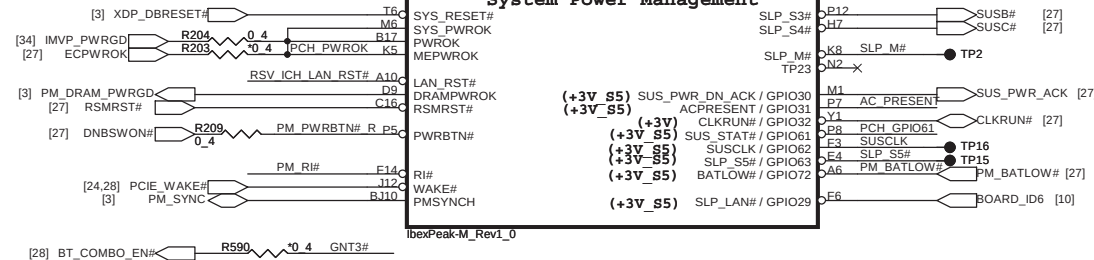
Discrete Only



IBEX PEAK-M (DMI,FDI,GPIO)

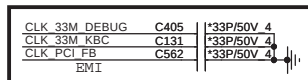
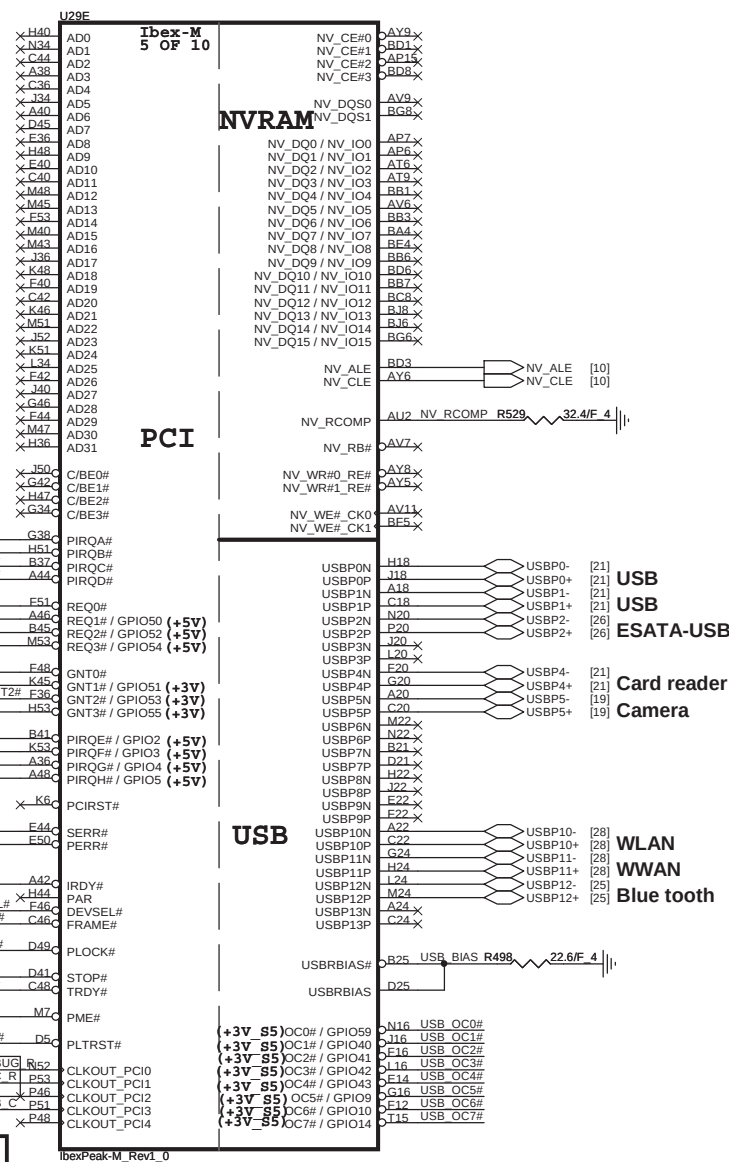
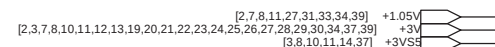


System Power Management



PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number PCH 3/5(PCI,ONFI,USB,DMI)	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 9 of 44		

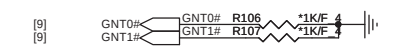
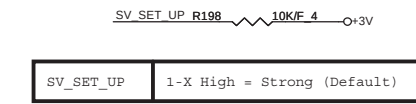
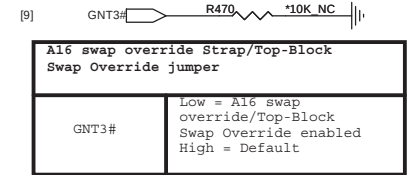
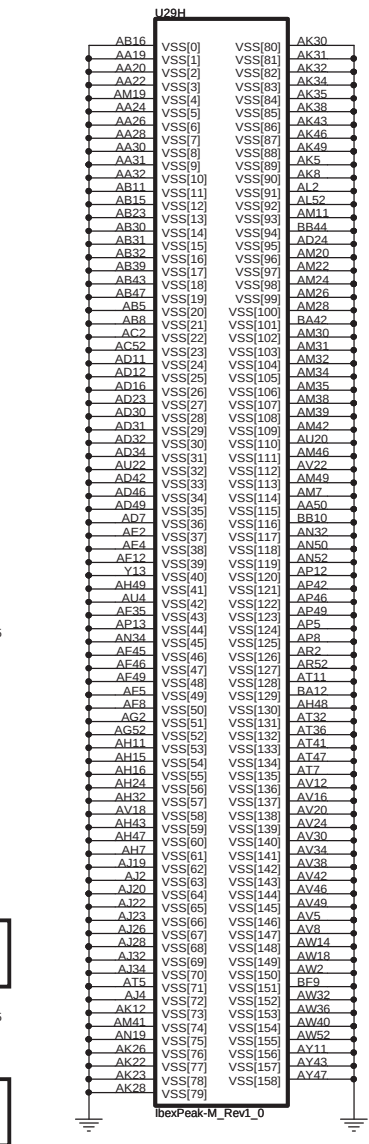
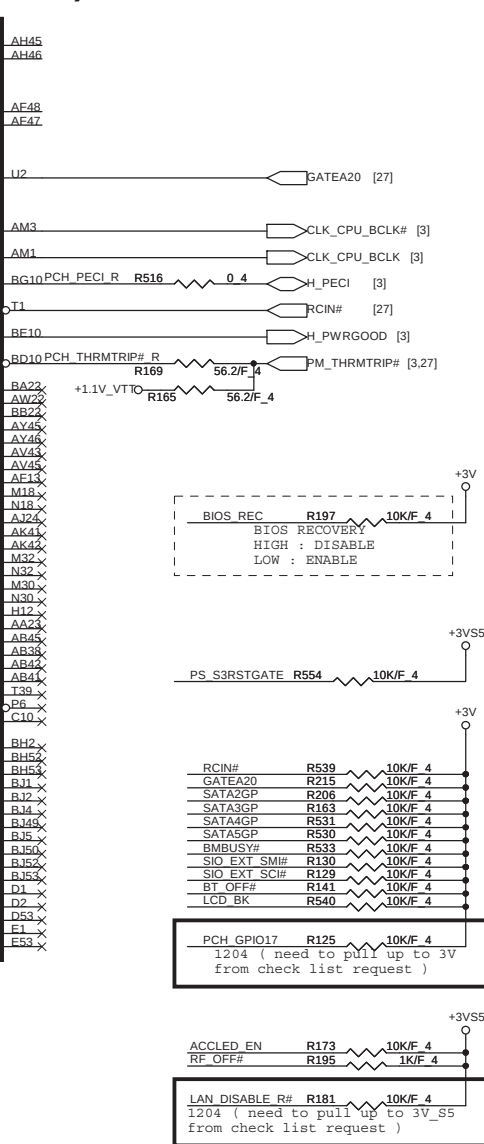
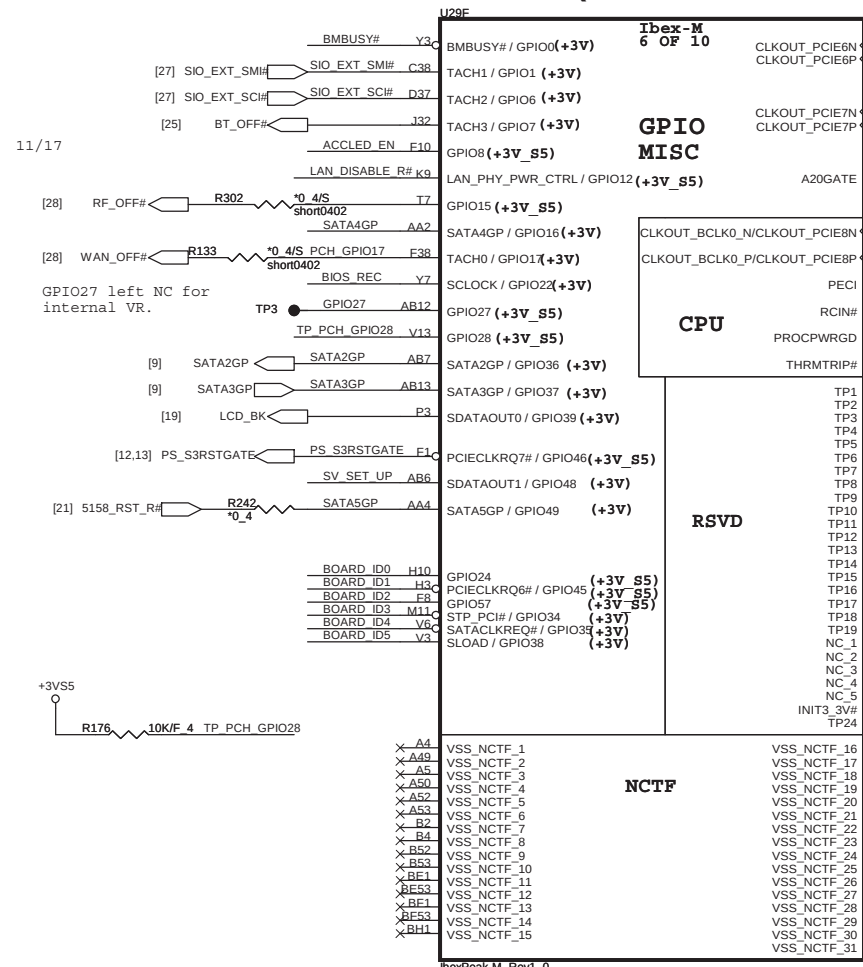


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

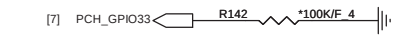
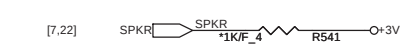
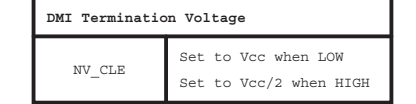
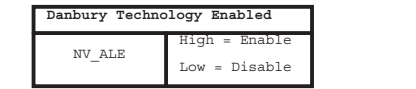
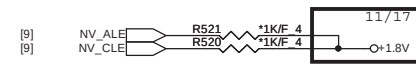
<http://hobi-elektronika.net>

IBEX PEAK-M (GND)

10



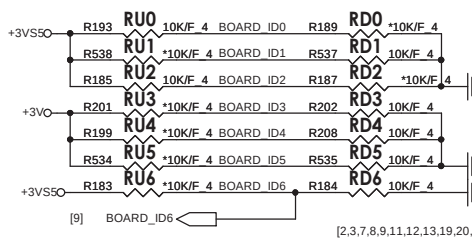
Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6" / 14"			0=QL4/TW9 1=QL2/SW9				
MDC				0=YES 1=NO			

BOARD ID SETTING

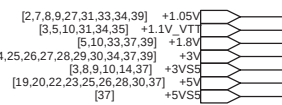
Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)



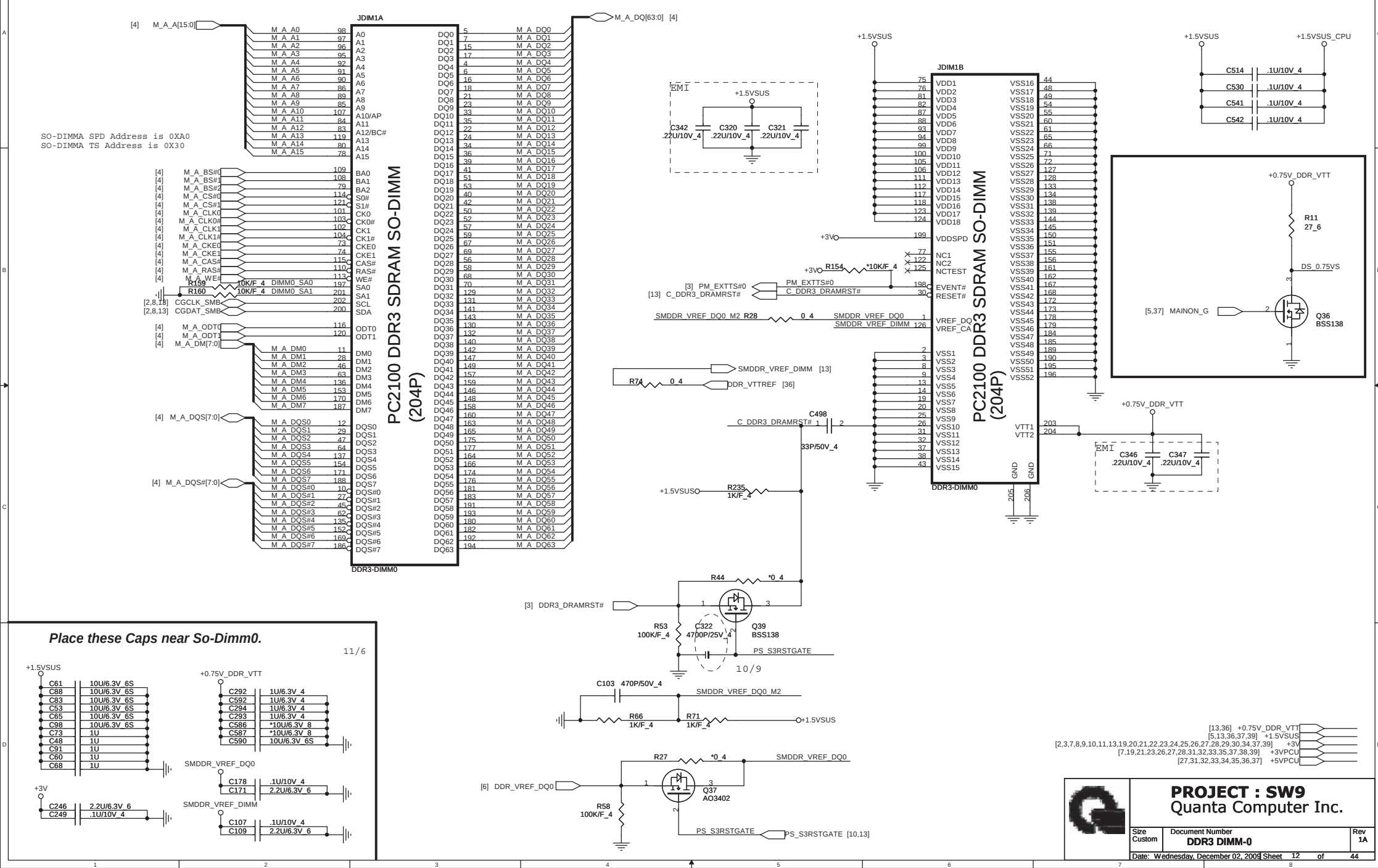
[3,5,11,31,34,35] +1.1V_VT1
[5,11,33,37,39] +1.8V
[3,8,9,11,14,37] +3VSS

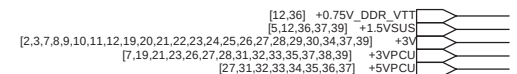
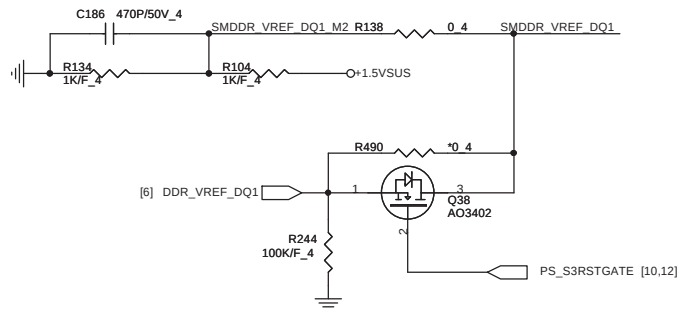
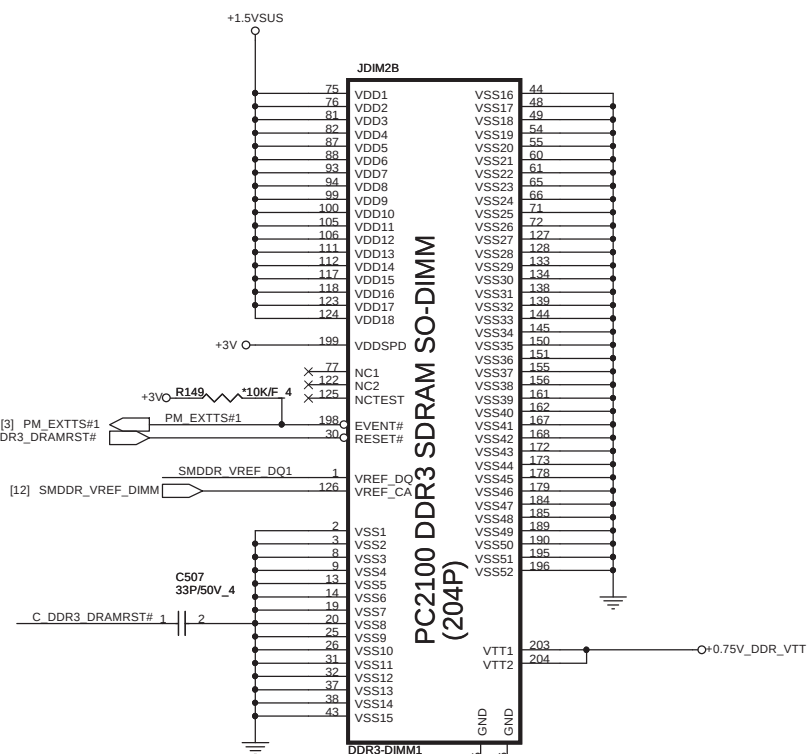


PROJECT : SW9 Quanta Computer Inc.		
Size Custom	Document Number PCH 4/5 (GPIO & Strap)	R



Size Custom	Document Number PCH 5/5 (POWER)	Rev 1A
Date: Wednesday, December 02, 2009 Sheet		11 of 44

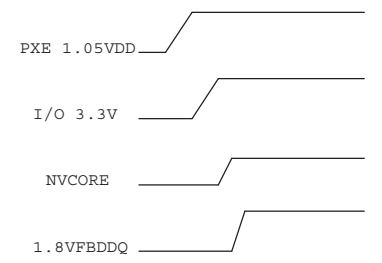




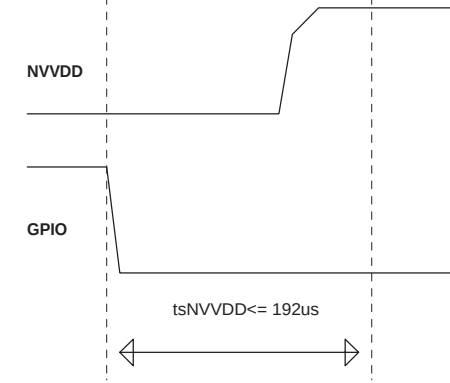
PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM-1	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 13 of 44		

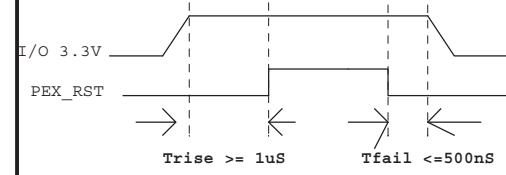
power up sequence



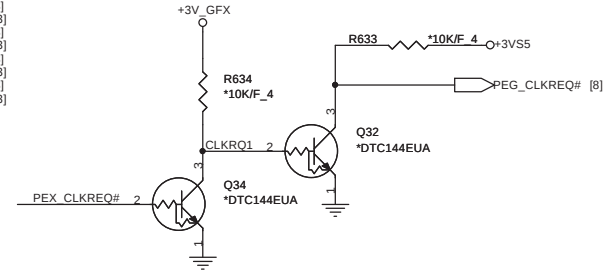
NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time



PEX_RST timing



For Switchable only

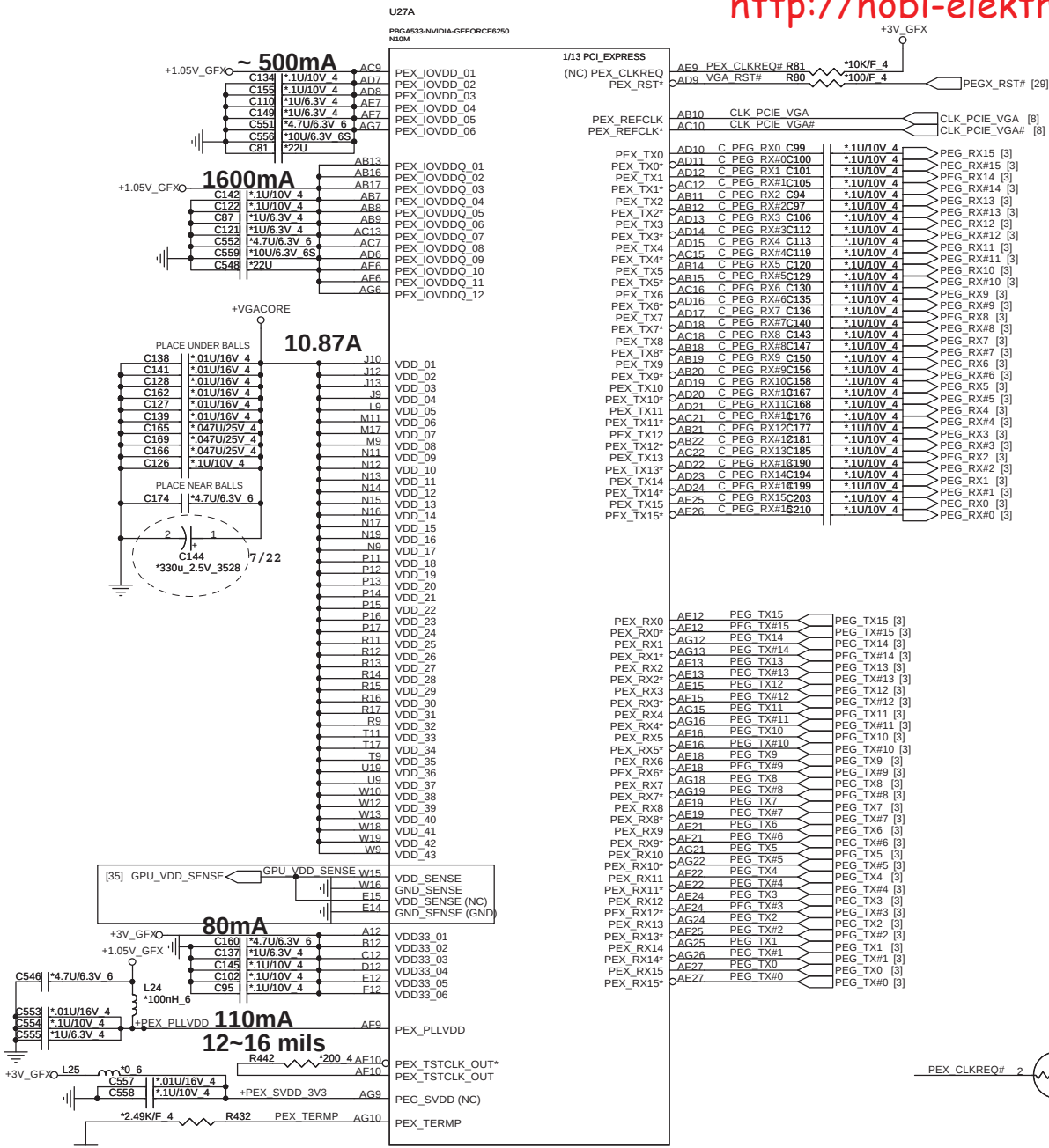


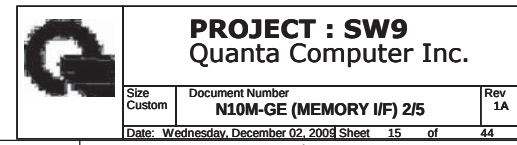
VGA Thermal Circuit ==> Del 6/16

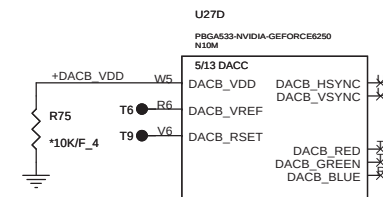
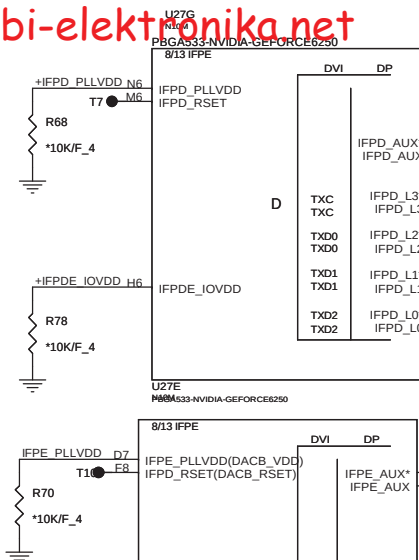


PROJECT : SW9
Quanta Computer Inc.

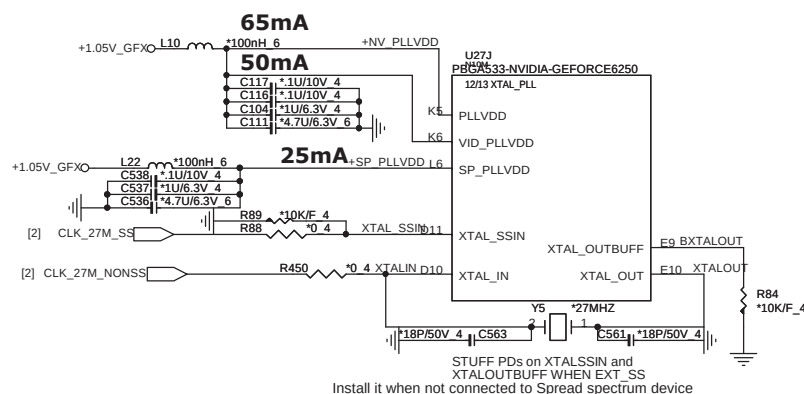
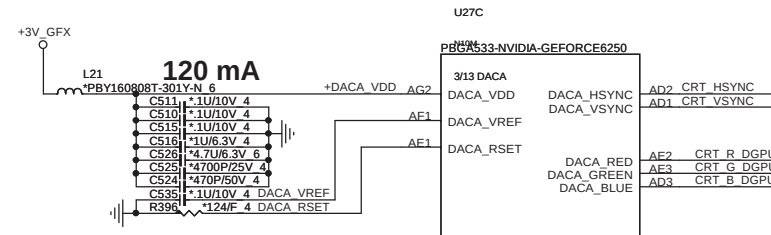
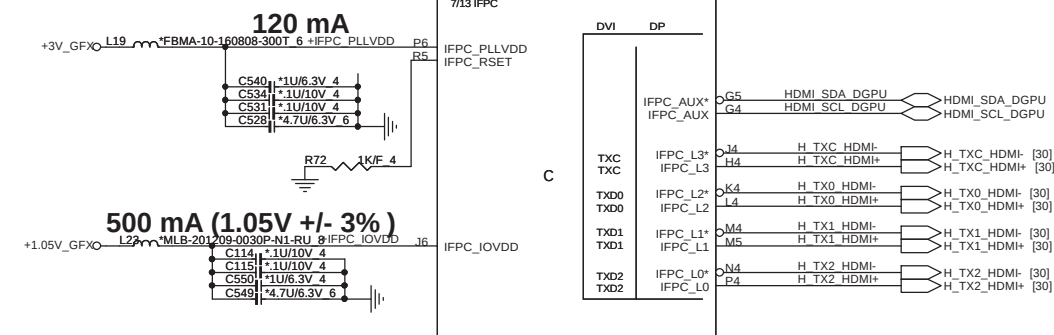
Size Custom	Document Number N10M-GE (PCIE I/F) 1/5	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 14 of 44		







CRT R DGPU R473	*0 4	CRT R	CRT_R	[7,20]
CRT G DGPU R474	*0 4	CRT G	CRT_G	[7,20]
CRT B DGPU R475	*0 4	CRT B	CRT_B	[7,20]
CRT HSYNC R476	*0 4	HSYNC COM	HSYNC_COM	[7,20]
CRT VSYNC R477	*0 4	VSYNC COM	VSYNC_COM	[7,20]

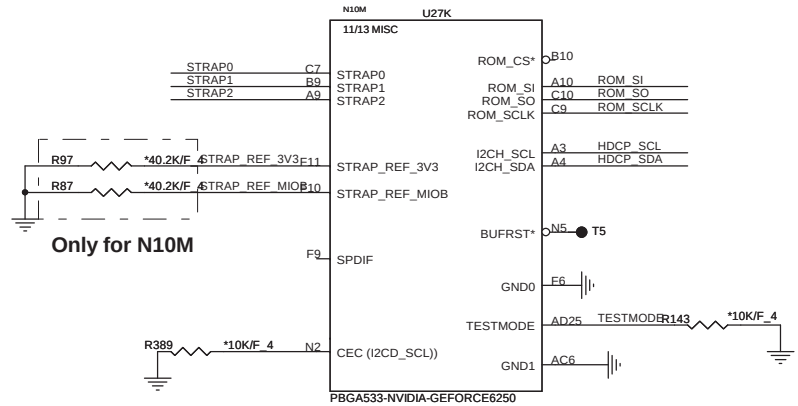


SPREAD SPECTRUM == >Del 6/16

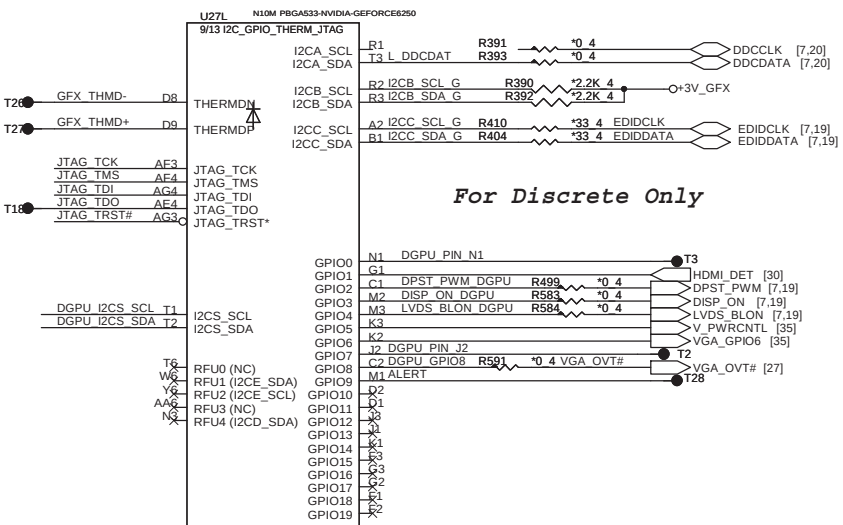


PROJECT : SW9
Quanta Computer Inc.

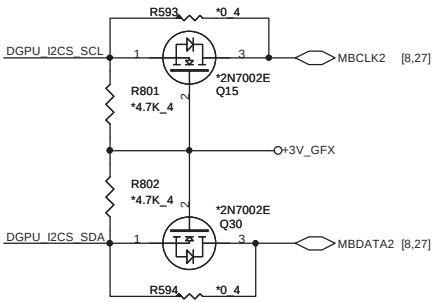
Size Custom	Document Number N10M-GE (DISPLAY) 3/5	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 16 of 44		



Only for N10M



For Discrete Only



Mount Q15, Q30, R801, R802
For Switchable only

PCI_DEVID:	STRAP2
N11P-GE1	0x0A29
N11M-GE1	0x0A75

Logical Strapping Bit Mapping	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)] Default: Hynix VRAM
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK		PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1		3GIO_PADCFC[3]	3GIO_PADCFC[2]	3GIO_PADCFC[1]	3GIO_PADCFC[0]
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
0101		Reserved		
0110	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646E-EC12	

(Ra)

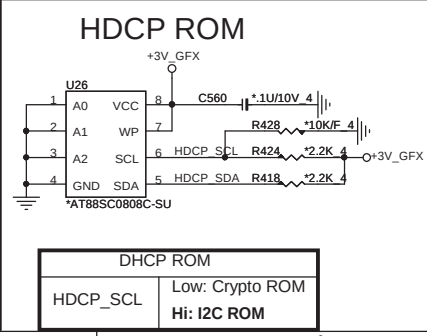
GPIO ASSIGNMENTS

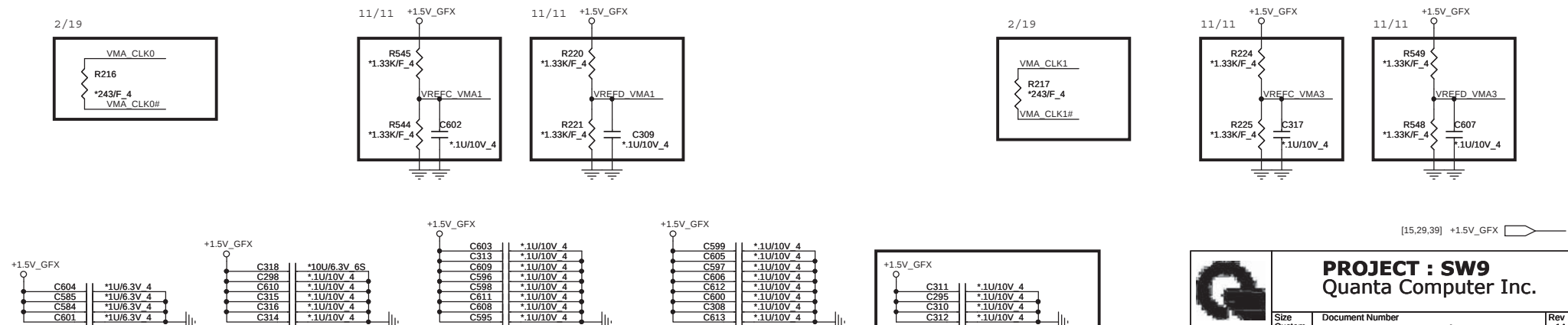
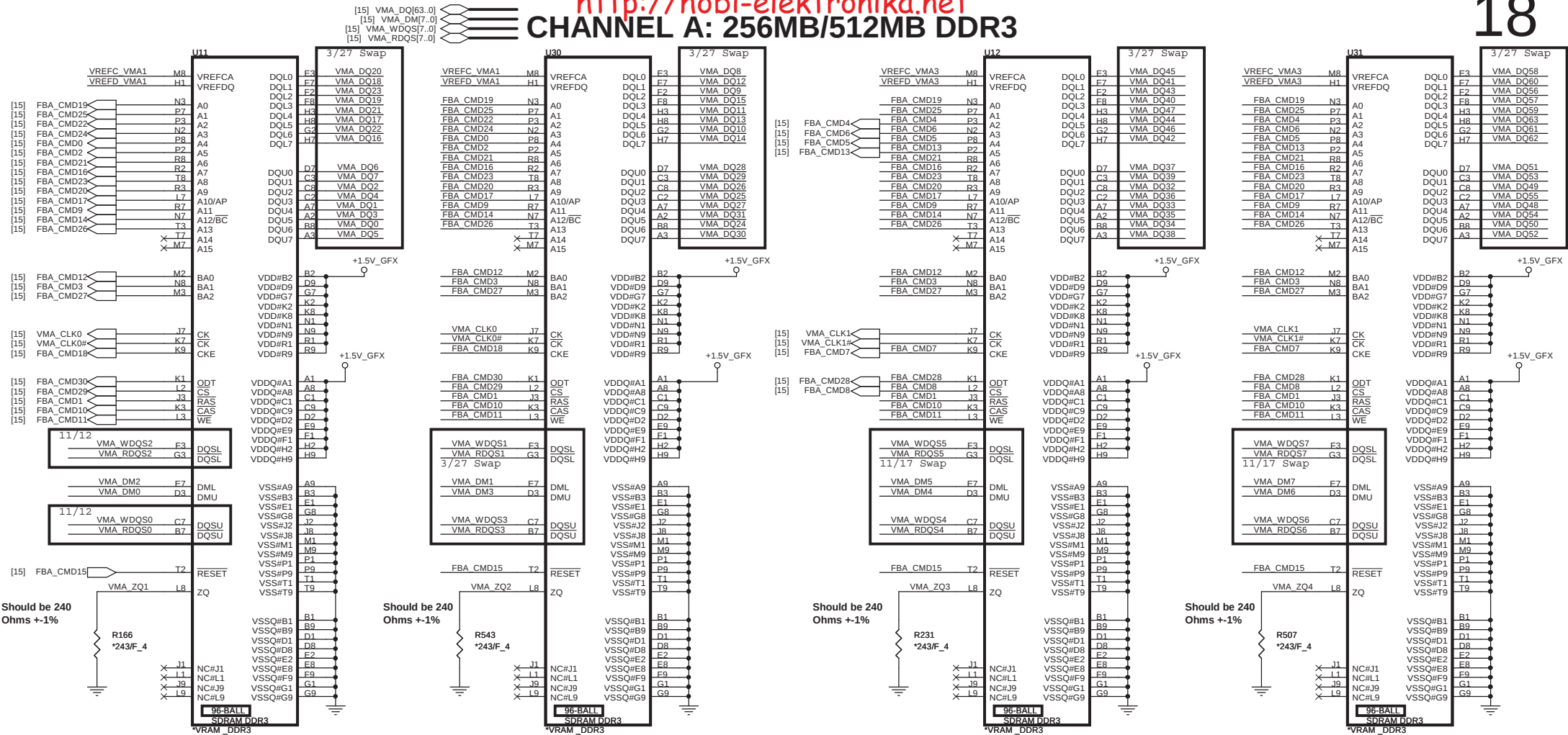
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VID0
6	OUT	N/A	NVVD VID1
7	OUT	N/A	NVVD VID2 ^{11/13}
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL ^{11/13}
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



PROJECT : SW9
Quanta Computer Inc.

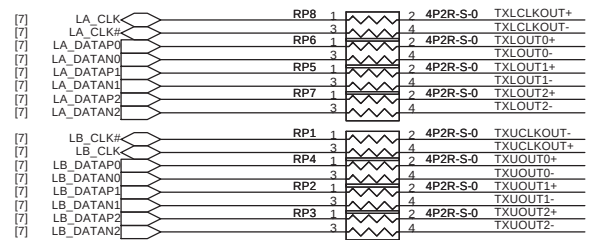
Size	Document Number	Rev
Custom	N10M-GE (GPIO&STRAPS) 4/5	1A
Date: Wednesday, December 02, 2009 Sheet 17 of 44		



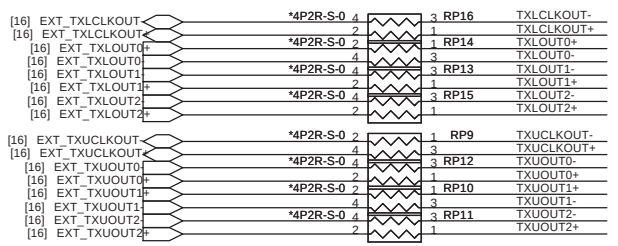


1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

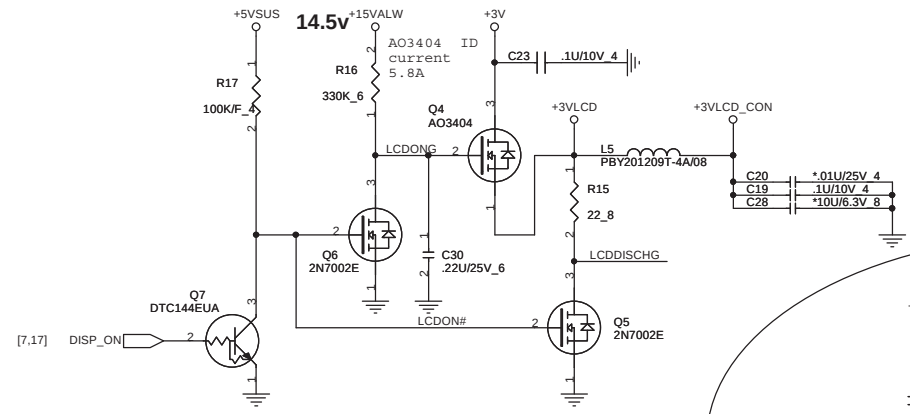
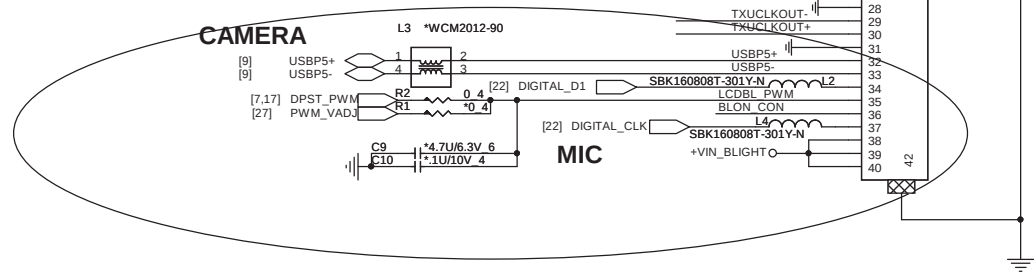
OPTION SIGNAL FROM NB FOR UMA VGA



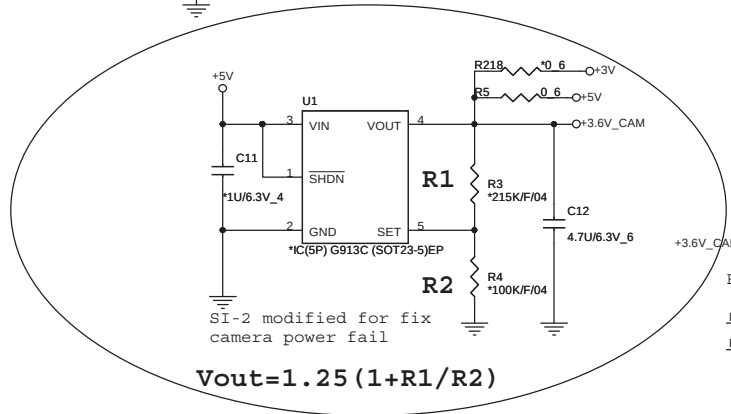
OPTION SIGNAL FROM Nvidia to VGA



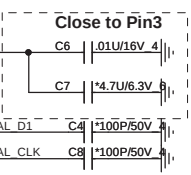
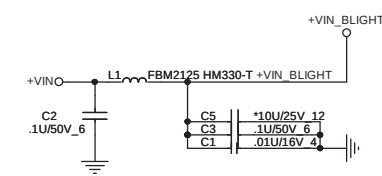
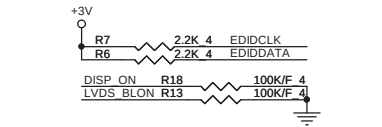
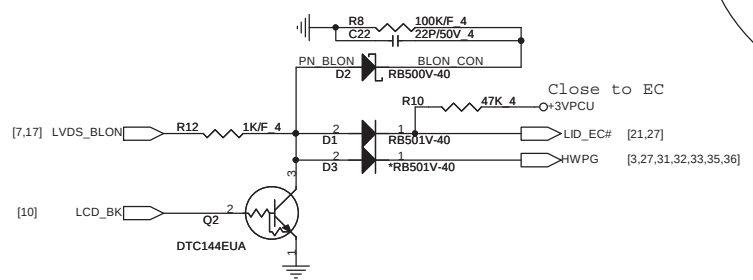
0820 add camera function



0820 add camera function

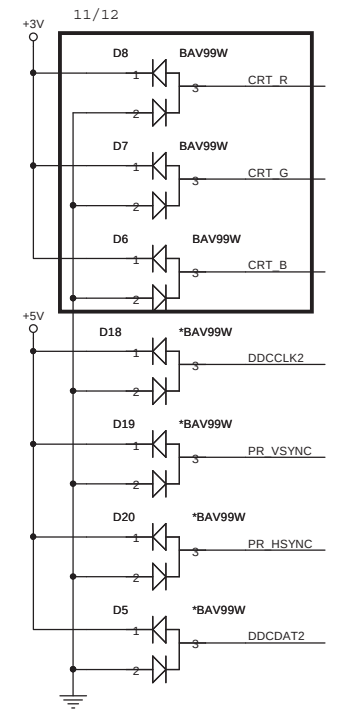
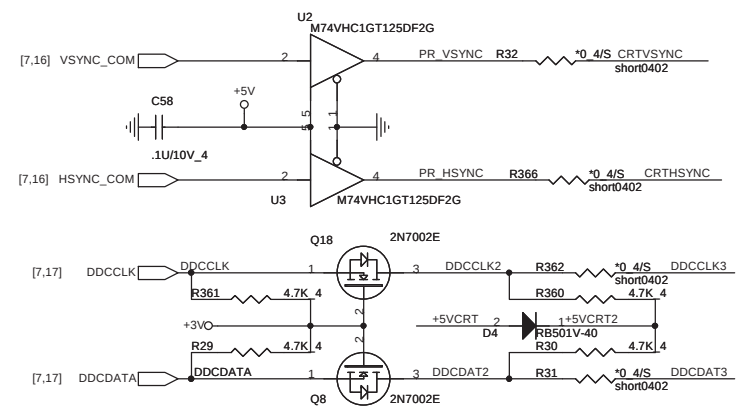
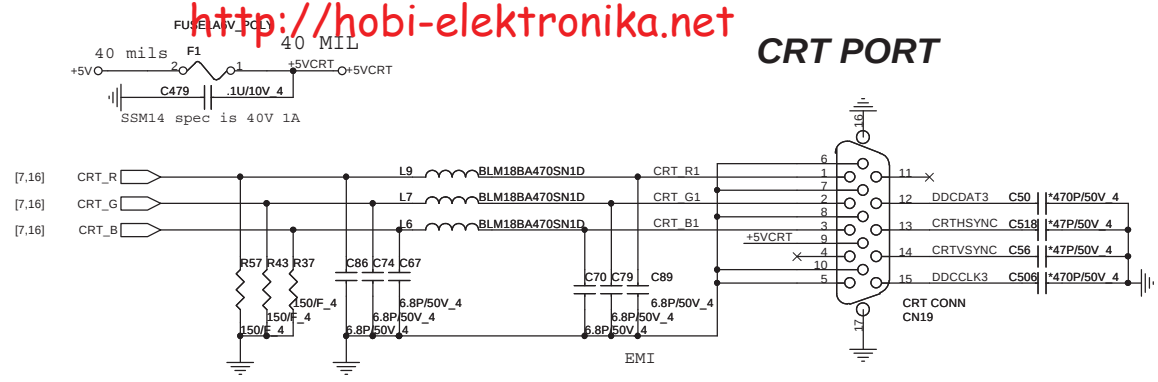


$V_{out} = 1.25 (1 + R1/R2)$



PROJECT : SW9
Quanta Computer Inc.

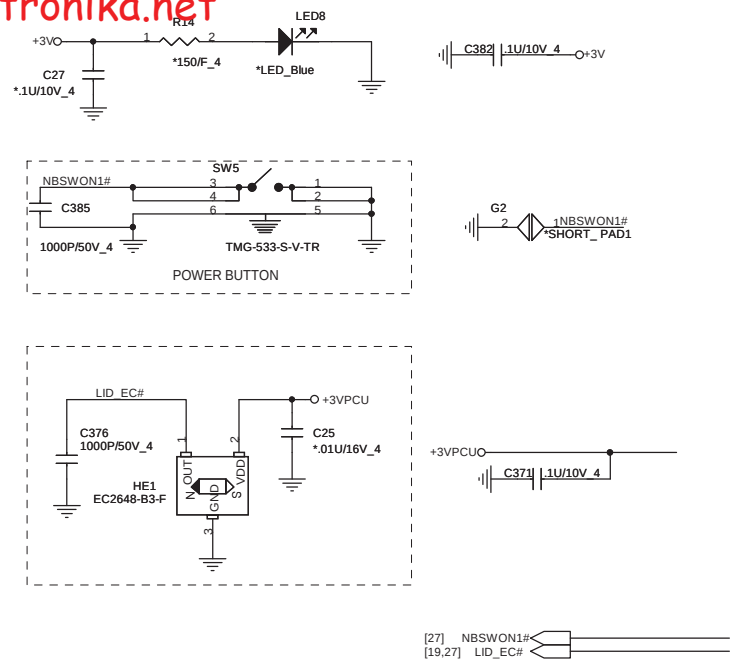
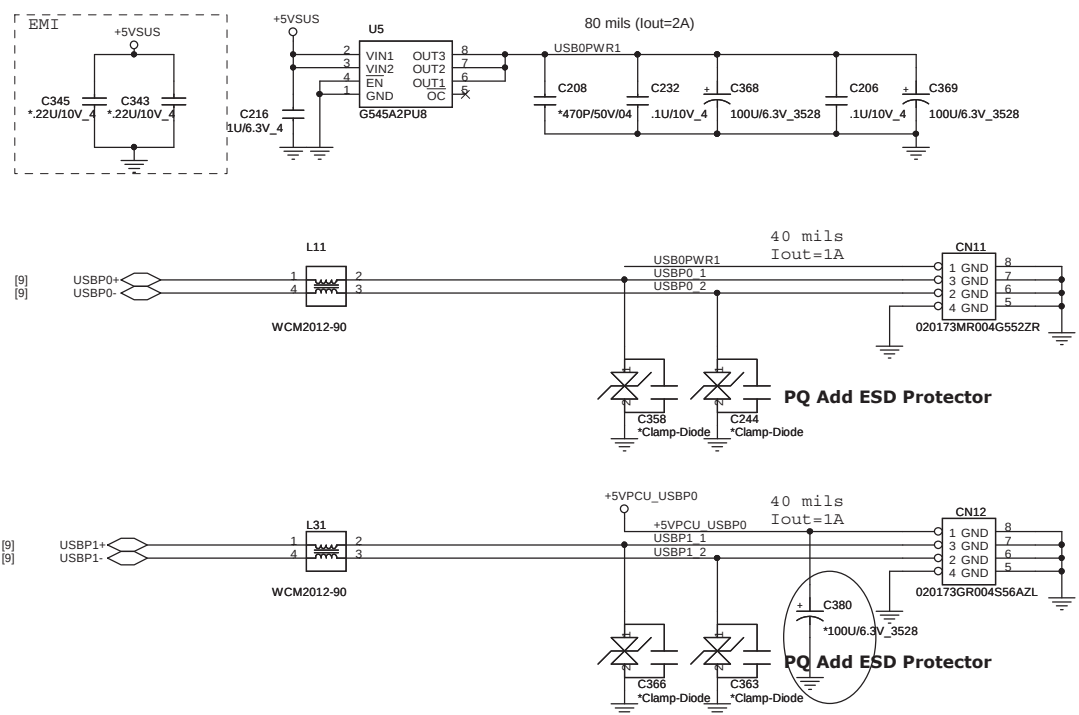
Size	Document Number	Rev
Custom	LCD CONN	1A
Date: Thursday, December 03, 2009		Sheet 19 of 44



PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A
Date: Wednesday, December 02, 2009 Sheet 20 of 44		

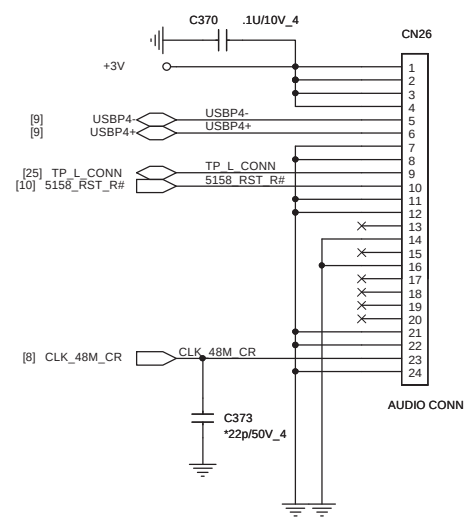
USB CONNECTOR



- 1. NBSWON1#
- 2. GND
- 3. GND
- 4. LID_EC#
- 5. +3V
- 6. +3VPCU

TO M/B CON.

PV Change CN2 footprint 88501-2001-24p-I-nb5

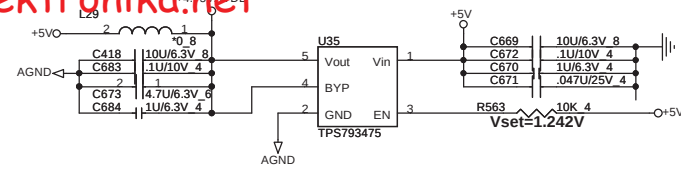
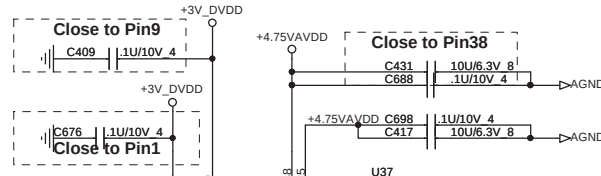
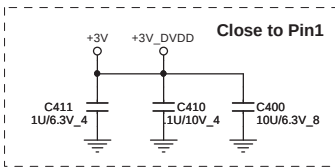


[2,3,7,8,9,10,11,12,13,19,20,22,23,24,25,26,27,28,29,30,34,37,39] +3VPCU +3V

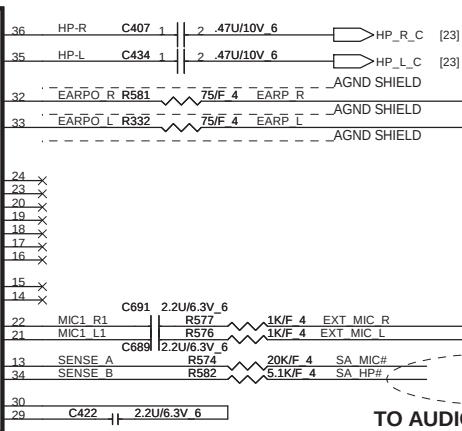
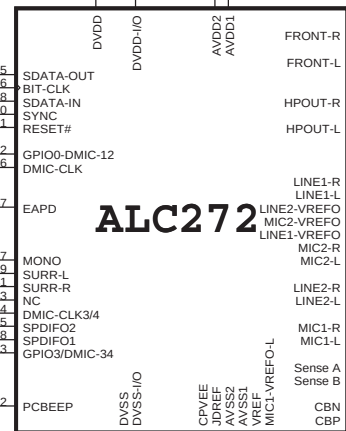
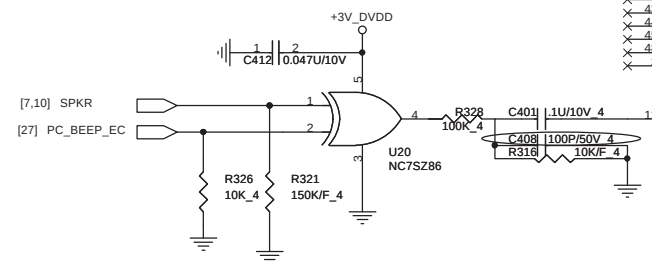
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159 & CR SOCKET	1A

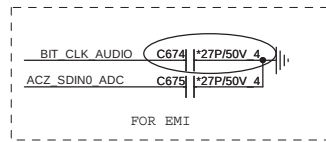
Date: Wednesday, December 02, 2009 Sheet 21 of 44



- [7] ACZ_SDOUT_AUDIO
- [7] BIT_CLK_AUDIO
- [7] ACZ_SDIN0_ADC
- [7] ACZ_SYNC_AUDIO
- [7] ACZ_RST#_AUDIO
- [19] DIGITAL_D1
- [19] DIGITAL_CLK

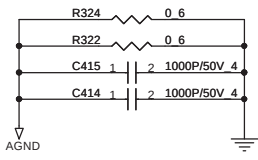


To Internal Speakers



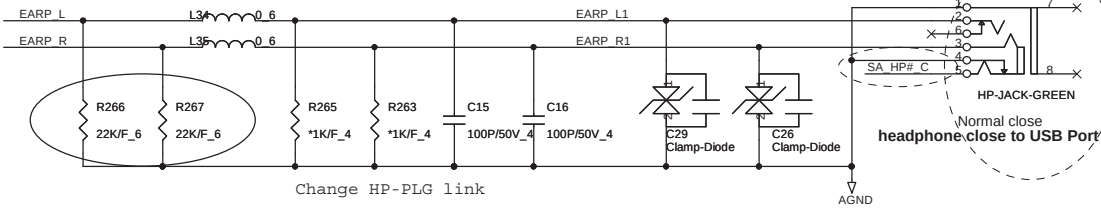
TO AUDIO/CON.

TO Audio Jack MIC



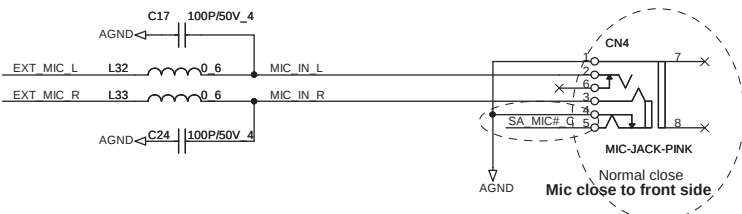
AUDIO CONNECTOR

10/07

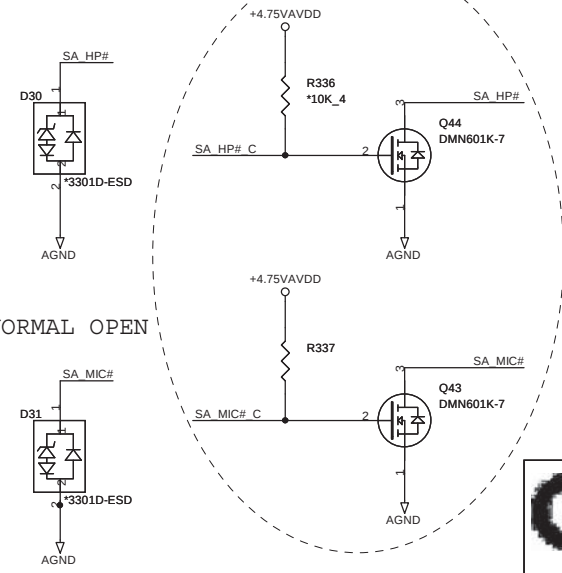


Change HP-PLG link

AUDIO JACKS CHANGE TO NORMAL OPEN



Mic close to front side

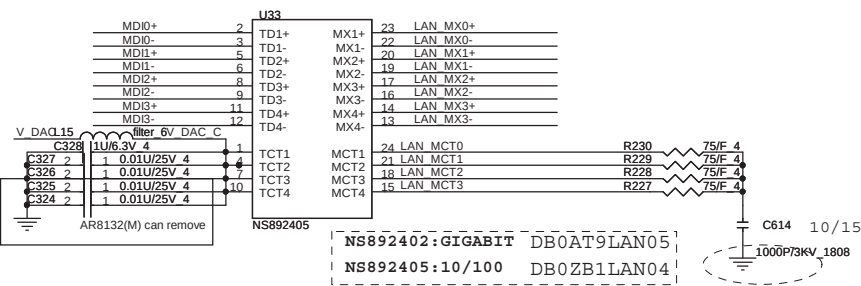


PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC272/BT CONN	1A
Date:	Wednesday, December 02, 2009	Sheet 22 of 44

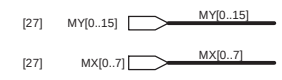
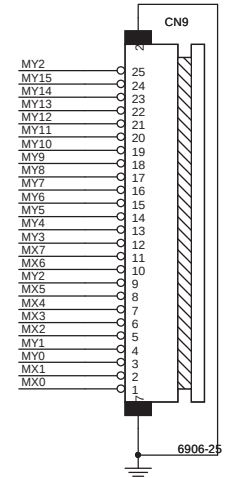
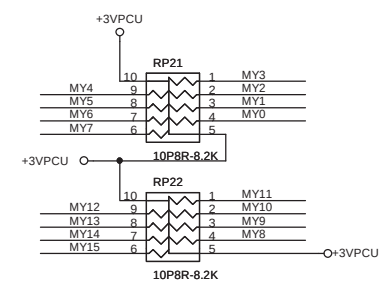
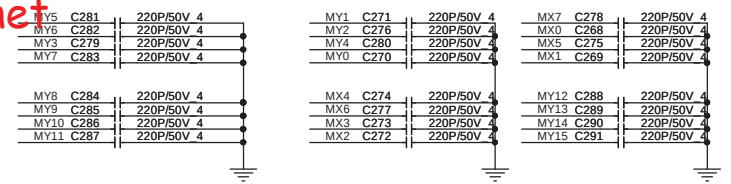
GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Size Custom	Document Number AMP_TPA6017/SPK/MDC/LED	Rev 1
Date: Wednesday, December 02, 2009 Sheet 23 of 44		

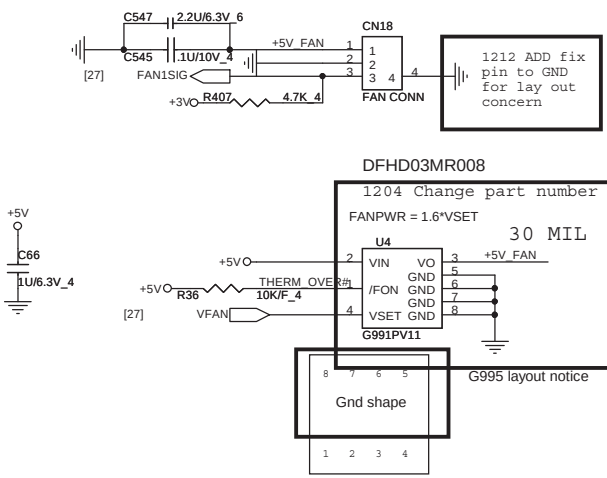


Size Custom	Document Number AR8131(M)/RJ45	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 24 of 44		

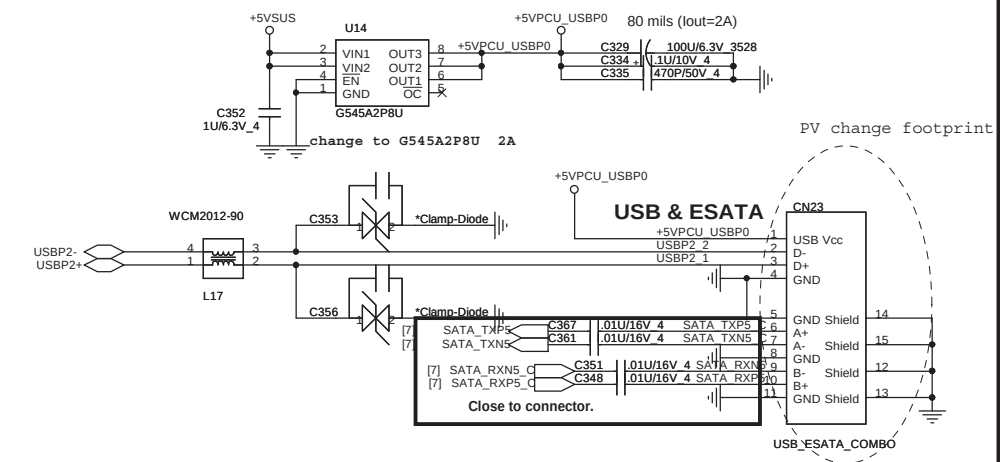
KEYBOARD Con.



CPU FAN



E-SATA/USB COMBO

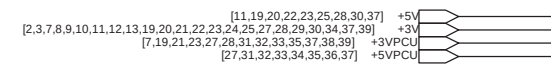


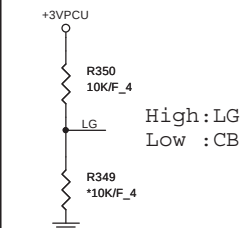
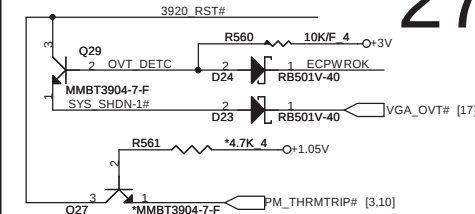
Capacity board Con.



PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/PWR/ESATA/FAN/CAM/MIC	1A
Date: Wednesday, December 02, 2009 Sheet 26 of 44		

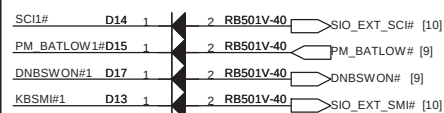
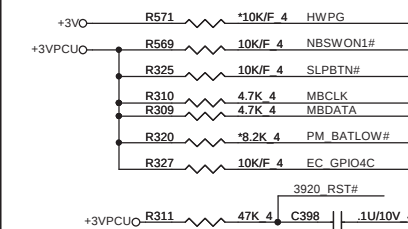
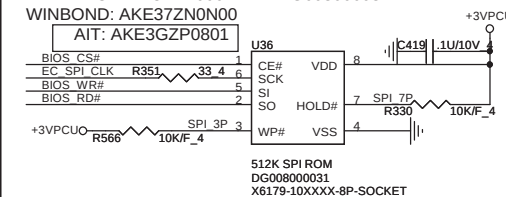




SPI BIOS

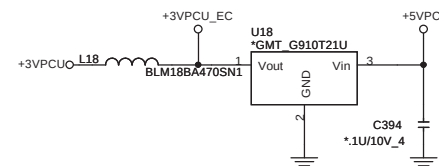
512K byte SPI ROM for EC SPI ROM Socket

MXIC: AKE3KZP0001
WINBOND: AKE37ZN0N00
AIT: AKE3GZP0801



PROJECT : SW9
Quanta Computer Inc.

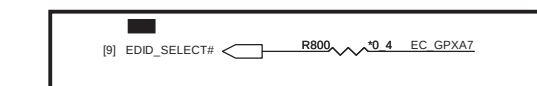
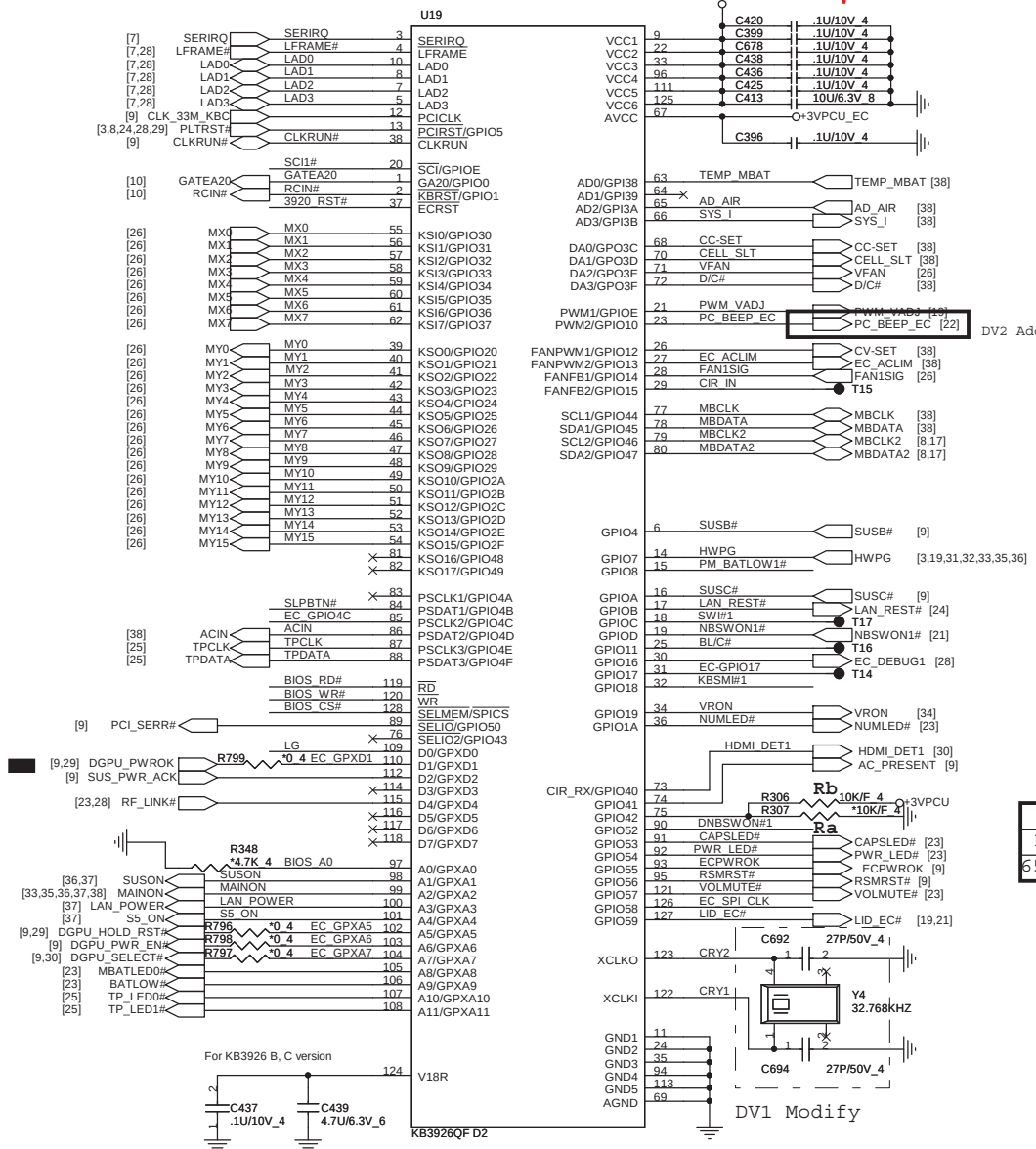
Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A
Date:	Wednesday, December 02, 2009	Sheet 27 of 44



For Switchable Only
Un-mount D24

Adapter table select

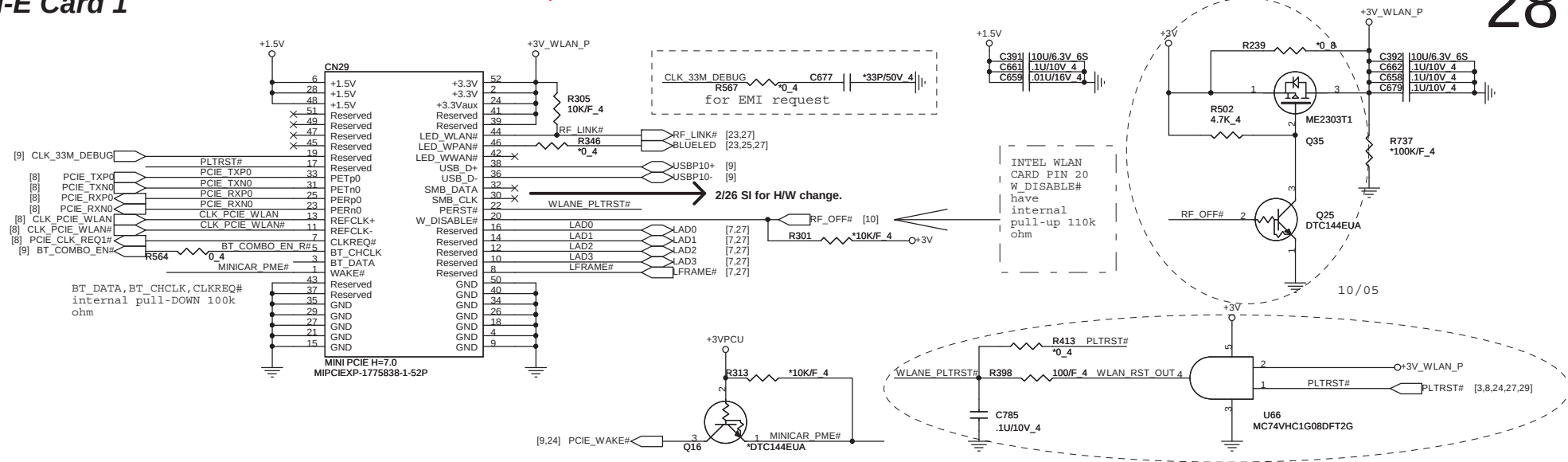
ID	Ra	Rb
120W	10K	N/A
65W/90W	N/A	10K



[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,28,29,30,34,37,39] +3V
[7,19,21,23,26,28,31,32,33,35,37,38,39] +3VPCU
[31,32,33,34,35,36,37] +5VPCU

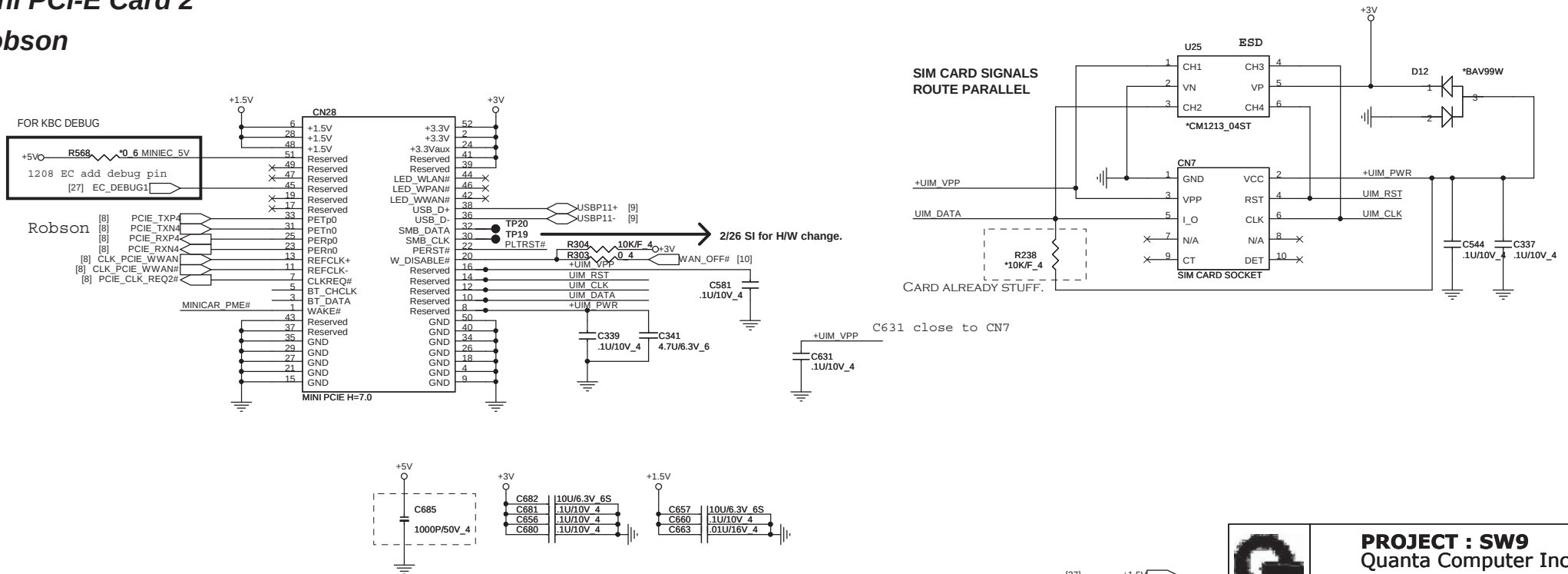
Mini PCI-E Card 1

WLAN



Mini PCI-E Card 2

Robson



[37] +1.5V
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,27,29,30,34,37,39] +3V
[7,19,21,23,26,27,31,32,33,35,37,38,39] +3VPCU
[11,19,20,22,23,25,26,30,37] +5V



PROJECT : SW9
Quanta Computer Inc.

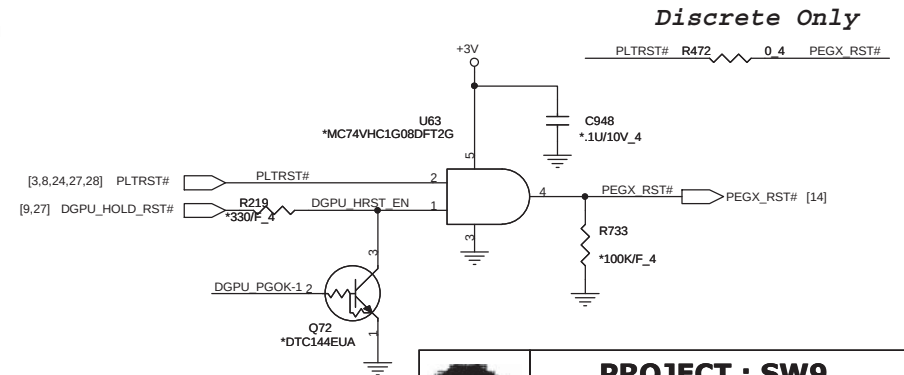
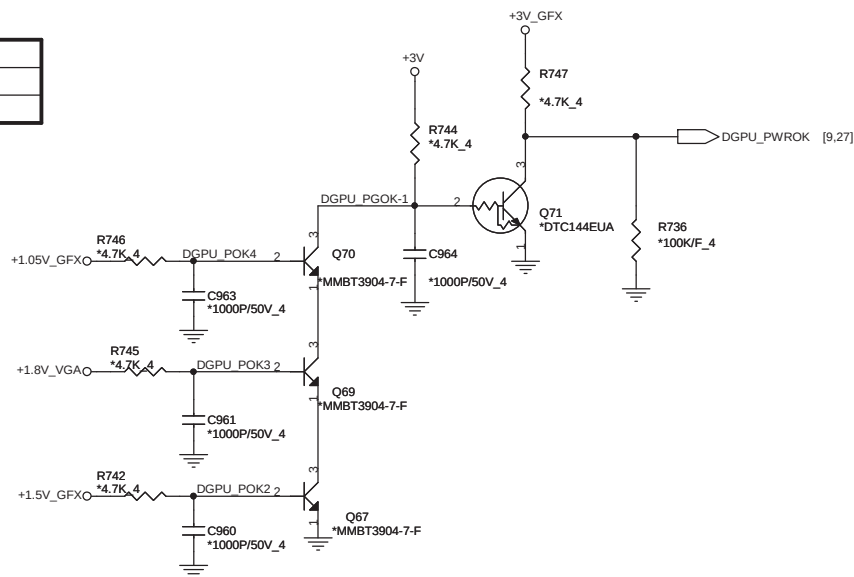
Size	Document Number	Rev
Custom	MINI PCIE CONN X2	1A
Date: Wednesday, December 02, 2009	Sheet	28of 44

DEL Switch IC

DEL Switch IC

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

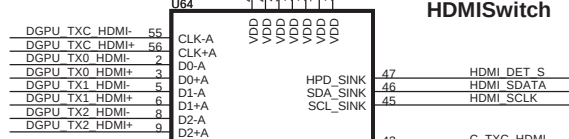
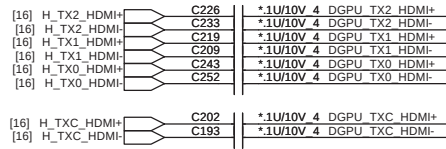
SELx	Ay
LOW	B1
HIGH	B2



PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number LVDS / CRT Switch	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 29 of 44		

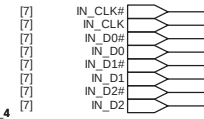
DGPU_HDMI



HDMISwitch

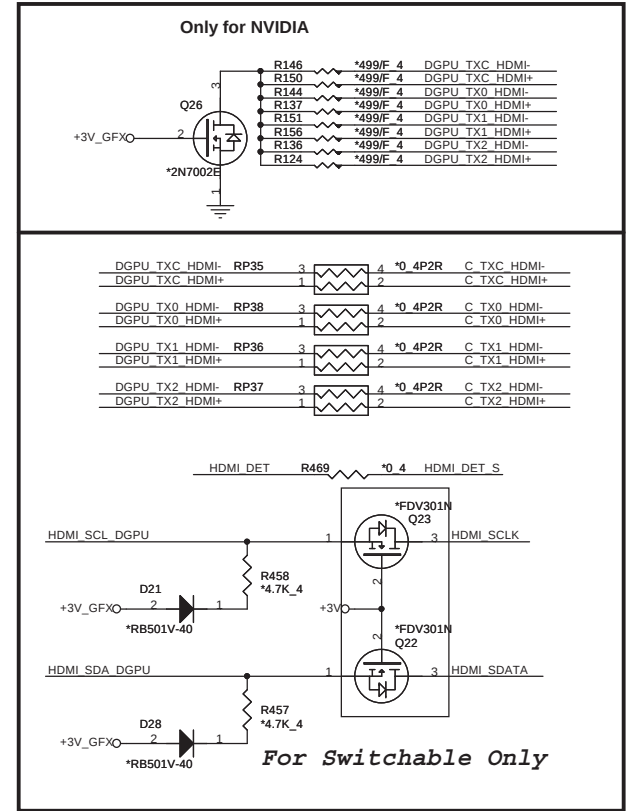


IGPU_HDMI



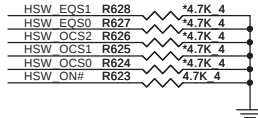
SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

To HDMI Conn.



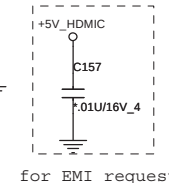
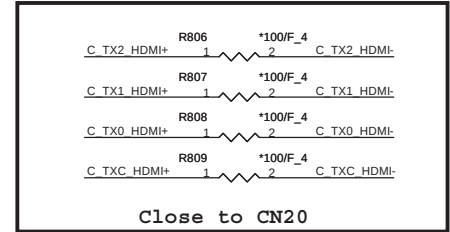
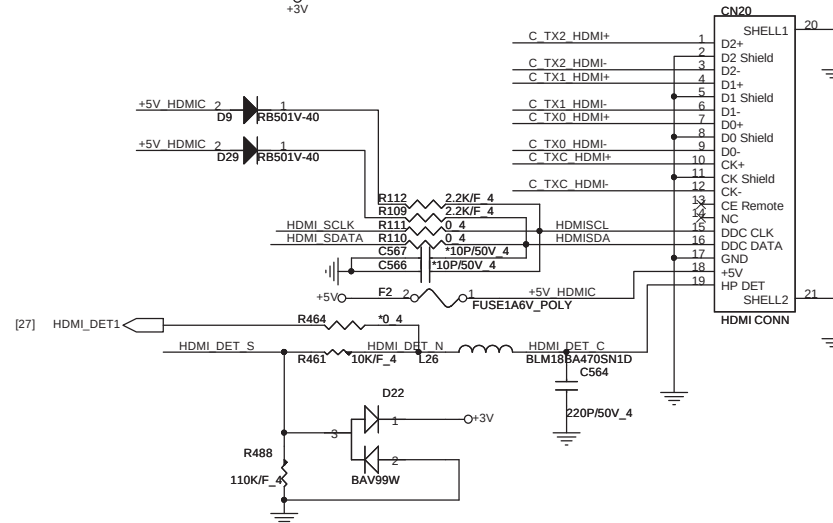
OC SETTING
 S2 S1 S0 = 1 : 1 : 1 500mV 0dB Default
 S2 S1 S0 = 1 : 1 : 0 750mV 0dB
 S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
 S2 S1 S0 = 1 : 0 : 0 600mV 0dB
 S2 S1 S0 = 0 : 1 : 1 500mV 0dB
 S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
 S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
 S2 S1 S0 = 0 : 0 : 0 500mV 6dB

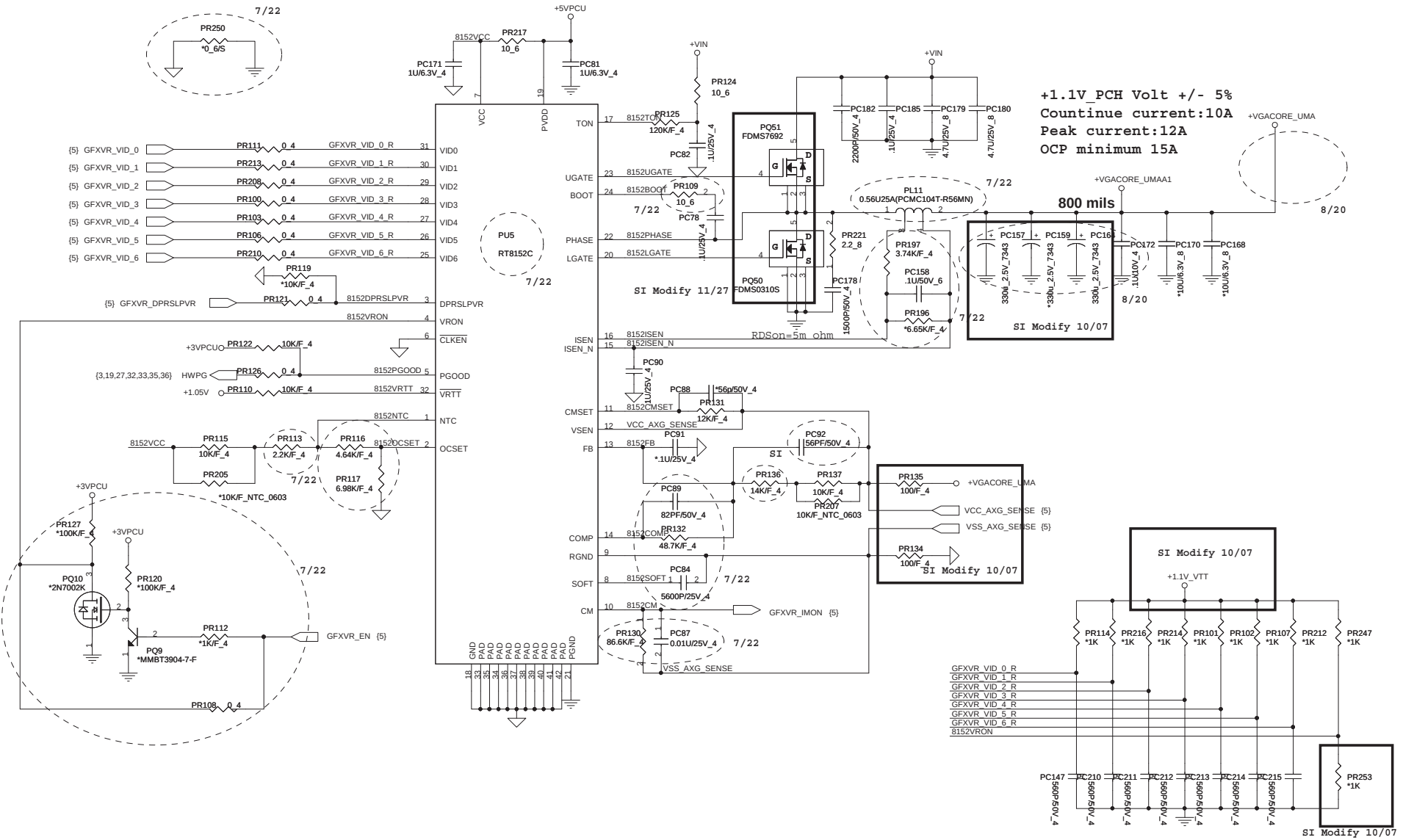
EQ SETTING
 S1 S0 = 1 : 1 3dB Default
 S1 S0 = 1 : 0 8dB
 S1 S0 = 0 : 1 3dB
 S1 S0 = 0 : 0 15dB



Mount R629 / R632 for UMA only

HDMI PORT







Size Custom	Document Number PCH +1.05V (RT8204)	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 33 of 44		



Size Custom	Document Number CPU Core (ADP3212)
Date: Wednesday, December 02, 2009 Sheet 34 of 4	

OCP Setting	Operation Max current	PR30	PR42
45W CPU (60A)	50A	1.91 Kohm	4.02 Kohm
35W CPU (48A)	40A	1.54 Kohm	4.99 Kohm

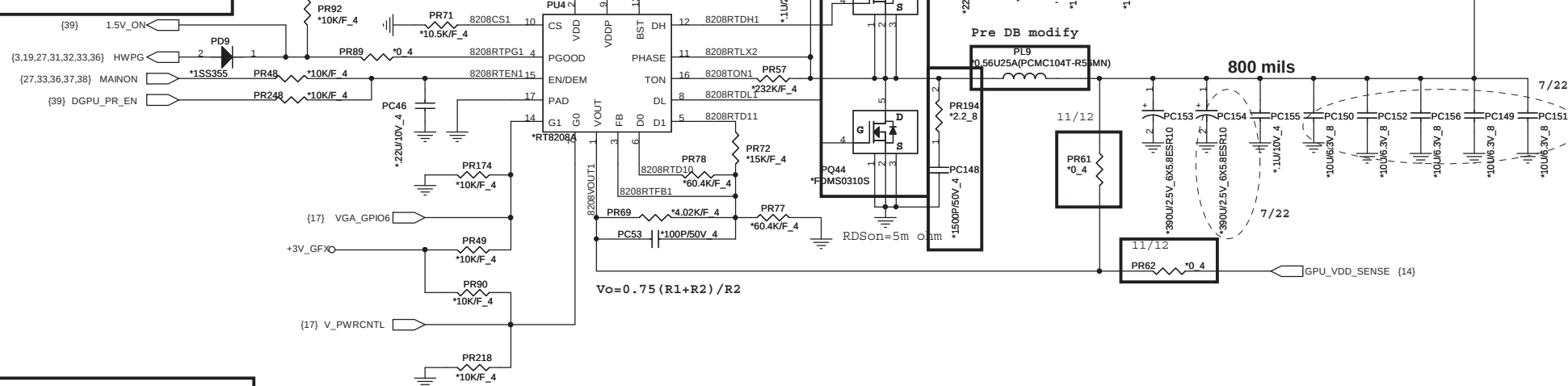
VGA Core & VCC1.1

<http://hobi-elektronika.net>

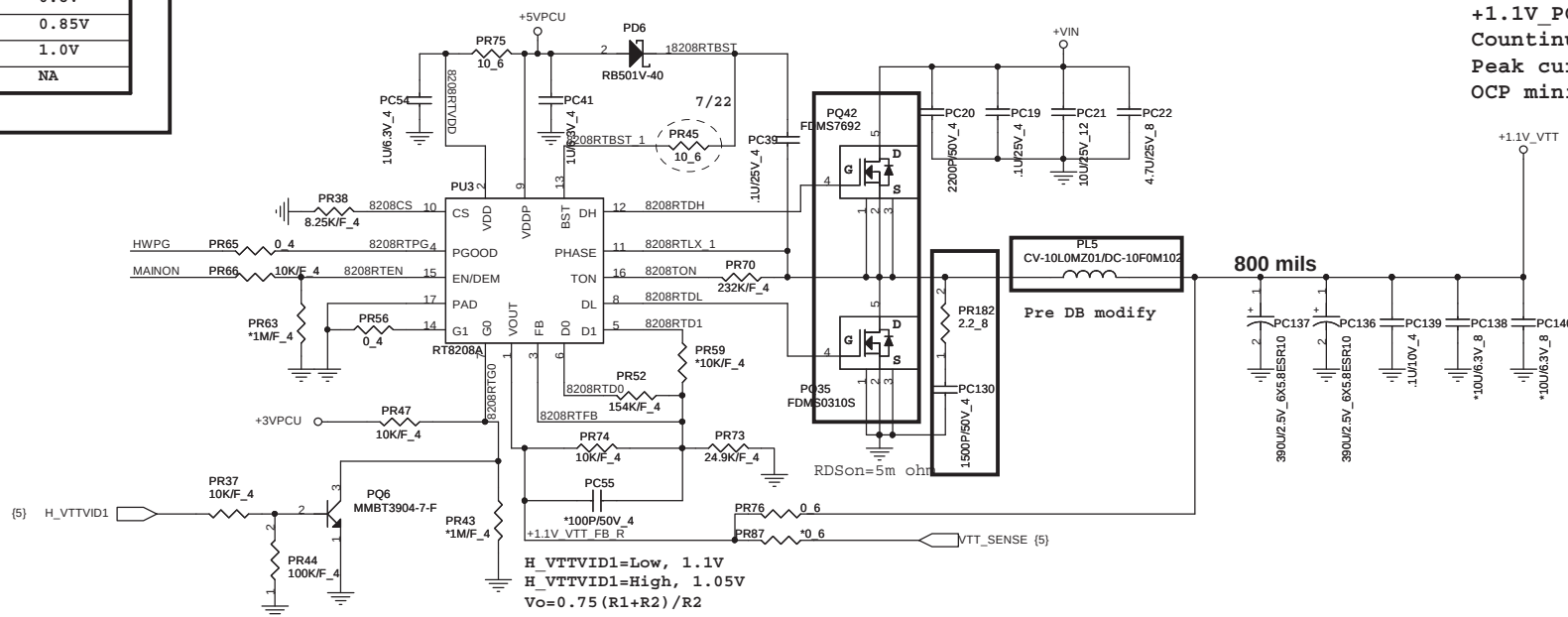
35

- 1 : un-Mount PD9/PR48 for Switchable
2 : un-Mount PR248 for Discrete

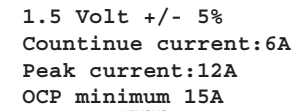
+VGACORE Volt +/- 5%
Continue current:16A
Peak current:18A
OCP minimum 23A



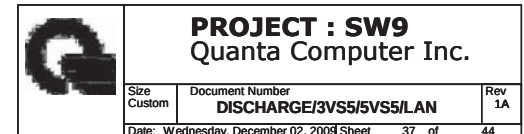
VGA_GPIO6	V_PWRCNTL	N10M-GS
GPIO6	GPIO5	
0	0	0.8V
0	1	0.85V
1	0	1.0V
1	1	NA



+1.1V_PCH Volt +/- 5%
Continue current:12A
Peak current:15A
OCP minimum 18A



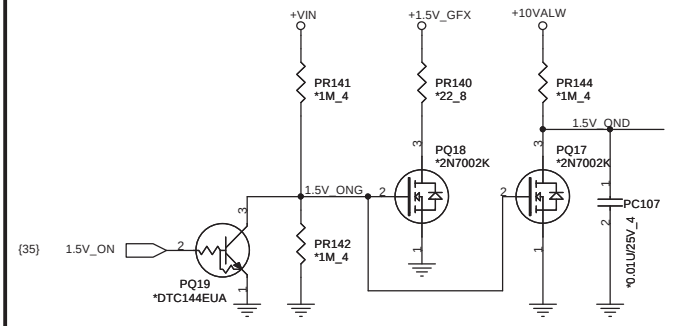
Date: Wednesday, December 02, 2009 Sheet 36 of 44





Size Custom	Document Number Charger (ISL6251)	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 38 of 44		

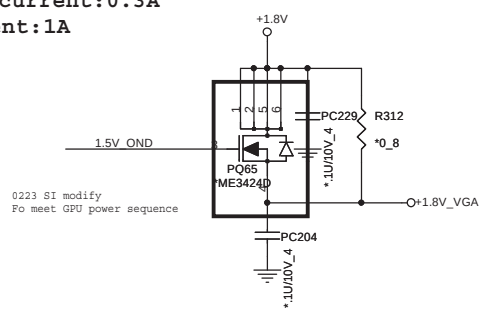
For Discrete or switchable Only



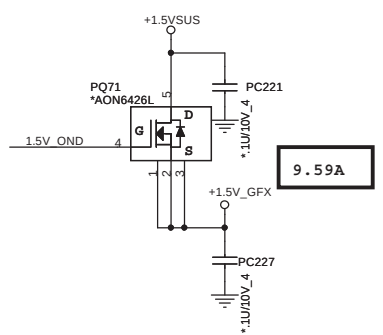
Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete or switchable Only

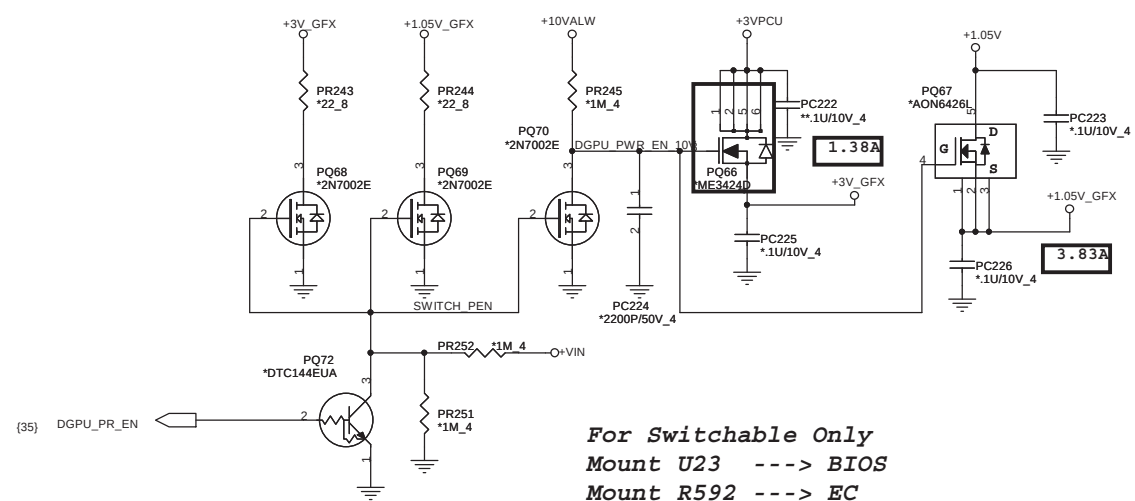
+1.8 Volt +/- 0.1V
Countinue current:0.3A
Peak current:1A



0223 SI modify
Fo meet GPU power sequence



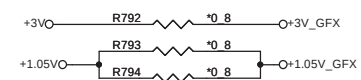
9.59A



For Switchable Only
Mount U23 ---> BIOS
Mount R592 ---> EC

R51 co-lay PQ71
R53/R54 co-lay PQ68

For Discrete Only



For Hybrid DGPU Power Rails Sequence

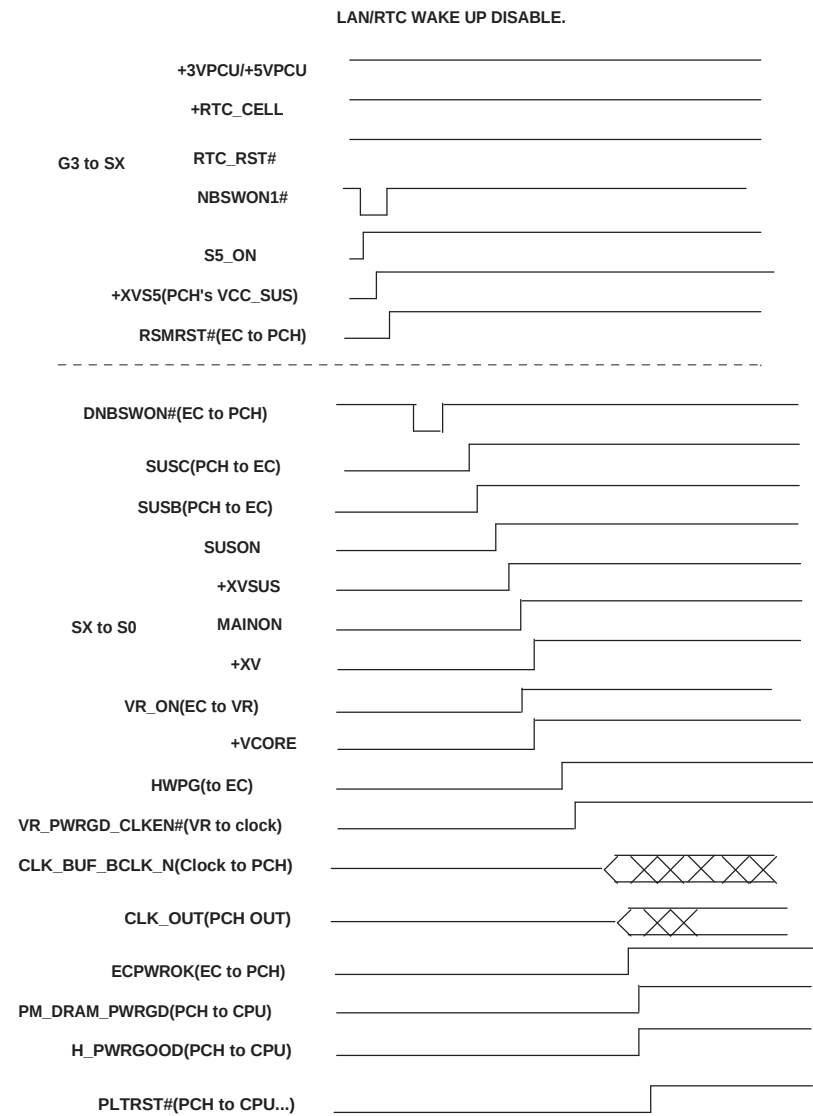
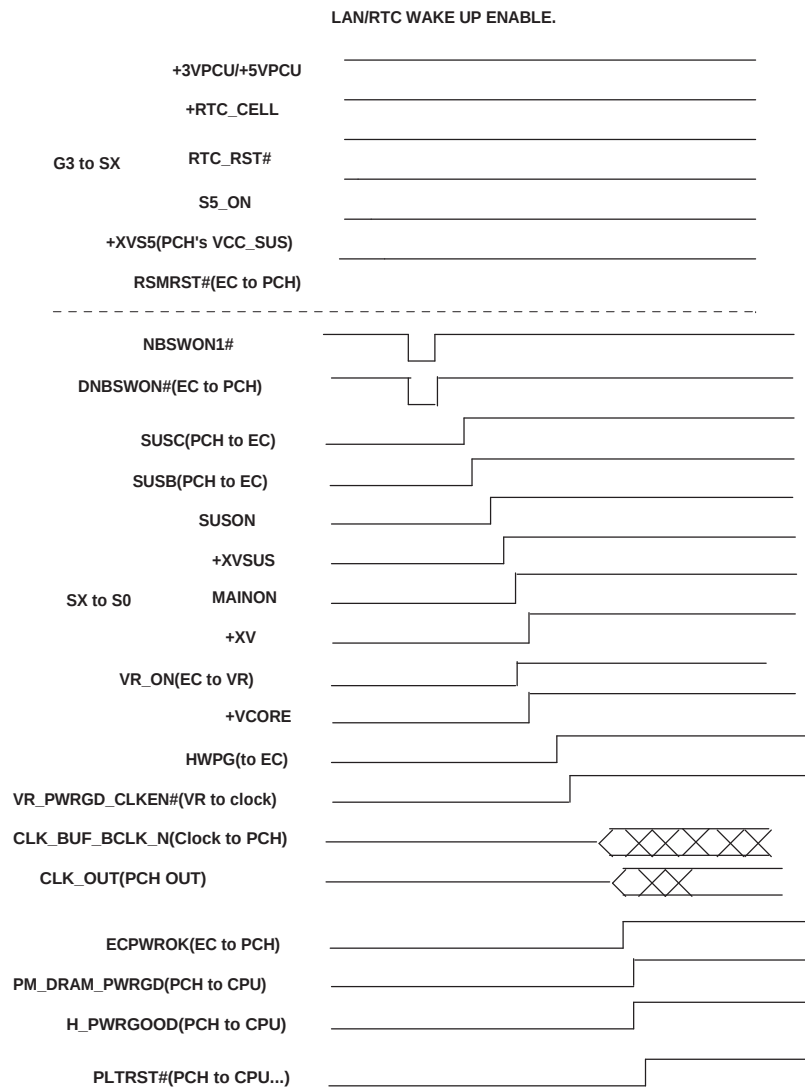
1. +3V_GFX, +1.05V_GFX
2. +VGA_CORE -> DGPU_PG
3. 1.5V_GFX, +1.8V_GFX



PROJECT : SW9
Quanta Computer Inc.

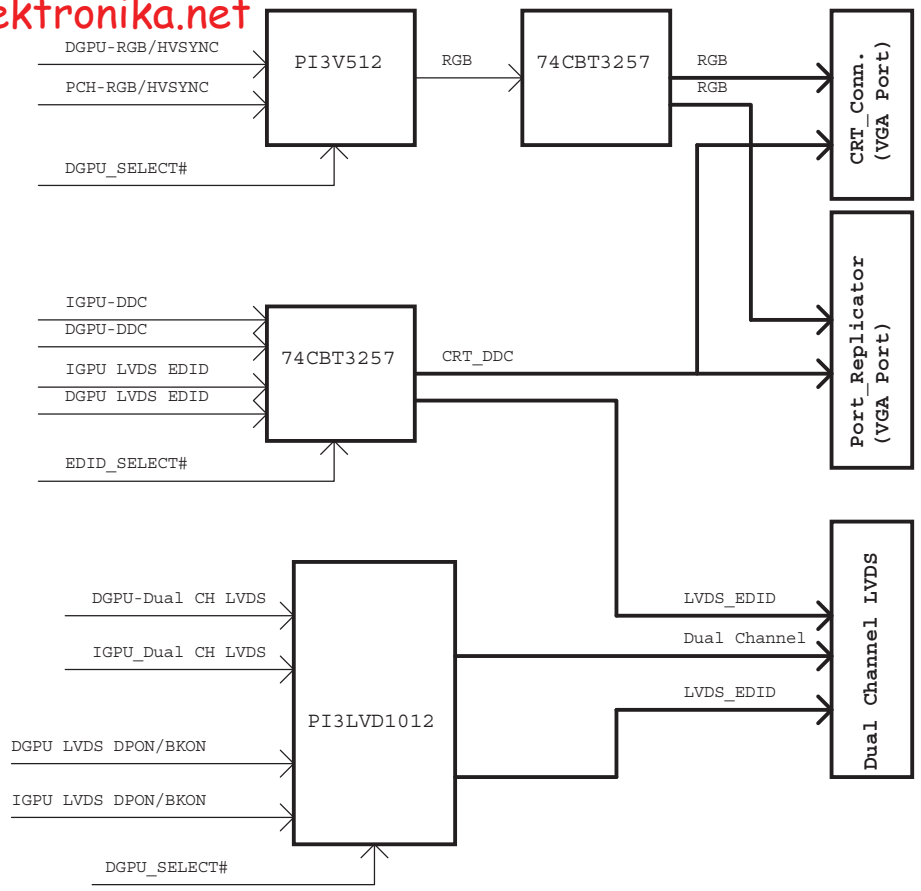
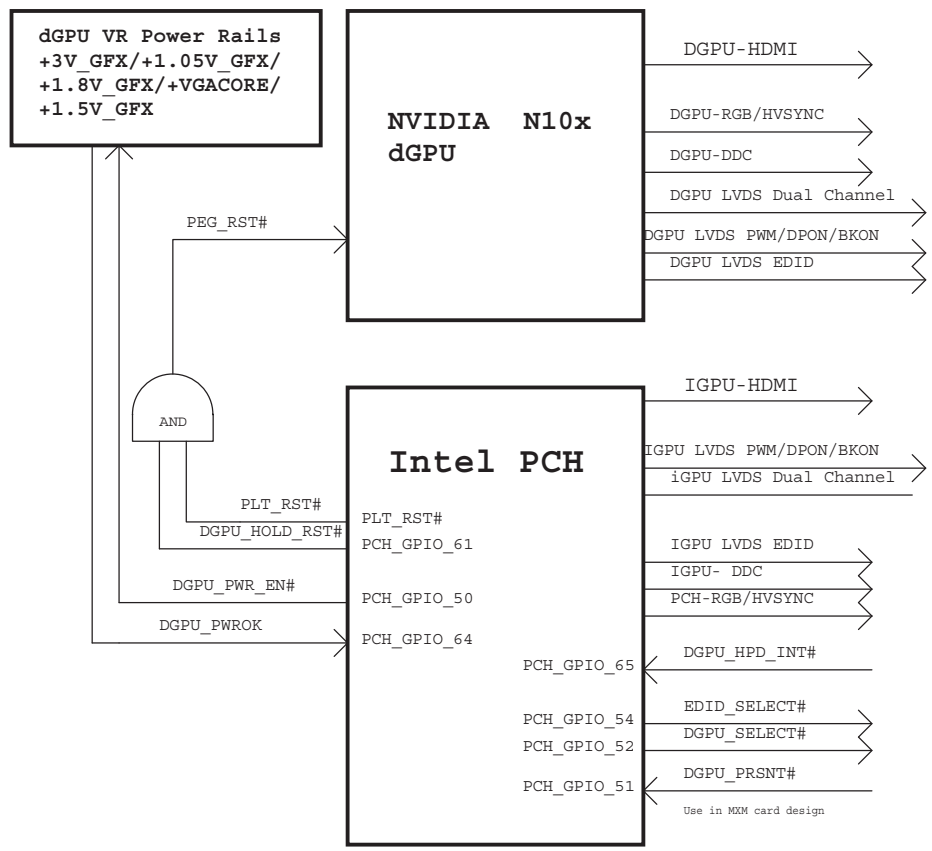
Size	Document Number	Rev
A3	Switchable Power	1A
Date: Wednesday, December 02, 2009 Sheet 39 of 44		

Power up sequence



PROJECT : SW9
Quanta Computer Inc.

Size Custom	Document Number Power up sequence	Rev 1A
Date: Wednesday, December 02, 2009 Sheet 40 of 44		



Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO61	DGPU_HOLD_RST#
PCH_GPIO50	DGPU_PWR_EN#
PCH_GPIO64	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO51	DGPU_PRSENT#
PCH_GPIO53	PWM_SELECT#

