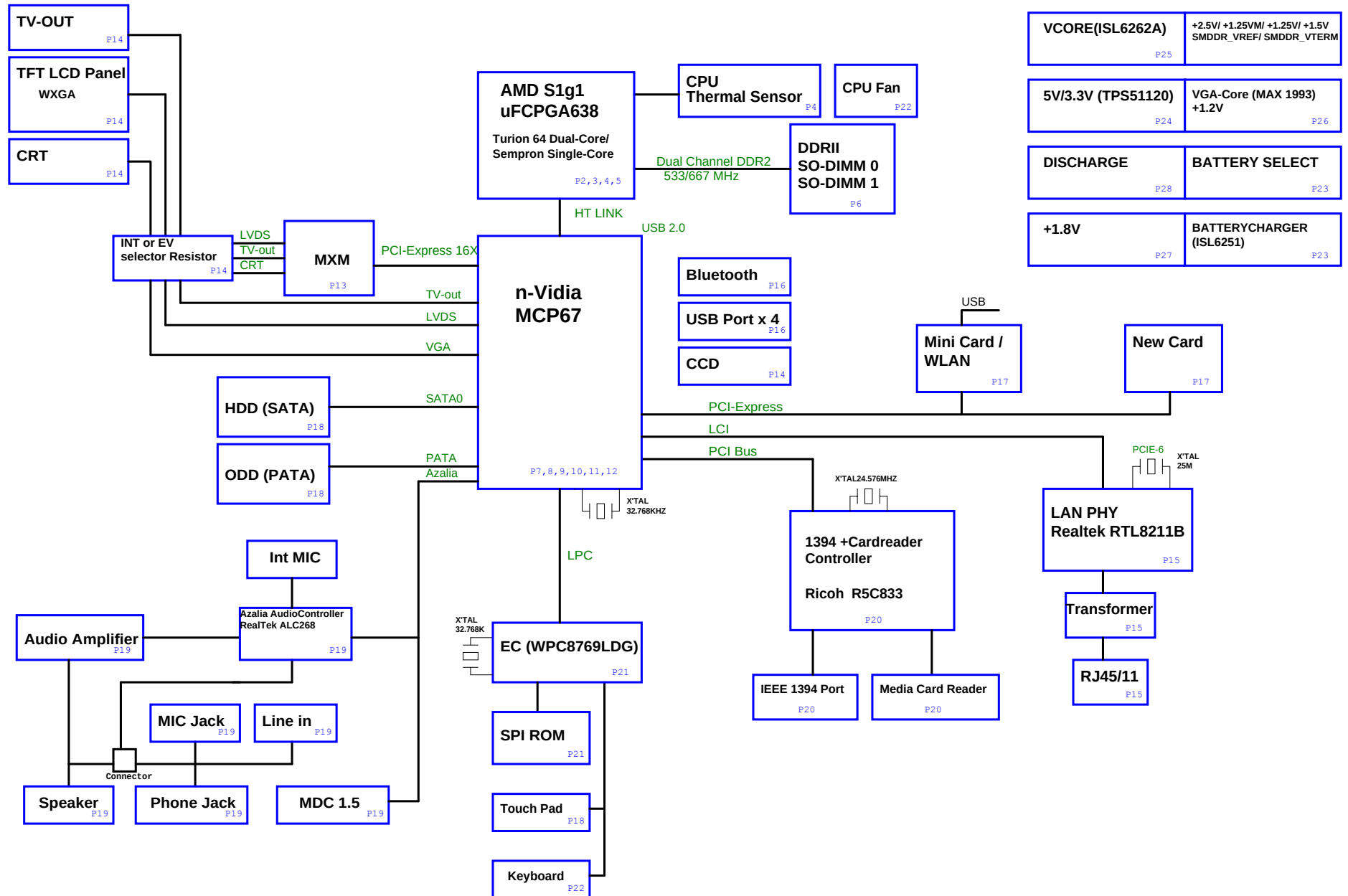


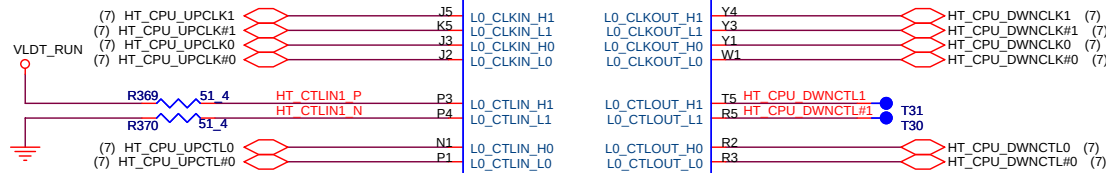
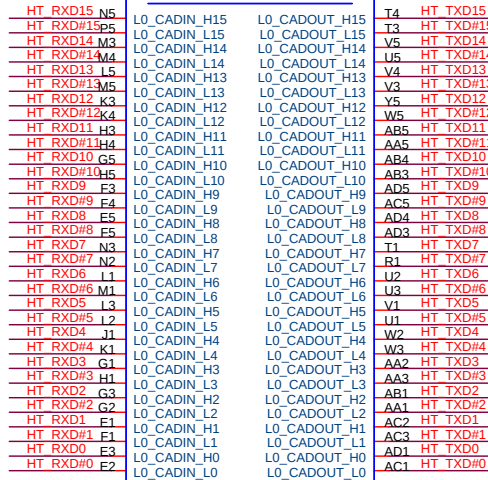
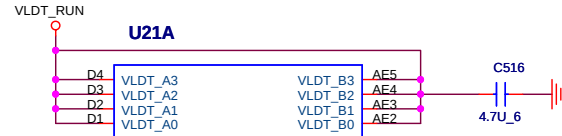
ZO3 SYSTEM BLOCK DIAGRAM



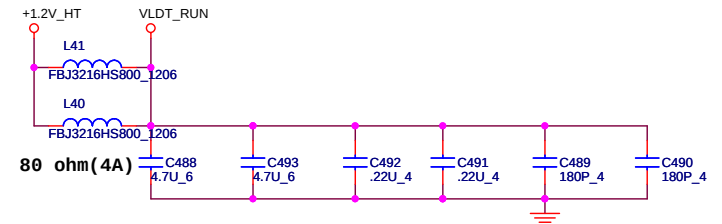


PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1
Processor Socket



LAYOUT: Place bypass cap on topside of board



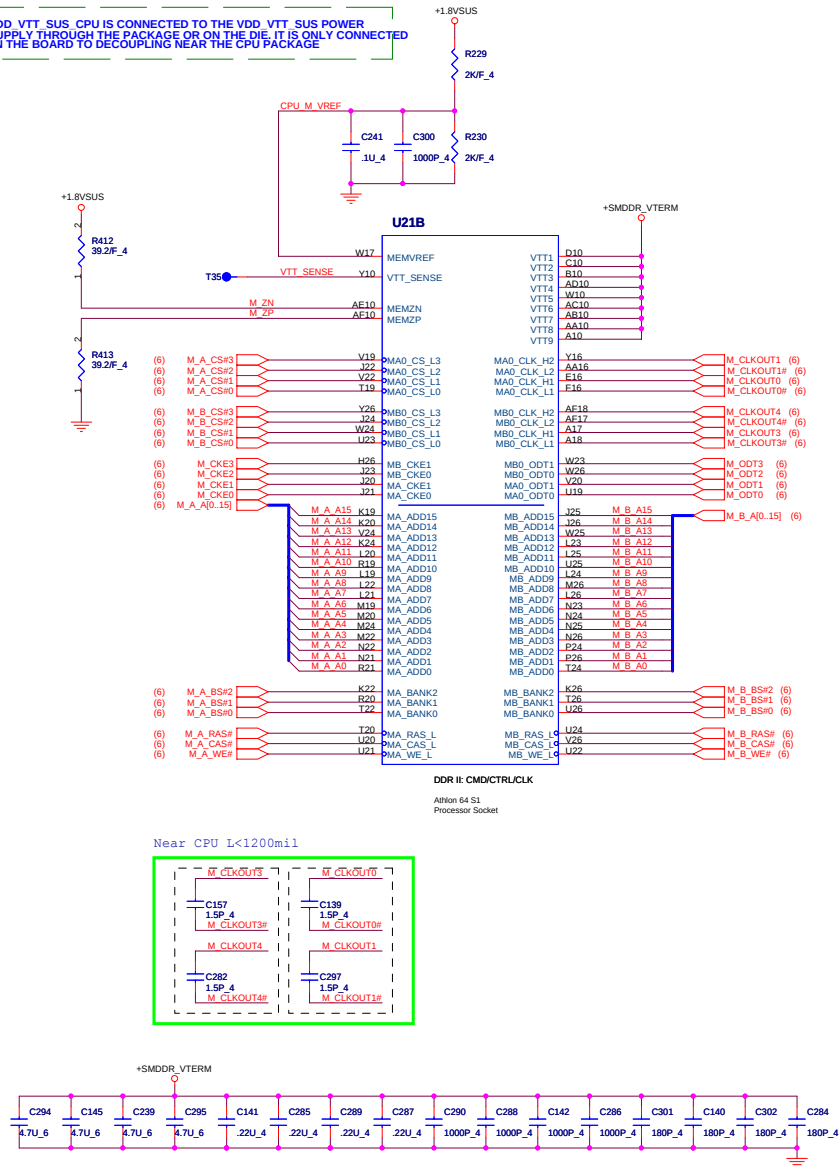
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



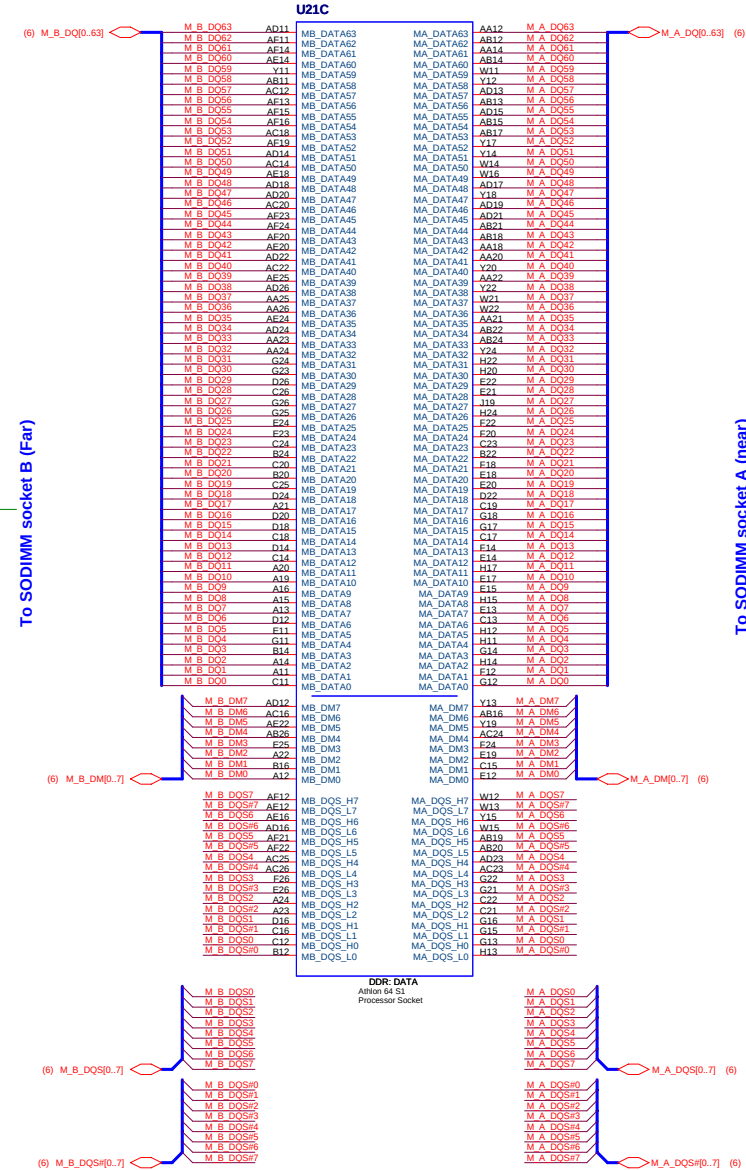
PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 HT I/F	1A
Date:	Wednesday, April 25, 2007	Sheet 2 of 30

VDD VTT SUS CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



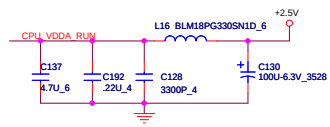
Processor DDR2 Memory Interface



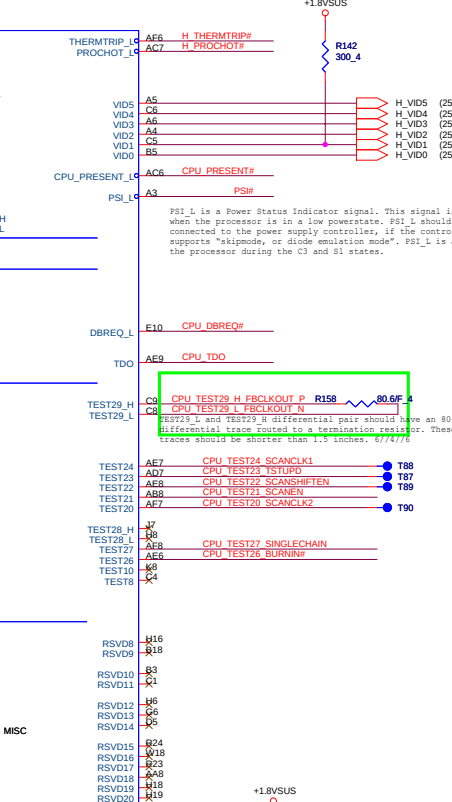
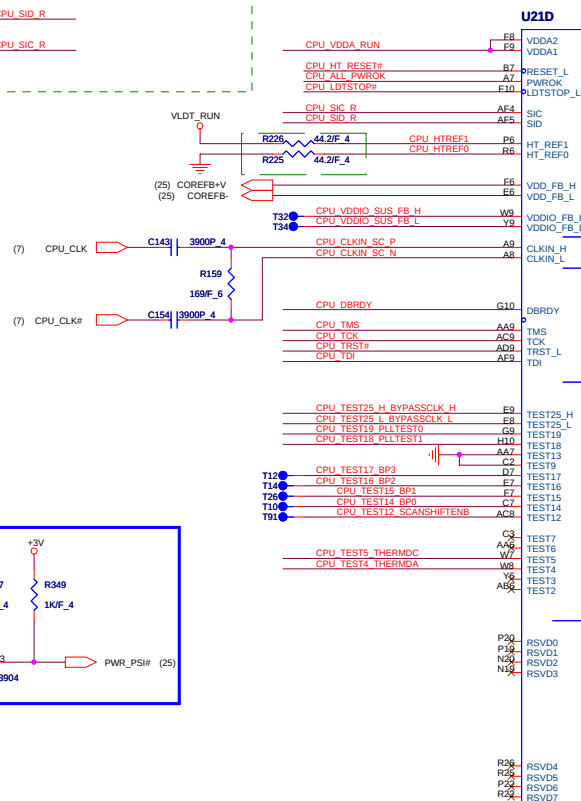
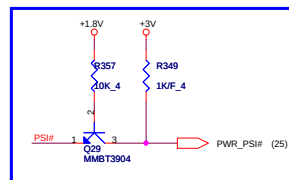
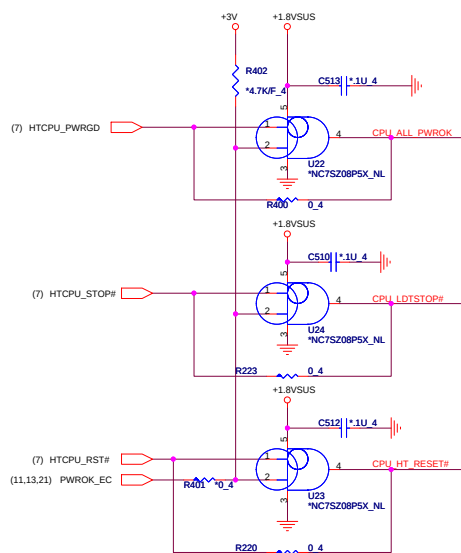
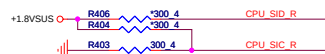
PROJECT : Z03
Quanta Computer Inc.



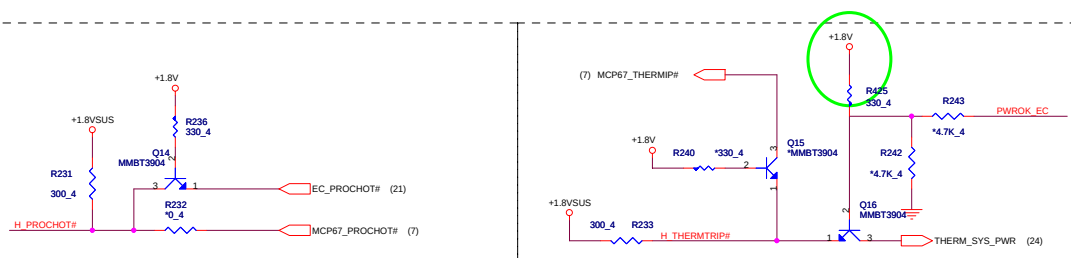
CPU_VDDA_RUN



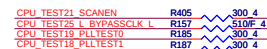
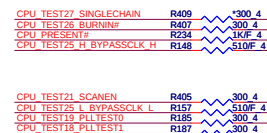
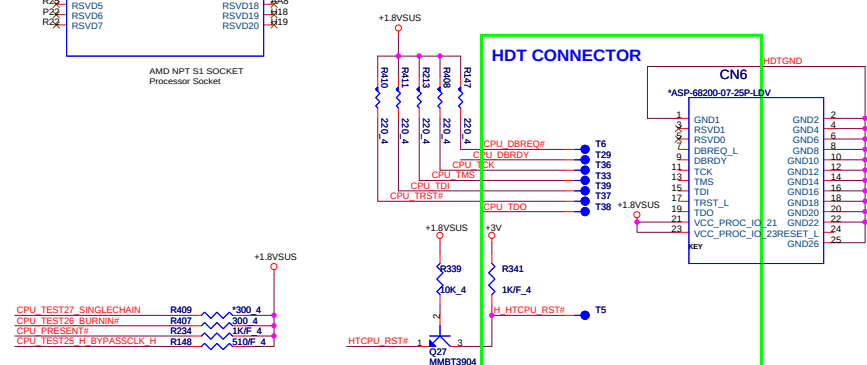
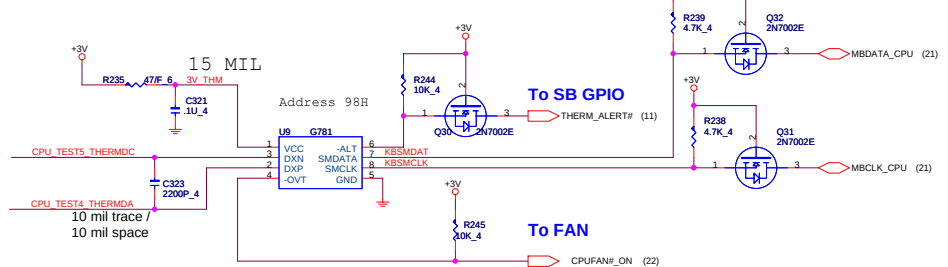
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300- Ω ($\pm 5\%$) pulldown to VSS.



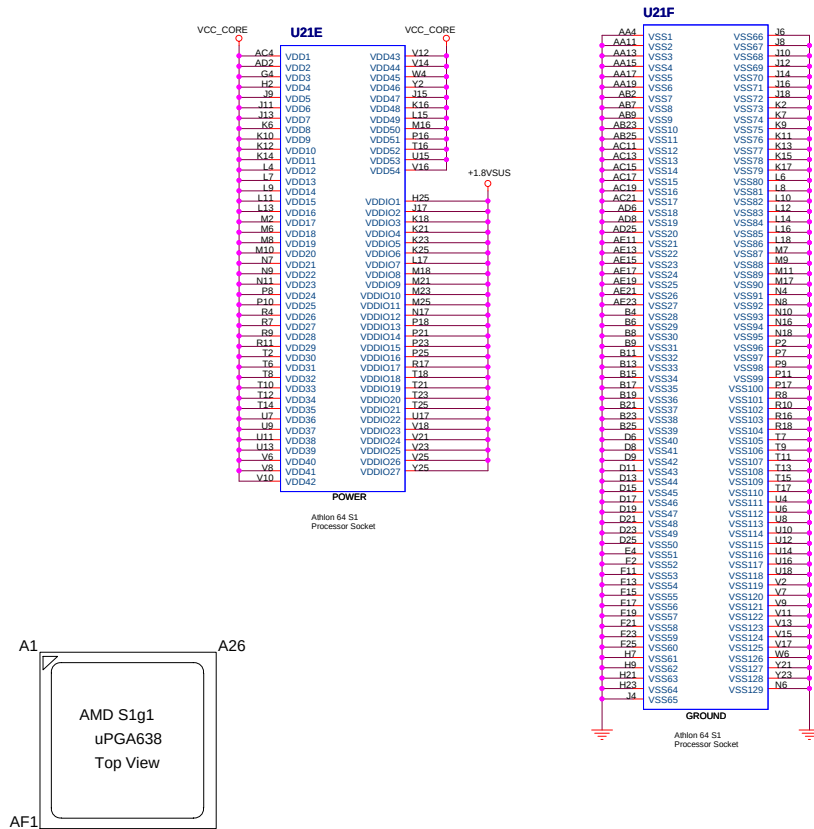
PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

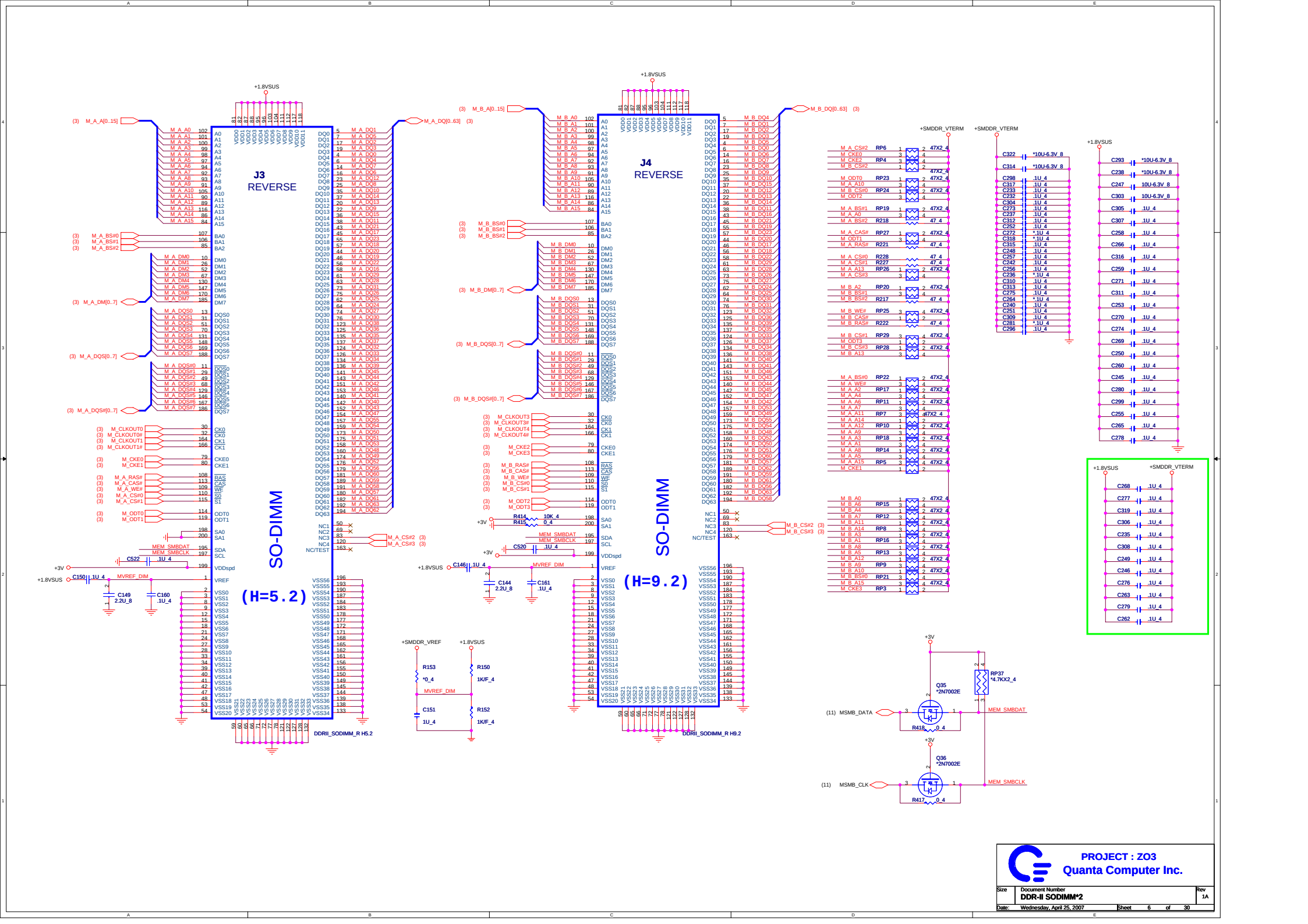


CPU H/W MONITOR

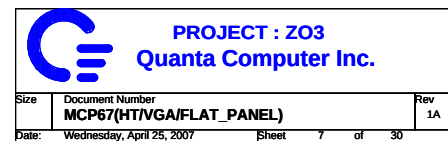
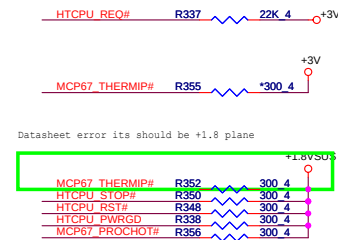


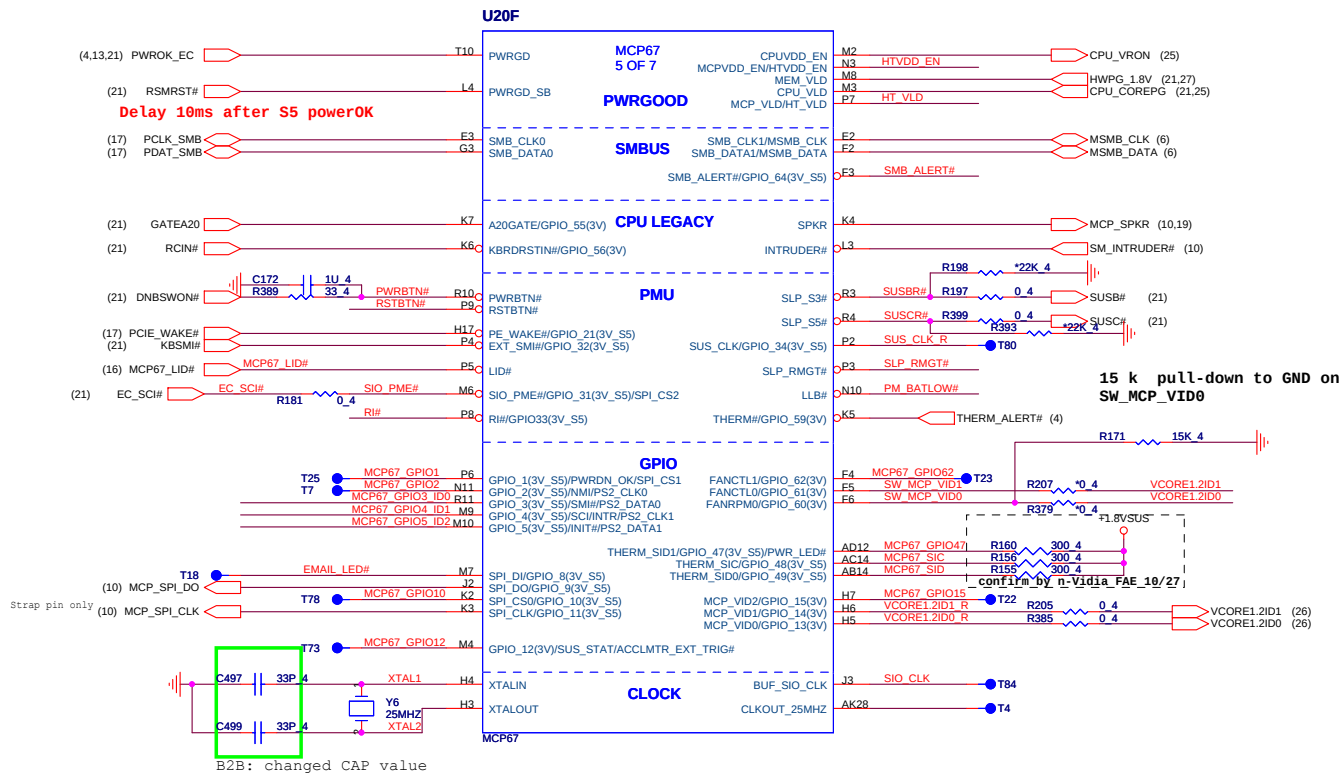
PROCESSOR POWER AND GROUND



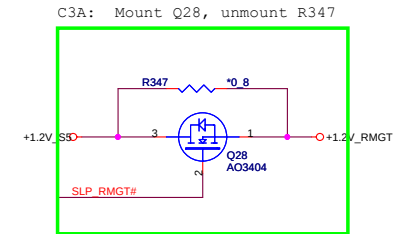


MCP67 Unused UMA Only	
MCP67 Signal Name	Component
RGB_DAC_RSET RGB_DAC_VREF DDC_DATA0A	STUFF STUFF 10K PULLHIGH
TV_DAC_RSET TV_DAC_VREF	STUFF STUFF
IFPAB_RST IFPAB_VPROBE DDC_DATA2 HPLUG_DET3	STUFF STUFF 10K PULLHIGH 22K PULLDOWN
HDMI_RSET HDMI_VPROBE DDC_DATA3_R HDCP_ROM_SDATA HPLUG_DET2_R	STUFF STUFF 10K PULLHIGH 10K PULLHIGH 6.2K PULLDOWN

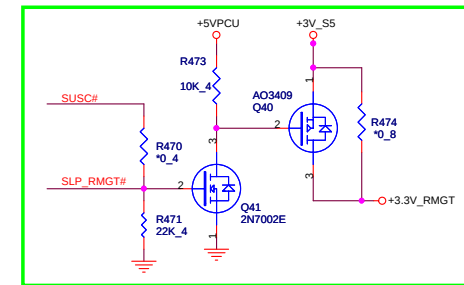




FOR SLEEP MODE CORE POWER CIRCUIT



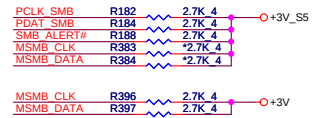
C3A: Mount Q40, Q41, R473, R471, unmount RR74



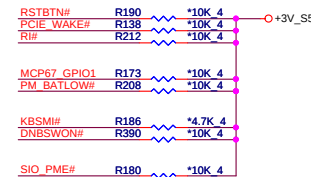
CPU LEGACY PULL-UP



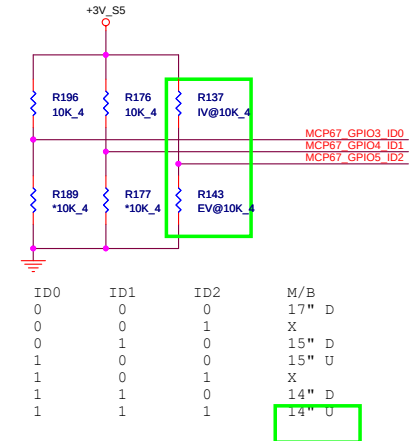
SMB/I2C PULL-UP



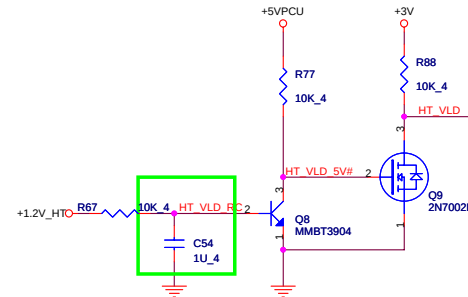
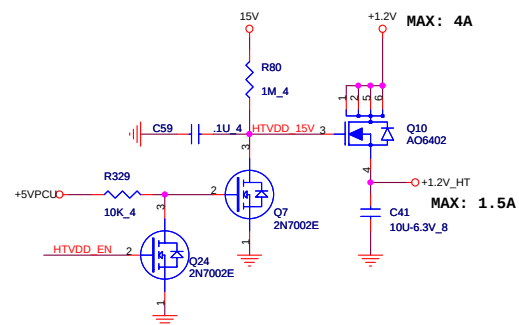
PMU PULL-UP



M/B ID for 14"/15"/17"



HyperTransport Link 1.2 V_HT Power Valid

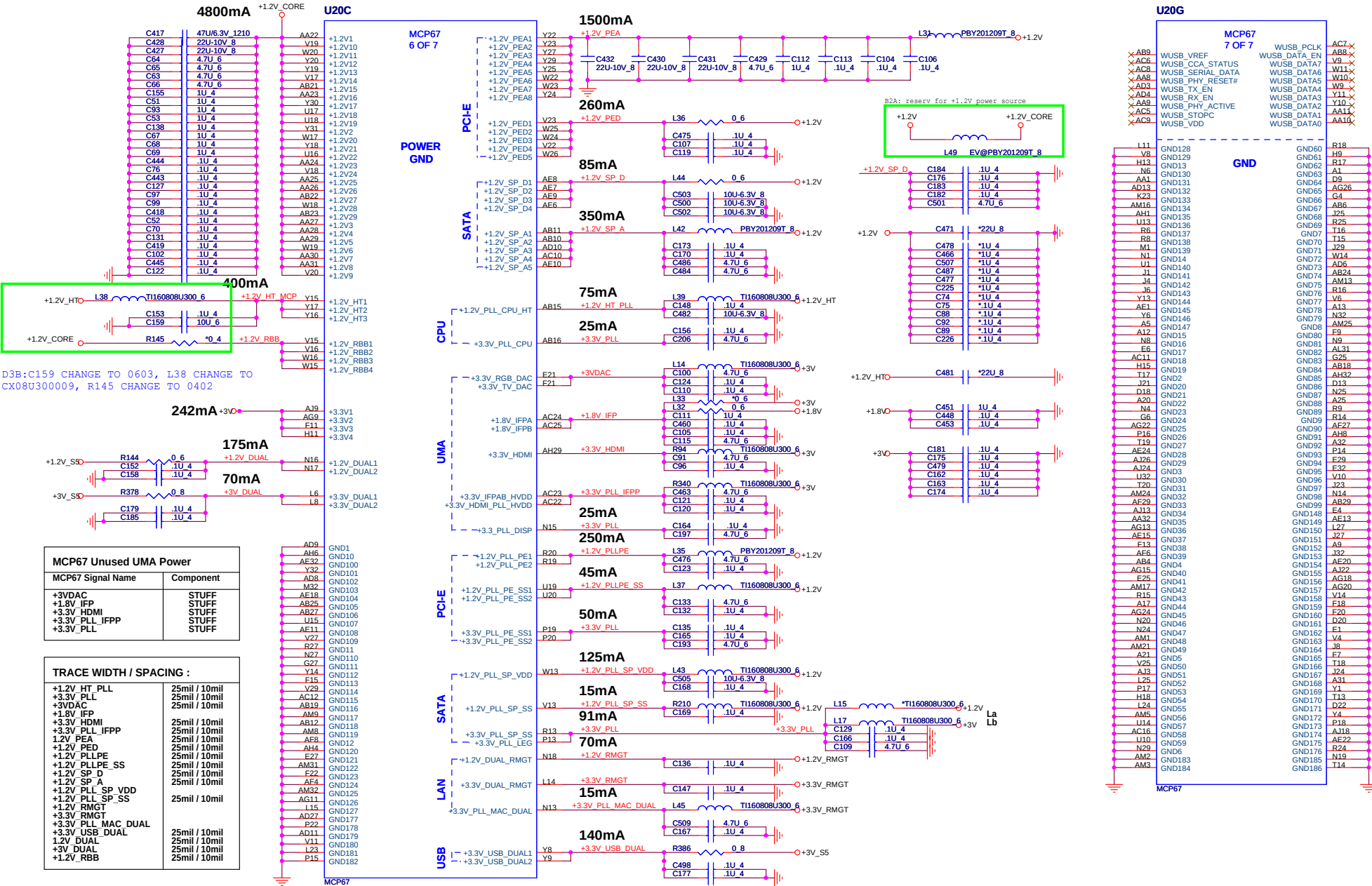


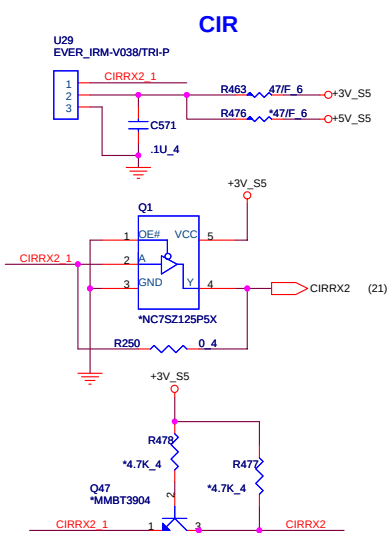
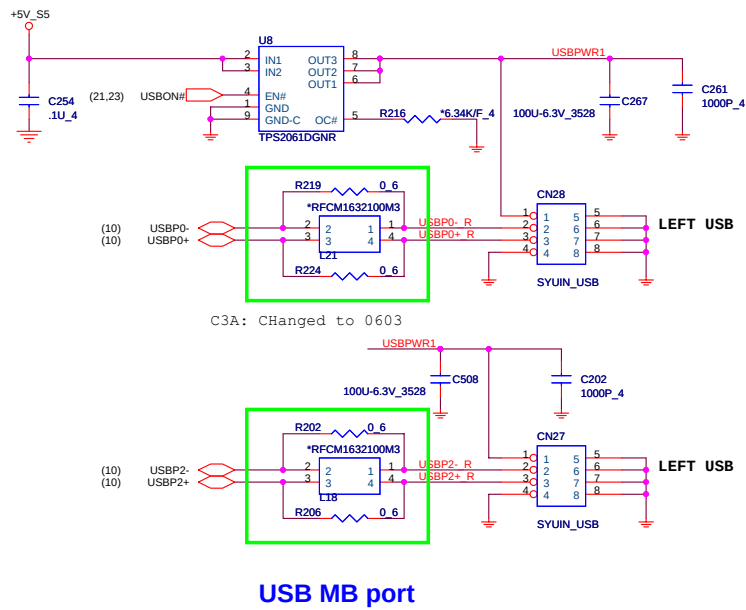
B2B: CHANGED CAP FROM 0.1U TO 1U FOR DELAY HT_VLD

PROJECT : Z03
Quanta Computer Inc.

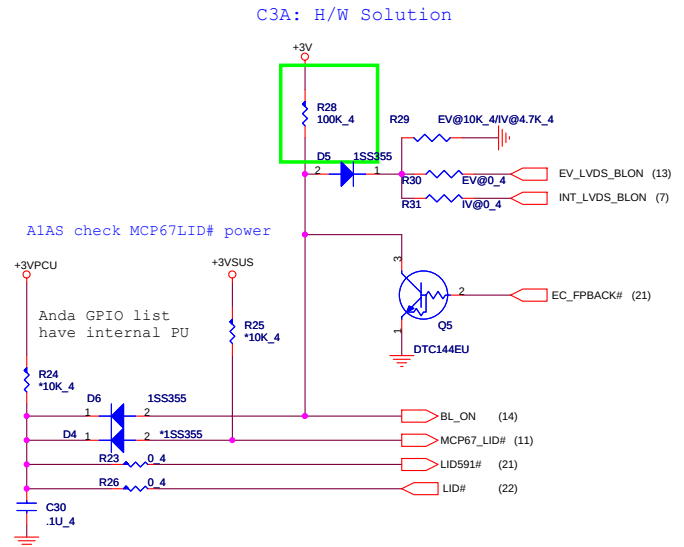
Size	Document Number	Rev
	MCP67(SMB/GPIO/CLK/PMU)	1A
Date:	Wednesday, April 25, 2007	Sheet 11 of 30

MCP67 POWER PLANE/GND & BYPASS

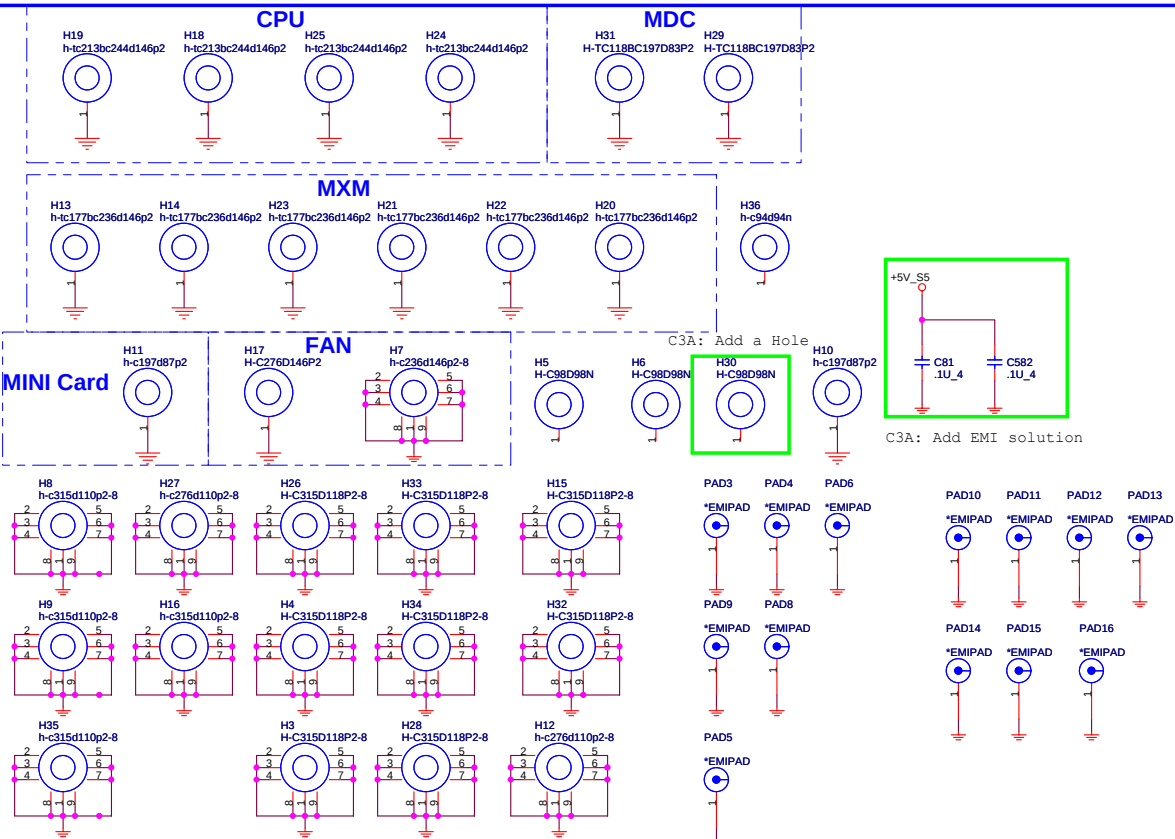
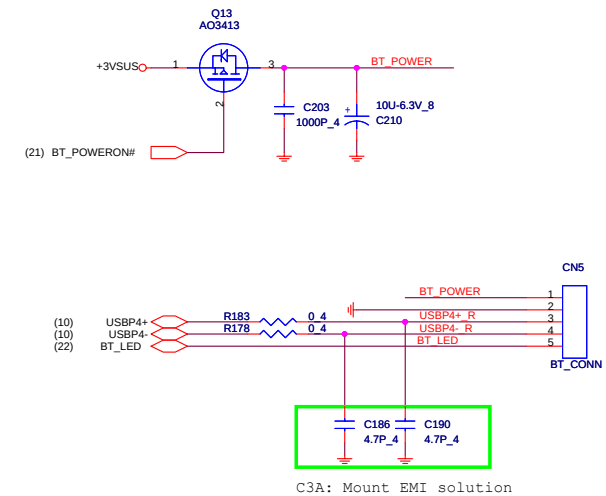




LID SWITCH

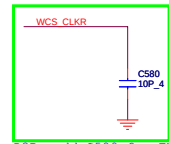


BLUETOOTH MODULE CONNECTOR

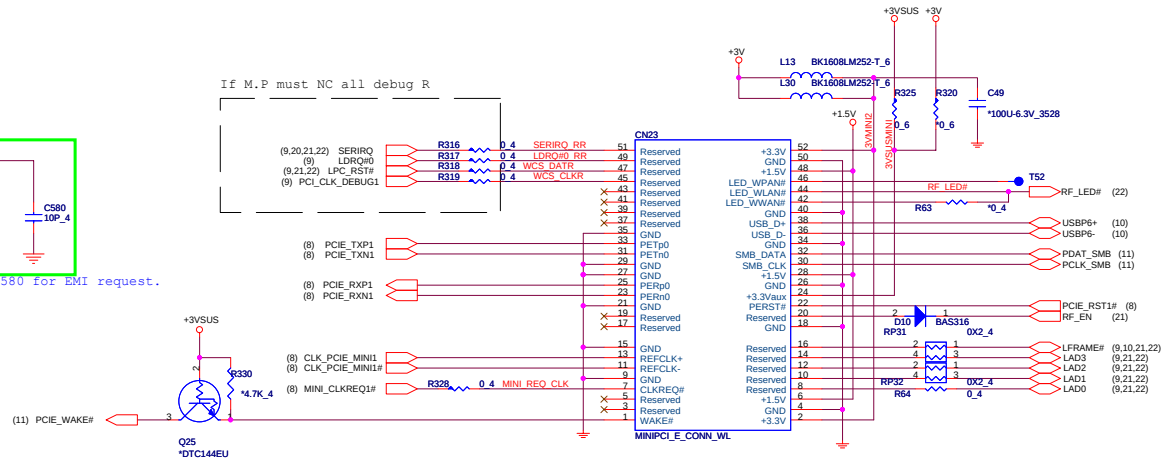


PROJECT : ZO3
Quanta Computer Inc.

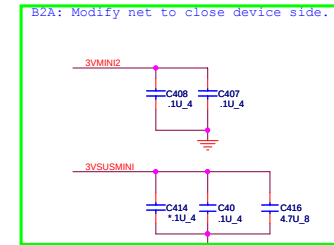
MINI-Card



D3B: add C580 for EMI request.



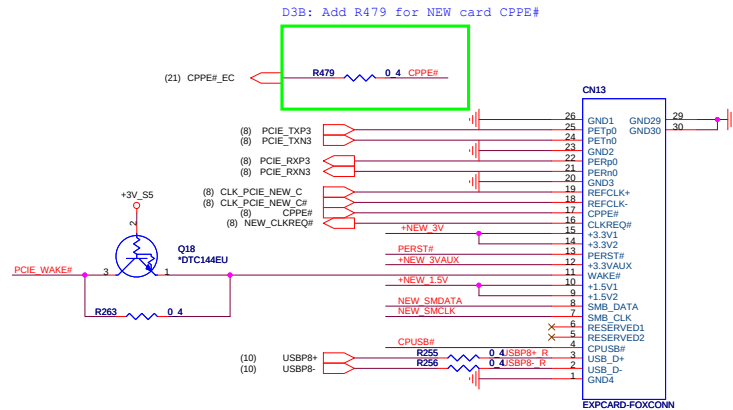
Need reserve 3G pin define
Check Footprint



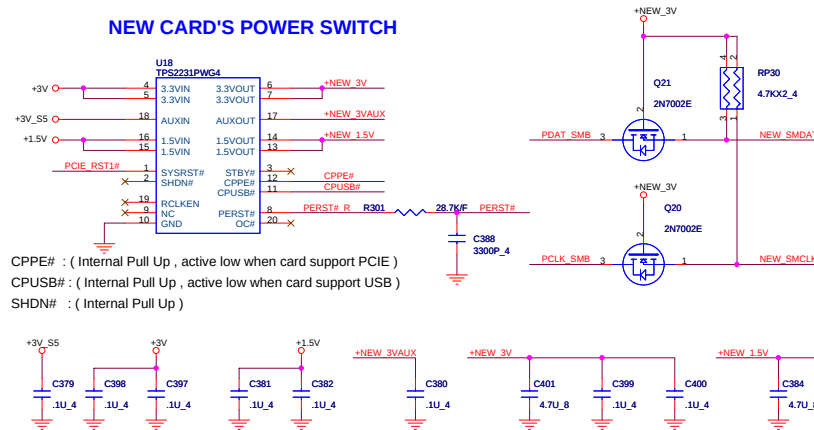
B2A: Modify net to close device side.

New card

D3B: Add R479 for NEW card CPPE#



NEW CARD'S POWER SWITCH



The schematic diagram illustrates the connection of a SATA-HDD to a SATA controller. The SATA controller is represented by a block with pins 1 through 24. The SATA-HDD is connected to the controller via a SATA-to-HDD adapter. The diagram shows the connection of SATA signals (TXP0, RXN0, TXN0, RXN0) and power (3.3V, 5V, GND) to the SATA controller. It includes components like resistors (R424, R257), capacitors (C353, C354, C519, C518, C332, C337, C340, C333), and a 100u-6.3V_3528 capacitor. The SATA-HDD is connected to the SATA controller via a SATA-to-HDD adapter.

TP CONN

TP VCC: +5V, L46 BKP1608HS181T_6_1.5A, 25mil, TP VCC, C511 .1uF 4

TPDATA_R: L19 LZA10-2ACB104MT 6 0.1A, L20 LZA10-2ACB104MT 6 0.1A, TPDATA_R

TPCLK_R: TPCLK_R

EMI near CN15:

- TPDATA C231 12P 4
- TPCLK C224 12P 4

C3A: Add EMI solution

RIGHT#

SCR RIGHT#

SCR UP#

SCR LEFT#

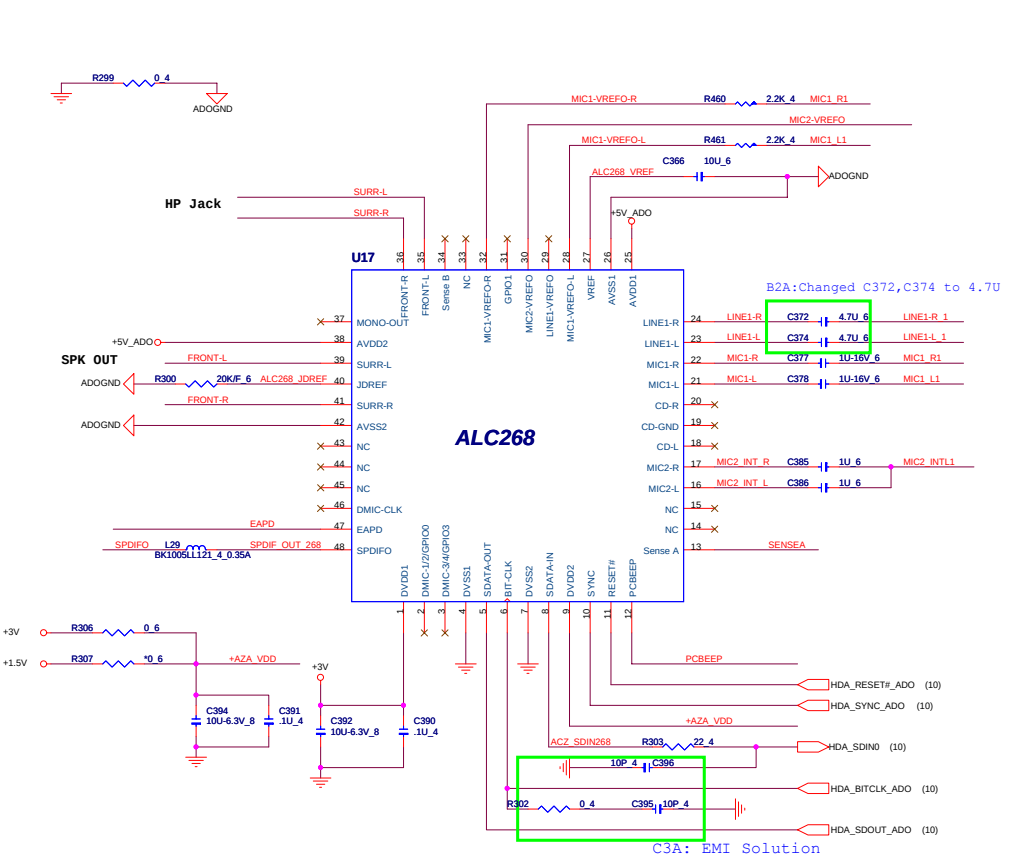
SCR DN#

LEFT#

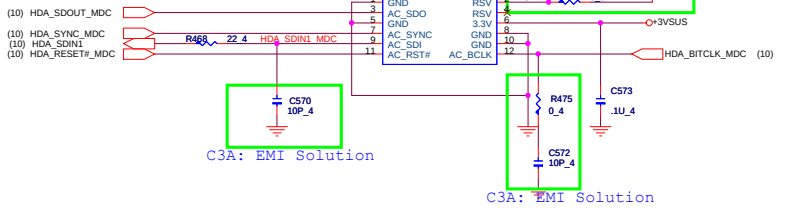
TOUCH_PAD_TP_12P

The schematic diagram illustrates the internal components and connections of the PDA module. Key components include the DTC144EU transistor (Q19), a 10K_4 resistor (R290), and a 100P_4 capacitor (C330). The module is connected to the PDD module via a 10K_4 resistor (R271) and a 100P_4 capacitor (C330). The PDA module also includes a 10K_4 resistor (R274) and a 100P_4 capacitor (C330). The PDCS module includes a 100P_4 capacitor (C330), a 10K_4 resistor (R254), and a 100P_4 capacitor (C330). The diagram shows the internal connections and the external connections to the PDD module and the PDCS module.

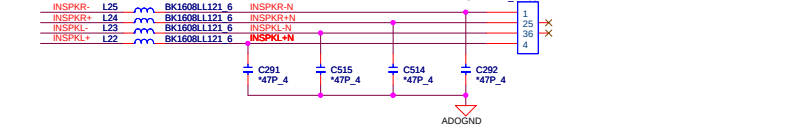
CODEC(ALC268)



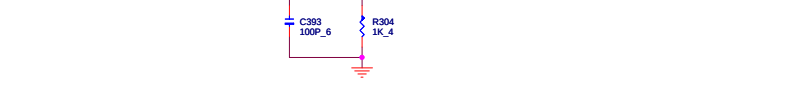
MDC



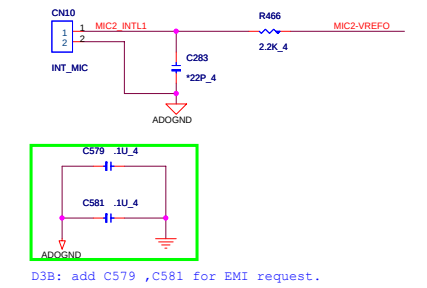
SPK



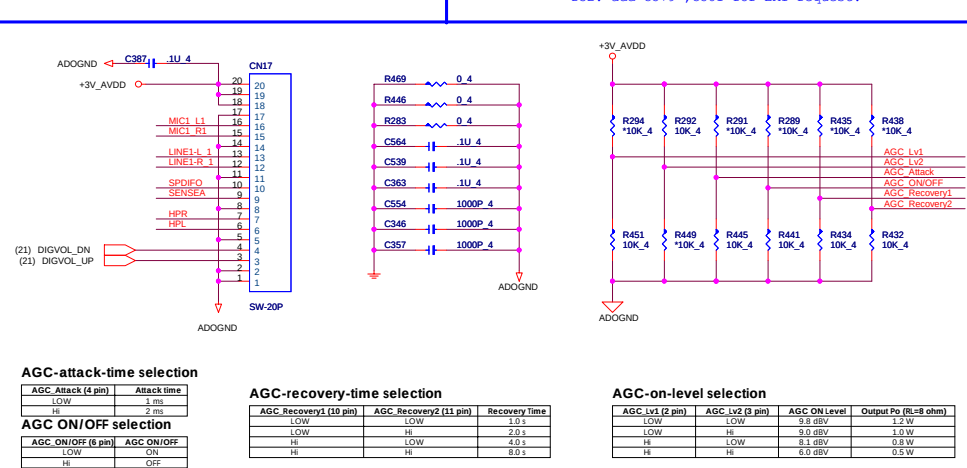
Beep



INT MIC array

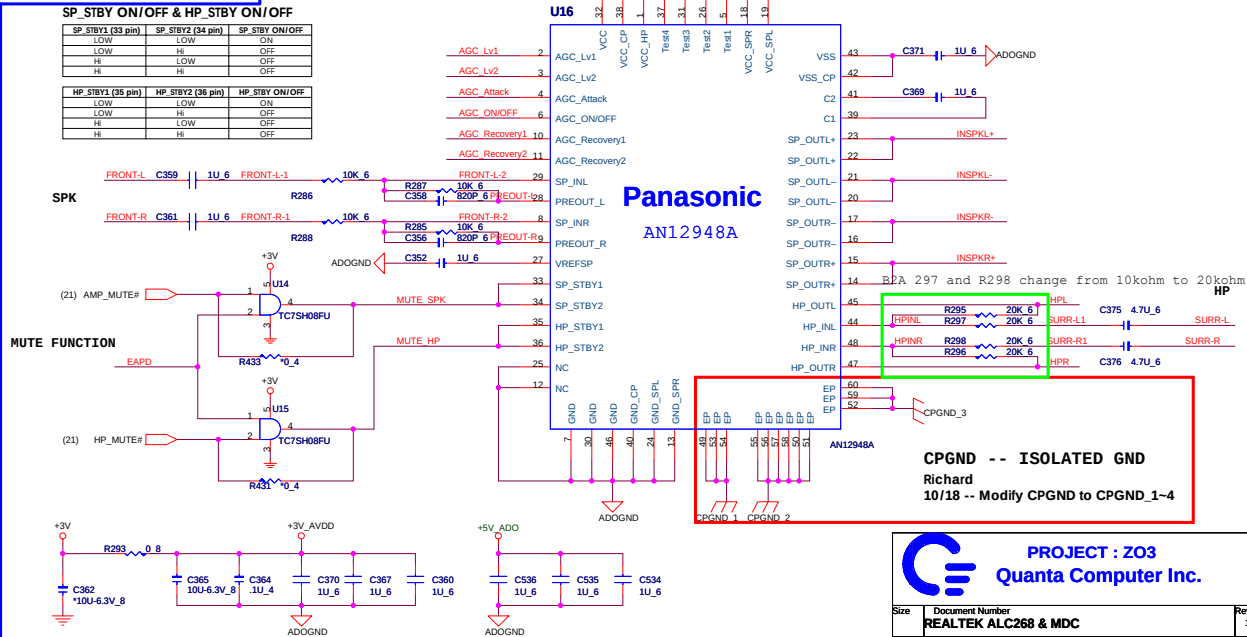


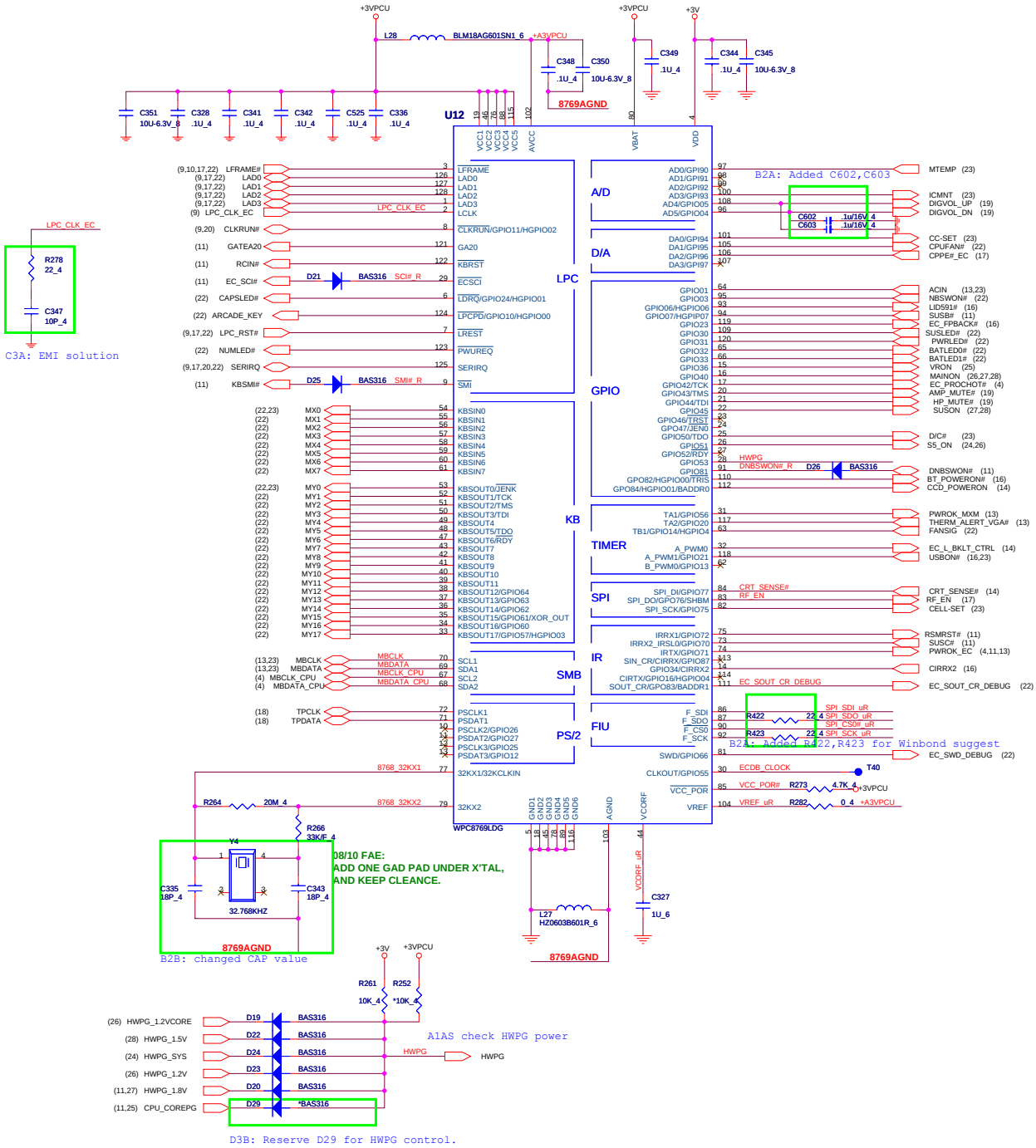
CODEC(ALC268) Power



Panasonic

AN12948A

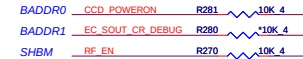




I/O ADDRESS SETTING

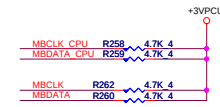
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

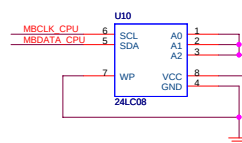


1/13 Confirm by vendor mail :
Disabled ('1') if using FW device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

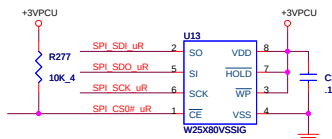
SMBUS PULL-UP



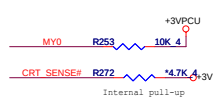
ACER ID



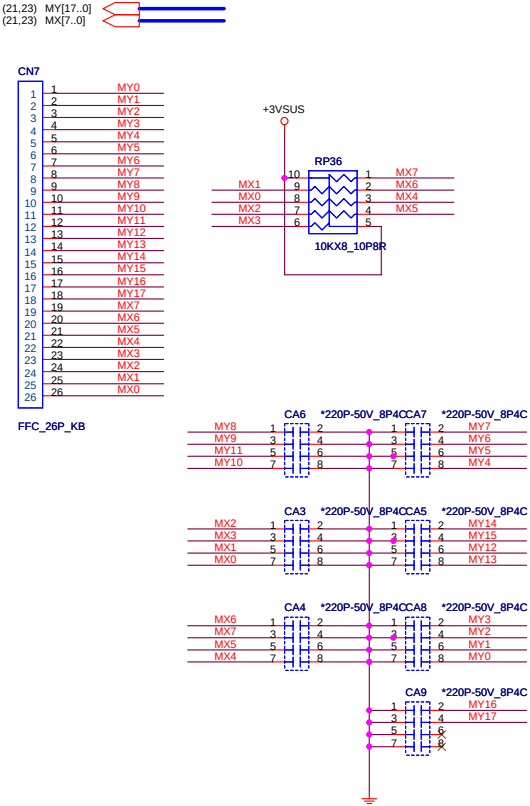
SPI FLASH



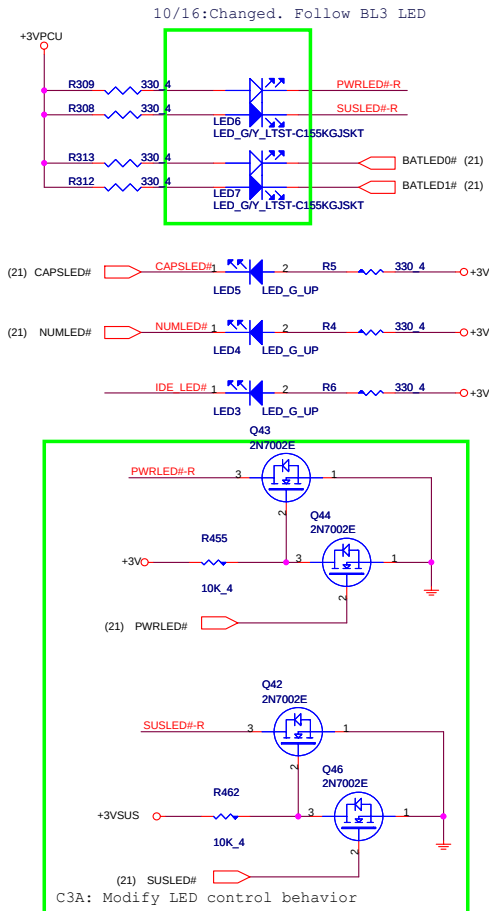
INTERNAL KEYBOARD STRIP SET



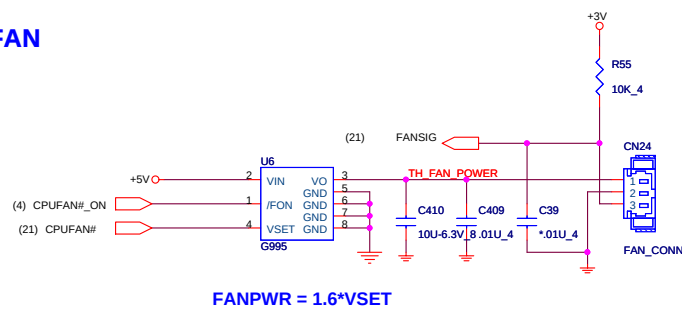
INT K/B



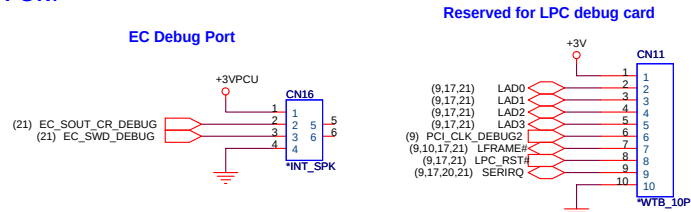
LED



CPU FAN



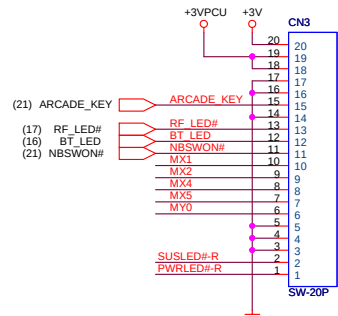
DEBUG PORT



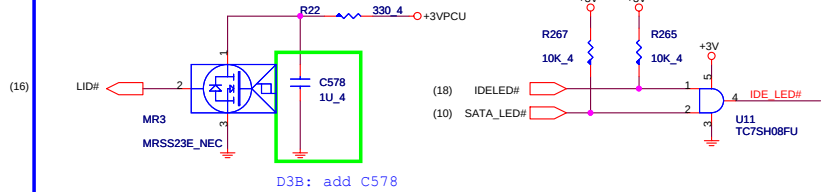
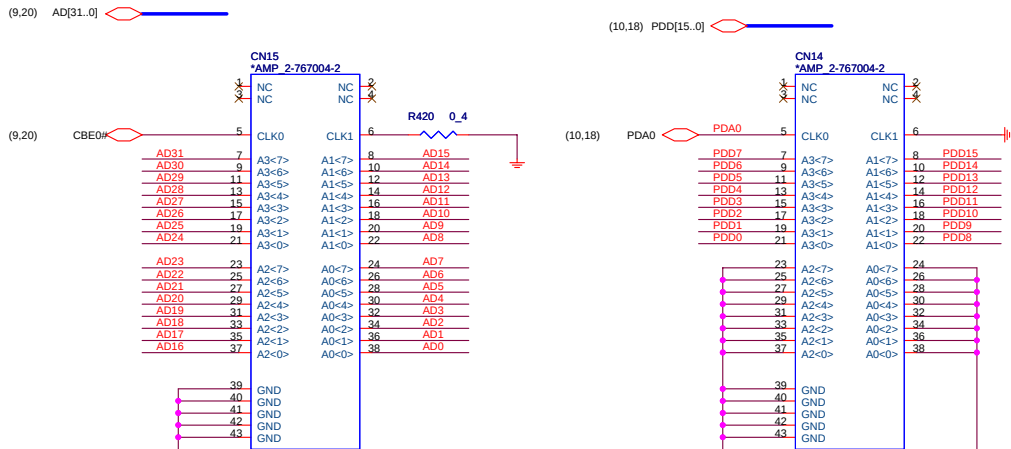
Button

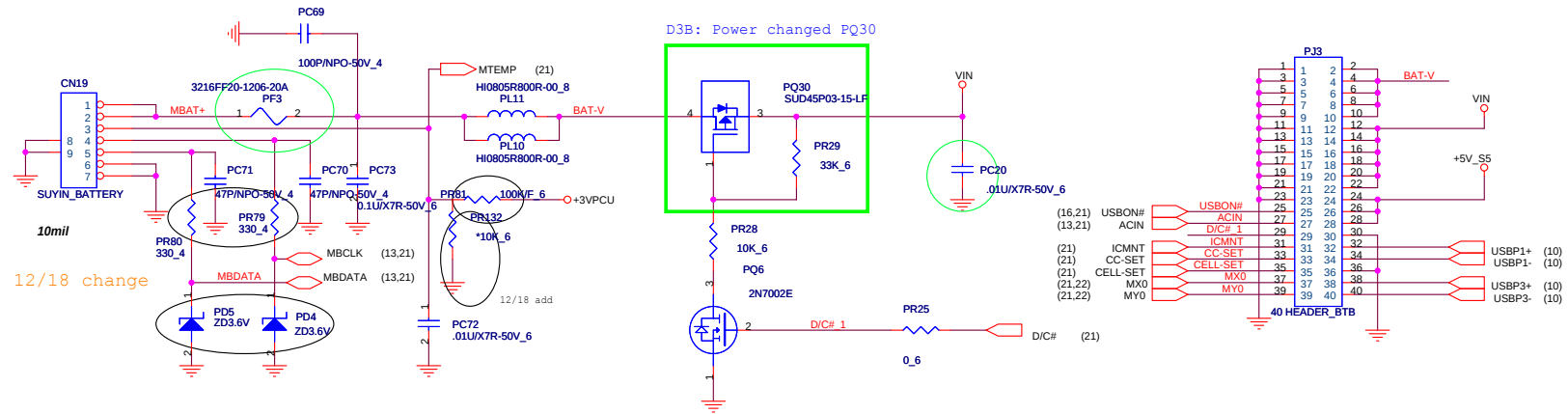
BUTTON MATRIX

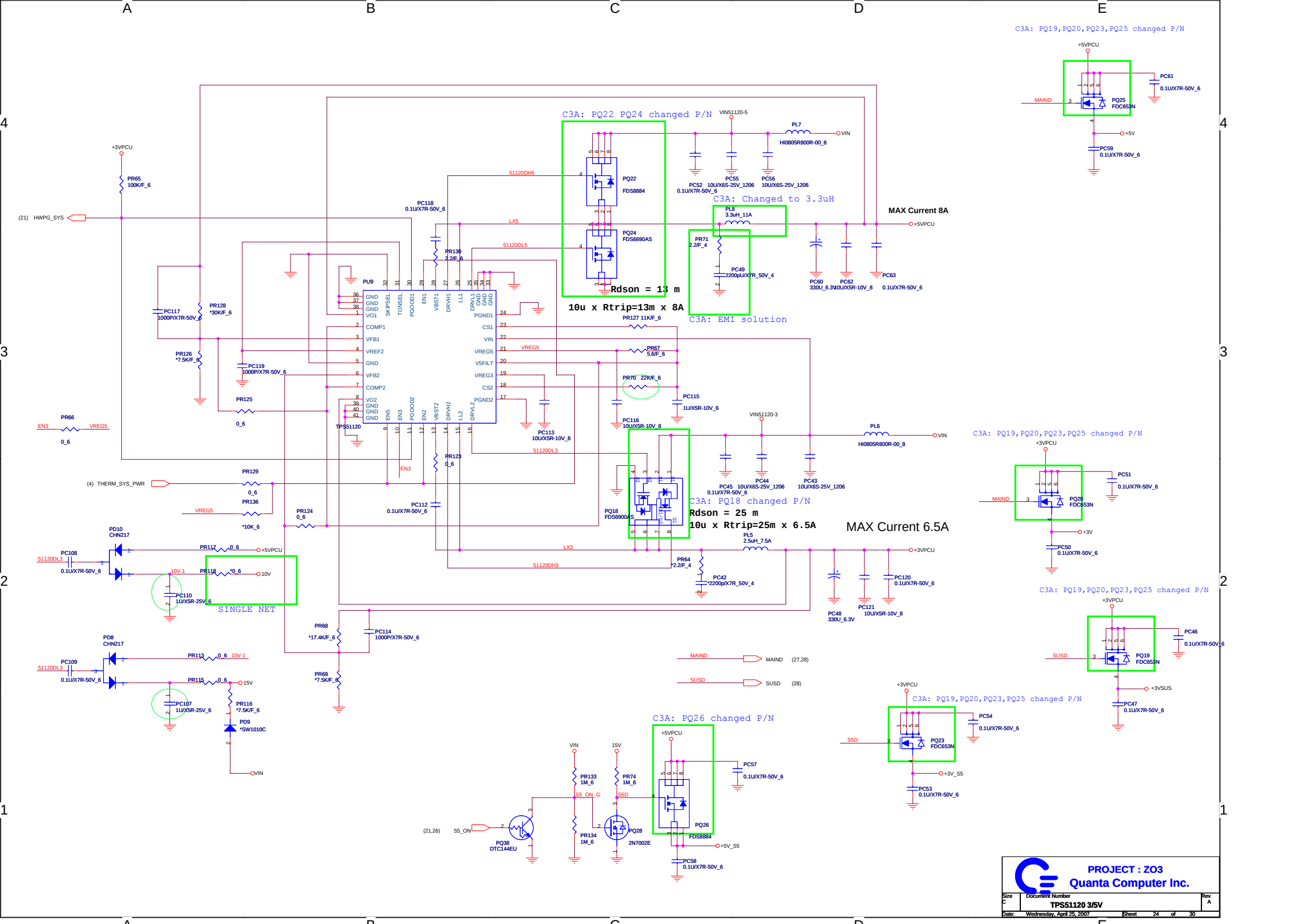
	MY0
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH

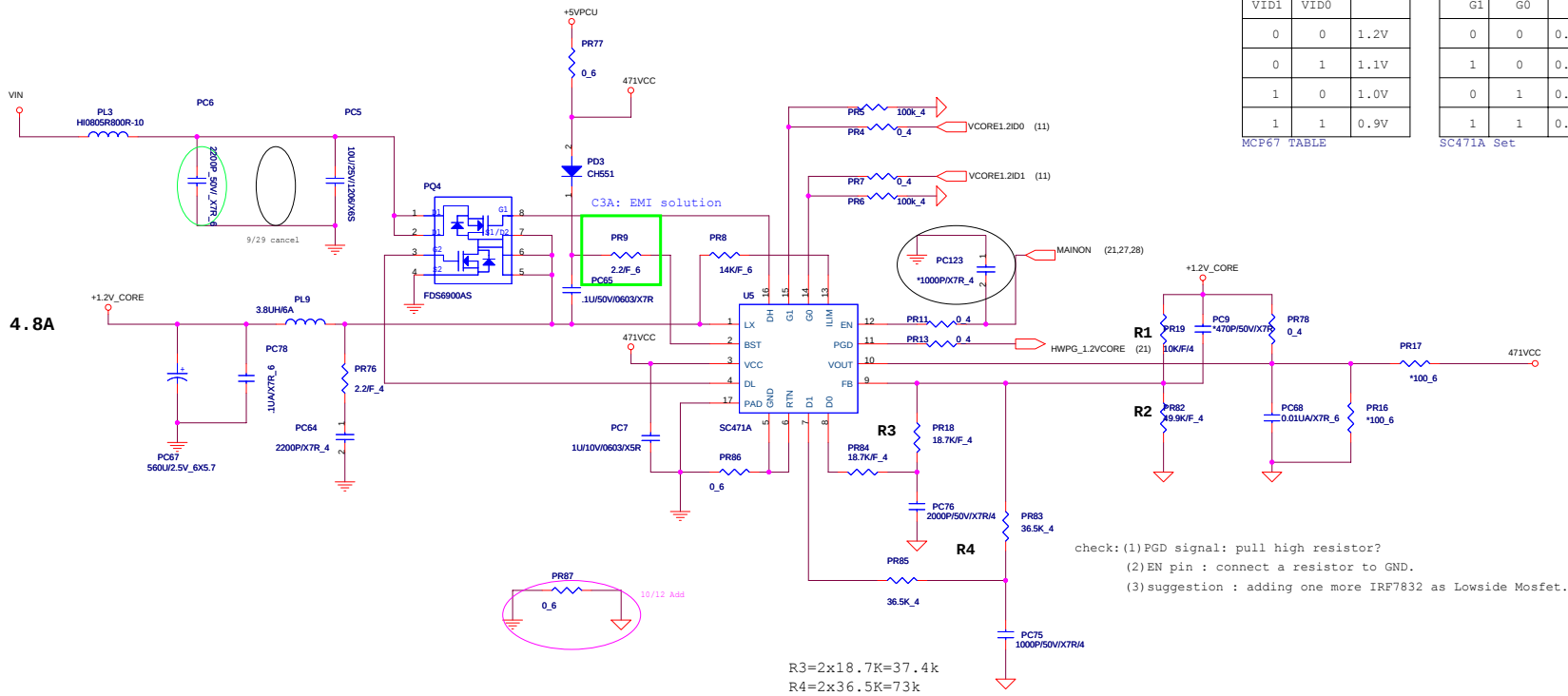


Debug









B2B: FOR UMA ONLY

