

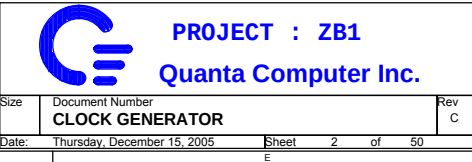
ZB1 SYSTEM BLOCK DIAGRAM

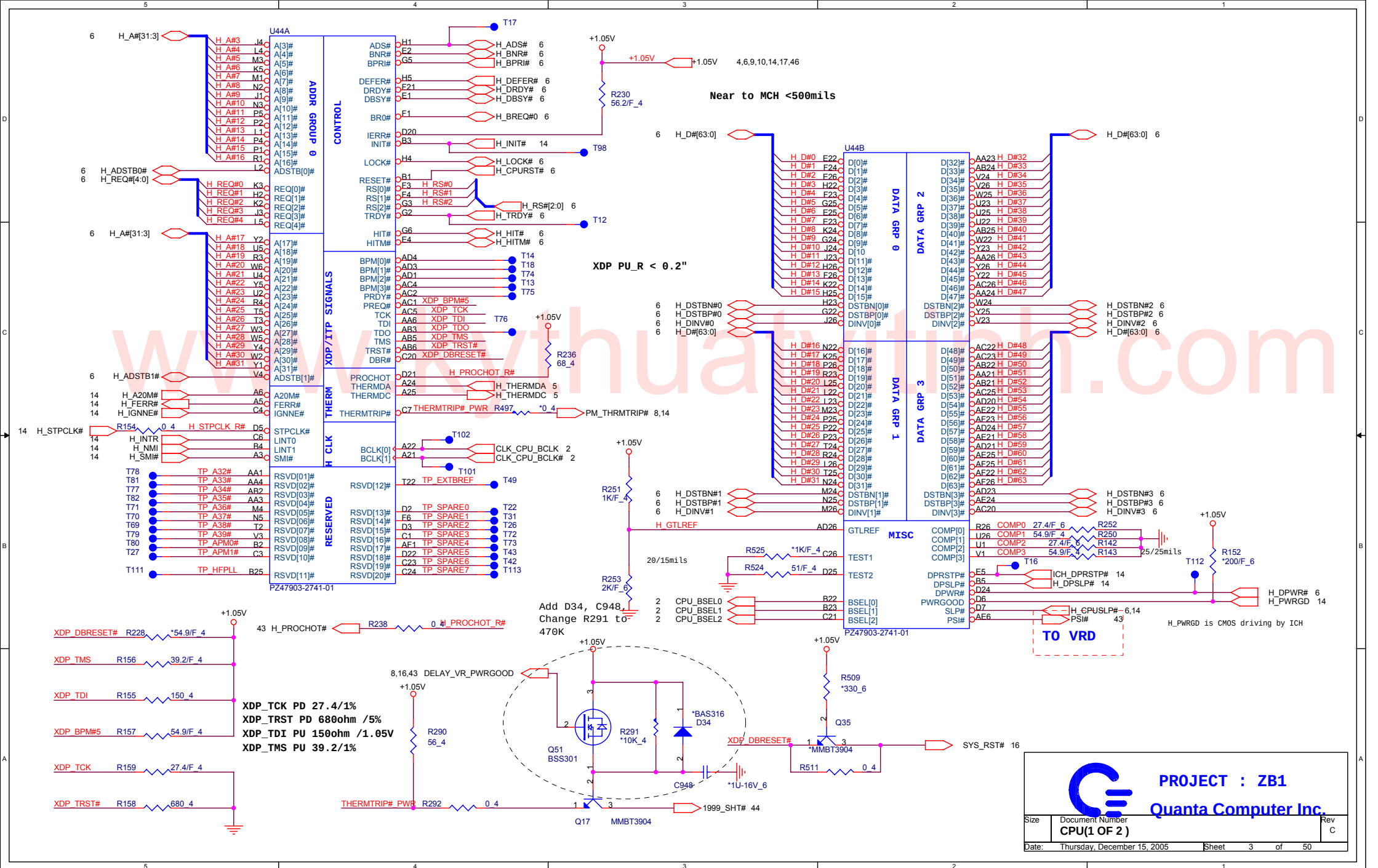
The diagram illustrates the system architecture of the ZB1 laptop. Key components and their connections include:

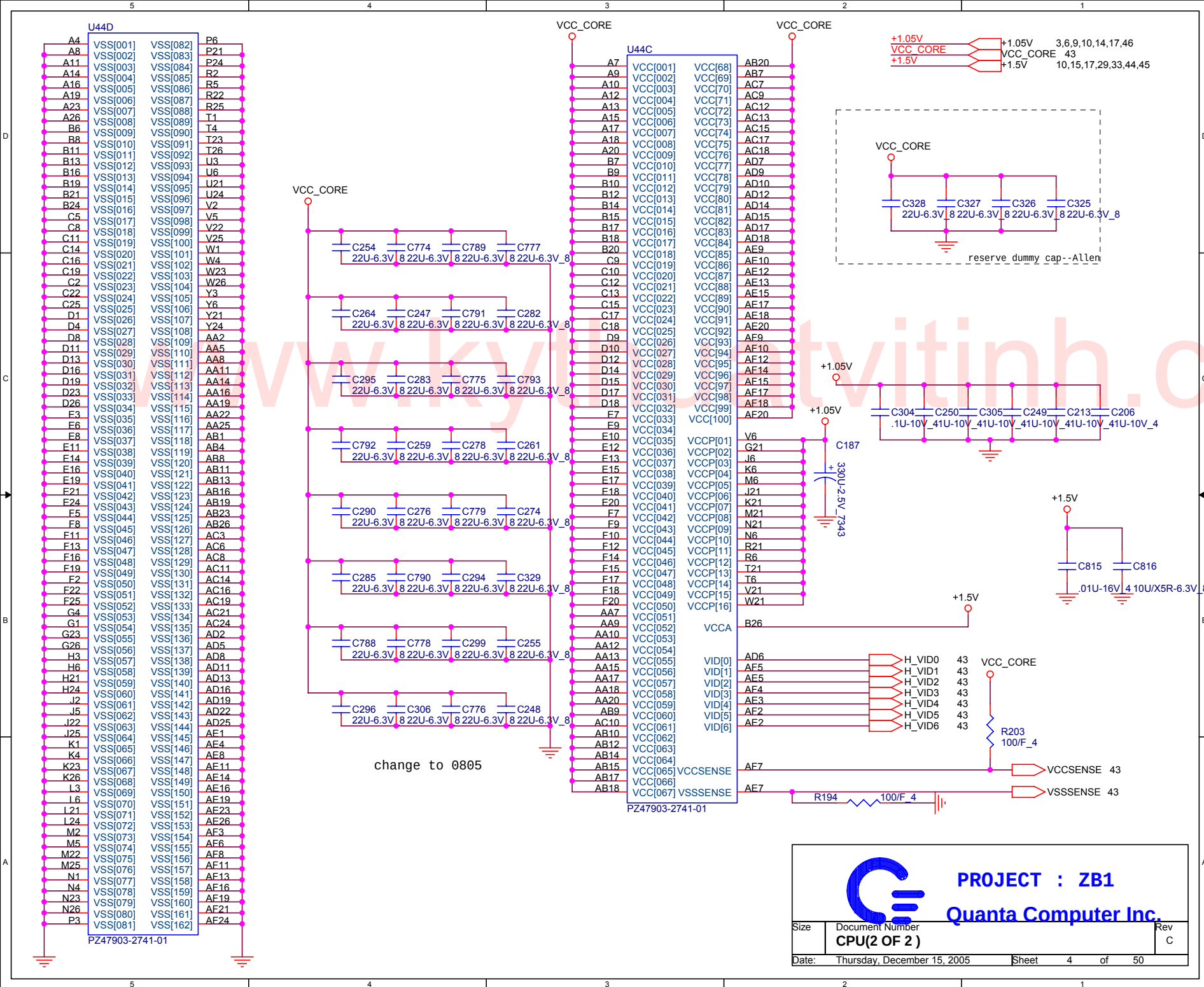
- Processor:** Yonah/Merom 479 uFCPGA U44 (P3, P4) connected to the FSB.
- Chipset:** CALISTOGA 945GM/PM 1466 FCBGA U43 (P6, P7, P8, P9, P10, P11) connected to the FSB and ICH7M.
- Southbridge:** ICH7M 82801 652 BGA U49 (P14, P15, P16, P17) connected to the CALISTOGA and various peripherals.
- Memory:** Dual Channel DDR2 (533/667 Mhz) consisting of DDR II SODIMM0 CN36 and DDR II SODIMM1 CN37 (P12, P13).
- Storage:** HDD Master CN41 (P35) and ODD Slave CN24 (P35) connected via SATA0 and SATA1.
- Audio:** Azalia Audio Controller ALC883 (P36) connected to the ICH7M and various audio components like the Speaker (P37), Phone Jack, and Line in.
- Network:** Broadcom 5789/87/88 (P27) connected to the ICH7M via PCI-Express.
- Peripherals:** Various other components like the DVI/7307 Chronitel (P41), TVOUT (P25), TFT LCD Panel (P25), CRT (P26), Bluetooth (P29), USB Port x 4 (P29), CCD (P29), Audio Amplifier (P37), Int MIC (P36), MIC Jack, Line in, MDC 1.5 (P36), Touch Pad (Dual-Point) (P40), Super I/O SMSC SIO1000 (P38), FIR CIR, and Fan Header (P5, P40).

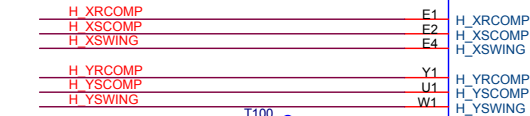
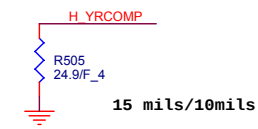
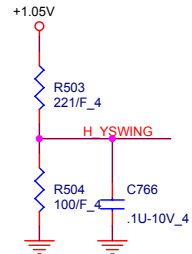
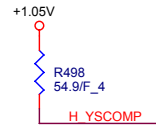
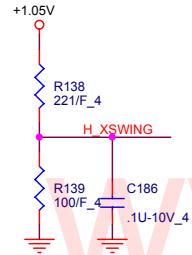
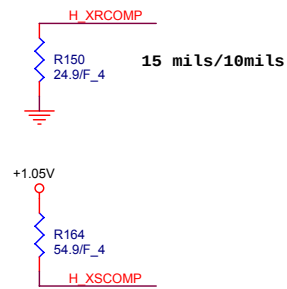
Digitally signed by dd
 DN: cn=dd, o=dd, ou=dd
 email=dd@yahoo.com
 c=US
 Date: 2009.11.29 07:50:51 +07'00'

Diễn Đàn
KyThuatViTinh.Com

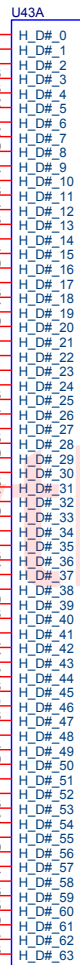




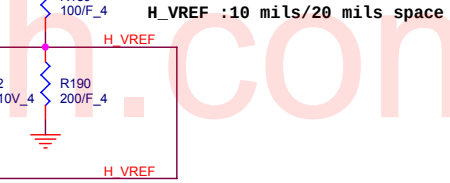
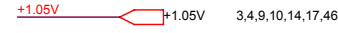
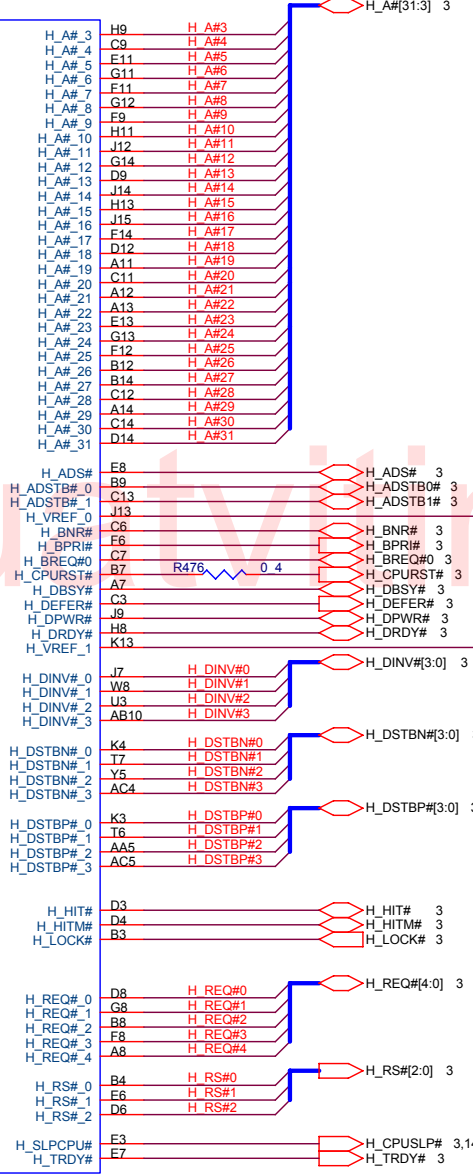




Short Stub < 100mils
extract from same point



HOST

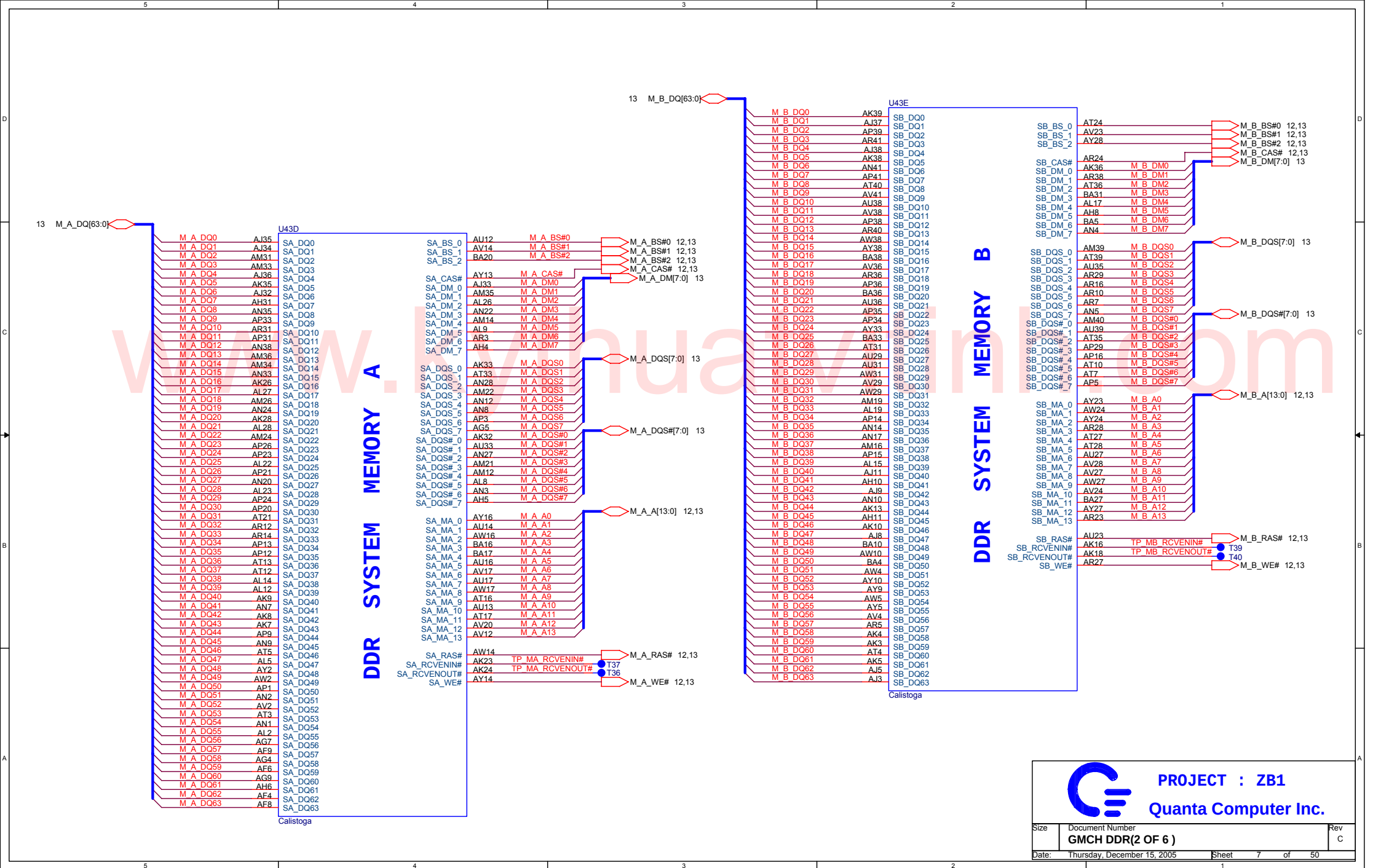


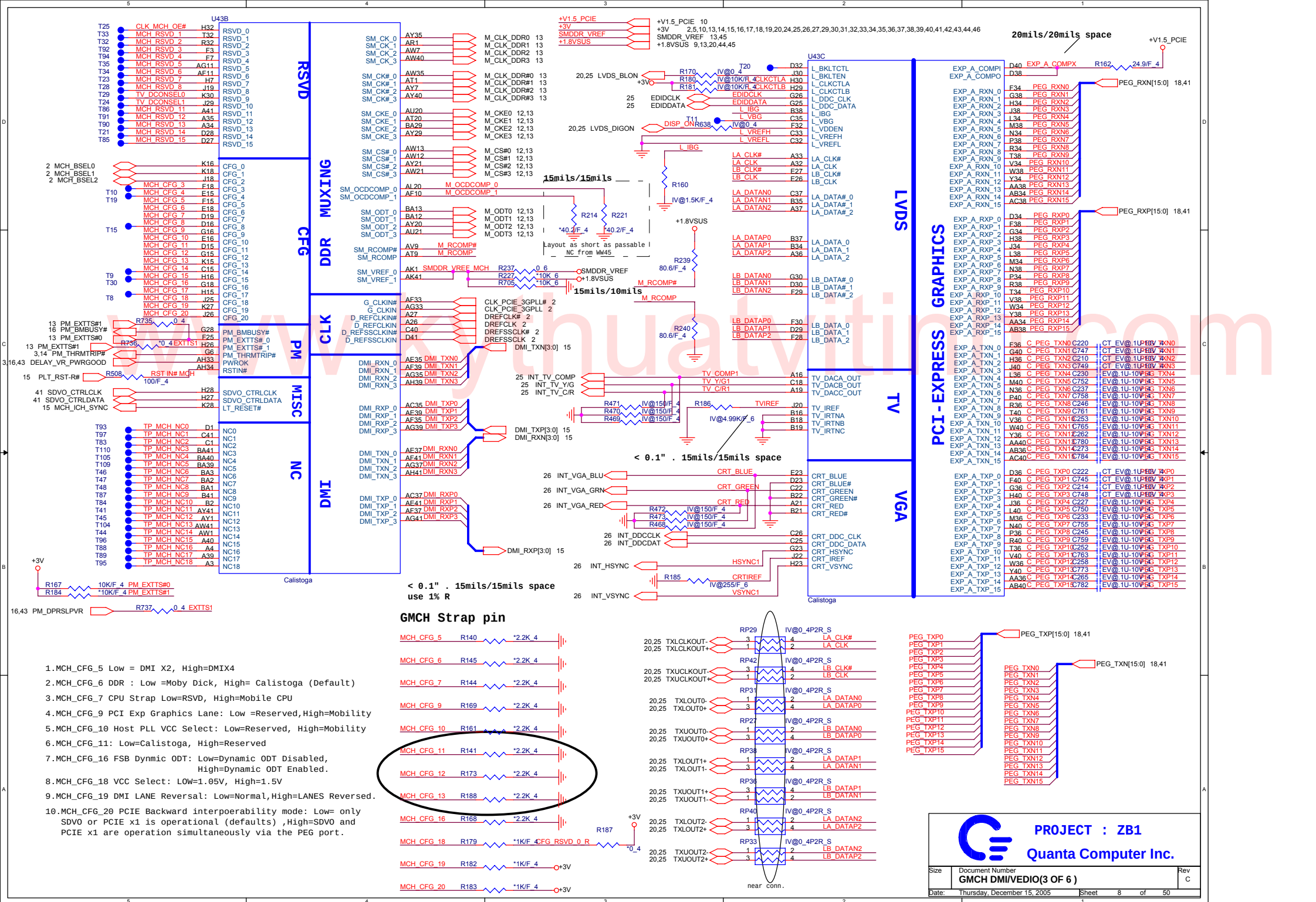
COMPONENTS	P/N
945GM	AJ009450T04
945PM	AJ009450T12

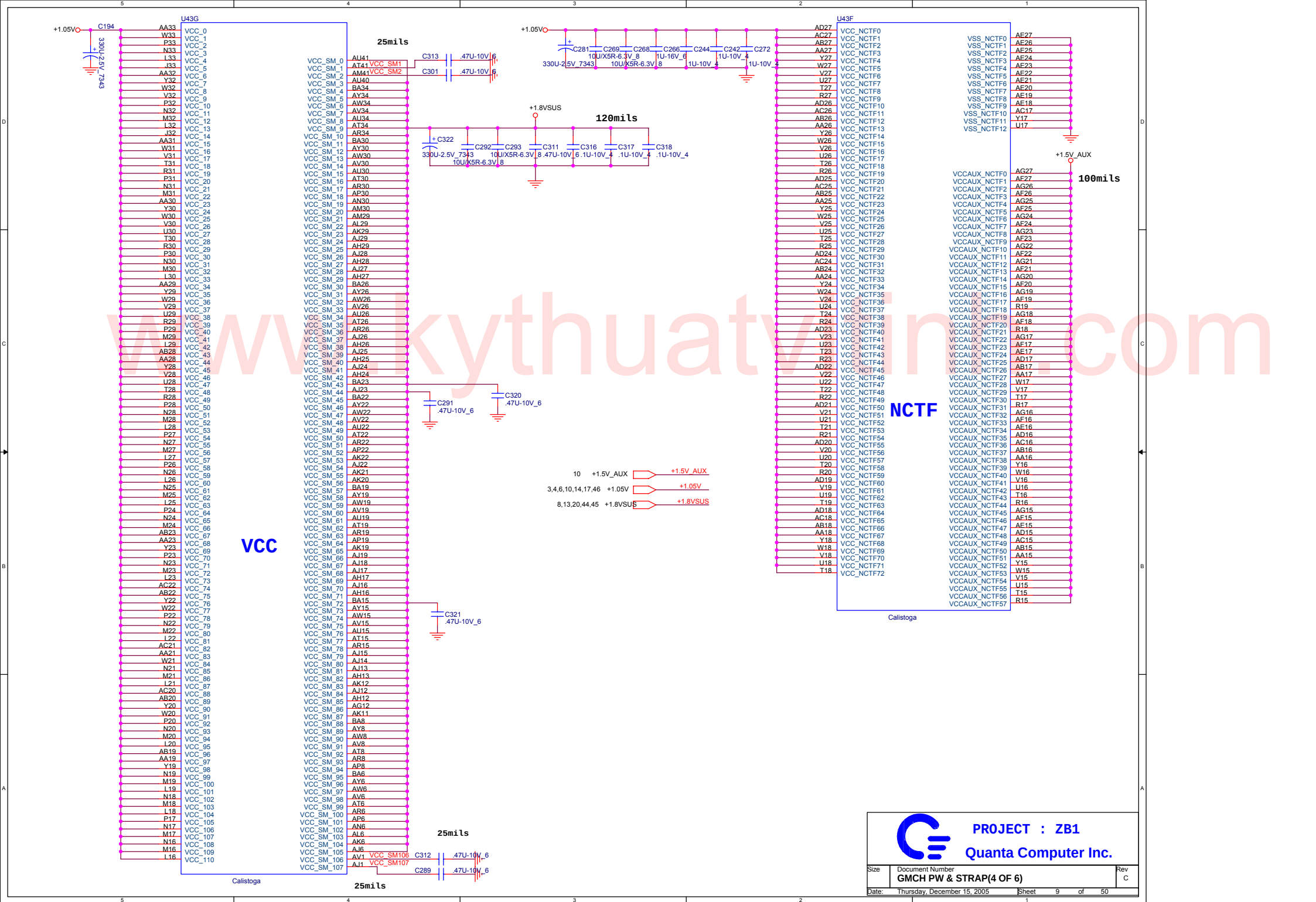


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U43I		
AC41	VSS_0	AK34
AA41	VSS_1	AG34
W41	VSS_2	AF34
T41	VSS_3	AE34
P41	VSS_4	AC34
M41	VSS_5	C34
J41	VSS_6	AW33
F41	VSS_7	AV33
AV40	VSS_8	AP33
AF40	VSS_9	AE33
AN40	VSS_10	AB33
AK40	VSS_11	Y33
AL40	VSS_12	V33
AH40	VSS_13	T33
AG40	VSS_14	R33
AF40	VSS_15	M33
AE40	VSS_16	H33
E40	VSS_17	G33
AY39	VSS_18	F33
AW39	VSS_19	D33
AV39	VSS_20	B33
AR39	VSS_21	AH32
AN39	VSS_22	AG32
AJ39	VSS_23	AF32
AC39	VSS_24	AE32
AB39	VSS_25	AC32
AA39	VSS_26	AB32
Y39	VSS_27	G32
W39	VSS_28	B32
V39	VSS_29	AY31
T39	VSS_30	AV31
R39	VSS_31	AN31
P39	VSS_32	AJ31
N39	VSS_33	AG31
M39	VSS_34	AB31
L39	VSS_35	Y31
J39	VSS_36	AB30
H39	VSS_37	E30
G39	VSS_38	AT29
F39	VSS_39	AN29
D39	VSS_40	AB29
AT38	VSS_41	T29
AM38	VSS_42	N29
AH38	VSS_43	K29
AG38	VSS_44	G29
AF38	VSS_45	E29
AE38	VSS_46	C29
C38	VSS_47	B29
AK37	VSS_48	A29
AH37	VSS_49	BA28
AB37	VSS_50	AW28
AA37	VSS_51	AU28
Y37	VSS_52	AP28
W37	VSS_53	AM28
V37	VSS_54	AD28
T37	VSS_55	AC28
R37	VSS_56	W28
P37	VSS_57	J28
N37	VSS_58	E28
M37	VSS_59	AP27
L37	VSS_60	AM27
J37	VSS_61	AK27
H37	VSS_62	J27
G37	VSS_63	G27
F37	VSS_64	F27
D37	VSS_65	C27
AY36	VSS_66	B27
AW36	VSS_67	AN26
AV36	VSS_68	M26
AR36	VSS_69	K26
AG36	VSS_70	F26
AF36	VSS_71	D26
AE36	VSS_72	AK25
AC36	VSS_73	P25
C36	VSS_74	K25
B36	VSS_75	H25
BA35	VSS_76	E25
AV35	VSS_77	D25
AR35	VSS_78	A25
AH35	VSS_79	BA24
AB35	VSS_80	AU24
AA35	VSS_81	AL24
Y35	VSS_82	AW23
W35	VSS_83	
V35	VSS_84	
T35	VSS_85	
R35	VSS_86	
P35	VSS_87	
N35	VSS_88	
M35	VSS_89	
L35	VSS_90	
J35	VSS_91	
H35	VSS_92	
G35	VSS_93	
F35	VSS_94	
D35	VSS_95	
AN34	VSS_96	

Calistoga

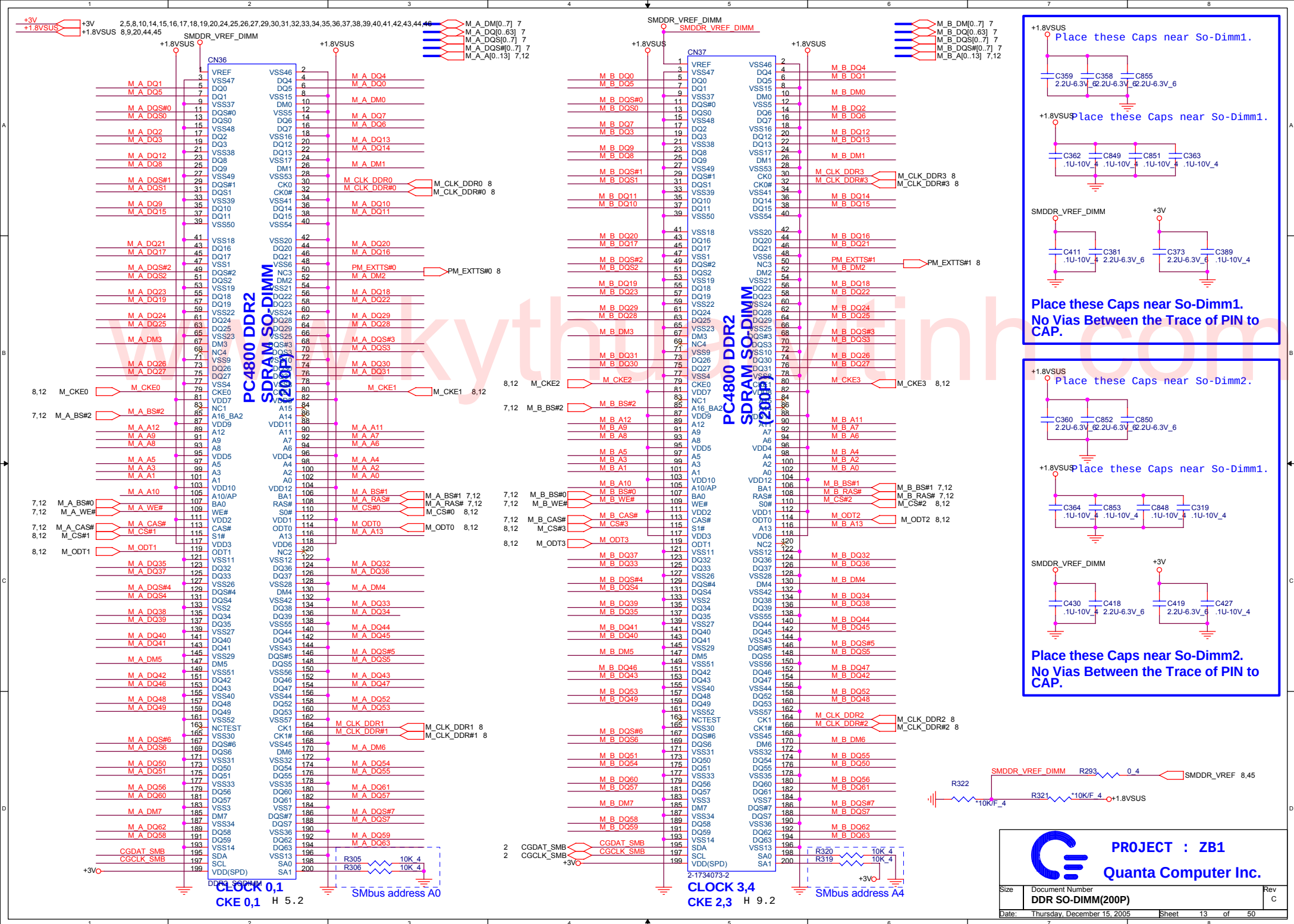
U43J		
AT23	VSS_180	J11
AN23	VSS_181	D11
AM23	VSS_182	B11
AH23	VSS_183	AV10
AC23	VSS_184	AP10
W23	VSS_185	AL10
K23	VSS_186	AJ10
J23	VSS_187	AG10
F23	VSS_188	AC10
AE33	VSS_189	W10
AB33	VSS_190	U10
Y33	VSS_191	BA9
G22	VSS_192	AW9
F22	VSS_193	AR9
E22	VSS_194	AH9
D22	VSS_195	AB9
A22	VSS_196	Y9
BA21	VSS_197	AG9
AV21	VSS_198	G9
AR21	VSS_199	E9
AN21	VSS_200	A9
AL21	VSS_201	AG8
AB21	VSS_202	AD8
Y21	VSS_203	AA8
P21	VSS_204	U8
K21	VSS_205	K8
J21	VSS_206	C8
H21	VSS_207	BA7
C21	VSS_208	AV7
AW20	VSS_209	AP7
AR20	VSS_210	AL7
AM20	VSS_211	AJ7
AA20	VSS_212	AH7
K20	VSS_213	AF7
B20	VSS_214	AC7
A20	VSS_215	R7
AN19	VSS_216	G7
AC19	VSS_217	D7
W19	VSS_218	AG6
K19	VSS_219	AD6
G19	VSS_220	AB6
C19	VSS_221	Y6
AH18	VSS_222	U6
K18	VSS_223	N6
H18	VSS_224	K6
D18	VSS_225	V6
A18	VSS_226	B6
AY17	VSS_227	AV5
AR17	VSS_228	AF5
AP17	VSS_229	AD5
AM17	VSS_230	AY4
AK17	VSS_231	AR4
AV16	VSS_232	AP4
AN16	VSS_233	AL4
AL16	VSS_234	AJ4
J16	VSS_235	Y4
F16	VSS_236	U4
C16	VSS_237	R4
AN15	VSS_238	J4
AM15	VSS_239	F4
AK15	VSS_240	C4
N15	VSS_241	AY3
M15	VSS_242	AW3
L15	VSS_243	AV3
B15	VSS_244	AL3
A15	VSS_245	AH3
BA14	VSS_246	AG3
AT14	VSS_247	AF3
AK14	VSS_248	AD3
K14	VSS_249	AC3
AD14	VSS_250	AA3
U14	VSS_251	G3
K14	VSS_252	AT2
H14	VSS_253	AR2
E14	VSS_254	AP2
AV13	VSS_255	AK2
AR13	VSS_256	AJ2
AM13	VSS_257	AD2
AL13	VSS_258	AB2
AG13	VSS_259	Y2
P13	VSS_260	U2
F13	VSS_261	T2
D13	VSS_262	N2
B13	VSS_263	J2
AY12	VSS_264	H2
AC12	VSS_265	F2
K12	VSS_266	C2
H12	VSS_267	AL1
E12	VSS_268	
AD11	VSS_270	
AA11	VSS_271	
Y11	VSS_272	

Calistoga

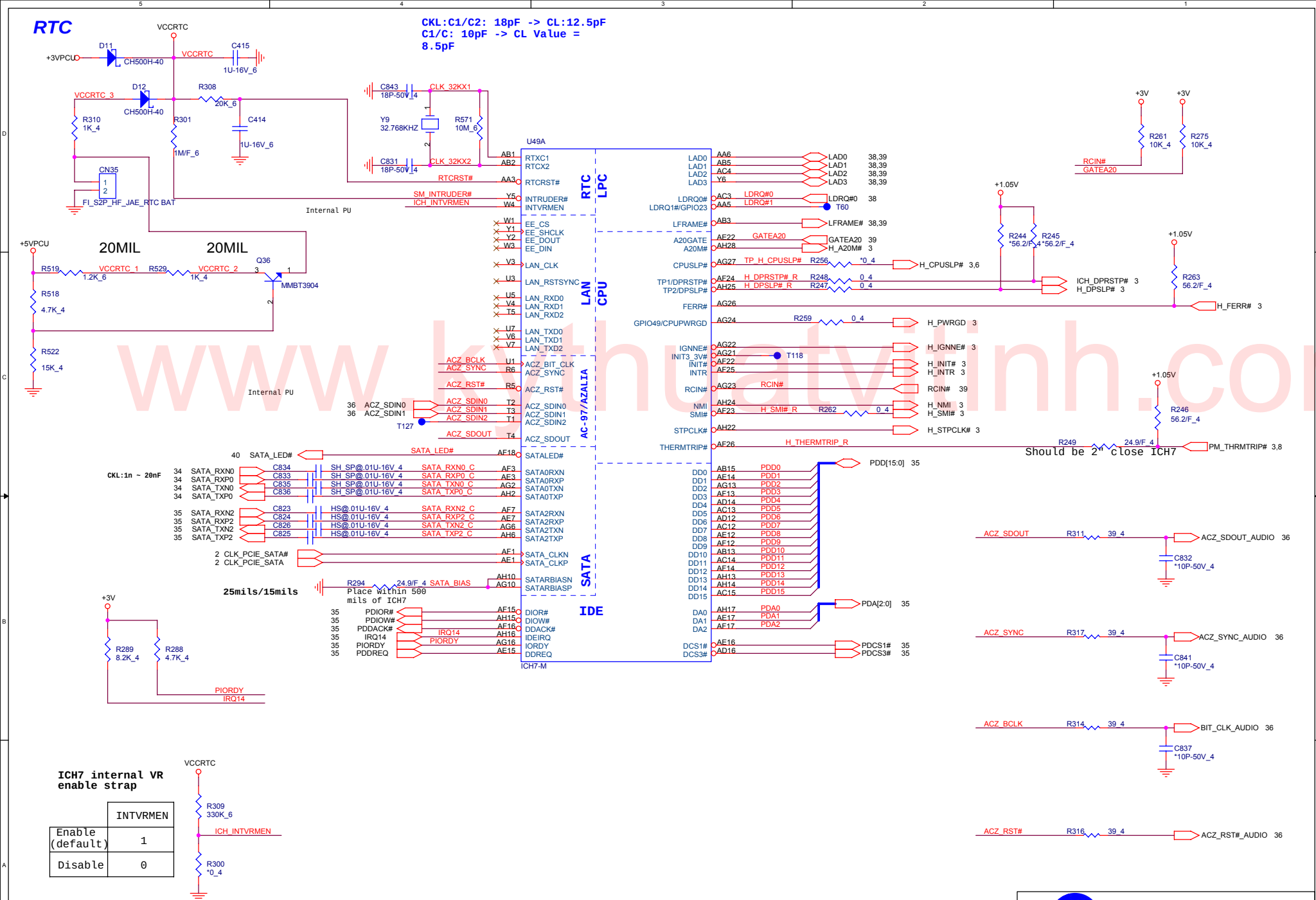


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RTC



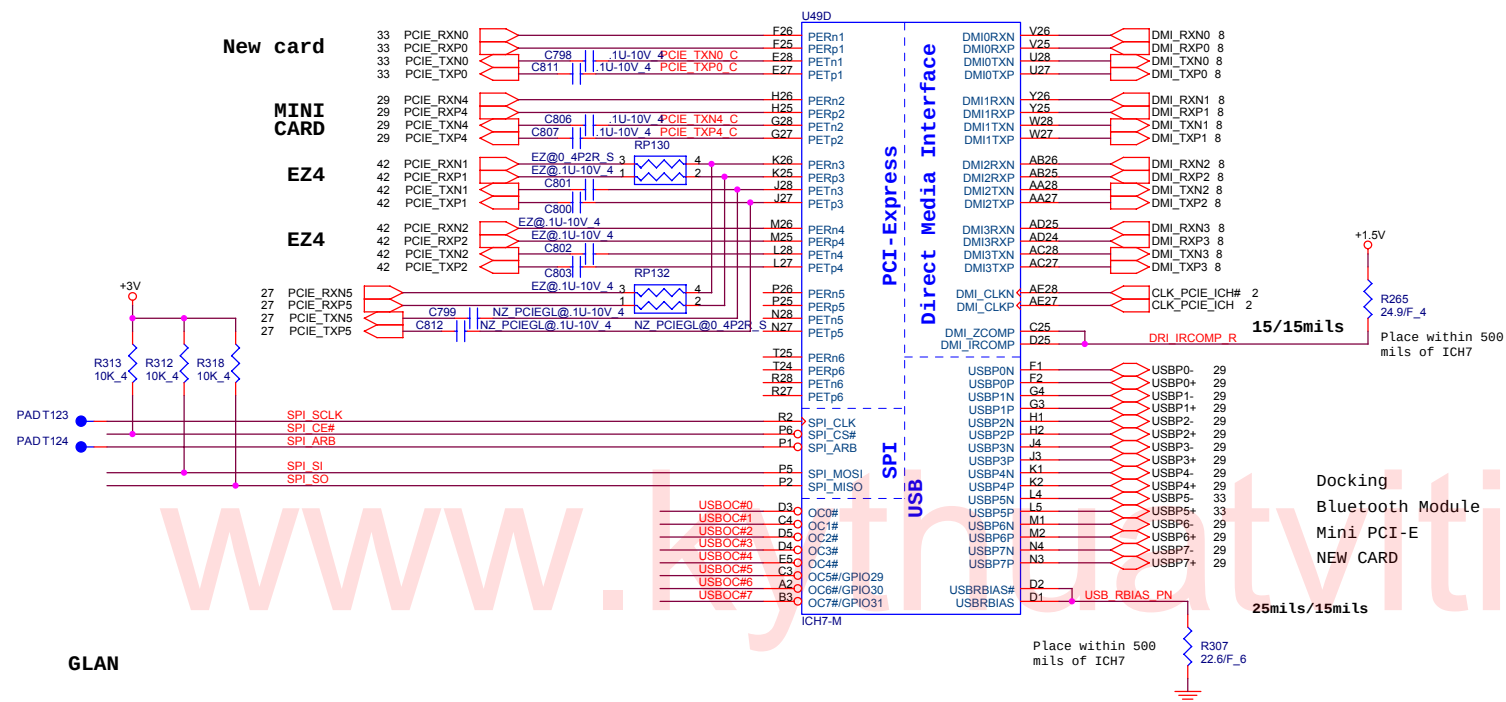
ICH7 internal VR enable strap	
	INTVRMEN
Enable (default)	1
Disable	0

New card

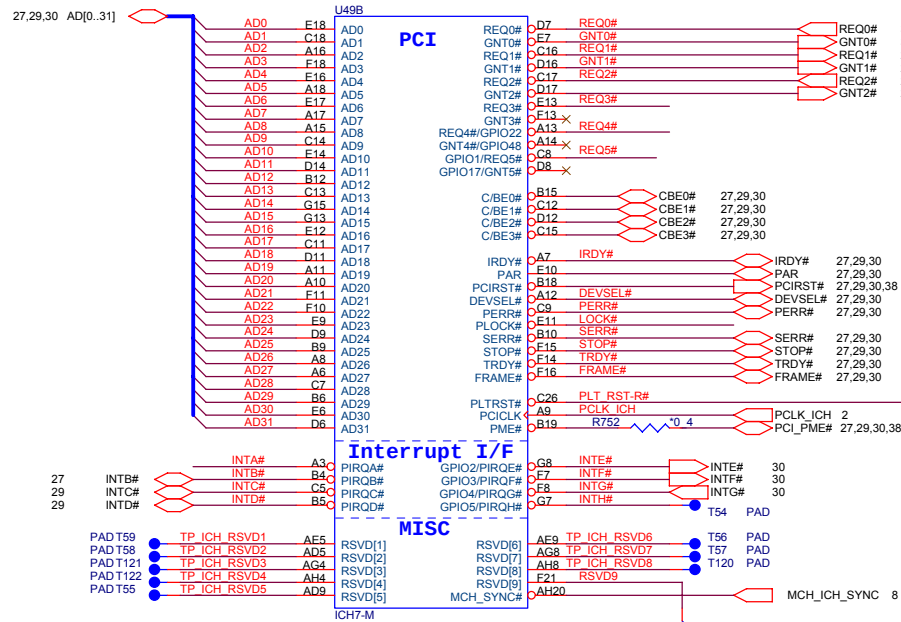
MINI CARD

EZ4

EZ4

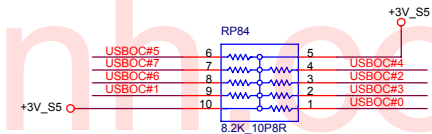
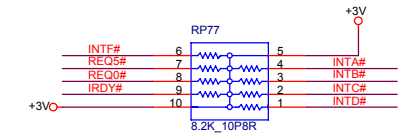
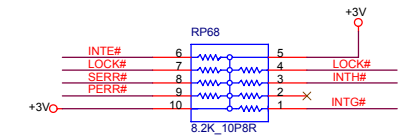
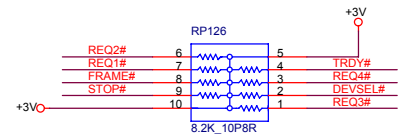


GLAN

Place within 500
mils of ICH7

25mils/15mils

Don't connect to PCI device / Express card



CKL use 10Kohm

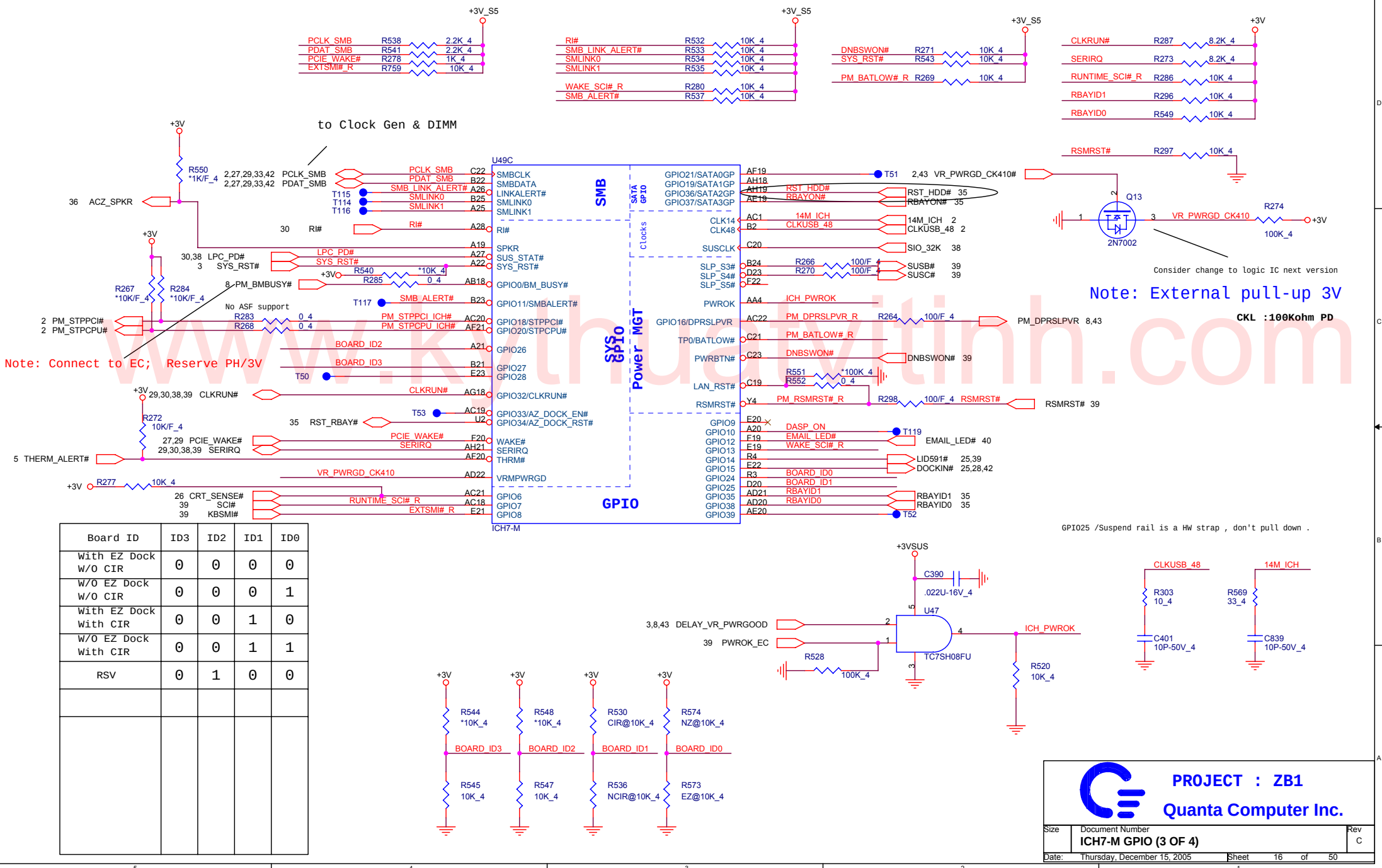
ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ0# / GNT0#	INT E/F/G#
Realtek Lan	AD16	REQ1# / GNT1#	INT B#
MINI PCI	AD19	REQ2# / GNT2#	INT C/D#

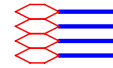
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NOTE: some of the PCIE testpoints will be available through via on traces.

8,41 PEG_RXP[15:0]
8,41 PEG_RXN[15:0]
8,41 PEG_TXP[15:0]
8,41 PEG_TXN[15:0]



U34A

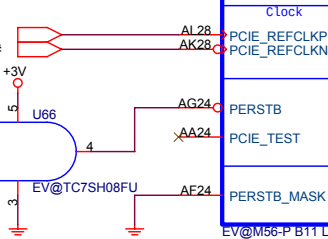
PART 1 OF 7

P
C
I
-
E
X
P
R
E
S
S

I
N
T
E
R
F
A
C
E



2 CLK_PCIE_M56
2 CLK_PCIE_M56#



15,27,29,31,33,34,35,36,39,41,42 PLTRST#

PLTRST#

Tie To VSS

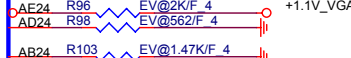
EV@M56-P B11 LF

Calibration

PCIE_CALRN

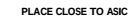
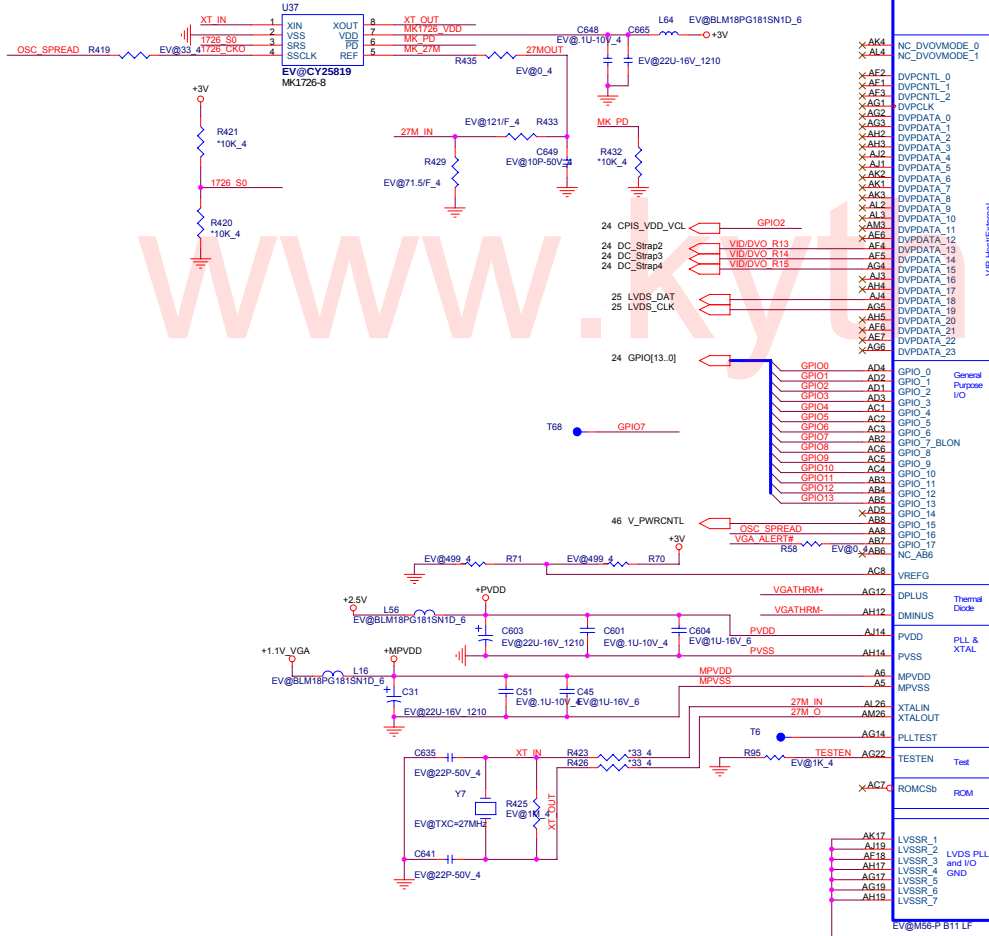
PCIE_CALRP

PCIE_CALI

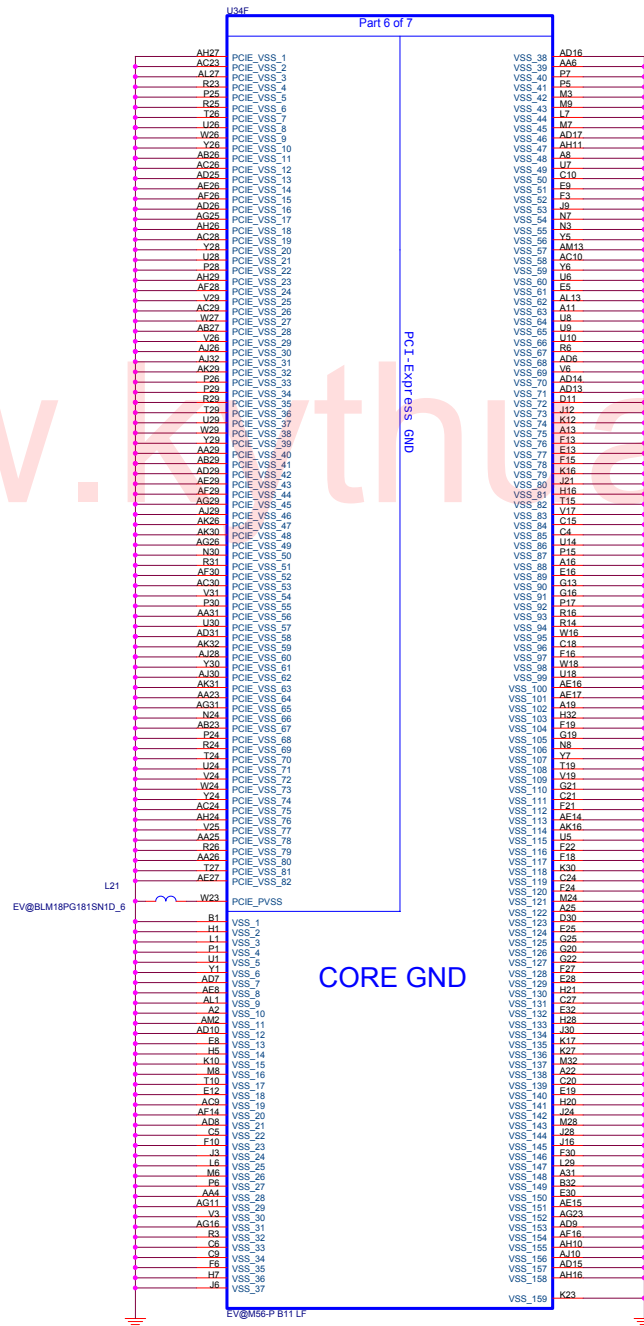


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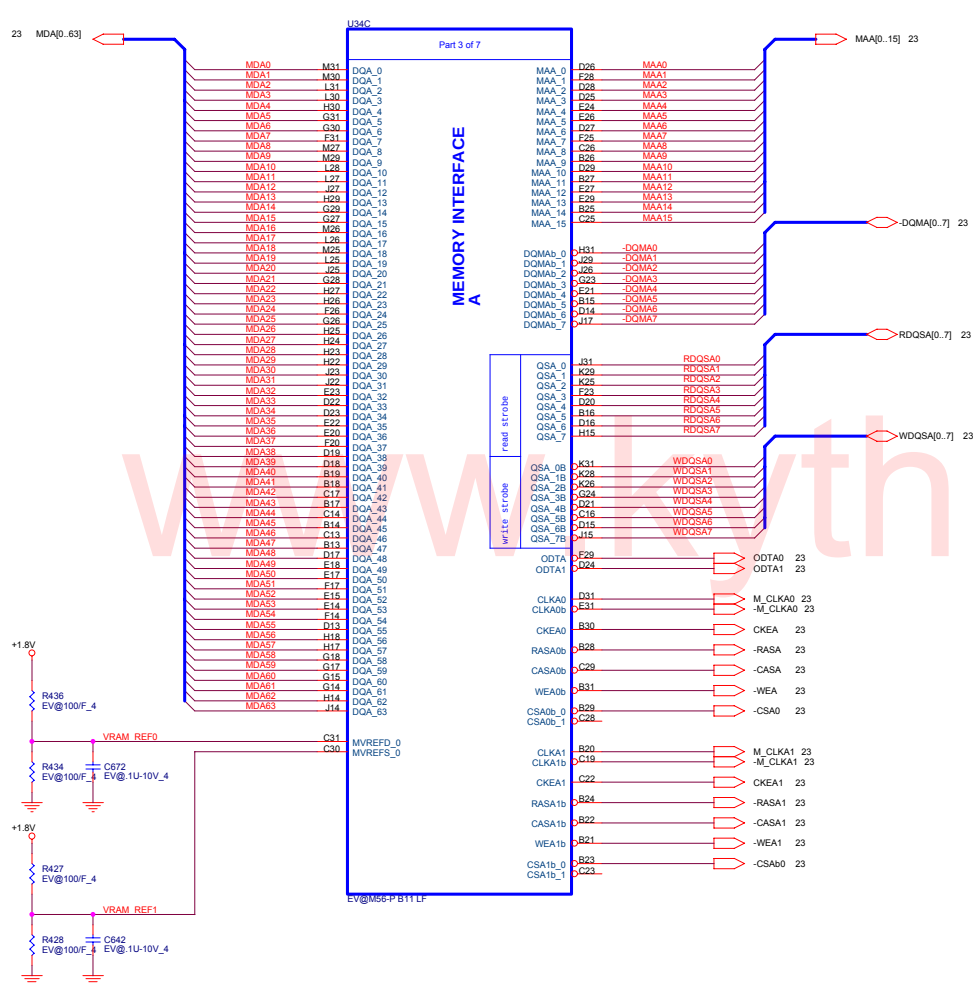


www.kvthuatvithinh.com

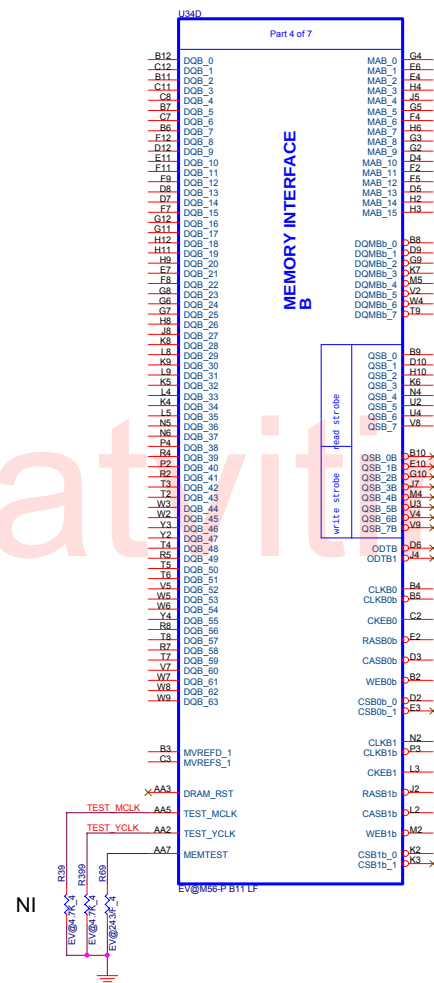


RV410 MEMORY CHANNELS A and B

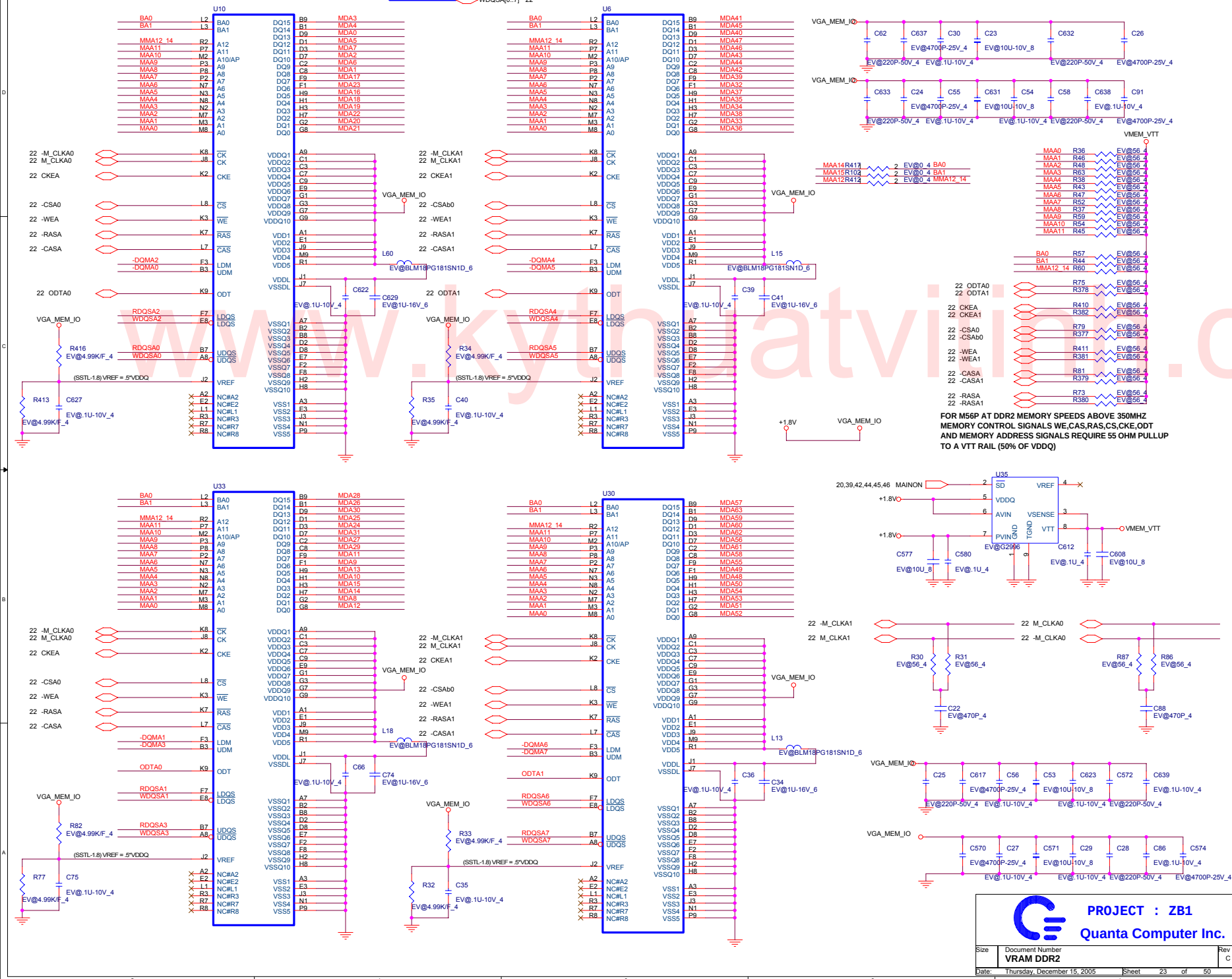
Channel A



Channel B



CHAN A DDR2 84BGA 16MX16 MEMORY



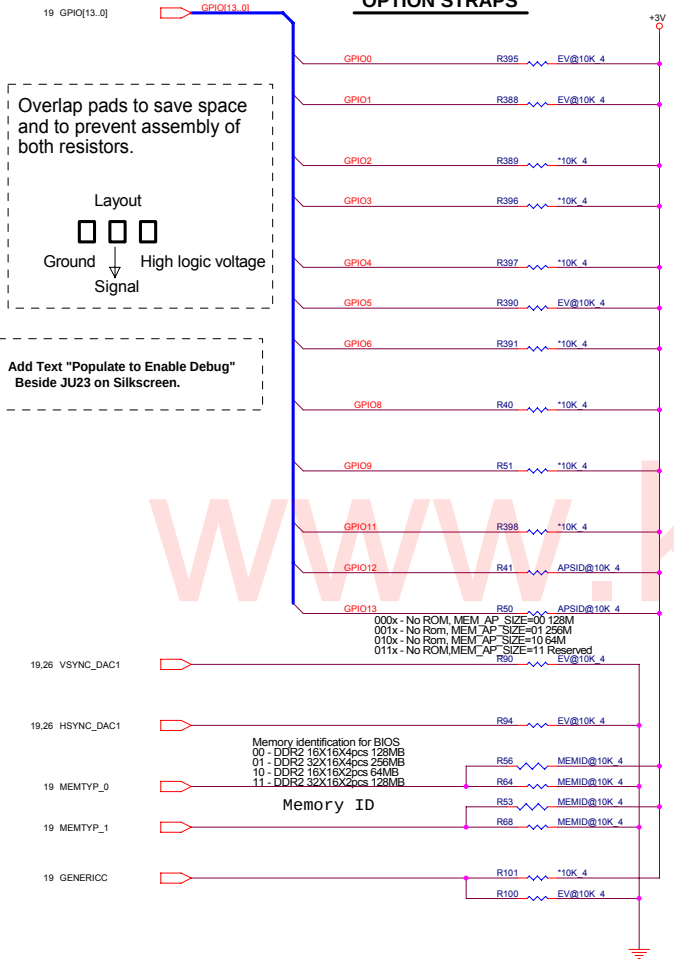
001x - No ROM, MEM_AP_SIZE=01
256M

OPTION STRAPS

Overlap pads to save space
and to prevent assembly of
both resistors.



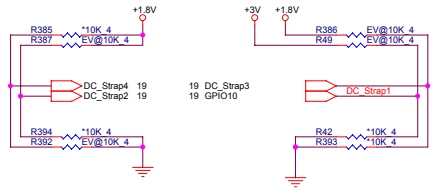
Add Text "Populate to Enable Debug"
Beside JU23 on Silkscreen.



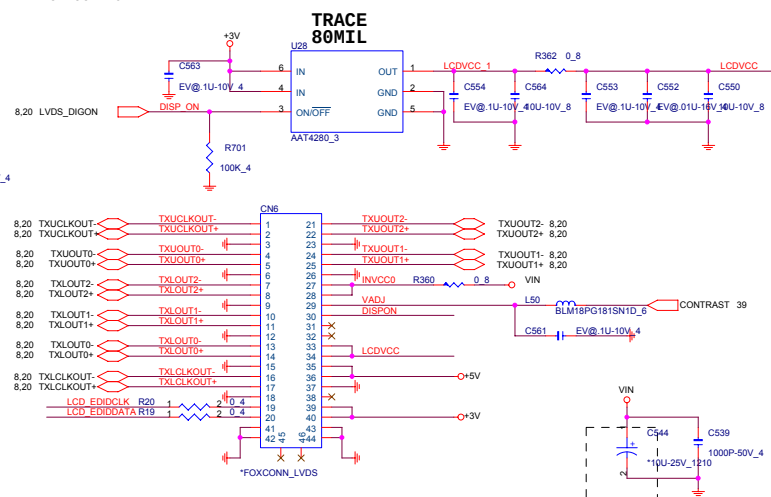
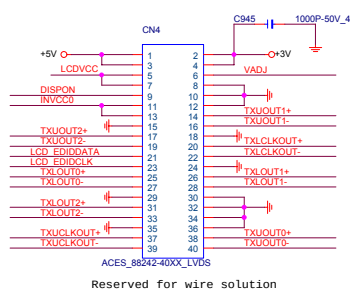
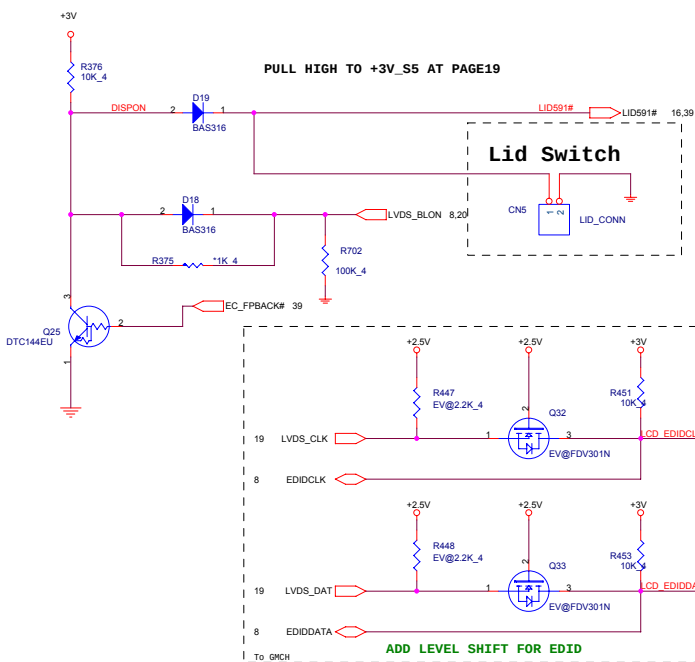
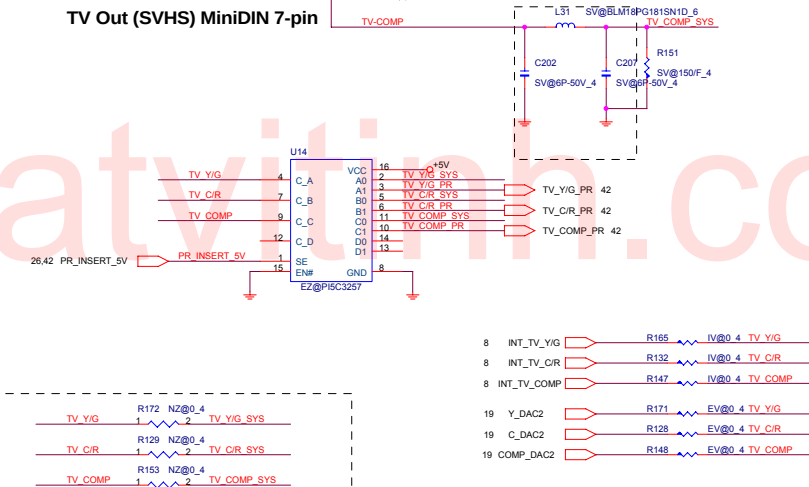
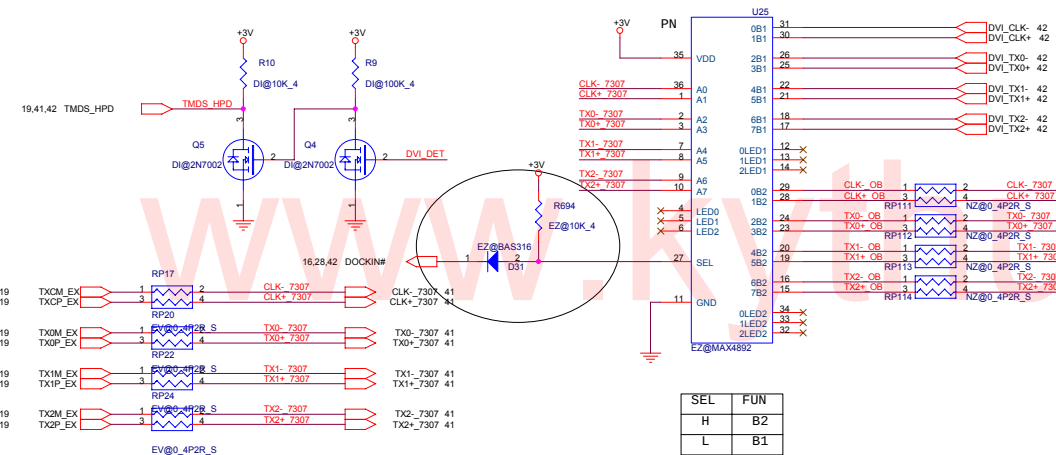
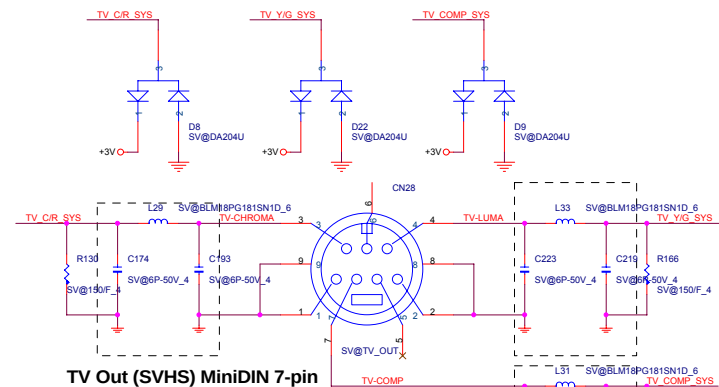
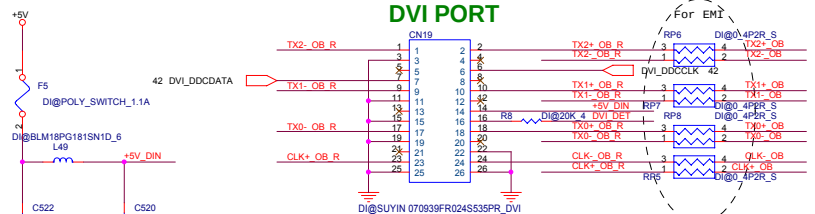
M56-P Strap

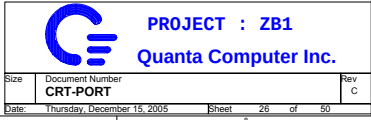
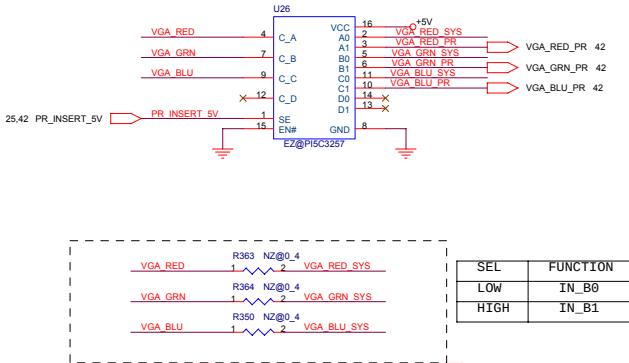
STRAPS	PIN	DESCRIPTION	Board DEFAULT
TX_PWR_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	1
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	1
	GPIO(3:2)	RSVD	
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5	RSVD	
	GPIO6	RSVD	
Force Compliance	GPIO8	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128M 001x - No Rom, MEM_AP_SIZE=01 256M 010x - No Rom, MEM_AP_SIZE=10 64M 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDs from ROM 1001 - Serial AT28F1024 ROM (Atmel), chip IDs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDs from ROM 1011 - Serial M25P10 ROM (ST), chip IDs from ROM 1100 - Serial M25P05 ROM (ST), chip IDs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDs from ROM	000
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port devices present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYNC, V2SYNC, GENERICC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

Board Straps		REV. 0.3	
STRAPS	PIN	DESCRIPTION	VALUE
MEMTYP(1:0)	GPIO25,26	Memory identification for BIOS 00 - DDR2 16X16X4pcs 128MB 01 - DDR2 32X16X4pcs 256MB 10 - DDR2 16X16X2pcs 64MB 11 - DDR2 32X16X2pcs 128MB	
DC_Strap1	GPIO(10)	Internal TMD5 Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PALNTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1

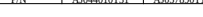
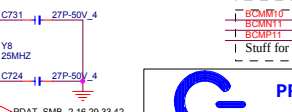
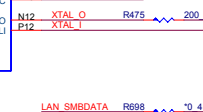
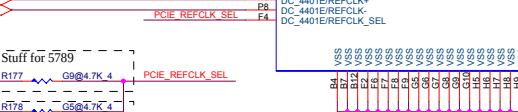
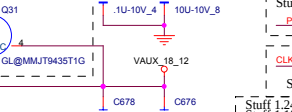
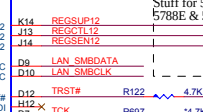
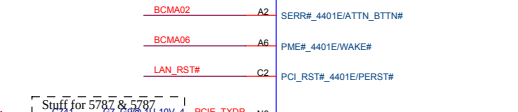
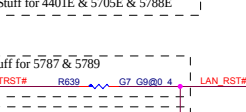
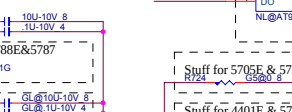
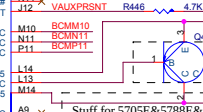
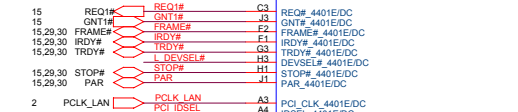
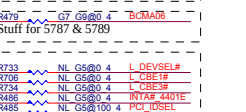
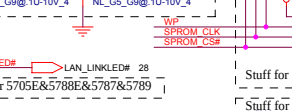
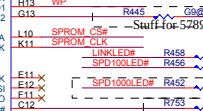
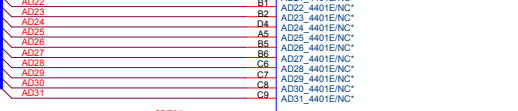
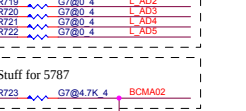
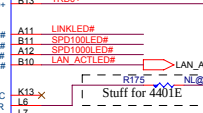
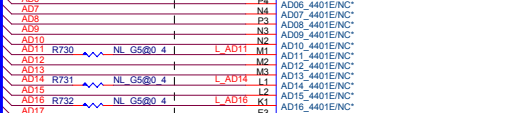
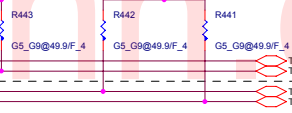
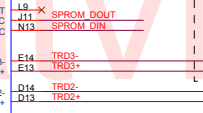
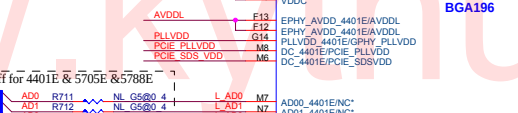
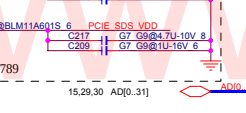
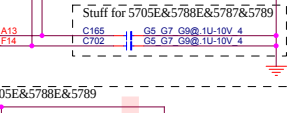
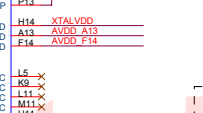
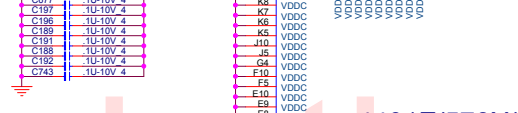
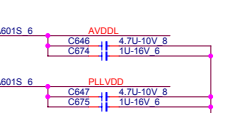
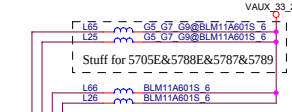
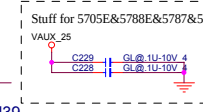
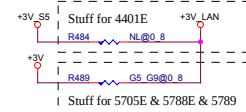
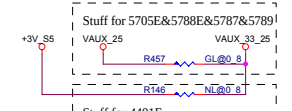
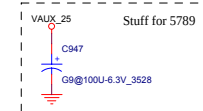
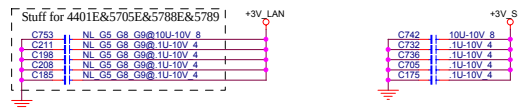
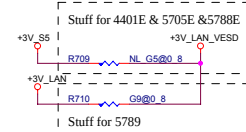


DVI-I CONNECTOR (DVI-D)





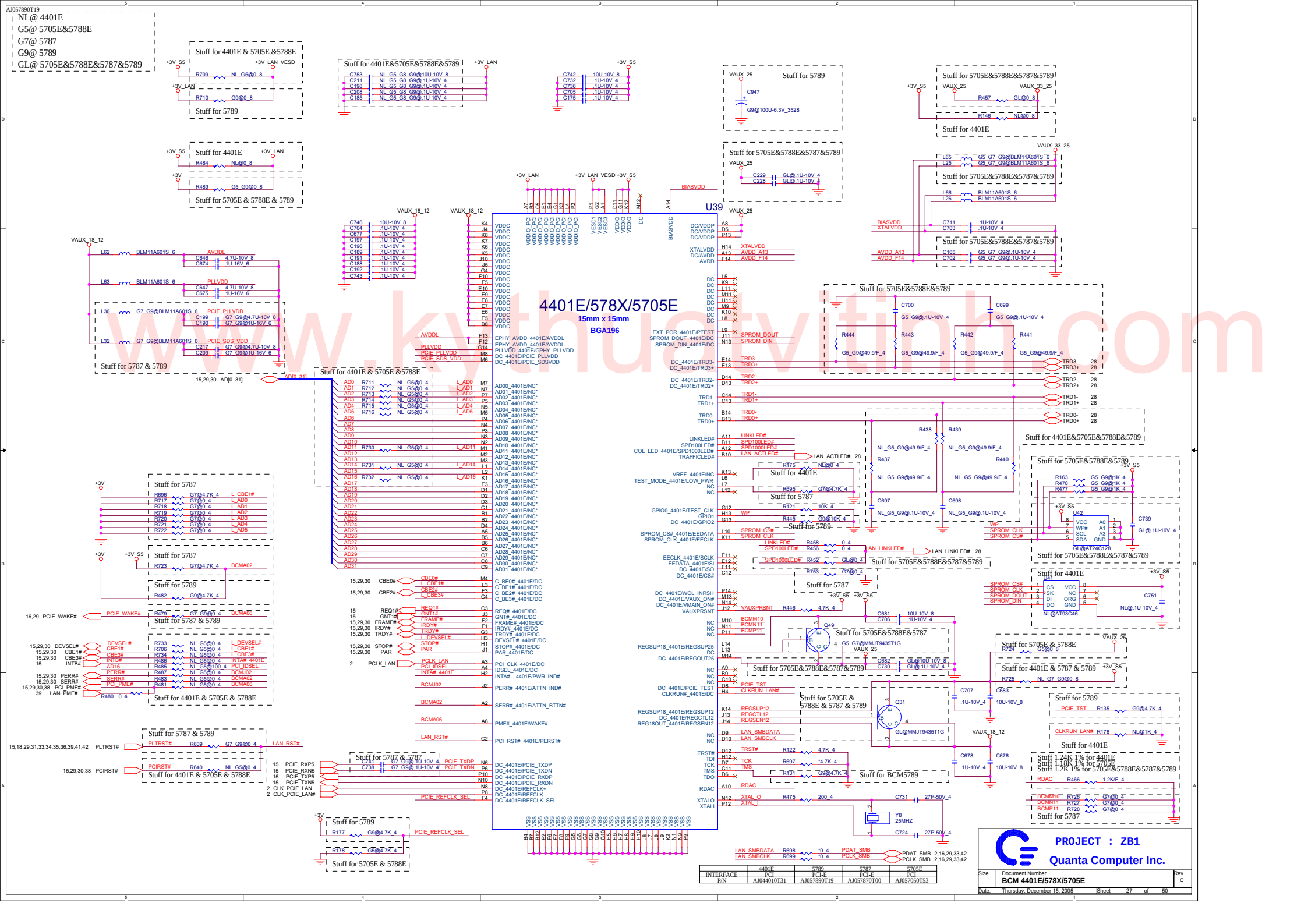
NL @ 4401E
G5@ 5705E&5788E
G7@ 5787
G9@ 5789
GL@ 5705E&5788E&5787&5789



4401E/578X/5705E

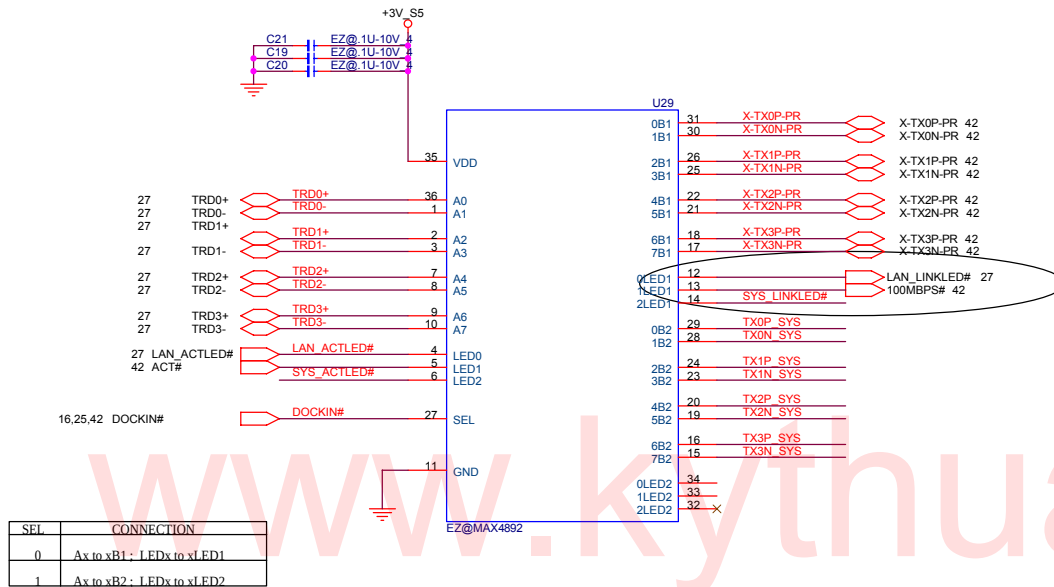
15mm x 15mm

BGA196

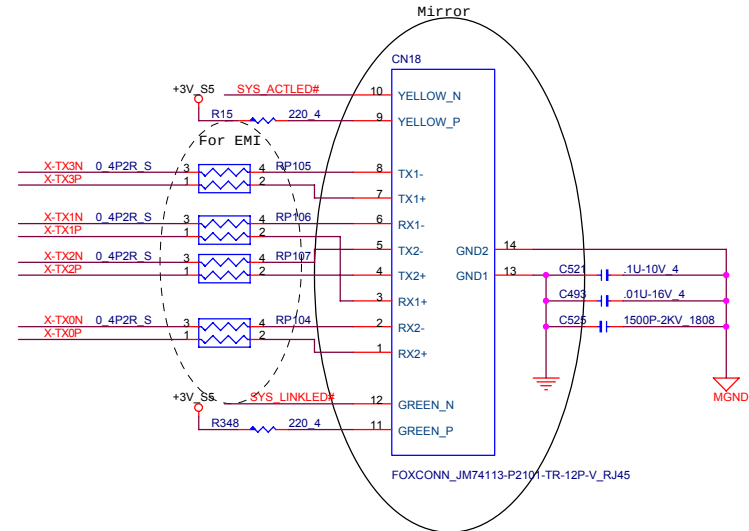
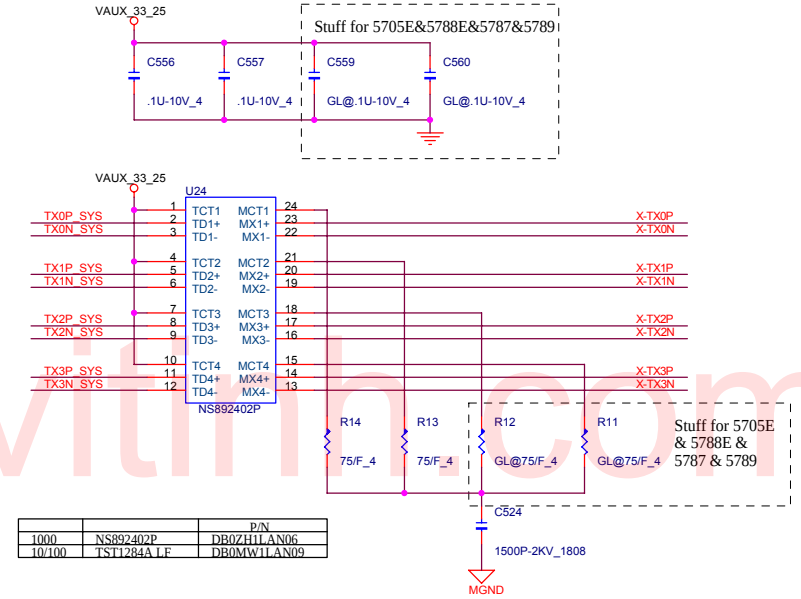
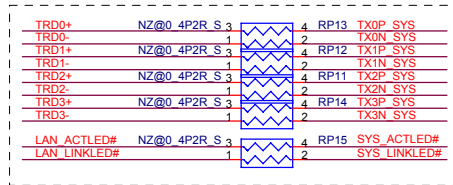


PROJECT : ZB1
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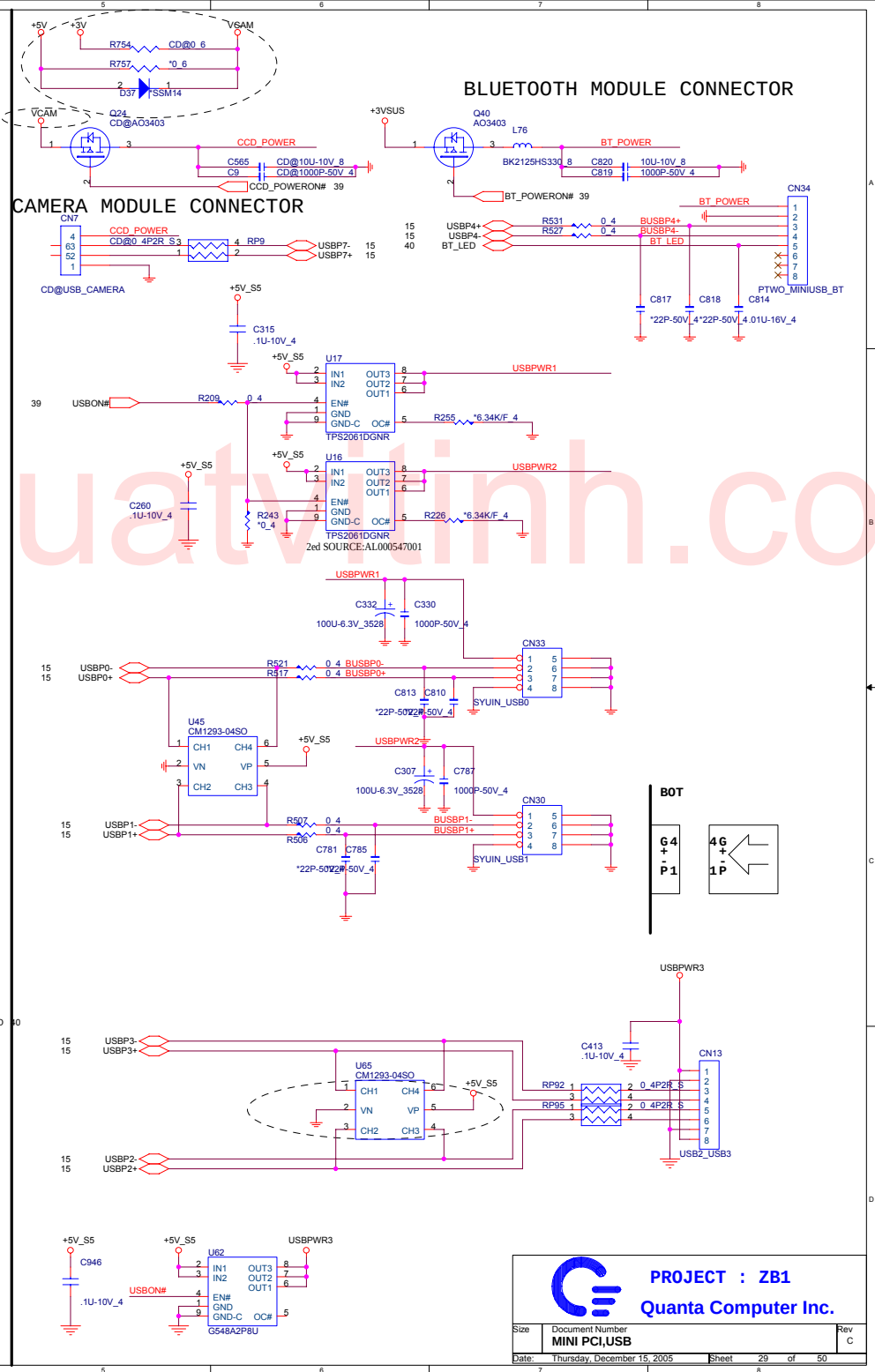
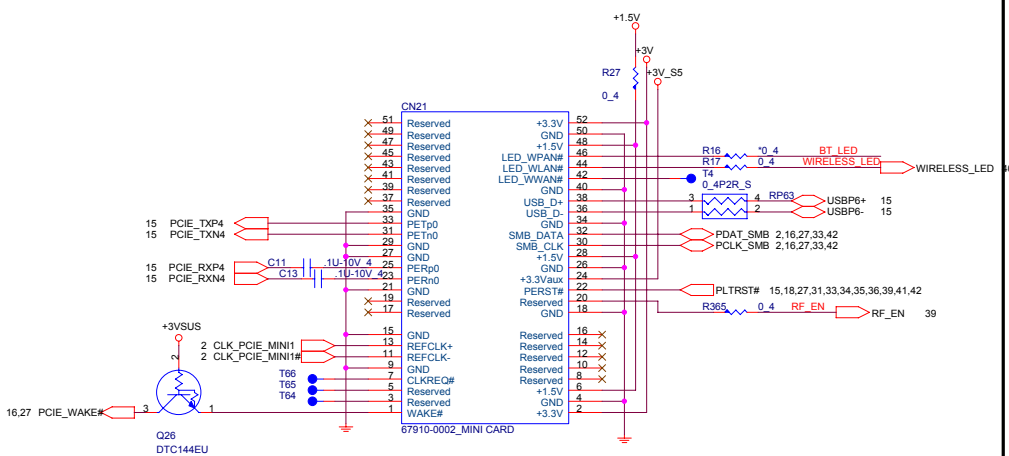
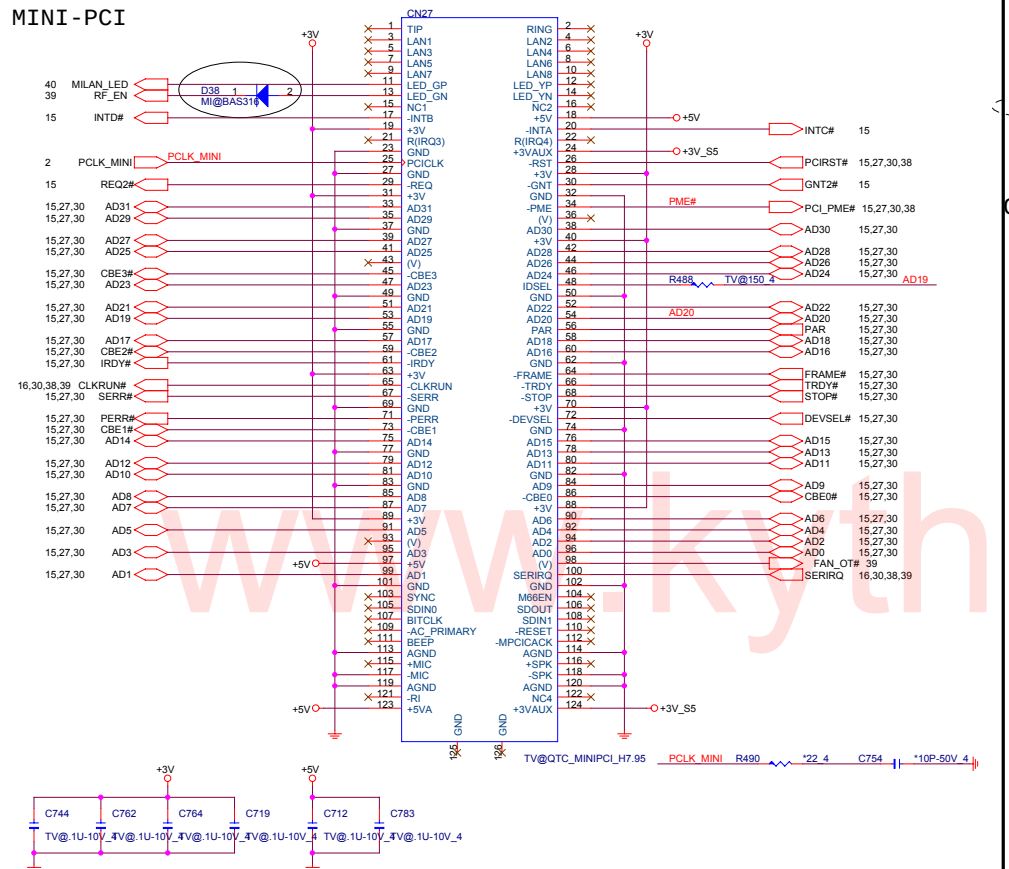
INTERFACE	4401E	5789	5705E
P/N	A10440101T1	A0578901T1	A0578701T0

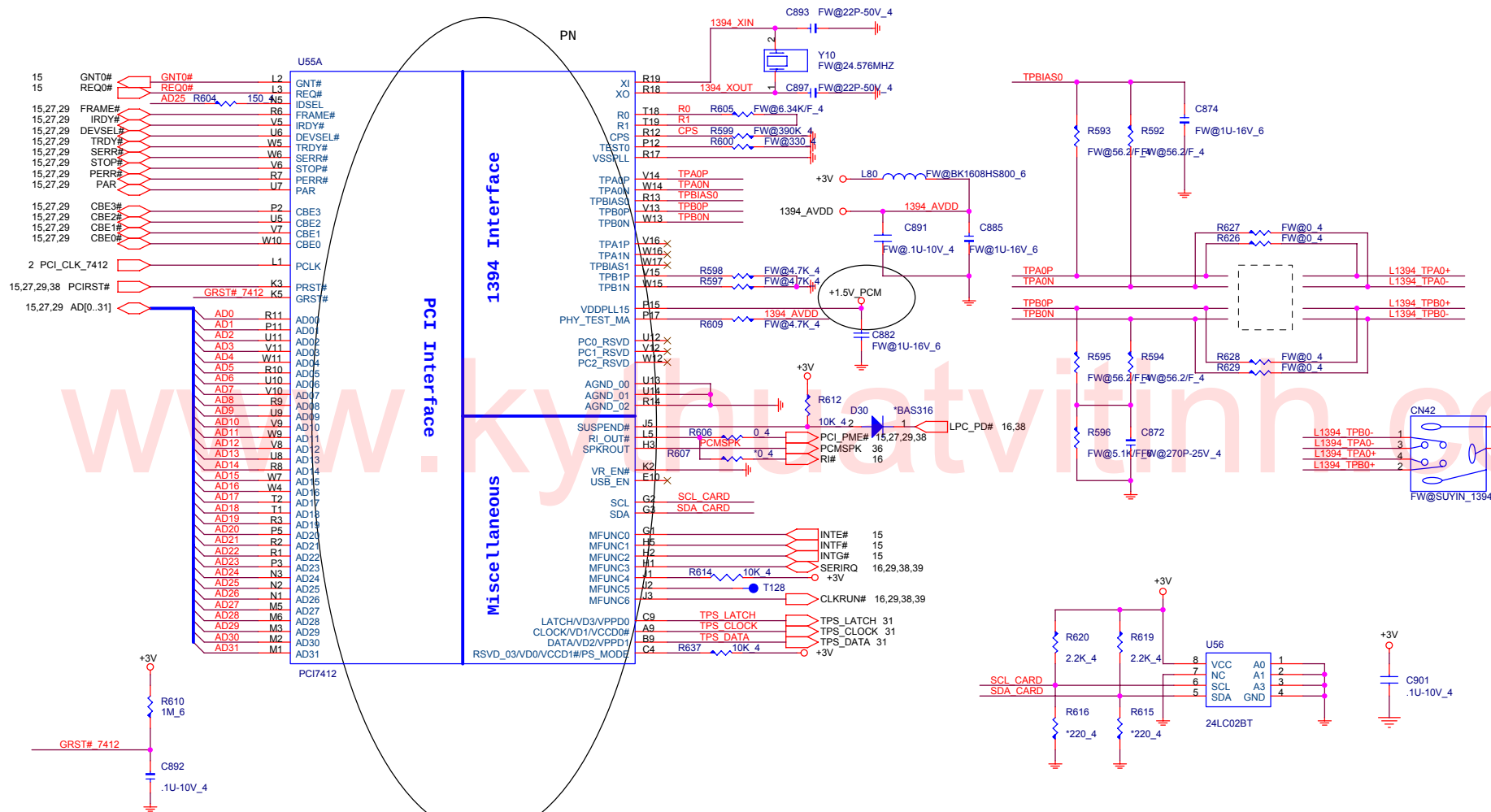


ADD CIRCUITS WHEN NO DOCKING



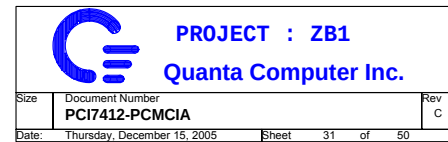
MINI-PCI



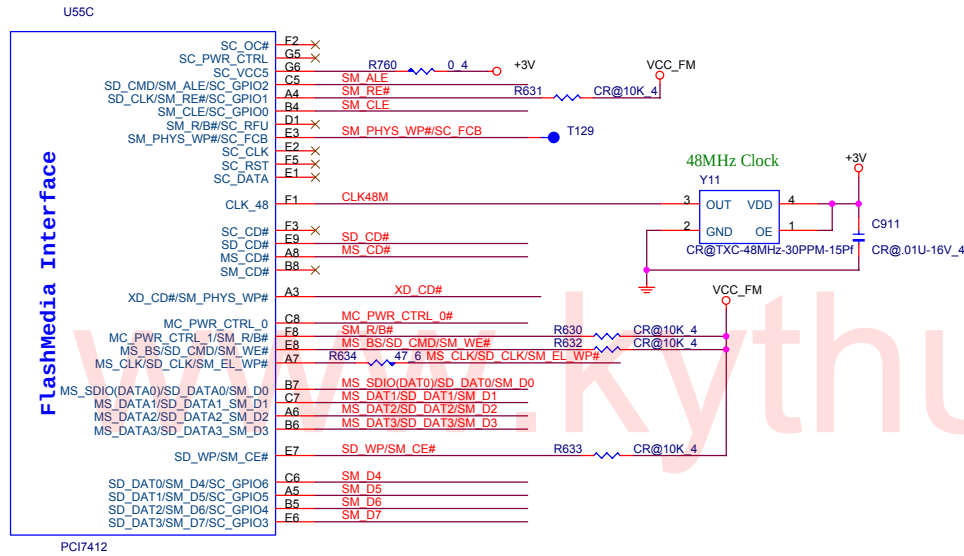


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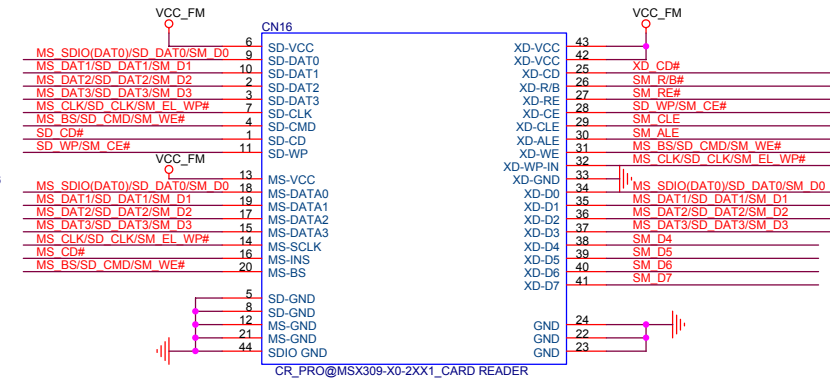
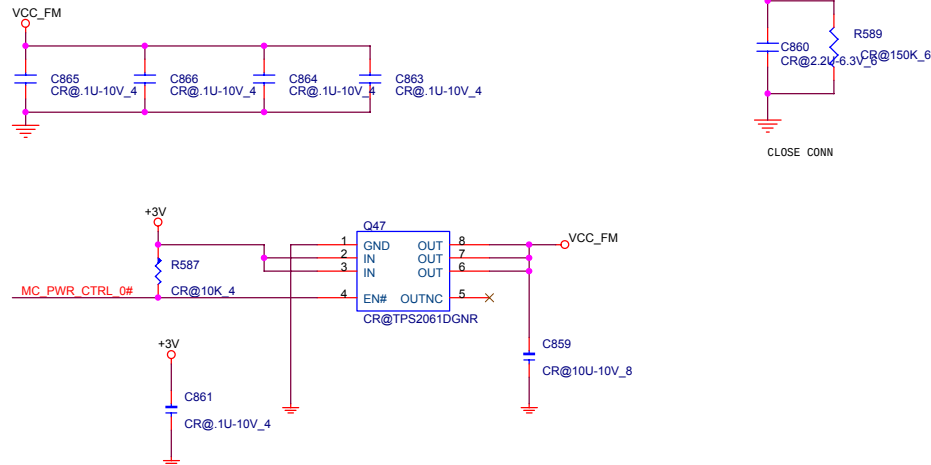
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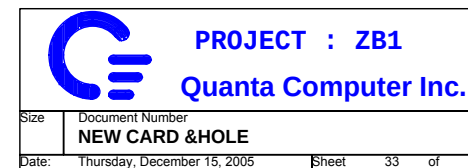
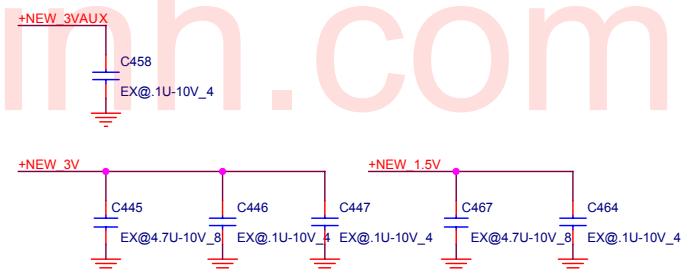
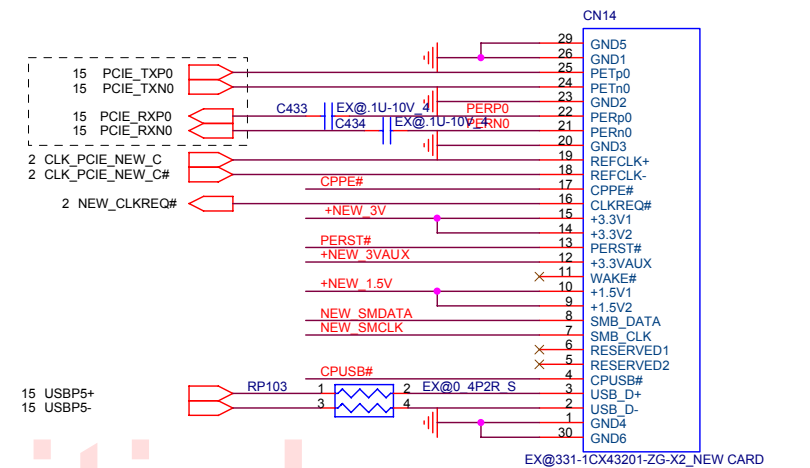
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.



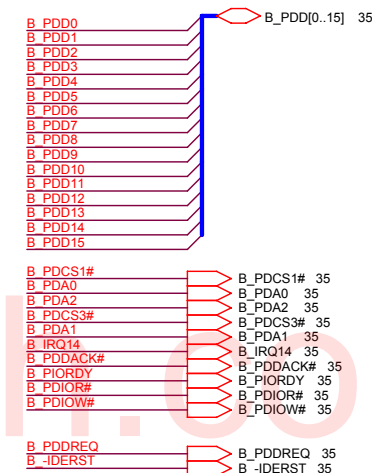
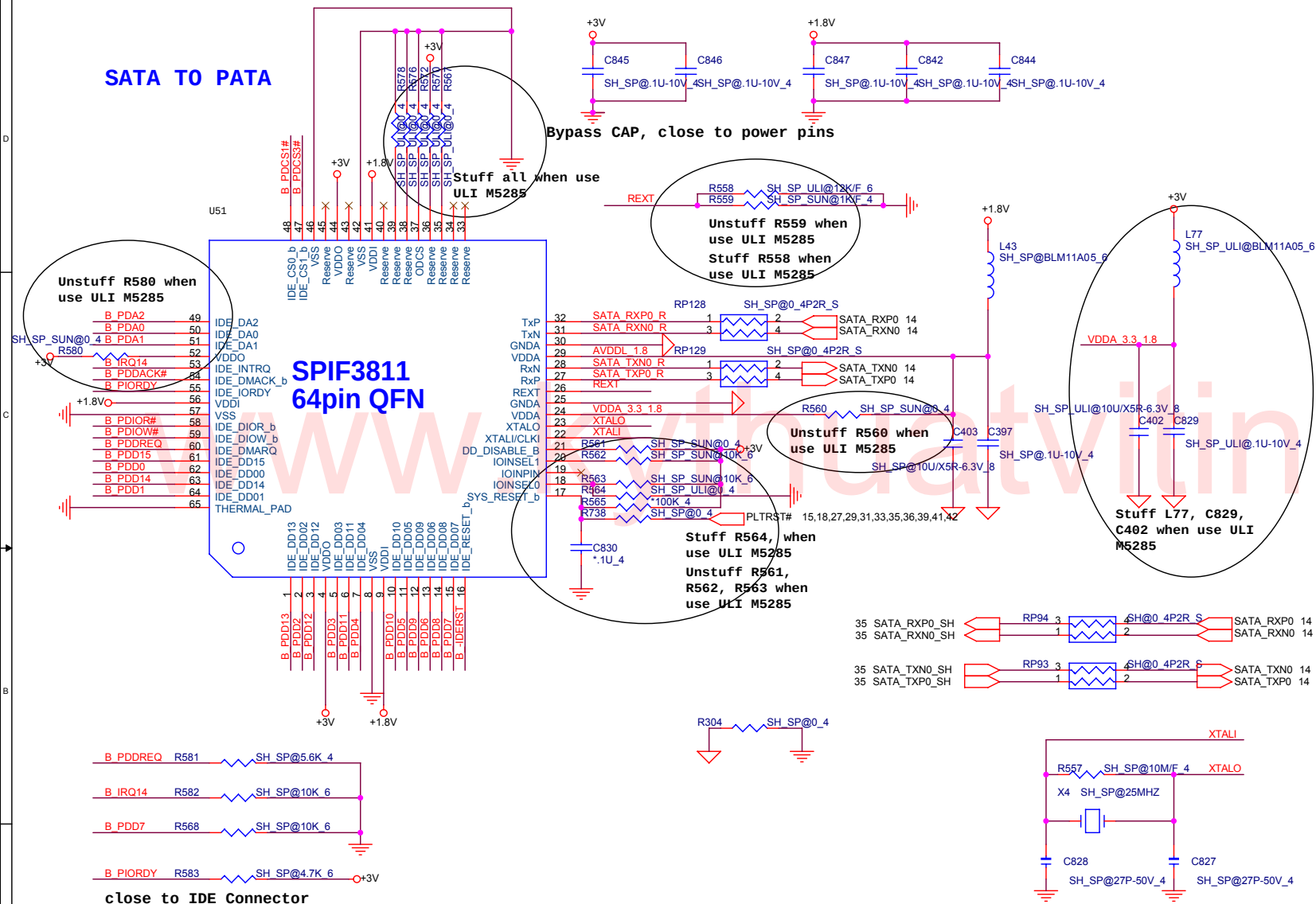
5 IN1 CARD READER



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SATA TO PATA



Reference clock select

ATAIOEN	Note
0	disable PATA output
1	enable PATA output

1	enable
Operation Mode	

MODE[2..0]	
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	Device mode 150MB/S
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVED

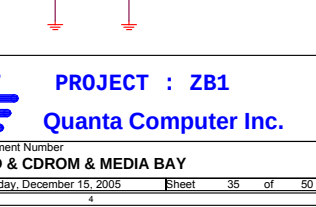
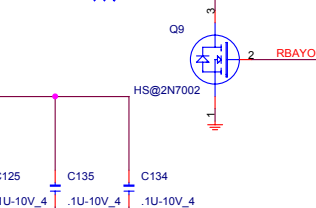
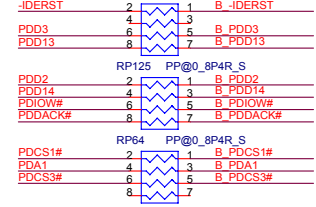
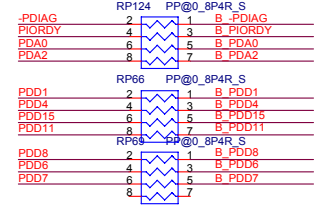
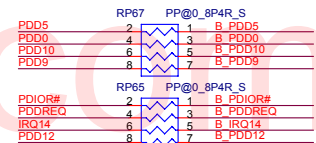
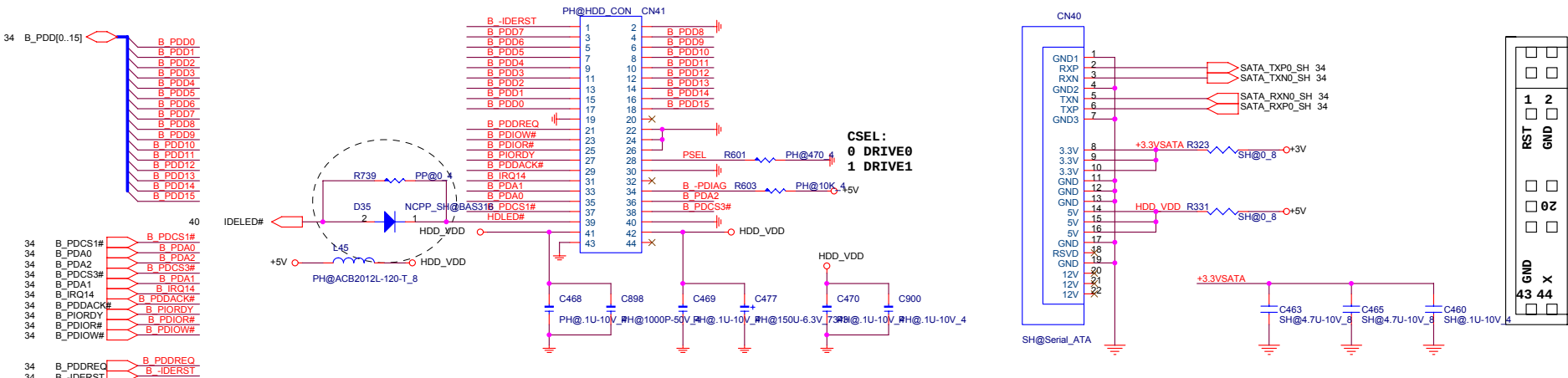
1 1 1	RESERVED
Reference clock select	

CLKSEL[1..0]	External clock
0 0	20 MHz
0 1	25 MHz

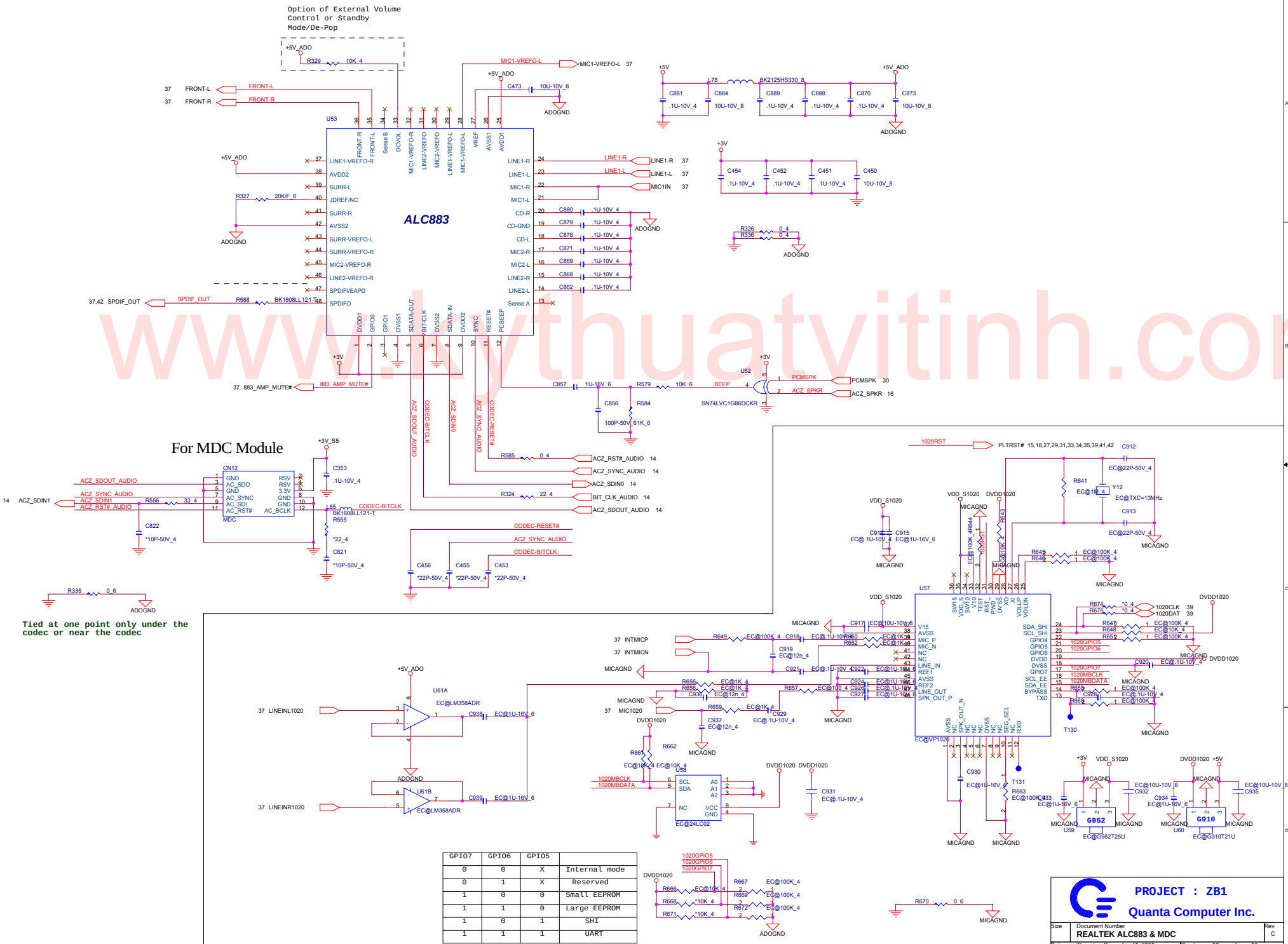


PROJECT : ZB1
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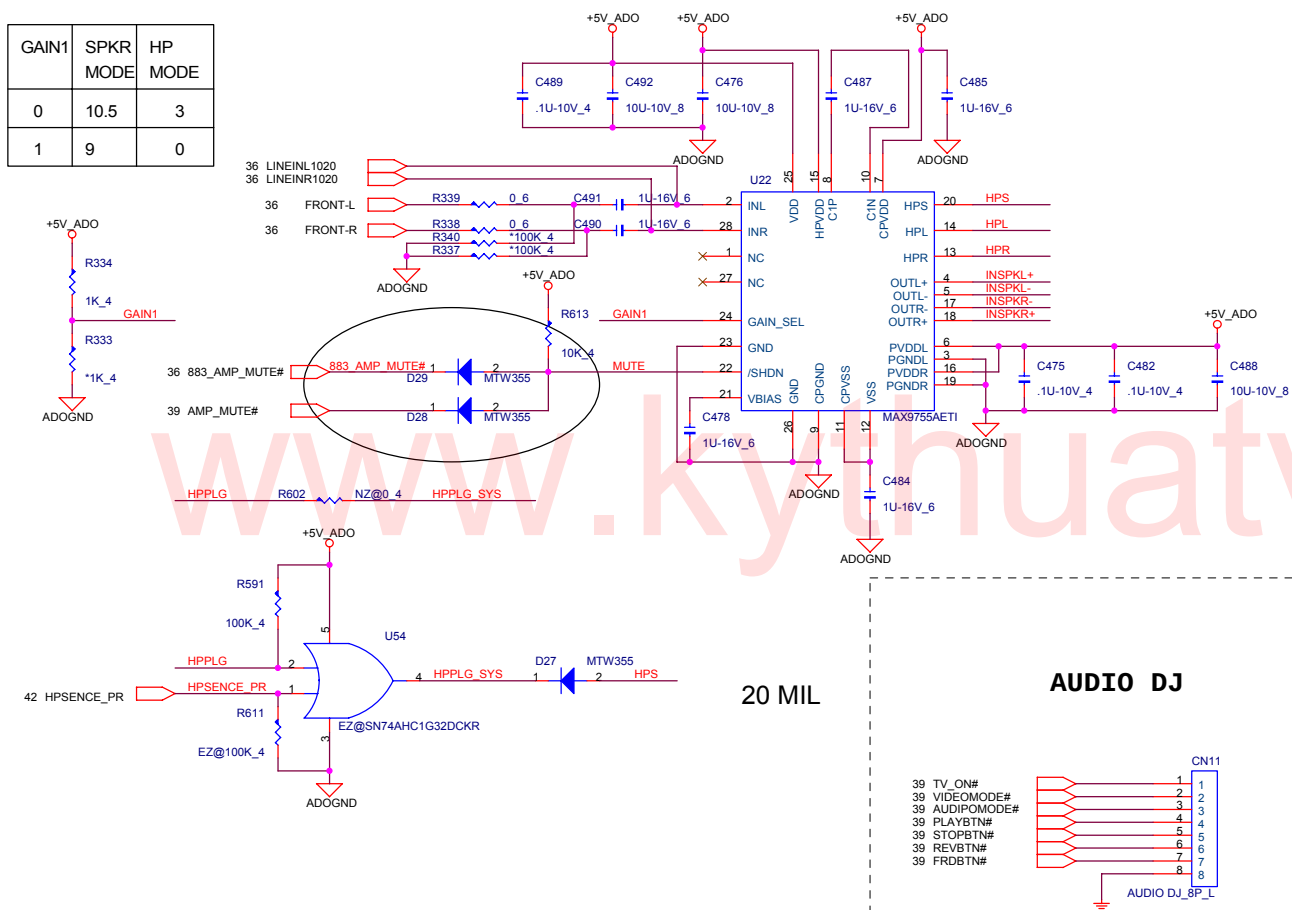
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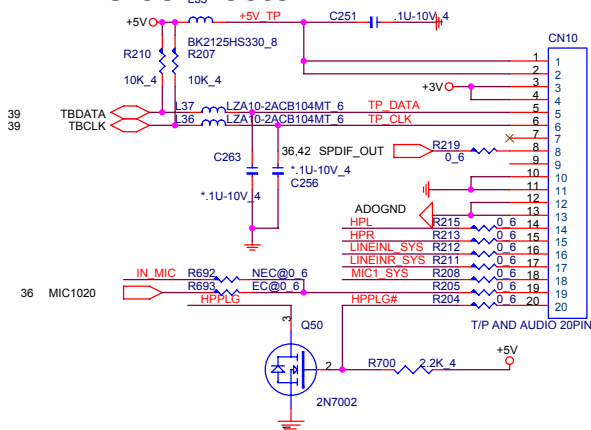
PROJECT : ZB1
Quanta Computer Inc.



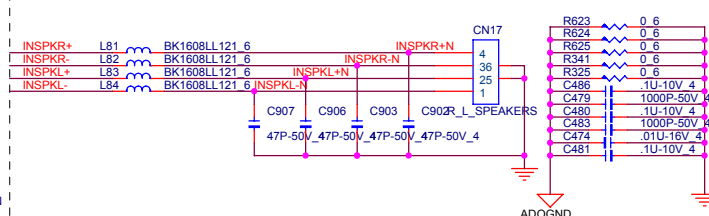
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



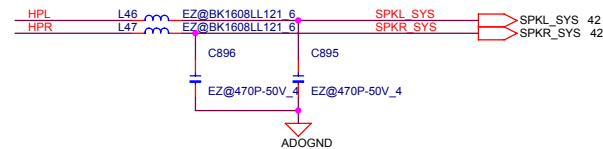
**TOUCH PAD/AUDIO JACK
FFC connector**



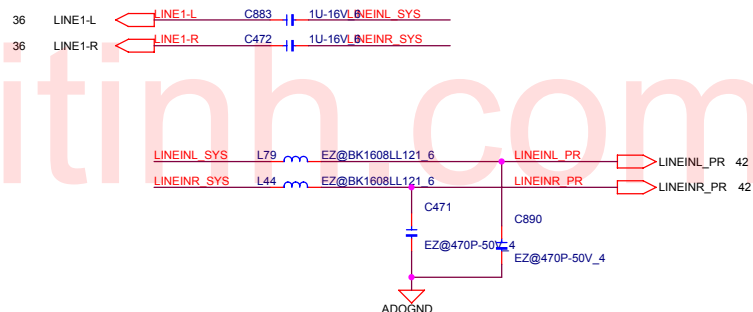
SPEAKER CONNECTOR



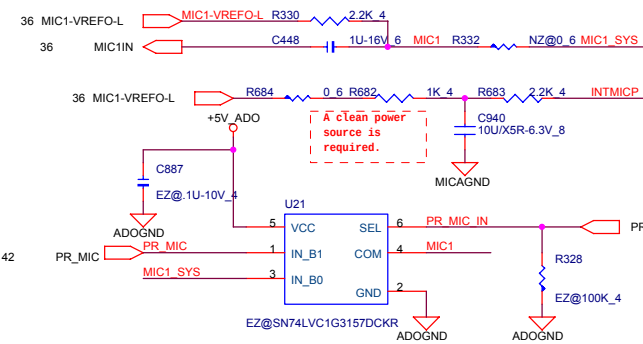
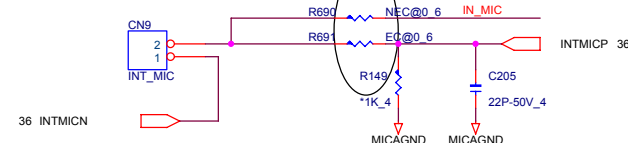
LINE OUT



LINE IN



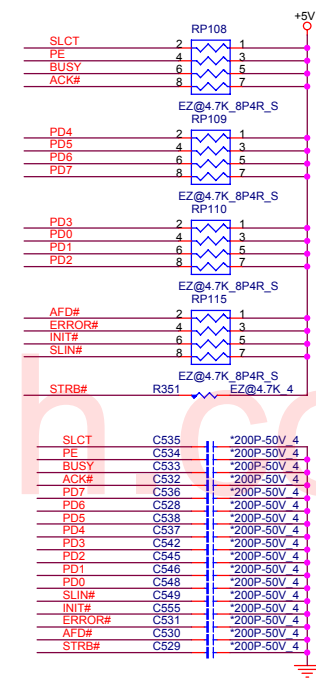
MIC



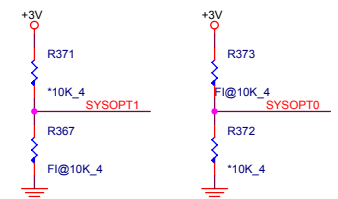
SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



PROJECT : ZL6
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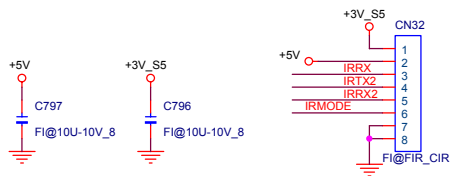


SYSOPT1	SYSOPT0	DEFAULT CONFIGURATION PORT BASE ADDRESS
0	0	0X002E
0	1	0X004E
1	0	0X162E
1	1	0X164E

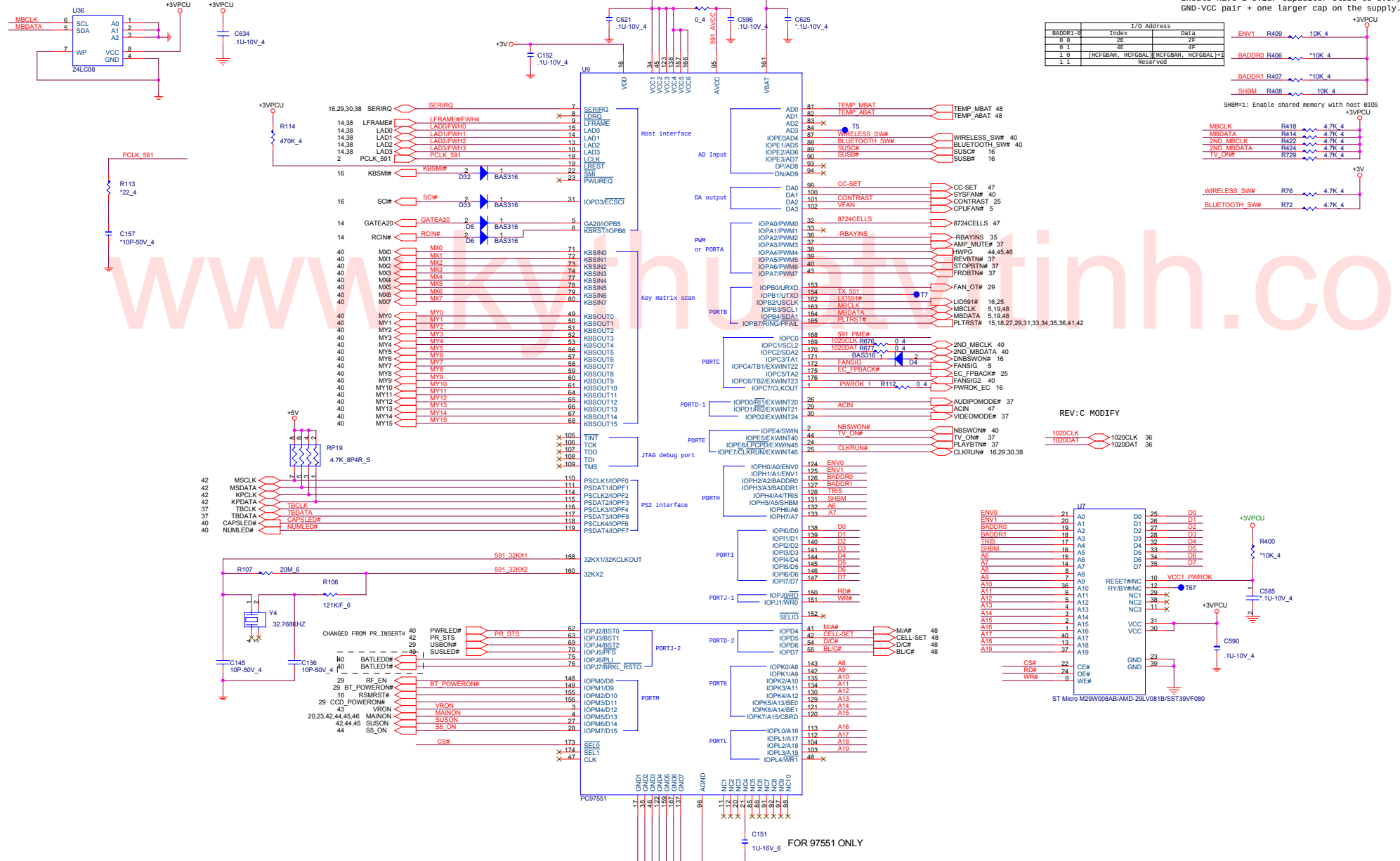


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FIR&CIR



U36 +3VPCU +3V



27 LAN_PME# ☐

Size	Document Number
	97551 & FLASH

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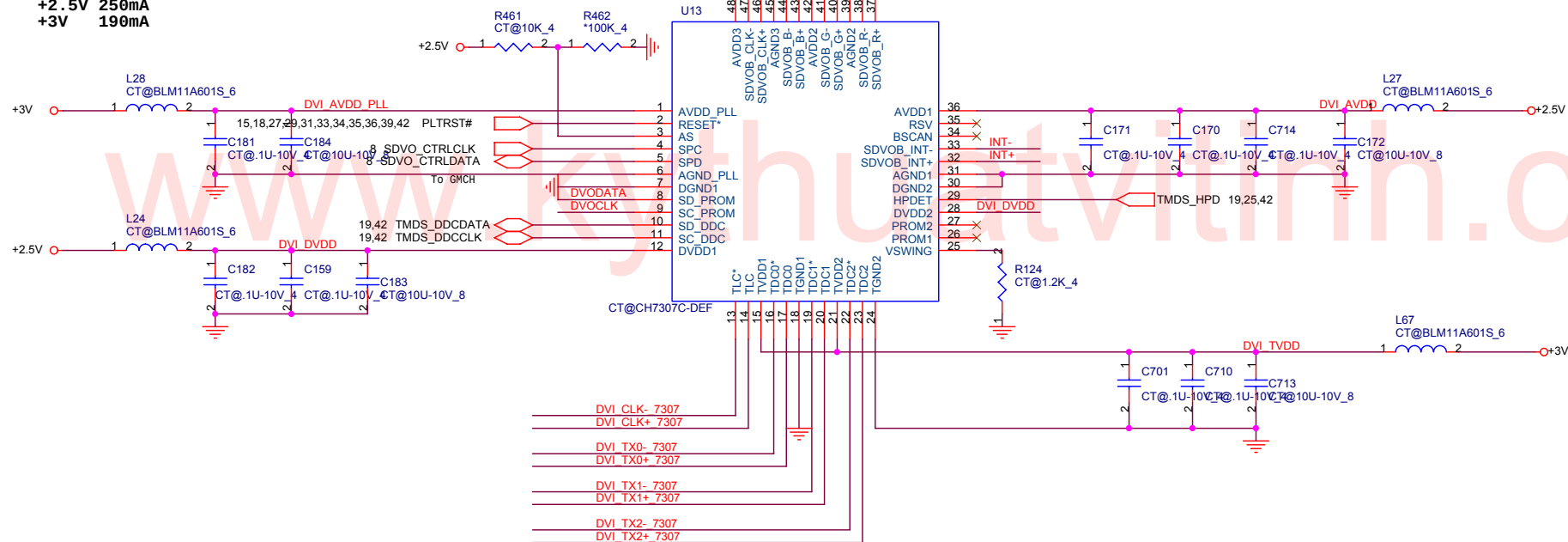
8,18 PEG_TXP0
8,18 PEG_TXN0
8,18 PEG_TXP1
8,18 PEG_TXN1
8,18 PEG_TXP2
8,18 PEG_TXN2
8,18 PEG_TXP3
8,18 PEG_TXN3

SDVOB_R+
SDVOB_R-
SDVOB_G+
SDVOB_G-
DVI_AVDD
SDVOB_B+
SDVOB_B-
SDVOB_CLK+
SDVOB_CLK-

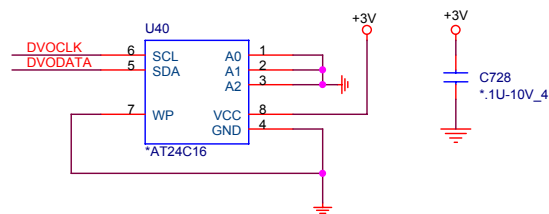
+2.5V R136 CT@4.7K 4 SDVO_CTRLCLK
+2.5V R137 CT@4.7K 4 SDVO_CTRLDATA

PULL LOW FOR DVO NOT PRESENT (INTERNAL PULLLOW IN 915GM)

+2.5V 250mA
+3V 190mA



ALWAYS NOT ON, TEST ONLY



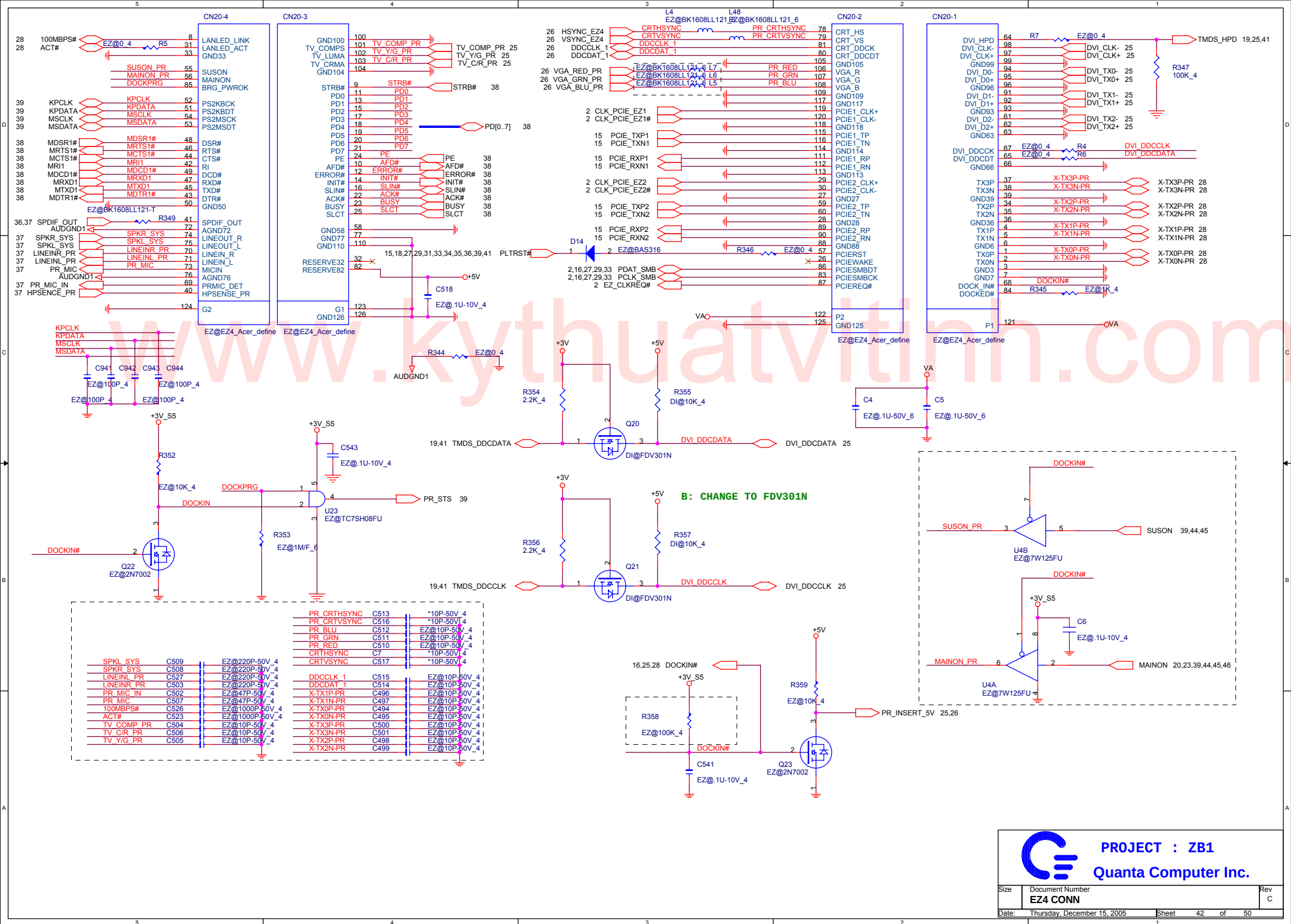
+3V R464 *1K_4 DVOCLK
+3V R465 *1K_4 DVODATA

RP18 CT@0_4P2R_S
DVI_CLK-_7307 3 4
DVI_CLK+_7307 1 2
RP21 CT@0_4P2R_S
DVI_TX0-_7307 3 4
DVI_TX0+_7307 1 2
RP23 CT@0_4P2R_S
DVI_TX1-_7307 3 4
DVI_TX1+_7307 1 2
RP25 CT@0_4P2R_S
DVI_TX2-_7307 3 4
DVI_TX2+_7307 1 2

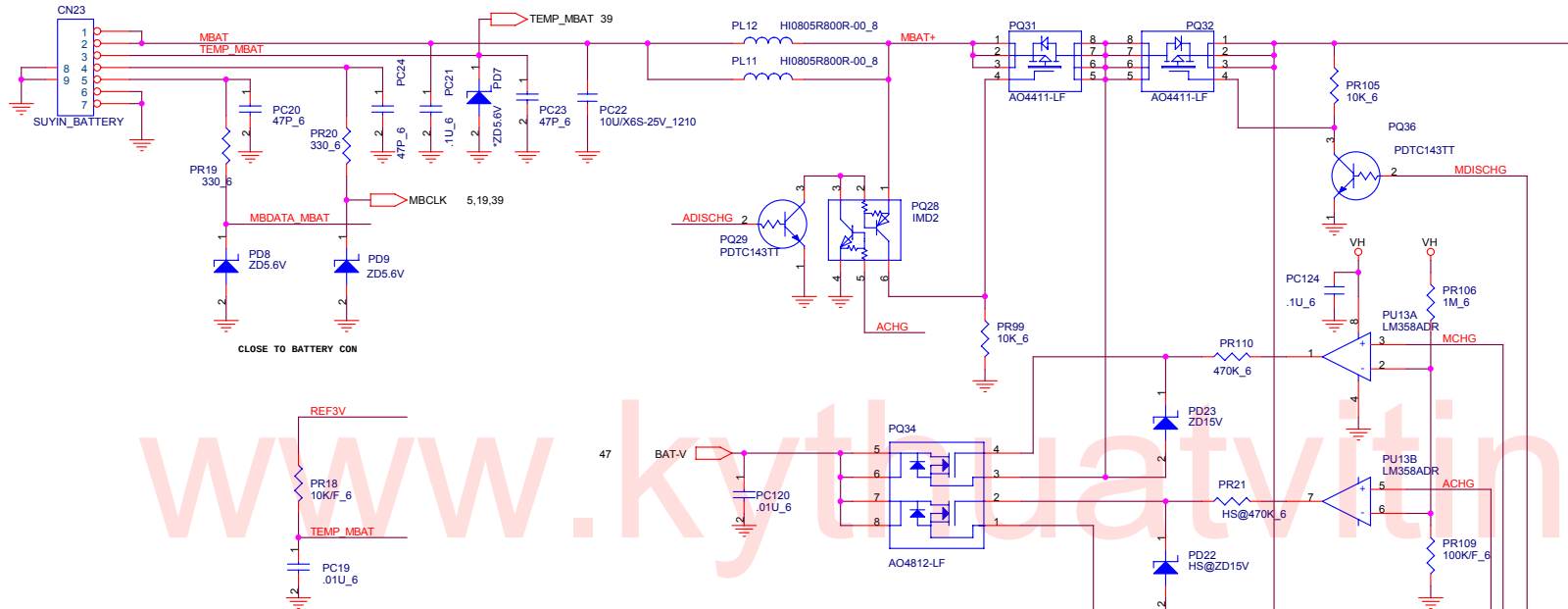


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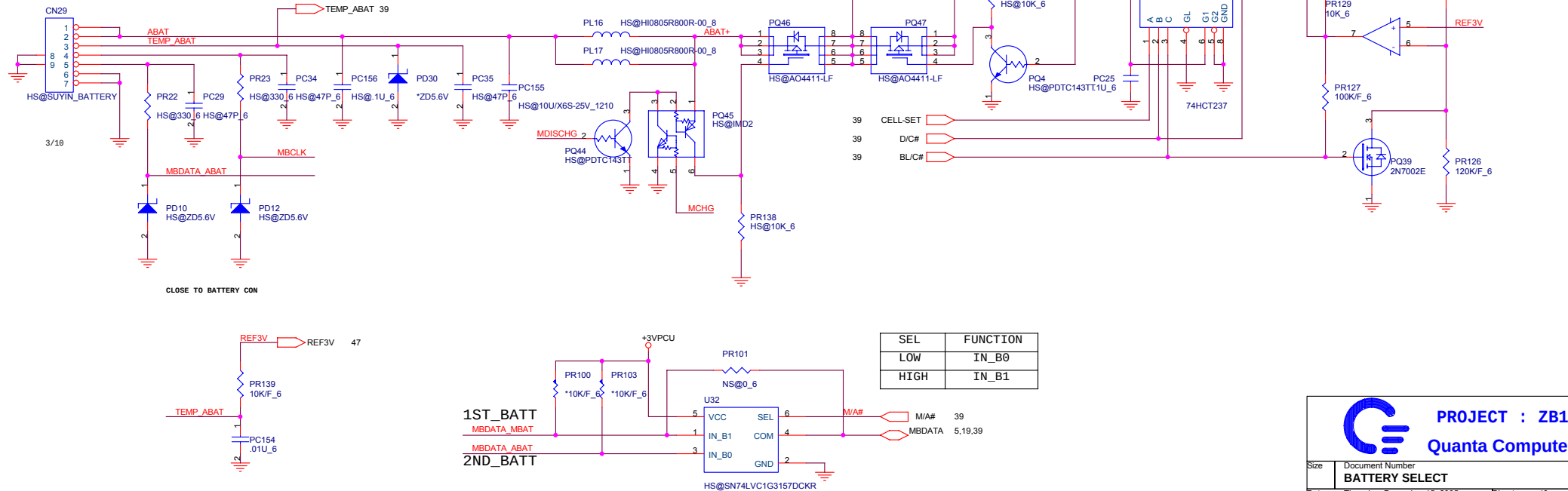
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1ST_BATT_CONN



2ND_BATT_CONN



SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1



PROJECT : ZB1
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- | | | |
|---|---------------------------------------|----------------|
|  <div style="display: inline-block; vertical-align: middle;"> PROJECT : ZB1
 Quanta Computer Inc. </div> | | |
| Size | Document Number
Change List | Rev
C |
| Date: | Thursday, December 15, 2005 | Sheet 49 of 50 |



NCPP@ Unstuff when use PATA HDD + PATA ODD.
 EV@ Stuff when use external VGA.
 IV@ Stuff when use UMA.
M56@ unstuff when use M52/54 ASIC.
 EZ@ Stuff when use EZ4.
 NZ@ Stuff when no EZ4.
 DI@ Stuff when use DVI port.
 CT@ Stuff when UMA with DVI port.
 CT_EV@ Stuff when UMA with DVI port or external VGA.
 SV@ Stuff when use S-video.
 GL@ Stuff when use Giga lan.
 NL@ Stuff when use 10/100 lan.
 CR@ Stuff when use card reader
 CR_PRO@ Stuff when card reader connector use PROCONN
 FI@ Stuff when use FIR.
 FW@ Stuff when use IEEE1394.
 PH@ Stuff when use PATA HDD.
 PP@ Stuff when use PATA HDD + PATA ODD.
 SH@ Stuff when use SATA HDD.
 SH_SP@ Stuff when use PATA to SATA bridge.
 SH_SP_SUN@ Stuff when PATA to SATA bridge use SUNPLUS chip.
 SH_SP_ULI@ Stuff when PATA to SATA bridge use ULI chip.
 WIRE@ Stuff when LCD connector use wire type.
 TV@ Stuff when use TV in.
 CD@ Stuff when use camera.
NCD@ unstuff when use camera.

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	SKU Note	C
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