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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0~S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well, Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0~S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0~S5



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Size
A3

Document Number

FRONTPAGE

Rev
1B

Date:

Tuesday, October 20, 2009

Sheet

2

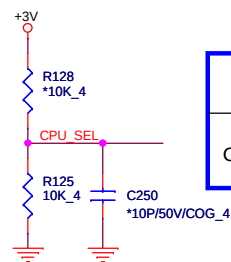
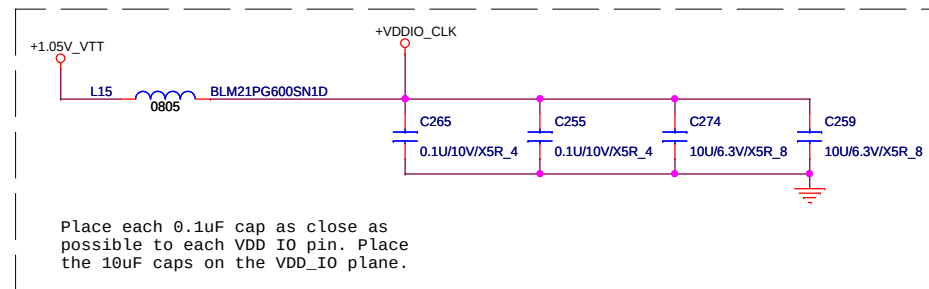
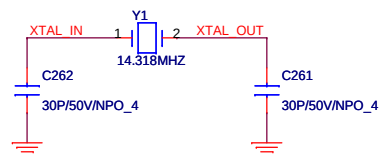
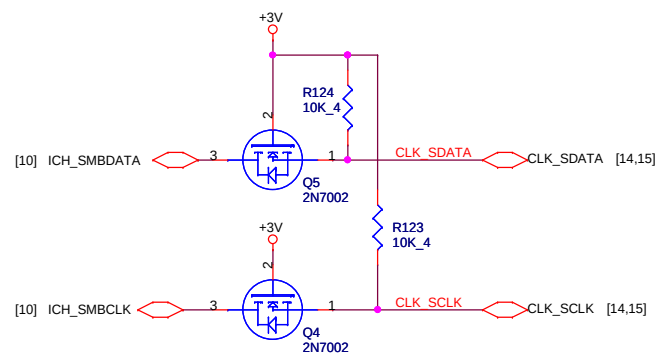
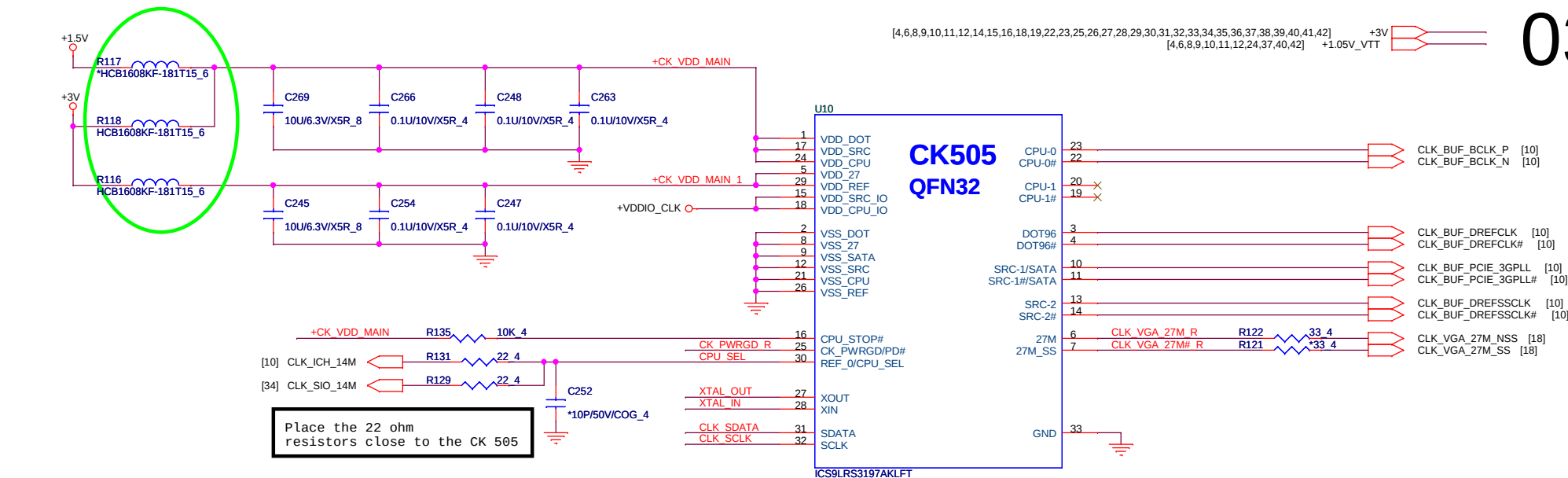
of

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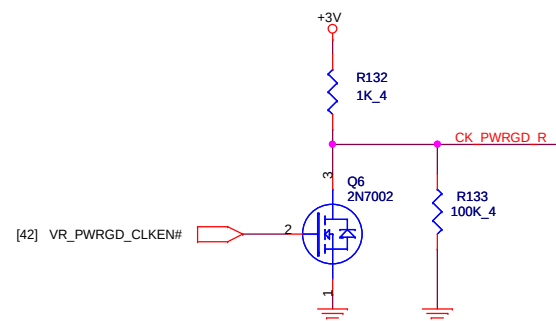
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[4,6,8,9,10,11,12,24,37,40,42]

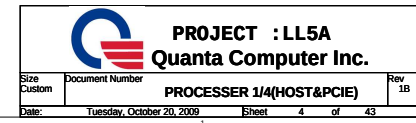
+3V

+1.05V_VTT



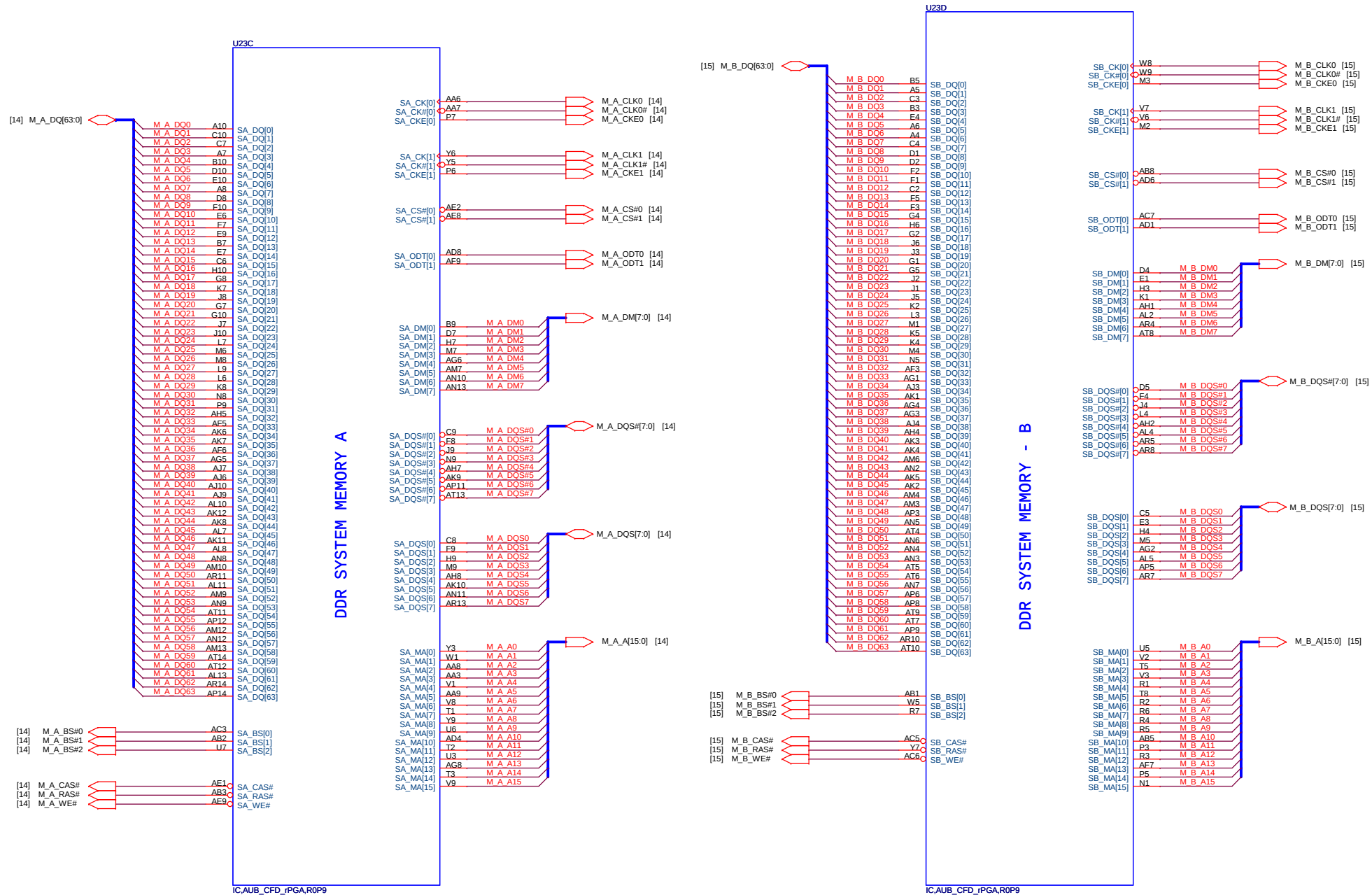
	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz





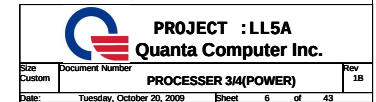
AUBURNDALE PROCESSOR (DDR3)

05



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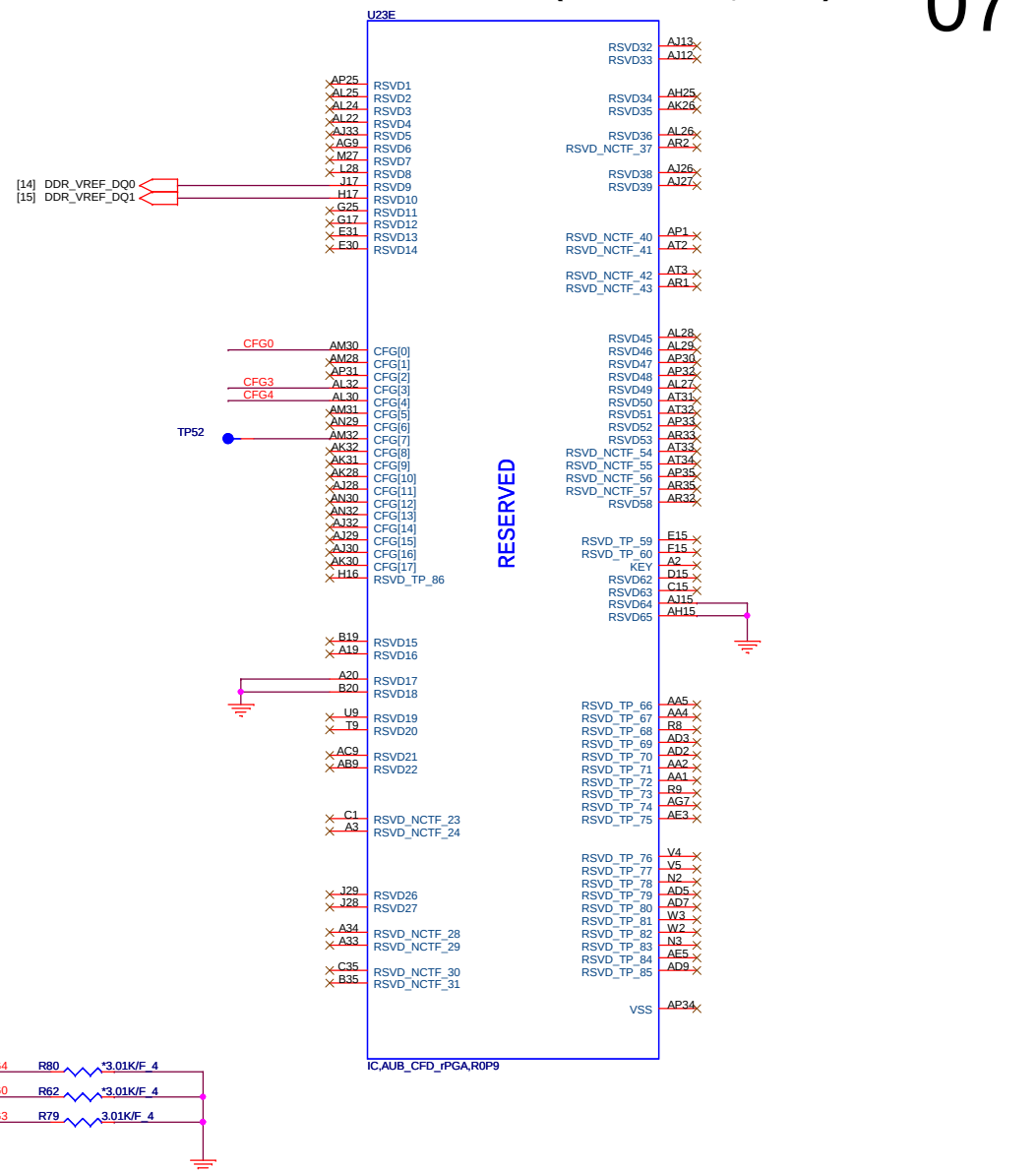
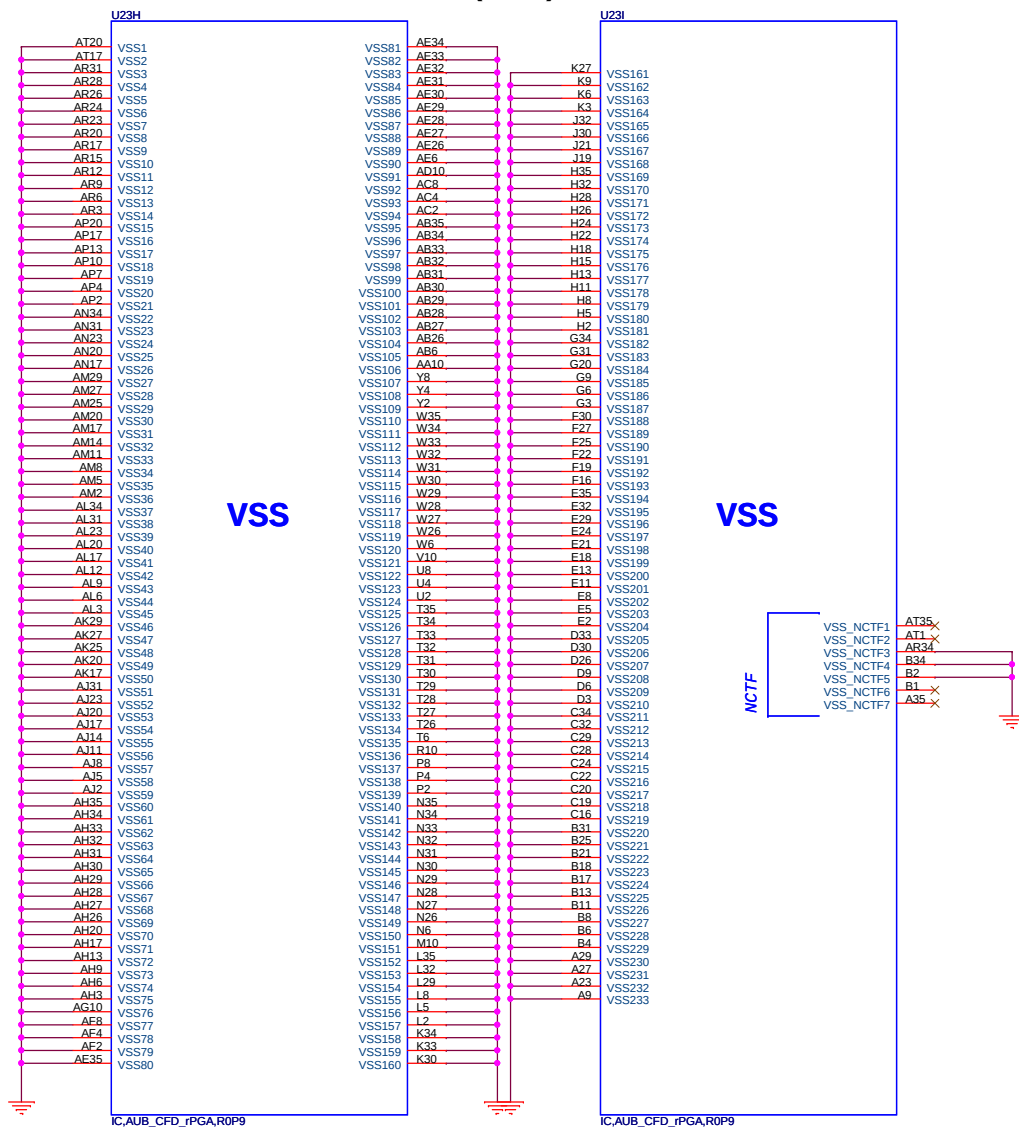
Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	1B
Date:	Tuesday, October 20, 2009	Sheet 5 of 43



AUBURNDALE PROCESSOR (GND)

AUBURNDALE PROCESSOR(RESERVED, CFG)

07



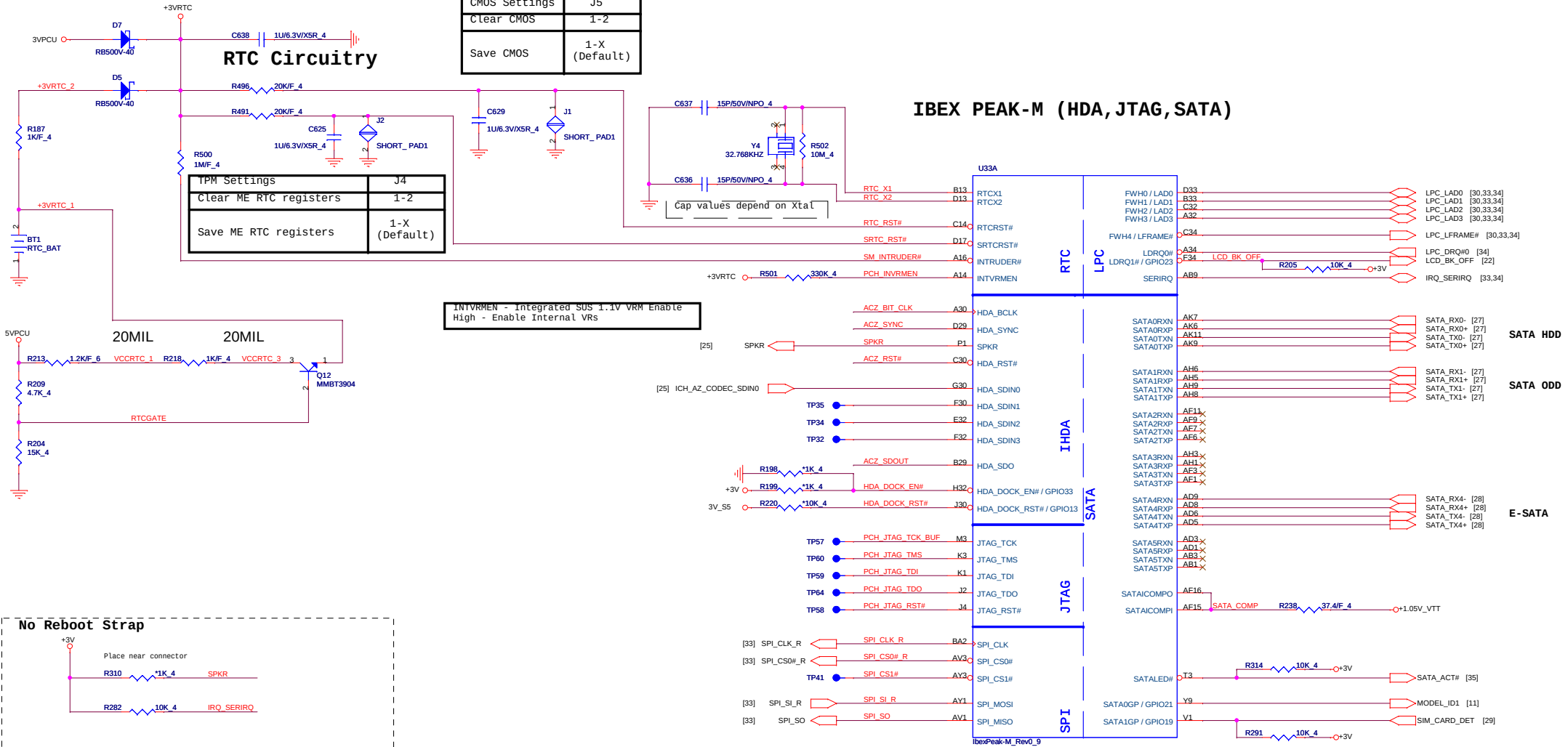
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

RTC Circuitry

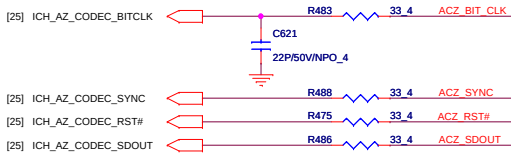
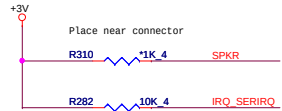
CMOS Settings	J5
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J4
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

IBEX PEAK-M (HDA, JTAG, SATA)



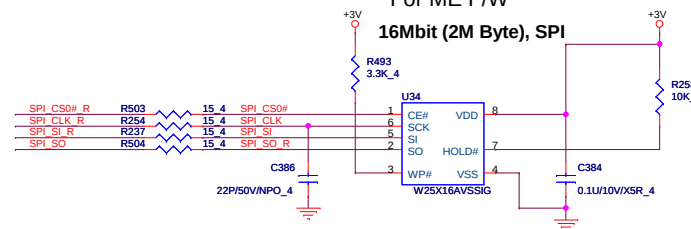
No Reboot Strap



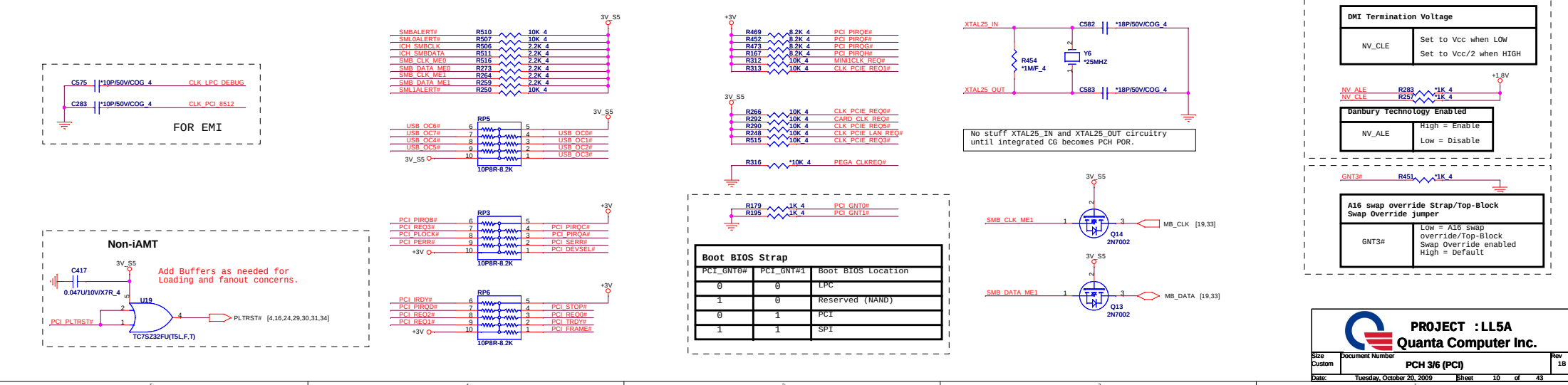
Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

iTPM ENABLE/DISABLE

TPM Function	R292
Enable	Stuff
Disable	NC (Default)



For ME F/W 16Mbit (2M Byte), SPI



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

[3,4,6,8,9,10,12,14,15,16,18,19,22,23,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42]

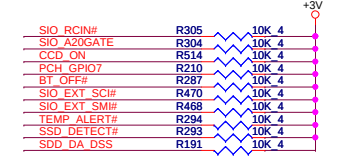
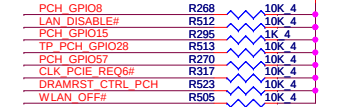
+3V

[4,8,9,10,12,24,30,37]

3V_S5

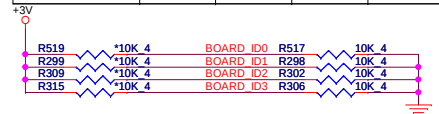
[3,4,6,8,9,10,12,24,37,40,42]

11



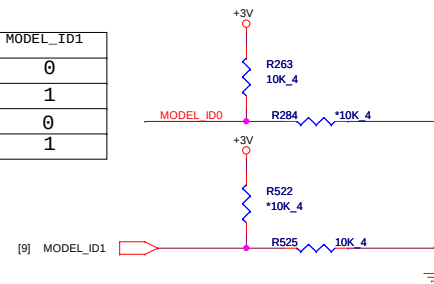
Board ID

Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0



Model ID

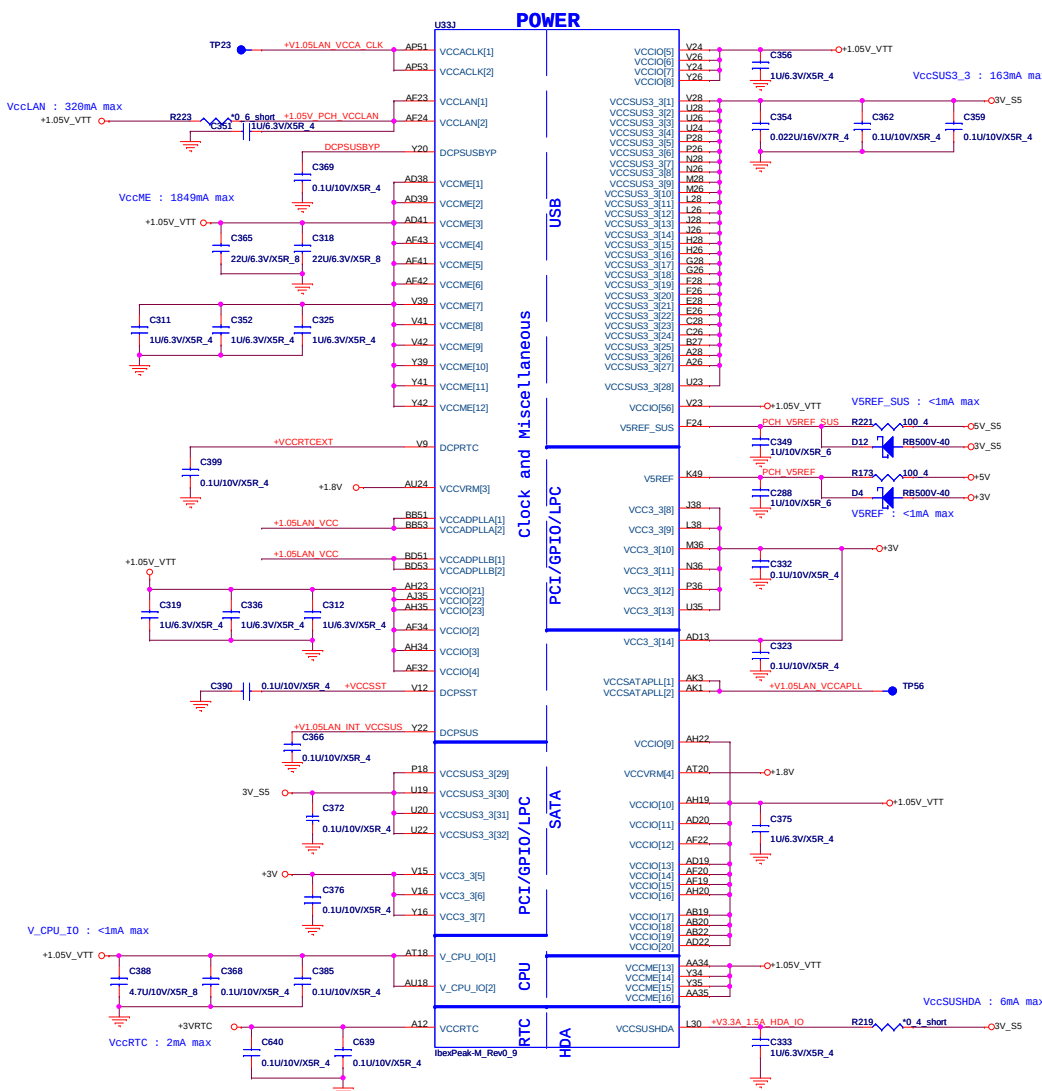
Model ID	MODEL_ID0	MODEL_ID1
Default	0	0
LL3/LL3A	0	1
LL5/LL5A	1	0
	1	1

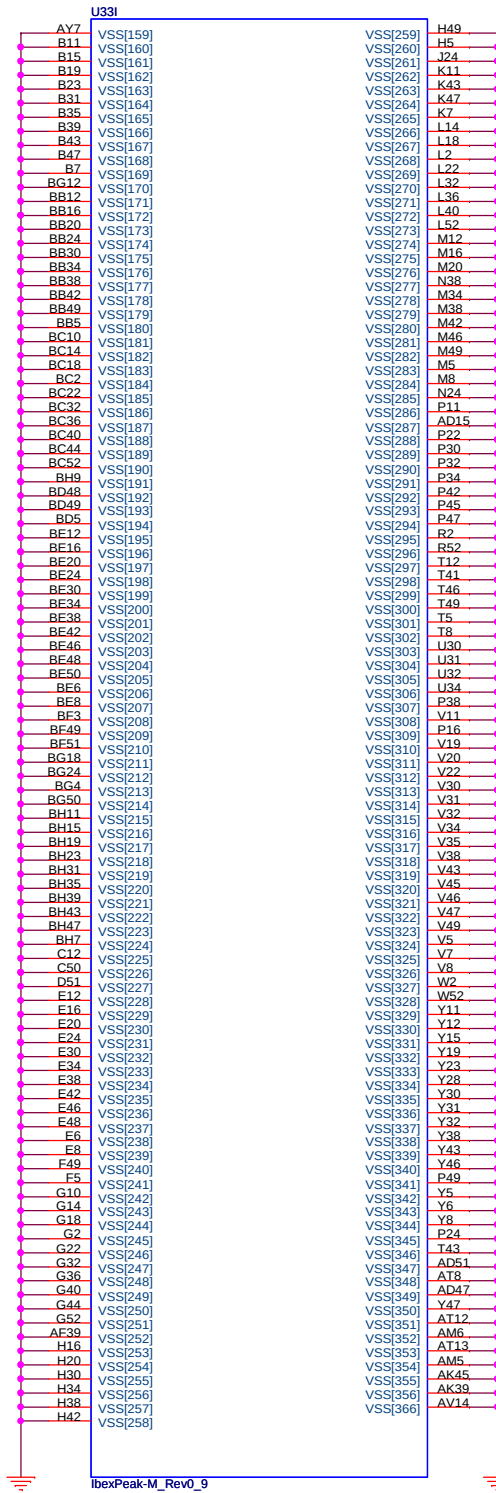
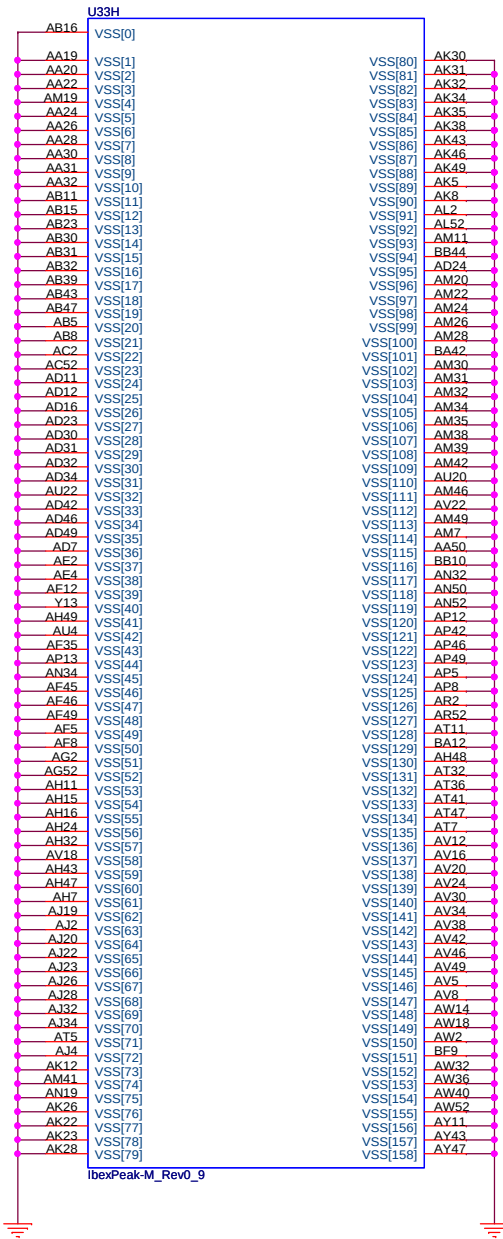


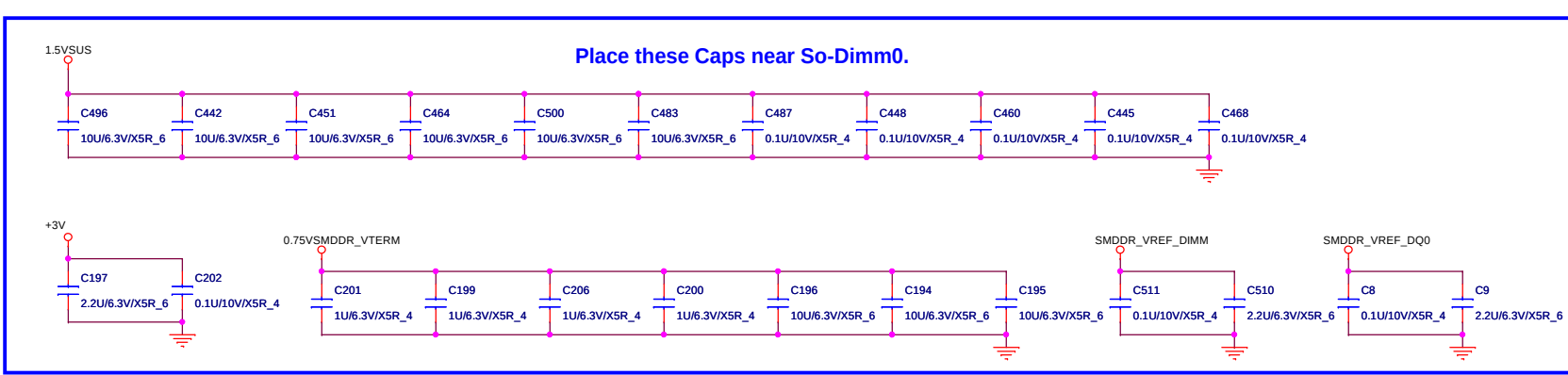
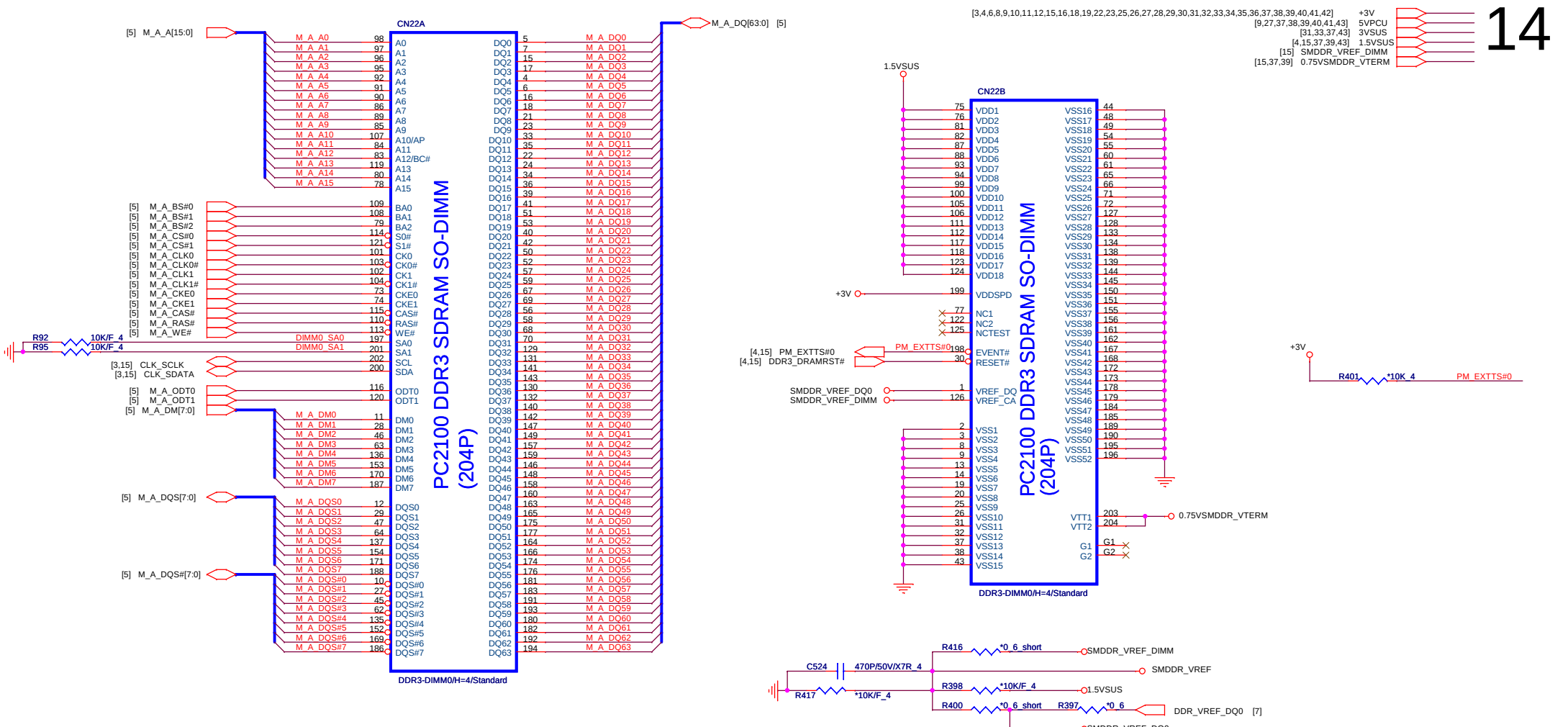
SV_SET_UP 1-X High = Strong (Default)

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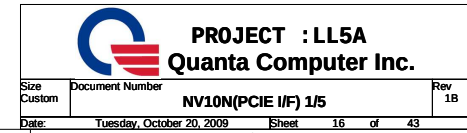
Size Custom Document Number PCH 4/6 (GPIO) Rev 1B
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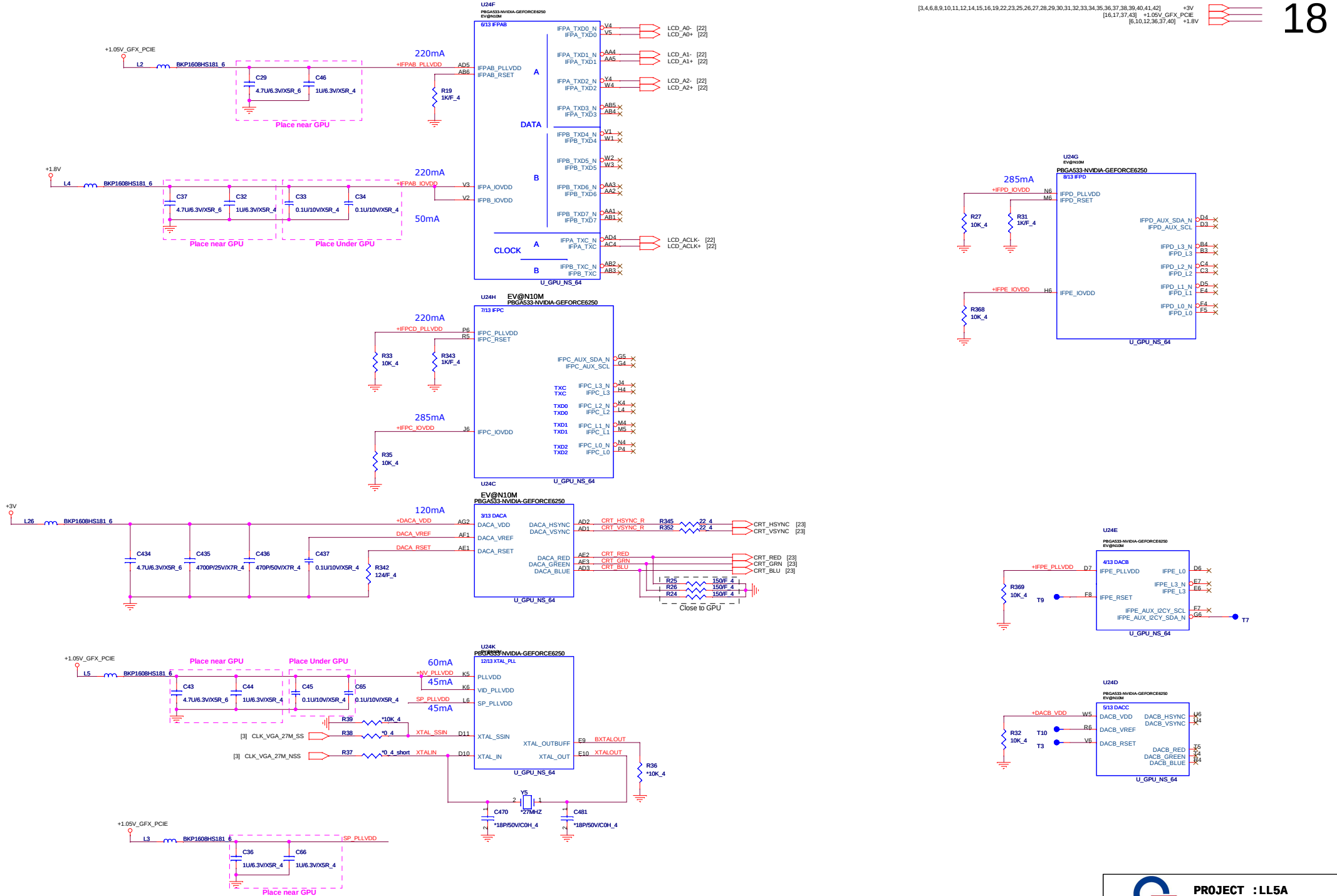




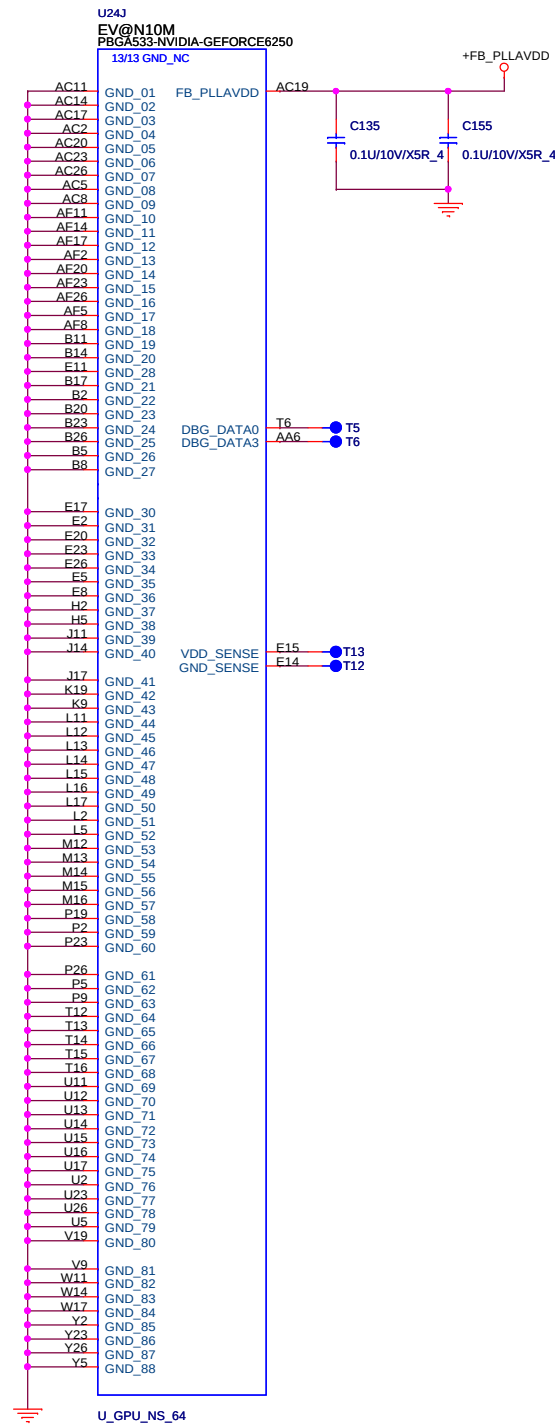




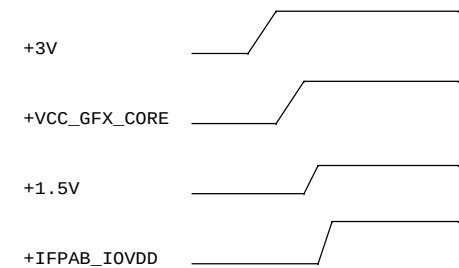








power up sequence



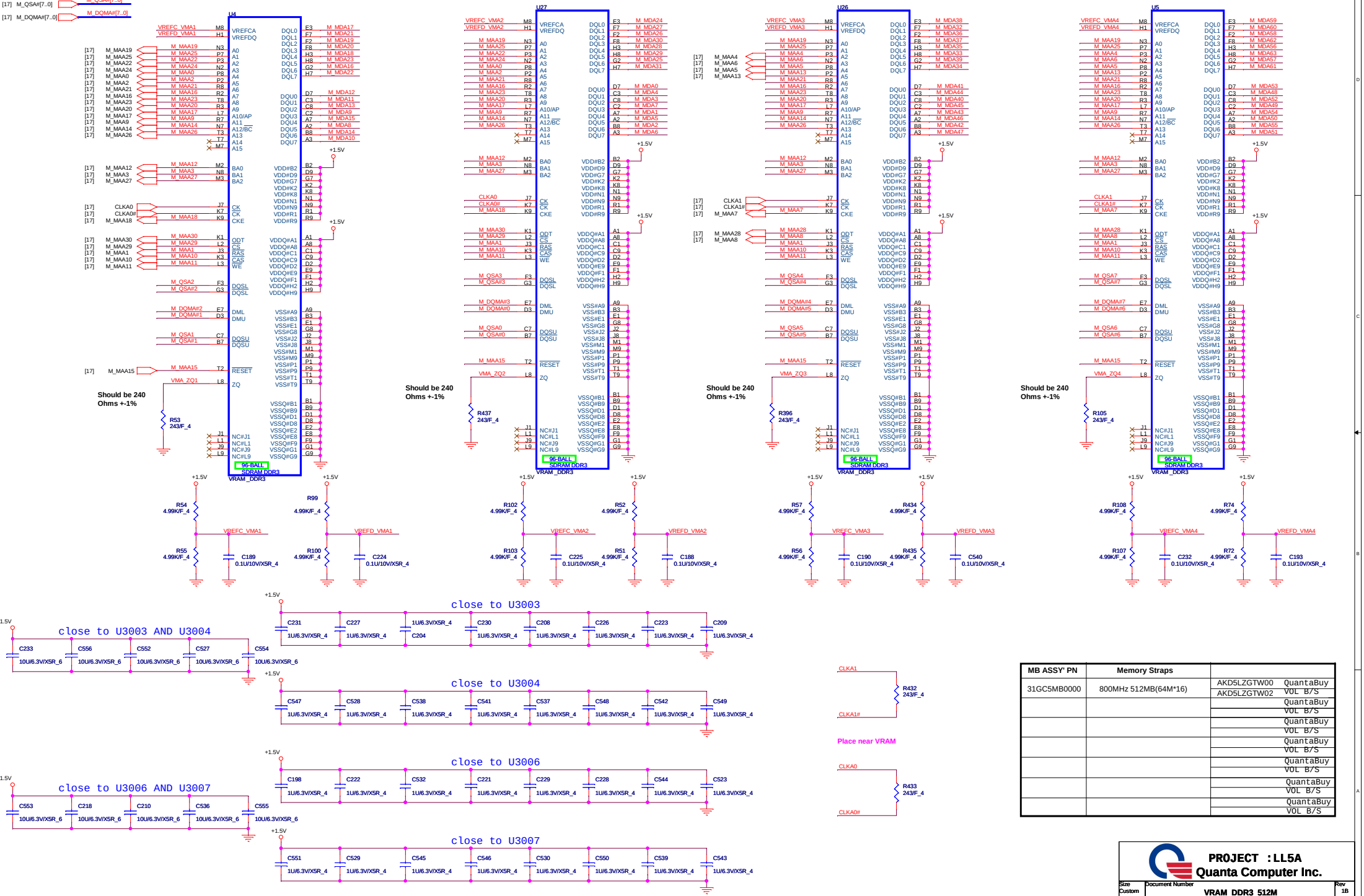
PROJECT : LL5A
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Size Custom	Document Number N10M (GND) 5/5	Rev 1B
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256MB/ 512MB DDR3

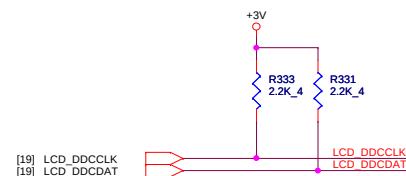
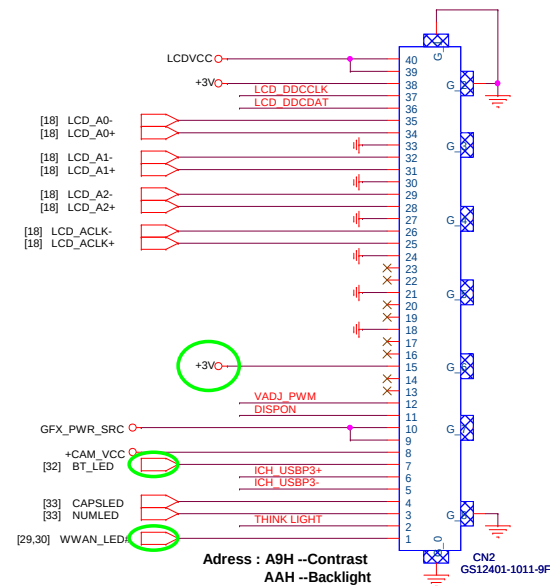
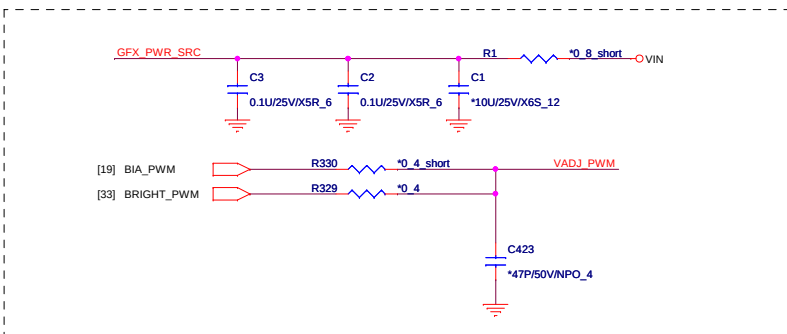
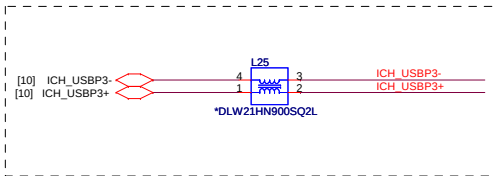
[3.17,29,30,31,39] +1.5V

- [17] M_MDA[63..0] M_MDA[63..0]
- [17] M_QSA[7..0] M_QSA[7..0]
- [17] M_QSA[7..0] M_QSA[7..0]
- [17] M_QMA[7..0] M_QMA[7..0]



MB ASSY PN	Memory Straps		
31G55MB0000	800MHz 512MB(64M*16)	AKD5LZGTW00	QuantaBuy
		AKD5LZGTW02	VOL B/S
			QuantaBuy
			VOL B/S
			QuantaBuy
			VOL B/S
			QuantaBuy
			VOL B/S
			QuantaBuy
			VOL B/S
			QuantaBuy
			VOL B/S

The schematic diagram illustrates the LCDVCC power supply circuit. It starts with a 15V input connected to a 330K_4 resistor (R328). The output of R328 is connected to the gate of MOSFET Q20 (2N7002). The source of Q20 is grounded, and its drain is connected to the gate of MOSFET Q21 (AO3404). The source of Q21 is grounded, and its drain is connected to the gate of MOSFET Q23 (2N7002). The source of Q23 is grounded, and its drain is connected to the LCDVCC output. A 10_8_short resistor (R332) is connected between the drain of Q21 and the LCDVCC output. A 22_8 resistor (R338) is connected between the LCDVCC output and ground. A 0.022U/25V/X7R_6 capacitor (C424) is connected between the gate of Q21 and ground. A 10U/6.3V/X5R_8 capacitor (C426) is connected between the LCDVCC output and ground. The ENVDD input is connected to a 100K_4 resistor (R335) and a 100K_4 resistor (R334). The output of R334 is connected to the gate of Q20. The output of R335 is connected to the gate of Q23. The output of R334 is also connected to the gate of Q21. The output of R335 is also connected to the gate of Q23. The output of R334 is also connected to the gate of Q20. The output of R335 is also connected to the gate of Q23.

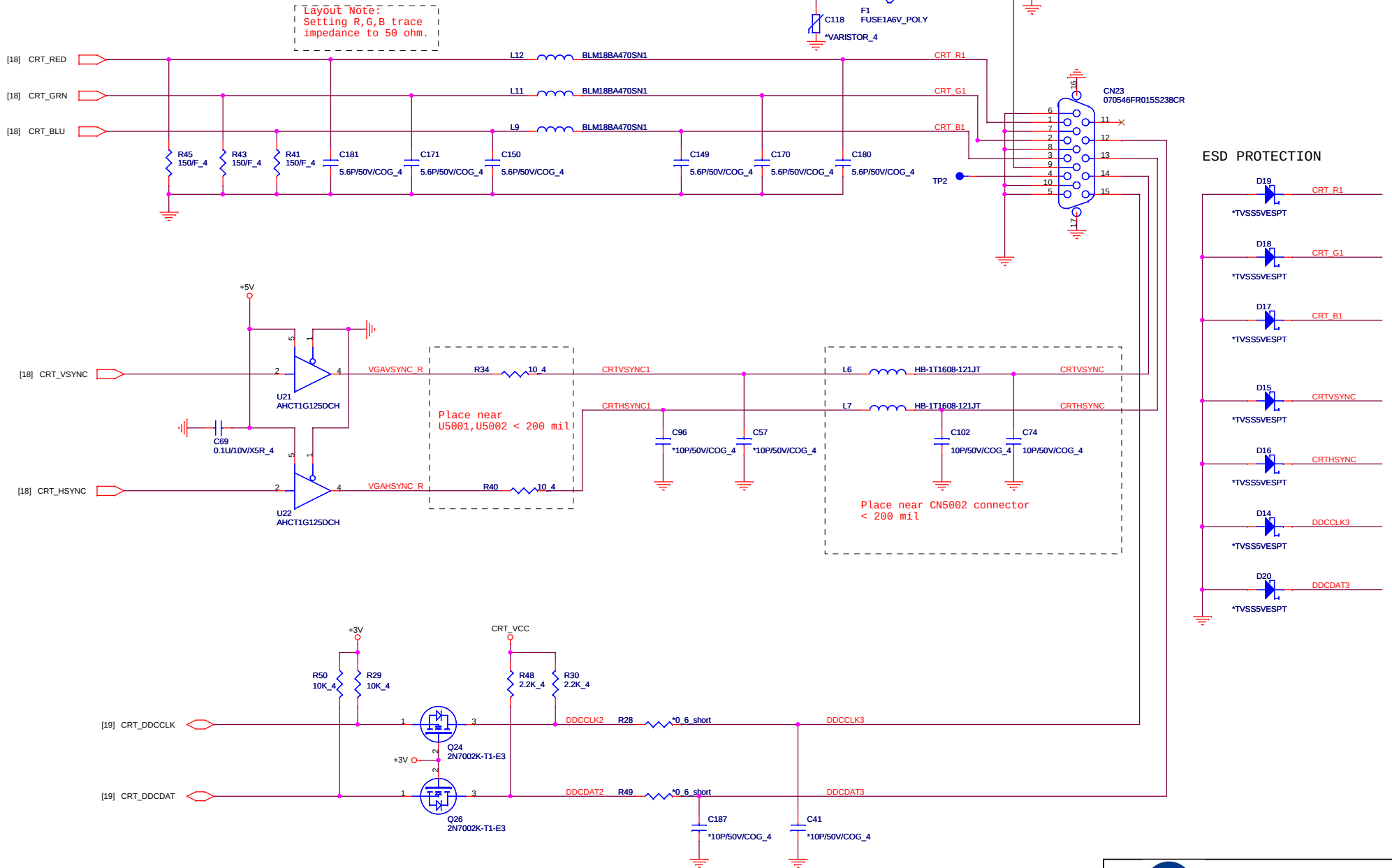
[illegible]

THINK LIGHT LED ON

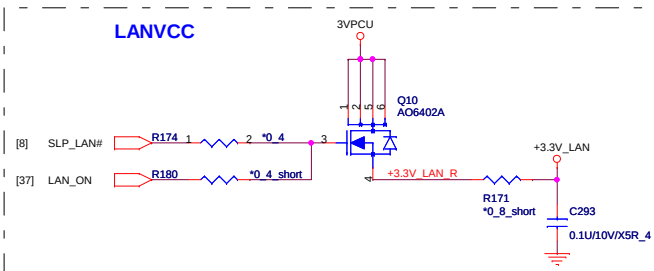
[33] THINK LIGHT#

CAMERA VCC Control

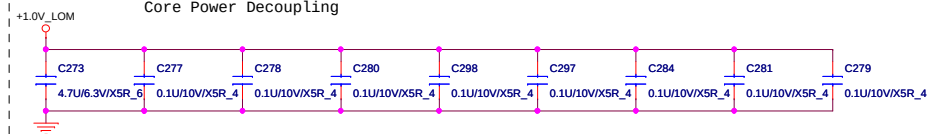
The schematic diagram illustrates the CAMERA VCC Control circuit. It includes a +5V supply, a +CAM_VCC output, and a ground connection. A CCD_ON signal is connected to a red trapezoidal symbol. The circuit features a 1uF/6.3V/X5R_4 capacitor (C13) connected to the +5V supply. A 10k resistor (R9) is connected between the +5V supply and the VIN pin of the U1 AT5231H-3.3KER chip. A 10k resistor (R3) is connected between the CCD_ON signal and the SHDN pin of U1. The GND pin of U1 is connected to ground. The VOUT pin of U1 is connected to the +CAM_VCC output. A 215kF_4 resistor (R5) is connected between the +CAM_VCC output and the SET pin of U1. A 100kF_4 resistor (R2) is connected between the SET pin of U1 and ground. A 4.7uF/6.3V/X5R_6 capacitor (C12) is connected between the +CAM_VCC output and ground.



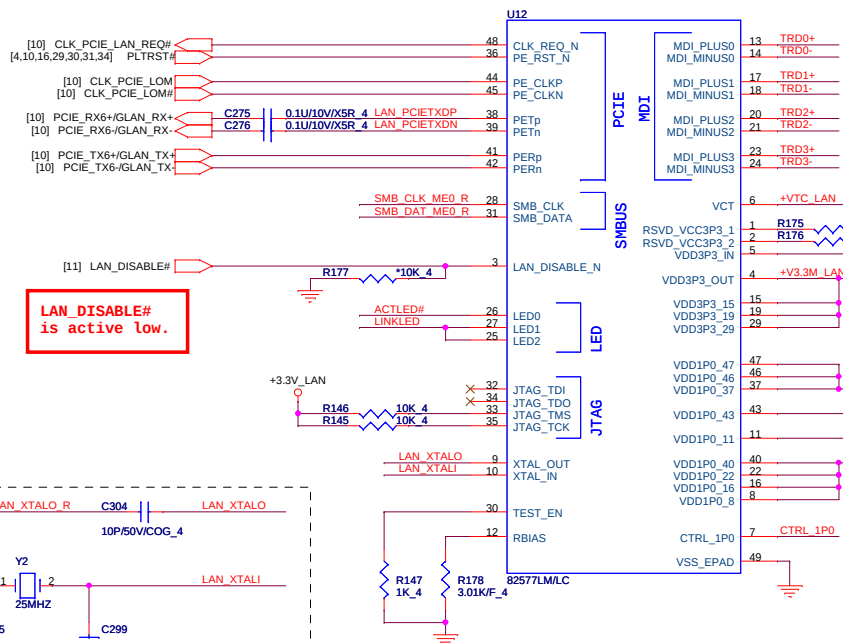
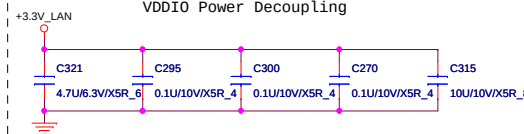
LANVCC



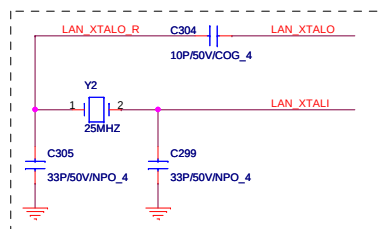
Core Power Decoupling



VDDIO Power Decoupling

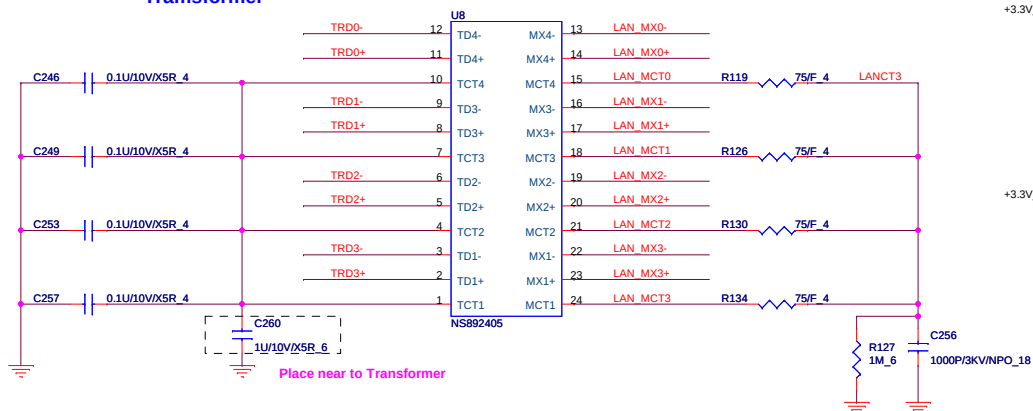


LAN_DISABLE#
is active low.



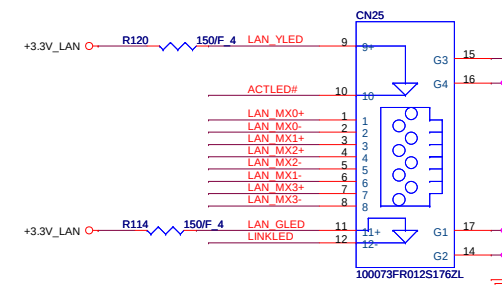
C stage(For EMI)

Transformer



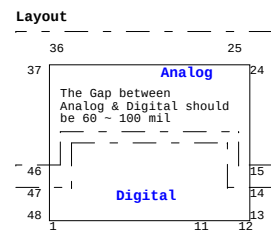
Place near to Transformer

RJ45 Connector

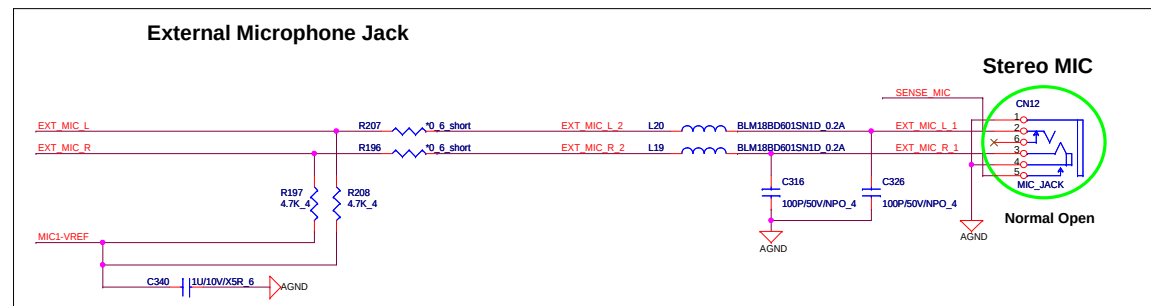
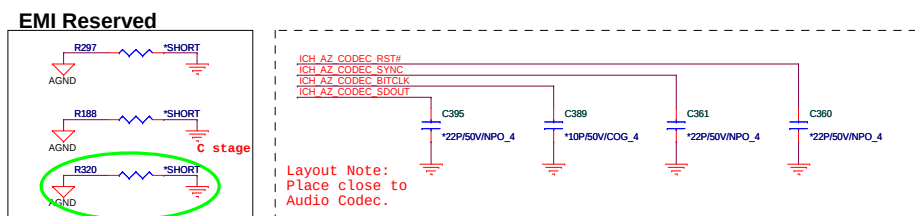
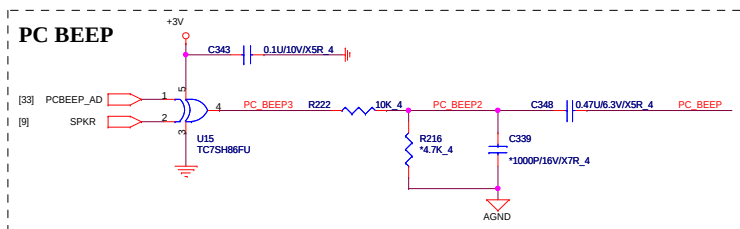
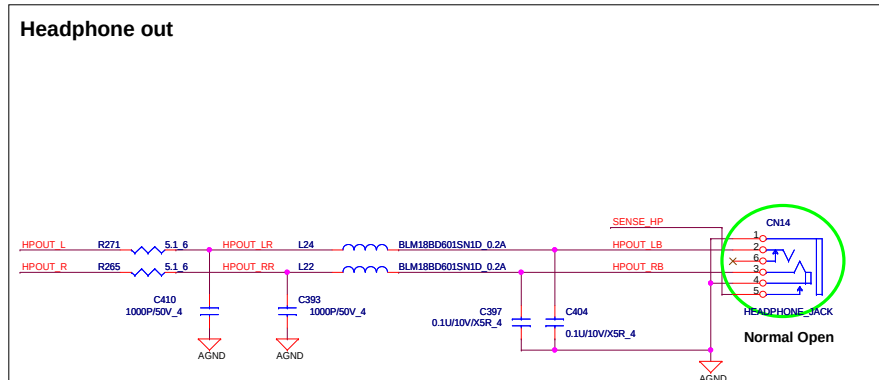


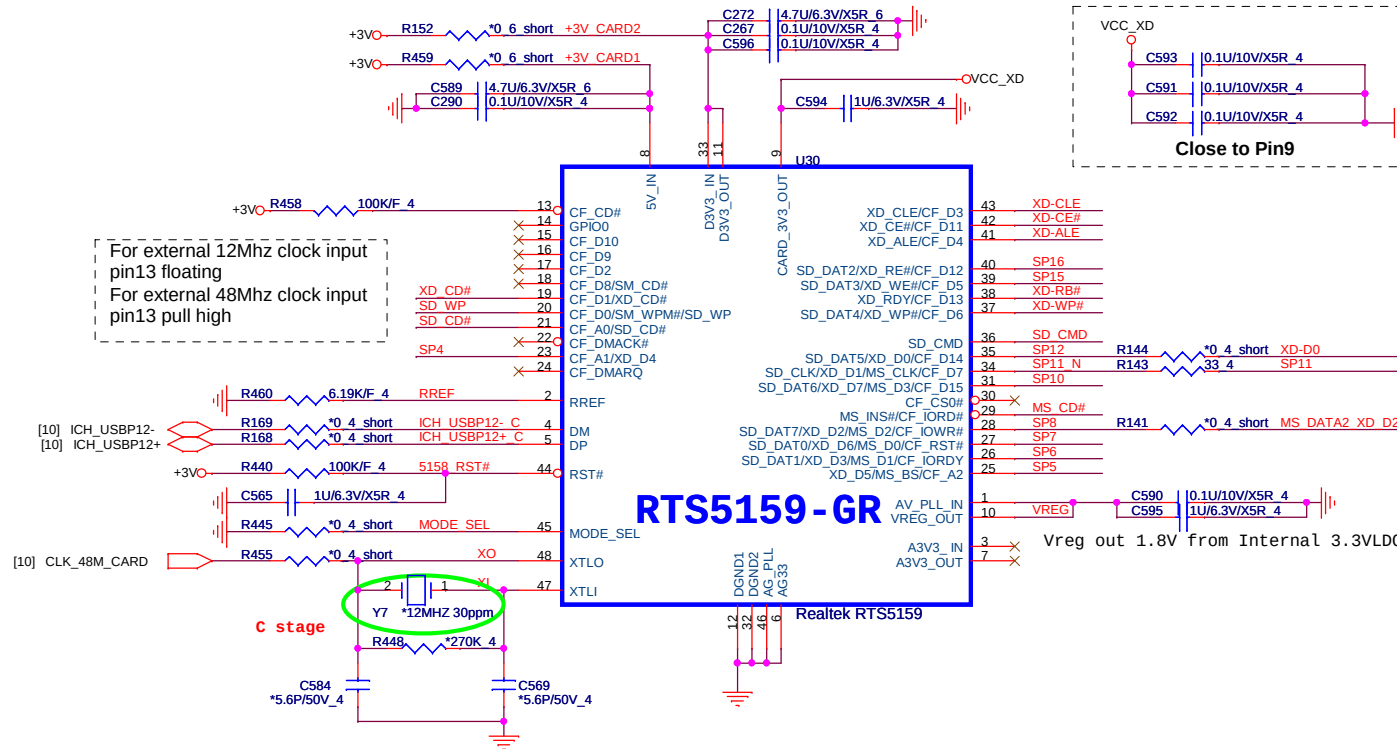
PROJECT : LL5A
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Custom	LAN(82577LM)	1B
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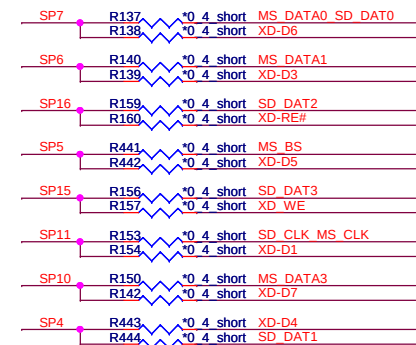
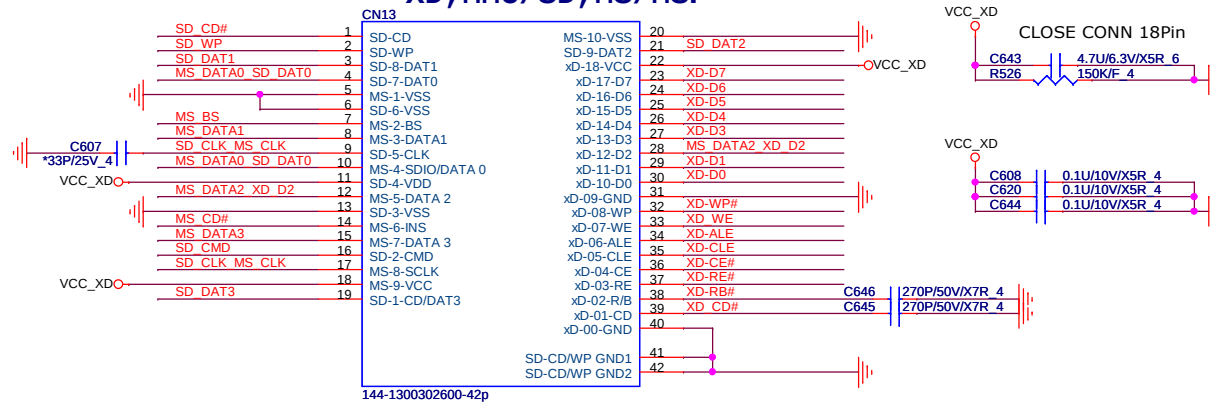


Sense_A	Sense_B	RES
Port_A	Port_E	39.2K
Port_B	Port_F	20K



**Note:**

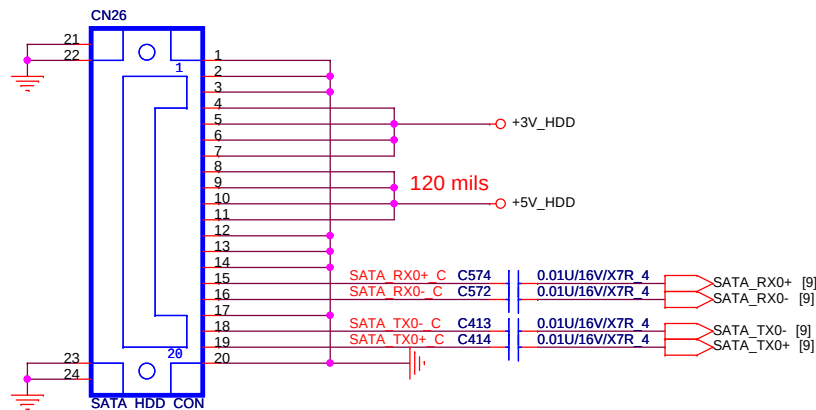
SD/MMC	MS	XD
SP0		
SP1	SD WP	XD_CD#
SP2	SD CD#	
SP3	SD DAT1	XD D4
SP4		XD D5
SP5	MS BS	XD D3
SP6	MS D1	XD D6
SP7	SD DAT0	XD D2
SP8	MS D2	
SP9	MS INS#	
SP10	SD DAT6	XD D7
SP11	SD CLK	XD D1
SP12	SD DAT5	XD D0
SP13	SD DAT4	XD WP#
SP14		XD R/B#
SP15	SD DAT3	XD WE#
SP16	SD DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE

For RTS5159**5 IN1 CARD READER
XD, MMC/SD, MS/MSP**

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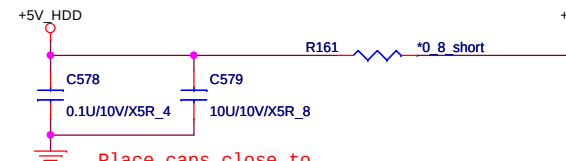
Size	Document Number	Rev
B	Card Reader (RTS5159)	1B
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SATA-HDD CONNECTOR

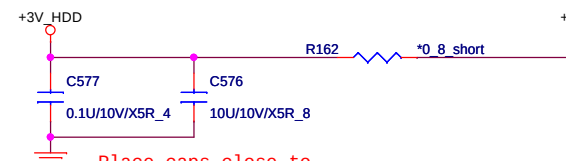


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 [12,22,23,25,32,33,34,35,37,38] +3V
 [22,37,39,41] +5V
 [9,37,38,39,40,41,43] 5VPCU
 [9,22,24,33,34,35,37,38,40,41,43] 3VPCU

27

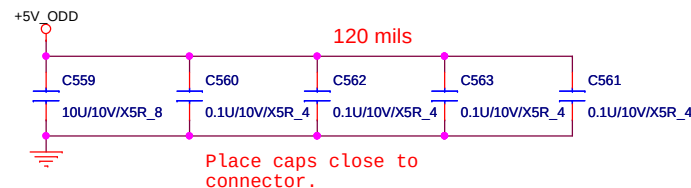
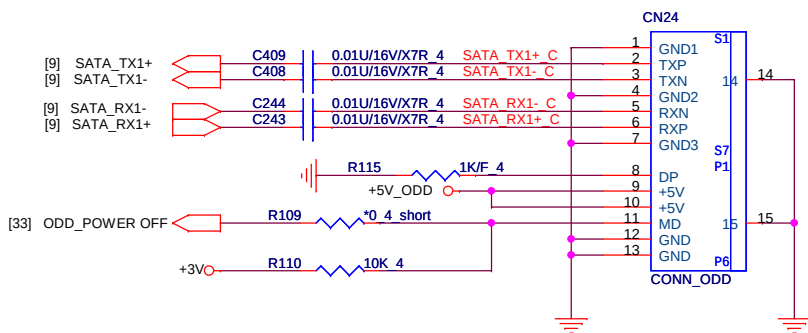


Place caps close to connector.

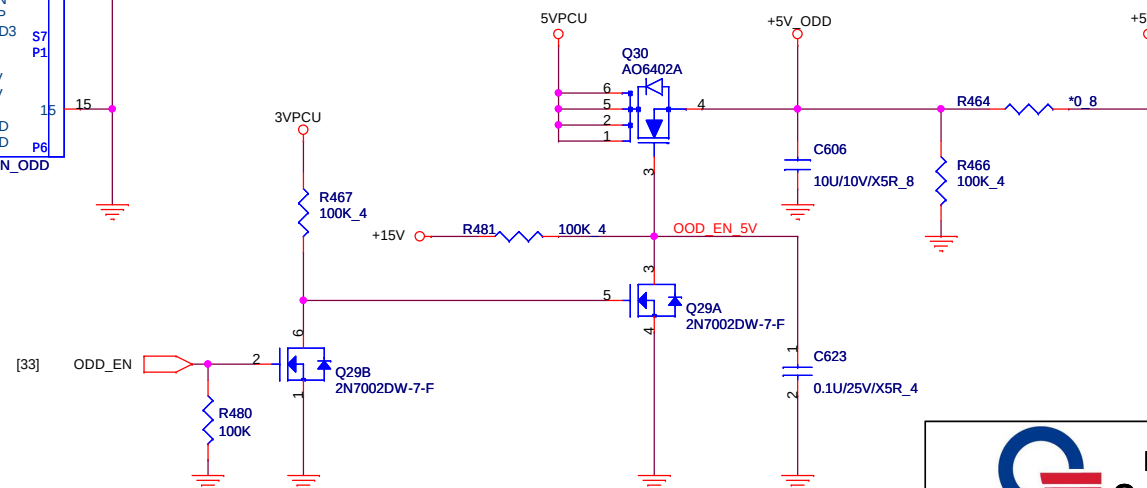


Place caps close to connector.

SATA CD-ROM



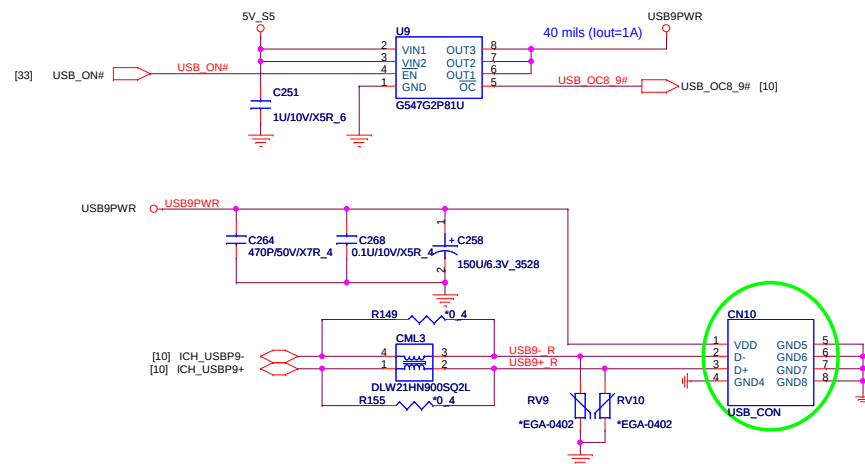
Place caps close to connector.



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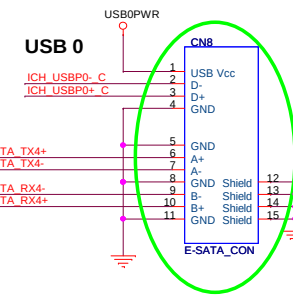
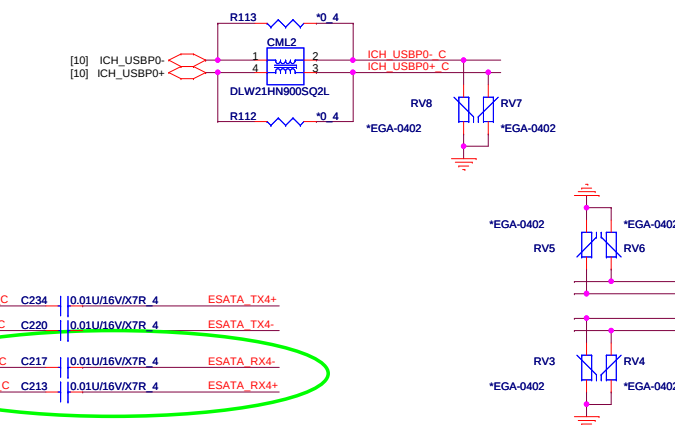
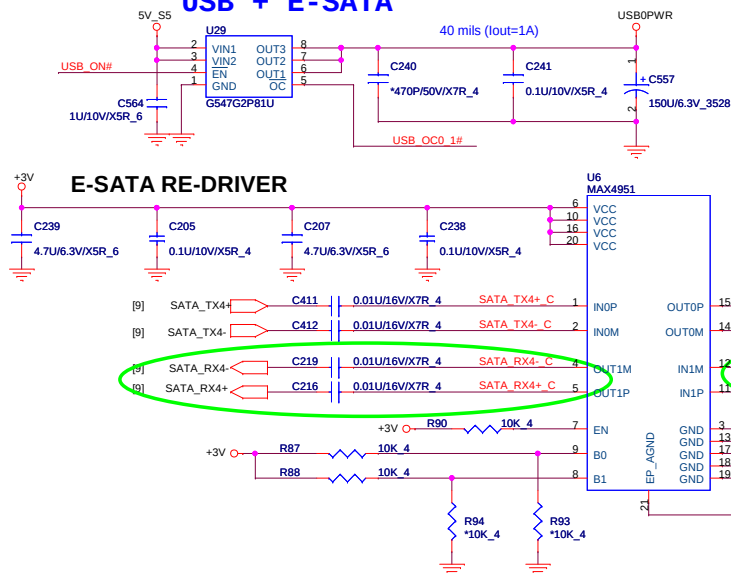
Size	Document Number	Rev
Custom	HDD/ODD	1B
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USB 4



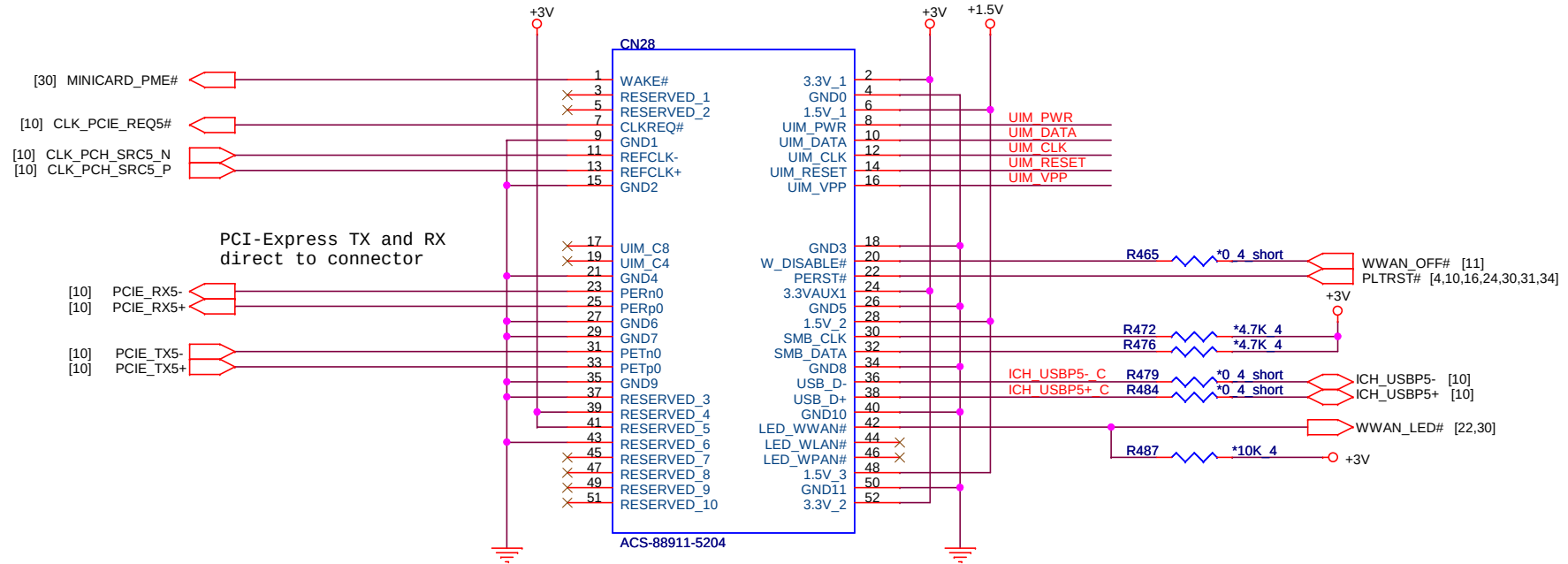
USB 1

USB + E-SATA

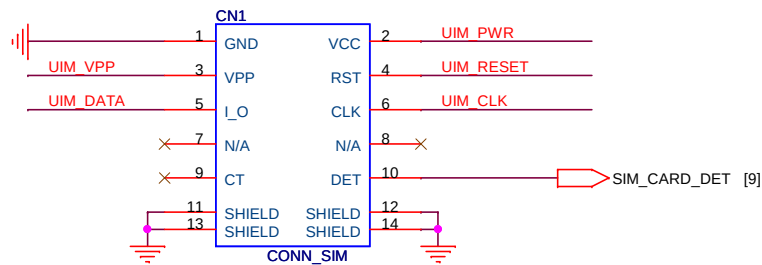


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

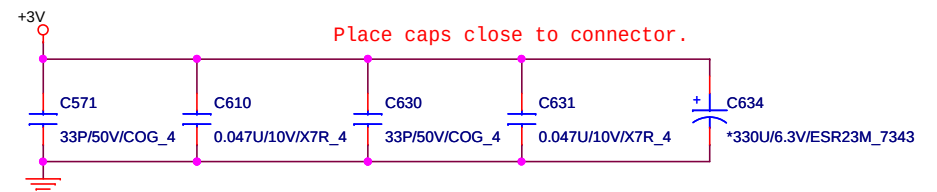
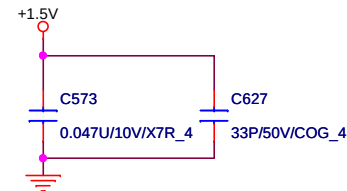
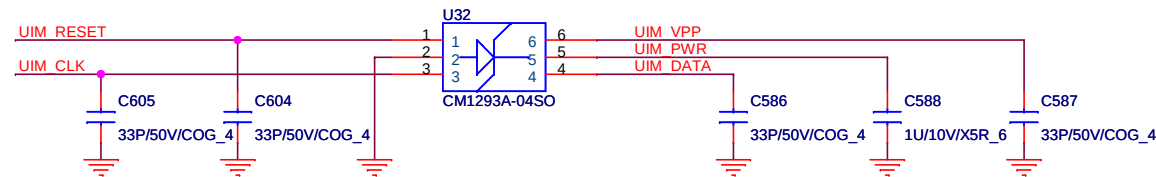
MiniCard WWAN connector



SIM Card CONN



Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible



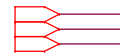
PROJECT : LL5A
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Size Custom	Document Number	Rev 1B
	MINI-Card (WWAN)	
Date:	Tuesday, October 20, 2009	Sheet 29 of 43

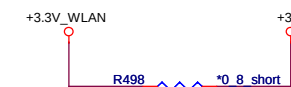
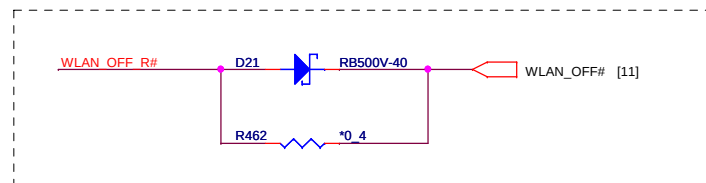
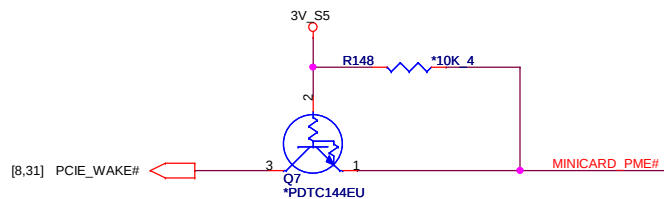
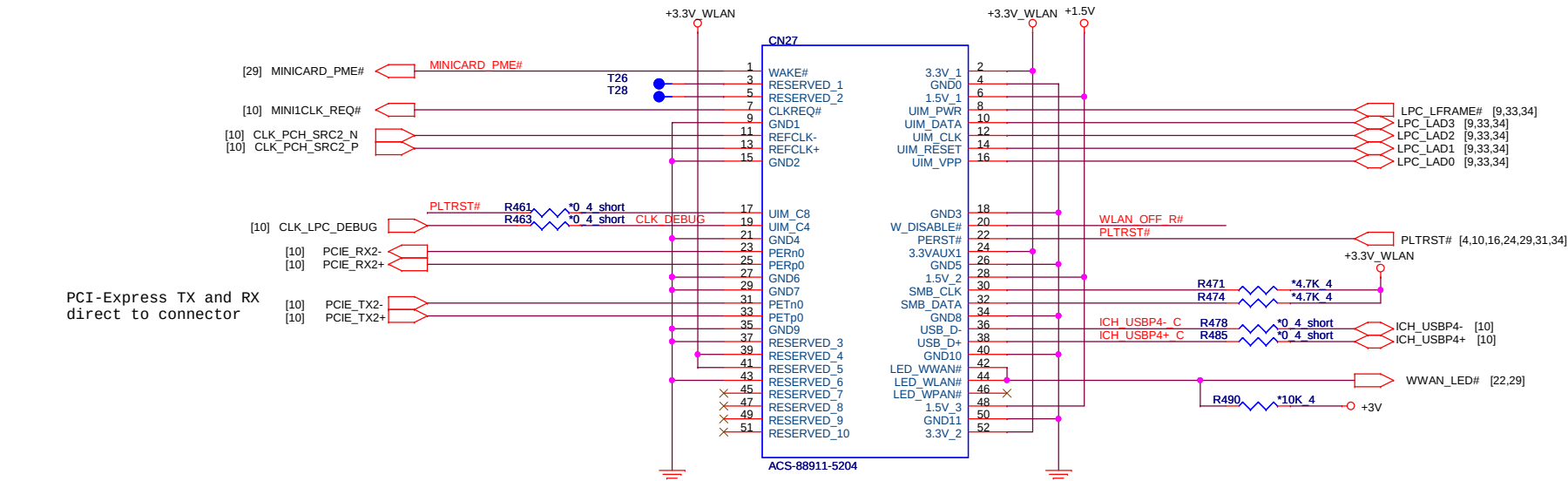
MiniCard WLAN/WiMAX connector

[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,25,26,27,28,29,31,32,33,34,35,36,37,38,39,40,41,42]
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[4,8,9,10,11,12,24,37]

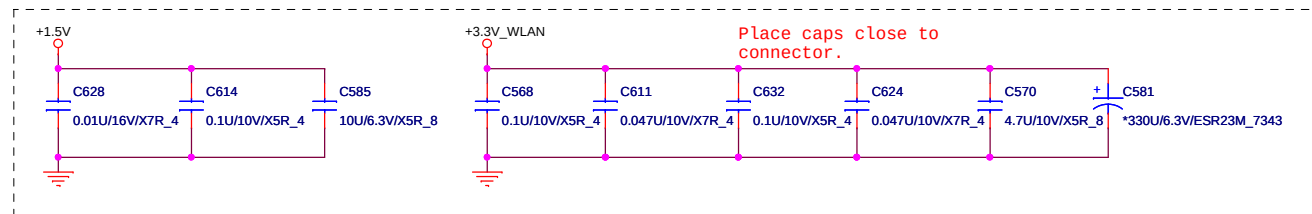
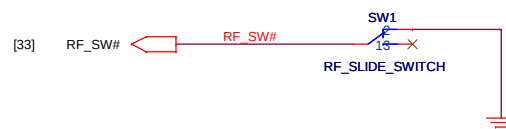
+3V
+1.5V
3V_S5



30



RF ON/OFF SWITCH



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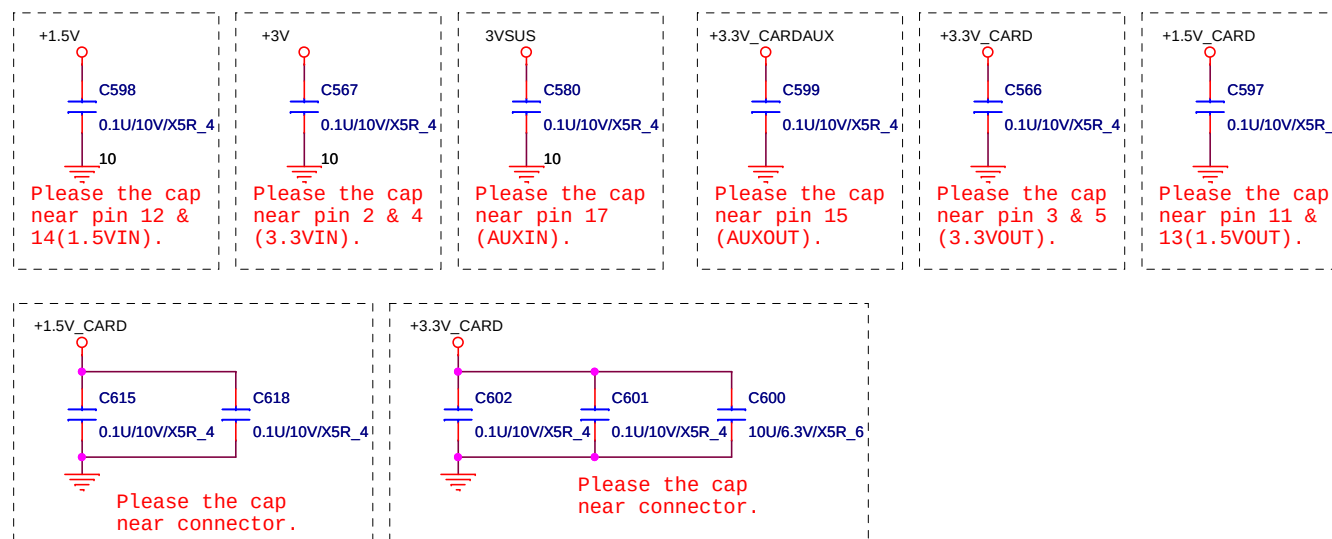
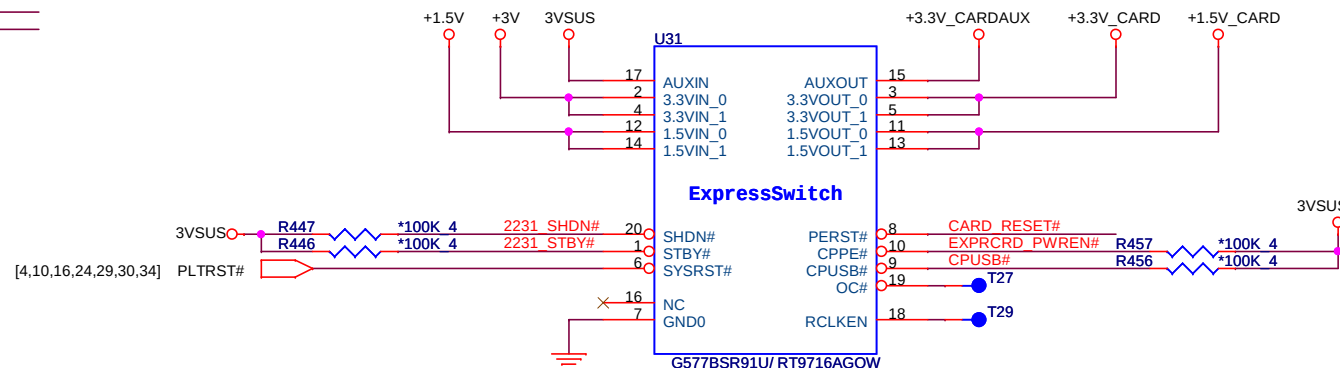
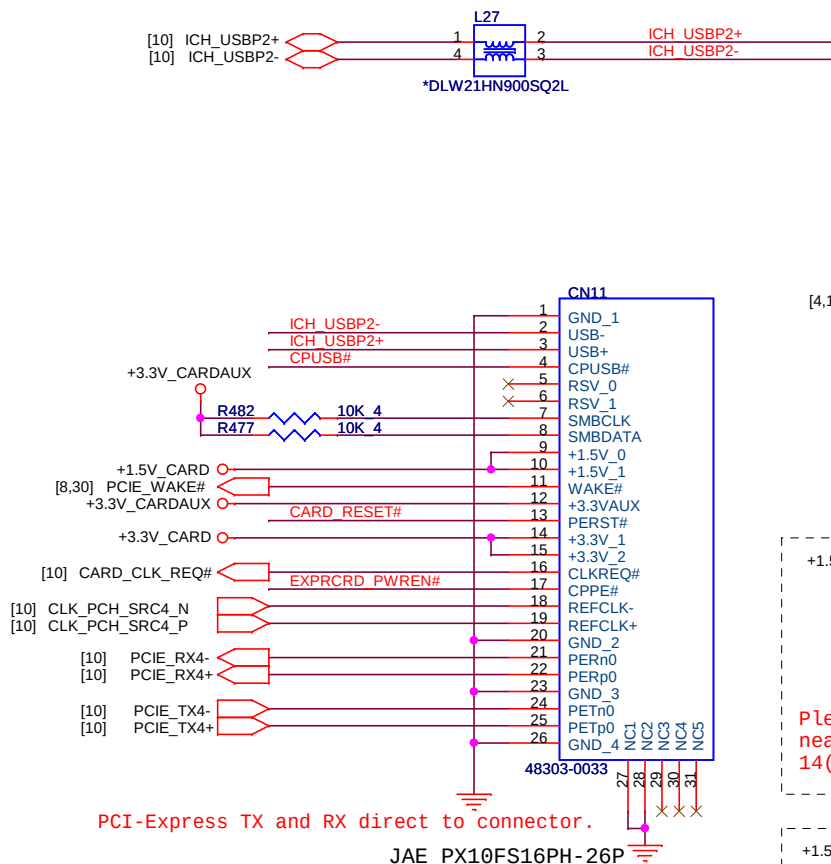
Size Custom Document Number MINI-Card (WLAN) Rev 1B

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Express Card

31

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA.

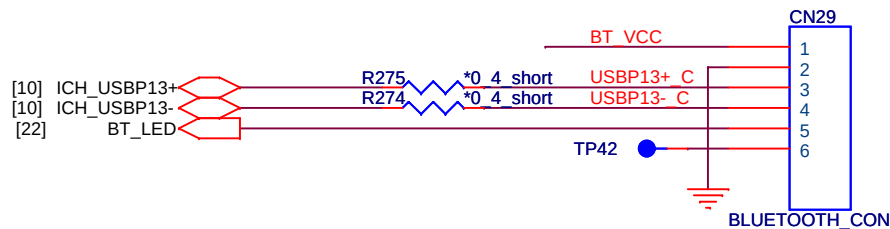


PROJECT : LL5A
Quanta Computer Inc.

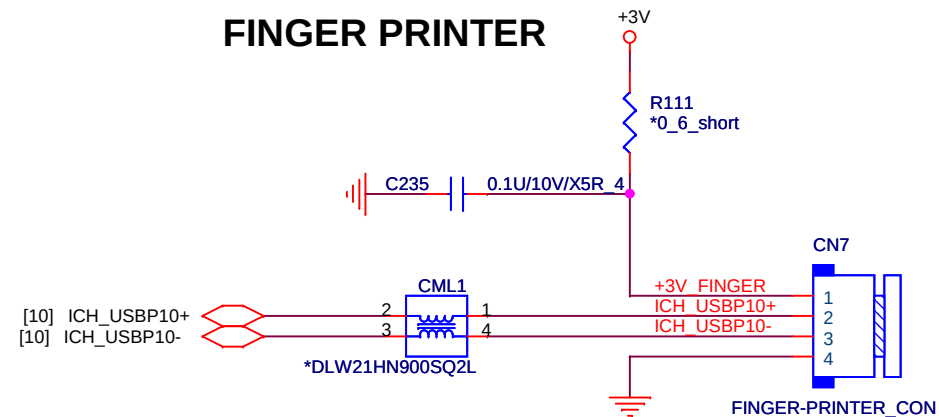
Size Custom	Document Number	Express Card	Rev 1B
Date:	Tuesday, October 20, 2009	Sheet 31 of 43	



BLUETOOTH



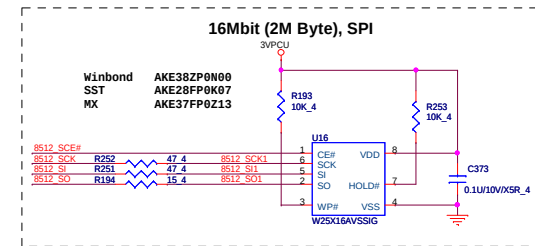
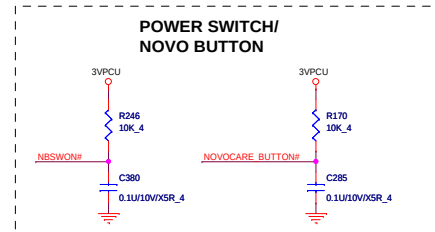
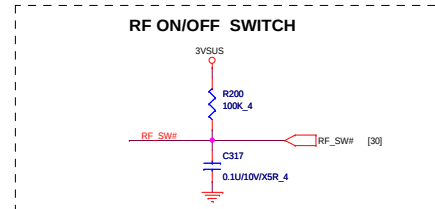
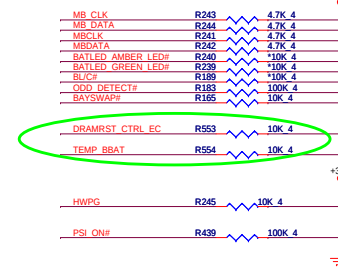
FINGER PRINTER



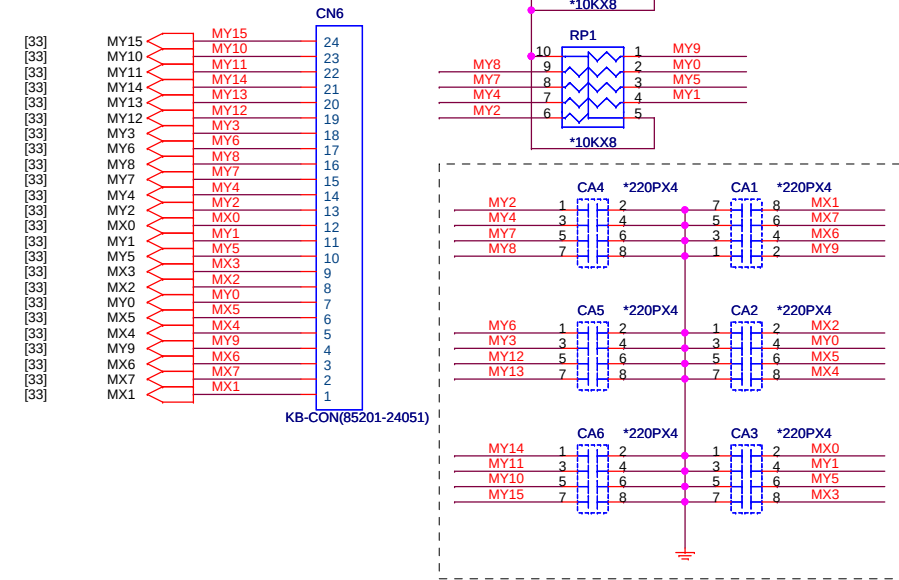
PROJECT : LL5A
Quanta Computer Inc.

Size Custom	Document Number	Rev 1B
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BT/FP

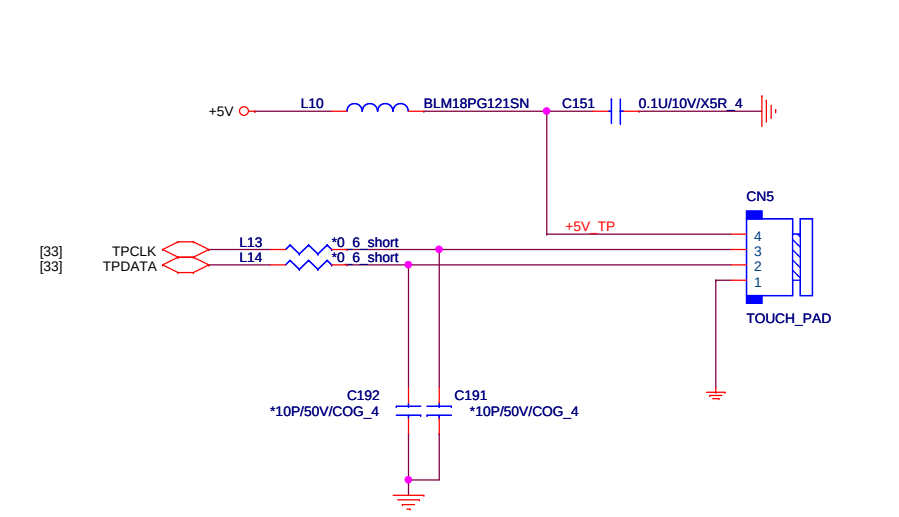


KEYBOARD

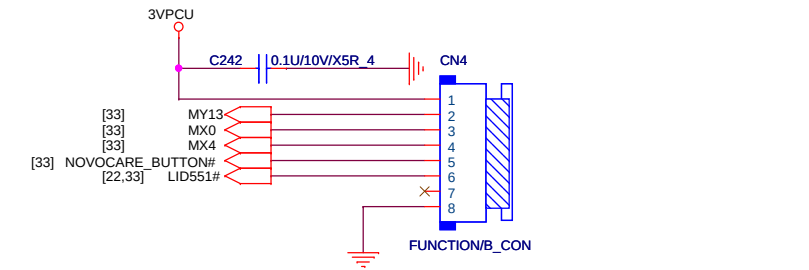


For EMI request

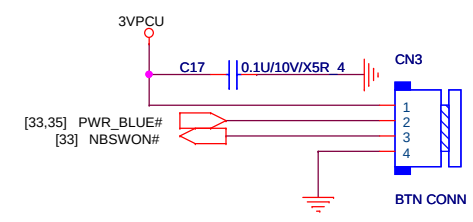
TOUCH PAD



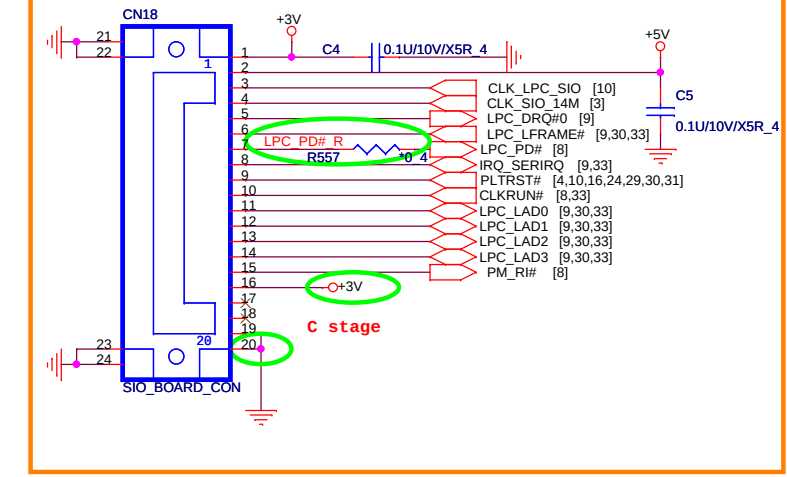
FUNCTION BUTTON BOARD



POWER BUTTON BOARD



SIO BOARD



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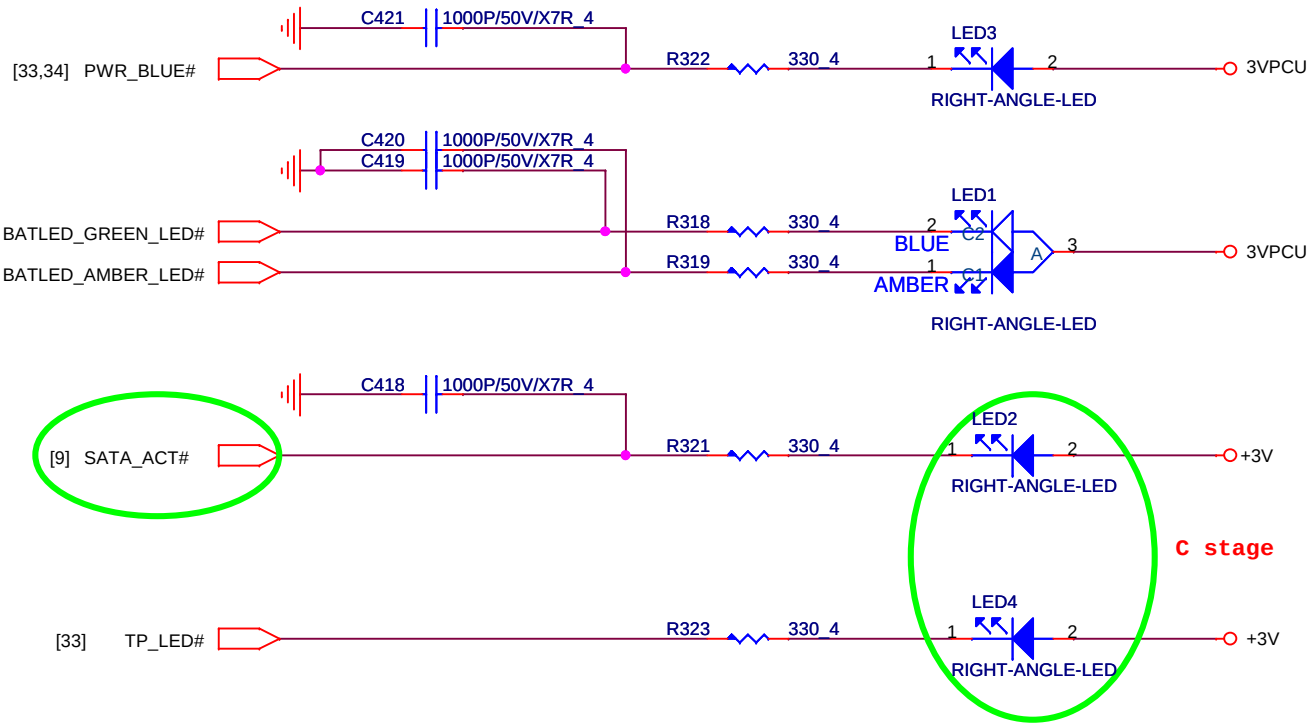
Size	Document Number	Rev
Custom	KB/TP/PW-B/FN-B	1B
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LED

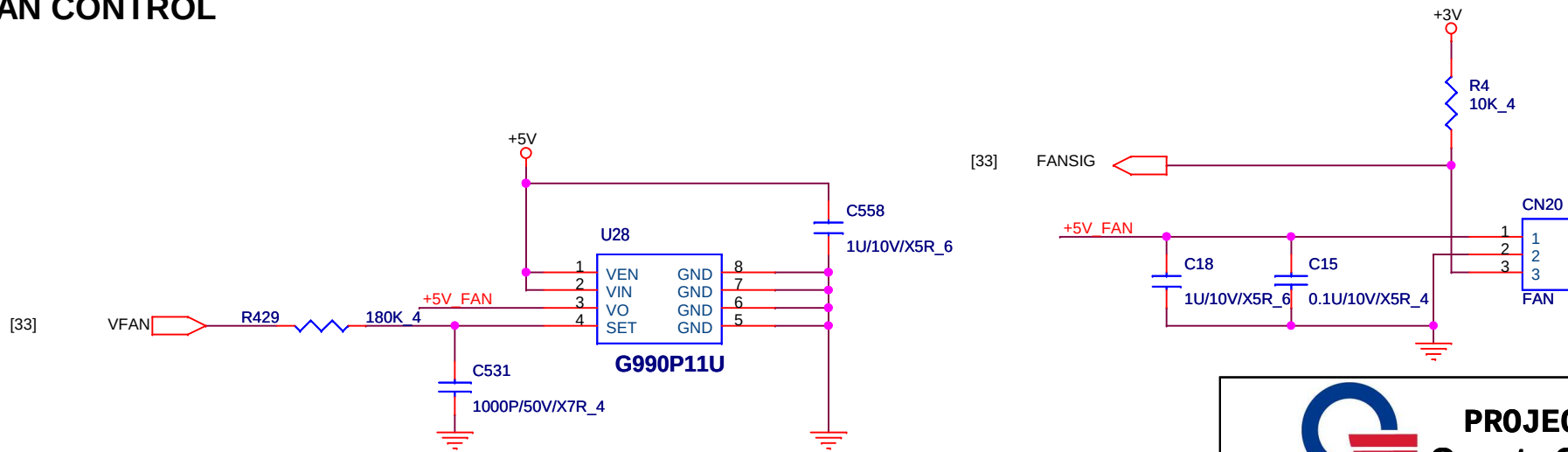
[3,4,6,8,9,10,11,12,14,15,16,18,19,22,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,42] +3V
[12,22,23,25,27,32,33,34,37,38] +5V



35



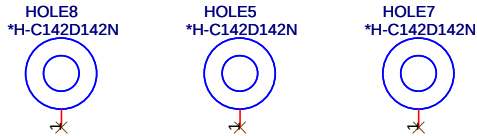
FAN CONTROL



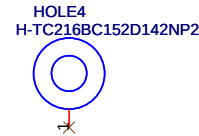
PROJECT : LL5A
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Size Custom	Document Number LED/FAN	Rev 1B
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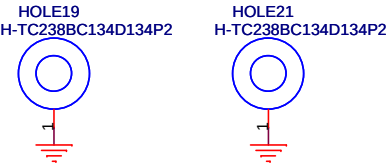
Hole for CPU support



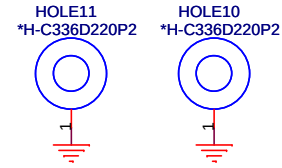
Hole for CPU Nut



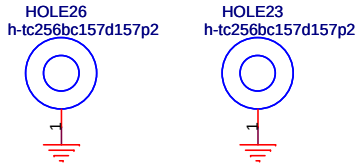
VGA nut



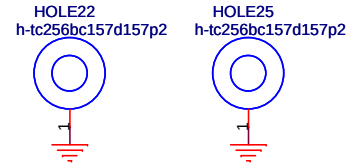
Drink Hole



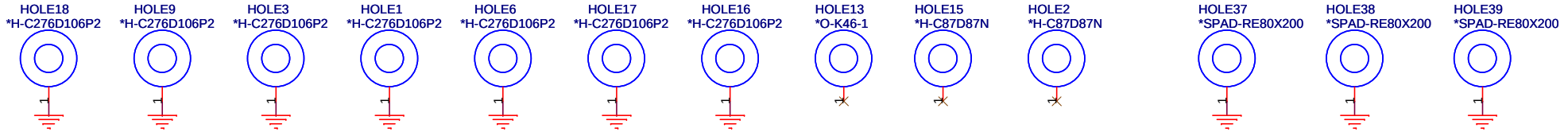
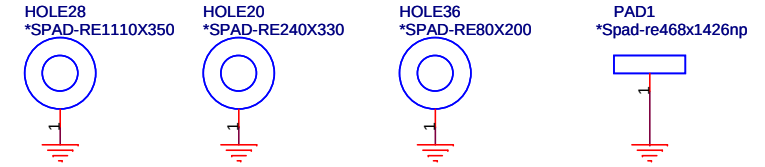
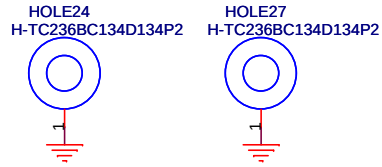
MINI CARD nut (WLAN)



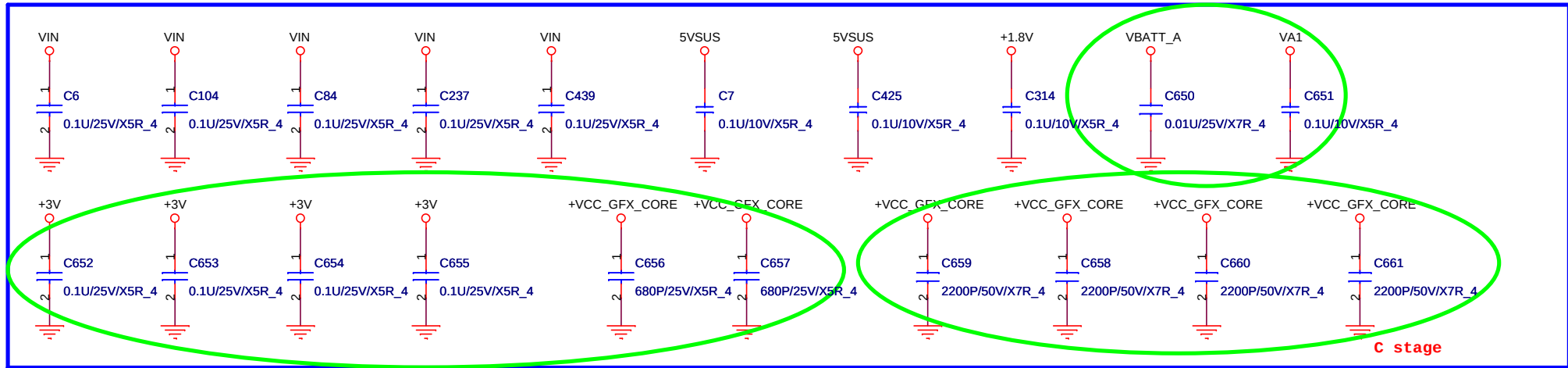
MINI CARD nut (WWAN)



Hole for PCH Thermal

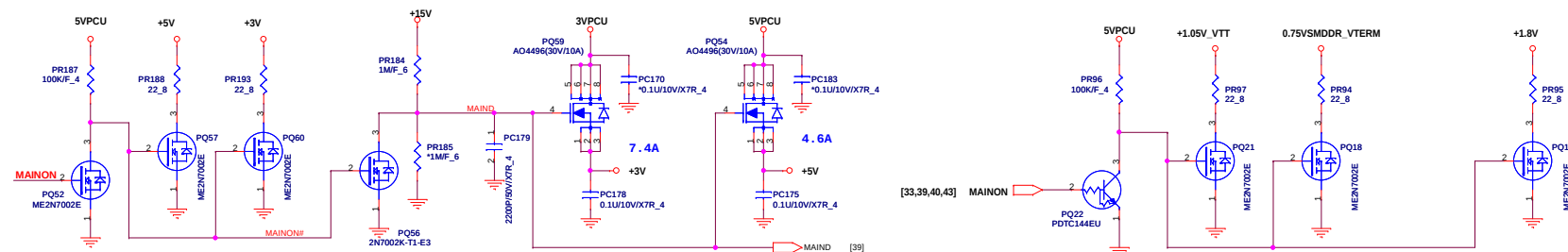


EMI Reserved

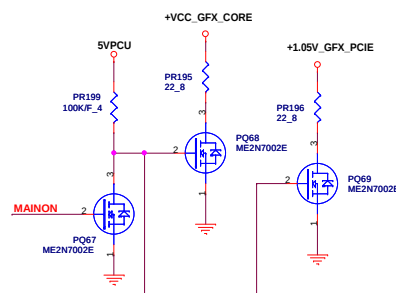
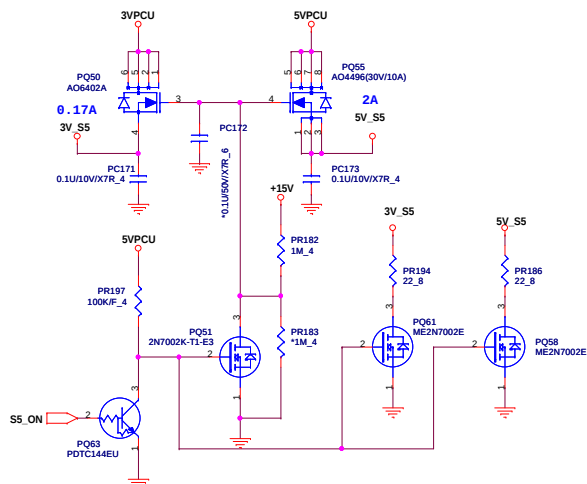


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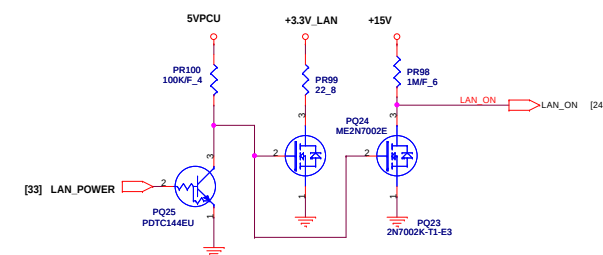
+3V, +5V



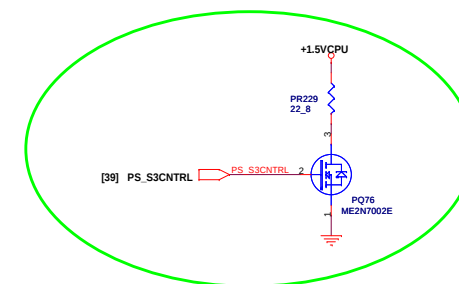
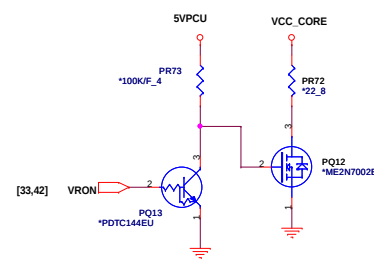
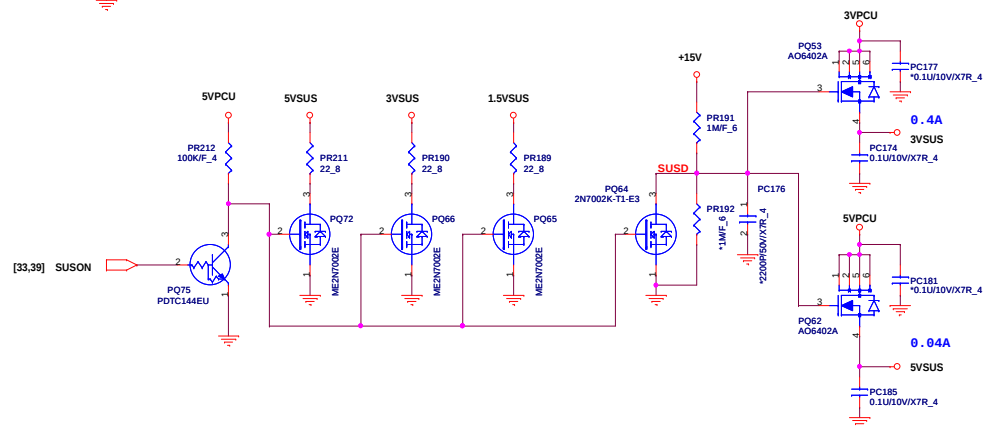
3V_S5, 5V_S5

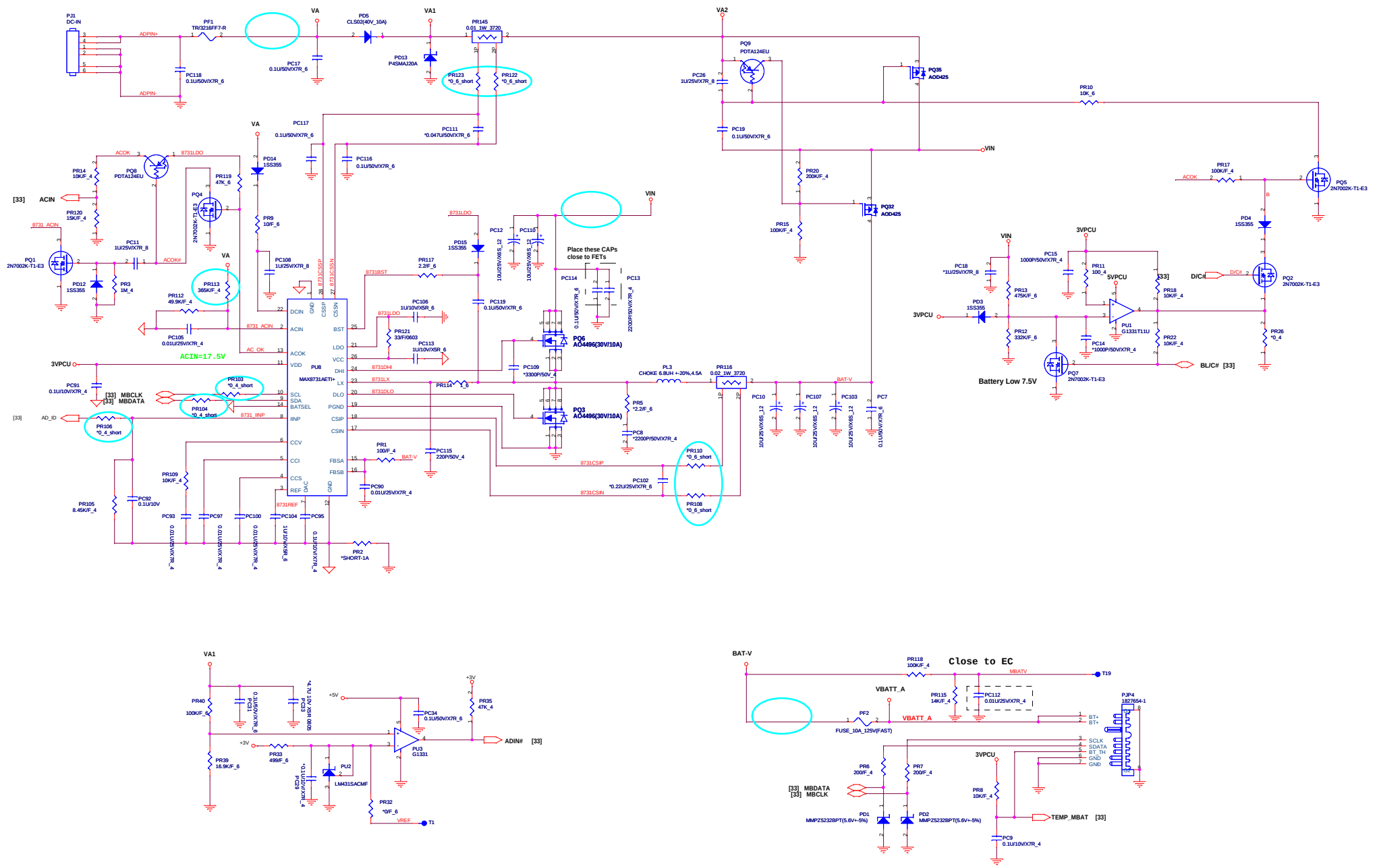


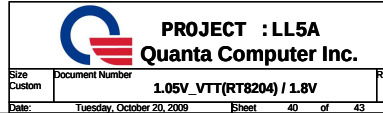
LANVCC

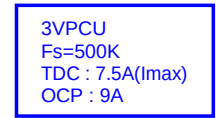


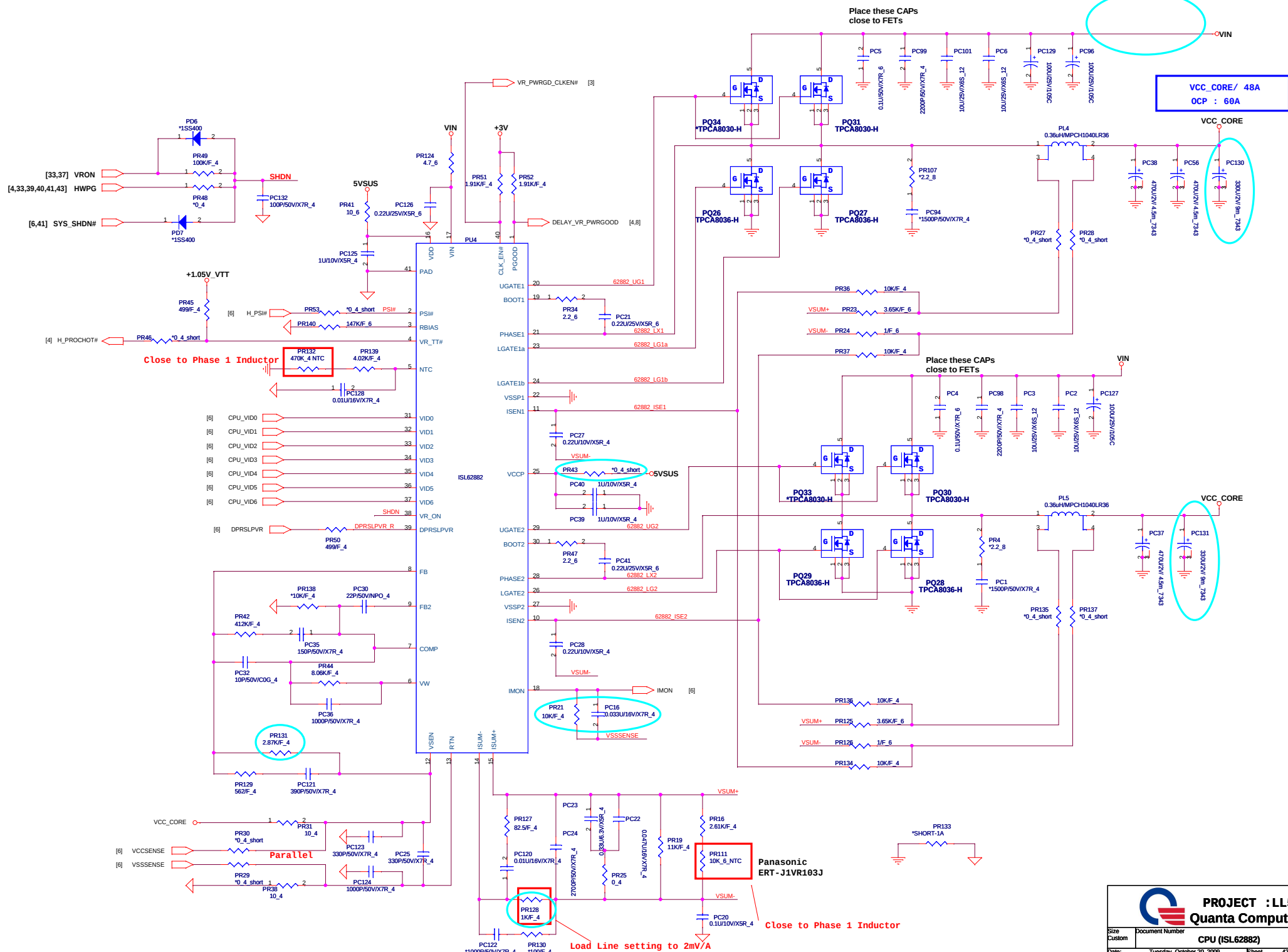
3VSUS, 5VSUS



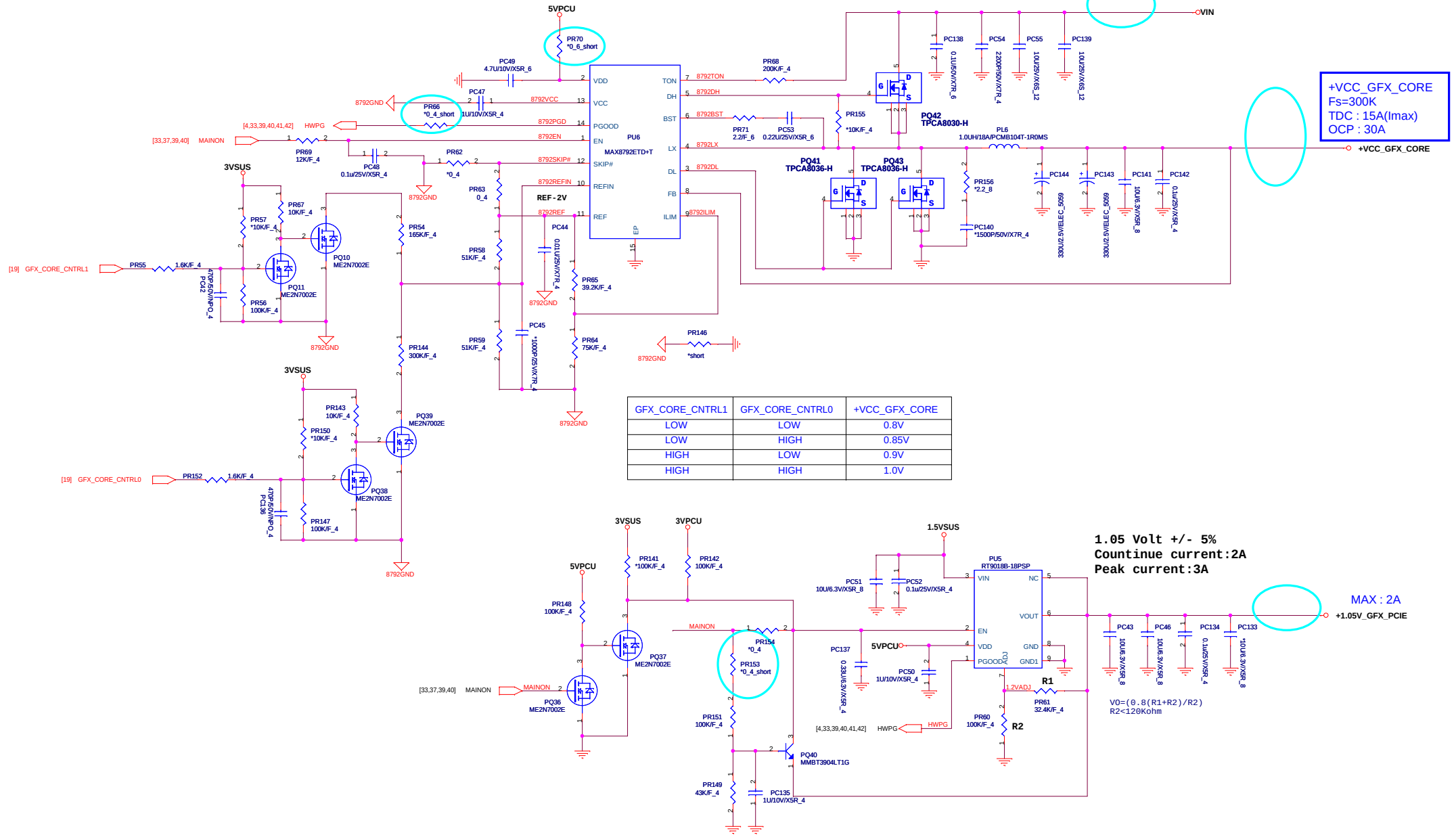








For Descrete N10M VGA Only



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