

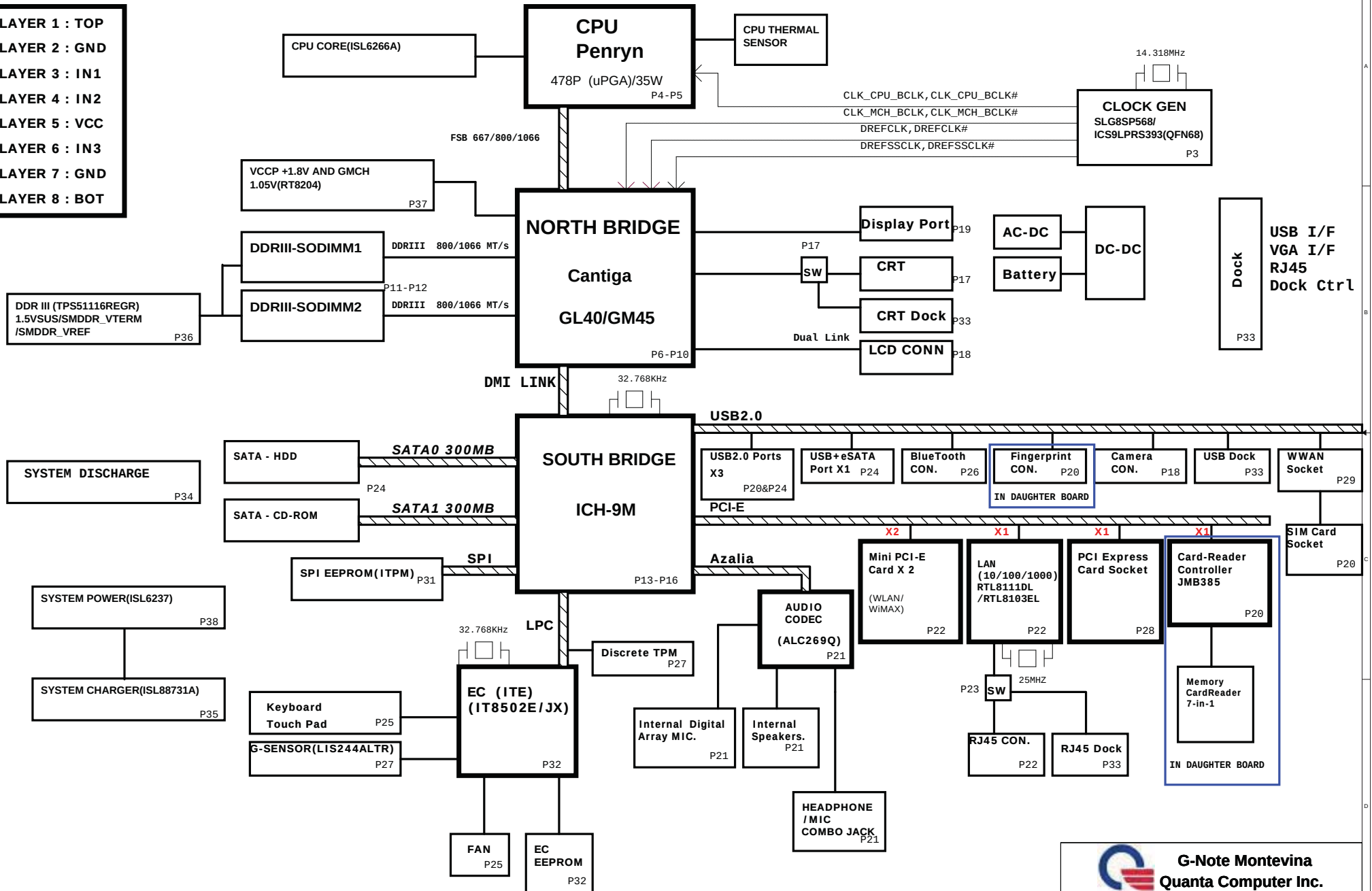
R410 Montevina Block Diagram

01

PCB STACK UP

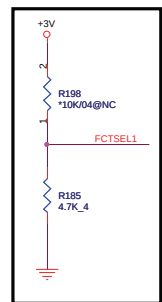
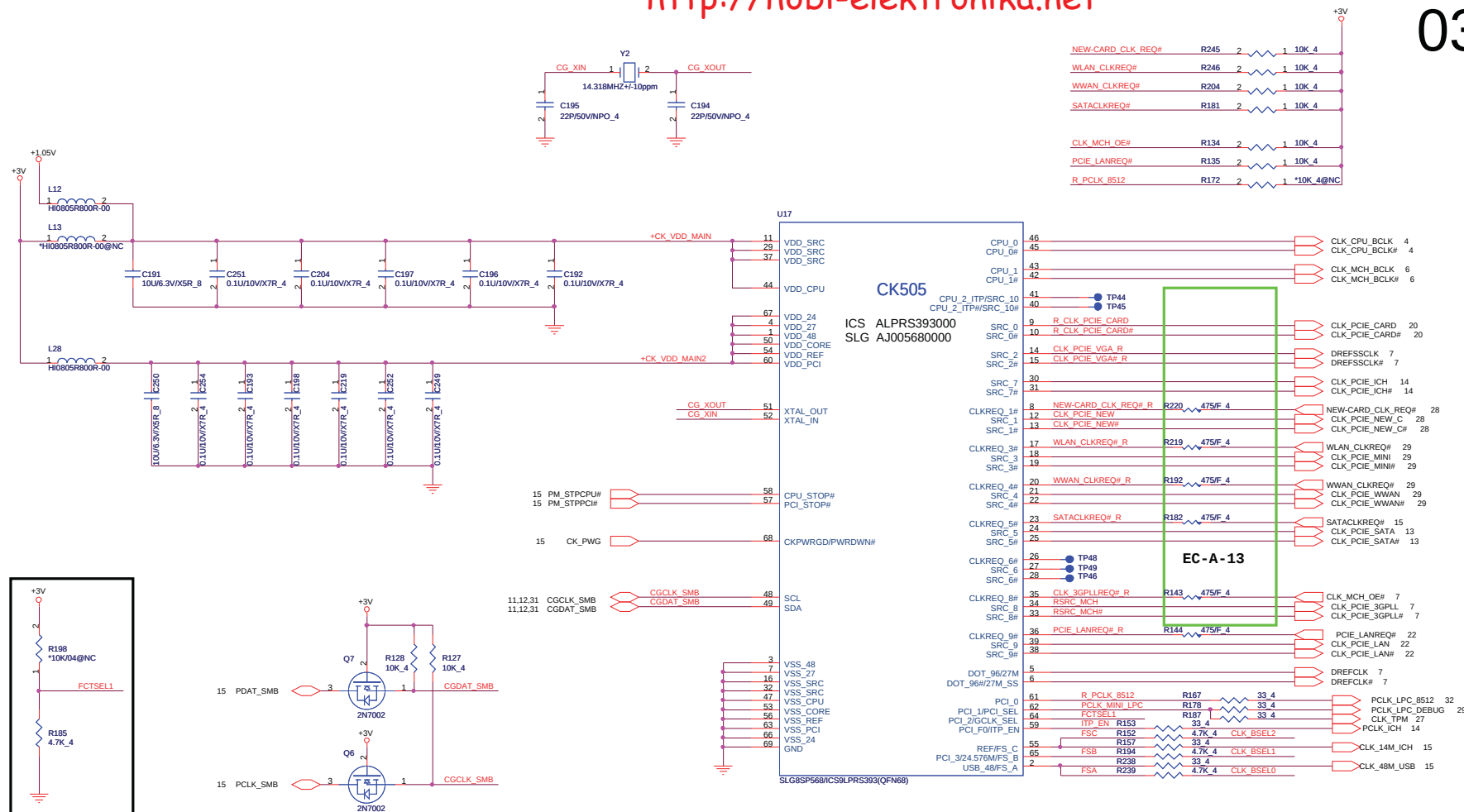
8L

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



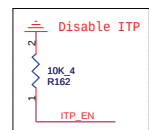
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+19V	18, 33, 34, 35, 36, 37, 38, 39	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	13, 16, 32	RTC		S0~S5
3VPCU	+3.3V	13, 18, 22, 24, 30, 32, 33, 34, 36, 37	8051 POWER		S0~S5
5VPCU	+5V	30, 33, 34, 35, 36, 37, 38	LCD/CHARGE POWER		S0~S5
+15V	+15V	18, 26, 33, 37	LARGE POWER	5VPCU	S0~S5
LANVCC	+3.3V	22, 33	LAN POWER	LAN_ON	
5VSUS	+5V	18, 30, 33, 38	SLP_S5# CTRLD POWER	SUSON	
3VSUS	+3.3V	14, 15, 27, 28, 29, 32, 33, 38	SLP_S5# CTRLD POWER	SUSON	
1.8VSUS	+1.8V	10, 33, 36		SUSON	
1.5VSUS	+1.5V	07, 09, 10, 11, 12, 33, 35	SODIMM POWER CALISTOGA/ICH8 POWER	SUSON	
SMDDR_VREF_DIMM	+0.75V	11, 12	SODIMM POWER		
+5V	+5V	16, 17, 18, 19, 21, 23, 24, 25, 32, 33, 34	SLP_S3# CTRLD POWER	MAINON	
+3V	+3.3V	03, 05, 07, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38	SLP_S3# CTRLD POWER	MAINON	
+1.5V	+1.5V	05, 10, 13, 14, 15, 16, 21, 27, 28, 29, 35	CALISTOGA/ICH8 POWER	MAINON	
+1.05V	+1.05V	03, 04, 05, 06, 07, 09, 10, 13, 16, 33, 36, 38	CPU/CALISTOGA/ICH8 POWER	MAINON	
VCC_CORE	+0.7V~+1.77V	04, 05, 33, 38	CPU CORE POWER	VRON	
LCDVCC	+3.3V	18	LCD Power	NT_DISP_ON	
+5VHDD	+5V	23	HDD Power	MAINON	
MBATV	+10V~+17V	32, 34	MAIN BATTERY	D/C#	

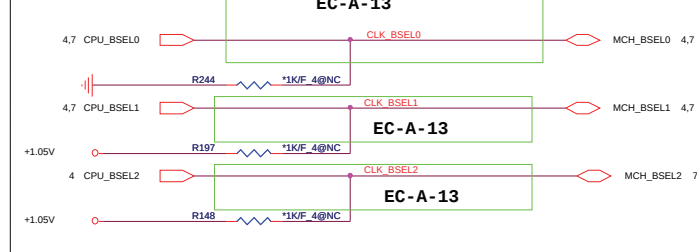


CGCLK_SEL = FCTSEL1

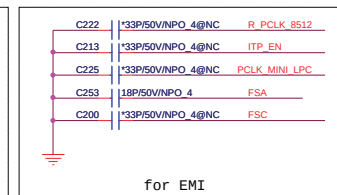
FCTSEL1 (PIN64)	PIN5	PIN6
0	DOT96	DOT96#
1	27Mout-NSS	27Mout-SS



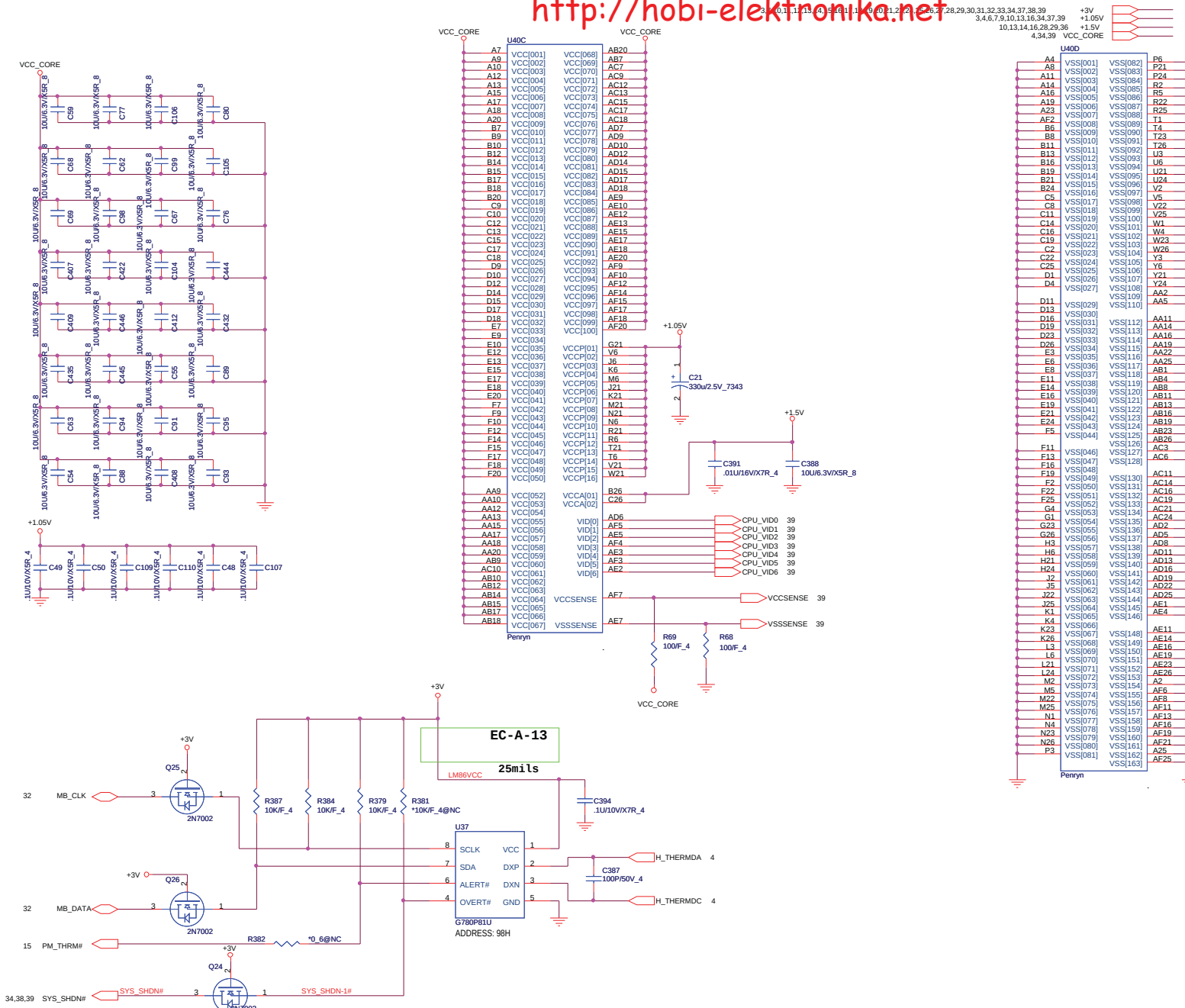
CPU Clock select



FSC	FSB	FSA	CPU	SRC	PCI
0	0	0	266.6	100	33
0	0	1	133.3	100	33
0	1	0	200.0	100	33
0	1	1	166.6	100	33
1	0	0	Reserved		
1	0	1	Reserved		
1	1	0	Reserved		
1	1	1	Reserved		





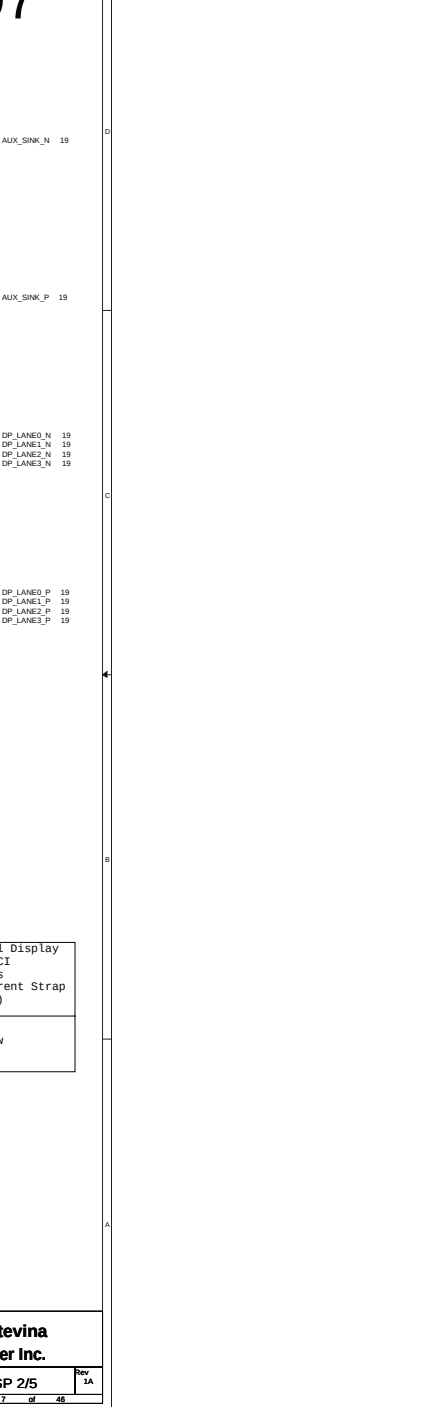
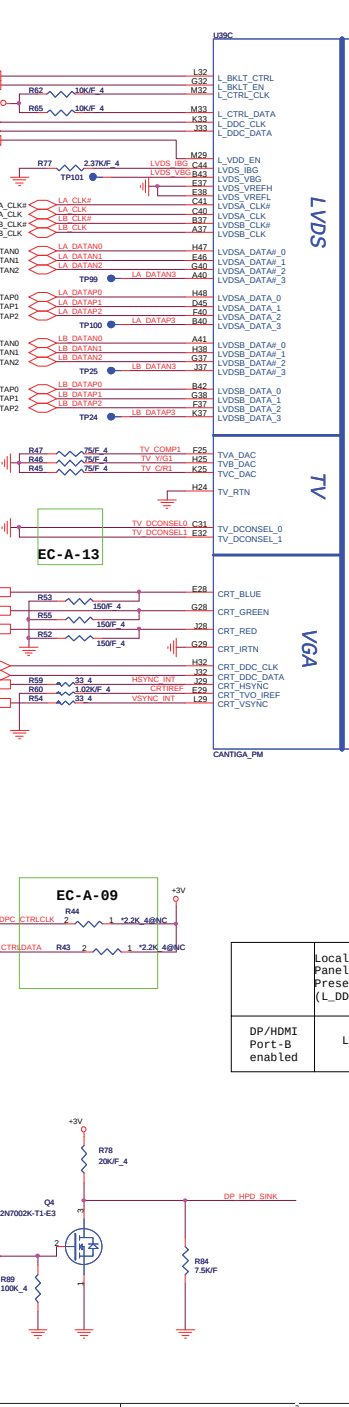
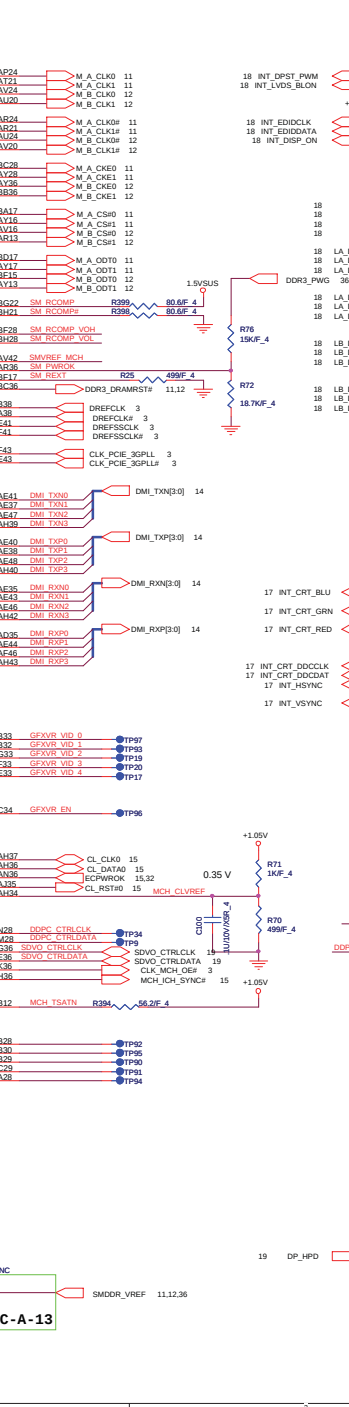
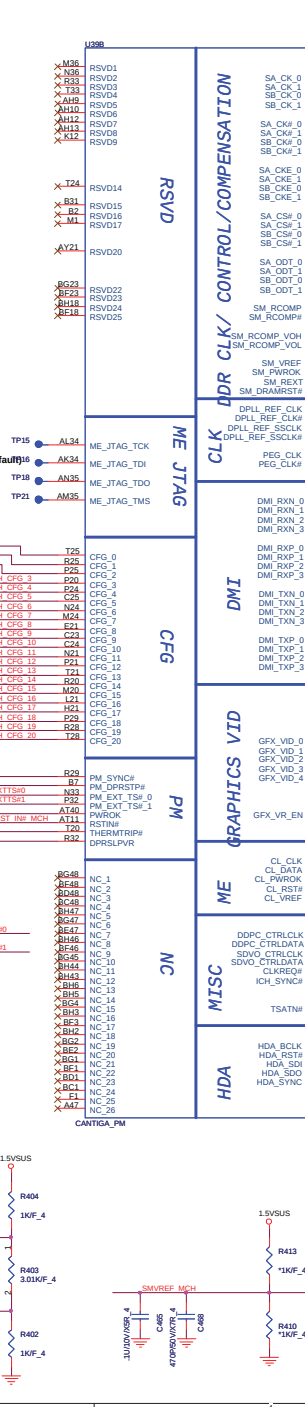
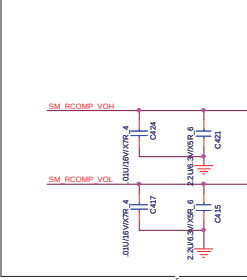
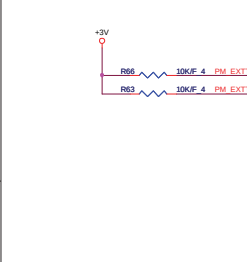
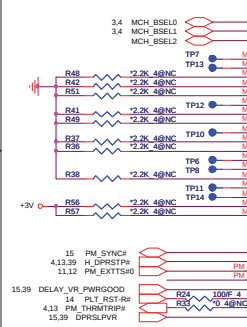




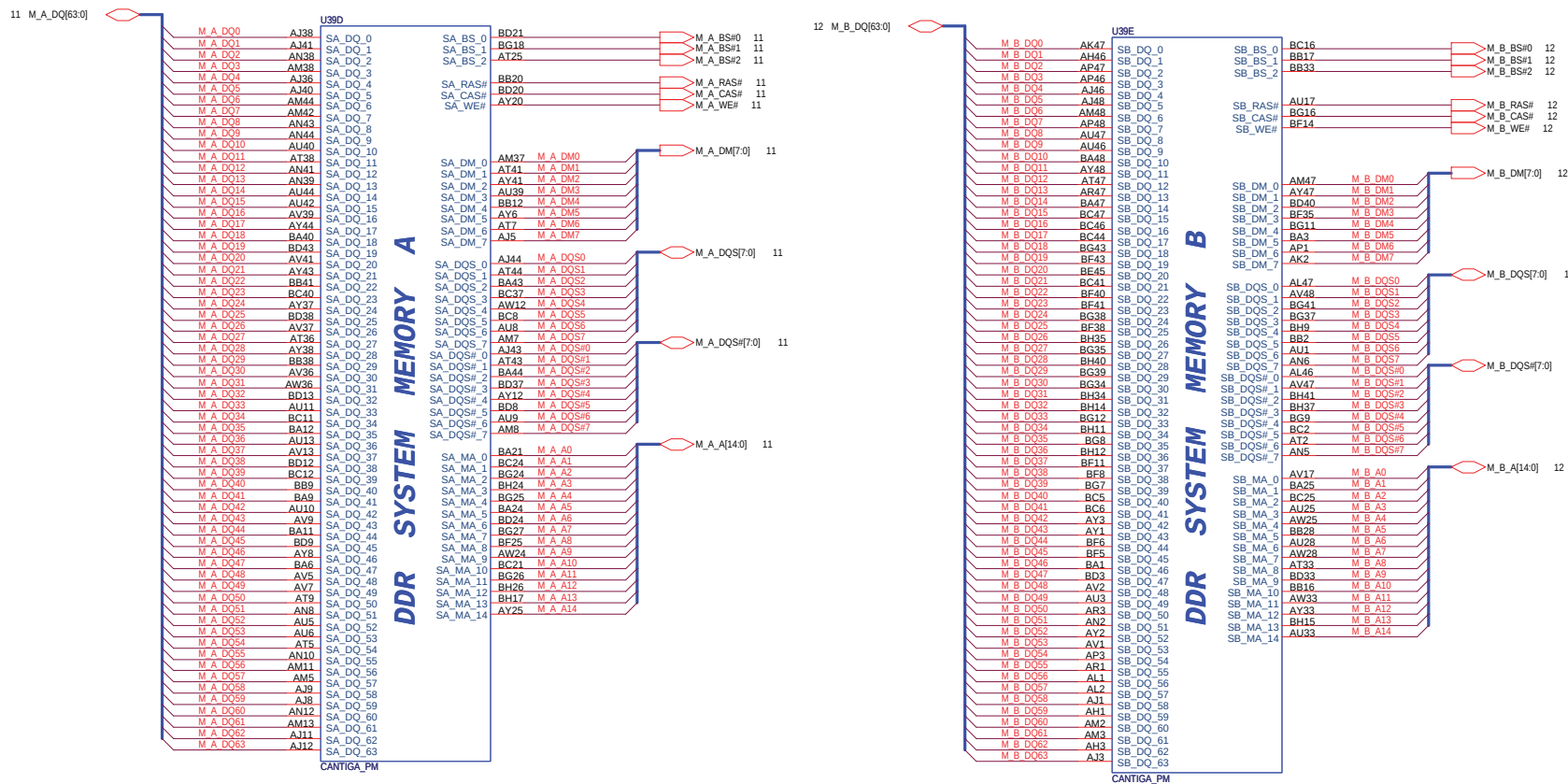
Date: Thursday, September 03, 2009 Sheet 6 of 46

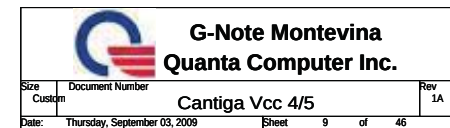
MCH_CFG_5 DMi2 selection
Low: DMi2
High: DMi4 (Default)
MCH_CFG_16 FSB Dynamic ODT
Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)
MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation (Default)
MCH_CFG_19 DMI Lane Reversal
Low: Normal (Default)
High: Lane Reserved
MCH_CFG_6 iTPM Host Interface
Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)
MCH_CFG_7 Intel(R) Management Engine Crypto
Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_10 PCIe Lookback Enable
Low: Enabled
High: Disabled (Default)
MCH_CFG_1213 XOR/ALL2/CLOCK Un-gating
MCH_CFG_13 MCH_CFG_12 Configuration

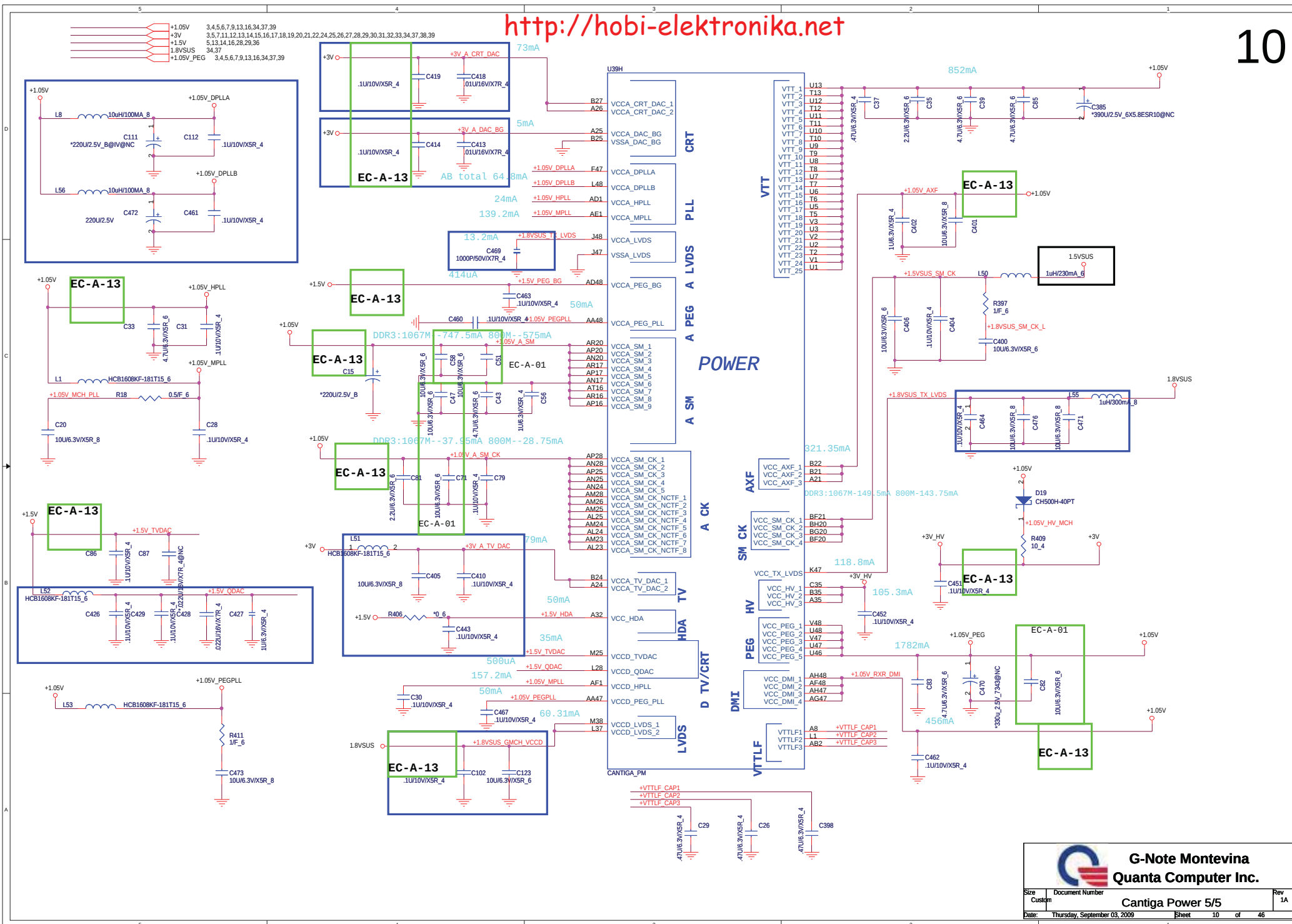
0 0 Reserved
0 0 XOR Mode enabled
0 1 All-Z Mode enabled
1 1 Normal operation (Default)

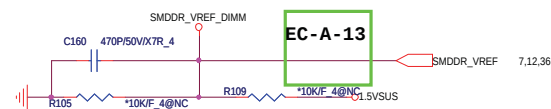
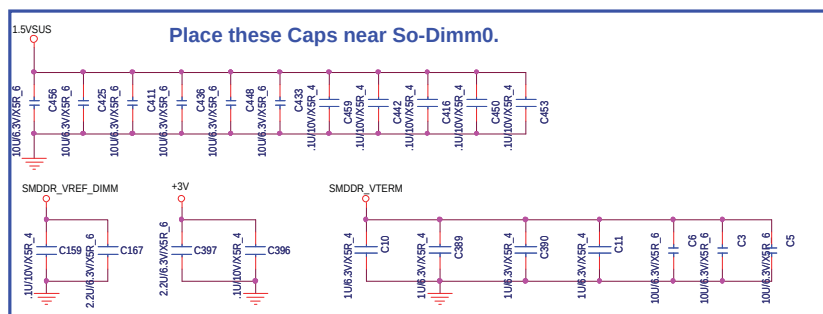


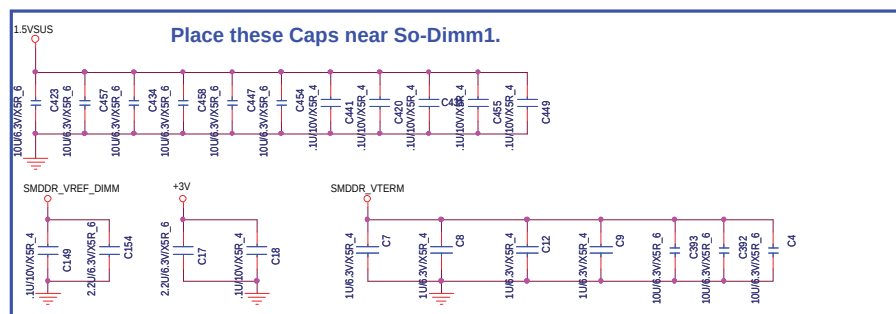
	Local Flat Panel (LFP) Present Strap (L_DDCC_DATA)	DP/HDMI Present Strap (DDPC_CTRLDATA)	SDVO Present Strap (SDVO_CTRLDATA)	Digital Display Port/PCI Express Content Strap (CF626)
DP/HDMI Port-B enabled	Low	Low	High	Low

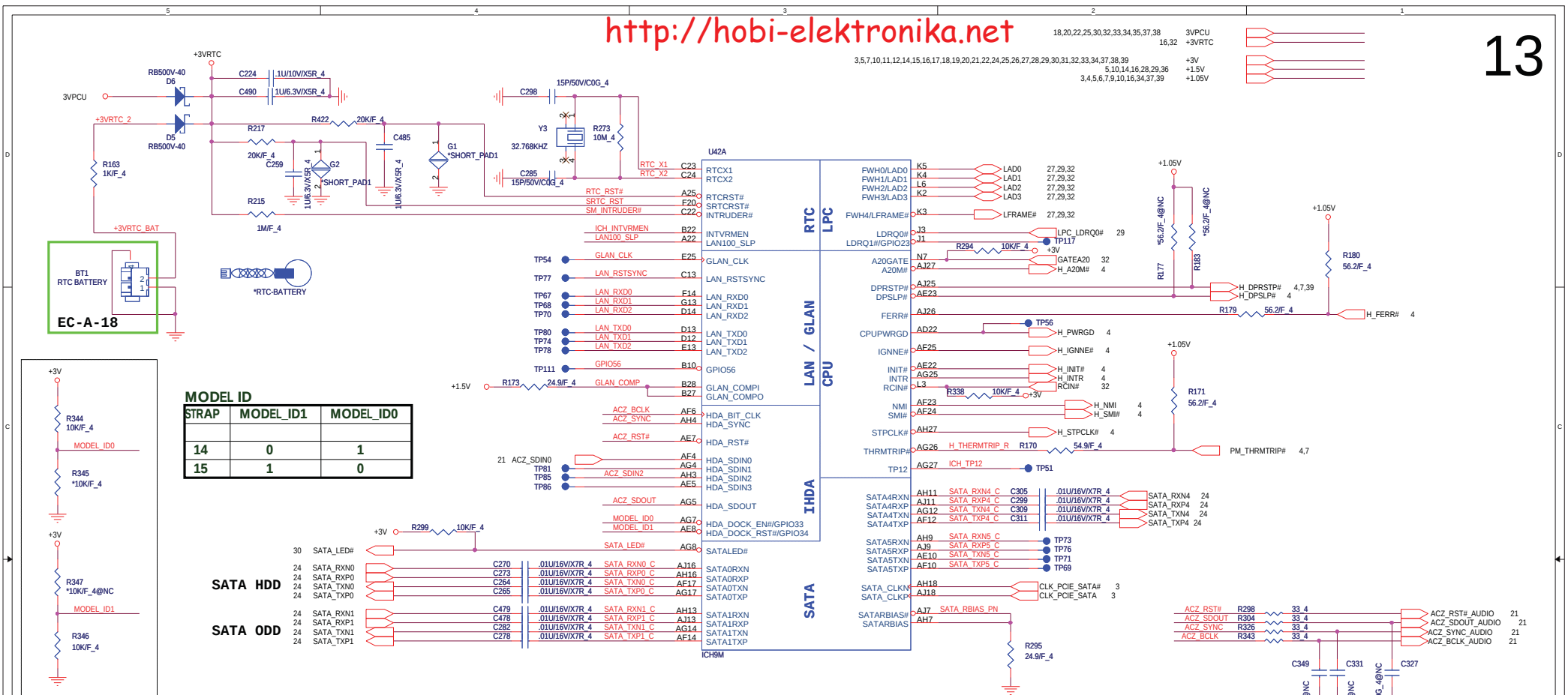












SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for Vccsus1_05, Vccsus1_5 and VccCL1_5)

ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

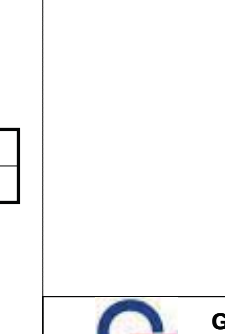
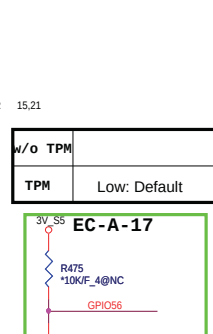
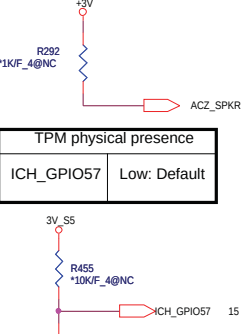
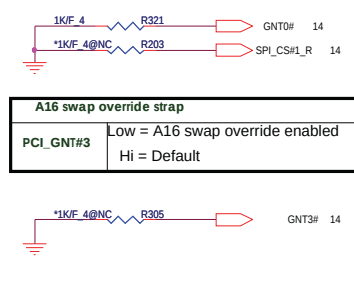
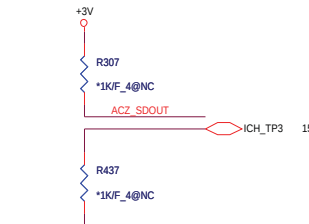
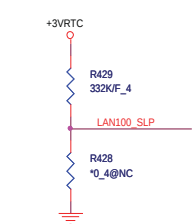
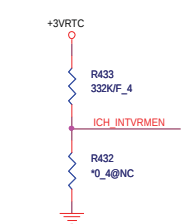
STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

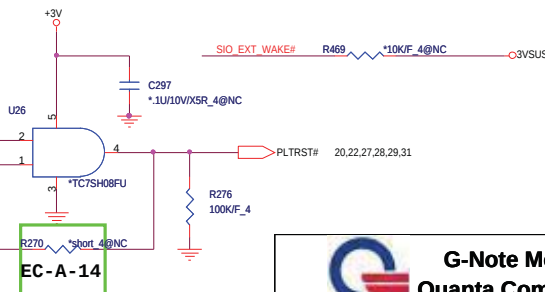
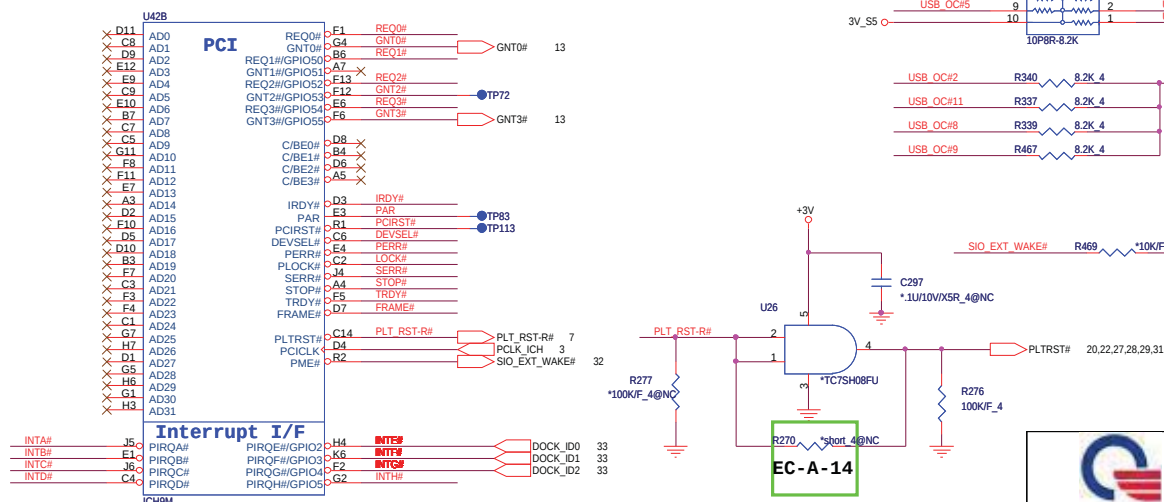
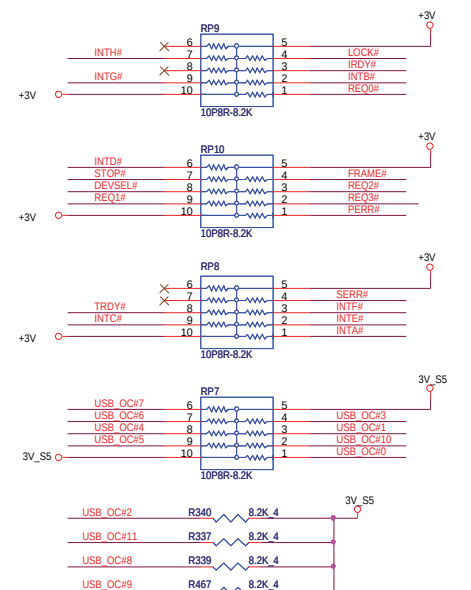
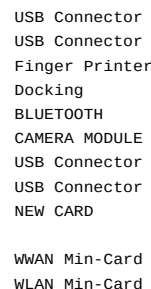
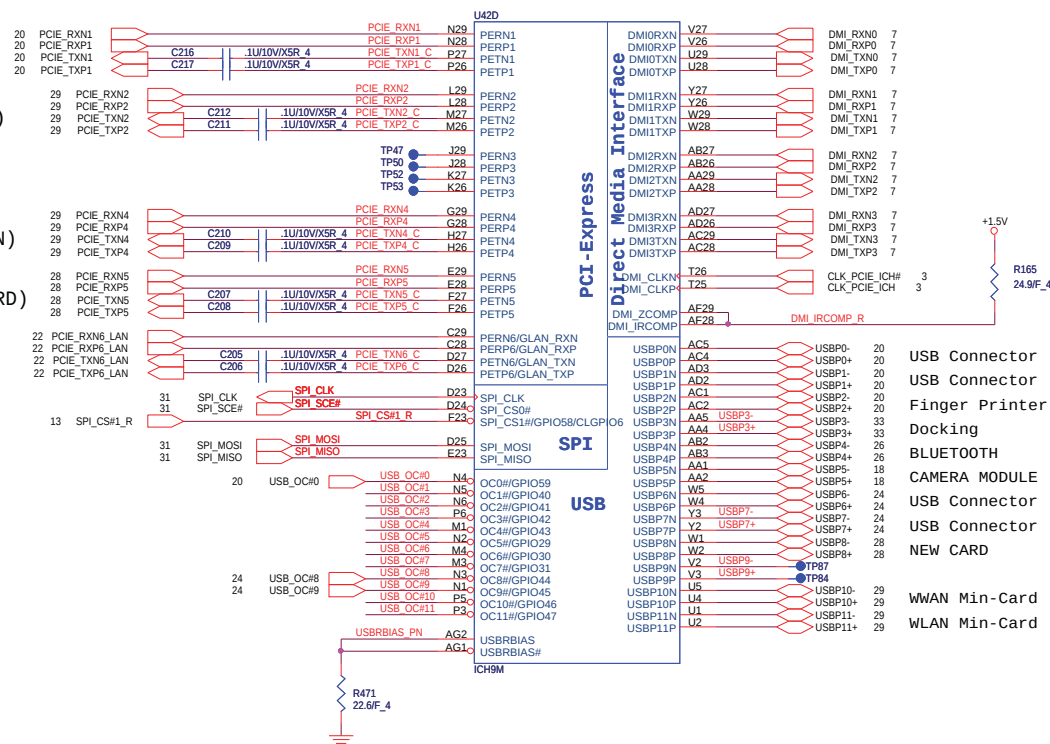
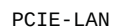
No Reboot Strap
ACZ_SPKR
Low: Default
Hi: No reboot

A16 swap override strap
PCI_GNT#3
Low = A16 swap override enabled
Hi = Default

TPM physical presence
ICH_GPIO57
Low: Default

w/o TPM
TPM
Low: Default



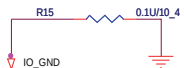




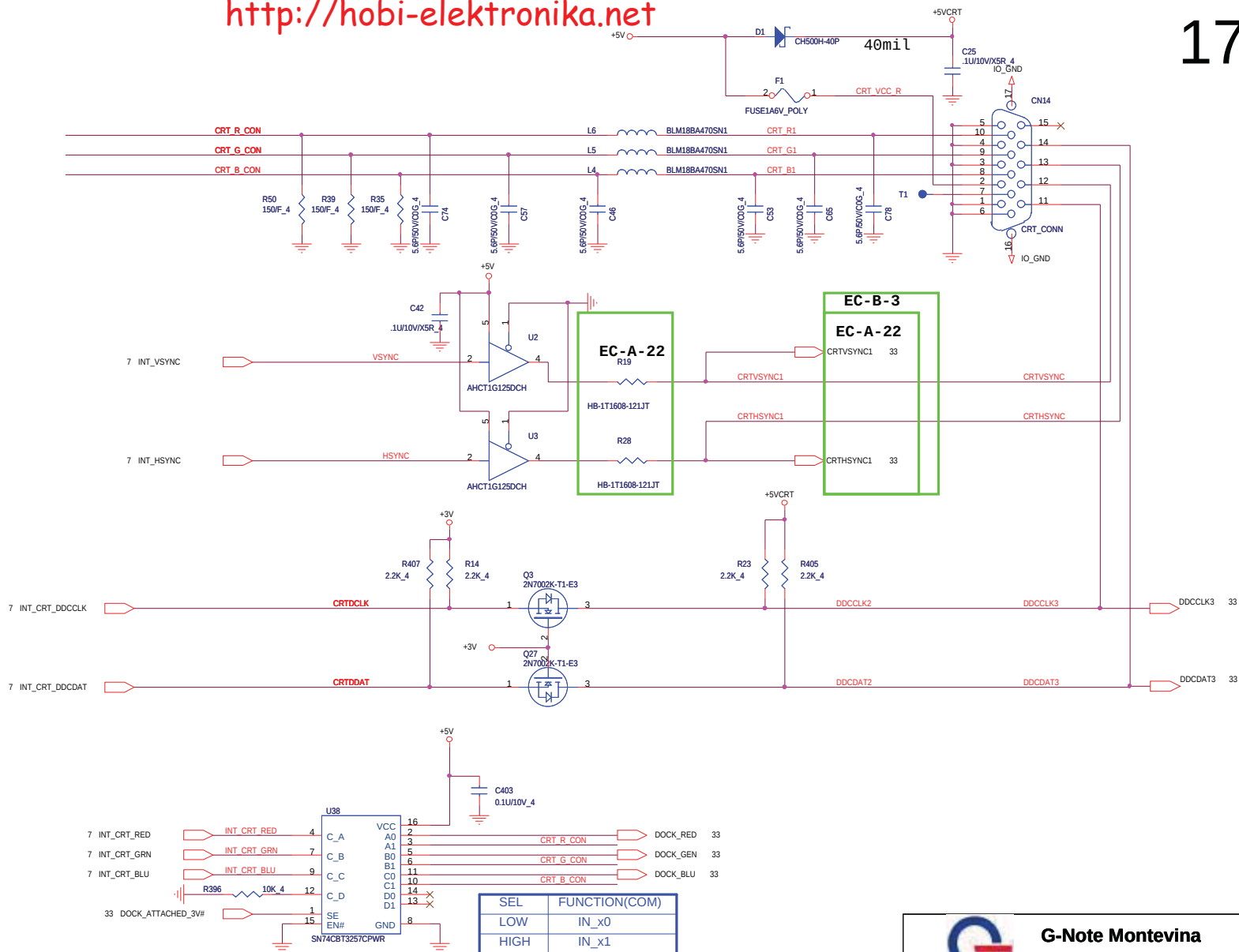
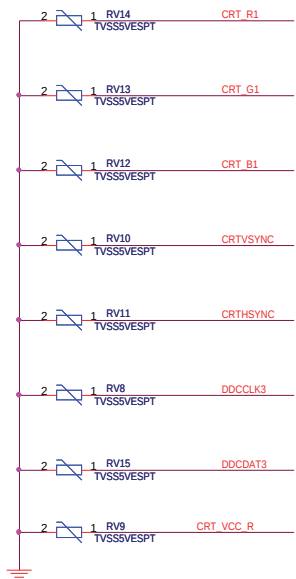


CRT PORT

EMI



ESD PROTECTION close CRT connector



SEL	FUNCTION(COM)
LOW	IN_x0
HIGH	IN_x1

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Quanta Computer Inc.

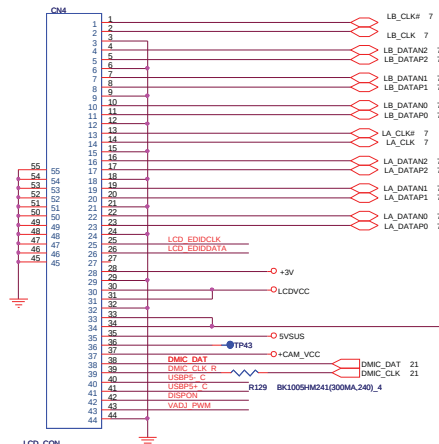
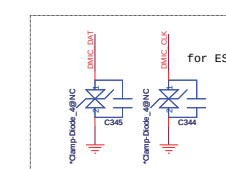
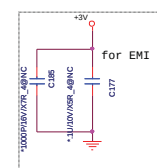
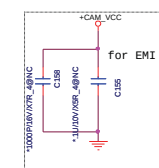
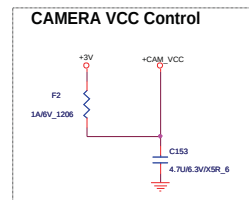
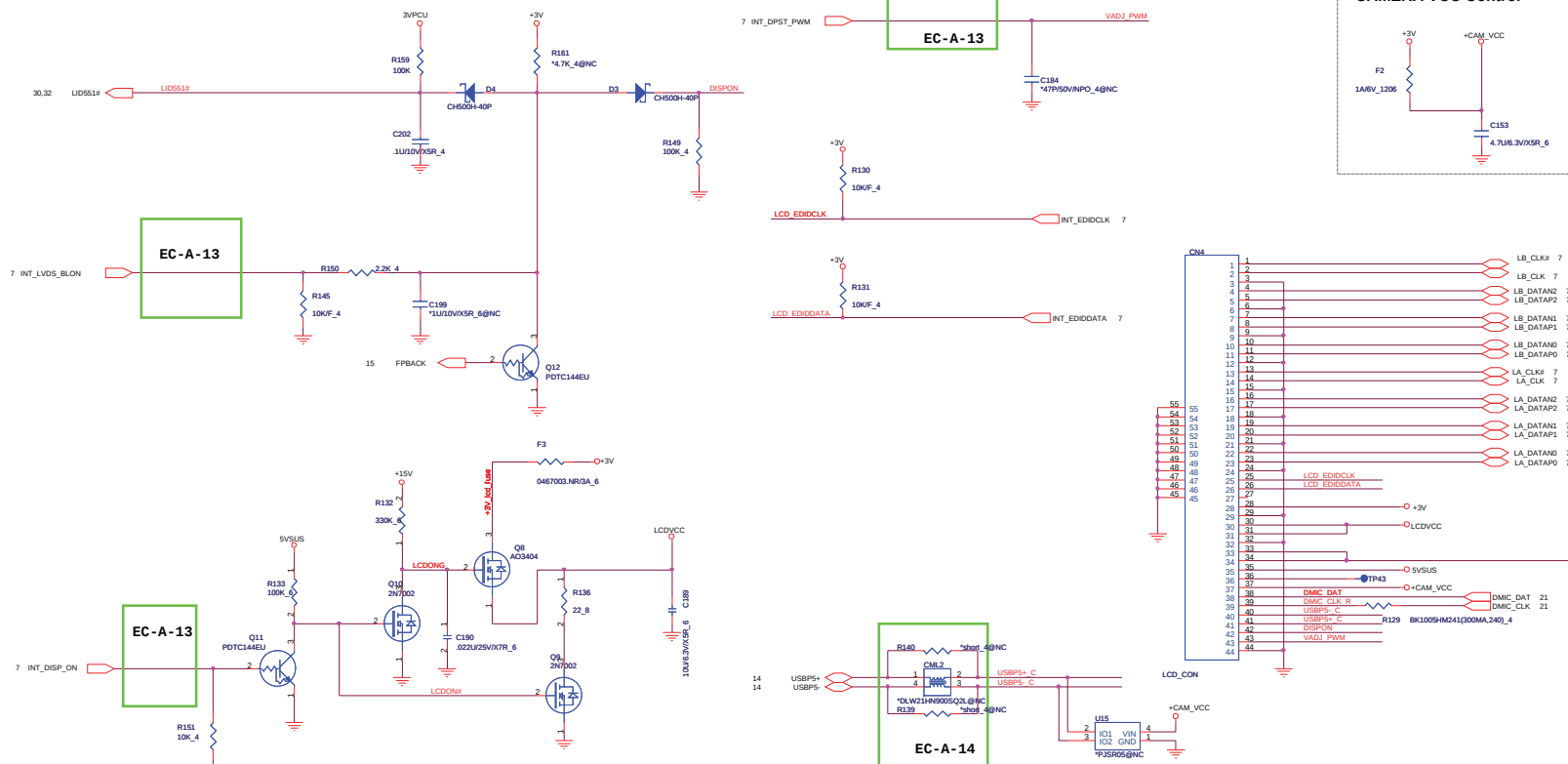
Size: Custom

Document Number: **CRT CON**

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Rev: 1A



EMI:trace DMIC_CLK should reference with GND



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Custom	LCD/LID/CCD CON	1A
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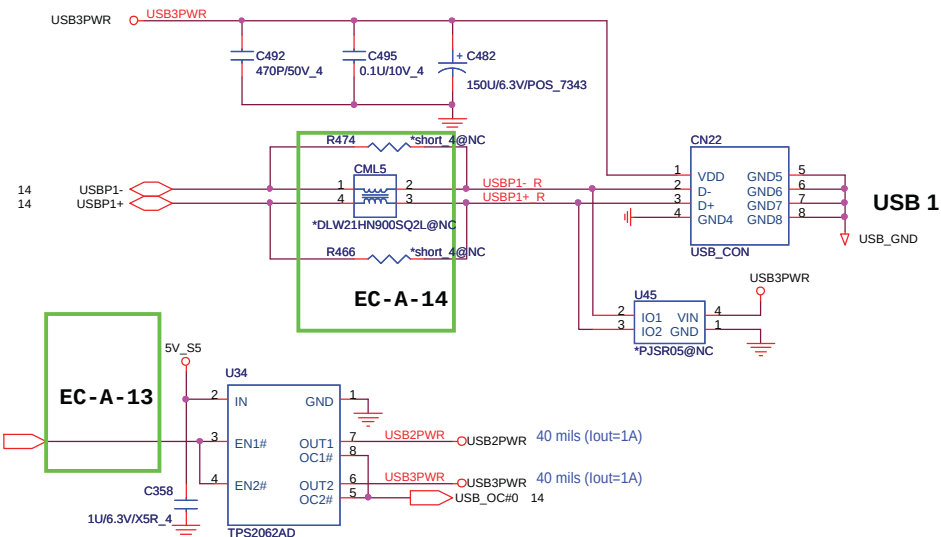
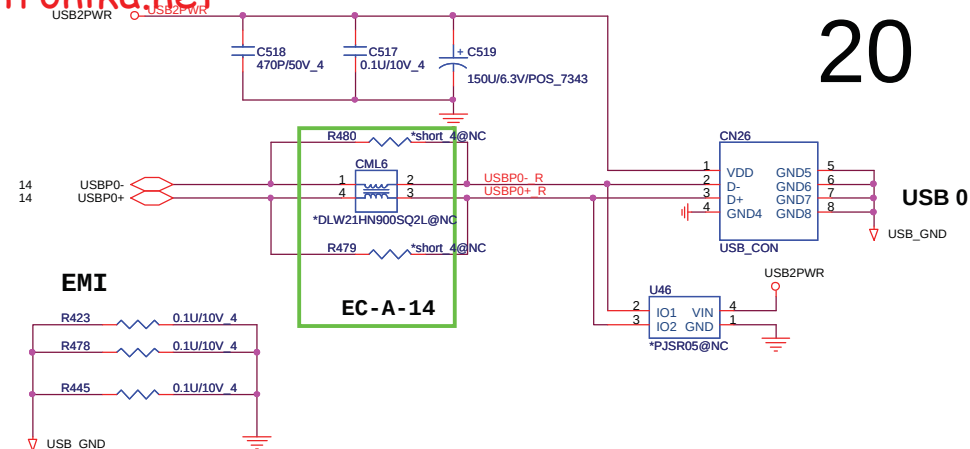
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32 BATLED_GREEN R366 221/F 4 2 LED2 GREEN C2 1 3 3VPCU **Battery**

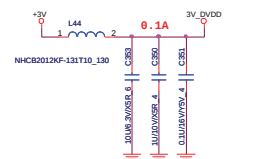
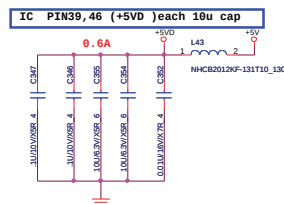
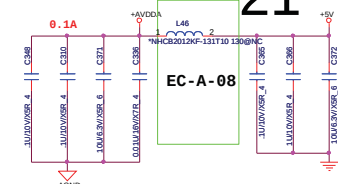
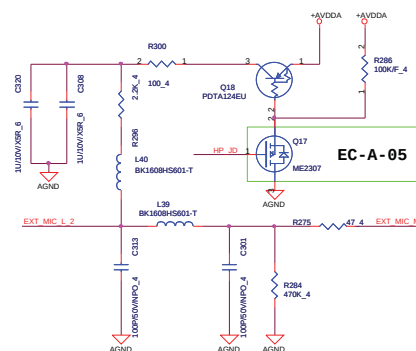
32 BATLED_AMBER R368 221/F 4 1 AMBER C2 2 3 3VPCU

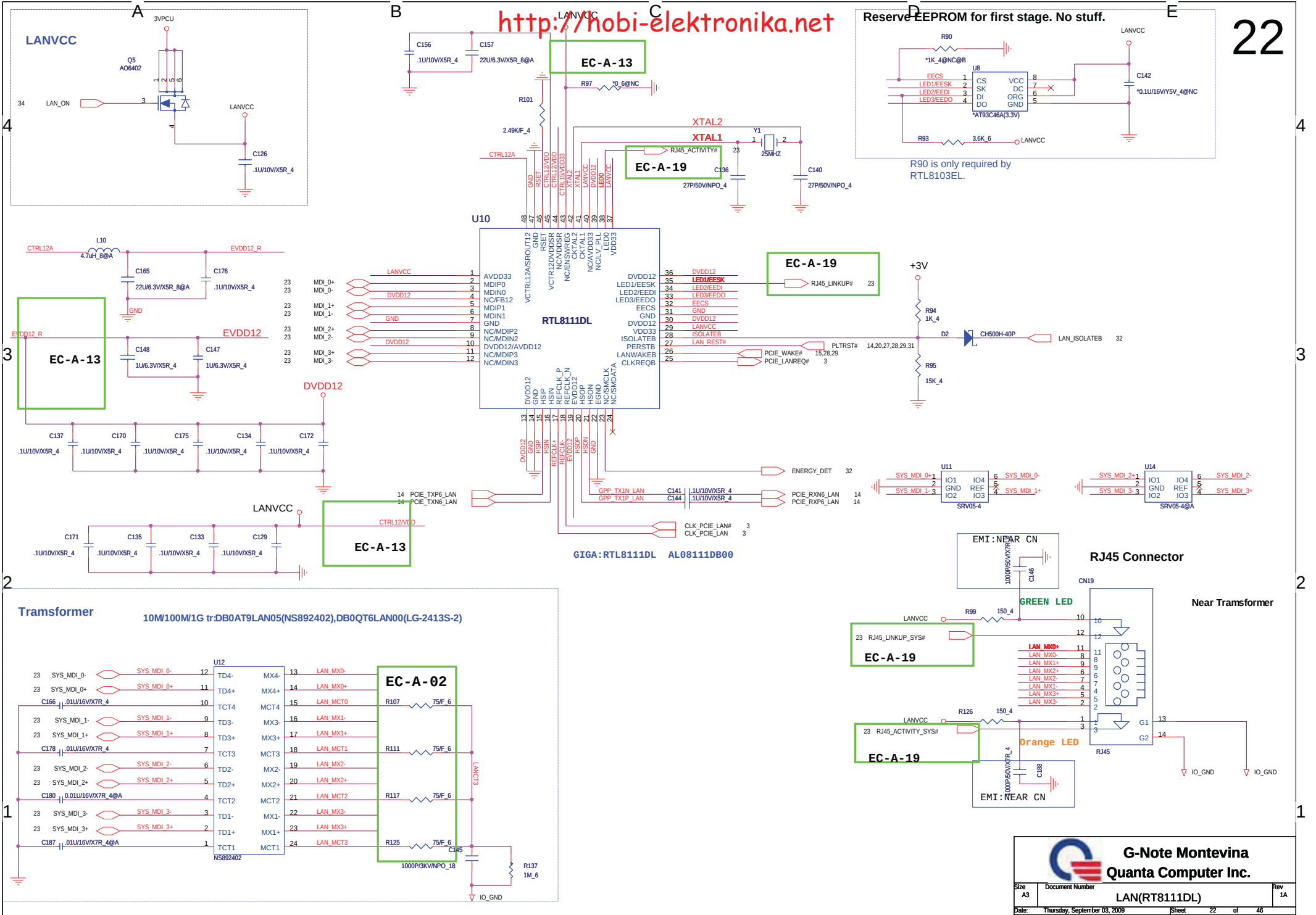
RIGHT-ANGLE-LED

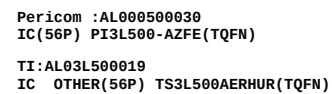
32 SUSPEND_LED# R367 221/F 4 1 LED1 SUSPEND_LED_GREEN 3 3VSUS **Suspend**



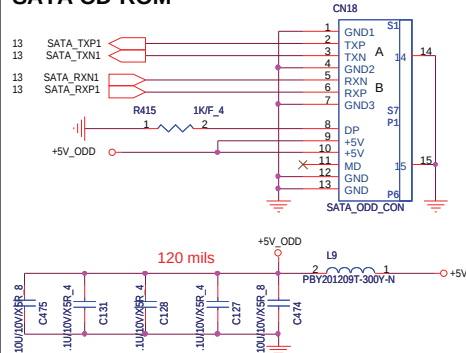
		PROJECT : G NOTE Quanta Computer Inc.	
Size Custom	Document Number USB X2/SIM_CARD/LEDs/RF	Rev 1A	
Date:	Thursday, September 03, 2009	Sheet	20 of 46

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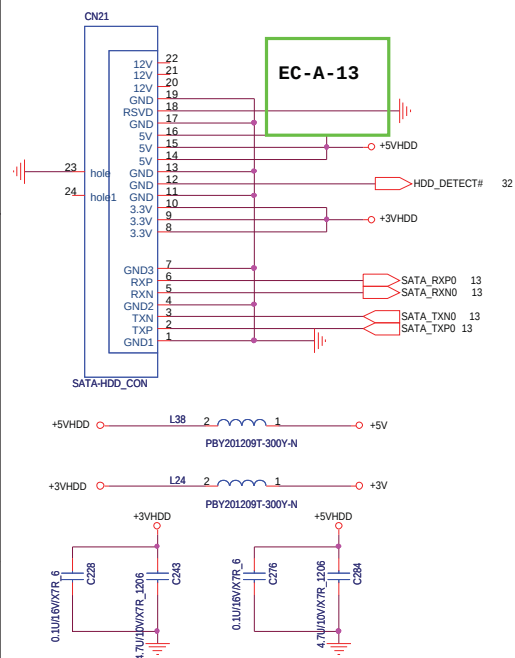




SATA CD-ROM



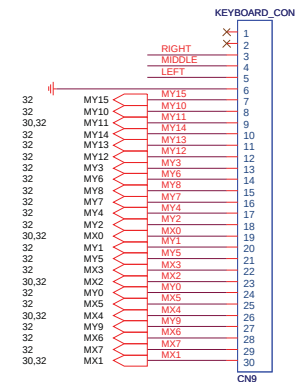
SATA-HDD



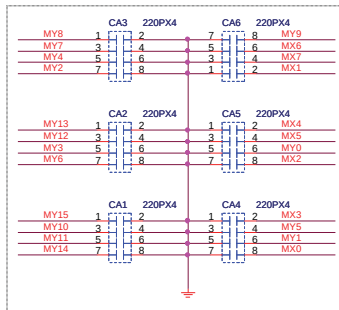
E-SATA RE-DRIVER

FAN, K/B, T/P & Track Point

KEYBOARD connector

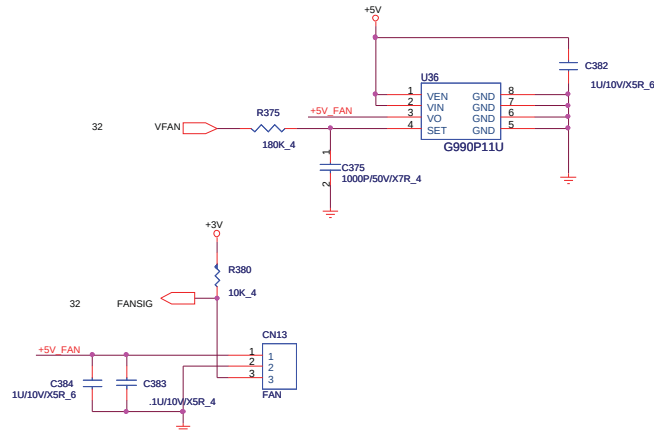


EC-A-20

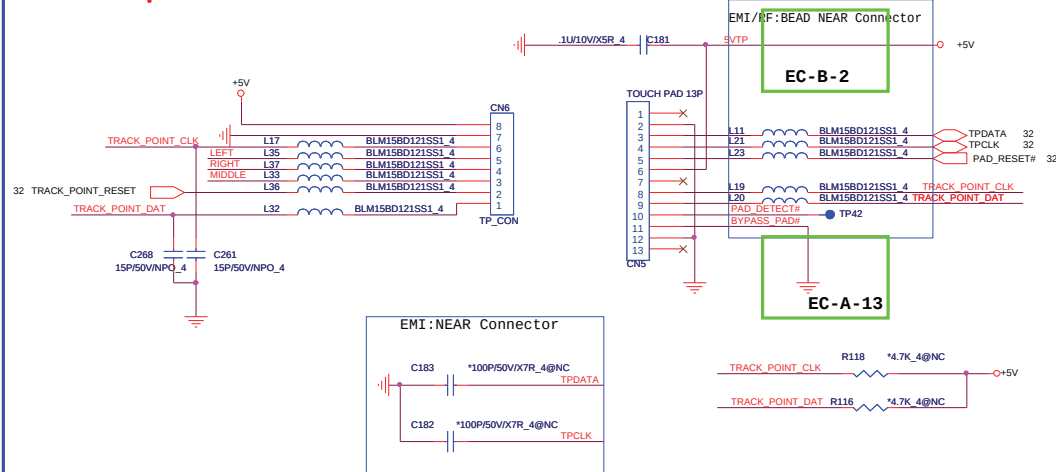


For EMI request

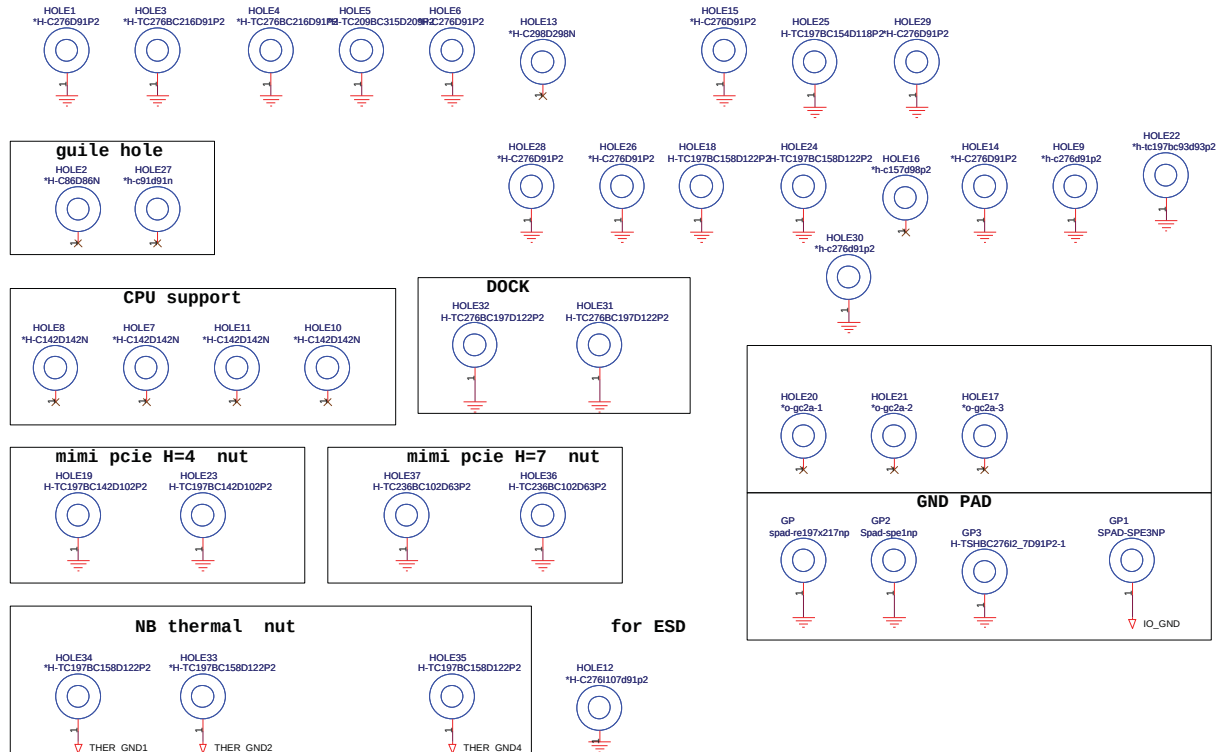
FAN Controller

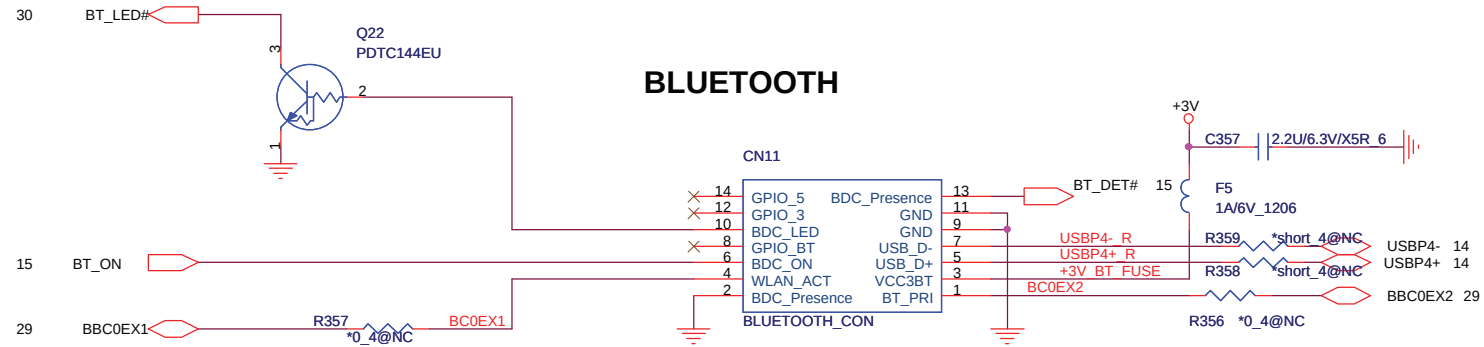


TRACK POINT TOUCH PAD



SCREW HOLE/GNDPAD



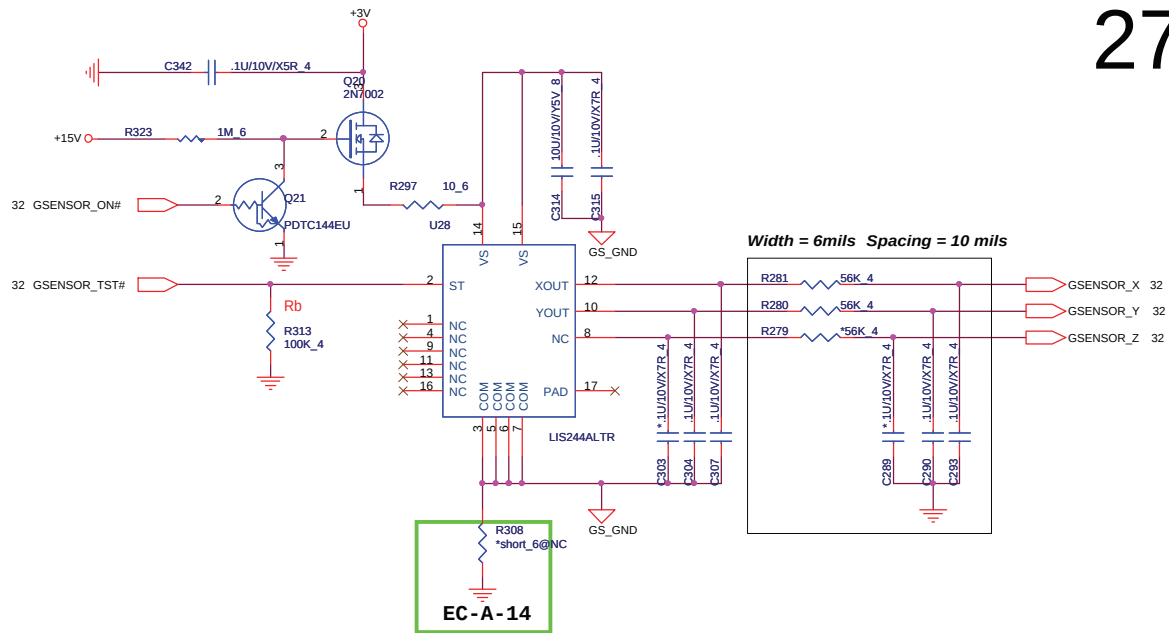


G-Note Montevina
Quanta Computer Inc.

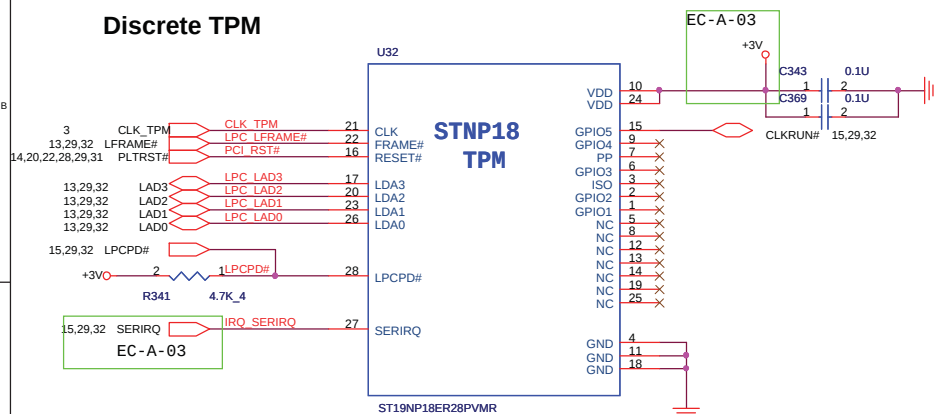
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G-SENSOR (2-Axial)

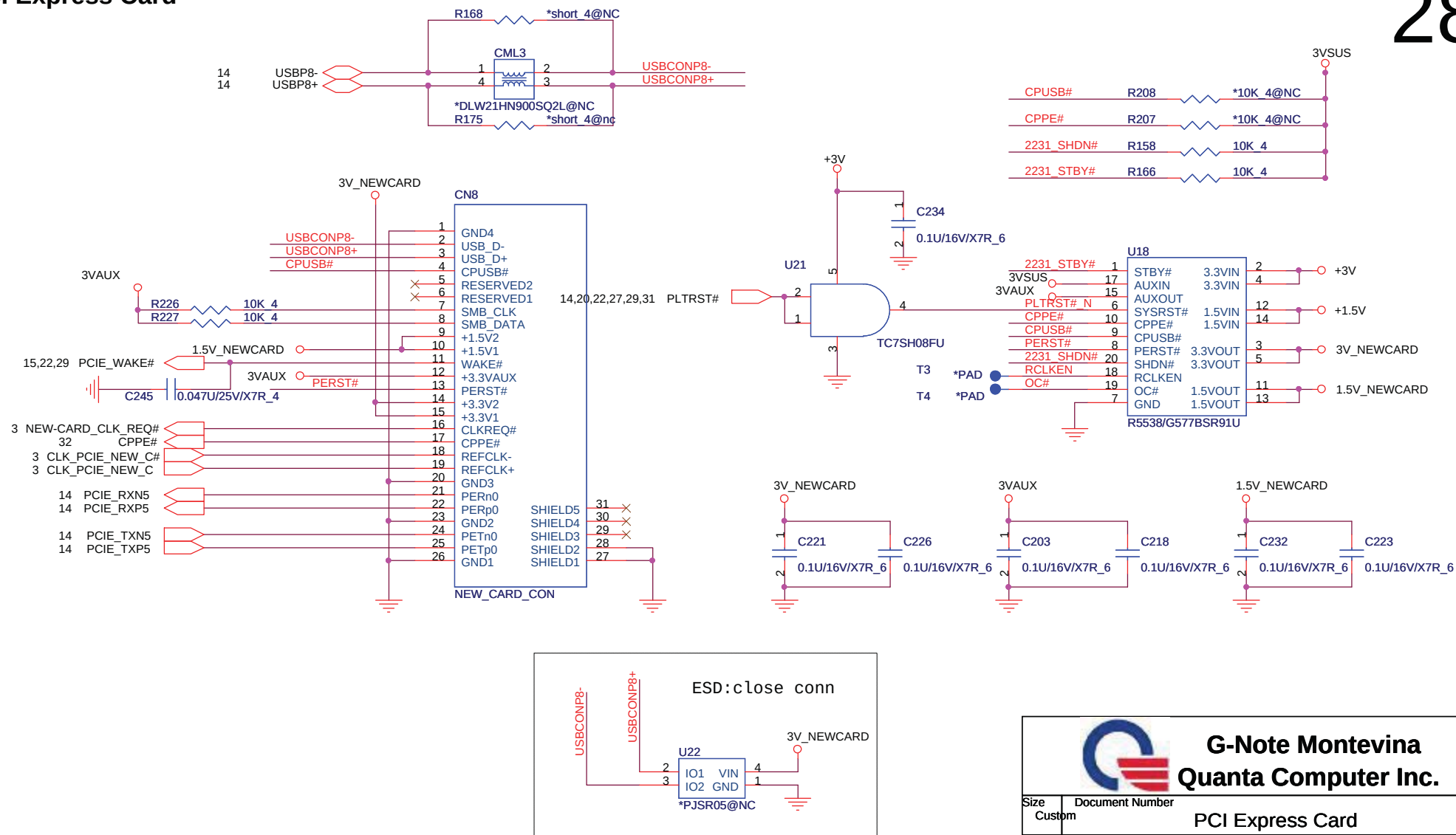


Discrete TPM

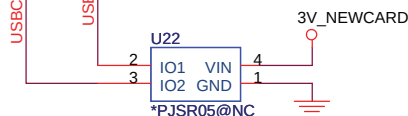


supplier P/N:ST19NP18ER28PVMR
Quanta P/N:AL19NP18K13
F/P:tssop28-6_4-65-1_2h

PCI Express Card



ESD:close conn



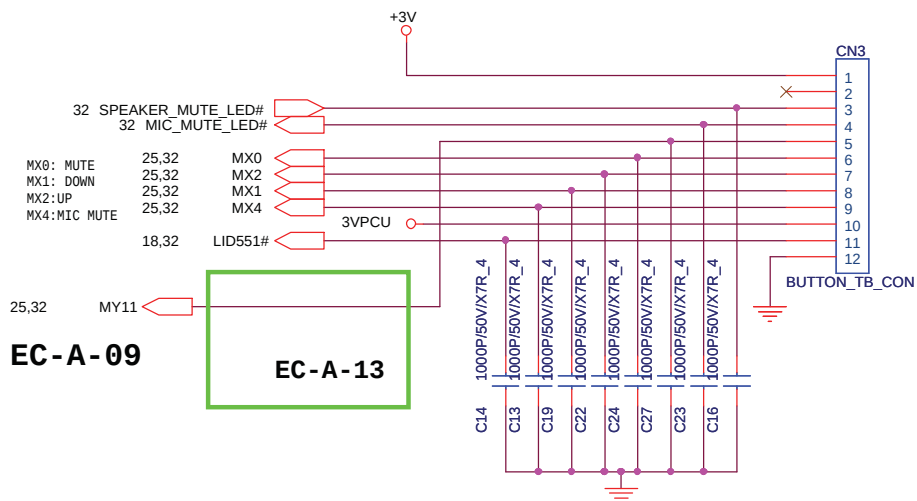


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Quanta Computer Inc.

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Custom	PCI Express Card	1A
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Daughter Boards for LEDs & Ports

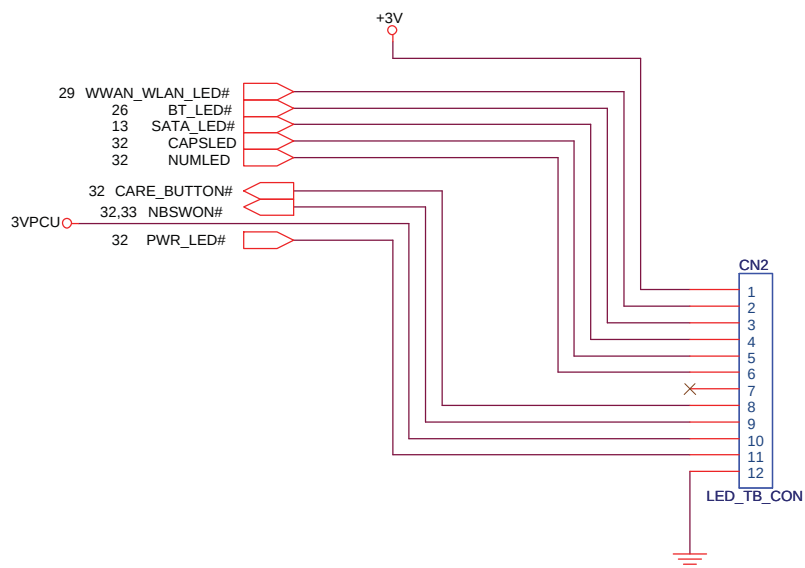
FFC TO KBD LEFT SIDE CONNECTOR



EC-A-09

EC-A-13

FFC TO LED RIGHT SIDE CONNECTOR

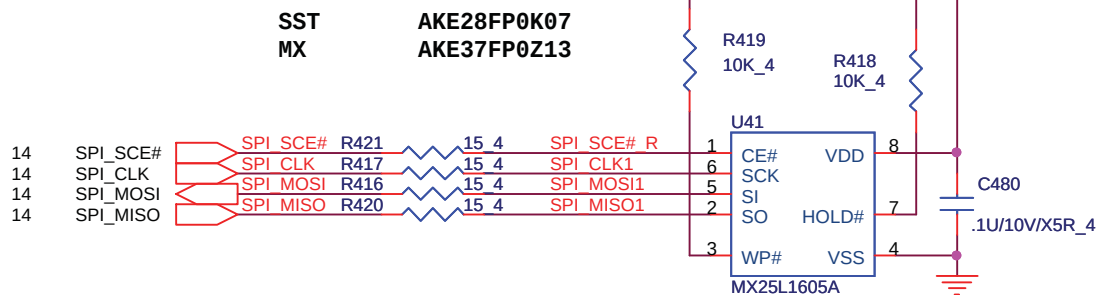


G-Note Montevina
Quanta Computer Inc.

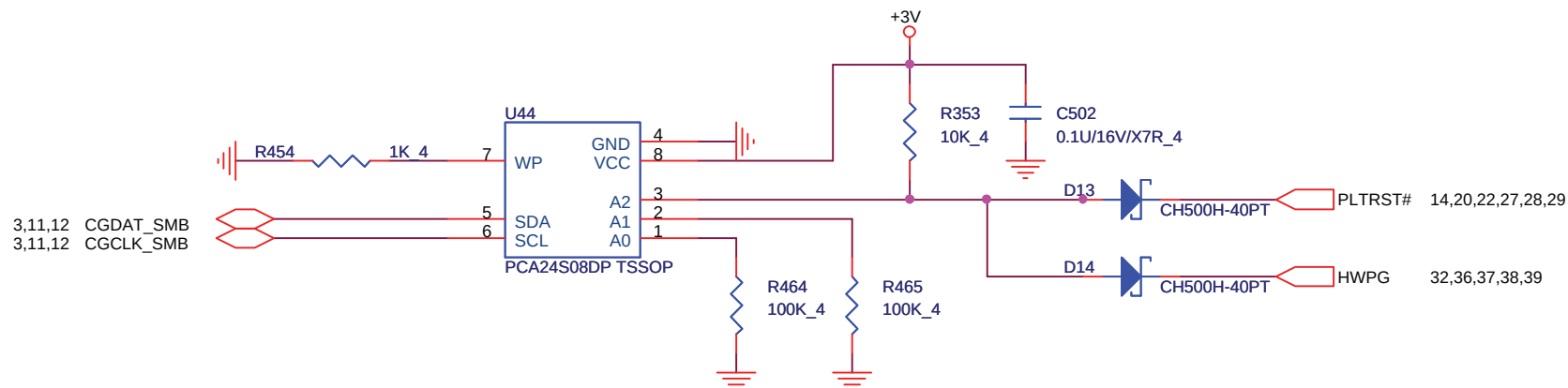
Size Custom	Document Number	Rev 1A
Date: Thursday, September 03, 2009	Sheet 30 of 46	

SPI EEPROM

16Mbit (2M Byte), SPI

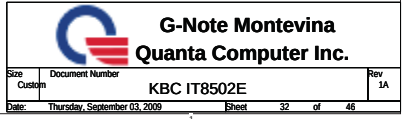


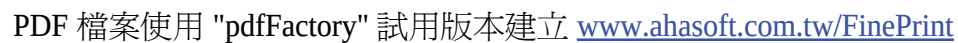
RFID EEPROM



G-Note Montevina
Quanta Computer Inc.

Size A	Document Number	Rev 1A
RFID&ITPM EEPROM		
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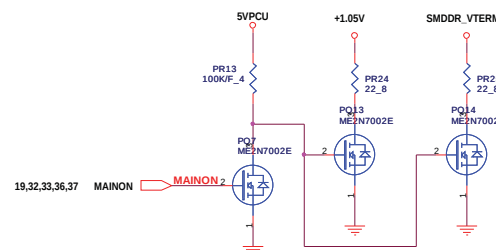
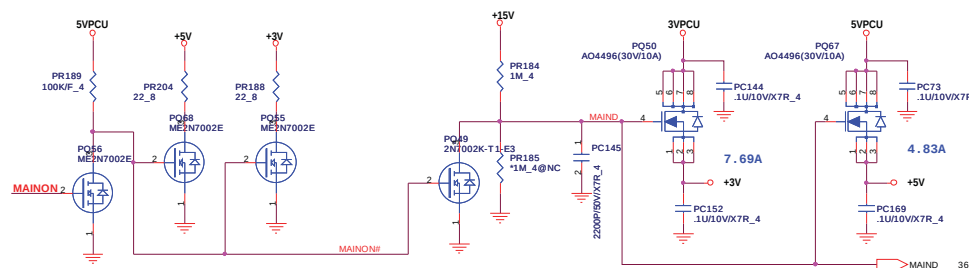




DISCHARGE

+3V, +5V

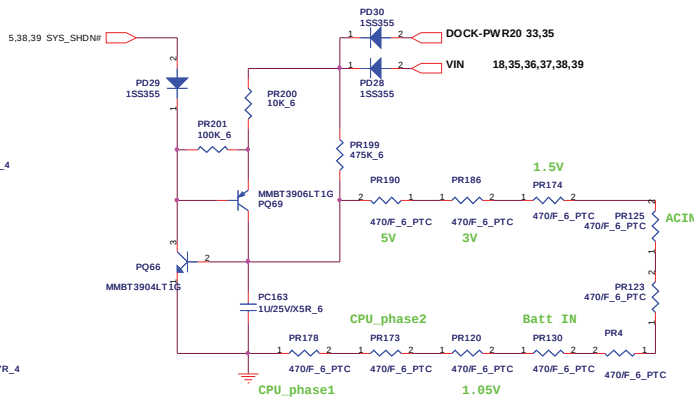
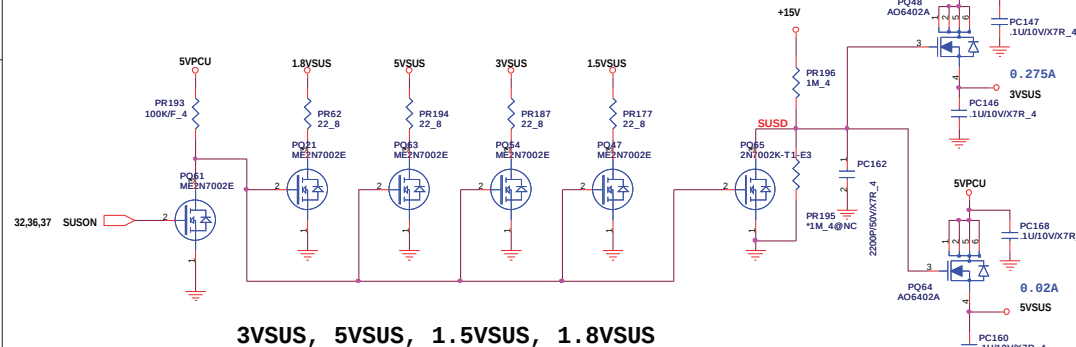
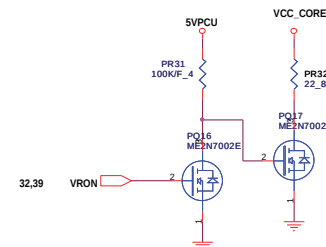
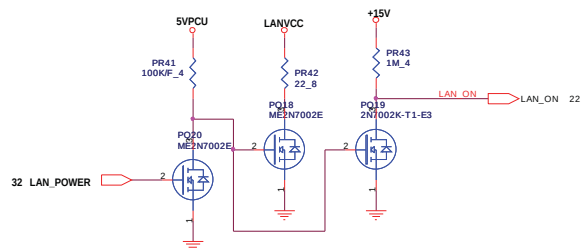
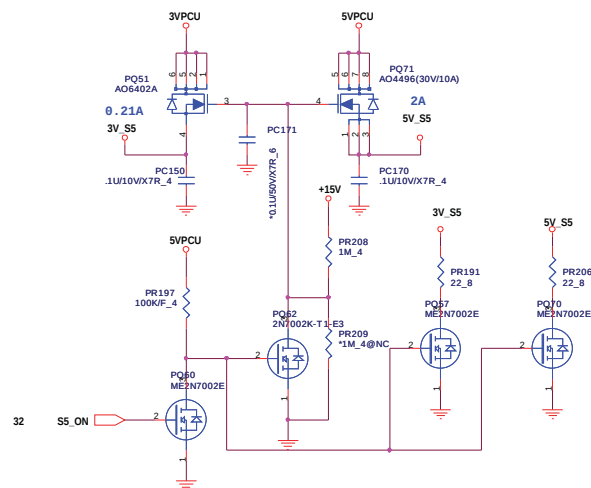
+1.05V, SMDDR_VTERM



3V_S5, 5V_S5

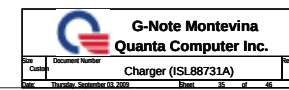
LANVCC

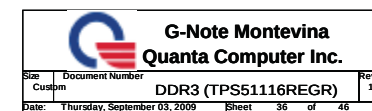
VCC_CORE

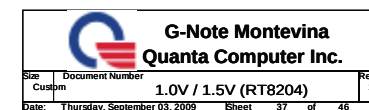


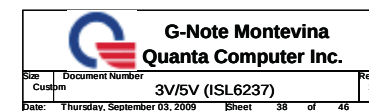
3VSUS, 5VSUS, 1.5VSUS, 1.8VSUS

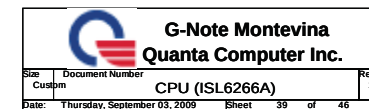
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Cuspm	Discharge
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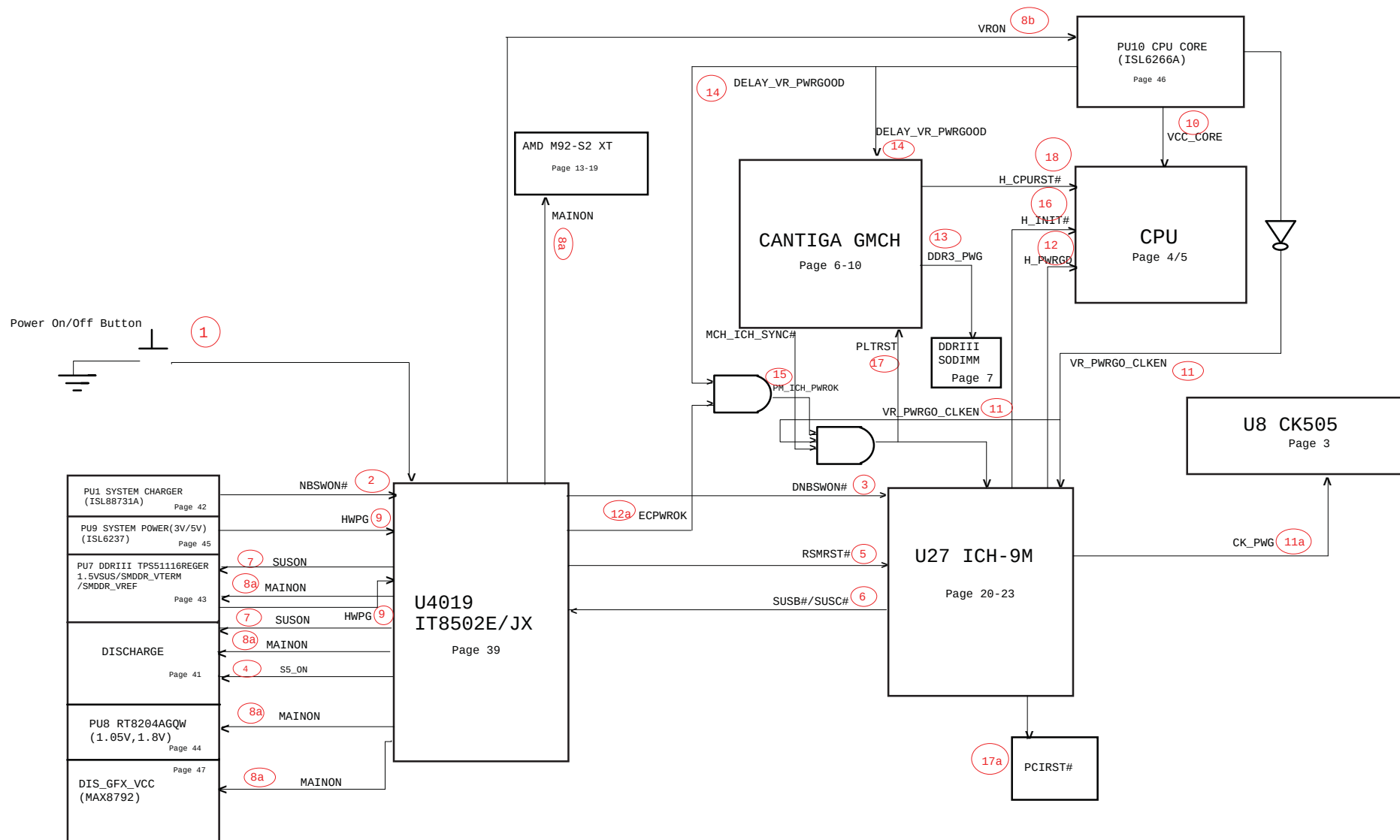












Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4@NC	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4@NC	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

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stage	EC NO.	Page	Location	description
EC-A-01	9,10		C47,C51,C58,C71,C82,C75,C66,C52	change to 0603 For height limit
EC-A-02	22		r107,r111,r117,r125	change to 0603 for hi po
EC-A-03	27			SERIRQ,+3v connect to correct
EC-A-04	33		del R3,R13	DOCK_PWRGOOD(active high) for crt switch
EC-A-05	21		Q17	change footprint (P mos)
EC-A-06	33		R2	R2 no asm, dock site already pull up
EC-A-07	33		R481,R482,R483	DOCK_PWR20-IN do not trun on when AC Adapter(at Dock) plugged. Dock#102(D/C#) pin is not low at default.---r483 No power at 5V_AL--r481,r482
EC-A-08	21		U35,L46,C367	mic noise issue
EC-A-09	7		R43,R44	R43,R44 no asm for display port(port B)
EC-A-10	19			SDVO,AUX swap
EC-A-11	31			change SPI rom power plane to 3v_S5(EC Chei-ho)
EC-A-12	24		removed R6,R7 Add U47,C520,R32,R40 R488 use 0ohm	usb switch circuit
EC-A-13			3:R222,R235,R196,R195,141,R142 RP1,RP2,RP3,RP4 4:R32 5:R388 7:R414,R61,R64 10:R401,R400,L2,R58,R88,R40,R28,R412,L54,R408,R395 11:R108 15:R301 R232 16:R268,R289,R452 R191 R424 R253 R472 R475 R476 R290 R477 R164 R223 R288 18: R147 R122 R146 R106 20: R451 R361 21: R320 R306 R278 22: R104 R102 R100 R98 23: R271 R5 25: R119 29: R438 R434 R443 30: R19 32: R319	0ohm no asm(reserved(,r121,r120,r123,r124)
EC-A-14			14: R270 18: R139 R140 19:R216 R212 R193 R188 R176 R160 R156 R169 R241 R231 20:R310 R309 R479 R480 R474 R466 21:R254 R265 R250 28:R360 R249 R168 R175 R430 R431 R444 R463 R324 R325 32 R302 33: R10 R11 26:R358 R359	0ohm use short pad
EC-A-15	15		R201,R202	change Board ID to SIT R201-->no ASM,R202--> ASM
EC-A-16	32		L30	change to 10ohm for GC2/3 g-sensor issue

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stage	EC NO.	Page	Location	description
EC-A-17	13		R472	add TPM strap
EC-A-18	13		BT1	change right footprint for smt
EC-A-19	22,23			correct act/ link singal name
EC-A-20	25		RP5,RP6	RP5,RP6 no asm by EC command
EC-A-21	33		L47, L48, L49 ,C376,C377,C378,C379,C380,C381 ,R376,R377,R378	L47,L48,L49 use 0ohm C376,C377,C378,C379,C380,C381 no ASM intel spec filter should be add in dock station R376,R377,R378 ASM(150ohm)
EC-A-22	17		R19,R28,L3,L7	H/Vsync Overshoot at Tf Vmax=1.5V issue L3,L7 use 0ohm R19,R28 use bead
EC-B-1	24			AU03 :U47 change power plane to 5v_S5
EC-B-2			L57	power combustion fail,EMI OK REMOVED
EC-B-3			del L3,L7,L47,L48,L49	0 ohm del



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Size B	Document Number EC list	Rev 1A
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EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-PA-01	35	7/23	PD8,PD10	Change to 1SS355 for improve leakage current
EC-PA-02	35	7/23	PD18	Reverse PD18
EC-PA-03	36	7/23	PR159	Change to 6.49k for OCP
EC-PA-04	36,37	7/23	PJP1,PJP2,PJP3,PJP4,PJP6,PJP7	Delete default open
EC-PA-05	36,37	7/23	PC25,PC134,PC109,PC110	Changefrom 330U/2V/9mohm to 330U/2.5V/15mohm for ESR
EC-PA-06	36	7/23	PC95	Add 100p for feedback stability
EC-PA-07	38	7/23	PL17,PL20	Change to CV-15A0MZ00 for epoxy



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Size A	Document Number Revision & Schematic Value	Description Description	Rev 1A
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