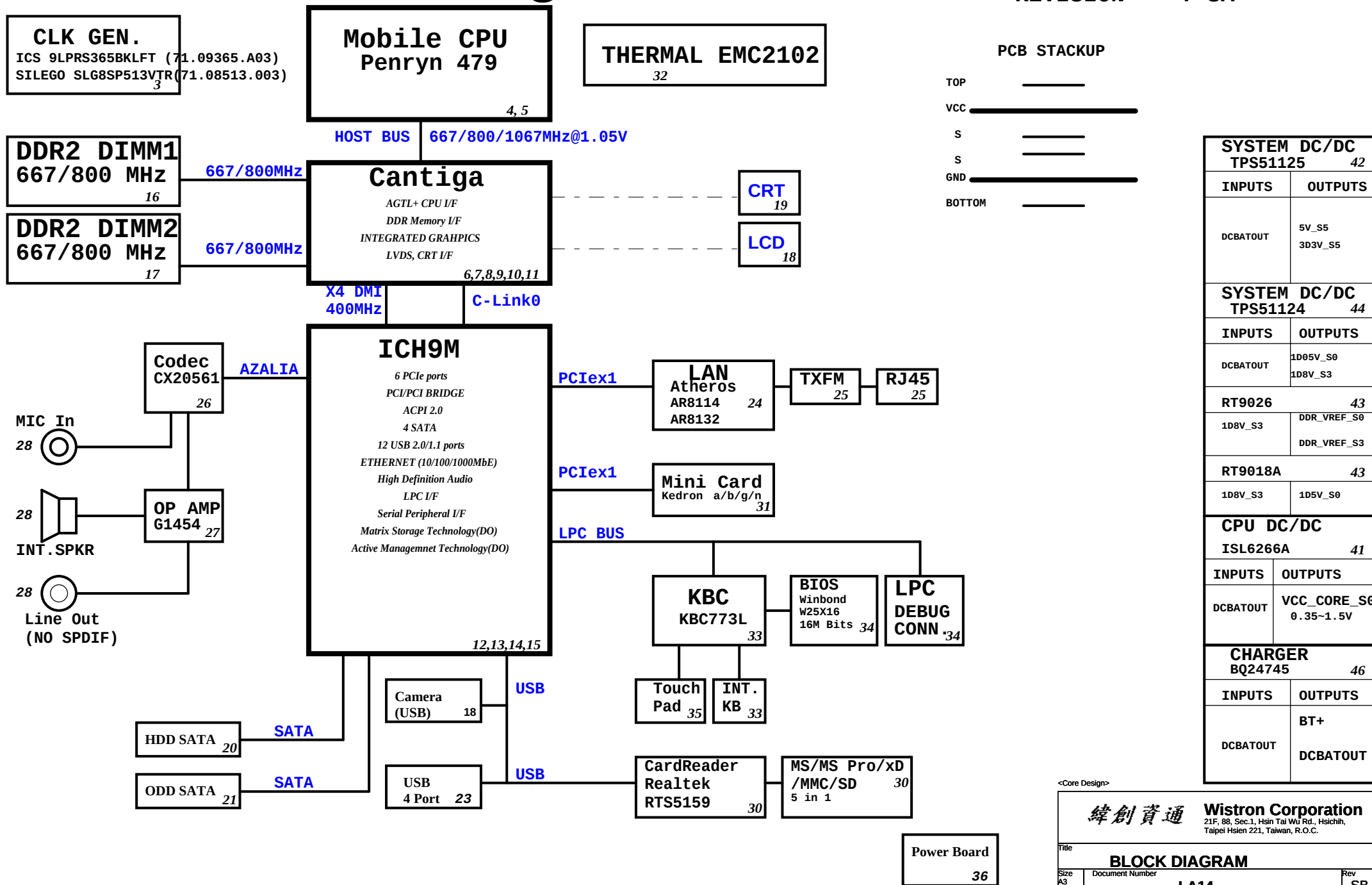


# LA14 Block Diagram

Project code: 91.4BW01.001  
PCB P/N : 48.4BW01.01M  
REVISION : SA



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

| BLOCK DIAGRAM                |                 |        |
|------------------------------|-----------------|--------|
| Size A3                      | Document Number | Rev SB |
| LA14                         |                 |        |
| Date: Thursday, May 07, 2009 | Sheet 1 of 52   |        |

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

| Signal                | Usage/When Sampled                                                     | Comment                                                                                                                                                                                                          |
|-----------------------|------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HDA_SDOUT             | XOR Chain Entrance/<br>PCIE Port Config1 bit1,<br>Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down             |
| HDA_SYNC              | PCIE config1 bit0,<br>Rising Edge of PWROK.                            | This signal has a weak internal pull-down.<br>Sets bit0 of RPC.PC(Config Registers:Offset 224h)                                                                                                                  |
| GNT2#/GPIO53          | PCIE config2 bit2,<br>Rising Edge of PWROK.                            | This signal has a weak internal pull-up.<br>Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)                                                                                                                  |
| GPIO20                | Reserved                                                               | This signal should not be pulled high.                                                                                                                                                                           |
| GNT1#/GPIO51          | ESI Strap (Server Only)<br>Rising Edge of PWROK                        | ESI compatible mode is for server platforms only.<br>This signal should not be pulled low for desttp and mobile.                                                                                                 |
| GNT3#/GPIO55          | Top-Block Swap Override.<br>Rising Edge of PWROK.                      | Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space).<br>Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#:SPI_CS1#/GPIO58 | Boot BIOS Destination Selection 0:1.<br>Rising Edge of PWROK.          | Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10).<br>GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.                                                                                   |
| SPI_MOSI              | Integrated TPM Enable,<br>Rising Edge of CLPWROK                       | Sample low: the Integrated TPM will be disabled.<br>Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.                                    |
| GPIO49                | DMI Termination Voltage,<br>Rising Edge of PWROK.                      | The signal is required to be low for desktop applications and required to be high for mobile applications.                                                                                                       |
| SATALED#              | PCI Express Lane Reversal. Rising Edge of PWROK.                       | Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)                                                                                                                          |
| SPKR                  | No Reboot.<br>Rising Edge of PWROK.                                    | If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.                                            |
| TP3                   | XOR Chain Entrance.<br>Rising Edge of PWROK.                           | This signal should not be pull low unless using XOR Chain testing.                                                                                                                                               |
| GPIO33/HDA_DOCK_EN#   | Flash Descriptor Security Override Strap<br>Rising Edge of PWROK       | Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.      |

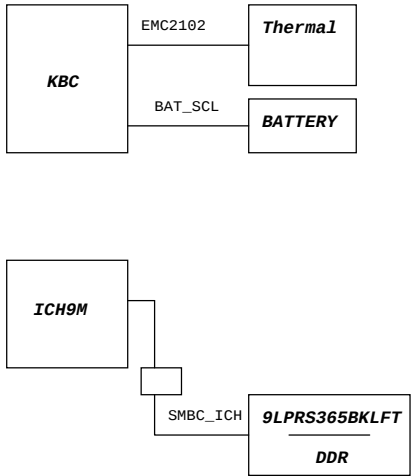
PCIE Routing

|       |                     |
|-------|---------------------|
| LANE1 | LAN Atheros AR8114A |
| LANE2 | MiniCard WLAN       |
| LANE3 | NC                  |
| LANE4 | NC                  |
| LANE5 | NC                  |
| LANE6 | NC                  |

USB Table

| USB  |                  |
|------|------------------|
| Pair | Device           |
| 0    | USB1             |
| 1    | NC               |
| 2    | NC               |
| 3    | MINIC1           |
| 4    | WEBCAM           |
| 5    | NC               |
| 6    | NC               |
| 7    | Bluetooth        |
| 8    | NC               |
| 9    | USB2(High speed) |
| 10   | NC               |
| 11   | CardReader       |

SMBus



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

| SIGNAL                     | Resistor Type/Value                                                                                                 |
|----------------------------|---------------------------------------------------------------------------------------------------------------------|
| CL_CLK[1:0]                | PULL-UP 20K                                                                                                         |
| CL_DATA[1:0]               | PULL-UP 20K                                                                                                         |
| CL_RST0#                   | PULL-UP 20K                                                                                                         |
| DPRSLPVR/GPIO16            | PULL-DOWN 20K                                                                                                       |
| ENERGY_DETECT              | PULL-UP 20K                                                                                                         |
| HDA_BIT_CLK                | PULL-DOWN 20K                                                                                                       |
| HDA_DOCK_EN#/GPIO33        | PULL-UP 20K                                                                                                         |
| HDA_RST#                   | PULL-DOWN 20K                                                                                                       |
| HDA_SDIN[3:0]              | PULL-DOWN 20K                                                                                                       |
| HDA_SDOUT                  | PULL-DOWN 20K                                                                                                       |
| HDA_SYNC                   | PULL-DOWN 20K                                                                                                       |
| GLAN_DOCK#                 | The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller |
| GNT[3:0]#/GPIO[55, 53, 51] | PULL-UP 20K                                                                                                         |
| GPIO[20]                   | PULL-DOWN 20K                                                                                                       |
| GPIO[49]                   | PULL-UP 20K                                                                                                         |
| LDA[3:0]#/FHW[3:0]#        | PULL-UP 20K                                                                                                         |
| LAN_RXD[2:0]               | PULL-UP 20K                                                                                                         |
| LDRQ[0]                    | PULL-UP 20K                                                                                                         |
| LDRQ[1]/GPIO23             | PULL-UP 20K                                                                                                         |
| PME#                       | PULL-UP 20K                                                                                                         |
| PWRBTN#                    | PULL-UP 20K                                                                                                         |
| SATALED#                   | PULL-UP 15K                                                                                                         |
| SPI_CS1#/GPIO58/CLGPIO6    | PULL-UP 20K                                                                                                         |
| SPI_MOSI                   | PULL-DOWN 20K                                                                                                       |
| SPI_MISO                   | PULL-UP 20K                                                                                                         |
| SPKR                       | PULL-DOWN 20K                                                                                                       |
| TACH_[3:0]                 | PULL-UP 20K                                                                                                         |
| TP[3]                      | PULL-UP 20K                                                                                                         |
| USB[11:0][P,N]             | PULL-DOWN 15K                                                                                                       |

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

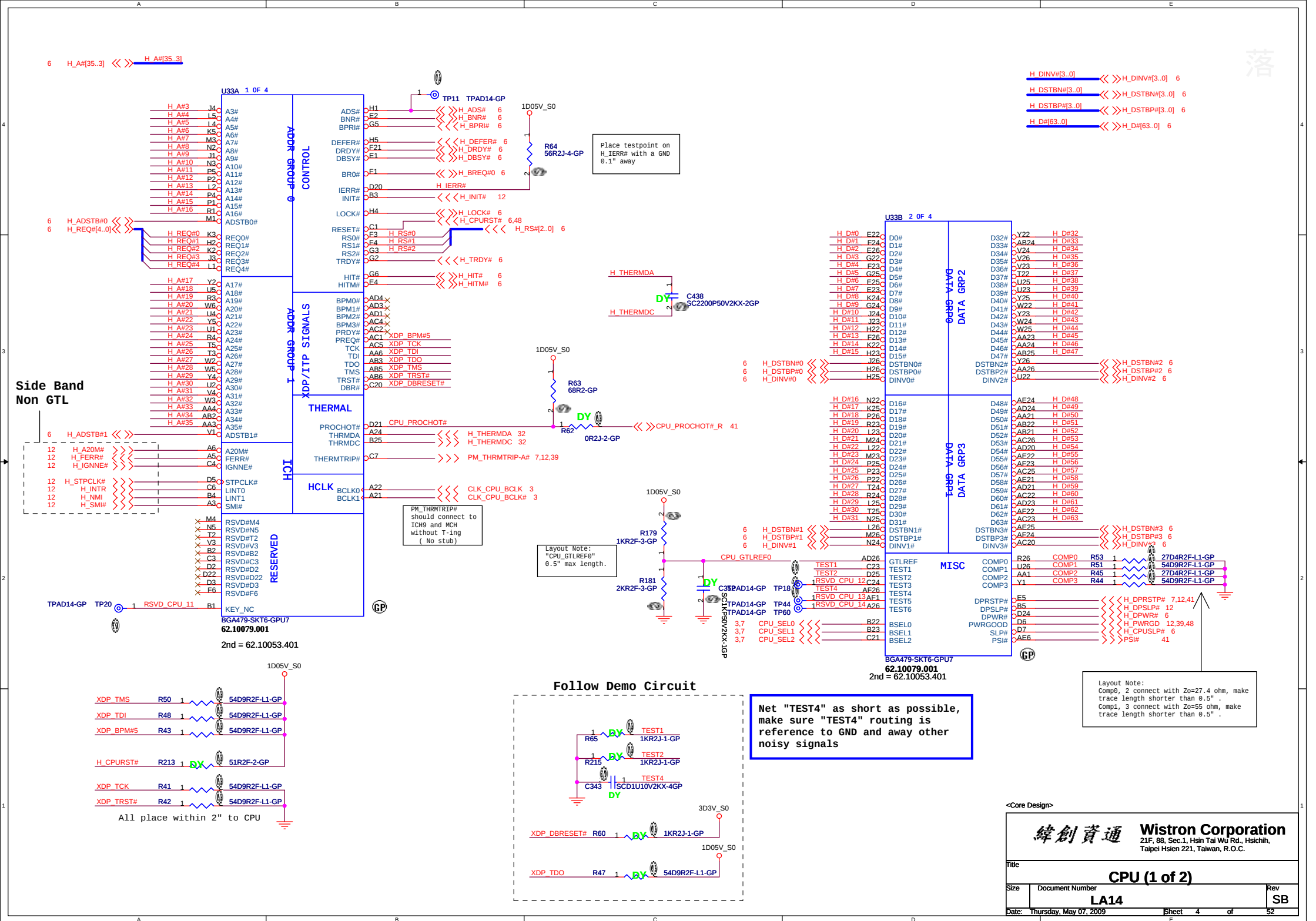
| Pin Name                                     | Strap Description                                         | Configuration                                                                                                                                                        |
|----------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG[2:0]                                     | FSB Frequency Select                                      | 000 = FSB1067<br>011 = FSB667<br>010 = FSB800<br>others = Reserved                                                                                                   |
| CFG[4:3]<br>CFG8<br>CFG[15:14]<br>CFG[18:17] | Reserved                                                  |                                                                                                                                                                      |
| CFG5                                         | DMI x2 Select                                             | 0 = DMI x2<br>1 = DMI x4 (Default)                                                                                                                                   |
| CFG6                                         | iTPM Host Interface                                       | 0= The iTPM Host Interface is enabled(Note2)<br>1=The iTPM Host Interface is disabled(default)                                                                       |
| CFG7                                         | Intel Management engine Crypto strap                      | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality<br>1 = TLS cipher suite with confidentiality (default)                                       |
| CFG9                                         | PCIE Graphics Lane                                        | 0 = Reverse Lanes,15->0,14->1 ect..<br>1= Normal operation(Default):Lane Numbered in order                                                                           |
| CFG10                                        | PCIE Loopback enable                                      | 0 = Enable (Note 3)<br>1= Disabled (default)                                                                                                                         |
| CFG[13:12]                                   | XOR/ALL                                                   | 00 = Reserve<br>10 = XOR mode Enabled<br>01 = ALLZ mode Enabled (Note 3)<br>11 = Disabled (default)                                                                  |
| CFG16                                        | FSB Dynamic ODT                                           | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default)                                                                                                        |
| CFG19                                        | DMI Lane Reversal                                         | 0 = Normal operation(Default): Lane Numbered in Order<br>1 = Reverse Lanes<br>DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3)<br>DMI x2 mode[MCH -> ICH]:(3->0,2->1) |
| CFG20                                        | Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE | 0 = Only Digital Display Port or PCIE is operational (Default)<br>1 = Digital display port and PCie are operating simultaneously via the PEG port                    |
| SDVO_CTRLDATA                                | SDVO Present                                              | 0 =No SDVO Card Present (Default)<br>1 = SDVO Card Present                                                                                                           |
| L_DDC_DATA                                   | Local Flat Panel (LFP) Present                            | 0 = LFP Disabled (Default)<br>1= LFP Card Present; PCIE disabled                                                                                                     |

NOTE:  
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.  
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.  
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

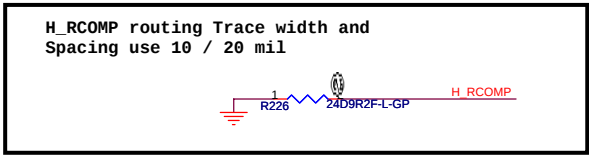
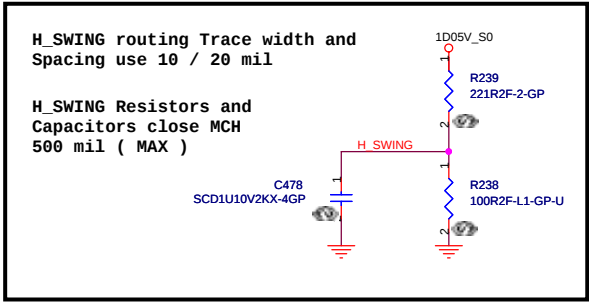
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|                                                                            |                      |
|----------------------------------------------------------------------------|----------------------|
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| Title                                                                      |                      |
| Reference                                                                  |                      |
| Size A3                                                                    | Document Number LA14 |
| Date: Thursday, May 07, 2009                                               | Sheet 2 of 52        |

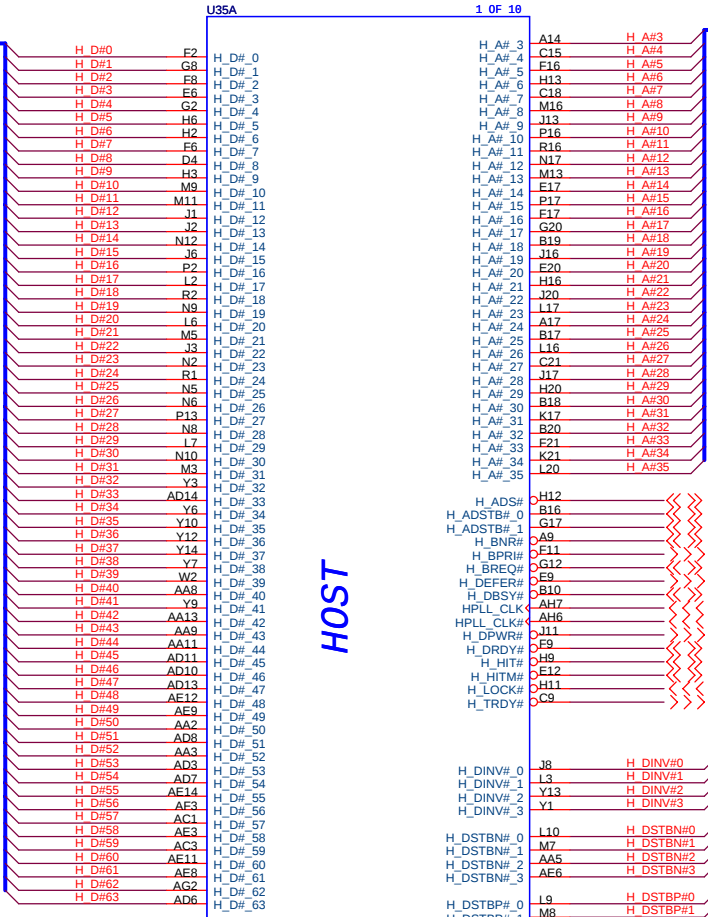
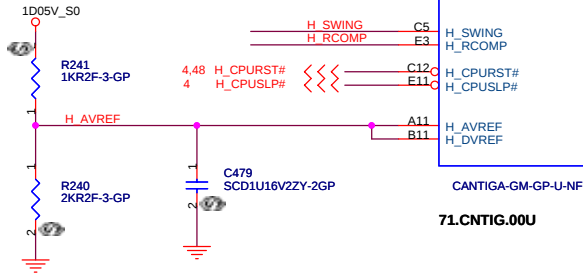




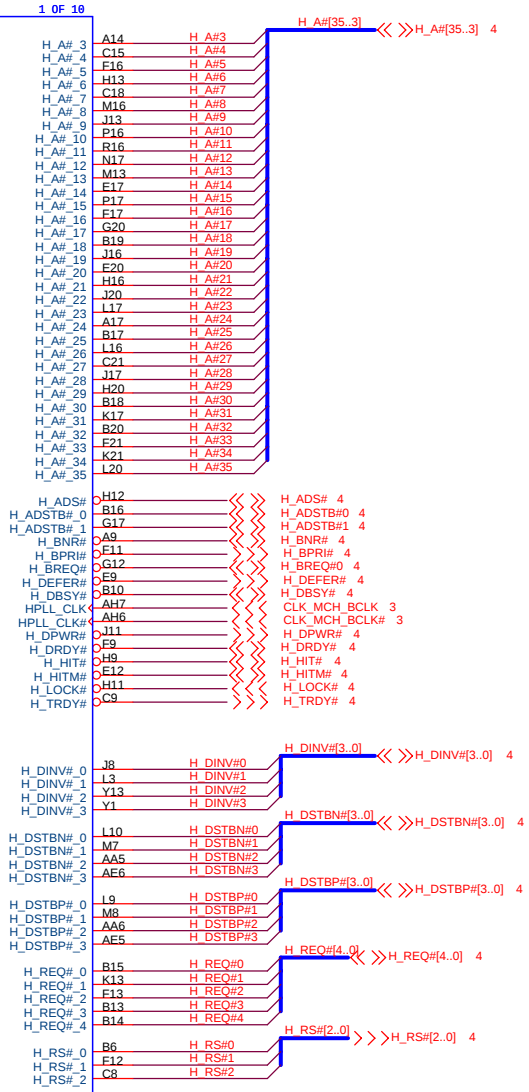


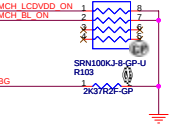
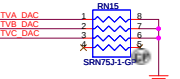
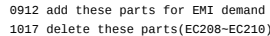


Place them near to the chip ( < 0.5")



HOST

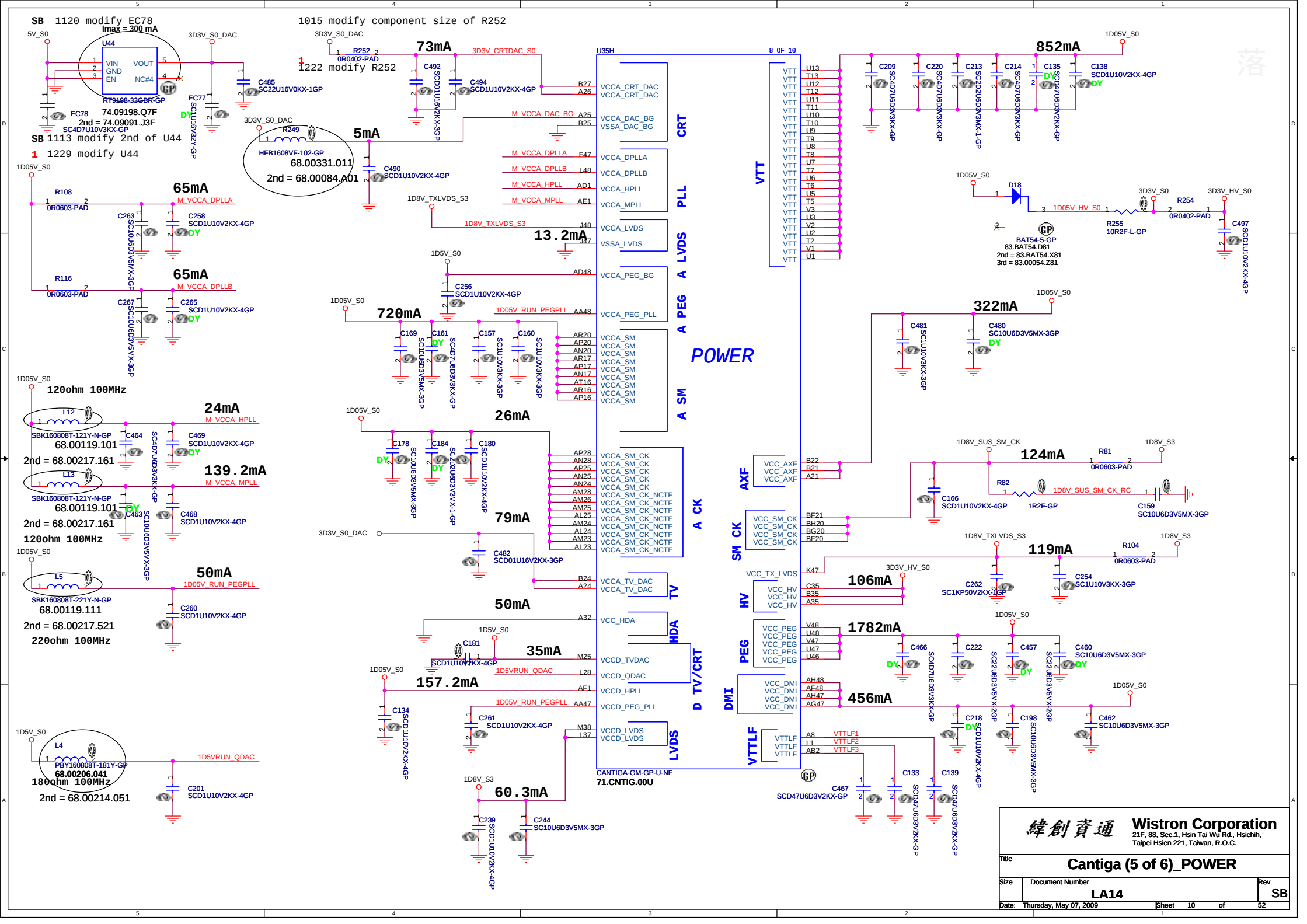


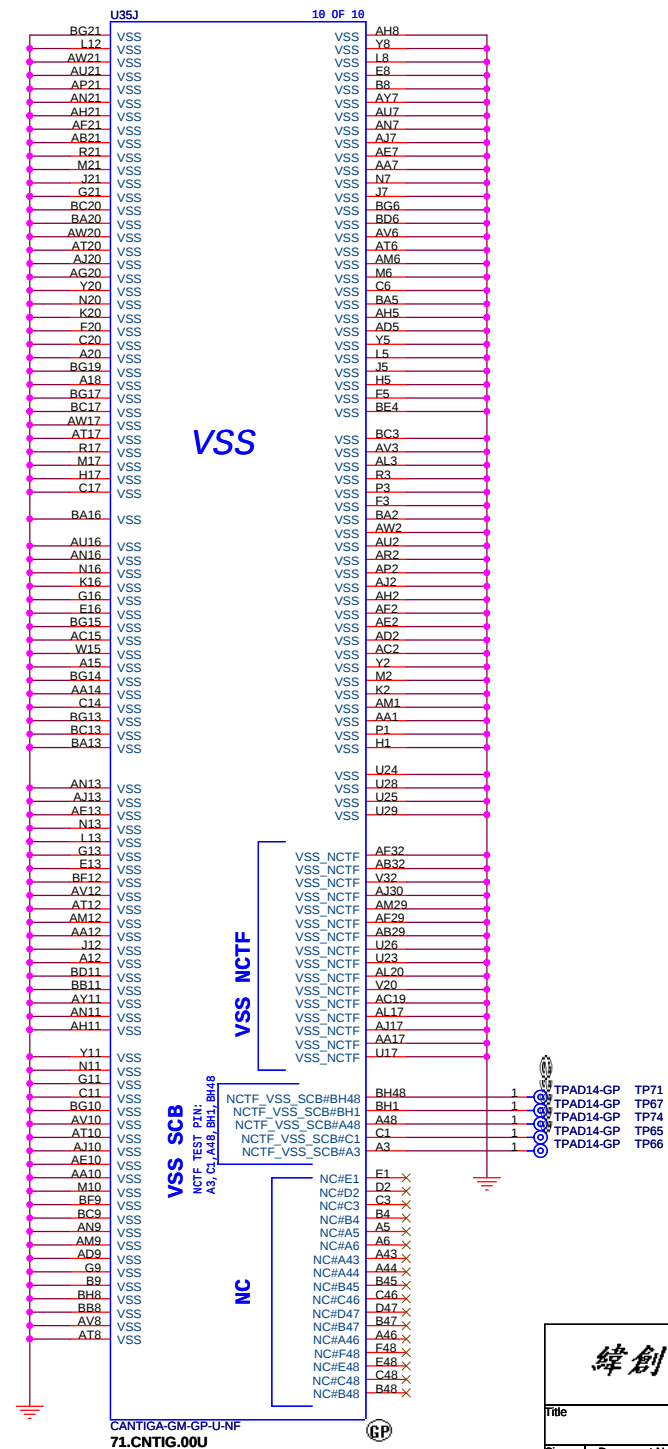
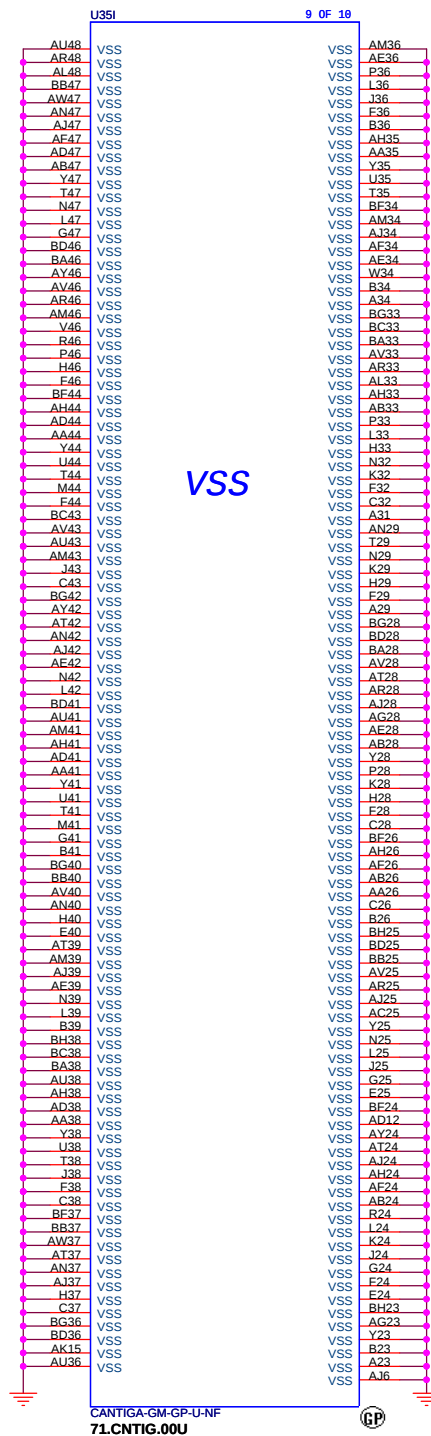


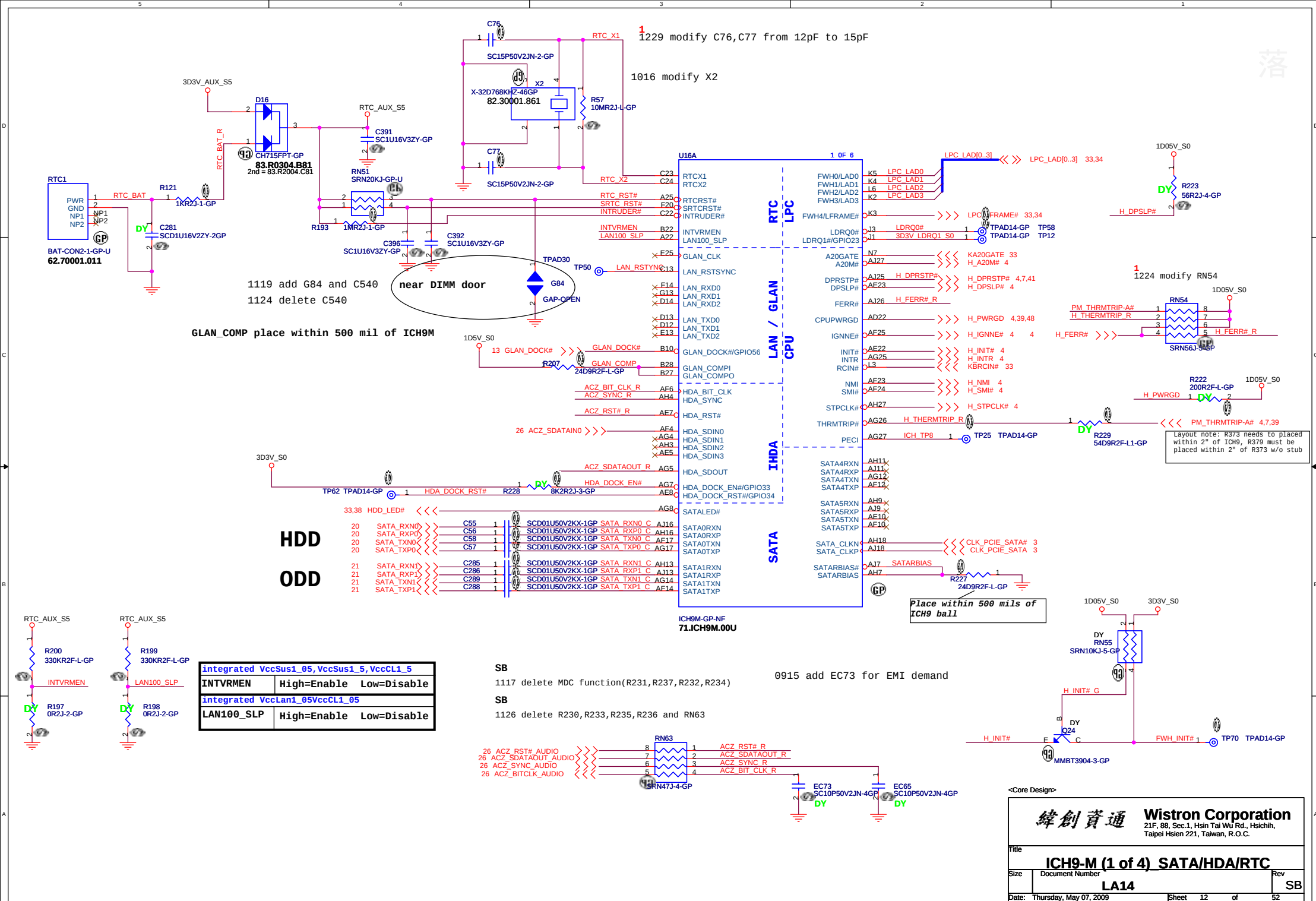
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| Title                                                                                                                                                                                             |                                |
| <b>Cantiga (2 of 6) DMI/PM/CFG</b>                                                                                                                                                                |                                |
| Size                                                                                                                                                                                              | Document Number<br><b>LA14</b> |
| Date: Thursday, May 07 2009                                                                                                                                                                       | Sheet 7 of 52<br><b>SB</b>     |

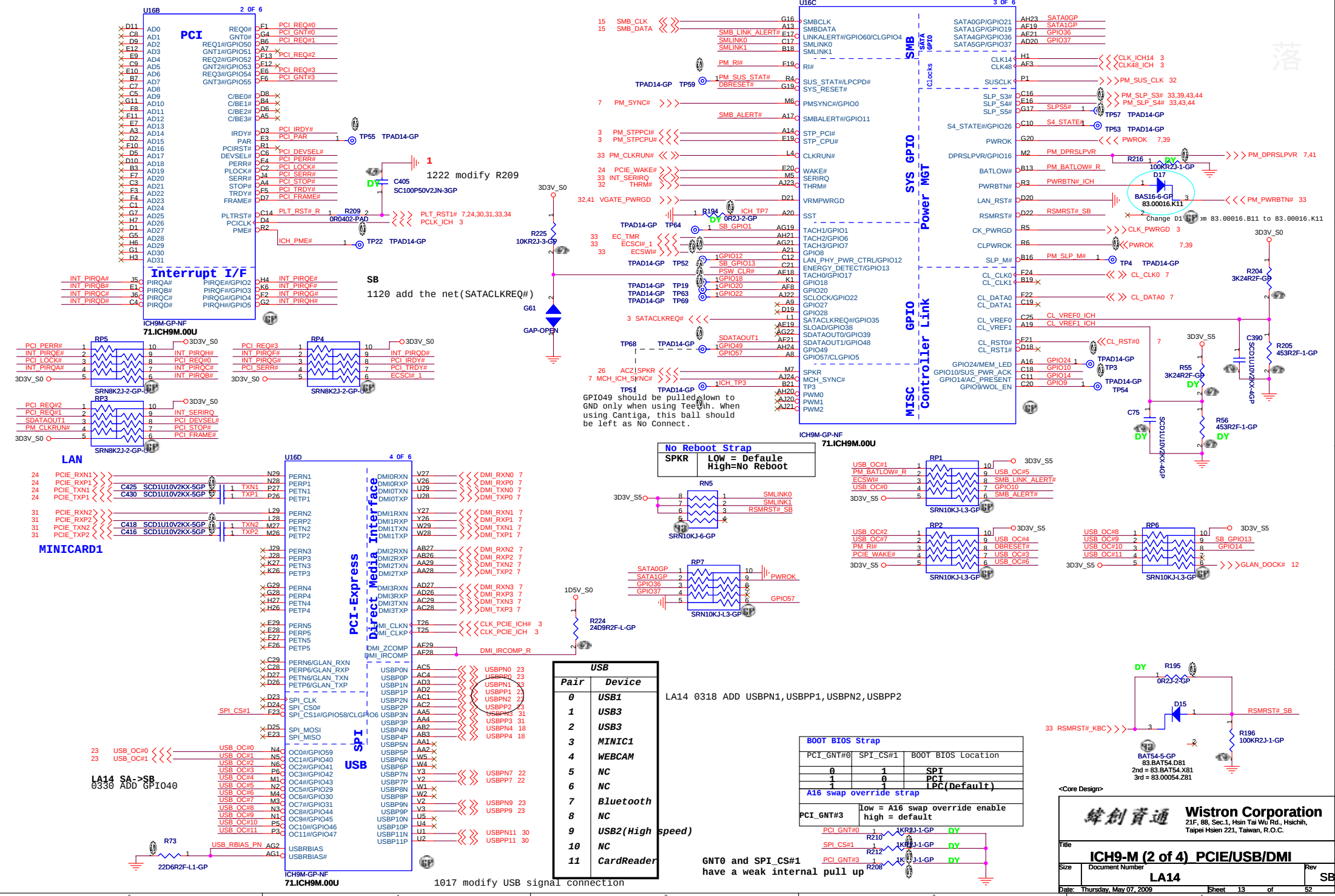












| USB  |                  |
|------|------------------|
| Pair | Device           |
| 0    | USB1             |
| 1    | USB3             |
| 2    | USB3             |
| 4    | MINIC1           |
| 4    | WEBCAM           |
| 5    | NC               |
| 6    | NC               |
| 7    | Bluetooth        |
| 8    | NC               |
| 9    | USB2(High speed) |
| 10   | NC               |
| 11   | CardReader       |

| BOOT BIOS Strap                |          |                    |
|--------------------------------|----------|--------------------|
| PCI_GNT#0                      | SPI_CS#1 | BOOT BIOS Location |
| 0                              | 1        | SPI                |
| 1                              | 0        | PCI                |
| 1                              | 1        | IPC(Default)       |
| A16 swap override strap        |          |                    |
| low = A16 swap override enable |          |                    |
| high = default                 |          |                    |

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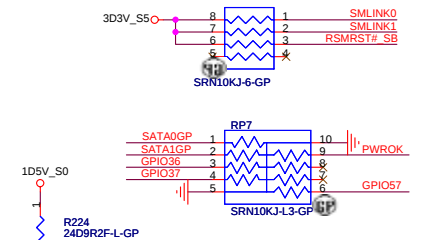
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|       |                              |       |          |
|-------|------------------------------|-------|----------|
| Title | ICH9-M (2 of 4) PCIE/USB/DMI |       |          |
| Size  | Document Number              | LA14  | Rev      |
| Date  | Thursday, May 07, 2009       | Sheet | 13 of 52 |

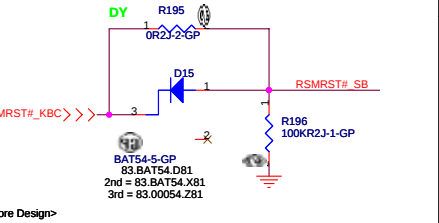
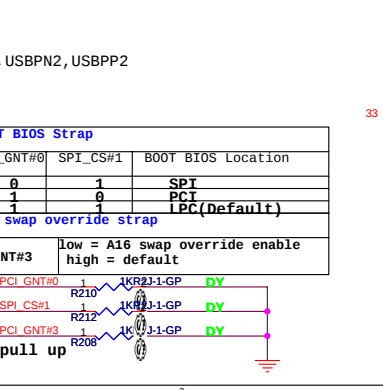
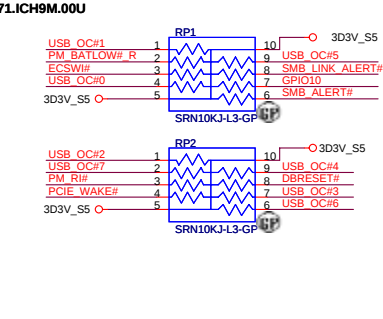
No Reboot Strap

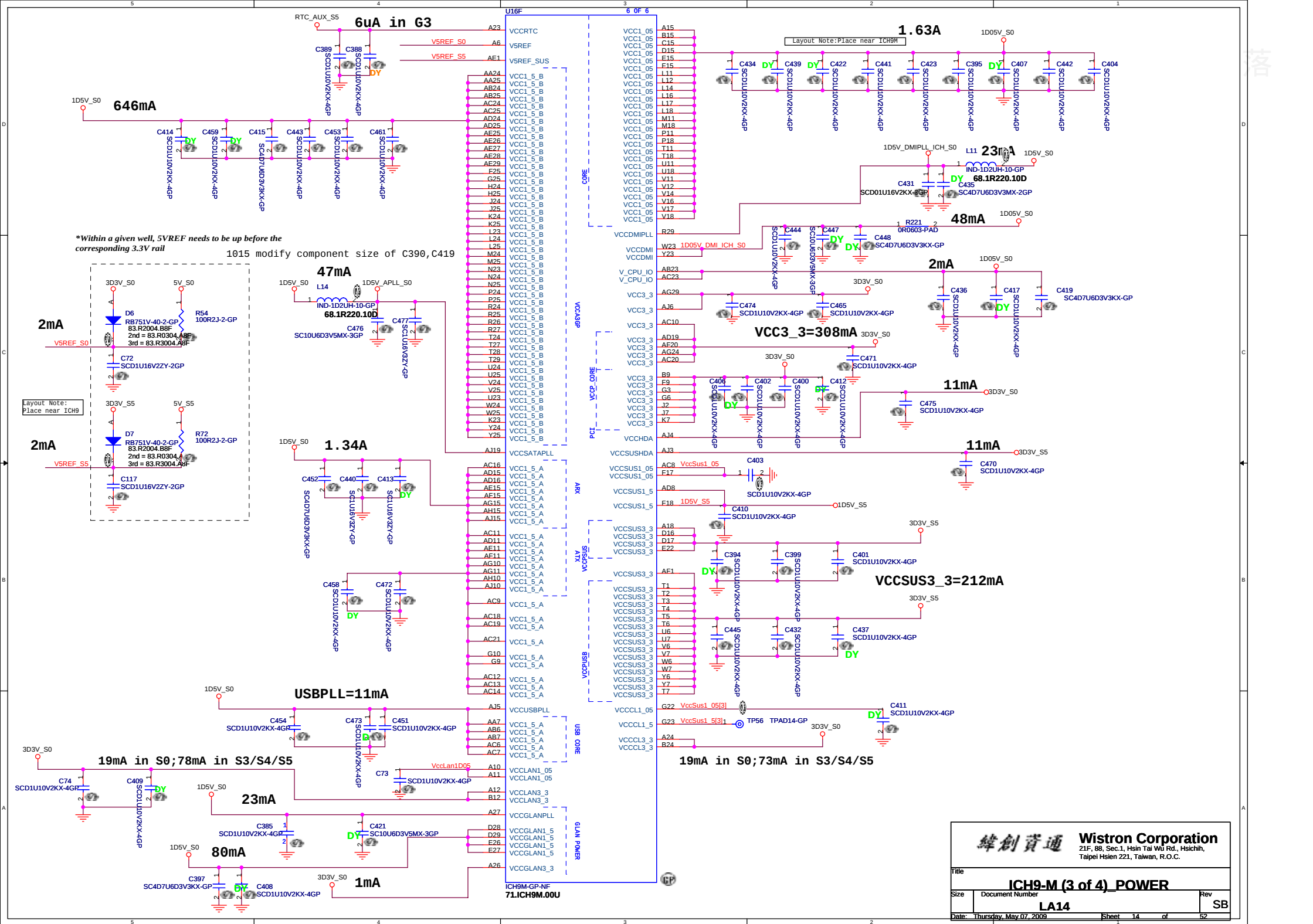
SPKR LOW = Default High = No Reboot

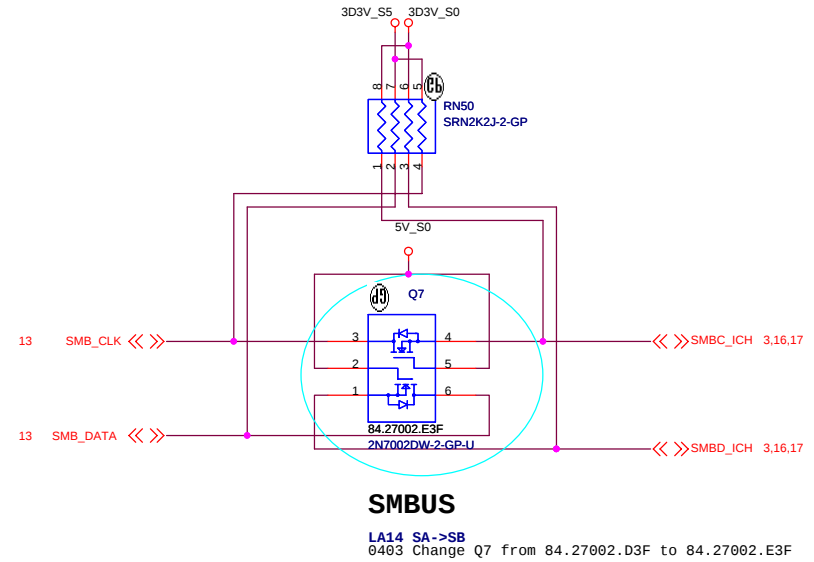
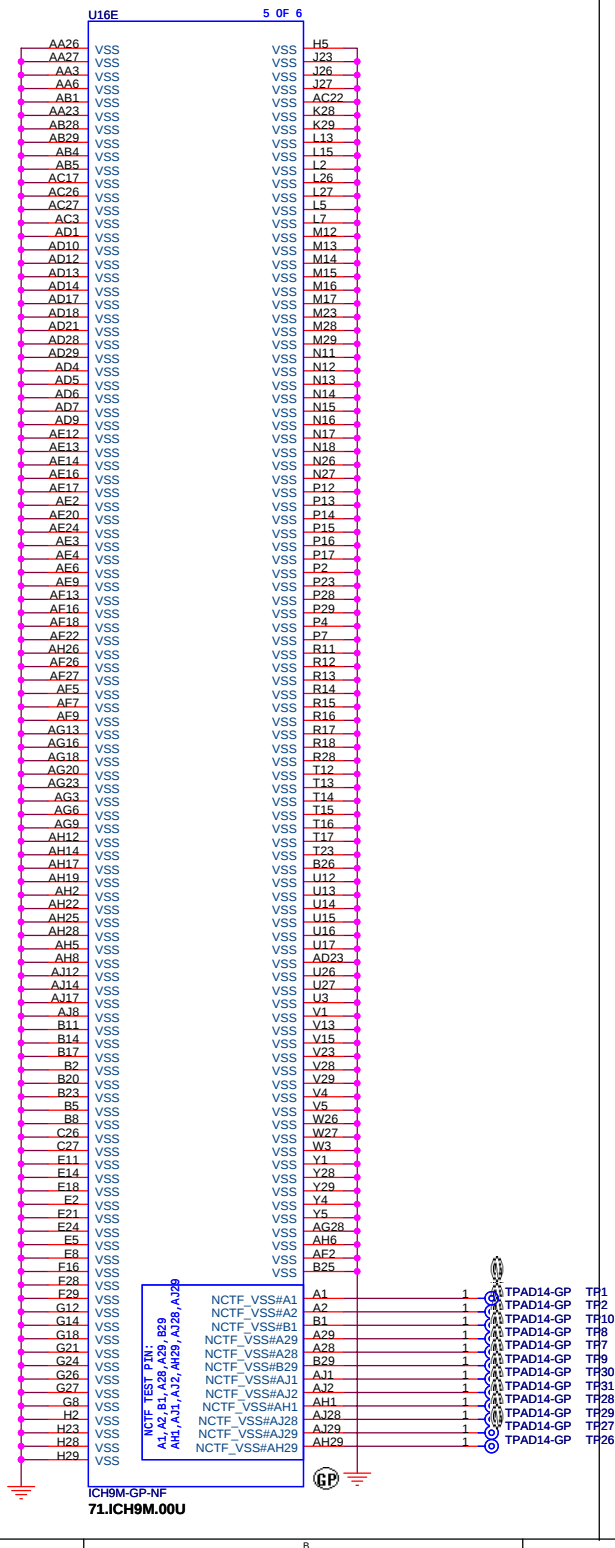


LA14 0318 ADD USBP1, USBP11, USBP2, USBP22

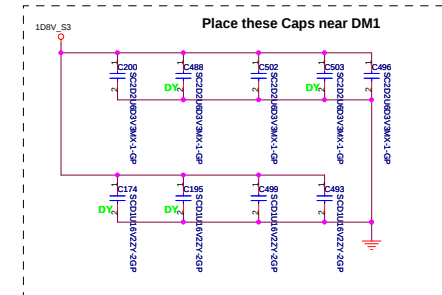
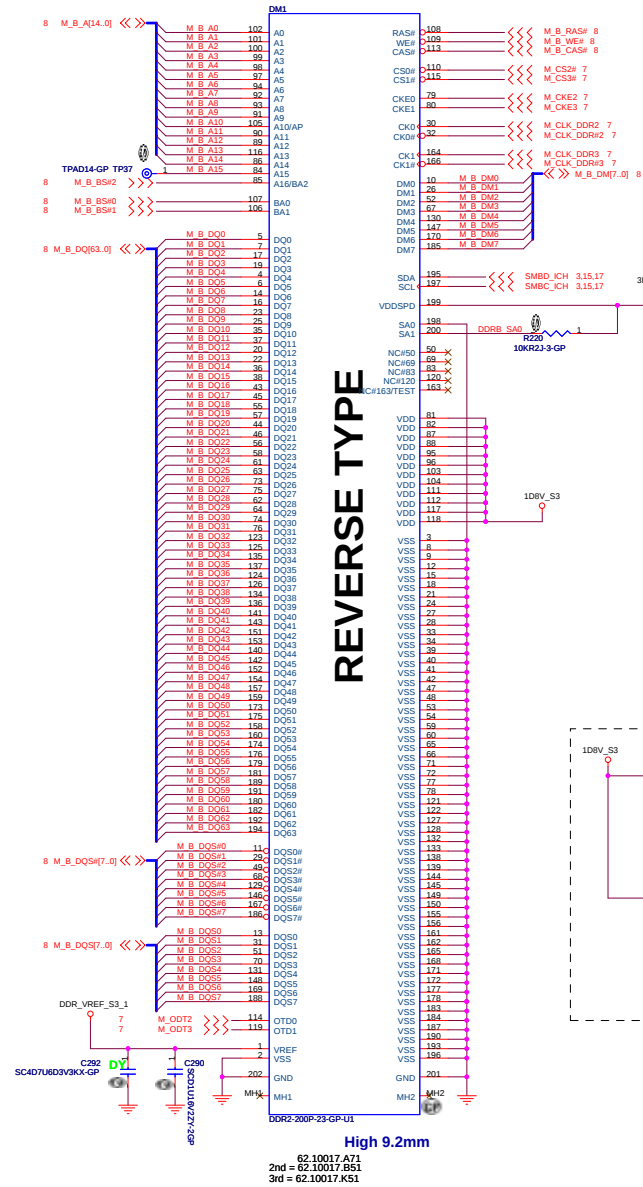
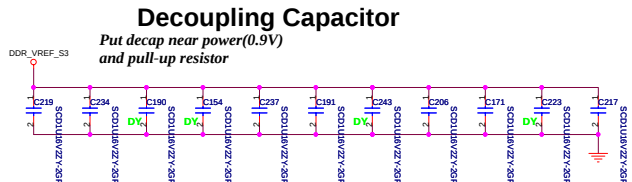
1017 modify USB signal connection





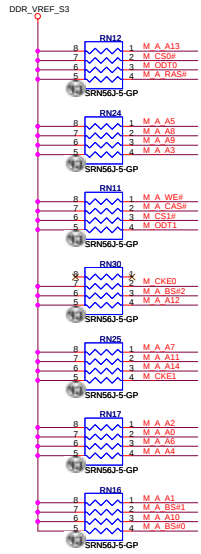


*Put decap near power(0.9V) and pull-up resistor*



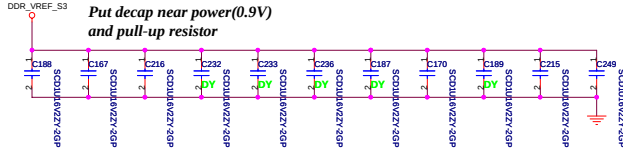
## PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

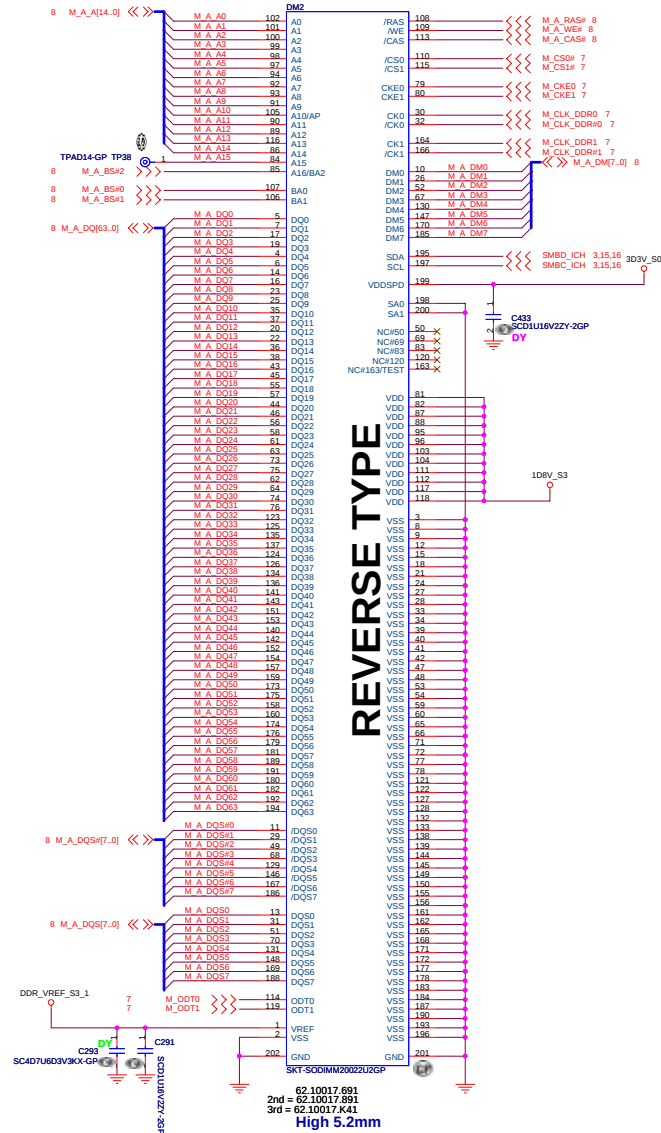
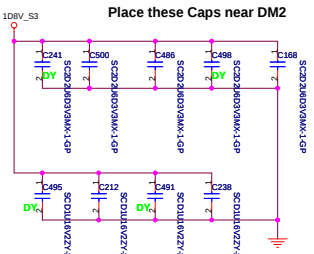


## Decoupling Capacitor

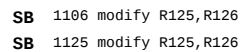
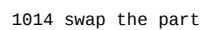
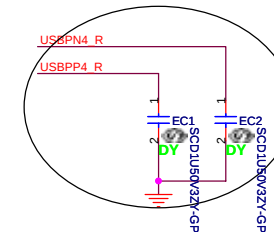
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM2



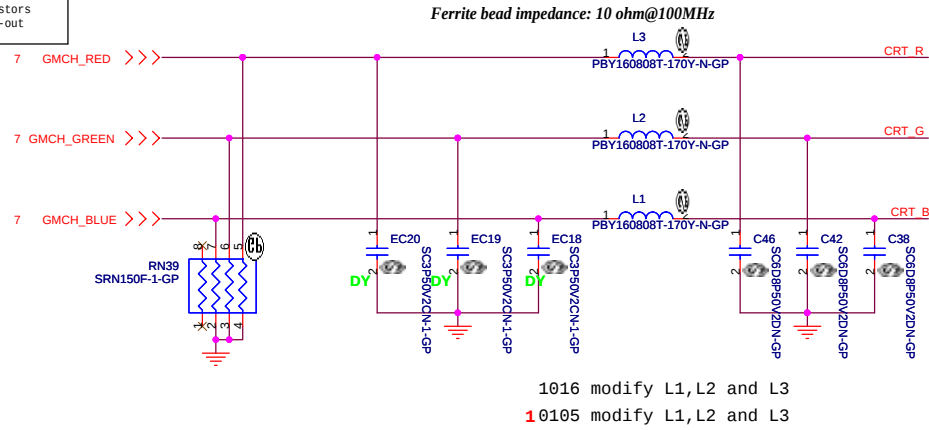
REVERSE TYPE



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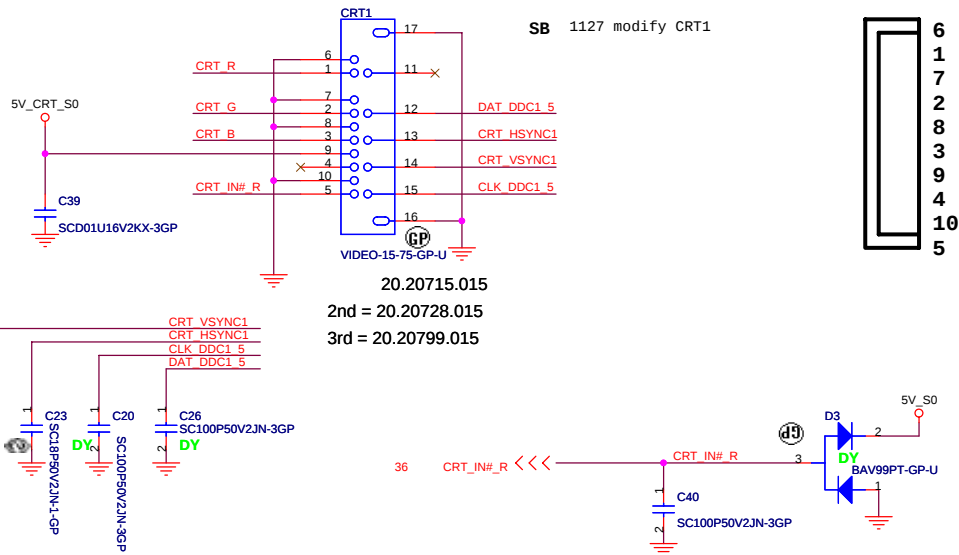
|                 |                        |             |           |
|-----------------|------------------------|-------------|-----------|
| Title           |                        |             |           |
| <b>LCD CONN</b> |                        |             |           |
| Size            | Document Number        |             | Rev       |
|                 | <b>LA14</b>            |             | <b>SB</b> |
| Date:           | Thursday, May 07, 2009 | Sheet 18 of | 52        |

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

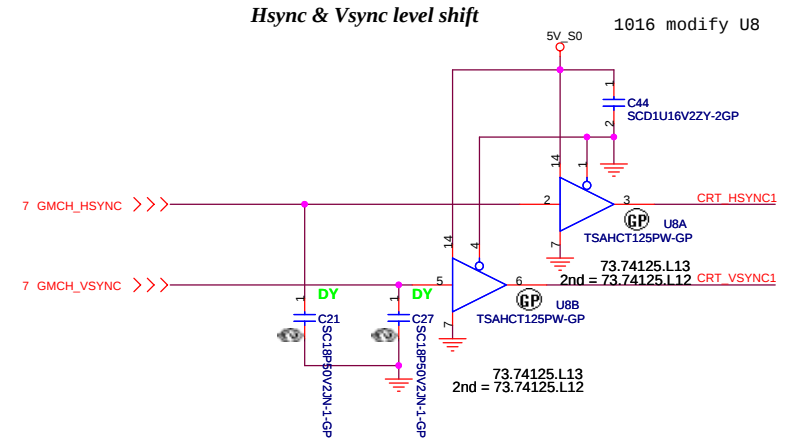


Layout Note:  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

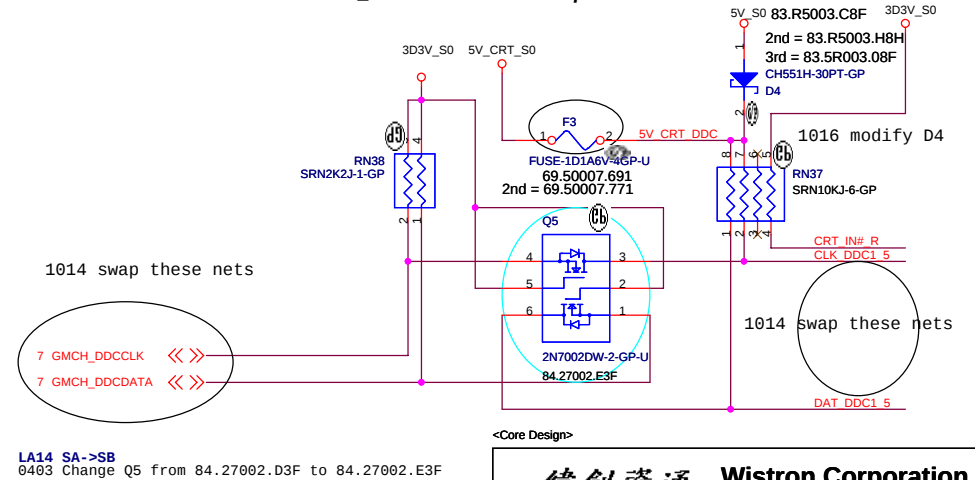
## CRT I/F & CONNECTOR



## Hsync & Vsync level shift



## DDC\_CLK & DATA level shift



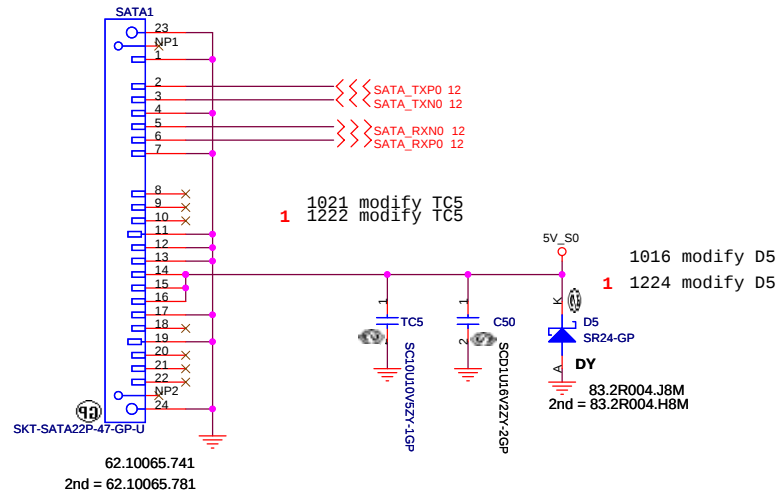
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|                              |                 |    |     |
|------------------------------|-----------------|----|-----|
| Title                        |                 |    |     |
| CRT Connector                |                 |    |     |
| Size                         | Document Number |    | Rev |
|                              | LA14            |    | SB  |
| Date: Thursday, May 07, 2009 | Sheet 19        | of | 52  |

# SATA Connector

0912 add these parts for EMI demand  
1001 delete these parts for EMI demand  
1021 modify SATA1



<Core Design>

|             |                        |                                                                                                             |           |
|-------------|------------------------|-------------------------------------------------------------------------------------------------------------|-----------|
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| Title       |                        |                                                                                                             |           |
| <b>HDD</b>  |                        |                                                                                                             |           |
| Size        | Document Number        |                                                                                                             | Rev       |
|             | <b>LA14</b>            |                                                                                                             | <b>SB</b> |
| Date:       | Thursday, May 07, 2009 | Sheet 20 of                                                                                                 | 52        |

5V\_S0

1 2

CS273

SCSDJUBVZZY-3GP

1

TC7

SCSDJUBVZZY-1GP

12 SATA\_TXP1

12 SATA\_TXN1

12 SATA\_RXP1

12 SATA\_RXN1

S2

S3

S6

S5

NP1

NP2

SGT-SATA7P+6P-73-GP

5120065881

1001 delete these parts for EMI dem

1230 modify ODD1

1231 modify ODD1

0113 modify ODD1

ODD1

P2 +5V

P3 +5V

DP

P1 ODD\_DP

P4 ODD\_MD

TP40 TPAD14-GP

TP39 TPAD14-GP

S1

S4

S7

P5

P6

8

9

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|       |                        |             |    |
|-------|------------------------|-------------|----|
| Title |                        |             |    |
| ODD   |                        |             |    |
| Size  | Document Number        | Rev         |    |
|       | LA14                   |             | SB |
| Date: | Thursday, May 07, 2009 | Sheet 21 of | 52 |

D



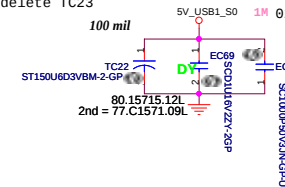
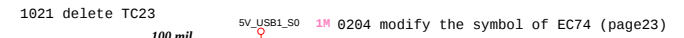
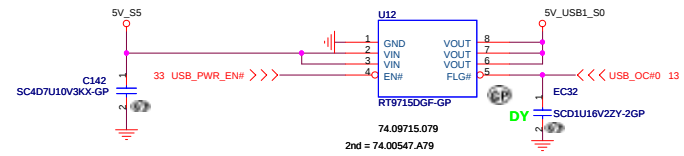
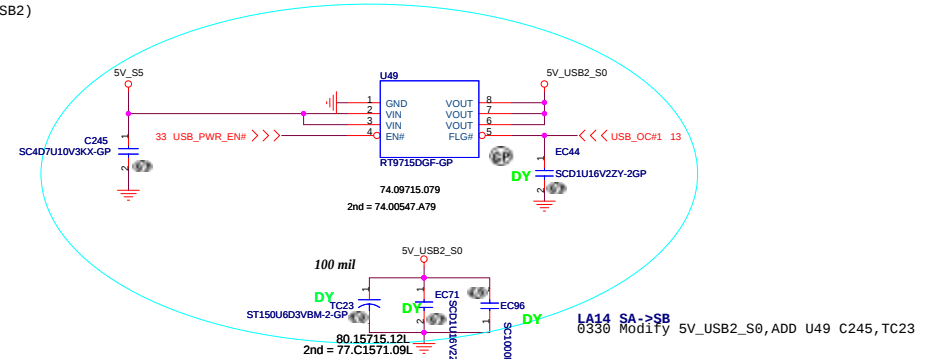
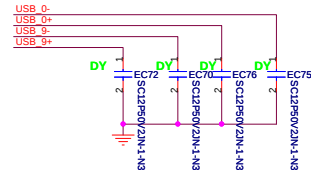
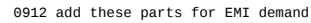
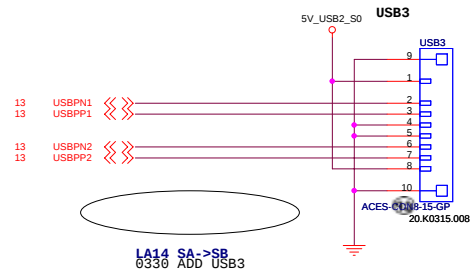
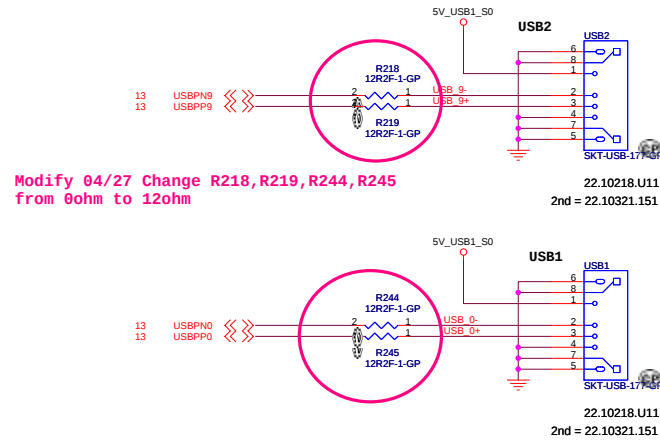
B

A

1

|                  |                        |             |           |
|------------------|------------------------|-------------|-----------|
| Title            |                        |             |           |
| <b>Bluetooth</b> |                        |             |           |
| Size             | Document Number        |             | Rev       |
|                  | <b>LA14</b>            |             | <b>SB</b> |
| Date:            | Thursday, May 07, 2009 | Sheet 22 of | 52        |

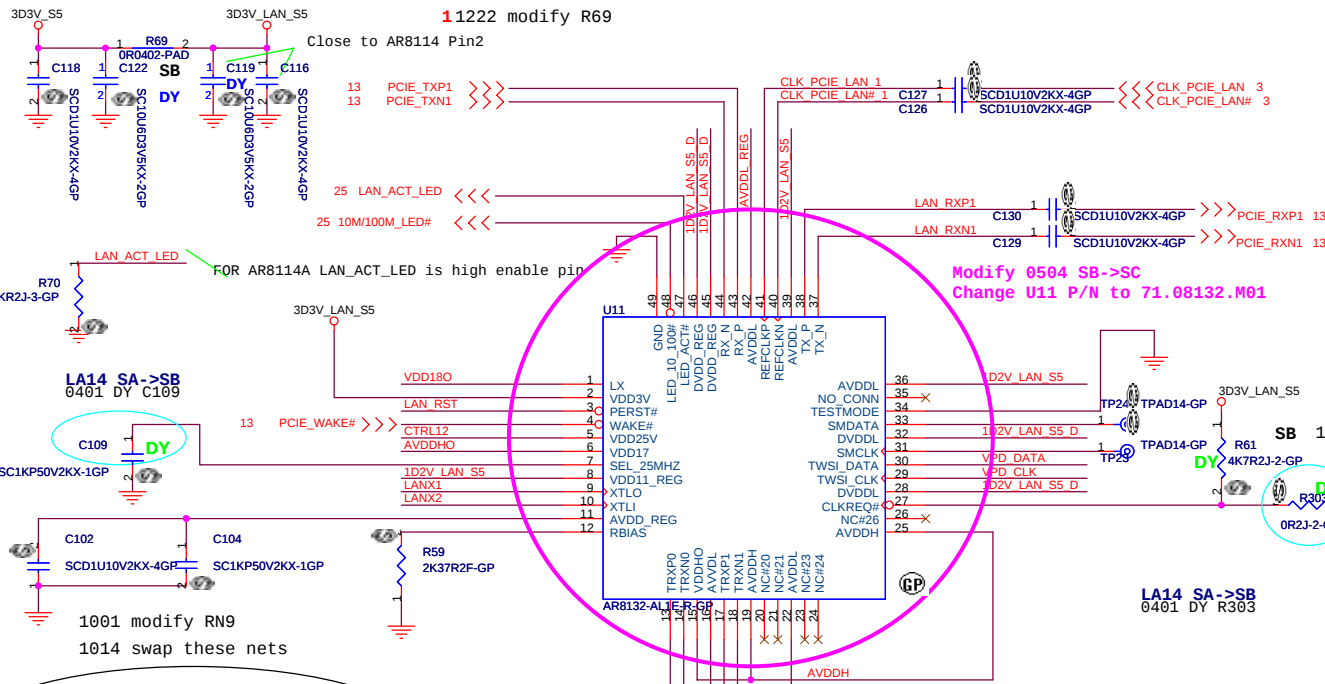
```
1017 modify USB signal connection
1021 modify and swap these parts(USB1 and USB2)
```



1015 modify component size of R69

11222 modify R69

Close to AR8114 Pin2

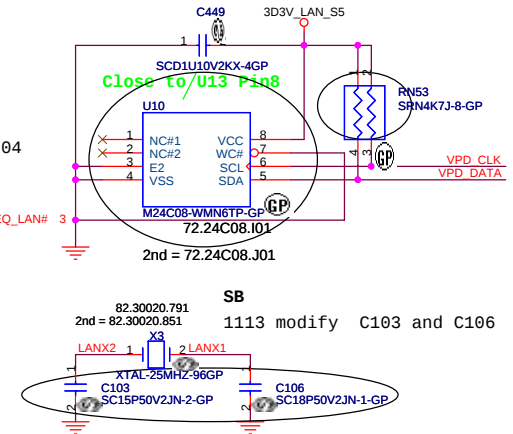


AR8132 use 0 ohm resiter

AR8114A Atheros suggestion change to Bead  
60 ohms/100Mhz 500mA (68.60090.0D1)

1224 modify R71

1016 modify RN53 and U10



```
1 1222 modify R68
```

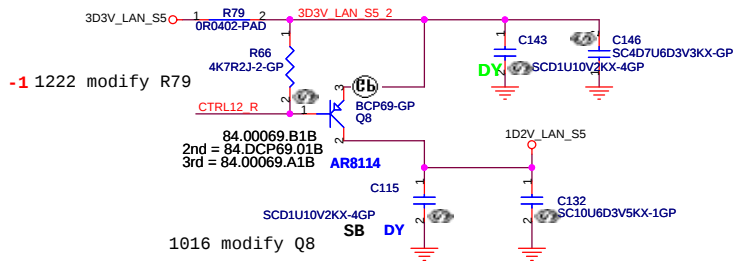


AR8114 use 0ohm resister

AR8132 Atheros suggest to change 4.7uH choke

```
1 1229 modify L19
```

```
1015 modify component size of R79
```



**SB**  
1128 Add L19

Close to AR8114 Pin1

1016 modify Q8

```
1
1224 modifyv R67
```

Atheros suggestion change to Bead  
60 ohms/100Mhz 500mA (68.60090.00D1)

1224 add R307 and R308

Close to AR8114 Pin6

Close to AR8114 Pin28  
Close to AR8114 Pin32  
Close to AR8114 Pin45  
Close to AR8114 Pin46

Close to AR8114 Pin8  
Close to AR8114 Pin16  
Close to AR8114 Pin22  
Close to AR8114 Pin36  
Close to AR8114 Pin39

<Core Design>

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|       |                            |
|-------|----------------------------|
| Title | <b>Atheros AR8114/8132</b> |
|-------|----------------------------|

|            |                 |
|------------|-----------------|
| Size<br>A3 | Document Number |
|------------|-----------------|

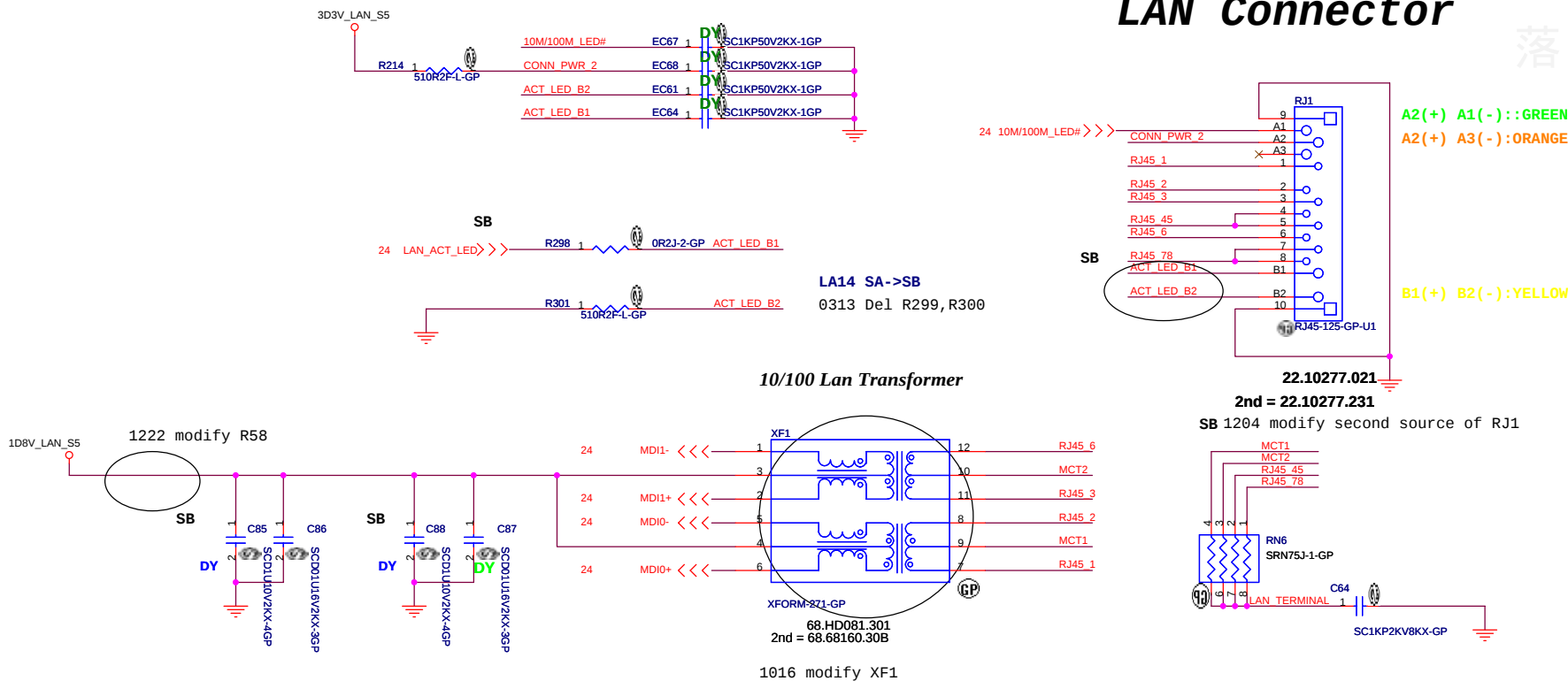
**LA14**

Date: Thursday, May 07, 2009

Sheet 24 of 52

# LAN Connector

落



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

**RJ11 signal must leave the other signal or power plane 100mil.**

DOC\_TIP,DOC\_RING,TIP,RING:  
W/S : 10/100 @ Surface layers  
10/20 @ Inner layers

| 10/100 LAN Transformer | RJ45 PIN |
|------------------------|----------|
| TD+ --> TX+            | RJ45-1   |
| TD- --> TX-            | RJ45-2   |
| RD+ --> RX+            | RJ45-3   |
| RD- --> RX-            | RJ45-6   |

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|                              |                 |     |
|------------------------------|-----------------|-----|
| Title                        |                 |     |
| LAN Connector                |                 |     |
| Size                         | Document Number | Rev |
| A3                           | LA14            | SB  |
| Date: Thursday, May 07, 2009 | Sheet 25 of 52  |     |

SB 1118 delete C245 and C270

0911 add net name(DVDD\_1\_8)

0911 add net name(ACZ\_SDATAIN0\_R)

SB 1126 add C541 and modify R101

0121 add R310

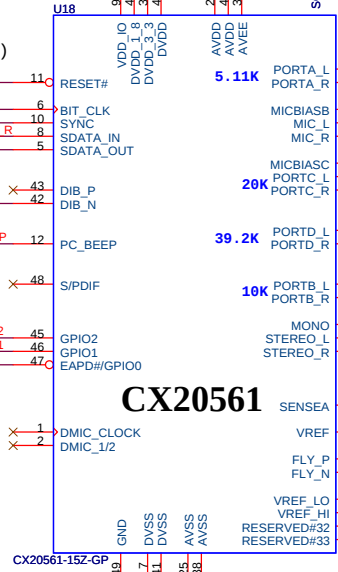
EAPD# <<<

## PC BEEP GAIN CONTROL

Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.

0912 add the part for EMI demand

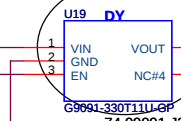
| GAIN  | 10K GPIO RESISTORS |          |
|-------|--------------------|----------|
|       | R105               | R106     |
| 0dB   | Populate           | Populate |
| -6dB  | Omit               | Omit     |
| -12dB | Populate           | Omit     |
| -18dB | Omit               | Populate |



CX20561

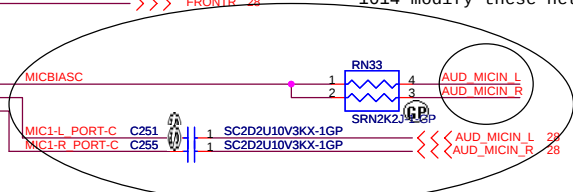
68.00119.081  
2nd = 68.00230.021  
1001 Add R107  
SB 1113 modify 2nd of U19  
SB 1118 delete R107 and add L18

SC1U10V3KX-3GP



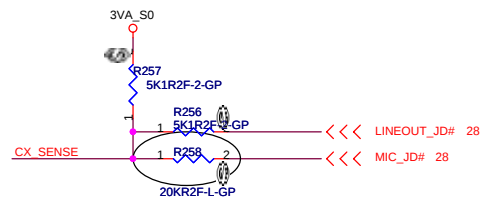
1113 modify 2nd of U19

1014 swap these nets  
1014 modify these nets



1230 dummy C507

0911 add net name(FLY\_P, FLY\_N, VREF\_LO, VREF\_HI)

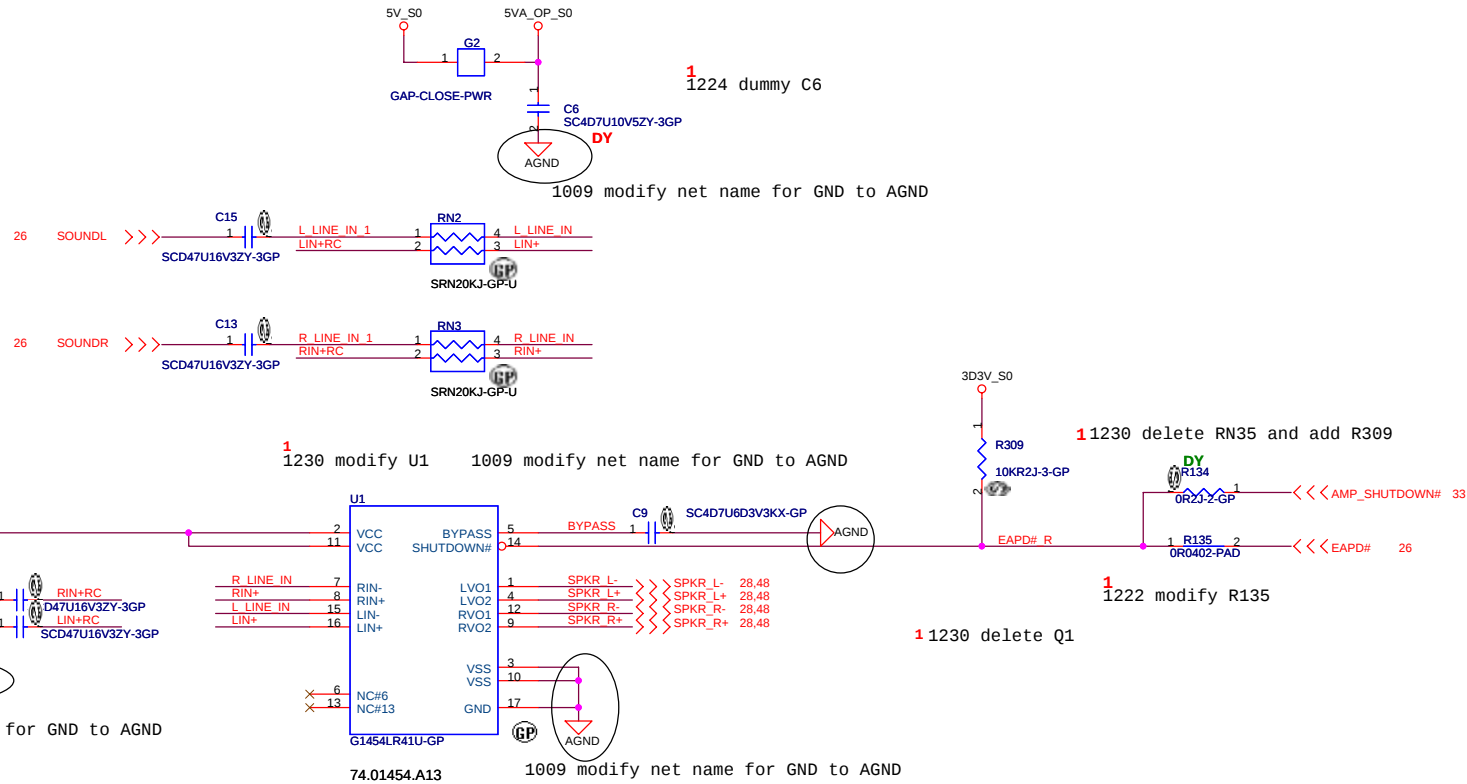


1014 modify R258 from 10k to 20k ohm

<Core Design>

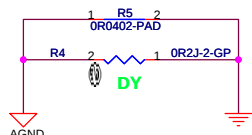
# AUDIO OP AMPLIFIER

落

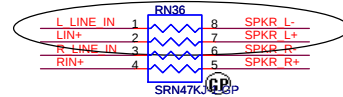


## AC decoupling

1222 modify R5



1014 swap these nets



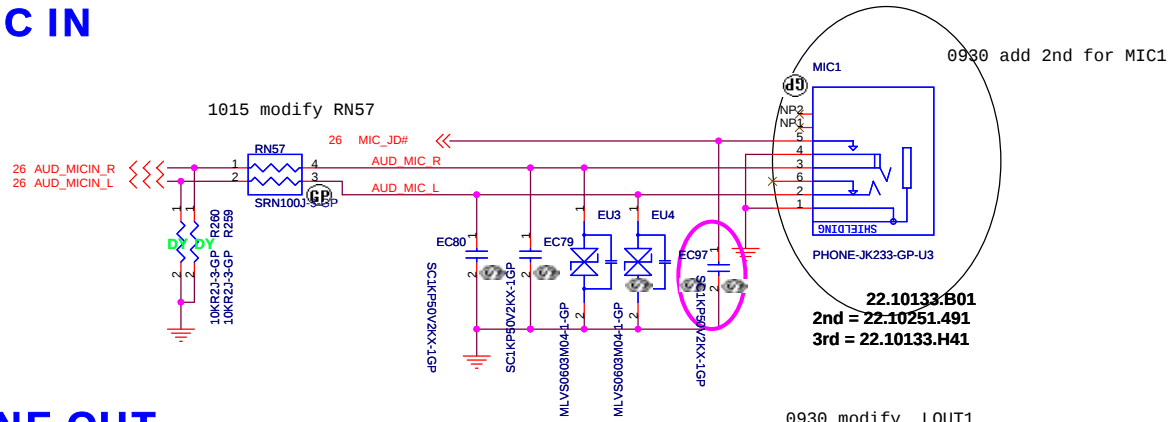
SB 1204 modify RN36

<Core Design>

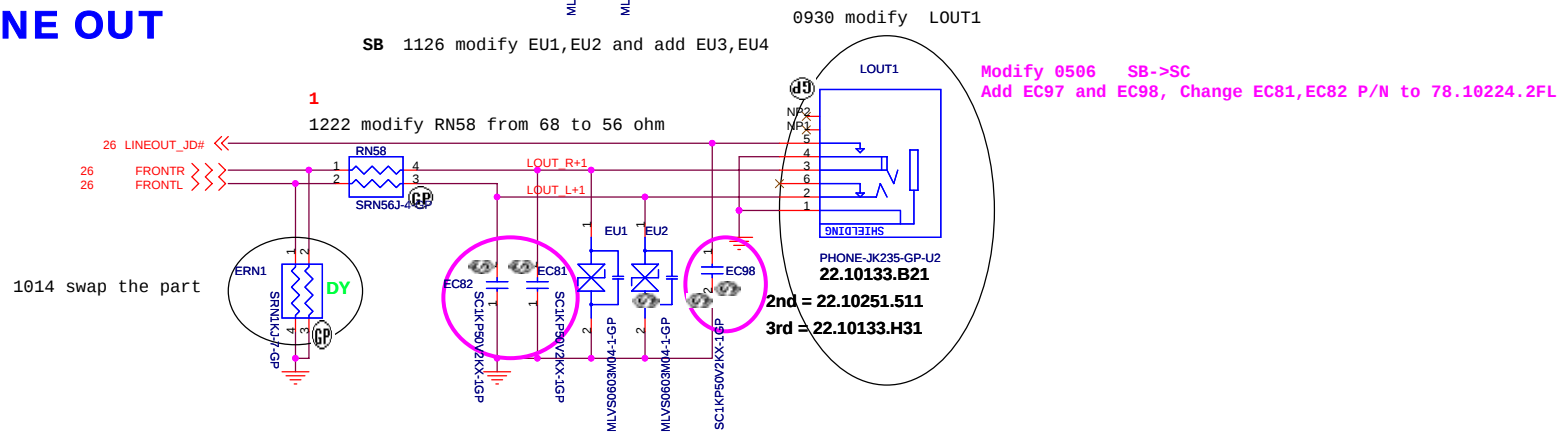
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Taipei Hsien 221, Taiwan, R.O.C.

|                              |                 |             |     |
|------------------------------|-----------------|-------------|-----|
| Title                        |                 |             |     |
| AUDIO AMP                    |                 |             |     |
| Size                         | Document Number |             | Rev |
|                              | LA14            |             | SB  |
| Date: Thursday, May 07, 2009 |                 | Sheet 27 of | 52  |

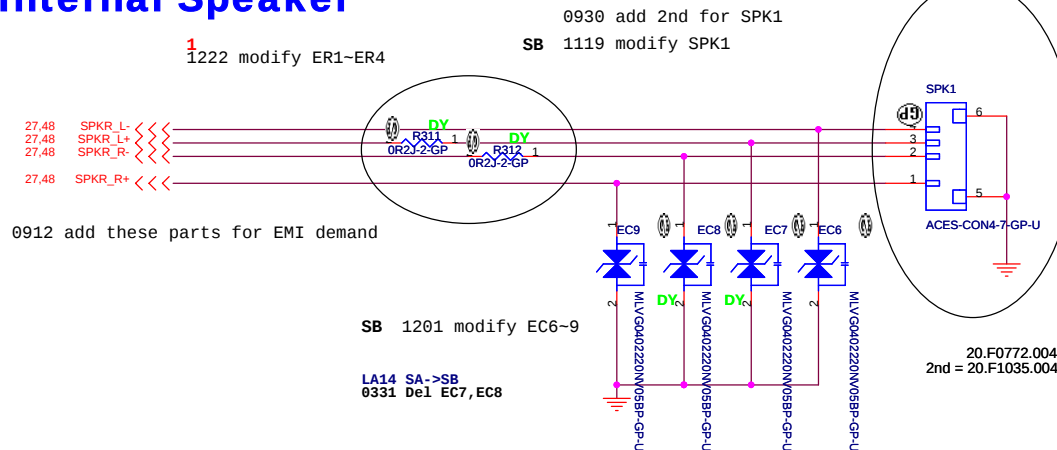
## MIC IN



## LINE OUT



## Internal Speaker



<Core Design>

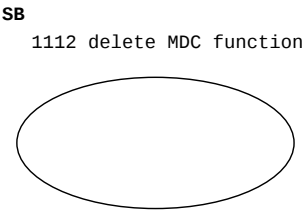
緯創資通

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| Title                        |                 |      | Rev |
|------------------------------|-----------------|------|-----|
| AUDIO JACK                   |                 |      | SB  |
| Size                         | Document Number | LA14 |     |
| Date: Thursday, May 07, 2009 | Sheet 28        | of   | 52  |

# MDC 1.5 CONN

0912 add the part for EMI demand  
1002 modify MDC1



<Core Design>

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Title

MDC

Size

Document Number

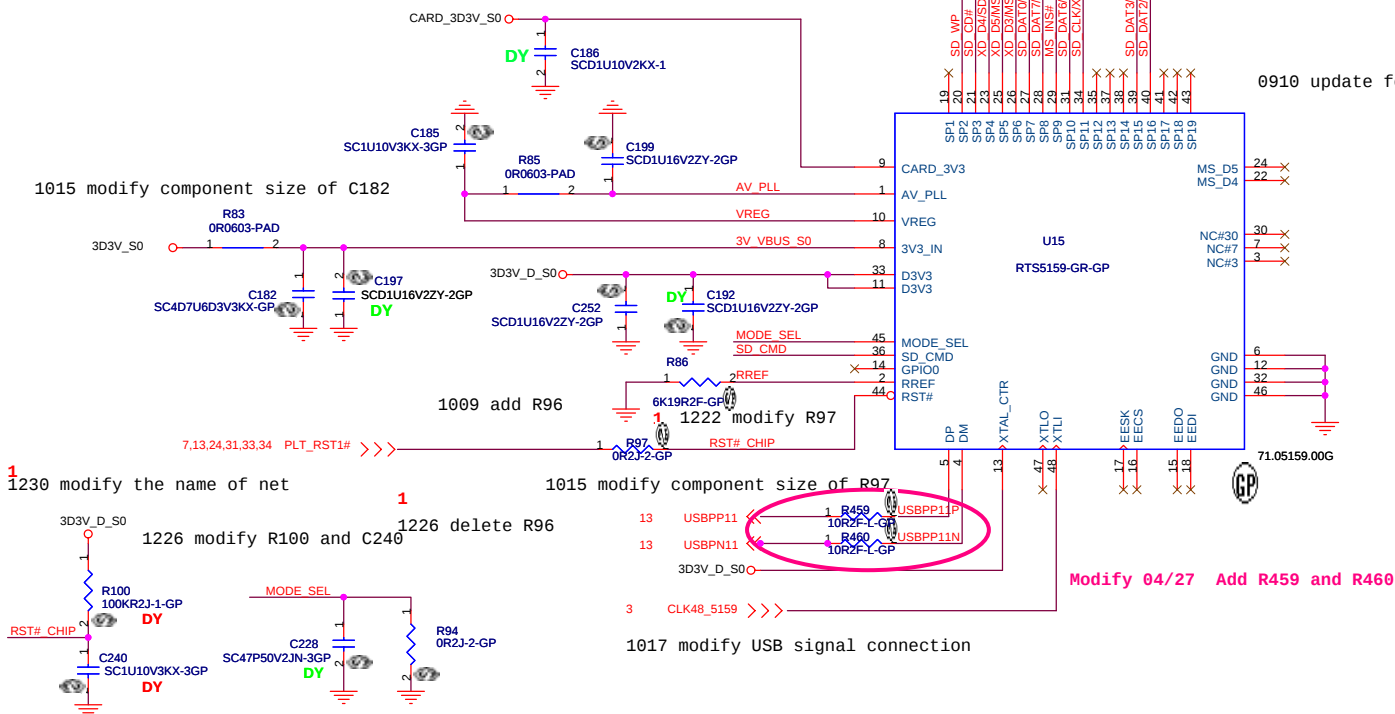
Rev

LA14

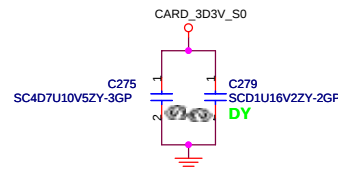
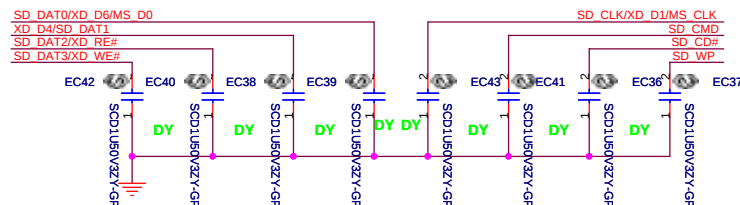
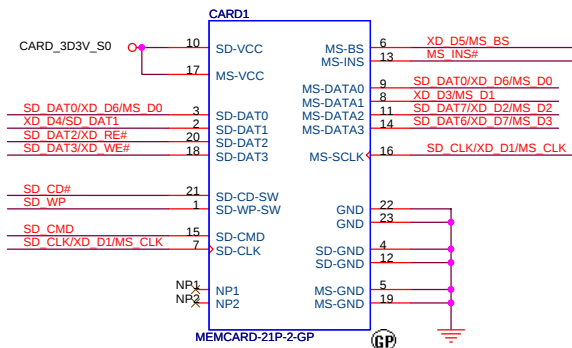
SB

Date: Thursday, May 07, 2009

Sheet 29 of 52



### 3 IN1 CARD-READER (SD/MMC/MS)



<Core Design>

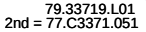
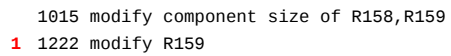
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|                             |                        |       |          |
|-----------------------------|------------------------|-------|----------|
| Title                       |                        |       |          |
| <b>CARD READER- RTS5159</b> |                        |       |          |
| Size                        | Document Number        |       | Rev      |
|                             | <b>LA14</b>            |       | <b>S</b> |
| Date:                       | Thursday, May 07, 2009 | Sheet | 30 of 52 |

```

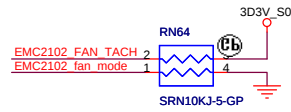
1009 modify this net
1013 modify card1
1 1222 modify card1 from 20.I0043.001 to 20.I0043.011
1 1229 modify card1
LA14 SA 0217 modify card1 from 20.I0043.011 to 20.I0033.021

```



Sheet 31 of 52

1224 delete R165 and add RN64



0930 modify FAN1  
1017 modify FAN1  
1224 modify FAN1

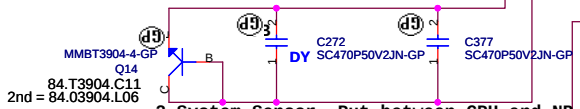
1222 modify U42

GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected

4 H\_THERMDC >>>  
4 H\_THERMDA <<<

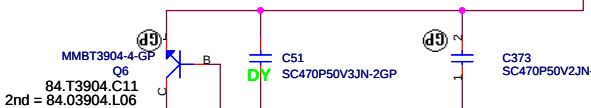
### 1.For CPU Sensor

CC272 must be near Q7  
C377 must be near EMC2102



### 2.System Sensor, Put between CPU and NB.

Layout notice : Both EMC2102\_DN2 and EMC2102\_DP2 routing  
10 mil trace width and 10 mil spacing



### 3.HW T8 sensor

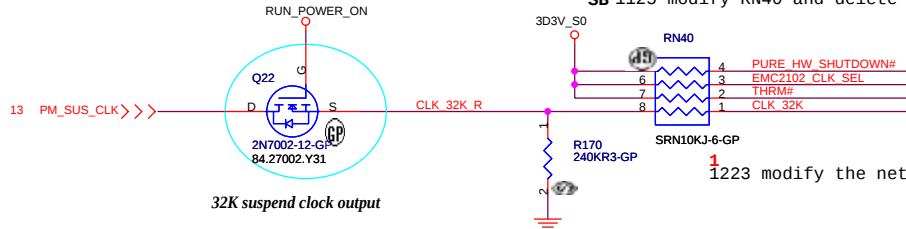
Layout notice : Both EMC2102\_DN3 and EMC2102\_DP3 routing  
10 mil trace width and 10 mil spacing

C51 must be near Q8  
C373 must be near EMC2102

PIN9 = Channel 1  
GND = Channel 3  
+3.3V = Disabled

PIN10 = Fan is OFF  
GND = Fan is at 60% full-scale  
+3.3V = Fan is at 75% full-scale

SB 1125 modify RN40 and delete RN42



1223 modify the net(EMC2102\_CLK\_SEL)

LA14 SA->SB  
0403 Change Q21,Q22 from 84.27002.W31 to 84.27002.Y31

13.41 VGATE\_PWRGD >>>



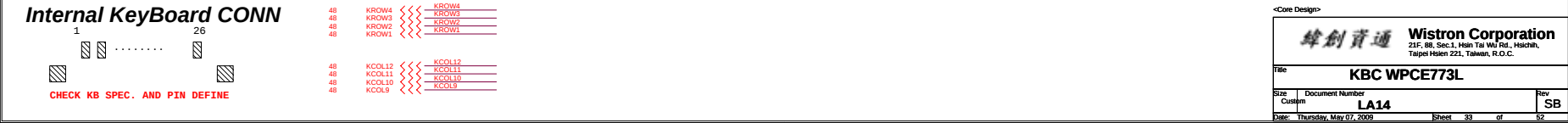
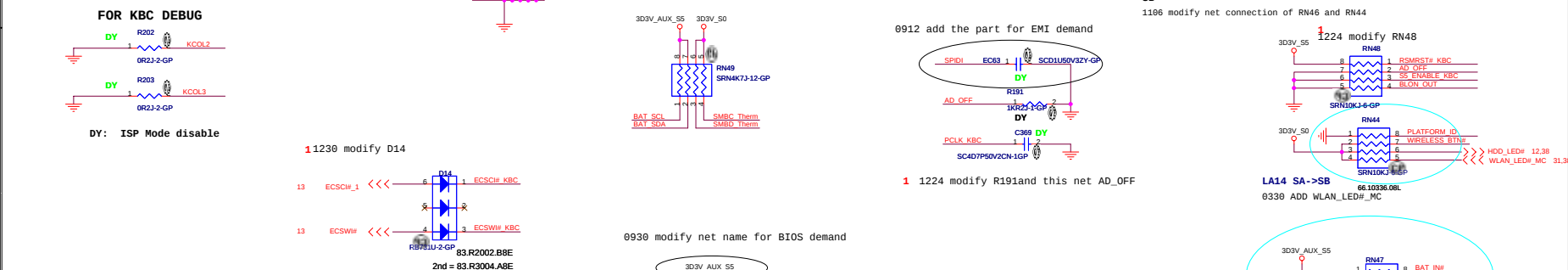
(dummy, KBC already delay)

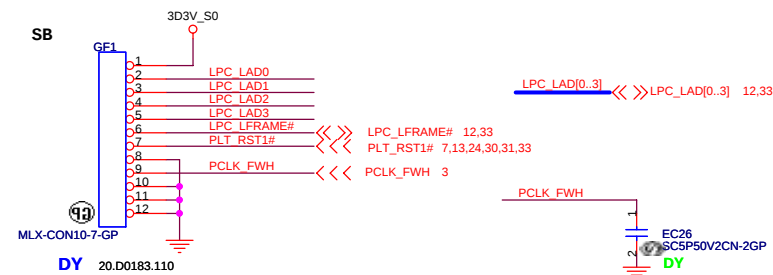
C335 DY  
SCD1U16V2ZY-2GP

<Core Design>

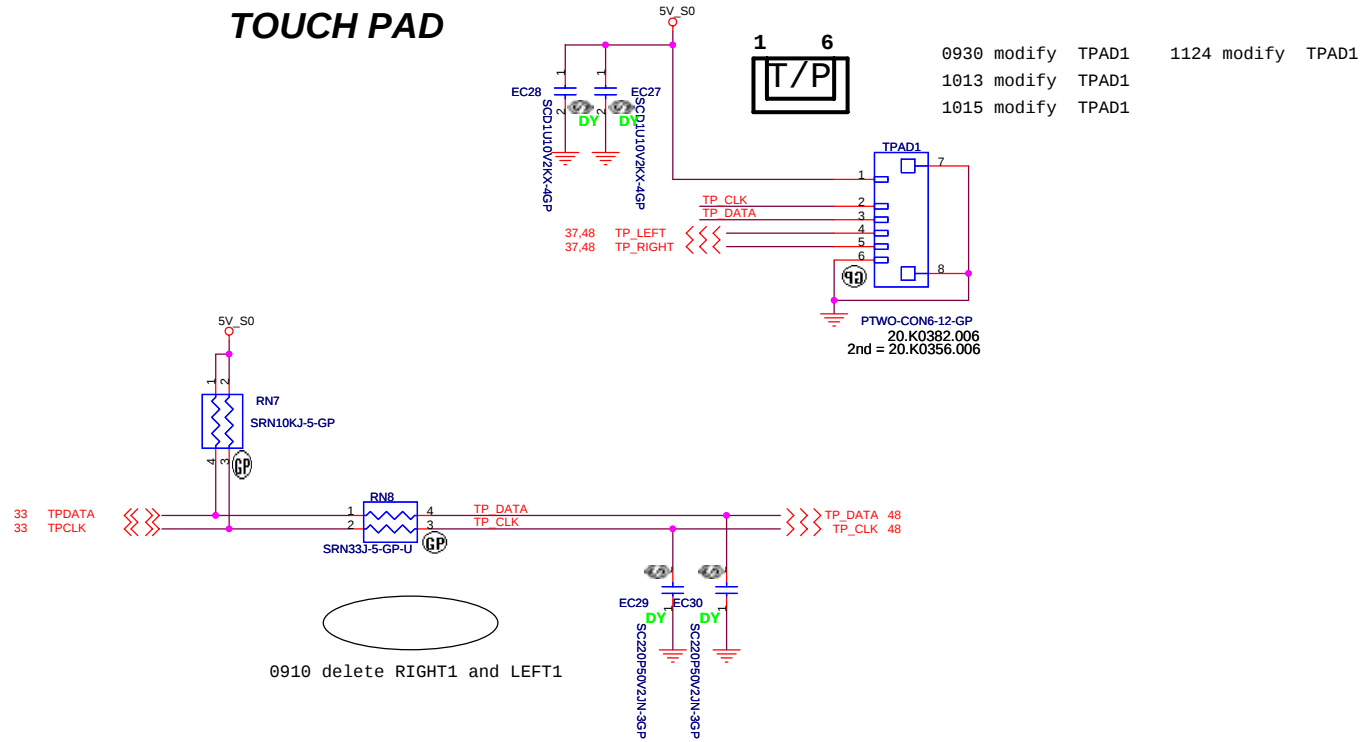
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|                              |                 |                |     |
|------------------------------|-----------------|----------------|-----|
| Title                        |                 |                |     |
| Thermal/Fan Controller       |                 |                |     |
| Size                         | Document Number |                | Rev |
|                              | LA14            |                | SB  |
| Date: Thursday, May 07, 2009 |                 | Sheet 32 of 52 |     |





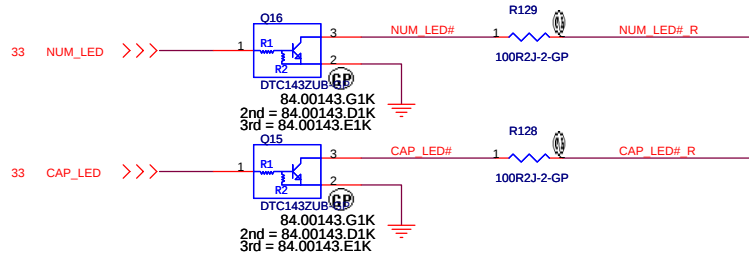
# TOUCH PAD



<Core Design>

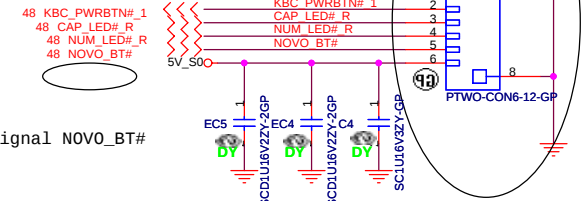
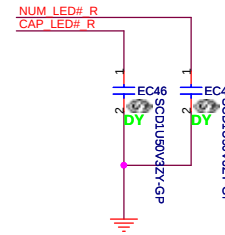
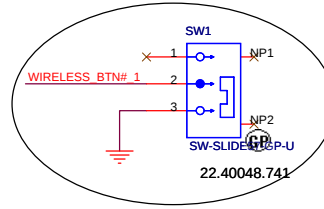
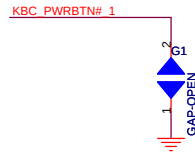
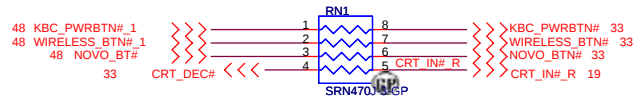
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|                              |                 |     |           |
|------------------------------|-----------------|-----|-----------|
| Title                        |                 |     | Touch pad |
| Size                         | Document Number | Rev | SB        |
|                              | LA14            |     |           |
| Date: Thursday, May 07, 2009 | Sheet 35        | of  | 52        |



LA14\_SA

0205 remove signals(TP\_LOCK\_LED,TP\_LOCK\_LED#,TP\_LOCK\_LED#\_R)and R132,Q17



LA14\_SA

0205 ADD signal NOVO\_BTN#

LA14\_SA

0205 modify POWERCN1 from 20.K0384.016 to 20.K0204.006

0223 modify POWERCN1 from 20.K0204.006 to 20.K0382.006

LA14\_SA

0205 remove EC49

<Core Design>

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Title

**Power Board**

Size

Document Number

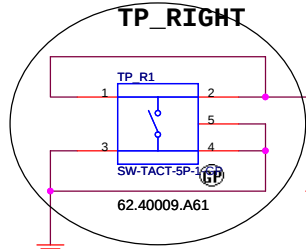
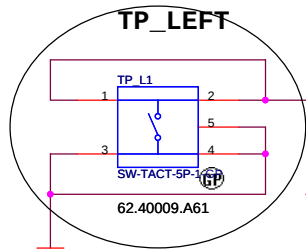
**LA14**

Rev

**SB**

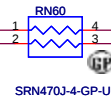
Date: Thursday, May 07, 2009

Sheet 36 of 52



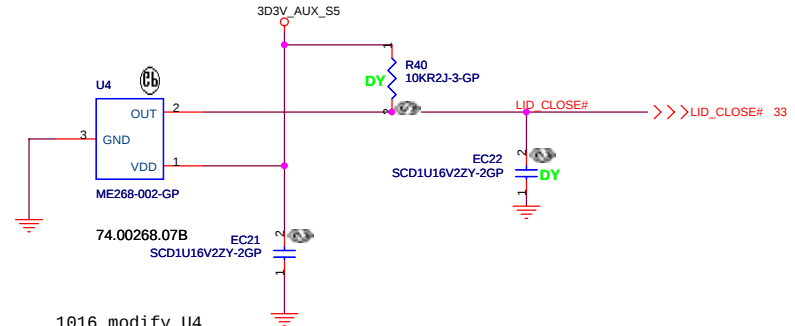
1  
1226 modify TP\_L1 and TP\_R1

1017 modify RN60



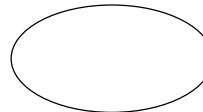
TP\_LEFT 35,48  
TP\_RIGHT 35,48

## Cover Up Switch



1016 modify U4  
1017 modify U4

1017 add U61,R52,EC24 and EC23  
1020 delete U61,R52,EC24 and EC23



<Core Design>

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Title

**SWITCHS**

Size

Document Number

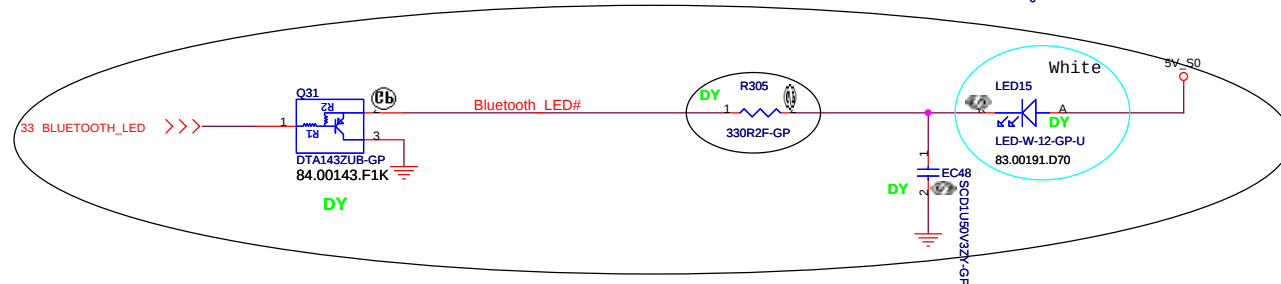
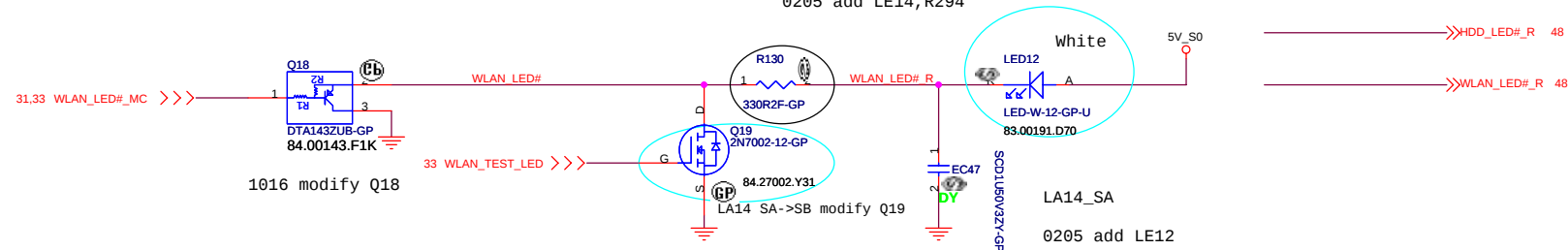
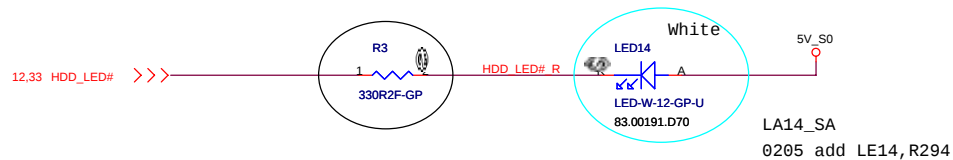
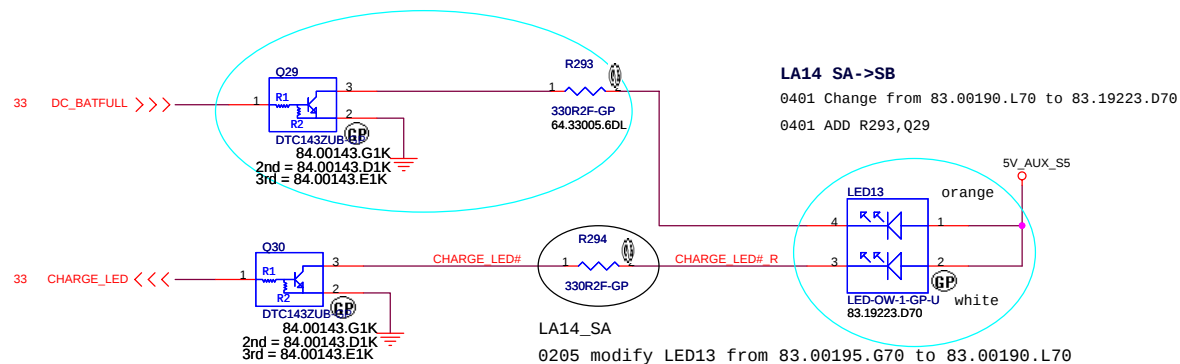
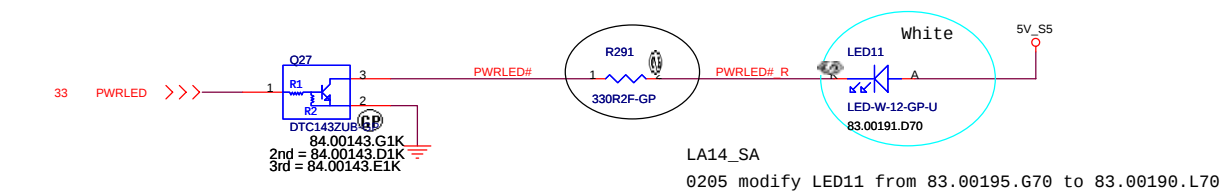
**LA14**

Rev

**SB**

Date: Thursday, May 07, 2009

Sheet 37 of 52



LA14\_SA

0209 Change R305,R291,R294,R130,R3 from 29L2589AA to 64.33005.6DL

LA14 SA->SB

0331 Change LED11,LED12,LED14,LED15 from 83.19213.H70 to 83.00191.D70

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|     | Title |
|-----|-------|
| 1   |       |
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**LED**

Size

|                 |
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| Document Number |
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LA14

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|-----|
| Rev |
|-----|

Date: Thursday, May 07, 2009

Sheet 38

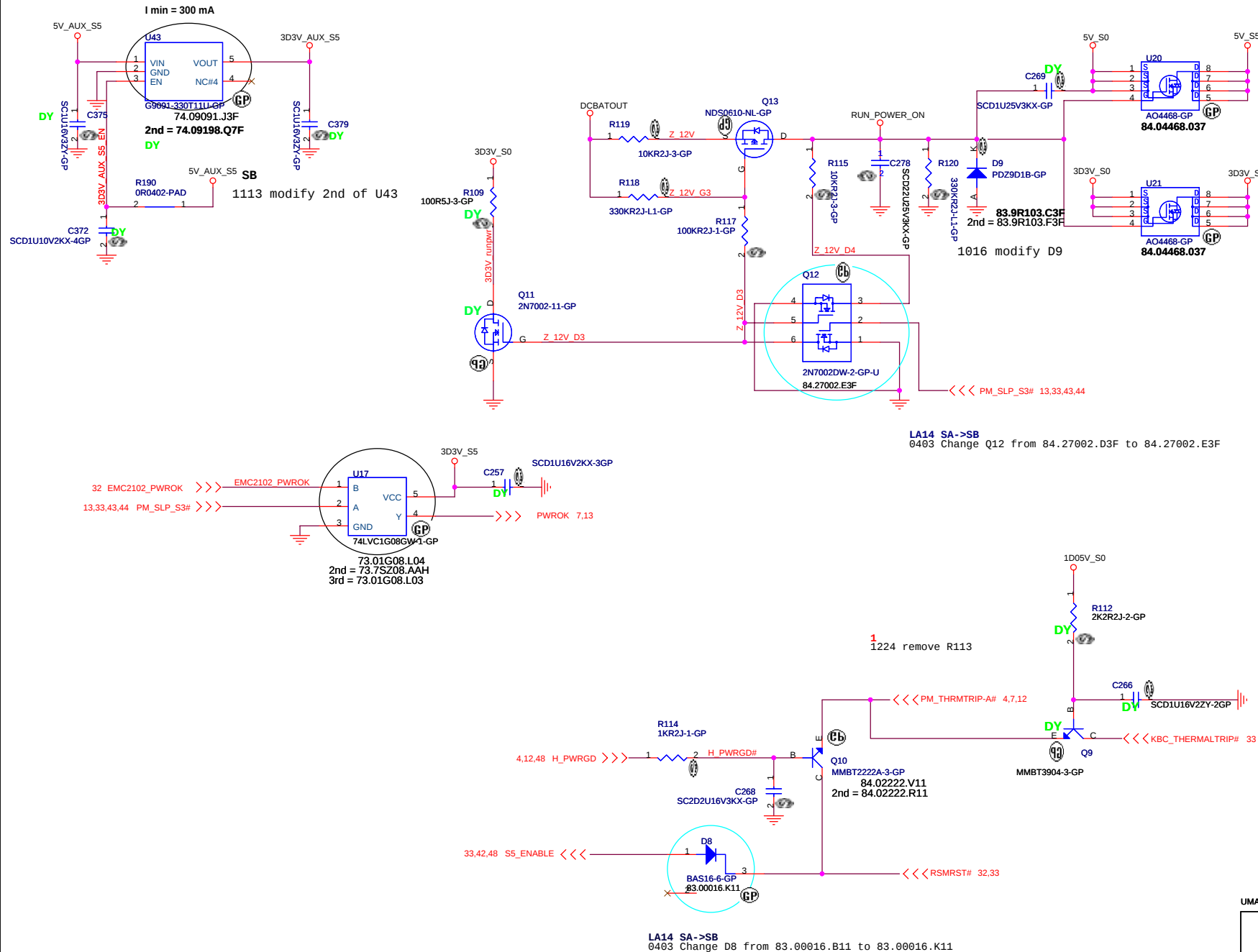
1 3

52

# Aux Power 3D3V\_AUX\_S5

# Run Power

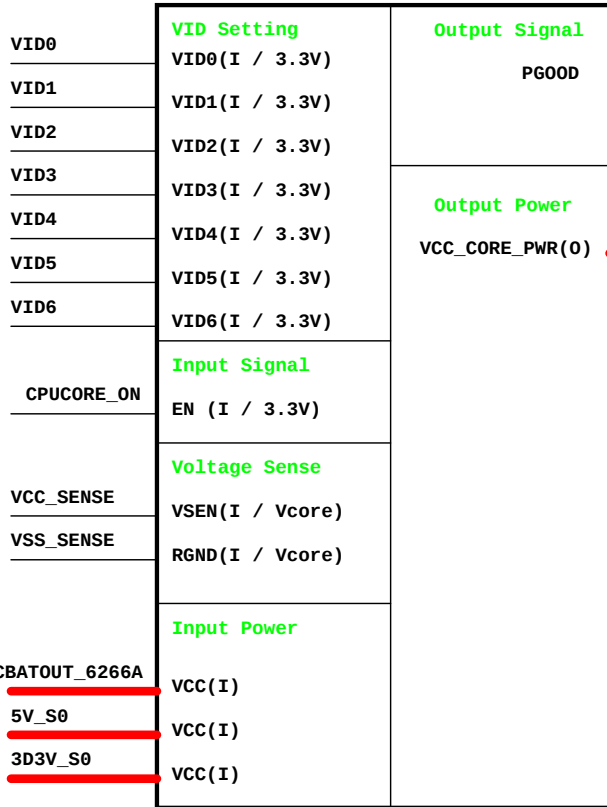
落



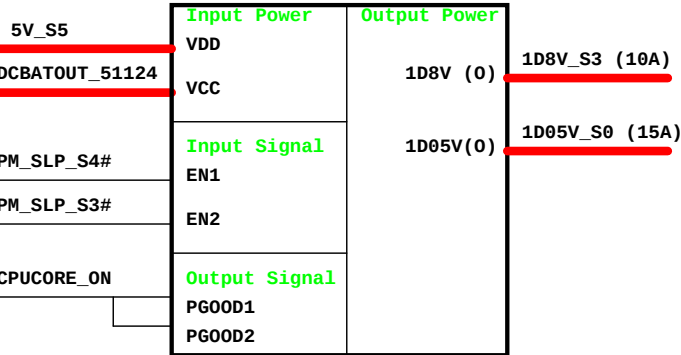
UMA Two Phase

|                                  |                        |                                                                               |           |
|----------------------------------|------------------------|-------------------------------------------------------------------------------|-----------|
| <b>緯創資通</b>                      |                        | <b>Wistron Corporation</b>                                                    |           |
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| Title                            |                        |                                                                               |           |
| <b>RUN POWER and 3D3V_AUX_S5</b> |                        |                                                                               |           |
| Size                             | Document Number        |                                                                               | Rev       |
|                                  | <b>LA14</b>            |                                                                               | <b>SB</b> |
| Date:                            | Thursday, May 07, 2009 | Sheet 39 of 52                                                                |           |

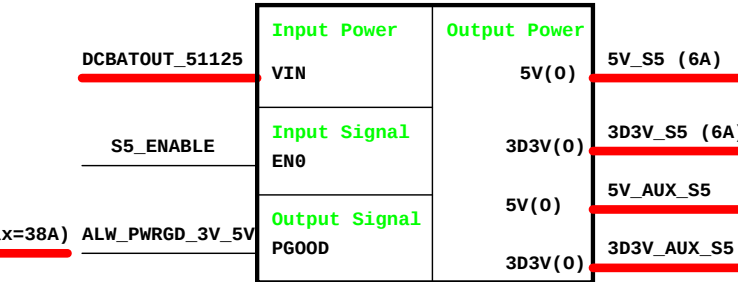
CPU\_CORE  
ISL6266A



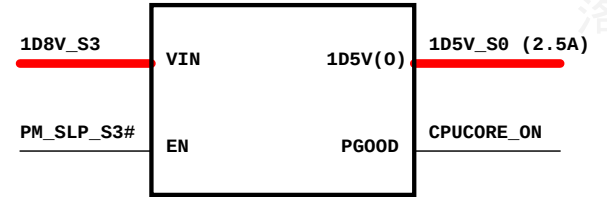
TPS51124  
1D8V/1D05V



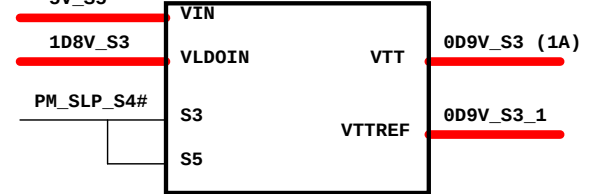
TPS51125  
5V/3D3V



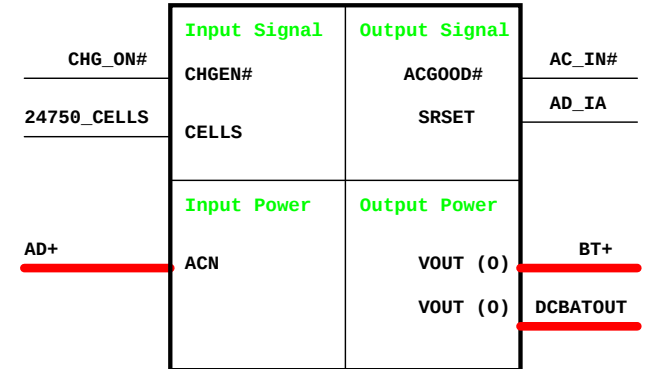
RT9018A  
1D5V\_S0



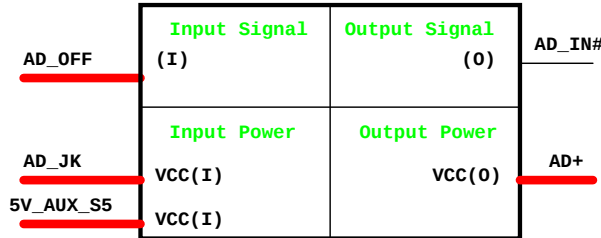
RT9026  
0D9V\_S0



Charger BQ24745



Adapter

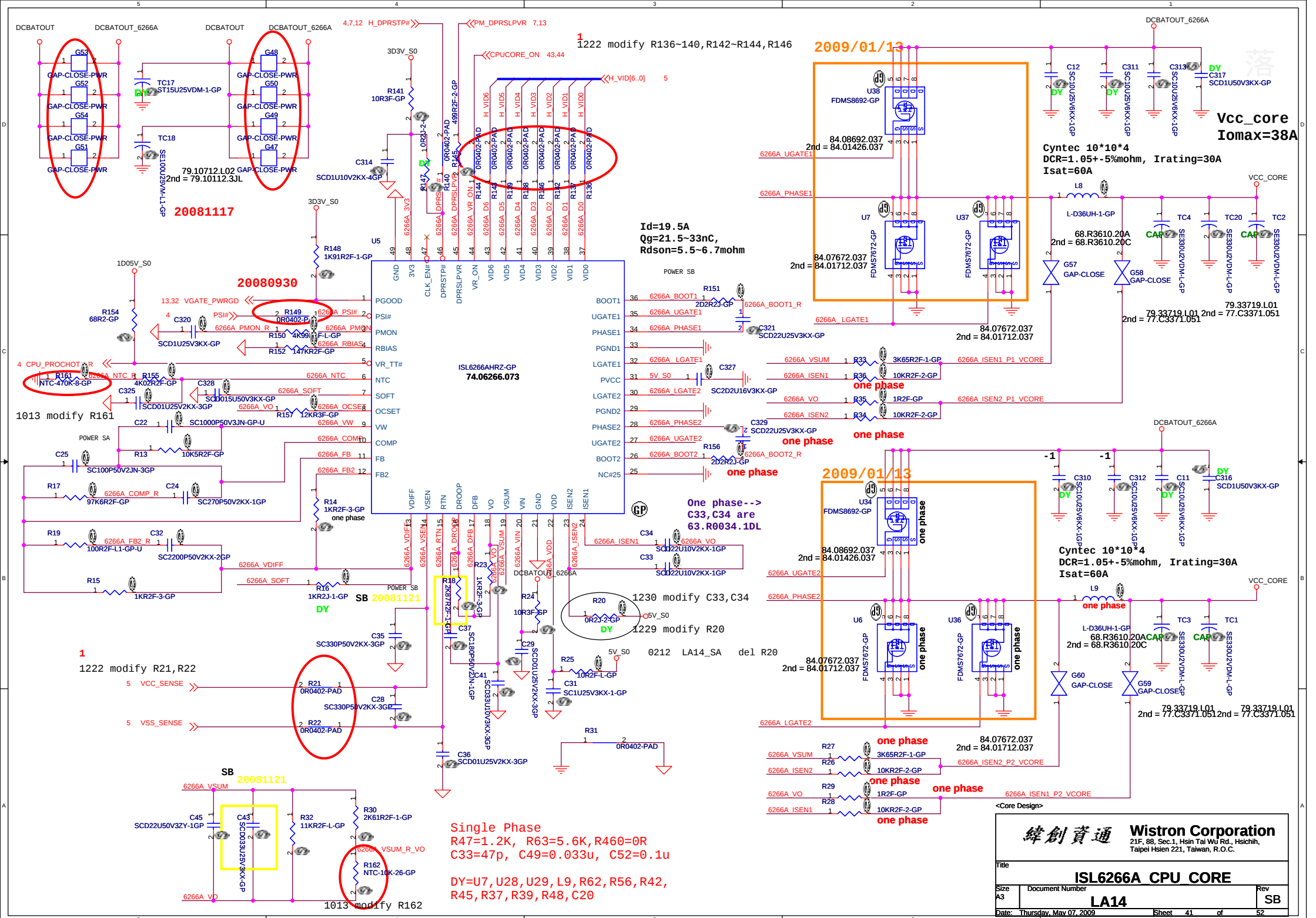


<Core Design>

緯創資通

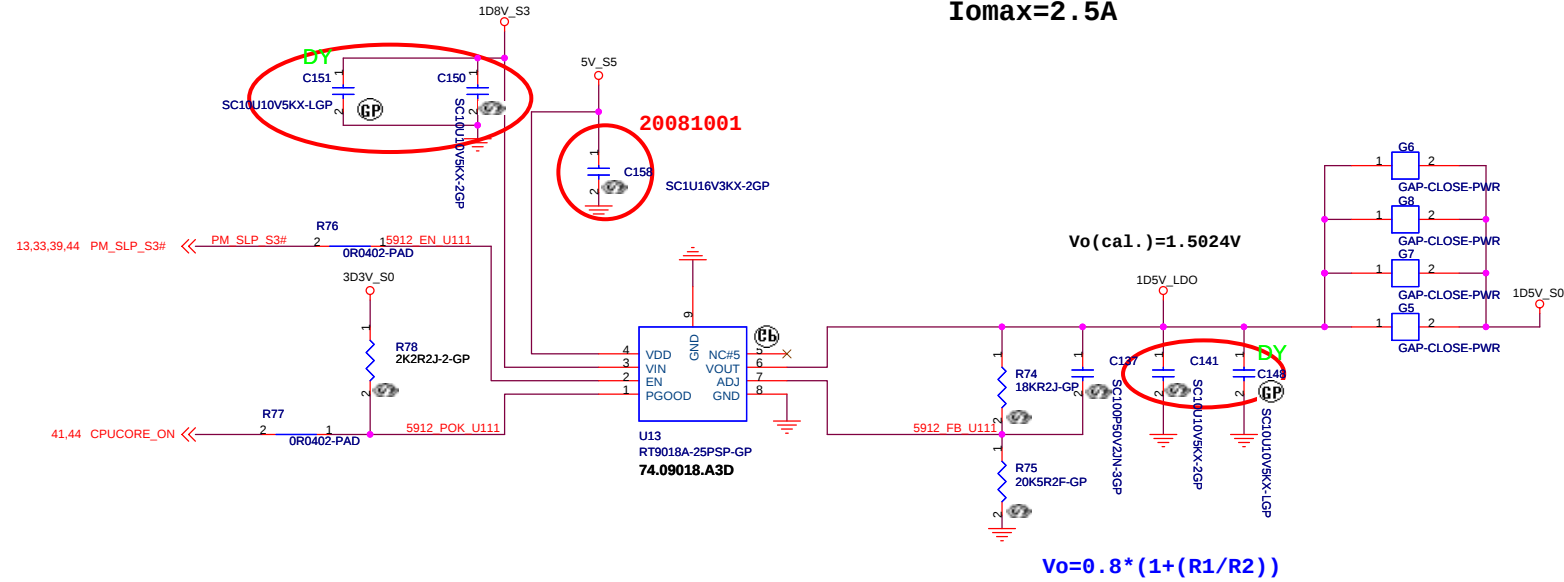
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|                              |                 |      |                      |        |
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| Title                        |                 |      | Power Sequence Logic |        |
| Size B                       | Document Number | LA14 |                      | Rev SB |
| Date: Thursday, May 07, 2009 | Sheet 40        | of   | 52                   |        |



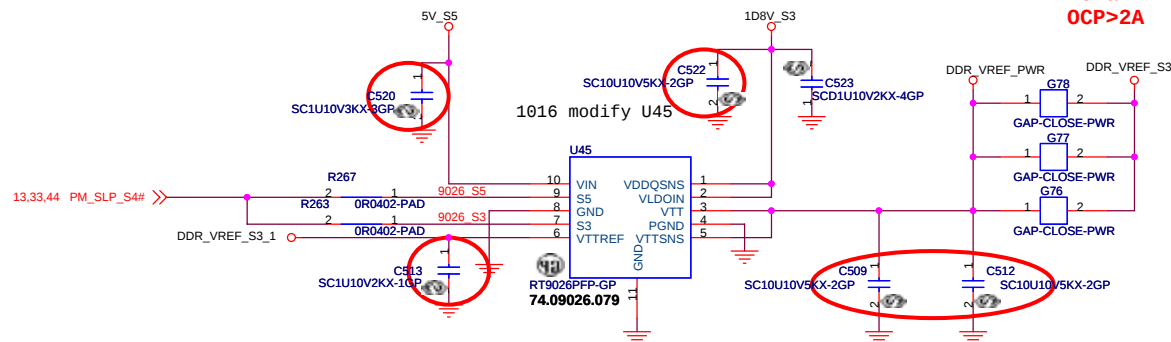


# 1D5V\_S0 Iomax=2.5A



20081001

Iomax=1A  
OCP>2A



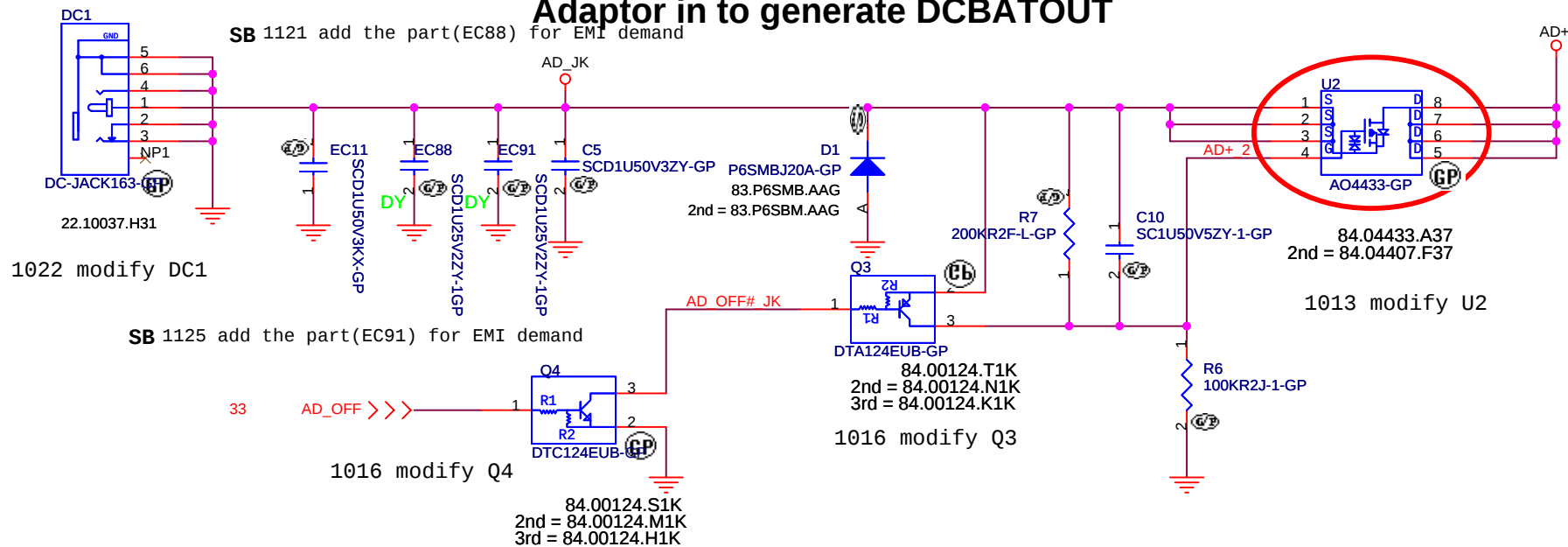
&lt;Core Design&gt;

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Taipei Hsien 221, Taiwan, R.O.C.

|             |                        |       |          |
|-------------|------------------------|-------|----------|
| Title       |                        |       |          |
| 1D5V & 0D9V |                        |       |          |
| Size        | Document Number        | Rev   |          |
| A3          | LA14                   | SB    |          |
| Date:       | Thursday, May 07, 2009 | Sheet | 43 of 52 |



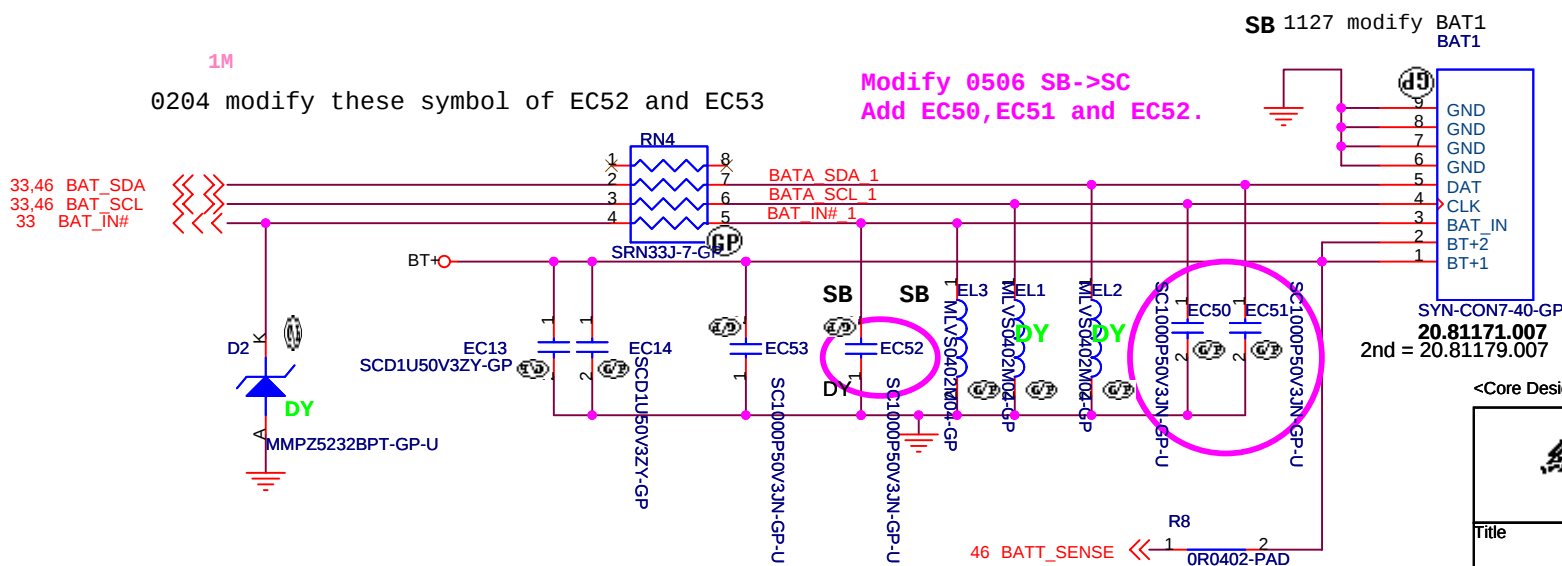
# Adaptor in to generate DCBATOUT



LA\_SA 0216 Change DC1 from 22.10037.F11 to 22.10037.H31

BATA\_SDA\_1 48  
BATA\_SCL\_1 48  
BAT\_IN#\_1 48

## BATTERY CONNECTOR

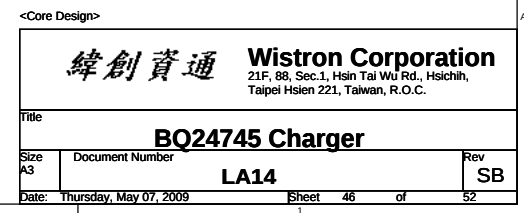


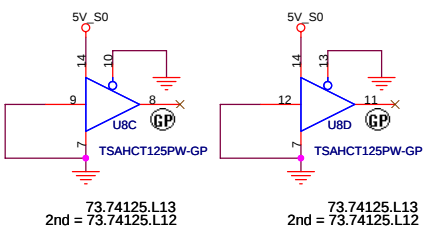
<Core Design>

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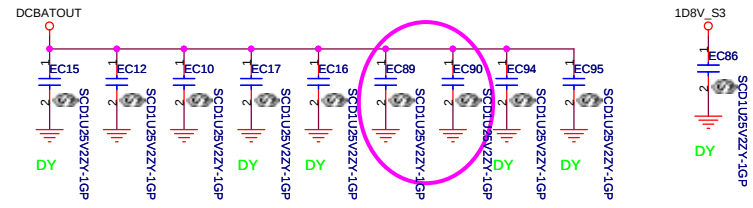
| Title        |                        |  |                |
|--------------|------------------------|--|----------------|
| AD/BATT CONN |                        |  |                |
| Size         | Document Number        |  | Rev            |
|              | LA14                   |  | SB             |
| Date         | Thursday, May 07, 2009 |  | Sheet 45 of 52 |



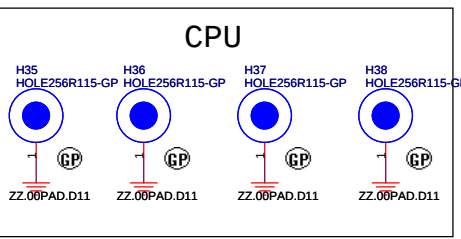
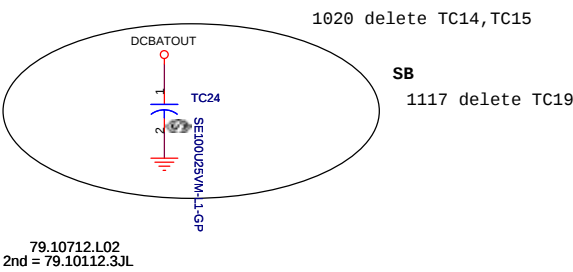


1016 modify U32

- 1017 add these parts(EC10,EC12,EC15~EC17,EC86) for EMI demand
- 1020 add the part(EC86) for EMI demand
- 1125 add the part(EC90) for EMI demand
- SB 1121 add the part(EC89) for EMI demand
- 1128 add EC94,EC95 for EMI demand



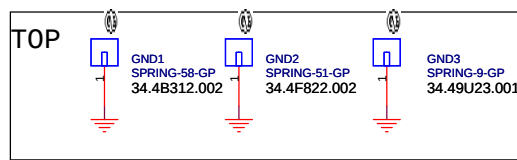
Modify 0506 SB->SC  
Add EC89 and EC90 for EMI demand



1016 modify H35-H38  
1016 delete H9-H12

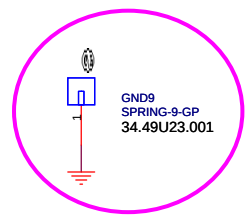
LA14 SB 0402 modify H35~H36

1016 modify H31 and H32  
SB 1120 remove H31and H32



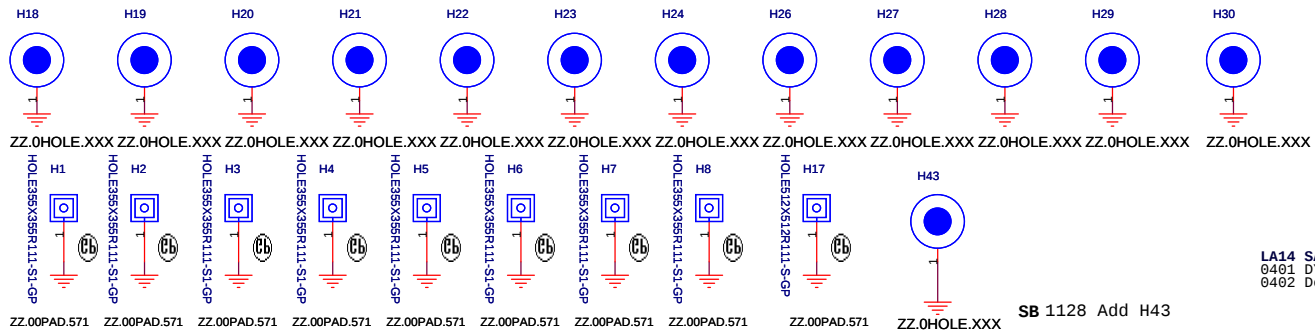
SB 1128 Add GND4,GND7,GND8

1 1230 Add GND9



Modify 0506 SB->SC  
Add GND9 for EMI demand

LA\_SA 0218 Change H35-H38 from ZZ.00PAD.571 to ZZ.00PAD.801



SB 1128 Add H43

LA14 SA->SB  
0401 DY H8  
0402 Del H8

|                 |  |  |  |
|-----------------|--|--|--|
| Title           |  |  |  |
| Size            |  |  |  |
| Document Number |  |  |  |
| Date            |  |  |  |
| Sheet           |  |  |  |
| Rev             |  |  |  |
| SB              |  |  |  |

## Speaker



## Touch pad



## Keyboard

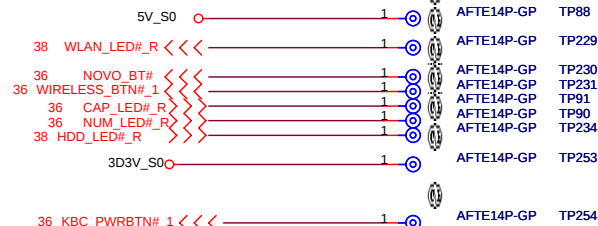


## Bluetooth



1017 modify USB signal connection

## LED



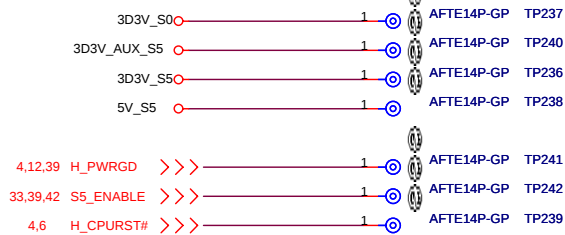
## SB

1112 remove the signal( STDBY\_LED#\_R)

## Battery



## Check test point



Test Point放在Dimm Door打開可量測處

## FAN



<Core Design>

|                              |                 |                                                                            |           |
|------------------------------|-----------------|----------------------------------------------------------------------------|-----------|
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| Title                        |                 |                                                                            |           |
| <b>AFTE test point</b>       |                 |                                                                            |           |
| Size                         | Document Number |                                                                            | Rev       |
|                              | <b>LA14</b>     |                                                                            | <b>SB</b> |
| Date: Thursday, May 07, 2009 |                 | Sheet 48 of 52                                                             |           |

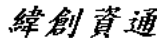
0910 delete F4(Page 18)  
0910 update footprint of U15(Page 30)  
0910 delete RIGHT1 and LEFT1(Page 33)  
0910 modify net names of TP\_LEFT and TP\_RIGHT(Page 36)  
0910 modify test points of AFTE and TPAD  
0911 modify net name from LPC\_RST to PLT\_RST1#(Page 24)  
0911 add net name(RBIAS, LED\_DUPLEX#, SMDATA, SMCLK)(Page 24)  
0911 add net name(DVDD\_1\_8, ACZ\_SDATIN0\_R, FLY\_P, FLY\_N, VREF\_LO, VREF\_HI)(Page 26)  
0911 add net name(EAPD#\_R)(Page 27)  
0912 modify the schematic of Page 33  
0912 delete GMCH\_TXB\*(Page 7& 18)  
0912 add these parts for EMI demand(page 7, 18, 20, 21, 23, 26, 28, 29, 30, 32, 33, 34, 35)  
0915 modify net name from 10M/100M/1G\_LED# to 10M/100M\_LED#(page24, 25)  
0915 delete these parts for EMI demand(page 30)  
0915 add EC34 for EMI demand(page3)  
0915 add EC73 for EMI demand(page 12)  
0915 modify LEDs port  
0916 move net(SPI\_WP#) from U9 pin120 to pin25(page33)  
0930 modify BLUE1(page22)  
0930 add 2nd for SPK1, MIC1 and modify LOUT1 (page28)  
0930 modify FAN1(page32)  
0930 modify TPAD1(page35)  
0930 modify KB1(page33)  
0930 modify net name for BIOS demand(page33)  
1001 delete these parts for EMI demand(ED1~8)  
1009 modify net name for GND to AGND(page27)  
1009 add R4, R5 for AC decoupling(page27)  
1009 add R96(page30)  
1013 modify TPAD1(page35)  
1013 modify U40 from 72.25X16.001 to 72.25X16.A01(page 34)  
1013 modify TC11 and add TC12(page42)  
1013 modify TC10 and add TC26(page44)  
1013 modify U2(page45)  
1013 modify U3 and U31(page 46)  
1013 modify R161 and R162(page41)  
1013 modify card1(page 30)  
1014 modify these LEDs(LED11, LED12)(page38)  
1014 modify these nets(page 26)  
1014 modify R258 from 10k to 20k ohm(page26)  
1014 add ER5 for EMI deamnd(page3)  
1015 modify LCD1 pin define(page 18)  
1015 modify the power from 3D3V\_S5 to 5V\_S5(page38)  
1015 modify TPAD1(page35)  
1015 modify RN57(page28)  
1015 modify F1(page18)

<Core Design>

|                                                                                       |                 |                                                                                                             |     |
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|                                                                                       | LA14            |                                                                                                             | SB  |
| Date: Thursday, May 07, 2009                                                          |                 | Sheet 49 of                                                                                                 | 52  |

1016 modify L1,L2 and L3(page 19)  
1016 modify XF1(page 25)  
1016 modify RN53 and U10(page 24)  
1016 modify U8(page19,47)  
1016 modify U4(page 37)  
1016 modify U23(page 43)  
1016 modify X2(page12)  
1016 modify X1(page 33)  
1016 modify X3(page 3)  
1016 modify D13(page 46)  
1016 modify D23(page 20)  
1016 modify D9(page 39)  
1016 modify D4(page 19)  
1016 modify Q3 and Q4(page45)  
1016 modify Q18(page 36)  
1016 modify Q15-Q17(page 36)  
1016 modify Q27-Q30(page38)  
1016 modify Q6 and Q14(page 32)  
1016 modify Q8(PAGE 24)  
1016 add GND1 nad GND2 for EMI demand(page 47)  
1016 modify LCD1 pin define(page 18)  
1016 delete H9-H12 and modify H35-H38,H31,H32(page 47)  
1017 add these parts for EMI demand(page 47)  
1017 delete these parts(EC208-EC210)(page 7)  
1017 modify BLUE1(page 22)  
1017 modify FAN1(page 32)  
1017 modify R291 and R293(page 38)  
1017 add U61,R52,EC23 and EC24(page 37)  
1017 modify RN60(page37)  
1017 add TC25(page 44)  
1017 add GND3 and modify GND2 for EMI demand(page 47)  
1017 modify USB signal connection(page13,18,22,23,30,31,48)  
1020 delete C537 for Power demand(page42)  
1020 add the part(EC86) for EMI demand(page 47)  
1020 delete U61,R52,EC24 and EC23(page 37)  
1020 delete TC14,TC15(page 47)  
1021 modify TC16(page 31)  
1021 delete TC23(page 23)  
1021 modify TC5(page 20)  
1021 modify and swap these parts(USB1 and USB2)(page 23)  
1021 modify SATA1(page 20)  
1022 modify DC1(page 45)

<Core Design>

|                                                                                       |                        |                                                                                                             |     |
|---------------------------------------------------------------------------------------|------------------------|-------------------------------------------------------------------------------------------------------------|-----|
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| Title                                                                                 |                        |                                                                                                             |     |
| <b>Change List</b>                                                                    |                        |                                                                                                             |     |
| Size                                                                                  | Document Number        |                                                                                                             | Rev |
|                                                                                       | LA14                   |                                                                                                             | SB  |
| Date:                                                                                 | Thursday, May 07, 2009 | Sheet 50 of 52                                                                                              |     |

SA to SB

1106 modify net connection of RN46 and RN44(page33) for layout demand  
1106 modify LED11 and LED12(page38) for fixing issue  
1106 modify LED power from 5V\_S5 to 5V\_AUX\_S5(page38) for customer demand  
1112 remove the signal(STDBY\_LED#\_FR)page38 for customer demand  
1112 remove these signals( STDBY\_LED#\_FR and STDBY\_LED#\_R) and R131(page36) for customer demand  
1112 remove the signal( STDBY\_LED#\_R)page36 for customer demand  
1112 remove the signal( STDBY\_LED#\_R)and TP253(page48) for customer demand  
1113 modify C103 and C106(page24) for crystal issue  
1113 modify 2nd of U19(page26)  
1113 modify 2nd of U43(page39)  
1113 modify 2nd of U44(page10)  
1113 modify U48(page22)  
1117 delete MDC function(R231,R237,R232,R234)(page12)  
1117 delete TC19(page 47) for ME deamnd  
1118 modify PCB Ver. from SA to SB(page33)  
1118 delete TC12(page42) for layout demand  
1118 delete TC27(page9) for layout demand  
1118 delete R107 and add L18 for cost down  
1119 modify R130 and R133(page 36) for LED brightness  
1119 modify EC52 and EL3(page45) for EMI demand  
1119 modify SPK1(page 28) for ME deamnd  
1119 add G84 for RTC reset demand  
1120 modify EC78for EMI demand((page10)  
1120 modify PowerCN1 pin3 and remove EC44(page36) fro LED function  
1120 remove H31 and H32(page47)for ME demand  
1120 add RN61 and RN62(page3) for layout demand  
1120 swap these nets(CLK\_MCH\_3GPLL,CLK\_MCH\_3GPLL#, CLK\_PCIE\_MINI1,CLK\_PCIE\_MINI1#)(page3)for CLK REQ demand  
1120 add the net( SATACLKREQ#)(page3,13)for CLK REQ demand  
1120 move these nets (CLK\_PCIE\_MINI1,CLK\_PCIE\_MINI1#)(page3)for CLK REQ demand  
1120 modify RN61 and RN62(page3)for CLK REQ demand  
1121 add EC87 for EMI demand(page18)  
1121 add the part(EC89) for EMI demand(page47)  
1121 add the part(EC88) for EMI demand(page45)  
1121 modify R18,C43(page41) for Power demand  
1121 modify R275(page42)for Power demand  
1121 modify R271,R272,R286 and L16(page44) for Power demand  
1124 modify U42 and delete R182,R185 (page32) for thermal function  
1124 modify these names of these nets(G7922\_SGND2,G7922\_SGND3...) (page32) for thermal function  
1124 add R302(page3) for clock gen function  
1125 add the part(EC90) for EMI demand(page47)  
1125 add the part(EC91) for EMI demand(page45)  
1125 modify R125,R126(page18) for LCD brightness control  
1125 modify RN40 and delete RN42(page32) for layout demand  
1125 add EC92 and EC93 for EMI demand(page 22)  
1126 add these nets (PCIE\_REQ\_LAN#,PCIE\_REQ\_MINI#)(page3)for CLK REQ demand  
1126 delete R230,R233,R235,R236 and RN63(page12) for removing MDC function  
1126 add C541 and modify R101(page26) for codec function  
1126 modify RN61 and RN62(page3) for layout demand  
1126 modify EU1,EU2 and add EU3,EU4 for EMI demand(page28)  
1127 modify CRT1(page19) for customer demand  
1127 swap the nets of RN61 and RN62 for layout demand(page3)  
1127 modify BAT1(page45) for ME demand  
1127 modify U27(page44) for power demand

1127 modify C377(page32) for thermal function  
1128 Add H43,GND4,GND7,GND8(page47) for EMI demand  
1128 modify LCD1(page18) for cost down  
1128 Add L19(page24) for vender demand  
1128 add EC94,EC95 for EMI demand(page47)  
1201 modify C3 (page18)  
1201 modify EC6-9(page28)  
1204 modify RN36  
1204 modify second source of R11

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|                                                                                       |                 |                                                                                                             |     |
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|                                                                                       | LA14            |                                                                                                             | SB  |
| Date: Thursday, May 07, 2009                                                          |                 | Sheet 51 of 52                                                                                              |     |

SB to 1

1222 modify U42 for customer demand(page32)

1222 modify these names of nets (BMC2102\_DN2,DP2,DN3,DP3,PWROK,FAN\_TACH,FAN\_DRIVE)(page32)

1222 modify RN58 from 68 to 56 ohm for customer demand(page28)

1222 modify PCB Ver. from SB to -1(page33)

1222 modify TC5 for HDD side(page20)

1222 modify card1 from 20.I0043.001 to 20.I0043.011for CE demand(PAGE30)

1223 modify the net(EMC2102\_CLK\_SEL) for reducing component (page32)

1223 modify the net(RSMRST#) for reducing component(page33)

1224 dummy C6(page27)

1224 add R306 for FSB Dynamic ODT(dummy)(page7)

1224 add R307 and R308 for LAN co-layout demand(page24)

1224 modify FAN1for CE demand(page32)

1224 remove R113 for reducing component (page39)

1224 modify RN54 for reducing component (page12)

1224 modify R191,RN48 and this net AD\_OFF for reducing component (page33)

1224 modify D5(dummy)(page20)

1224 delete R165 and add RN64 for reducing component (page32)

1226 modify TP\_L1 and TP\_R1 for ME demand(page37)

1226 modify R100 and C240(dummy)(page30)

1226 delete R96 for reducing component (page30)

1229 modify C76,C77 from 12pF to 15pF for vender demand(page12)

1229 modify L19 for vender demand(page24)

1229 modify U30 for cost down(page18)

1229 modify U44 for cost down(page10)

1229 modify R20 for power team demand(page41)

1230 modify the name of net(RST#\_CHIP)(beacuse R97 was removed)(page30)

1230 modify ODD1 for CE demand(page21)

1230 modify C33,C34 for power team demand (page41)

1230 modify D14 for CE demand(page33)

1230 Add C393,C398 for power team demand(page46)

1230 Add GND9 for EMI demand(page47)

1230 dummy C507(page26)

1230 delete Q1 and modify U1 for new AMP IC(page27)

1230 delete RN35 and add R309(page27)

1231 modify R80 for clock gen voltage(3.3V to 1.05V) (page3)

1231 modify ODD1 for ME demand(page21)

0105 modify R3,R128,R129,R130,R132 and R133 for LED brightness conrtol(page36)

0105 modify R291,R292,R293 and R294 for LED brightness conrtol (page38)

0105 modify L1,L2 and L3 for EMI demand(page19)

0112 modify TC10(page44)

0113 modify ODD1 for ME demand(page21)

0113 modify U34,U38,U6,U7,U36 and U37 for power demand(page41)

0113 modify U23 and U29 for power demand(page42)

0113 modify U25,U27,TC10 and L16 for power demand(page44)

1 to 1M

0121 modify PCB Ver. from 1 to 1M(page33)

0121 add R310(page26)

0204 add R457,R458 for power demand(co-layout)(page42)

0204 modify R130,R132 and R133 for LED brightness conrtol(page36)

0204 modify KB1 for CE demand(add mylar)(page33)

0204 modify the symbol of C22 (page41)

0204 modify these symbol of C531and C532 (page44)

0204 modify these symbol of EC52 and EC53 (page45)

0204 modify the symbol of EC74 (page23)

0 ohm to short pad

1222 modify R277,R278(page44)

1222 modify R135,R5(page27)

1222 modify R58(page25)

1222 modify R136~140,R142~R144,R146,R149(page41)

1222 modify R21,R22(page41)

1222 modify R80,R87(page3)

1222 modify R252(page10)

1222 modify R209(page13)

1222 modify R68,R69,R79(page24)

1222 modify R97(page30)

1222 modify R159(page31)

1222 modify R189(page33)

1222 modify R281(page42)

1222 modify ER1~ER4(page28)

1224 modify R91(page3)

1224 modify R67,R71(page24)

1224 modify ERN2(page34)

<Core Design>

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|---------------------------------------------------------------------------------------|-----------------|-------------------------------------------------------------------------------------------------------------|-----|
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