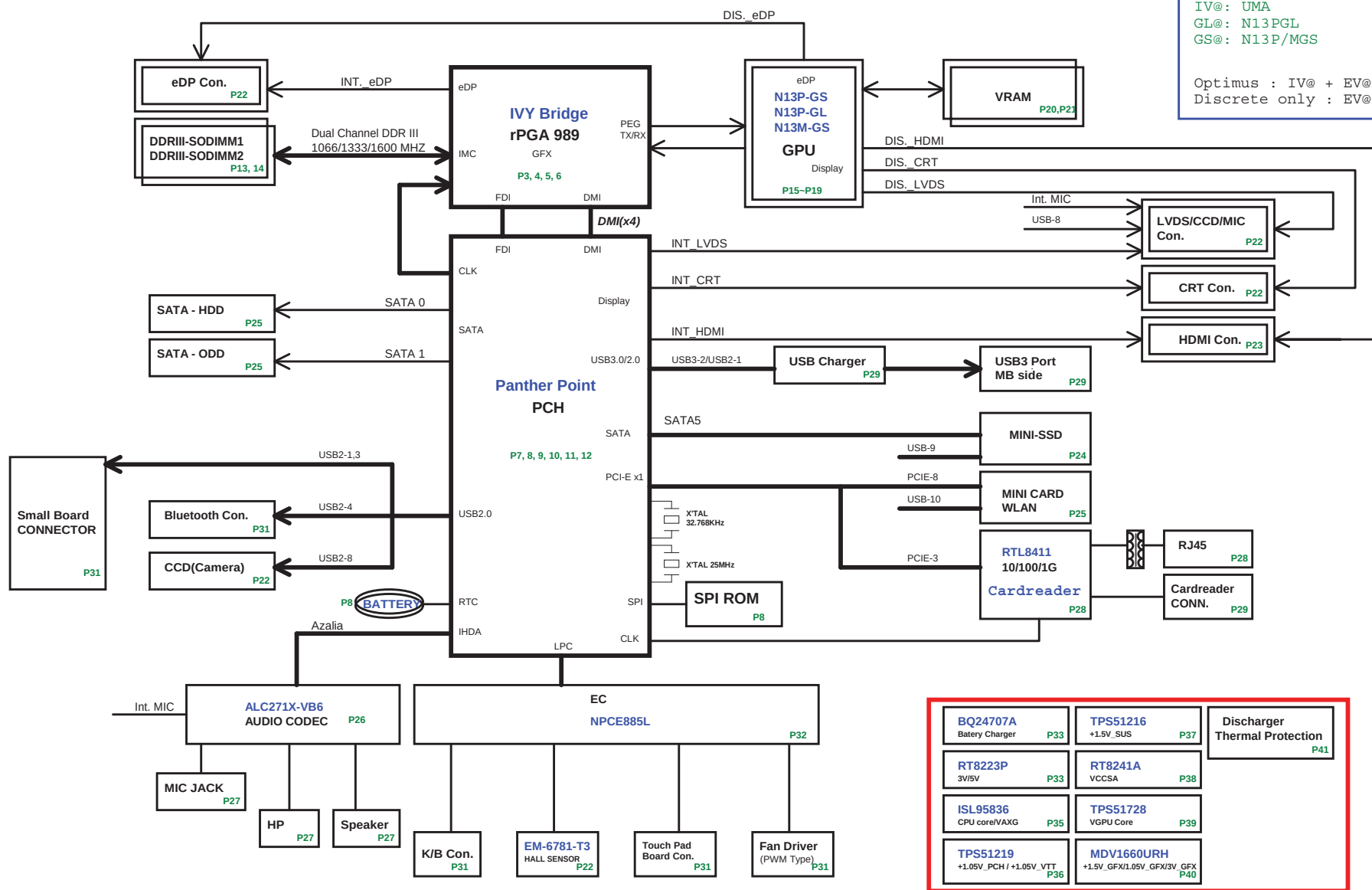


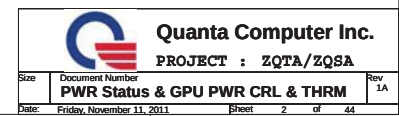
IV@ : iGPU  
EV@ : dGPU  
OP@ : Optimus  
DO@ : Discrete only  
SP@ : Special  
SNP@ : N13PGS/GL  
IV@ : UMA  
GL@ : N13PGL  
GS@ : N13P/MGS

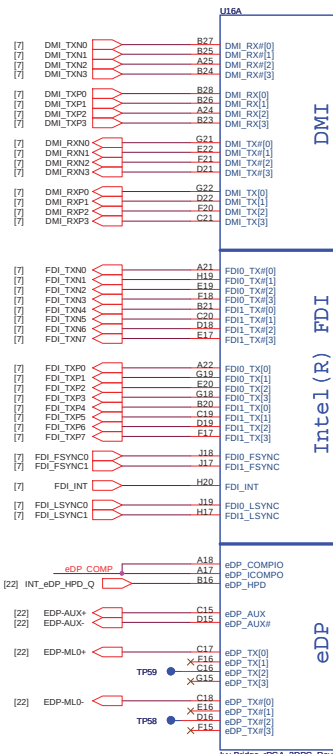
Optimus : IV@ + EV@ + OP@  
Discrete only : EV@ + DO@





### Thermal Follow Chart





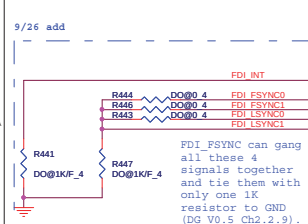
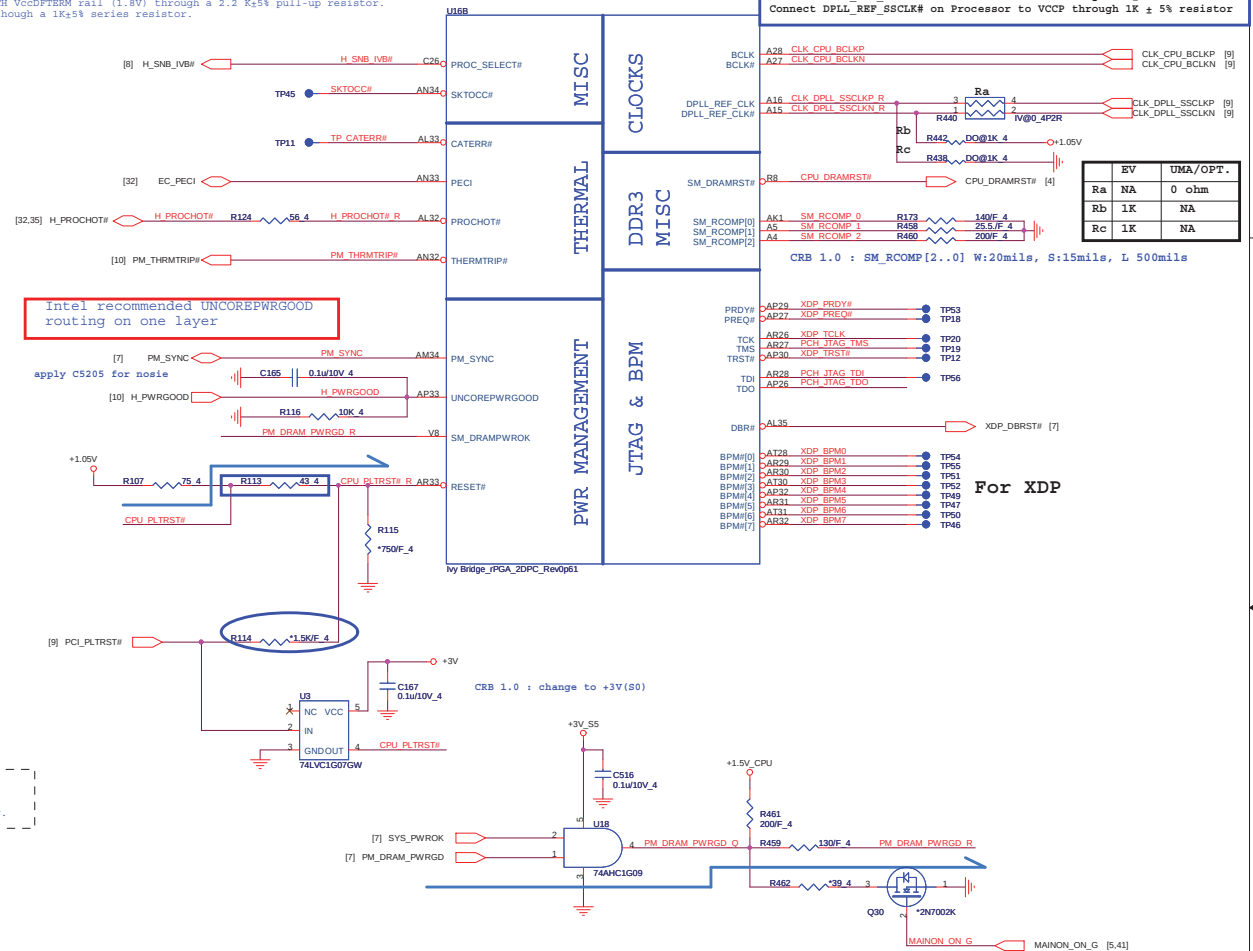
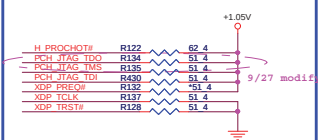
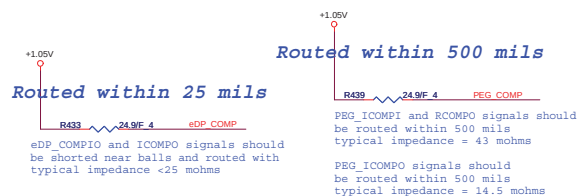
**HPD disable**

This signal can be left as no connect if entire eDP interface is disabled.

```

-----
DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with
PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.
-----

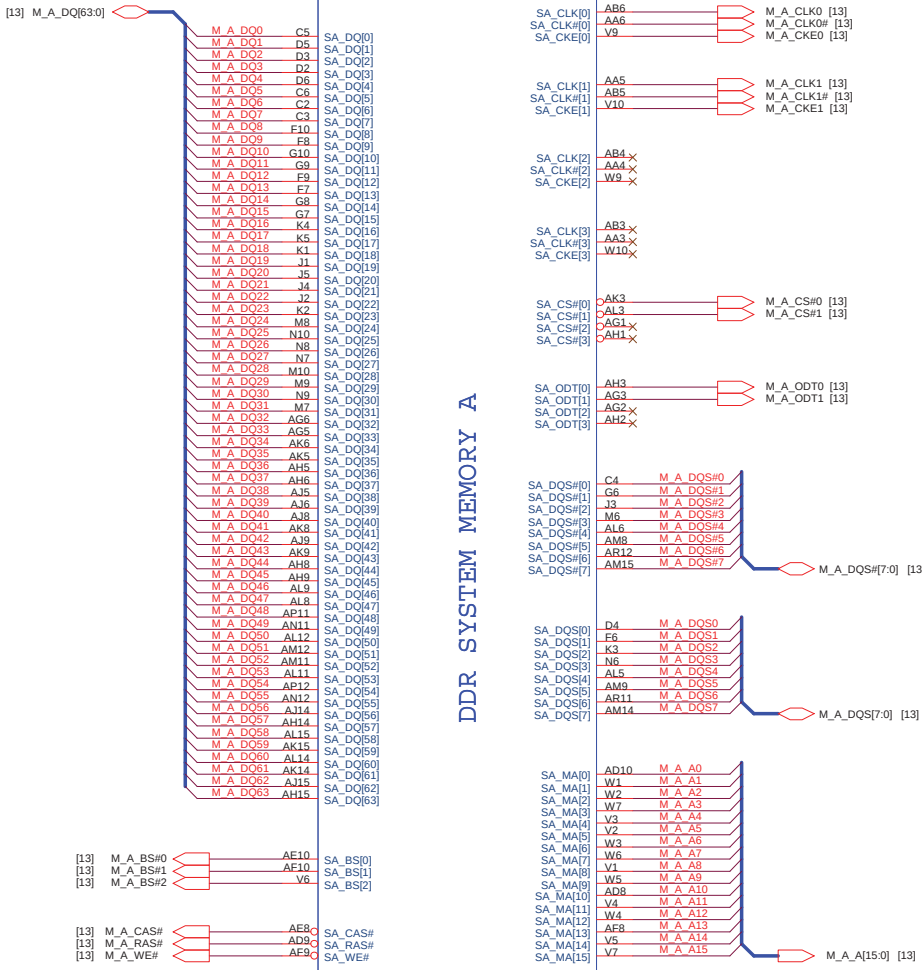
```



U16C

Ivy Bridge\_rPGA\_2DPC\_Rev0p61

DDR SYSTEM MEMORY A

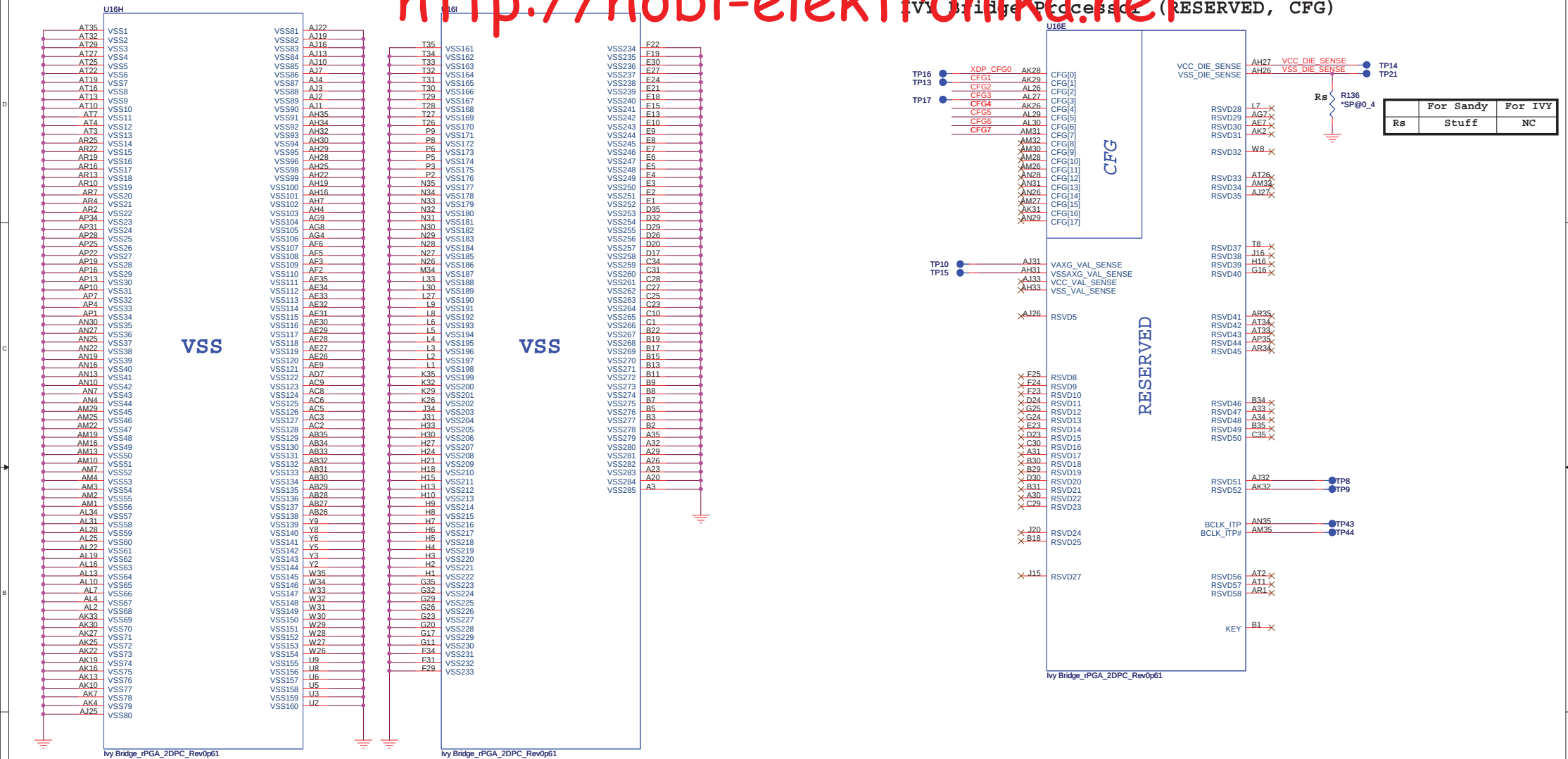




# IVY Bridge Processor (PNU)

<http://hobi-elektronika.net>

# IVY Bridge Processor (RESERVED, CFG)

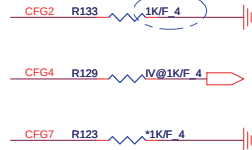


## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

|                                    | 1                                                        | 0                                            |
|------------------------------------|----------------------------------------------------------|----------------------------------------------|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation                                         | Lane Reversed                                |
| CFG4<br>(DP Presence Strap)        | Disable; No physical DP attached to eDP                  | Enable; An ext DP device is connected to eDP |
| CFG7<br>(PEG Defer Training)       | PEG train immediately following<br>xxRESETB de assertion | PEG wait for BIOS training                   |

9/26 modify



## CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



**Quanta Computer Inc.**  
**PROJECT : ZQTA/ZQSA**

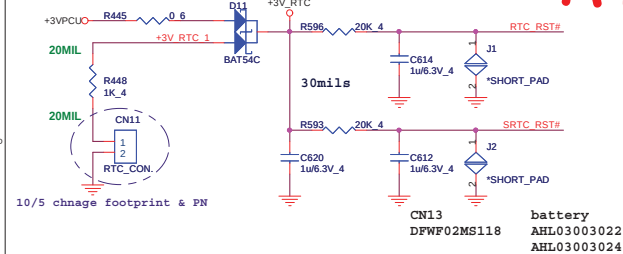
|      |                       |     |
|------|-----------------------|-----|
| Size | Document Number       | Rev |
|      | <b>IVY Bridge 4/4</b> | 1A  |

Date: Friday, November 11, 2011 Sheet 6 of 44

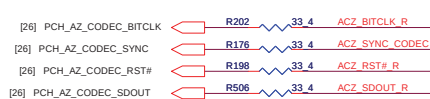


http://hobi-elektronika.net

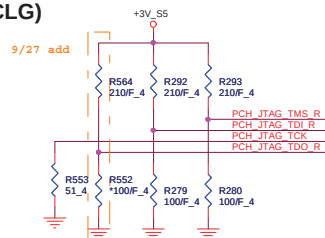
RTC Circuitry(RTC)  
*20mils*



## HDA Bus(CLG)

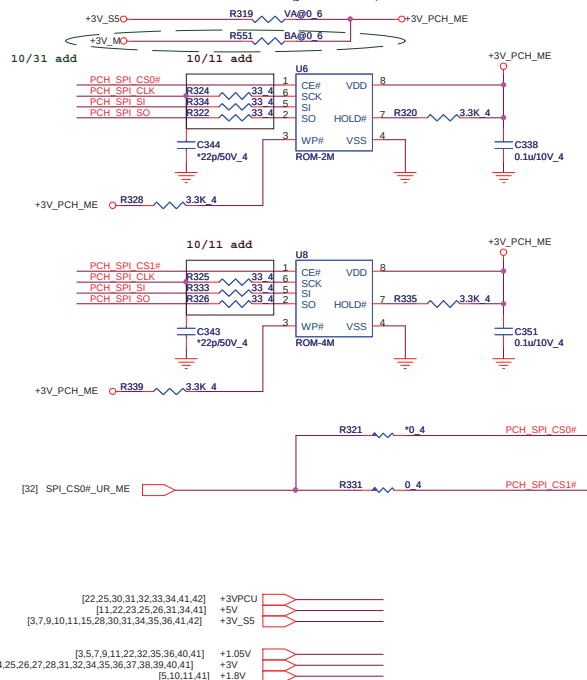


## PCH JTAG Debug (CLG)

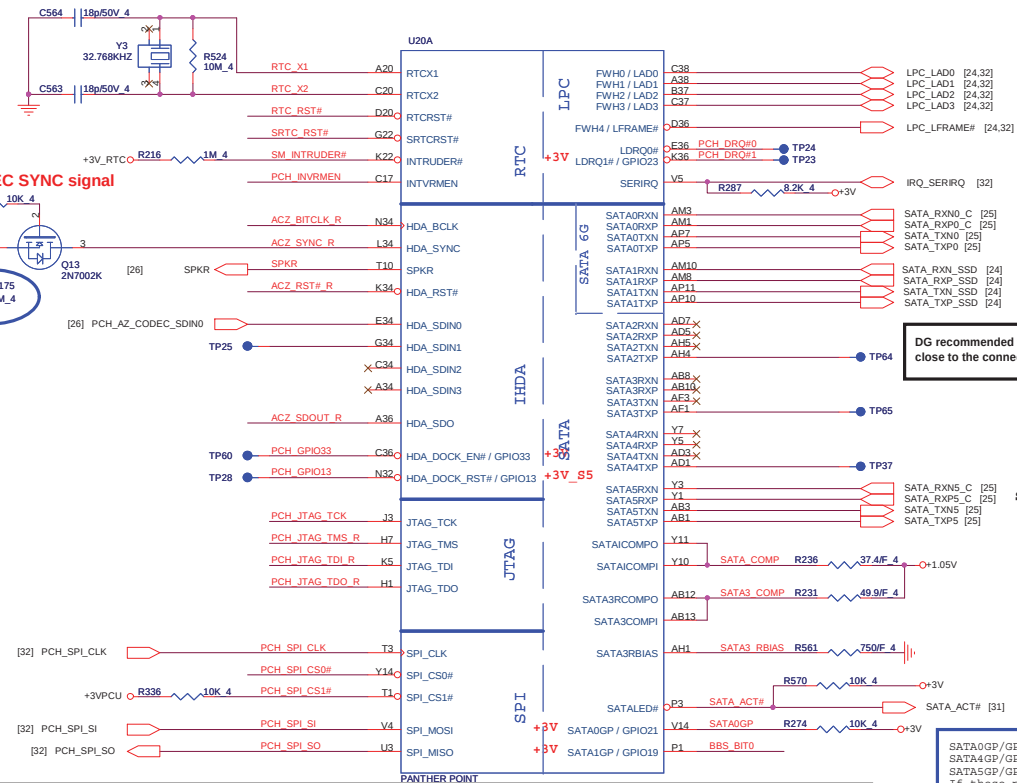
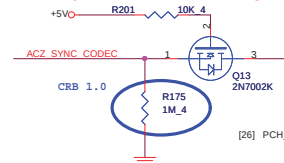


**PCH Dual SPI (CLG)** (Default for WIN8)

```
W25Q32BVSSIG / AKE391P0N00----->4MB
W25Q16BVSSIG / AKE38FP0N01----->2MB
for BA W25Q64BVSSIG / AKE38FP0N00----->8MB
```



**Add MOSFET to separate CODEC SYNC signal**



DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

SATA0GP/GPIO21  
SATA4GP/GPIO16  
SATA5GP/GPIO49  
If these pins are unused use 8.2k  
to 10k pull-up to +Vcc3\_3 or 8.2k  
to 10k pull-down to ground

### PCH Strap Table

| Pin Name       | Strap description                                                       | Sampled       | Configuration                                                                                                                                                                                           |                                                                                                          |       |               |   |   |       |   |   |     |                                                                                       |
|----------------|-------------------------------------------------------------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|-------|---------------|---|---|-------|---|---|-----|---------------------------------------------------------------------------------------|
| SPKR           | No reboot mode setting                                                  | PWROK         | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode                                                                                                                                       | +3V <sub>CC</sub>     |       |               |   |   |       |   |   |     |                                                                                       |
| GNT3# / GPIO55 | Top-Block Swap Override                                                 | PWROK         | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K)                                                                                                                                             | PCI_GNT3# [9]                                                                                            |       |               |   |   |       |   |   |     |                                                                                       |
| INTVRMEN       | Integrated 1.05V VRM enable                                             | ALWAYS        | Should be always pull-up                                                                                                                                                                                | +3V <sub>RTC</sub>  |       |               |   |   |       |   |   |     |                                                                                       |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1]                                           | PWROK         | <table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table> | GNT1#                                                                                                    | GNT0# | Boot Location | 1 | 1 | SPI * | 0 | 0 | LPC |  |
| GNT1#          | GNT0#                                                                   | Boot Location |                                                                                                                                                                                                         |                                                                                                          |       |               |   |   |       |   |   |     |                                                                                       |
| 1              | 1                                                                       | SPI *         |                                                                                                                                                                                                         |                                                                                                          |       |               |   |   |       |   |   |     |                                                                                       |
| 0              | 0                                                                       | LPC           |                                                                                                                                                                                                         |                                                                                                          |       |               |   |   |       |   |   |     |                                                                                       |
| GPIO19         | Boot BIOS Selection 0 [bit-0]                                           | PWROK         |                                                                                                                                                                                                         |                                                                                                          |       |               |   |   |       |   |   |     |                                                                                       |
| HDA_SDO        | Flash Descriptor Security                                               | RSMRST        | 0 = effect (default)(weak pull-down 20K)<br>1 = overridden                                                                                                                                              | 32] ME_WR           |       |               |   |   |       |   |   |     |                                                                                       |
| DF_TVS         | DMI/FDI Termination voltage                                             | PWROK         | 0 = Set to Vss (weak pull-down 20K)<br>1 = Set to Vcc                                                                                                                                                   |                                                                                                          |       |               |   |   |       |   |   |     |                                                                                       |
| GPIO28         | On-die PLL Voltage Regulator                                            | RSMRST#       | 0 = Disable<br>1 = Enable (weak pull-up 20K)                                                                                                                                                            | PLL_ODVR_EN [10]                                                                                         |       |               |   |   |       |   |   |     |                                                                                       |
| HDA_SYNC       | On-Die PLL VR Voltage Select                                            | RSMRST        | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V                                                                                                                                             | +3V <sub>SS</sub>   |       |               |   |   |       |   |   |     |                                                                                       |
| GPIO15         | Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD | RSMRST        | 0 = Disable (Default)<br>1 = Enable                                                                                                                                                                     | +3V <sub>SS</sub> PCH_GPIO15 [10]                                                                        |       |               |   |   |       |   |   |     |                                                                                       |
| DSWVREN        | DEEP S4/S5 well<br>On Die DSW VR Enable                                 | DSW           | High = Enable (Default)<br>Low = Disable                                                                                                                                                                | +3V <sub>RTC</sub> DSWVREN [7]                                                                           |       |               |   |   |       |   |   |     |                                                                                       |
| NV_ALE         | Intel Anti-Theft HDD protection<br>Only for Interposer                  | PWROK         | 0 = Disable (Internal pull-down 20kohm)                                                                                                                                                                 | +1.8V <sub>CC</sub> INV_ALE [9]                                                                          |       |               |   |   |       |   |   |     |                                                                                       |

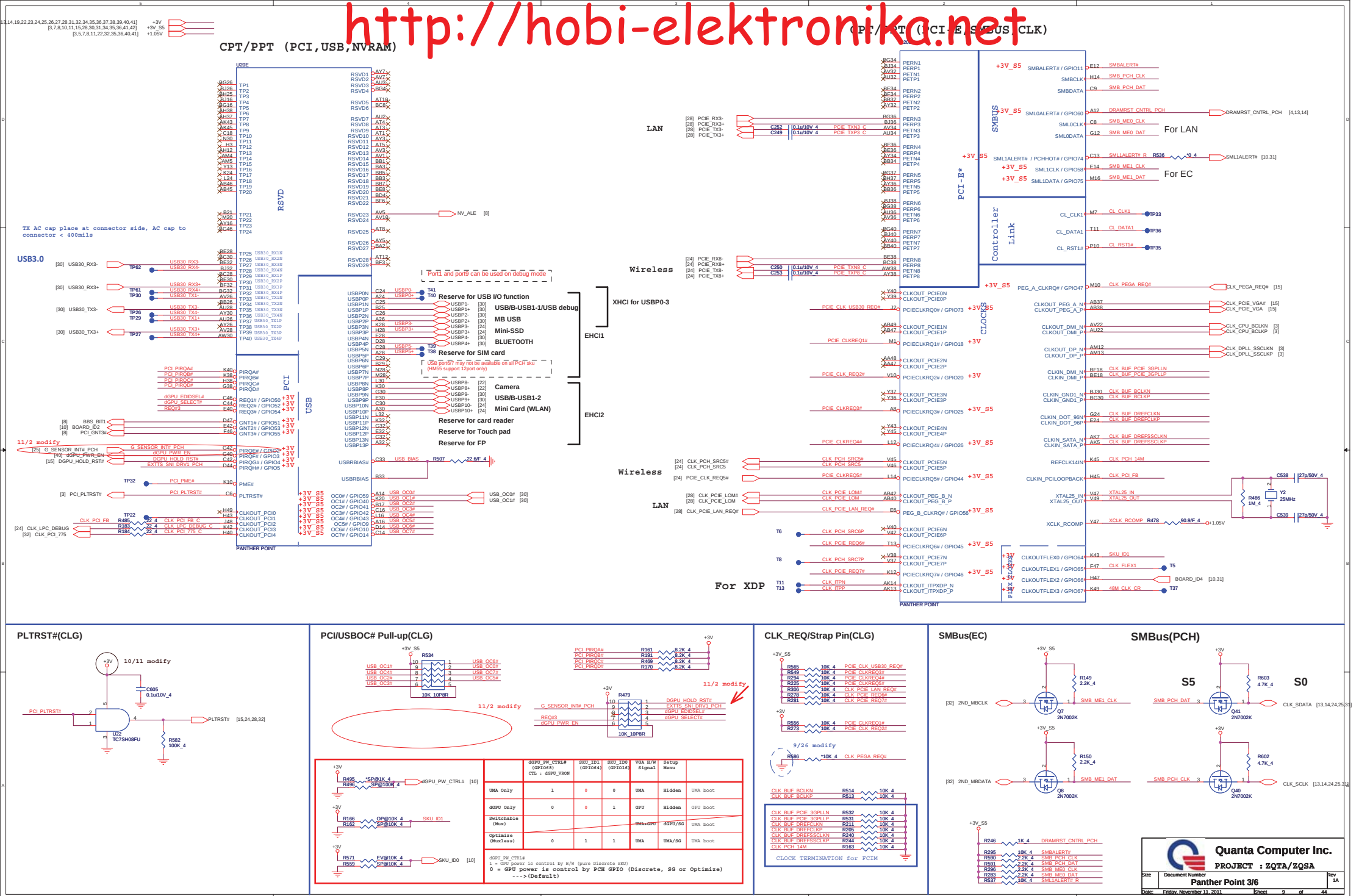
Used as GPIO only. at chklist 1.2

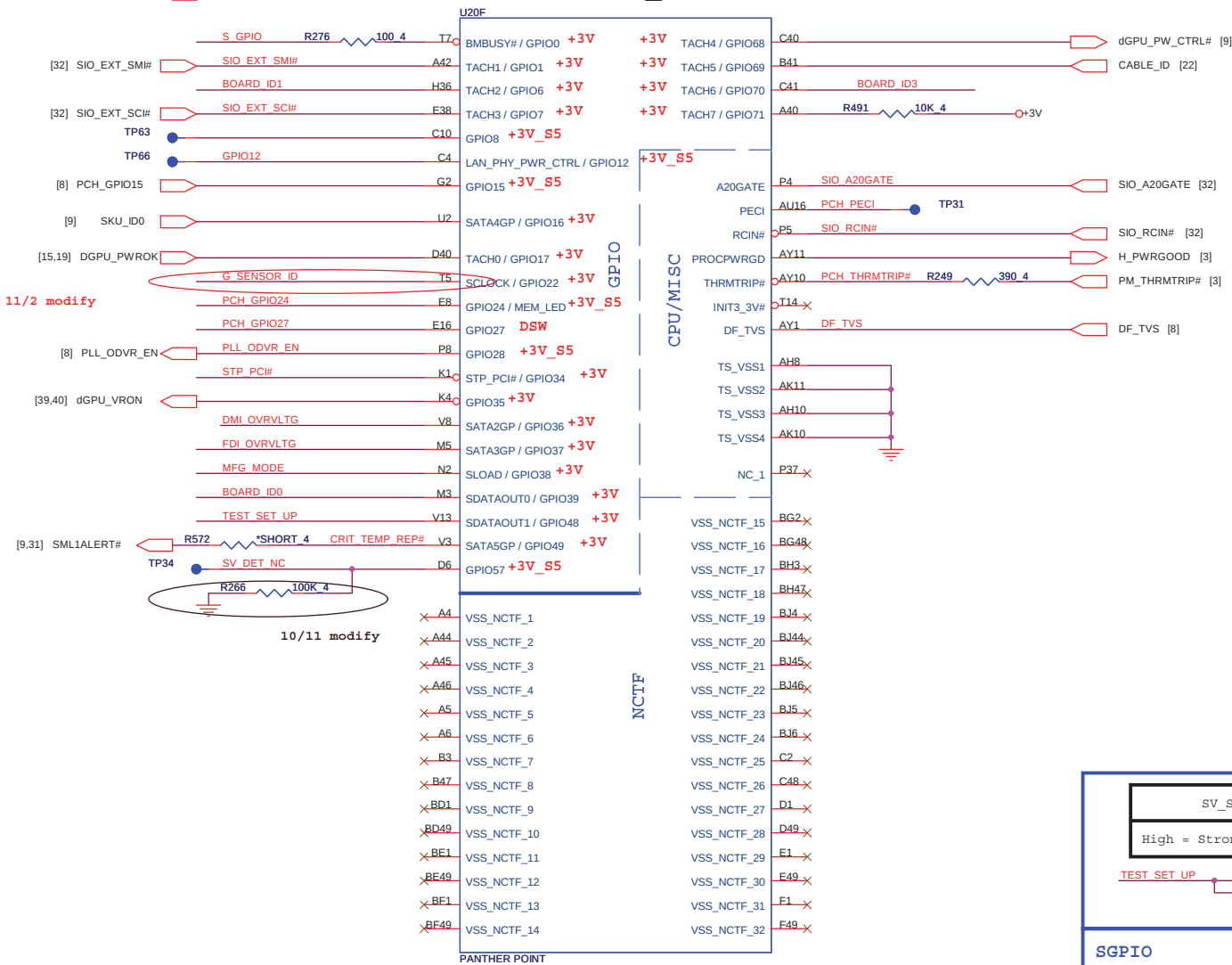
**Default weak pull-up on GNT0/1#**  
**[Need external pull-down for LPC BIOS]**

ME WR default EC setting folating

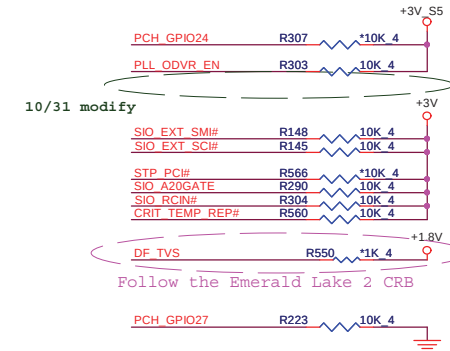
for future CPU, Sandy Bridge NC  
DF\_TVS needs to be pulled up to VccDFTERM power rail  
through 2.2 kOhm  $\pm 5\%$  - R8361 change to 0 or not??

Needs to be pulled High for Huron River platform.  
chklist 1.2



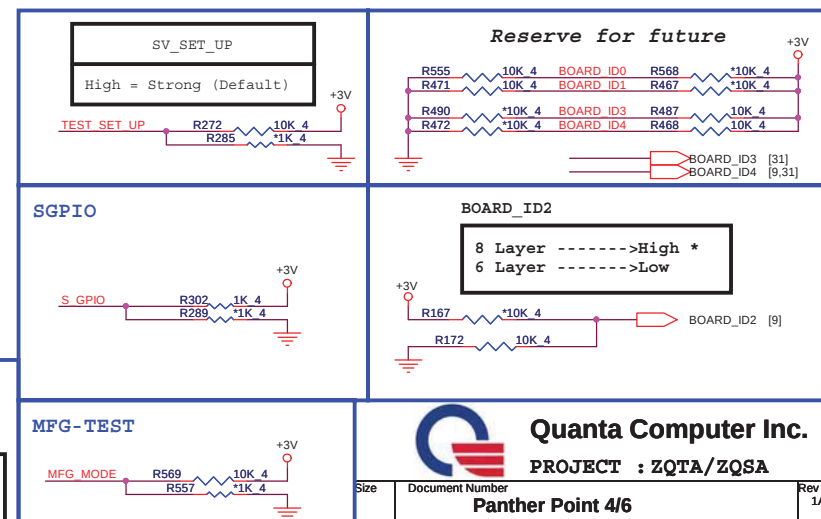
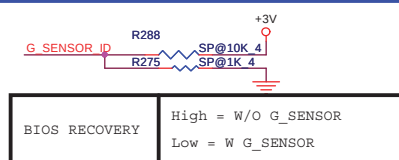
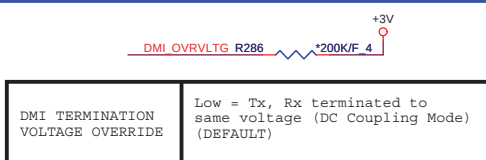
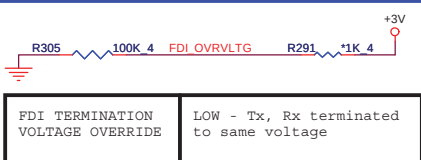


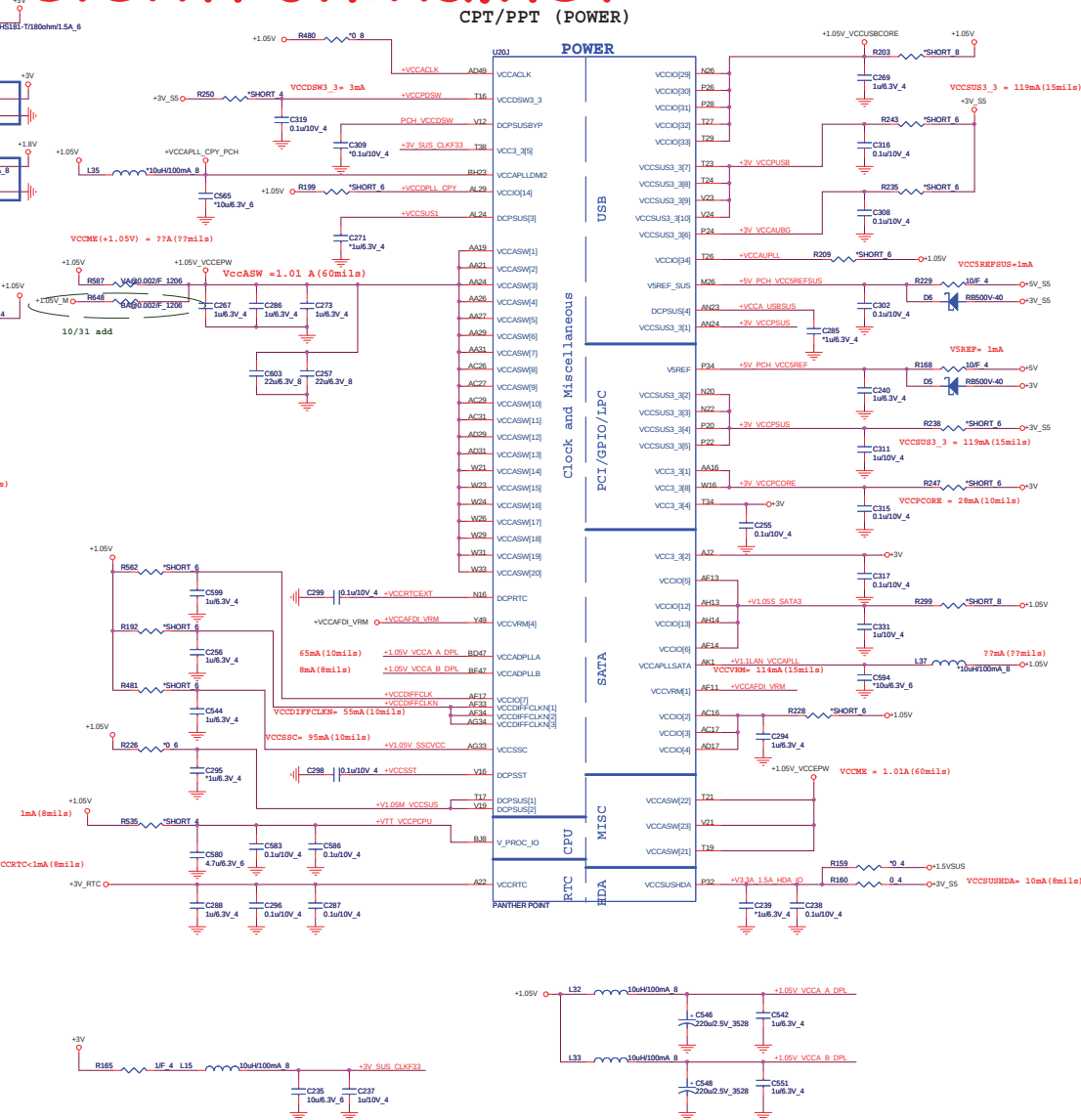
### GPIO Pull-up/Pull-down(CLG)



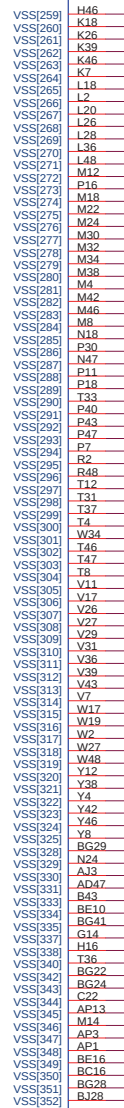
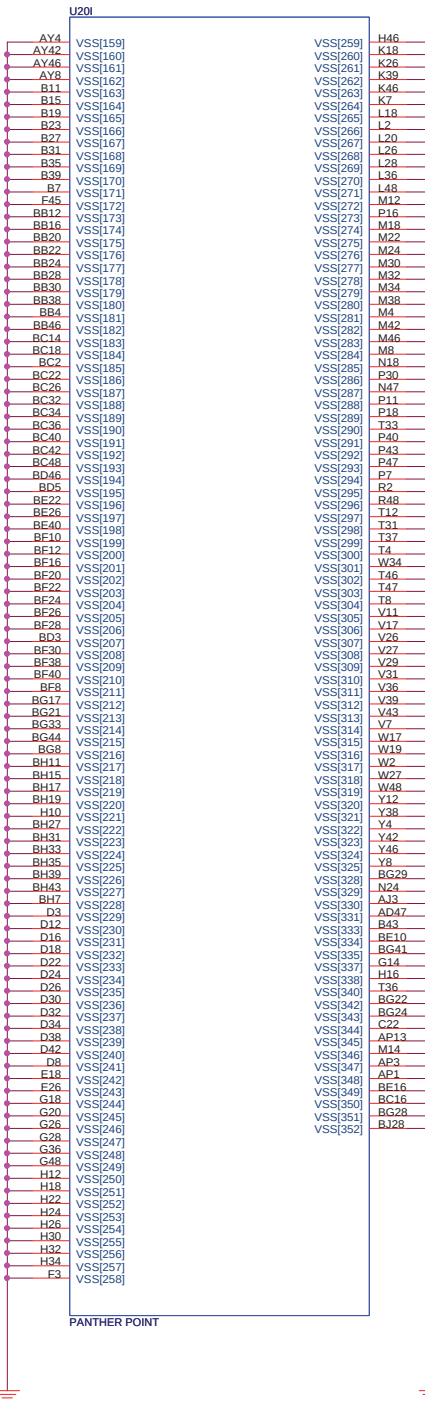
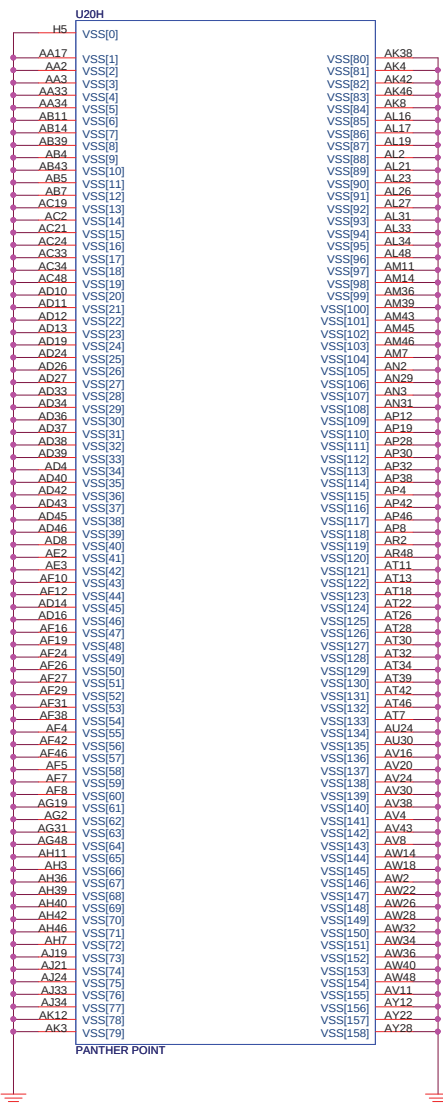
GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

SATA2GP : strap for reserved at chklist 1.2  
SATA3GP : strap for reserved at chklist 1.2  
NOTE: The internal pull-down is disabled after PLTRST# deasserts.  
NOTE: This signal should not be pulled high when strap is sampled.





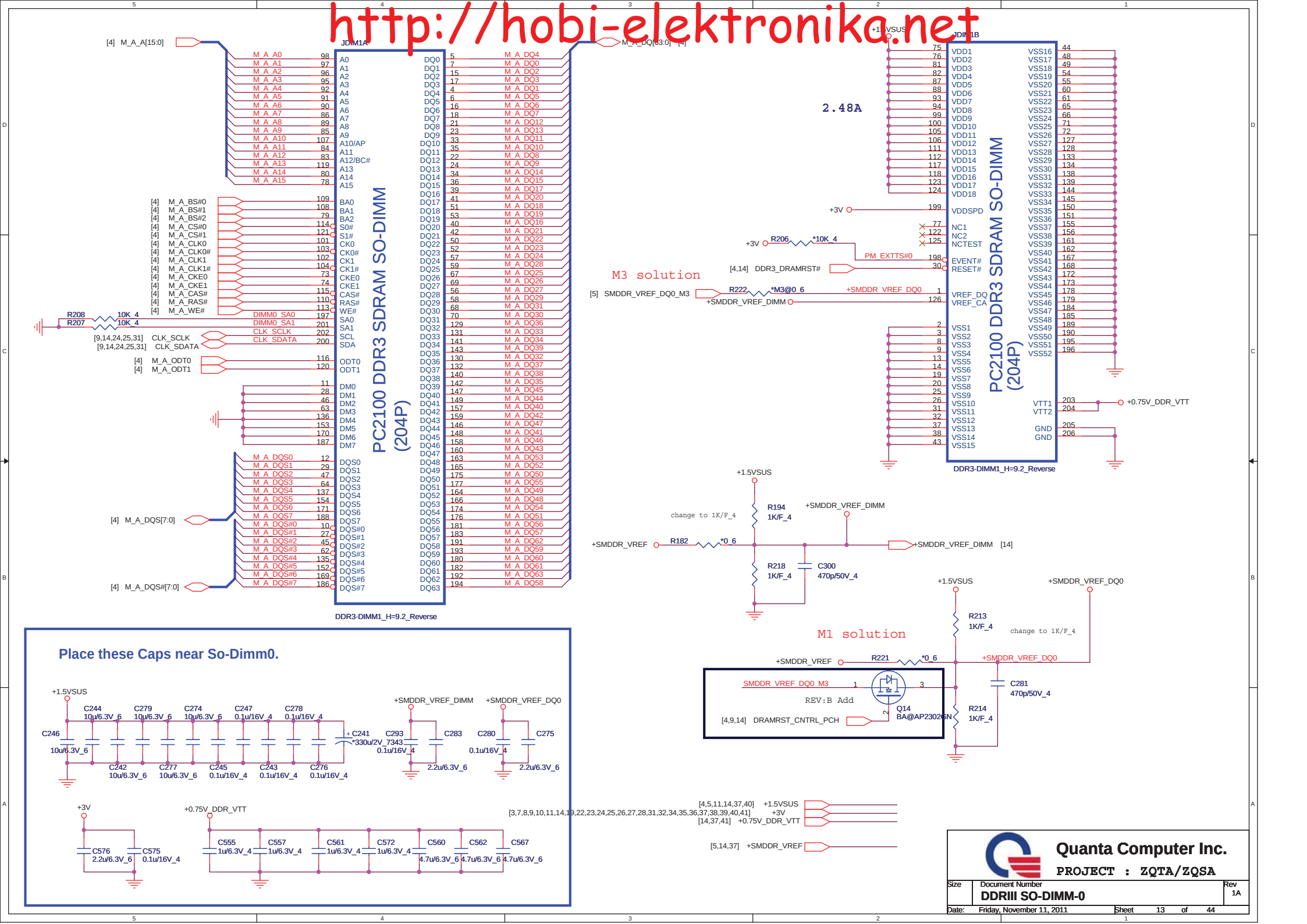
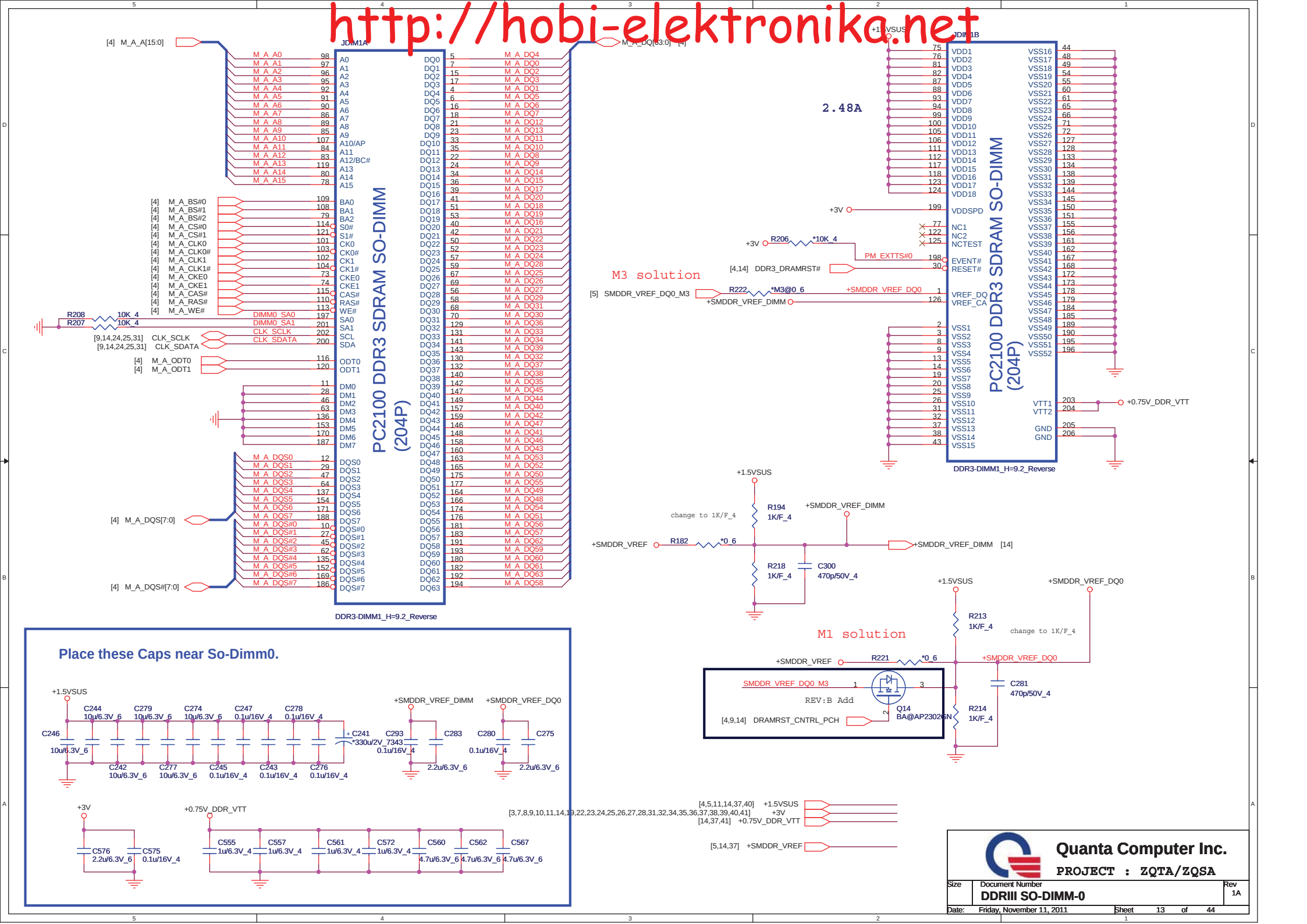
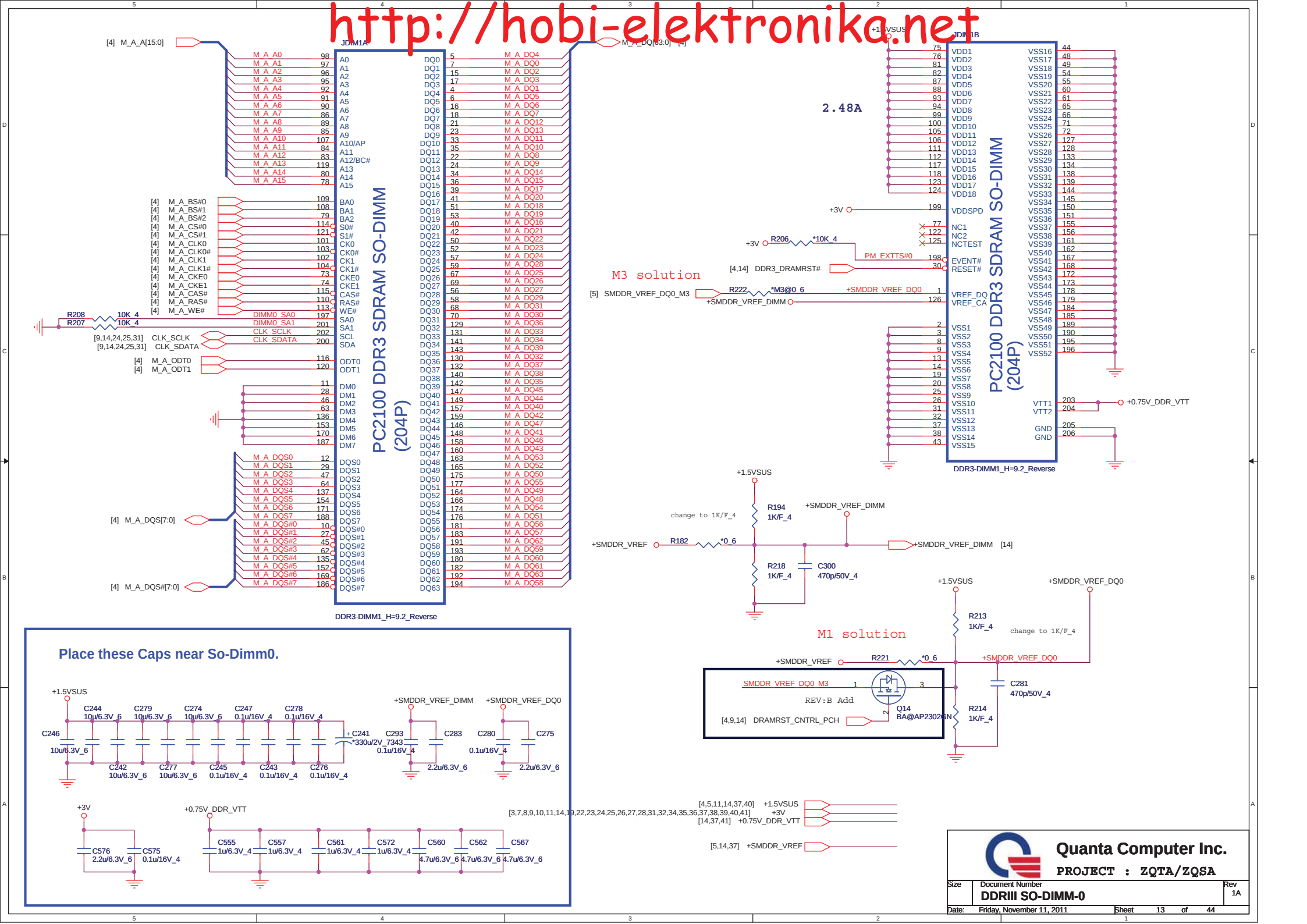
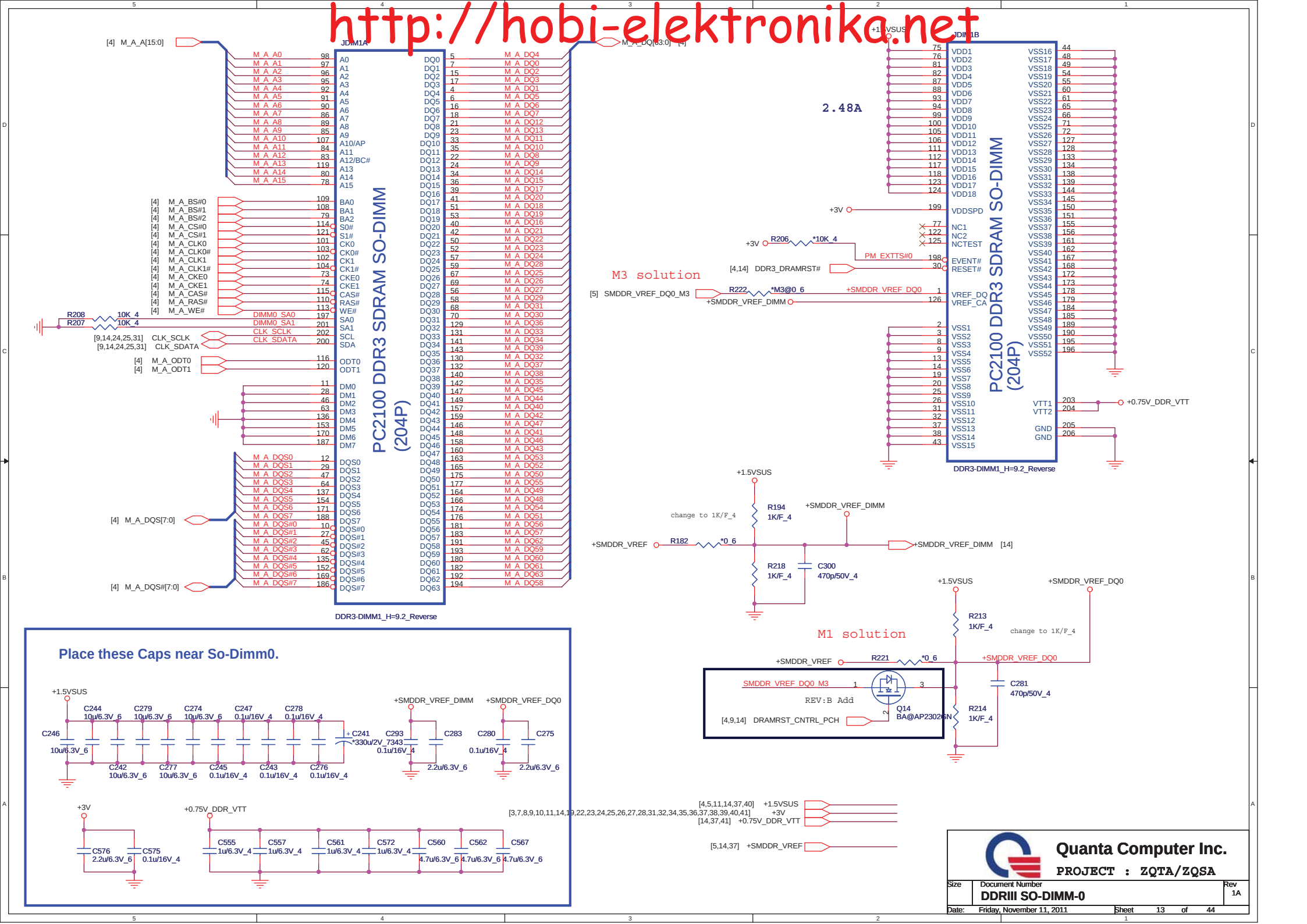
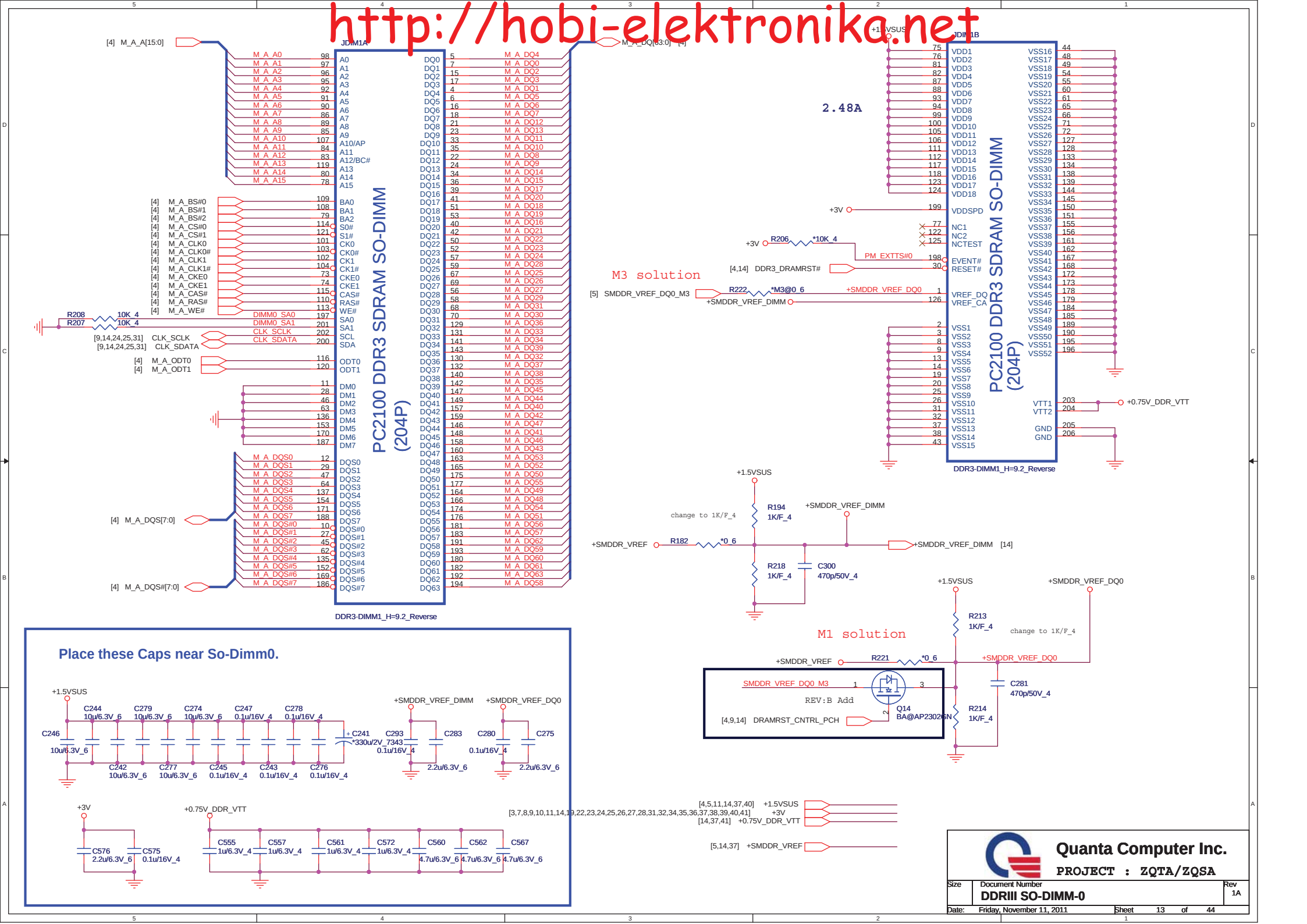
## IBEX PEAK-M (GND)

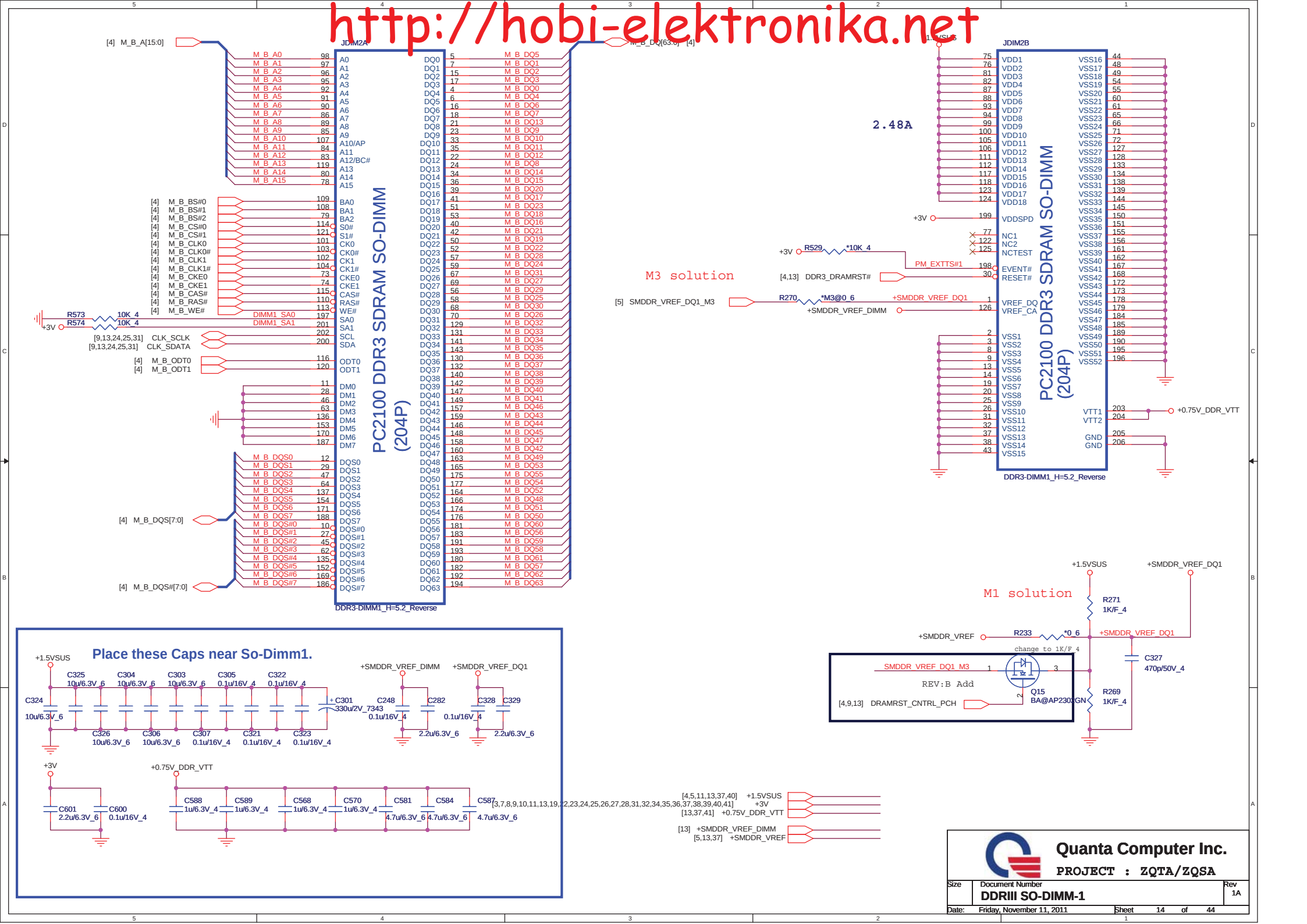
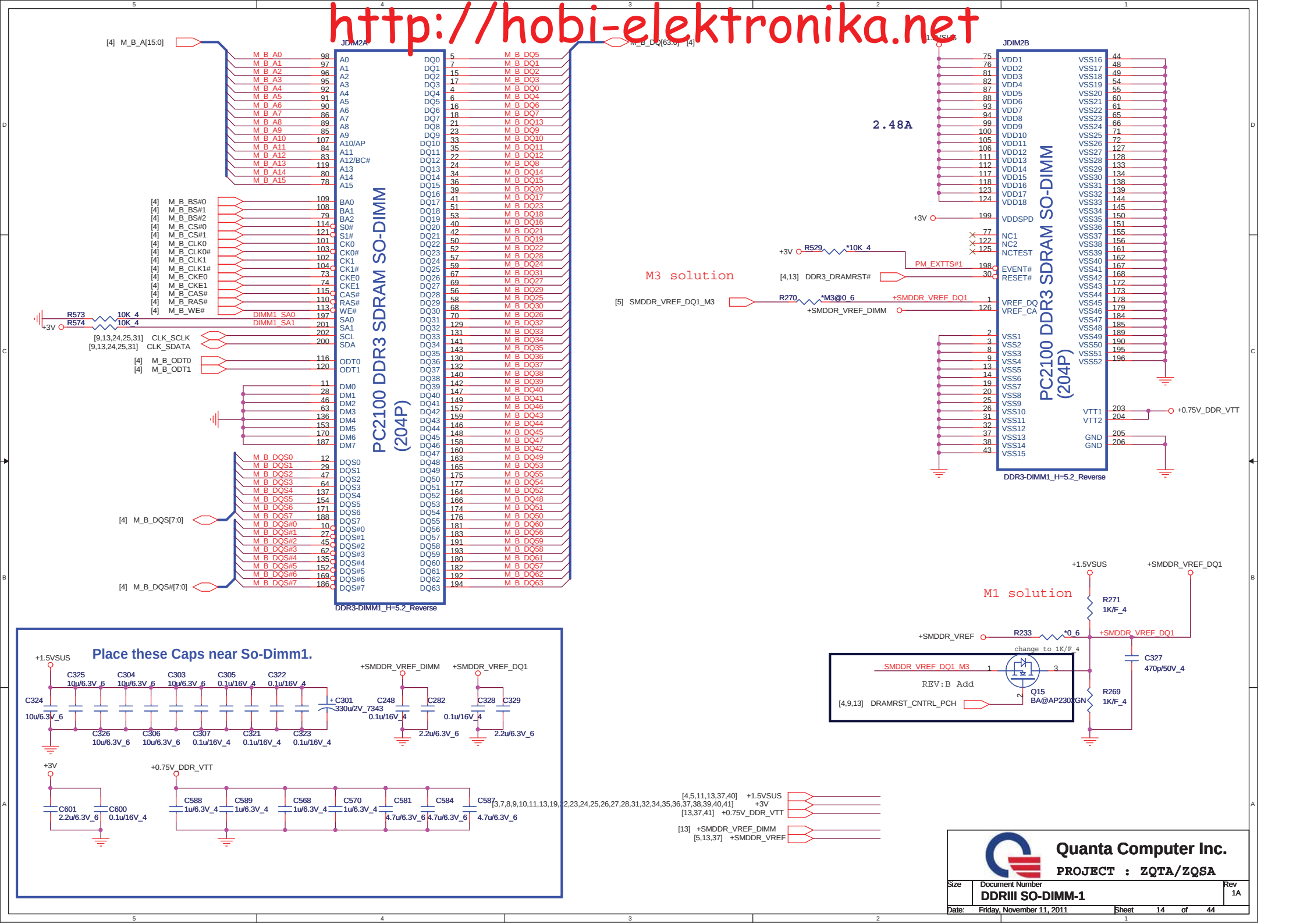
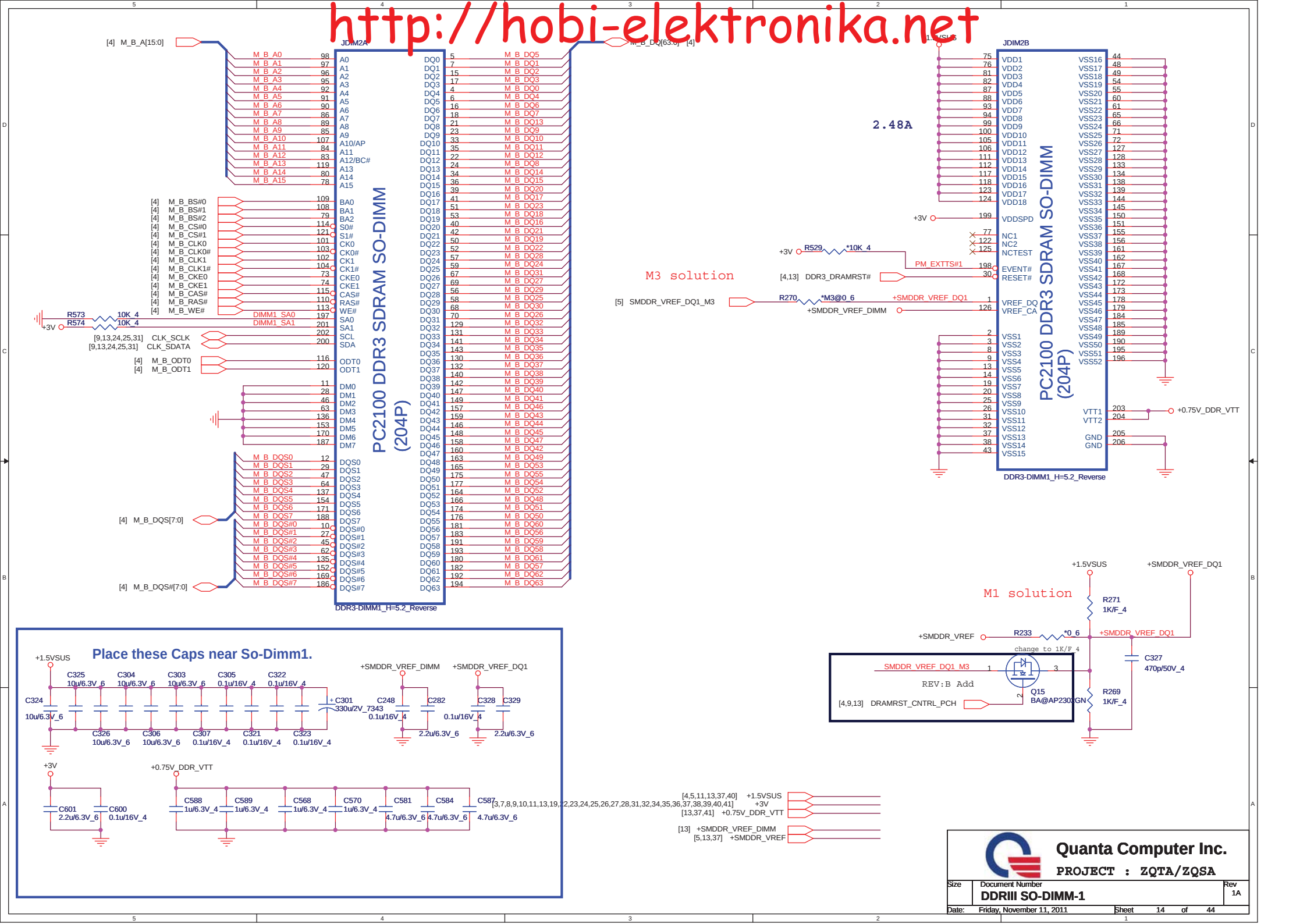
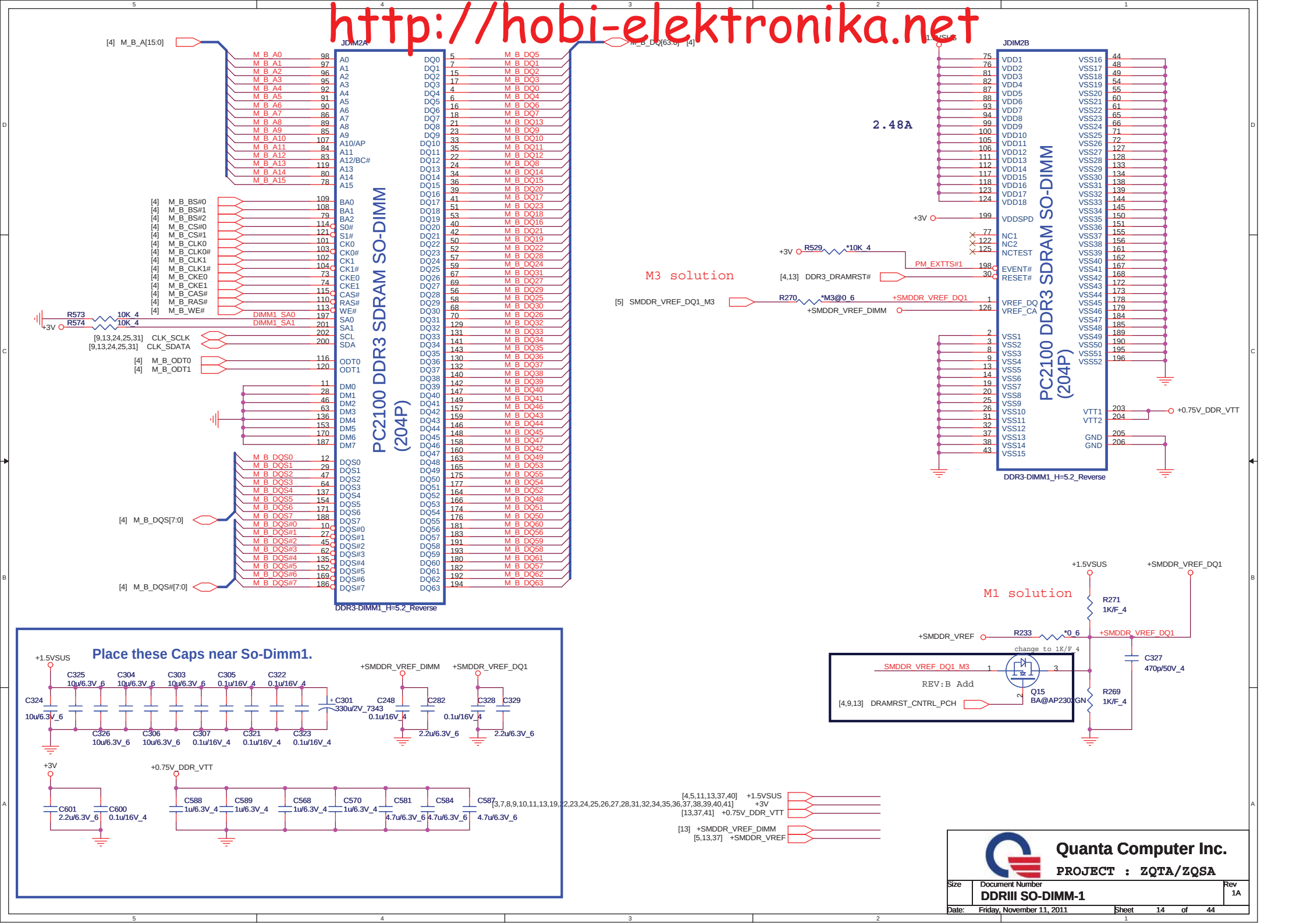


Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

|       |                           |                |
|-------|---------------------------|----------------|
| Size  | Document Number           | Rev            |
|       | Panther Point 6/6         | 1A             |
| Date: | Friday, November 11, 2011 | Sheet 12 of 44 |





1 modify

R384  
EV@10K/F\_4

R649 \*EV@10K/F 4

PEX\_CLKREQ#

10/11 chnagne type

+3V\_GFX

R589 10K/F 4

+3V\_S5

CLK\_PEGA\_REQ# [9]

Q39  
EV@DTC144EUA

Q22  
EV@PDT143TT

+3V\_GFX

10/5 modify

C390  
EV@0.1u/10V\_4

U14  
EV@MC74VHC1G08DF2G

R374  
EV@100K\_4

PEX\_RST#

[9,24,28,32] PLTRST#

[9] DGPU\_HOLD\_RST#

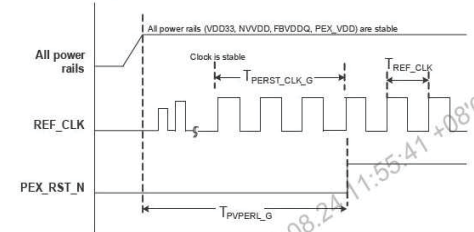
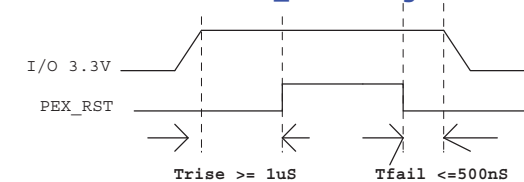


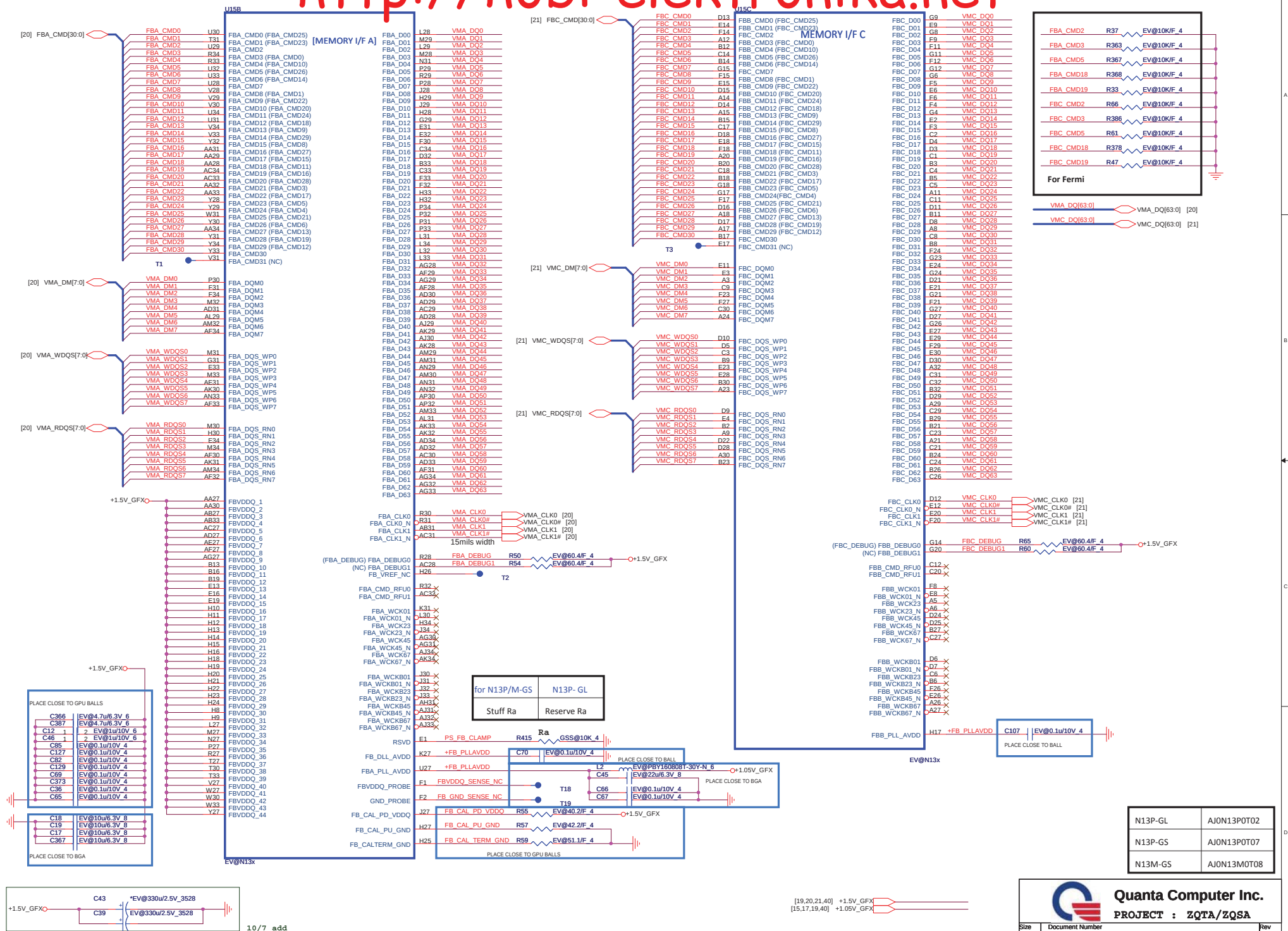
Table 3-8. N11x Reset Requirements for PCI Express 2.0

| Constraint Parameter | Requirement                             | Notes |
|----------------------|-----------------------------------------|-------|
| $T_{FVPERL\_G}$      | $T_{FVPERL\_G} \geq 1\mu s$             |       |
| $T_{FPERST\_CLK\_G}$ | $T_{FPERST\_CLK\_G} \geq 1T_{REF\_CLK}$ |       |

## PEX\_RST timing



|                                                                                                                                                 |                                          |                  |
|-------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|------------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : ZQTA/ZQSA</b> |                                          |                  |
| Size                                                                                                                                            | Document Number<br><b>DGPU 1/5 (PEG)</b> | Rev<br><b>1A</b> |
| Date:                                                                                                                                           | Friday, November 11, 2011                | Sheet 15 of 44   |

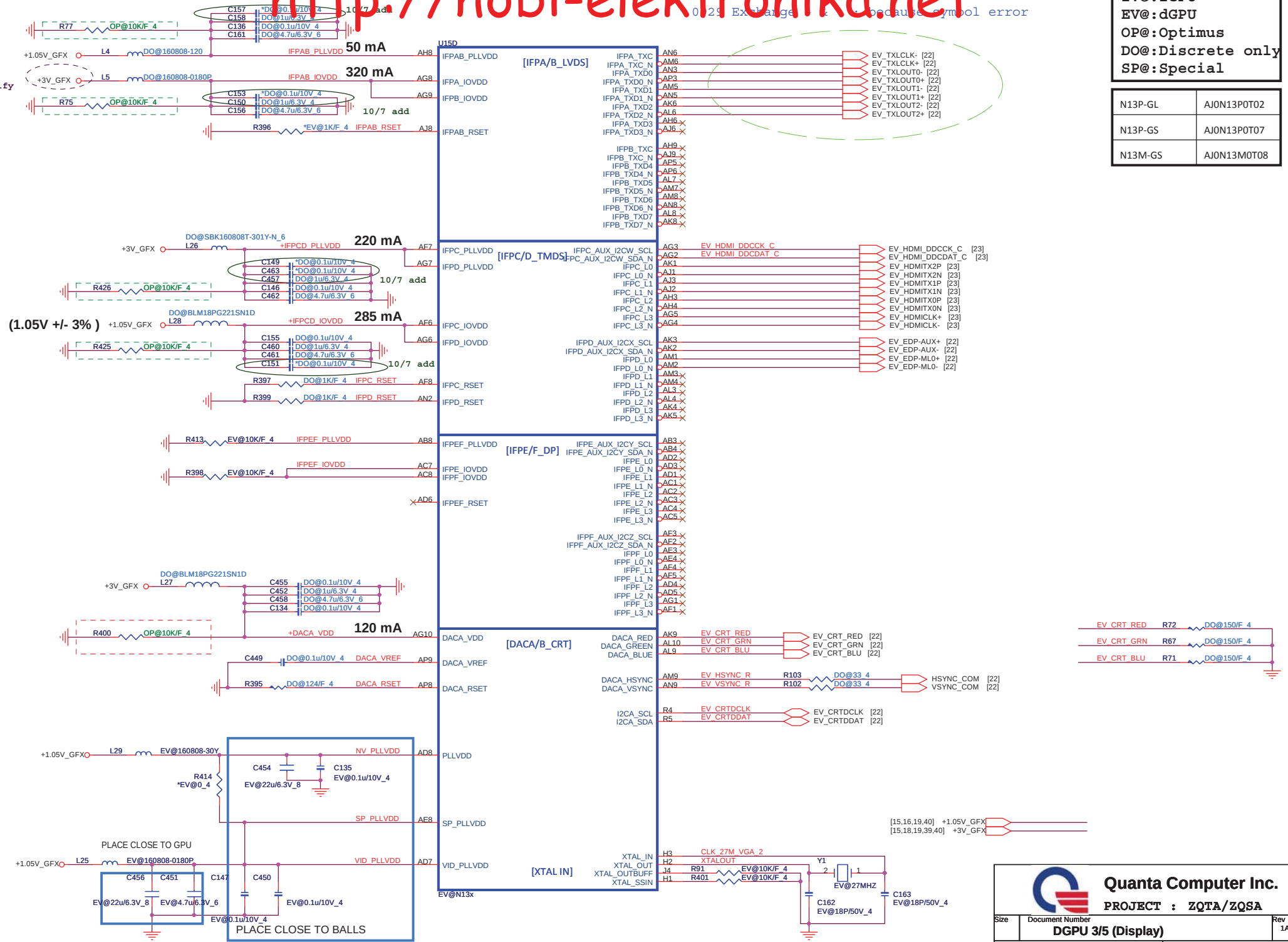


0.25 Exchange because symbol error

IV@:iGPU  
EV@dGPU  
OP@:Optimus  
DO@:Discrete only  
SP@:Special

|         |             |
|---------|-------------|
| N13P-GL | AJON13POT02 |
| N13P-GS | AJON13POT07 |
| N13M-GS | AJON13MOT08 |

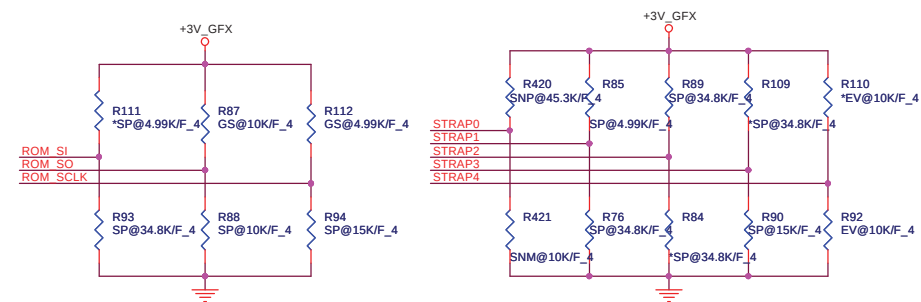
10/6 modify



| Logical Strapping Bit Mapping |        |        |
|-------------------------------|--------|--------|
| PU VDD                        | PU VDD | PU VDD |
| 4.99K                         | 1000   | 0000   |
| 10K                           | 1001   | 0001   |
| 15K                           | 1010   | 0010   |
| 20K                           | 1011   | 0011   |
| 24.9K                         | 1100   | 0100   |
| 30.1K                         | 1101   | 0101   |
| 34.8K                         | 1110   | 0110   |
| 45.3K                         | 1111   | 0111   |

| Logical Strapping Bit2 |                | Logical Strapping Bit1 |                | Logical Strapping Bit0 |      |
|------------------------|----------------|------------------------|----------------|------------------------|------|
| ROM_SO                 | FB_1           | FB_0                   | SMB_ALT_ADDR   | VGA_DEVICE             | 0001 |
| ROM_SCLK               | PCI_DEVID[4]   | SUB_VENDOR             | PCI_DEVID[5]   | PEX_PLL_EN_TERM        | 1010 |
| ROM_SI                 | RAMCFG[3]      | RAMCFG[2]              | RAMCFG[1]      | RAMCFG[0]              | XXXX |
| STRAP0                 | USER[3]        | USER[2]                | USER[1]        | USER[0]                | 1111 |
| STRAP1                 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2]         | 3GIO_PADCFG[1] | 3GIO_PADCFG[0]         | 0110 |
| STRAP2                 | PCI_DEVID[3]   | PCI_DEVID[2]           | PCI_DEVID[1]   | PCI_DEVID[0]           | 1110 |
| STRAP3                 | SOR3_EXPOSED   | SOR2_EXPOSED           | SOR1_EXPOSED   | SOR0_EXPOSED           | 0010 |
| STRAP4                 | RESERVED       | PCI SPEED CHANGE GEN3  | PCI_MAX SPEED  | DP_PLL_VDD33           | 0011 |

|         |             |
|---------|-------------|
| N13P-GL | AJ0N13P0T02 |
| N13P-GS | AJ001070T00 |
| N13M-GS | AJ001170T00 |



N13P-GS/-GL Strapping table

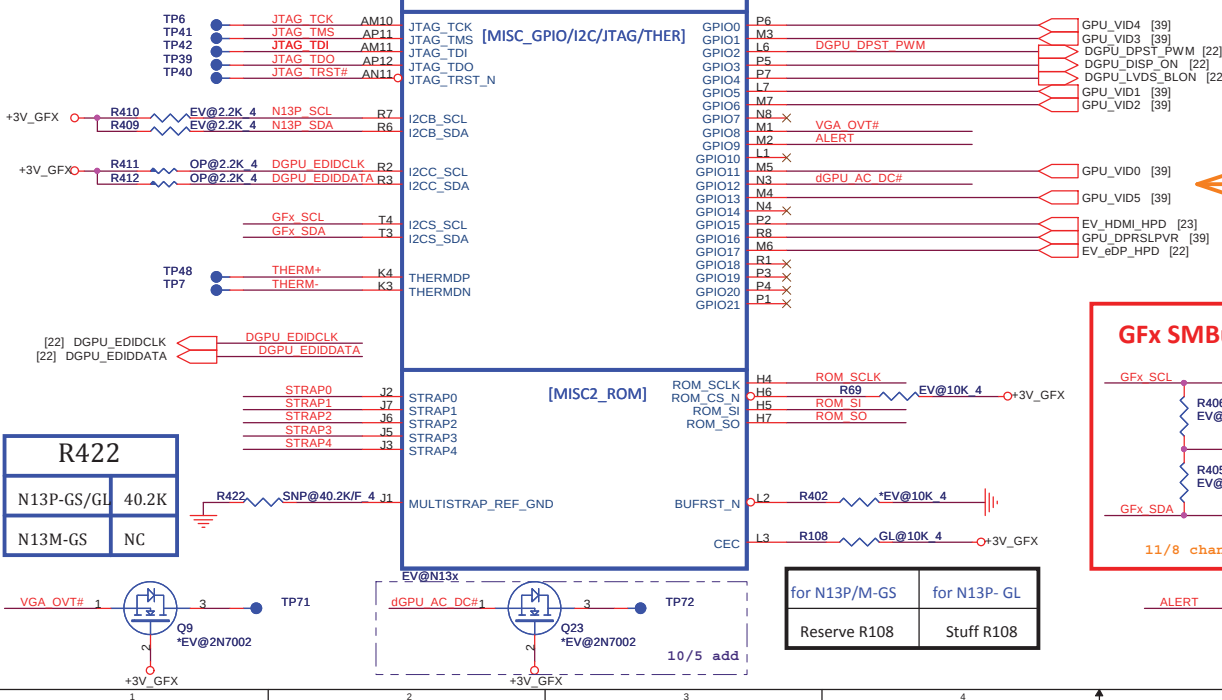
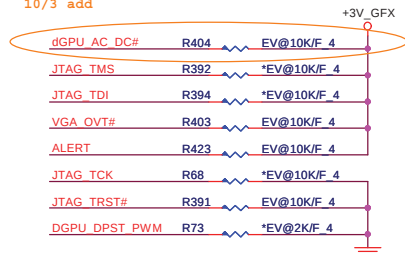
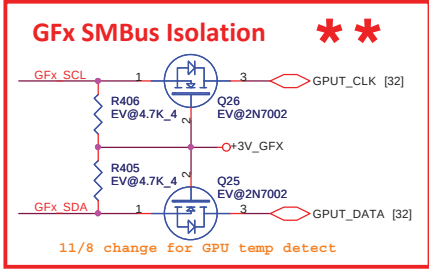
|        |                                                                                                                                |        |                                          |          |                                                          |
|--------|--------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------|----------|----------------------------------------------------------|
| ROM_SI | 1G Hynix 64Mx16 -->15K PD<br>1G Micron 64Mx16 -->20K PD<br>2G Hynix 128Mx16 -->35K PD (Default)<br>2G Micron 128Mx16 -->45K PD | ROM_SO | N13P-GL --> 10K PD<br>N13P-GS --> 10K PU | ROM_SCLK | N13P-GL (0010) --> 15k PD<br>N13P-GS (1000) --> 4.99K PU |
|--------|--------------------------------------------------------------------------------------------------------------------------------|--------|------------------------------------------|----------|----------------------------------------------------------|

N13M-GS Strapping table

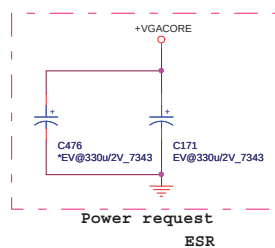
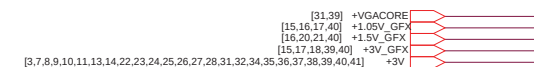
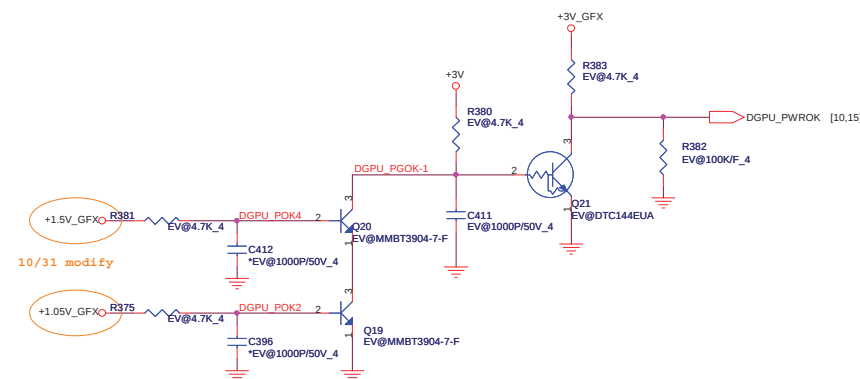
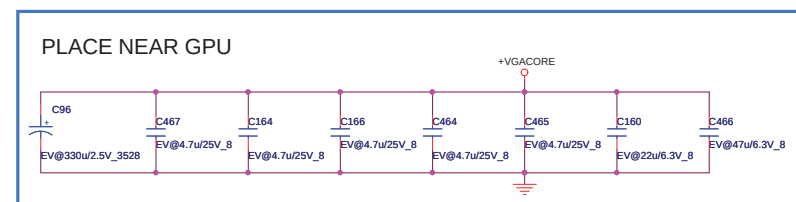
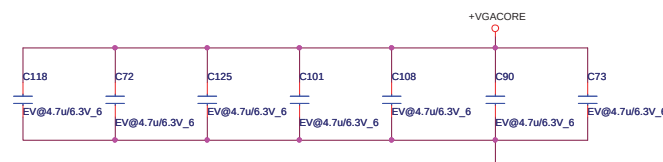
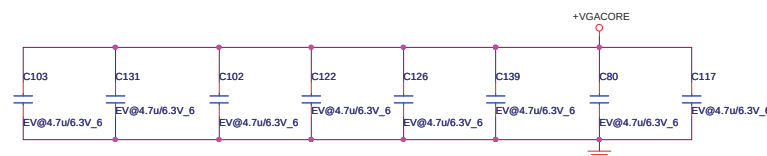
| Pin Name    | Strap Mapping  | Value                                     |
|-------------|----------------|-------------------------------------------|
| ROM_SCLK    | SMB_ALT_ADDR   | 0                                         |
| ROM_SI      | SUB_VENDOR     | 0                                         |
| ROM_SO      | VGA_DEVICE     | 0                                         |
| STRAP[3..0] | RAM_CFG[3..0]  | 0010(Hynix 64Mx16)<br>0110(Hynix 128Mx16) |
| STRAP[4]    | PCIE_MAX_SPEED | 0                                         |

Remark :

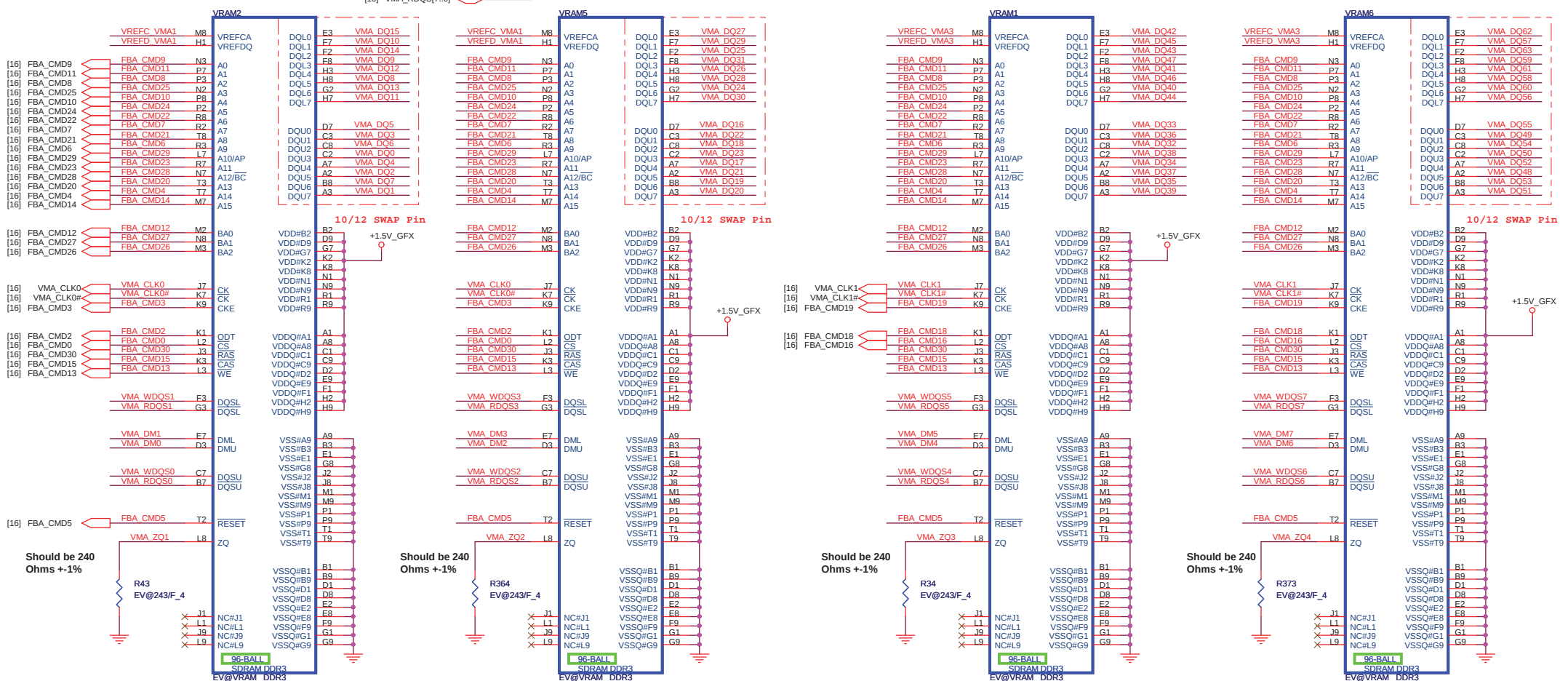
0 -> 10K PD  
1 -> 10K PU



|               |              |
|---------------|--------------|
| for N13P/M-GS | for N13P- GL |
| Reserve R108  | Stuff R108   |



CHANNEL A: 256MB/512MB DDR3

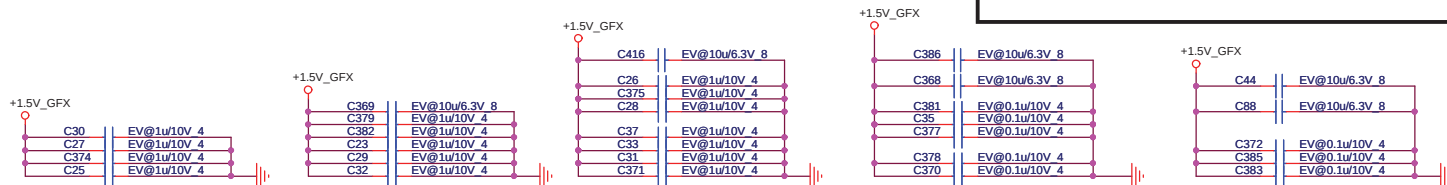


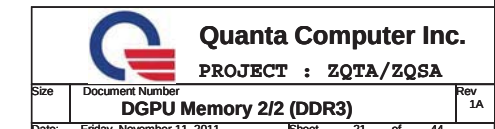
VMA\_CLK0  
R371 EV@162F\_4  
VMA\_CLK0#

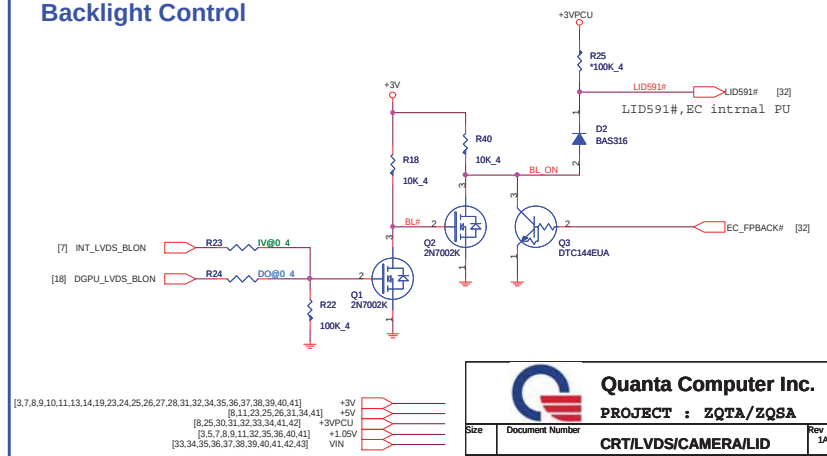
Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)  
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)

VMA\_CLK1  
R41 EV@162F\_4  
VMA\_CLK1#

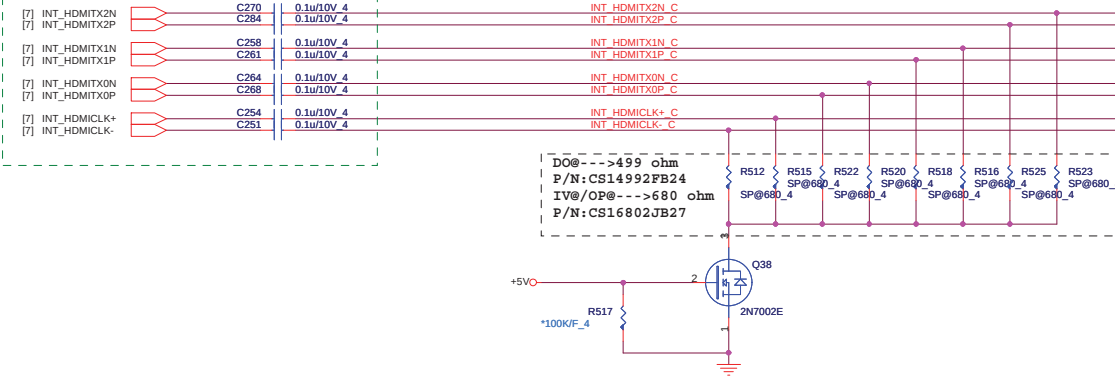
Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)  
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)







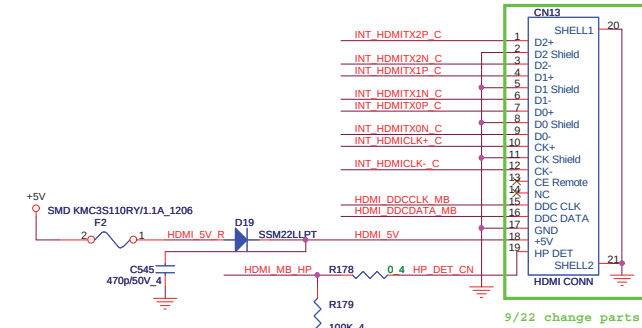
## From PCH



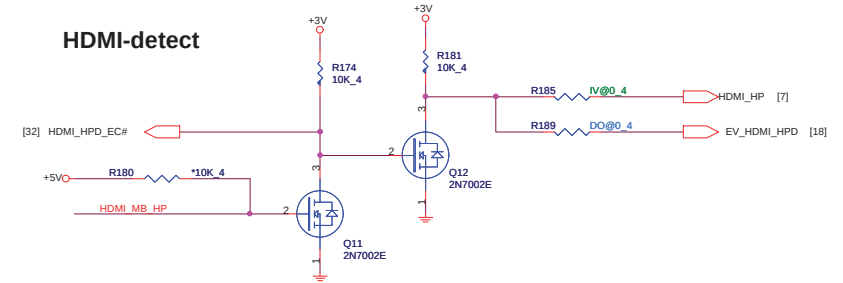
## From EXT VGA



IV@:iGPU  
EV@:dGPU  
OP@:Optimus  
DO@:Discrete only  
SP@:Special



## HDMI-detect



## I2C

|     |              |             |
|-----|--------------|-------------|
| UMA | R239<br>R245 | CS22202JB18 |
| DIS | R239<br>R245 | CS24702JB38 |

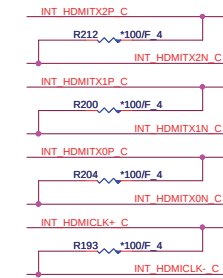
## From EXT VGA

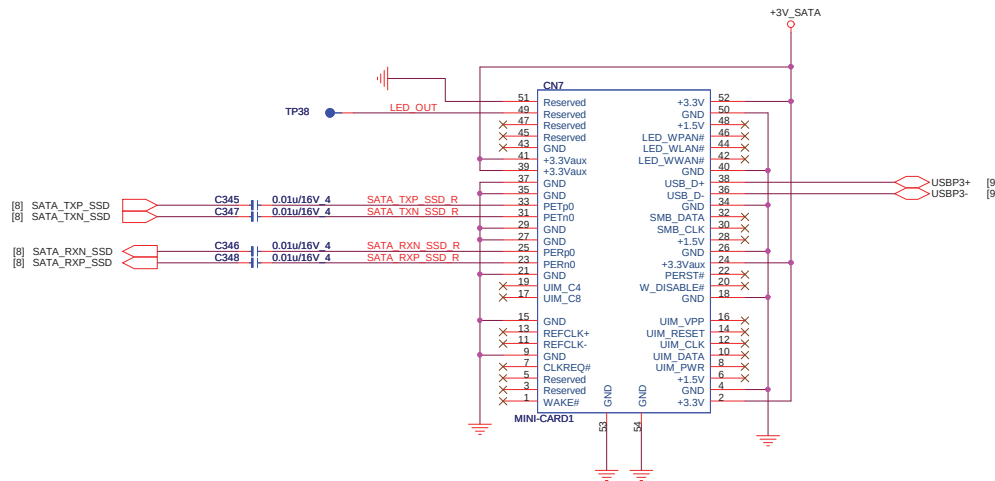
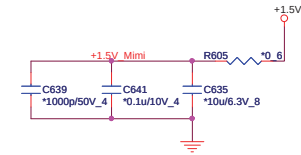


## From PCH

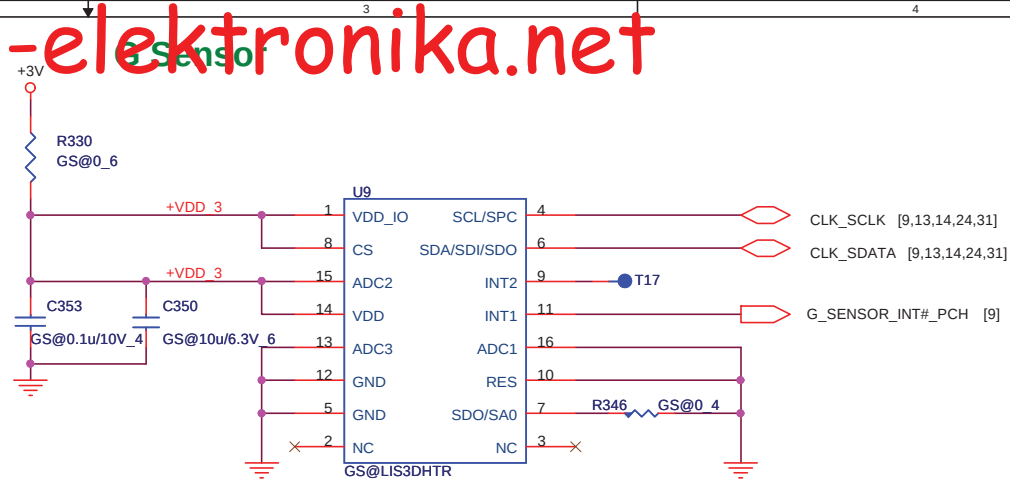
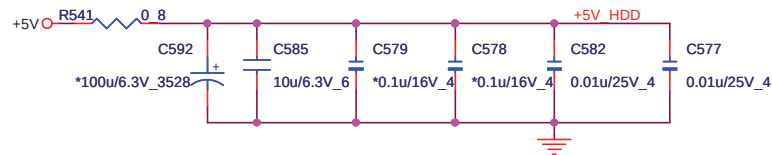
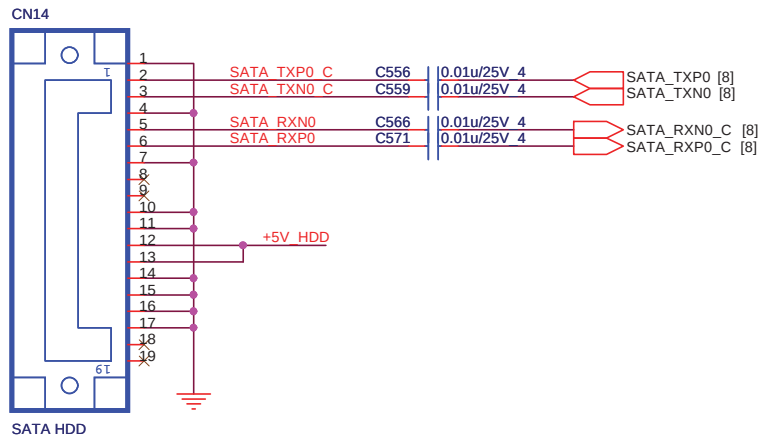


## EMI



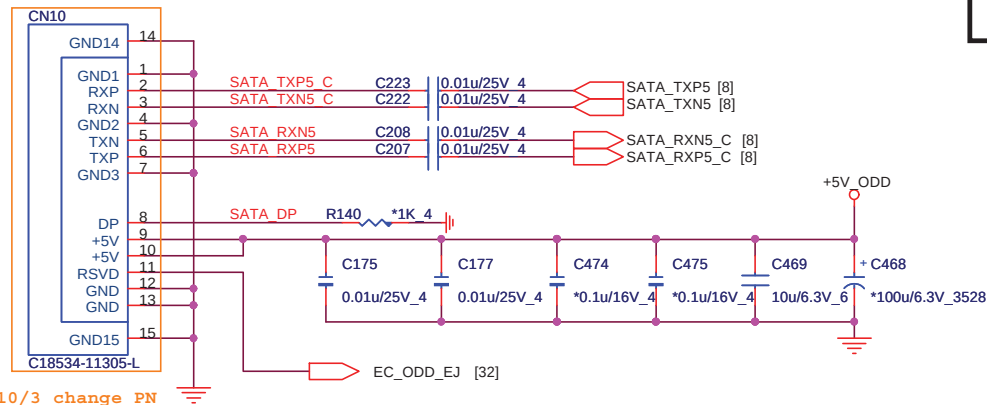


## MAIN SATA HDD(HDD)



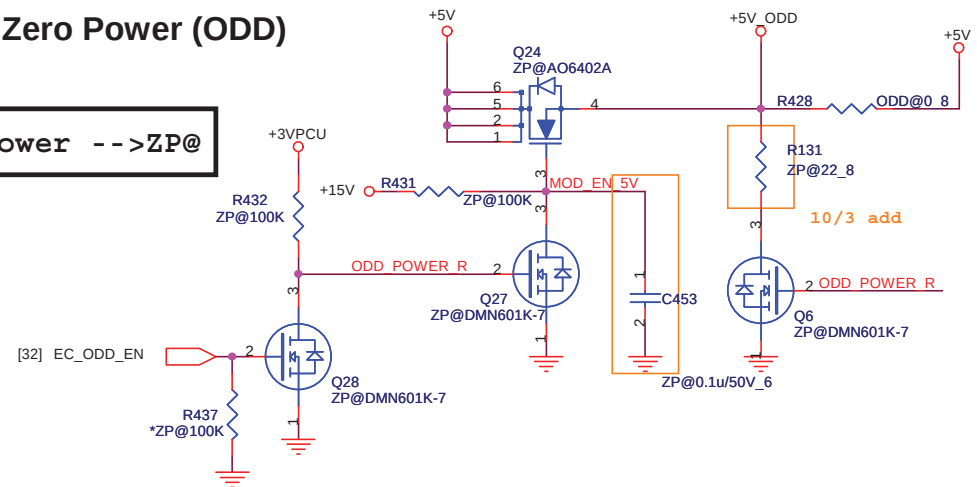
G-Sensor -->GS@

## ODD (ODD)



## Zero Power (ODD)

Zero Power -->ZP@

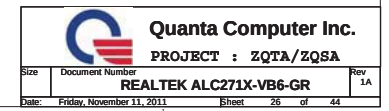


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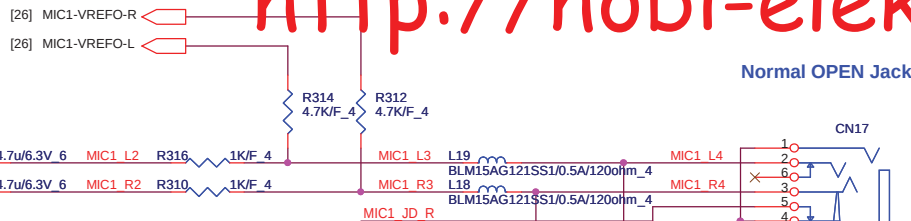
PROJECT : ZQTA/ZQSA

| Size | Document Number       | Rev |
|------|-----------------------|-----|
|      | SATA-HDD/ODD/G Sensor | 1A  |

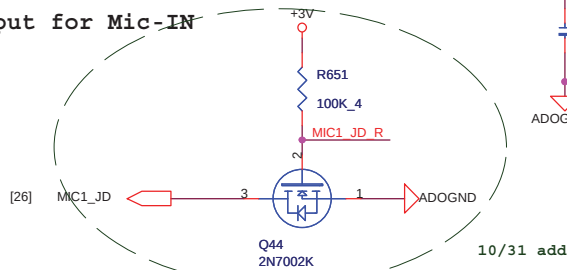
Date: Friday, November 11, 2011 Sheet 25 of 44



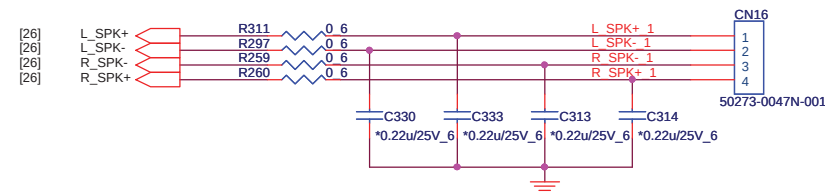
## MIC



Max. 100mVrms input for Mic-IN

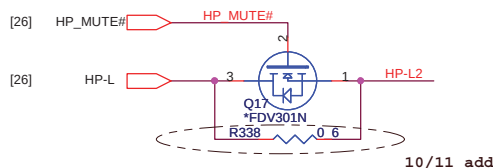


## Internal Speaker

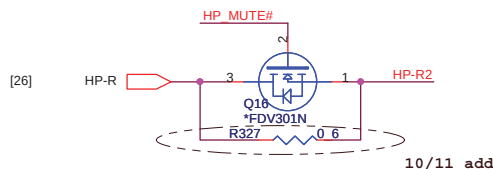


9/19 modify

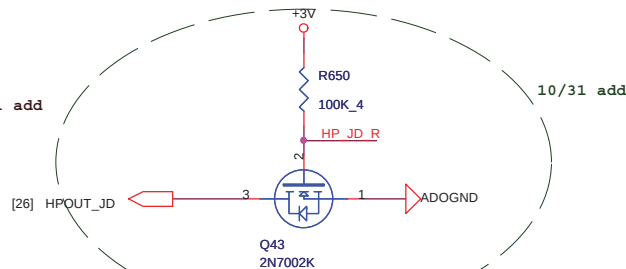
## HP



10/11 add

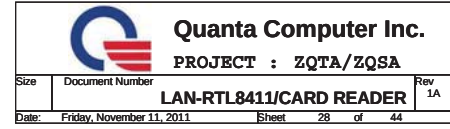
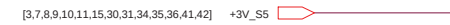


10/11 add



10/31 add

10/31 add

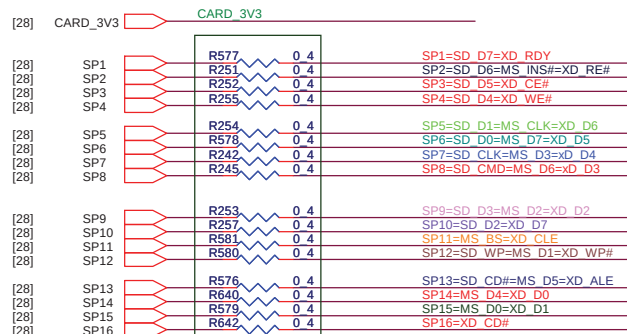


# CARD READER CONNECTOR

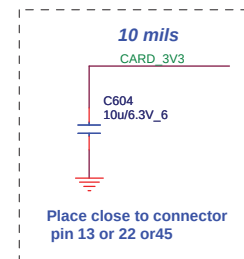
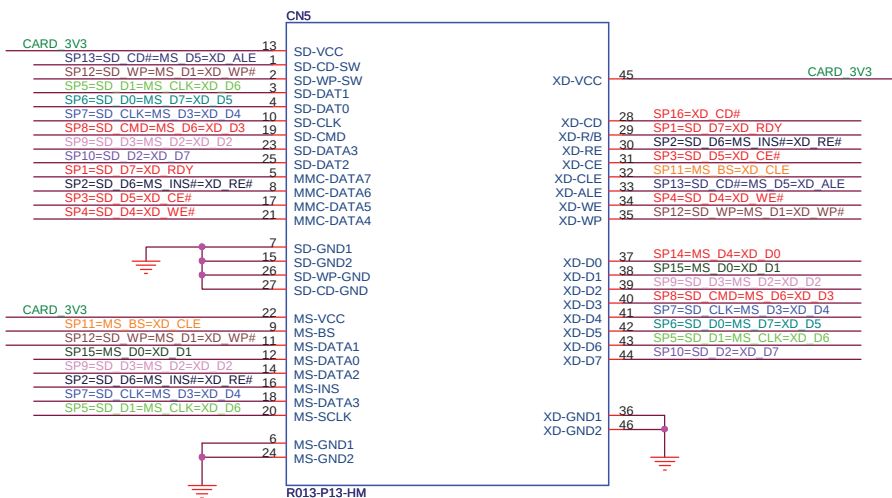
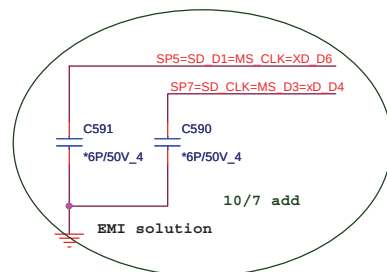
## XD, MMC 42/SD, MS/MSP 7 IN1 CARD READER

### Share Pin

|      |        |         |        |
|------|--------|---------|--------|
| SP1  | SD_D7  |         | xD_RDY |
| SP2  | SD_D6  | MS_INS# | xD_RE# |
| SP3  | SD_D5  |         | xD_CE# |
| SP4  | SD_D4  |         | xD_WE# |
| SP5  | SD_D1  | MS_CLK  | xD_D6  |
| SP6  | SD_D0  | MS_D7   | xD_D5  |
| SP7  | SD_CLK | MS_D3   | xD_D4  |
| SP8  | SD_CMD | MS_D6   | xD_D3  |
| SP9  | SD_D3  | MS_D2   | xD_D2  |
| SP10 | SD_D2  |         | xD_D7  |
| SP11 |        | MS_BS   | xD_CLE |
| SP12 | SD_WP  | MS_D1   | xD_WP# |
| SP13 | SD_CD# | MS_D5   | xD_ALE |
| SP14 |        | MS_D4   | xD_D0  |
| SP15 |        | MS_D0   | xD_D1  |
| SP16 |        |         | xD_CD# |

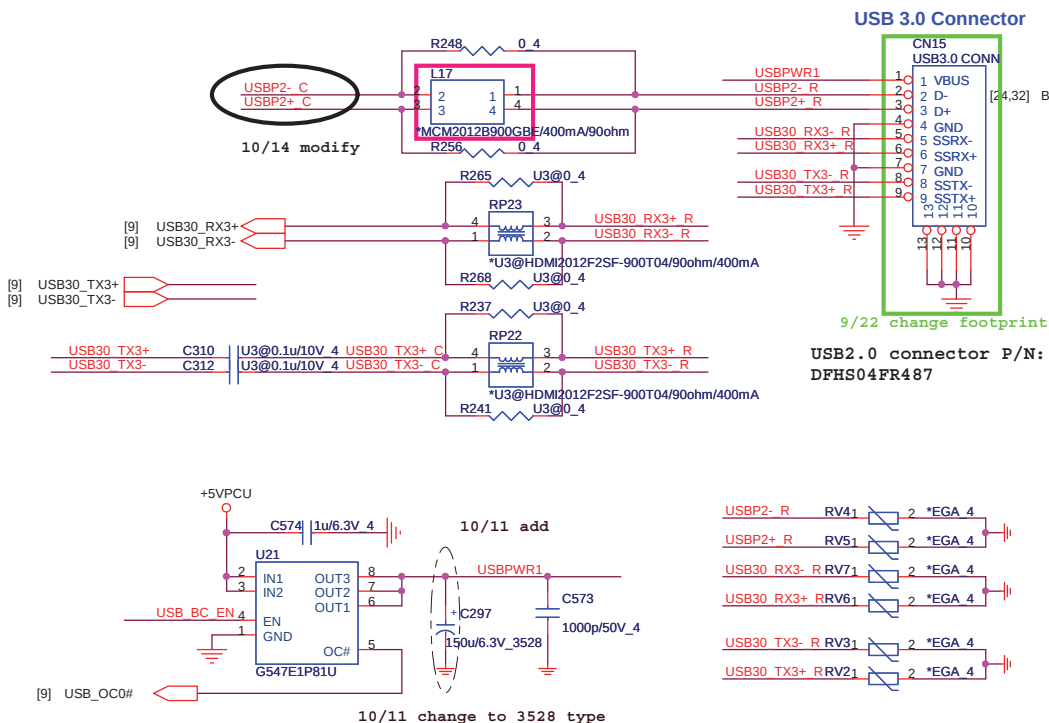


10/7 change 0 ohm



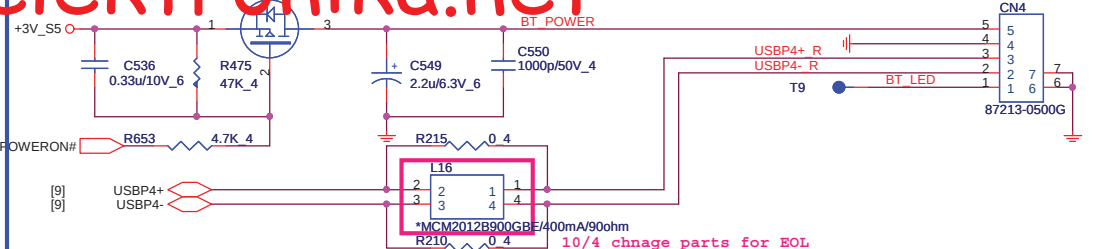
# USB3.0/2.0

http://hobi-elektronika.net

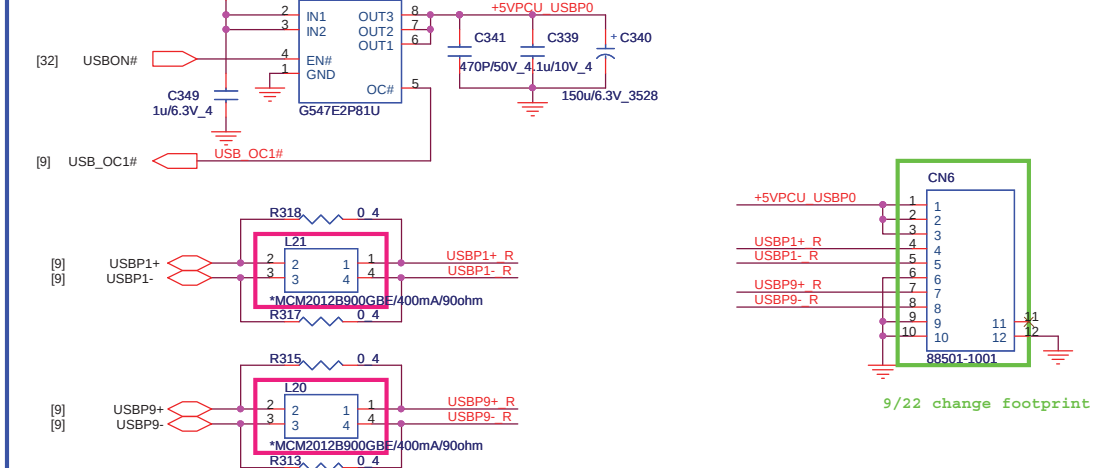


# Bluetooth

# BLUETOOTH CONNECTOR for BT3.0

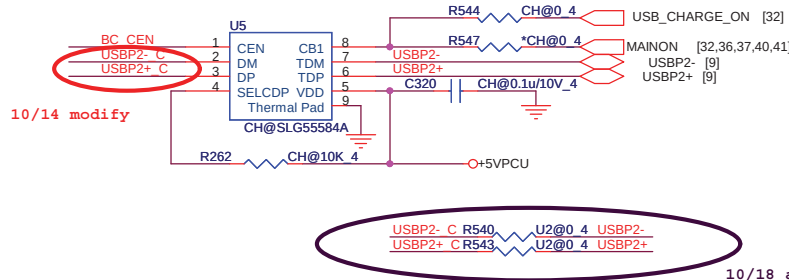


# USB/B

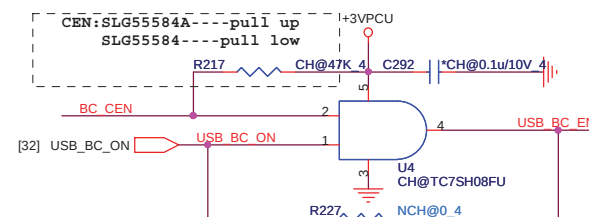


# USB Charger to 3.0

| CB | SELCDP | Function                                                        |
|----|--------|-----------------------------------------------------------------|
| 0  | X      | DCF autodetect with mouse/keyboard wakeup                       |
| 1  | 0      | S0 charging with SDP only                                       |
| 1  | 1      | S0 charging with CDP or SDP only (depending on external device) |



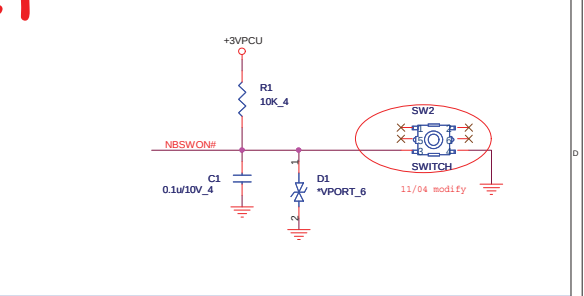
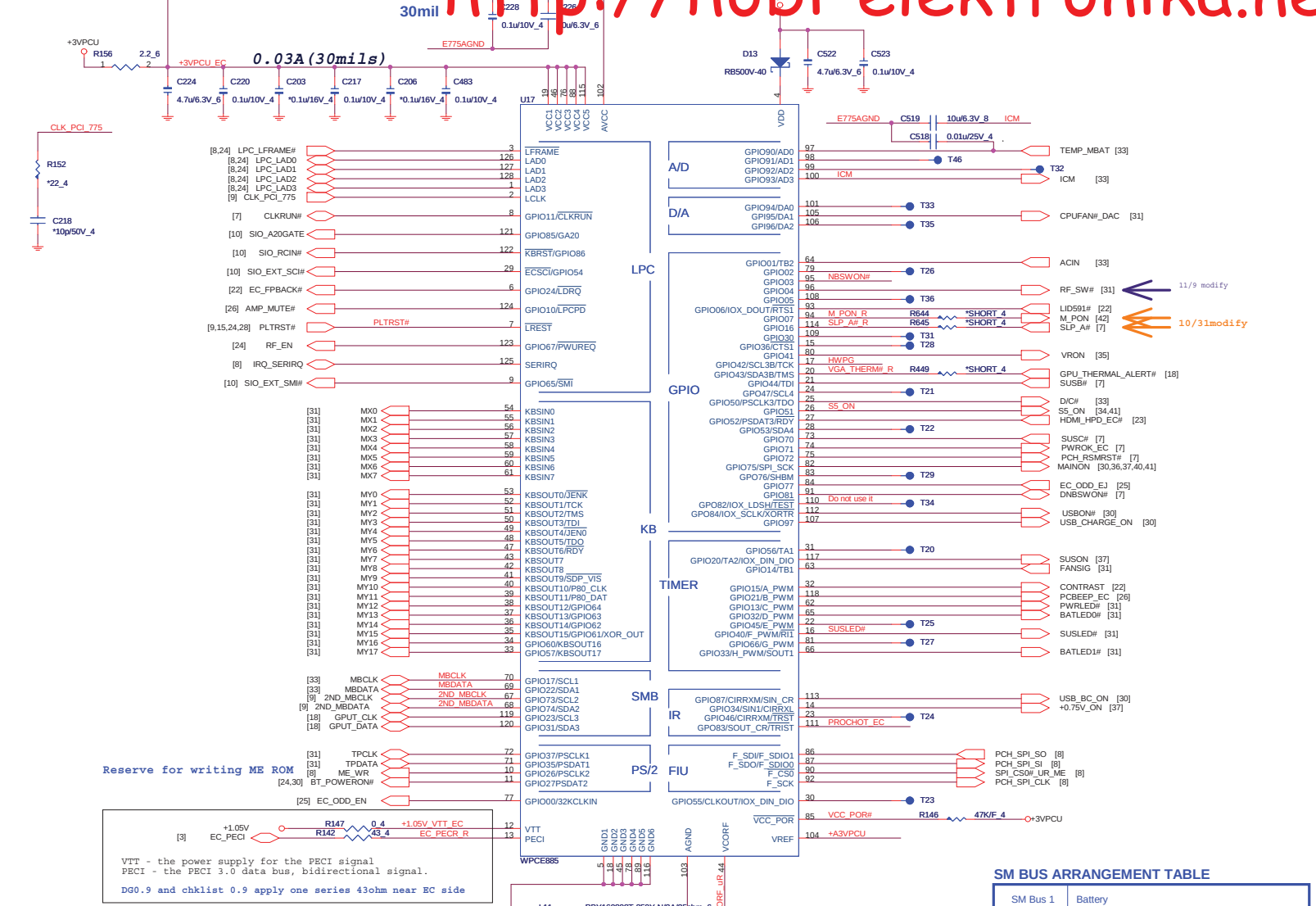
USB Charger -->CH@  
None Charger--> NCH@



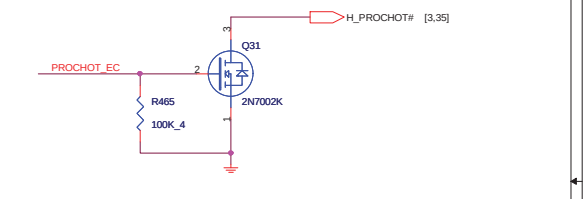
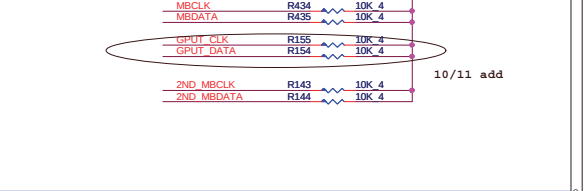
Quanta Computer Inc.  
PROJECT : ZQTA/ZQSA

| Size  | Document Number           | Rev            |
|-------|---------------------------|----------------|
|       | USB/ BT/CHARGER           | 1A             |
| Date: | Friday, November 11, 2011 | Sheet 30 of 44 |

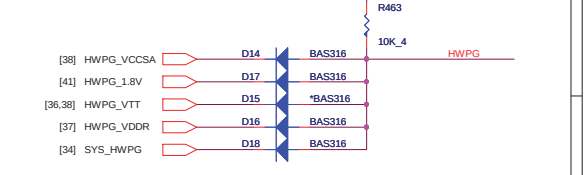




SM BUS PU(KBC)

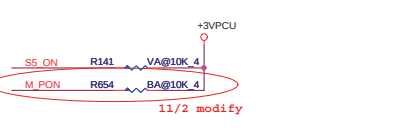


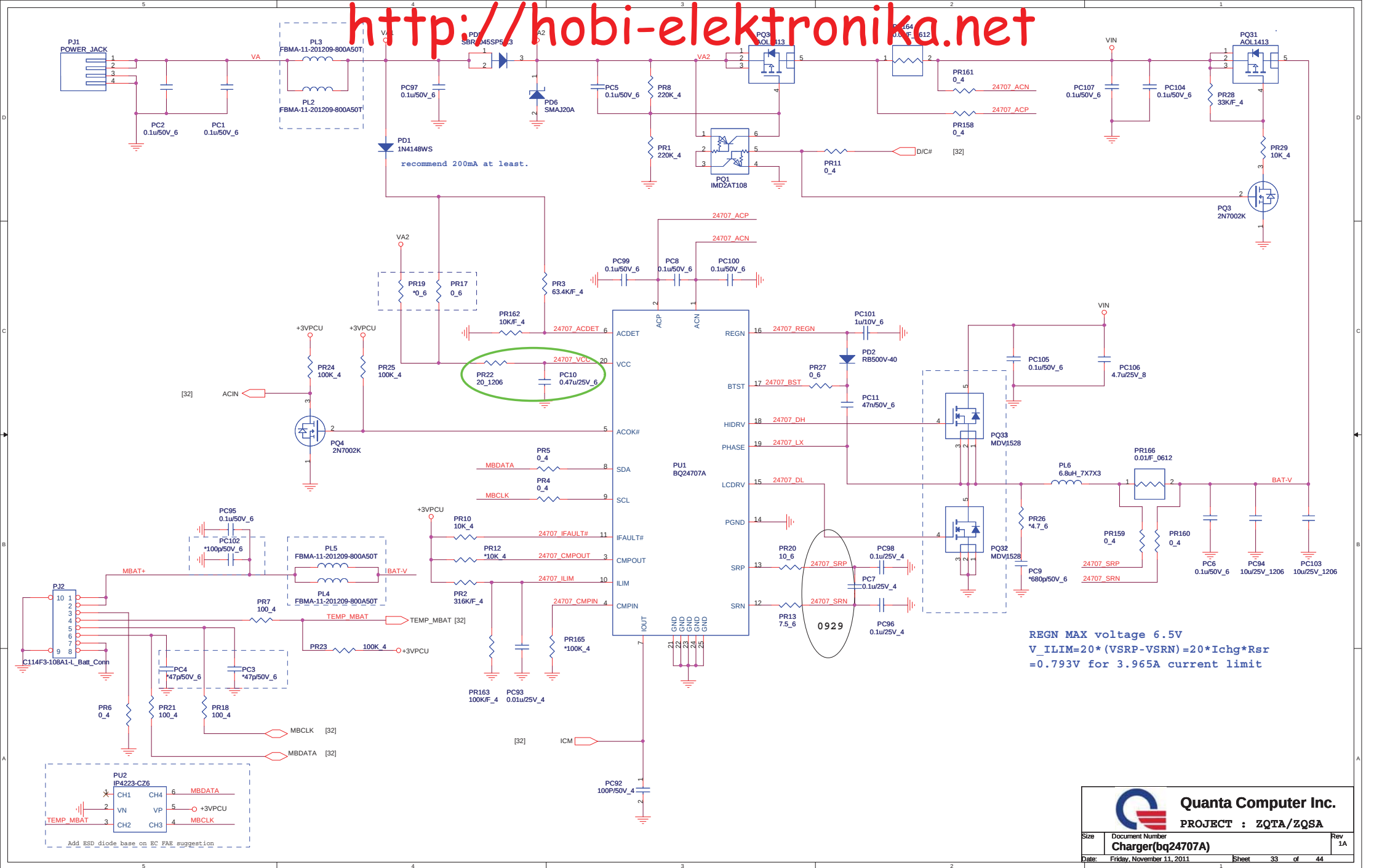
HWPGR(KBC)

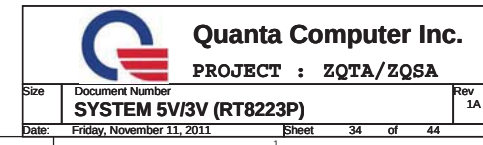
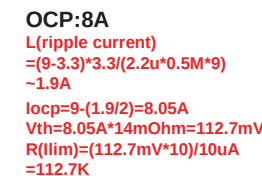


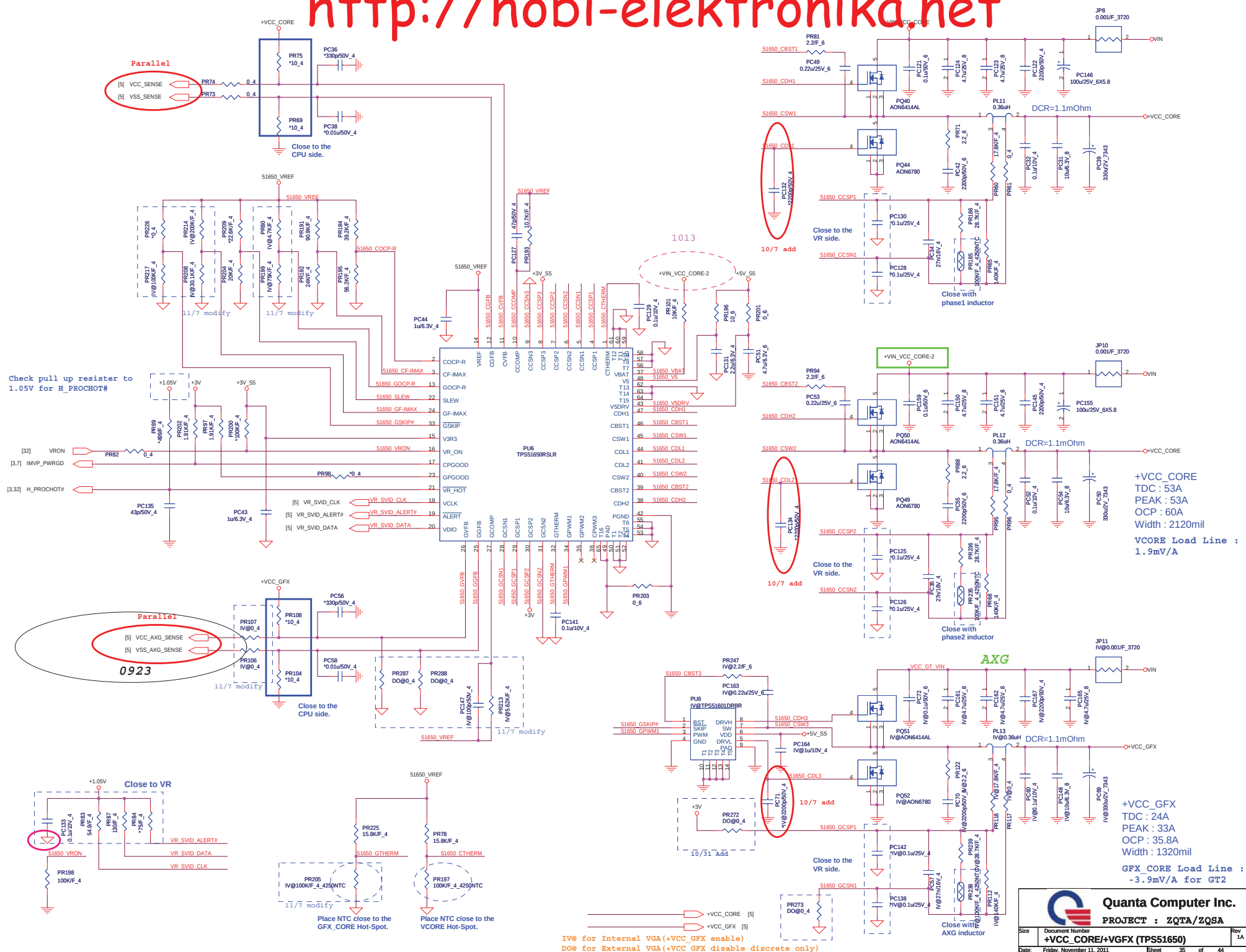
SM BUS ARRANGEMENT TABLE

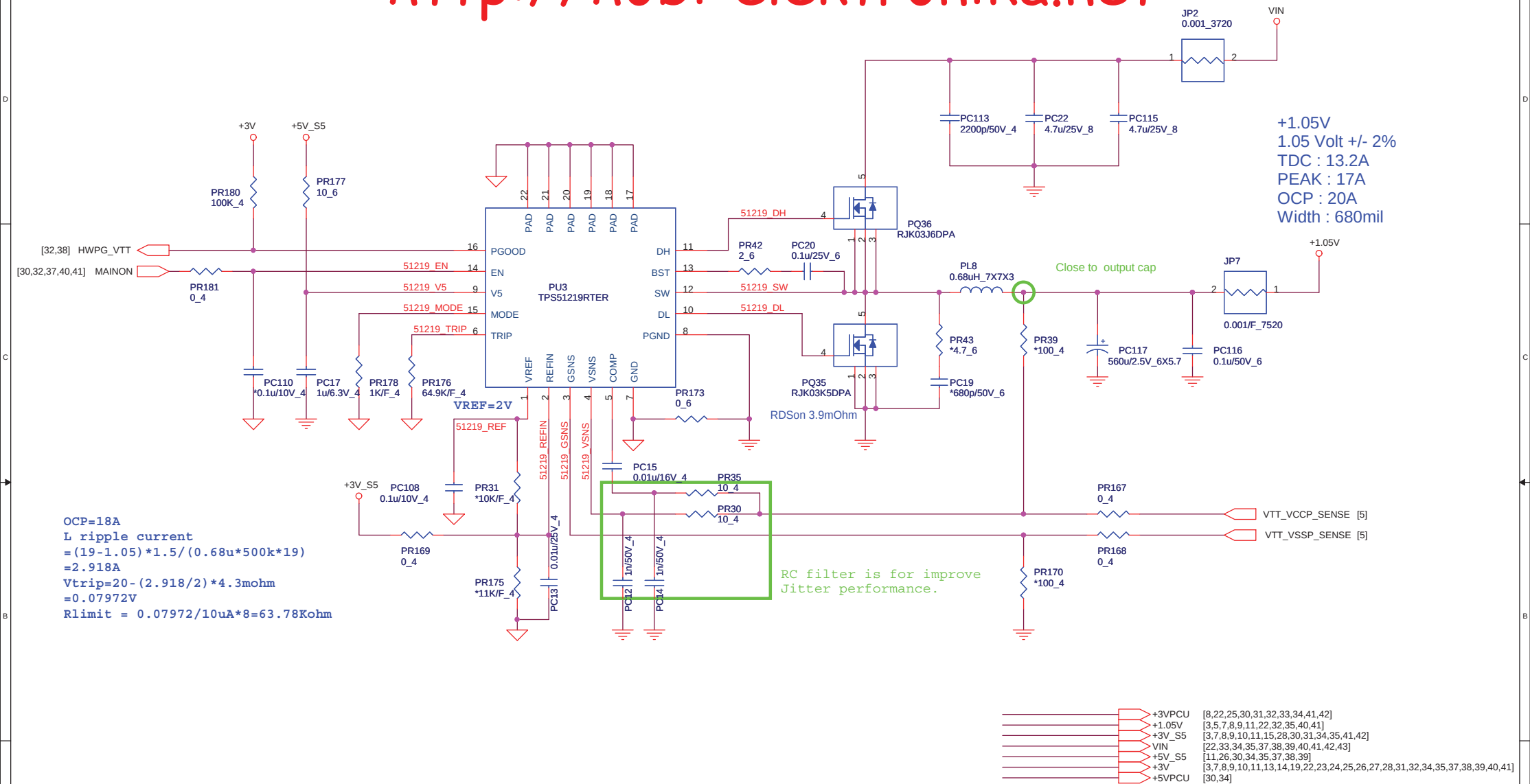
|          |         |
|----------|---------|
| SM Bus 1 | Battery |
| SM Bus 2 | PCH     |
| SM Bus 3 | VGA     |
| SM Bus 4 | HDMI    |











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PROJECT : ZQTA/ZQSA

|      |                          |     |
|------|--------------------------|-----|
| Size | Document Number          | Rev |
|      | <b>+1.05V (TPS51219)</b> | 1A  |

Date: Friday, November 11, 2011 Sheet 36 of 44

TDC : 0.38A  
PEAK : 0.5A  
Width : 20mil

TDC : 0.75A  
PEAK : 1A  
Width : 40mil

+SMDDR\_VREF

PC182  
0.22u/10V\_4

PR265  
100K/F\_4

VREF=1.8V

PC183  
0.1u/10V\_4

PR260  
51K/F\_4

PC181  
0.01u/25V\_4

Close to IC

Greater than or equal 40mil

+5V\_S5

PC87  
1u/10V\_4

PC184  
10u/6.3V\_8

JP18  
0.001\_3720

PC194  
4.7u/25V\_8

JP17  
0.001/F\_7520

+1.5V\_SUS  
1.5 Volt +/- 5%  
TDC : 14.67A  
PEAK : 18A  
OCP : 20A  
Width : 600mil

Close to output cap

TDC : 0.38A  
PEAK : 0.5A  
Width : 20mil

OCP=20A  
I ripple current  
= (19-1.5)\*1.5/(0.68u\*400k\*19)  
=5.079A  
Vtrip=20-(5.079/2)\*4.3mohm  
=0.07508V  
Rlimit=0.07508/10uA\*8=60.063Kohm

|                 | S3 | S5 | +1.5VSUS | REF | VTT |
|-----------------|----|----|----------|-----|-----|
| S0              | 1  | 1  | ON       | ON  | ON  |
| S3 (mainon off) | 0  | 1  | ON       | ON  | OFF |
| S4/S5           | 0  | 0  | OFF      | OFF | OFF |

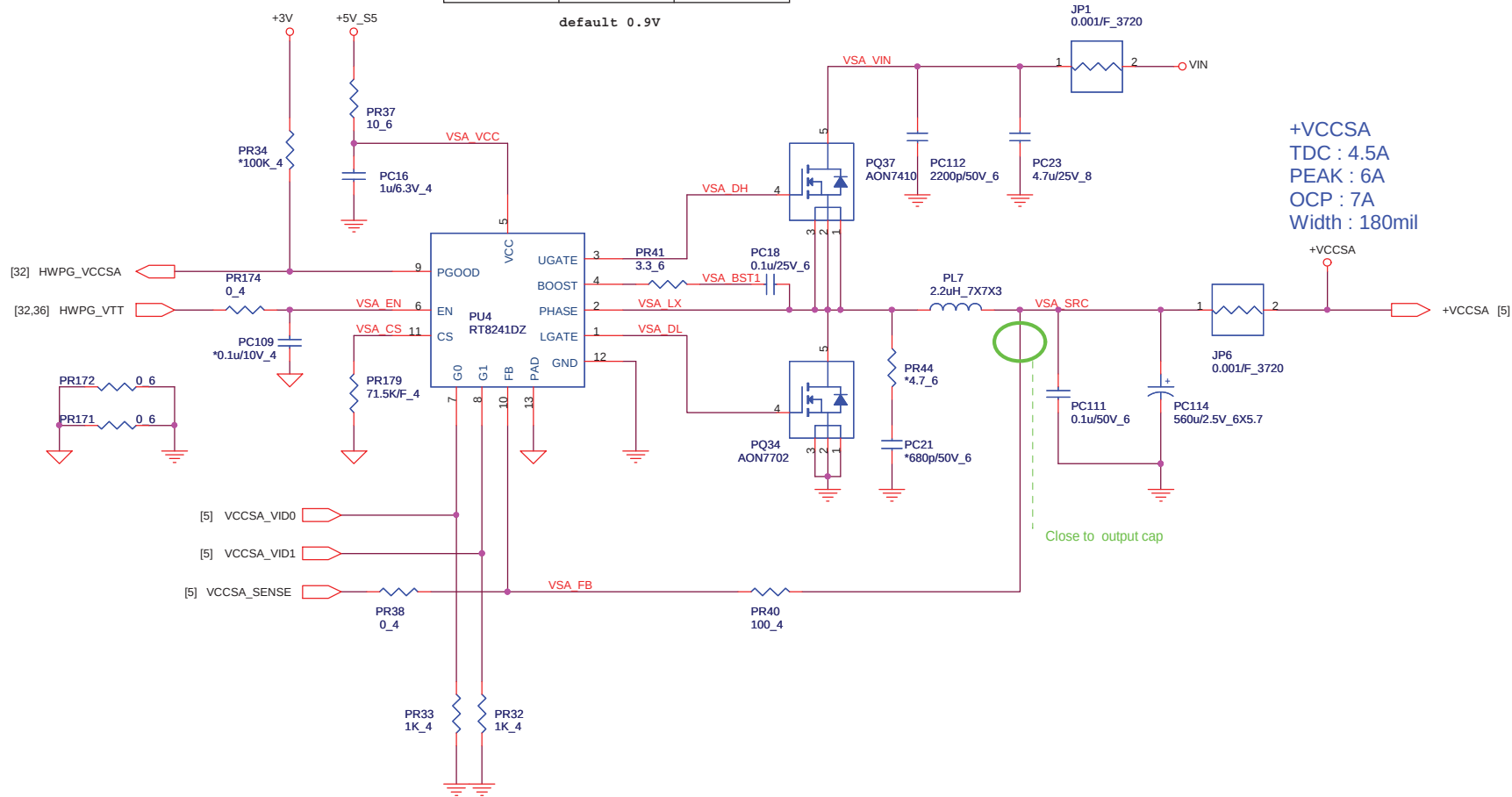


**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

|      |                           |                |
|------|---------------------------|----------------|
| Size | Document Number           | Rev            |
|      | <b>DDR 1.5V(TPS51216)</b> | 1A             |
| Date | Friday, November 11, 2011 | Sheet 37 of 44 |

| G0 | G1 | +VCCSA |
|----|----|--------|
| 0  | 0  | 0.9V   |
| 0  | 1  | 0.8V   |
| 1  | 0  | 0.725V |
| 1  | 1  | 0.675V |

default 0.9V



+VCCSA  
TDC : 4.5A  
PEAK : 6A  
OCP : 7A  
Width : 180mil

Close to output cap

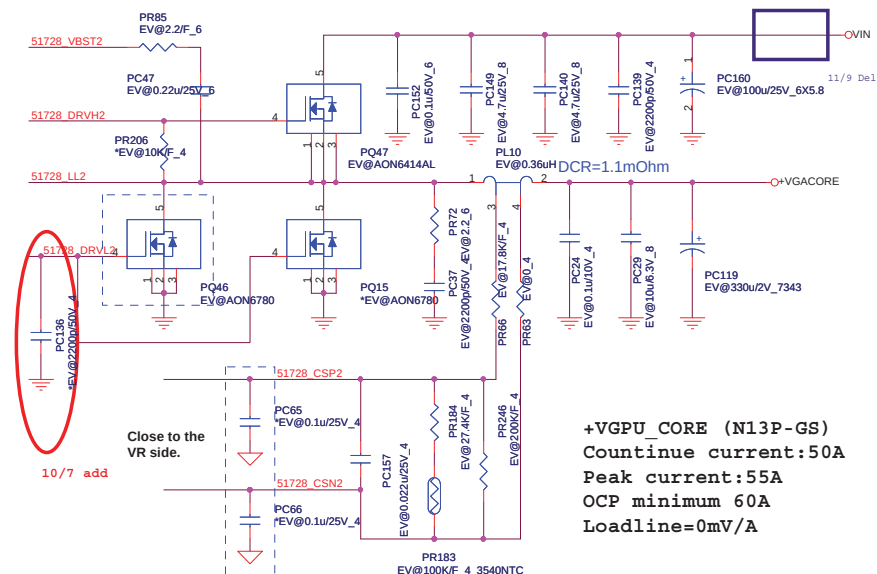
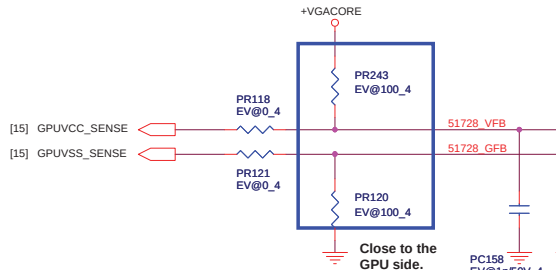
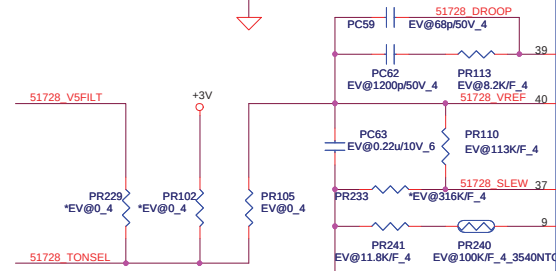
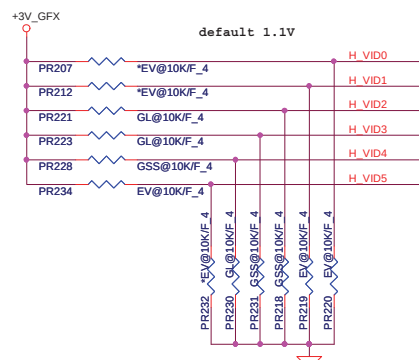
OCP=7A  
Iripple=(19-0.9)\*0.9/(2.2u\*300K\*19)  
=1.299A  
Rth=14mohm\*8\*(7-0.65)/10uA  
=71.125K  
Ipeak=8.299A



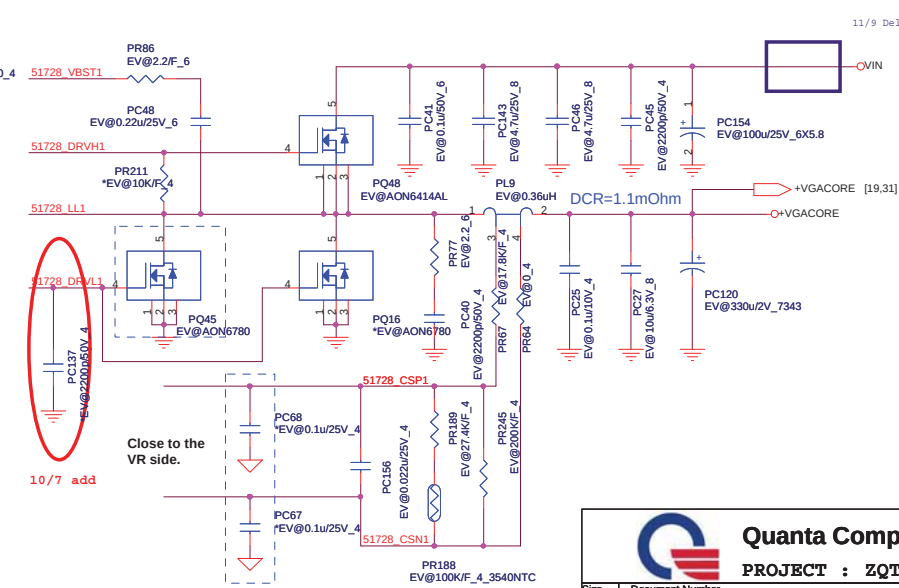
Quanta Computer Inc.

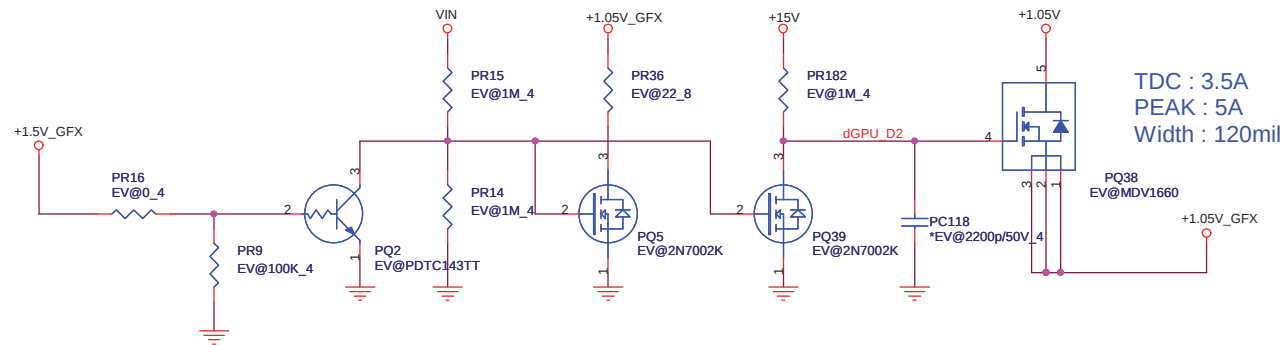
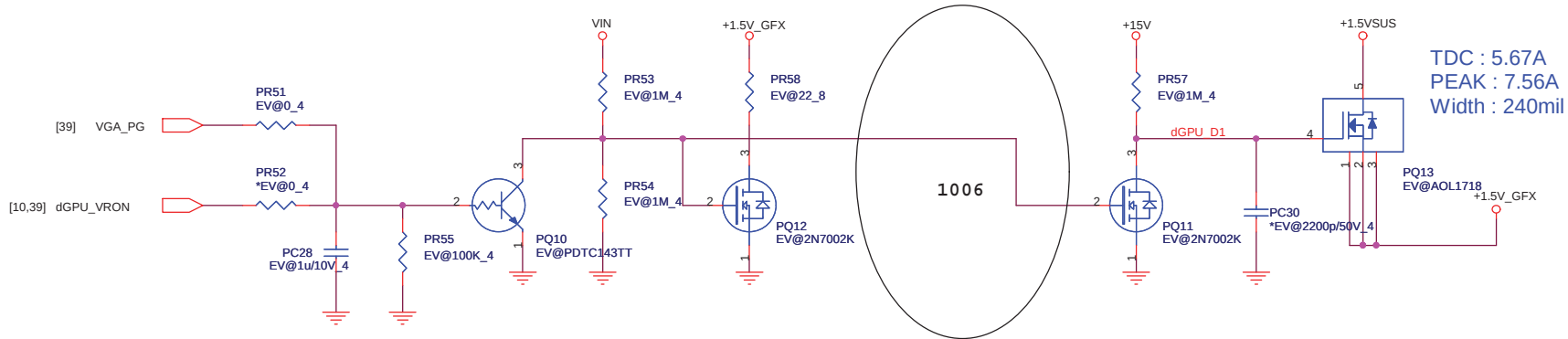
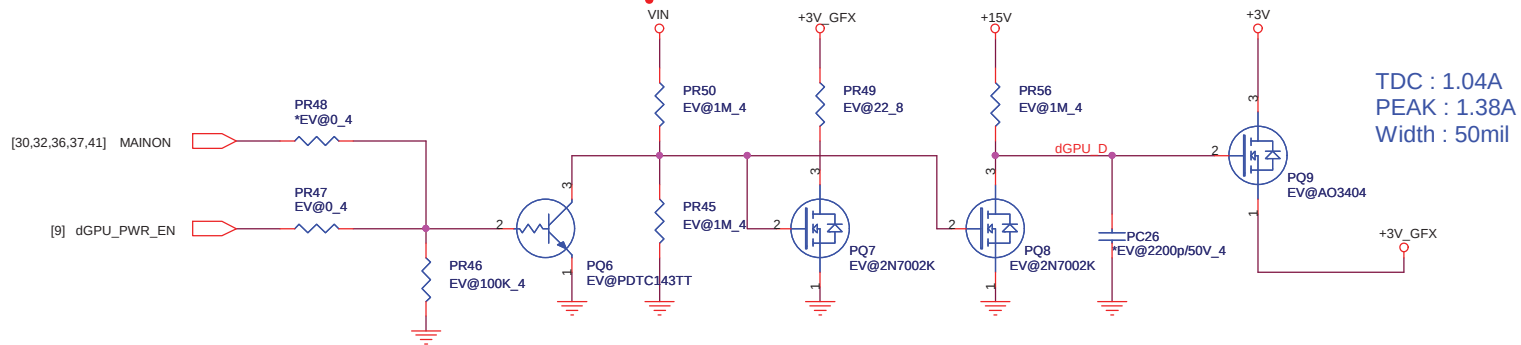
PROJECT : ZQTA/ZQSA

| Size  | Document Number           | Rev            |
|-------|---------------------------|----------------|
|       | VCCSA(RT8241DZ)           | 1A             |
| Date: | Friday, November 11, 2011 | Sheet 38 of 44 |

1013

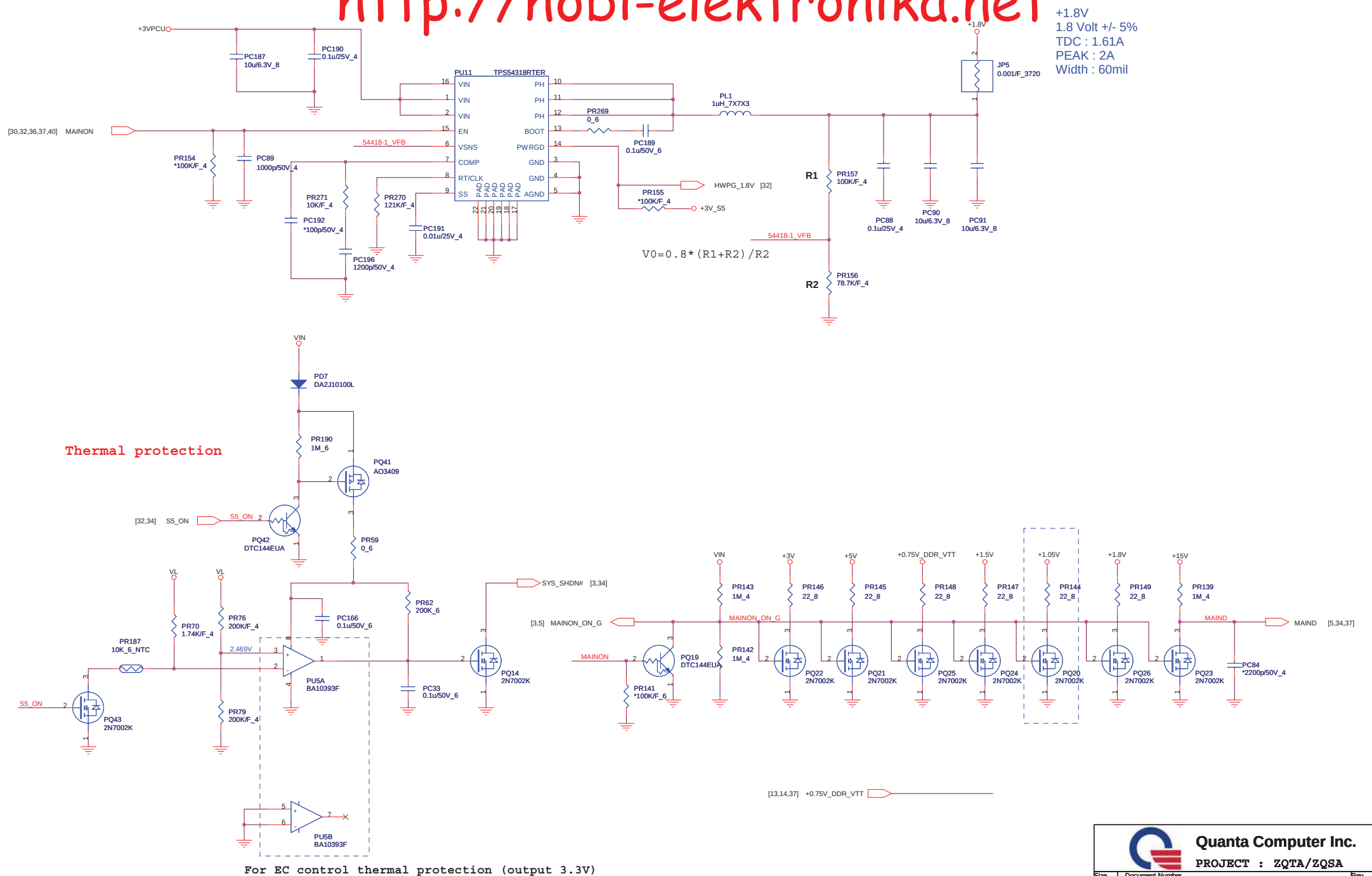
```
+VGPU_CORE (N13P-GS)
Continue current:50A
Peak current:55A
OCP minimum 60A
Loadline=0mV/A
```





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PROJECT : ZQTA/ZQSA

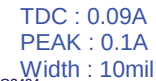
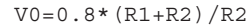
|       |                           |                |
|-------|---------------------------|----------------|
| Size  | Document Number           | Rev            |
|       | GPU_PWR                   | 1A             |
| Date: | Friday, November 11, 2011 | Sheet 40 of 44 |

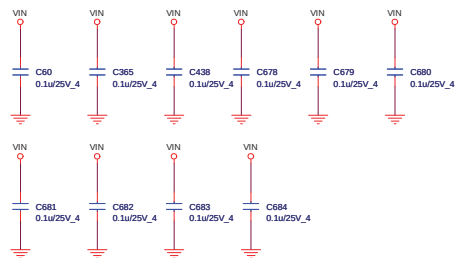


+1.8V  
1.8 Volt +/- 5%  
TDC : 1.61A  
PEAK : 2A  
Width : 60mil

$$V0 = 0.8 * (R1 + R2) / R2$$

For EC control thermal protection (output 3.3V)





| Model      | date  |                                                                                                                                                                                                                                                                                                                                          |
|------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ZASA/ZSQTA | 9/26  | page3 : add R511,R525,R527,R528,R529 for Discrete Only &PCH_JTAG_TDO net change pull-up from +3V_S5 to +1.05 rail                                                                                                                                                                                                                        |
|            | 9/27  | Update power circuit<br>Page19 : add C3777,C3778                                                                                                                                                                                                                                                                                         |
|            | 9/30  | Page18 : add Q3508 for U7 GPU_THERMAL_ALERT net<br>Page31 : Del CN1                                                                                                                                                                                                                                                                      |
|            | 10/3  | Page18 : add dGPU_ACDC# net to U7 GPIO04 & add R347<br>Page22 : add R557,R554 to pull-down & R548,R547 stuff for Discrete only<br>Page25 : add R3693,C116 for ODD zero power circuit                                                                                                                                                     |
|            | 10/4  | Page31 : CN8 add board id3 & board id4 net for touch pad ID control                                                                                                                                                                                                                                                                      |
|            | 10/5  | Page31 : CN8.2,CN8.3 add CLK_SDATA & CLK_SCLK net for touch pad & add R278,R279<br>Page15 : U41 Power rail change to +3V_GFX<br>Page24 : Del Q16 no't support wake up function<br>Page18 : add Q3509 for dGPU_ACDC# net<br>Page31 : add L35,R3694,R3695 for touch pad 5V & 3V option & add R297,R295 Fan PWR option                      |
|            | 10/6  | Page17 : IFPAB_PLLVDD rail change from +1.8V_GFX to +3V_GFX<br>Page27 : U6 change footprint<br>Page39 : PWR engineer add PQ3006,PQ3005<br>Page40 : PWR engineer Del PR193,PQ51,PQ54                                                                                                                                                      |
|            | 10/7  | Page16 :add C3779,C3780<br>Page29 :add C542,C530 for EMI solution & C544 change to 4.7u 0603 type<br>Page35 :PWR engineer add PC3037,PC3038,PC3039<br>Page35 :PWR engineer add PC3035,PC3036                                                                                                                                             |
|            | 10/11 | Page8 :add R376,R381,R393,R407,R421,R434 for Dual SPI ROM<br>Page9 :U13 power rail change to +3V<br>Page10 :SV_DET_NC net add R250 to pull-down<br>Page27 :add R133,R235<br>Page30 :C443 change to 3528 type & add C366,R340<br>Page31 :CN2.27 pin change to +VGACORE<br>Page32 :add R330,R328 pull-up +3VPCU for GPUT_CLK,GPUT_DATA net |
|            | 10/14 | Page20 :add C3781,C3782,R3569,R3570,R3571,R3576<br>Page21 :add C3783,C3784,R3577,R3578,R3579,R3581                                                                                                                                                                                                                                       |
|            |       |                                                                                                                                                                                                                                                                                                                                          |



**Quanta Computer Inc.**  
**PROJECT : ZQTA/ZQSA**

**DOC NO.**

**PROJECT MODEL :**

ZQTA/ZQSA

**APPROVED BY:**

**DATE:**

**PART NUMBER:**

**DRAWING BY:**

**REVISION:**

**Change list**

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