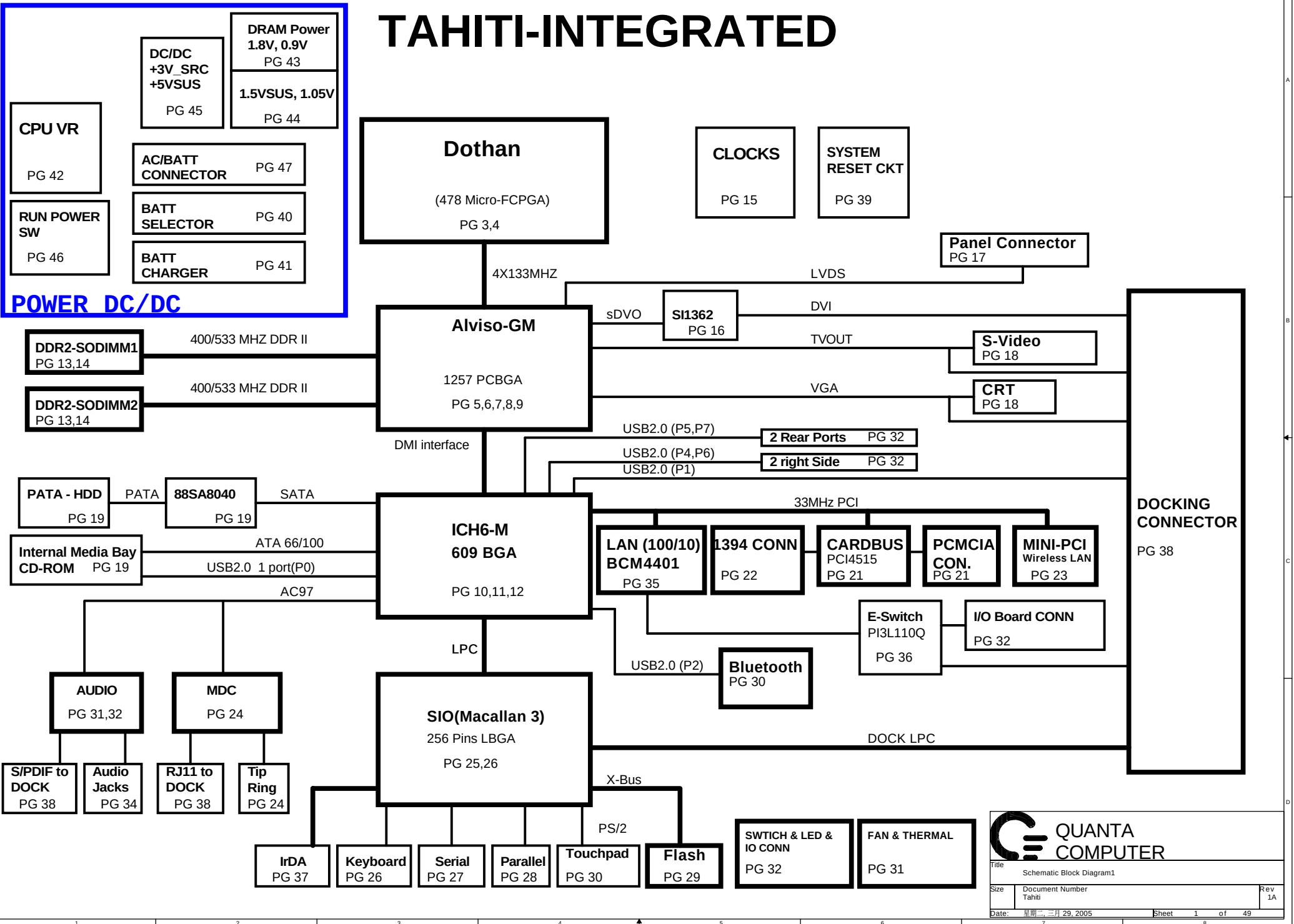
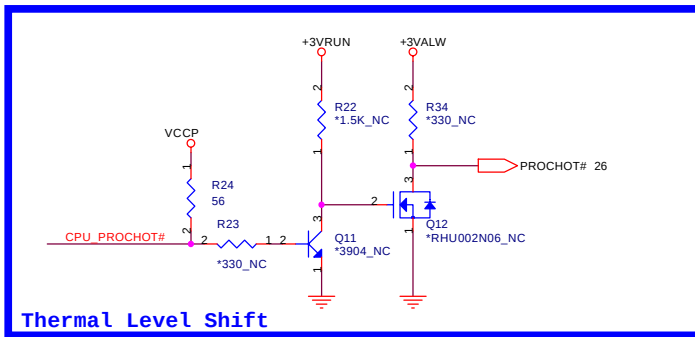
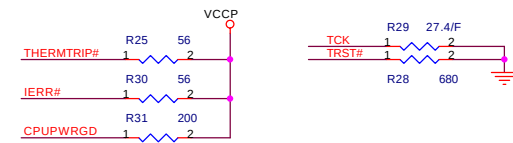
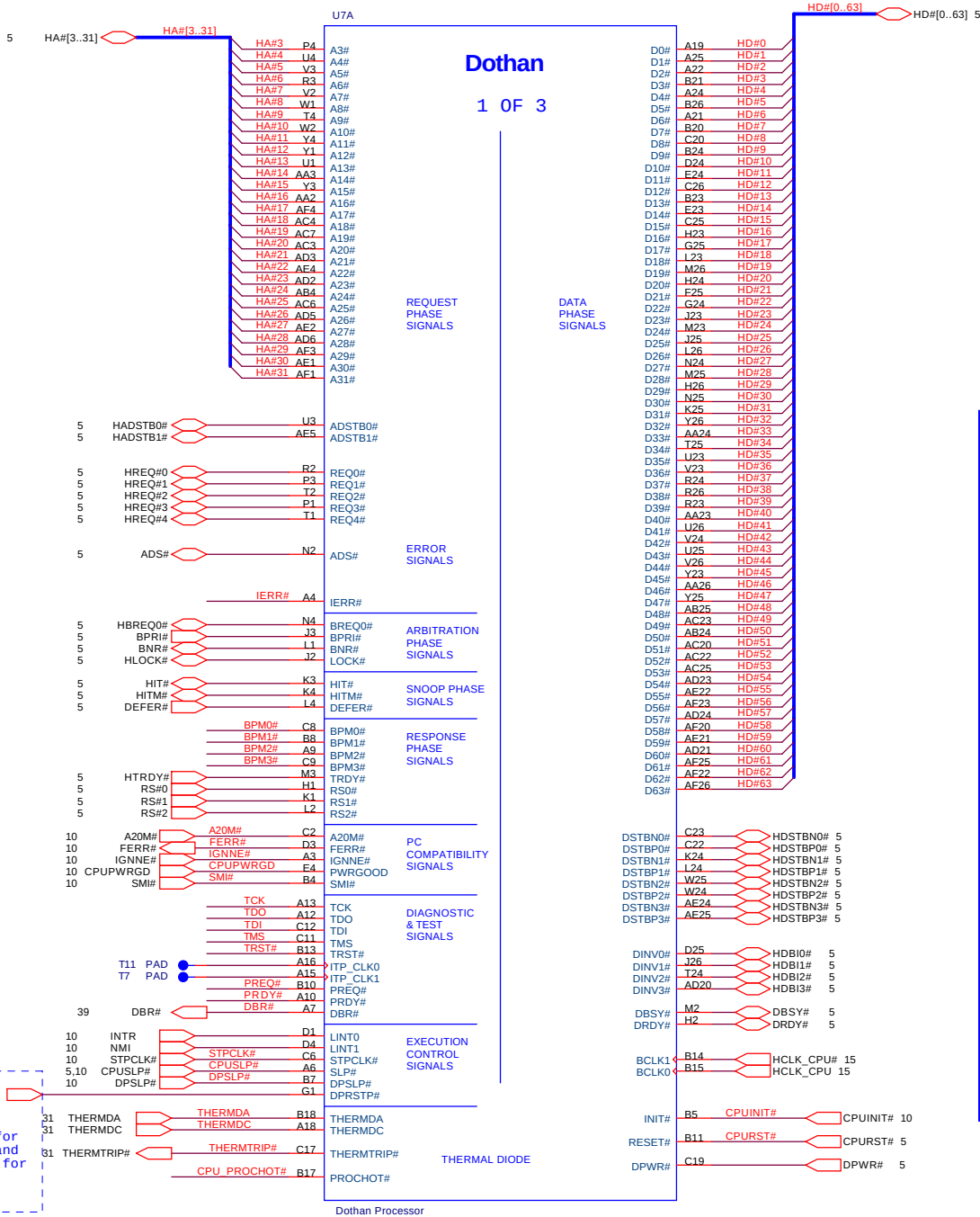


TAHITI-INTEGRATED



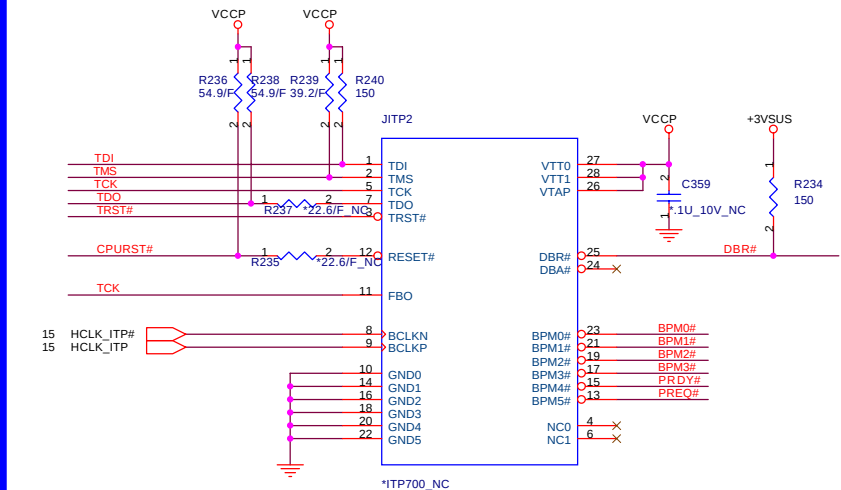
INDEX		
Pg#	Description	DNI LIST
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2	Front Page	
3-4	Dothan	
5-9	Alviso	
10-12	ICH6	
13-14	DDRII SO-DIMM(200P)	
15	Clock Generator	
16	SI1362	
17	LCD Conn. & SSP	
18	CRT & TV Conn.	
19	SATA & IDE Conn.	
20	PAD & Screw Hole	
21	TI PIC4510	
22	CB/1394 CONN	
23	Mini PCI Conn.	
24	MDC Conn.	
25-26	SIO (LPC47N354)	
27	Parallel Port	
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29	Flash ROM	
30	Touch Pad CONN.& Bluetooth CONN	
31	Switch Board Conn. & LED & IO Board	
32	FAN & Thermal	
33-34	Audio CODEC (STAC9751) & Phone Jack	
35-36	LAN Interface	
37	FIR	
38	MISCELLANEA	
39	Docking Conn.	
40	SYSTEM RESET/POWER GOOD	
41-42	Battery Selector & Charger	
43	CPU Power	
44	1.8VSUS/0.9V	
45	1.5V/1.05V	
46	D/D Power	
47	RUN Power Switch	
48	RUN POWER SW	

Power & Ground			
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
VHORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
1.05V		AGTL+ POWER (1.05V) I/O	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#/5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VRUN		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		ALVISO POWER Non-CPU I/O	
 GND	ALL PAGES	DIGITAL GROUND	
		COMBO CONN GND	

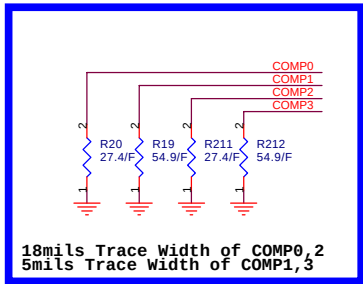


ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	VTT	Within 2.0" of the CPU

Note: Populate All NC component when ITP connector is populated.



Title Dothan Processor (HOST)			
Size	Document Number Tahiti(DM3L)	Rev 1A	
Date	星期二, 三月 29, 2005	Sheet	3 of 49



VCCP

R16 1K/F

R15 2K/F

Z0 = 55 ohm, 25 mils
spacing for switching
signals

COMP0 P25
COMP1 P26
COMP2 AB2
COMP3 AB1

GTLREF0 AD26

TEST1 C5
TEST2 F23

NC1 B2

RSVD2 C3
RSVD3 AF7
RSVD4 AC1
RSVD5 E26

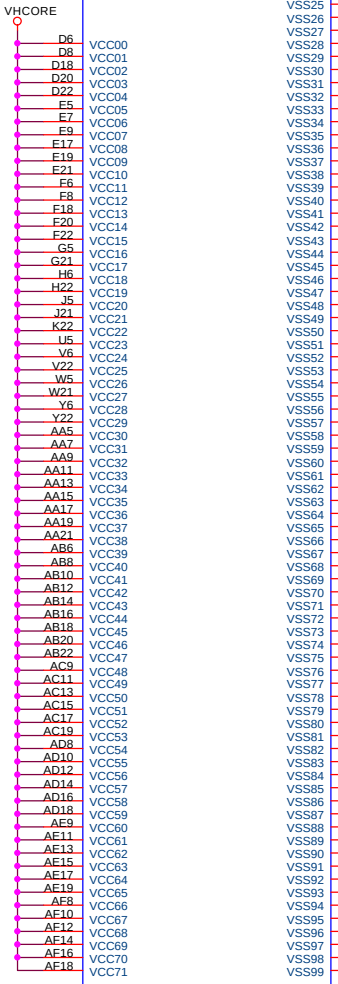
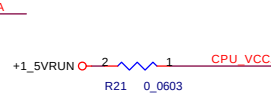
VCCA3 AC26
VCCA2 N1
VCCA0 B1 E26

VHCCORE

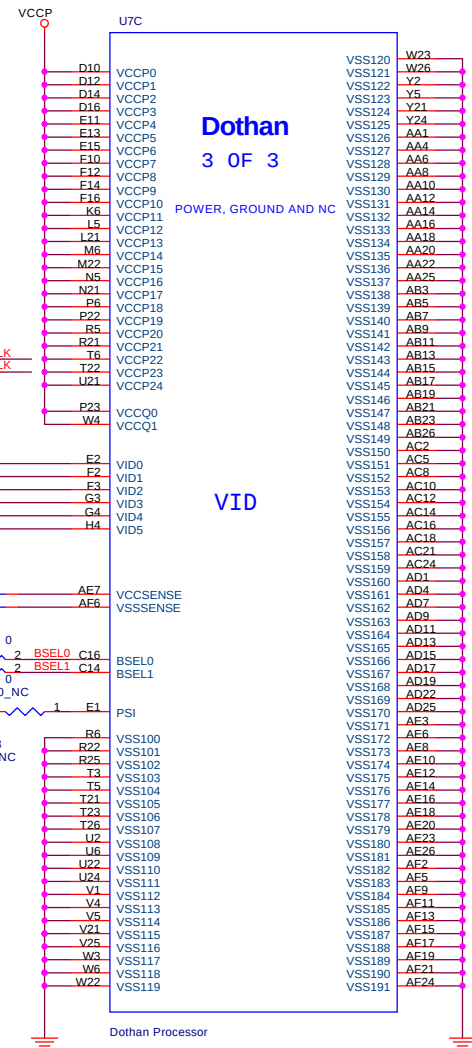
D6 VCC00
D8 VCC01
D18 VCC02
D20 VCC03
D22 VCC04
E5 VCC05
E7 VCC06
E9 VCC07
E17 VCC08
E19 VCC09
E21 VCC10
E6 VCC11
F8 VCC12
F18 VCC13
F20 VCC14
F22 VCC15
G5 VCC16
G21 VCC17
H6 VCC18
H22 VCC19
J5 VCC20
K22 VCC21
J5 VCC22
J6 VCC23
V6 VCC24
V22 VCC25
W5 VCC26
W21 VCC27
Y6 VCC28
Y22 VCC29
AA5 VCC30
AA7 VCC31
AA9 VCC32
AA11 VCC33
AA13 VCC34
AA15 VCC35
AA17 VCC36
AA19 VCC37
AA21 VCC38
AB6 VCC39
AB8 VCC40
AB10 VCC41
AB12 VCC42
AB14 VCC43
AB16 VCC44
AB18 VCC45
AB20 VCC46
AB22 VCC47
AC9 VCC48
AC11 VCC49
AC13 VCC50
AC15 VCC51
AC17 VCC52
AC19 VCC53
AD8 VCC54
AD10 VCC55
AD12 VCC56
AD14 VCC57
AD16 VCC58
AD18 VCC59
AE9 VCC60
AE11 VCC61
AE13 VCC62
AE15 VCC63
AE17 VCC64
AE19 VCC65
AE8 VCC66
AE10 VCC67
AE12 VCC68
AE14 VCC69
AE16 VCC70
AE18 VCC71

Dothan
2 OF 3

POWER, GROUND, RESERVED
SIGNALS



Dothan Processor

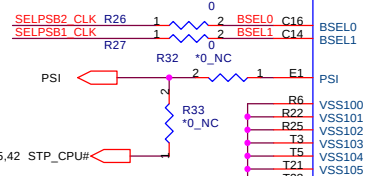


Dothan
3 OF 3

POWER, GROUND AND NC

VID

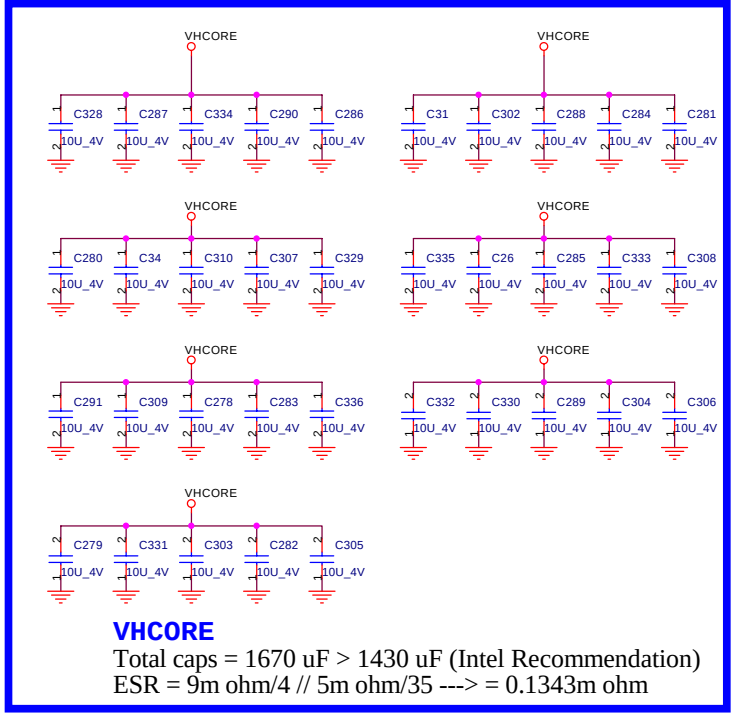
Differential Probe
Test Using



NO PSI (Power Saving
Indicator)

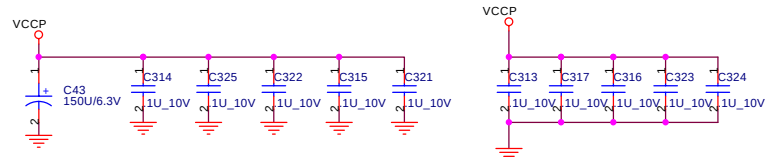
	DothanA	DothanB
R26	NC	Install

Dothan Processor

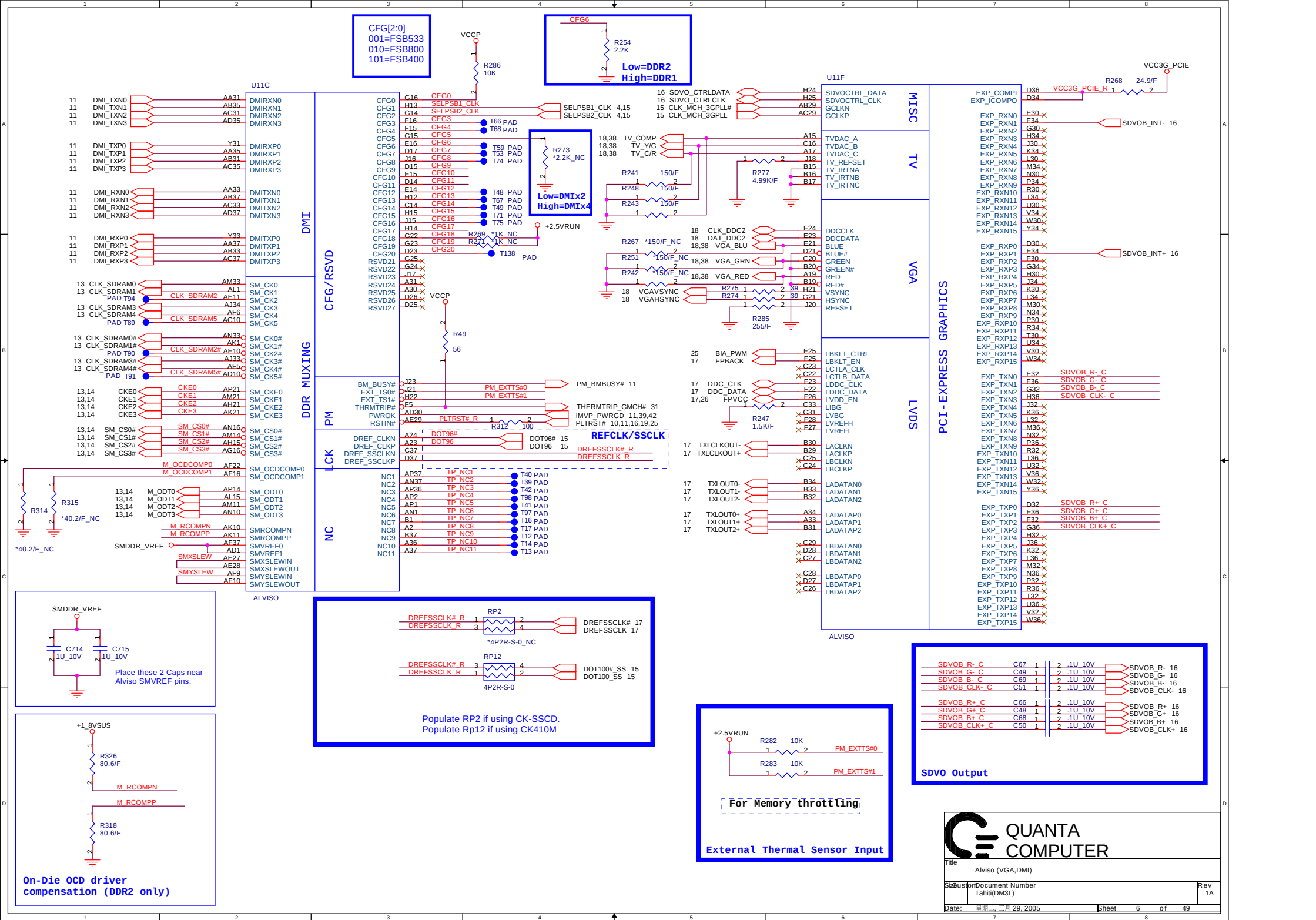


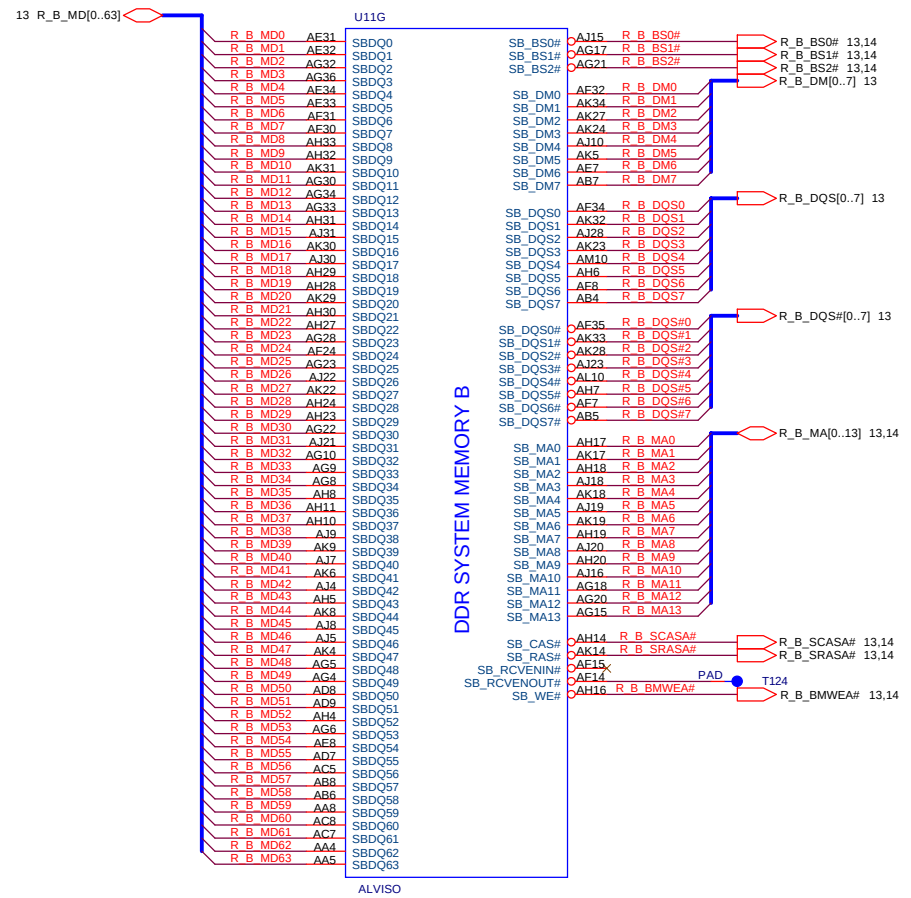
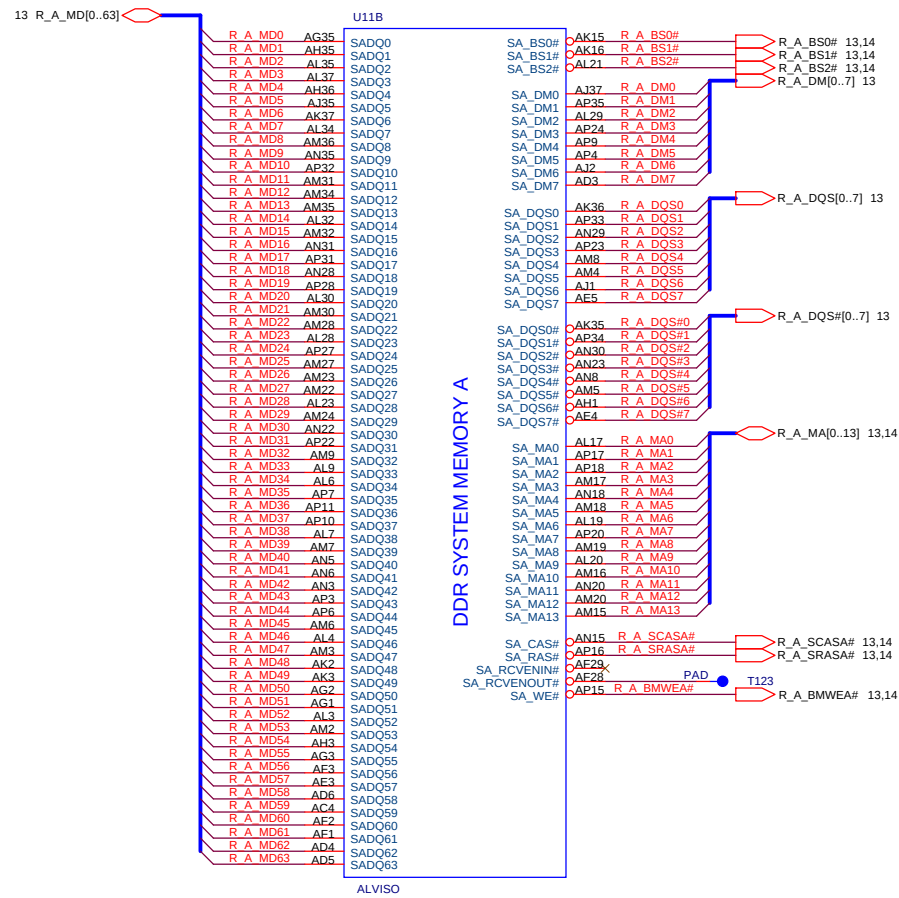
VHCORE

Total caps = 1670 uF > 1430 uF (Intel Recommendation)
ESR = 9m ohm/4 // 5m ohm/35 ----> = 0.1343m ohm

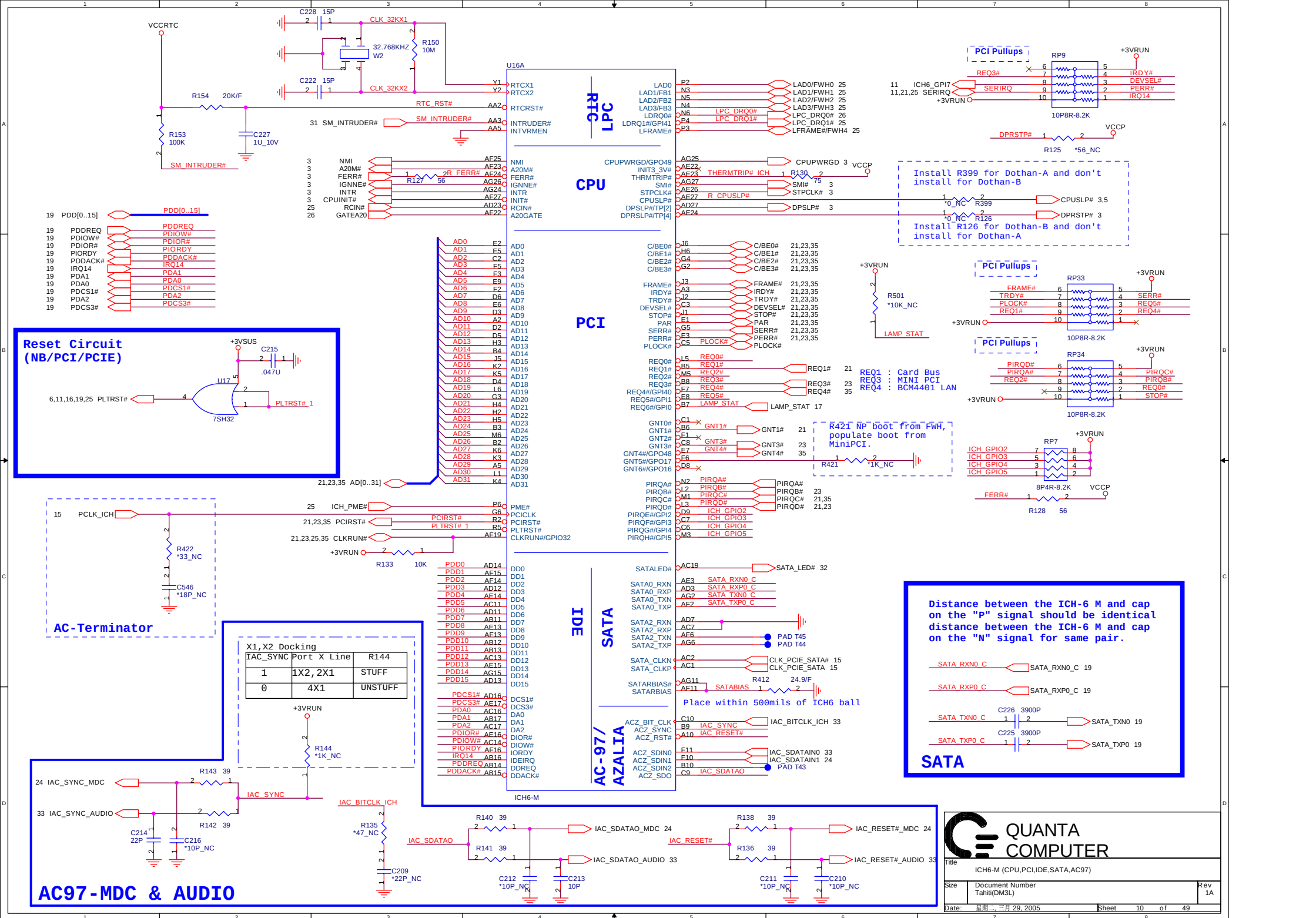


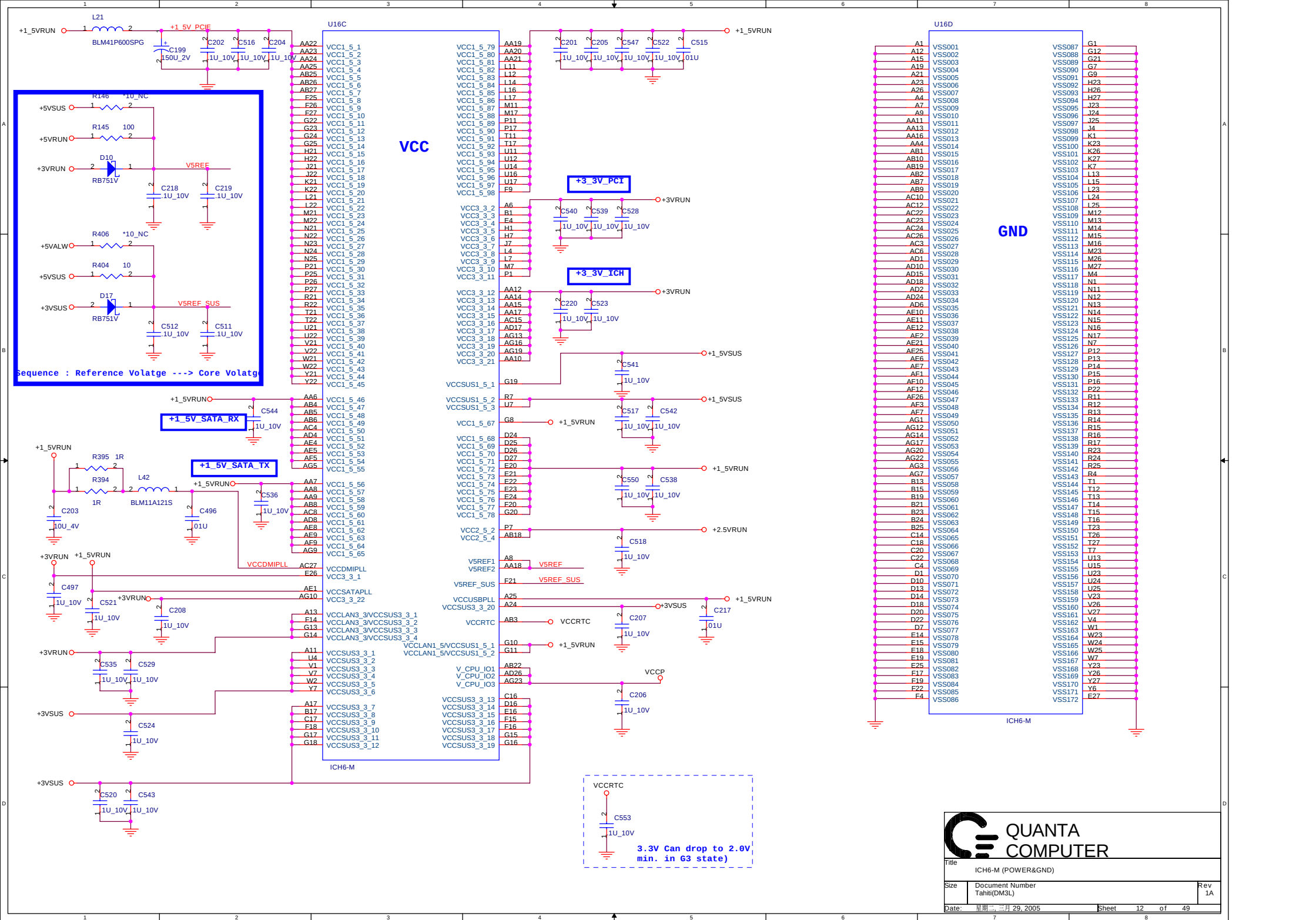
C, mF-----ESR, mW-----ESL, nH
1 x 150 mF-----42 mW (typ) / 2-----2.5 nH / 12
10 x 0.1 mF-----16 mW (typ) / 10-----0.6 nH / 10

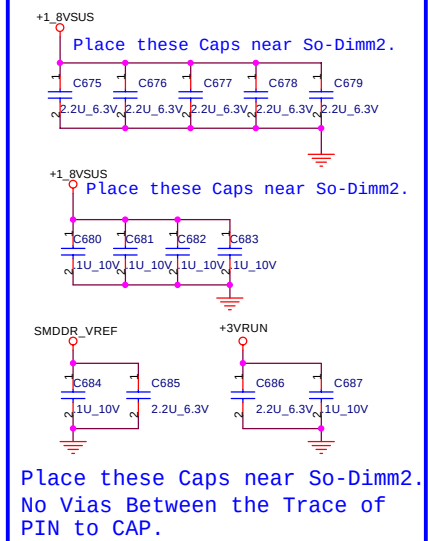
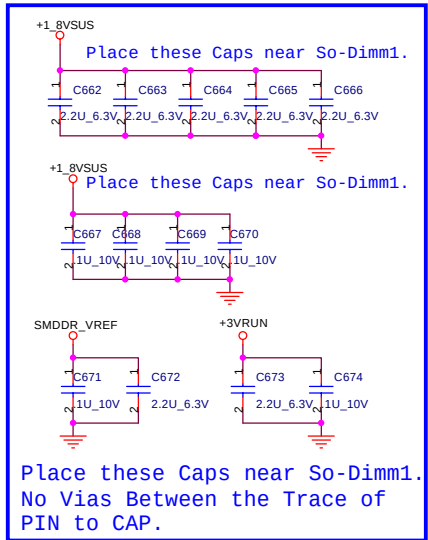
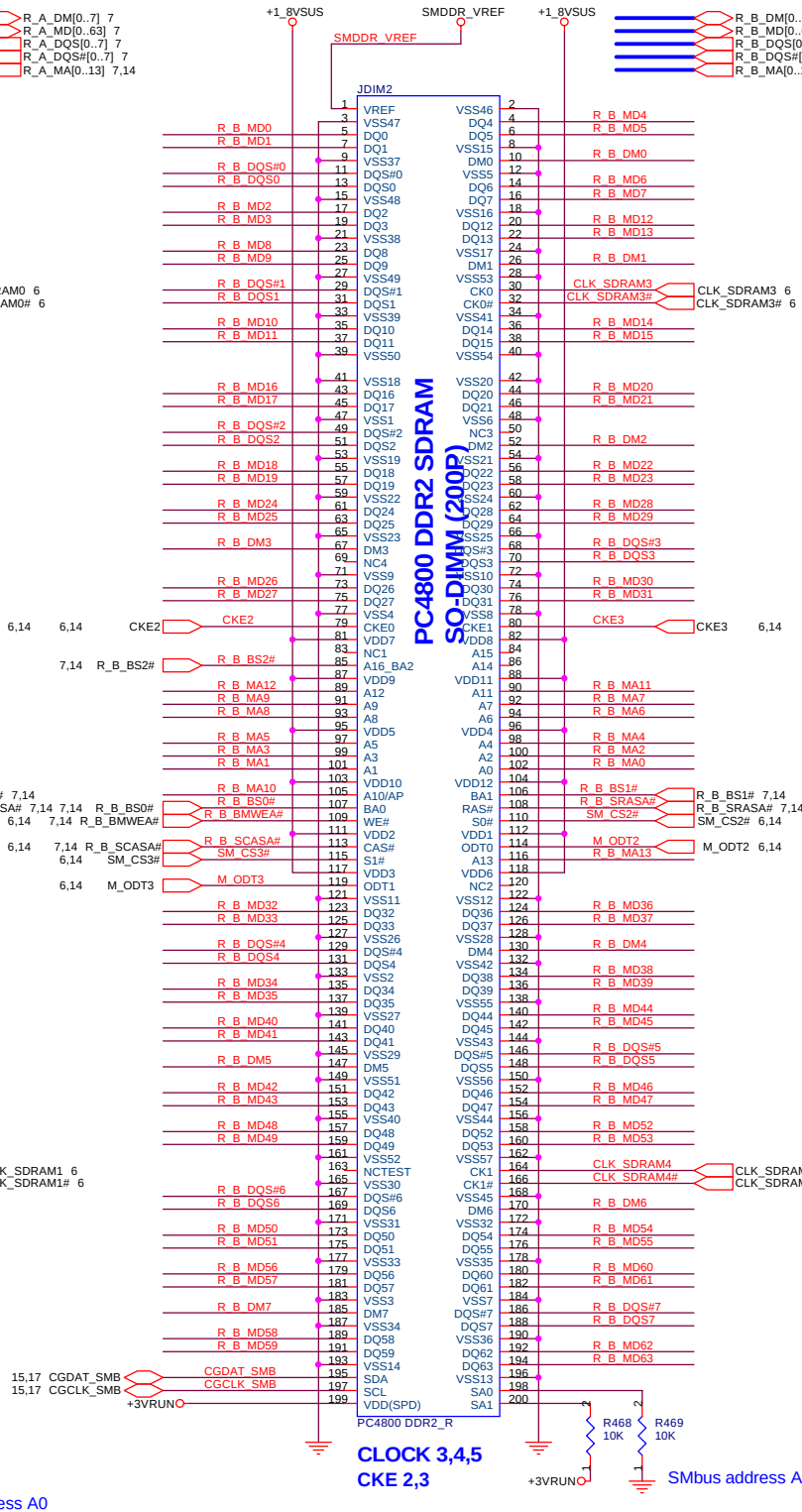
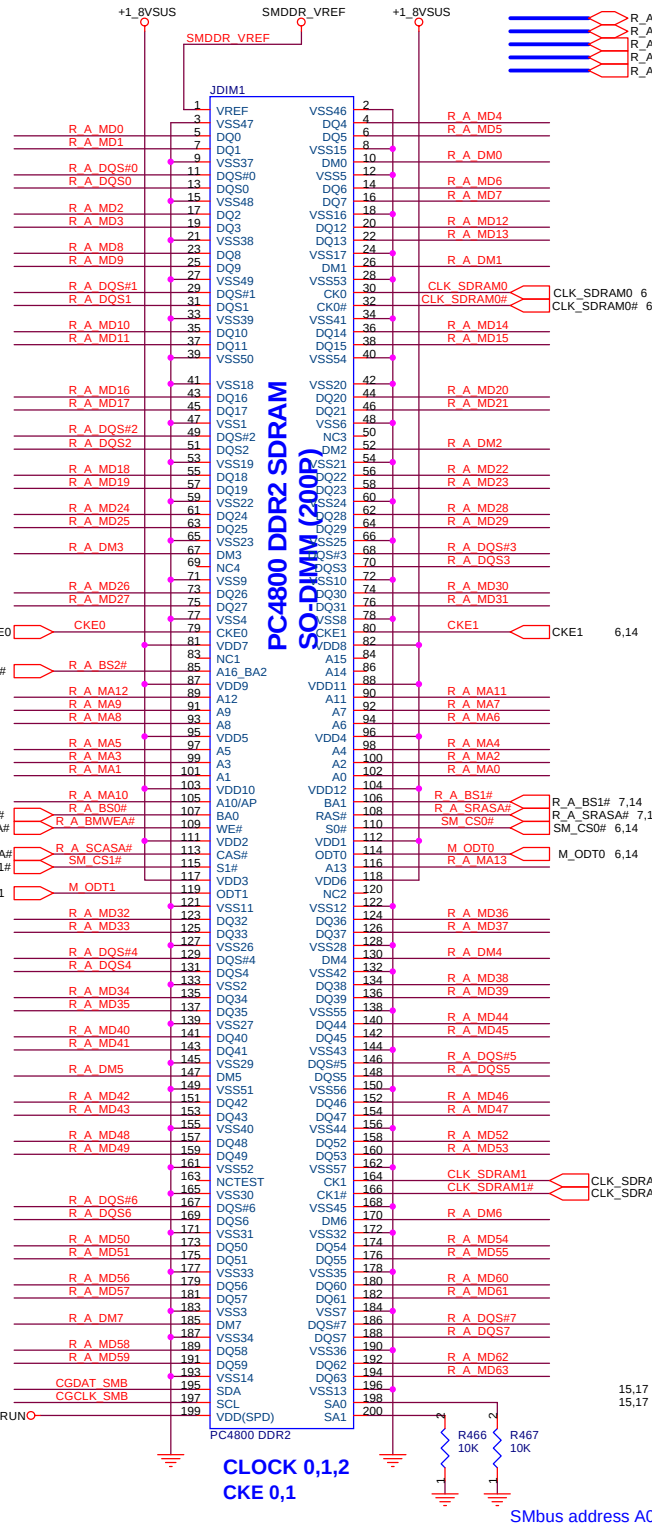




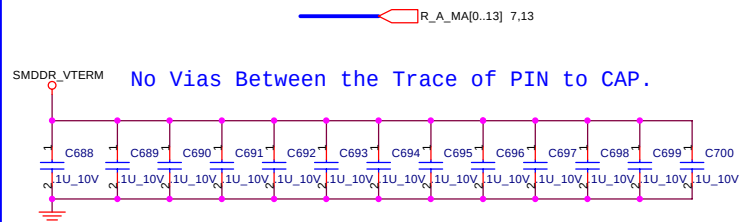




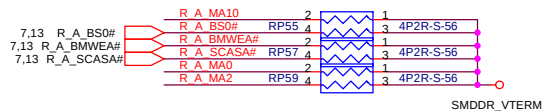
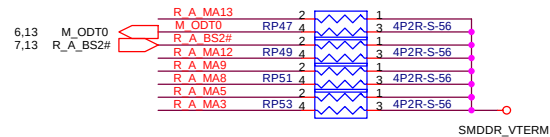
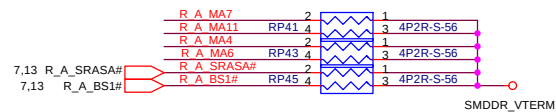




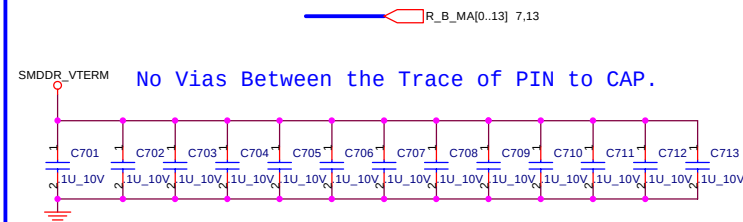
DDRII A CHANNEL



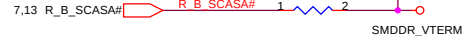
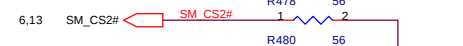
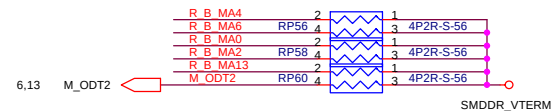
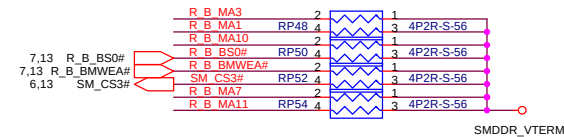
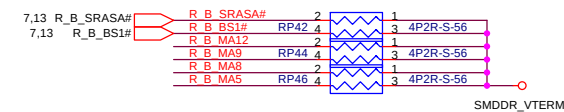
Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

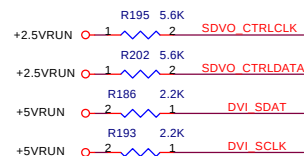


DDRII B CHANNEL

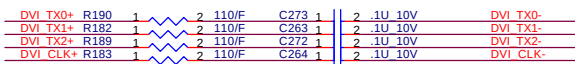
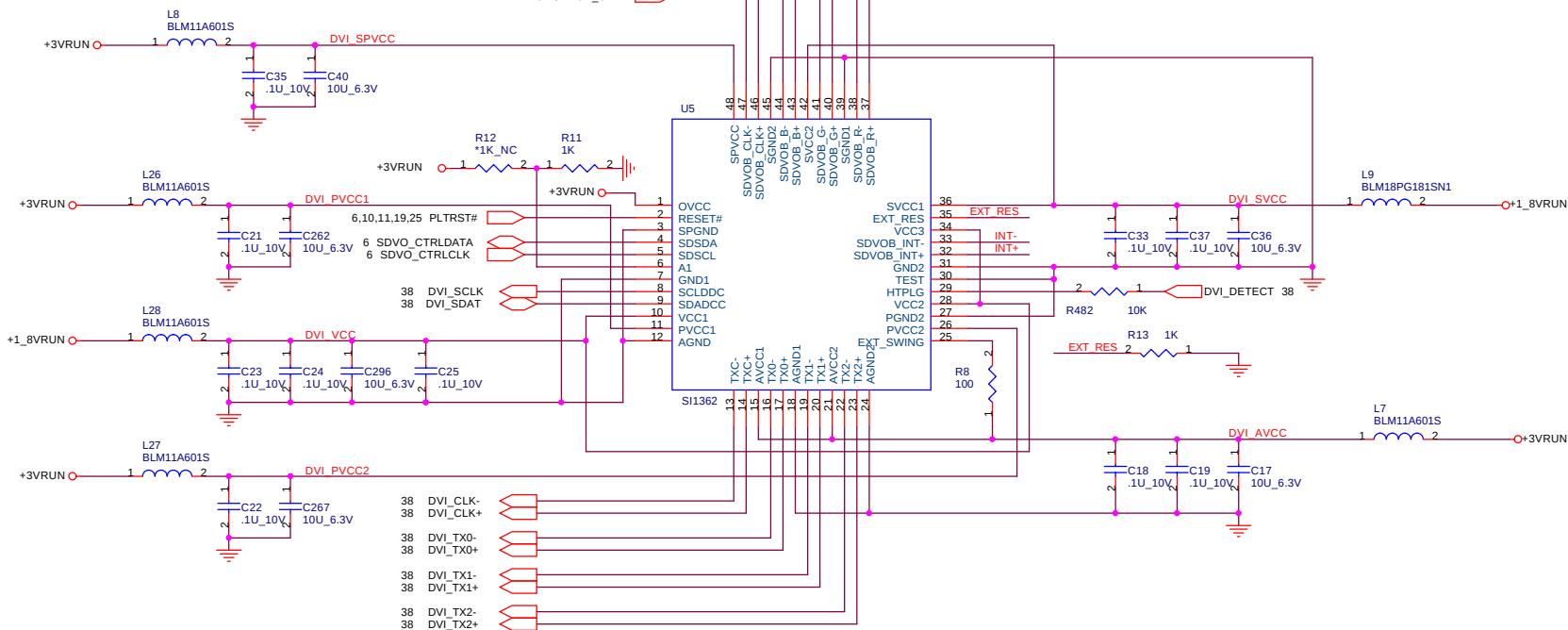
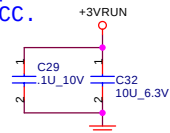


Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.



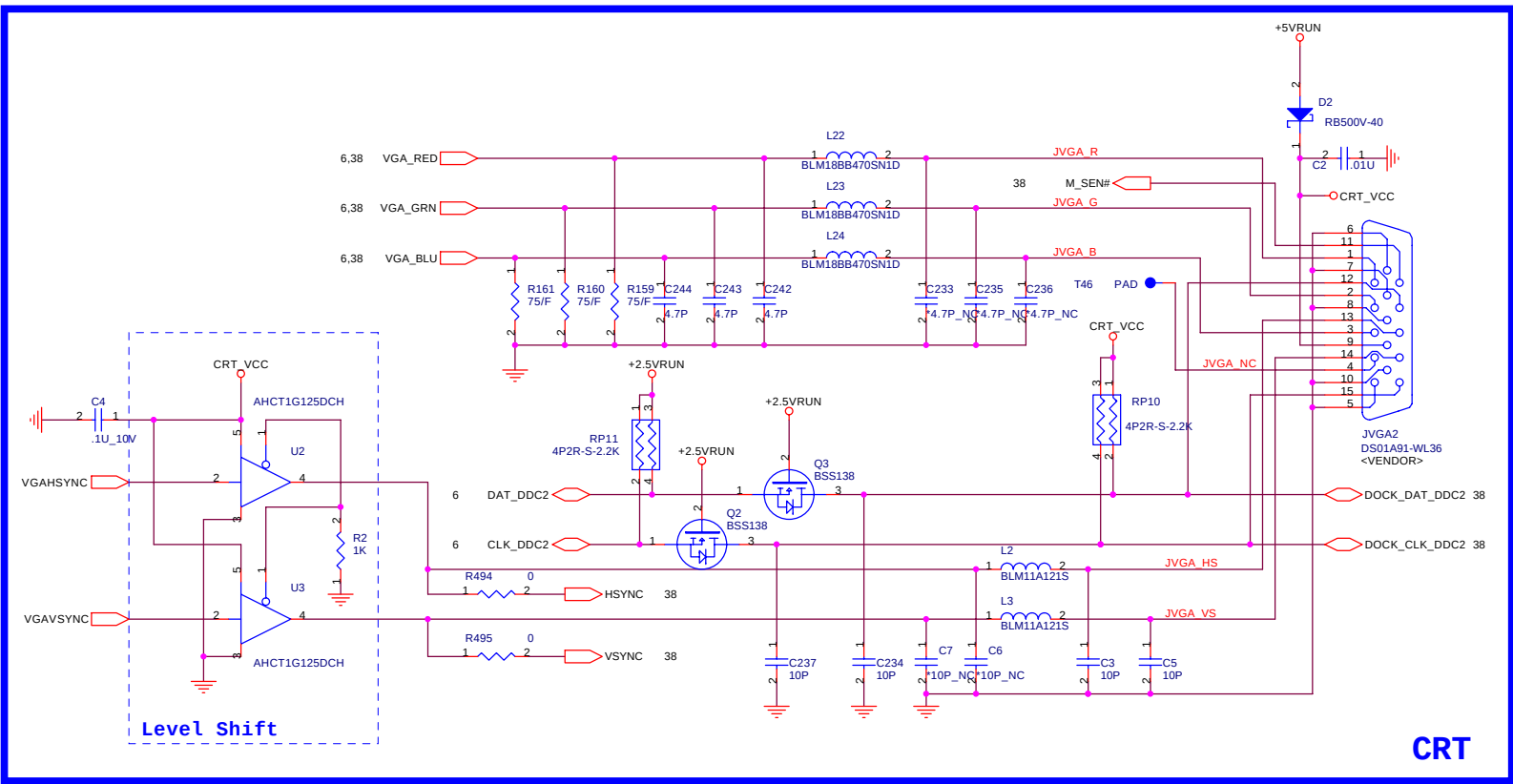


Placed this Bypass capacitor close to OVCC.

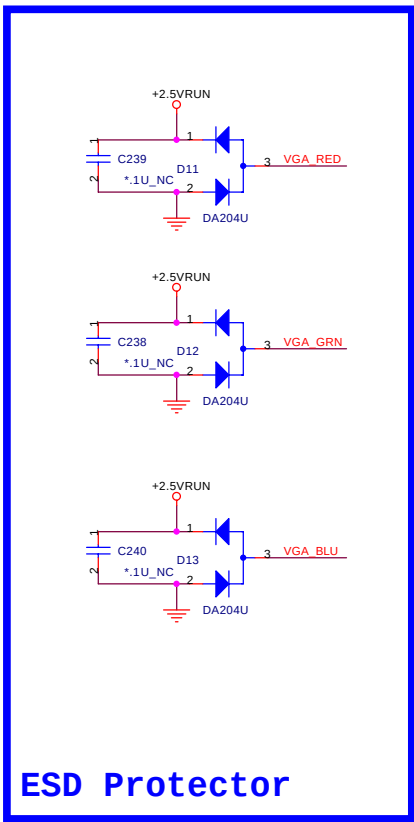


Put these 4 Resistors and 4 Capacitors close to the TX pin of SDVO device

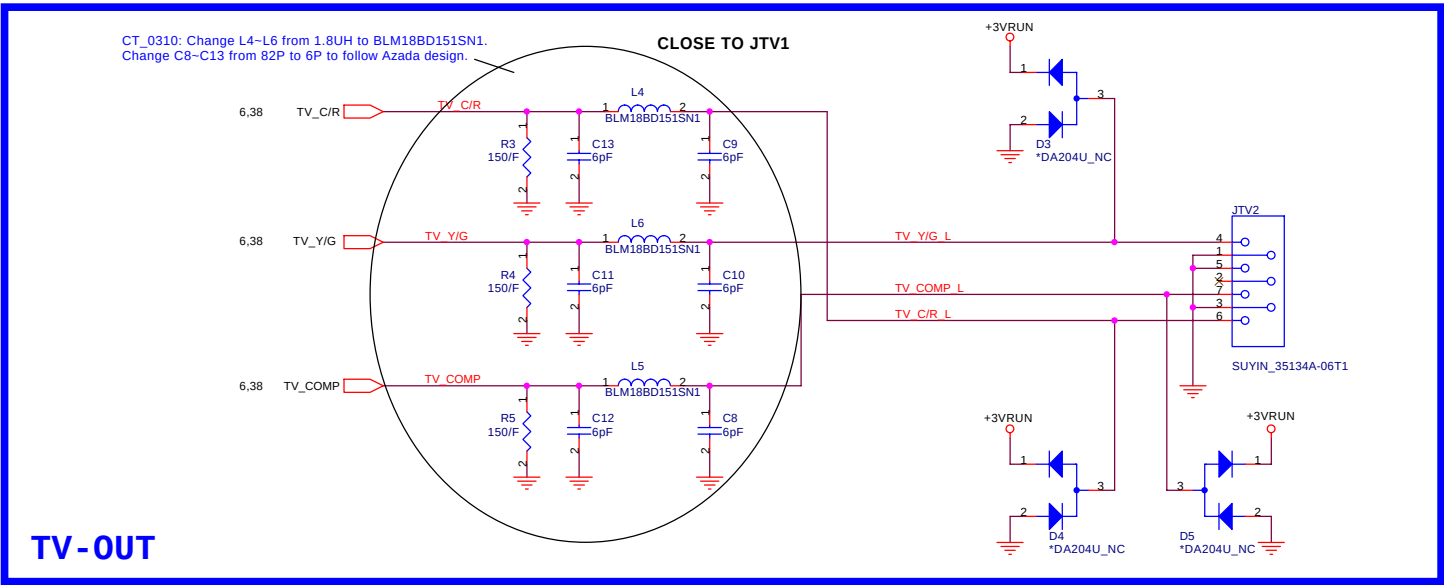




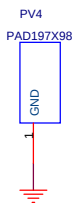
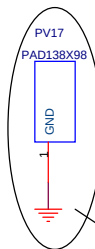
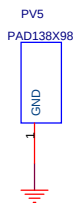
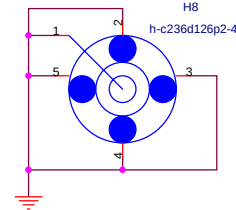
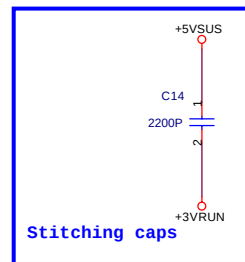
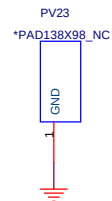
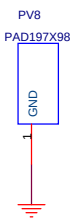
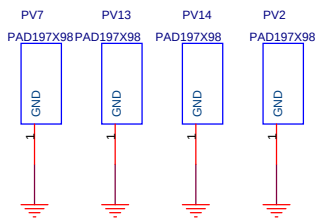
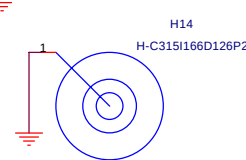
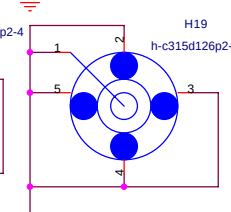
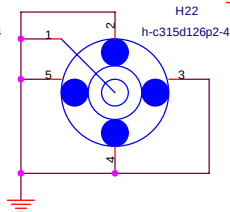
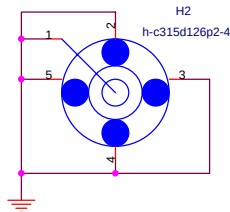
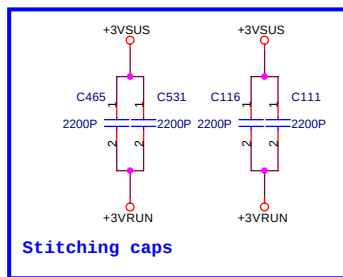
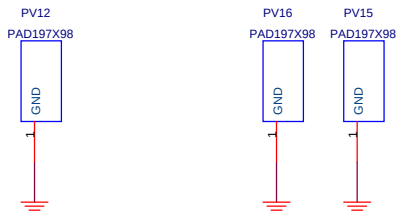
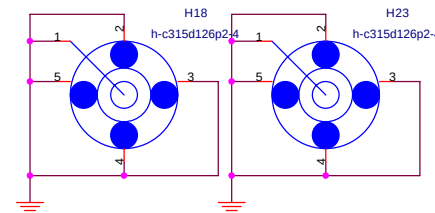
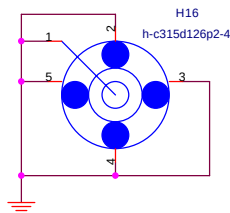
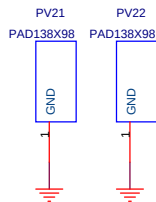
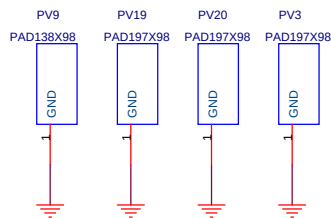
CRT



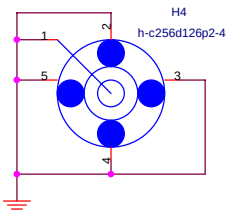
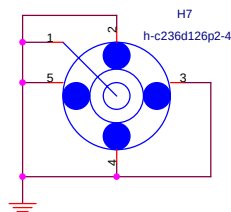
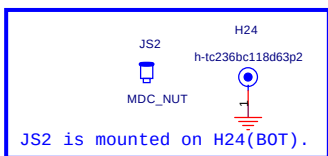
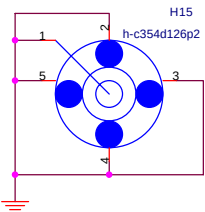
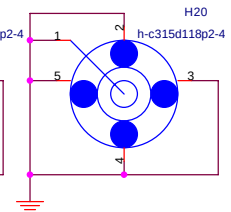
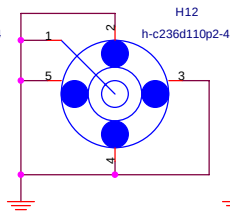
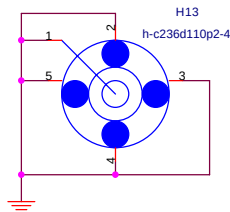
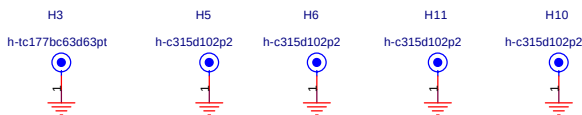
ESD Protector

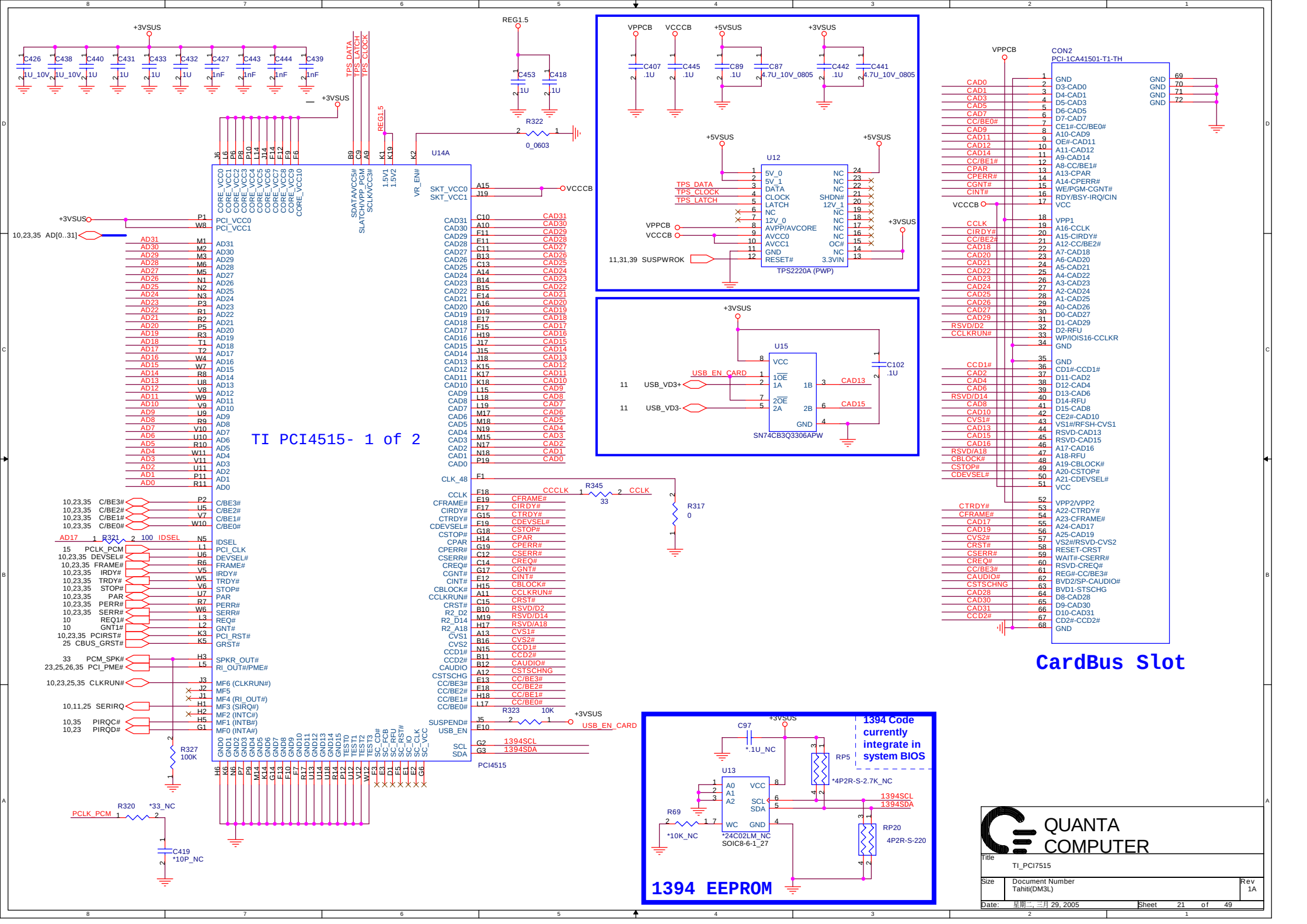


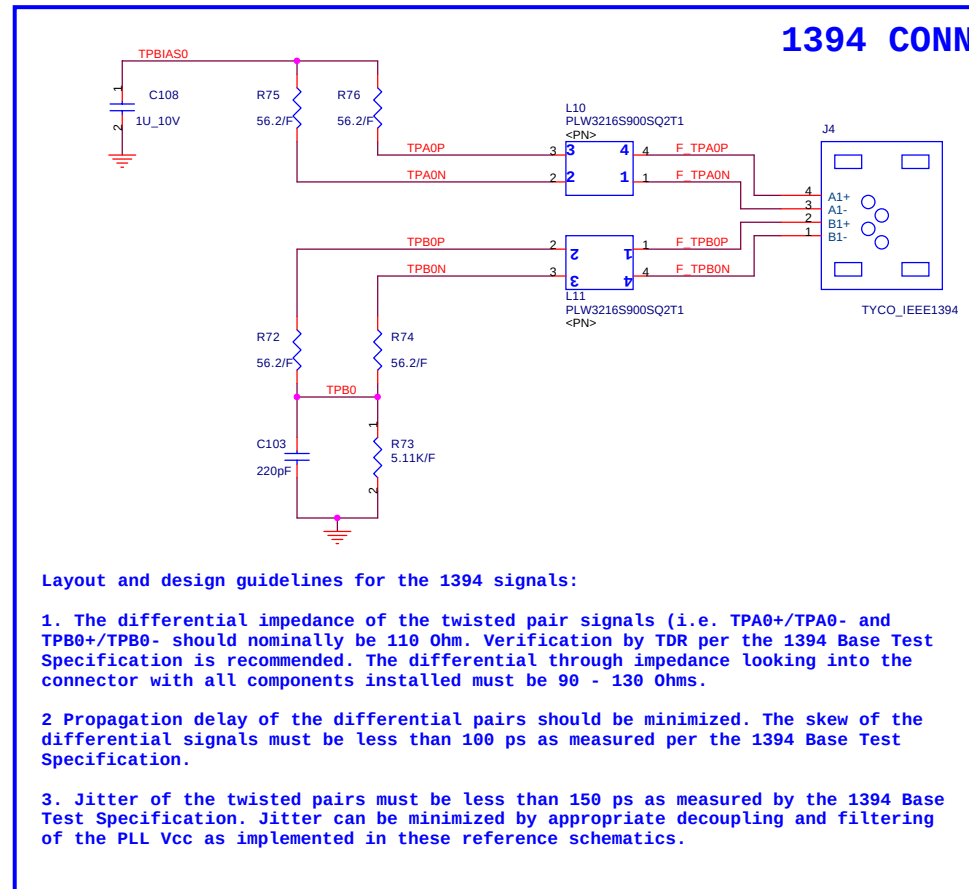
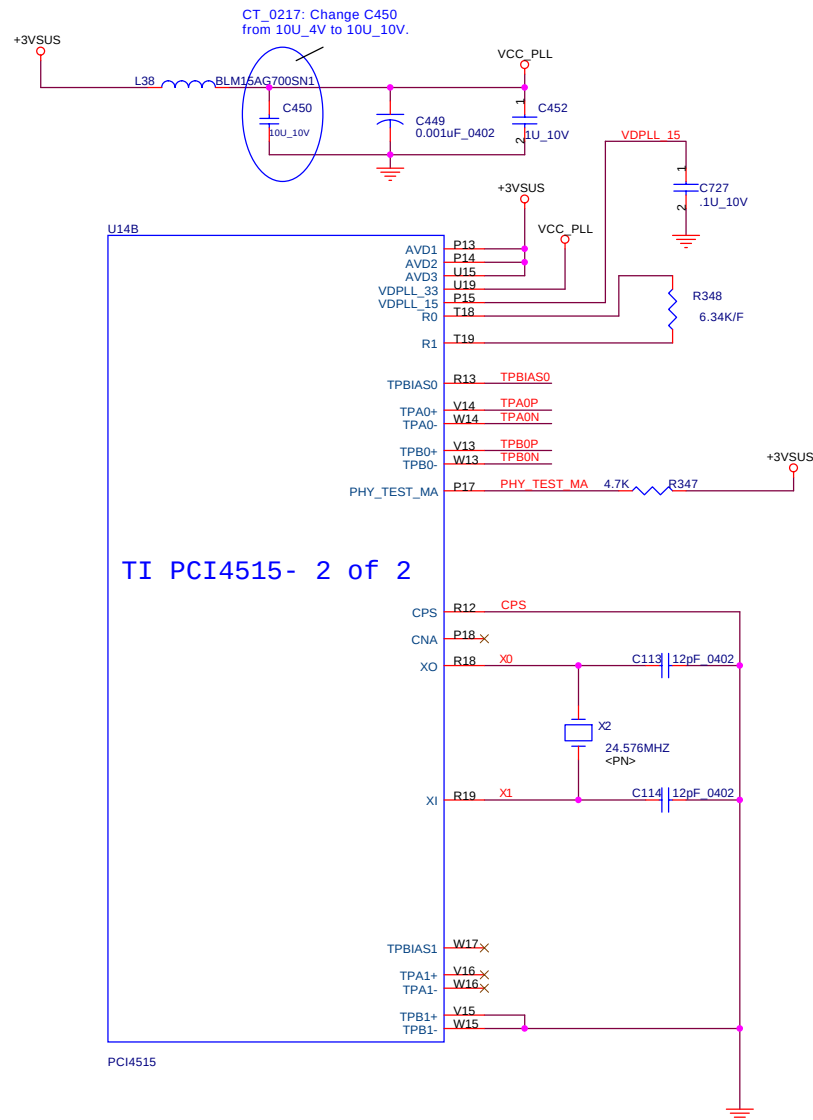
TV-OUT

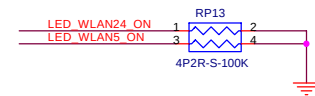
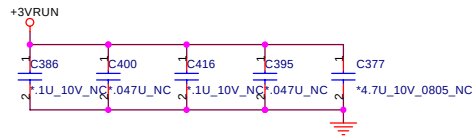
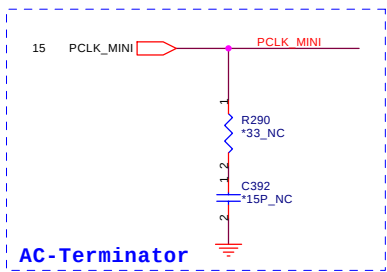


CT_0314:Change PV17 from PAD197x98 to PAD138x98 small size.

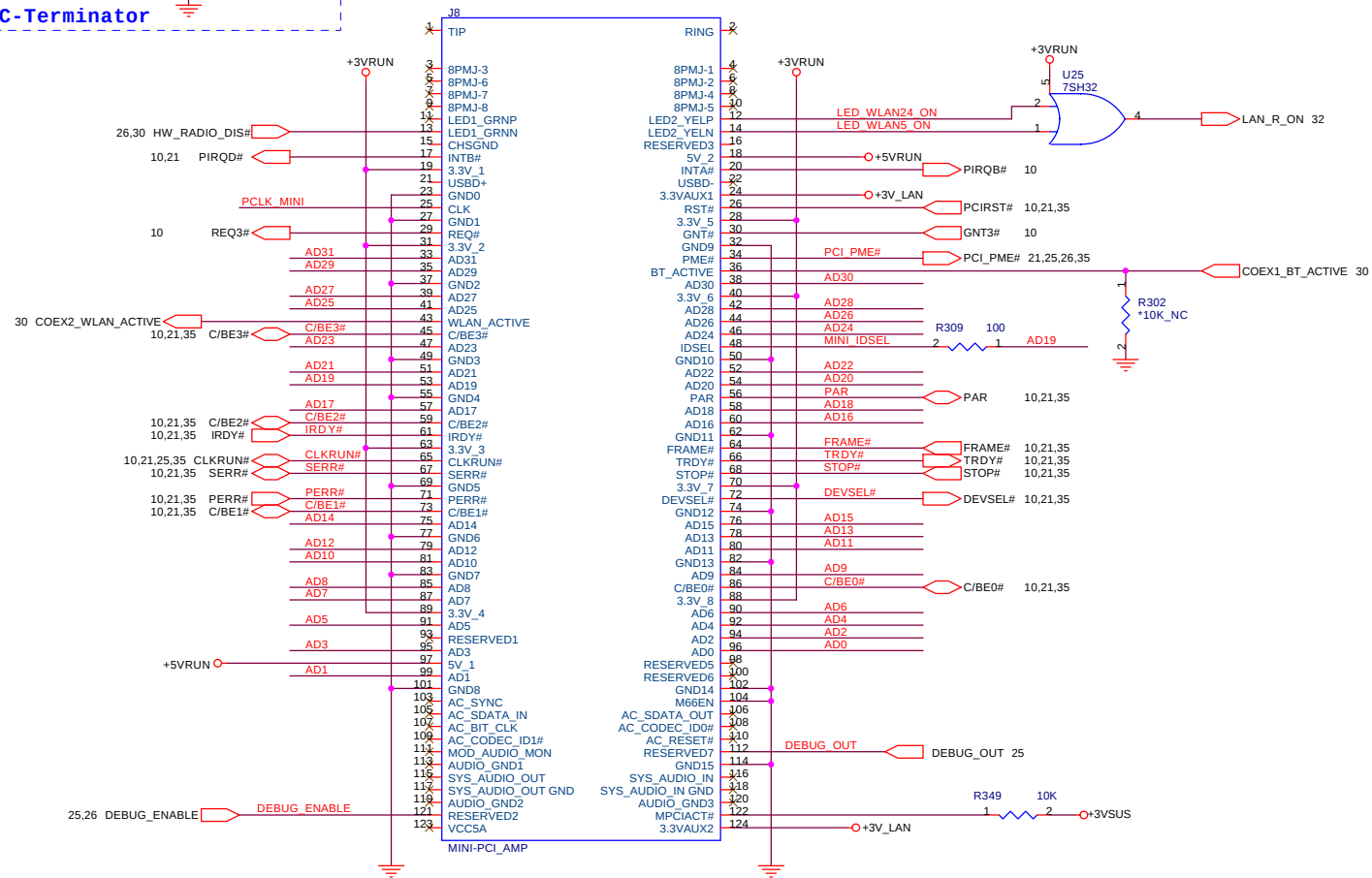


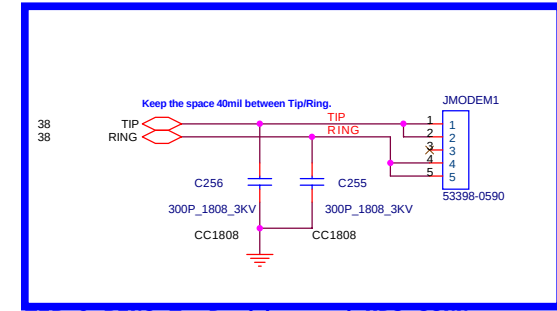
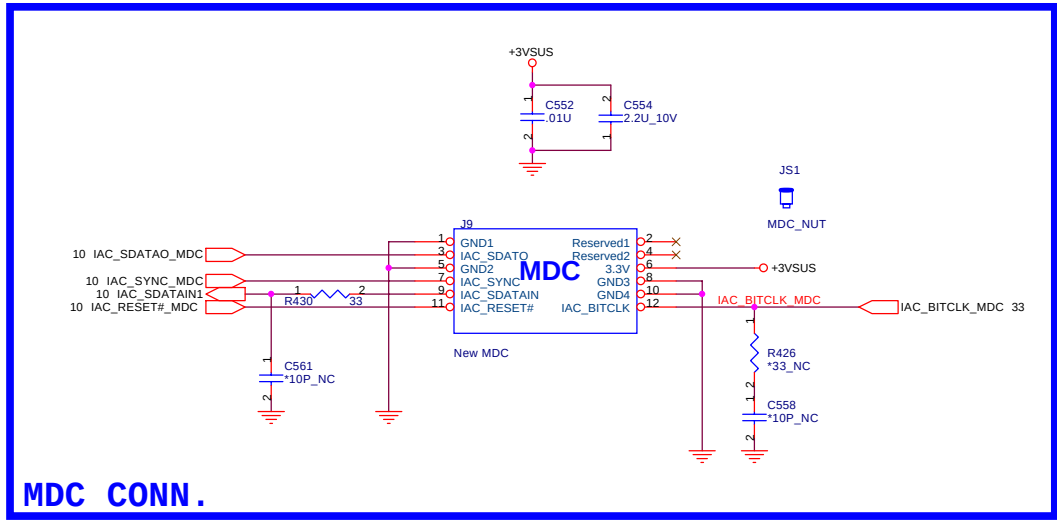


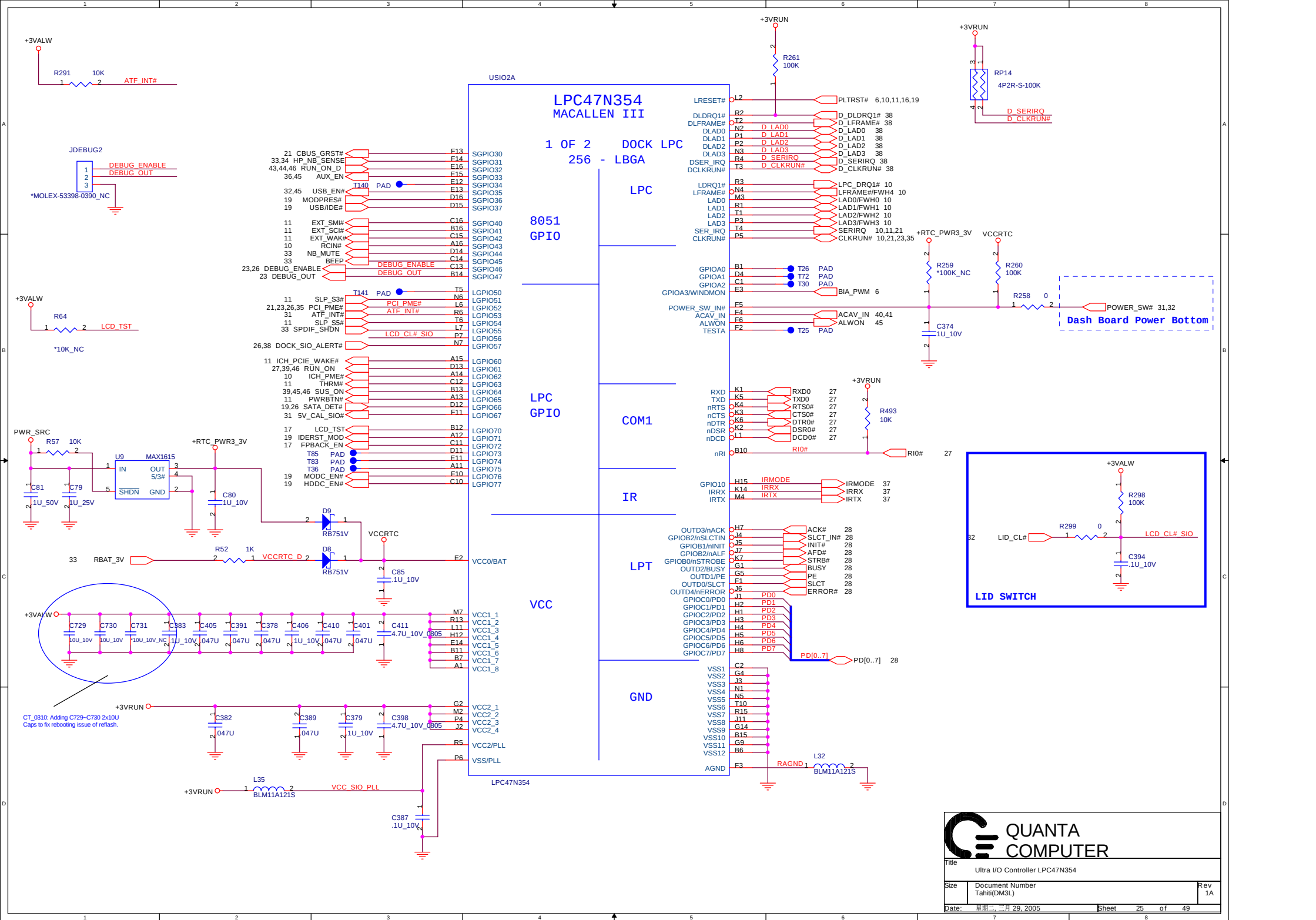


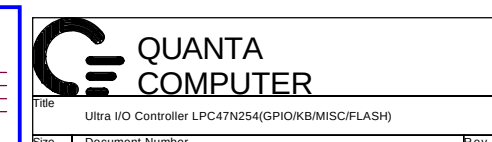
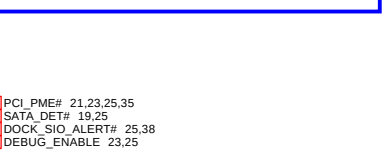
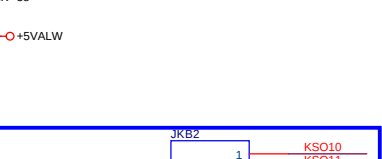
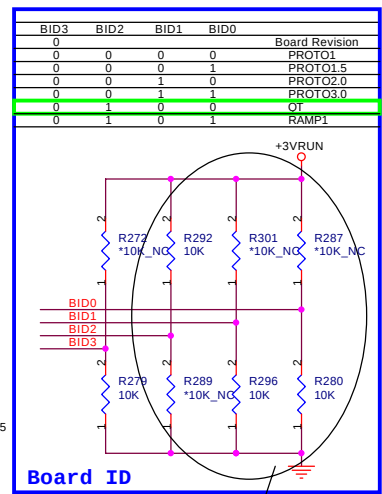
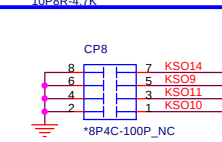
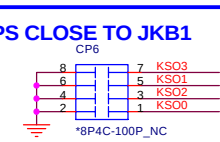
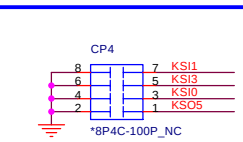
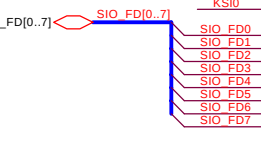
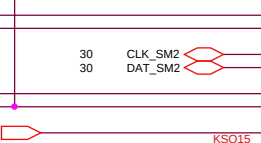
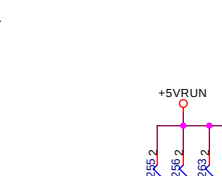
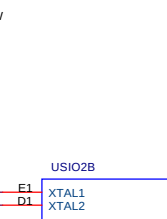


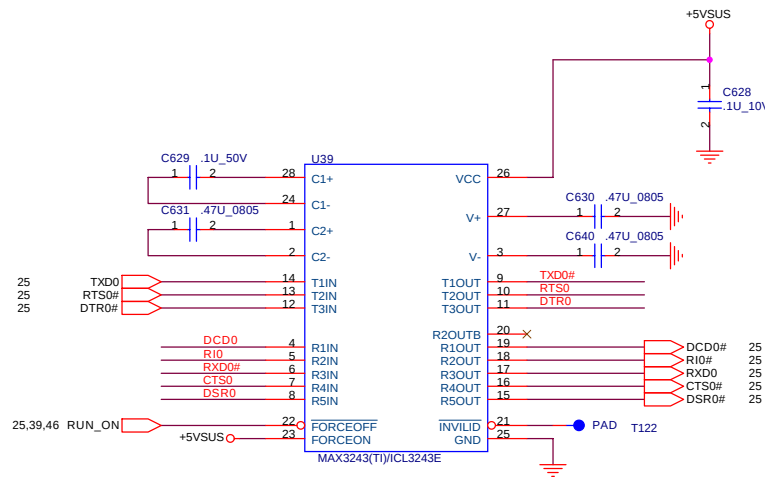
AD[0..31] 10,21,35



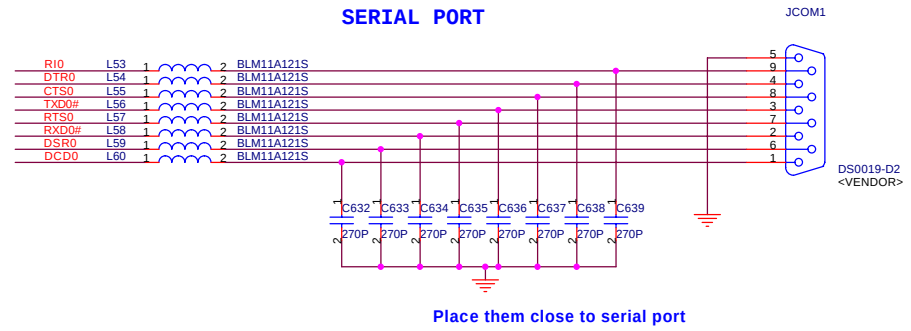








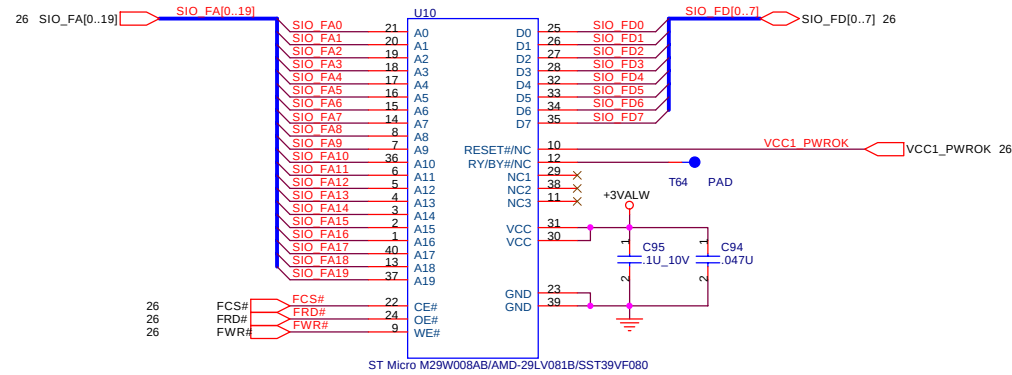
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out



Place them close to serial port

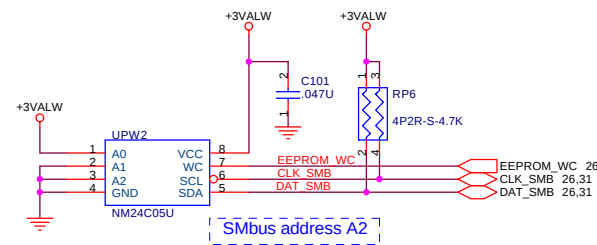
BIOS FLASH MEMORY

8Mbit (1M Byte), ISN'T PLCC TYPE



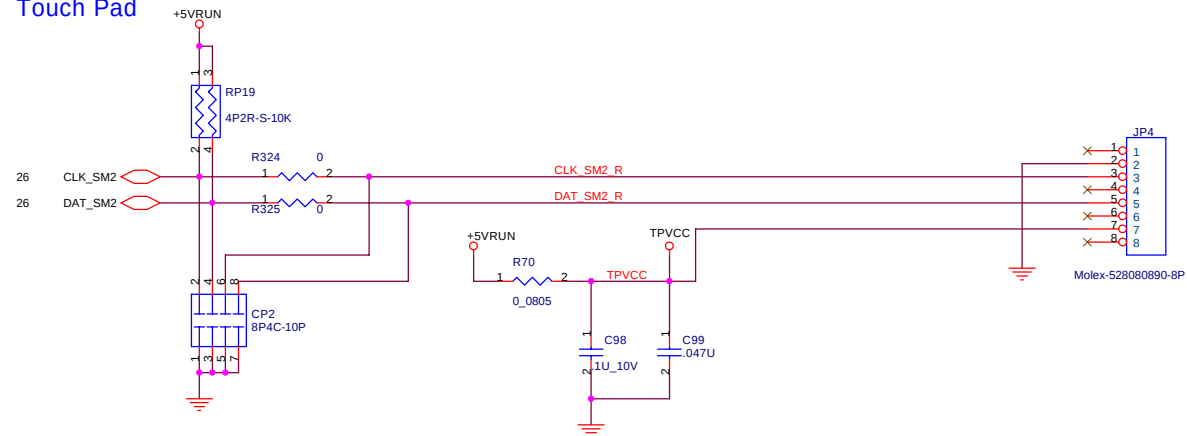
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

- 1.AMD-29LV081B require MAX 500ns Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

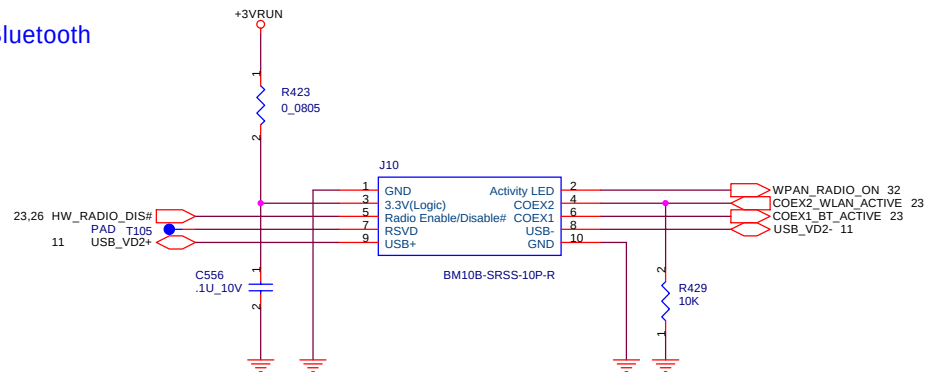


User Password

Touch Pad



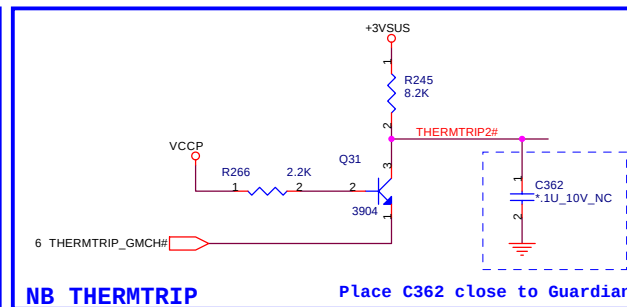
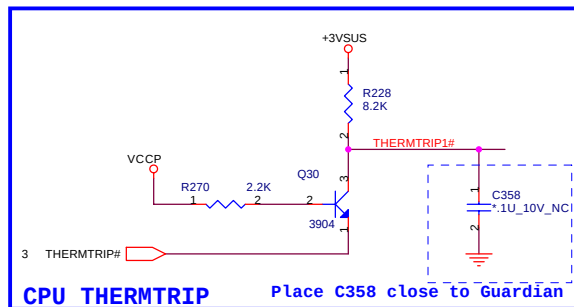
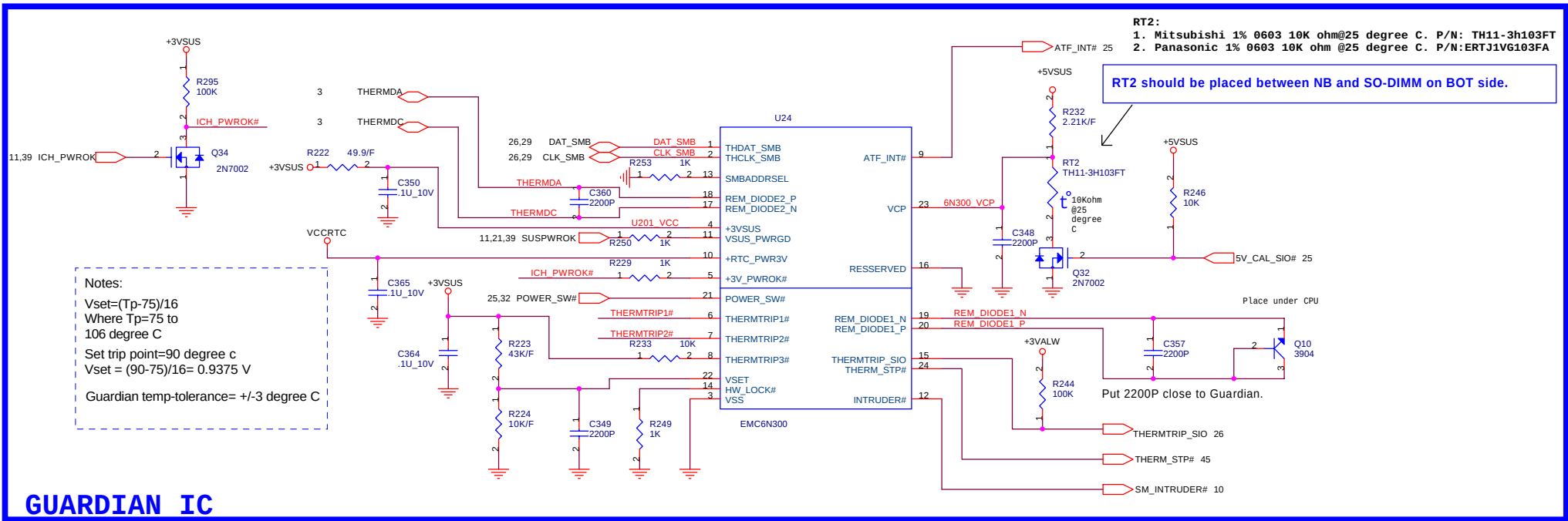
Bluetooth

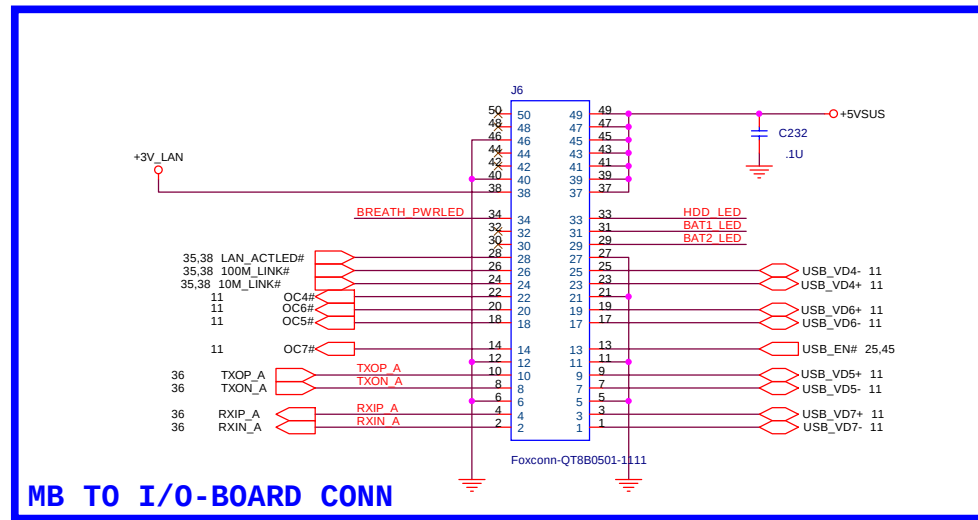
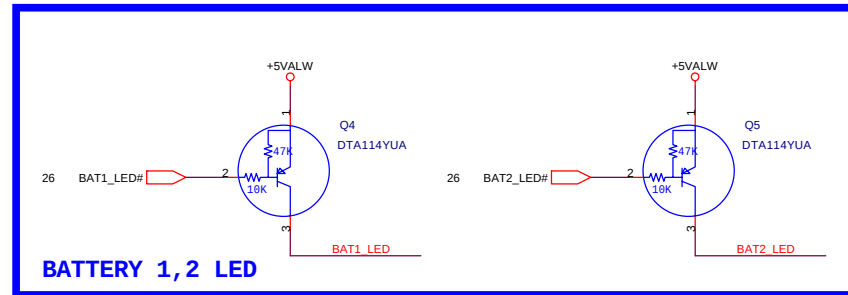
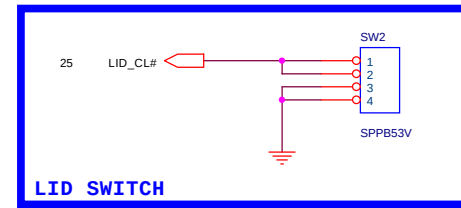
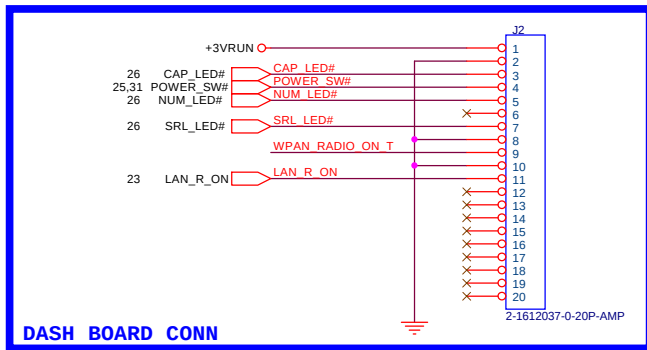
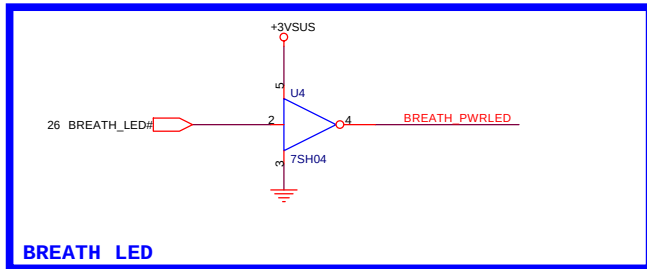
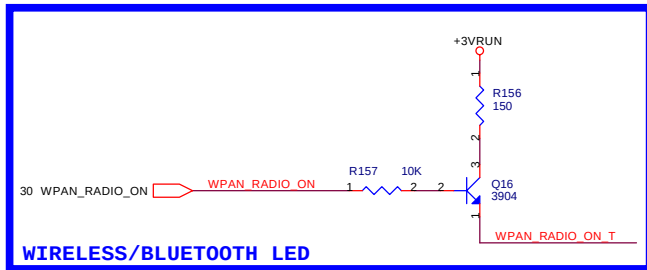
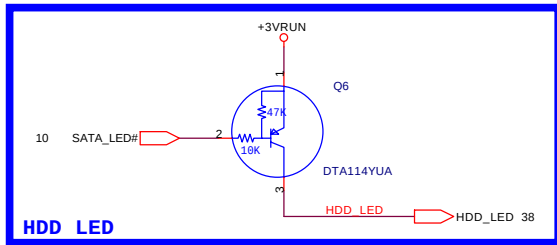


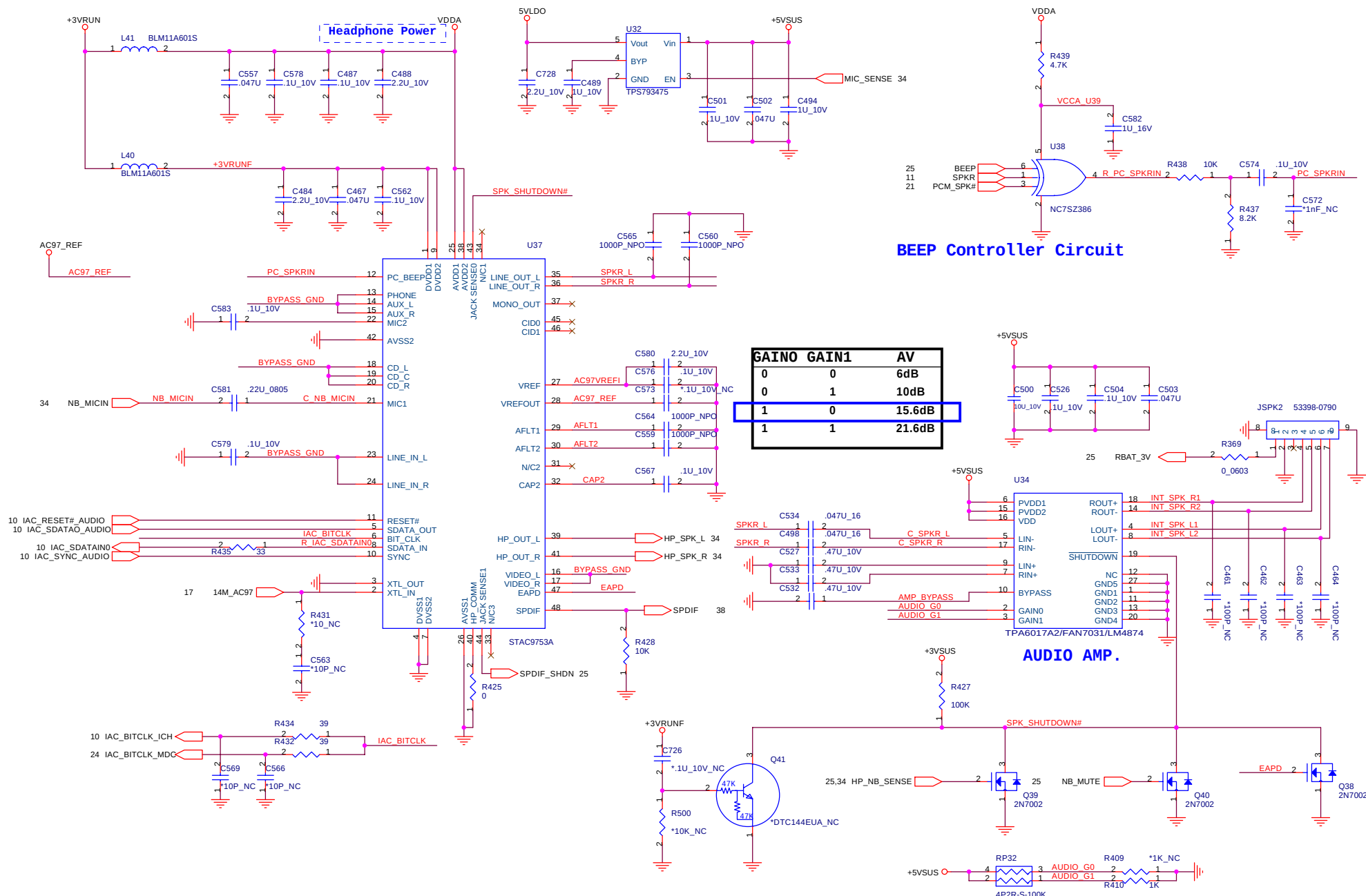
Title		
TOUCH PAD & BULE TOOTH		
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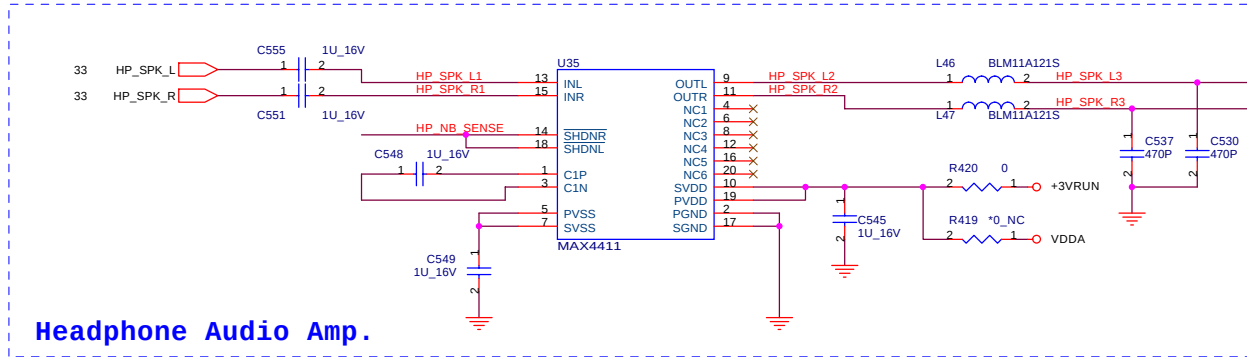
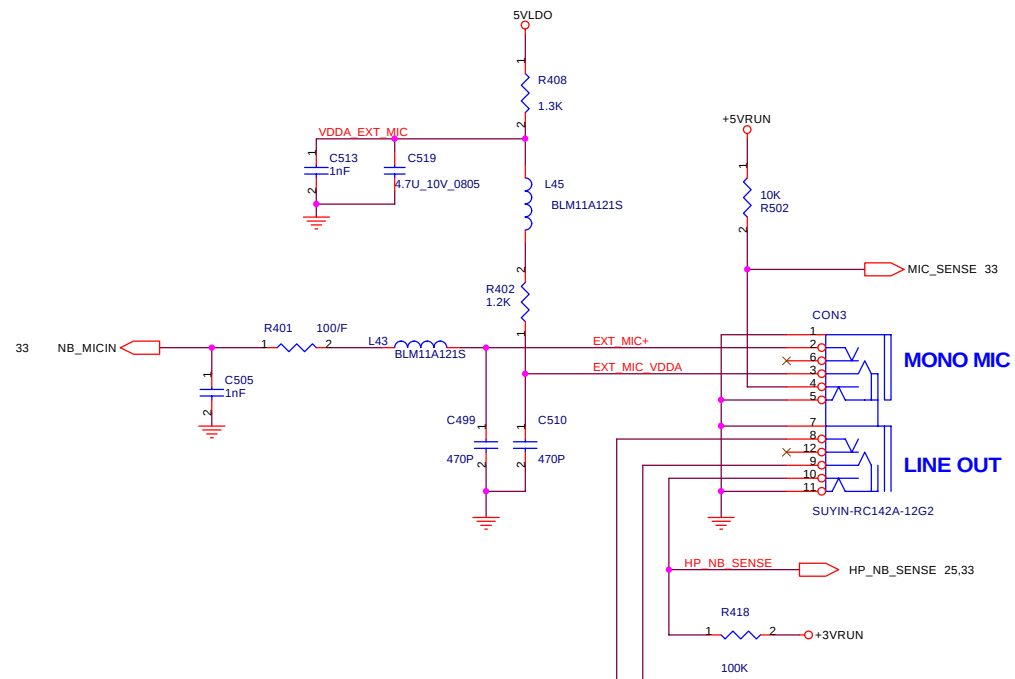
FAN Controller & FAN CONN.

The schematic diagram illustrates a fan control circuit. It starts with a 15V supply connected to the non-inverting input of an LM358 op-amp (U26A). The op-amp's output drives a MOSFET (Q13, FDC653N), which in turn controls the fan (FAN1, MOLEX-53398-0390). The circuit includes several passive components: resistors (R252, 120K, R42, 120K, R41, 78.7K/F, R40, 10K), capacitors (C375, .22U_0805, C372, 2200P, C384, .1U_50V, C70, 22U), and diodes (D7, DAN202U). The fan is connected to the VCCFAN1 pin of the FAN1 connector. The circuit is labeled with pin numbers and component values.



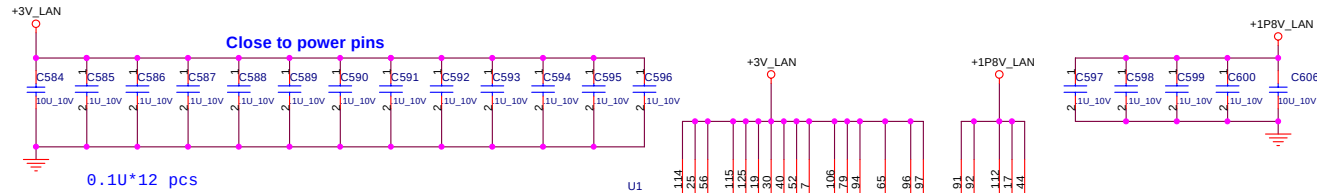






LAN - BCM4401KFB (10/100M)

BCM4401 - -10/100

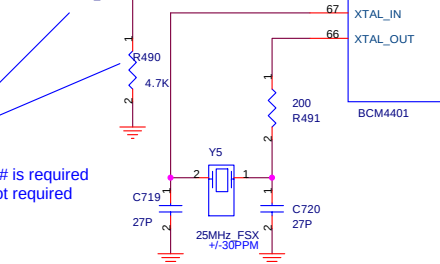
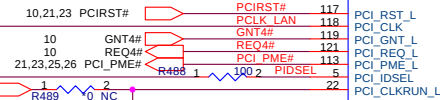
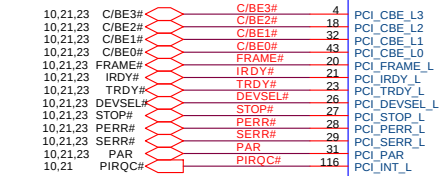
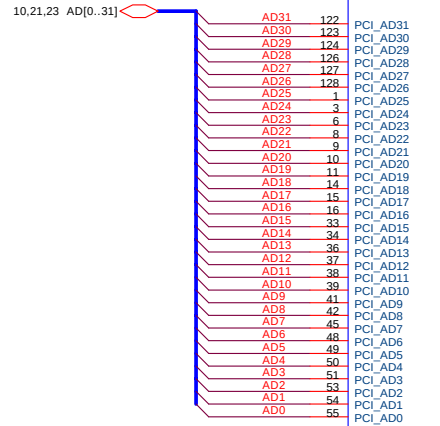


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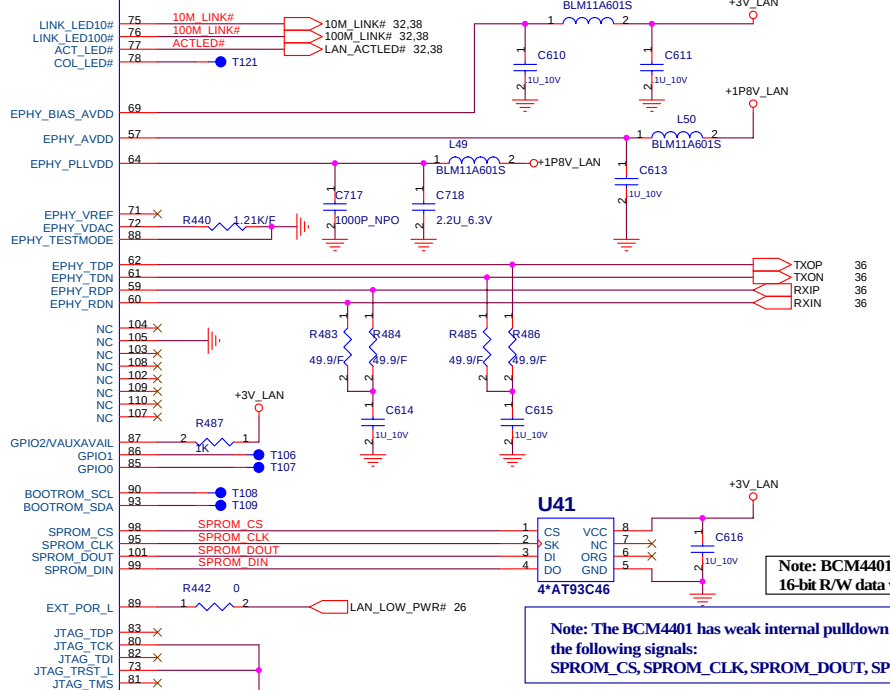
ID Select      : AD16
Interrupt Pin   : PIRQC#
Request indicate : REQ4#
Grant indicate  : GNT4#

```

BCM4401KQL
128P QFP



Note: Pop R489 depop R490 when CLKRUN# is required
Pop R490 depop R489 when CLKRUN# is not required



**Note: BCM4401 requires
16-bit R/W data width**

Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.

Note: EXT_POR_L has a internal pull up.



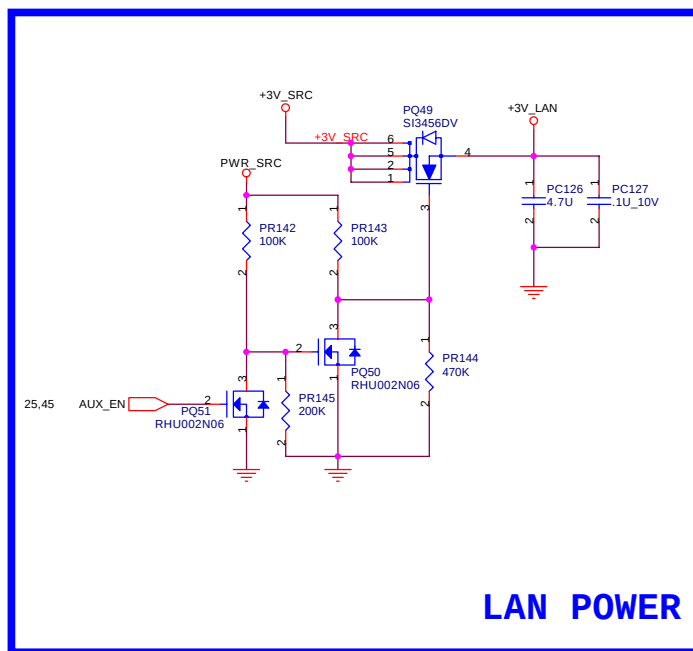
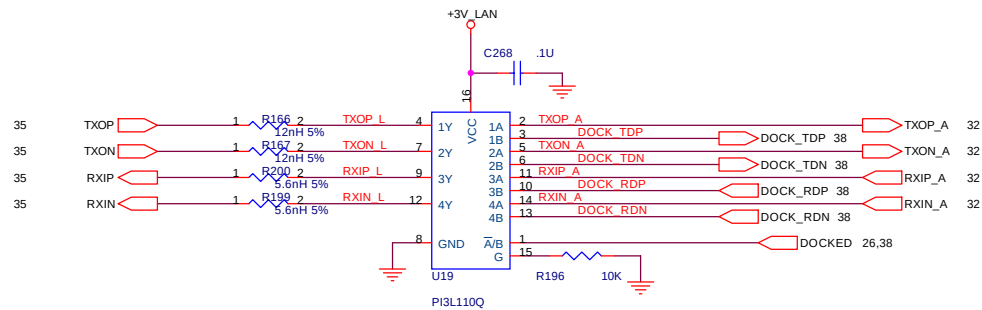
QUANTA
COMPUTER

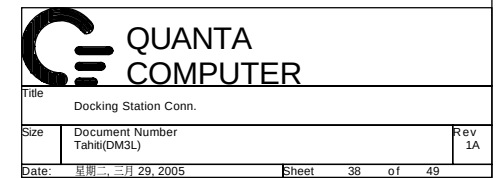
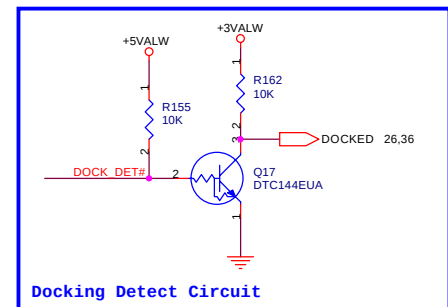
Title	BCM4401 100/10 LAN
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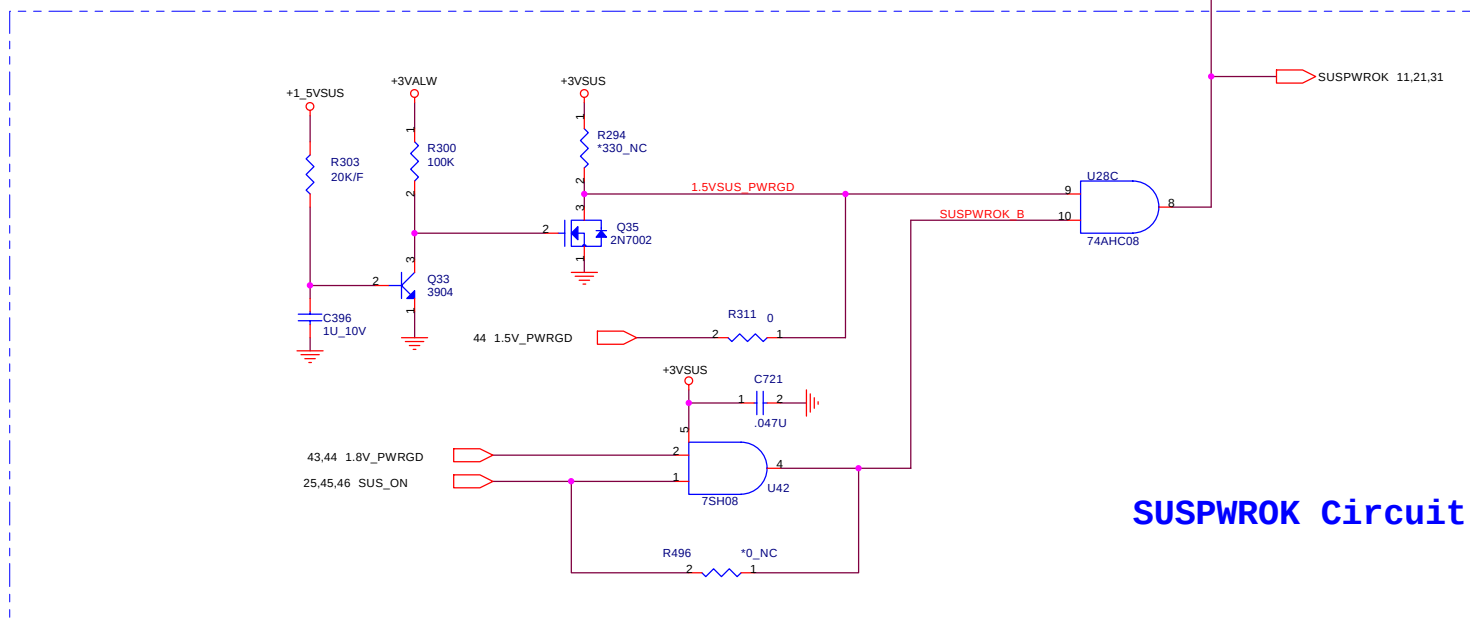
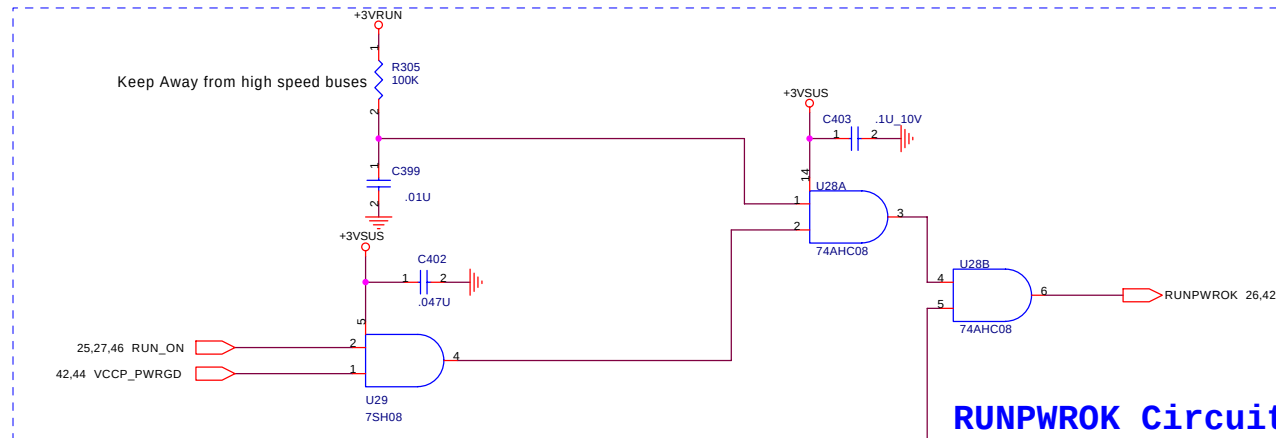
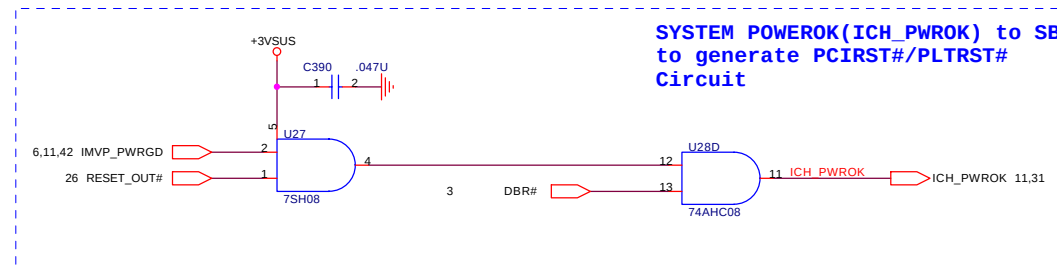
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1A

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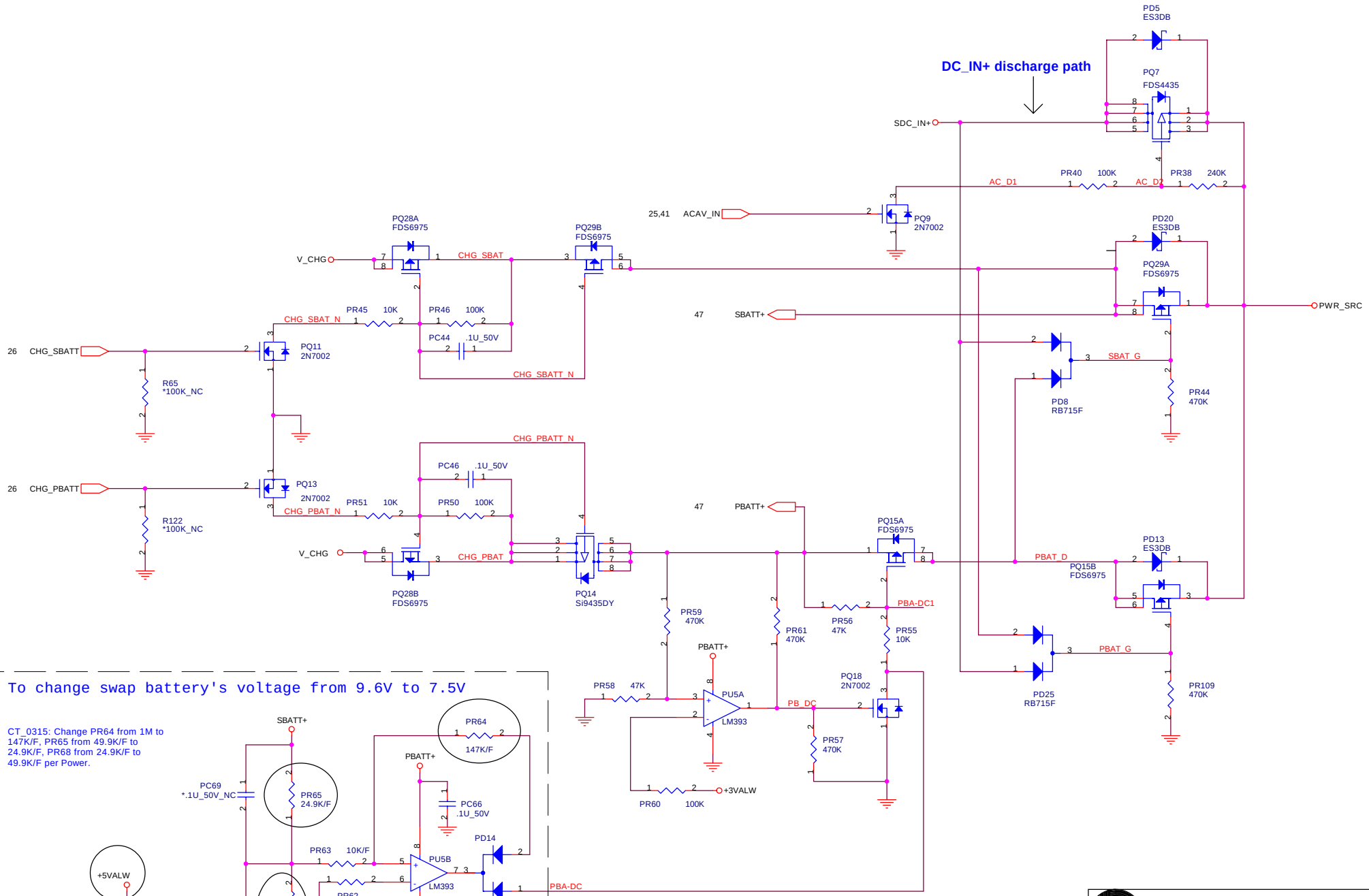
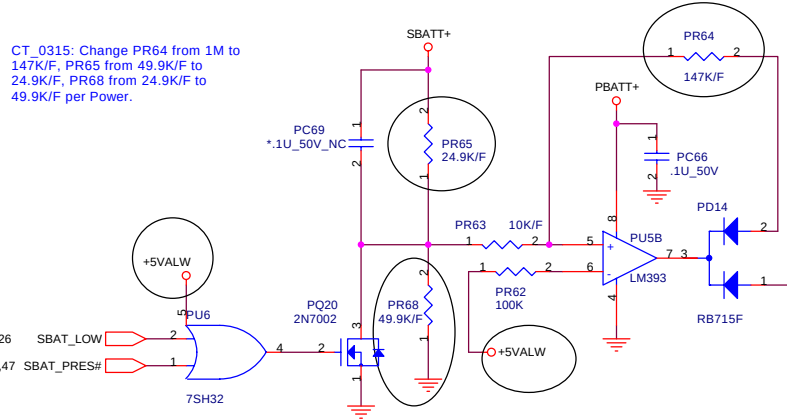






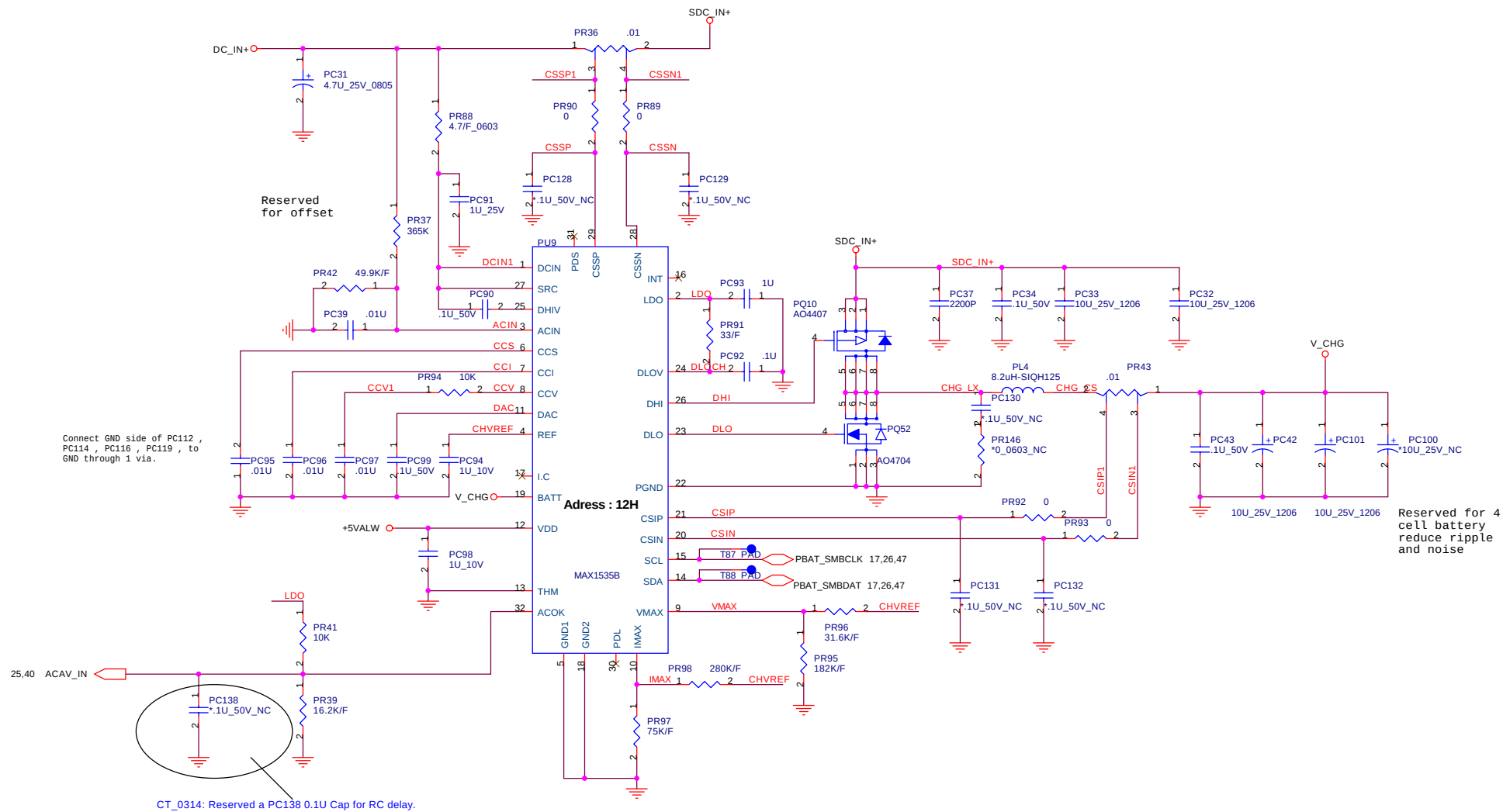
To change swap battery's voltage from 9.6V to 7.5V

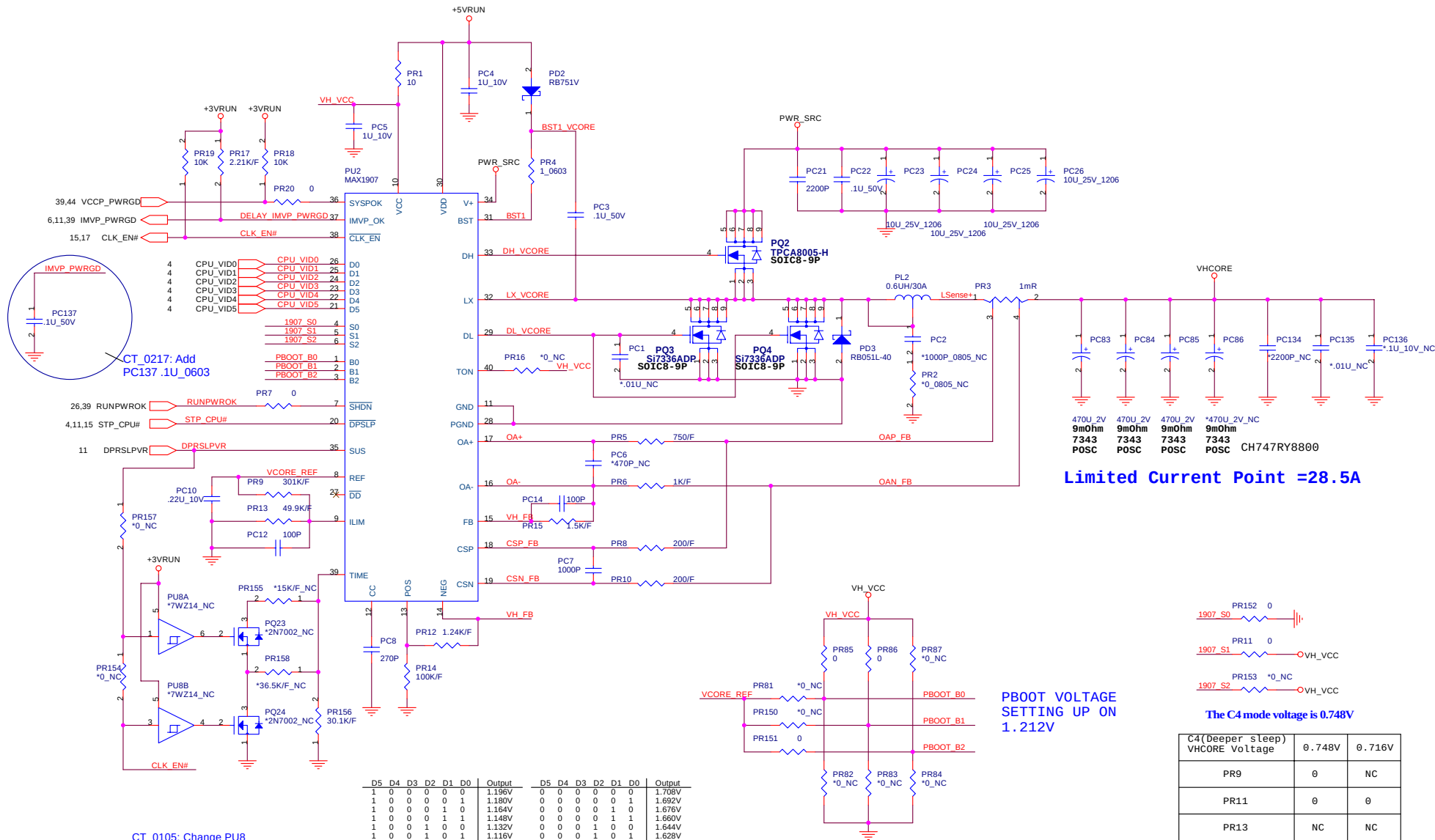
CT_0315: Change PR64 from 1M to 147K/F, PR65 from 49.9K/F to 24.9K/F, PR68 from 24.9K/F to 49.9K/F per Power.



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Title			BATTERY SELECTOR
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Limited Current Point =28.5A

PBOOT VOLTAGE
SETTING UP ON
1.212V

C4(deeper sleep) VHCORE Voltage	0.748V	0.716V
PR9	0	NC
PR11	0	0
PR13	NC	NC



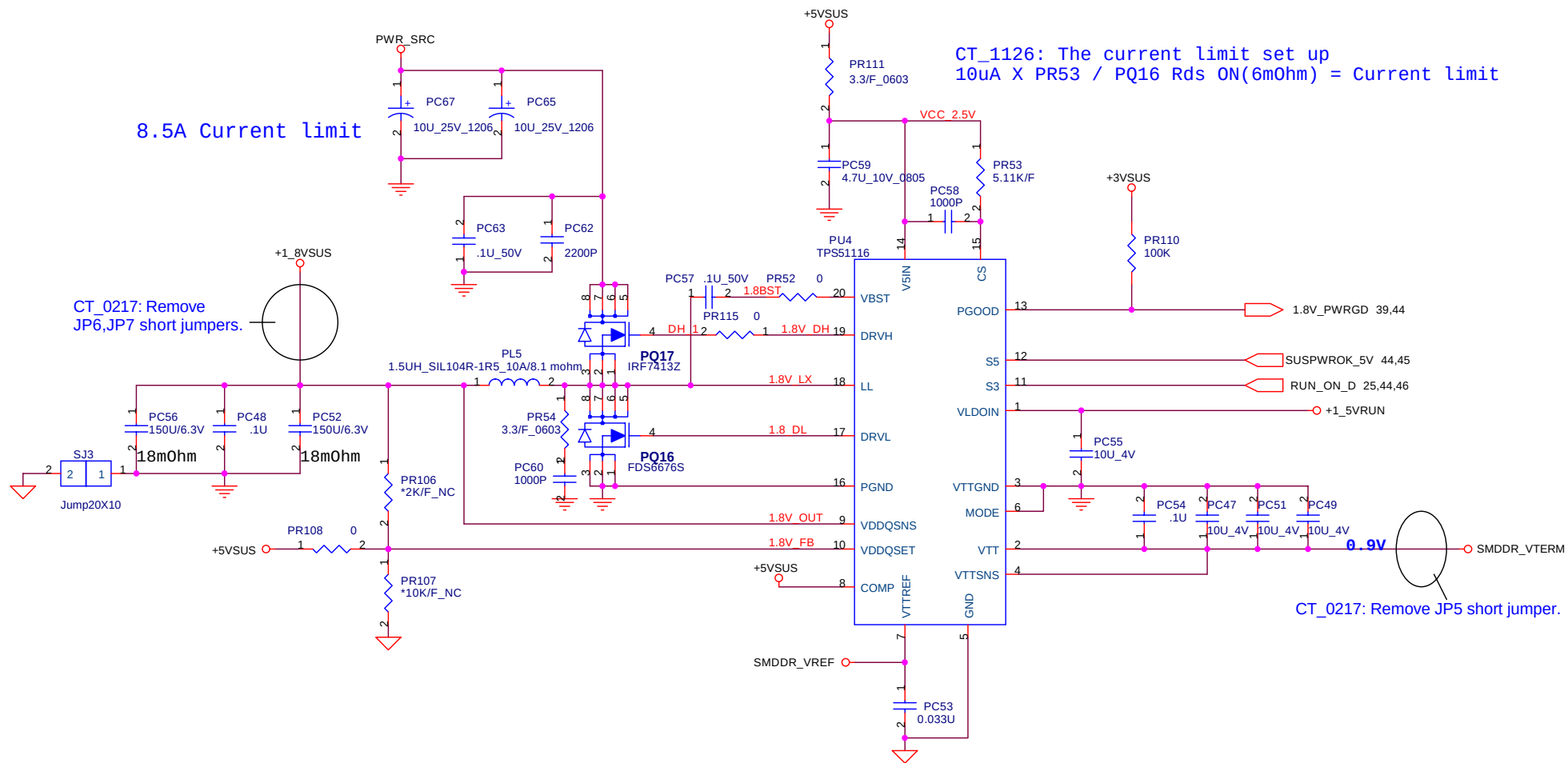
Title CPU POWER

Size Document Number DM3B

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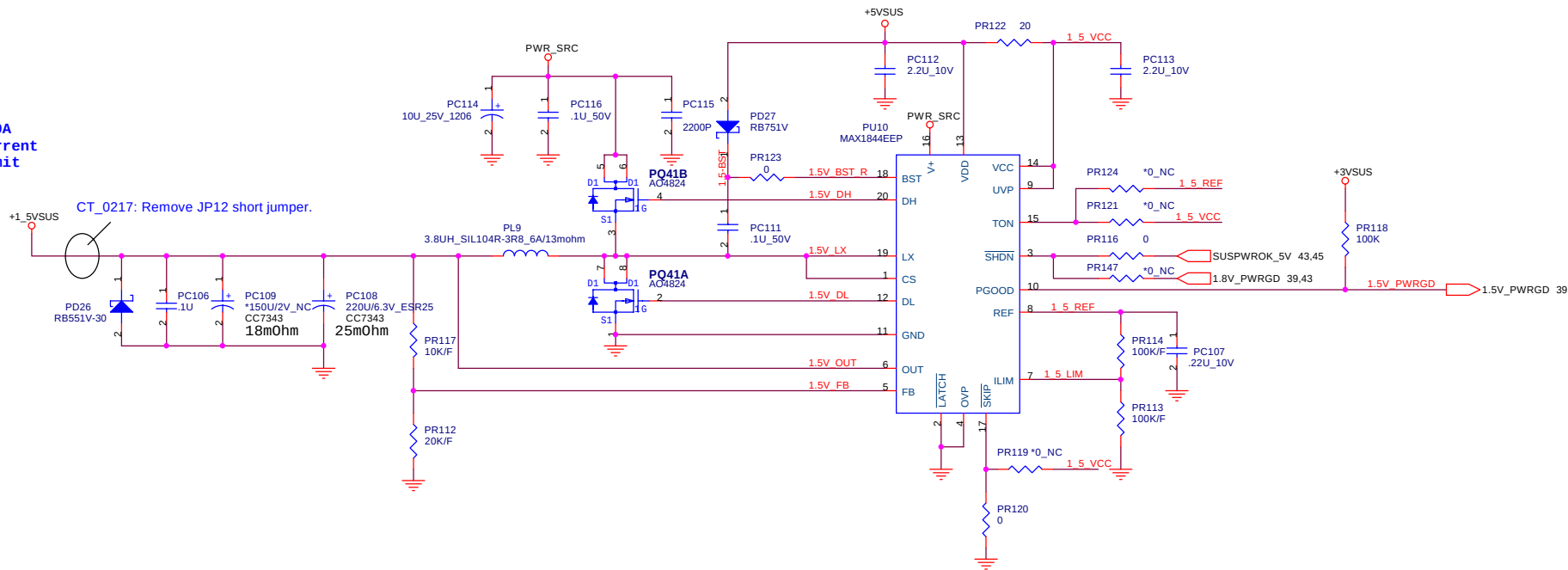
Rev 1A



Title			
1.8V, 0.9V			
Size	Document Number		Rev
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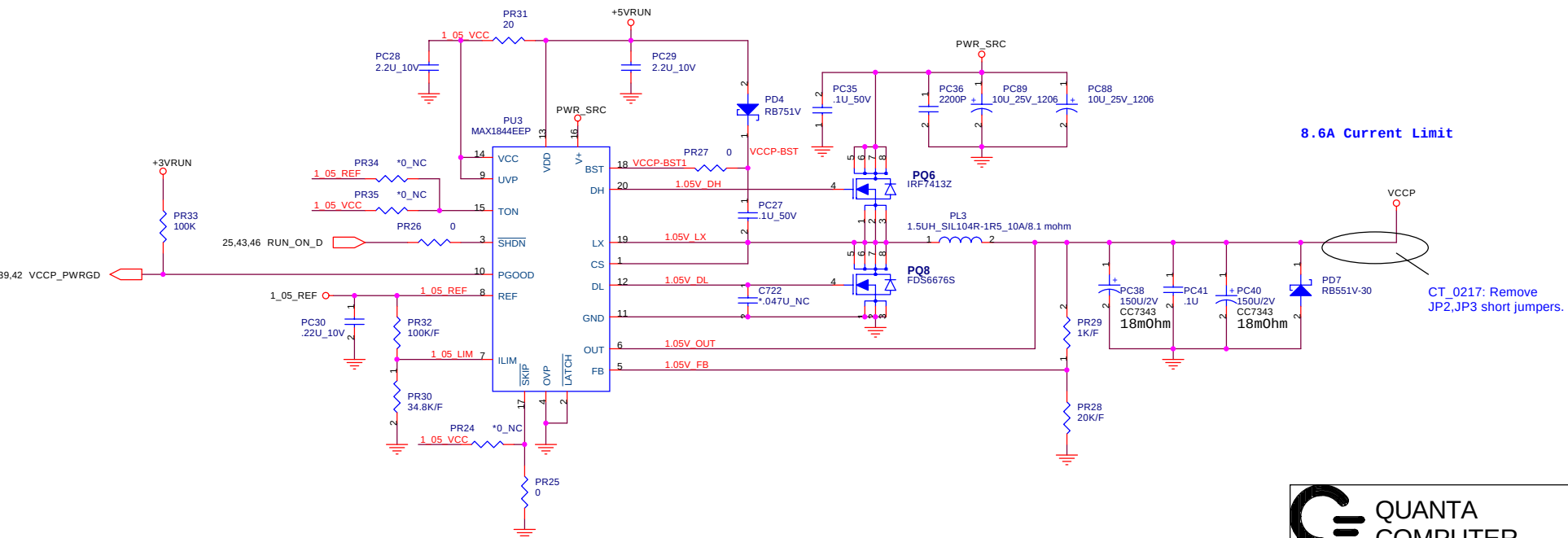
5.0A
Current
Limit

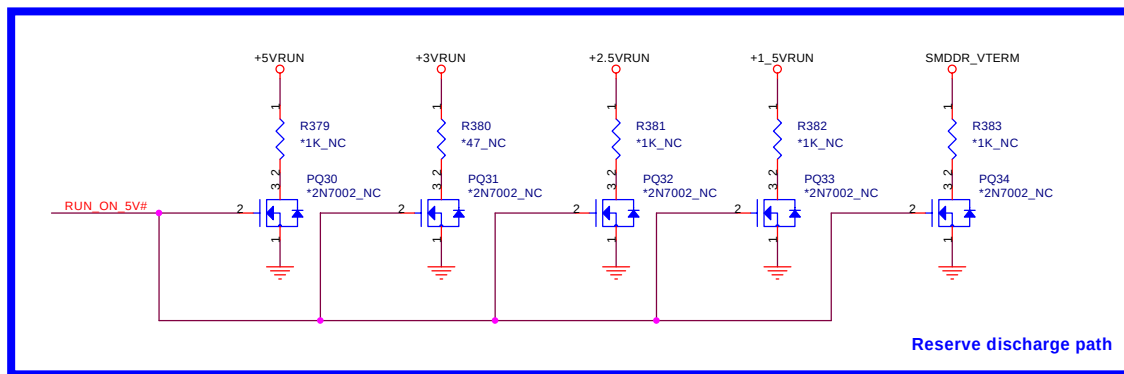
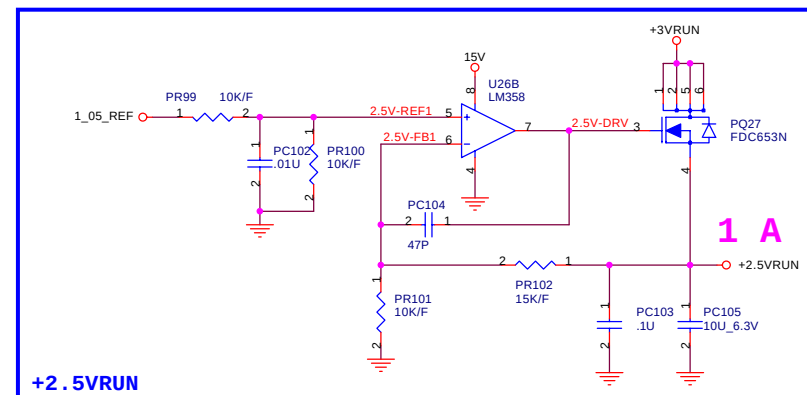
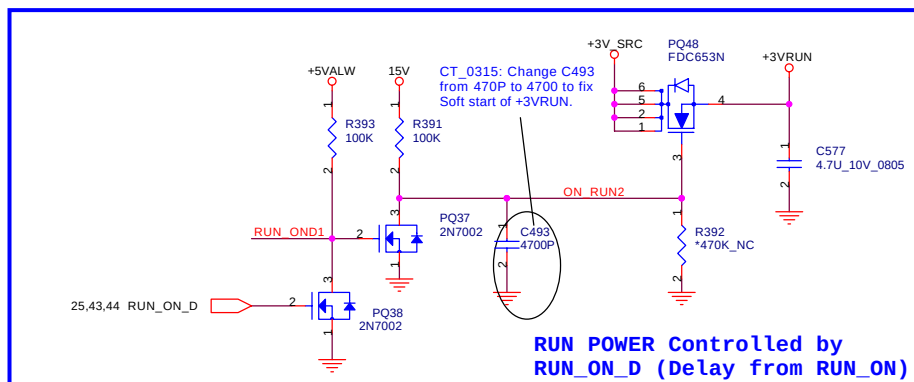
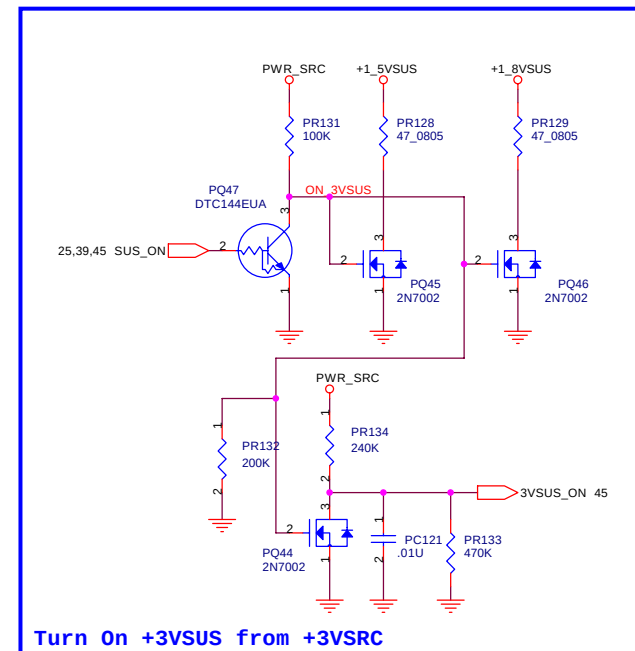
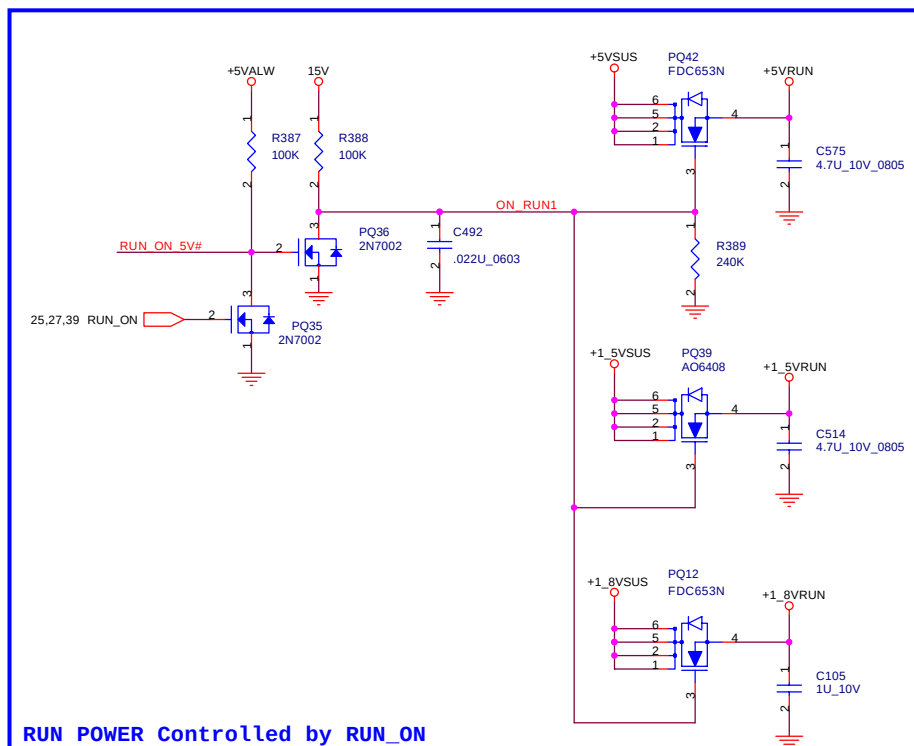
CT_0217: Remove JP12 short jumper.

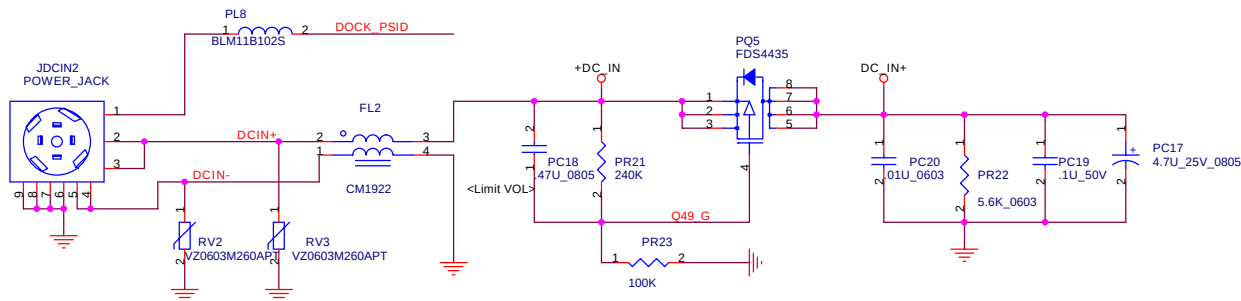
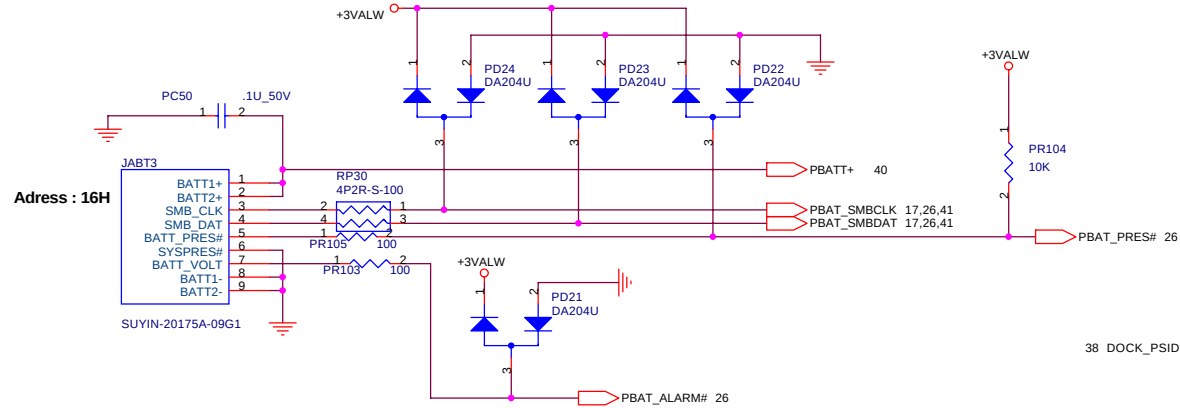
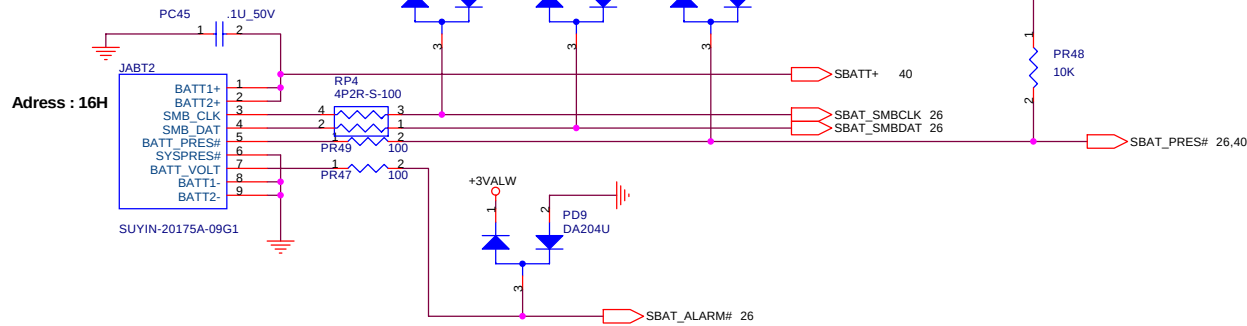


8.6A Current Limit

CT_0217: Remove
JP2,JP3 short jumpers.







QUANTA
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Title			DCIN,BATT CONNECTOR
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