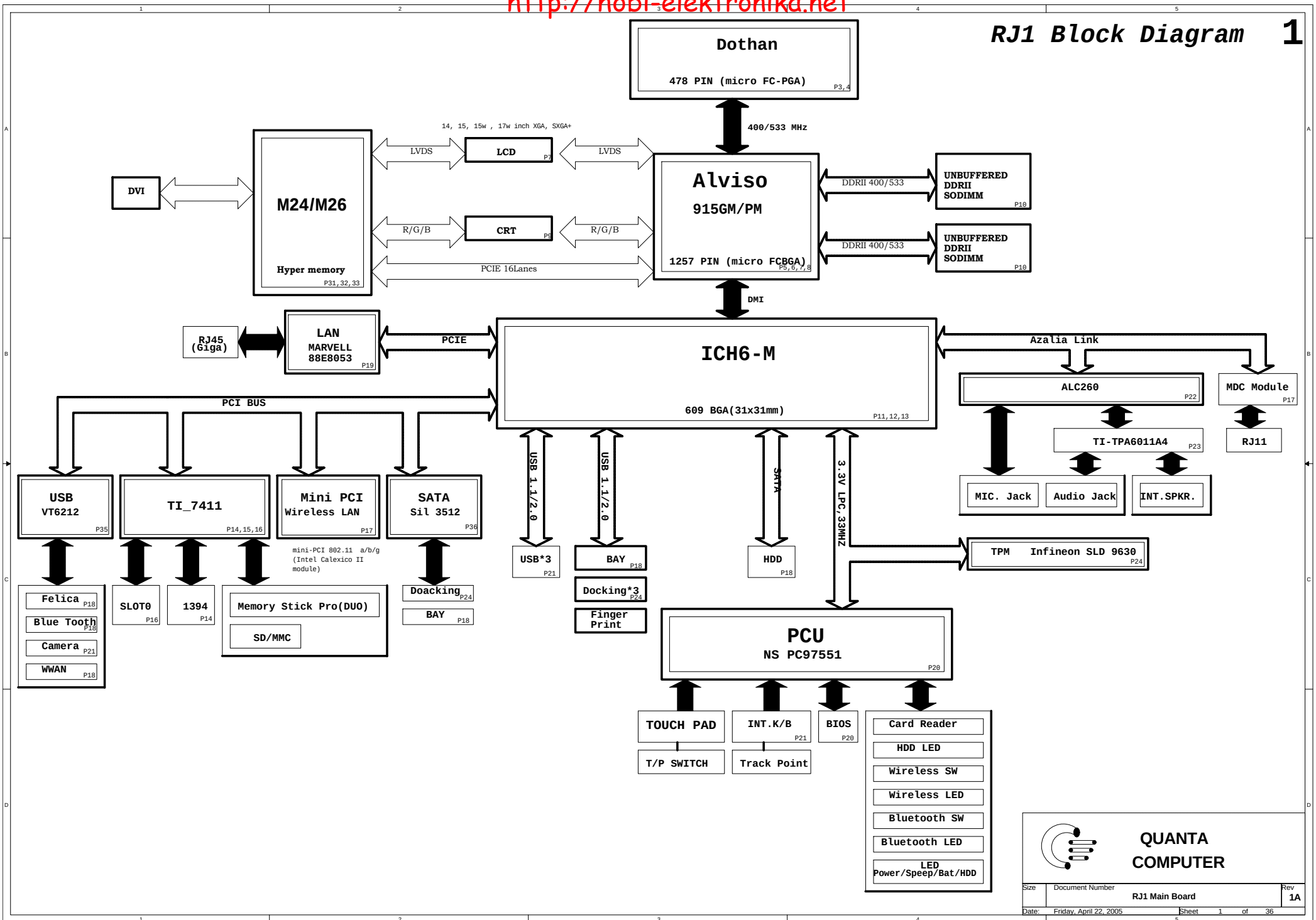
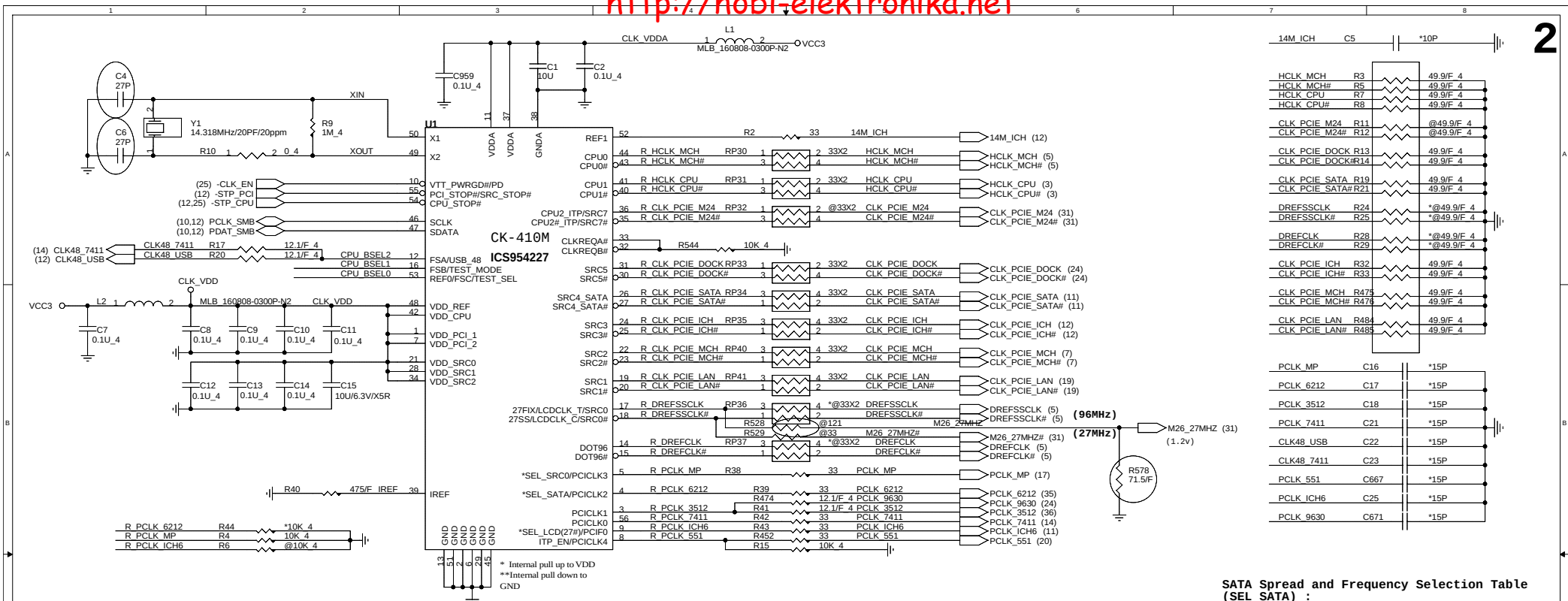


RJ1 Block Diagram 1





SEL_SRC0(Pin 17,18)(R4) 0: LCDCLK Pair 1: SRCCLK0 pair	SEL_SATA(Pin 26,27)(R44) 0: Clock from SRC PLL 1: Clock from SATA PLL
SEL_LCD(Pin 17,18)(R6) 0: 27MHZSS/27MHZSS# pair (M24/M26) 1: LCDCLK pair (9156M)	ITP_EN Function(Pin 35,36)(R15) 0: SRC 7 Pair (Pin 35,36) 1: CPU_2 ITP Pair (Pin 35,36)

IREF (Pin 39) :
475_1% : Sets the IREF current to 2.32mA

LCDCLK Spread and Frequency Selection Table (SEL_LCD) :

SEL_LCD	SS3	SS2	SS1	SS0	VCO MHZ	17, 18 MHZ	Spread %	SEL_LCD	SS3	SS2	SS1	SS0	VCO MHZ	17, 18 MHZ	Spread %
1	0	0	0	0	500	100	+/-1.5	0	0	0	0	0	864	27	+/-0.25
1	0	0	0	1	500	100	+/-1.25	0	0	0	0	1	864	27	+/-0.5
1	0	0	1	0	500	100	+/-1.0	0	0	0	1	0	864	27	+/-0.75
1	0	0	1	1	500	100	+/-0.8	0	0	0	1	1	864	27	+/-1
1	0	1	0	0	500	100	+/-0.6	0	0	1	0	0	864	27	+/-1.25
1	0	1	0	1	500	100	+/-0.5	0	0	1	0	1	864	27	+/-1.5
1	0	1	1	0	500	100	+/-0.4	0	0	1	1	0	864	27	+/-1.75
1	0	1	1	1	500	100	+/-0.3	0	0	1	1	1	864	27	+/-2
1	1	0	0	0	500	100	3	0	1	0	0	0	864	27	-0.5
1	1	0	0	1	500	100	2.5	0	1	0	0	1	864	27	-1
1	1	0	1	0	500	100	2	0	1	0	1	0	864	27	-1.25
1	1	0	1	1	500	100	1.75	0	1	0	1	1	864	27	-1.5
1	1	1	0	0	500	100	1.5	0	1	1	0	0	864	27	-1.75
1	1	1	0	1	500	100	1.25	0	1	1	0	1	864	27	-2
1	1	1	1	0	500	100	1	0	1	1	1	0	864	27	-2.5
1	1	1	1	1	500	100	0.8	0	1	1	1	1	864	27	-3

SATA Spread and Frequency Selection Table (SEL_SATA) :

SEL_SATA	SS3	SS2	VCO MHZ	27, 26 MHZ	Spread %
1	0	0	tbd	100	-0.2 Down
1	0	1	tbd	100	-0.3 Down
1	1	0	tbd	100	-0.4 Down
1	1	1	tbd	100	-0.5 Down

Signal		915GM	915PM
CLK_PCIE_M24	RP32	NI	33X2
	R11	NI	49.9/F_4
	R12	NI	49.9/F_4
DREFSSCLK	RP36	33X2	NI
	R24	49.9/F_4	NI
	R25	49.9/F_4	NI
DREFCLK	RP37	33X2	NI
	R28	49.9/F_4	NI
	R29	49.9/F_4	NI
DREFSSCLK	R528	NI	121
	R529	NI	33
R_PCLK_ICH6	R6	NI	10K_4

QUANTA COMPUTER

Title: **CLOCK GENERATOR**

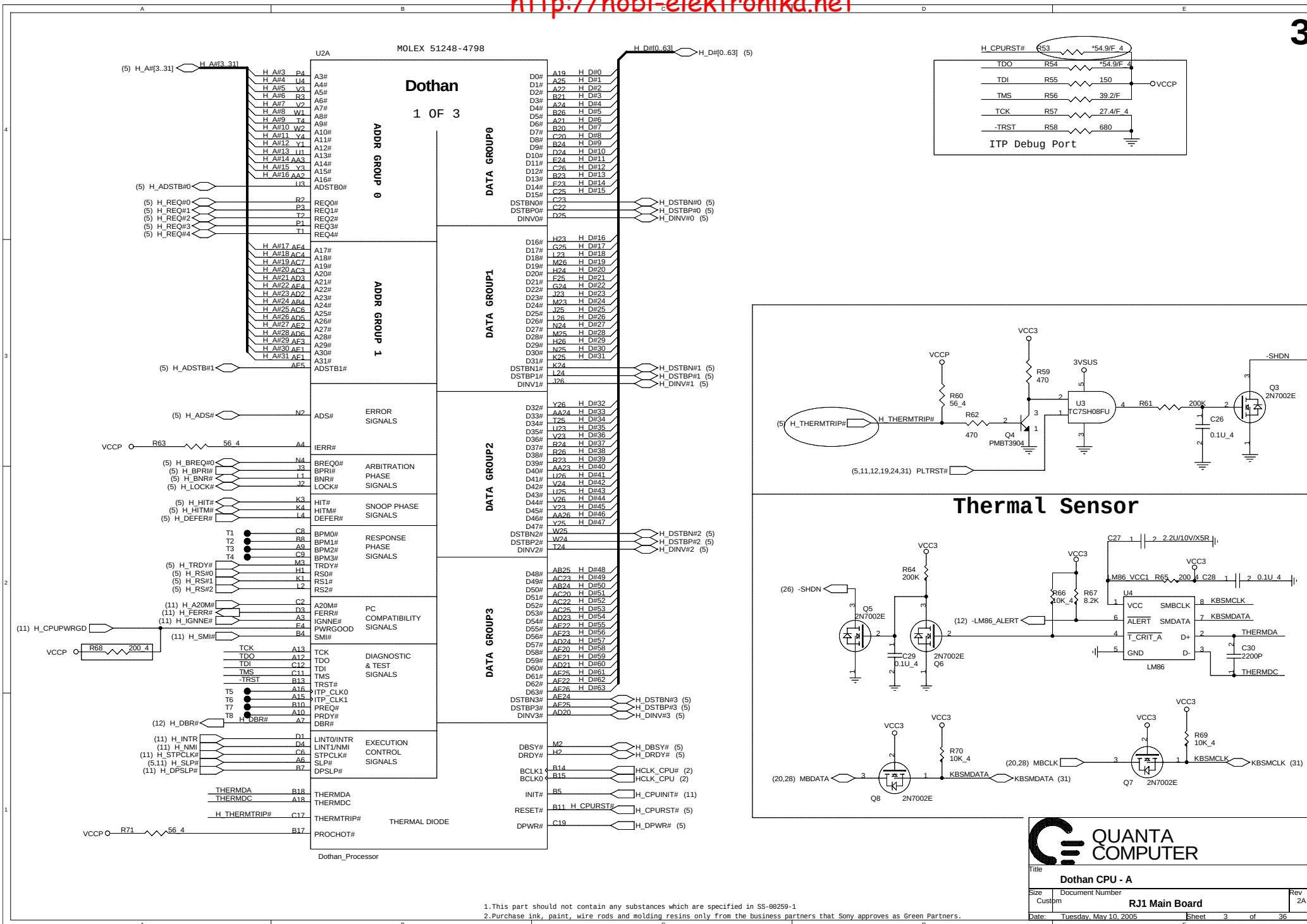
Size: **RJ1 Main Board**

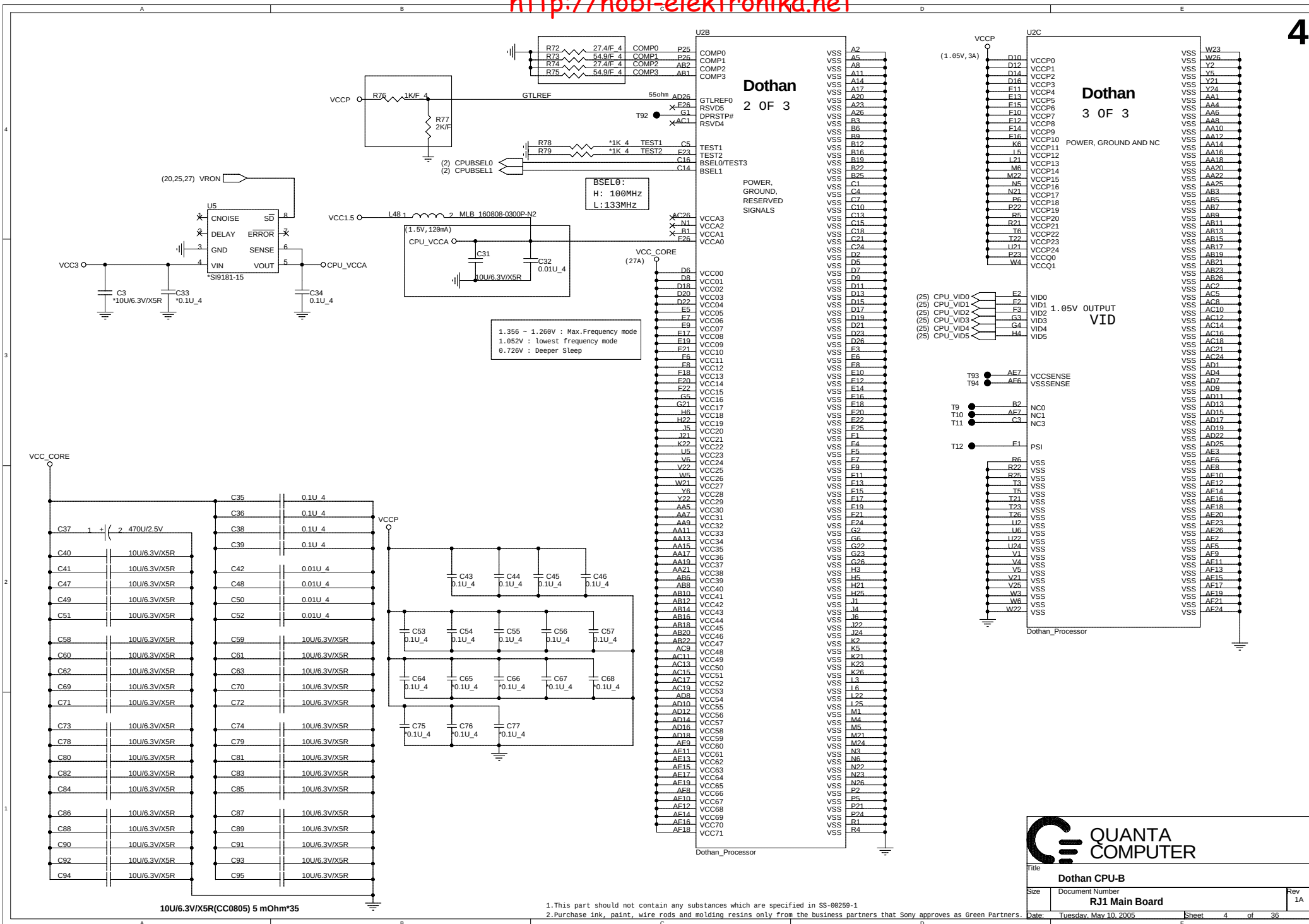
Document Number: **RJ1 Main Board**

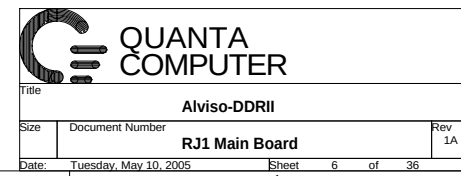
Date: **Tuesday, May 10, 2005**

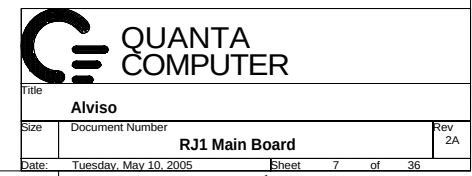
Sheet: **2** of **36**

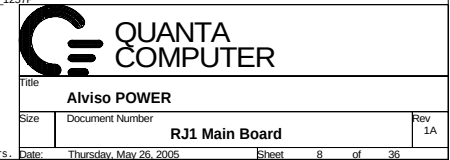
1. This part should not contain any substances which are specified in SS-00259-1
2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.



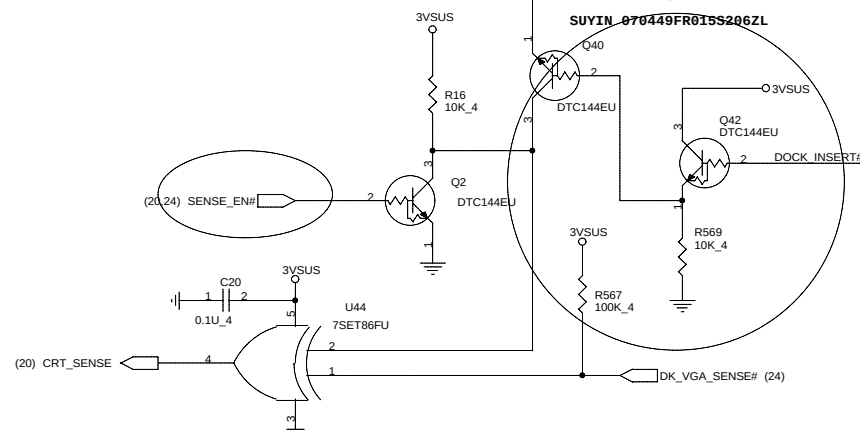
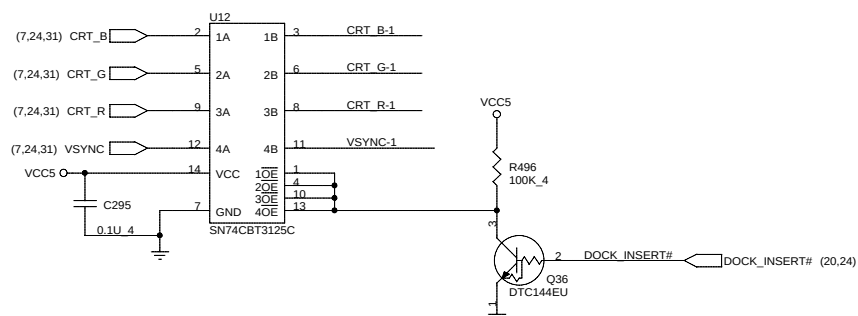
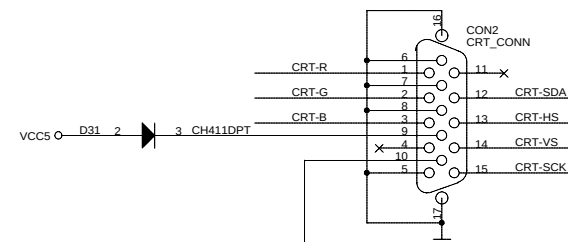








2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.



	SENSE_EN#	MB CRT	DOCK CRT	DOCK DVI	CRT_SENSE
All no Plug	L	H	H	L	L
MB CRT Plug	L	L	H	L	H
DOCK CRT Plug	L	H	L	L	H
DOCK DVI Plug	L	H	H	H	H
SENSE EN	H	X	X	X	L
DOCK CRT/DVI Plug	L	H	L	H	L
DOCK CRT/MB CRT Plug	L	L	L	L	L

A	B
H	H
H	L
L	H
L	L

Signal		915GM	915PM
VCC_DDC	R545	NI	0_4
	R546	0_4	NI

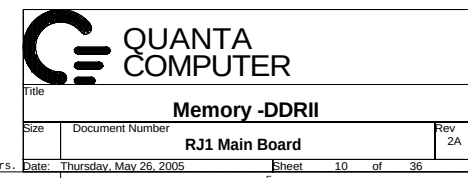


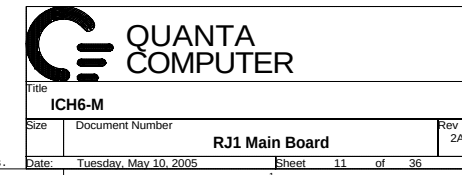
QUANTA
COMPUTER

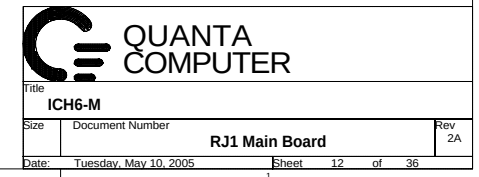
Title	CRT
-------	-----

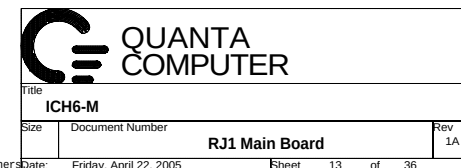
Size	Document Number	Rev
	RJ1 Main Board	2A
Date:	Tuesday, May 10, 2005	Sheet 9 of 36

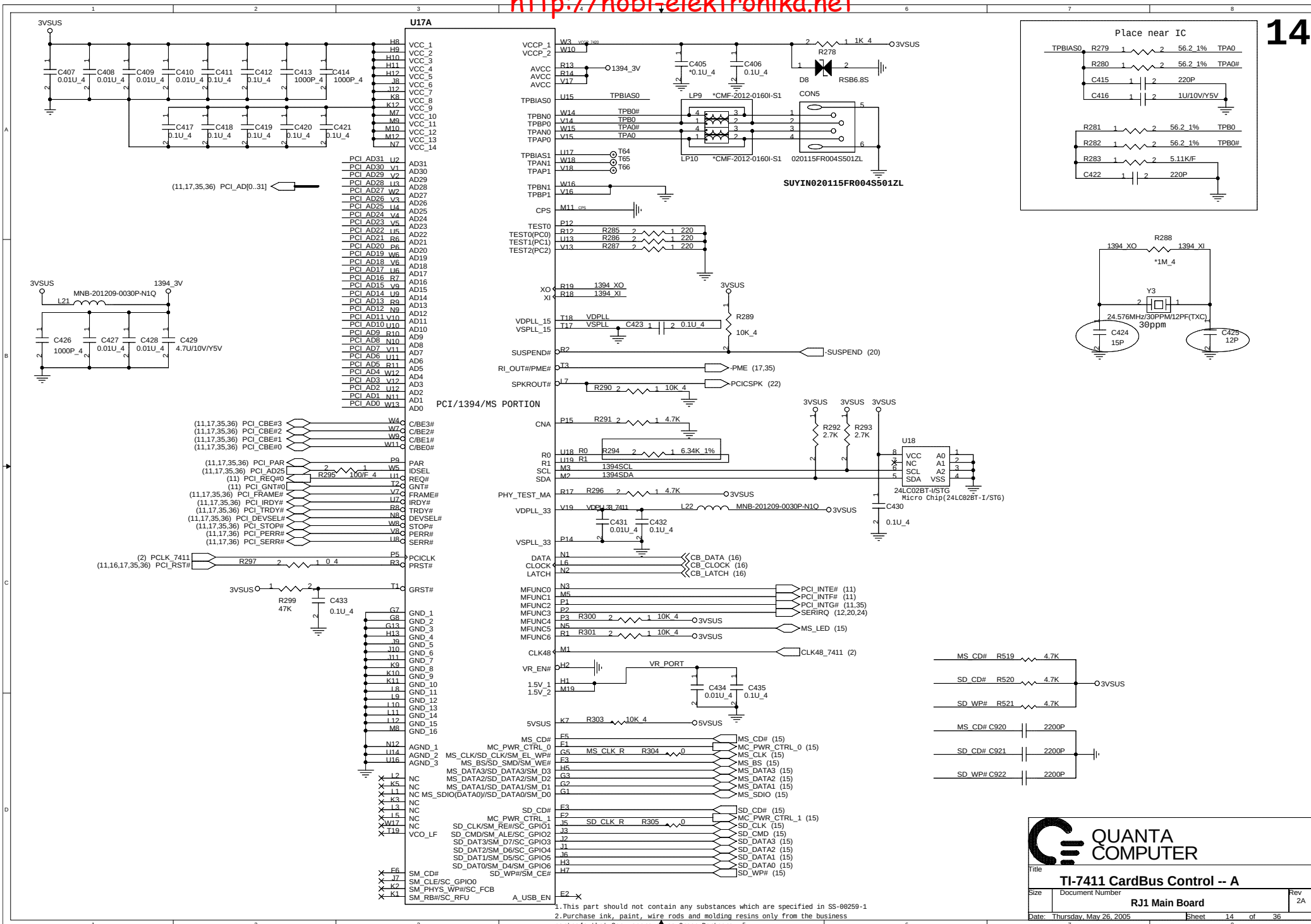
1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business
partners that Sony approves as Green Partners.

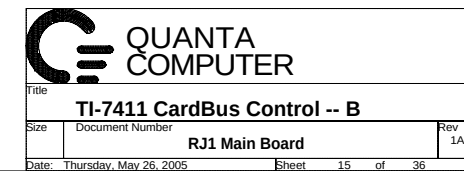






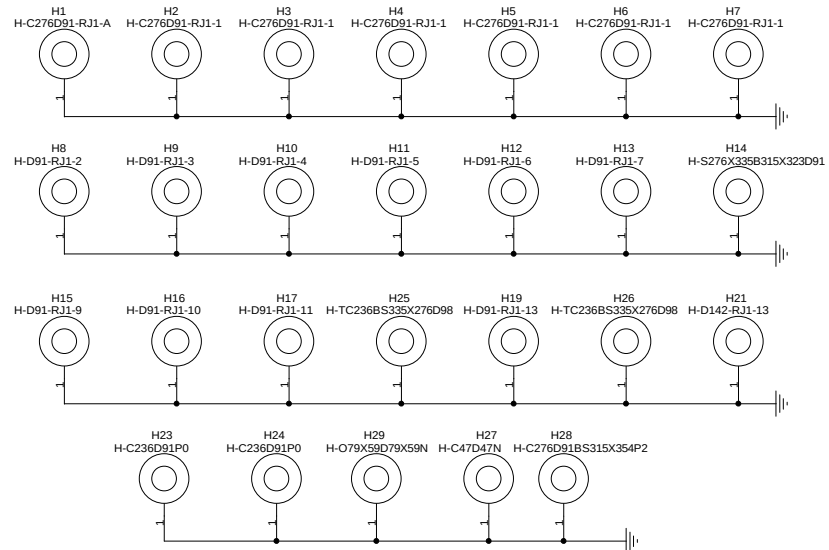
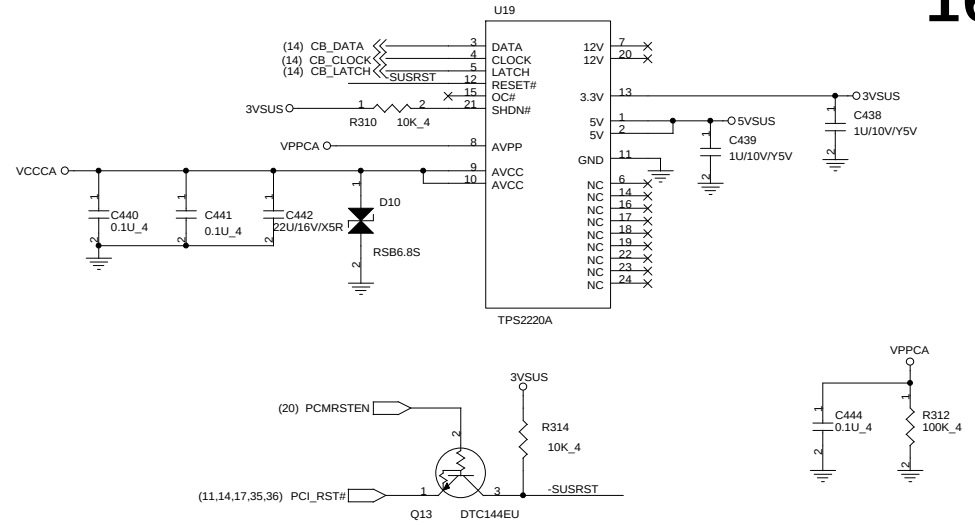
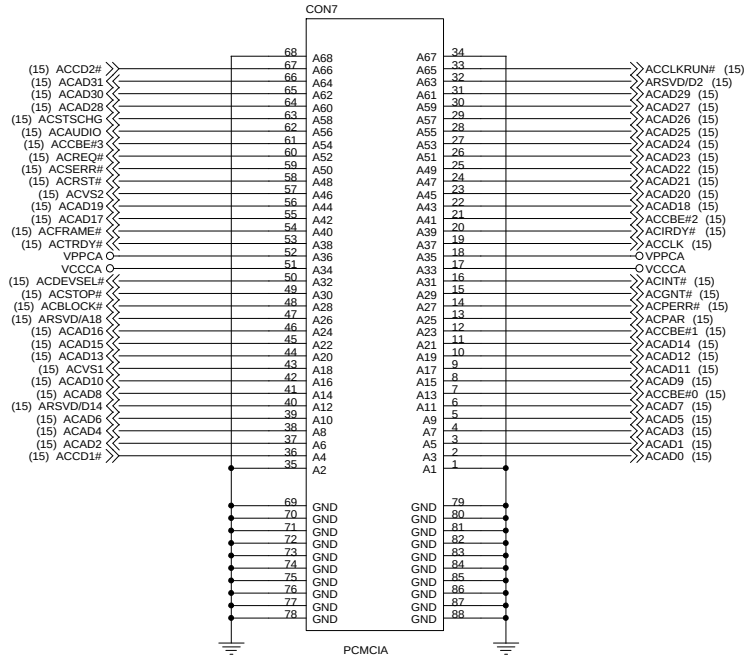






1. This part should not contain any substances which are specified in SS-00259-1
2. Purchase ink, paint, wire rods and molding resins only from the business
partners that Sony approves as Green Partners.

(15) ACAD[0..31] <<=====
(15) ACCBE#[0..3] <<=====



**QUANTA
COMPUTER**

Title
CARDBUS SLOT

Size
Document Number

Date: Thursday, May 26, 2005

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1A

RJ1 Main Board

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1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

LED_GP :LED WLEN LINK

Output Current : 7mA

Blink rate : 1 flash

per every 3 sec.

WLSW:

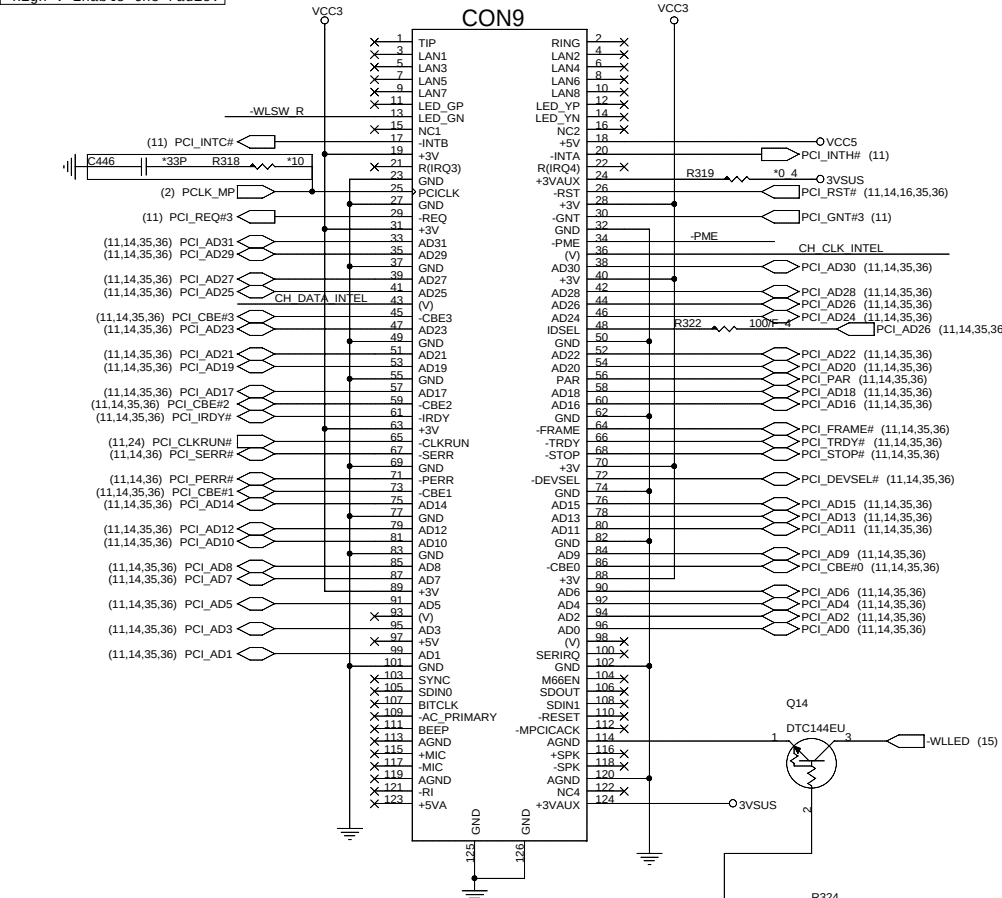
Low : disable the radio.

High : Enable the radio.

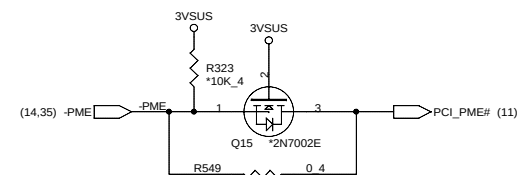
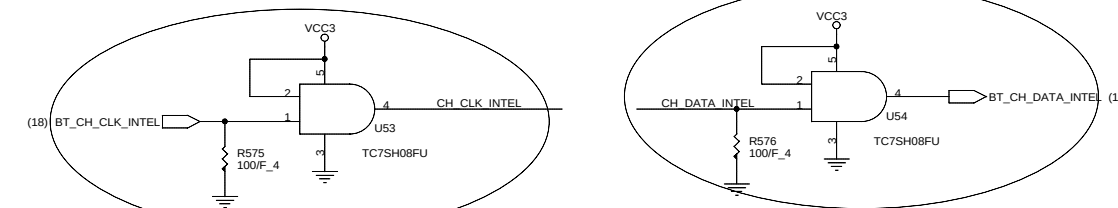
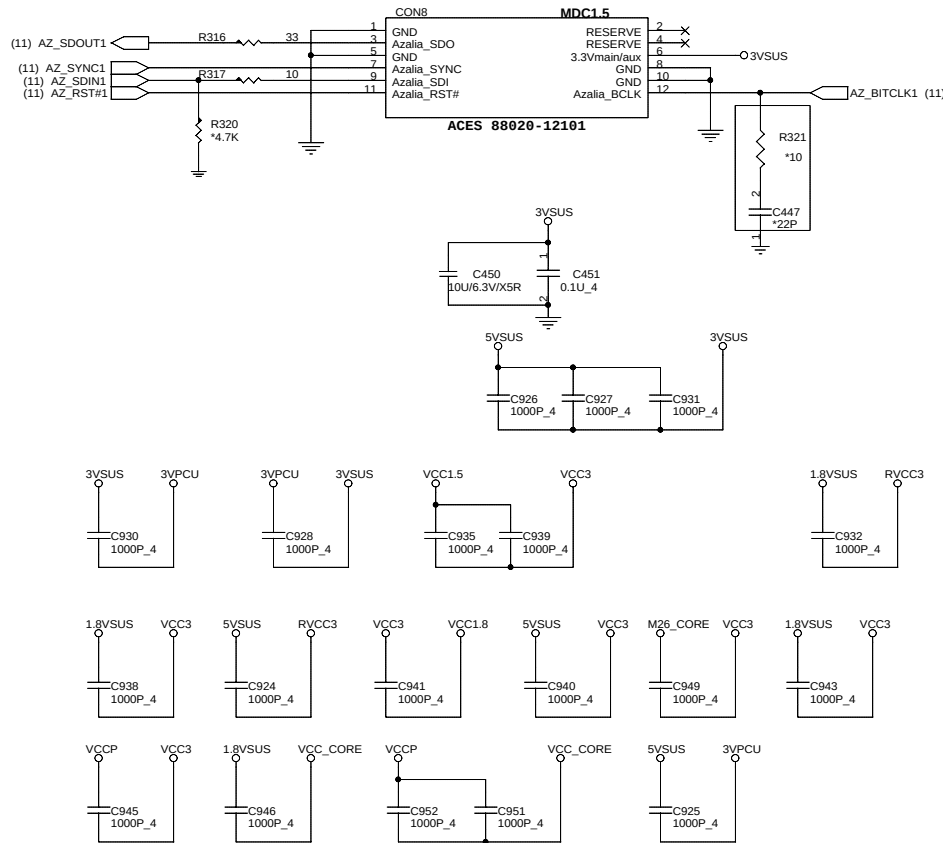
AMP 1734835-2

MINIPCI H=6.7

CON9



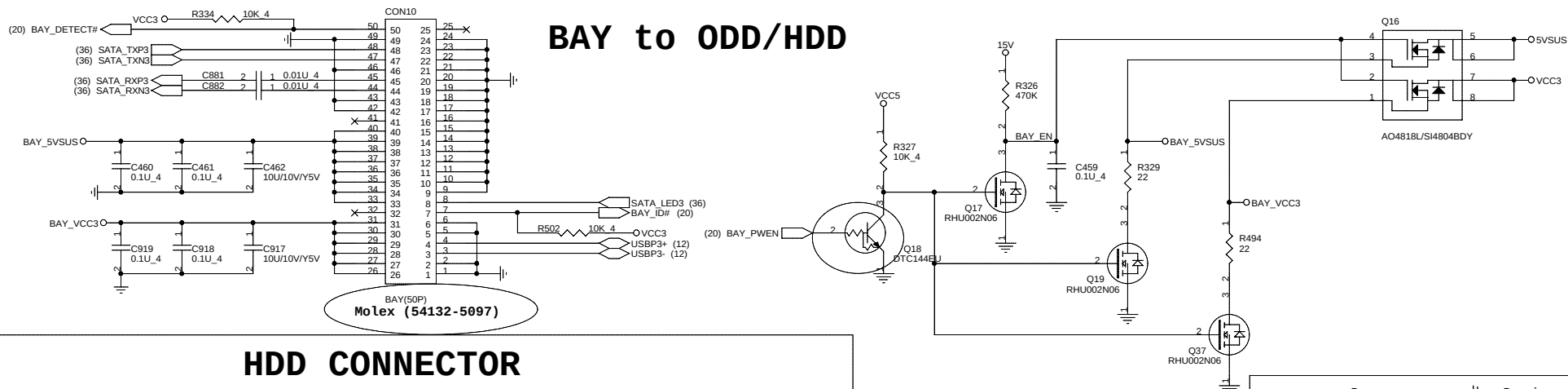
MDC V1.5



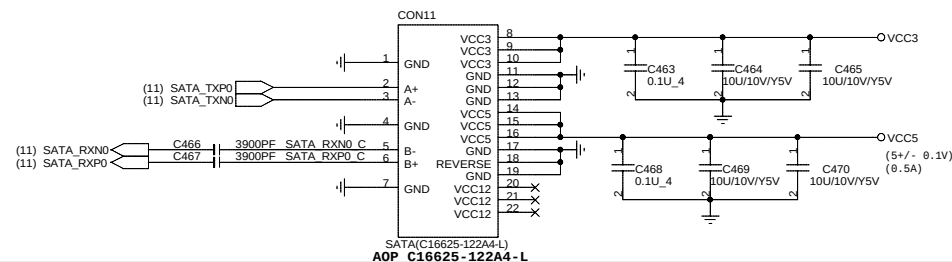
Title		MINIPCI /MDC	
Size	Document Number	Rev 2A	
Date: Tuesday, May 10, 2005		Sheet 17 of 36	

1. This part should not contain any substances which are specified in SS-00259-1
 2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

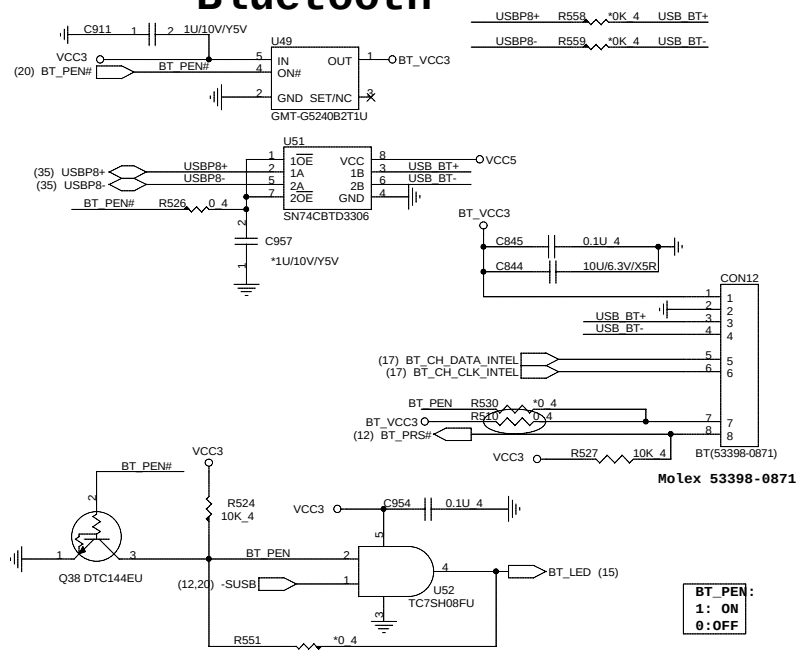
BAY to ODD/HDD



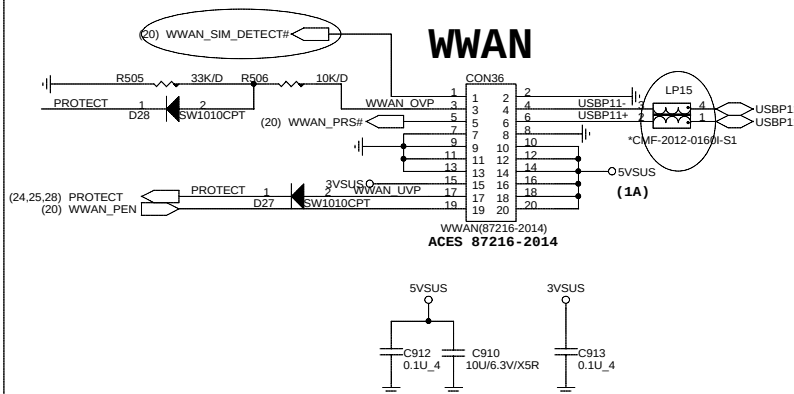
HDD CONNECTOR



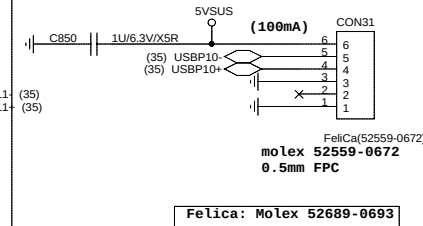
Bluetooth



WWAN



FeliCa



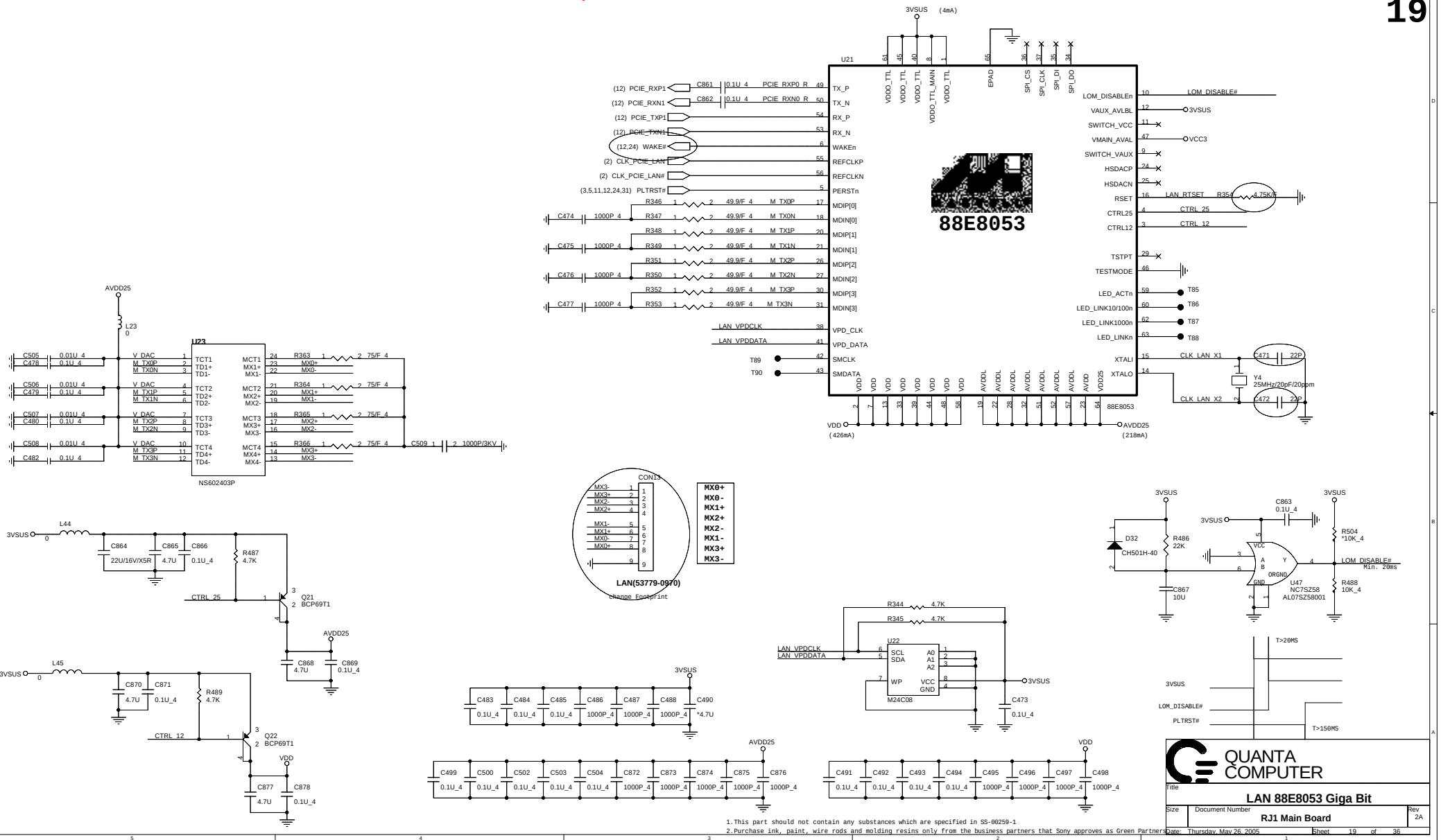
QUANTA COMPUTER

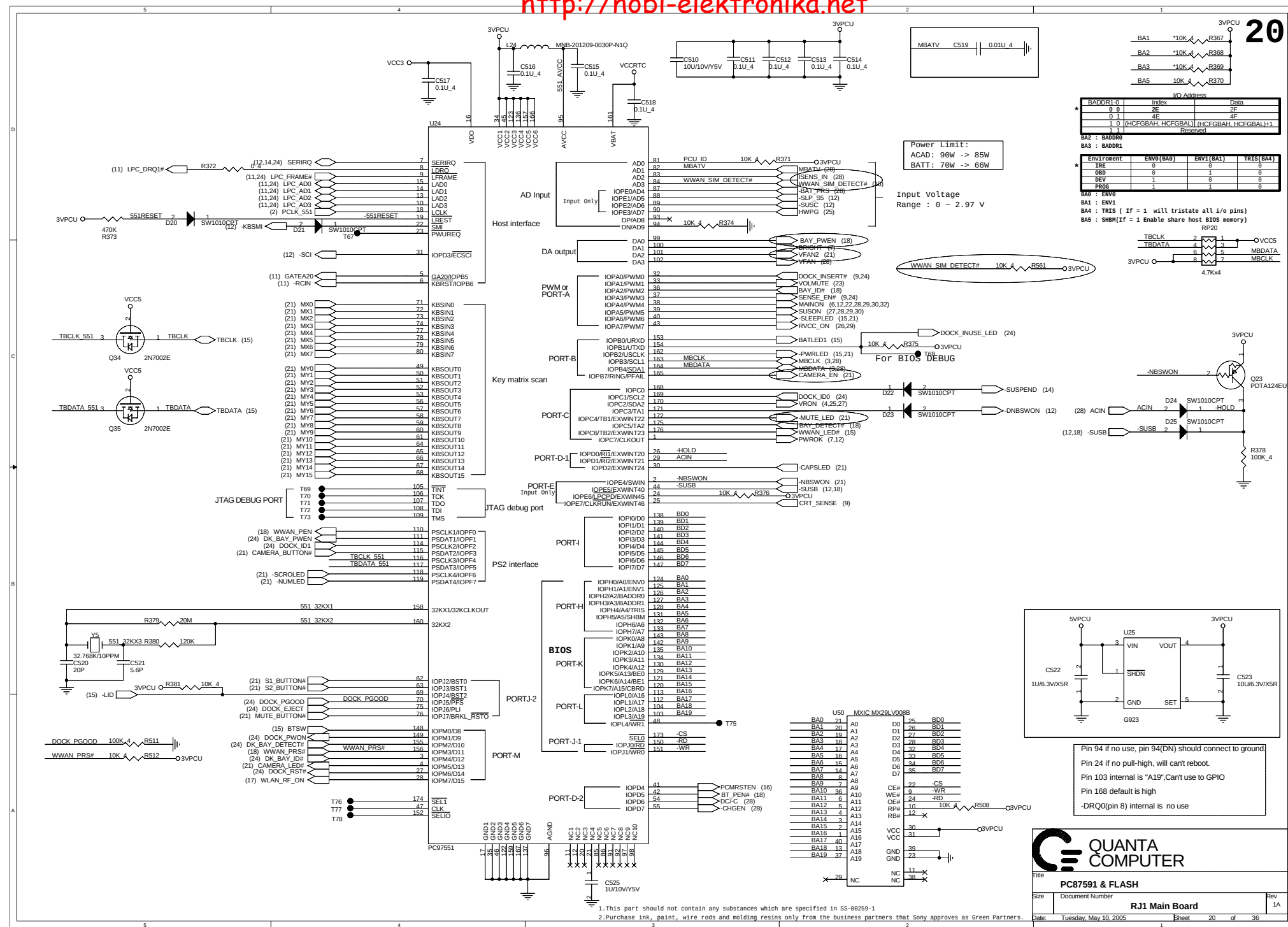
Title: **HDD/BAY/BT**

Size: **RJ1 Main Board**

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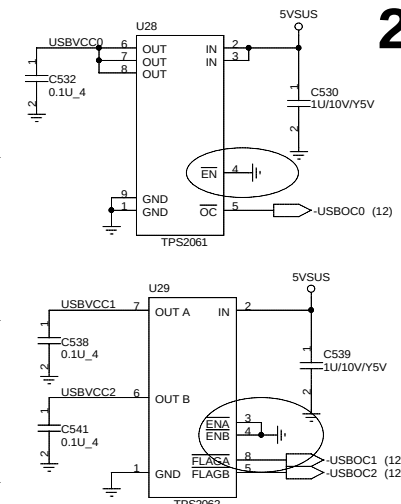
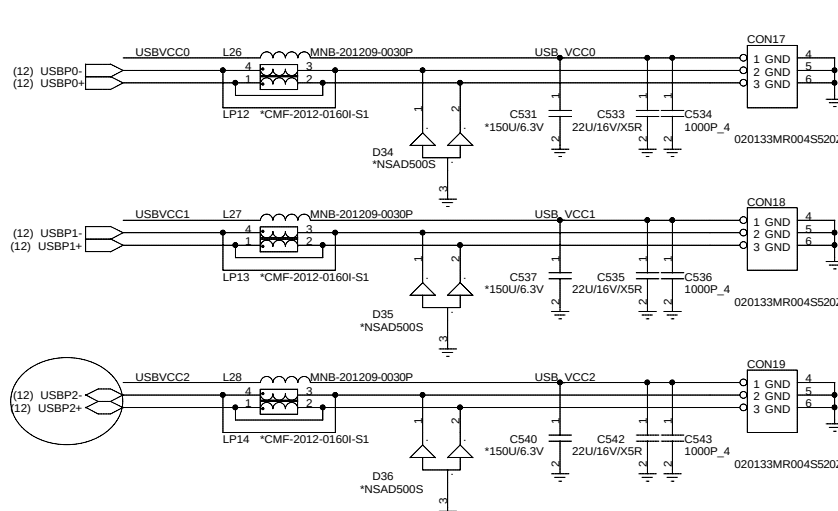
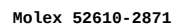
1. This part should not contain any substances which are specified in SS-90259-1.
2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.



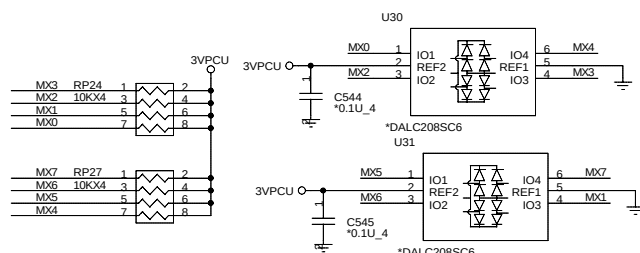


1. This part should not contain any substances which are specified in SS-06259-1

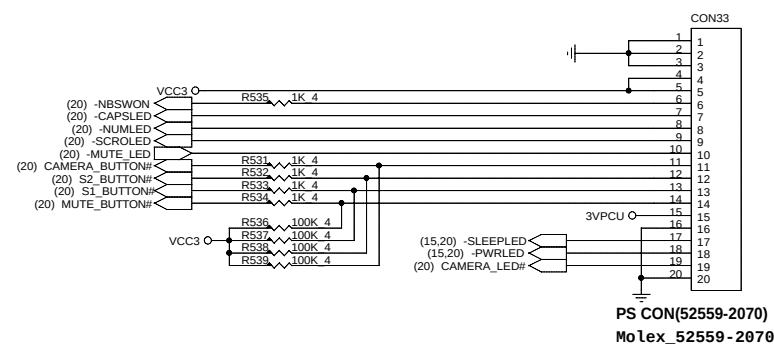
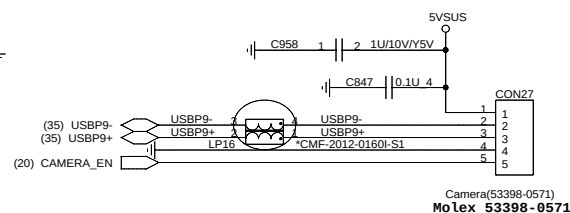
2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.



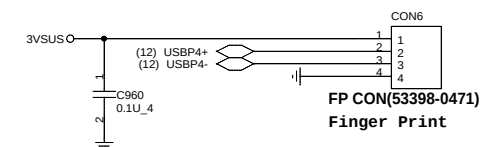
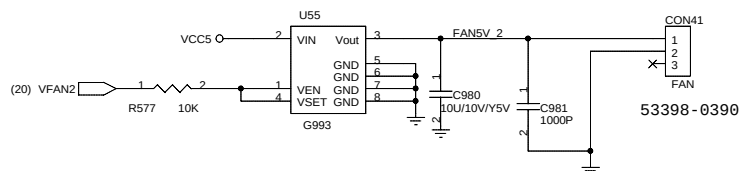
POWER SW BOARD



USB Camera

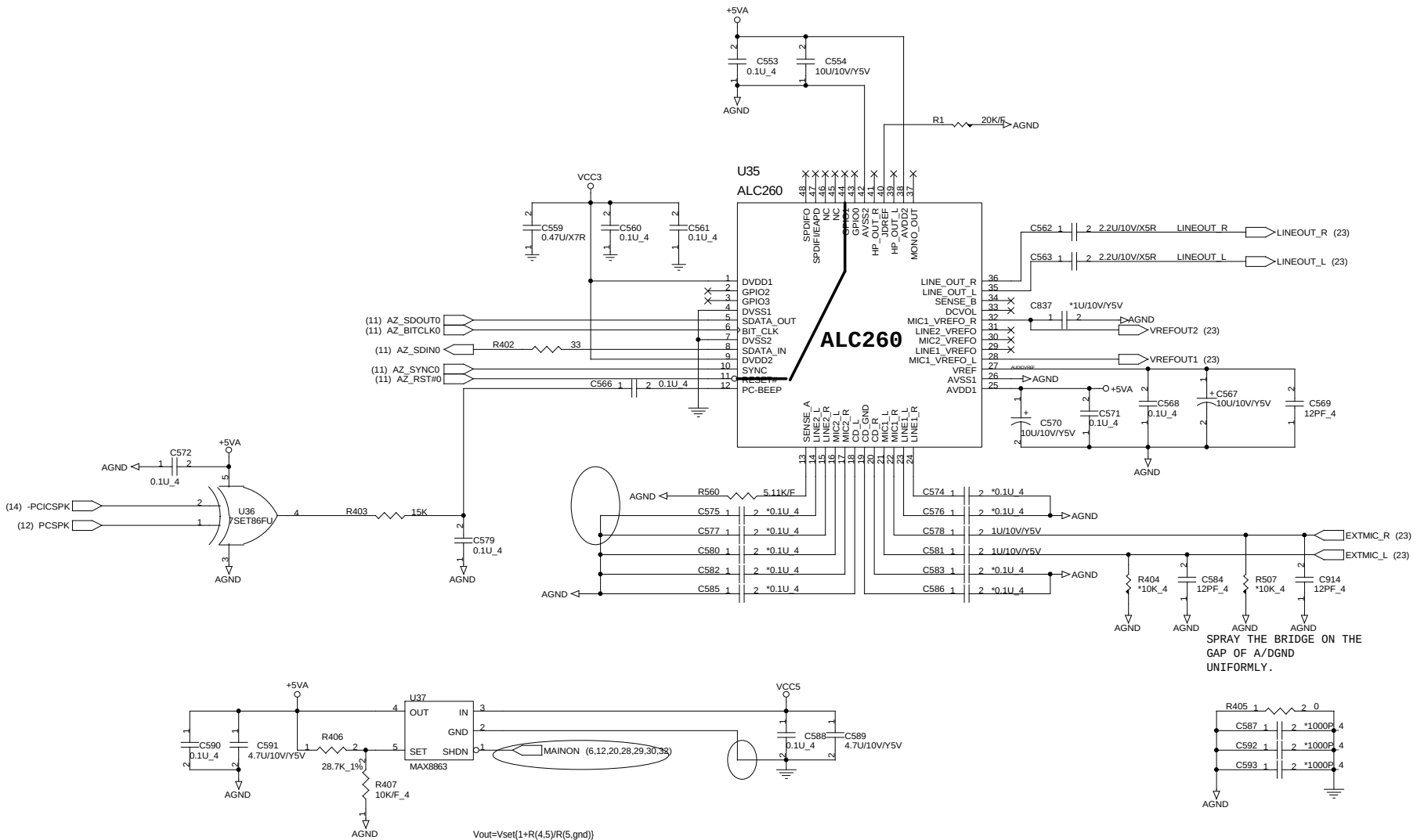


2nd FAN UNIT



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Title		K/B ,USB
Size	Document Number	
	RJ1 Main Board	



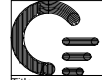
$$V_{out} = V_{set} \left(1 + \frac{R}{4.5} \right) \left(\frac{5}{R(5, gnd)} \right)$$

$$V_{set} = 1.25V$$

$$V_{out} = 1.25 \left(1 + \frac{29.4K(10K)}{10K} \right) = 4.925V$$

$$V_{out} = 1.25 \left(1 + \frac{28.7K(10K)}{10K} \right) = 4.8375V$$

$$V_{out} = 1.25 \left(1 + \frac{27K(10K)}{10K} \right) = 4.625V$$

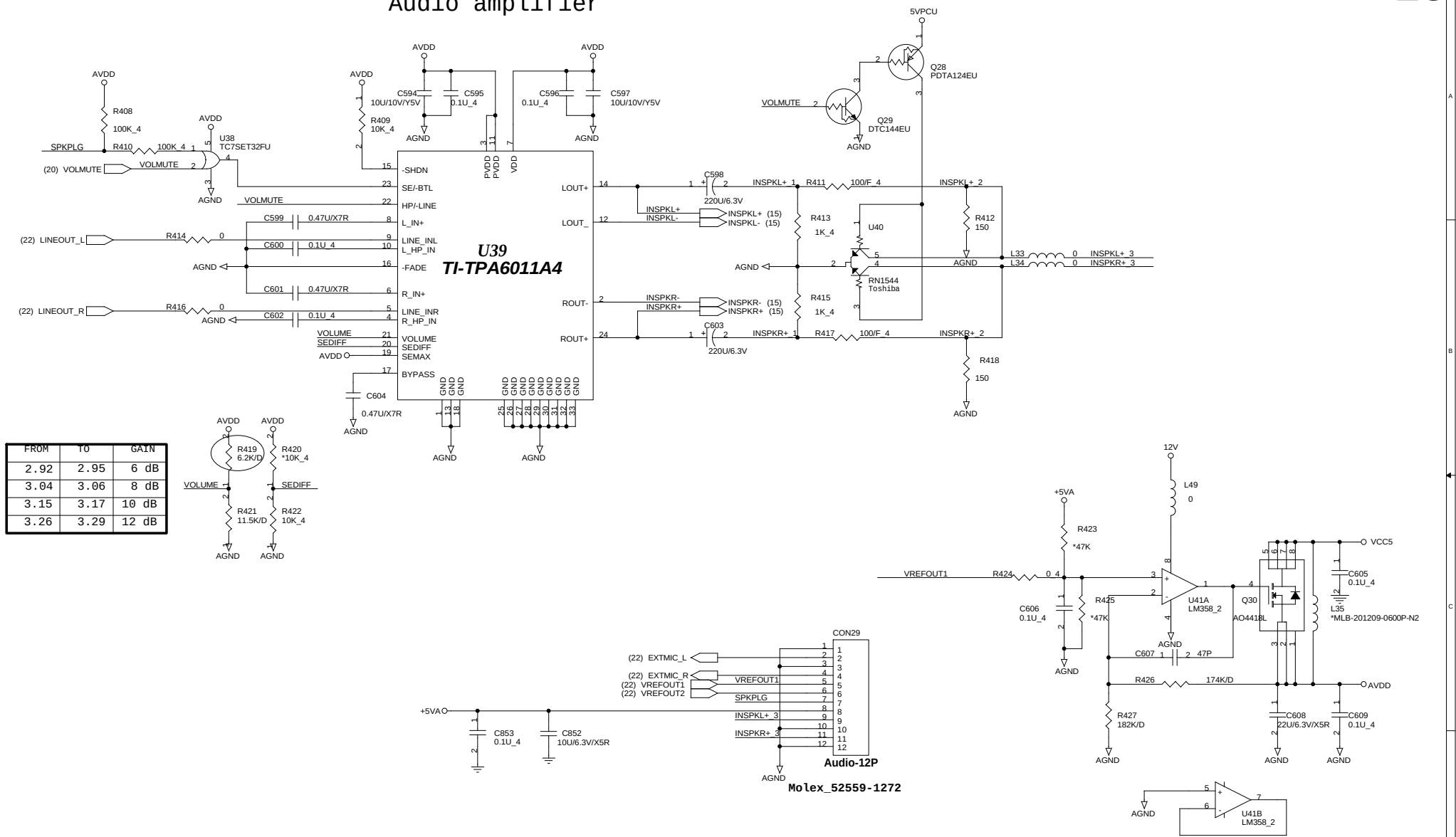


**QUANTA
COMPUTER**

Title Audio ALC260		
Size	Document Number	Rev 2A
RJ1 Audio Board		
Date: Thursday, May 26, 2005		
Sheet 22 of 36		

1. This part should not contain any substances which are specified in SS-00259-1
 2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

Audio amplifier





**QUANTA
COMPUTER**

Title
AUDIO AMP

Size
Document Number

Date: Thursday, May 26, 2005

Rev
1A

Sheet 23 of 36

1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

DOCKING Plug

DOCK_INSERT#
(DOCK -> PCU)

DOCK_PWON
(PCU -> DOCK)

-DNBSWON

DOCK_PG00D
(DOCK -> PCU)

DOCK_RST#
(PCU -> DOCK)

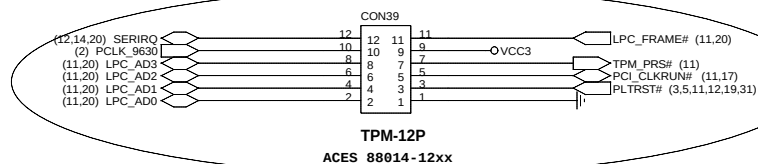
CLOCK Enable
(PCIE clock for LAN)

DOCKING Plug Out

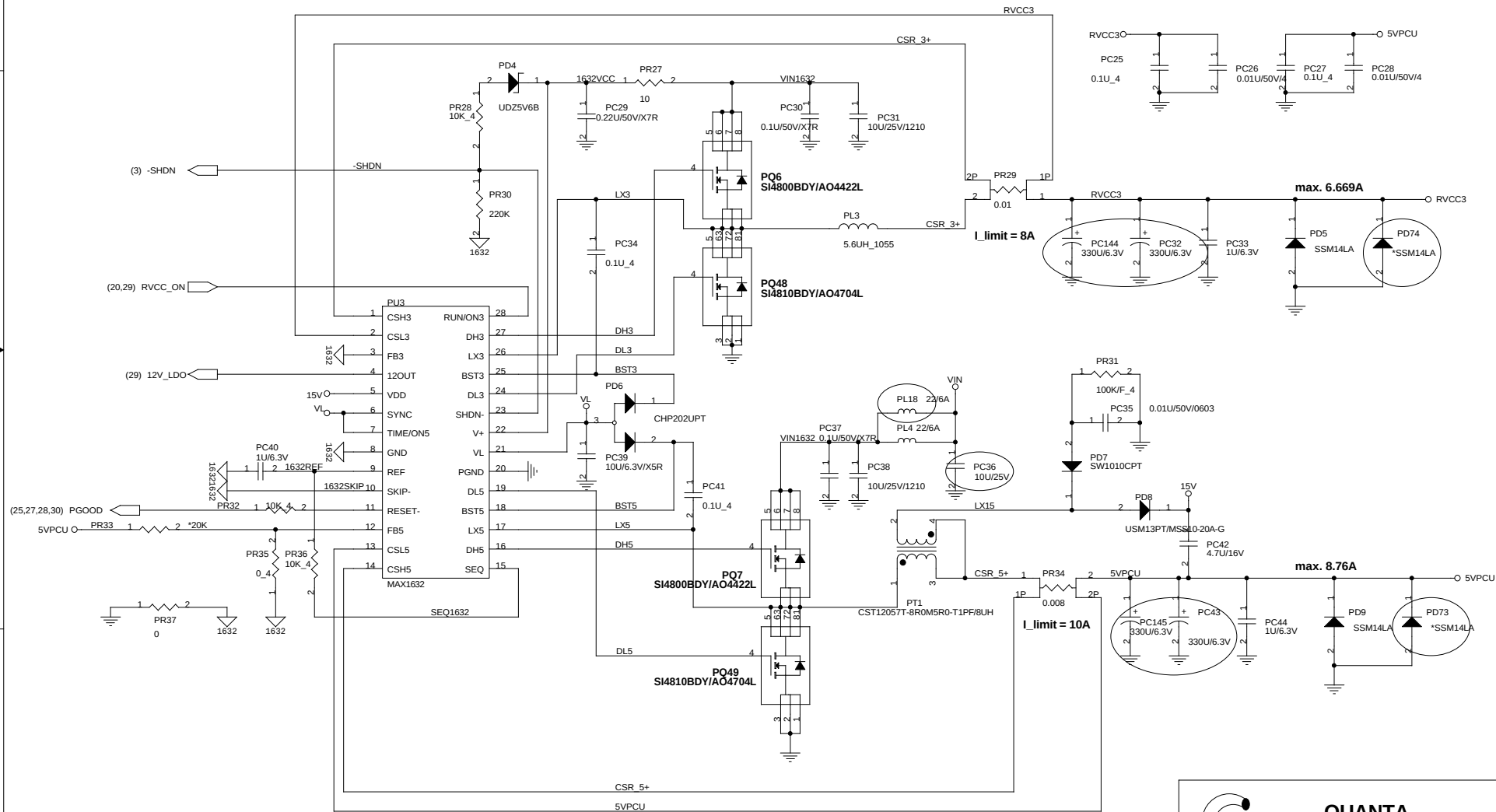
The diagram shows the timing relationships between several signals during PCIe initialization. The signals are:

- DOCK_BT_M** (DOCK -> PCU): Active high signal, starts high and transitions low.
- OS Close Device**: Active high signal, starts high and transitions low.
- CLOCK Disable** (PCIe clock for LAN): Active high signal, starts high and transitions low.
- DOCK_RST#** (PCU -> DOCK): Active low signal, starts high and transitions low.
- DOCK_PWON**: Active high signal, starts high and transitions low.

The signals are shown as horizontal lines with a step transition. The DOCK_RST# signal is the only one that transitions from high to low.



Title			
Docking/TPM			
Size	Document Number		Rev
	RJ1 Main Board		2
Date:	Tuesday, May 10, 2005	Sheet 24 of 36	



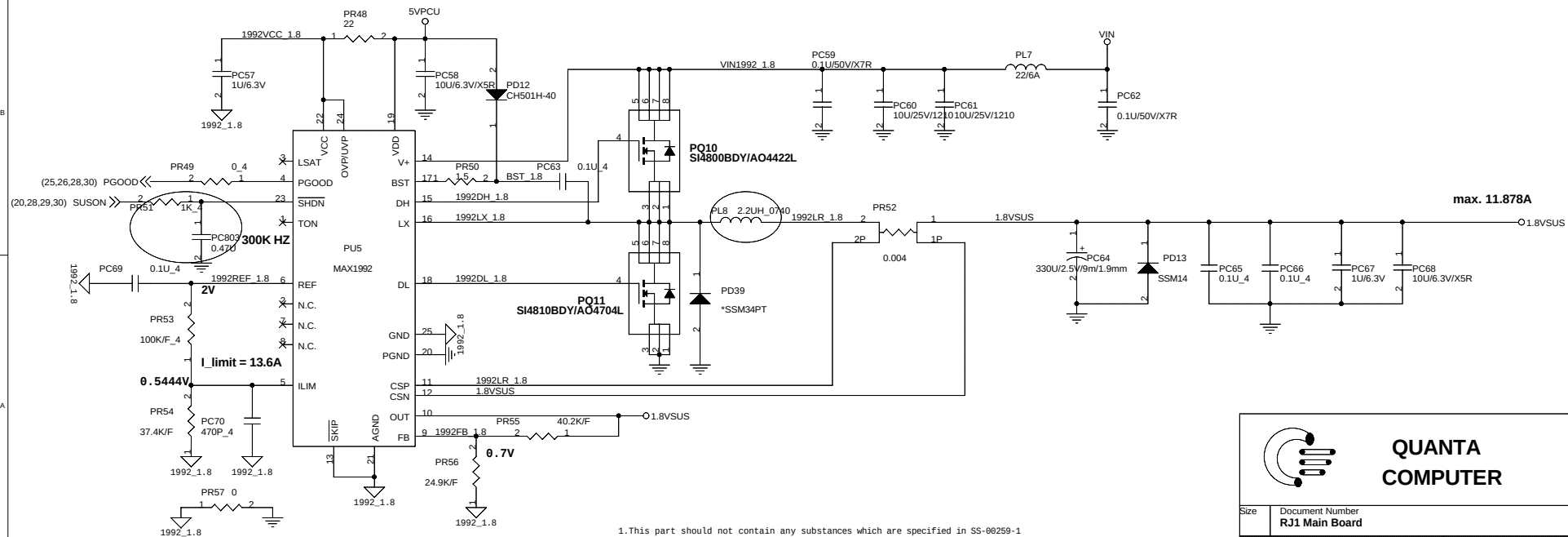
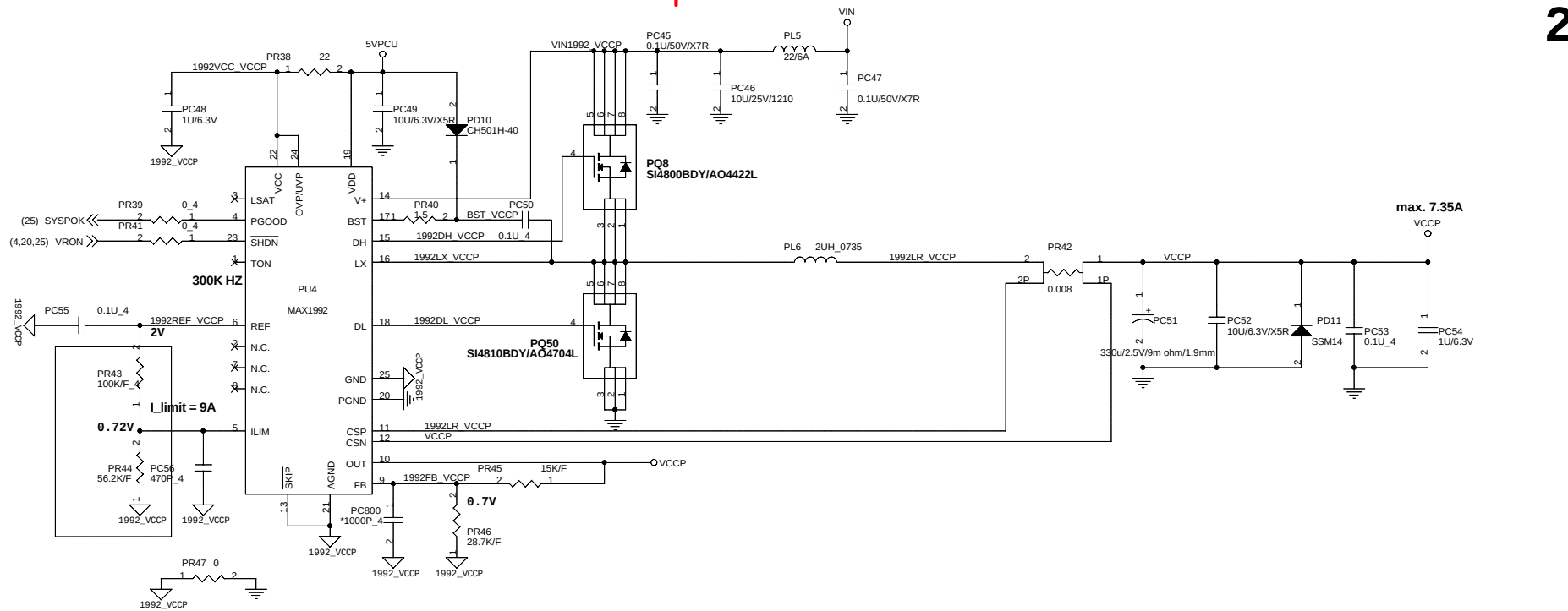


**QUANTA
COMPUTER**

Size	Document Number	RJ1 Main Board	Rev
		2A	

Date: Tuesday, May 10, 2005 Sheet 26 of 36

1.This part should not contain any substances which are specified in SS-90259-1
 2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.



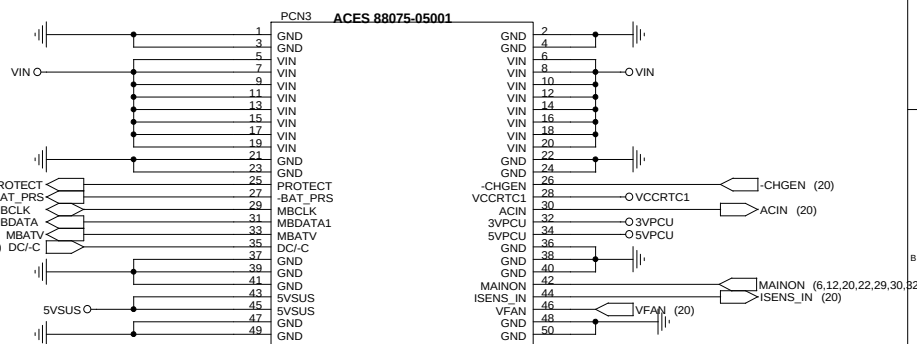
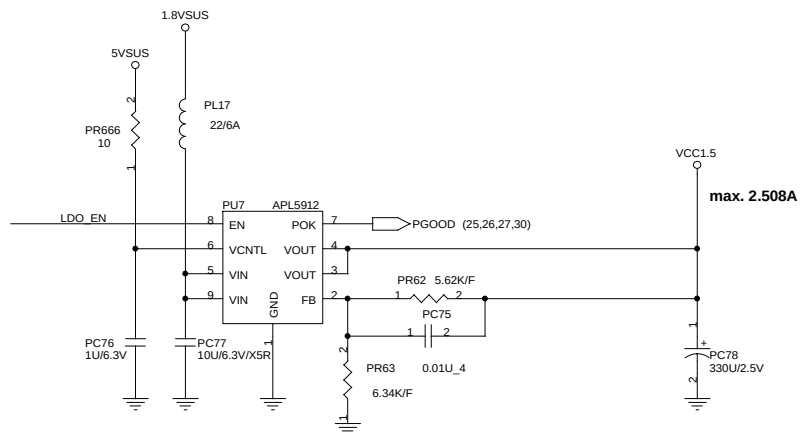
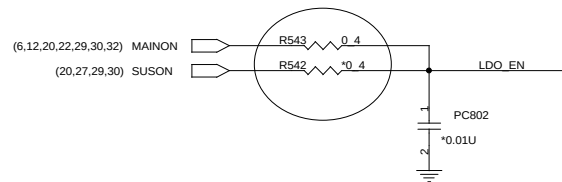
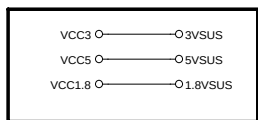
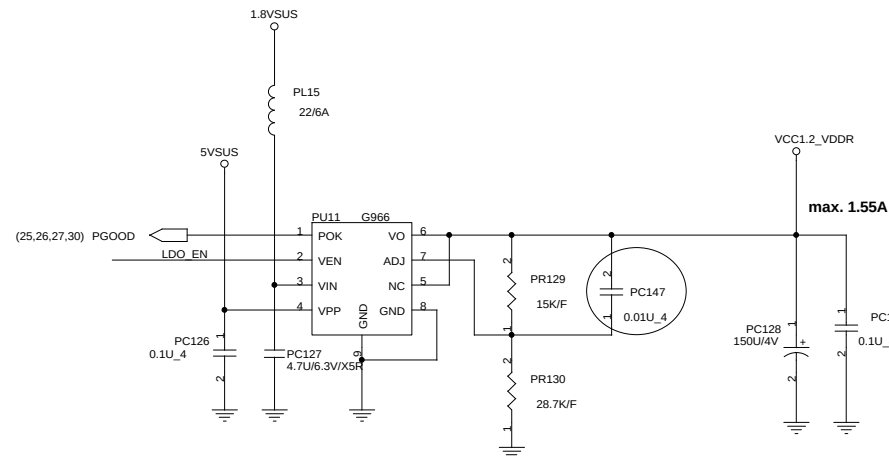
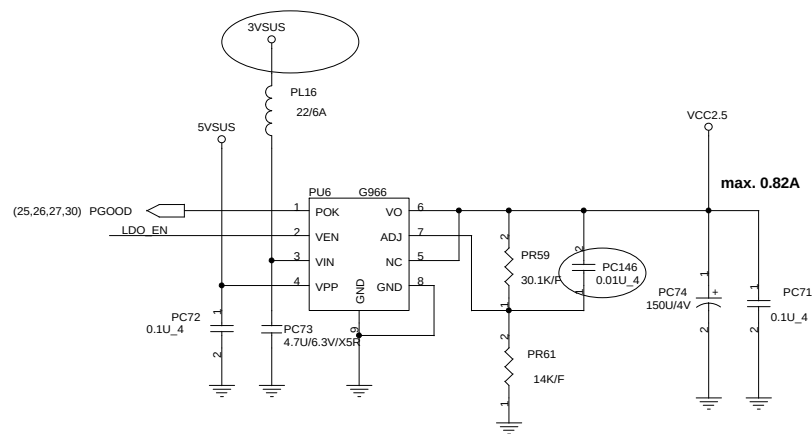


**QUANTA
COMPUTER**

Size	Document Number RJ1 Main Board	Rev 2A
Date: Tuesday, May 10, 2005 Sheet 27 of 36		

1. This part should not contain any substances which are specified in SS-00259-1

2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.





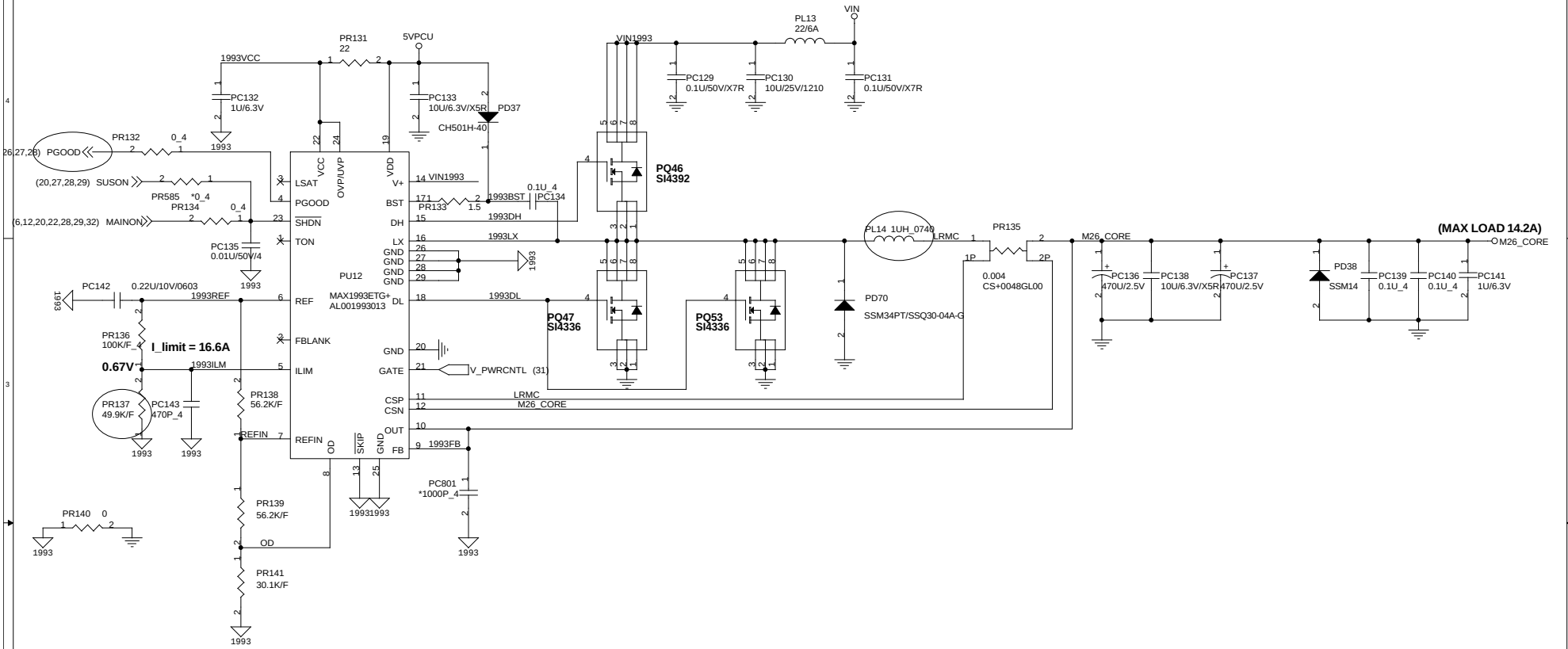
**QUANTA
COMPUTER**

Size	Document Number	Rev
	RJ1 Main Board	2A
Date: Tuesday, May 10, 2005		
Sheet 28 of 36		

1.This part should not contain any substances which are specified in SS-00259-1

2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.





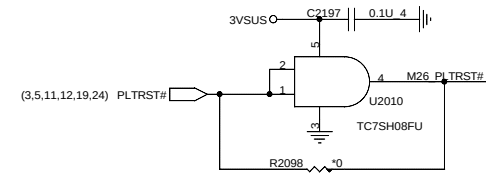
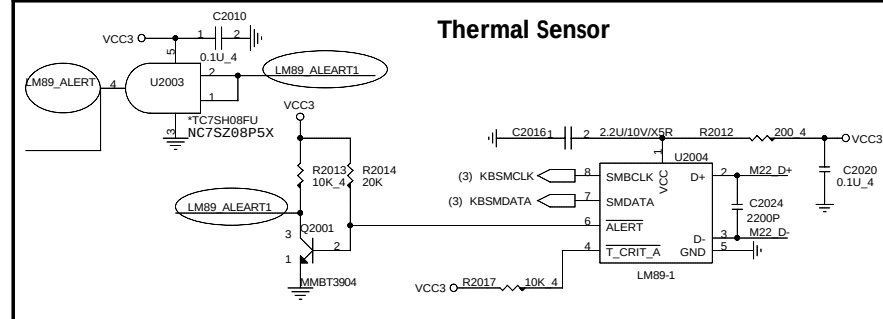
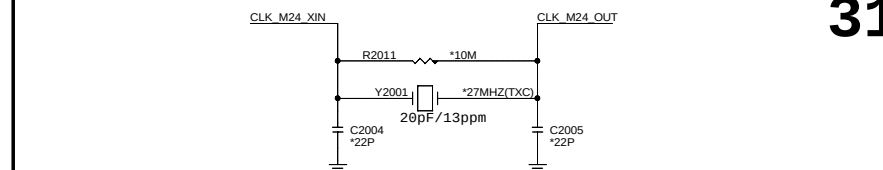
M24_CORE voltage setting:

	PR138 Value	PR139 Value	PR141 Value	V_PWRCNTL	
				Low	High
M24	49.9 K/F	49.9 K/F	27.4 K/F	1.215V	1V
	56.2 K/F	56.2 K/F	30.1 K/F	1.211V	1V



QUANTA
COMPUTER

1. This part should not contain any substances which are specified in SS-00259-1.
2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

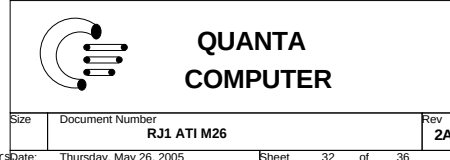


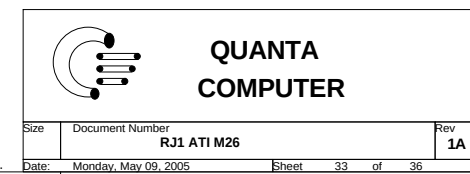
PCI_TEST	ATI Internal USE 0: Default
GPIO_0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing
GPIO_1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled
GPIO_(3,2)	00: PCI Express 1.0 mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)
GPIO_4	0: NON REVERSED LANES IN LAYOUT 1: REVERSED LANES IN LAYOUT
GPIO_5	DO NOT FORCE COMPLIANCE STATE QUICKLY
GPIO_6	COMMON MODE RANGE 0: Default
GPIO_8	DEBUG SIGNALS NOT BROUGHT OUT
GPIO(9,13,11) ROMIDCFG INT P/D	NO USE-0000 (ID[1:4] = GPIO[11,12,13,9]) 0x0x: No ROM, CHG_ID=0 0x1x: No ROM, CHG_ID=1 1011 - Serial M25P10 ROM (ST), chip ID is from ROM 1100 - Serial M25P05 ROM (ST), chip ID is from ROM



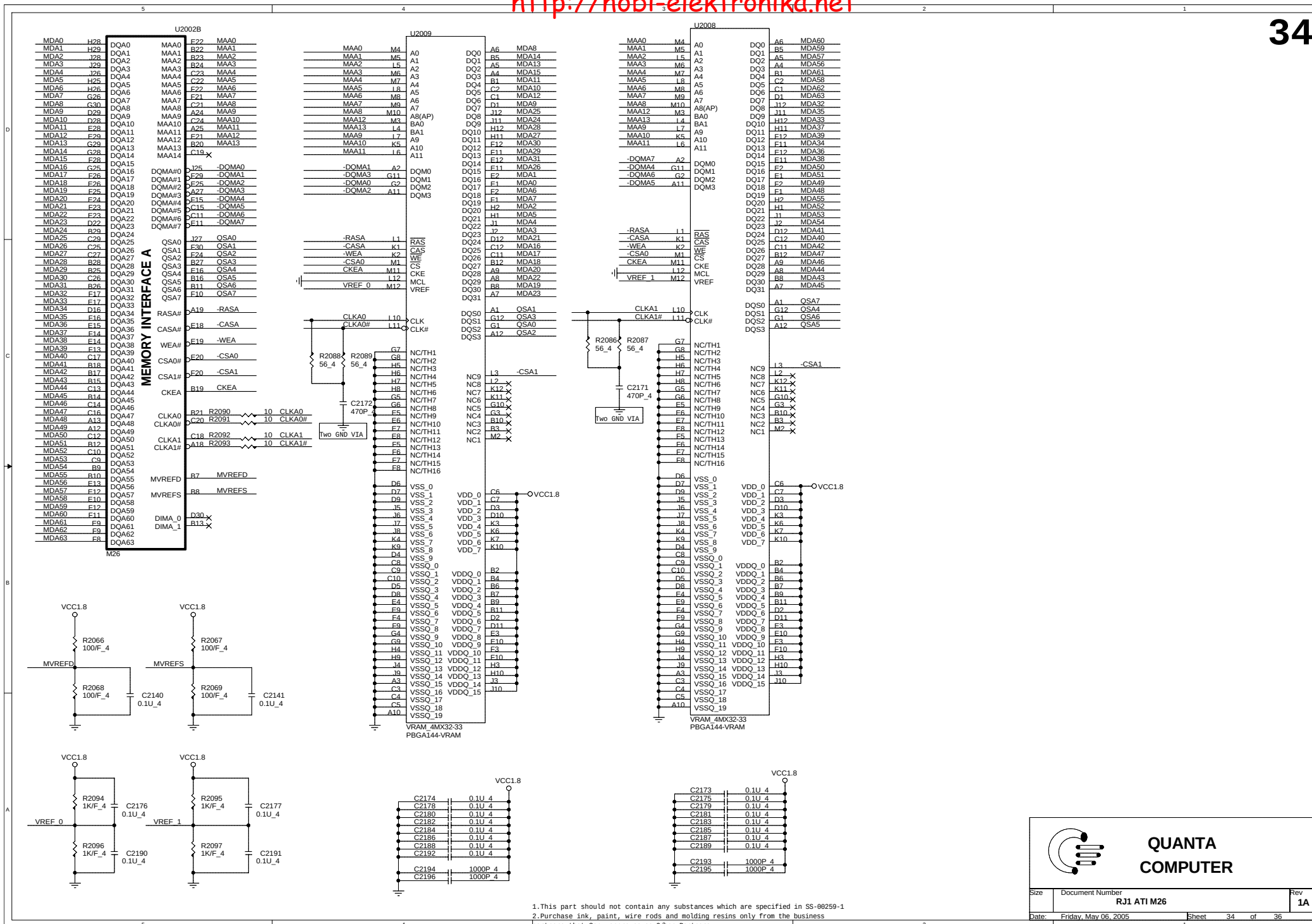
QUANTA
COMPUTER

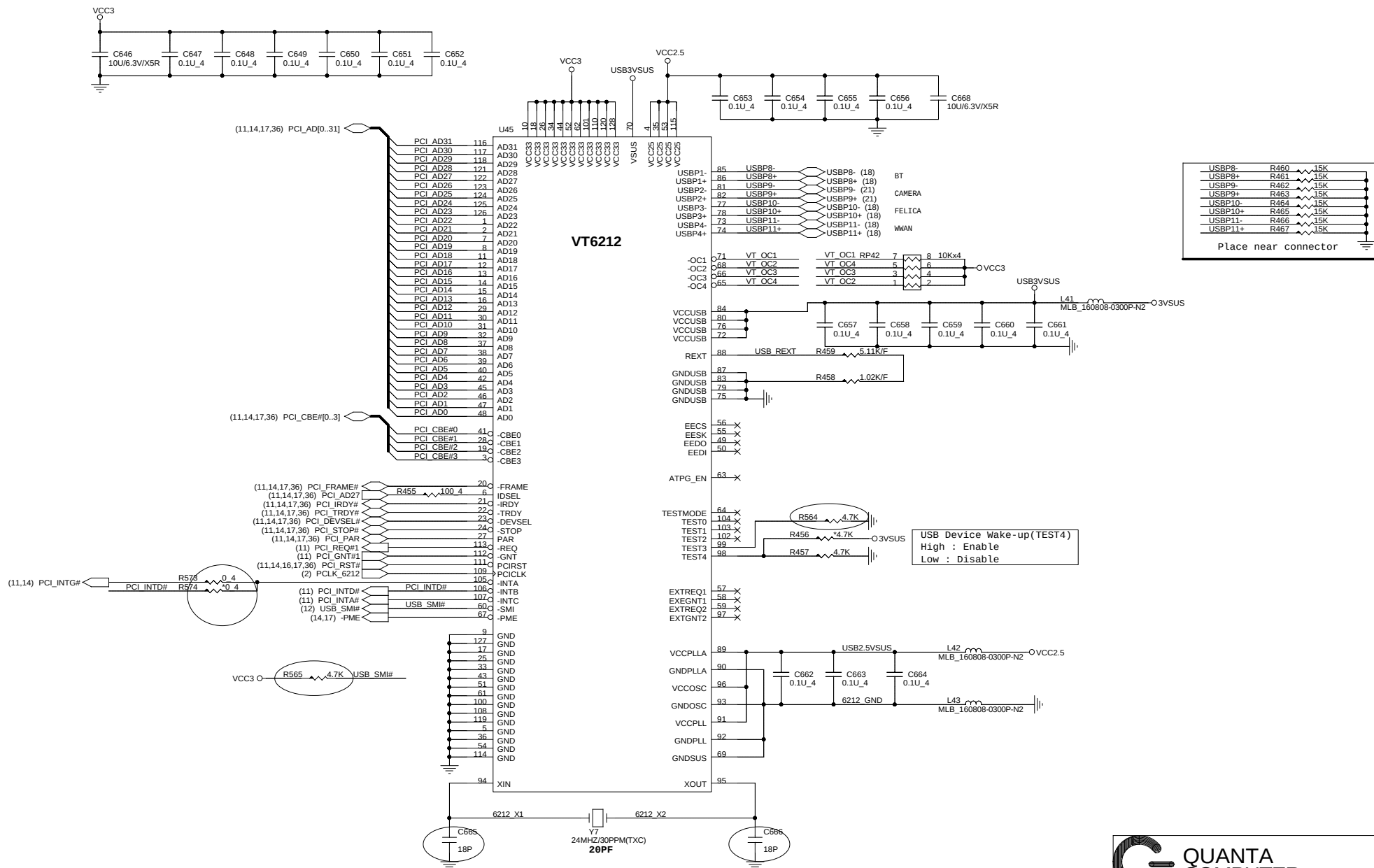
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2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners





1.This part should not contain any substances which are specified in SS-00259-1

2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

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