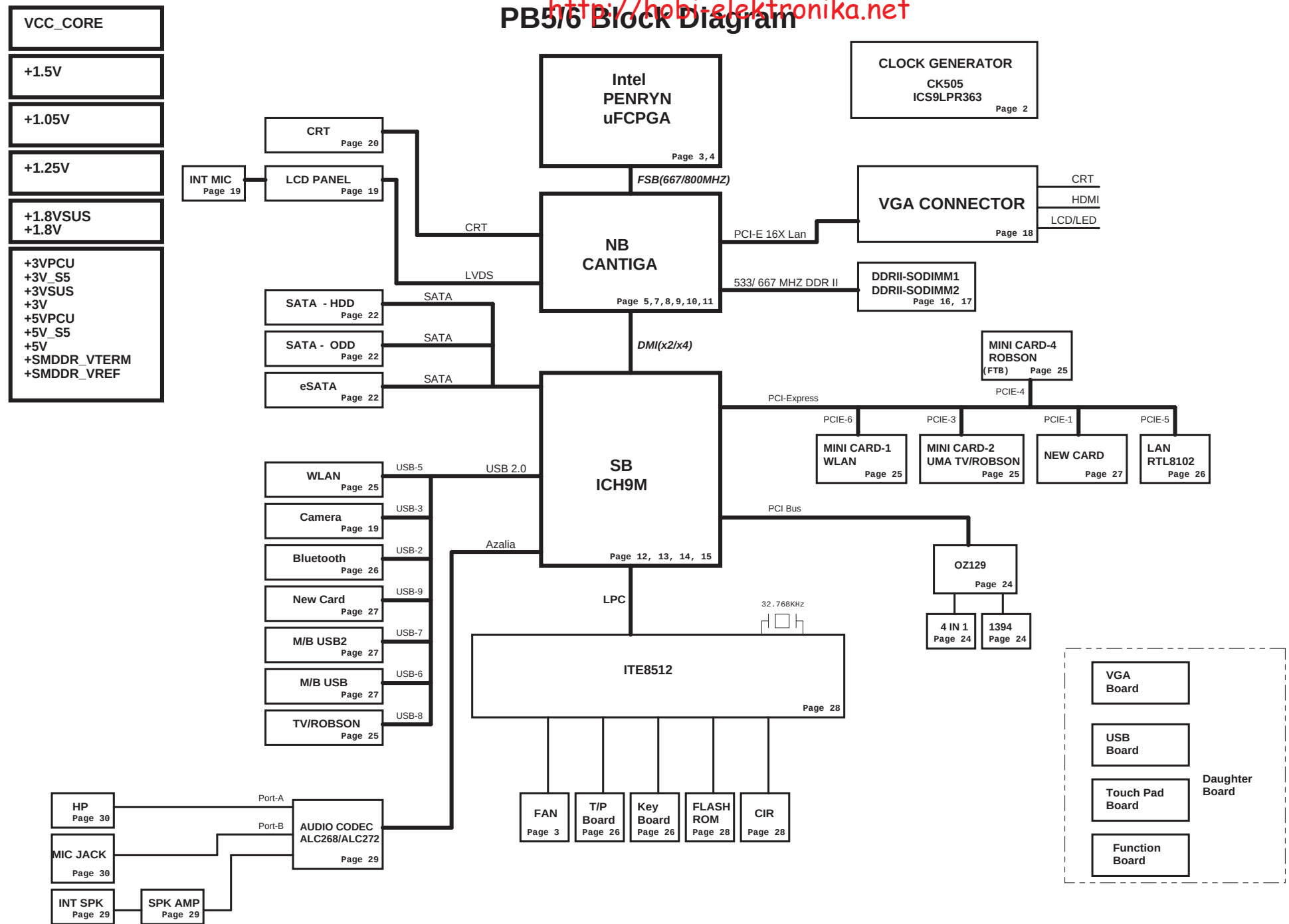
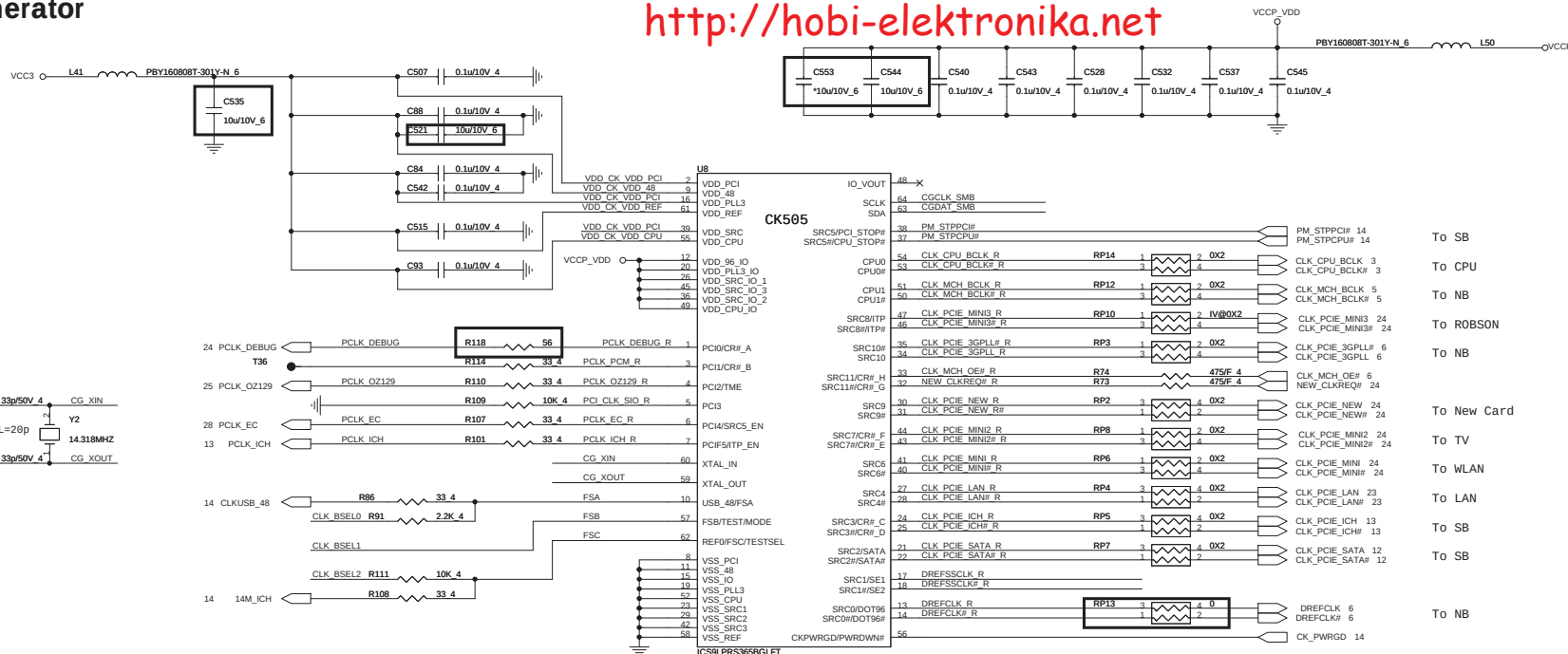


PB5/6 Block Diagram



<http://hobi-elektronika.net>



PM STPPCI# R76 2.2K 4

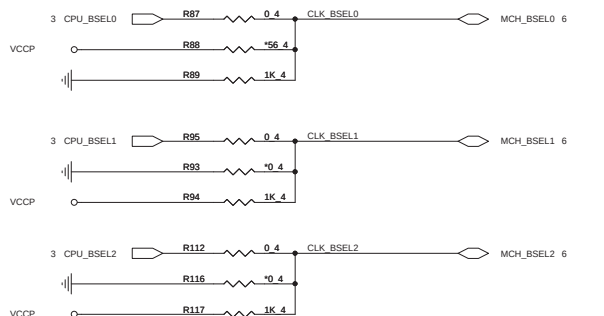
PM STPCPU# R75 2.2K 4

NEW CLKREO# R R560 10K 4

	KCSLP3S6505 (ALP3S365K13)	PIW761-606 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PC12/7ME	PC12/7ME Internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN Internal PD	PI3N7/38 IS SRC5	PI3N7/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL Internal PD	PI6 17/18 IS 27MHz	PI6 17/18 IS SRC/00T (default)
Pin 7	PCIF-5/1TP_EN	PCIF-5/1TP_EN Internal PD	PI6 46/47 IS CPU1PT	PI6 46/47 IS SRCB (default)

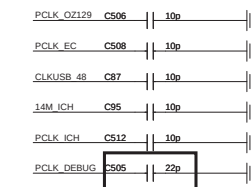
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

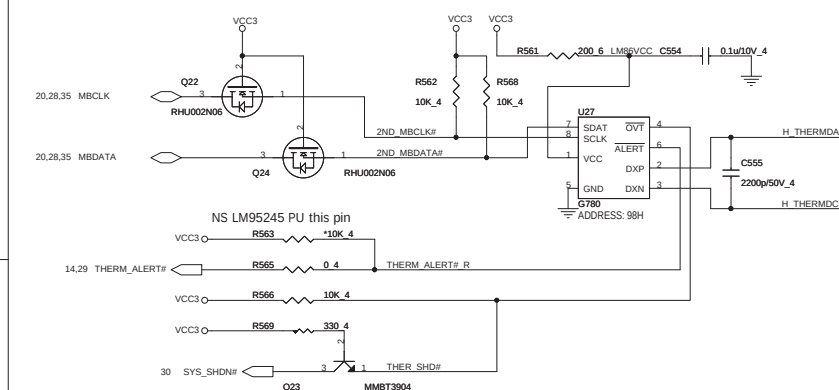
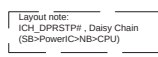


Black Gen I2C

The diagram illustrates the Black Gen I2C interface. It features two I2C transceivers, Q7 and Q8, connected to VCC3 and GND. Q7's input is connected to the SDATA signal (pin 14_24) and its output to CGDAT_SMB (pin 17). Q8's input is connected to the SCLK signal (pin 14_24) and its output to CGCLK_SMB (pin 17). Both transceivers have a 10K_4 pull-up resistor connected to VCC3.



		PROJECT : PB5/6 Quanta Computer Inc.	
Size	Document Number	Rev	
	CLK GEN		1A
Partno:	Erldns: Mnu 90 50008	Edwnt:	5 of 58



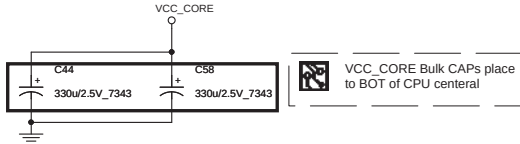
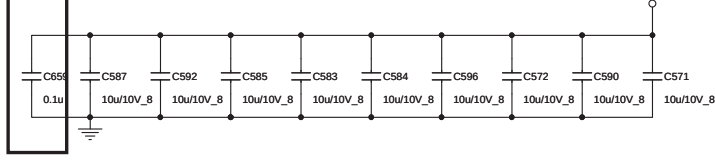
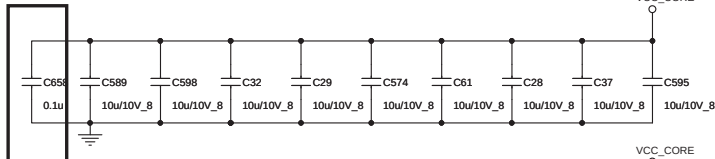
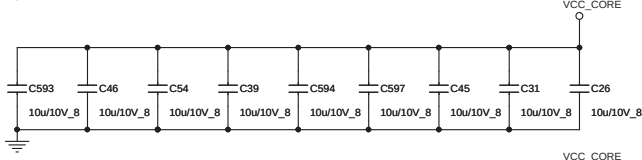
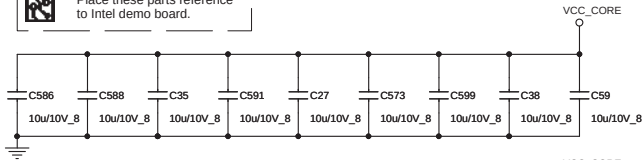
BOM Option Table

Reference	Description
N/A	N/A

Need NC 20PCS 10u before A1 BOM released(A0 all stuff)



Place these parts reference to Intel demo board.



Penryn CPU Power Status and max current table

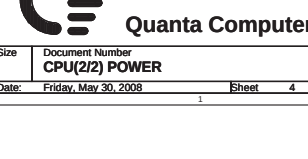
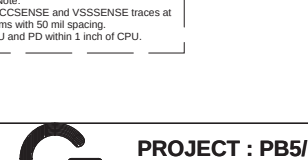
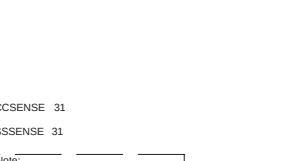
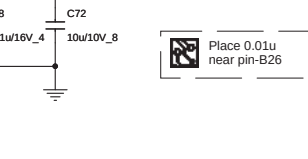
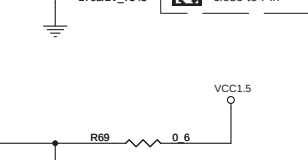
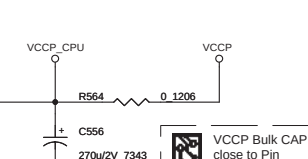
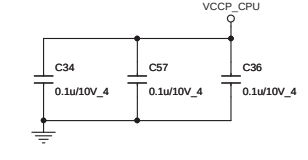
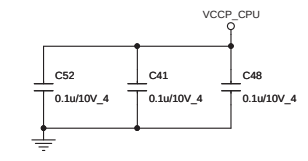
POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	47A	Standard Voltage CPU
VCC_CORE	O	X	X	VID	50A	SV Design Target
VCC_CORE	O	X	X	VID	TBD	Extreme Edition CPU
VCC_CORE	O	X	X	VID	67A	EE Design Target
VCCA	O	X	X	+1.5V	130mA	
VCCP	O	X	X	+1.05V	4.5A	Before VCC Stable
VCCP	O	X	X	+1.05V	2.5A	After VCC Stable

(See Penryn EMTS Rev:1.0 Table 7,8 for voltage and current)

(See Penryn EMTS Rev:1.0 Table-3 for VID table)



Layout Note:
Inside CPU center cavity in 2 rows

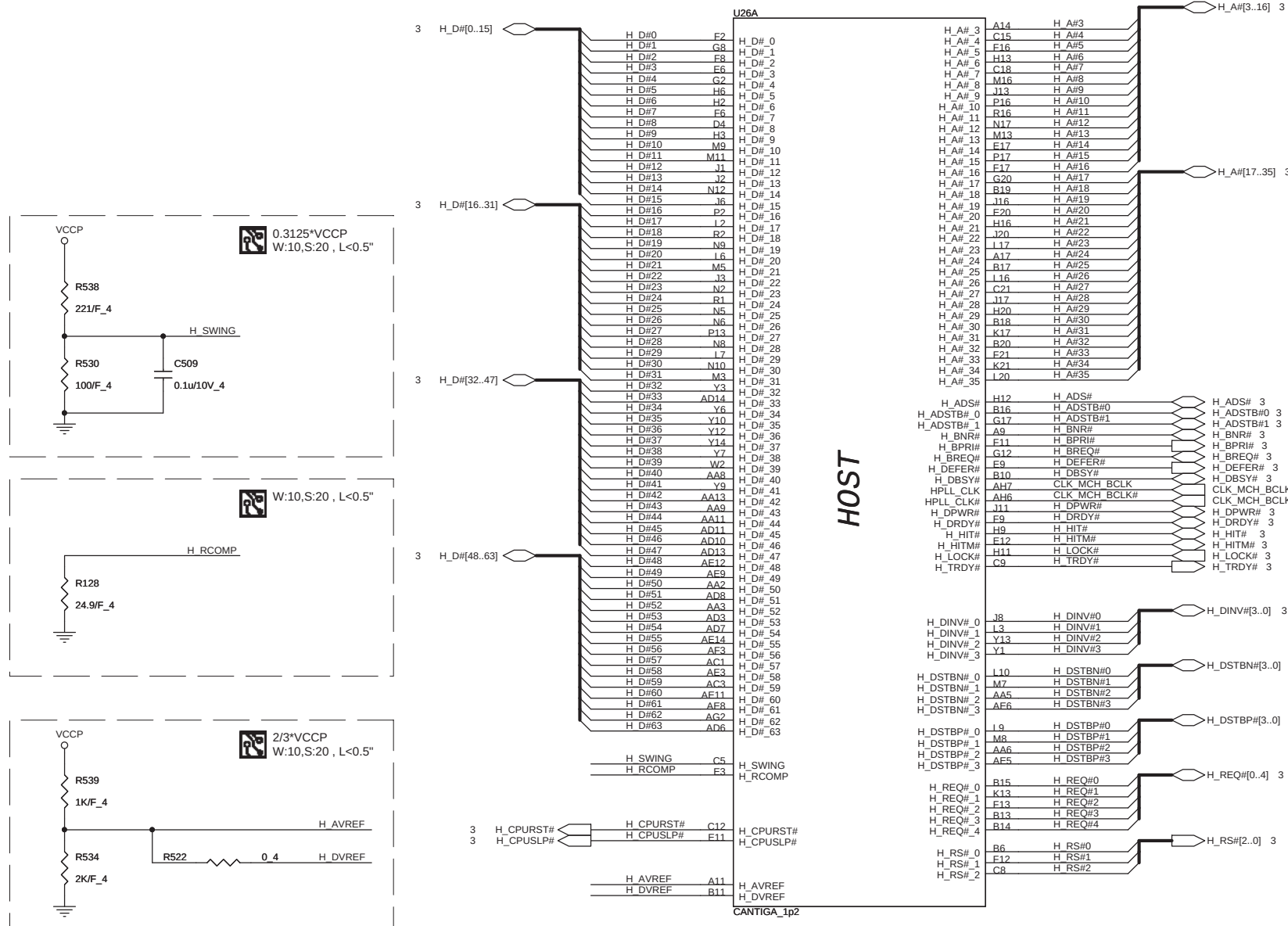


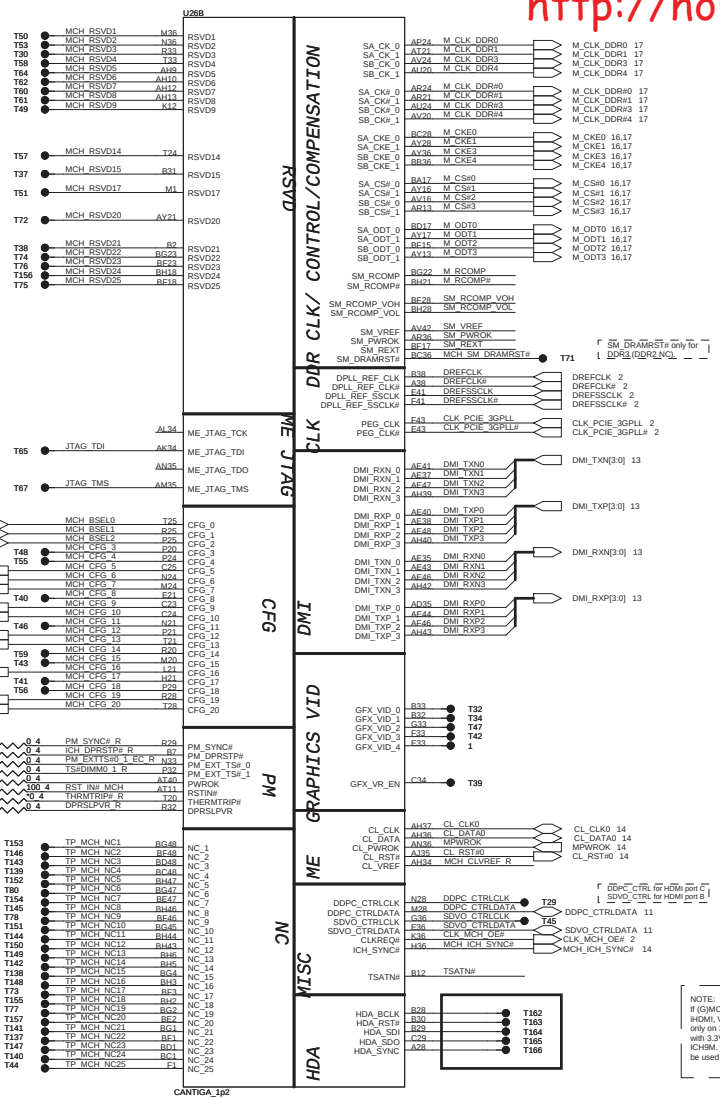
PROJECT : PB5/6
Quanta Computer Inc.

Size	Document Number	Rev
	CPU(2/2) POWER	1A
Date:	Friday, May 30, 2008	
Sheet	4	of 35

BOM Option Table

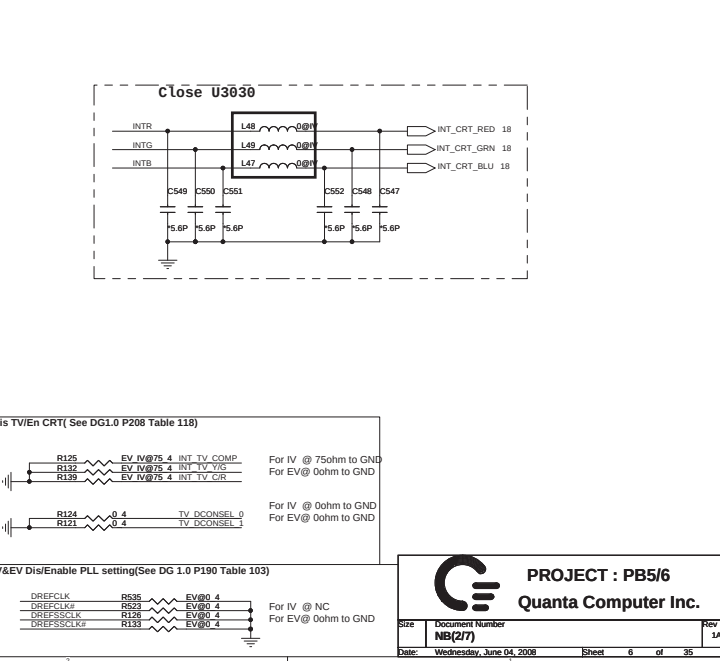
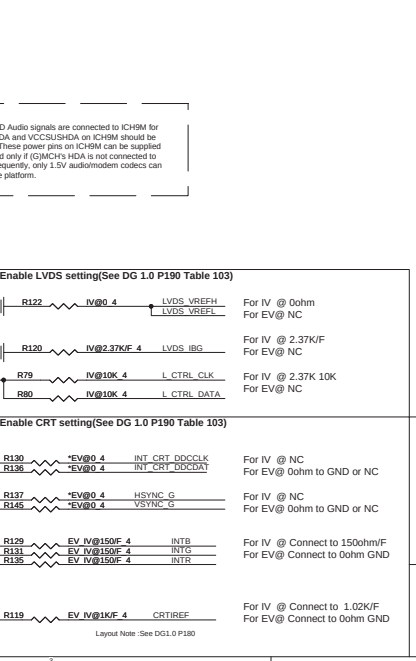
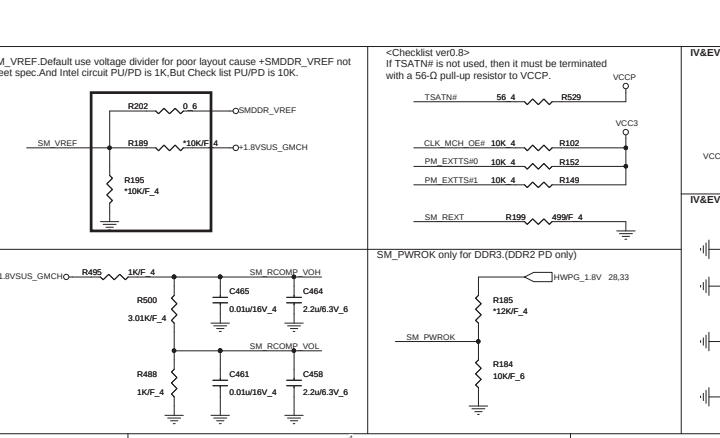
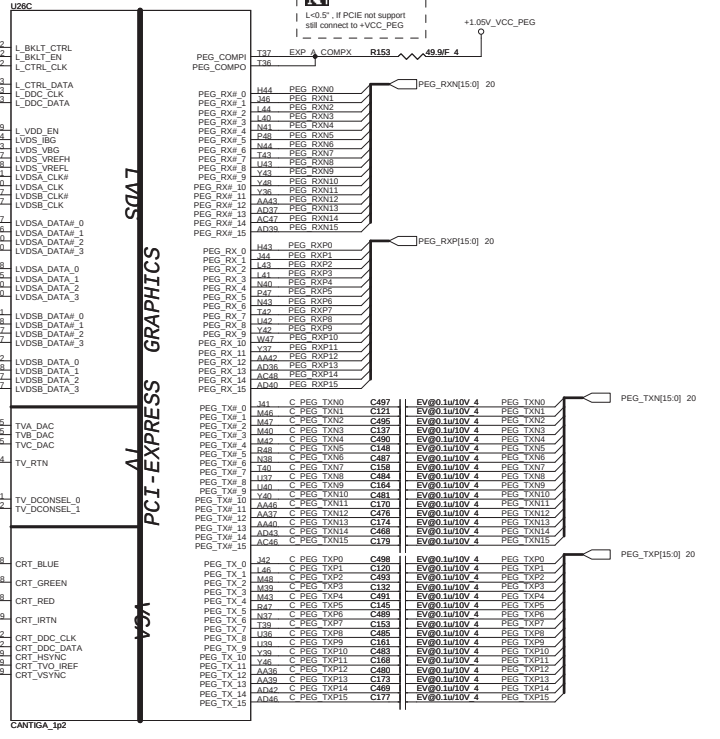
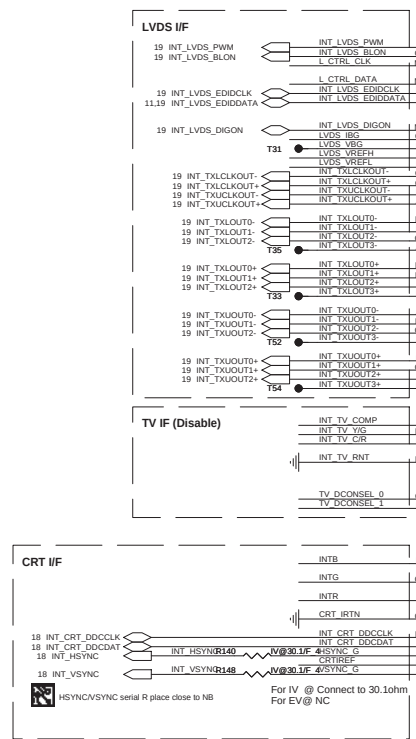
Reference	Description
N/A	N/A



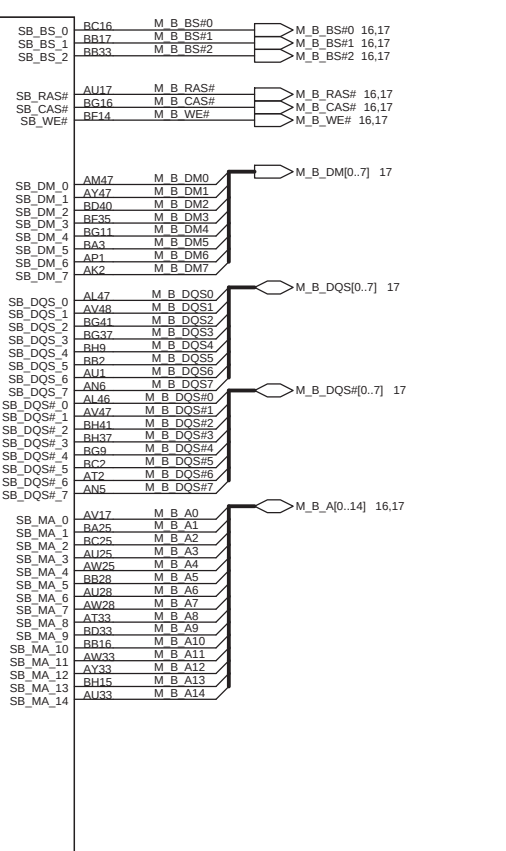
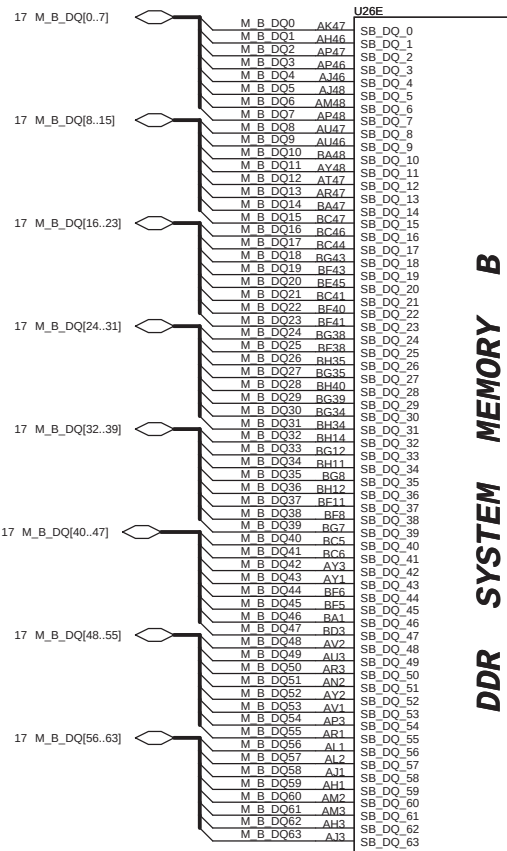
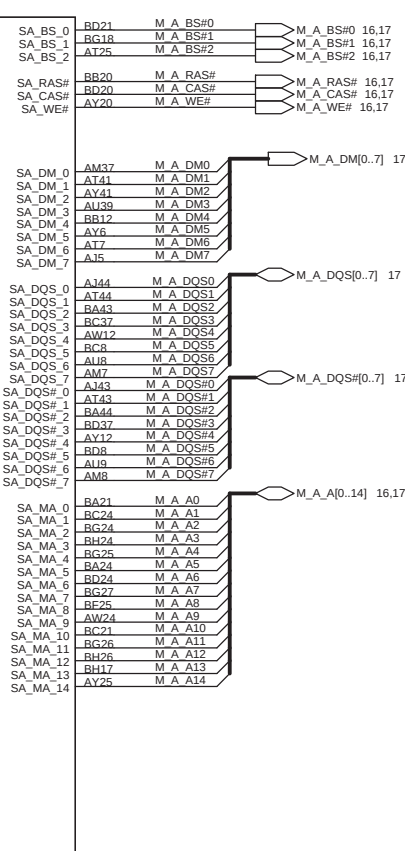
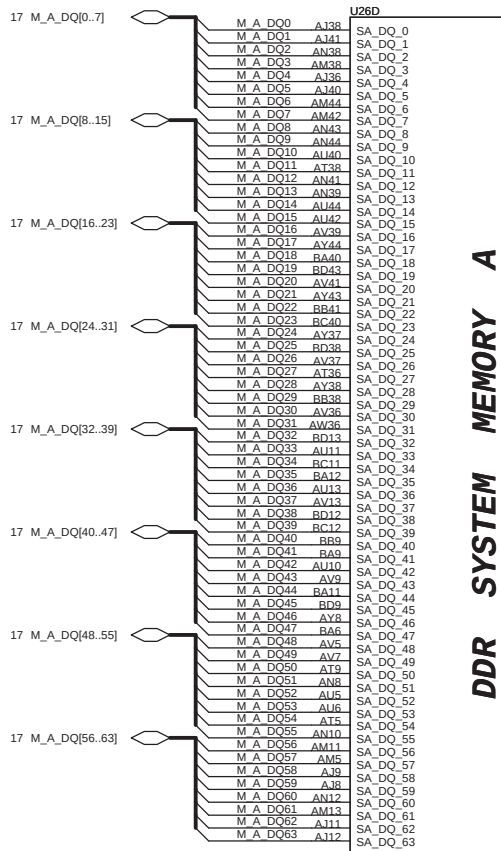


BQM Option Table

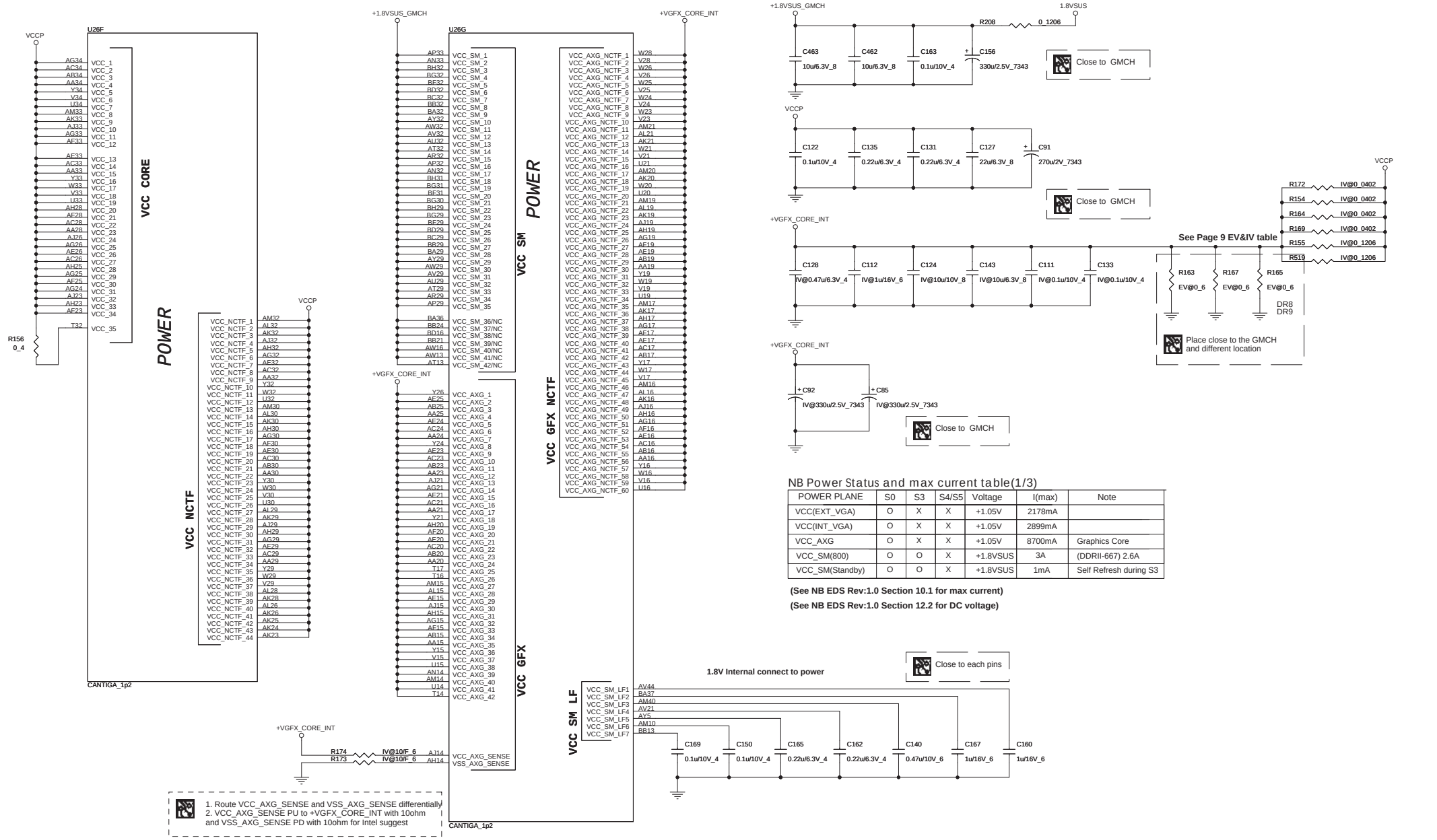
Symbol	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. value



Reference	Description
N/A	N/A



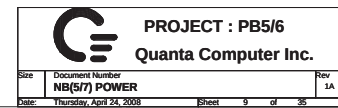
Reference	Description
IV@	INT VGA
EV@	EXT VGA



NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AGX	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)





Reference	Description
N/A	N/A

U24	MCH VSS 351	R160	0 4
U28	MCH VSS 352	R159	0 4
U25	MCH VSS 353	R151	0 4
U29	MCH VSS 354	R157	0 4
A16	MCH VSS 355	R178	0 4

VSS_NCTF_1	AF32
VSS_NCTF_2	AB32
VSS_NCTF_3	V32
VSS_NCTF_4	A130
VSS_NCTF_5	AM29
VSS_NCTF_6	AE29
VSS_NCTF_7	AB29
VSS_NCTF_8	U26
VSS_NCTF_9	U23
VSS_NCTF_10	AI.20
VSS_NCTF_11	V20
VSS_NCTF_12	AC19
VSS_NCTF_13	AI.17
VSS_NCTF_14	AI.17
VSS_NCTF_15	AA17
VSS_NCTF_16	UI7

VSS SCB

VSS_SCB_1	BH18
VSS_SCB_2	BH1
VSS_SCB_3	A48
VSS_SCB_4	C1
VSS_SCB_6	A3

NC	NC_26	D1	X
	NC_27	F2	X
	NC_28	C3	X
	NC_29	B4	X
	NC_30	A5	X
	NC_31	AB	X
	NC_32	AD3	X
	NC_33	B4	X
	NC_34	AD5	X
	NC_35	C46	X
	NC_36	D47	X
	NC_37	F47	X
	NC_38	AD6	X
	NC_39	E48	X
	NC_40	C48	X
	NC_41	B48	X
	NC_42	AD7	X
	NC_43		



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Quanta Computer Inc.

Size	Document Number NB(6/7) VSS	Rev 1A
Date:	Friday, March 21, 2008	Sheet 10 of 35

North Bridge Strap Pin Configuration Table

(See DG 1.0 P295 Table 184)
(See NB EDS 1.0 P187 Table 74)

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	6 MCH_CFG_5 	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	6 MCH_CFG_6 	Enable iTPM
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	6 MCH_CFG_7 	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	6 MCH_CFG_9 	
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)	6 MCH_CFG_10 	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	6 MCH_CFG_12 	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	6 MCH_CFG_13 	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	6 MCH_CFG_16 	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	6 MCH_CFG_19 	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	6 MCH_CFG_20 	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	6 SDVO_CTRLDATA 	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	6,19 INT_LVDS_EDIDDATA 	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	6 DDPC_CTRLDATA 	

BOM Option Table

Reference	Description
N/A	N/A

Enable iTPM Table

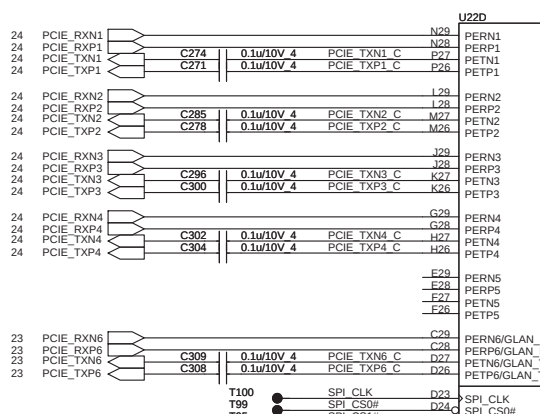
PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin



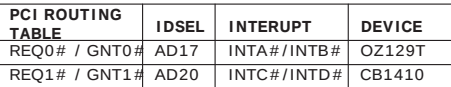
PROJECT : PB5/6
Quanta Computer Inc.

Size	Document Number NB(7/7) STRAP	Rev 1A
Date:	Friday, May 30, 2008	Sheet 11 of 35

25 AD[0..31] _____



PCI-Express



The diagrams show the connection of three resistors (RP48, RP47, RP46) to the PCI bus. Each resistor is an 8.2K_10P8R type. The connections are as follows:

- RP48:**
 - Pin 6: FRAME#
 - Pin 7: IRDY#
 - Pin 8: LOCK#
 - Pin 9: REQ2#
 - Pin 10: VCC3
 - Pin 5: VCC3
 - Pin 4: INTB# R
 - Pin 3: STOP#
 - Pin 2: REQ1#
 - Pin 1: DEVSEL#
- RP47:**
 - Pin 6: INTN#
 - Pin 7: REQ0#
 - Pin 8: X
 - Pin 9: X
 - Pin 10: VCC3
 - Pin 5: VCC3
 - Pin 4: INTG#
 - Pin 3: REQ3#
 - Pin 2: PERR#
 - Pin 1: INTD# R
- RP46:**
 - Pin 6: INTC# R
 - Pin 7: X
 - Pin 8: INTF#
 - Pin 9: X
 - Pin 10: VCC3
 - Pin 5: VCC3
 - Pin 4: INTA# R
 - Pin 3: SERR#
 - Pin 2: INT#
 - Pin 1: TRDY#

USB# PULL-UP

RP45

USB0C#7 6
 USB0C#1 7
 USB0C#0 8
 USB0C#3 9
 3VVSUS 10

5
 4
 3
 2
 1

G3VVSUS

10K_10P8R

RP38

USB0C#9 8
 USB0C#8 7
 USB0C#11 6
 USB0C#10 5
 2

7
 5
 3
 1

G3VVSUS

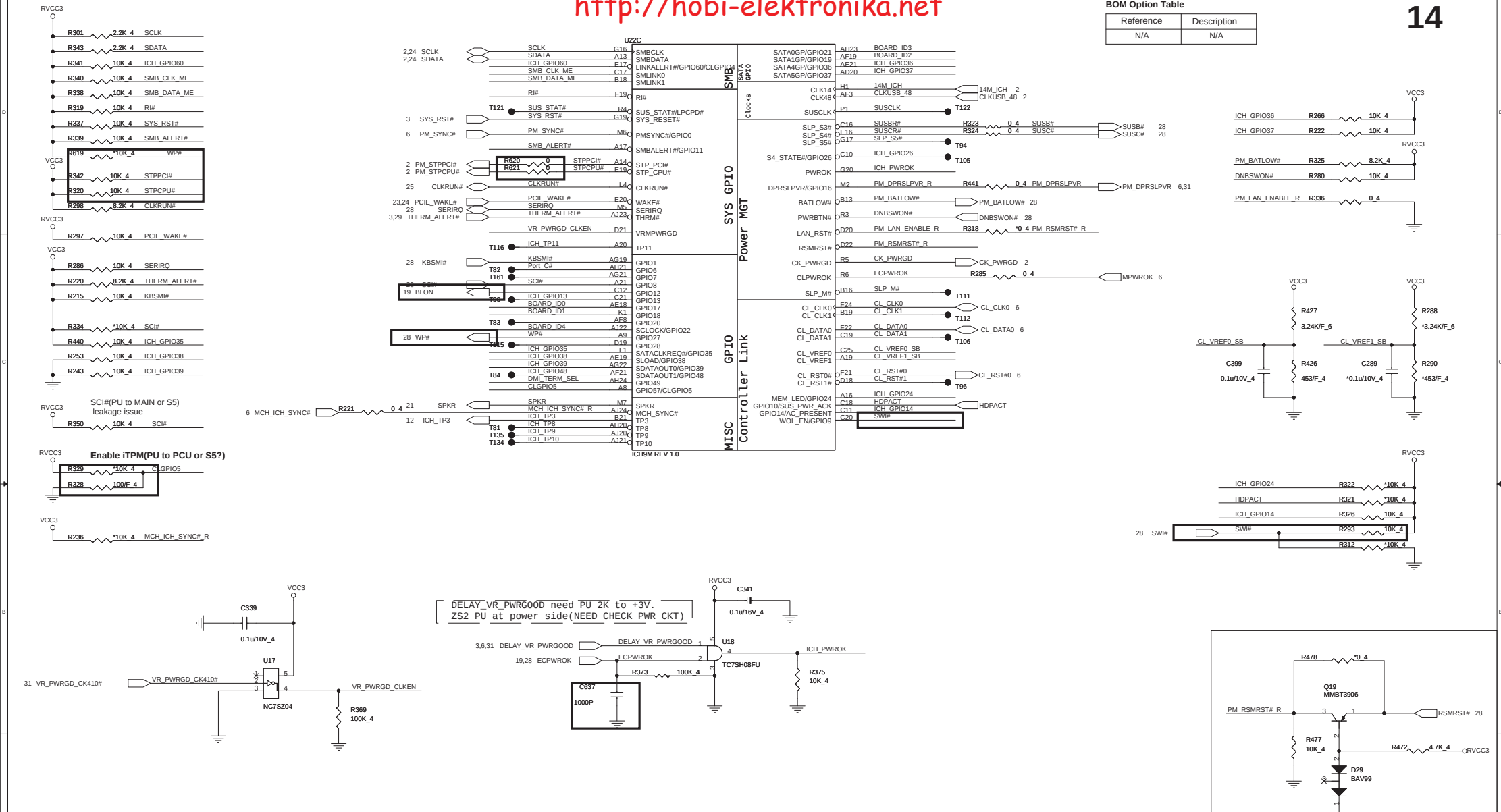
10K_8P4R

PROJECT : PB5/6

Quanta Computer Inc.

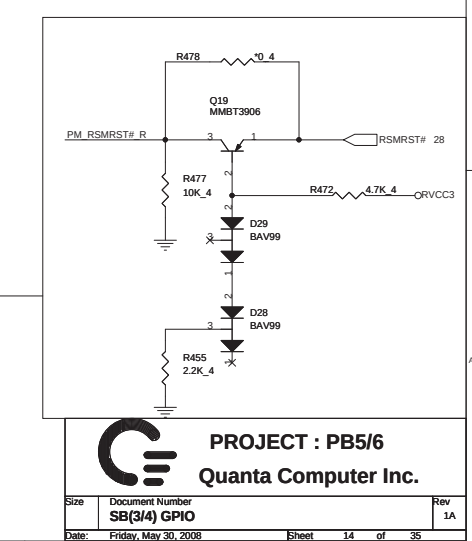
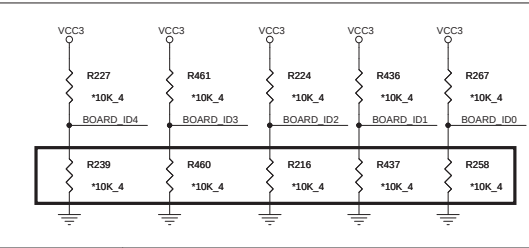
Size	Document Number	Rev
	SB (2/4) PCIE/PCI/USB	1A
Date:	Friday, May 30, 2008	Sheet 13 of 35

Reference	Description
N/A	N/A

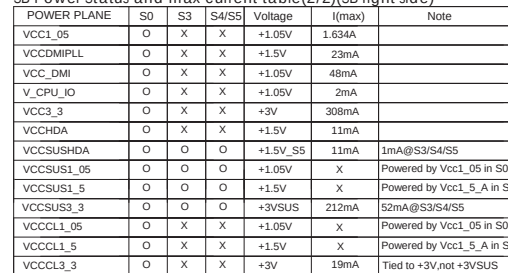


South Bridge Strap Pin (3/3)				
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R291 1K 4 VCC3
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R241 1K 4

Board ID Table					
BOARD_ID3 of TE1M always keep low, TE1 hasn't support TV					
Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	H L
W/ G-SENSOR W/O G-SENSOR			H L		
W/ TV W/O TV		H L			
W/ HDMI W/O HDMI	H L				

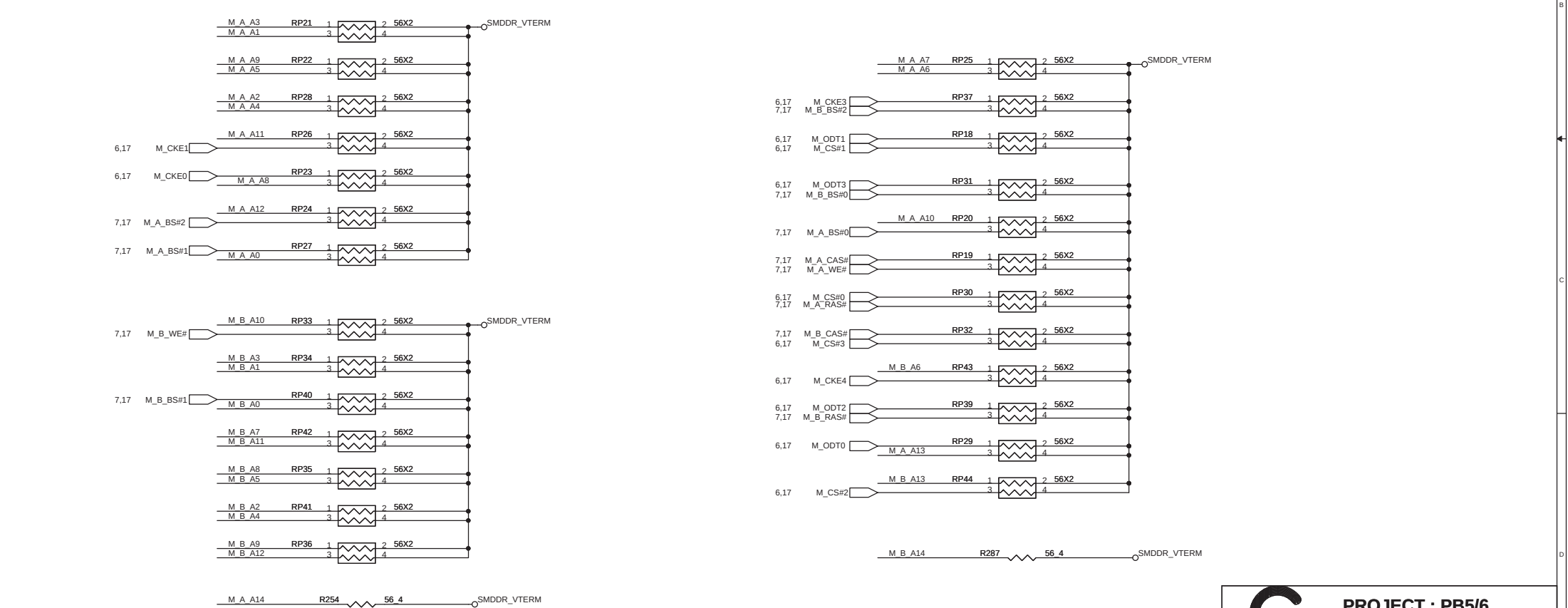
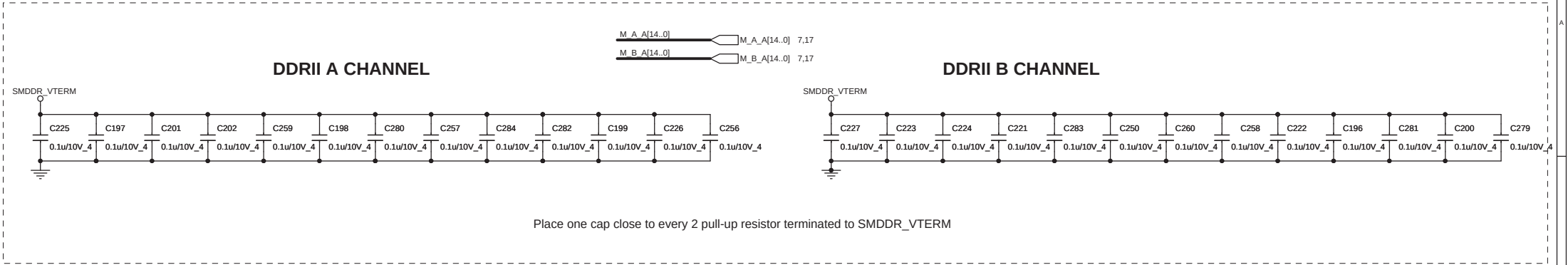


UZZE		
A426	VSS101	VSS107
A427	VSS102	VSS108
A43	VSS103	VSS109
A46	VSS110	VSS110
A51	VSS111	AC22
A52	VSS112	VSS112
A53	VSS113	K13
A58	VSS114	K23
A62	VSS115	VSS115
A64	VSS116	VSS116
A65	VSS117	VSS117
AC17	VSS118	VSS118
AC27	VSS119	VSS119
AC3	VSS120	VSS120
AD1	VSS121	M12
AD10	VSS122	M13
AD11	VSS123	M14
AD12	VSS124	M15
AD14	VSS125	M16
AD15	VSS126	M17
AD18	VSS127	M23
AD19	VSS128	M24
AD2	VSS129	M29
AD26	VSS130	N11
AD4	VSS131	N12
AD6	VSS132	N13
AD7	VSS133	N14
AD8	VSS134	N15
AD9	VSS135	N16
AE1	VSS136	N17
AE13	VSS137	N18
AE16	VSS138	N19
AE17	VSS139	N27
AE2	VSS140	P17
AE3	VSS141	P18
AE20	VSS142	P14
AE24	VSS143	P15
AE3	VSS144	P16
AE4	VSS145	P17
AE9	VSS146	P23
AE10	VSS147	P28
AE11	VSS148	P29
AE12	VSS149	P3
AE14	VSS150	P4
AE15	VSS151	P5
AE16	VSS152	R11
AE18	VSS153	R12
AE27	VSS154	R13
AE28	VSS155	R14
AE3	VSS156	R15
AE9	VSS157	R17
AG16	VSS158	R18
AG18	VSS159	R19
AG25	VSS160	R22
AG3	VSS161	R23
AG4	VSS162	T12
AG6	VSS163	T13
AG7	VSS164	T14
AG8	VSS165	T15
AG11	VSS166	T16
AG14	VSS167	T23
AM1	VSS168	B30
AM13	VSS169	L02
AH2	VSS170	L11
AH25	VSS171	L12
AH26	VSS172	L05
AH28	VSS173	L06
AH6	VSS174	L07
A13	VSS175	AD22
A34	VSS176	L02
A31	VSS177	L03
AH7	VSS178	V11
B1	VSS179	V12
B4	VSS180	V13
B7	VSS181	V14
B2	VSS182	V23
B20	VSS183	V29
B78	VSS184	V4
B79	VSS185	V5
B8	VSS186	W26
C28	VSS187	M27
C27	VSS188	AG28
C31	VSS189	AH6
E12	VSS190	V1
E14	VSS191	V23
E18	VSS192	V29
F2	VSS193	V4
F21	VSS194	V5
F4	VSS195	AG28
F9	VSS196	AH6
F91	VSS197	A62
F14	VSS198	B29
F28	VSS199	AH
F29	VSS199	A2
G14	VSS199	A28
G14	VSS199	A31
G21	VSS199	AH1
G26	VSS199	AH2
G28	VSS199	AH3
G27	VSS199	AH4
G4	VSS199	AH5
H2	VSS199	AH6
H2	VSS199	AH7
H2	VSS199	AH8
H2	VSS199	AH9
H2	VSS199	AH10
H2	VSS199	AH11
H2	VSS199	AH12
H2	VSS199	AH13
H2	VSS199	AH14
H2	VSS199	AH15
H2	VSS199	AH16
H2	VSS199	AH17
H2	VSS199	AH18
H2	VSS199	AH19
H2	VSS199	AH20
H2	VSS199	AH21
H2	VSS199	AH22
H2	VSS199	AH23
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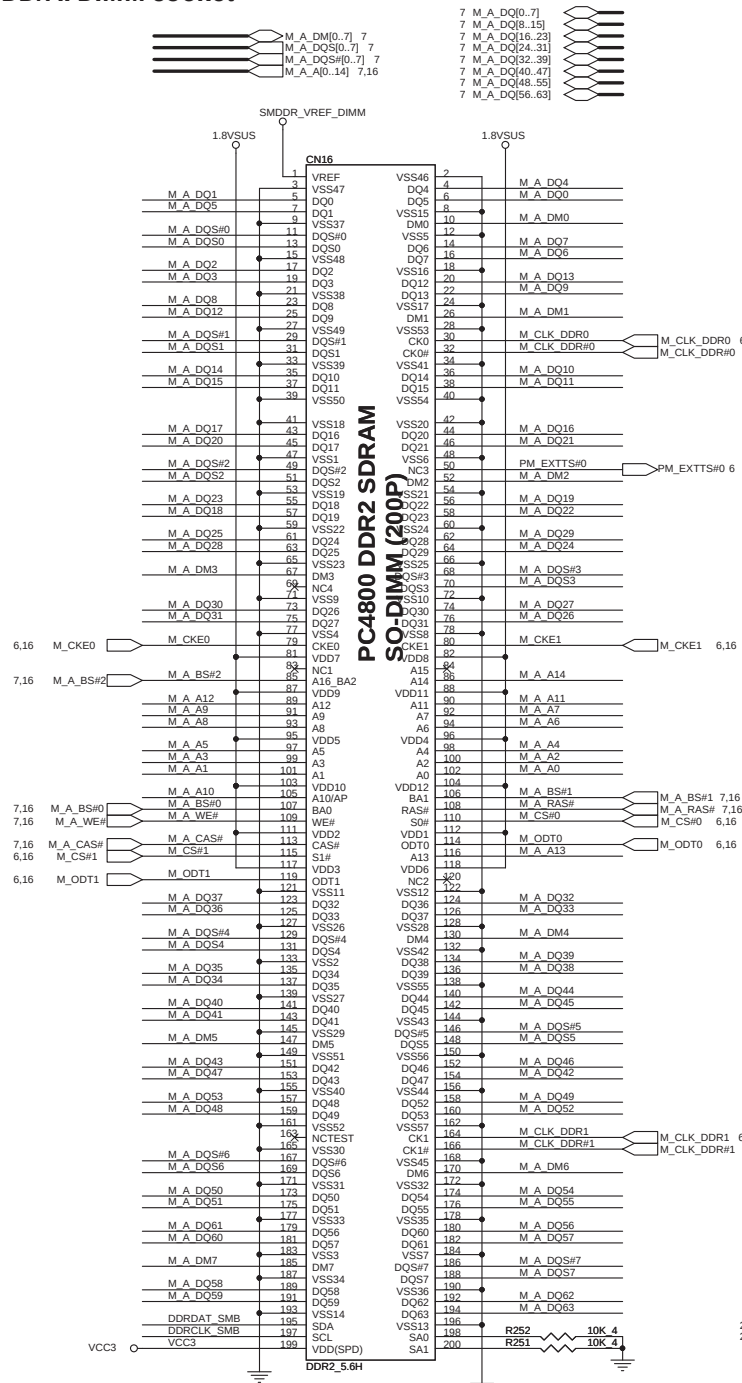


PROJECT : PB5/6
Quanta Computer Inc.

Reference	Description
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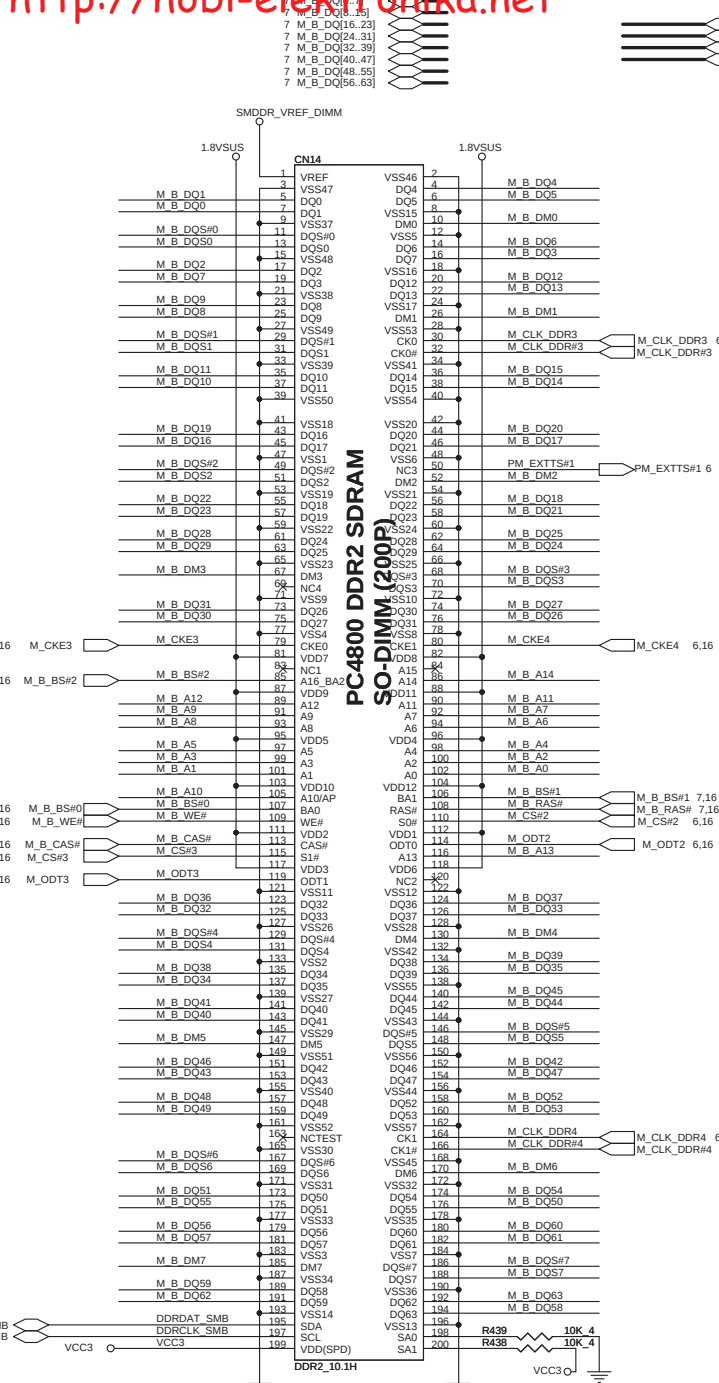


DDR II DIMM Socket



CH-A SPD ADDRESS:?????

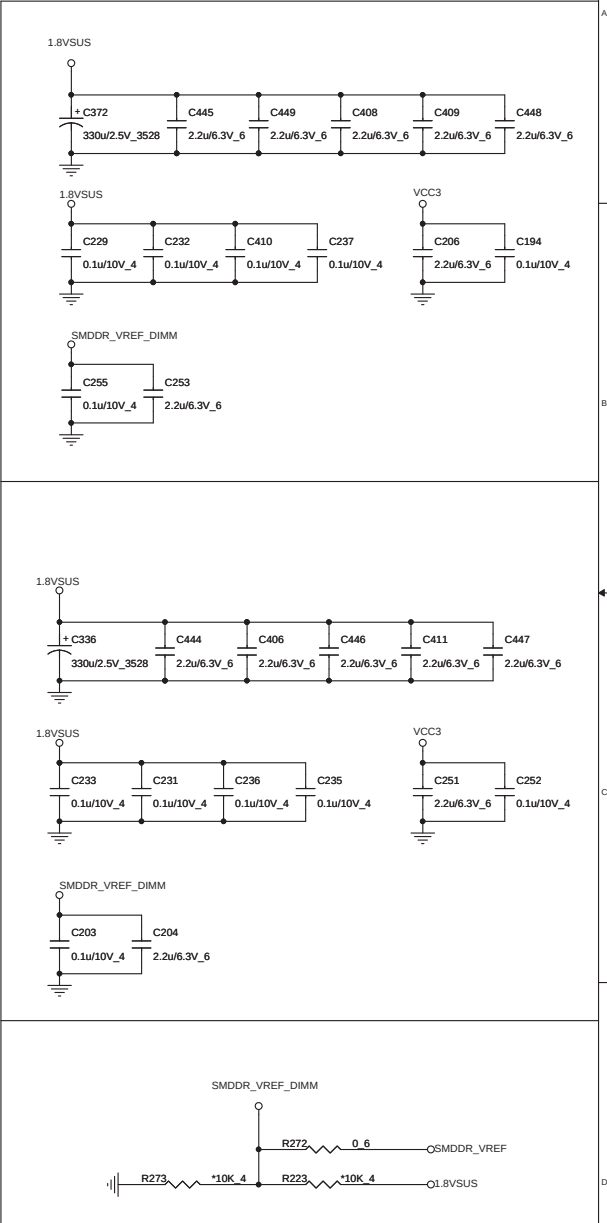
<http://hobi-elektronika.net>



CH-A SPD ADDRESS:??????

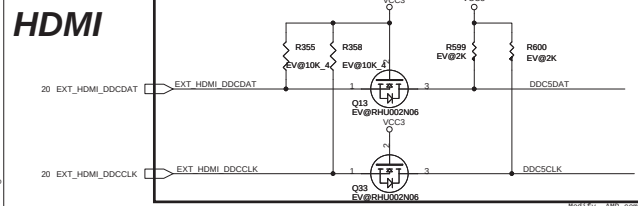
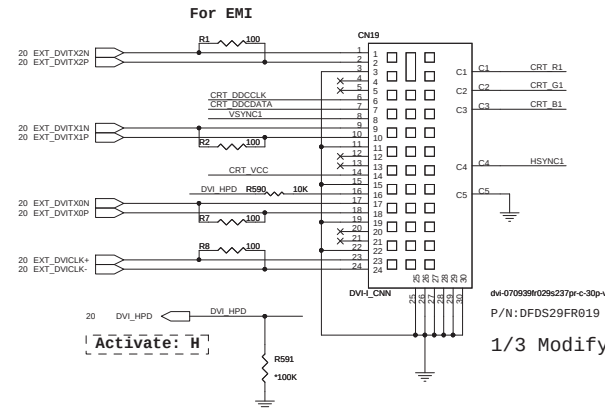
Reference	Description
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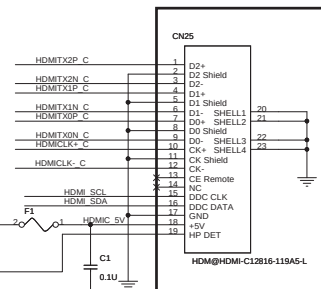
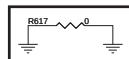
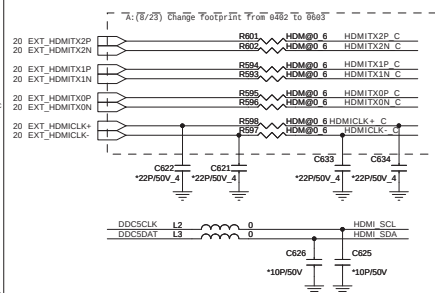
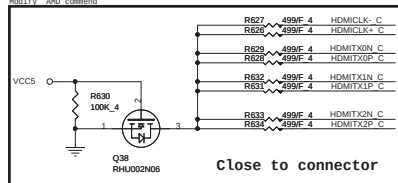
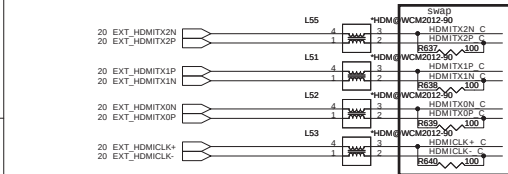
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		Quanta Computer Inc.	
Size	Document Number	Rev	
	DDR SO-DIMM	1A	
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7		8	

DVI-I

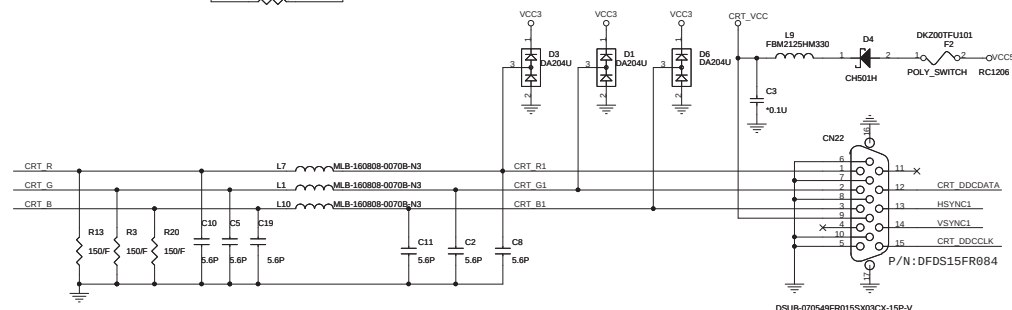
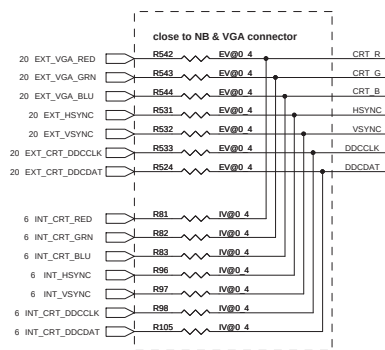
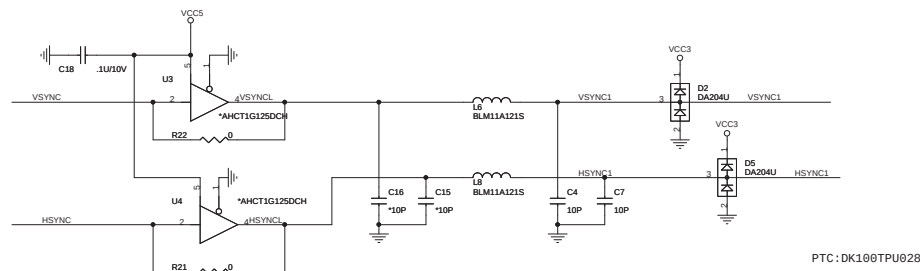
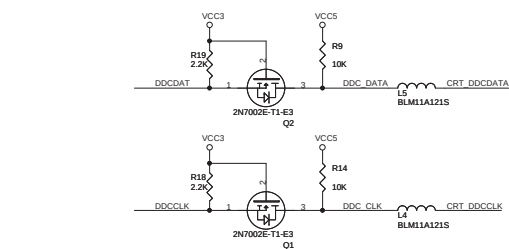


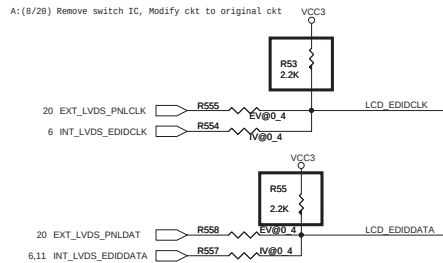
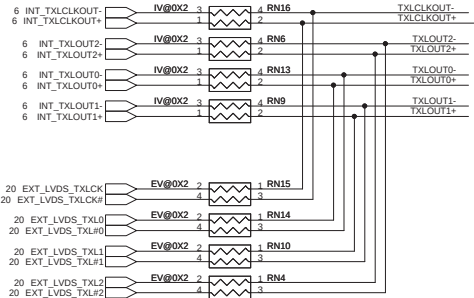
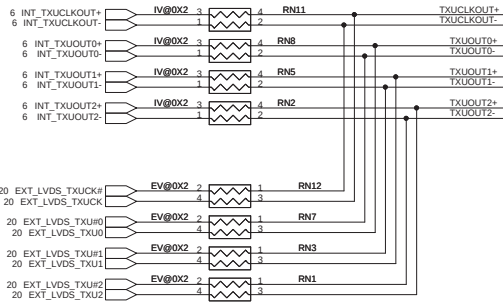
Close HDMI connector

Co-Layout

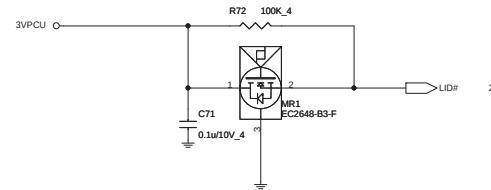


CRT PORT

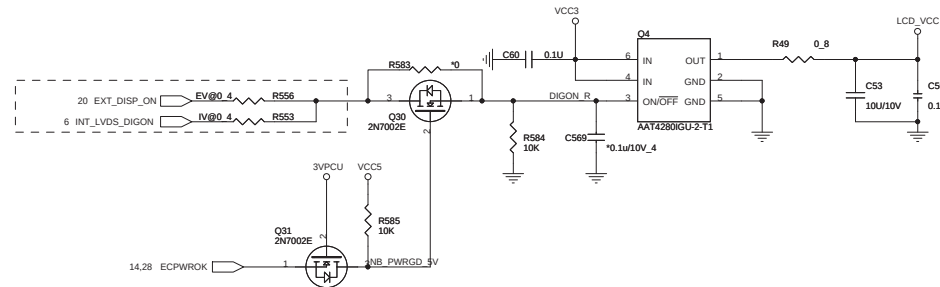
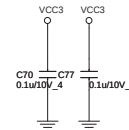




HALL SENSOR

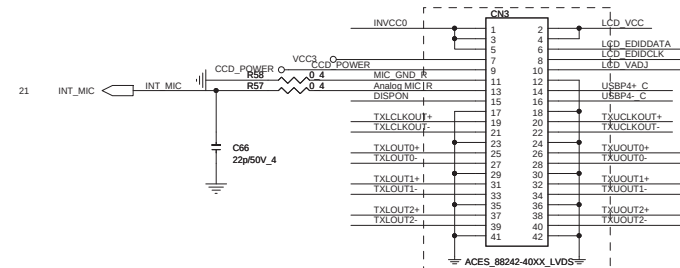


11/01 add stitch cap for LVDS

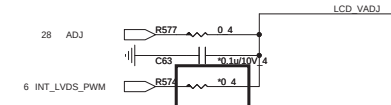
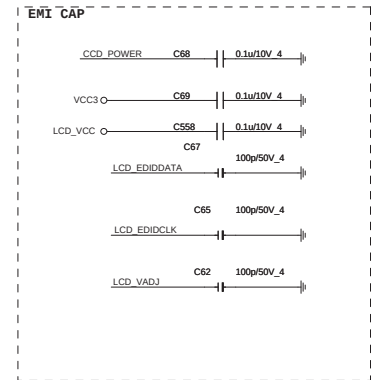


8/13 Change Size To 1206

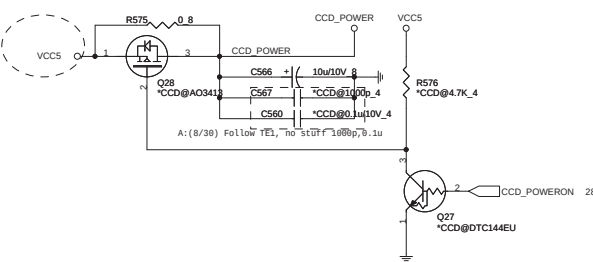
10/22 update p/n From DFHS40FS825 to DFWF40MS000



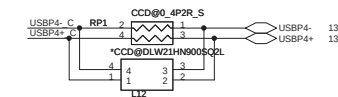
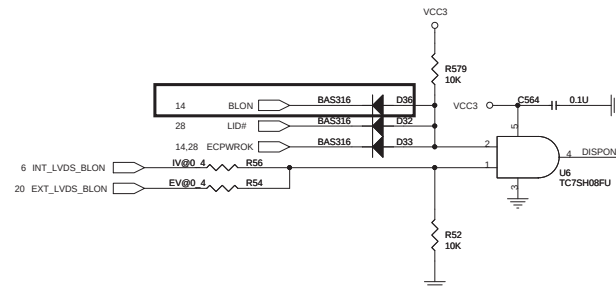
LCD PANEL MODULE

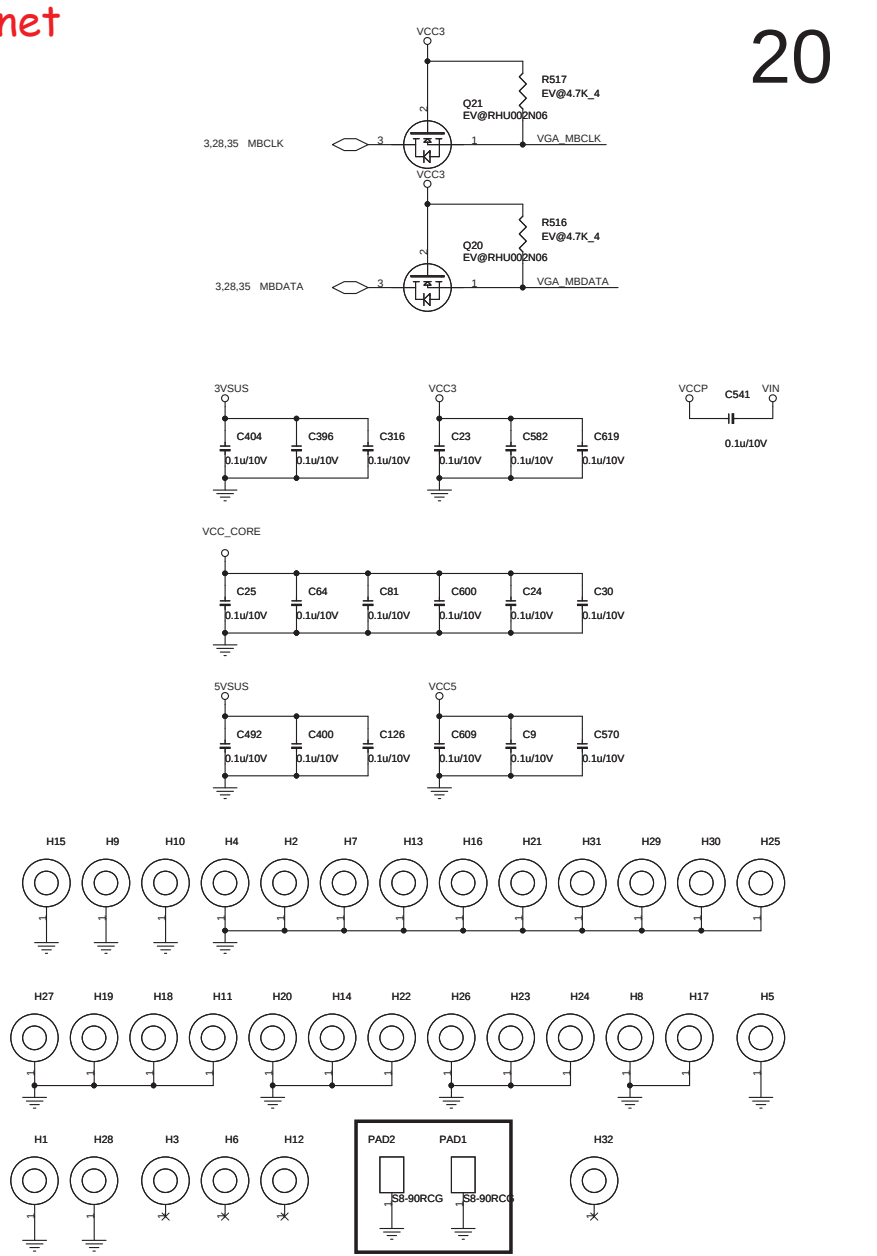
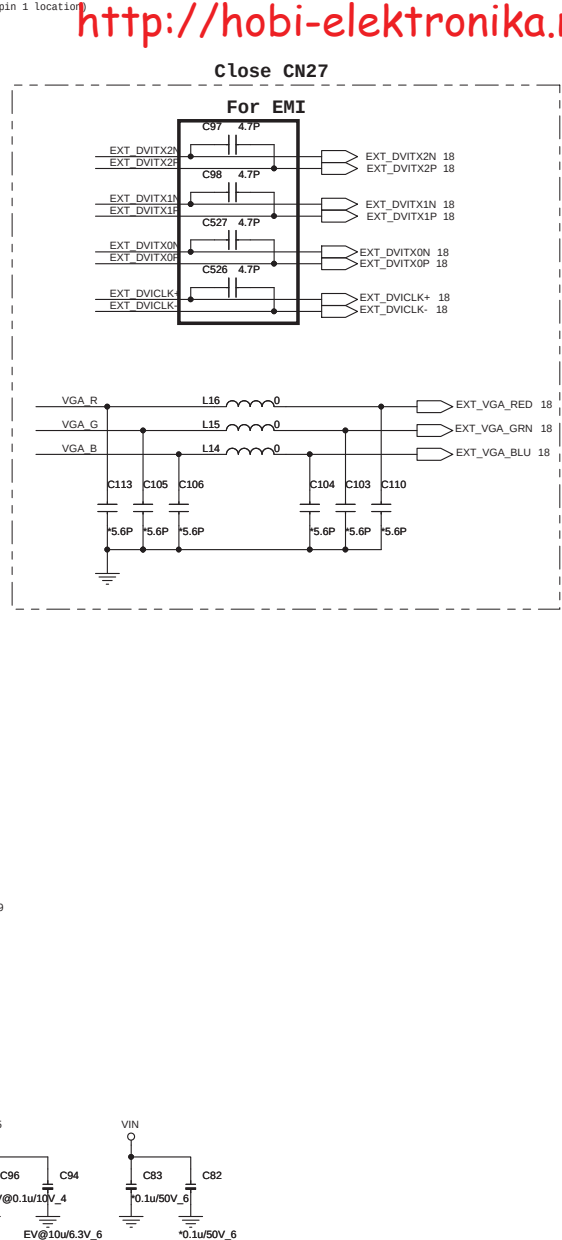
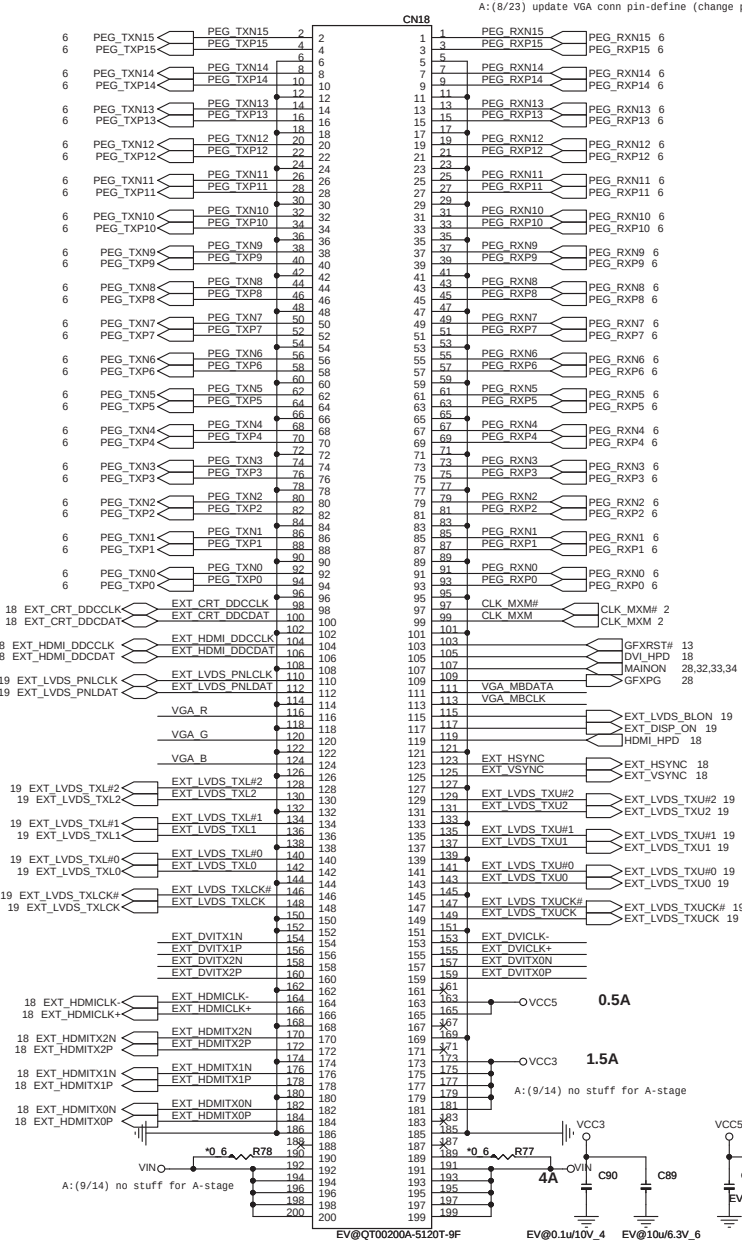


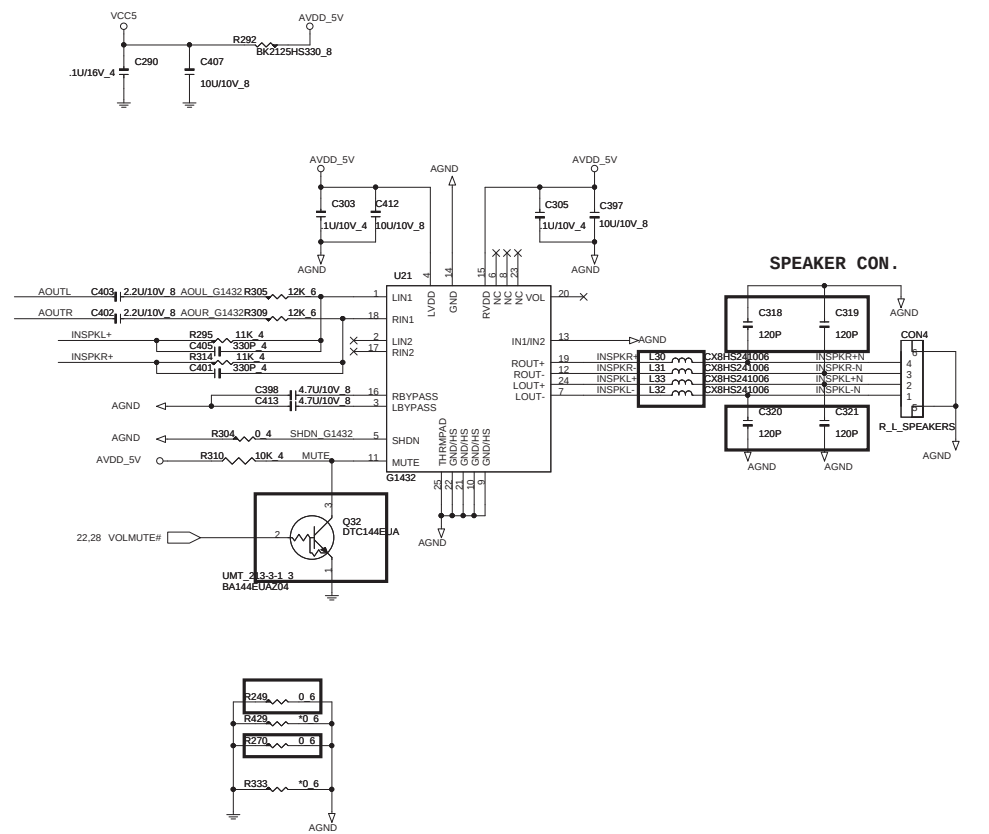
CAMERA MODULE



A:(11/27) Camera module power VCC5 or VCC3?

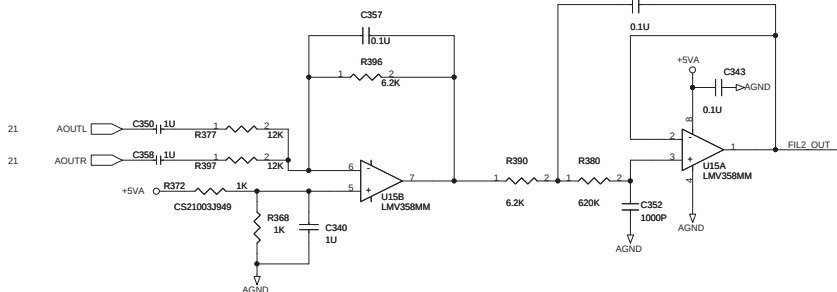




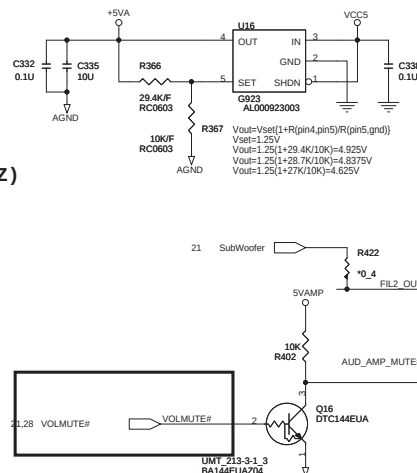
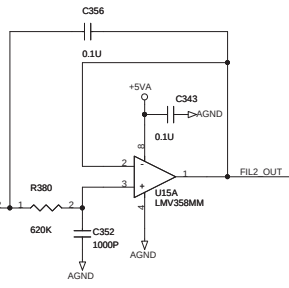
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Date:	Friday, May 30, 2008	Sheet 21 of 35

Mixer & 1st order low pass filter(338HZ)

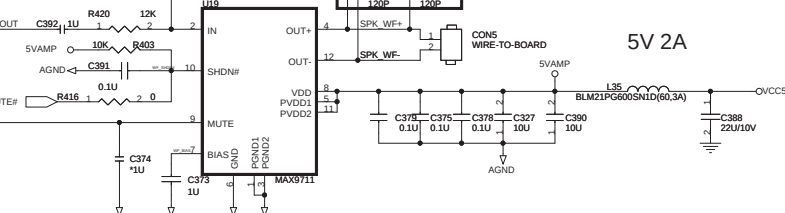


2nd order low pass filter(338HZ)

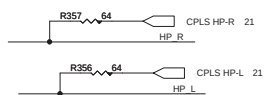


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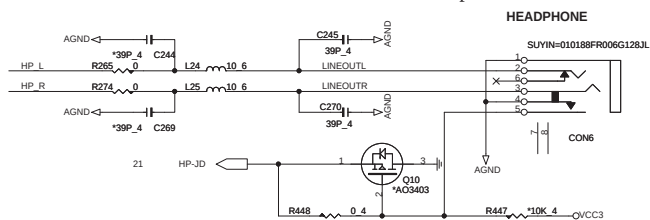
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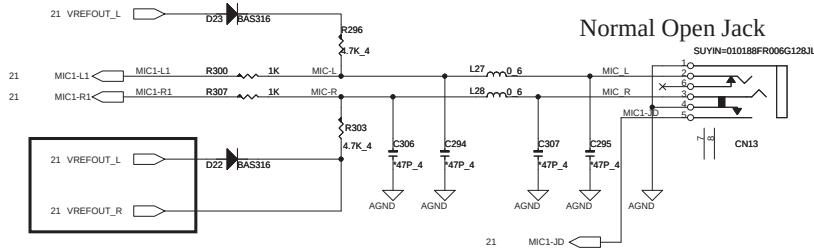
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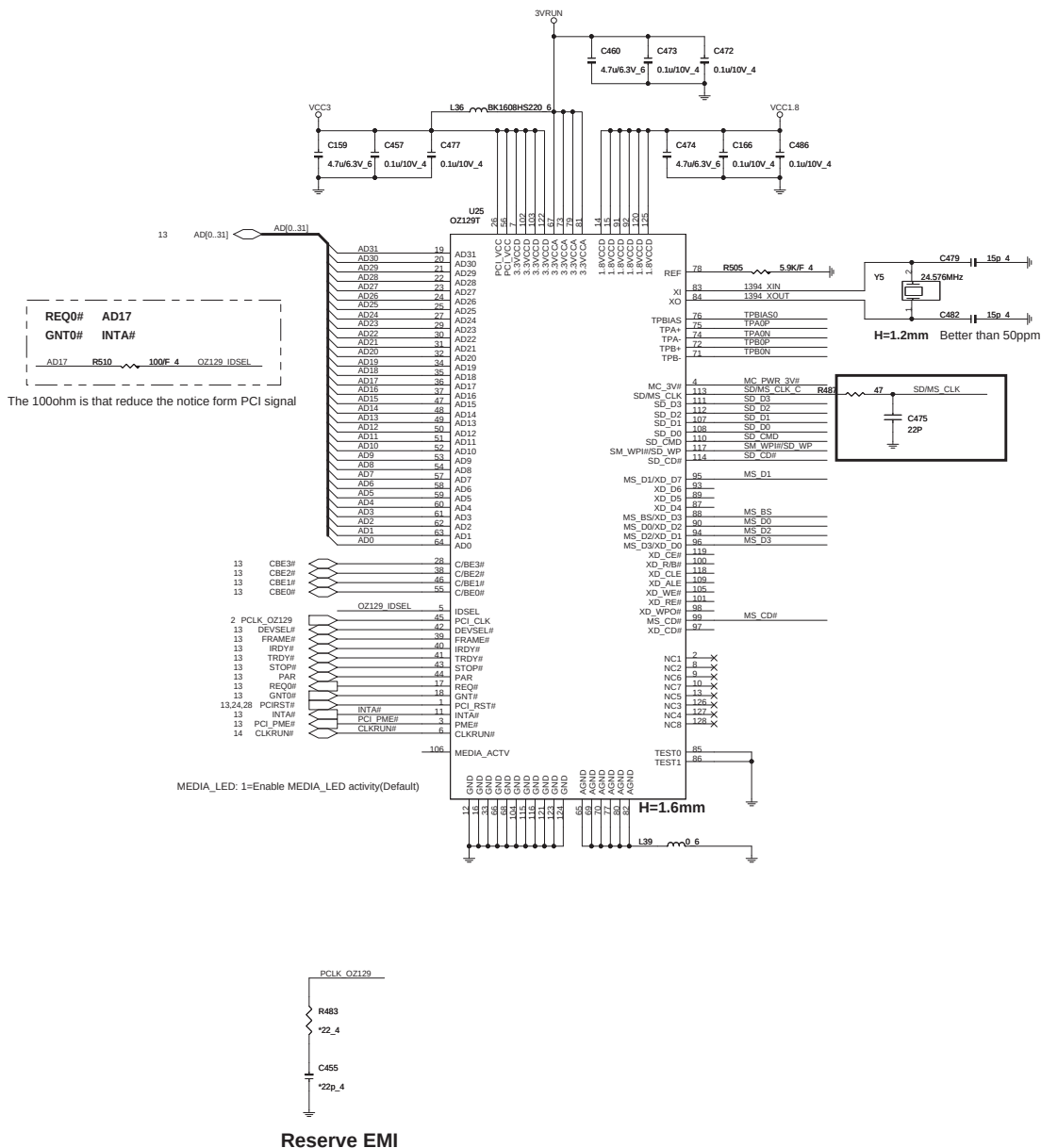
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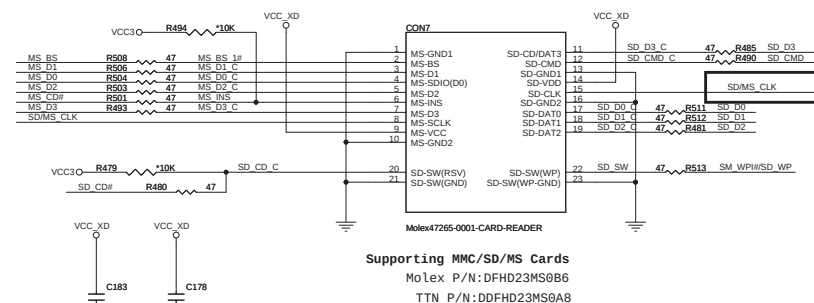
SYSTEM MIC



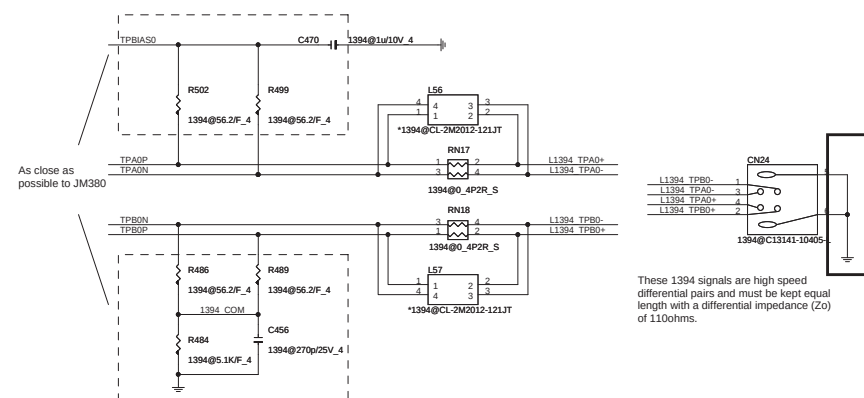
PROJECT : PB5/6
Quanta Computer Inc.

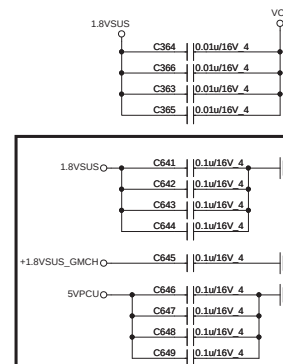
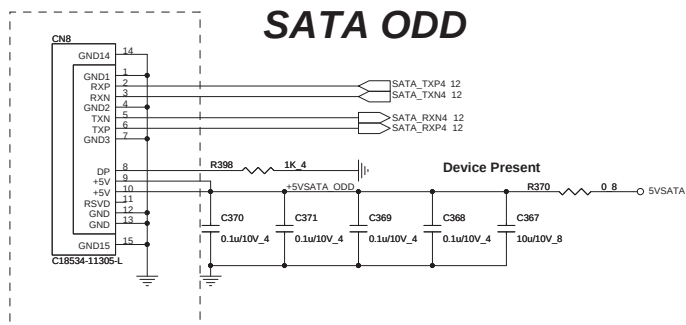


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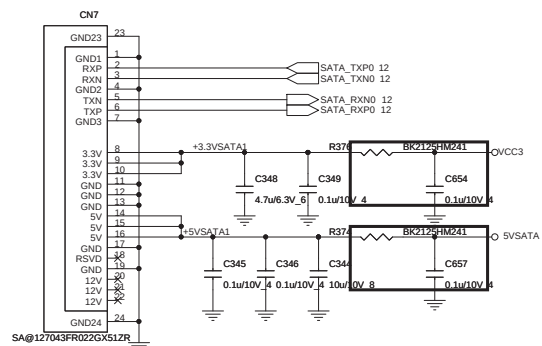


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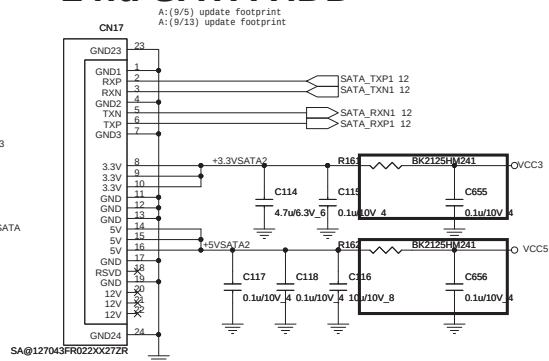




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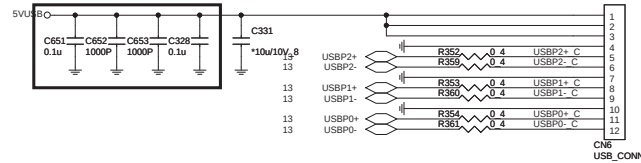
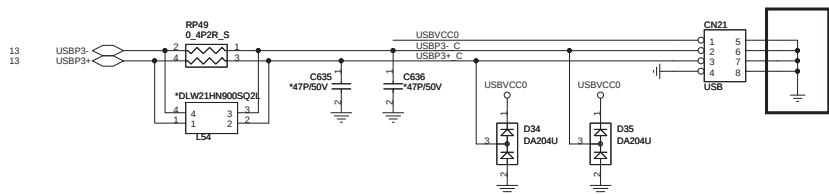
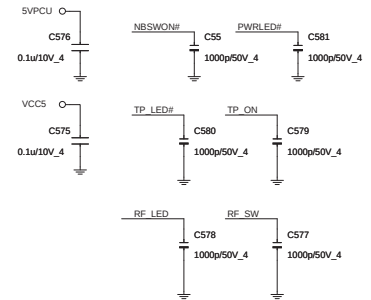
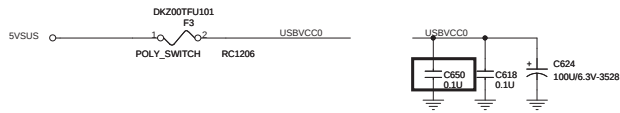
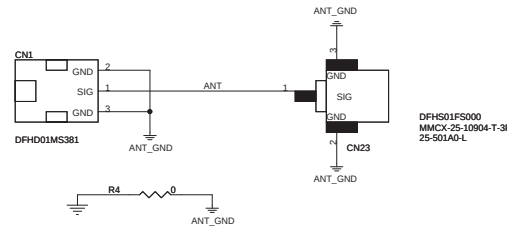
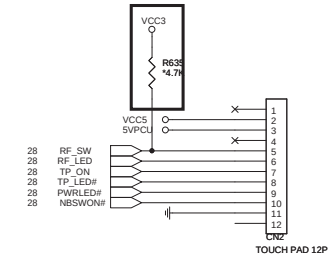
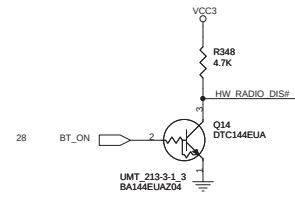
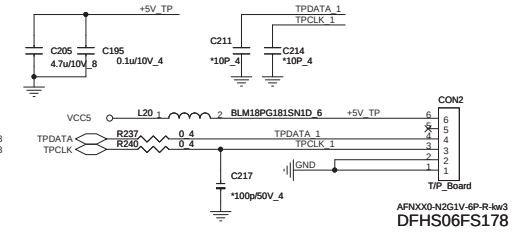
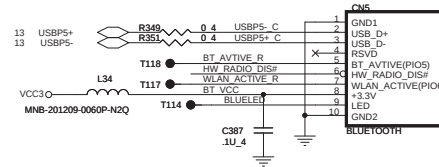
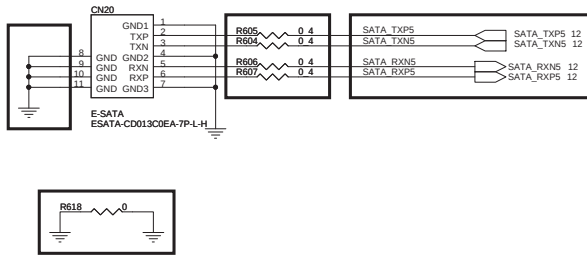


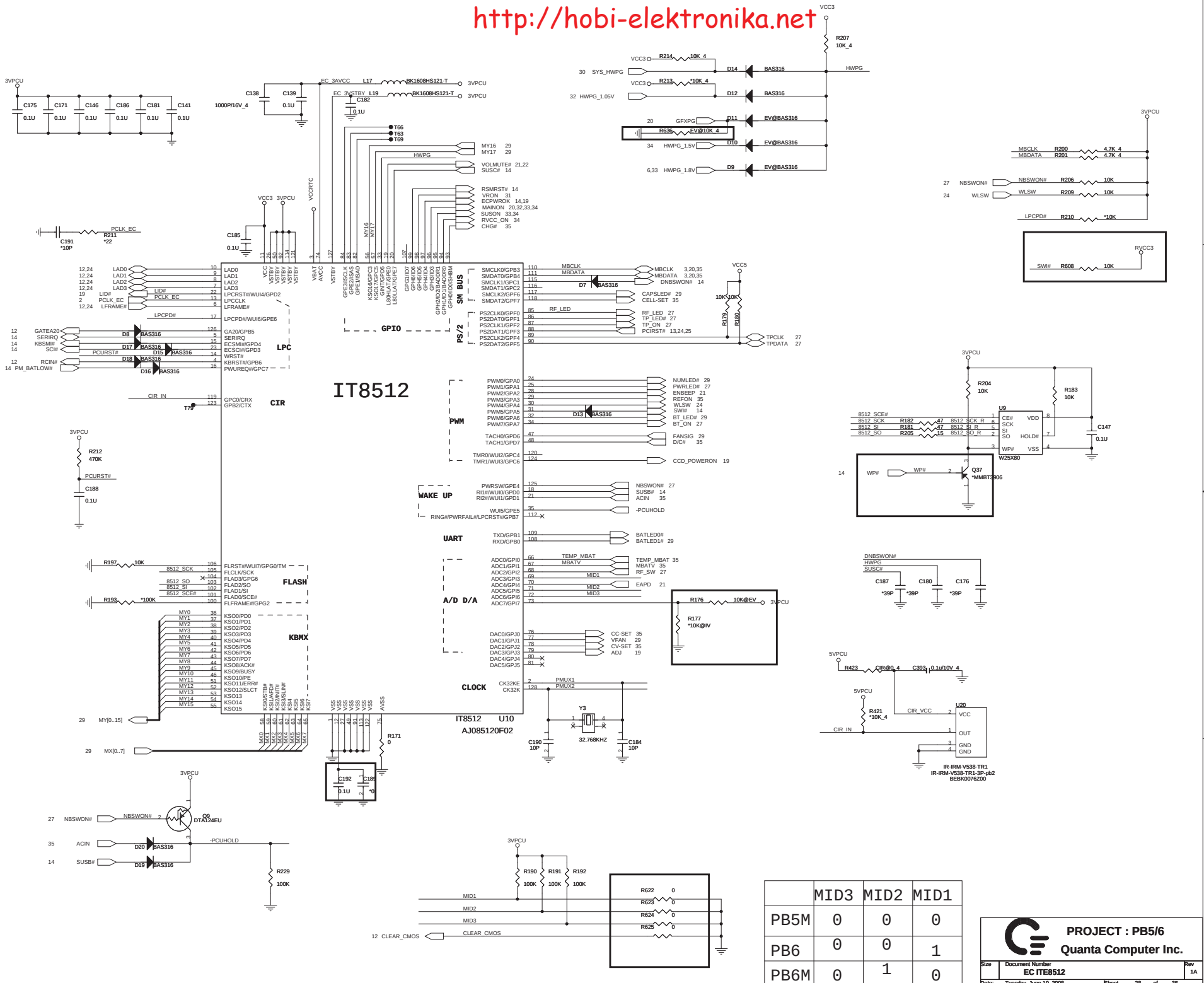
2'nd SATA HDD



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	SATA / HyberFLASH	1A
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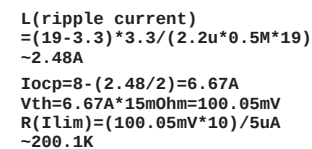


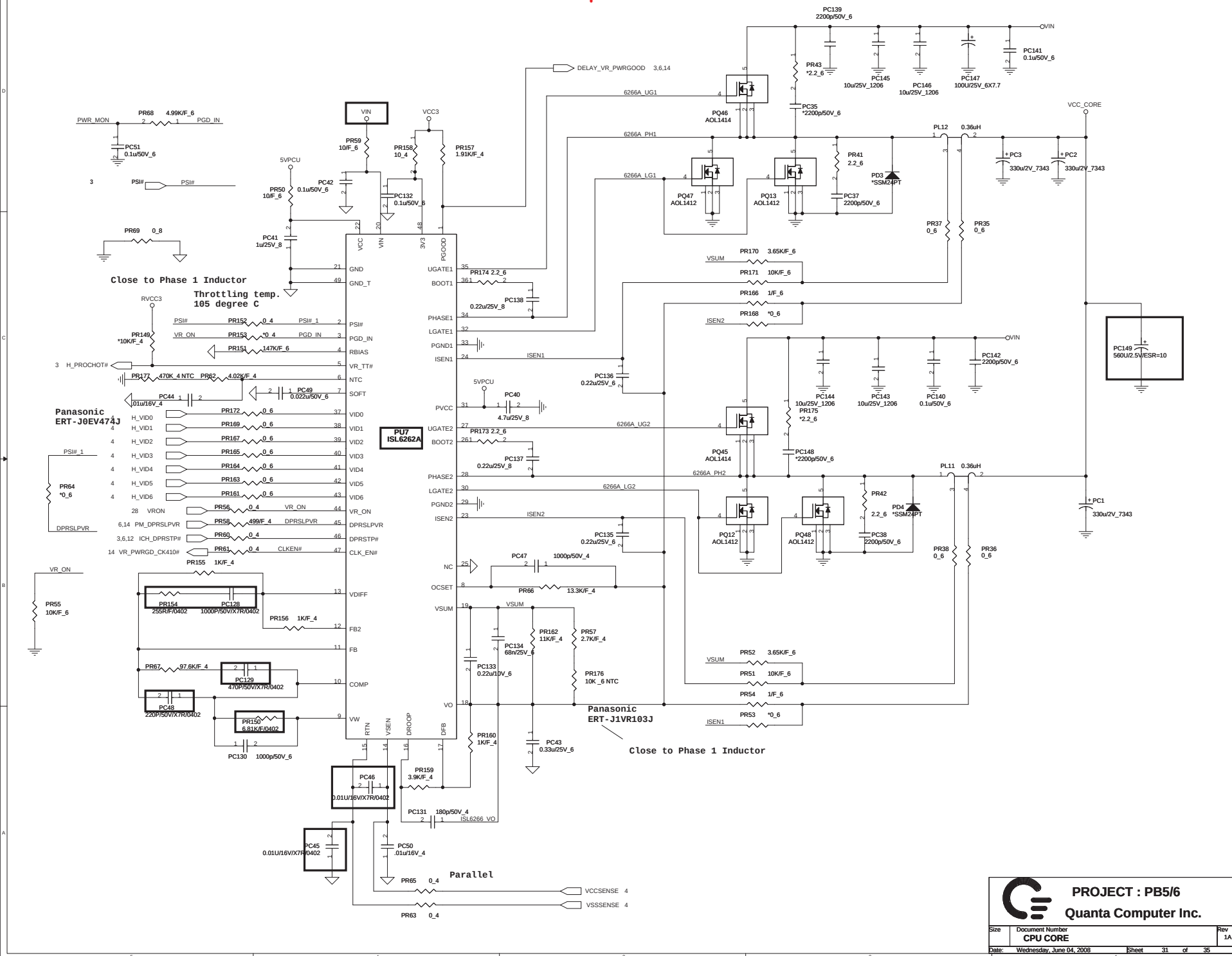


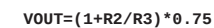
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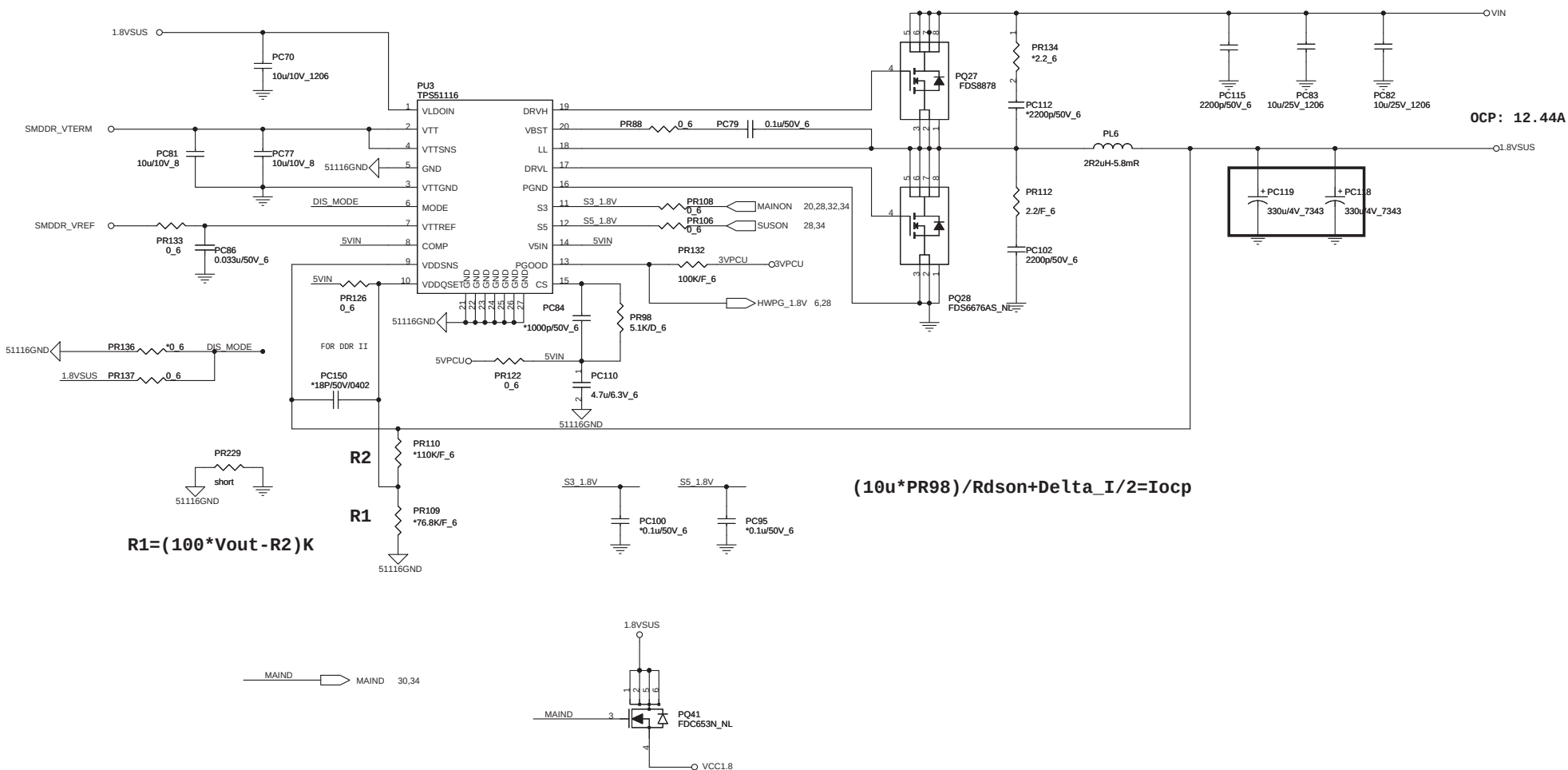
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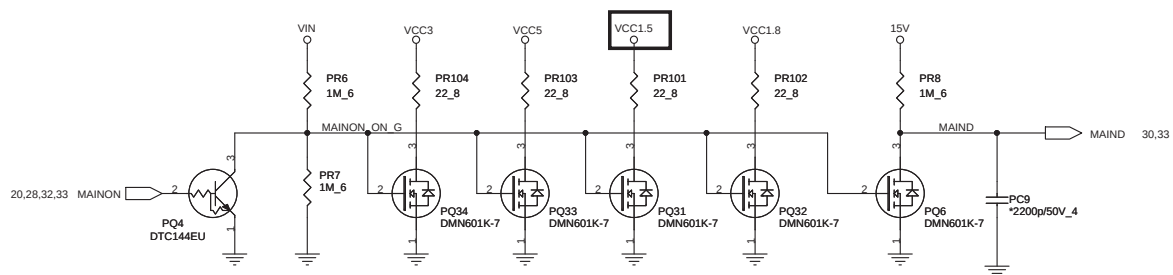
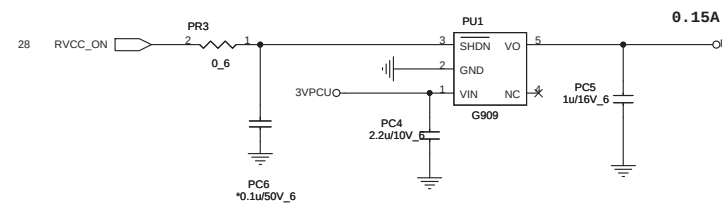
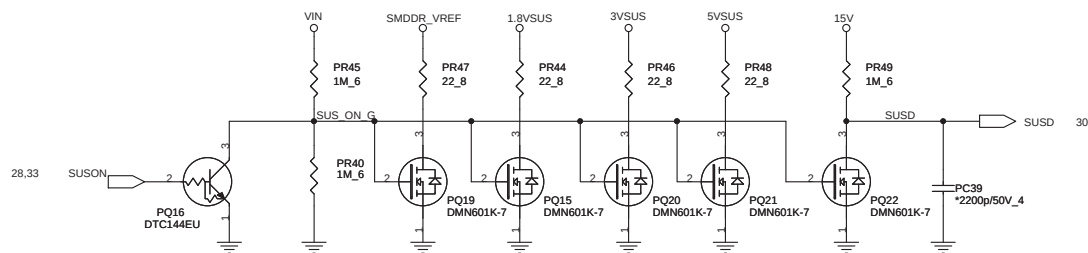
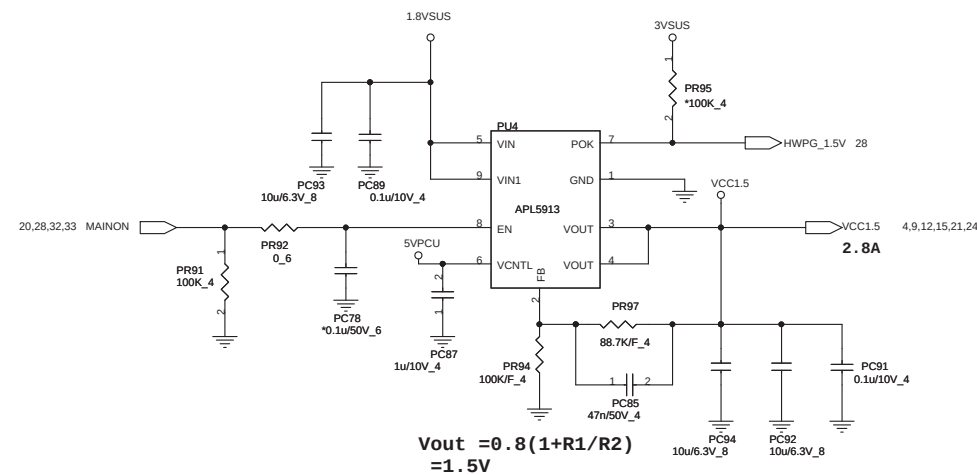
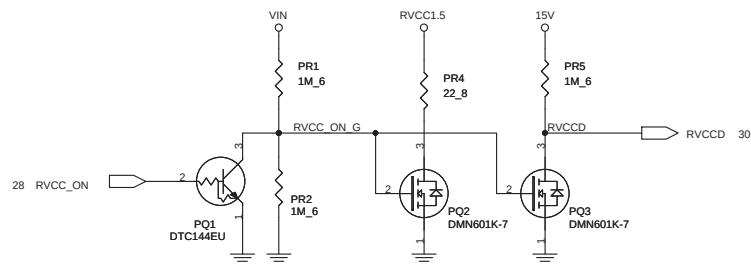
		PROJECT : PB5/6 Quanta Computer Inc.	
Size	Document Number	R	
	SW/LED/Keyboard		
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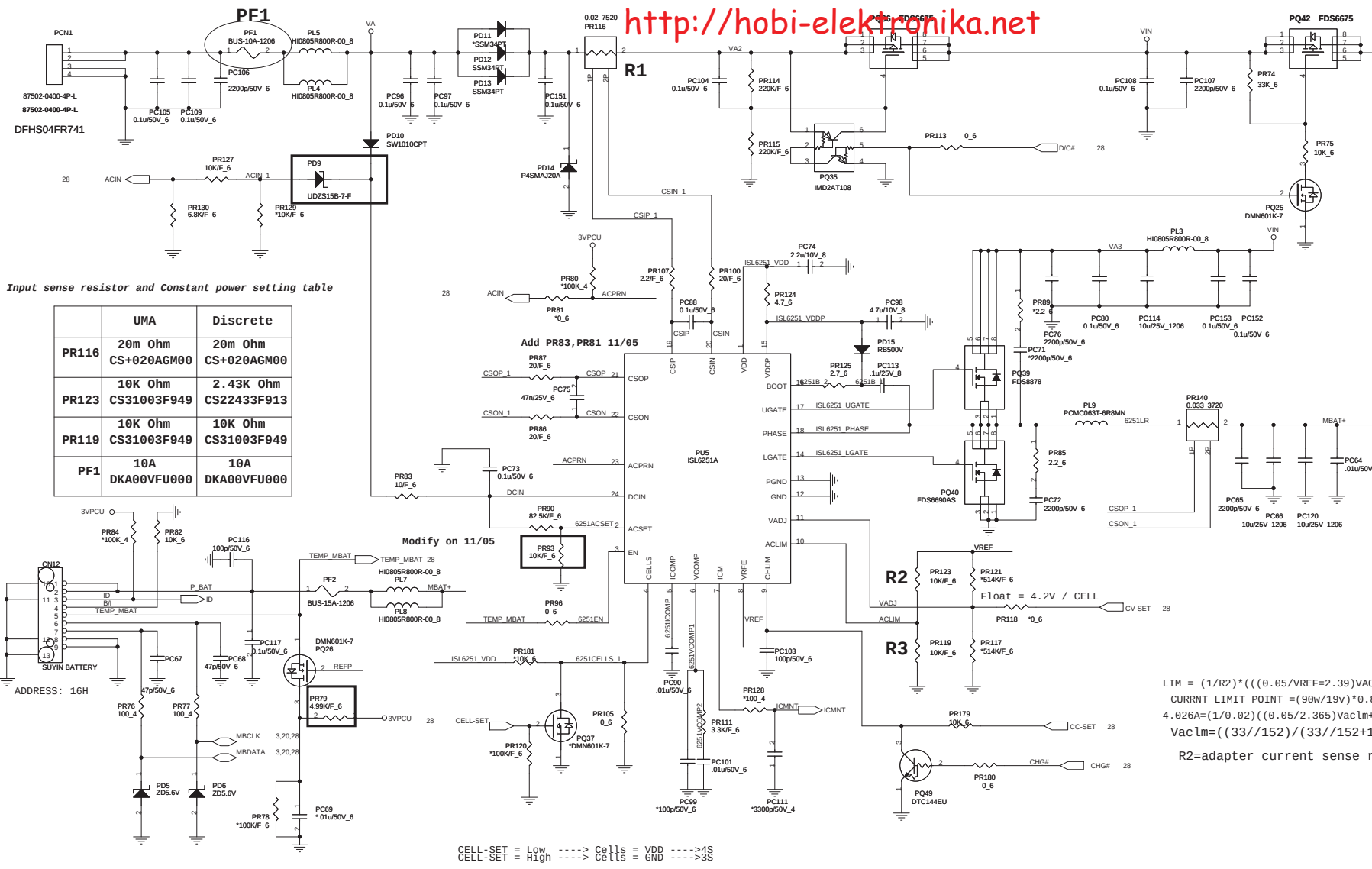












$$LIM = (1/R2) * (((0.05/VREF=2.39)VACLM)+0.050)$$

$$CURRNT LIMIT POINT = (90w/19v) * 0.85 = 4.026A$$

$$4.026A = (1/0.02) * ((0.05/2.365)VacLm+0.05)$$

$$VacLm = ((33//152)/(33//152+19.6//152)) * Vref$$

R2=adapter current sense resistence

