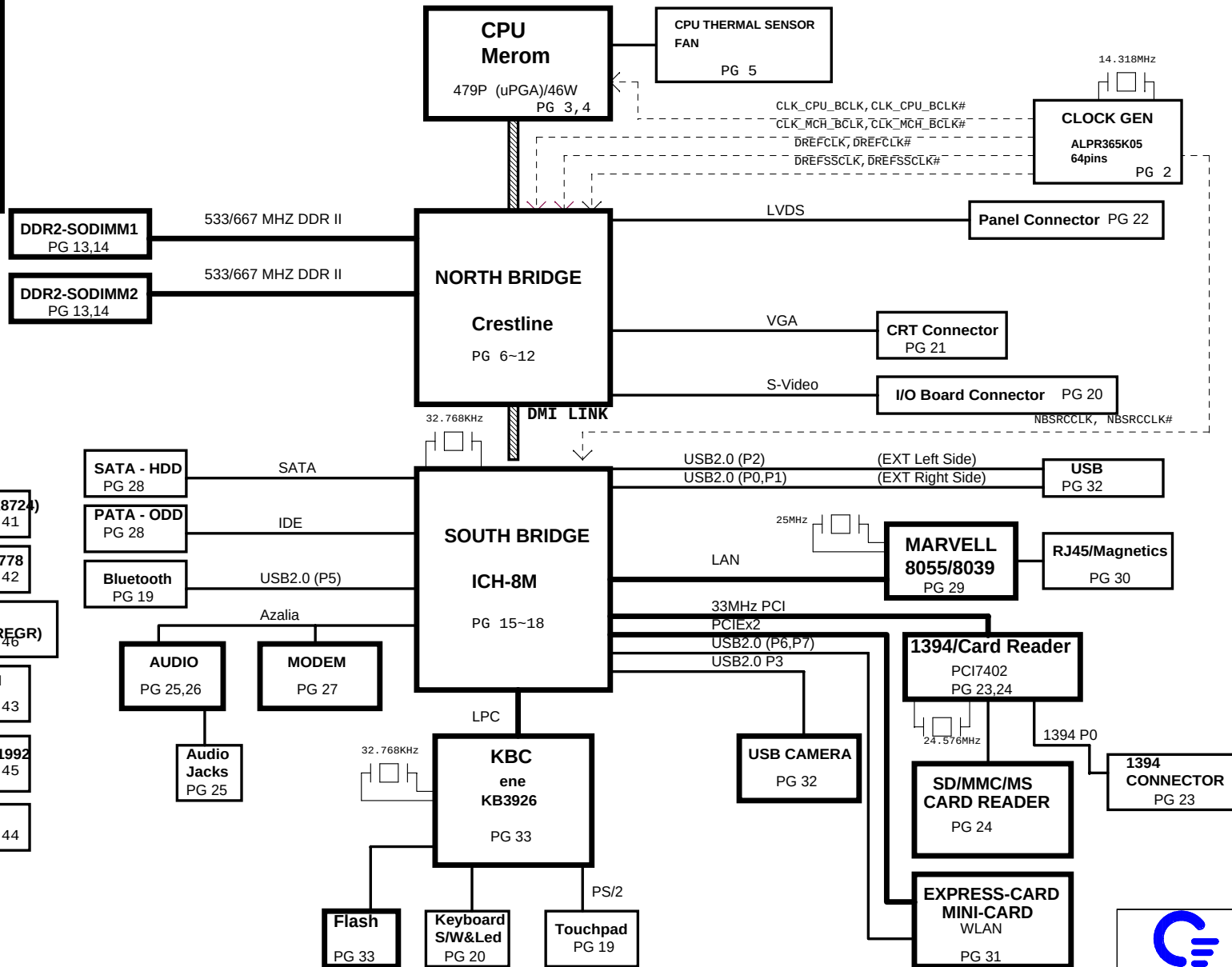


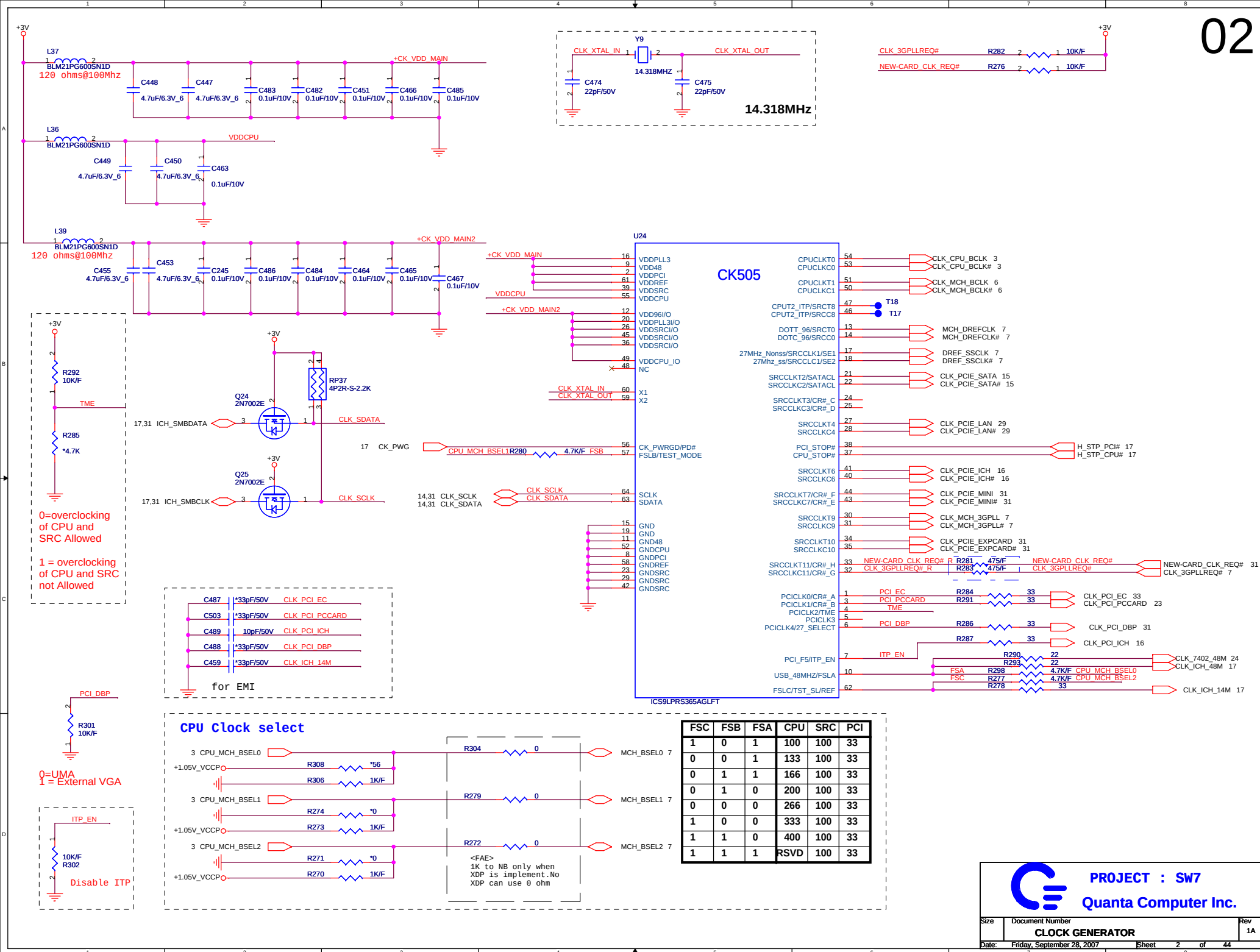
SW7 BLOCK DIAGRAM

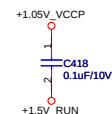
01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT







COMP0
COMP1
COMP2
COMP3

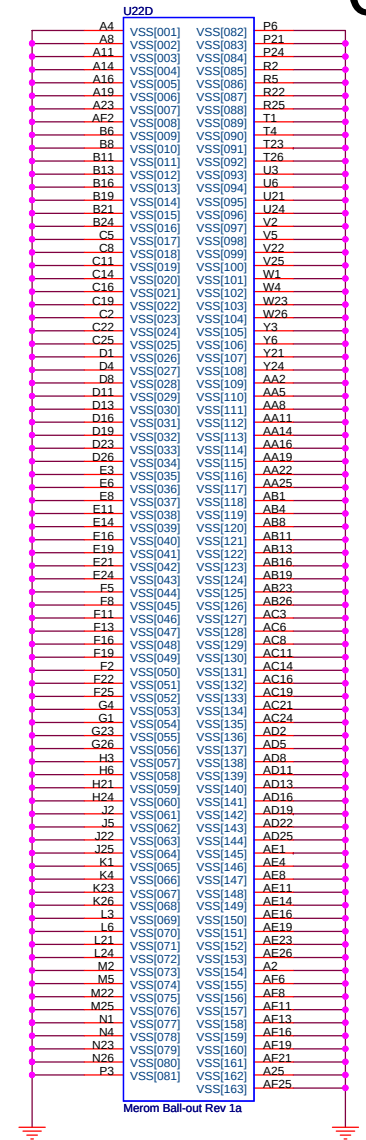
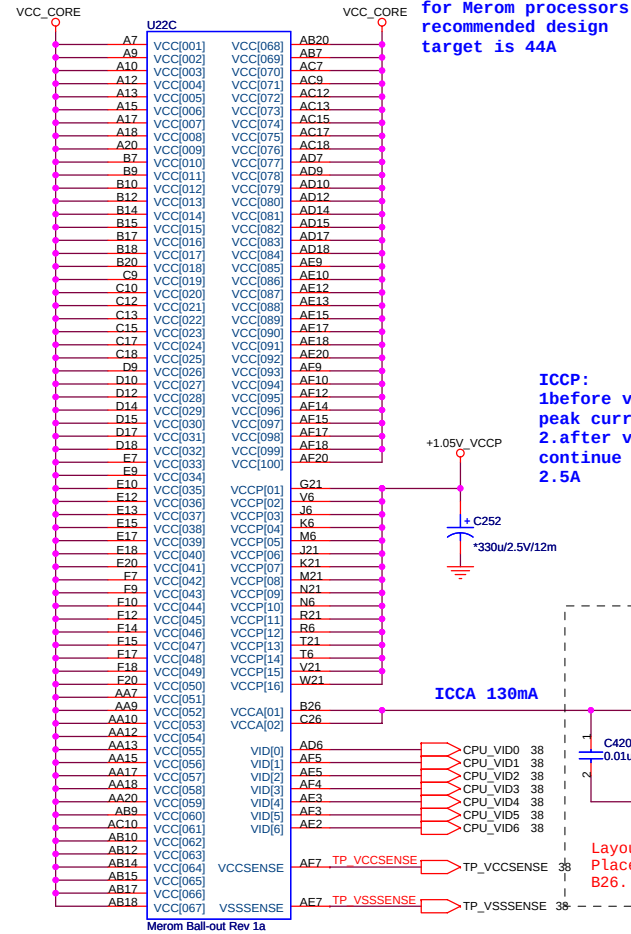
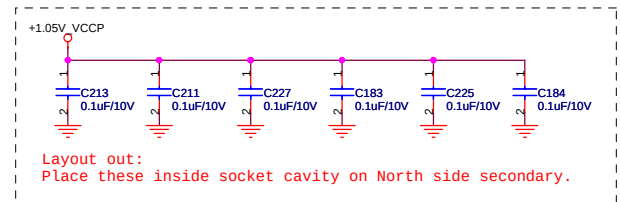
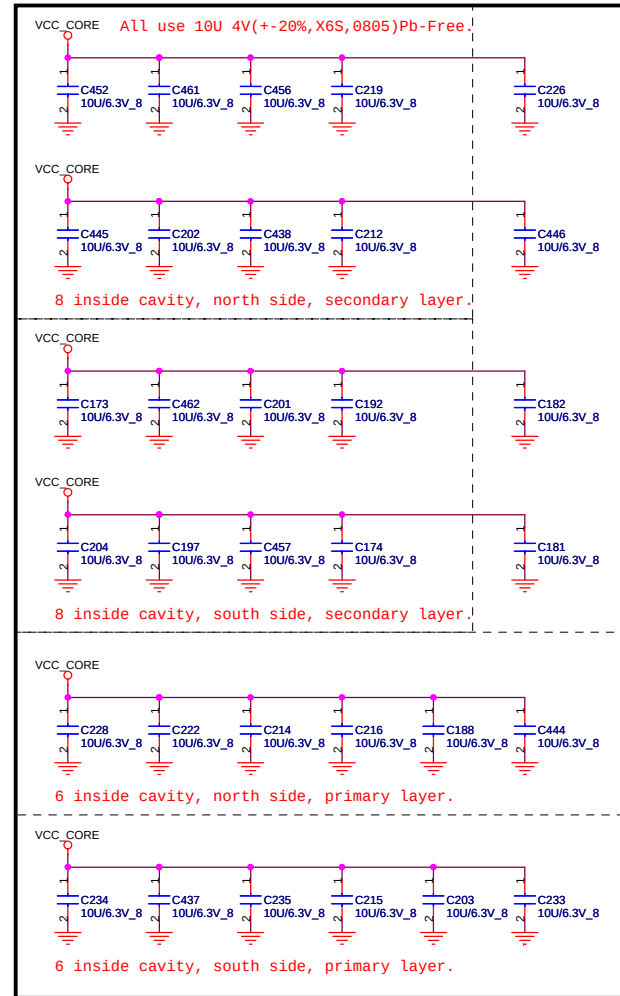
R110 54.9%
R109 27.4%
R58 54.9%
R59 27.4%

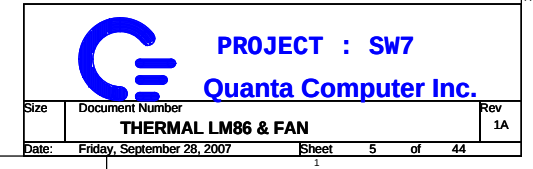
Comp0,2 connect with $Z_0=27.4\text{ohm}$, Comp1,3 connect with $Z_0=55\text{ohm}$, make those traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.

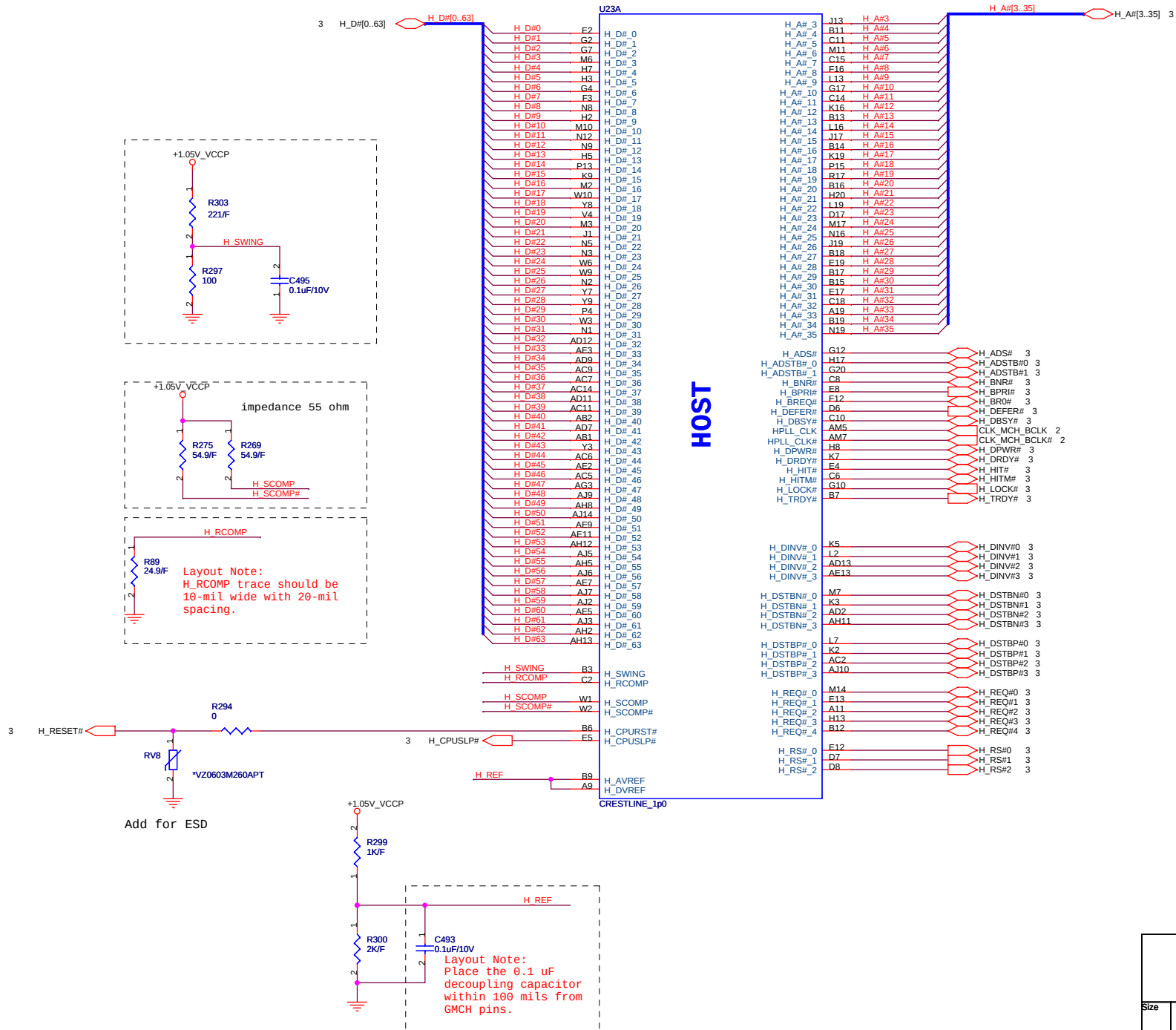


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.





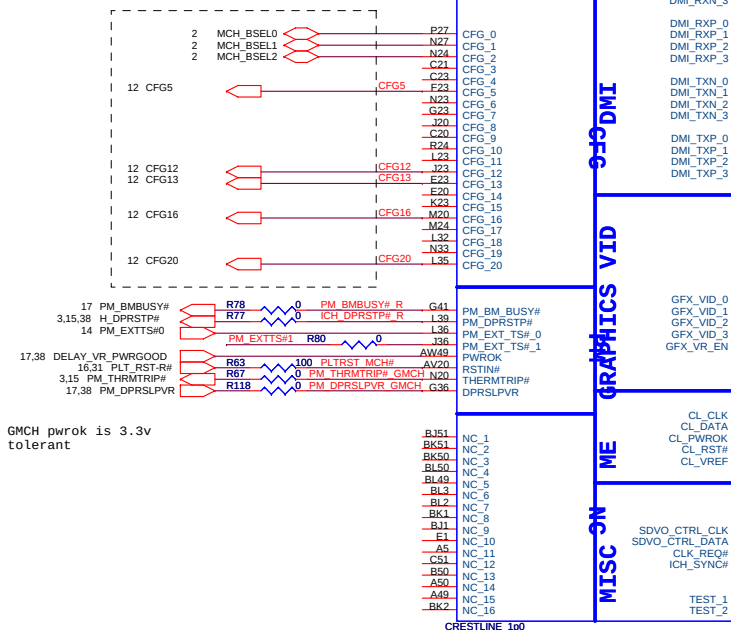


PROJECT : SW7
Quanta Computer Inc.

W22 update
--- MA14 needs
to be routed if
customers are
planning on
using 2Gb
technology and
width=8 (by 8)
DIMMs

CRESTLINE
new pin
define

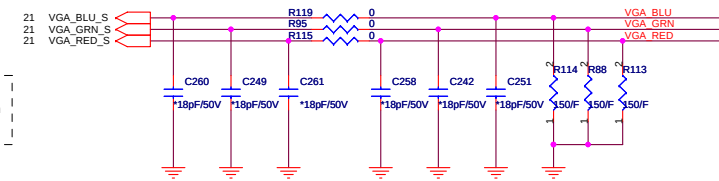
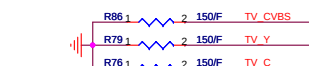
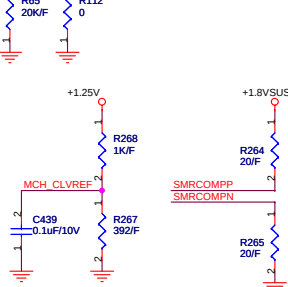
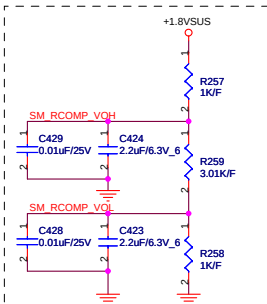
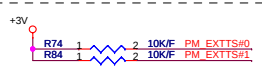
Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minimize stub.



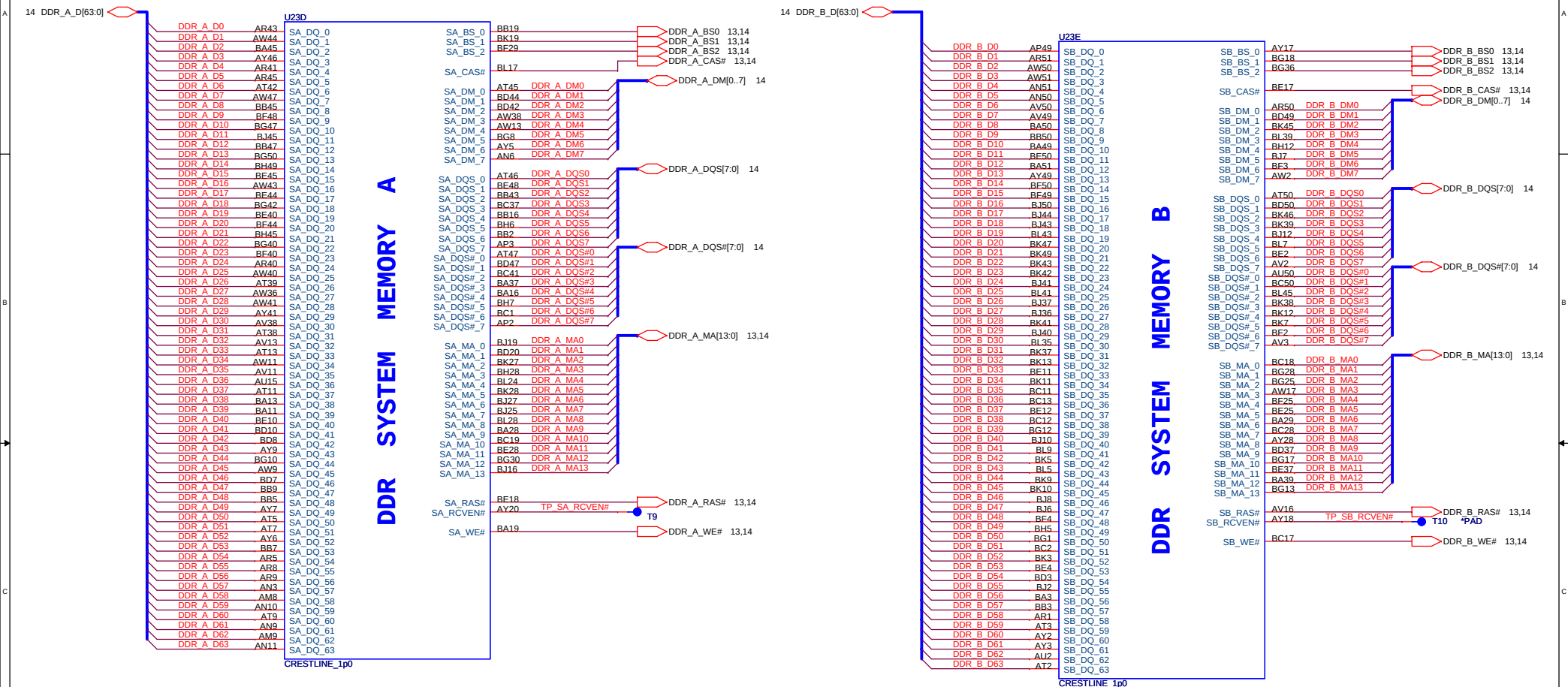
IV&EV Dis/Enable setting

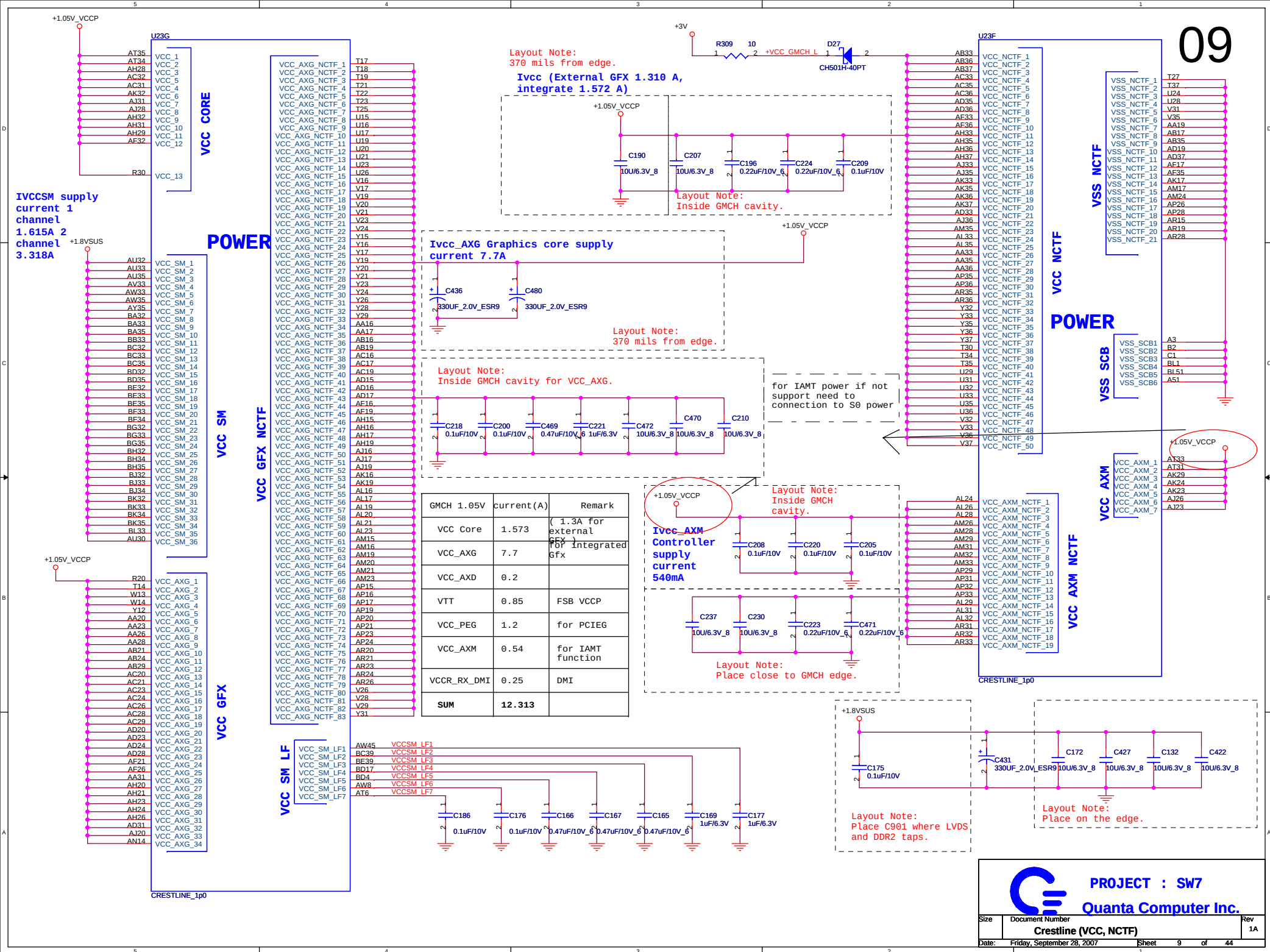
In Crestline EDS
Rev.1.0, Render
Standby Voltage is
not finalized
yet(TBD), 1.05V for
Graphic Voltage
range(VCC_AXG) is
between 0.9975V(min.)
and 1.1025V(max.).
Vgfx max at 1.1025V @
8A (estimated)

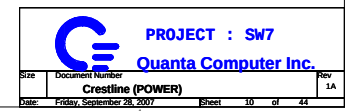
only resever A13/5 not
support IAMT, but design
line suggest to connection
these pin, do not NC

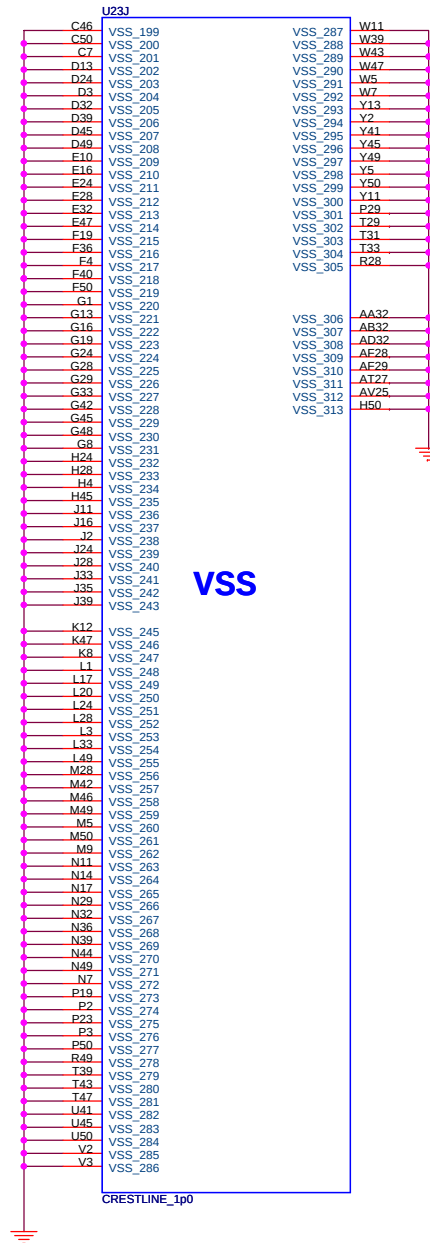
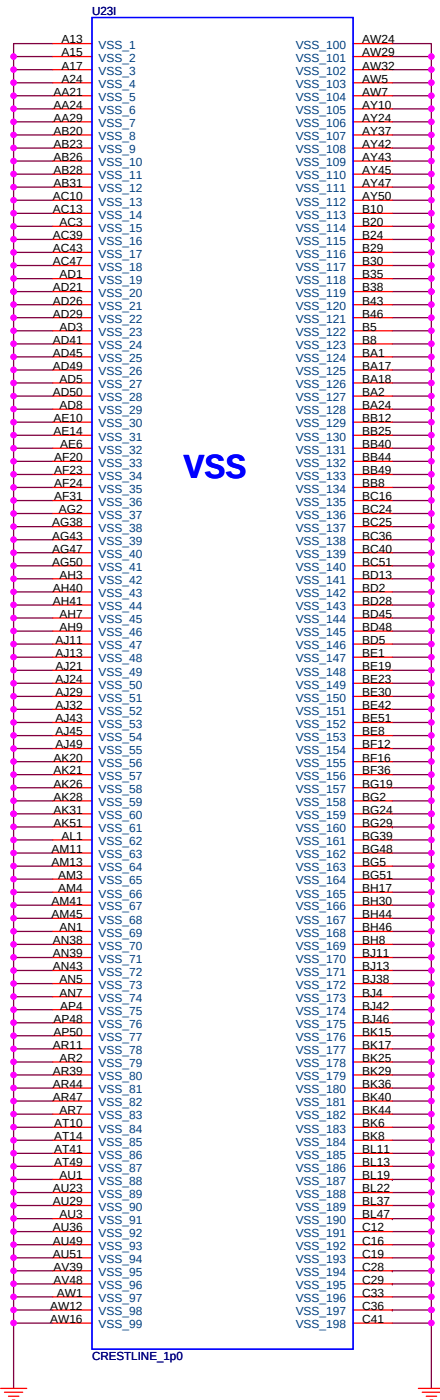


PROJECT : SW7
Quanta Computer Inc.









PROJECT : SW7
Quanta Computer Inc.

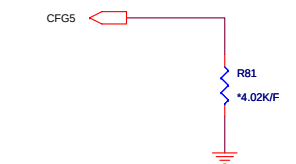
Size	Document Number	Rev
	CRESTLINE (VSS)	1A
Date:	Friday, September 28, 2007	Sheet 11 of 44

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)
-----------	---------------------------------------



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--

XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

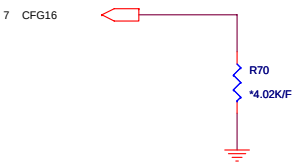
MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

SDVO Present

Strap define at External DVI control page

FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
------------	---





PROJECT : SW7
Quanta Computer Inc.

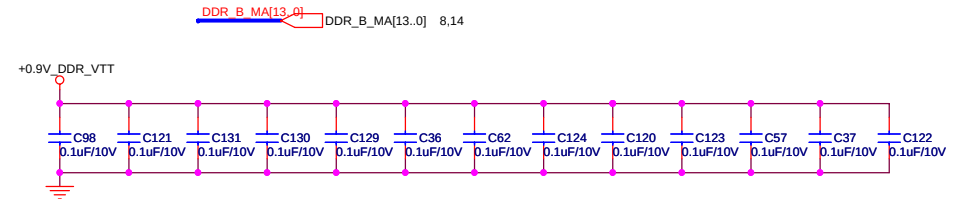
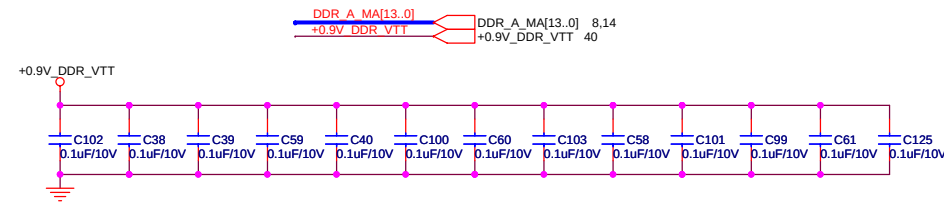
Size	Document Number	Rev
	GMCH STRAP	1A
Date:	Friday, September 28, 2007	Sheet 12 of 44

DDRII DUAL CHANNEL A, B.

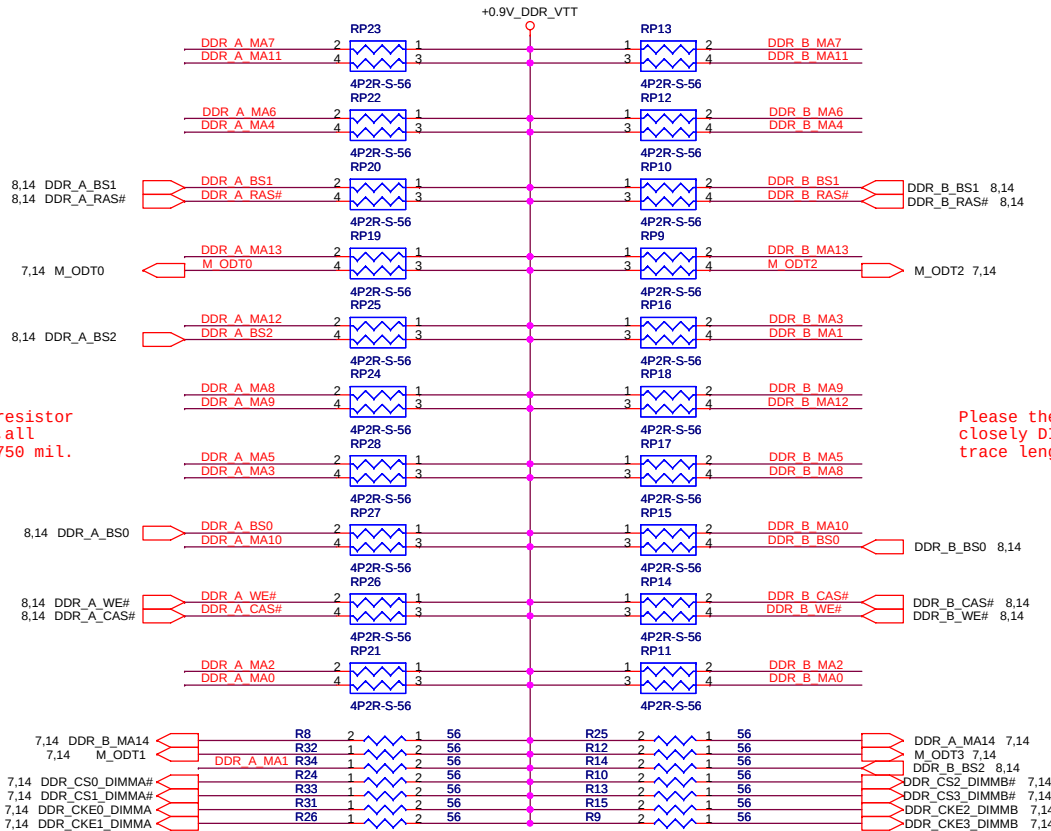
13

DDRII A CHANNEL

DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR_VTERM

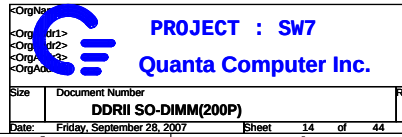


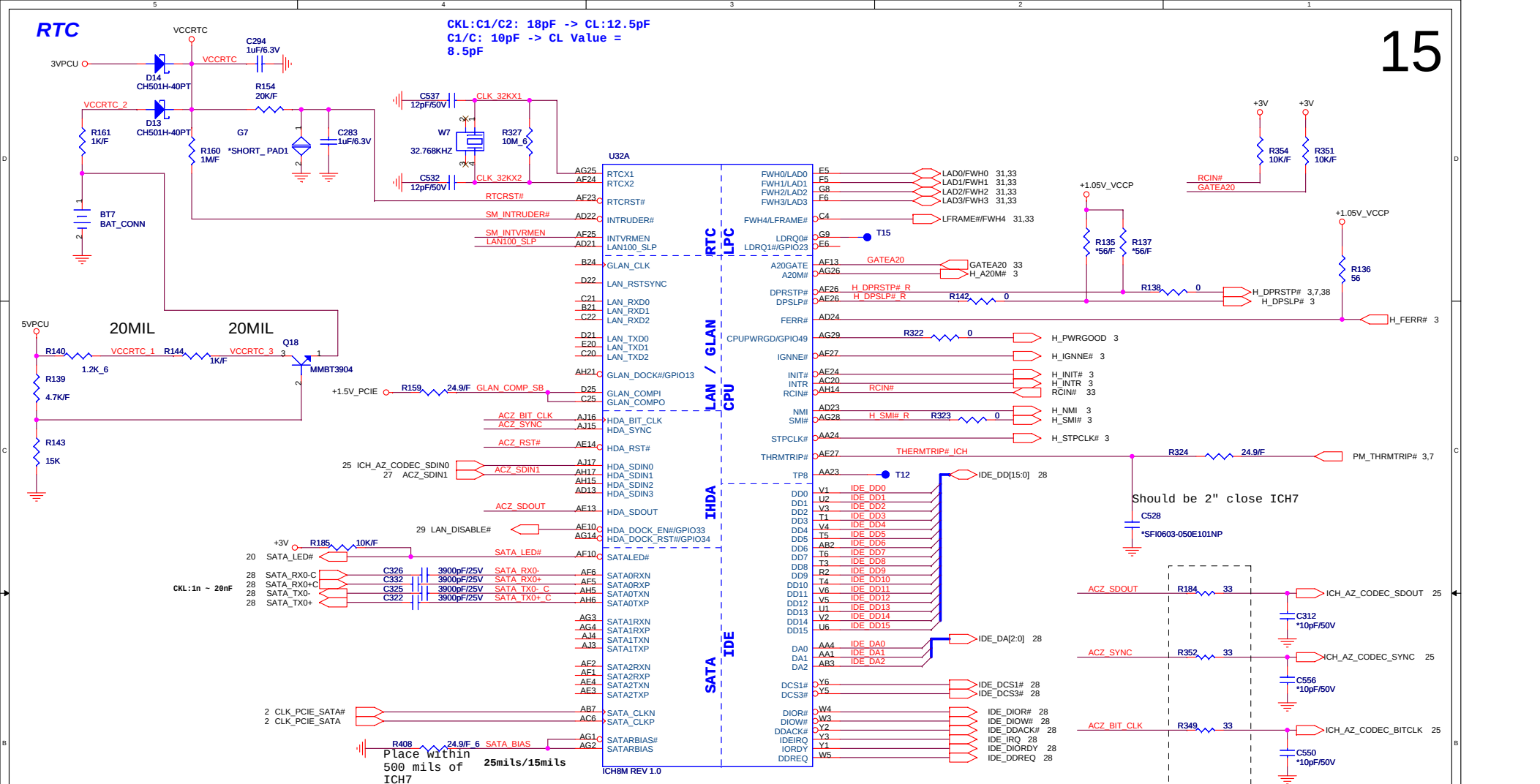
Please these resistor
closely DIMMA,all
trace length<750 mil.

Please these resistor
closely DIMMB,all
trace length<750 mil.

PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	DDRII RES.ARRAY	1A
Date:	Friday, September 28, 2007	Sheet 13 of 44





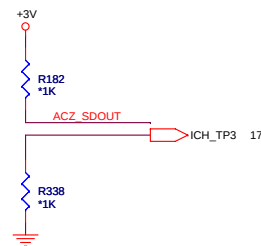
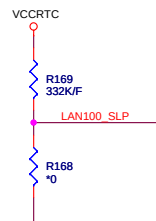
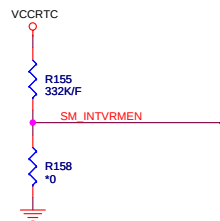
SB Strap

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

**ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and
VccCL1.05)**

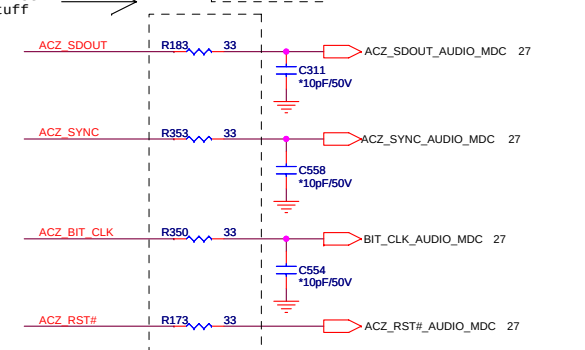
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---



XOR Chain Entrance Strap

ICH_RSVD0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

```
intel check list
define to stuff
33ohm
```



PROJECT : SW7
Quanta Computer Inc.

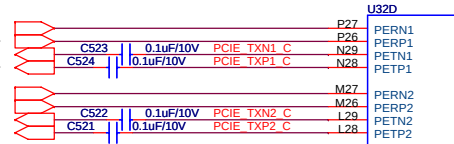
Size	Document Number	Rev
	ICH8-M HOST(1/4)	1A
Date:	Friday, September 28, 2007	Sheet 15 of 44

MINI CARD WLAN PCI-E

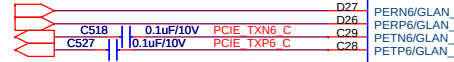
PCI-E-LAN

31 PCIE_RX1-
31 PCIE_RX1+
31 PCIE_TX1-
31 PCIE_TX1+

29 PCIE_RX2-
29 PCIE_RX2+
29 PCIE_TX2-
29 PCIE_TX2+



31 PCIE_RX6-
31 PCIE_RX6+
31 PCIE_TX6-
31 PCIE_TX6+



U32D
PERN1
PERP1
PETN1
PETP1

PERN2
PERP2
PETN2
PETP2

PERN3
PERP3
PETN3
PETP3

PERN4
PERP4
PETN4
PETP4

PERN5
PERP5
PETN5
PETP5

PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP

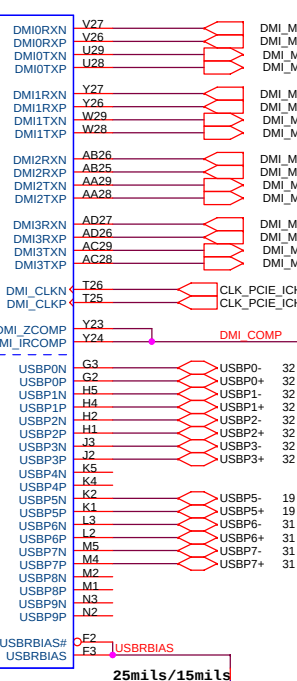
SPL_CLK
SPL_CS0#
SPL_CS1#

SPL_MOSI
SPL_MISO

USBOC#0
USBOC#1
USBOC#2
USBOC#3
USBOC#4
USBOC#5
USBOC#6
USBOC#7
USBOC#8
USBOC#9

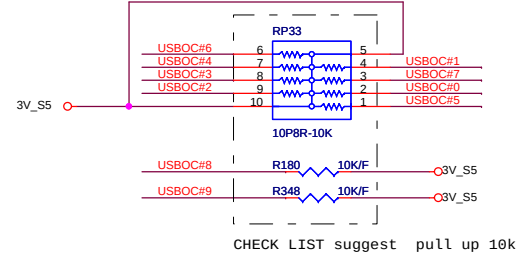
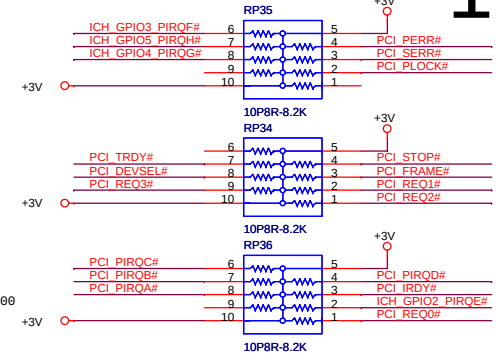
OC0#
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO44
OC6#/GPIO45
OC7#/GPIO46
OC8#
OC9#

USBRBIAS#
USBRBIAS



Ext Right Side Top
Ext Right Side
Ext Left Side
CAMERA
Dock
Bluetooth
Mini Card WLAN
Express Card

PCI Pullups



CHECK LIST suggest pull up 10k

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---

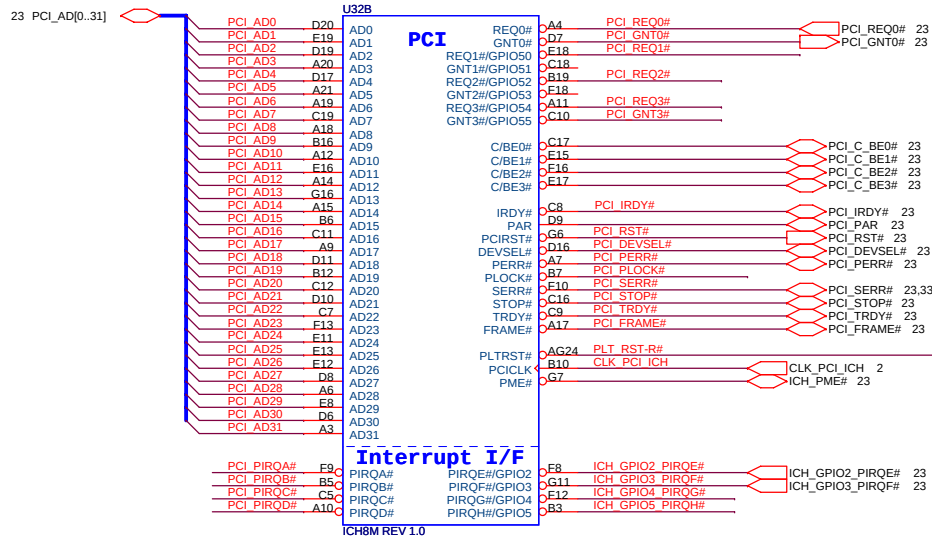


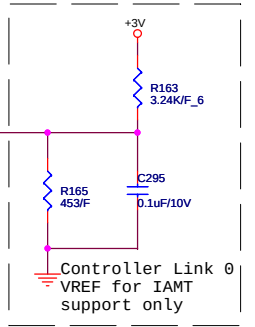
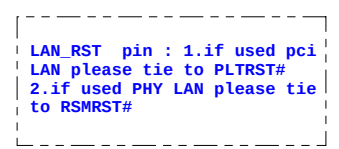
ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

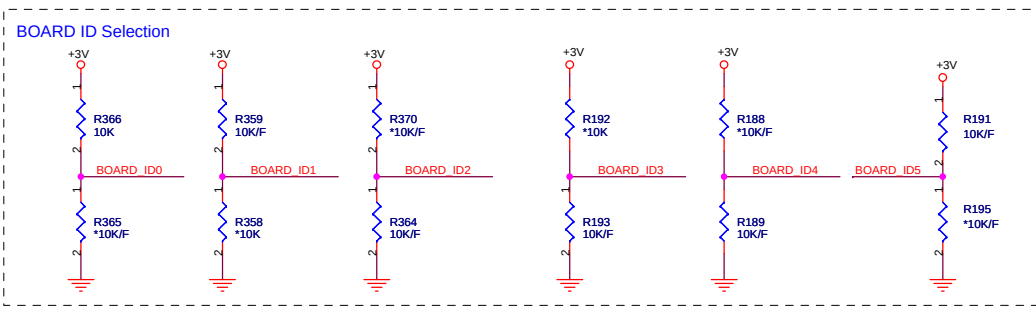


PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	PCI17402
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

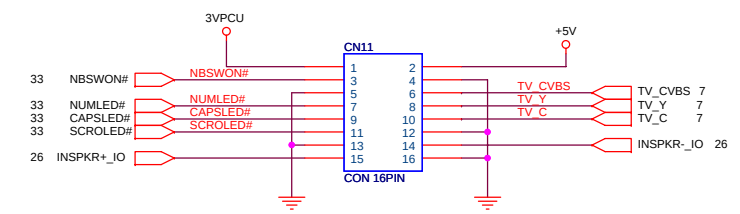
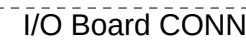
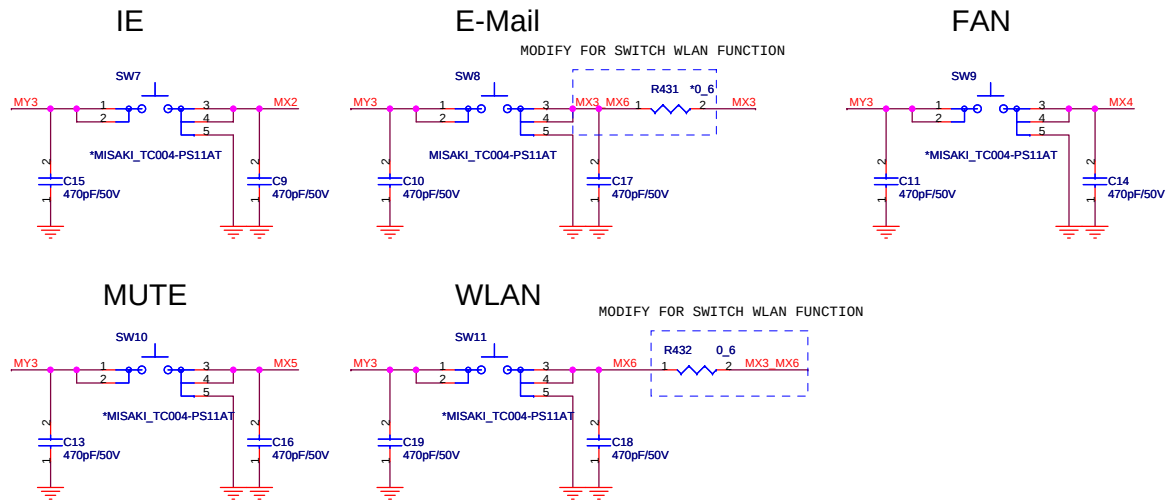
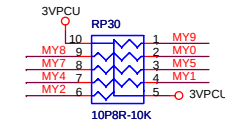
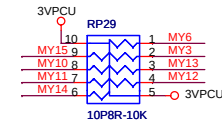
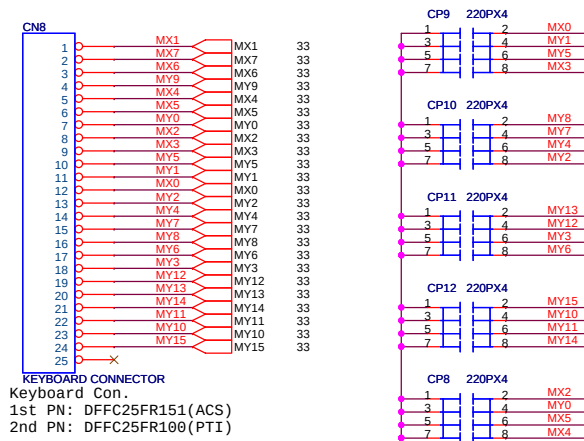
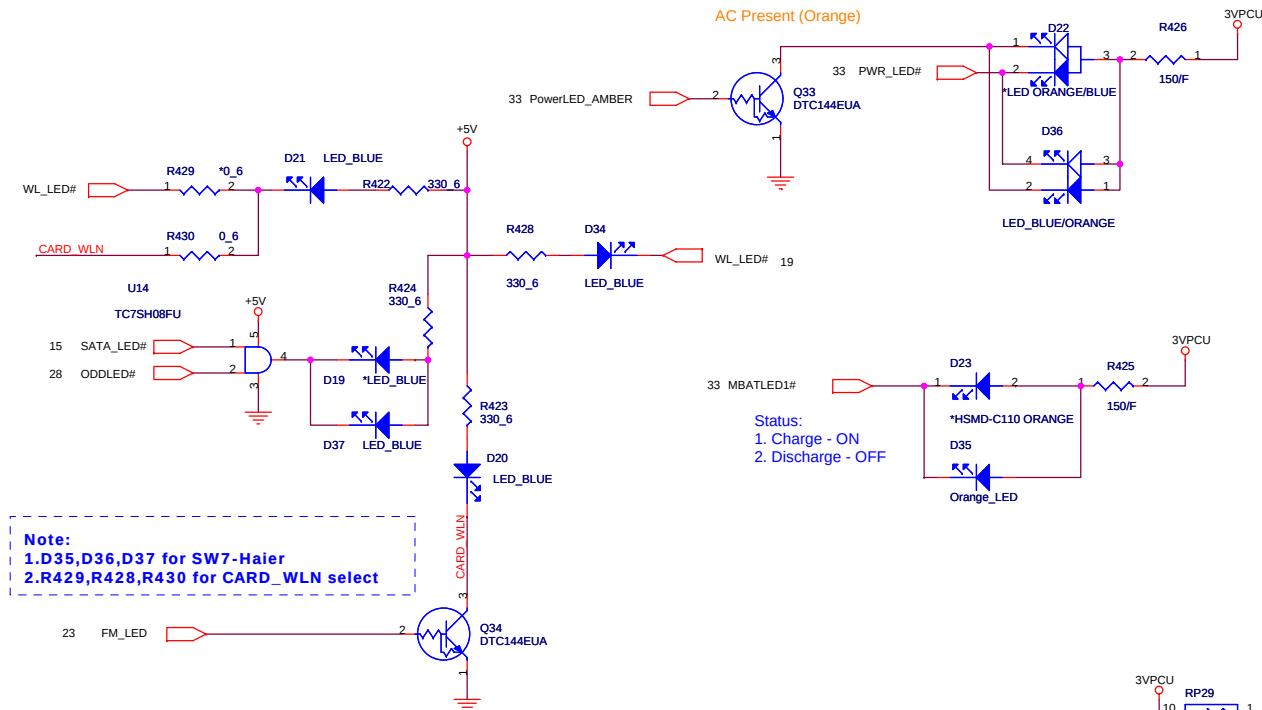


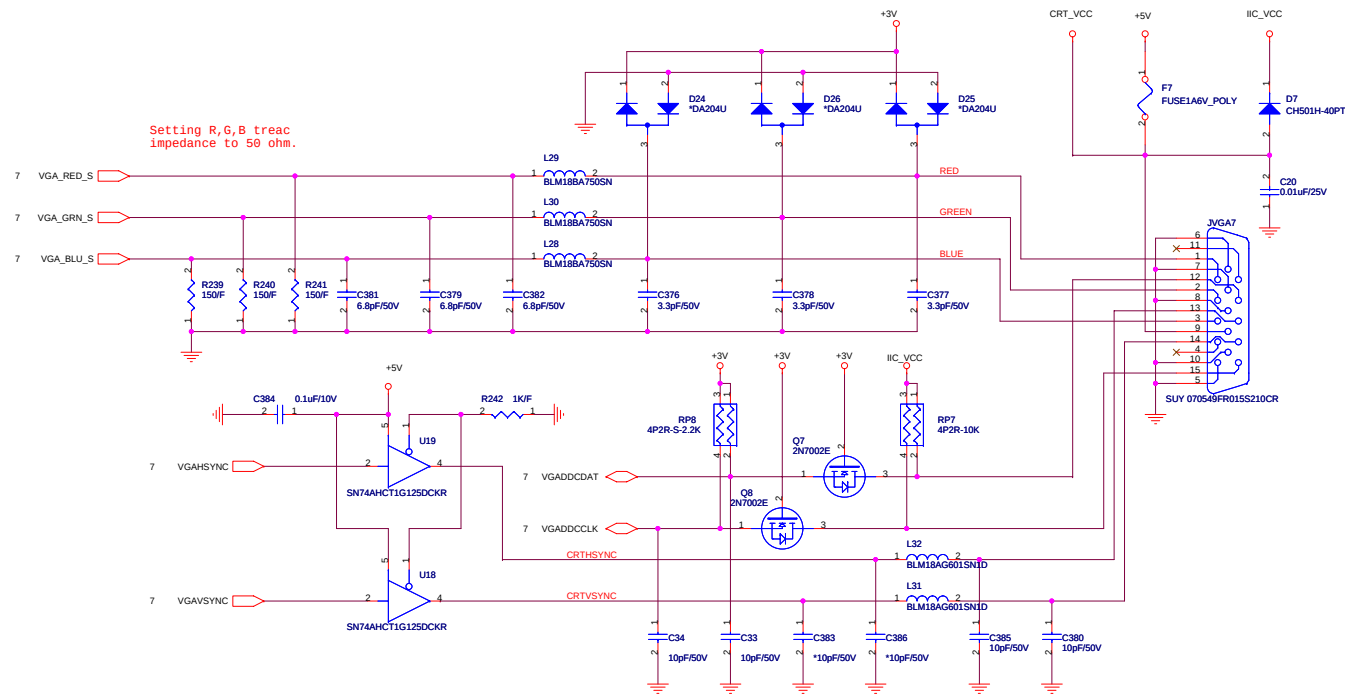


MBID5	
DVI	Low
CRT	High

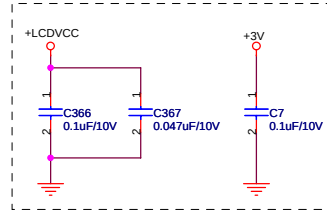
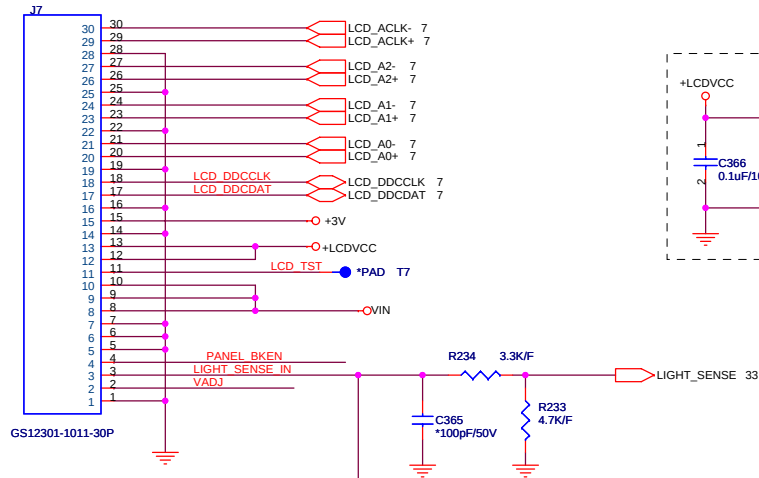


	PROJECT : SW7		
	Quanta Computer Inc.		
Size	Document Number		Rev
	ICH8-M GPIO(3/4)		1A
Date:	Friday, September 28, 2007	Sheet	17 of 44

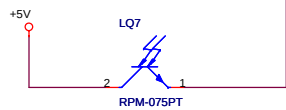




LCD CONNECTOR

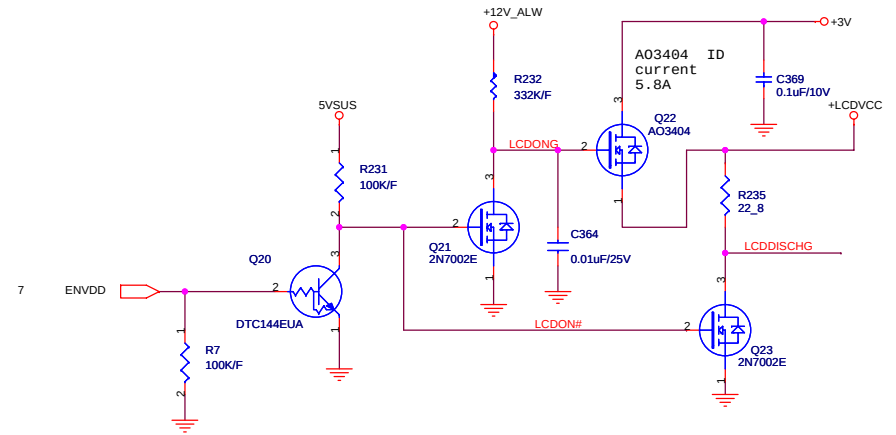
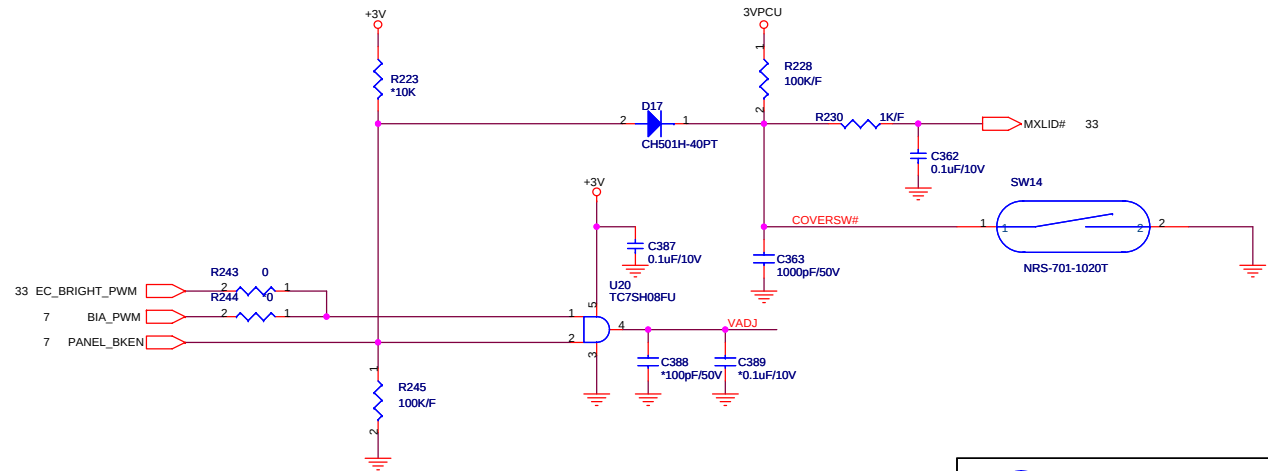
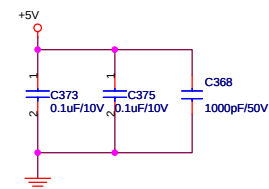


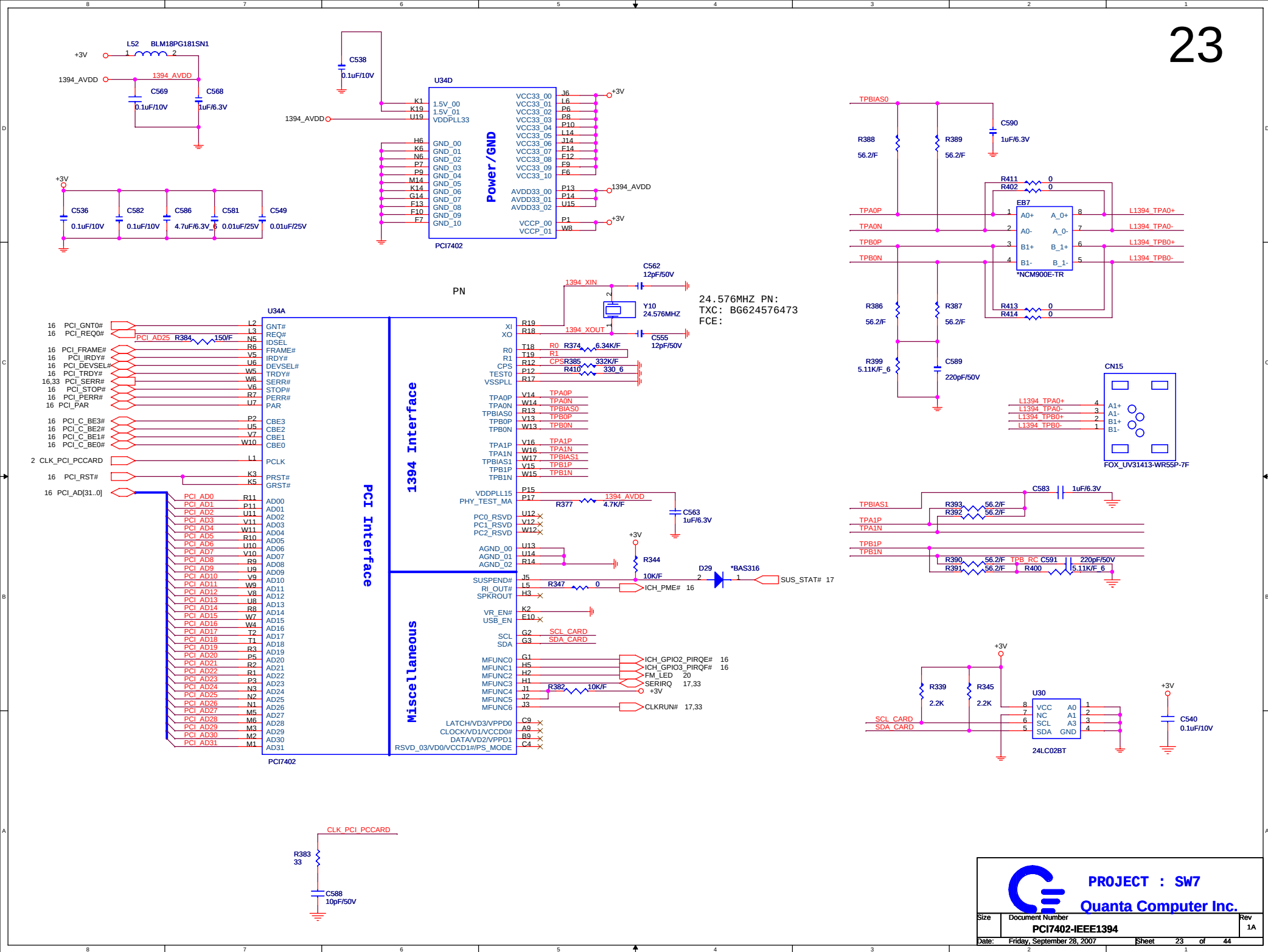
Light sensor

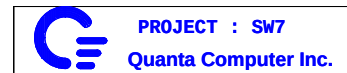
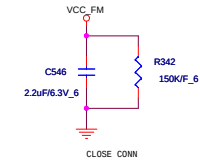


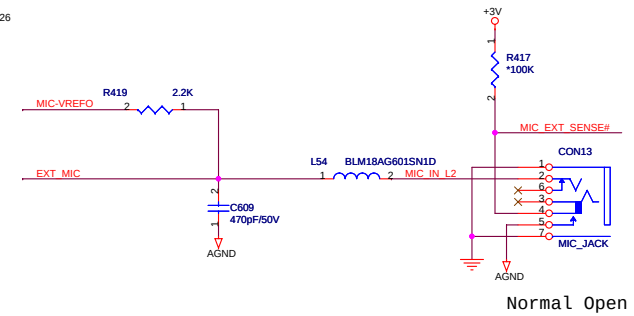
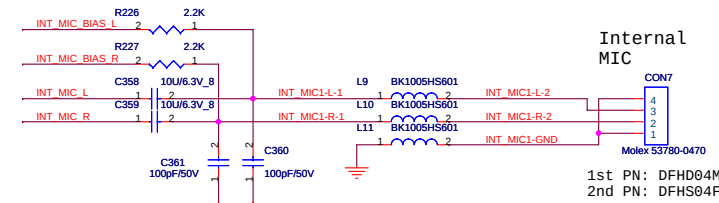
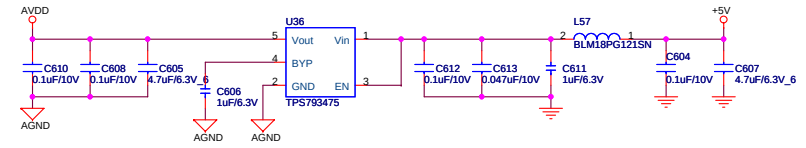
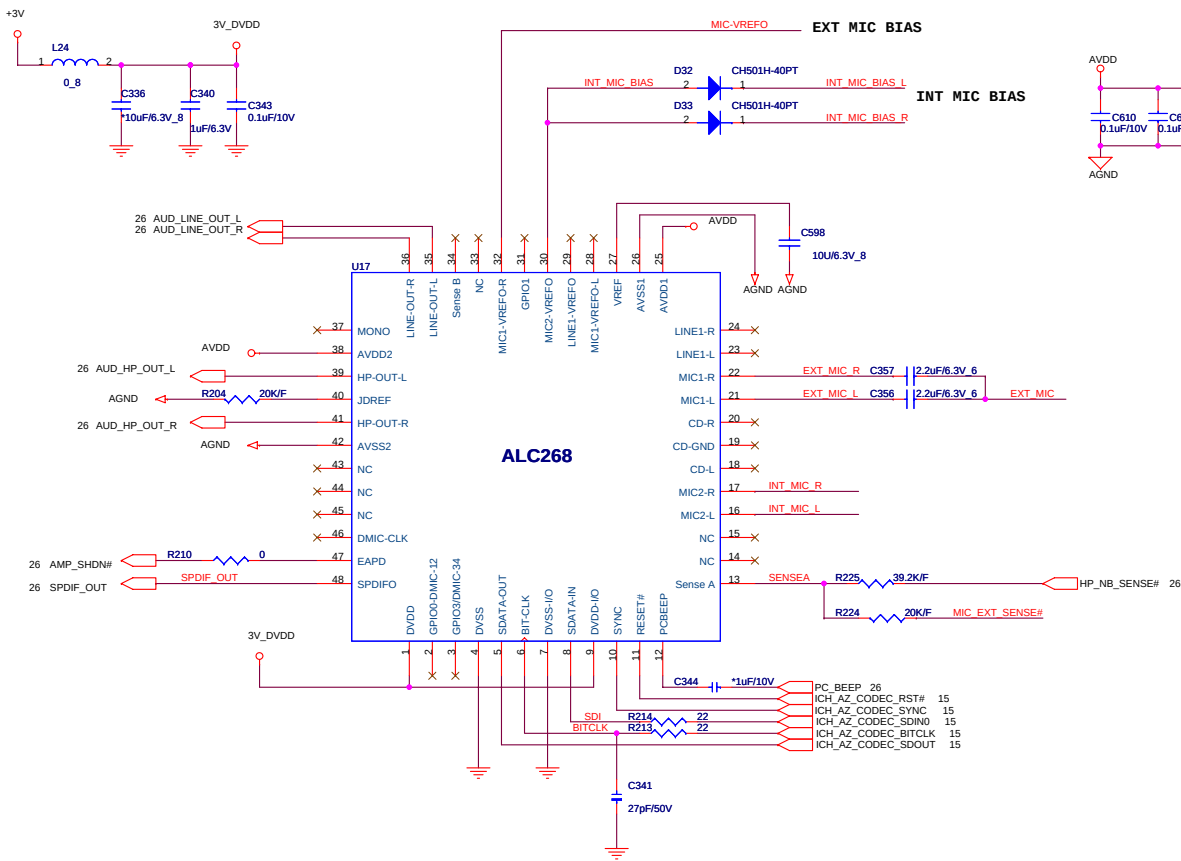
Pin 1: Emitter

Pin 2: Collector









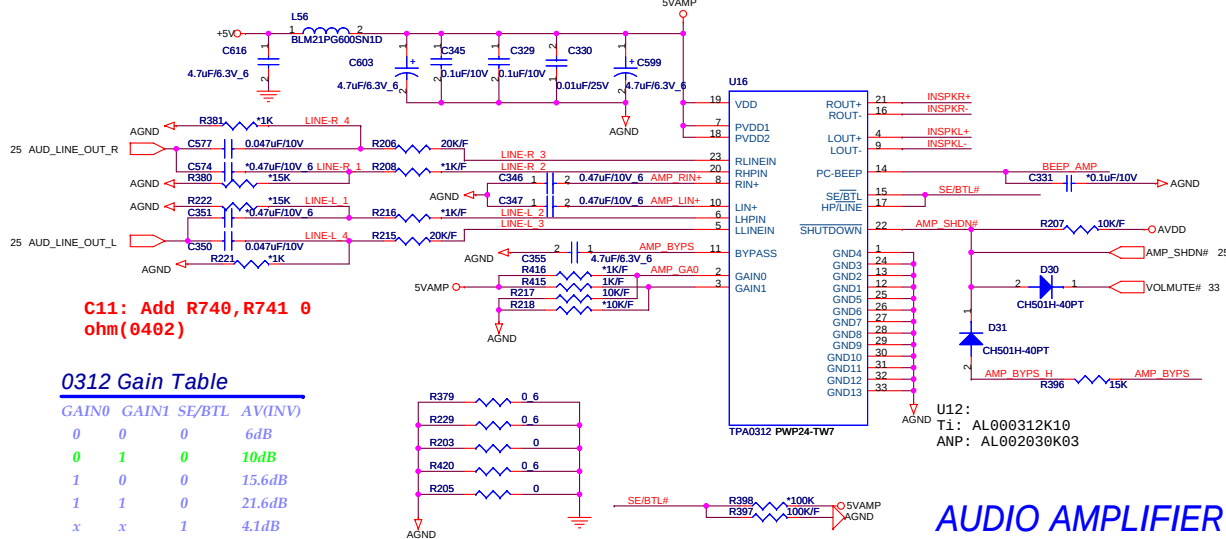
PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	Azalia ALC268	1A

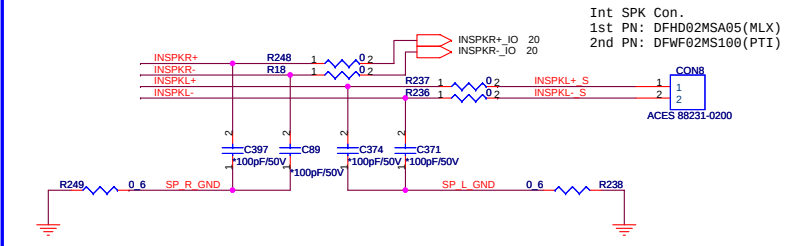
Date: Friday, September 28, 2007 Sheet 25 of 44



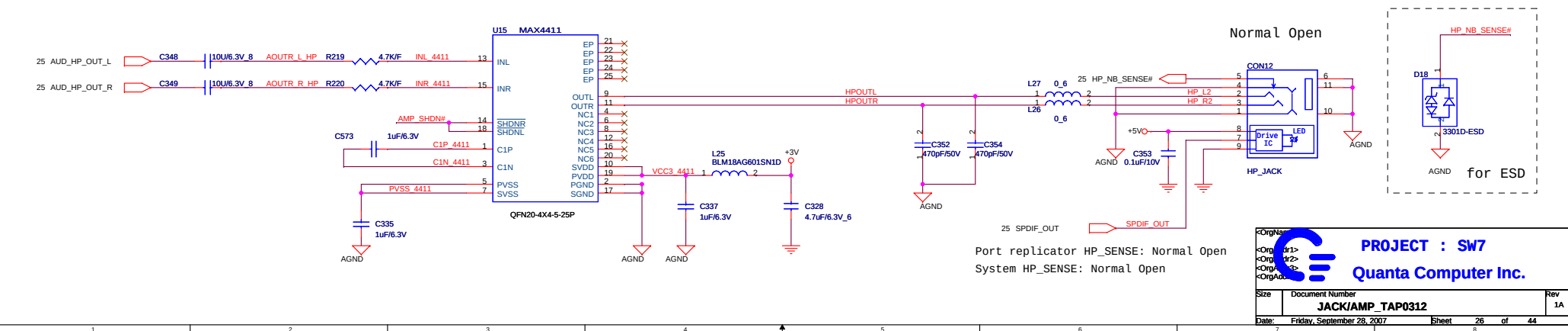
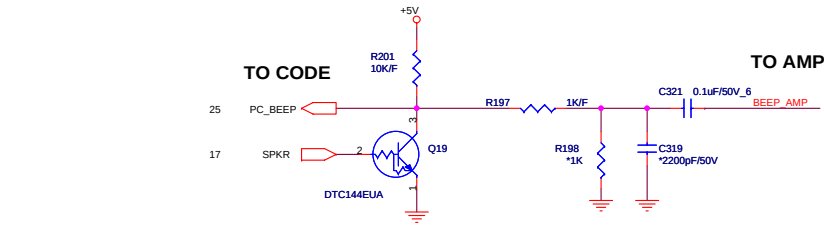
PROJECT : SW7
Quanta Computer Inc.



INT. SPEAKER



PCSPK BEEP



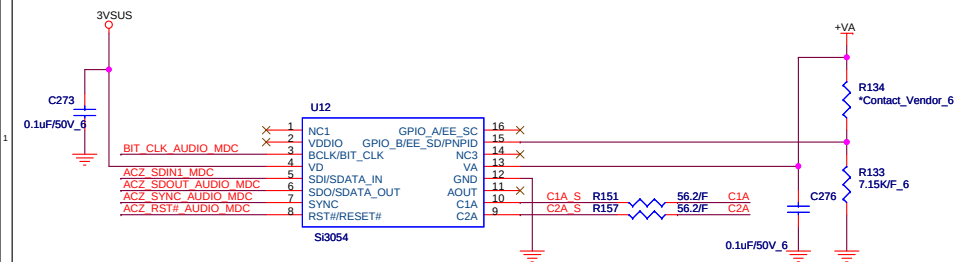
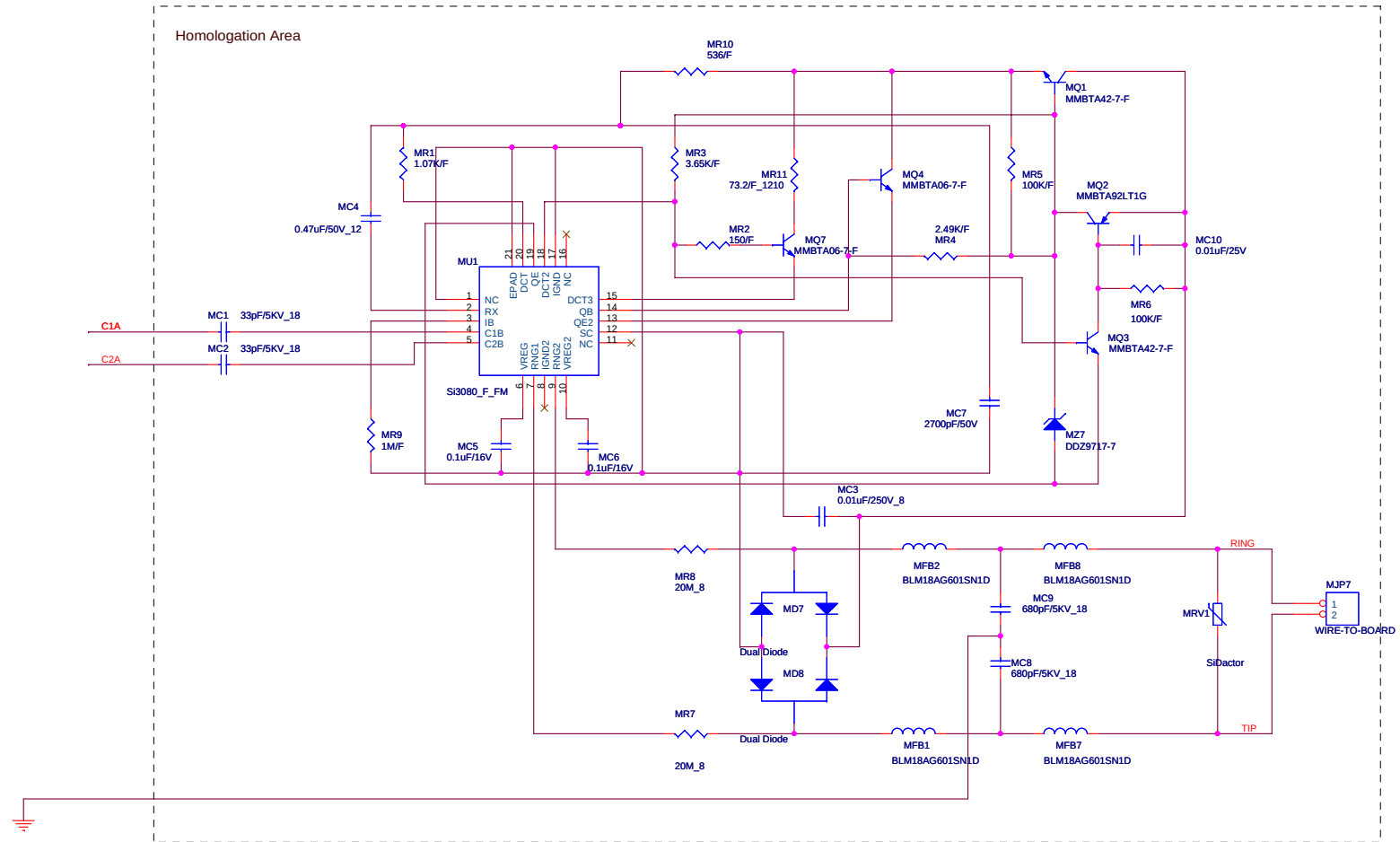
PROJECT : SW7
Quanta Computer Inc.

Size Document Number
JACK/AMP_TAP0312

Date: Friday, September 28, 2007 Sheet 26 of 44

Rev 1A

No Ground Plane In DAA Section

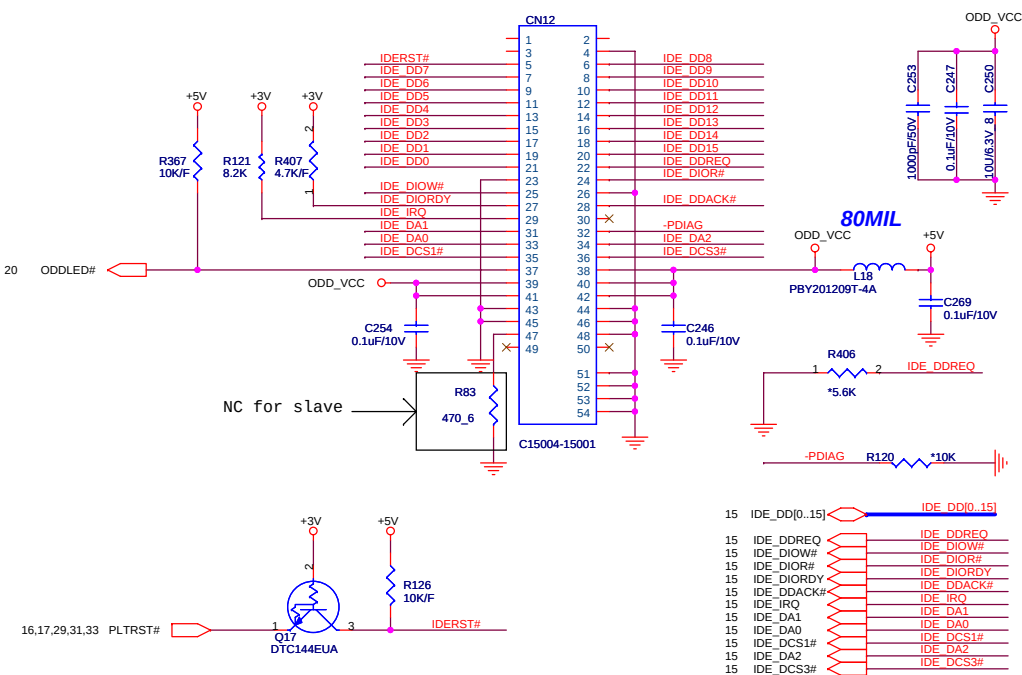


ACZ_RST#_AUDIO_MDC 15
 ACZ_SYNC_AUDIO_MDC 15
 BIT_CLK_AUDIO_MDC 15
 ACZ_SDOUT_AUDIO_MDC 15
 ACZ_SDIN1_MDC R147 33
 ACZ_SDIN1 15

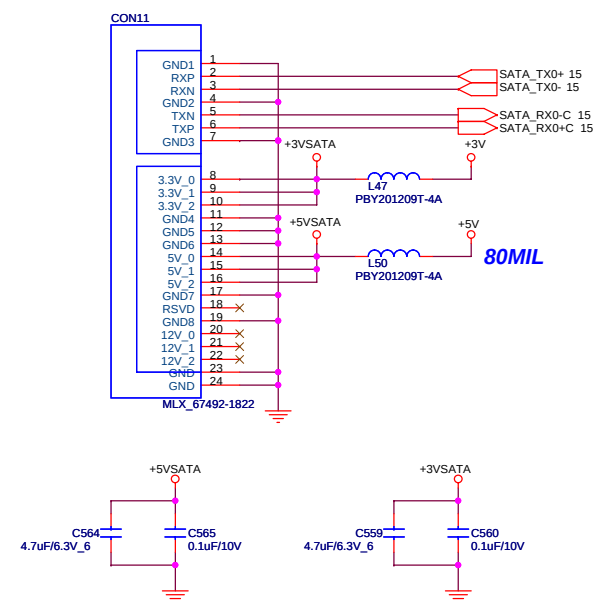
SILICON LABORATORIES CONFIDENTIAL

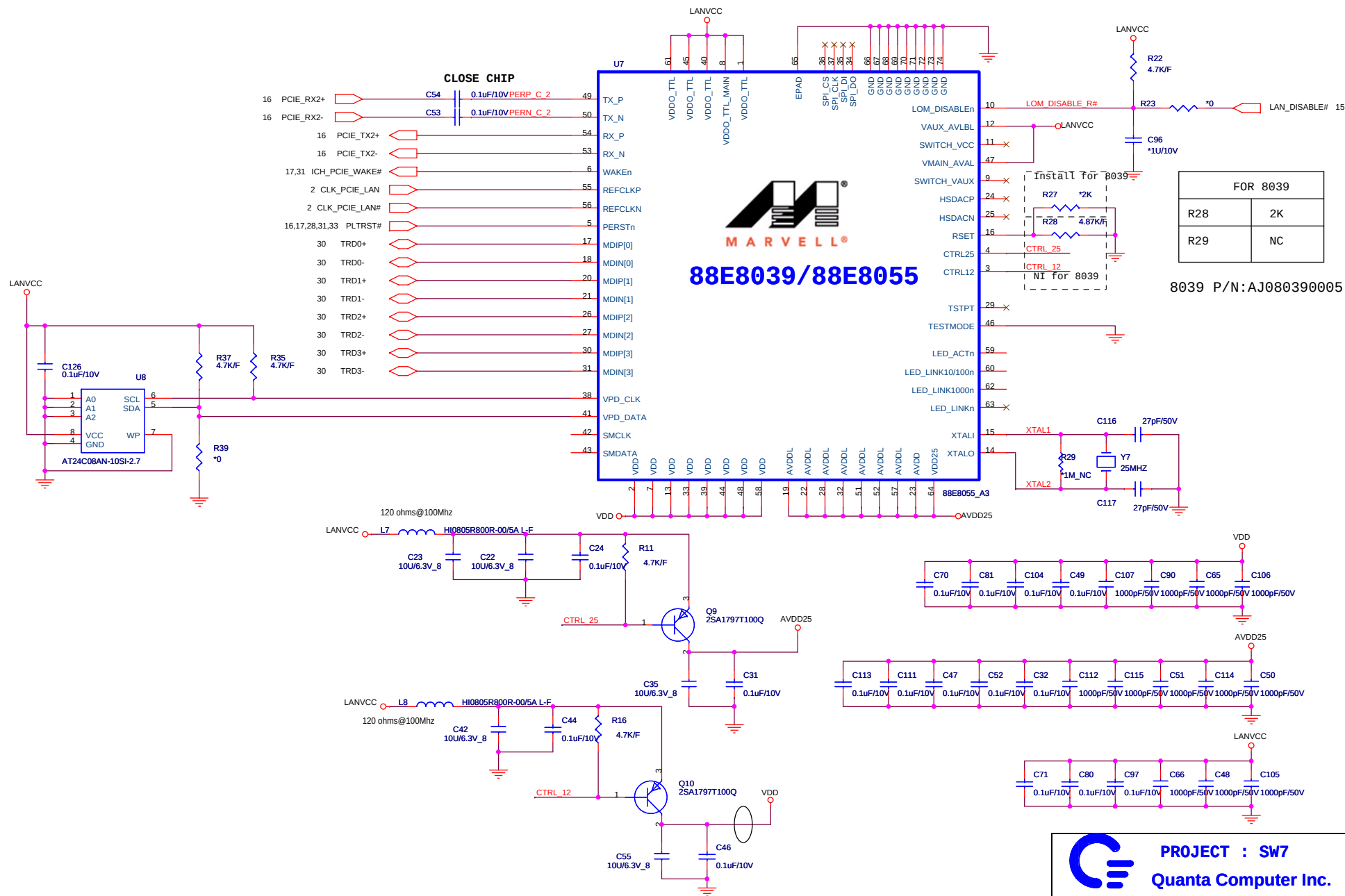
		PROJECT : SW7	
		Quanta Computer Inc.	
Size	Document Number	Rev 1A	
MODEM(DAA)			
Date:	Friday, September 28, 2007	Sheet	27 of 44

ODD CONNECTOR

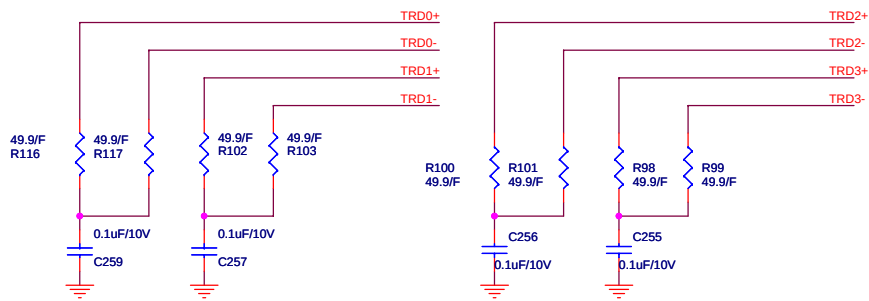
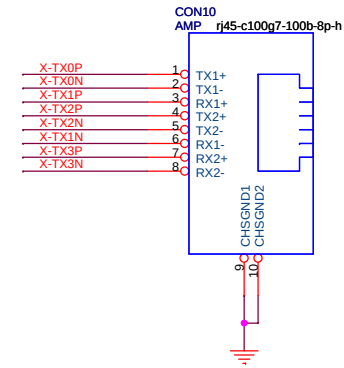
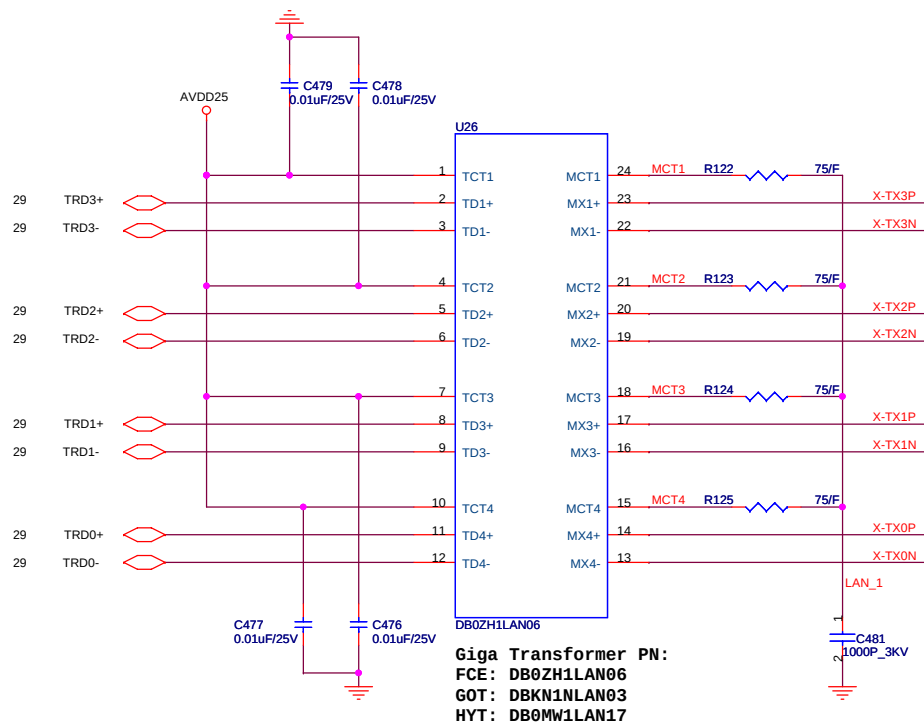


SATA Connector.

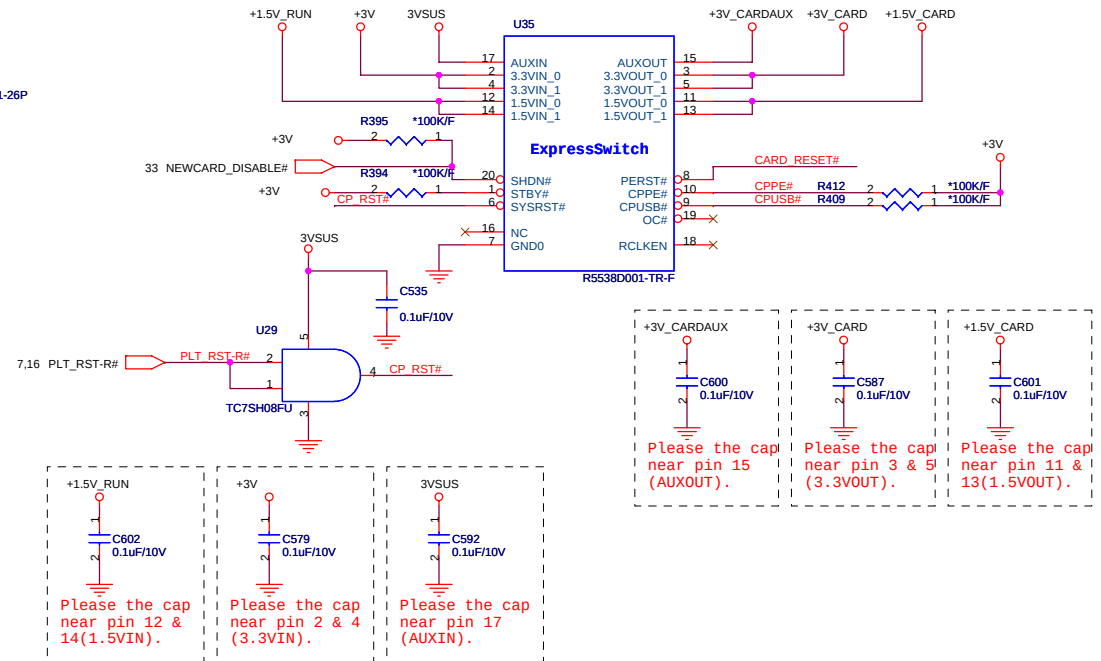
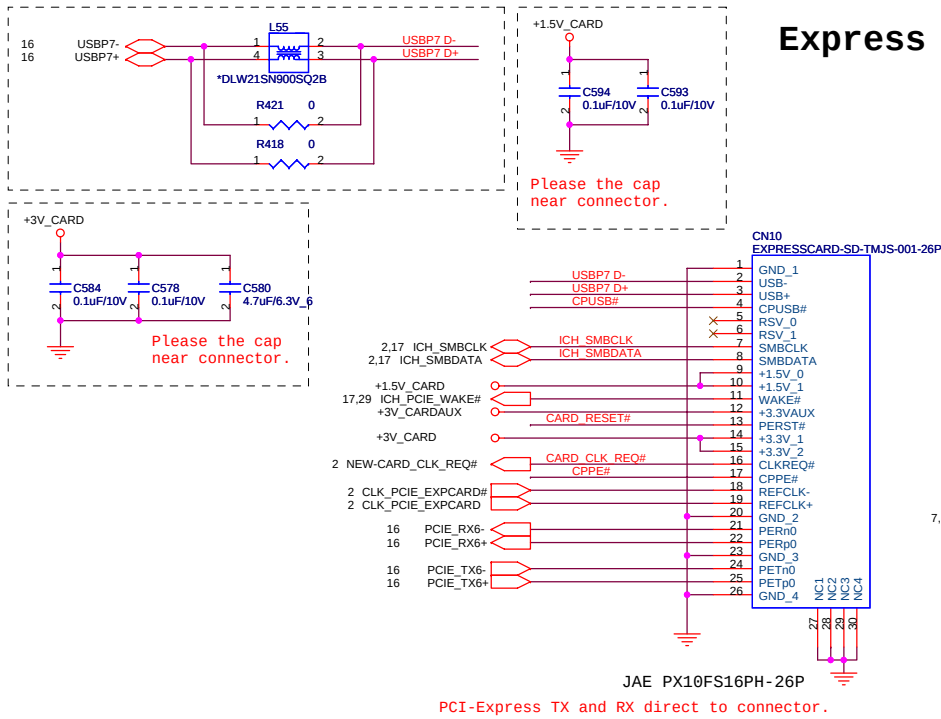




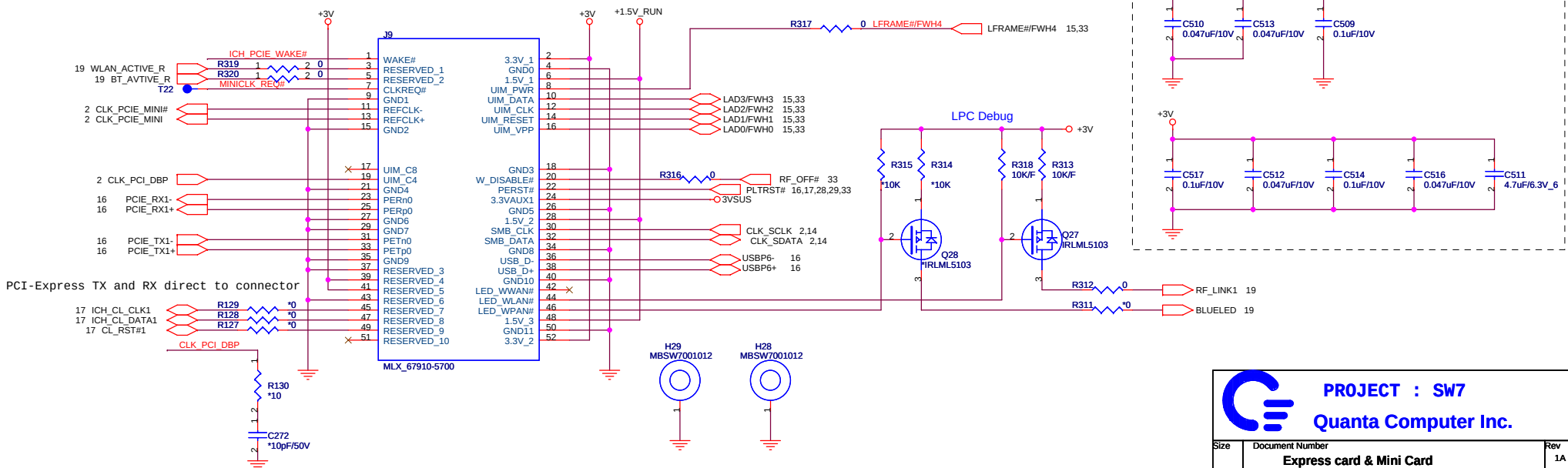
PROJECT : SW7
Quanta Computer Inc.

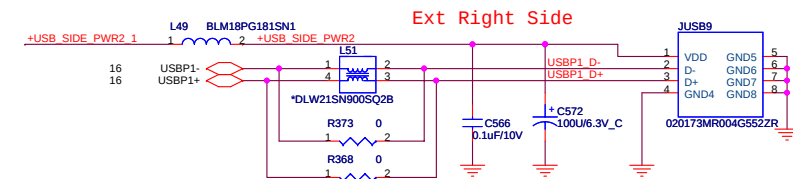
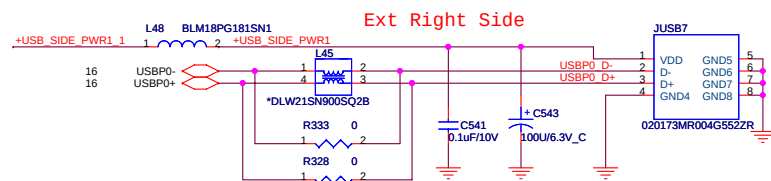
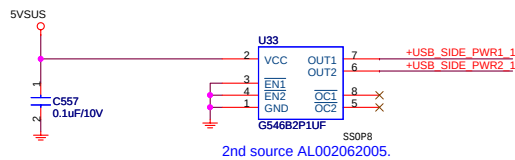


Express Card

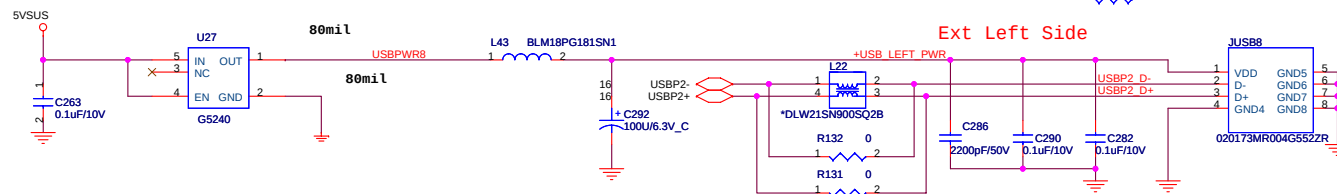


MiniCard WLAN connector

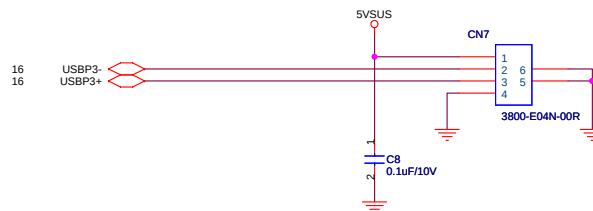


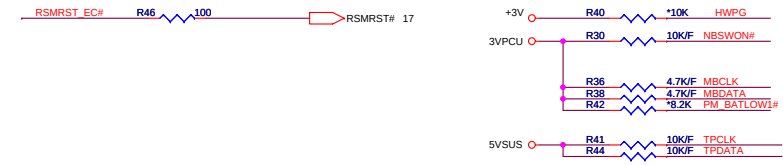
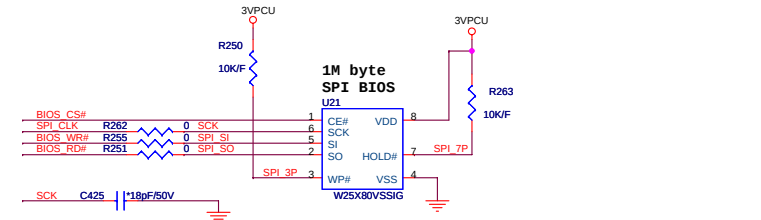
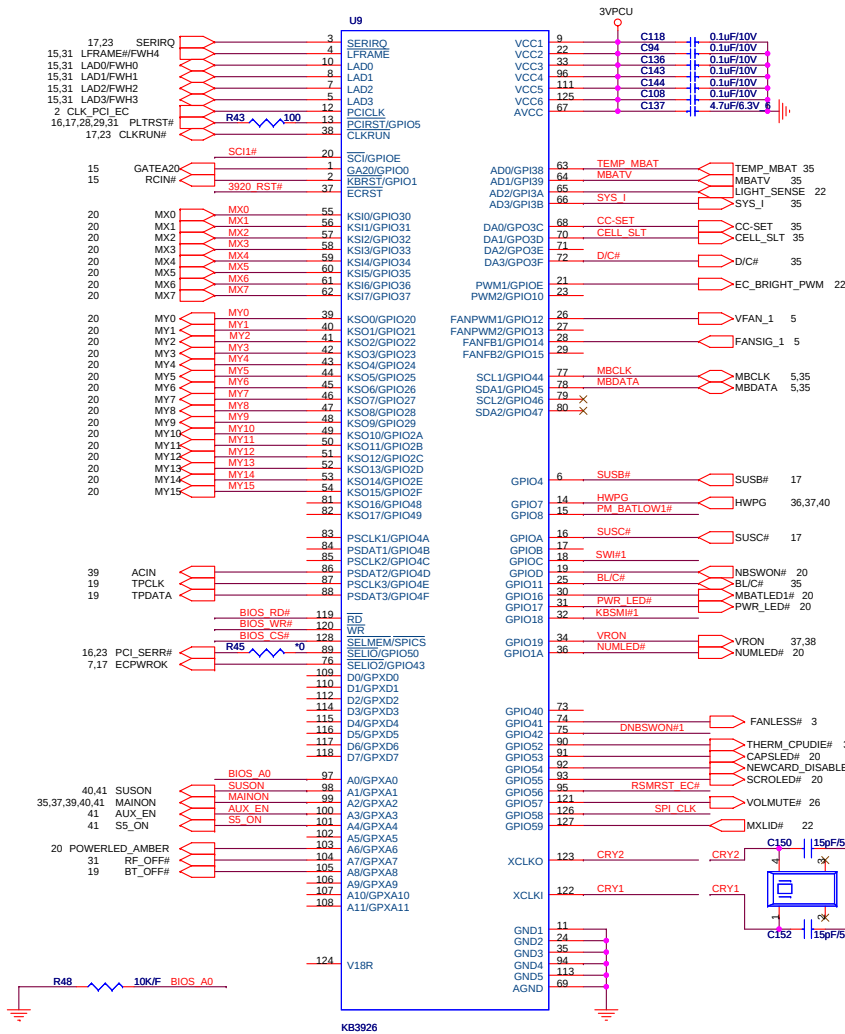


USB Con.
1st PN: DFHS04FR920(SUY)
2nd PN: DFHS04FRB11(A0P)



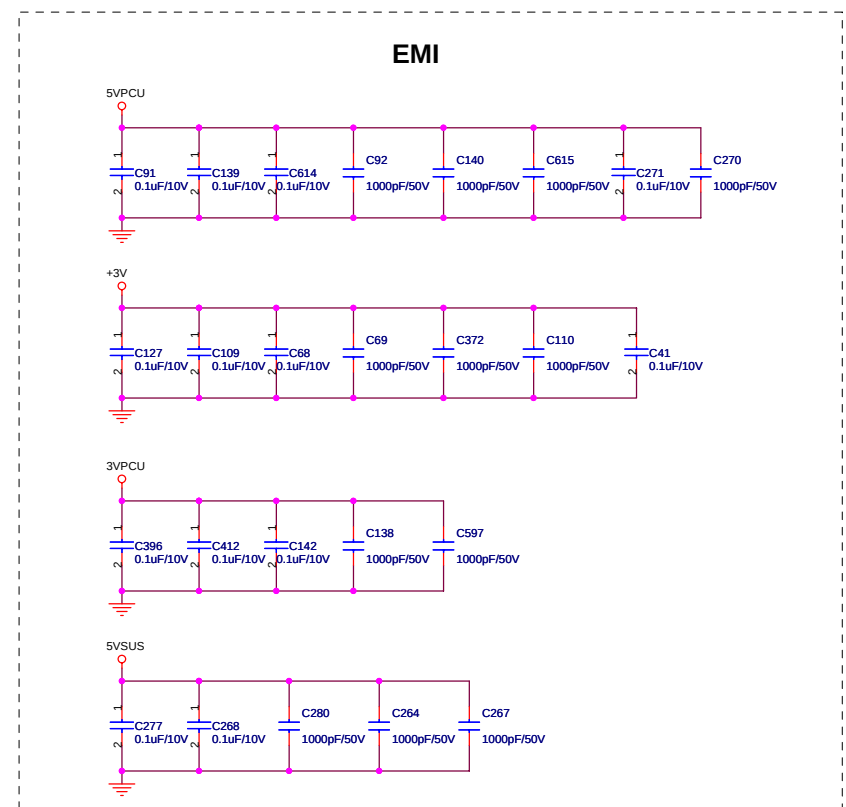
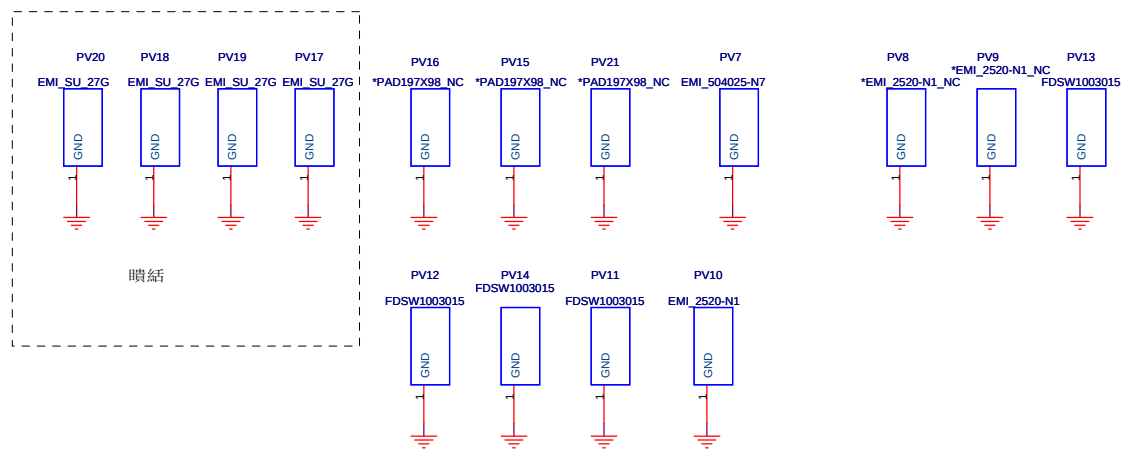
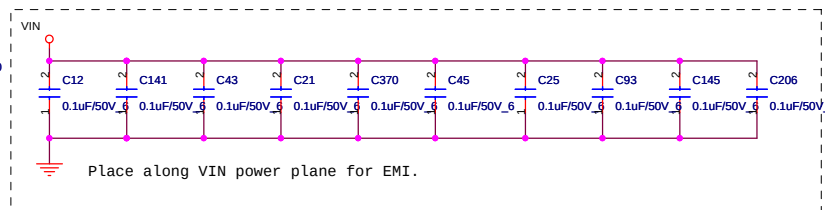
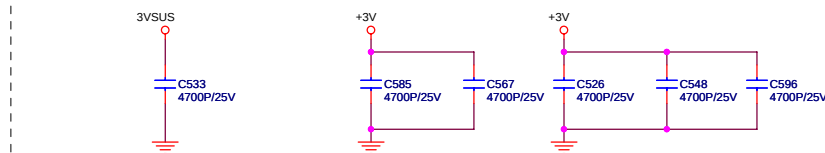
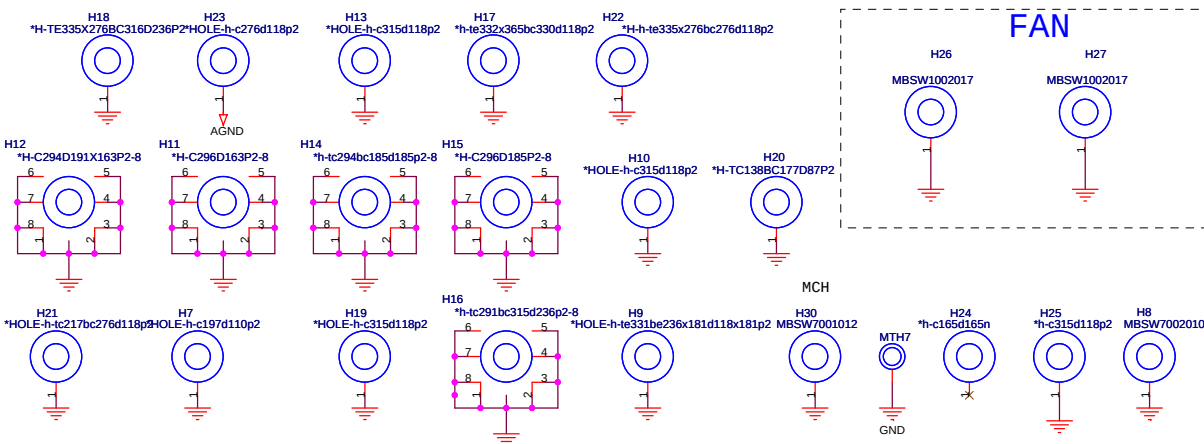
Int USB Con.
1st PN: DFHD04MR876(EIC)
2nd PN: DFHD04MR981(PTI)



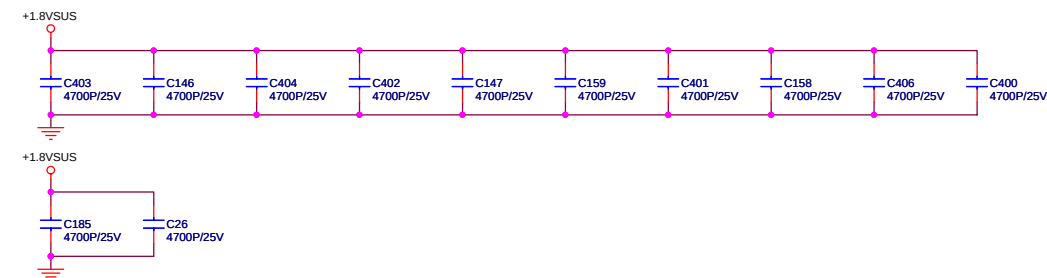


PROJECT : SW7
Quanta Computer Inc.

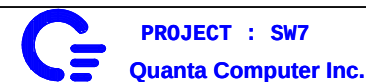
Size	Document Number	Rev
	KB3926/ROM	1A
Date:	Friday, September 28, 2007	Sheet 33 of 44



EMI for DDR DIMM.



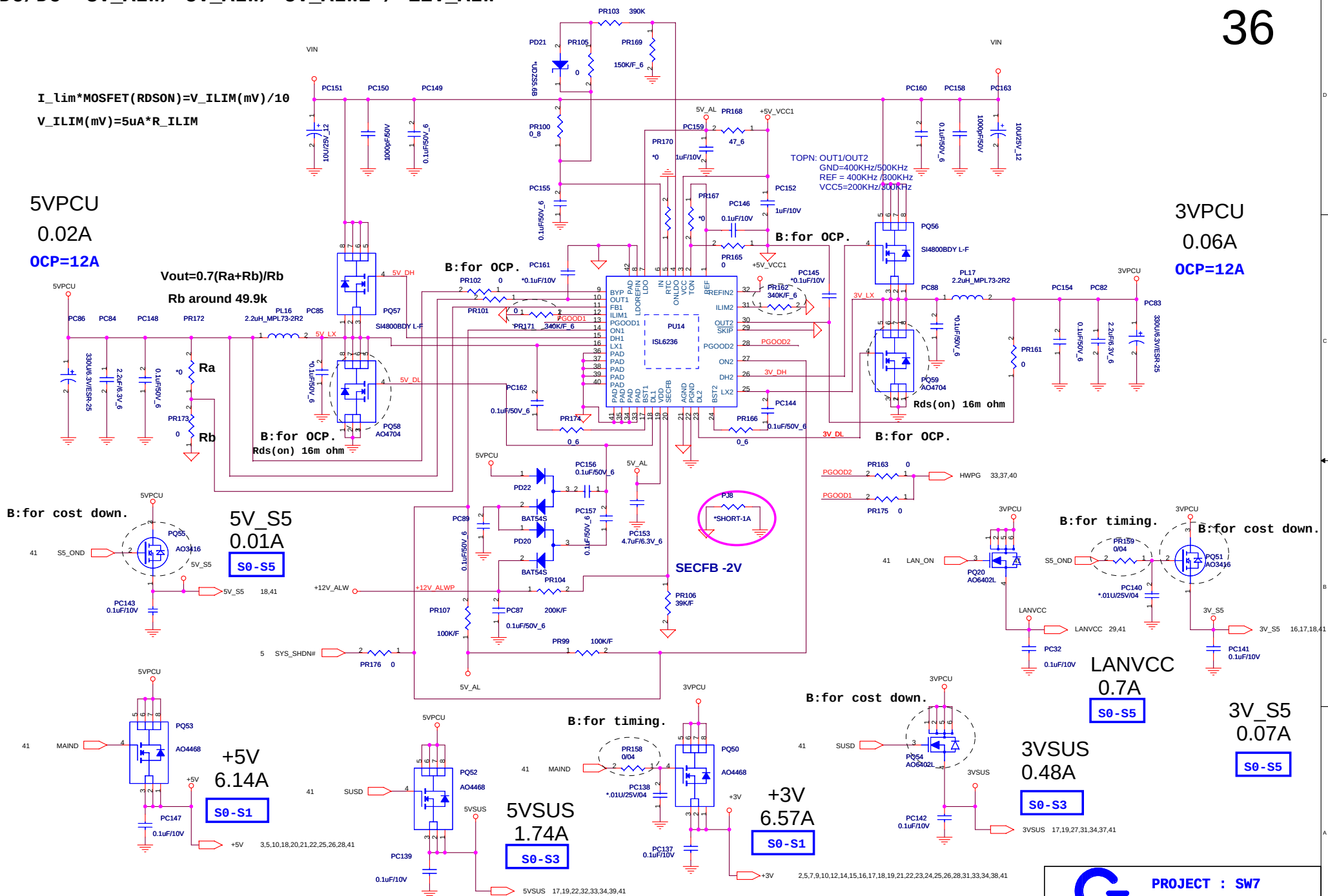
35



Size	Document Number	Rev
	SYSTEM CHARGER (MAX8724)	1
Date:	Friday, September 28, 2007	Sheet 35 of 44

5VPCU
0.02A
OCP=12A

3VPCU
0.06A
OCP=12A

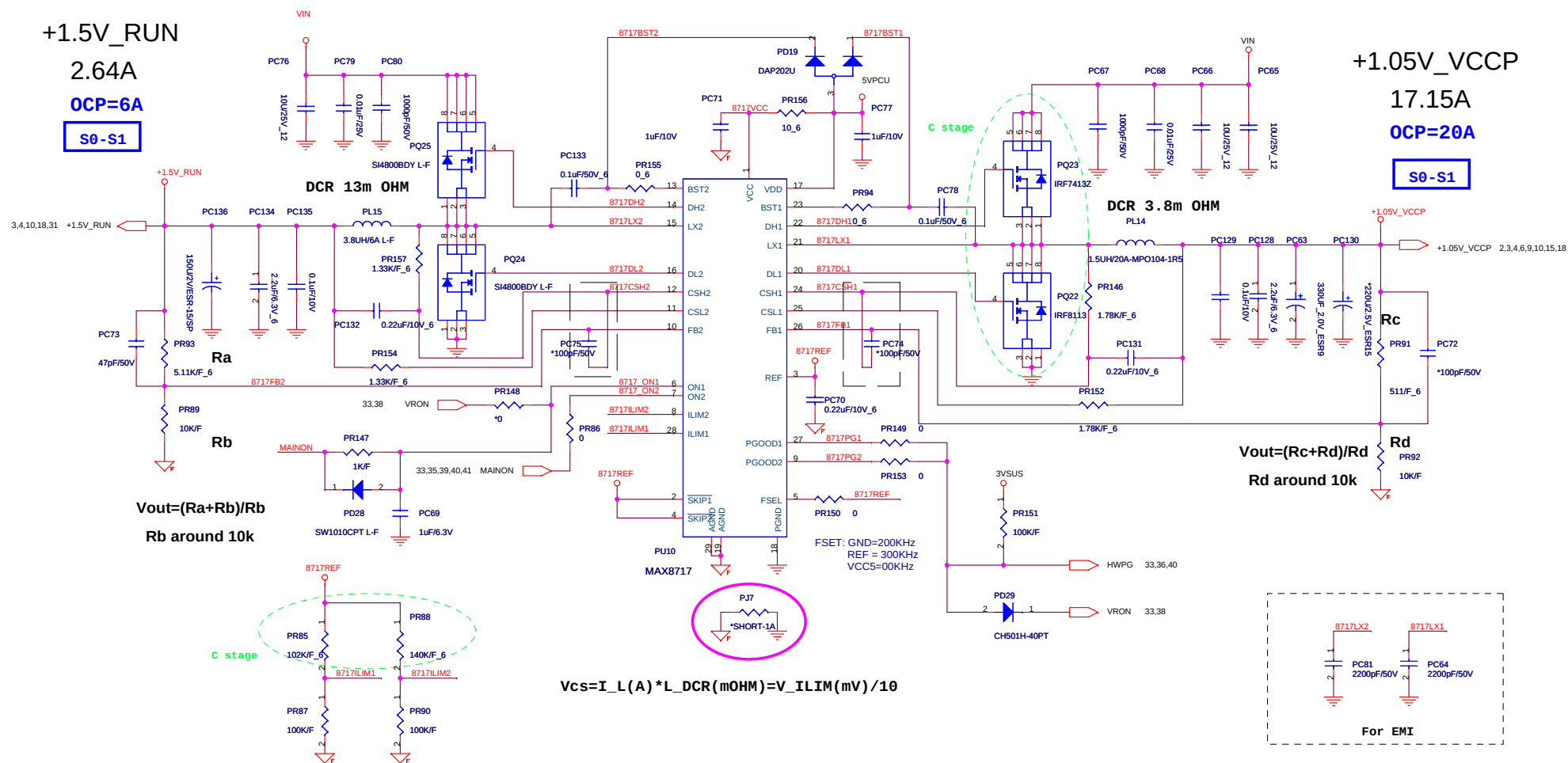


+1.5V RUN

2.64A

OCP=6A

S0-S1



+1.05V VCCP

17.15A

OCP=20A

S0-S1

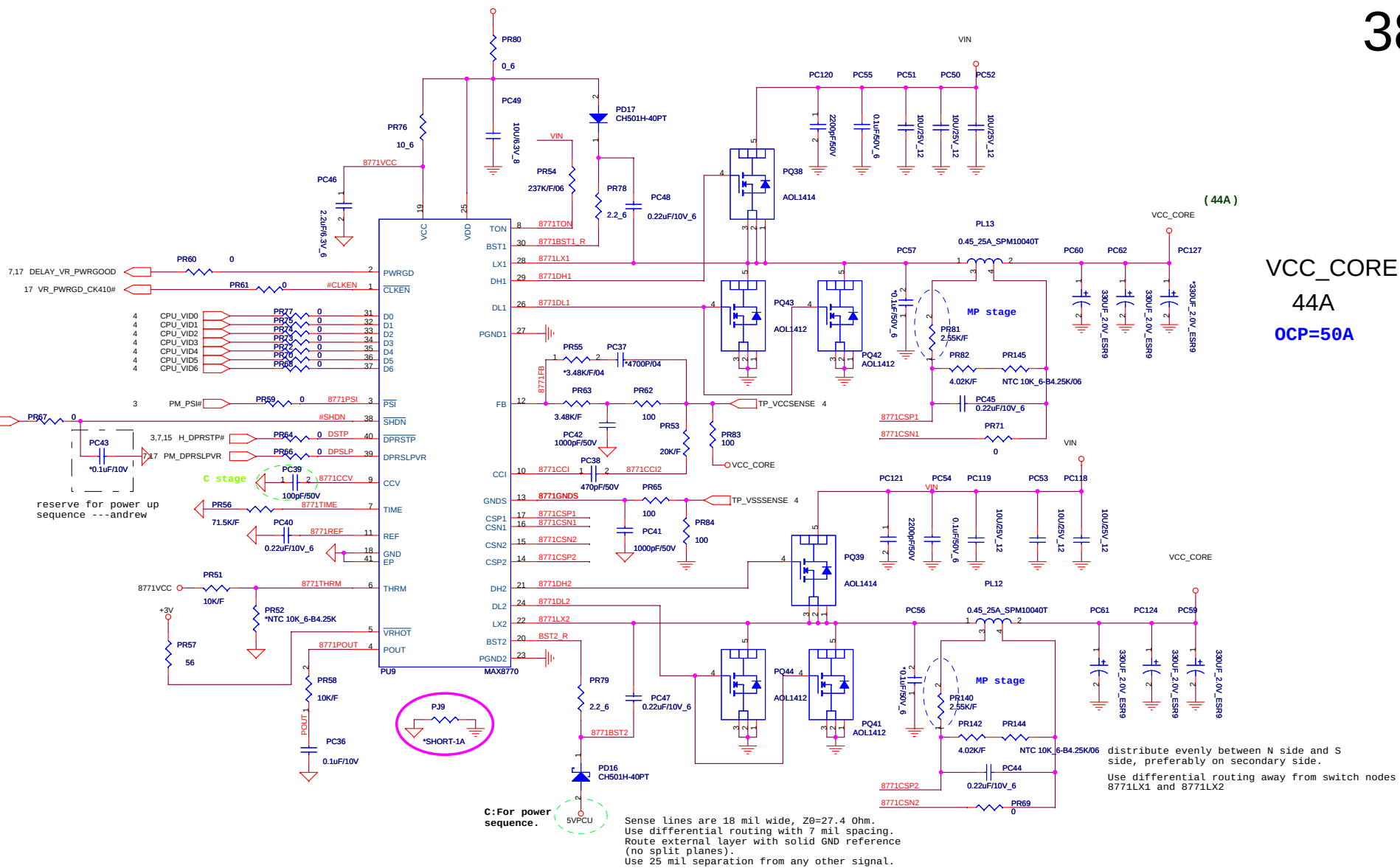
$V_{out} = (R_c + R_d) / R$
 R_d around 10k

For EMI

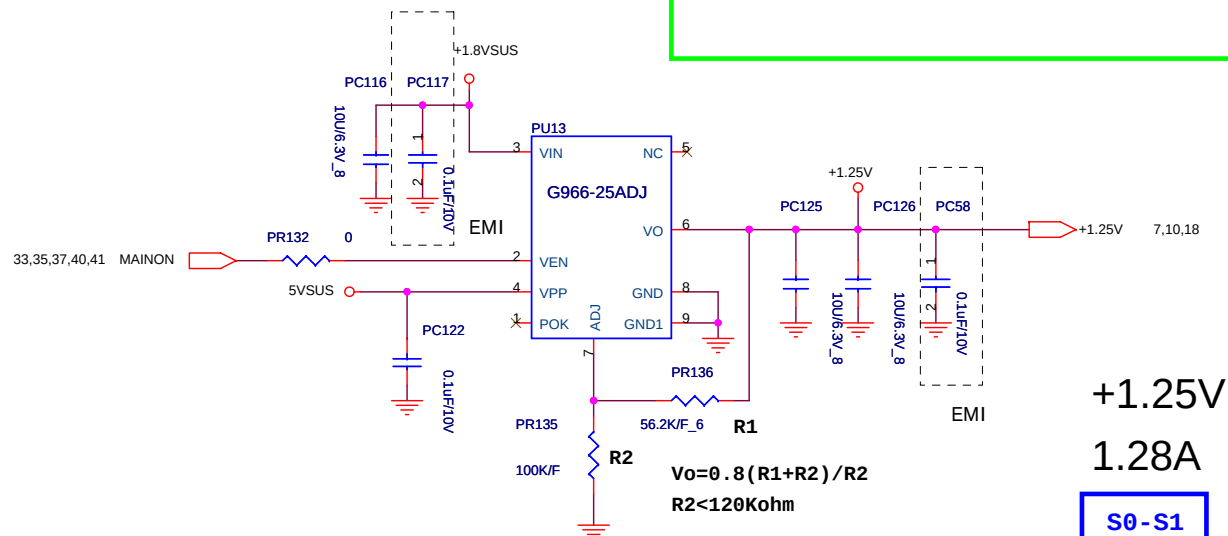
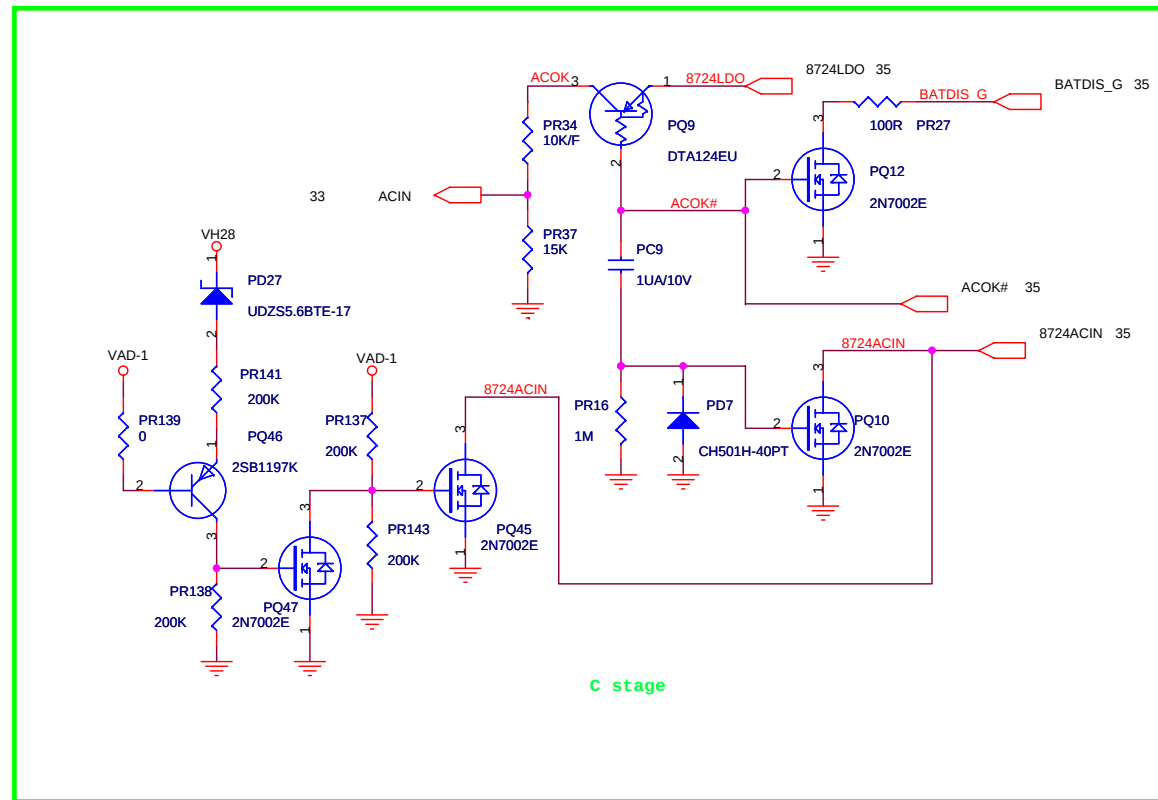


PROJECT : SW7
Quanta Computer Inc.

Size	Document Number	Rev
	+1.5V_RUN/+1.05V_VCCP (MAX8717)	1
Date:	Friday, September 28, 2007	Sheet 37 of 44



Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.



+1.25V
1.28A

S0-S1


$$V_{TRIP}(mV) = R_{TRIP}(Kohm) * 10(uA)$$
$$I_{OCP} = V_{trip} / R_{ds_on} + I_{Ripple} / 2$$

