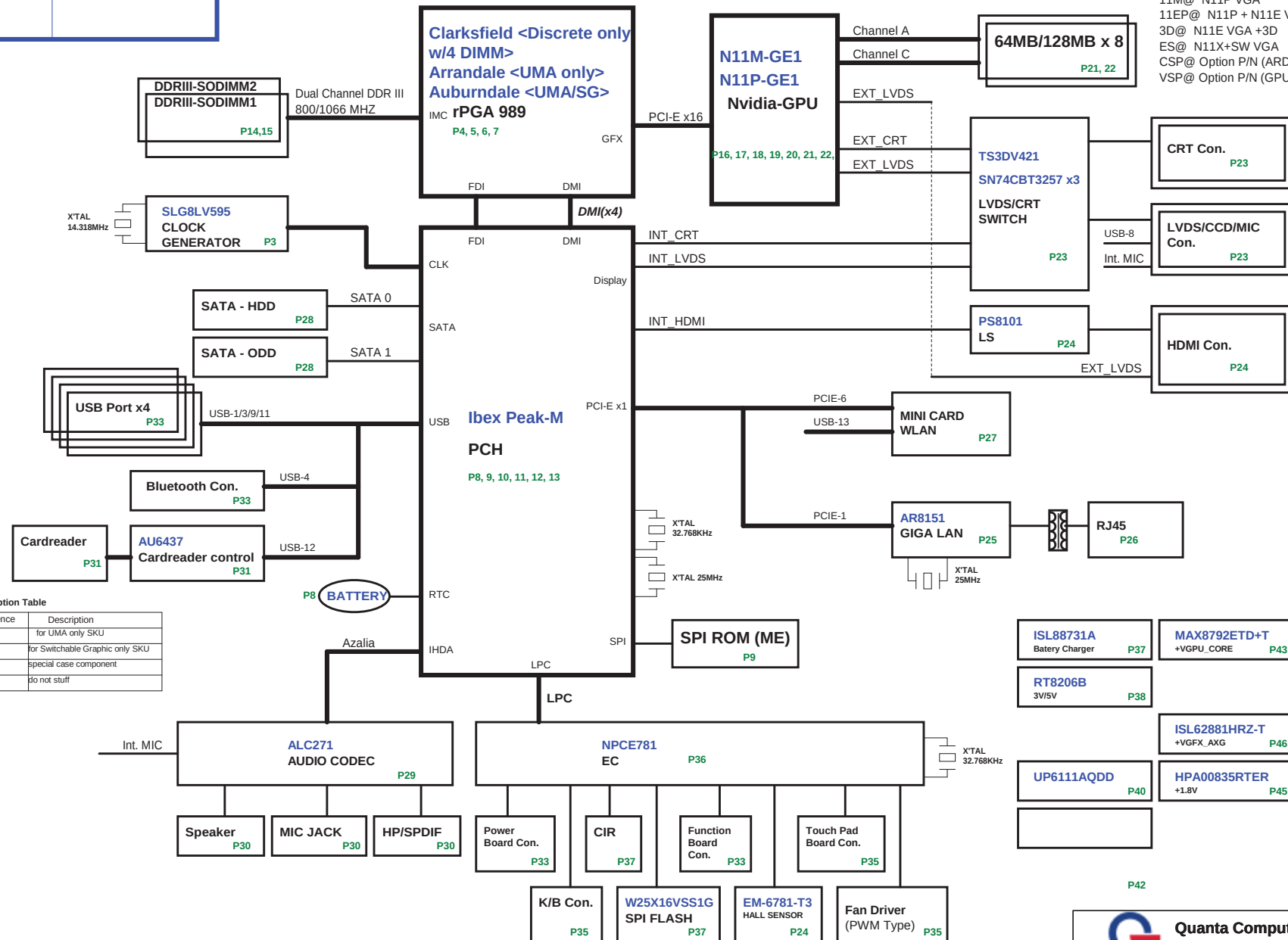


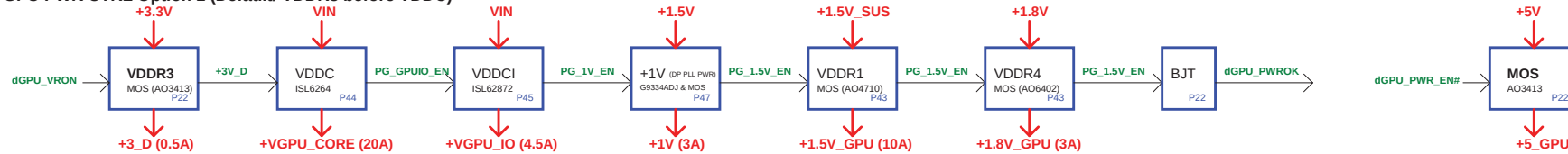
ZR7 SYSTEM BLOCK DIAGRAM

IV@ INT VGA
EV@ DISCRETE
SW@ SW VGA
11P@ N11P VGA
11M@ N11P VGA
11EP@ N11P + N11E VGA
3D@ N11E VGA +3D
ES@ N11X+SW VGA
CSP@ Option P/N (ARD&R D)
VSP@ Option P/N (GPU/ VRAM)

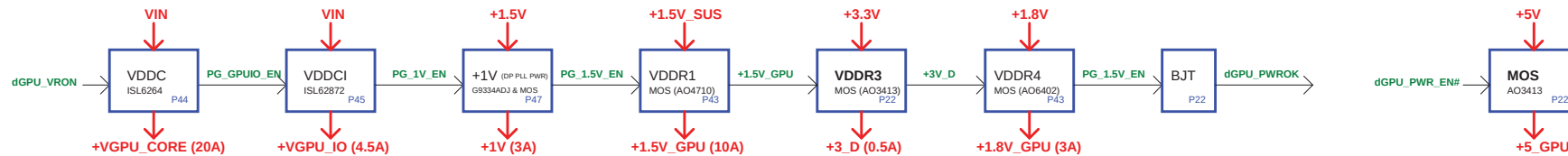
Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU
SP@	special case component
*	do not stuff



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



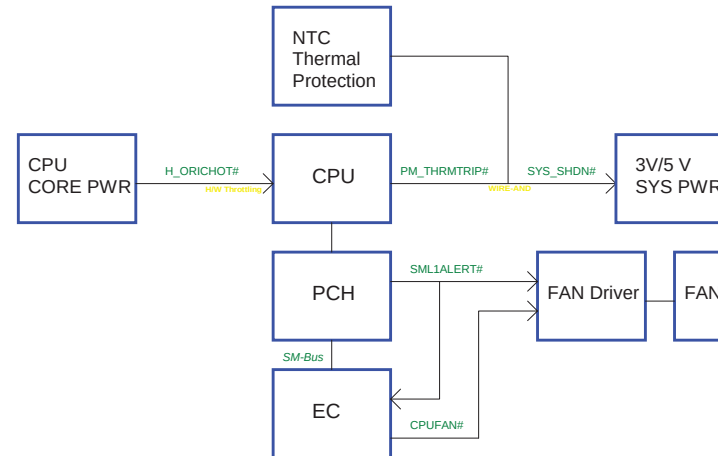
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



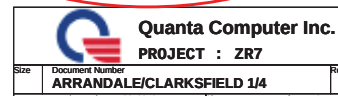
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

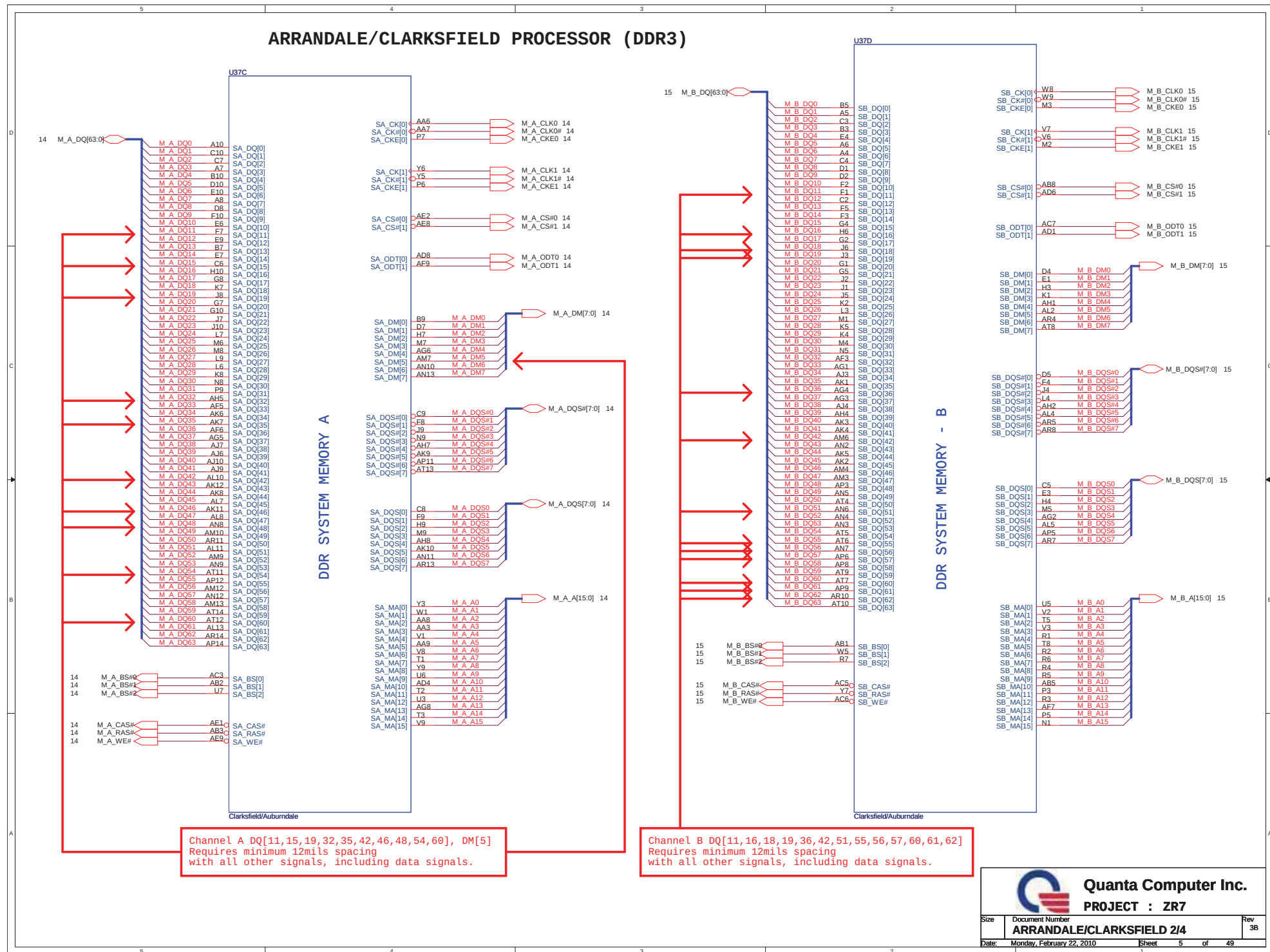
Thermal Follow Chart



ARRANDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



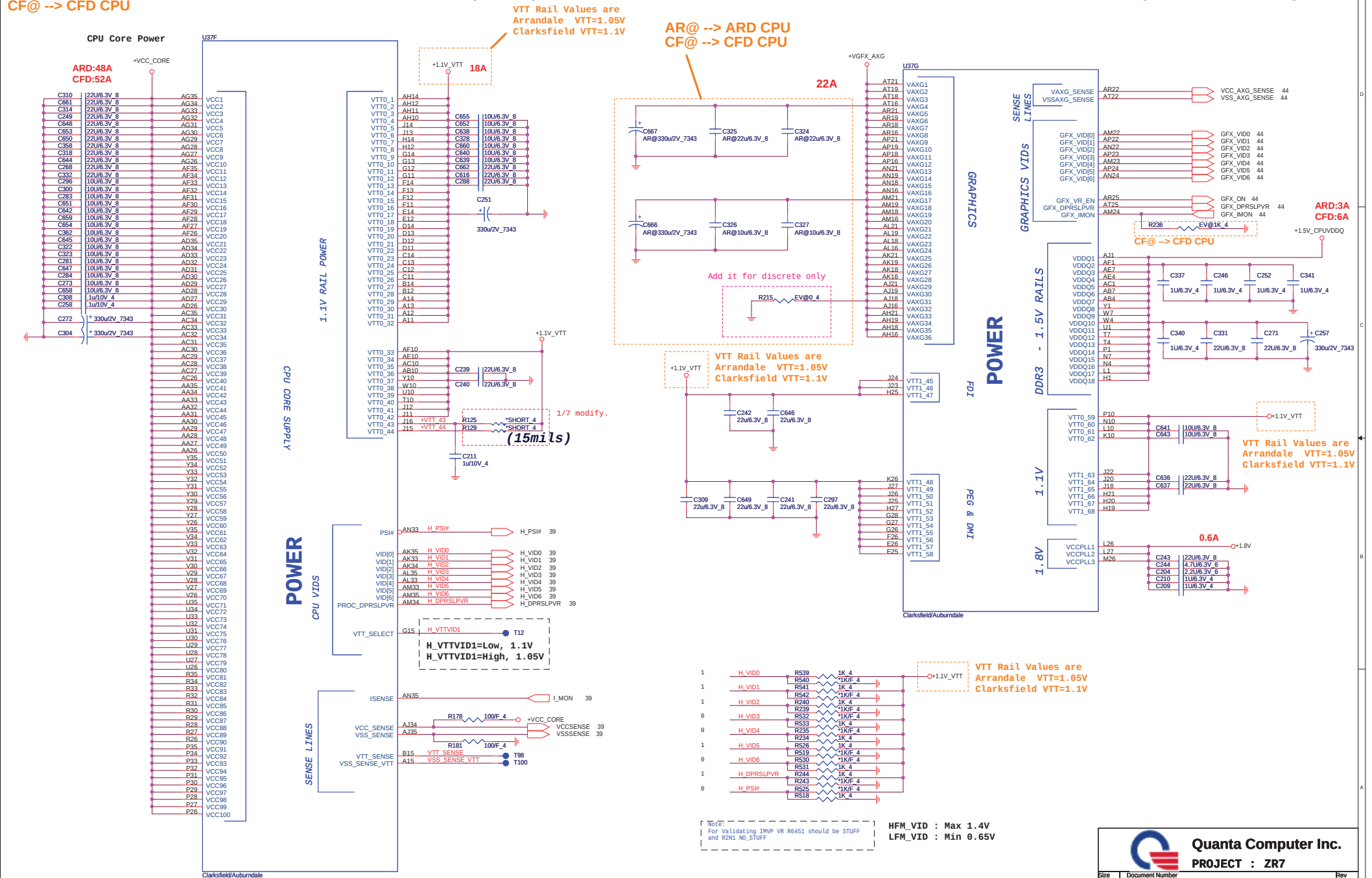
ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



ARRANDALE/CLARKSFIELD PROCESSOR (POWER)

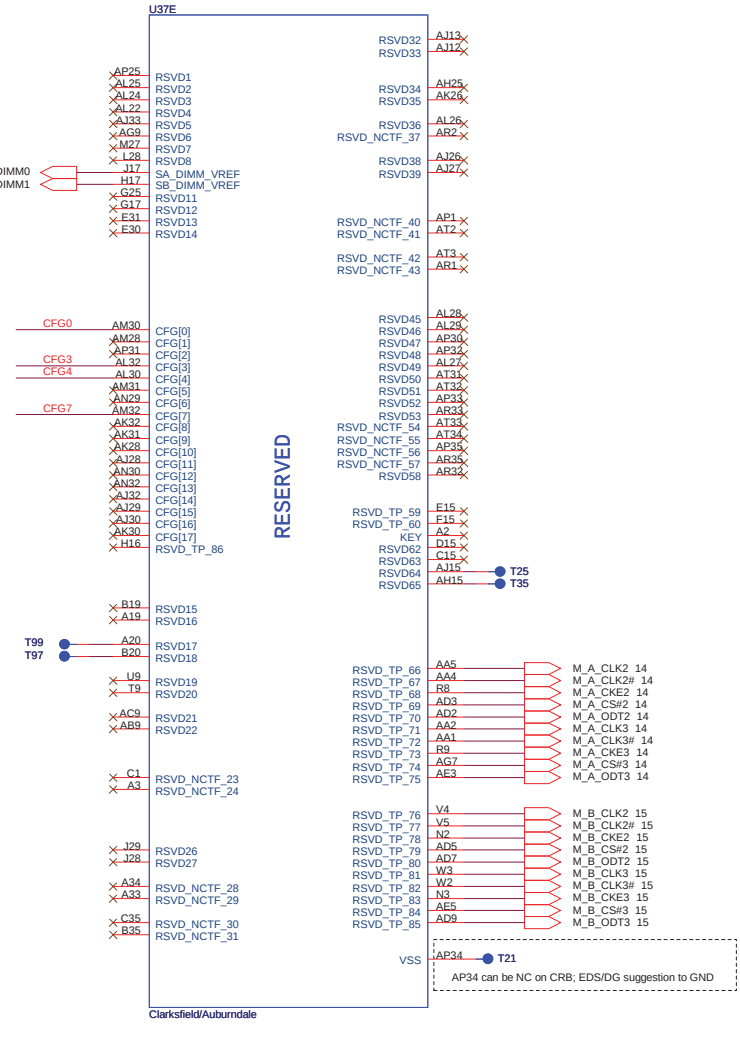
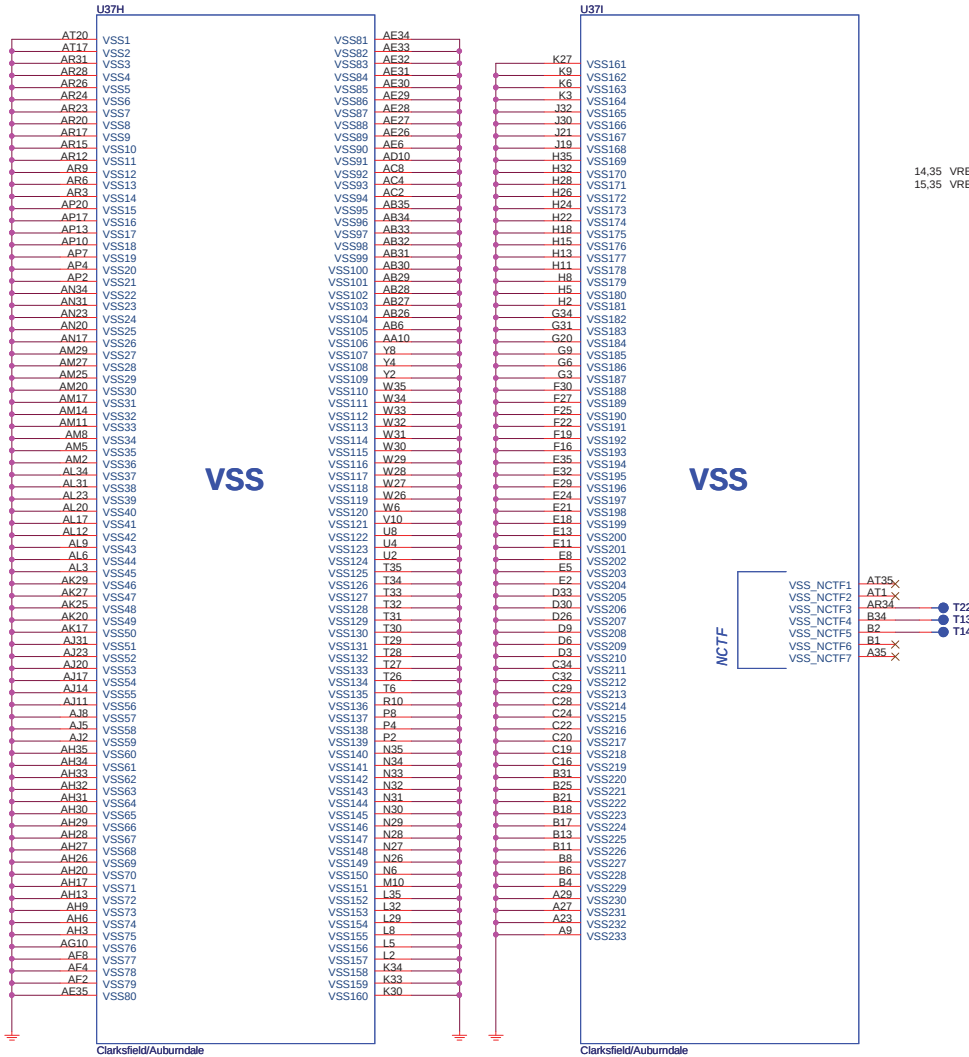
AR@ --> ARD CPU
CF@ --> CFD CPU

ARRANDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



ARRANDALE/CLARKSFIELD PROCESSOR (GND)

ARRANDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

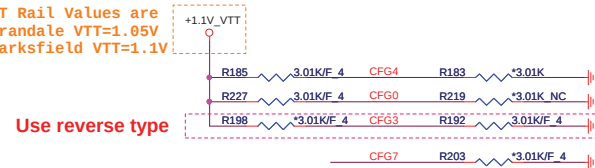


Processor Strapping

	1	0	DEFAULT
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

VTT Rail Values are
Arrandale VTT=1.05V
Clarksville VTT=1.1V



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	ARRANDALE/CLARKSFIELD 4/4	38
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AR@ --> ARD CPU
CF@ --> CFD CPU
IV@ --> iGPU only

IBEX PEAK-M (DMI, FDI, GPIO)

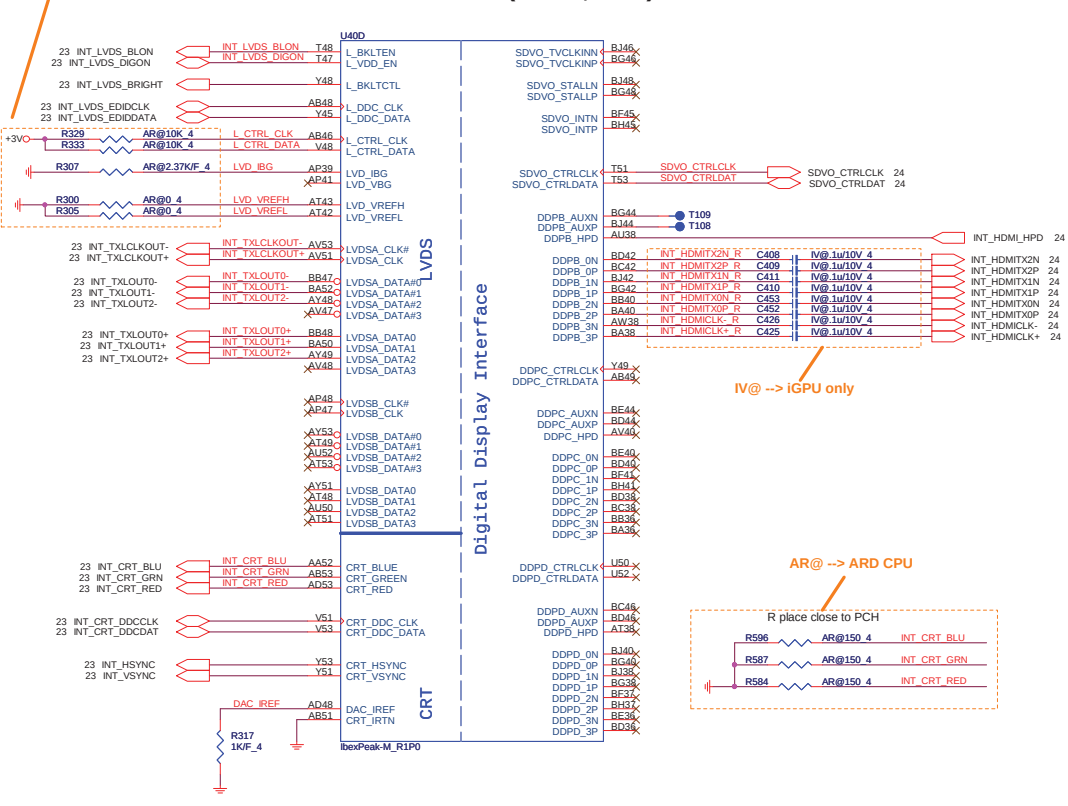
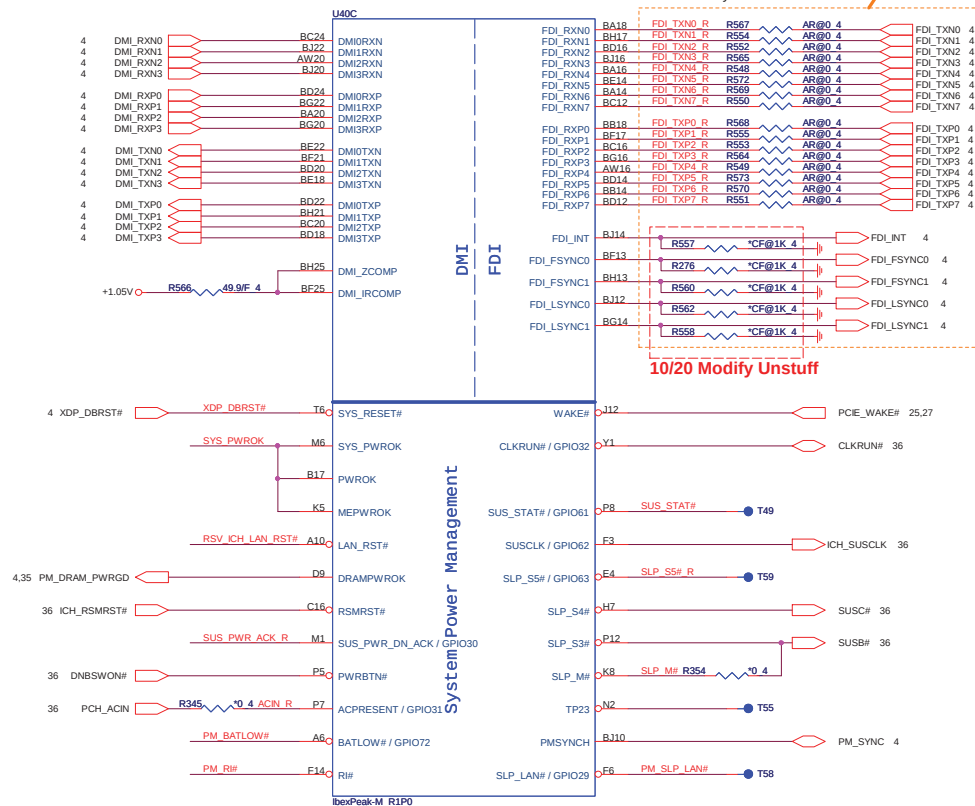
AR@ --> ARD CPU
CF@ --> CFD CPU

AR@ --> ARD CPU

IBEX PEAK-M (LVDS, DDI)

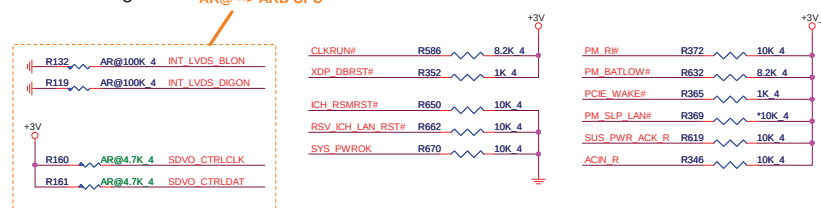
Arrandale only

10/20 Modify Unstuff

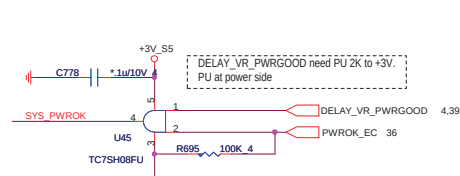


PCH Pull-high/low

AR@ --> ARD CPU



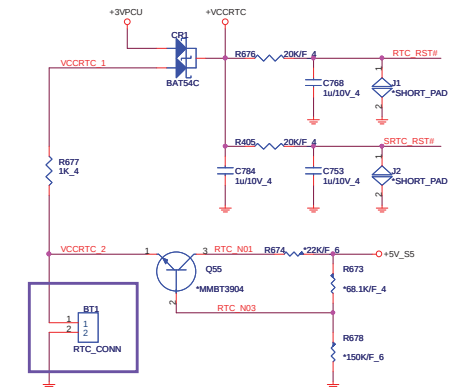
System PWR_OK



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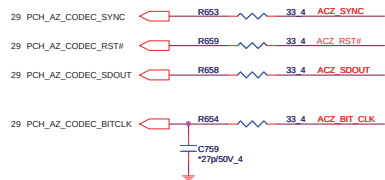
Size	Document Number	Rev
	IBEX PEAK-M 1/6	3B
Date:	Monday, February 22, 2010	Sheet 8 of 49

RTC Circuitry



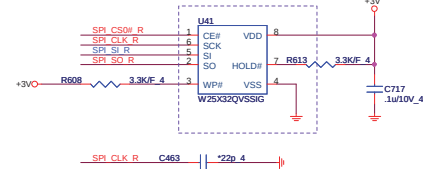
1/7 Change P/N by ME.

HDA Bus

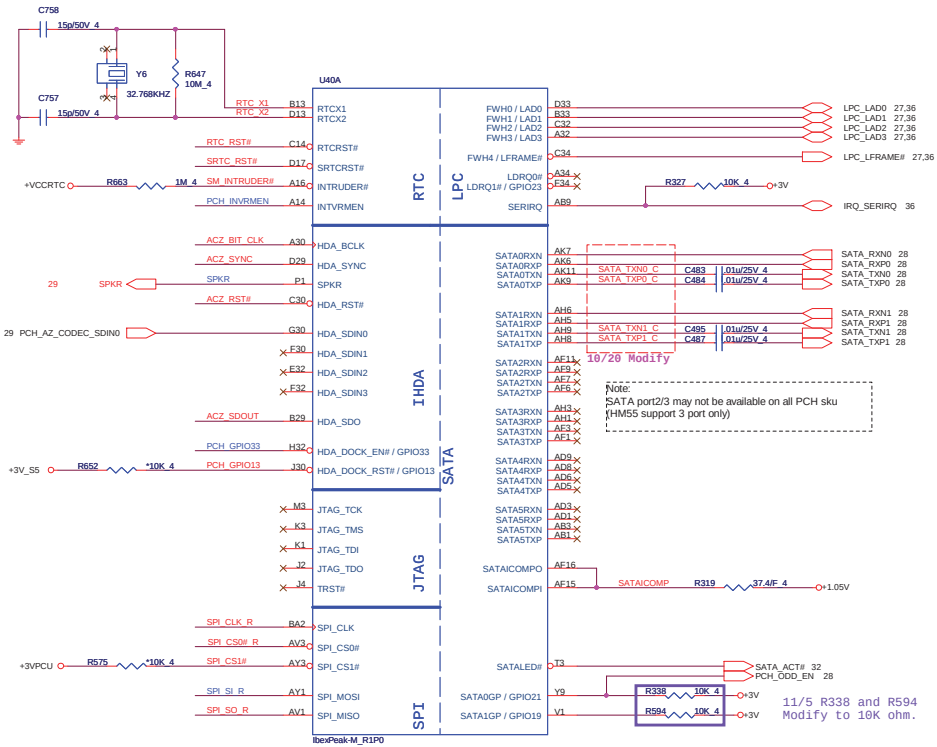


PCH SPI

10/29 Modify P/N to 2M
12/7 Modify P/N to 4M



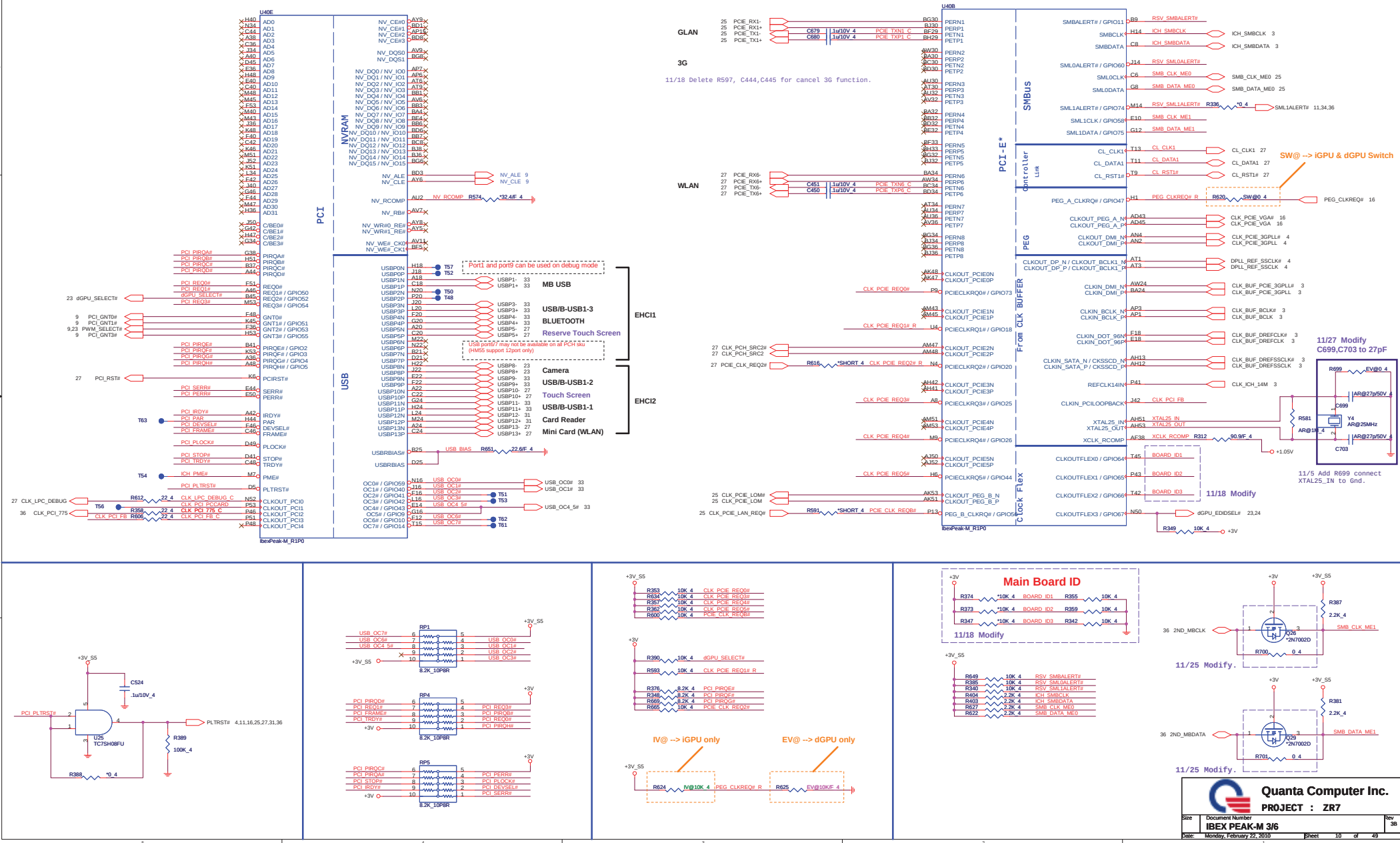
HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V



PCH Strap Pin Configuration Table-1

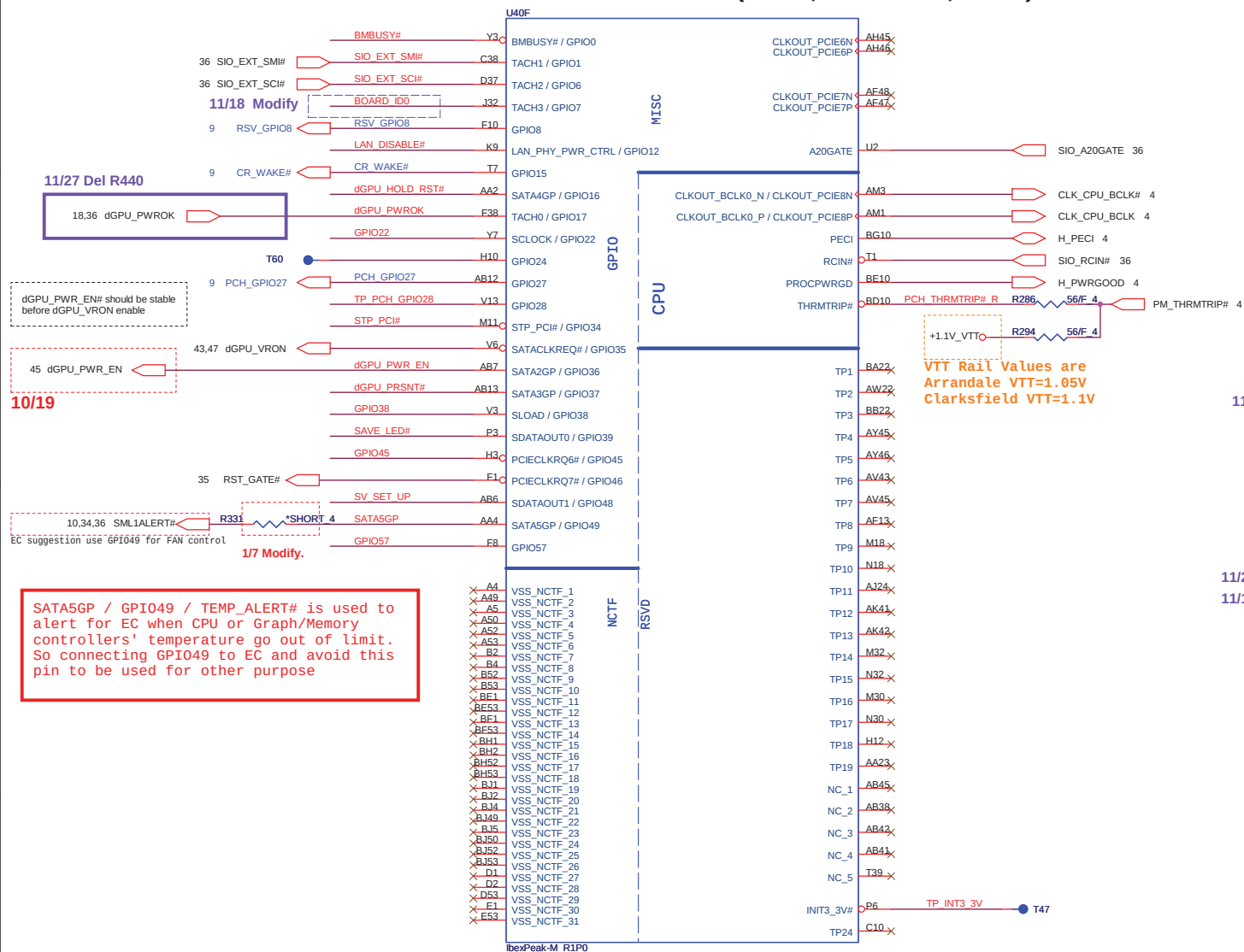
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC - R663 300K 6 PCH INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disabled	+3V - R618 1K 4 SPI SI R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V - R611 1K 4 SPI CS1#
HDA_DOCK# / GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH GPIO33 - R370 1K 4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	10 PCH_GNT0# - R360 1K 4 10 PCH_GNT1# - R363 1K 4
GNT2# / GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	10,23 PWM_SELECT# - R364 1K 4
GNT3# / GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	10 PCH_GNT3# - R628 10K 4
NV_ALE	Intel® Anti-Theft Technology HDD Data Protection (Intel AT-D) Enable	1 = Enabled 0 = Disabled (Default)	10 NV_ALE - R296 1K 4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	10 NV_CLE - R295 1K 4 +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	11 RSV_GPIO8 - R380 10K 4 +3V_S5
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	11 CR_WAKE# - R341 1K 4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	11 PCH_GPIO27 - R324 10K 4

IV@ --> iGPU only
EV@ --> dGPU only
SW@ --> iGPU & dGPU Switch

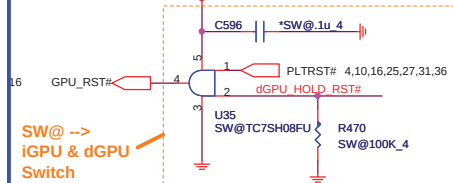


IV@ --> iGPU only
 EV@ --> dGPU only
 SW@ --> iGPU & dGPU Switch
 ES@ --> External VGA SKU

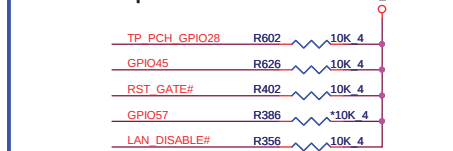
IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



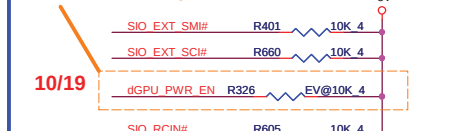
GPU RST#



GPIO Pull-up/Pull-down



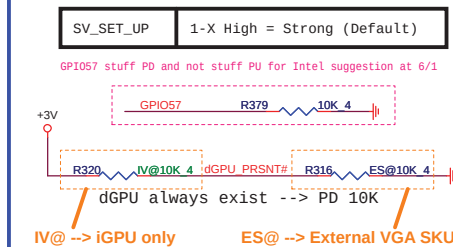
EV@ --> dGPU only



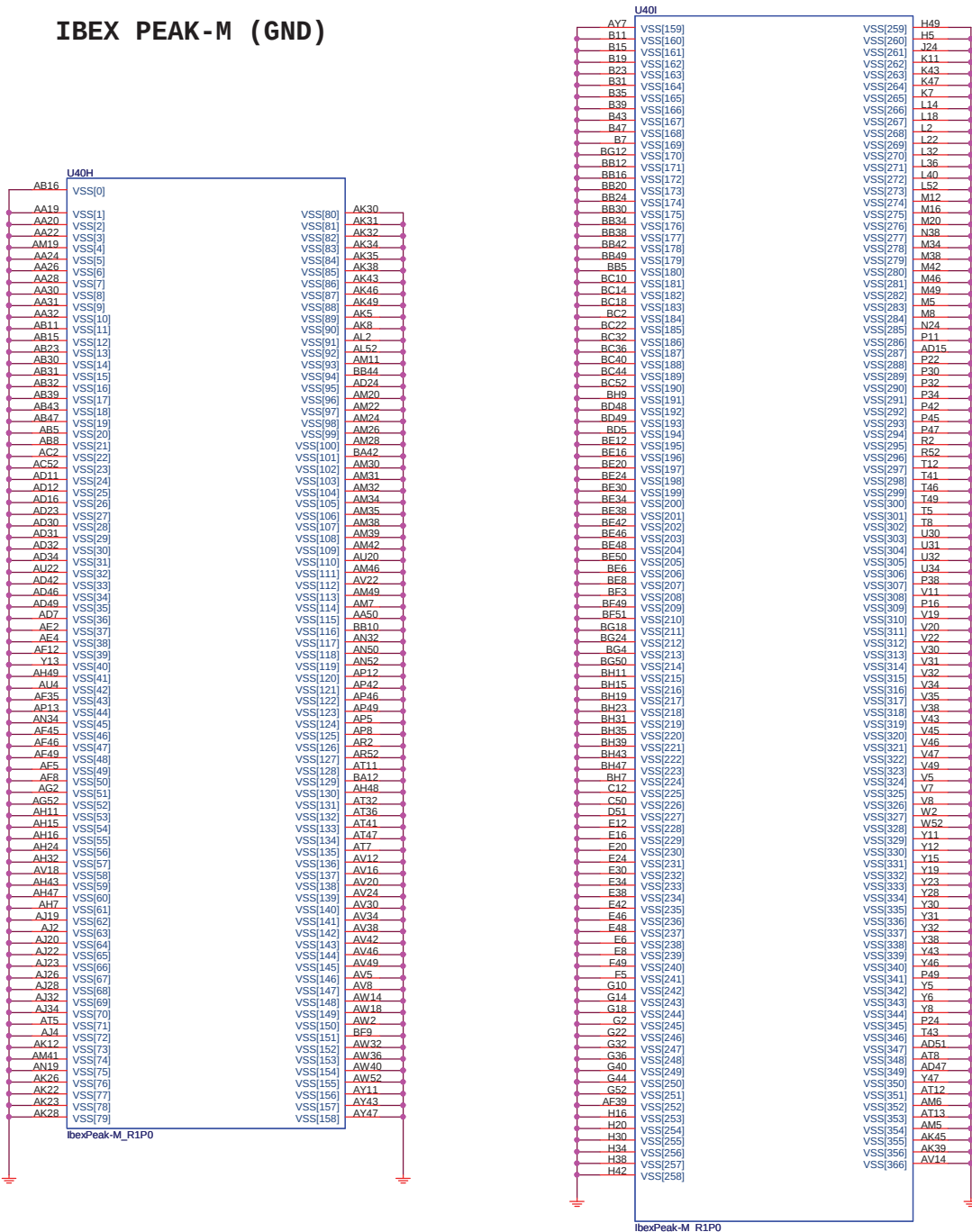
11/19 Modify.

11/26 Modify.

11/19 Modify.



IBEX PEAK-M (GND)



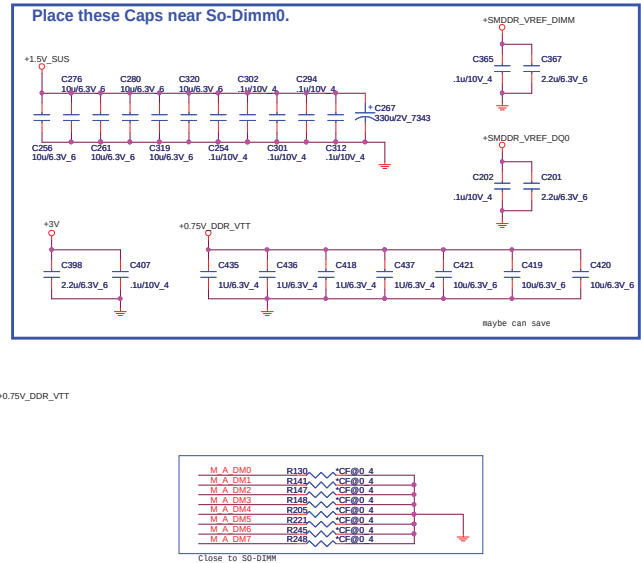
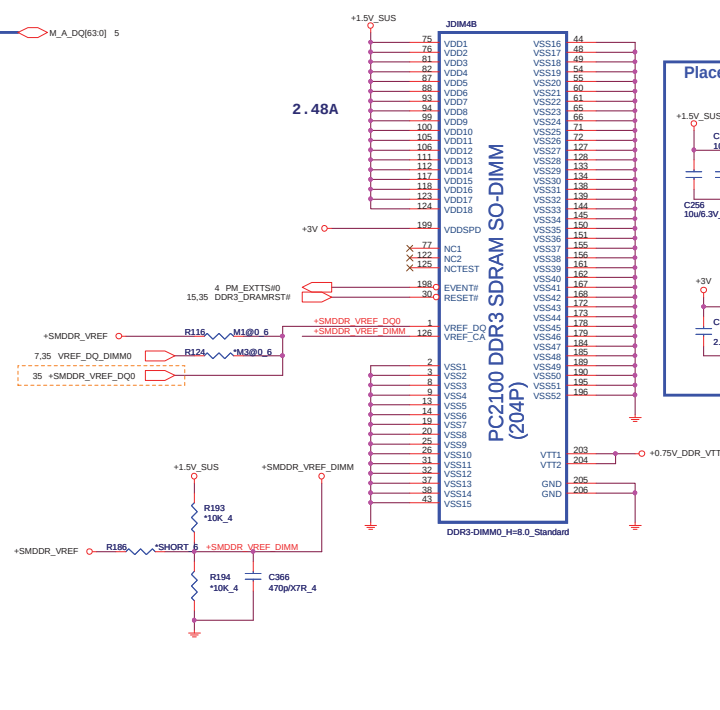
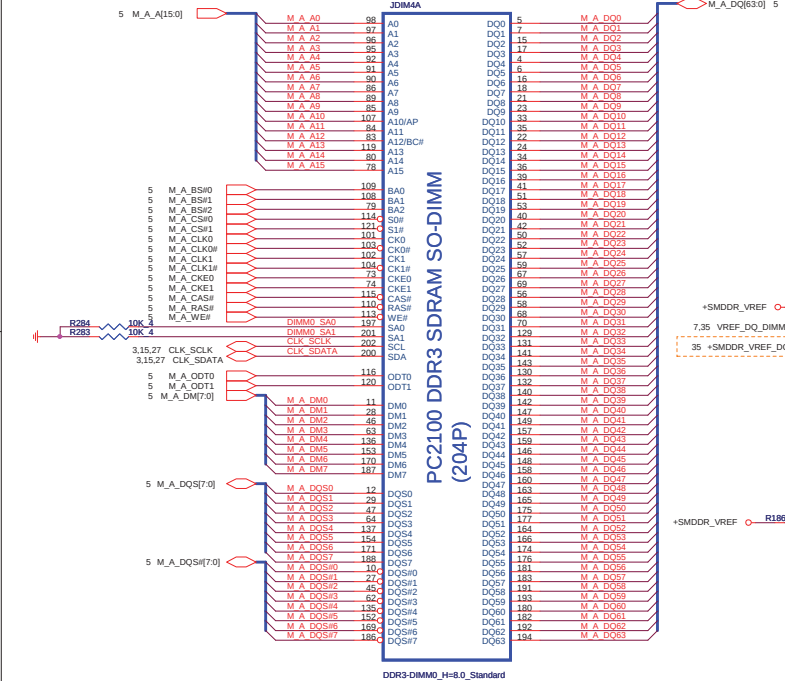


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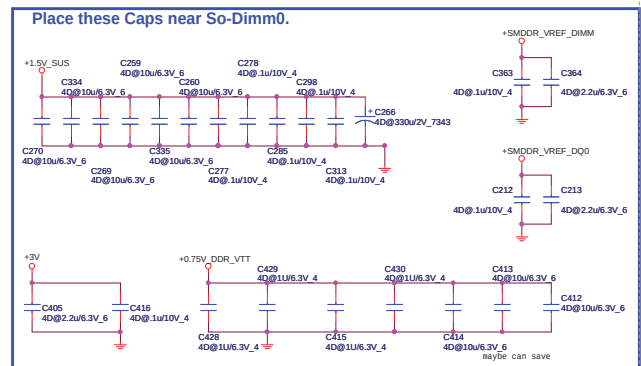
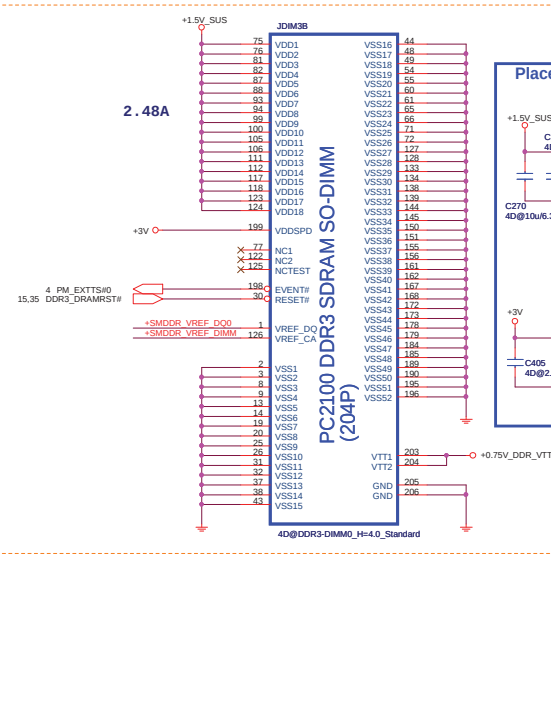
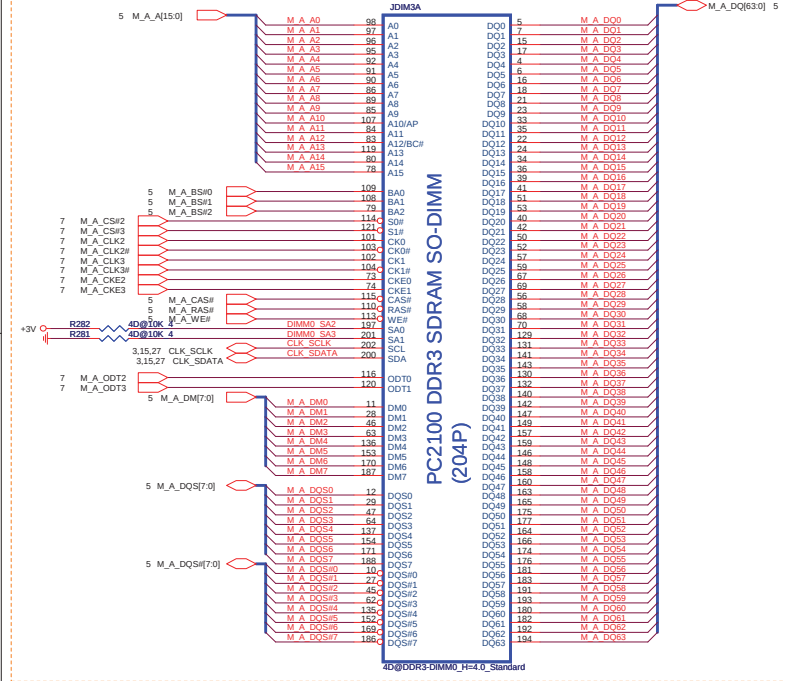
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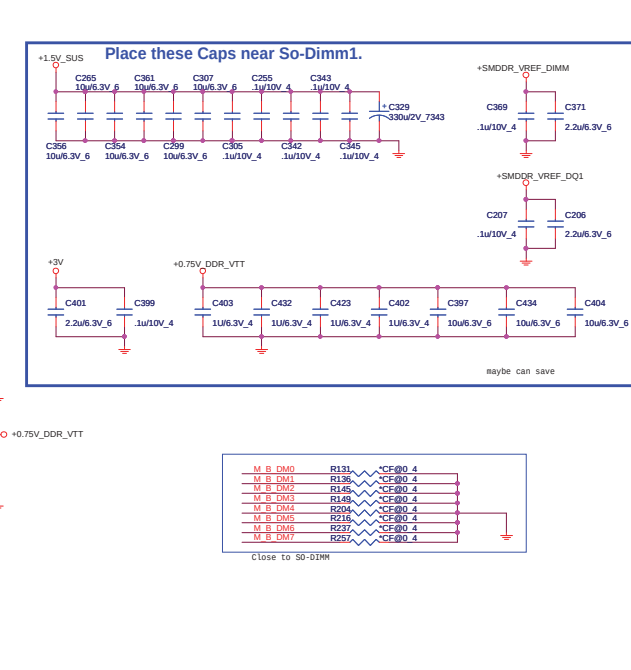
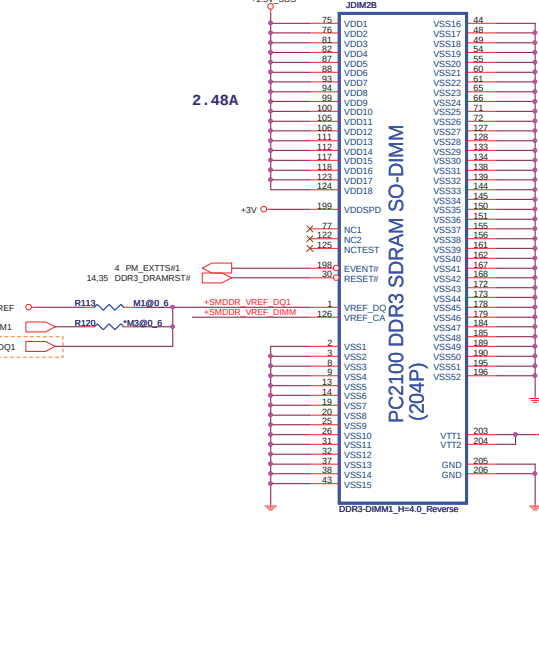
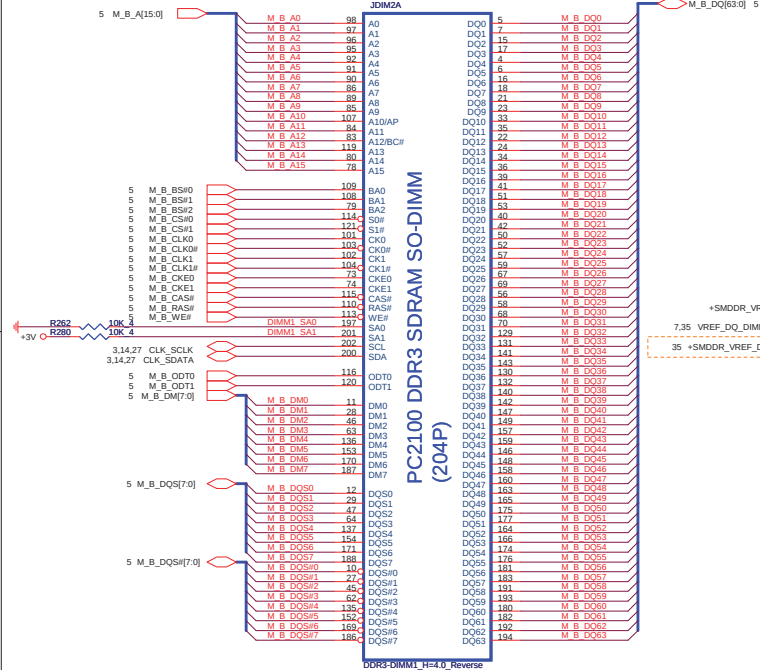
DIMM A0



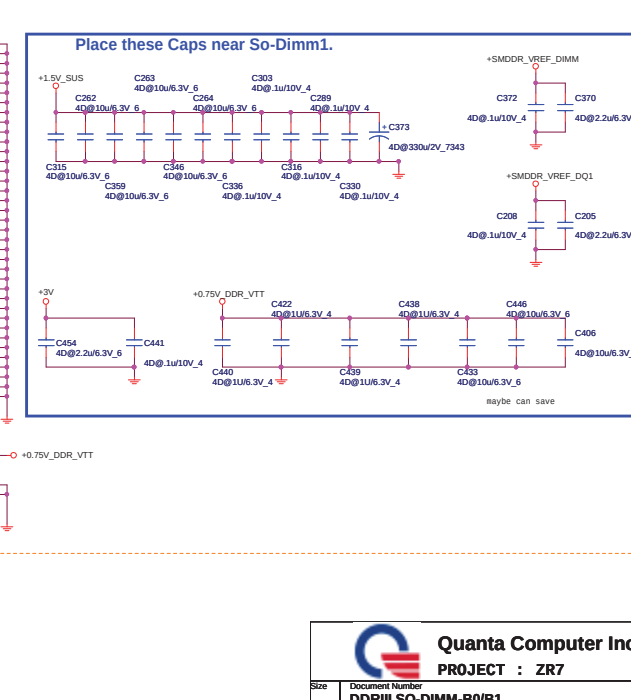
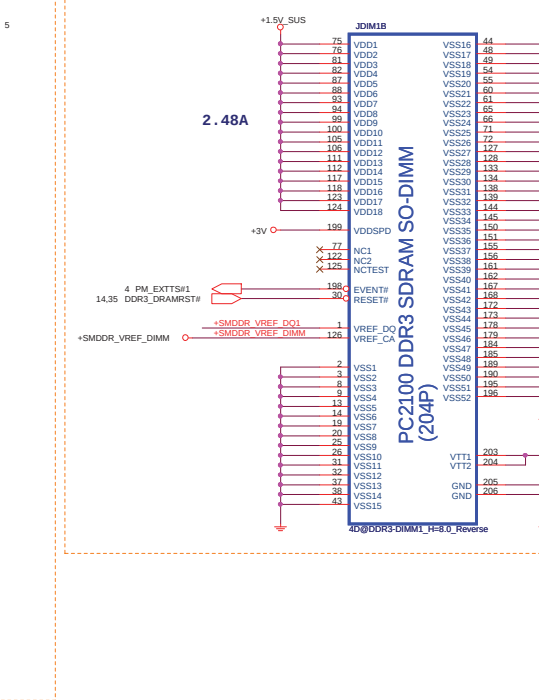
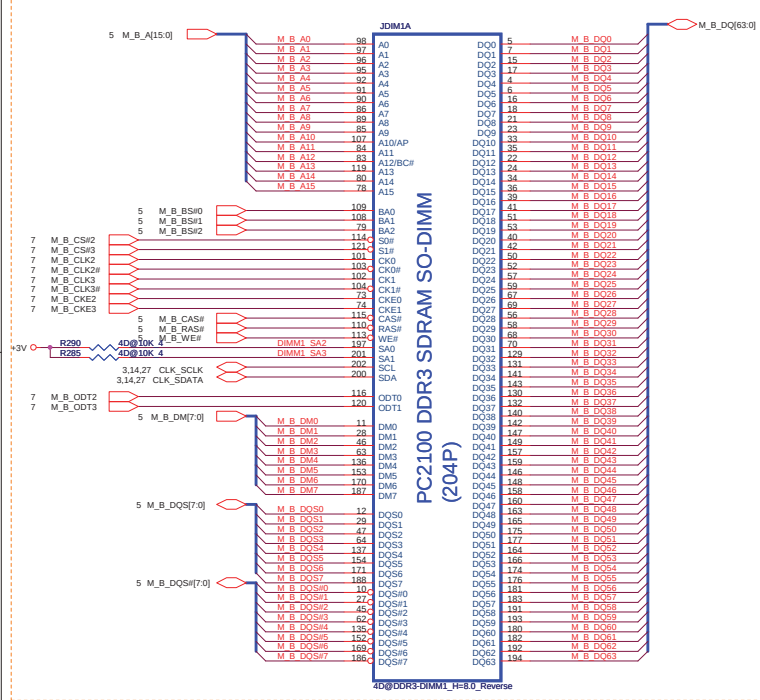
DIMM A1 4D@ --> 4 SO-DIMM

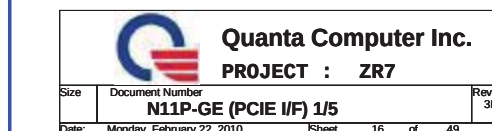
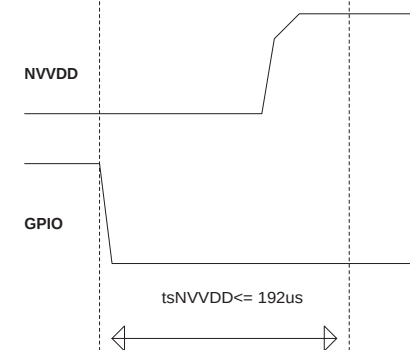
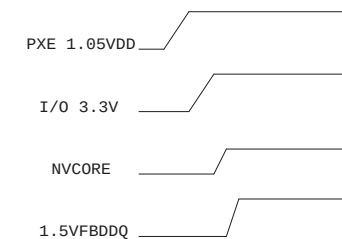
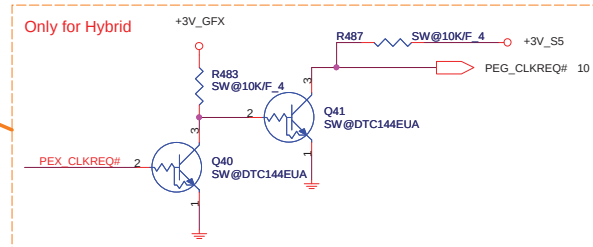
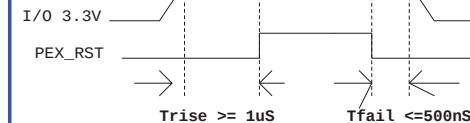
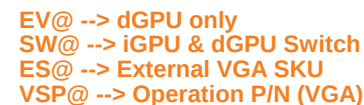


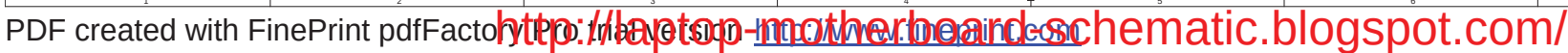
DIMM B0



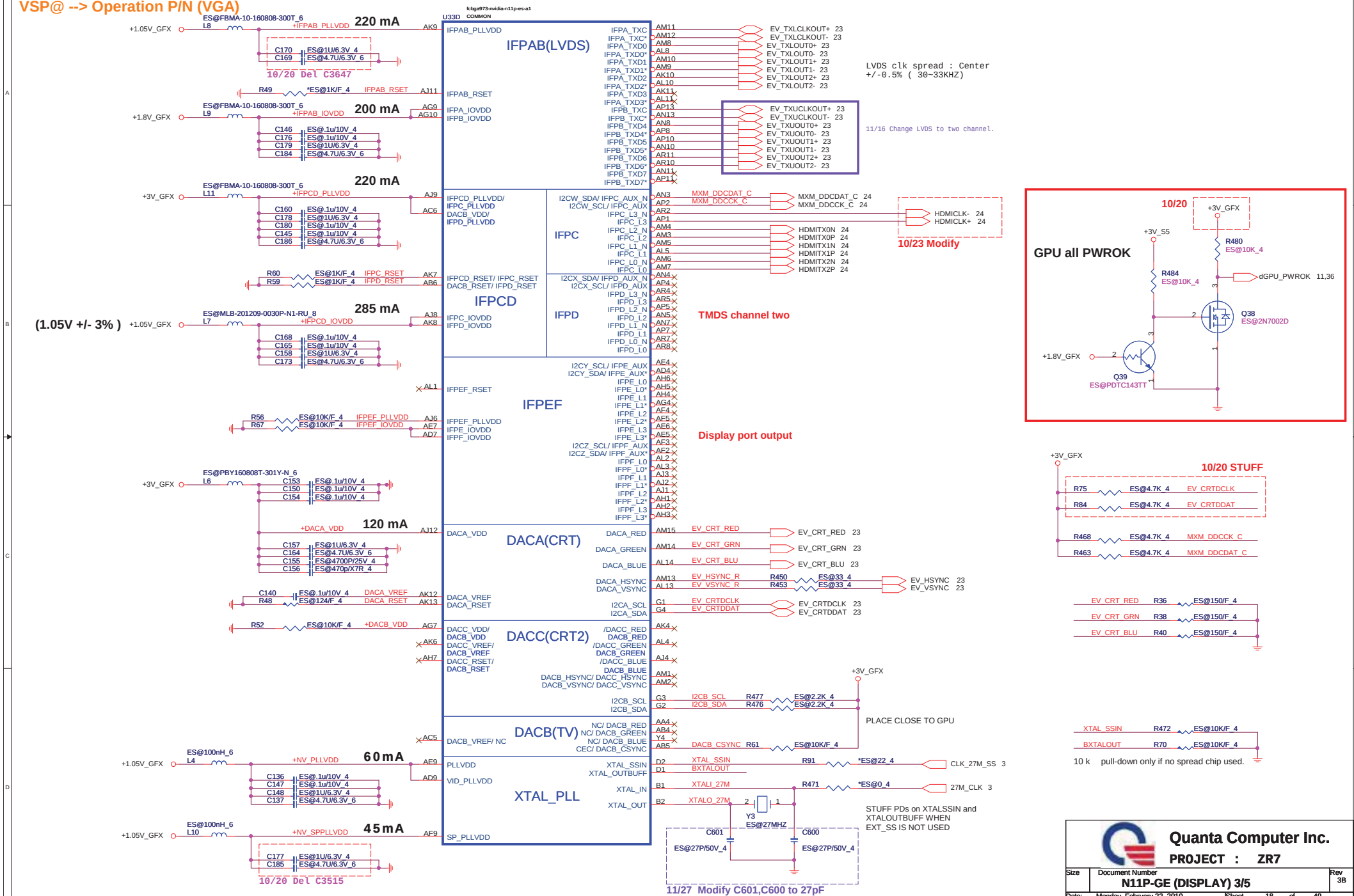
DIMM B1 4D@ --> 4 SO-DIMM

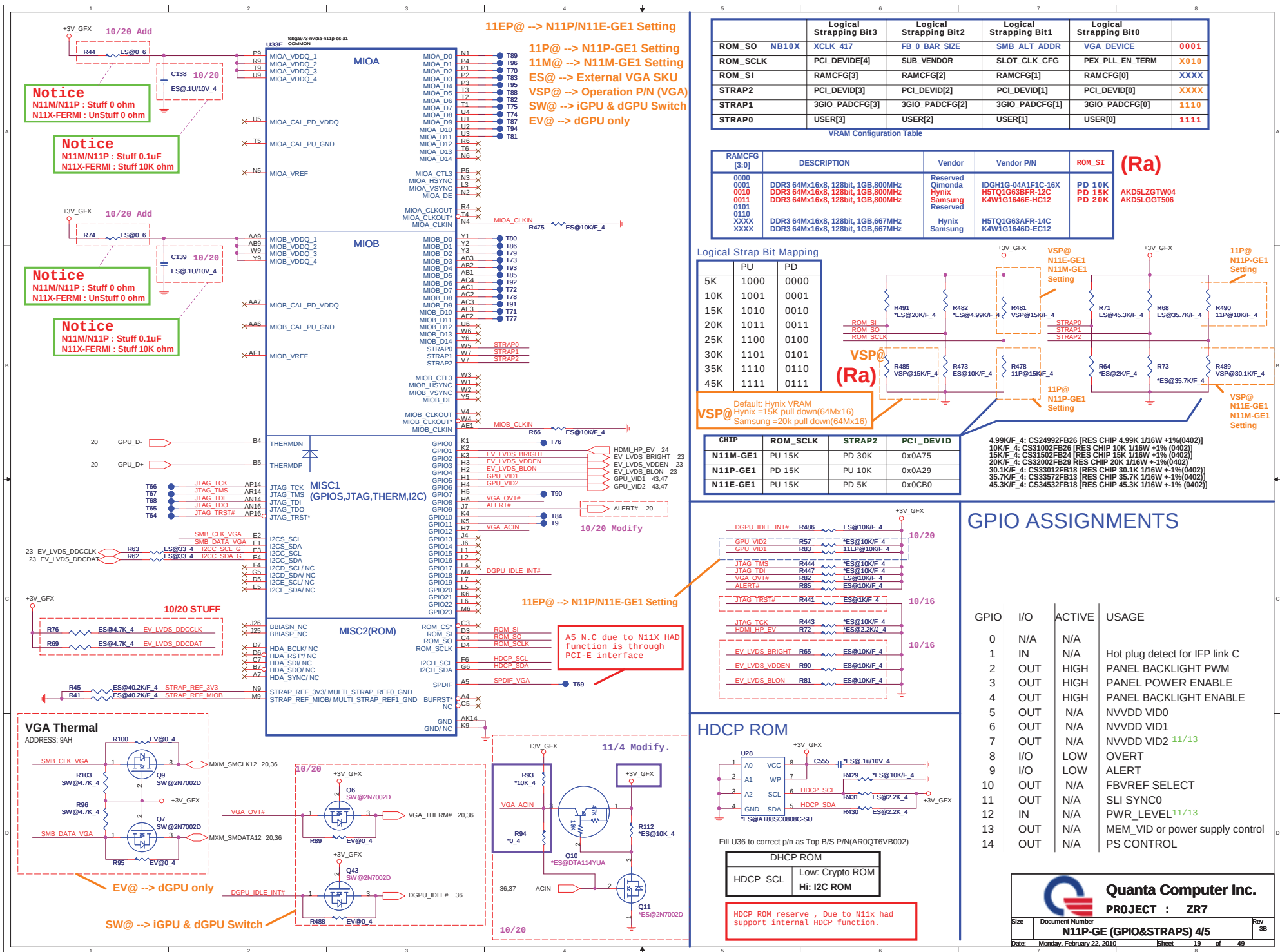




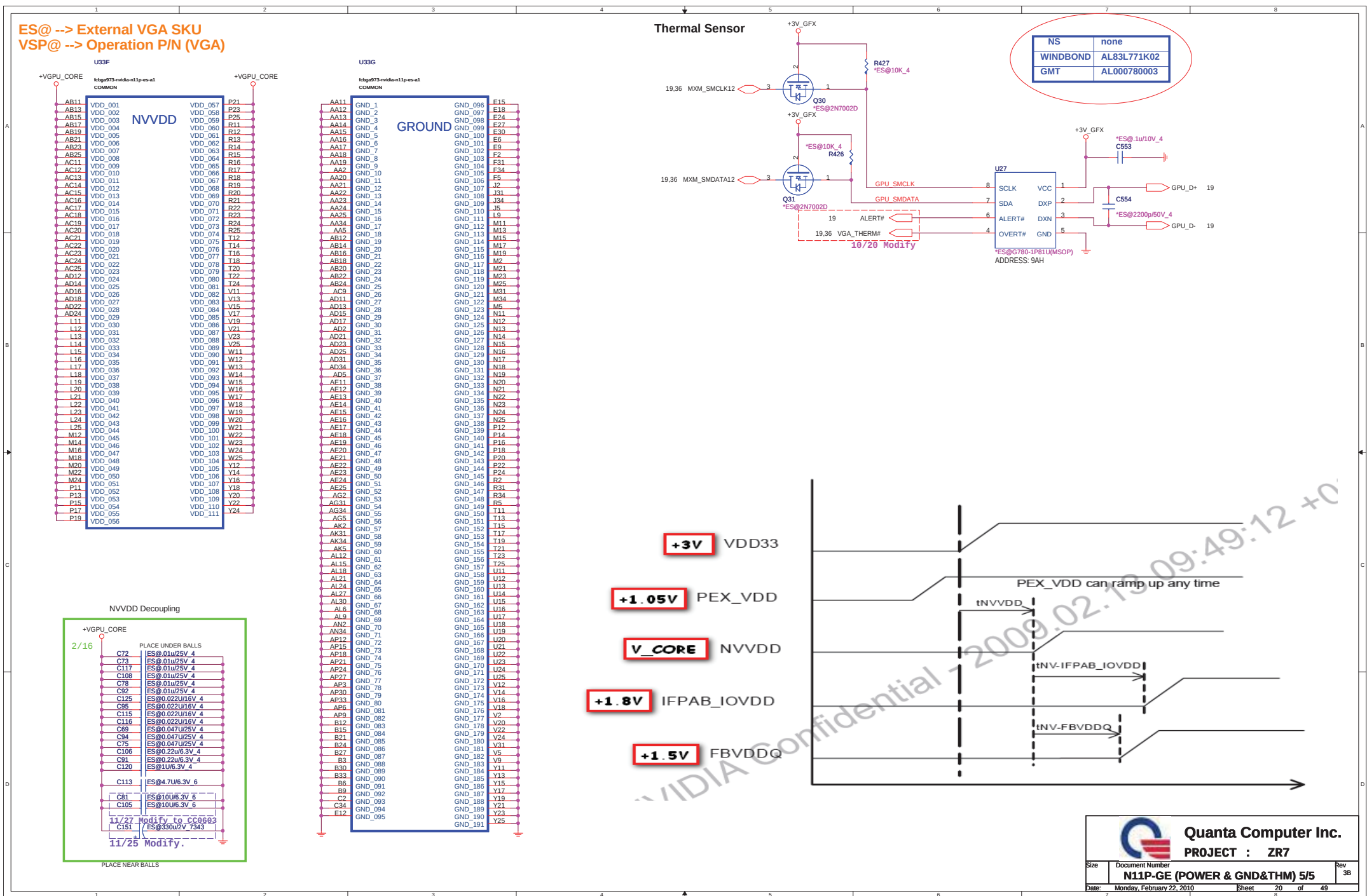


ES@ --> External VGA SKU
VSP@ --> Operation P/N (VGA)





ES@ --> External VGA SKU
VSP@ --> Operation P/N (VGA)

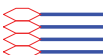


VSP@ --> Operation P/N (VGA-VRAM)

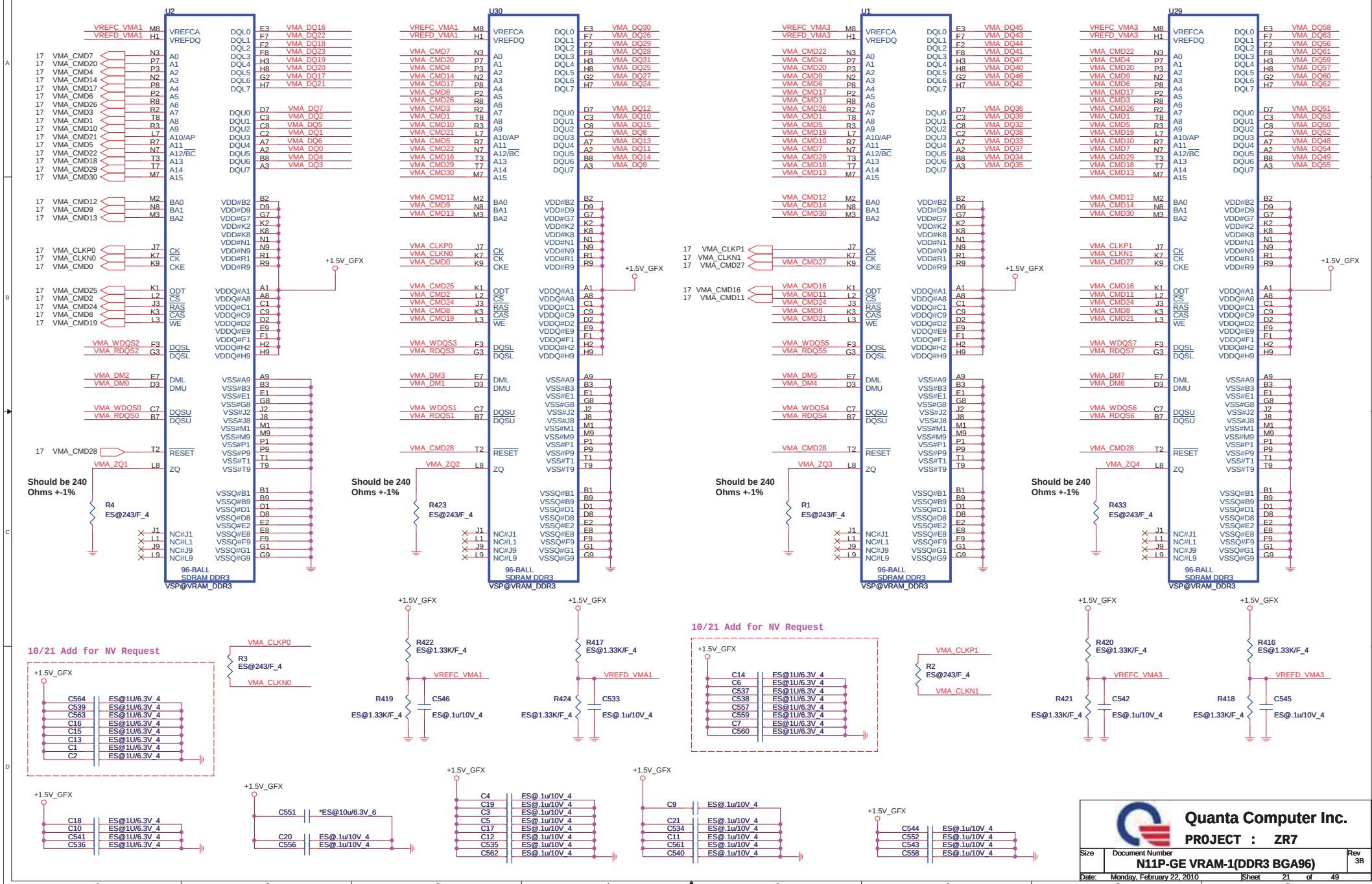
```

17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

```

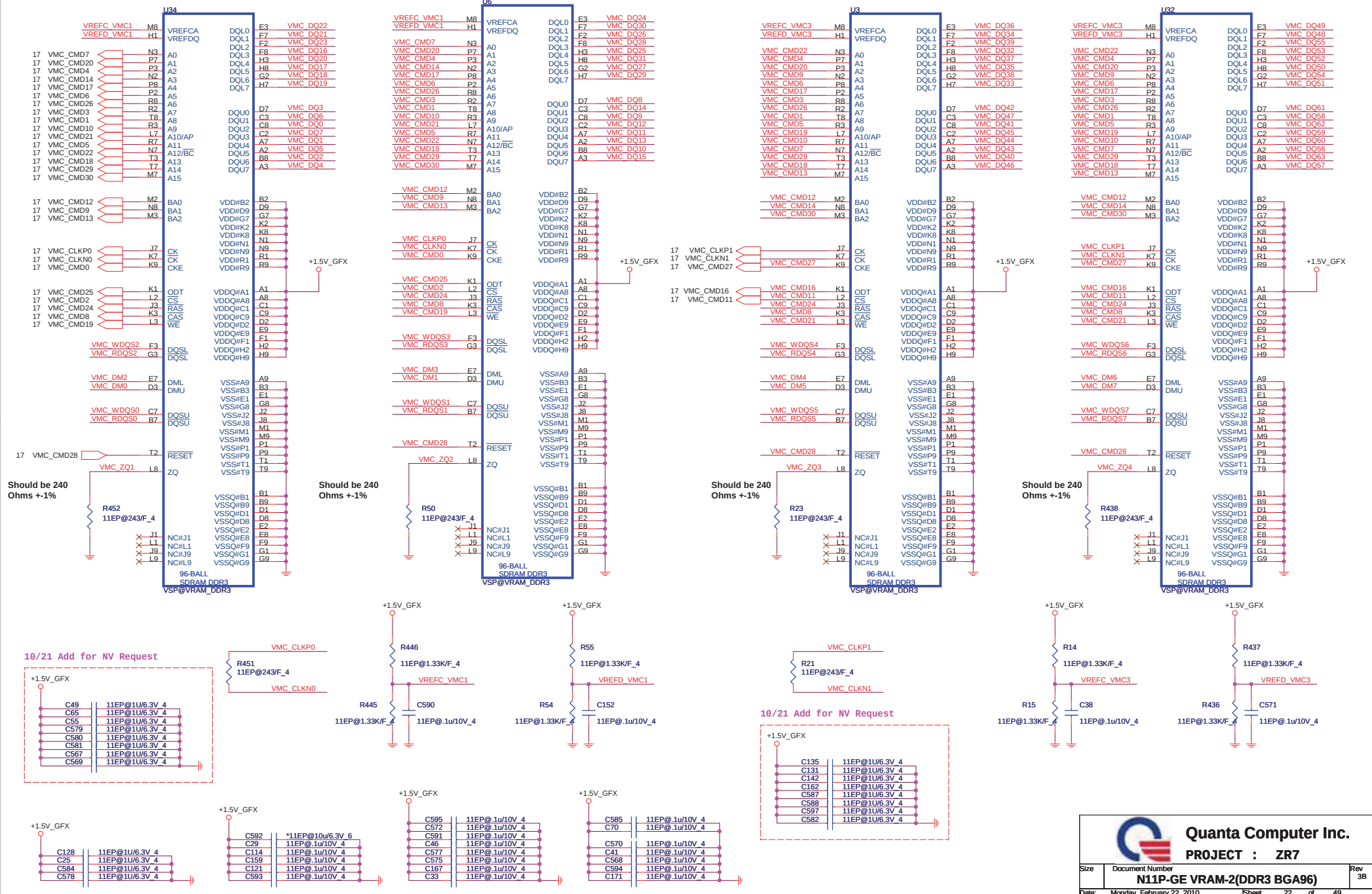


CHANNEL A: 256MB/512MB DDR3



11EP@ --> N11P/N11E-GE1 Setting
VSP@ --> Operation P/N (VGA-VRAM CH:B N11P/N11E only)

CHANNEL B: 256MB/512MB DDR3



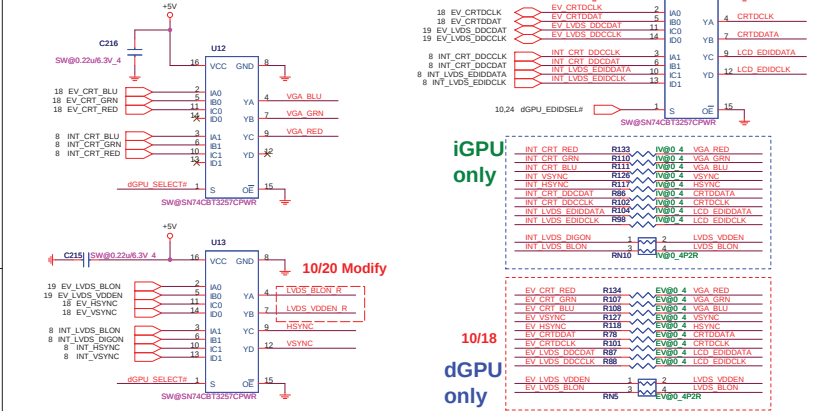
CRT Switch

SW@ -> iGPU & dGPU Switch

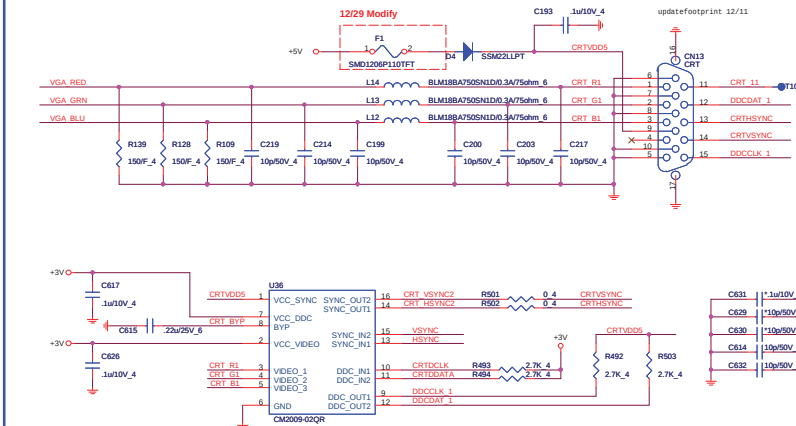
IV@ -> iGPU only

EV@ -> dGPU only

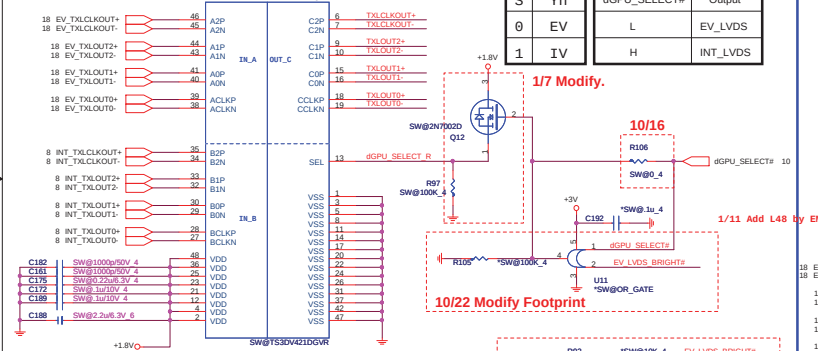
S	Yn	dGPU_SELECT# dGPU_EDIDSEL#	Output
0	EV	L	EV_LVDS/CRT
1	IV	H	INT_LVDS/CRT



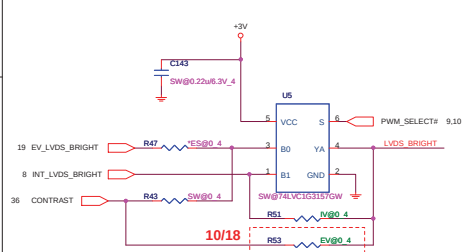
CRT



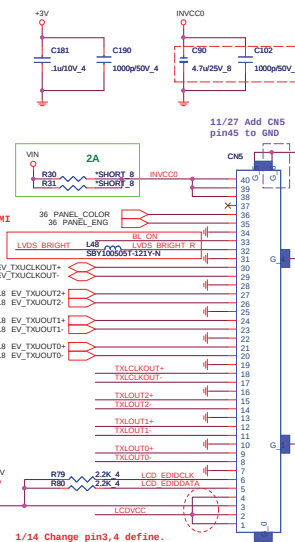
LVDS Switch



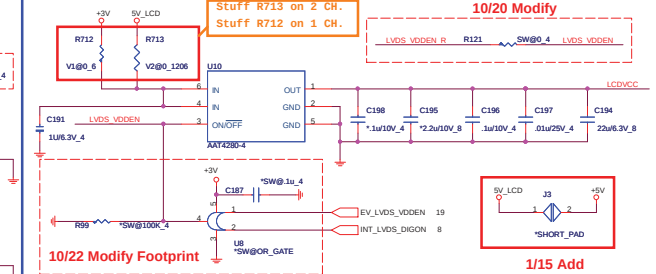
Brightness



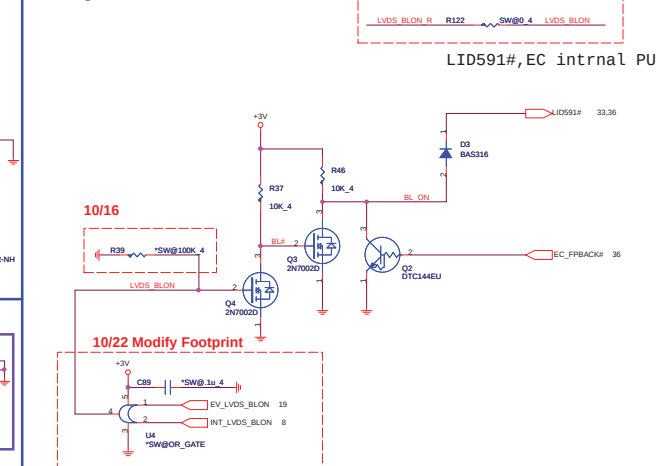
LVDS



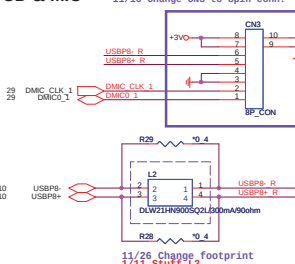
LCD_ON (LCD Power)



Backlight Control

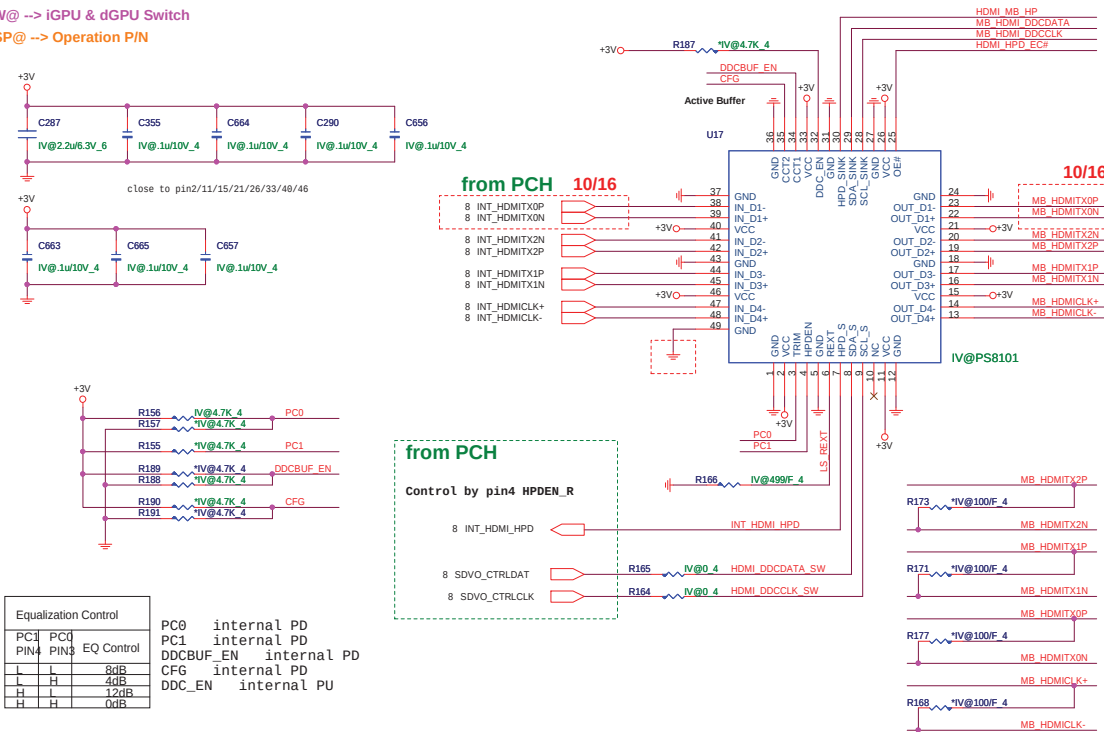


CCD & MIC

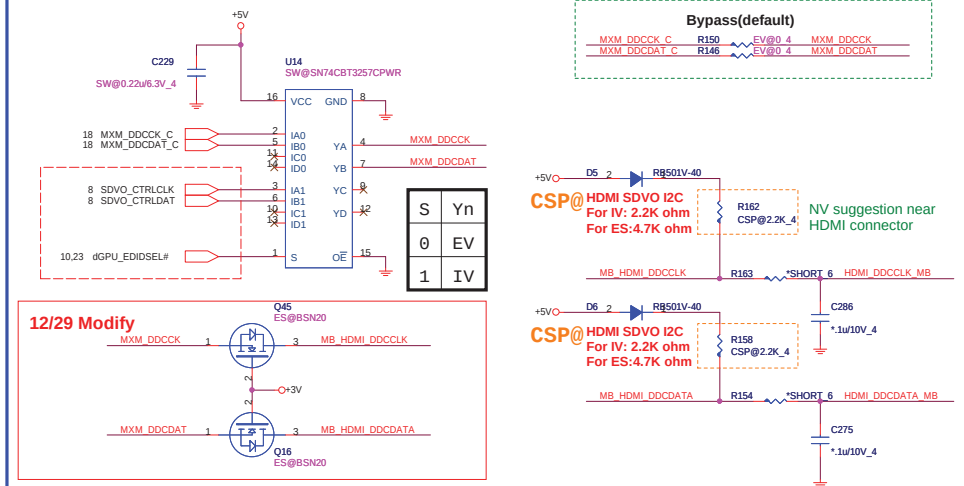


iGPU HDMI LEVEL SHIFTER

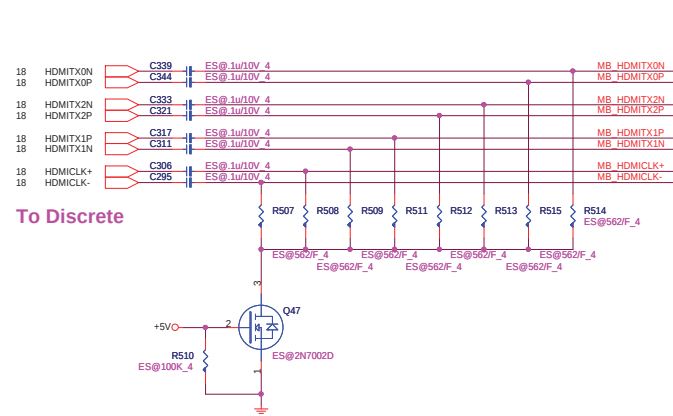
IV@ --> iGPU only
EV@ --> dGPU only
ES@ --> External VGA SKU
SW@ --> iGPU & dGPU Switch
CSP@ --> Operation P/N



SDVO I2C Control



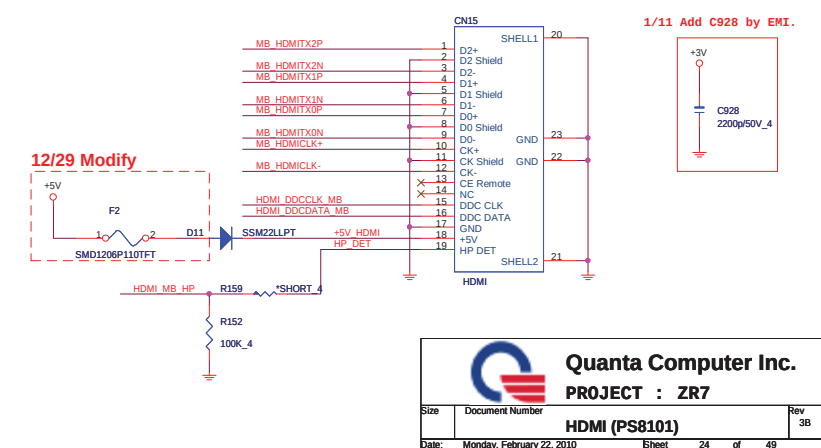
GPU Switchable Graphic HDMI source



ESD Protect

12/29 Delete U15, U16, U18.

HDMI connector



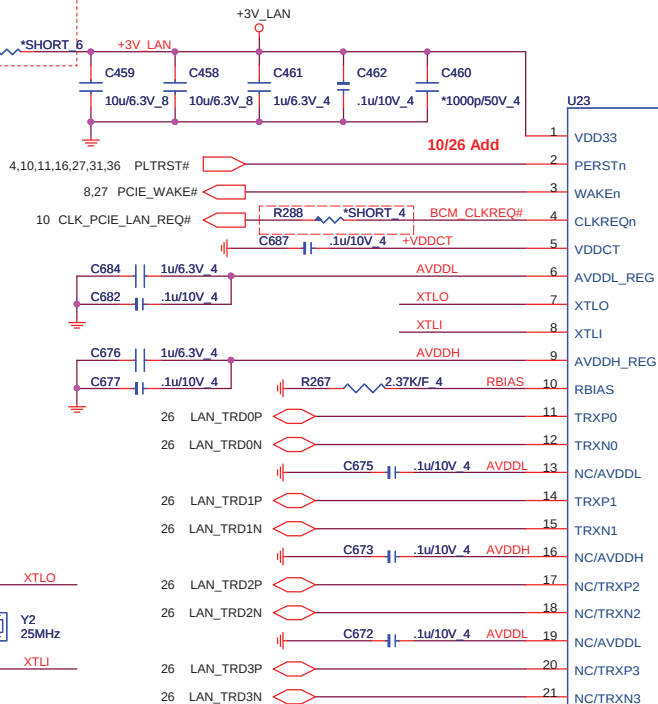
Quanta Computer Inc.
PROJECT : ZR7
HDMI (PS8101)

Size	Document Number	Rev
		38

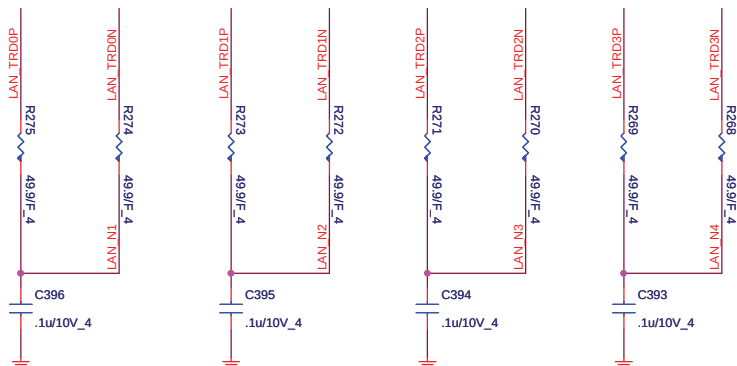
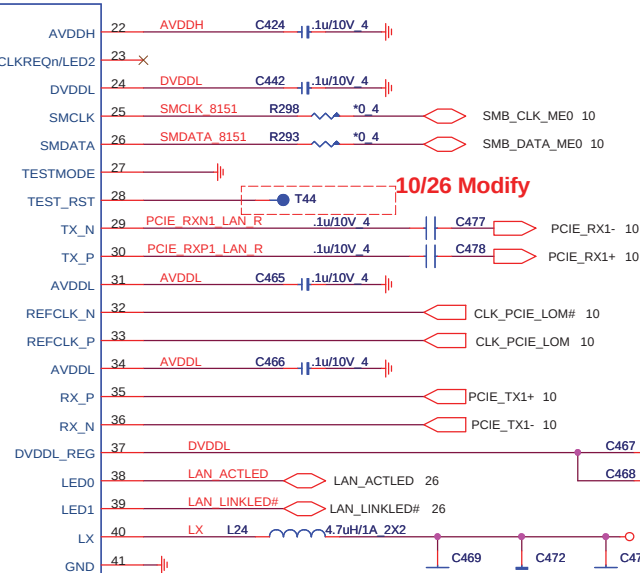
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Giga-LAN AR8151

10/26 Add

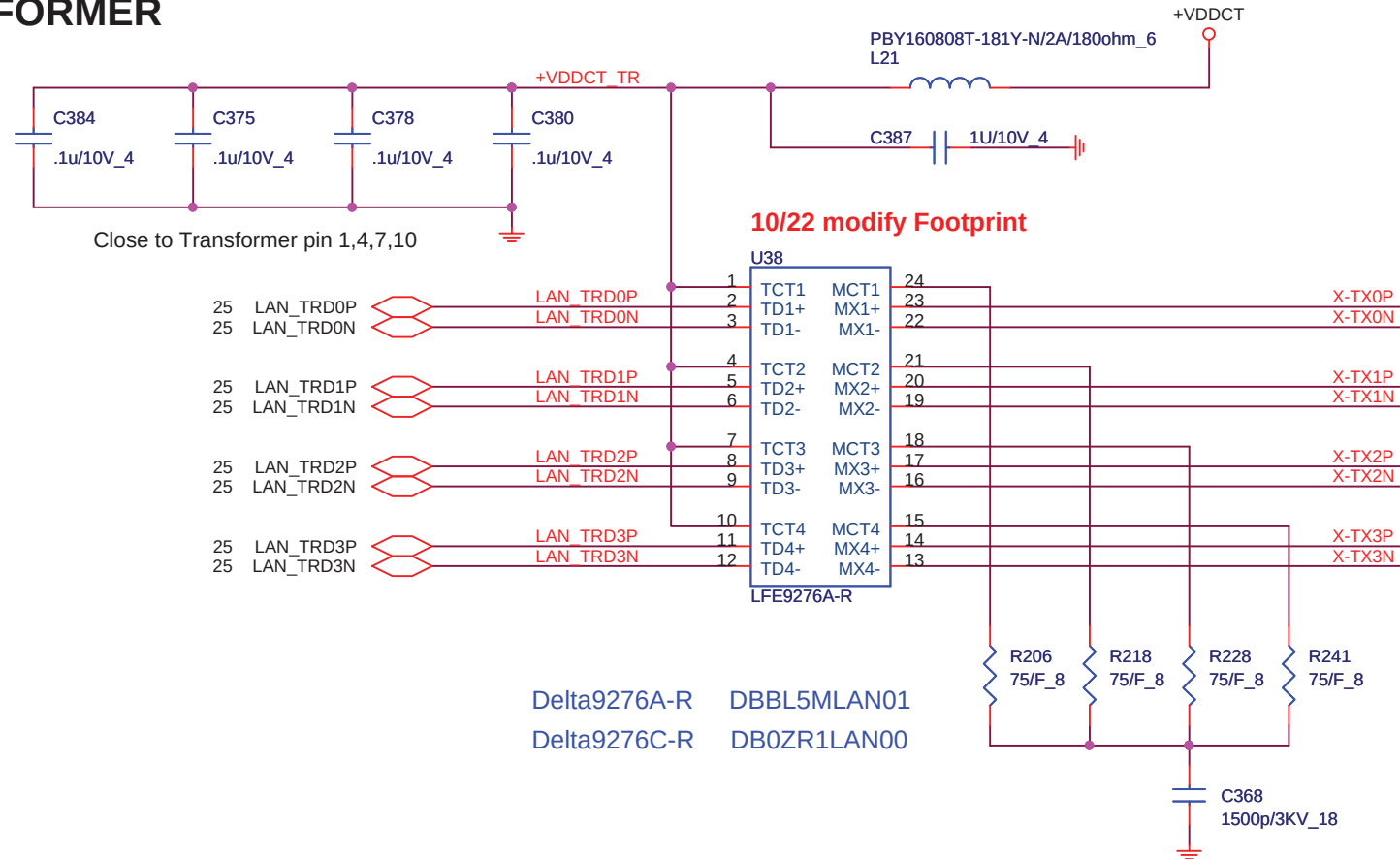


AR8151
5X5mm
40-Pin QFN

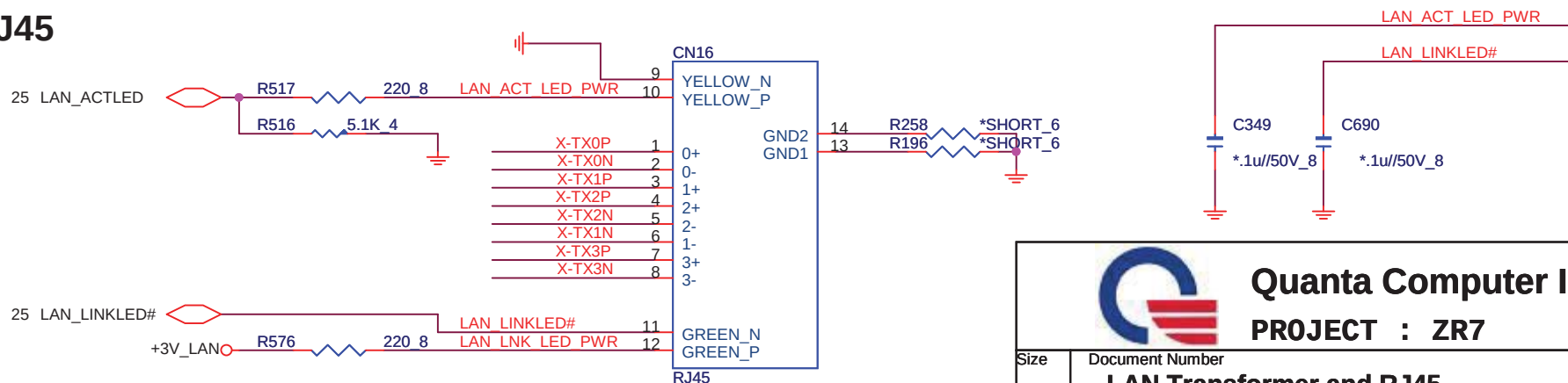


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TRANSFORMER



RJ45



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Size	Document Number	Rev
	LAN Transformer and RJ45	3B
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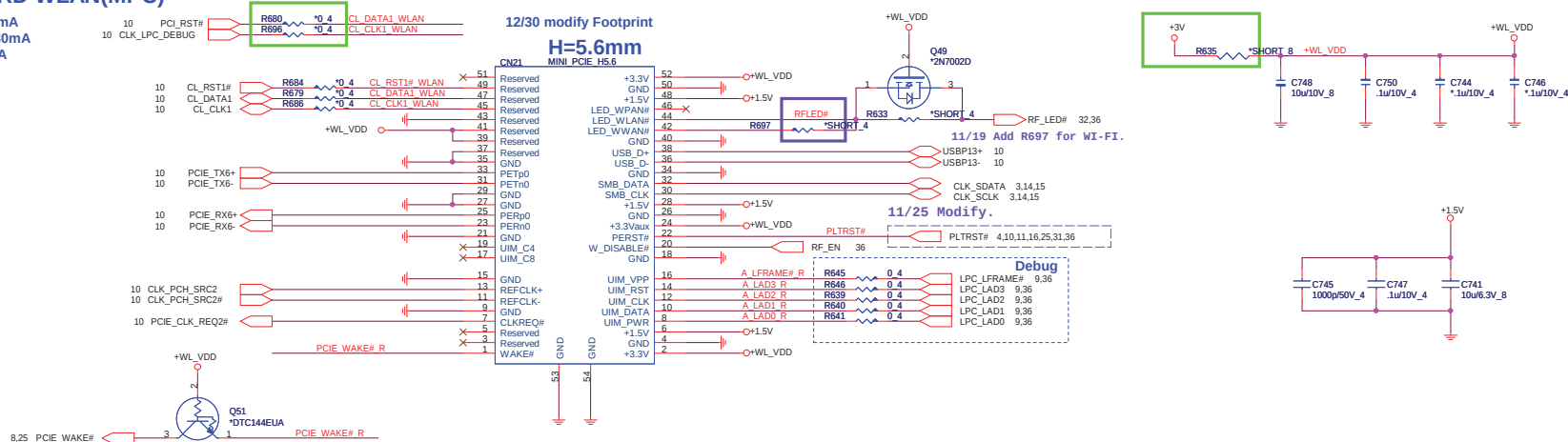
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

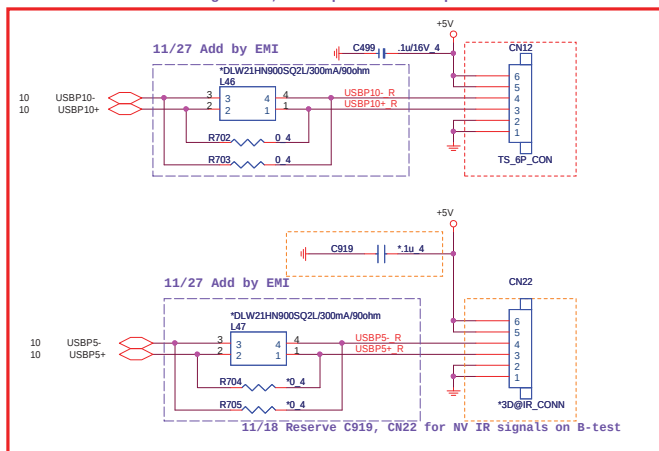
Check LED signal. (active high or low)

12/30 modify Footprint

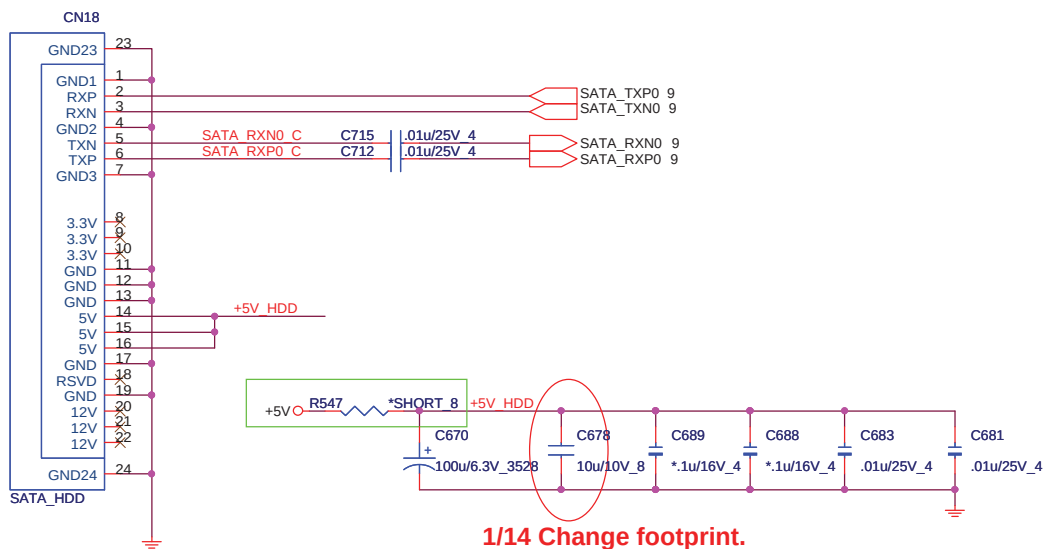
H=5.6mm



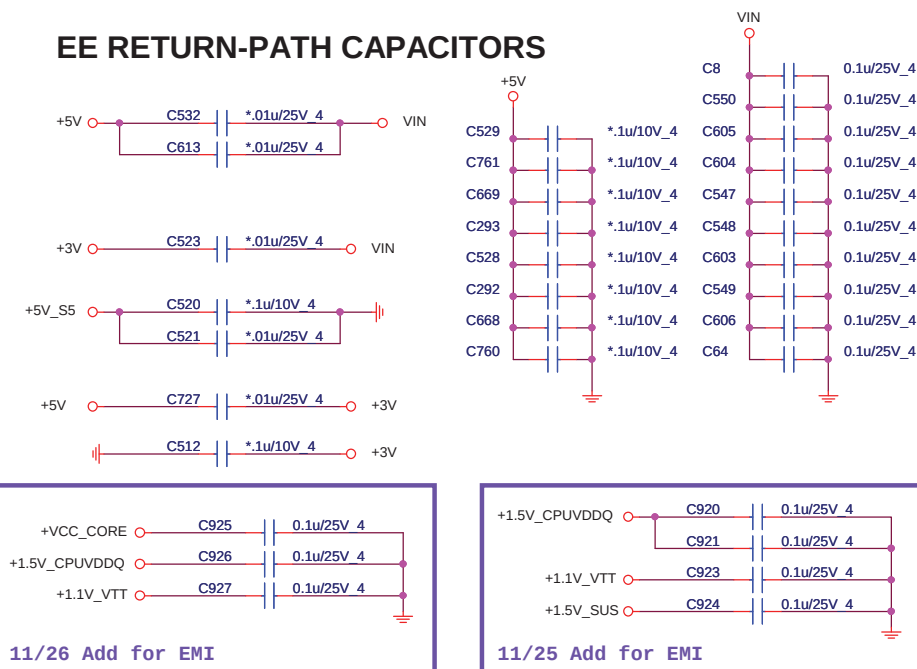
1/8 Change CN12,CN22 6pin conn footprint for Touch Screen.



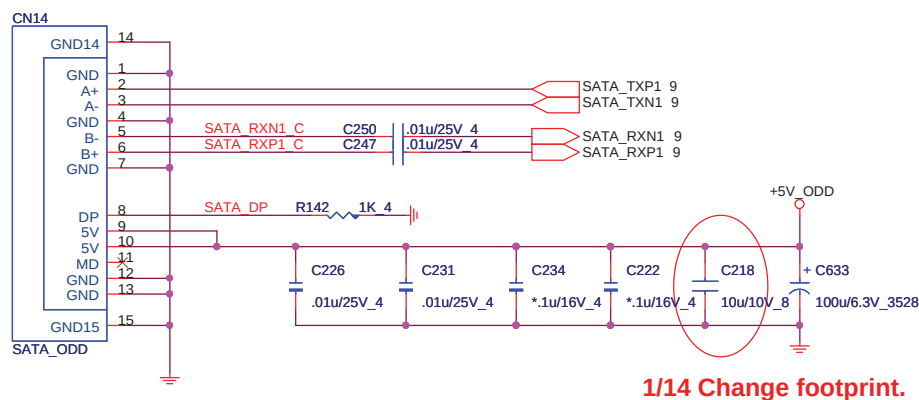
MAIN SATA HDD



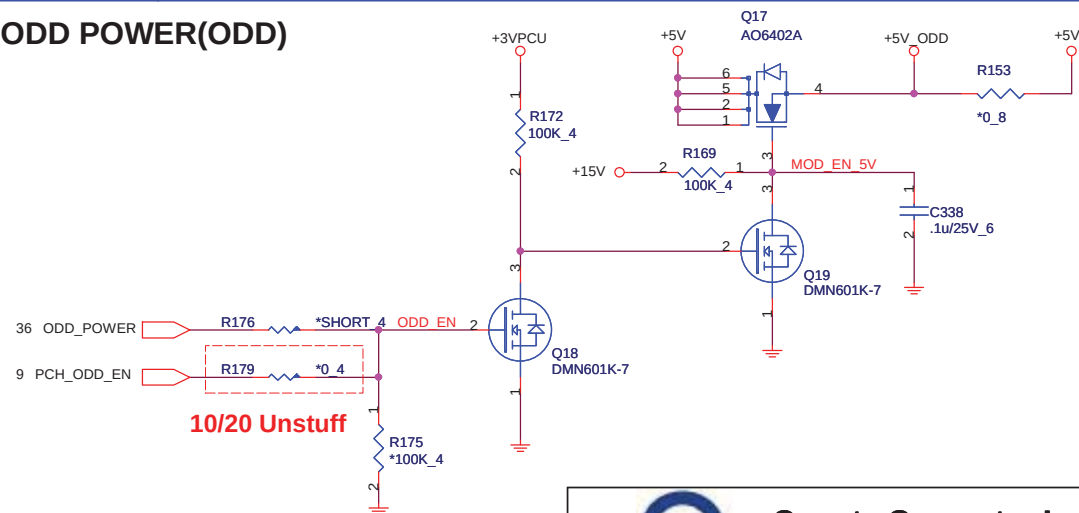
EE RETURN-PATH CAPACITORS



ODD (SATA)



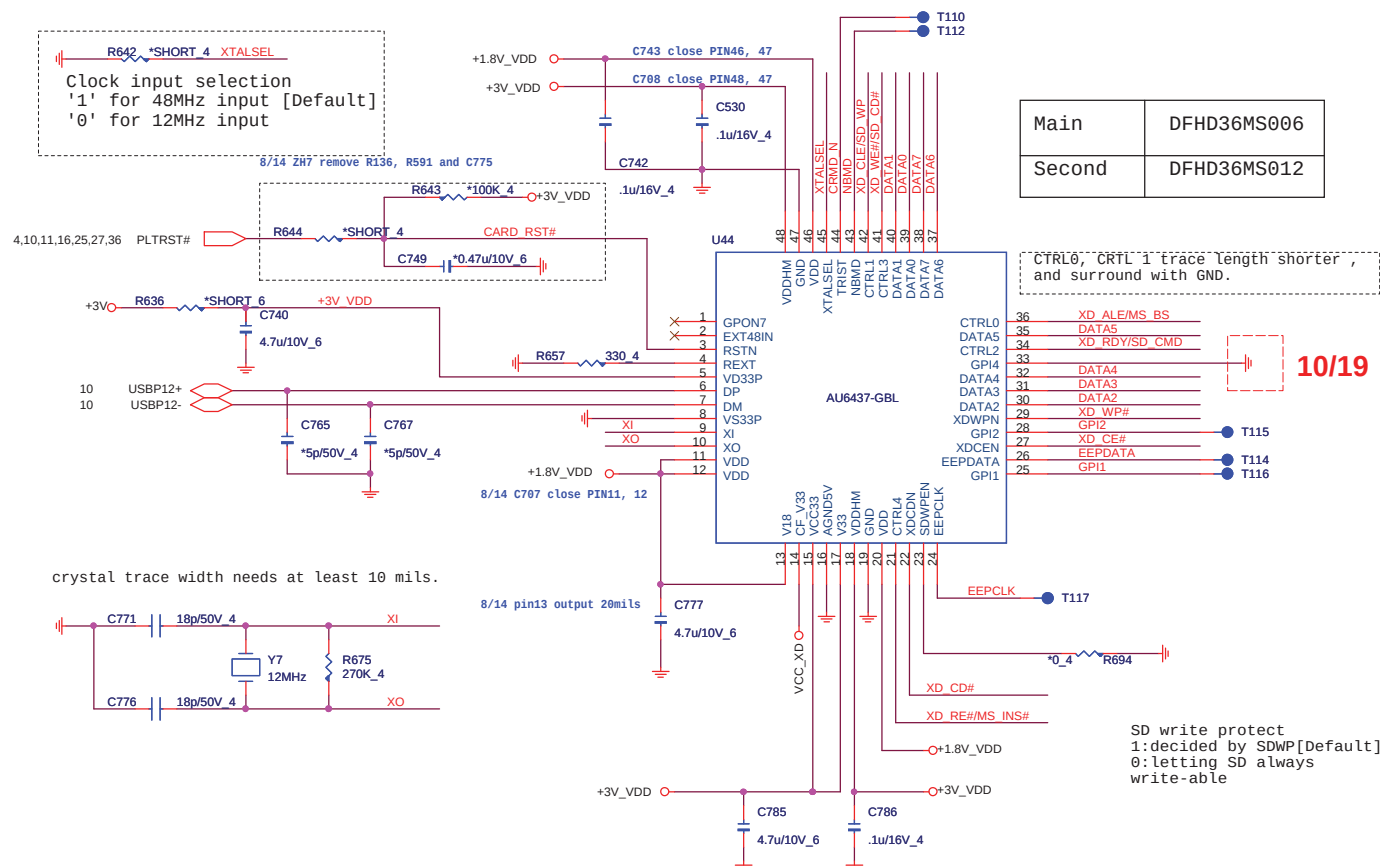
ODD POWER(ODD)



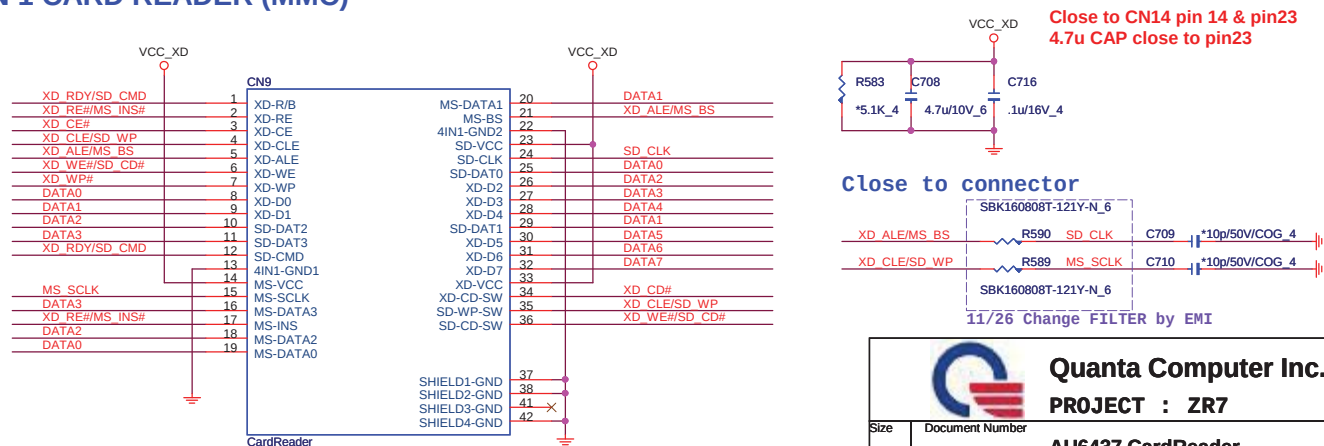
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Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	3B
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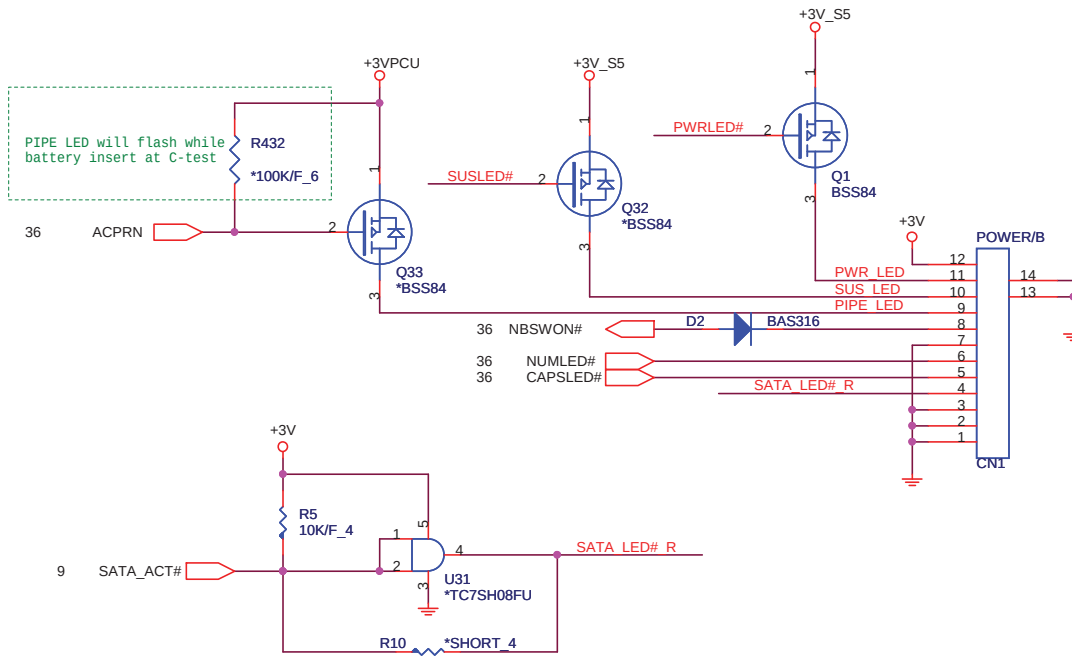
CARD READER Controller



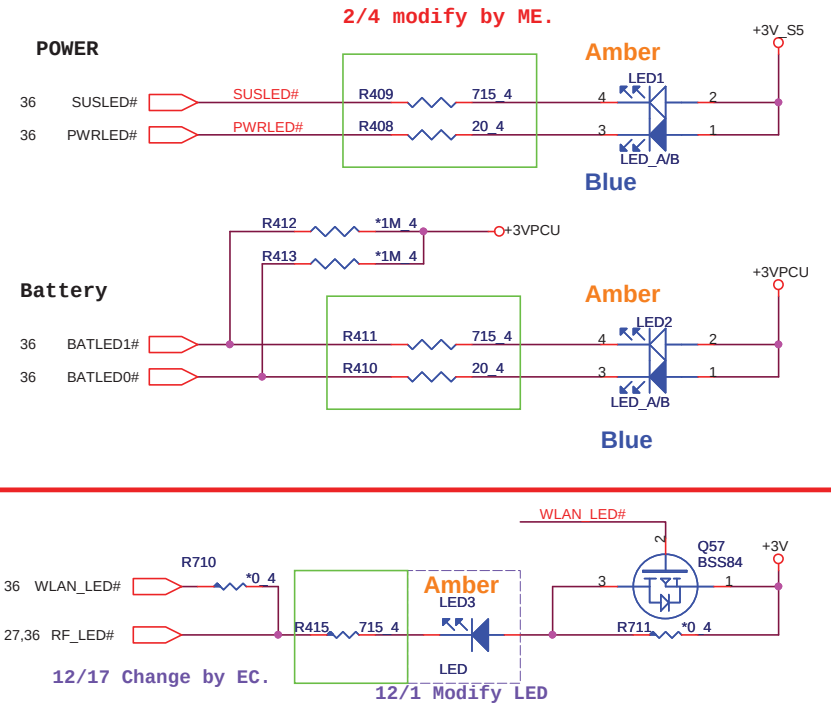
4 IN 1 CARD READER (MMC)



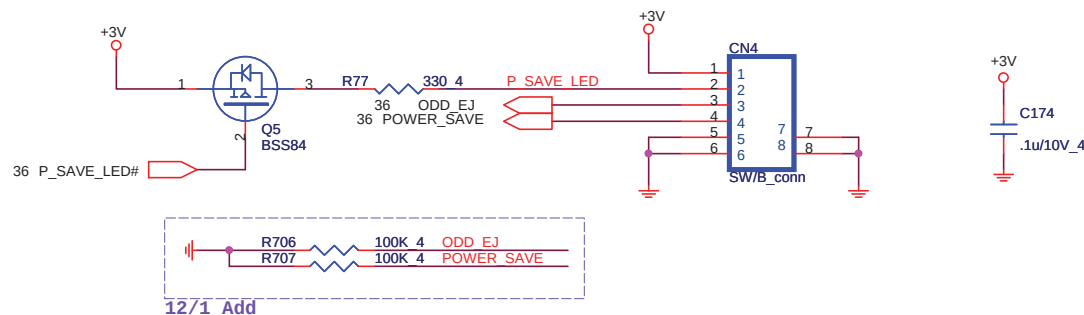
POWER BOARD CONN(UIF)



LED

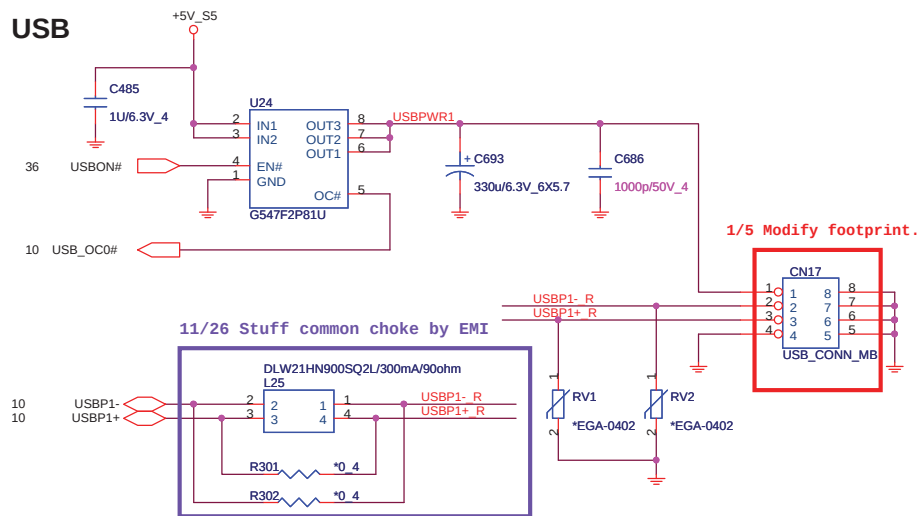


SW /B

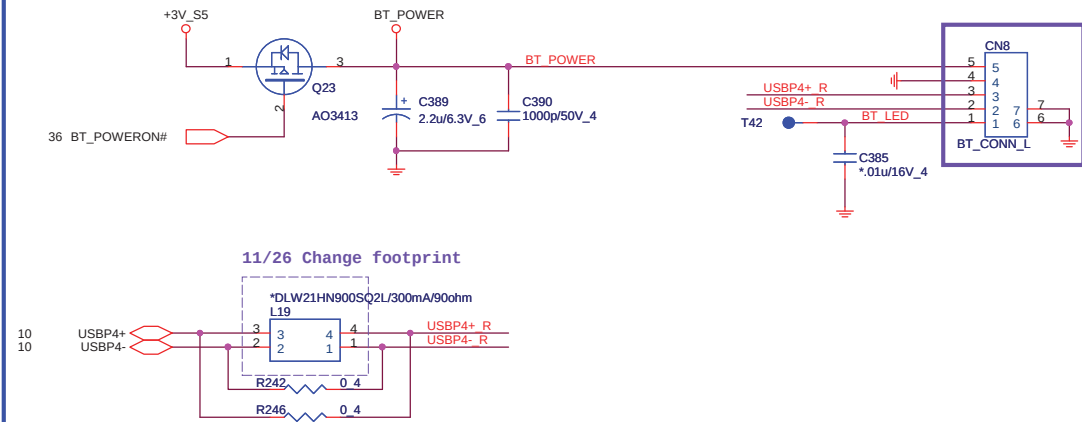


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		3B
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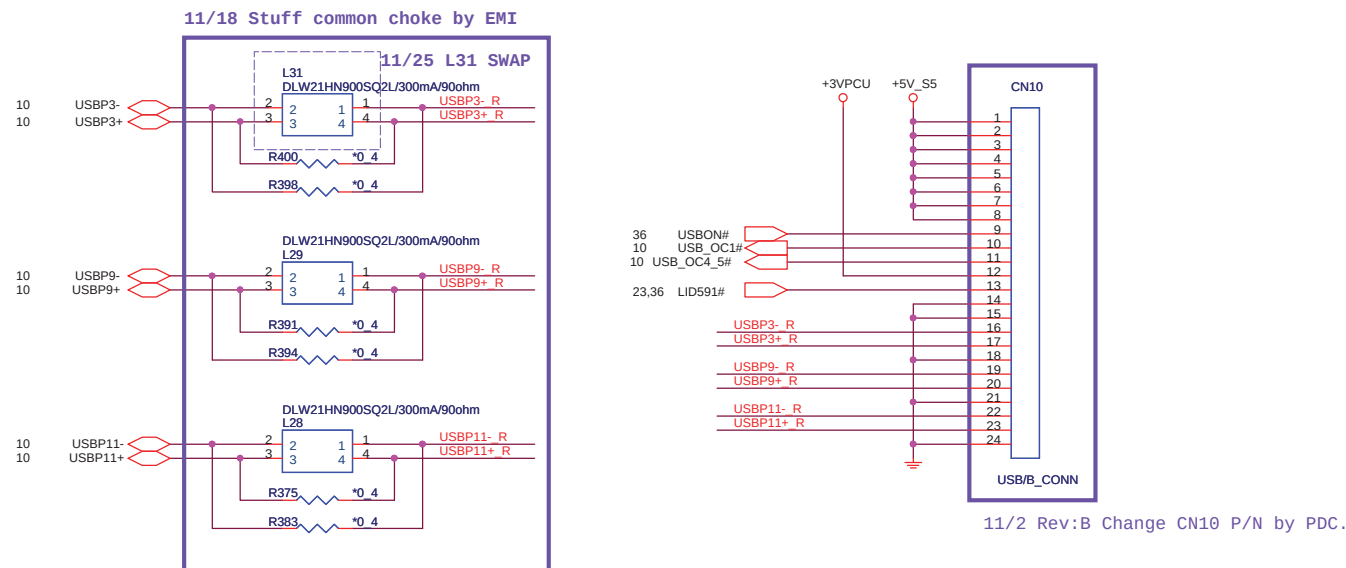
USB

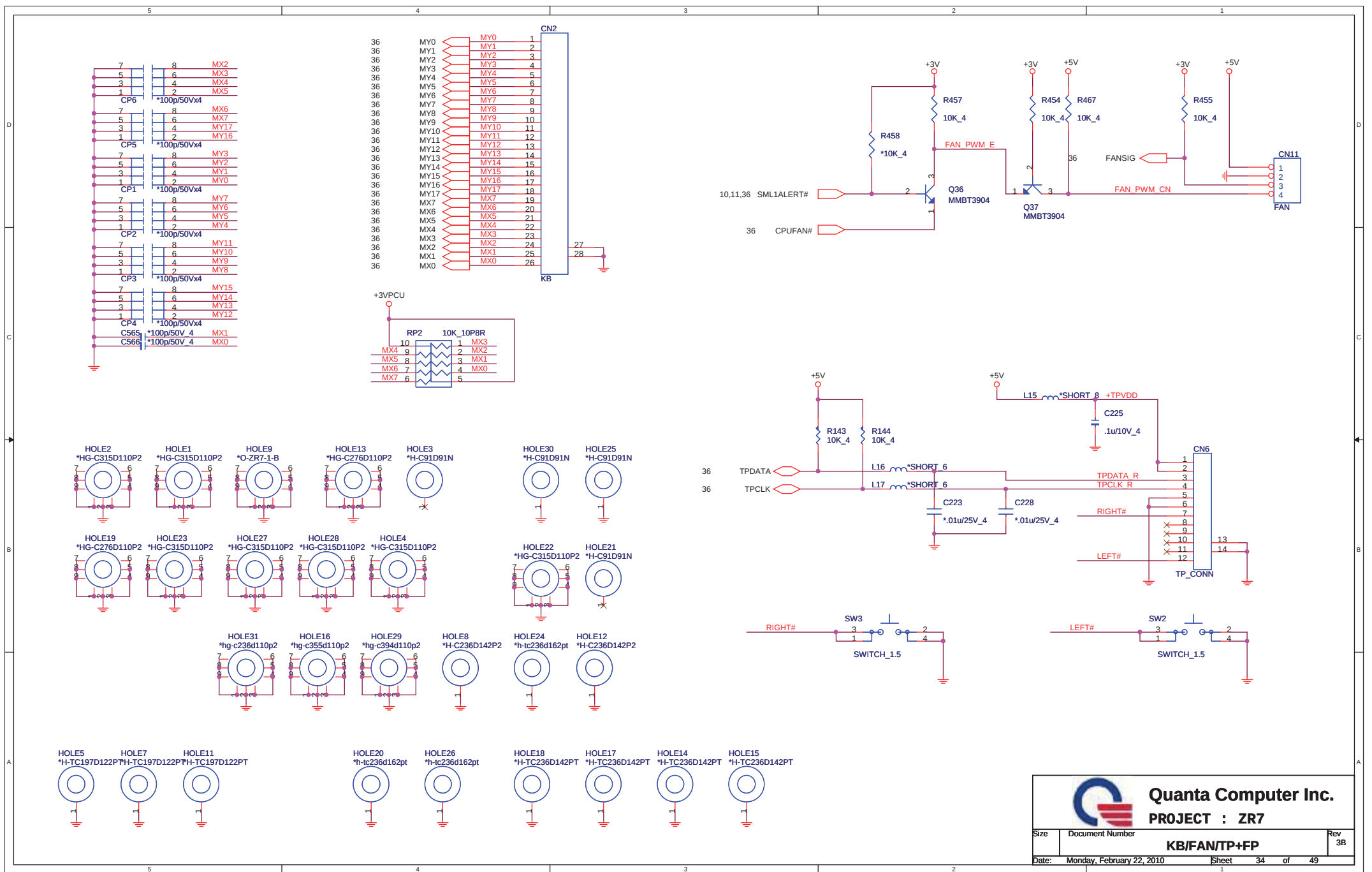


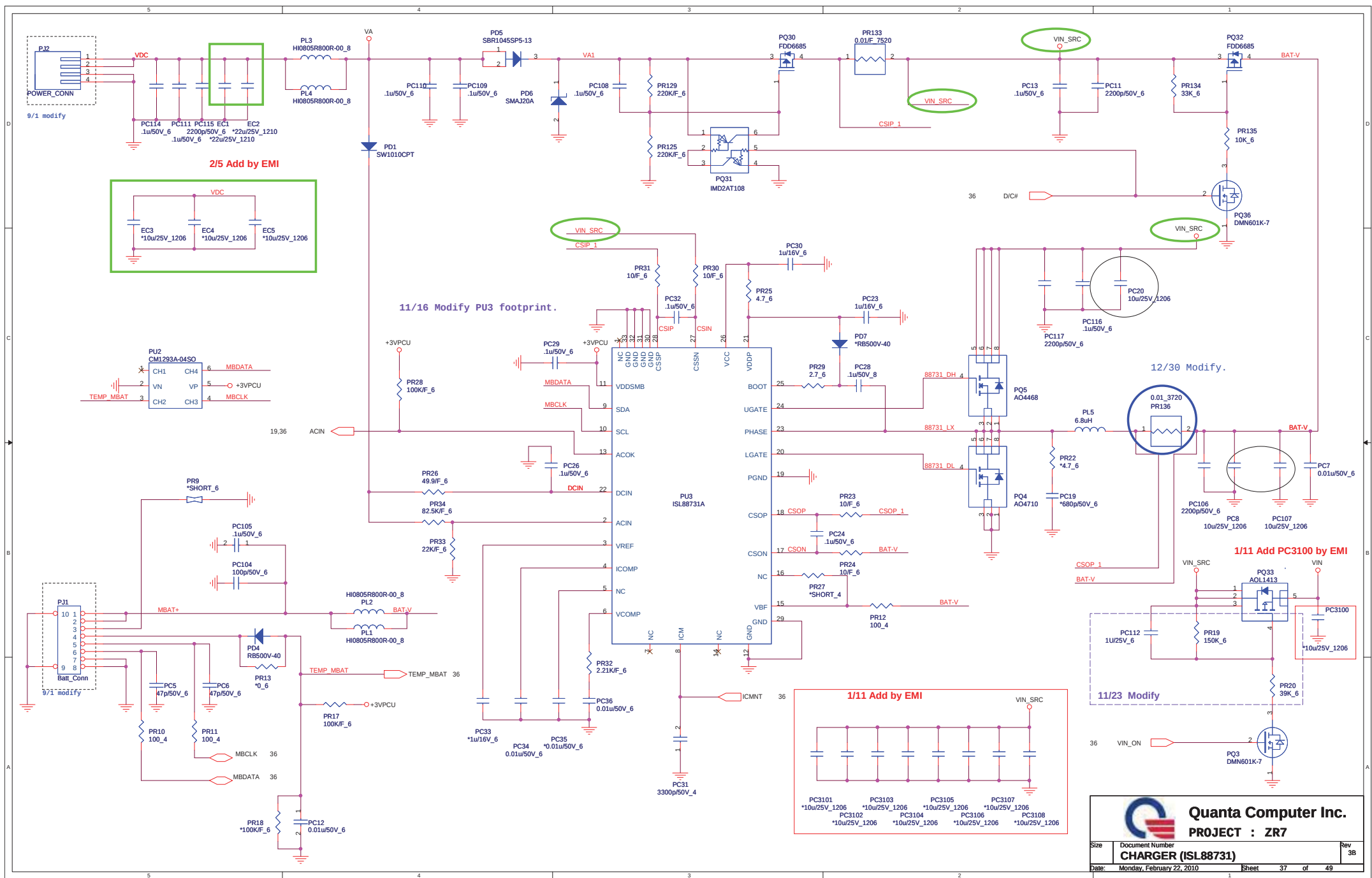
BLUETOOTH CONNECTOR

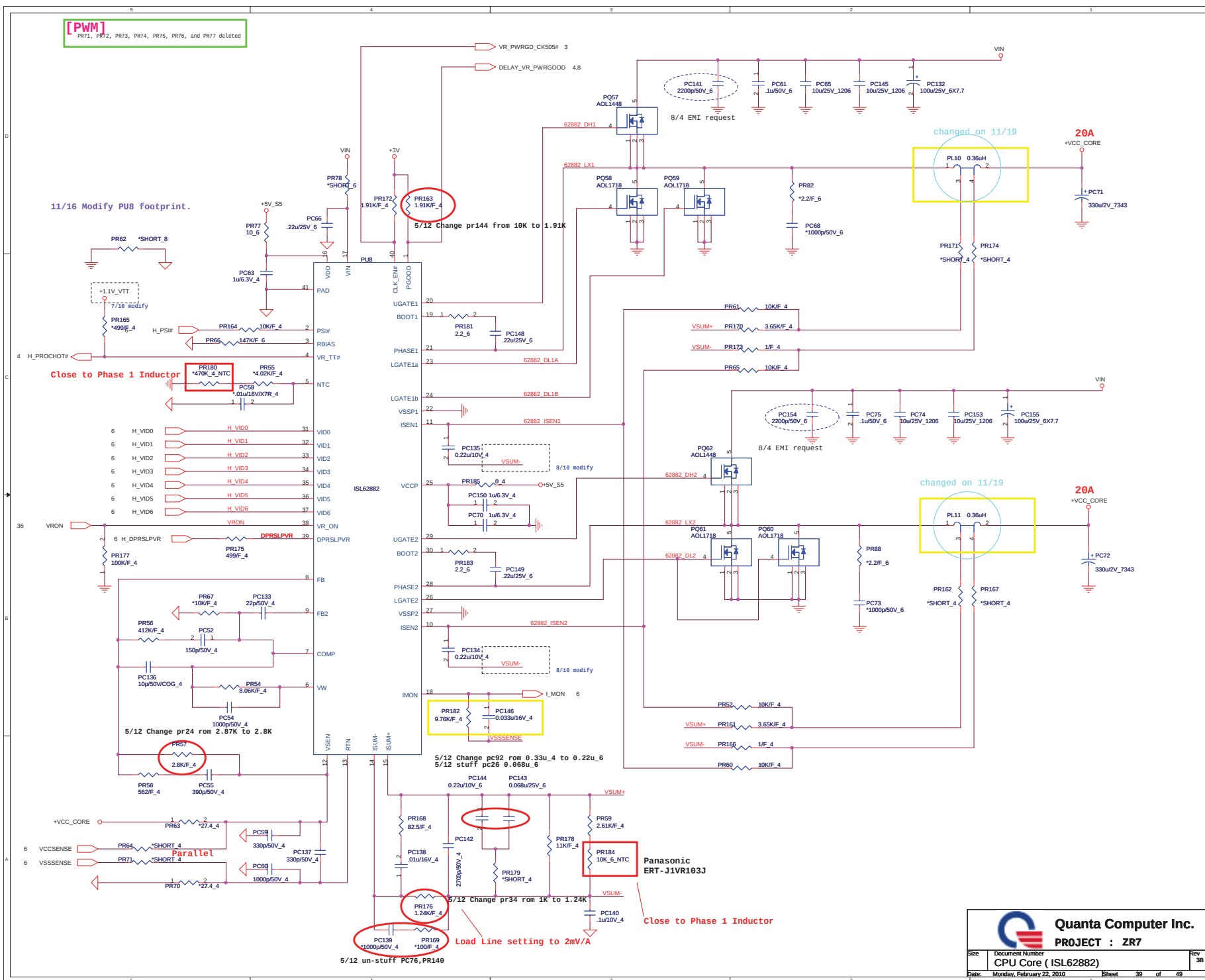


USB/B



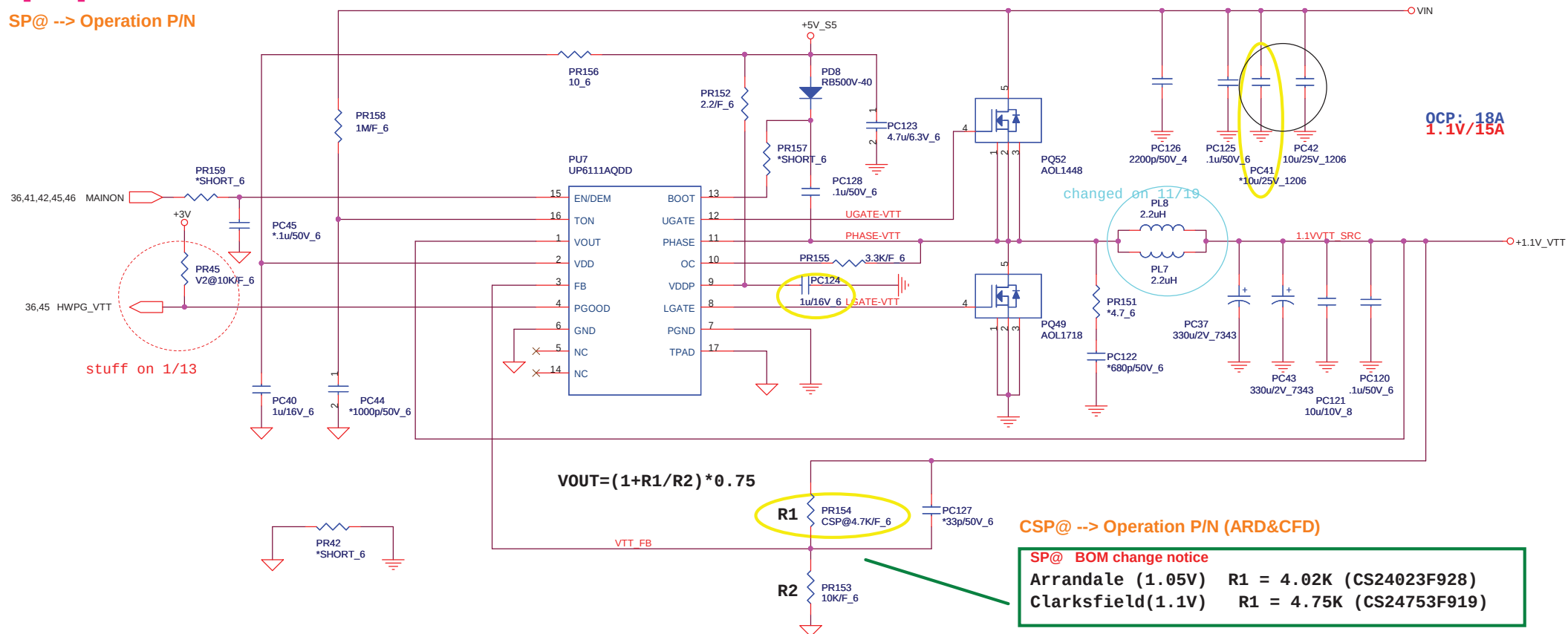






[PWM]

SP@ --> Operation P/N



$$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * T_{ON})$$

$$T_{ON} = 3.85p * 1M * 1 / (V_{in} - 0.5)$$

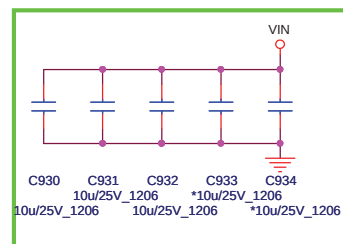
$$Frequency = 1 / (0.0036767) = 272K$$

A01718 Rdson=3~4.3mOhm

$$L(ripple\ current) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.64A$$

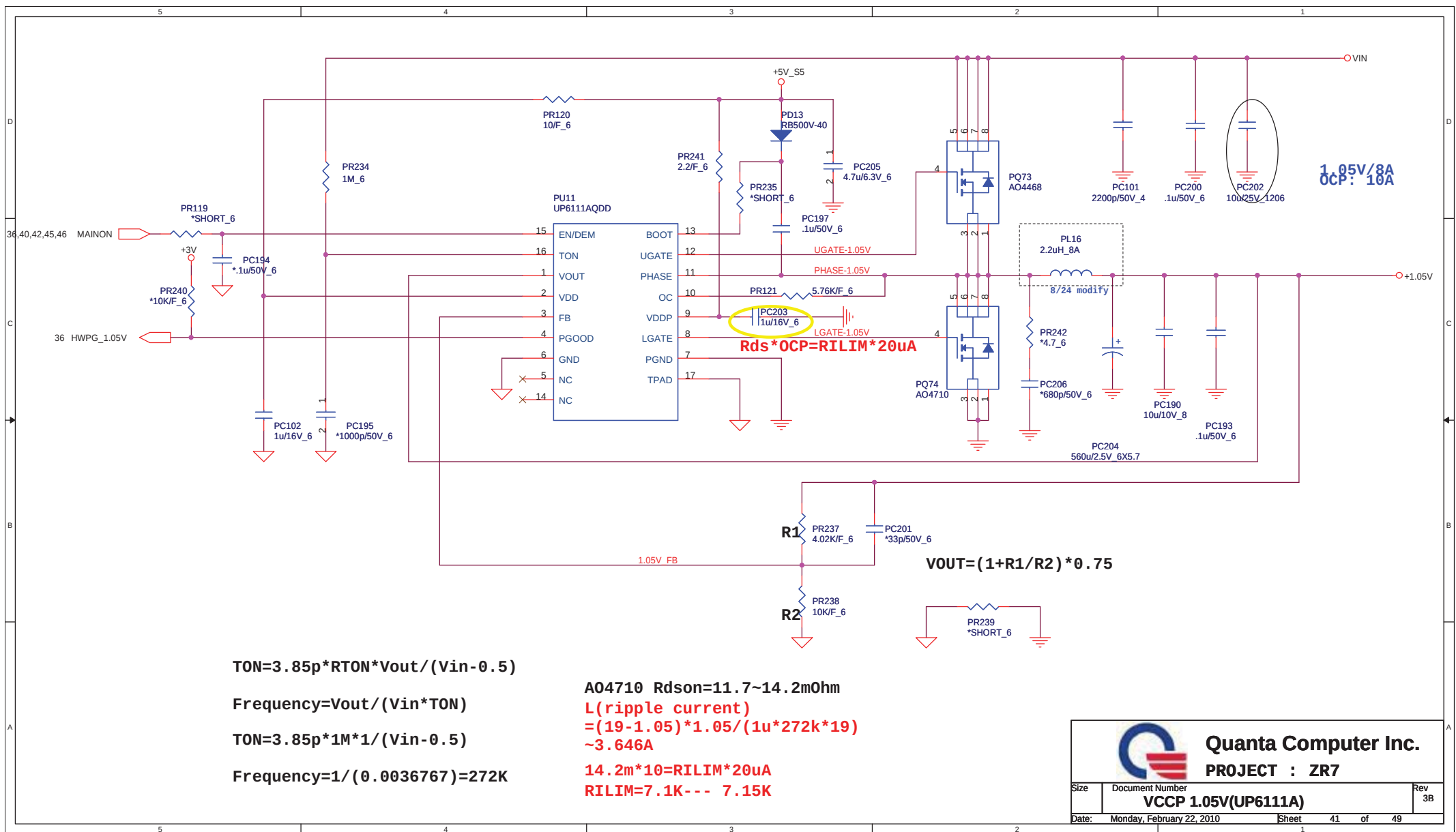
$$4.3m * 18 = RILIM * 20uA$$

$$RILIM = 3.87K \text{ --- } 3.92K$$



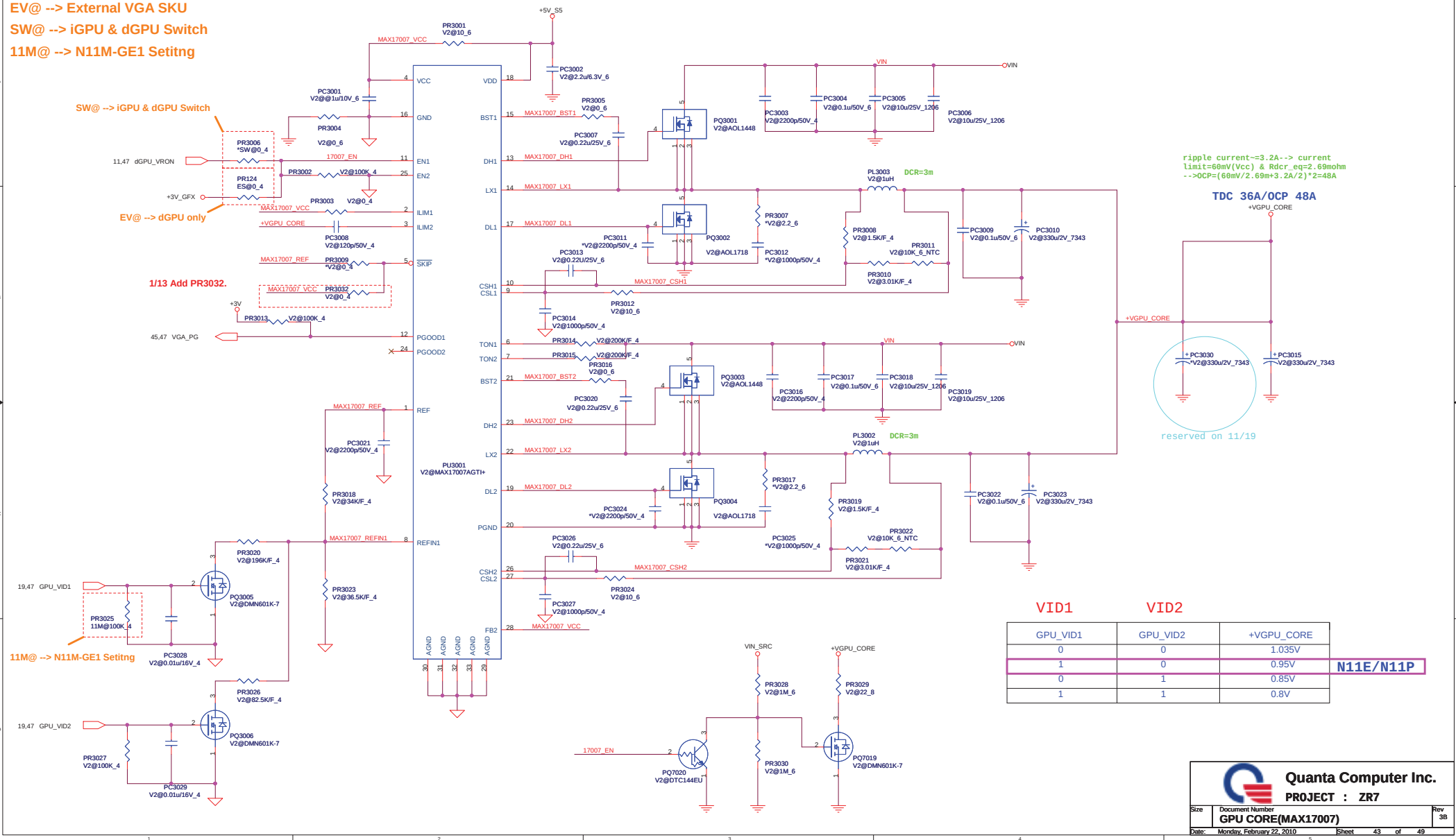
2/11 Add C930-C934 by monitor test.

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		3B
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	+VTT (UP6111A)	
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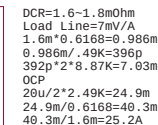


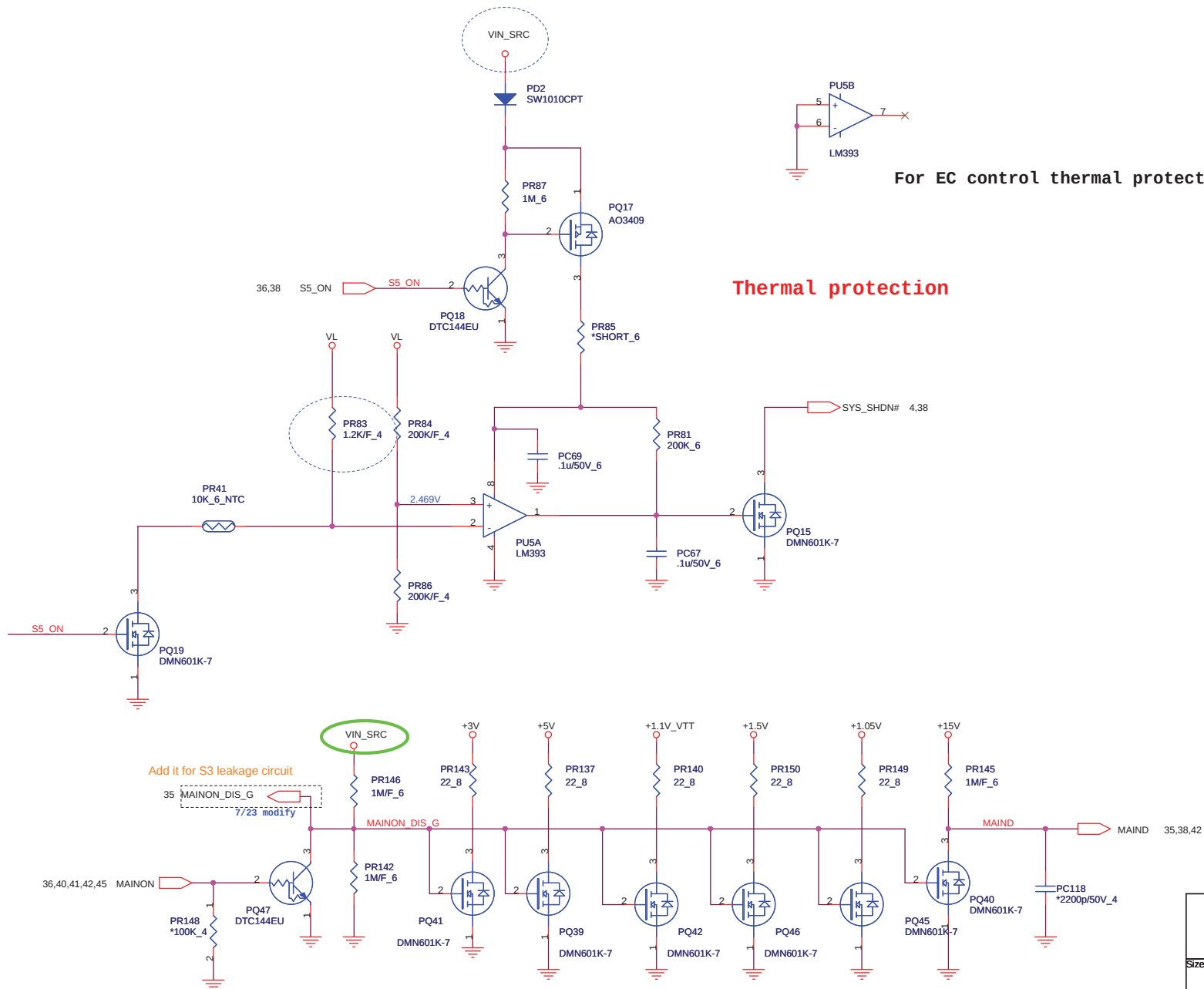
V2@ --> Two Phase dGPU only
 EV@ --> External VGA SKU
 SW@ --> iGPU & dGPU Switch
 11M@ --> N11M-GE1 Seting

11/16 Change VGPU_CORE to two phase solution.

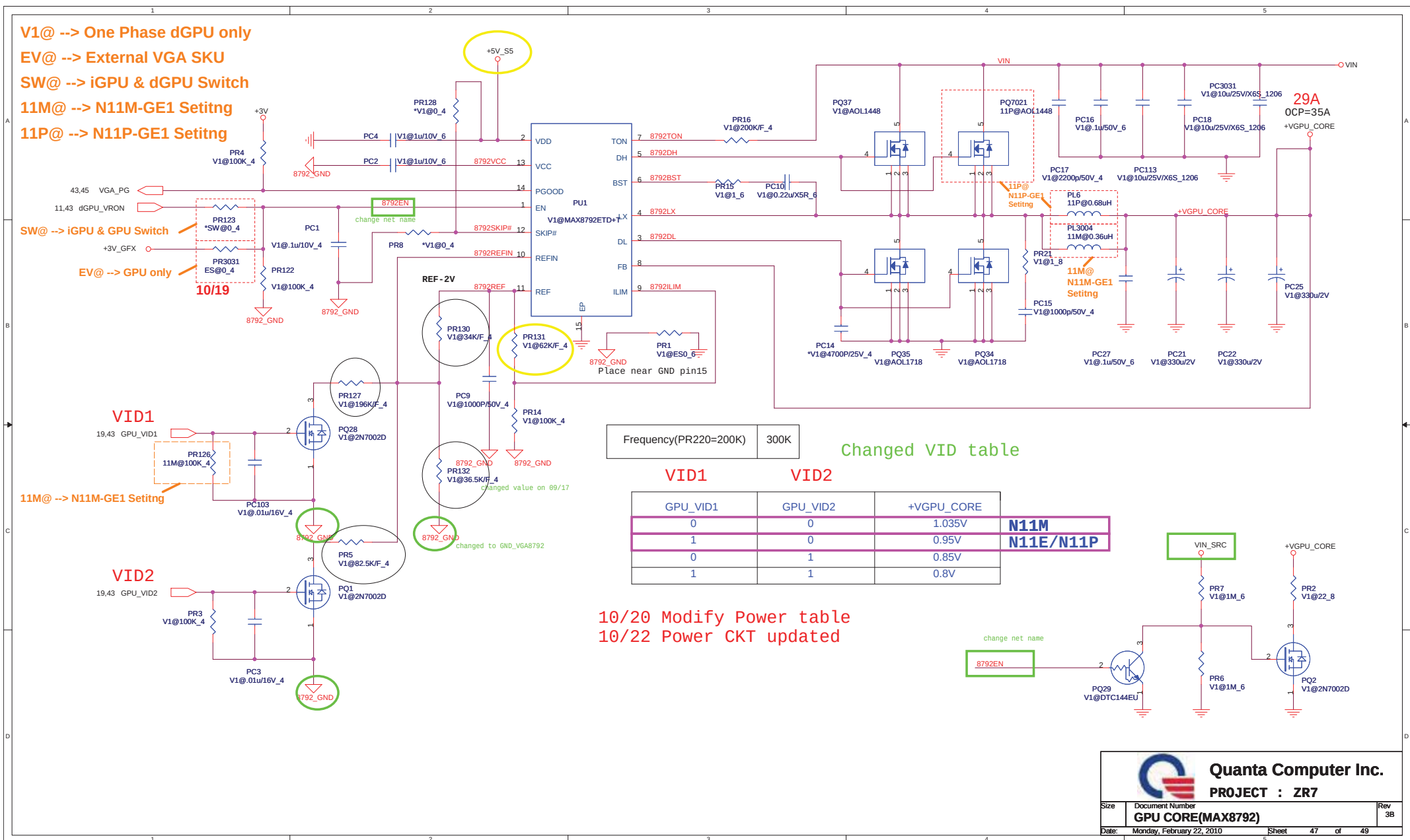


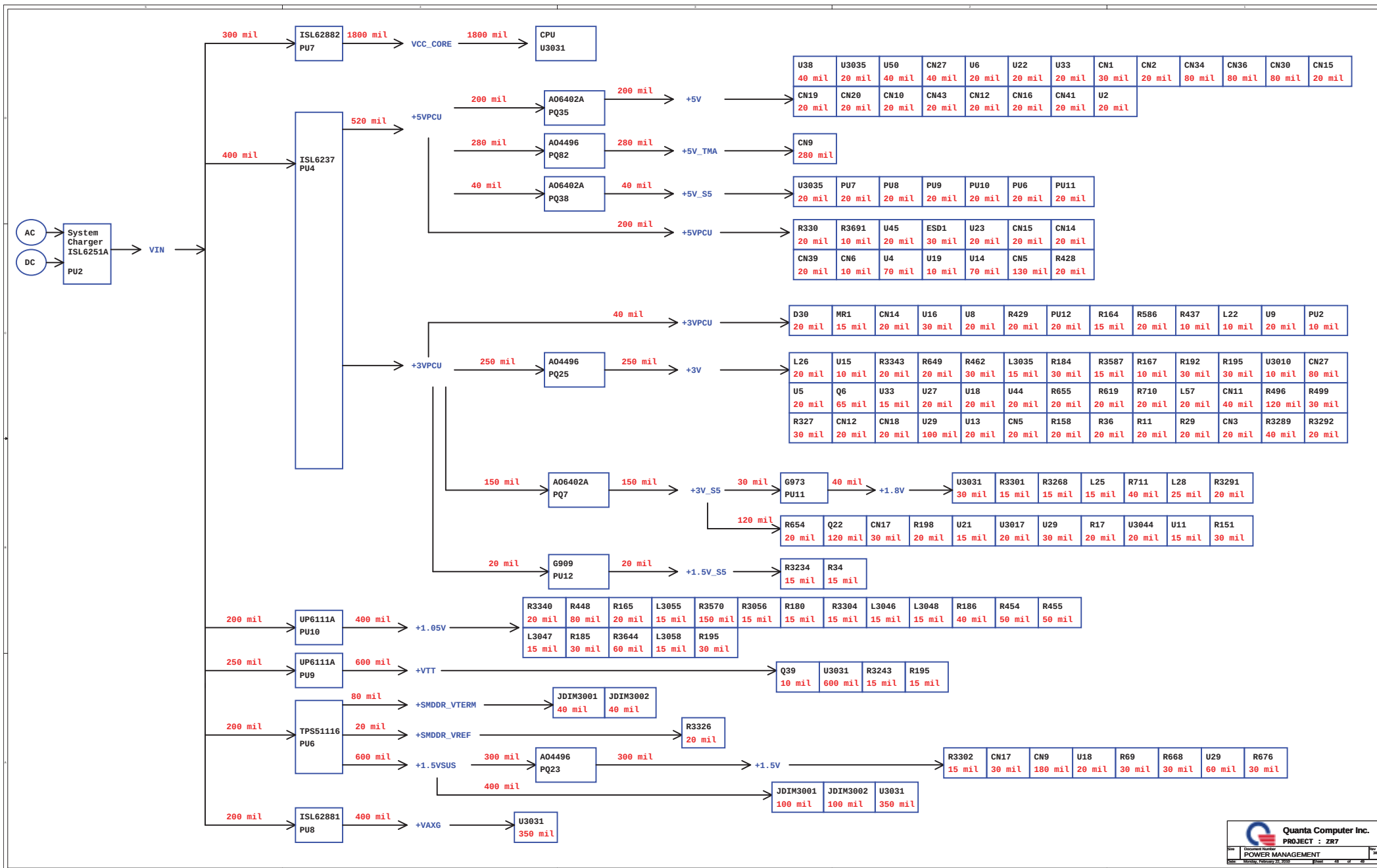
AR@ --> ARD CPU





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	Thermal Protection	3B
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Model		REV	CHANGE LIST	MODEL	ZR7		
					FROM	To	
ZR7 MB	2A	11/2 Page33	Change CN10 P/N by PDC.		1A	2A	
		11/5 Page9	change R338 and R584 to 10K ohm by checklist.		1A	2A	
		11/5 Page10	Add R699 connect XTAL25_IN to Gnd on EV sku and stuff Xtal components by checklist.		1A	2A	
		11/5 Page12	un-stuff R318 and del C499 and Add R698 contact VCCLAN to GND by checklist.		1A	2A	
		11/9 Page32	change W/L LED signal to control by EC.		1A	2A	
		11/9 Page36	Add EC pin82/112 for W/L LED control by EC.		1A	2A	
		11/12 Page35	PR806, PQ222 no stuff.		1A	2A	
		11/12 Page45	Add PR243,PR244 for option.		1A	2A	
		11/16 Page23	CN5 Add LVDS signal to two channel and change CN3 to 8pin conn.		1A	2A	
		11/16 Page43	GPU VCORE power change to two phase solution.		1A	2A	
		11/16 Page27	Add CN12 8pin conn for Touch Screen by ME.		1A	2A	
		11/16 Page44	Change P06 footprint by SMT.		1A	2A	
		11/16 Page45	Change PL15 footprint to CHOKE-PCMC663T-3R39N-NB4 by SMT.		1A	2A	
		11/16 Page30	Change P08 footprint to qfn40-SXS-4-41p-0.750-smt by SMT.		1A	2A	
		11/16 Page37	Change P03 footprint to QFN28-SXS-5-33P-SMT by SMT.		1A	2A	
		11/18 Page10	Delete R597, C444,C445 for cancel 3c function.		1A	2A	
		11/18 Page30	R368,R393 modify from 47ohm to 56ohm by Realtek.		1A	2A	
		11/18 Page10	Change BOARD_ID0-2 to BOARD_ID1-3.		1A	2A	
		11/18 Page11	Change GP107 to BOARD_ID0 and reserve R439 PD.		1A	2A	
		11/18 Page36	Add D23 to connect to dGPU_PWRON on EV sku.		1A	2A	
		11/18 Page9	Change P/N follow ZR7B that use right angle connector.		1A	2A	
		11/18 Page27	Reserve C919, CN22 for NV IR signals on B-test.		1A	2A	
		11/19 Page3	Change U30 PN to AL003197002 by vendor.		1A	2A	
		11/19 Page31	Change CN9 footprint & P/N follow ZR7B.		1A	2A	
		11/19 Page27	Add R897 for WI-FI.		1A	2A	
		11/19 Page11	Add R442, R440 to dGPU_PWRON_R and stuff R321 on EV sku.		1A	2A	
		11/19 Page23	Modify CN5 pin define.		1A	2A	
		11/20 Page45	Add PR124 on EV sku.		1A	2A	
		11/20 Page13	2-14 change core logic cap .1uF CH410032E35 to CH4102K1B03 by SMT.		1A	2A	
		11/20 Page45	del 3k power circuit.		1A	2A	
		11/20 Page34	del HOLE10, Add HOLES,HOLE6, HOLE7, HOLE10, HOLE11, HOLE12, HOLE14, HOLE15, HOLE17, HOLE18, HOLE20, HOLE24, HOLE25, HOLE26, HOLE30 P/N		1A	2A	
		11/25 Page10	Q26,Q29 change to unstuff , Add R700,R701 0 ohm for S3 leakage		1A	2A	
		11/25 Page20	C151 change to CCF343 package		1A	2A	
		11/25 Page34	Change HOLE10, HOLE12 footprint to H-C230D142P2 , Change HOLES,HOLE7,HOLE11 footprint to H-WC107D122PT ,		1A	2A	
		11/25 Page34	Change HOLE14, HOLE15, HOLE17, HOLE18 footprint to H-C230D142PT , Change HOLE20, HOLE24, HOLE26 footprint to H-C230D162PT ,		1A	2A	
		11/25 Page34	Change HOLE19 footprint to O-ZR7-1-B		1A	2A	
		11/25 Page36	R425 change to dGPU_IDLE# signal and value to SW SKU , R428 change value to SW SKU , R249,R250 change value to unstuff		1A	2A	
		11/25 Page28	Add C920,C921,C923,C924 0.1uF for EMI		1A	2A	
		11/25 Page33	L31 SWAP for Layout House		1A	2A	
		11/25 Page27	Modify L1N57W.7726 net name to PLTR57W		1A	2A	
		11/26 Page33	Change L19,L128 footprint , Stuff L25 common choke & unstuff R301,R302 by EMI		1A	2A	
		11/26 Page23	Change L2 footprint		1A	2A	
		11/26 Page23	Change R589,R590 to FLITER for EMI		1A	2A	
		11/26 Page28	Add C925,C926,C927 for EMI		1A	2A	
		11/26 Page11	Modify R422 Value to IV0 SKU		1A	2A	
		11/27 Page11	Del R440		1A	2A	
		11/27 Page20	C81,C105 change CC0603 package		1A	2A	
		11/27 Page16	C84,C109 change CC0603 package		1A	2A	
		11/27 Page23	Add CN5 pin45 to GND		1A	2A	
		11/27 Page20	Add L46,L47,R702,R703,R704,R705 by EMI		1A	2A	
11/27 Page10	Modify C699,C703 to 27pF		1A	2A			
11/27 Page18	Modify C601,C606 to 27pF		1A	2A			
12/1 Page27	Modify CN12 to 6 pin connector		1A	2A			
12/1 Page32	Modify LED3 & Add R706,R707 PD by EC 000_E1 & POWER_SAVE		1A	2A			
12/1 Page9	Add R708,R709 by SPI ROM		1A	2A			
3A	12/18 Page32	Add R710,R711,Q57 by EC.		2A	3A		
	12/18 Page23	Add R712,R713 by 3D feature.		2A	3A		
	12/18 Page47	Change PL6 footprint to choke-npl136-2r2-smt by SMT.		2A	3A		
	12/29 Page27	Change CN21 footprint to RIPC1-800065F80852X09p1-52P-smt by SMT.		2A	3A		
	12/29 Page23	Add F1 by safety.		2A	3A		
	12/29 Page34	Change Q16, Q45 P/N & add F2 by HMDI submit and safety; del U15, U16, U18.		2A	3A		
	12/29 Page30	Change CN19 color to black P/N: DFTJ08FR120 by ACER.		2A	3A		
	1/5 Page33	Change CN17 footprint to USB-UB1110C-RABED-7F-4P-R-V-SMT by PDC.		2A	3A		
	1/7 Page23	Change Q12 of dGPU_select# signal design by leakage issue.		2A	3A		
	1/8 Page9	Change B71 P/N to DFH02M5784 by ME issue.		2A	3A		
	1/8 Page27	Change CN12,CN22 6pin conn footprint for Touch Screen and IR.		2A	3A		
	1/11 Page23	Add L48 & stuff L2 and un-stuff R28 and R29 by EMI.		2A	3A		
	1/11 Page24	Add C928 by EMI.		2A	3A		
	1/13 Page12,36	Change C711,C382 to 100 6.3V.		2A	3A		
	1/14 Page23	Change LVDS connector Pin4 define from WC to LCDVCC & add J13 by 3D PWR.		2A	3A		
1/14 Page28	Change C218,C678 to 100/10V.8 and footprint 0805.		2A	3A			
3B	2/3 Page 16-22	Change U33 footprint to fcbga973-nvidia-nl1p-es-a1 by NV.		3A	3B		
	2/3 Page 30	Change R368,R393 to 75ohm.		3A	3B		
2A	Power modify:			1A	2A		
	11/19	Take out JP12, JP9, JP5, JP6, JP7, JP19, JP26, JP8, JP38, JP11,JP13, JP15, JP16, JP1, JP17, JP14, JP18.		1A	2A		
	11/19	Page38 Change PC158 value; change PR114 from 151K to 182K, PR115 from 220K to 290K,PR106 from 100K to 1K,PR105 from 200K to 150K.		1A	2A		
	11/19	Page40 Change PL7,PL8 from 1.0uH to 2.2uH.		1A	2A		
	11/19	Page30 Change PL19,PL11 from DC+36TVM000 to CV+18V0M284.		1A	2A		
	11/19	Page43 Reserve PC2030.		1A	2A		
	11/23	Page37 PR19 change to 150K , PR20 change to 35K , PC112 change to 1u Z5V		1A	2A		
3A	12/29 Page47	Change PL7,PL8,PL15,PL16 footprint to CHOKE-PCRC663T-3R39N-SMT by SMT.		2A	3A		
	12/29 Page37	Change PR136 footprint to RC3720-SMT by SMT.		2A	3A		
	1/5 Page37-48	Change footprint from CHOKE-ETQP4LR36WFC to CHOKE-ETQP4LR36WFC-SMT by PDC.		2A	3A		
	1/11 Page37	Add PC3100-PC3109 by EMI.		2A	3A		
	1/11 Page47	Change value of PQ7021,PL6,PL3004 by BOM.		2A	3A		
	1/13 Page43	Reserve PR3032 by PWR.		2A	3A		
	1/13 Page45	Reserve circuit of LCDVCC by PWR.		2A	3A		
3B	2/10 Page37	Reserve ECI-EC5 by EMI.		3A	3B		
	2/11 Page38	Del P03 by power.		3A	3B		
	2/11 Page40	Add C930-C934 by monitor test.		3A	3B		
				3A	3B		
Quanta Computer Inc.		DOC NO.	PROJECT MODEL :	ZR7	APPROVED BY:	DATE:	2009/11/06
Change list2			PART NUMBER:		DRAWING BY:	REVISION:	1A