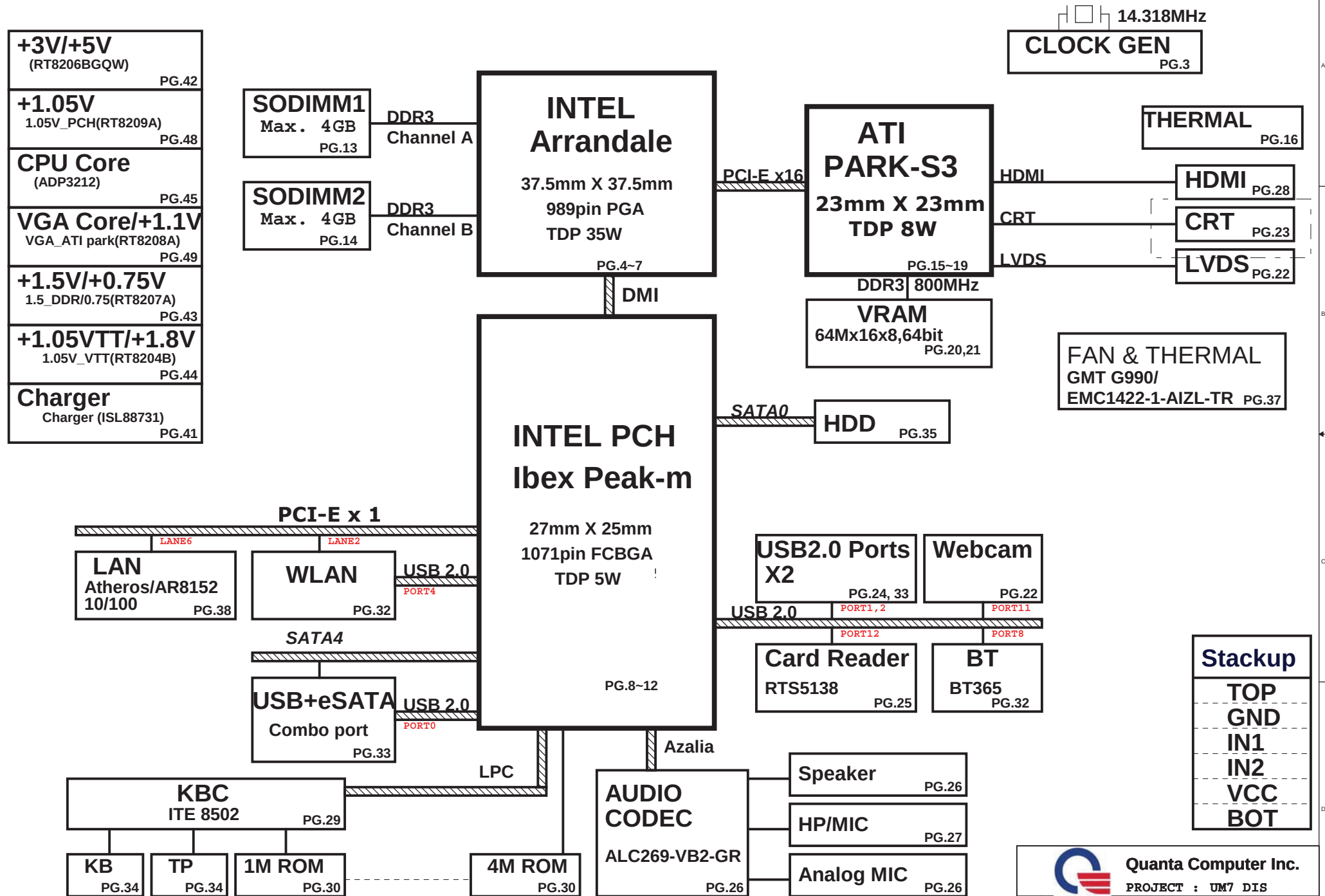


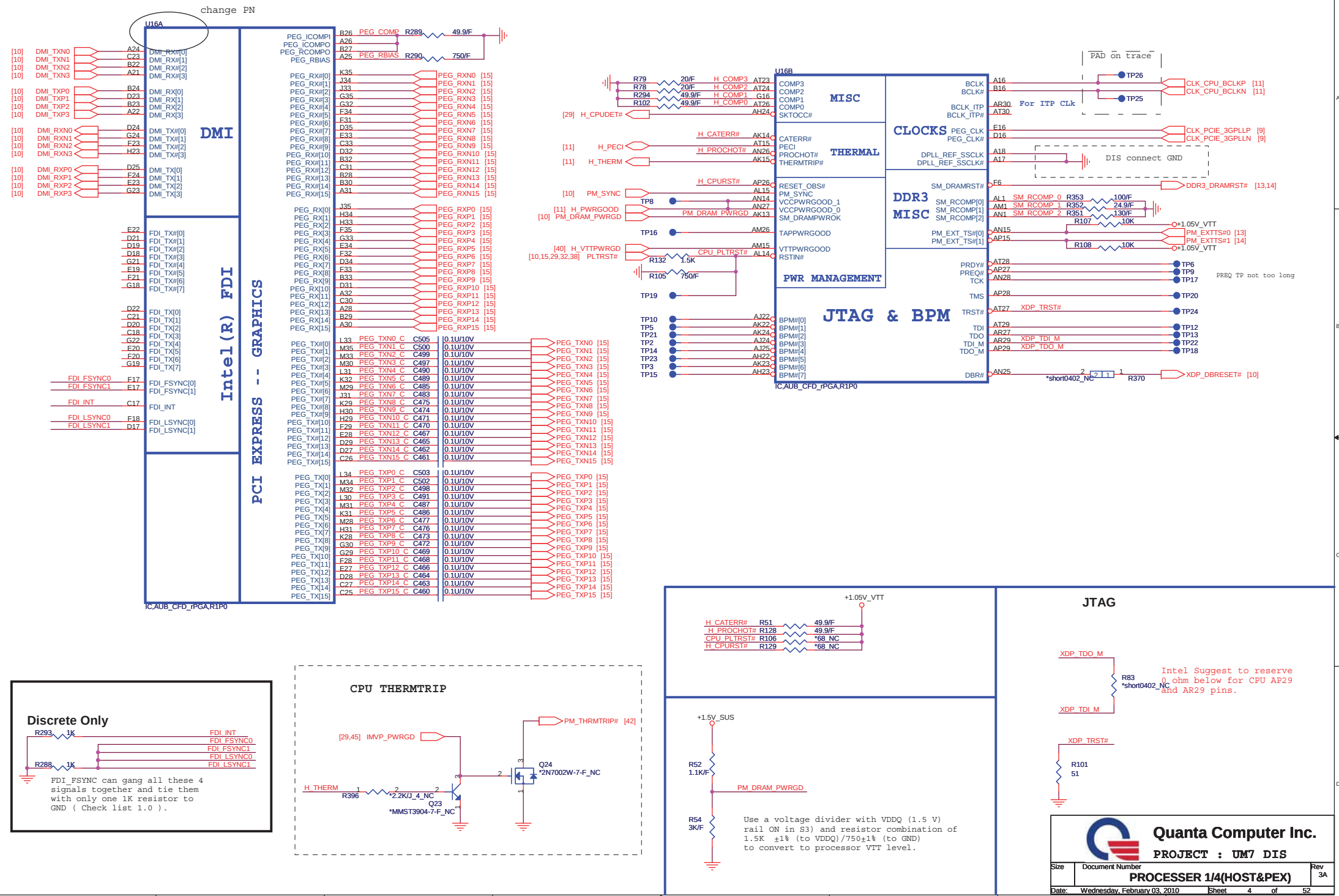
UM7B DISCRETE SYSTEM DIAGRAM



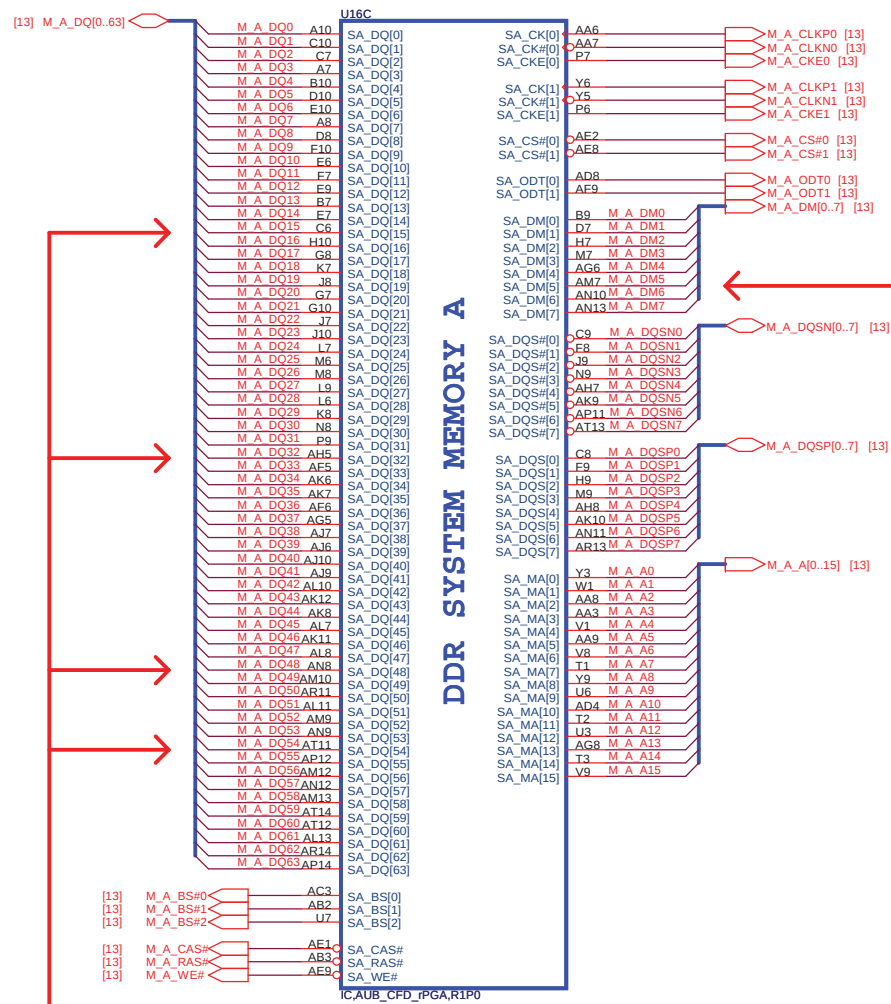
[illegible]

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	23,42,43,44,45,46,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	09,12,30,31	RTC		S0~S5
					S0~S5
+5V_ALW	+5V	37,43,44,47,48	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	30,31,37,42,43,45,47,48	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	12,25,34,37,43,44,45,46,47,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	03,08,09,10,11,12,23,35,37,39,41,46,47,50	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	04,06,14,15,44,47	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	14,15,44	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	08,12,23,24,27,28,29,35,36,3738,47	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,4,8,9,10,11,12,14,15,23,24,26,27,28,29,30,31,33,34,36,37,38,39,41,47	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	6,12,45	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	4,6,11,12,45,46	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	12,33,47	PCH/Min Card	RUN_ON	
+1.05V_PCH	+1.05V	3,8,9,10,12,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	6,46	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	23	LCD Power	LCDVCC_TST_EN & ENVDD	

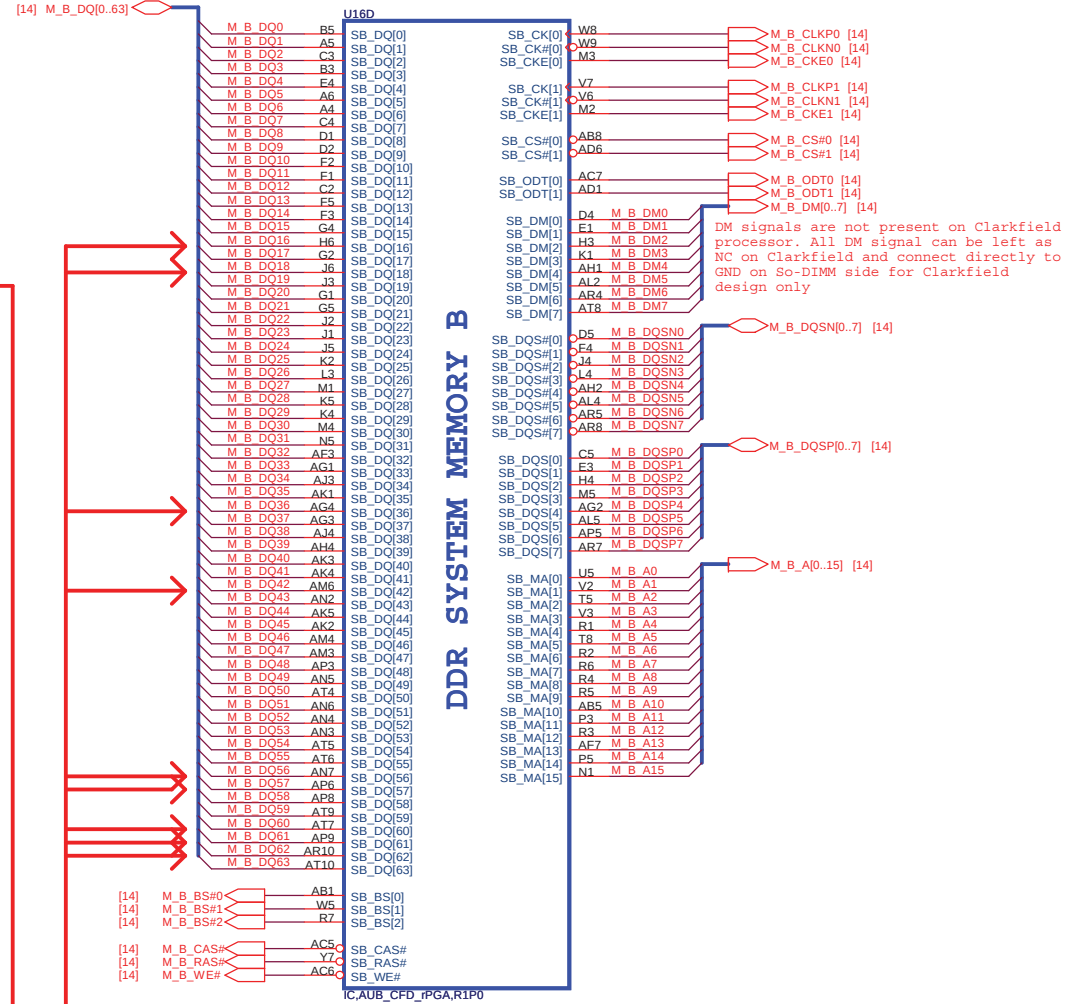
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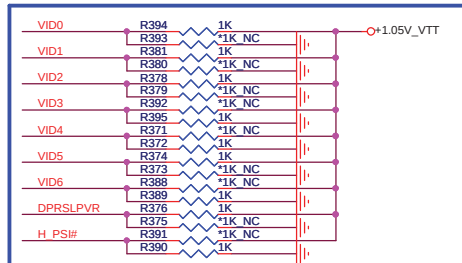
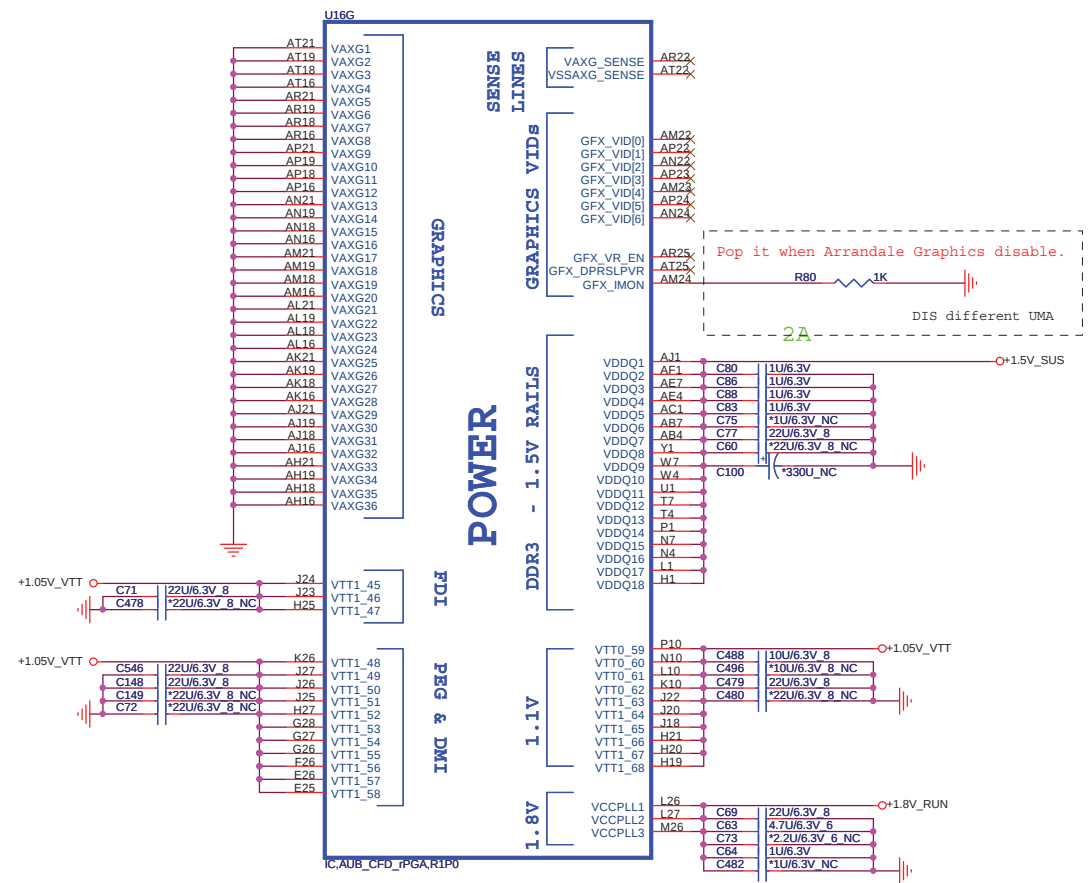
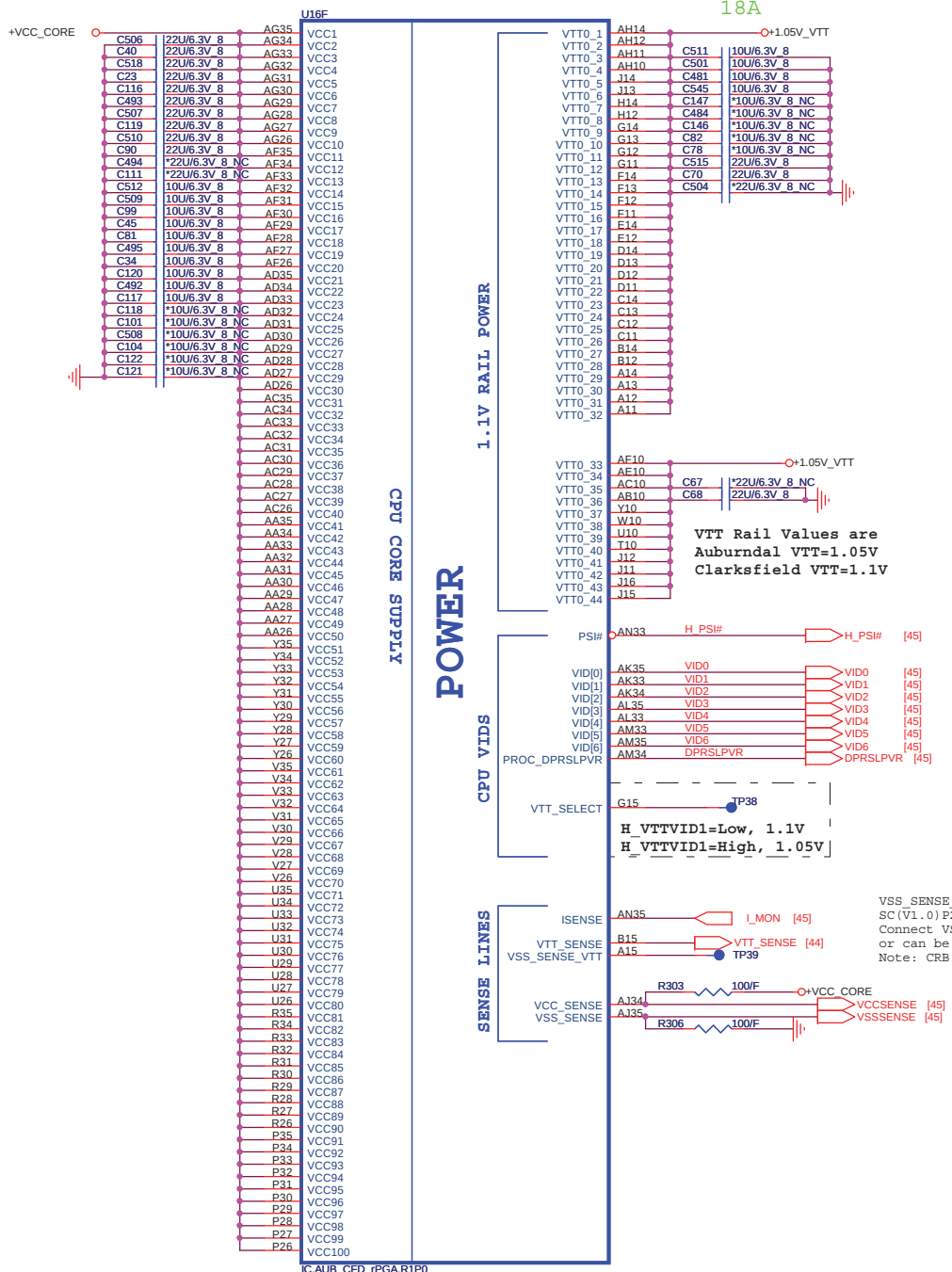
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.



Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data s



HFM_VID : Max 1.4V
LFM_VID : Min 0.65V



U16H			U16I		
AT20	VSS1	VSS81	AE34	K27	VSS161
AT17	VSS2	VSS82	AE33	K9	VSS162
AR31	VSS3	VSS83	AE32	K6	VSS163
AR28	VSS4	VSS84	AE31	K3	VSS164
AR26	VSS5	VSS85	AE30	J32	VSS165
AR24	VSS6	VSS86	AE29	J21	VSS166
AR23	VSS7	VSS87	AE28	J19	VSS167
AR20	VSS8	VSS88	AE27	H35	VSS168
AR17	VSS9	VSS89	AE26	H32	VSS169
AR15	VSS10	VSS90	AE6	H28	VSS170
AR9	VSS11	VSS91	AD10	H26	VSS171
AR6	VSS12	VSS92	AC8	H24	VSS172
AR3	VSS13	VSS93	AC4	H22	VSS173
AP20	VSS14	VSS94	AC2	H18	VSS174
AP17	VSS15	VSS95	AB35	H15	VSS176
AP13	VSS16	VSS96	AB34	H13	VSS177
AP10	VSS17	VSS97	AB33	H11	VSS178
AP7	VSS18	VSS98	AB32	H8	VSS179
AP4	VSS19	VSS99	AB31	H5	VSS180
AP2	VSS20	VSS100	AB30	H2	VSS181
AN34	VSS21	VSS101	AB29	G34	VSS182
AN31	VSS22	VSS102	AB28	G31	VSS183
AN28	VSS23	VSS103	AB27	G20	VSS184
AN20	VSS24	VSS104	AB6	G6	VSS185
AN17	VSS25	VSS105	AA10	G3	VSS186
AM29	VSS26	VSS106	Y8	F30	VSS188
AM27	VSS27	VSS107	Y4	F27	VSS189
AM25	VSS28	VSS108	Y2	F25	VSS190
AM20	VSS29	VSS109	W35	F22	VSS191
AM17	VSS30	VSS110	W34	F19	VSS192
AM14	VSS31	VSS111	W33	F16	VSS193
AM11	VSS32	VSS112	W32	F35	VSS194
AM8	VSS33	VSS113	W31	F32	VSS195
AM5	VSS34	VSS114	W30	F29	VSS196
AM2	VSS35	VSS115	W29	F24	VSS197
AL34	VSS36	VSS116	W28	E18	VSS198
AL31	VSS37	VSS117	W27	E18	VSS199
AL23	VSS38	VSS118	W26	E13	VSS200
AL20	VSS39	VSS119	W6	F11	VSS201
AL17	VSS40	VSS120	V10	E8	VSS202
AL12	VSS41	VSS121	V8	E5	VSS203
AL9	VSS42	VSS122	U4	E2	VSS204
AL6	VSS43	VSS123	U2	D33	VSS205
AL3	VSS44	VSS124	T35	D30	VSS206
AK29	VSS45	VSS125	T34	D26	VSS207
AK27	VSS46	VSS126	T33	D9	VSS208
AK25	VSS47	VSS127	T32	D6	VSS209
AK20	VSS48	VSS128	T31	D3	VSS210
AK17	VSS49	VSS129	T30	C34	VSS211
AK13	VSS50	VSS130	T29	C32	VSS212
AK23	VSS51	VSS131	T28	C29	VSS213
AK20	VSS52	VSS132	T27	C28	VSS214
AK17	VSS53	VSS133	T27	C24	VSS215
AK14	VSS54	VSS134	T26	C22	VSS216
AK11	VSS55	VSS135	R10	C20	VSS217
AK8	VSS56	VSS136	P8	C19	VSS218
AK5	VSS57	VSS137	P4	C16	VSS219
AK2	VSS58	VSS138	P2	B31	VSS220
AK35	VSS59	VSS139	P1	B25	VSS221
AK34	VSS60	VSS140	N35	B21	VSS222
AK31	VSS61	VSS141	N34	B18	VSS223
AK28	VSS62	VSS142	N33	B17	VSS224
AK26	VSS63	VSS143	N32	B13	VSS225
AK23	VSS64	VSS144	N31	B11	VSS226
AK20	VSS65	VSS145	N30	B8	VSS227
AK17	VSS66	VSS146	N29	B6	VSS228
AK14	VSS67	VSS147	N28	B4	VSS229
AK11	VSS68	VSS148	N27	A29	VSS230
AK8	VSS69	VSS149	N26	A27	VSS231
AK5	VSS70	VSS150	M10	A23	VSS232
AK2	VSS71	VSS151	M6	A9	VSS233
AK13	VSS72	VSS152	L35		
AK9	VSS73	VSS153	L32		
AK6	VSS74	VSS154	L29		
AK3	VSS75	VSS155	L8		
AG10	VSS76	VSS156	L5		
AF8	VSS77	VSS157	L2		

CFG0 R313 *3.01K/F NC

CFG3 R309 3.01K/F

CFG4 R310 *3.01K/F NC

CFG7 R311 *3.01K/F NC

U1G6

+M_VREF_DQ_DIMM0 H17 SA_DIMM_VREF

+M_VREF_DQ_DIMM1 H17 SB_DIMM_VREF

CFG0 AM30 CFG[0]

CFG3 AM28 CFG[1]

CFG4 AP31 CFG[2]

CFG7 AL32 CFG[3]

CFG7 AL30 CFG[4]

CFG7 AM31 CFG[5]

CFG7 AM32 CFG[6]

CFG7 AK32 CFG[7]

CFG7 AK31 CFG[8]

CFG7 AK28 CFG[9]

CFG7 AJ28 CFG[10]

CFG7 AN30 CFG[11]

CFG7 AN32 CFG[12]

CFG7 AJ32 CFG[13]

CFG7 AJ29 CFG[14]

CFG7 AJ30 CFG[15]

CFG7 AK30 CFG[16]

CFG7 H16 CFG[17]

CFG7 H16 RSVD_TP_86

CFG7 AP25 RSVD1

CFG7 AL25 RSVD2

CFG7 AL24 RSVD3

CFG7 AL22 RSVD4

CFG7 AJ33 RSVD5

CFG7 AG9 RSVD6

CFG7 M27 RSVD7

CFG7 L28 RSVD8

CFG7 G25 RSVD11

CFG7 G17 RSVD12

CFG7 E31 RSVD13

CFG7 E30 RSVD14

CFG7 B19 RSVD15

CFG7 A19 RSVD16

CFG7 A20 RSVD17

CFG7 B20 RSVD18

CFG7 U9 RSVD19

CFG7 T9 RSVD20

CFG7 AC9 RSVD21

CFG7 AB9 RSVD22

CFG7 C1 RSVD_NCTF_23

CFG7 A3 RSVD_NCTF_24

CFG7 J29 RSVD26

CFG7 J28 RSVD27

CFG7 A34 RSVD_NCTF_28

CFG7 A33 RSVD_NCTF_29

CFG7 C35 RSVD_NCTF_30

CFG7 B35 RSVD_NCTF_31

CFG7 AJ13 RSVD32

CFG7 AJ12 RSVD33

CFG7 AH25 RSVD34

CFG7 AK26 RSVD35

CFG7 AL26 RSVD36

CFG7 AR2 RSVD_NCTF_37

CFG7 AJ26 RSVD38

CFG7 AJ27 RSVD39

CFG7 AP1 RSVD_NCTF_40

CFG7 AP1 RSVD_NCTF_41

CFG7 AP1 RSVD_NCTF_42

CFG7 AP1 RSVD_NCTF_43

CFG7 AP1 RSVD45

CFG7 AP1 RSVD46

CFG7 AP1 RSVD47

CFG7 AP1 RSVD48

CFG7 AP1 RSVD49

CFG7 AP1 RSVD50

CFG7 AP1 RSVD51

CFG7 AP1 RSVD52

CFG7 AP1 RSVD53

CFG7 AP1 RSVD_NCTF_54

CFG7 AP1 RSVD_NCTF_55

CFG7 AP1 RSVD_NCTF_56

CFG7 AP1 RSVD_NCTF_57

CFG7 AP1 RSVD58

CFG7 AP1 RSVD_TP_60

CFG7 AP1 RSVD_TP_61

CFG7 AP1 RSVD_TP_62

CFG7 AP1 RSVD_TP_63

CFG7 AP1 RSVD_TP_64

CFG7 AP1 RSVD_TP_65

CFG7 AP1 RSVD_TP_66

CFG7 AP1 RSVD_TP_67

CFG7 AP1 RSVD_TP_68

CFG7 AP1 RSVD_TP_69

CFG7 AP1 RSVD_TP_70

CFG7 AP1 RSVD_TP_71

CFG7 AP1 RSVD_TP_72

CFG7 AP1 RSVD_TP_73

CFG7 AP1 RSVD_TP_74

CFG7 AP1 RSVD_TP_75

CFG7 AP1 RSVD_TP_76

CFG7 AP1 RSVD_TP_77

CFG7 AP1 RSVD_TP_78

CFG7 AP1 RSVD_TP_79

CFG7 AP1 RSVD_TP_80

CFG7 AP1 RSVD_TP_81

CFG7 AP1 RSVD_TP_82

CFG7 AP1 RSVD_TP_83

CFG7 AP1 RSVD_TP_84

CFG7 AP1 RSVD_TP_85

CFG7 AP1 RSVD_TP_86

CFG7 AP1 RSVD_TP_87

CFG7 AP1 RSVD_TP_88

CFG7 AP1 RSVD_TP_89

CFG7 AP1 RSVD_TP_90

CFG7 AP1 RSVD_TP_91

CFG7 AP1 RSVD_TP_92

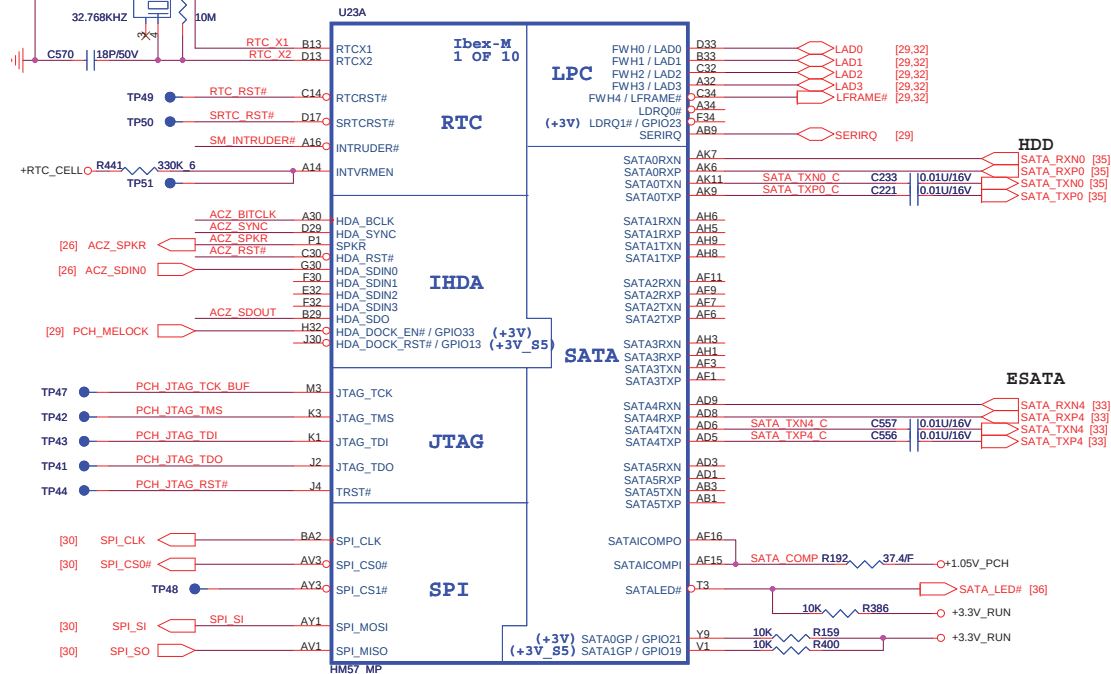
CFG7 AP1 RSVD_TP_93

CFG7 AP1 RS

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

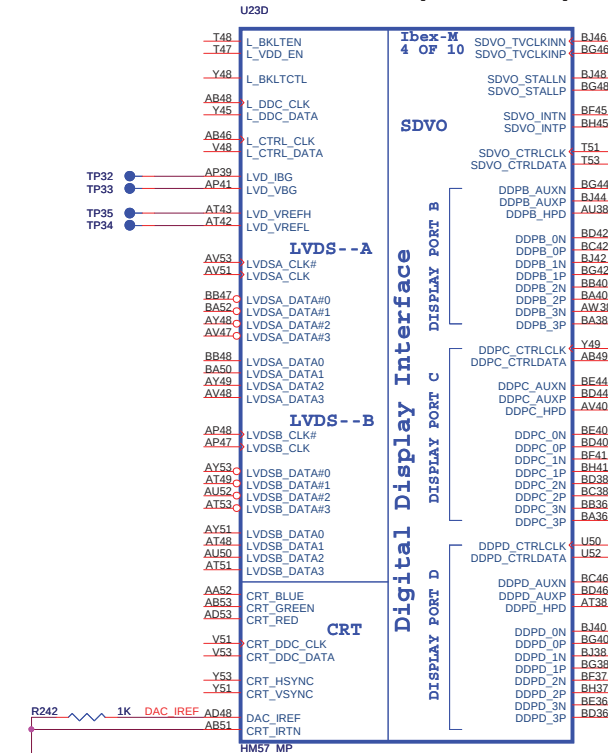
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

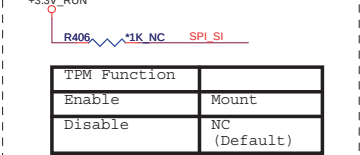


UMA CRT, LVDS&HDMI signals

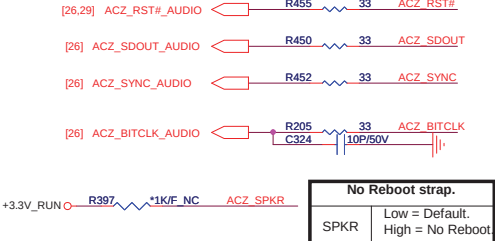
IBEX PEAK-M (LVDS,DDI)



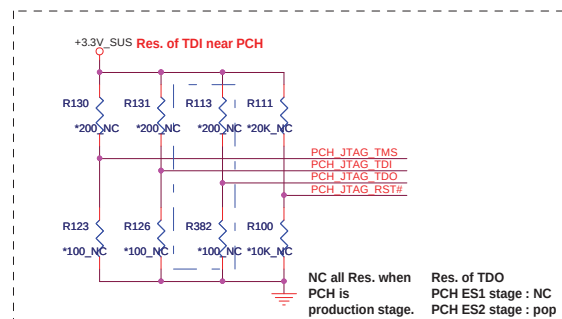
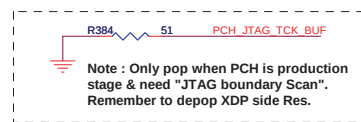
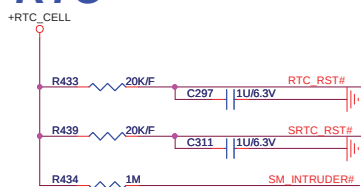
iTPM ENABLE/DISABLE



For AUDIO



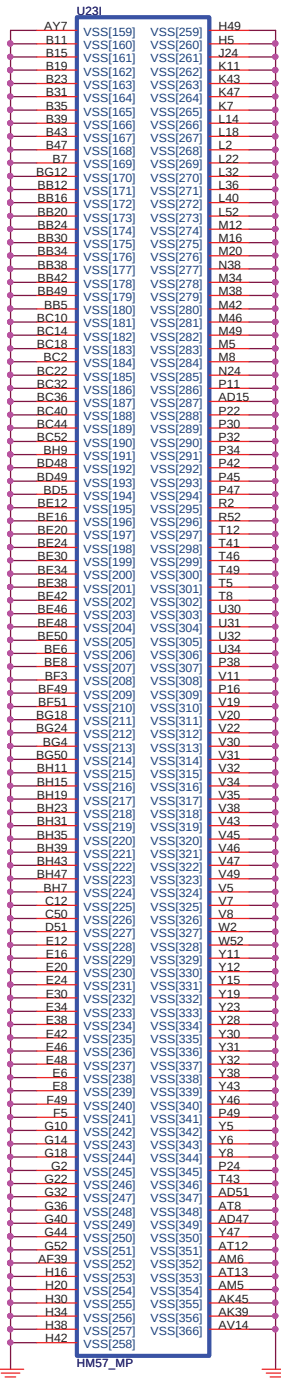
RTC 1mA



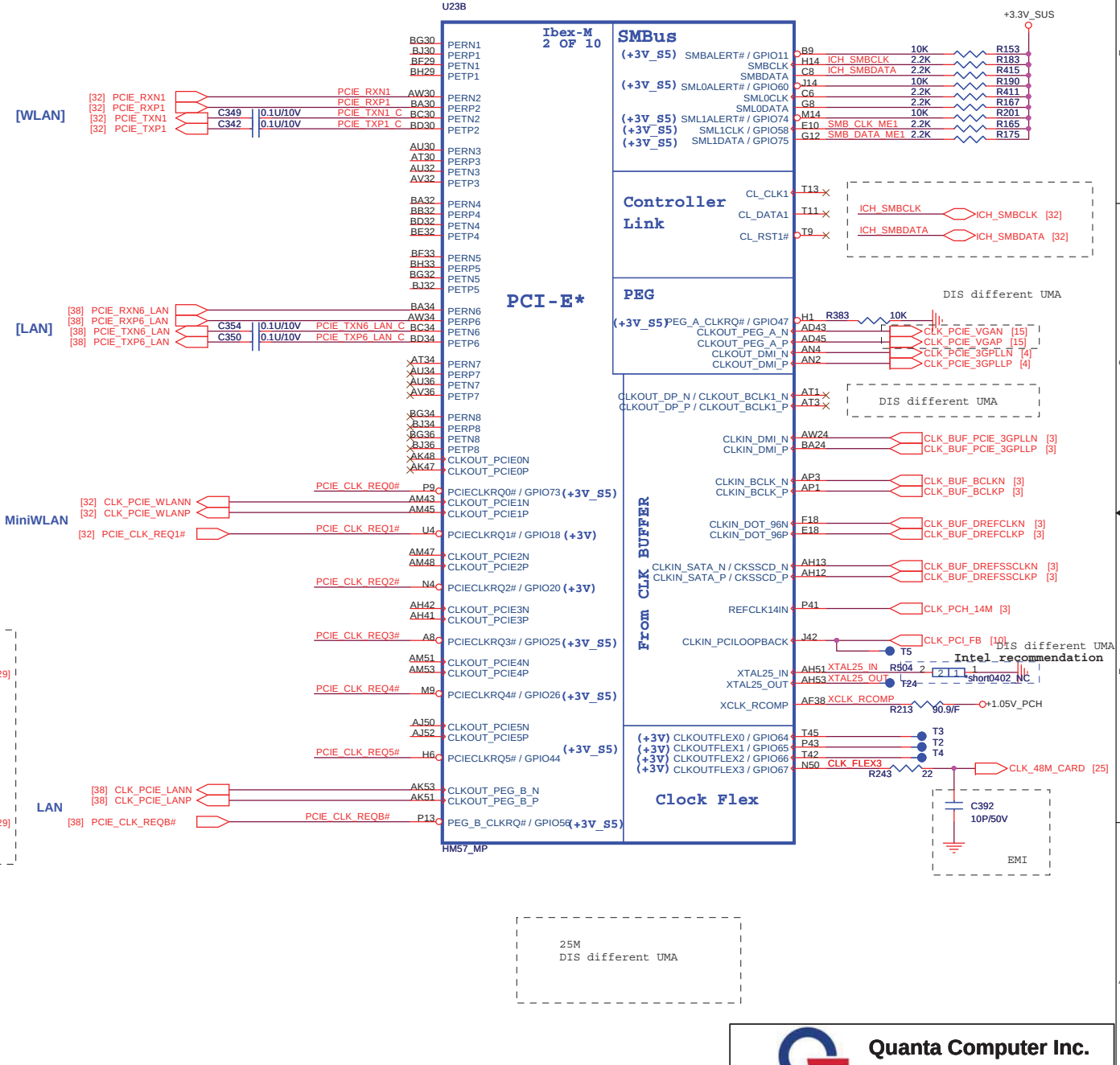
Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	3A
Date:	Wednesday, February 03, 2010	Sheet 8 of 52

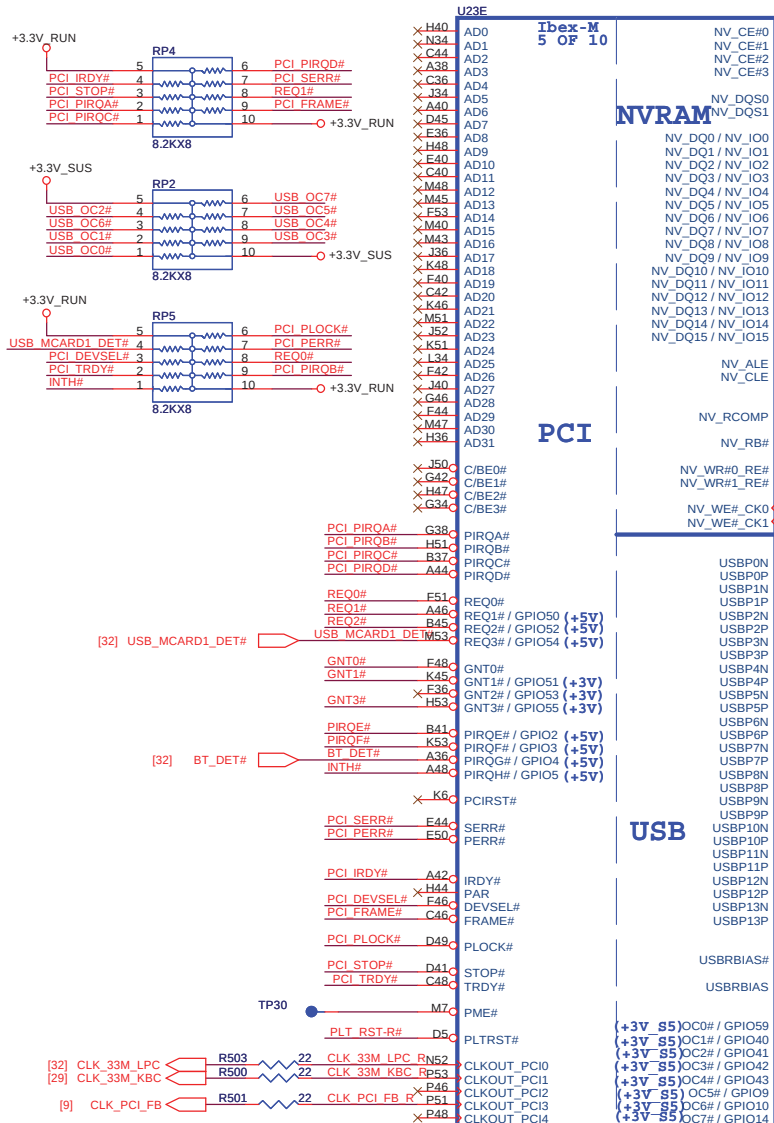
IBEX PEAK-M (GND)



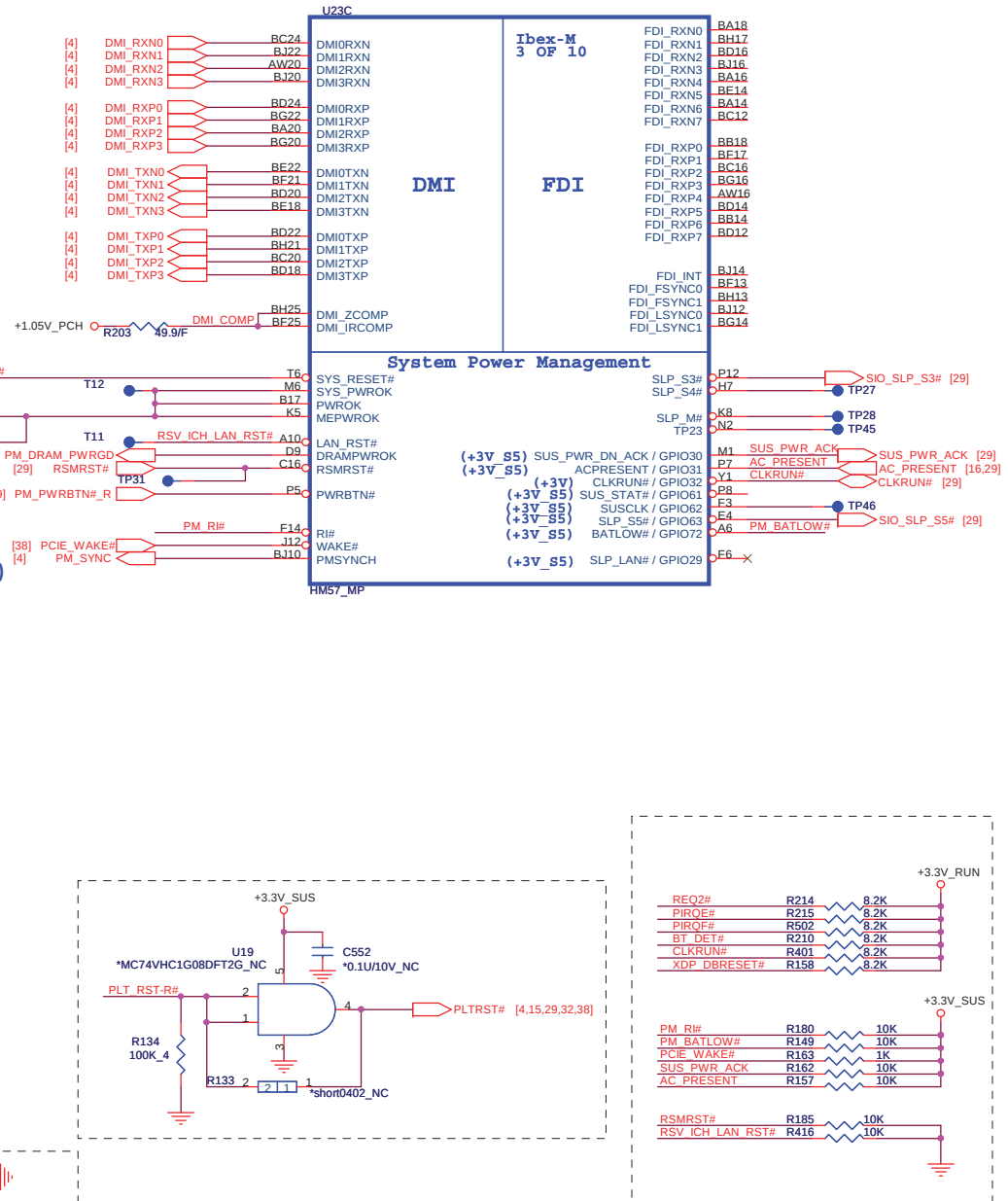
IBEX PEAK-M (PCI-E,SMBUS,CLK)



IBEX PEAK-M (PCI,USB,NVRAM)

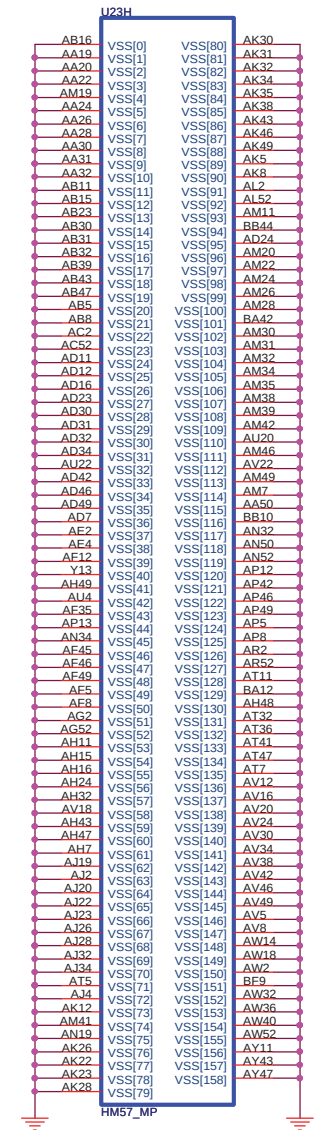
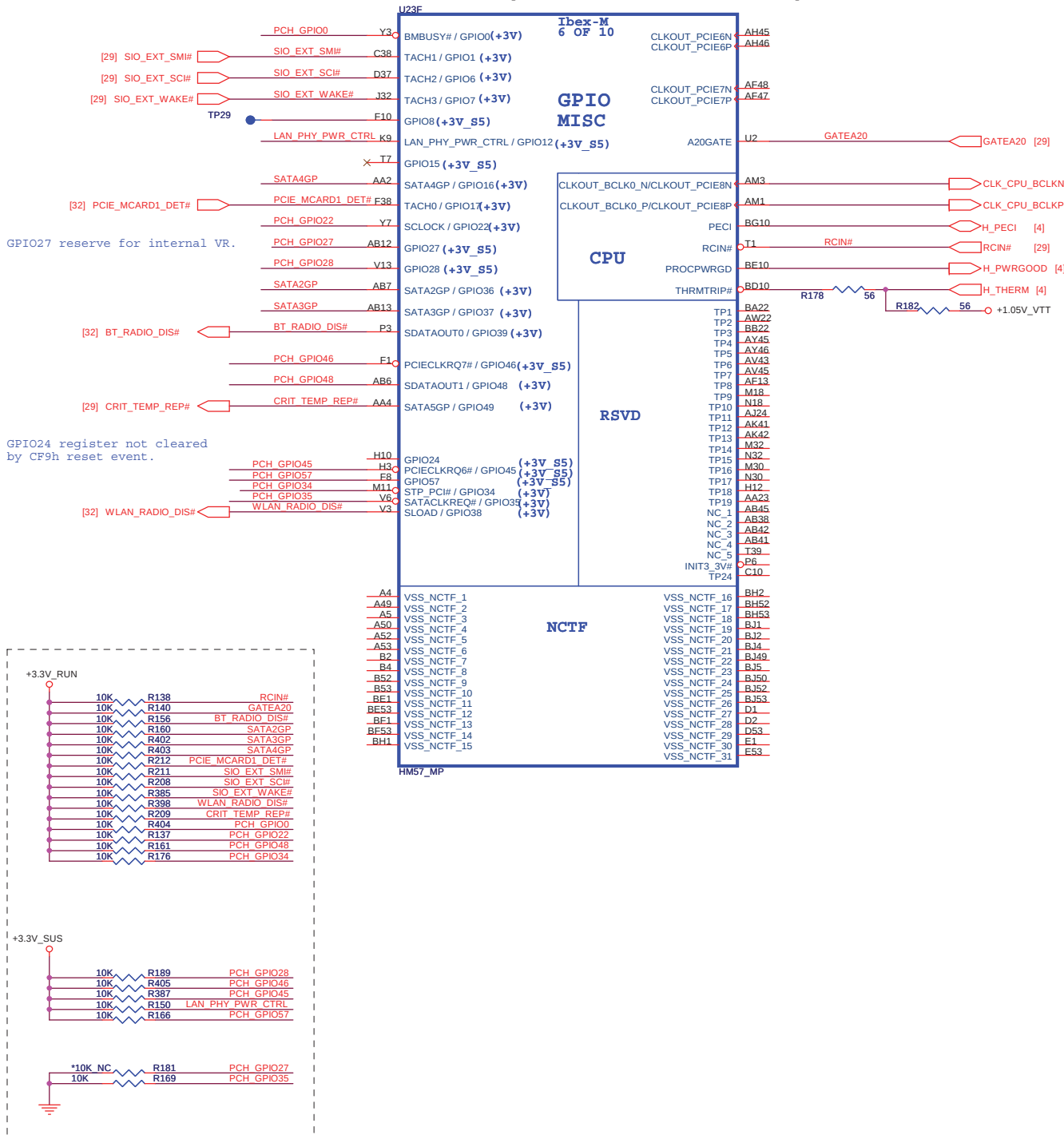


IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

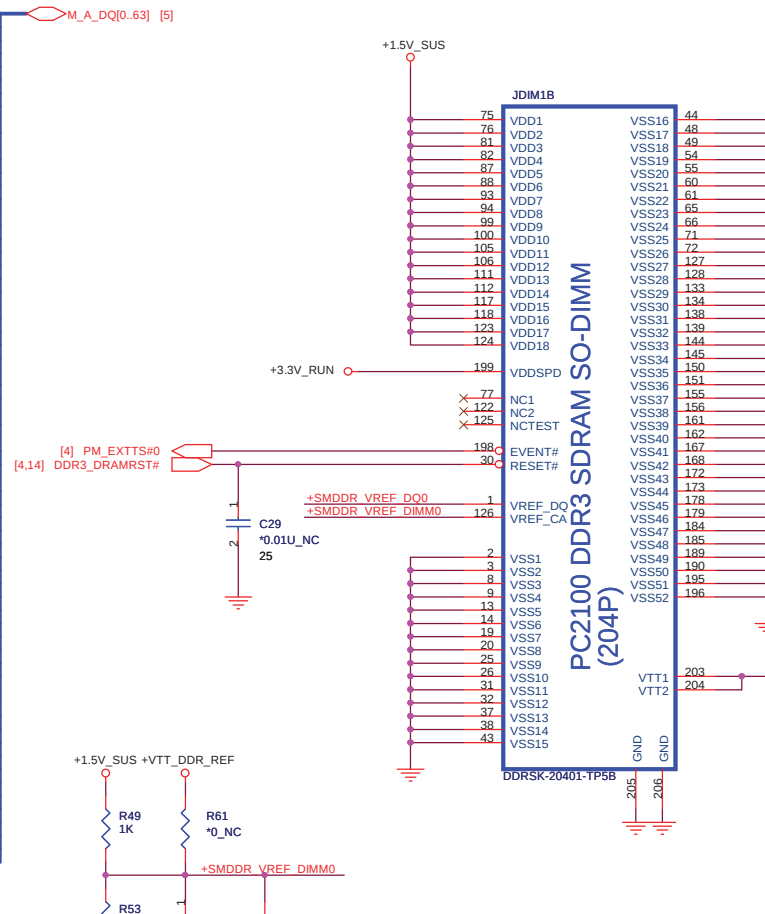
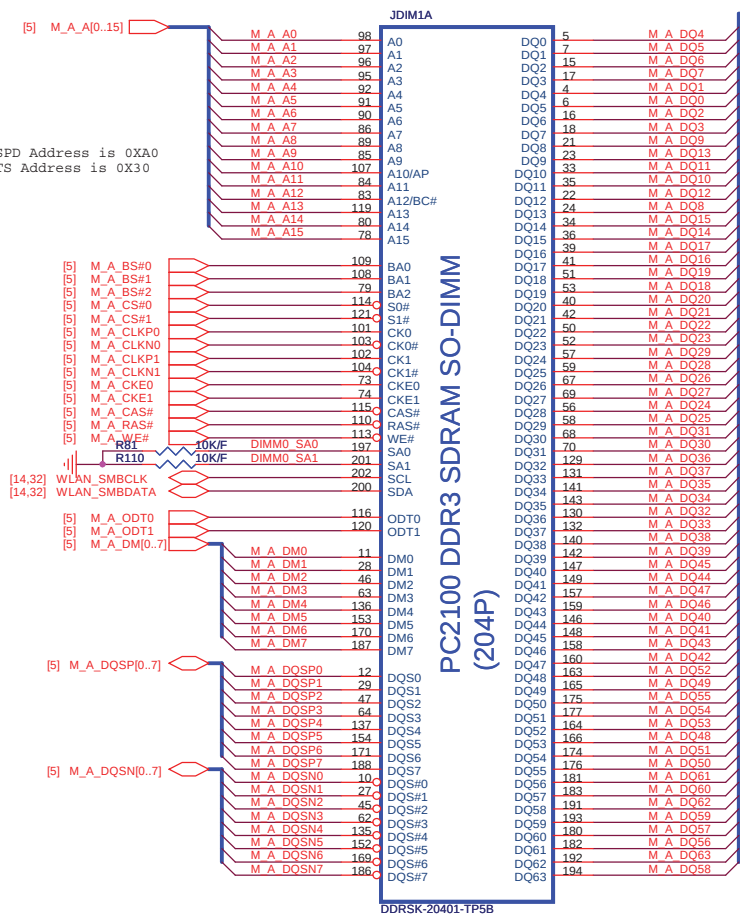
IBEX PEAK-M (GND)



L32 DIS→SHORT

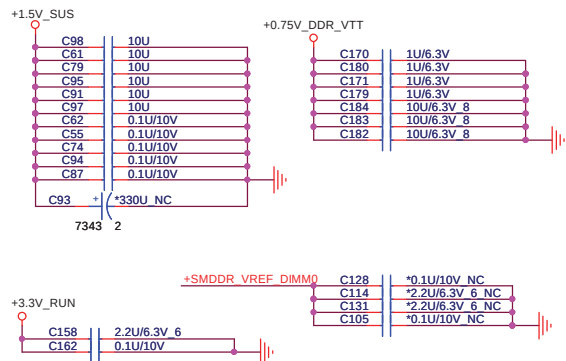


SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

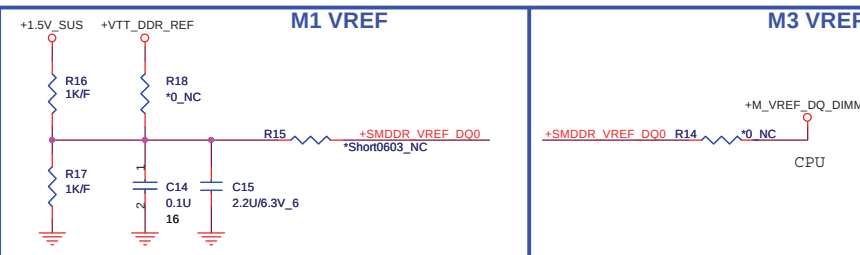
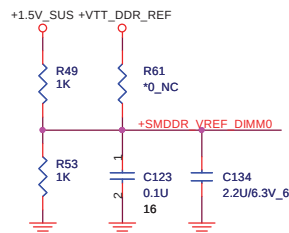


Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



H5.2

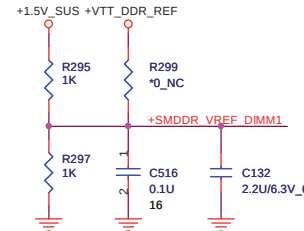
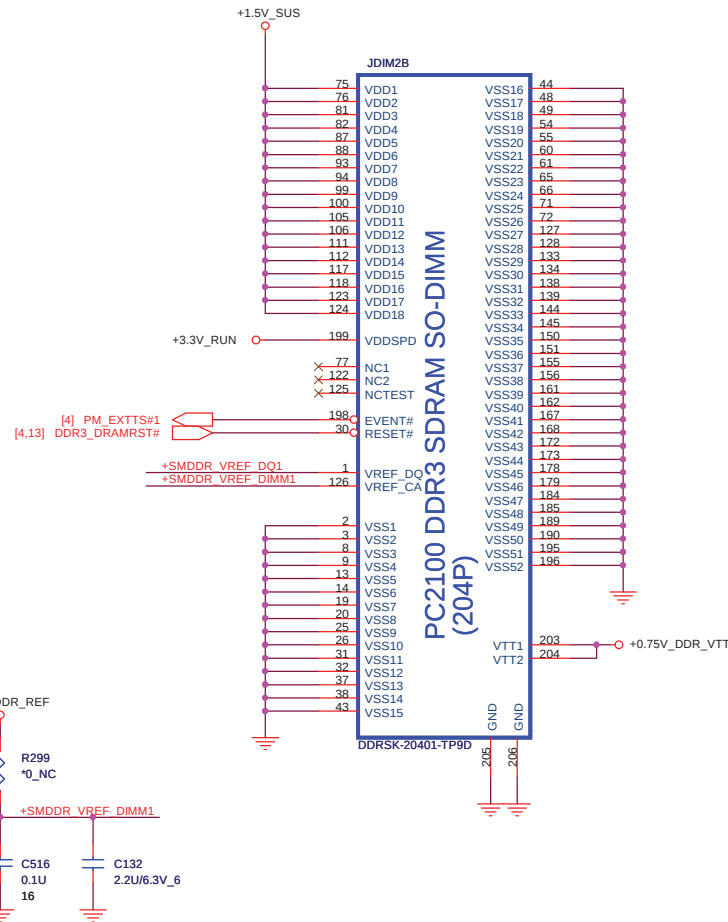
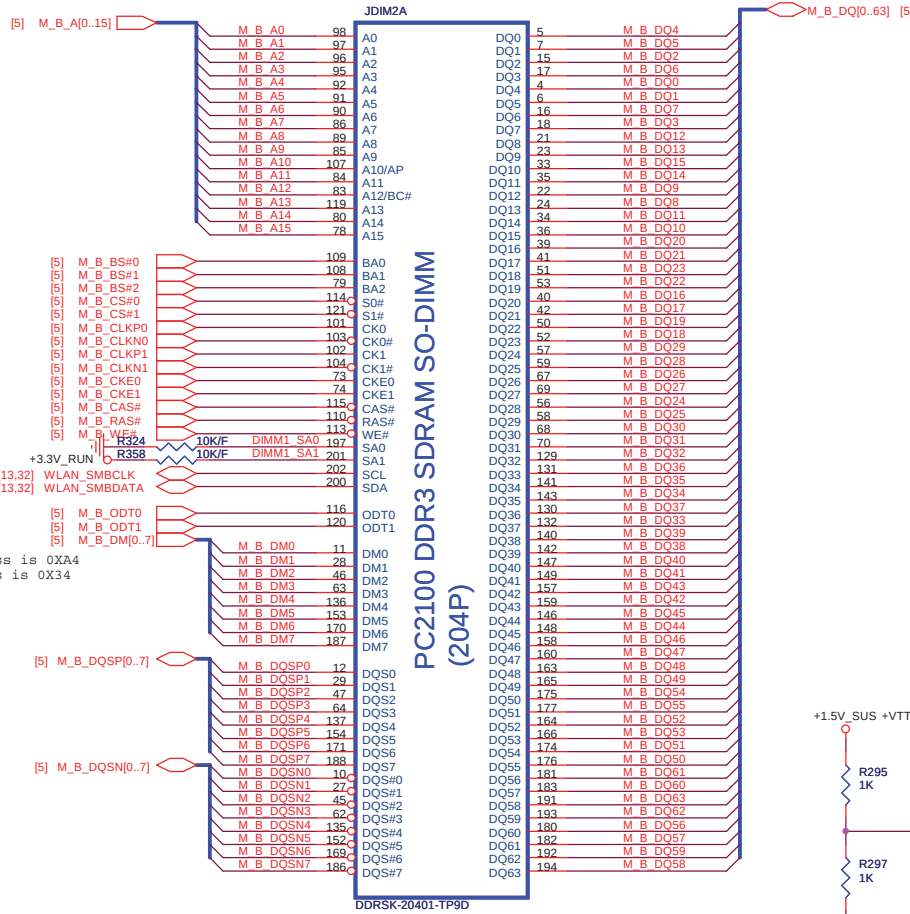


Quanta Computer Inc.

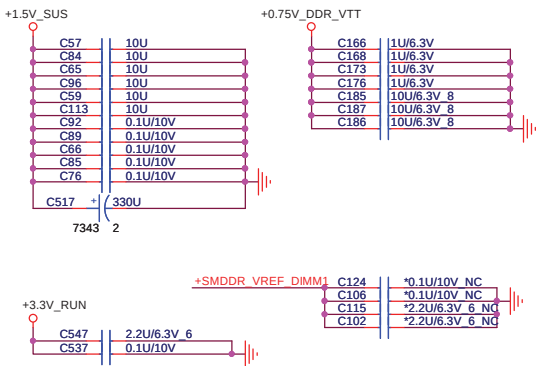
PROJECT : UM7 DIS

Size	Document Number	Rev
	DDR3 DIMM-0	3A
Date:	Wednesday, February 03, 2010	Sheet 13 of 52

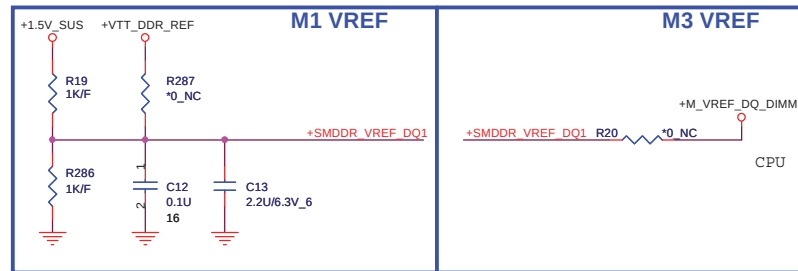
<http://laptop-motherboard-schematic.blogspot.com/>



Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

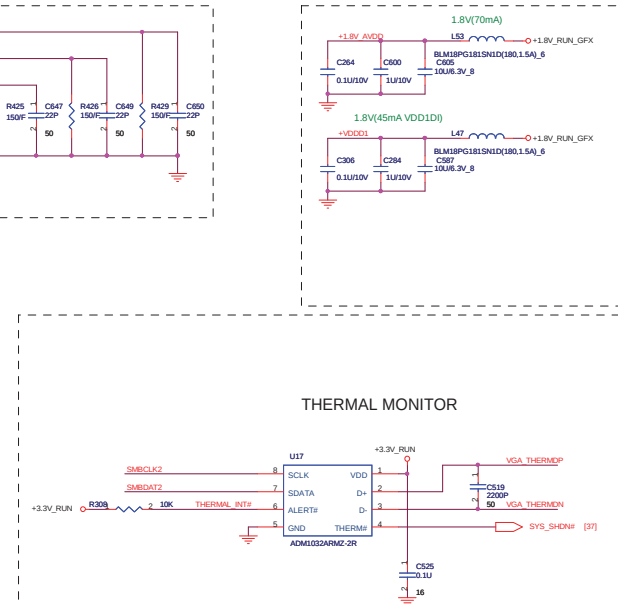


H9.2



GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

Figure 1: Pin connections of the board. The diagram shows two pin headers. The left header (pins 1-18) is connected to various components: R320, R319, R349, R374, R373, R369, R339, R356, R432, R435, R413, R329, R321, R345, R318, R341, R340, R317, and R318. The right header (pins 1-5) is connected to R523, R522, and R407. A dashed box on the right shows the connection of the HDMI_DET signal to the HDMI port (HPD1) through a 150K resistor (R523) and a 360K resistor (R522). A 3.3V RUN supply is also shown.



```
Power-Up

+3.3V_RUN -- +VCC_GFX_CORE

+PCIE_VDDC -- +1.8V_RUN_GFX

CLK_PCIE_VGAP/N -- +1.8V_RUN_GFX

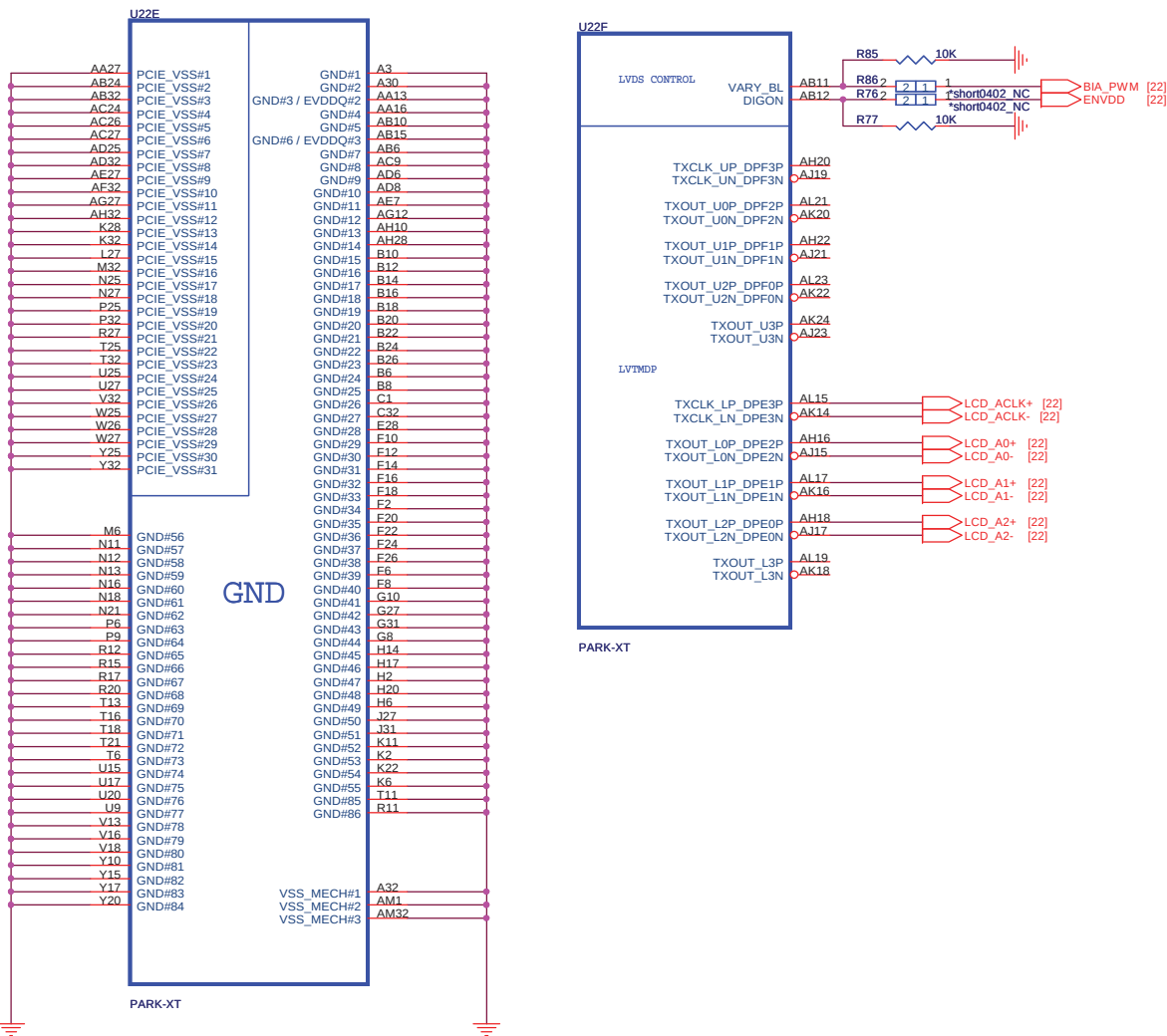
+3.3V_RUN early +VCC_GFX_CORE /+1.8V_RUN_GFX or
when +VCC_GFX_CORE /+1.8V_RUN_GFX up then +3.3V_RUN

+VCC_GFX_CORE reach 90% and +1.8V_RUN_GFX

power-down

+1.8V_RUN_GFX -- +PCIE_VDDC

PCIE ref clock(CLK_PCIE_VGAA/B) early +1.8V
```



Strap Name	Pin Straps description		Default Value
TX_PWRS_ENB	GPIO0	PCI Express Full TX Output Swing 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD [0]	VSYNC	AUD[1] AUD[0] 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1
AUD (1)	HSYNC		1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERICC		0



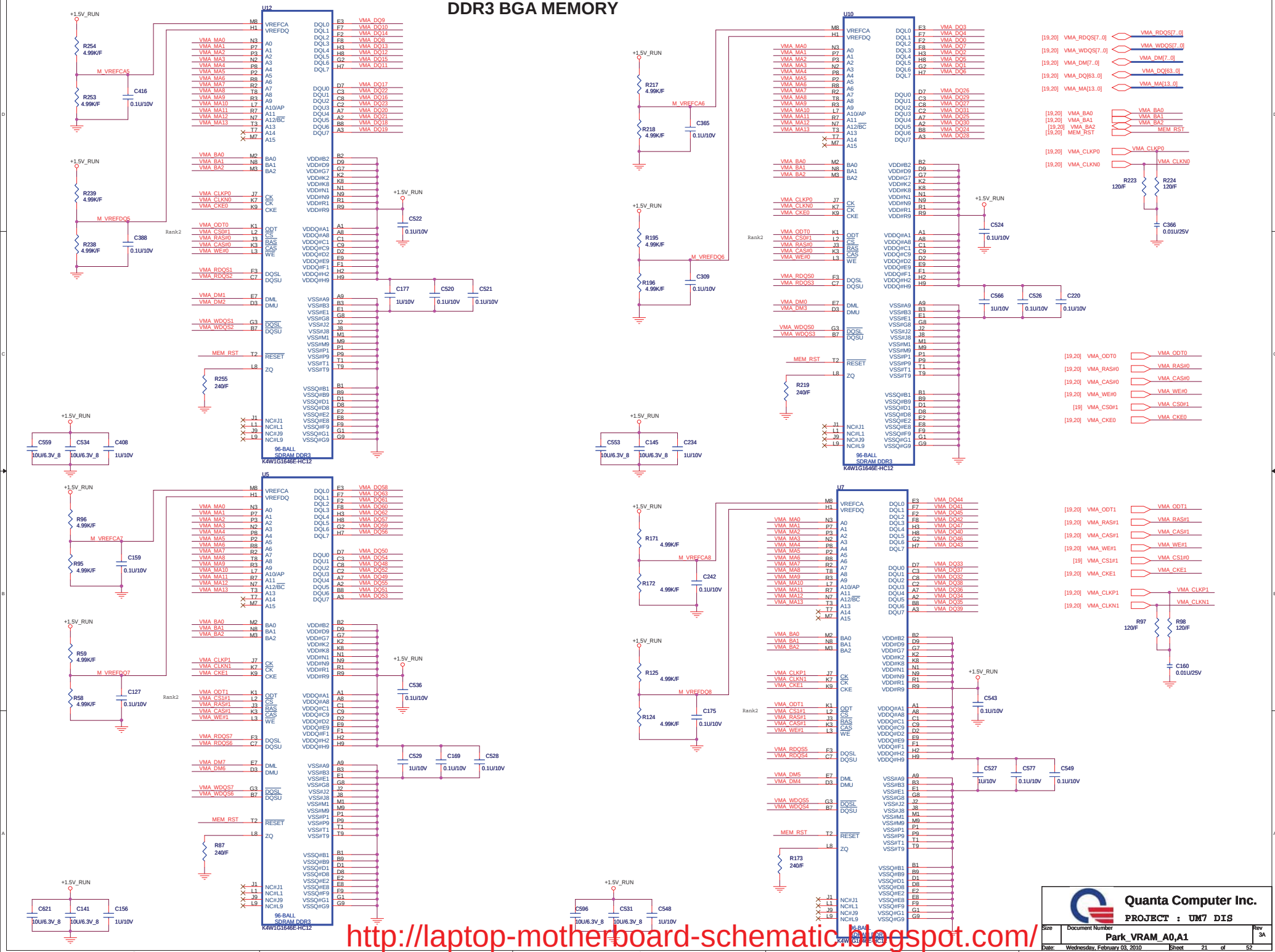
Quanta Computer Inc.
PROJECT : UM7 DIS

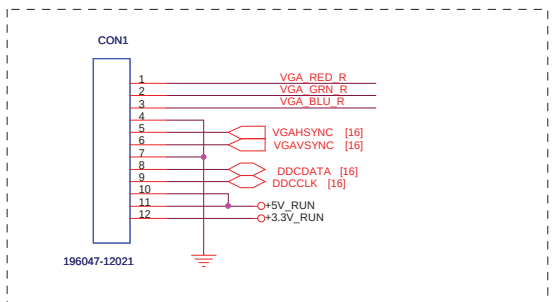
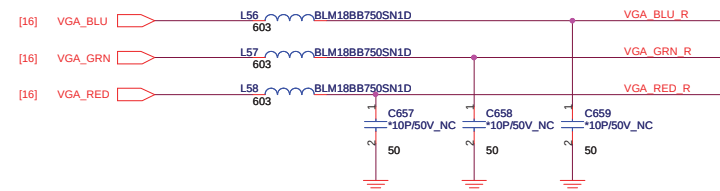
Size	Document Number	Rev
	Park_GND / LVDS/ Straps	3A
Date:	Wednesday, February 03, 2010	Sheet 17 of 52

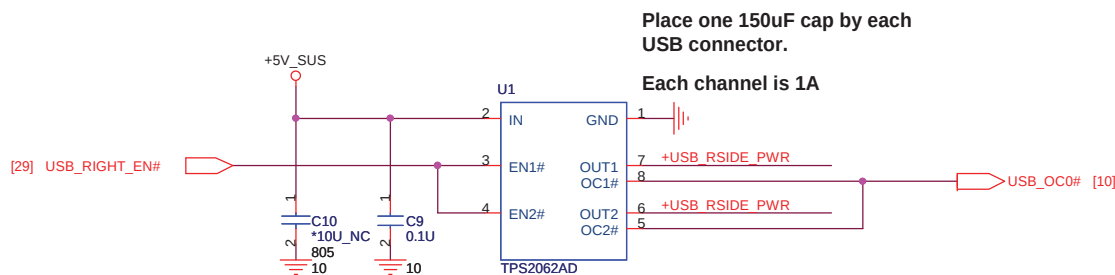
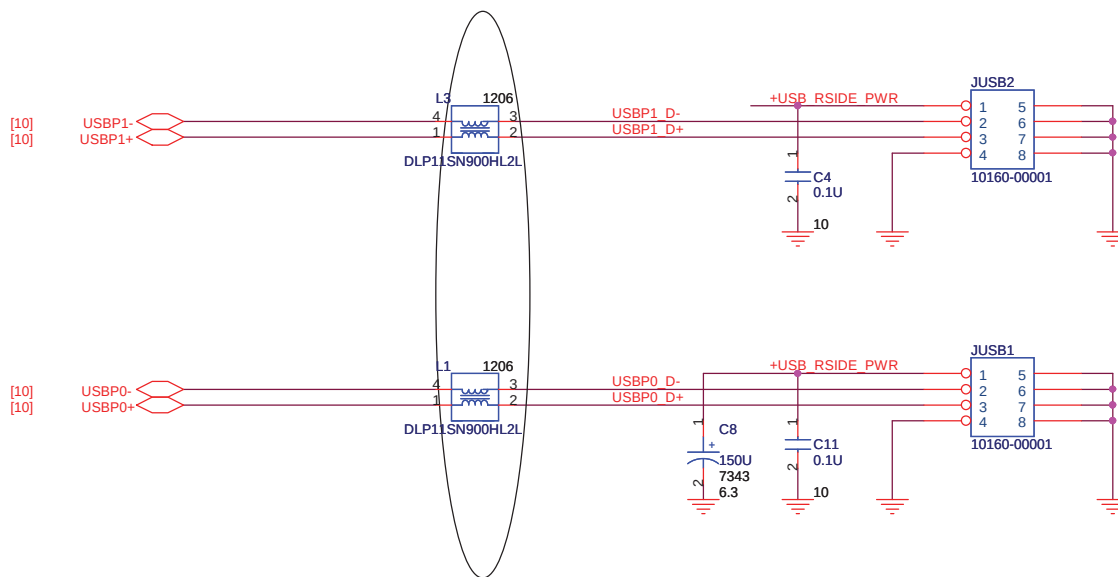

```
| Hynix
| AKD5LZGTW00
| IC DDR3 (96P) H5TQ1G63BFR-12C (FBGA)
|
| AKD5LZGTW03
| IC SDRAM (96P) H5TQ1G63BFR-12C(FBGA) WINBSQ
|
| Samsung
| AKD5LGGT502
| IC SDRAM (96P) K4W1G1646E-HC12 (FBGA)
|
| AKD5LGGT506
| IC SDRAM (96P) K4W1G1646E-HC12 (FBGA) WINBSQ
```



DDR3 BGA MEMORY





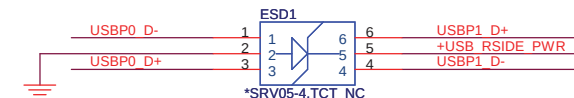


Place one 150uF cap by each USB connector.

Each channel is 1A

Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

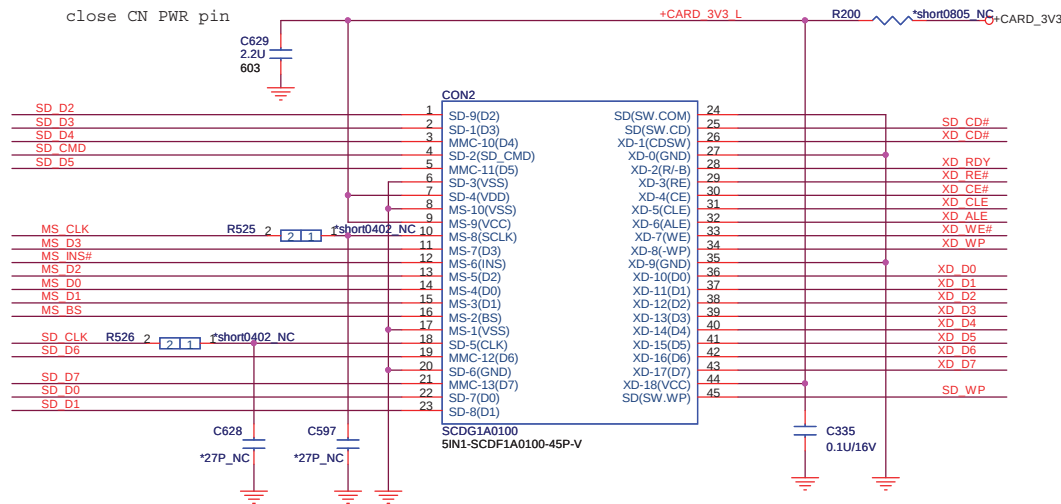
Place ESD diodes as close as USB connector.



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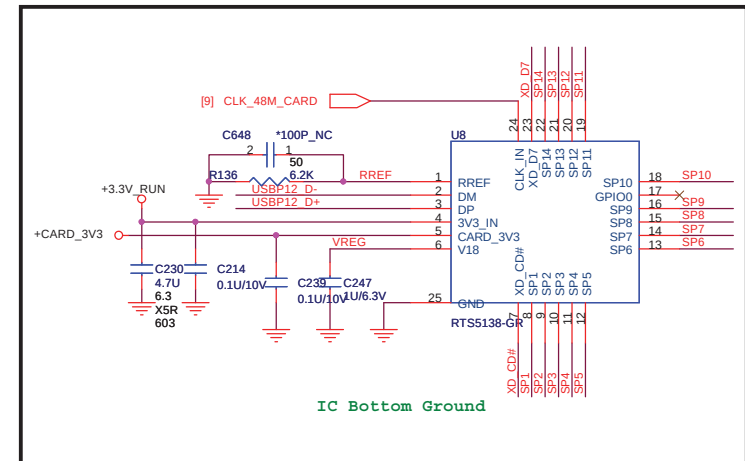
PROJECT : UM7 DIS

Size	Document Number	Rev
	Right USB	3A
Date	Wednesday, February 03, 2010	Sheet 24 of 52

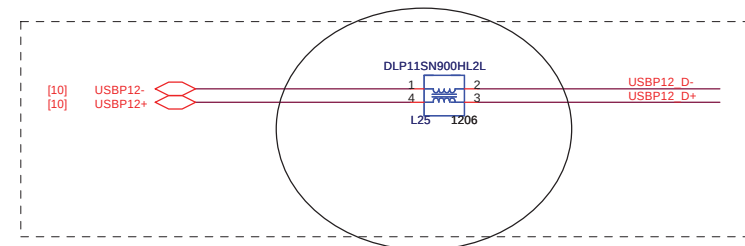


SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D7
SP4	XD CLE	SD D7	MS D3
SP5	XD ALE	SD CD#	
SP6	XD WE#	SD D6	MS D6
SP7	XD WP	SD CLK	MS D2
SP8	XD D0	SD D5	MS D0
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6	MS BS	

Share Pin

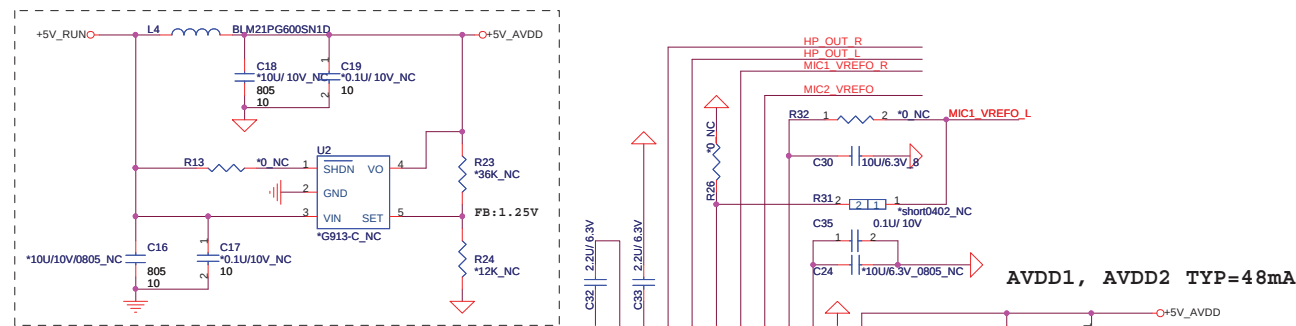


RTS5138-QFN24

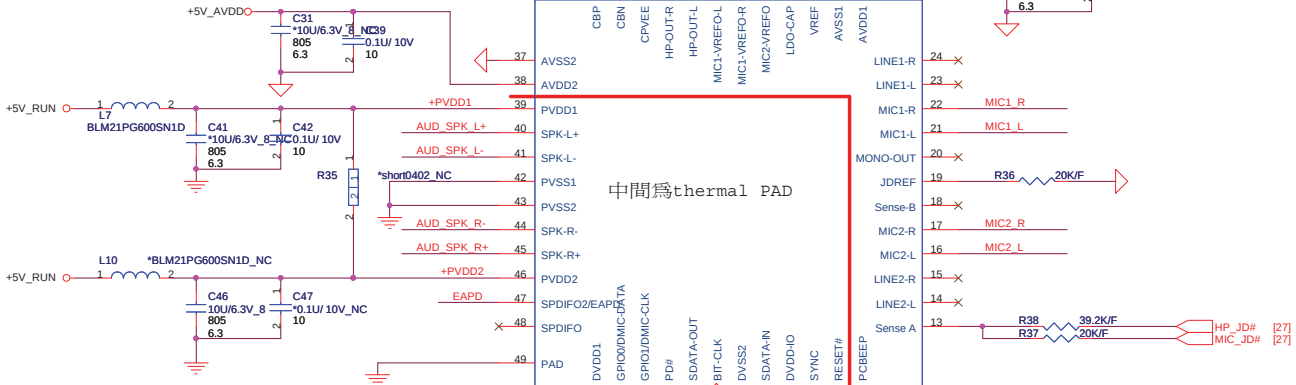


Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Card Reader(RTS5138)	3A
Date	Wednesday, February 03, 2010	Sheet 25 of 52



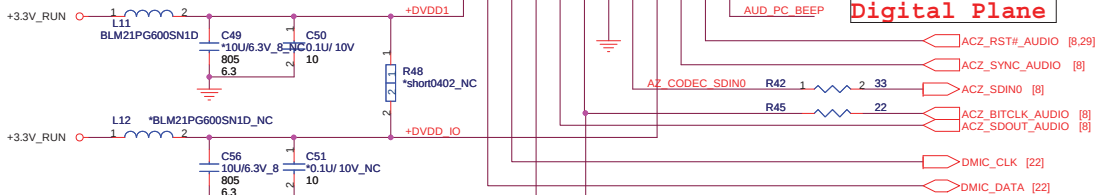
AVDD1, AVDD2 TYP=48mA



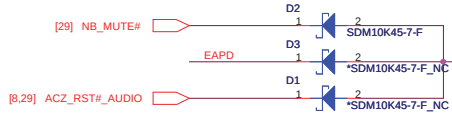
中間為thermal PAD

Analog Plane

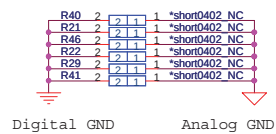
Digital Plane



DVDD & DVDD-IO TYP=50mA

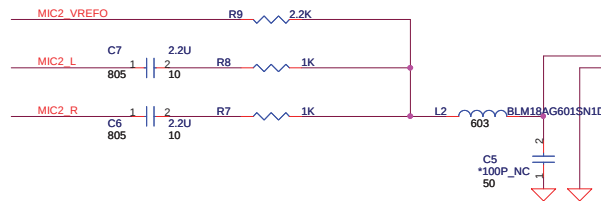


Reserve RC for EMI



Digital GND

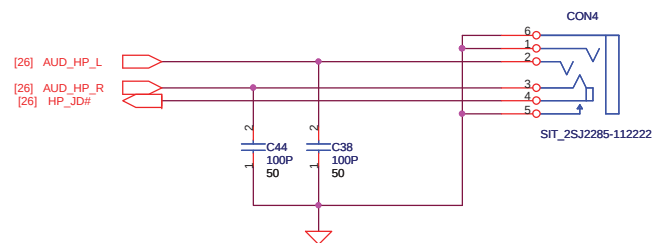
Analog GND



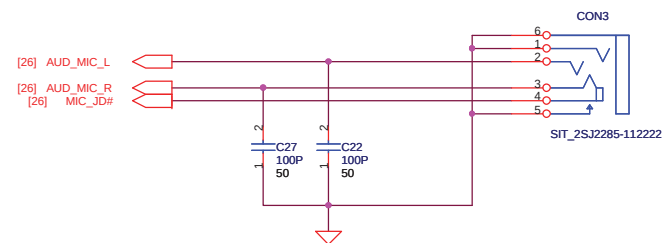
Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Azelia CODEC(ALC269)	Rev 3A
Date	Wednesday, February 03, 2010	Sheet 26 of 52	

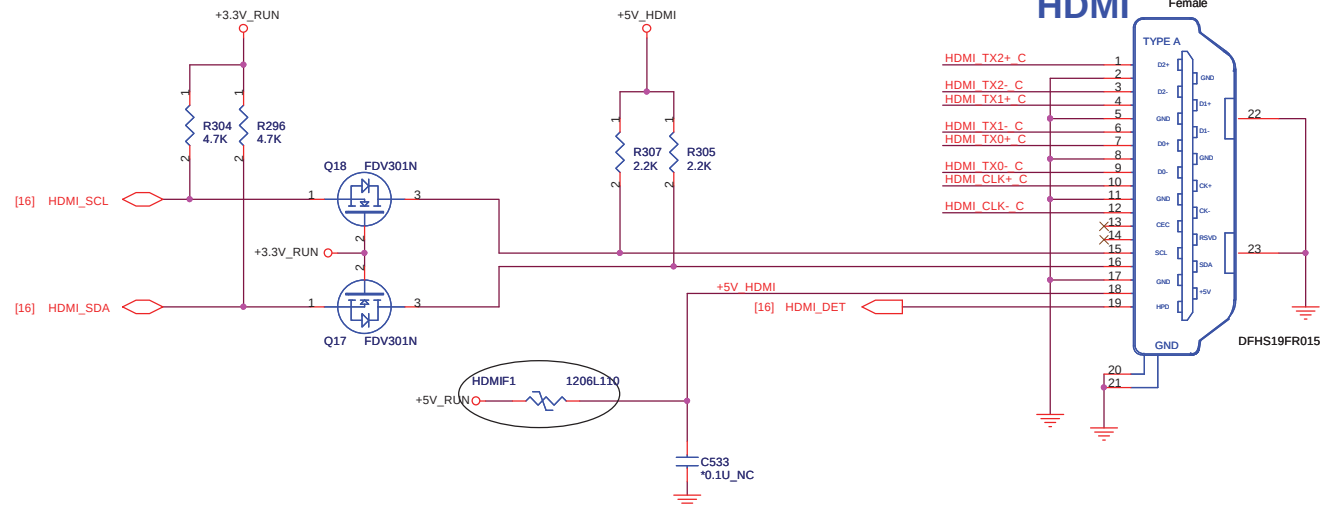
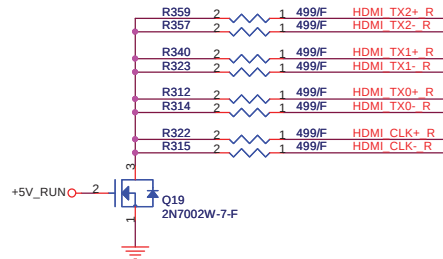
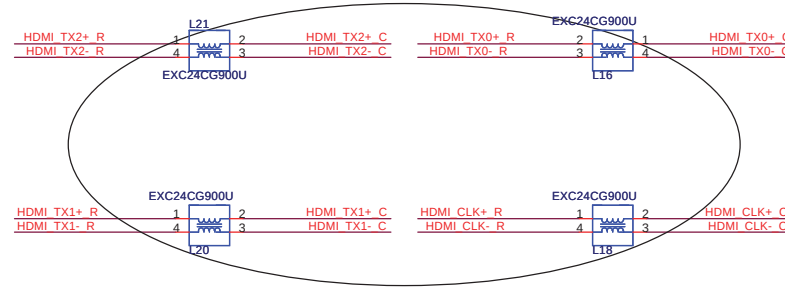
SUYIN NORMAL OPEN



SUYIN NORMAL OPEN



[16] HDMI_TX2+	C172	0.1U	HDMI TX2+ R
[16] HDMI_TX2-	C167	0.1U	HDMI TX2- R
[16] HDMI_TX1+	C164	0.1U	HDMI TX1+ R
[16] HDMI_TX1-	C157	0.1U	HDMI TX1- R
[16] HDMI_TX0+	C142	0.1U	HDMI TX0+ R
[16] HDMI_TX0-	C144	0.1U	HDMI TX0- R
[16] HDMI_CLK+	C155	0.1U	HDMI CLK+ R
[16] HDMI_CLK-	C150	0.1U	HDMI CLK- R

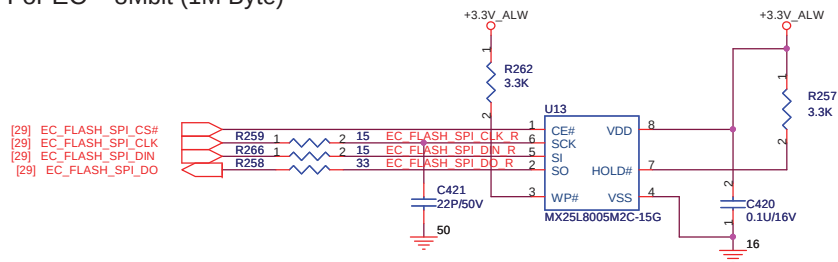


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PROJECT : UM7 DIS

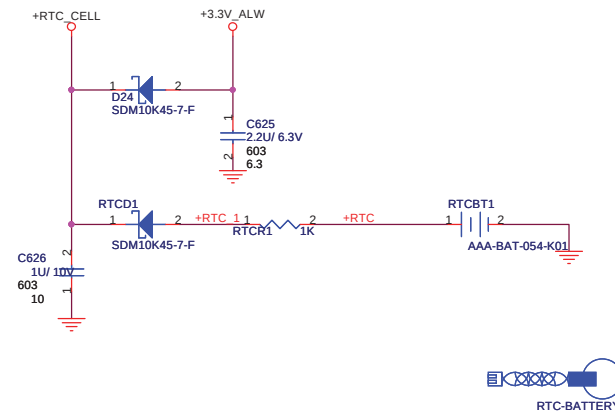
Size	Document Number	Rev
	Blank	3A
Date:	Wednesday, February 03, 2010	Sheet 28 of 52



For EC 8Mbit (1M Byte)



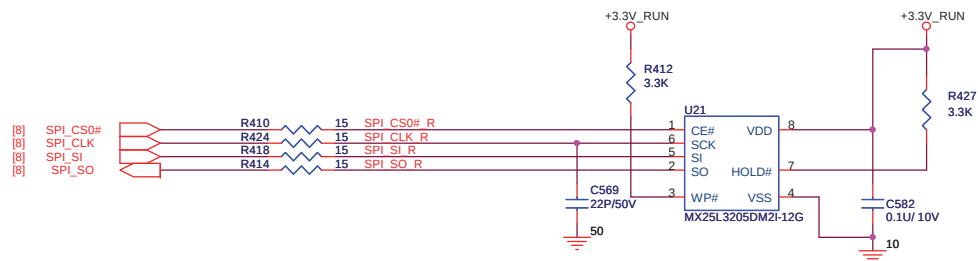
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



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PROJECT : UM7 DIS

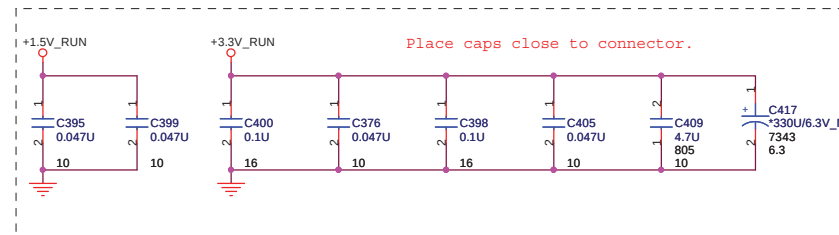
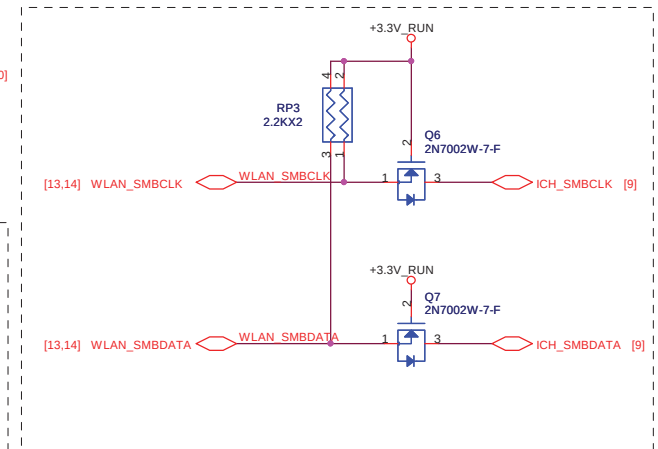
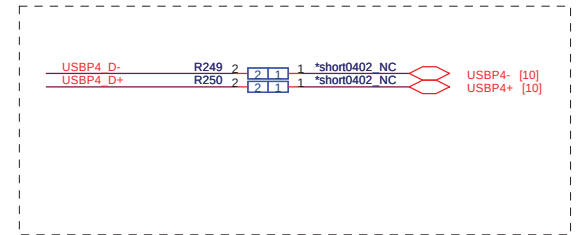
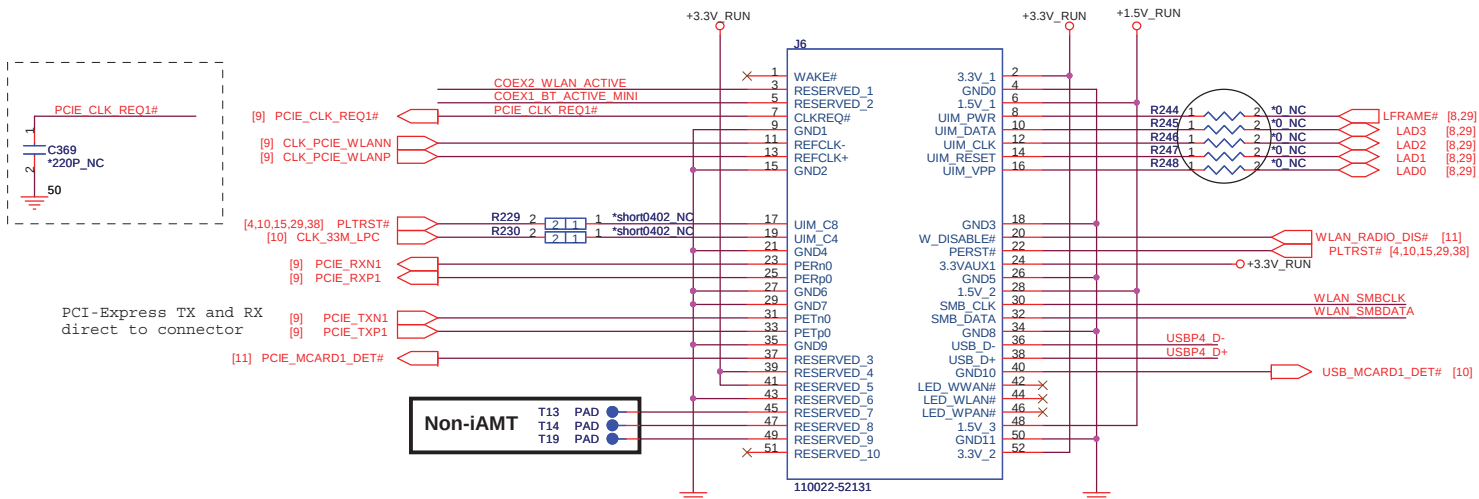
Size	Document Number	Rev
	FLASH/RTC	3A
Date:	Wednesday, February 03, 2010	Sheet 30 of 52



<http://laptop-motherboard-schematic.blogspot.com/>

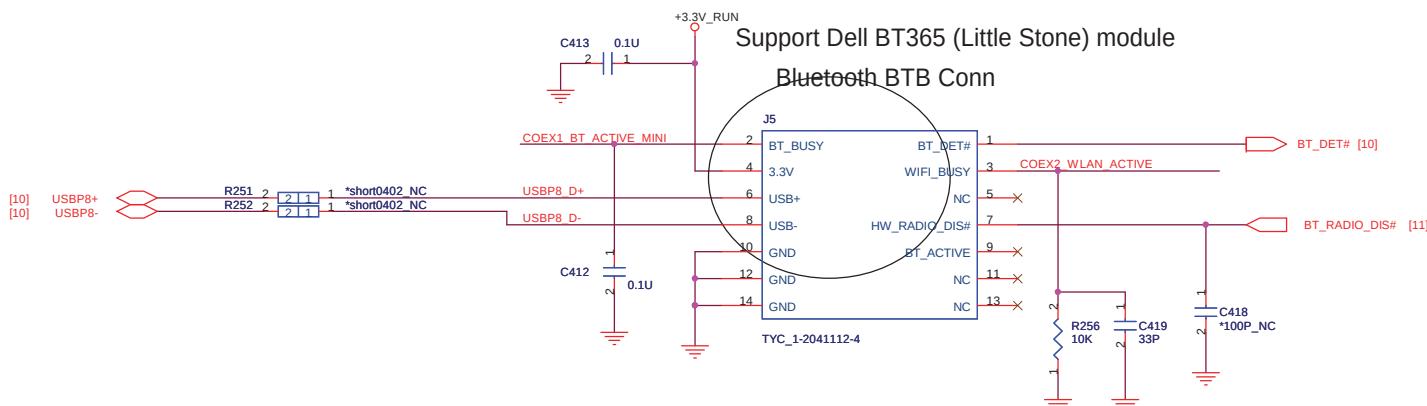
		Quanta Computer Inc.	
		PROJECT : UM7 DIS	
Size	Document Number		Rev
	MINI-Card WWAN		3A
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MiniCard WLAN connector



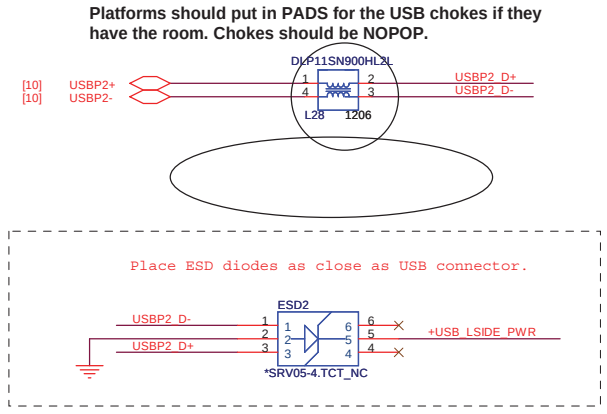
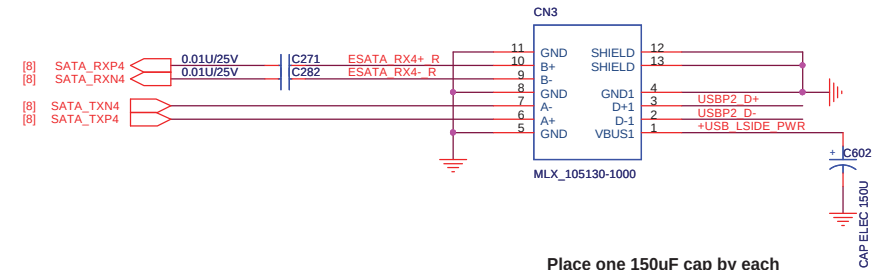
Support Dell BT365 (Little Stone) module

Bluetooth BTB Conn

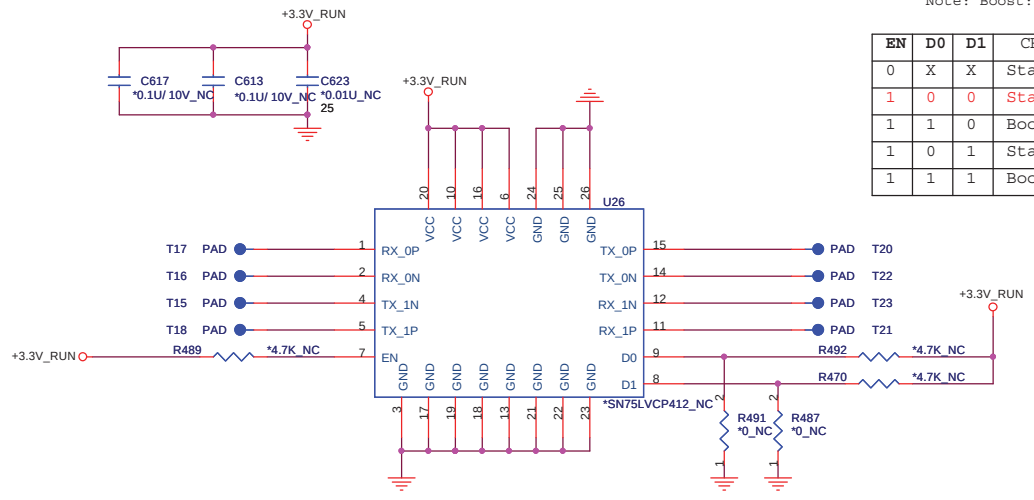


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PROJECT : UM7 DIS

USB and eSATA Conn.

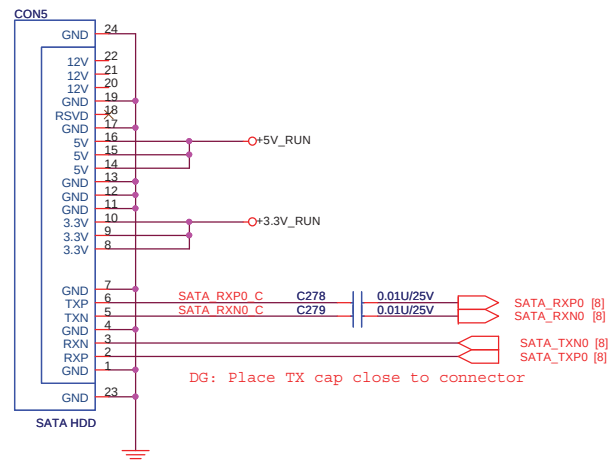


E-SATA Re-driver

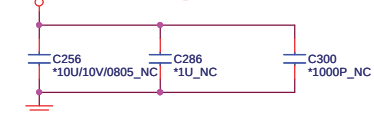


EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

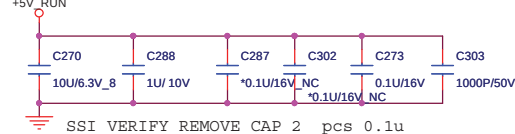
SATA Connector.



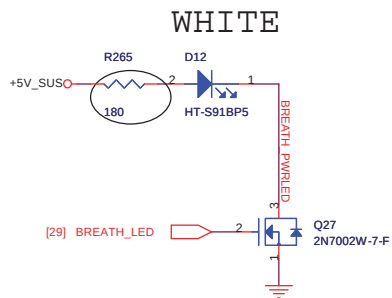
+3.3V_RUN Place caps close to connector.



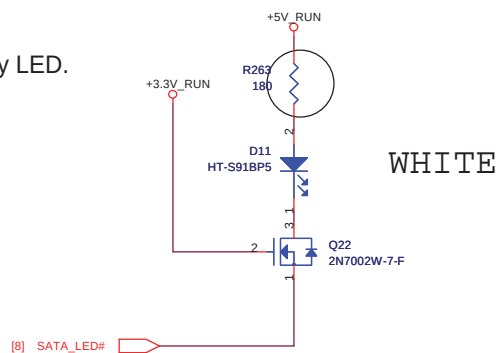
+5V_RUN Place caps close to connector.



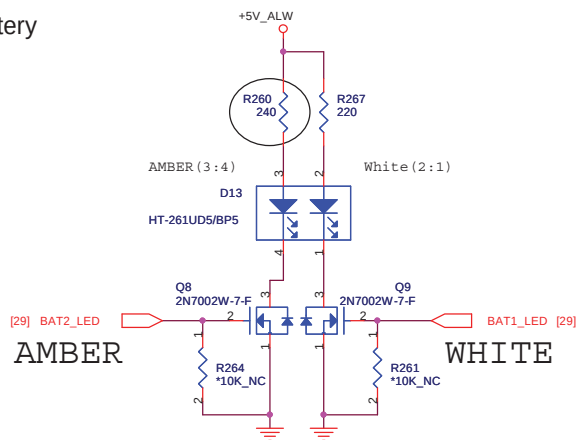
Power



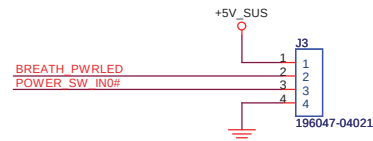
HDD activity LED.



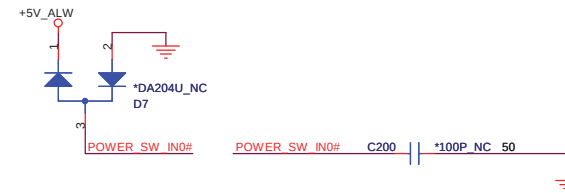
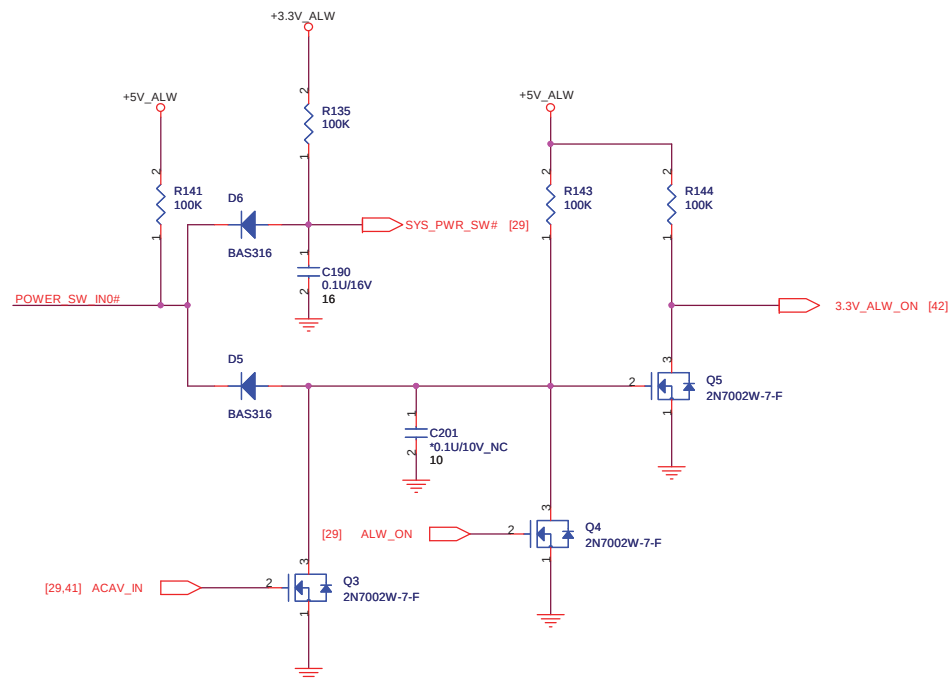
Battery



Power button Cable



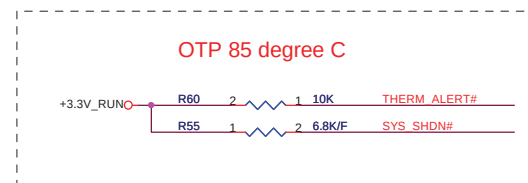
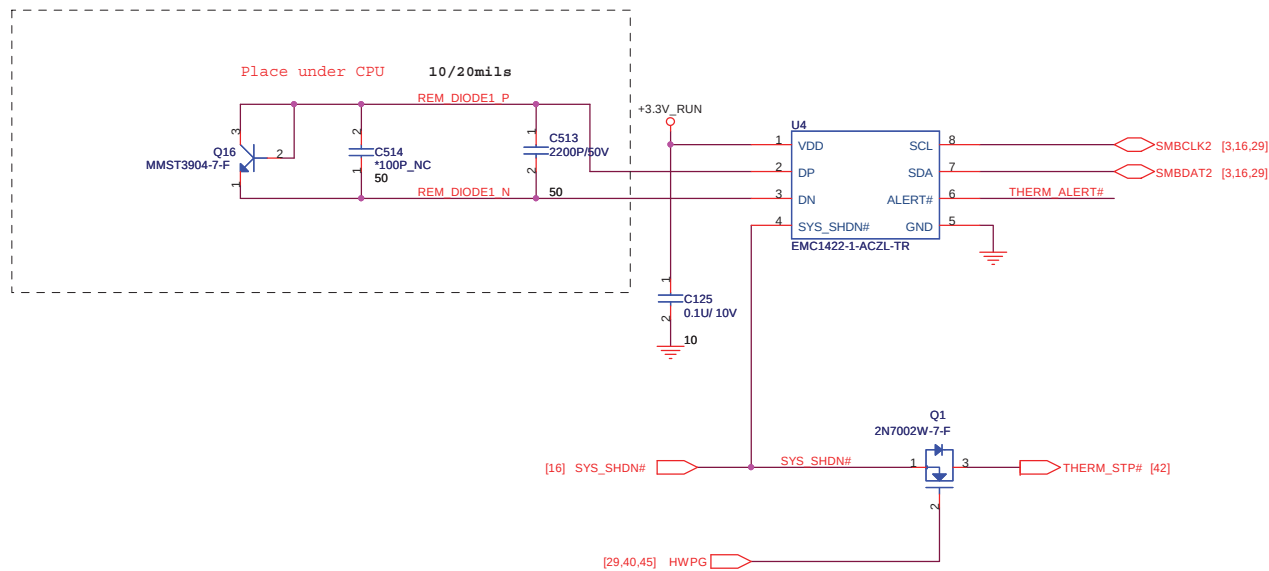
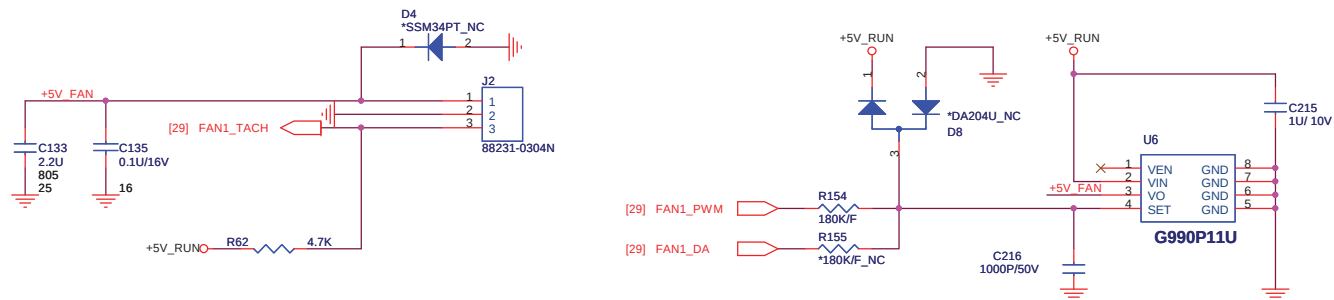
3VALW ON POWER LOGIC



Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	SWITCH, LED	3A
Date:	Wednesday, February 03, 2010	Sheet 36 of 52

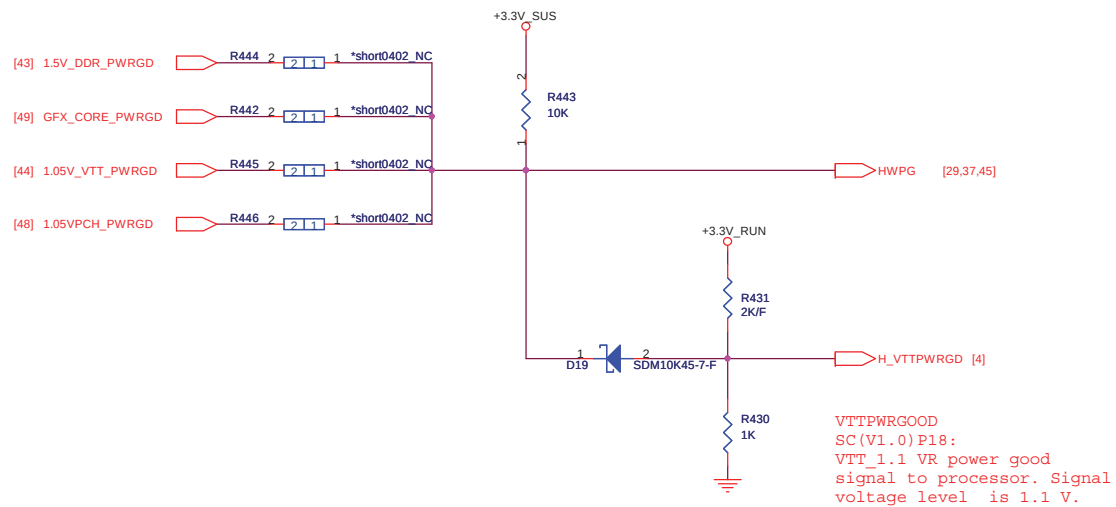
FAN CONTROL



Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	FAN & THERMAL	3A
Date:	Wednesday, February 03, 2010	Sheet 37 of 52

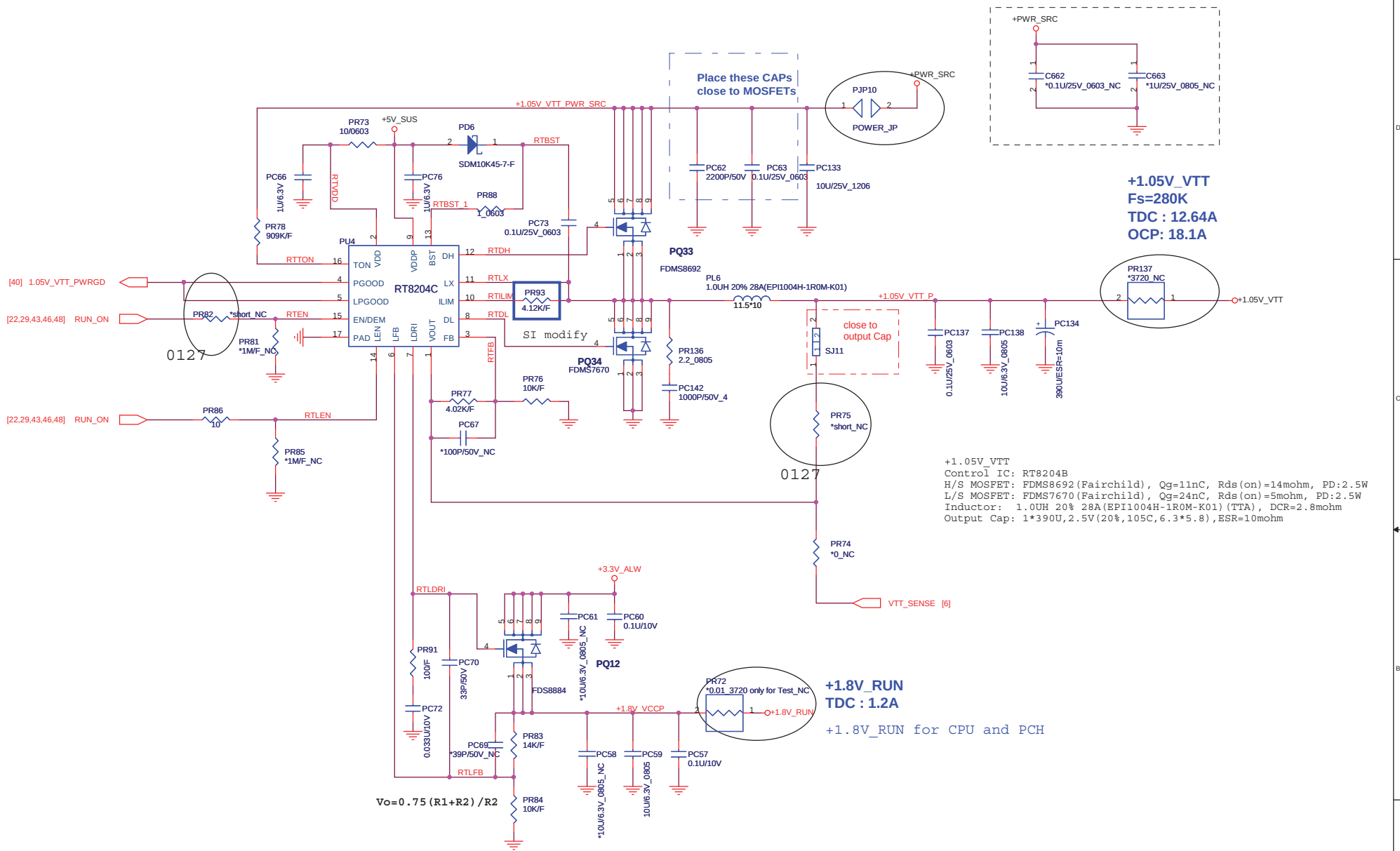


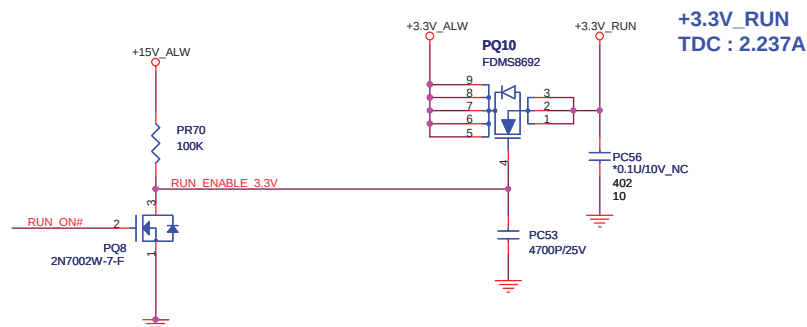
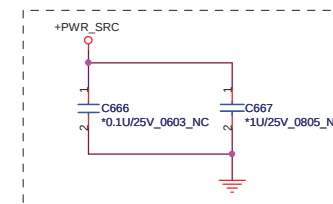
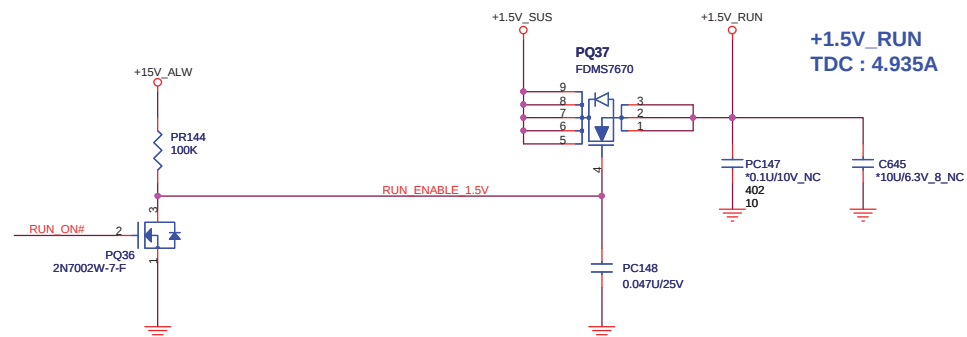
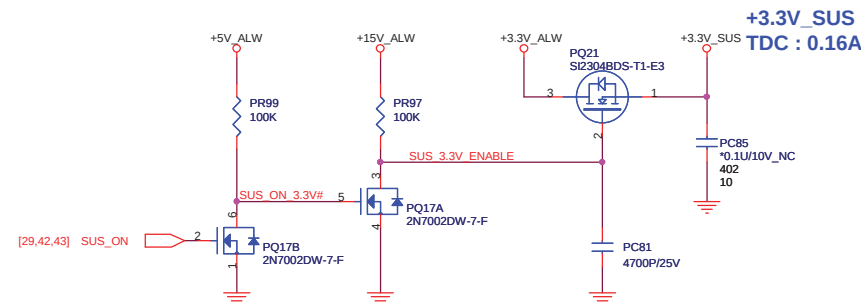
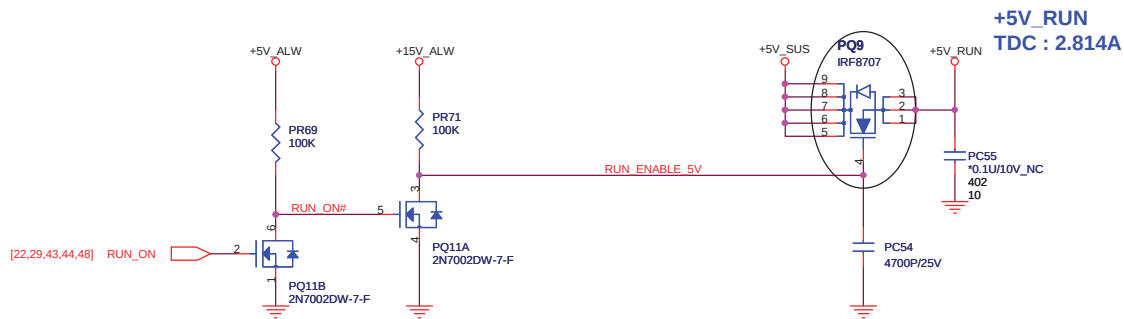


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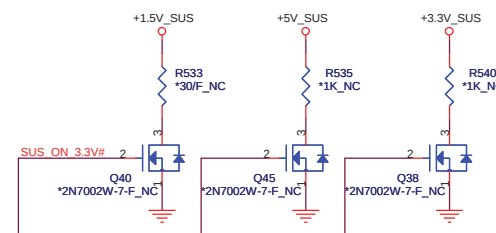
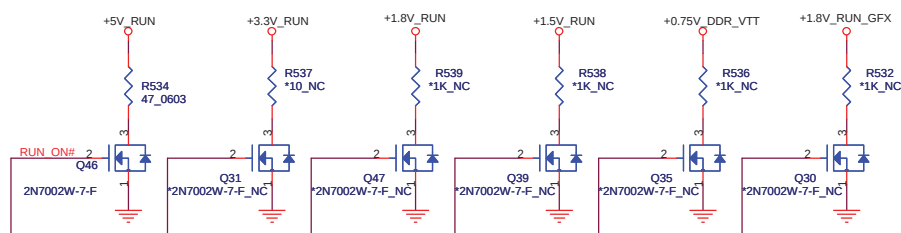
PROJECT : UM7 DIS

Size	Document Number	Rev
		3A
Date: Wednesday, February 03, 2010	Sheet 40 of 52	

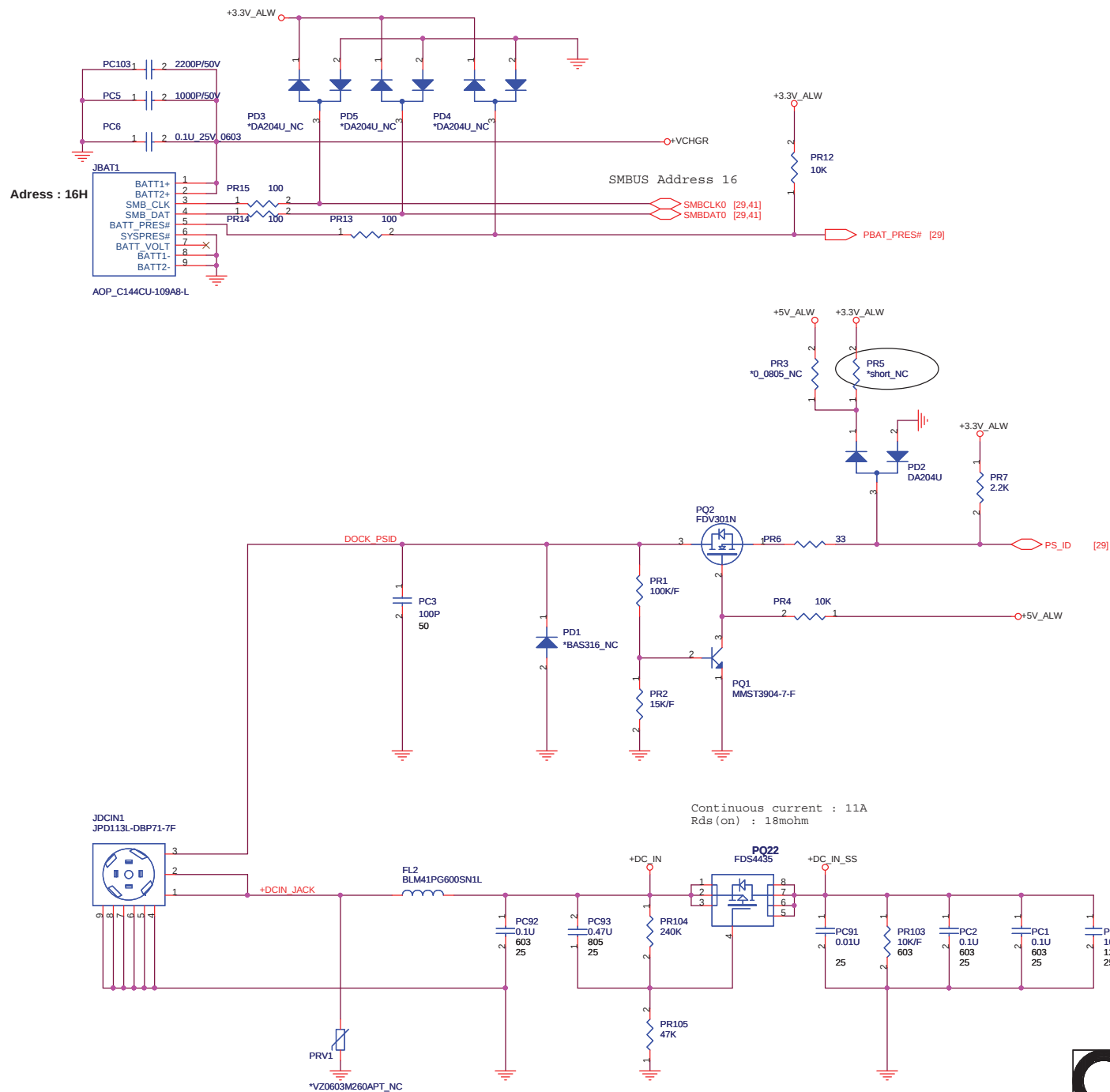




Reserve discharge path



Title		
RUN / SUS POWER SW		
Size	Document Number	Rev
UM7 Dis		3A
Date	Wednesday, February 03, 2010	Sheet
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QUANTA
COMPUTER

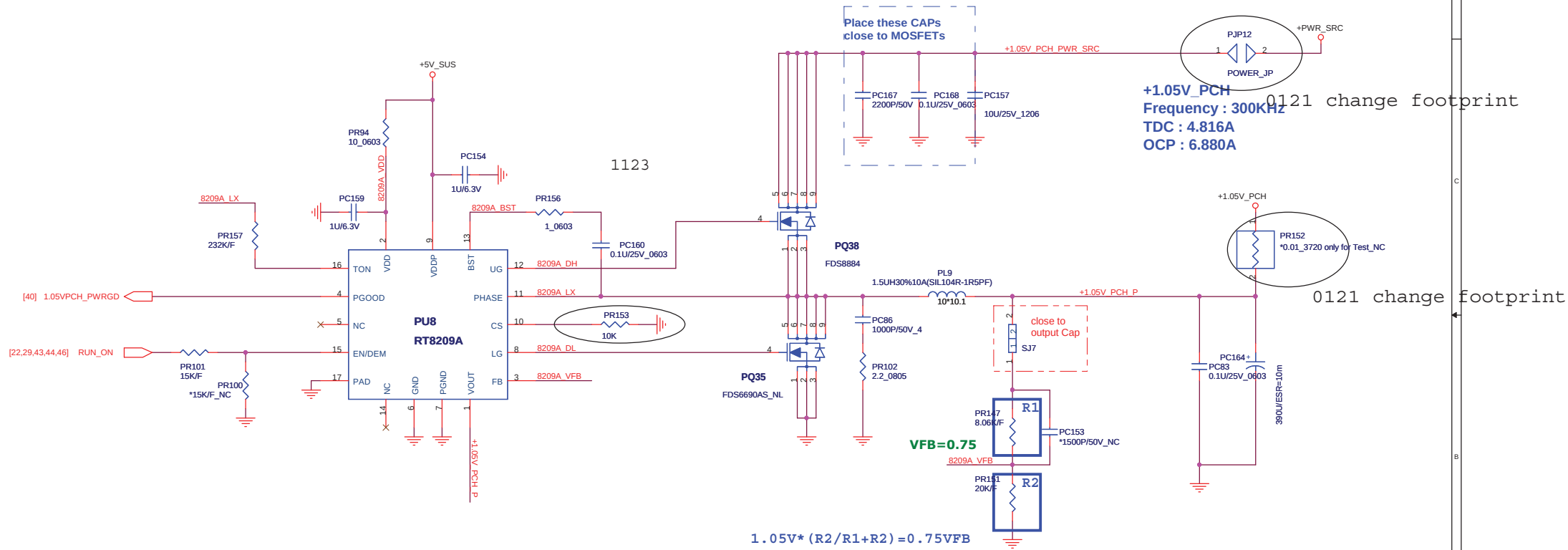
Title DCIN, BATT CONNECTOR

Size Document Number UM7 Dis

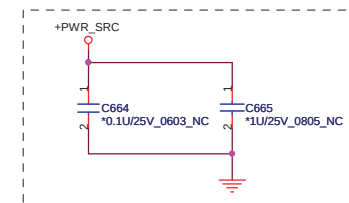
Rev 3A

Date: Wednesday, February 13, 2010

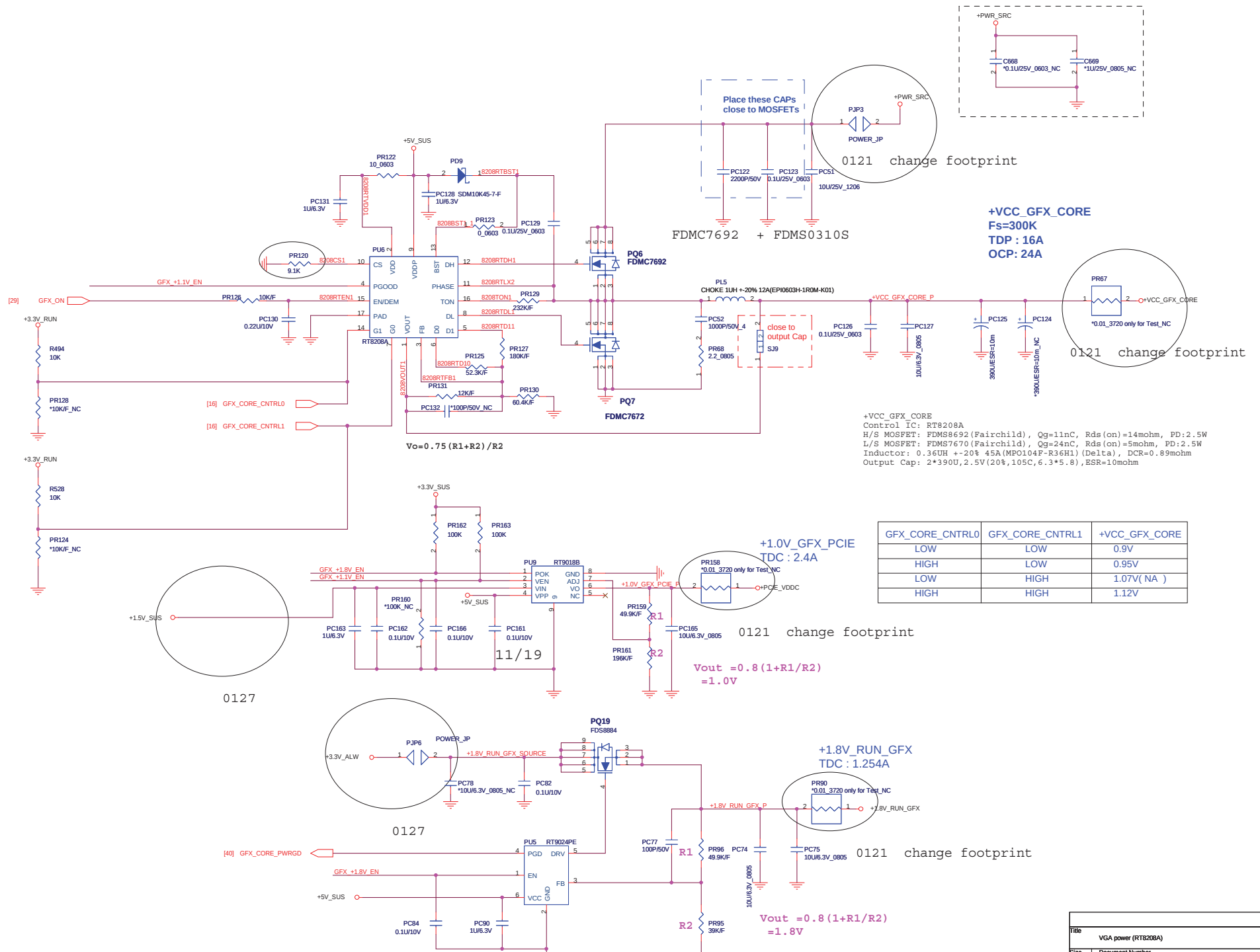
Sheet 47 of 52

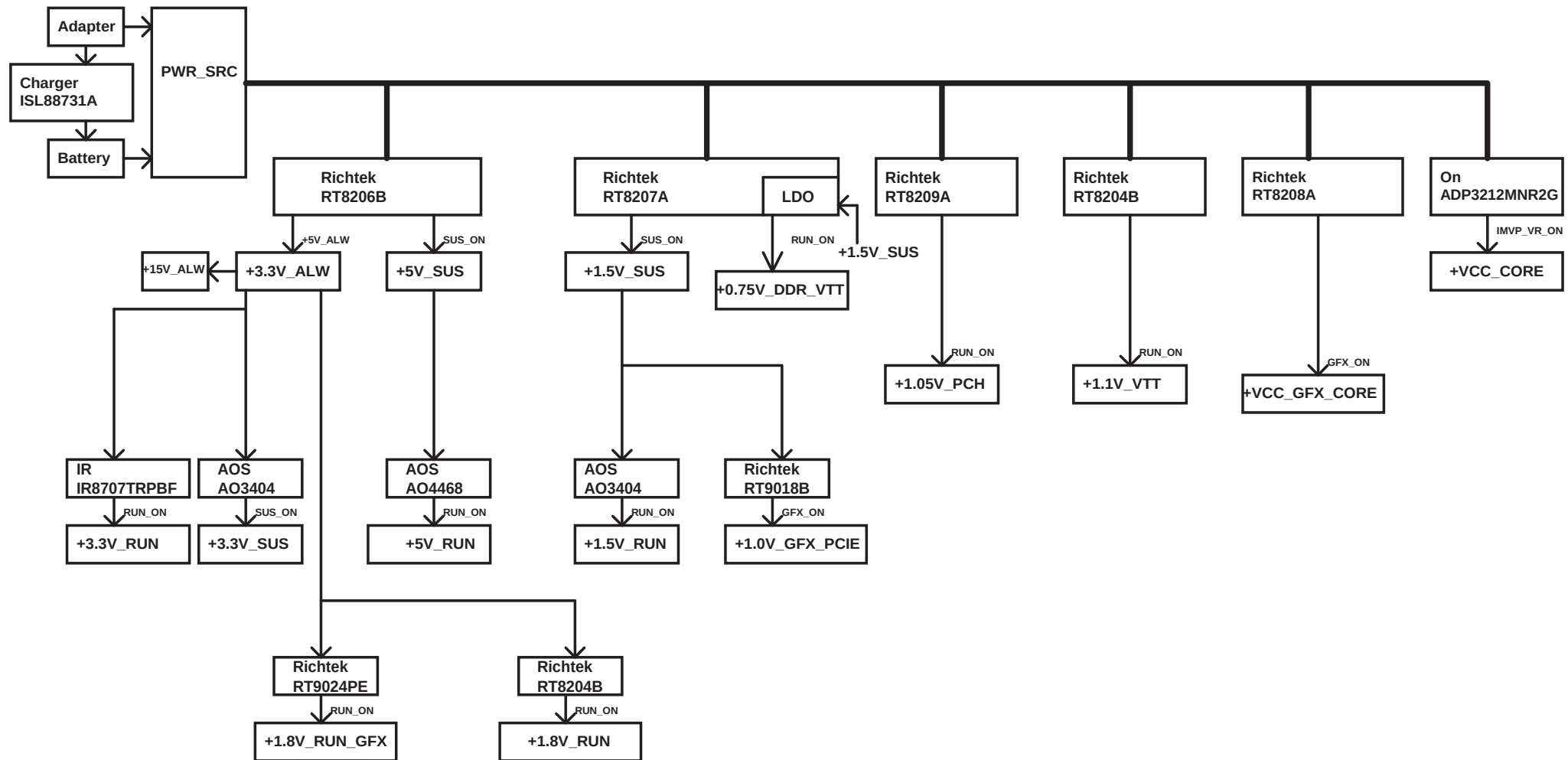


+1.05V_PCH
 Control IC: RT8209A
 H/S MOSFET: AO4496 (AOS), $Q_g=6.1nC$, $R_{ds(on)}=26m\Omega$, $P_D=3.1W$
 L/S MOSFET: AO4468 (AOS), $Q_g=12nC$, $R_{ds(on)}=22m\Omega$, $P_D=3.1W$
 Inductor: 1.5uH $\pm$ 20% 9A (10D40F-1R5M) (TTA), DCR=10.5mohm
 Output Cap: 1*390u, 2.5V(20%, 105C, 6.3*5.8), ESR=10mohm



Title		
+1.05V_PCH(RT8209A)		
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Power Design Block Diagram 2009/08/24

