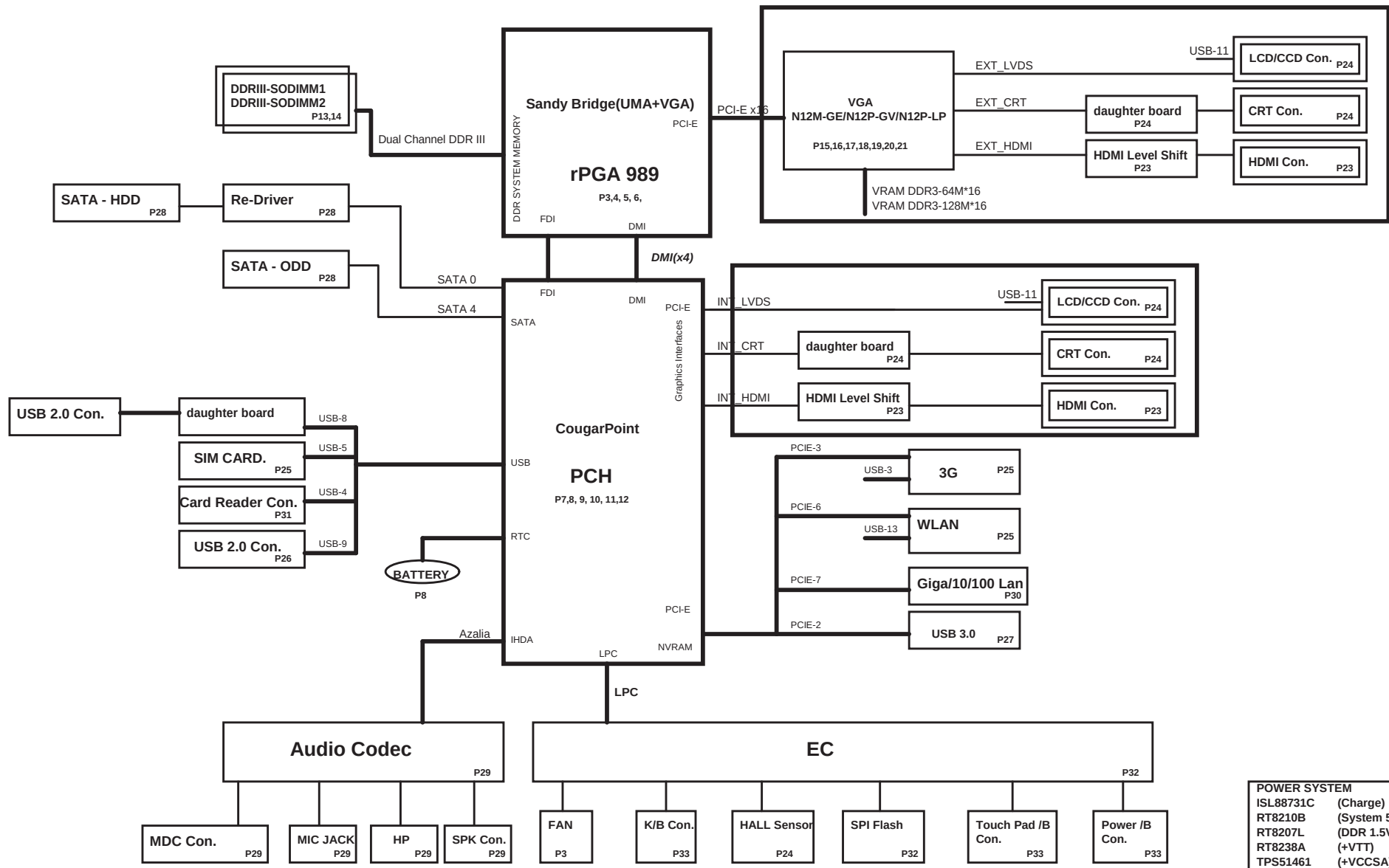


TE5 Block Diagram

<http://hobi-elektronika.net>

01



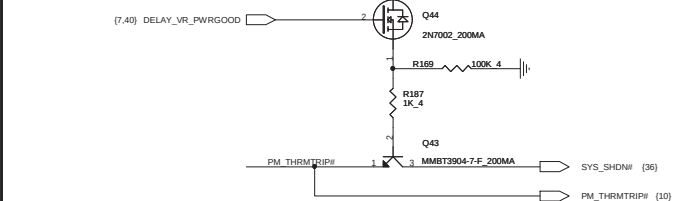
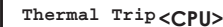
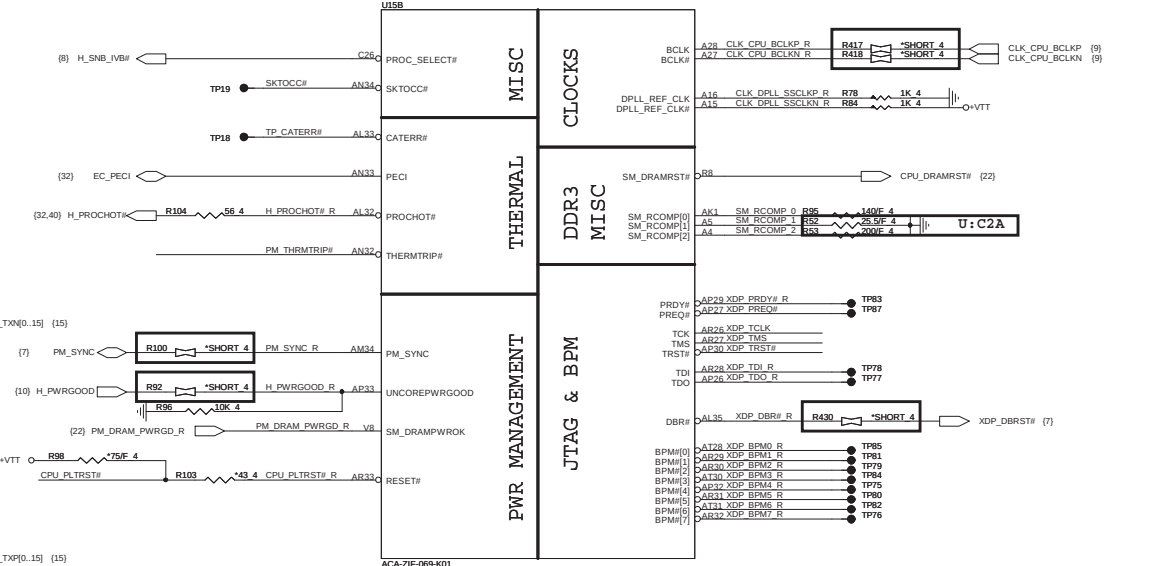
POWER SYSTEM		
ISL88731C	(Charge)	P35
RT8210B	(System 5V/3V)	P36
RT8207L	(DDR 1.5V)	P37
RT8238A	(+VTT)	P38
TPS51461	(+VCCSA)	P39
ISL95835	(+VCC_CORE)	P40
G966A	(+1.8V)	P41
ISL95870A	(+GPU_CORE)	P42

[illegible]

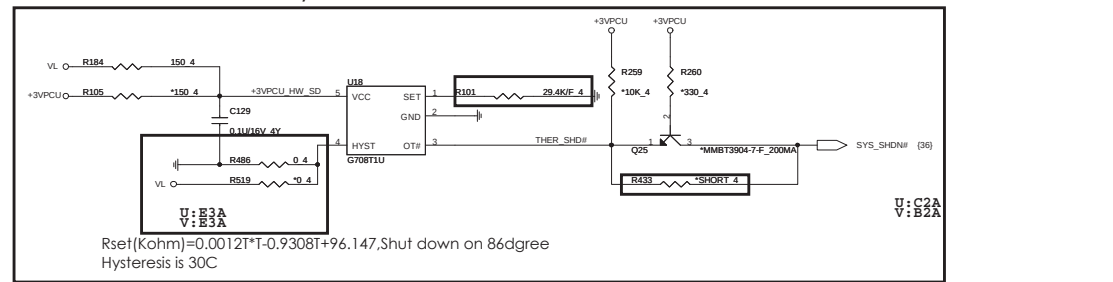
POWER PLANT	VOLTAGE	CONVERTED SIGNAL	Power States Active in
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

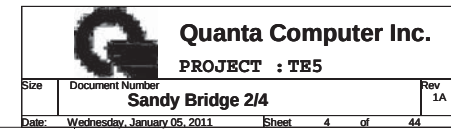
GND PLANE	PAGE
 8769AGND	32
 Audio_GND	29
 Shield_GND	29
 GND	ALL
 ISL95870A_AGND	29

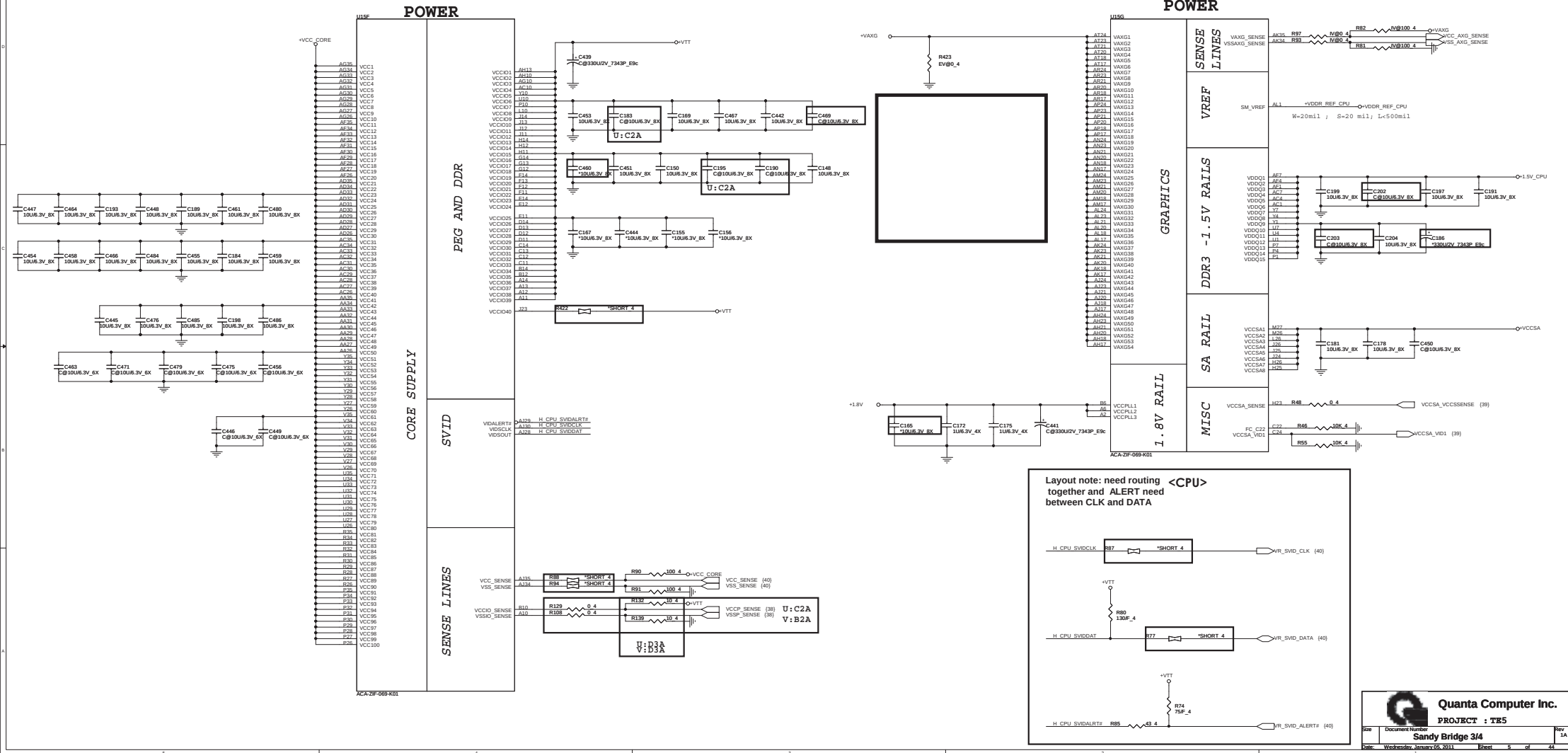
Sandy Bridge Processor (CLK,MISC,JTAG)<CPU>

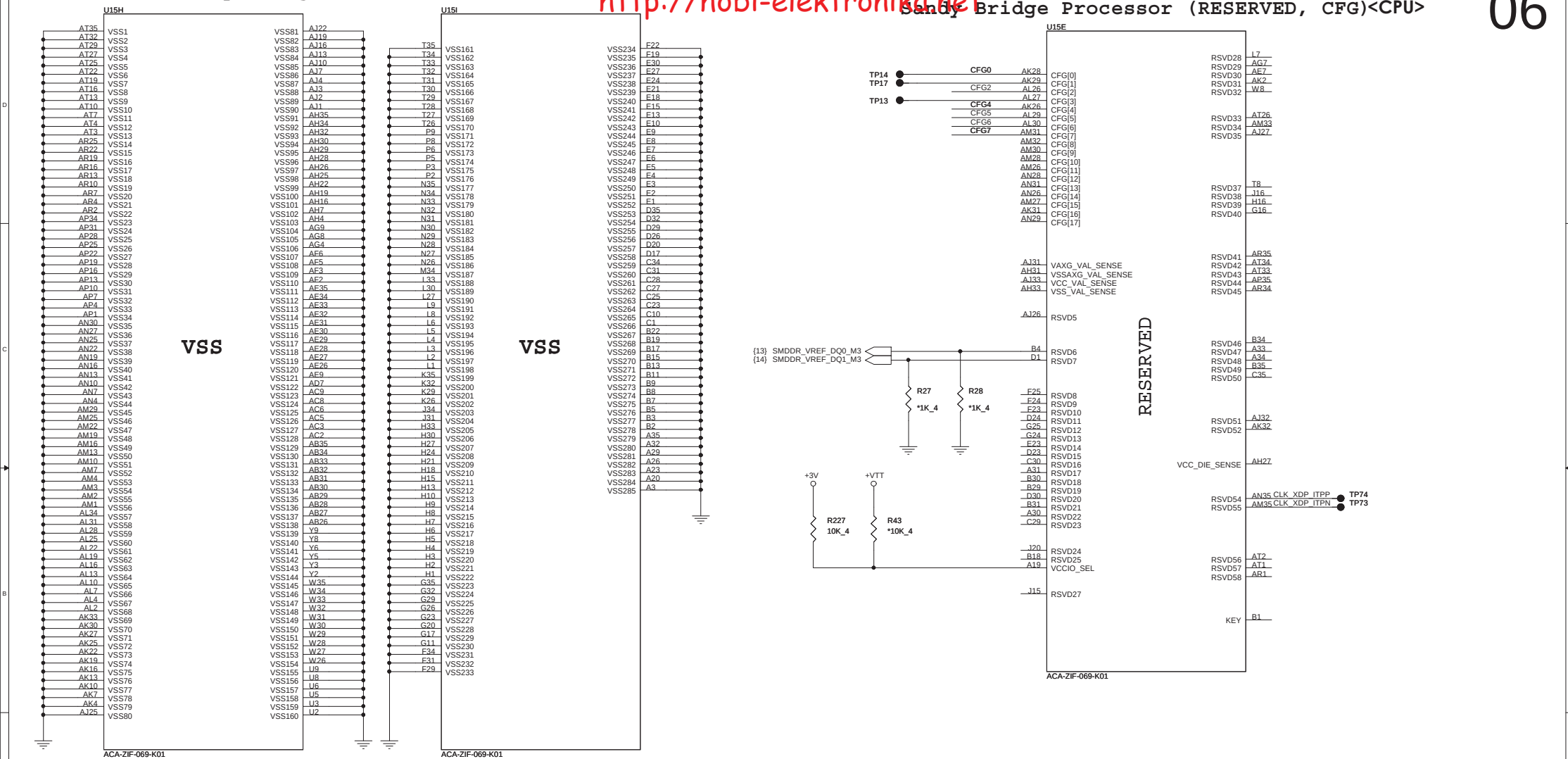


CPU Thermal sensor / MB Local TEMP <THC>







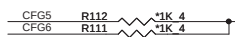
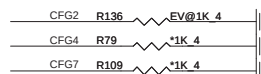


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

<CPU>



CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Quanta Computer Inc.
PROJECT : TE5

Size Document Number
Sandy Bridge 4/4
Rev 1A

Date: Wednesday, January 05, 2011 Sheet 6 of 44

<CLG,UGA,HMG>

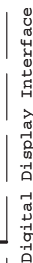
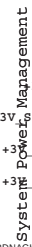


Figure 10 illustrates the pin connections for the R9400. The connections are as follows:

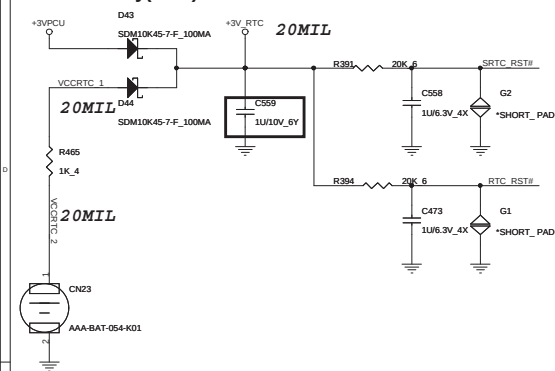
- Row 1:**
 - R496 (10K 4) connects to Rq (O-3V_SS).
 - R492 (10K 4) connects to Rh (O-3V_DSW).
 - R487 (0.4) connects to Rc (AC_PRESENT [32]).
- Row 2:**
 - R469 (0.4) connects to Rd (SUSACK# R).
 - R467 (0.4) connects to Re (SUS_PWR_ACK [32]).
- Row 3:**
 - R503 (0.4) connects to Rf (RSMST#).
 - R502 (0.4) connects to Rg (SYS_HPWP [32,36]).
- Row 4:**
 - R454 (0.4) connects to Rh (SLP_SUS# [32]).

Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff



Size	Document Number	Re
	Cougar Point 1/6	
Date:	Wednesday, January 05, 2011	Sheet 7 of 44

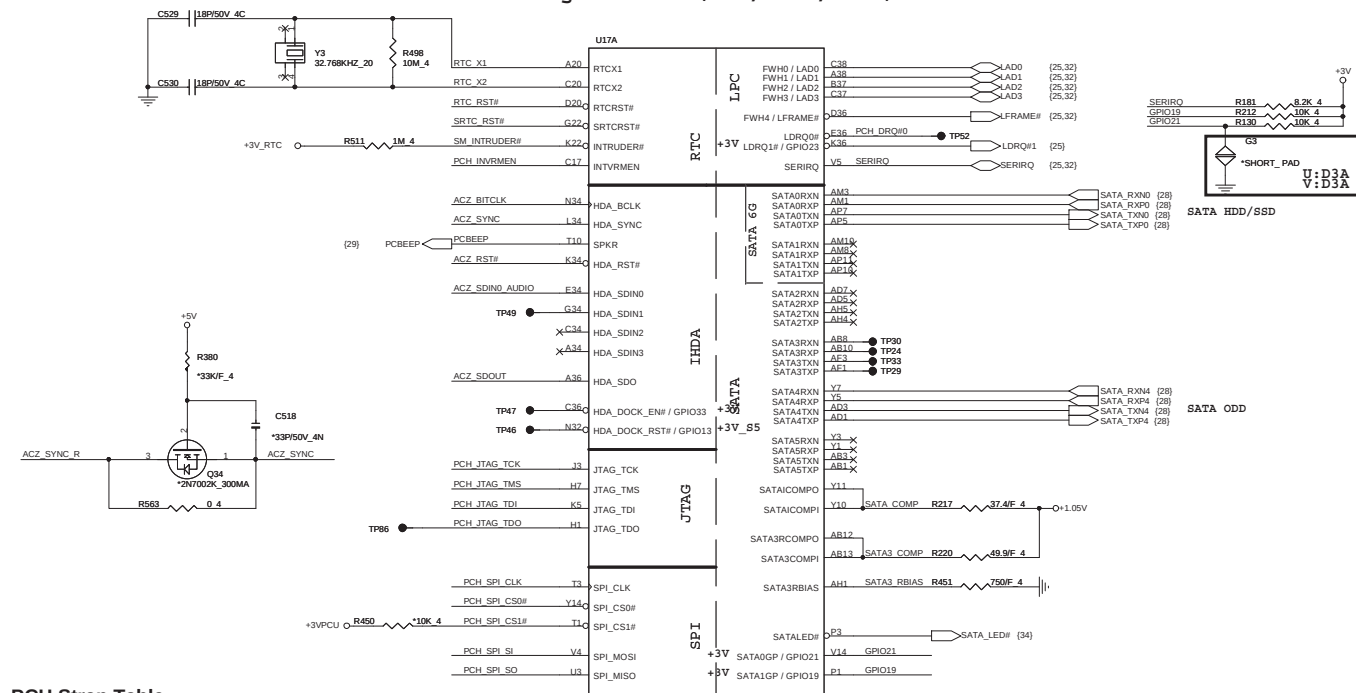
RTC Circuitry(RTC)



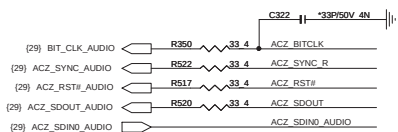
PCH2 (CLG)

<http://hobi-elektronika.net>

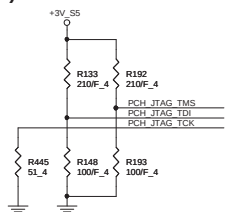
Cougar Point (HDA, JTAG, SATA)



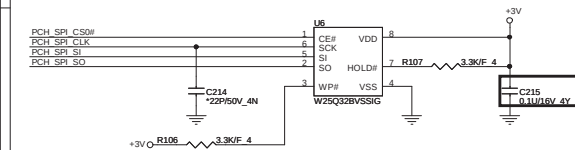
HDA Bus(CLG)



PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)



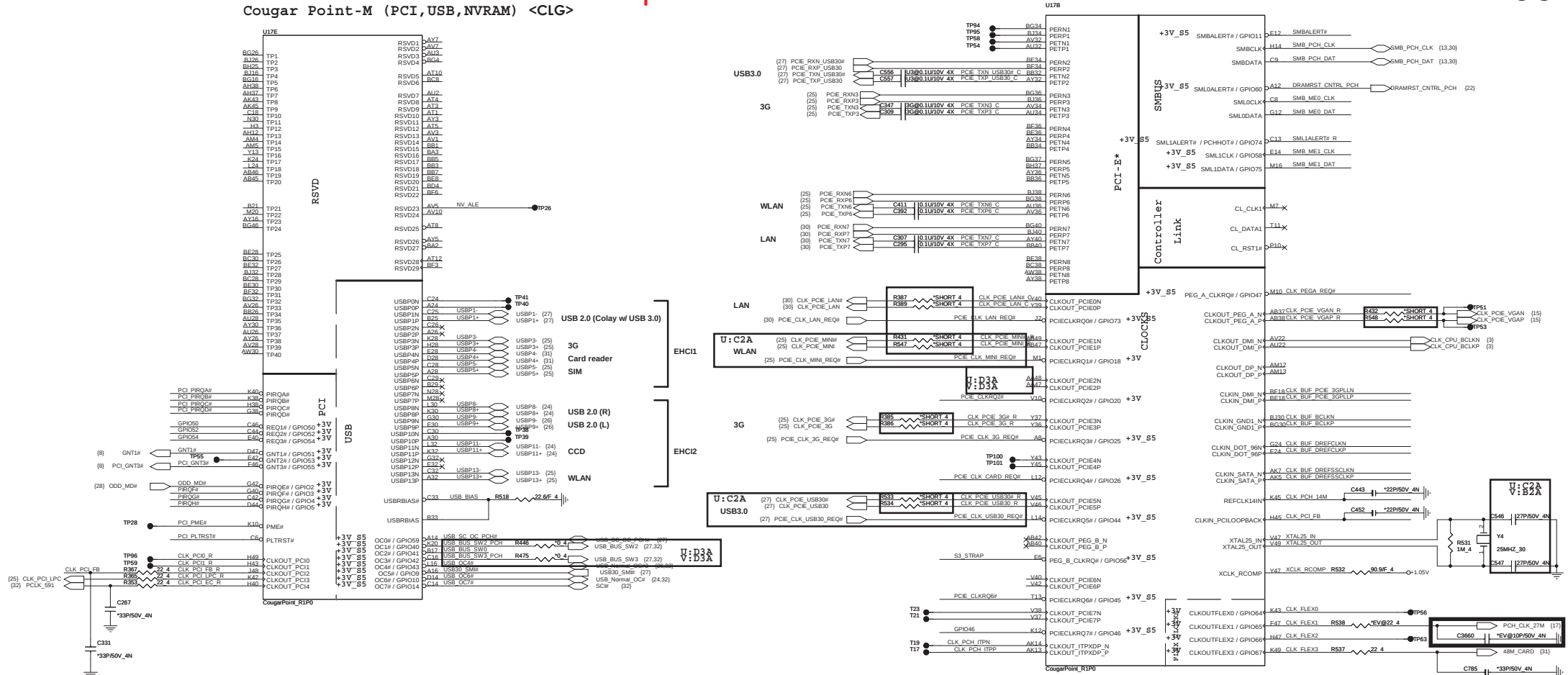
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V0 R116 1K 4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R530 1K 4 PCL_GNT3# (9)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC0 R497 330K 4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		R539 1K 4 GNT1# (9)
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R449 1K 4 GPIO19
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V0 R521 1K 4 ACZ_SDOUT ACZ_SDOUT (32)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R453 2.2K 4 DF_TVS (10) R452 1K 4 H_SNB_VBM# (3)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3V_S5 R206 10K 4 PLL_ODVR_EN (10) R195 1K 4
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S50 R525 1K 4 ACZ_SYNC
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect
GNT2# / GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S50 R313 1K 4 GPIO15 (10)
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GPI / GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled
SATA2GPI / GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	+3V_RTC0 R489 330K 4 DSWVRMEN (7) R490 330K 4

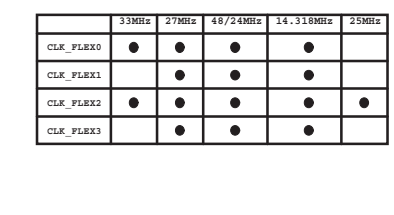
```

r Point-M (PCI-E,SMBUS,CLK) <CLG,U3B,VGA,MNG>

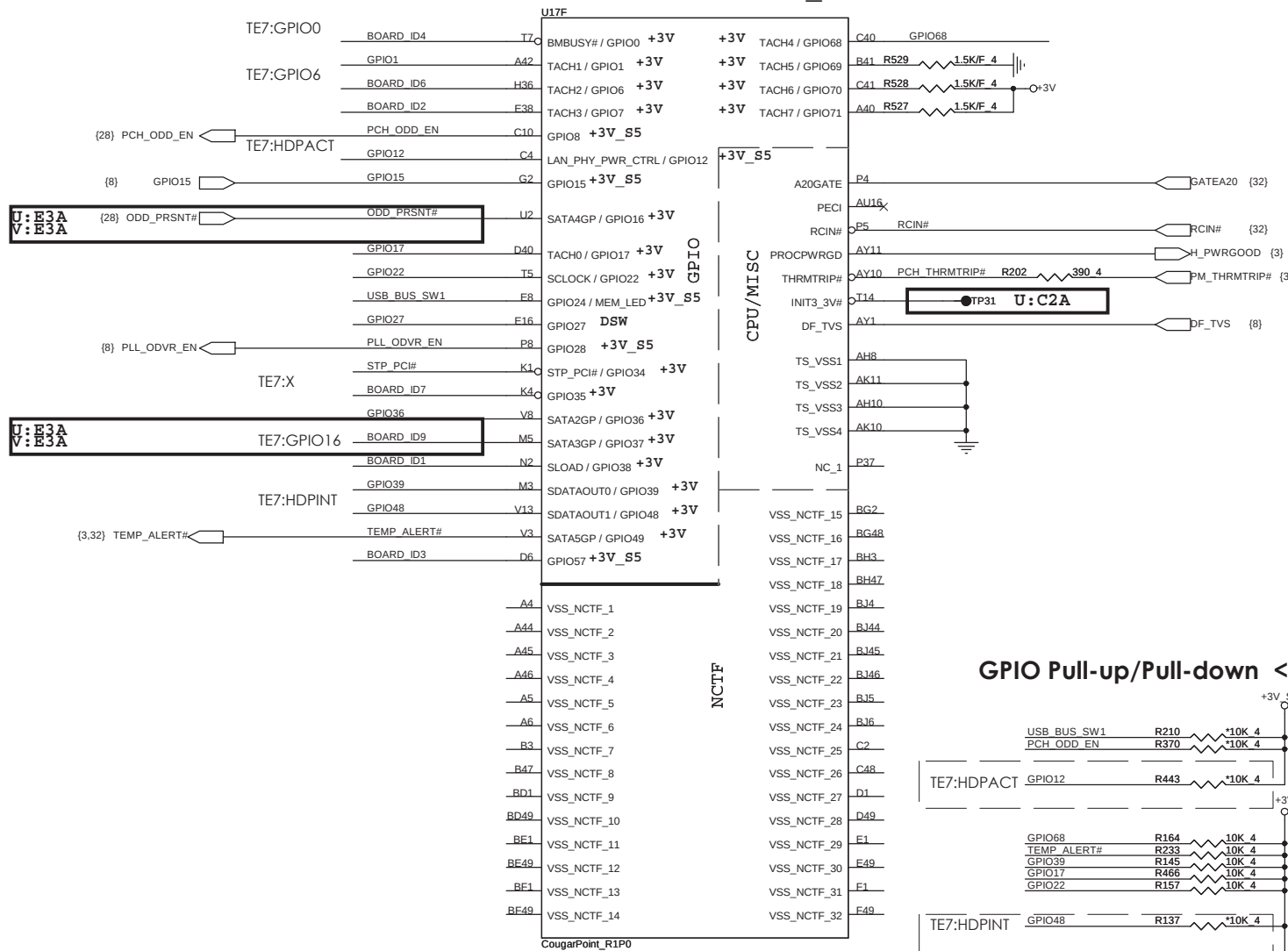
```



PLTRST# <CLG,VGA>	PCI/USB0C# Pull-up <CLG>	CLK_REQ/Strap Pin <CLG>	SMBus/Pull-up <CLG> +3V_55
-------------------	--------------------------	-------------------------	----------------------------

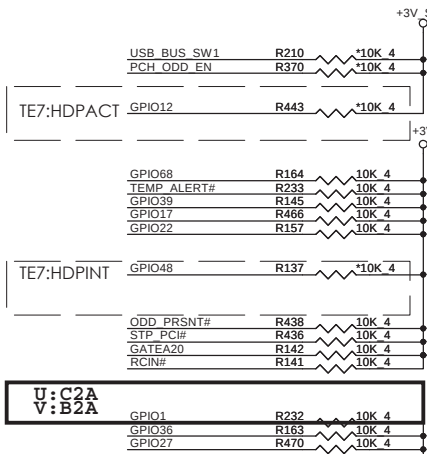


	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0	●	●	●	●	
CLK_FLEX1		●	●	●	
CLK_FLEX2	●	●		●	●
CLK_FLEX3		●		●	

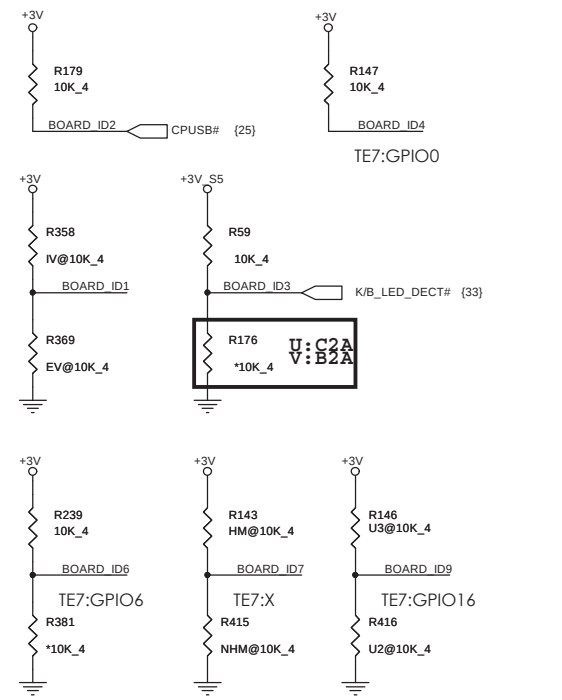


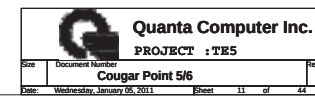
U:C2A

GPIO Pull-up/Pull-down <CLG>

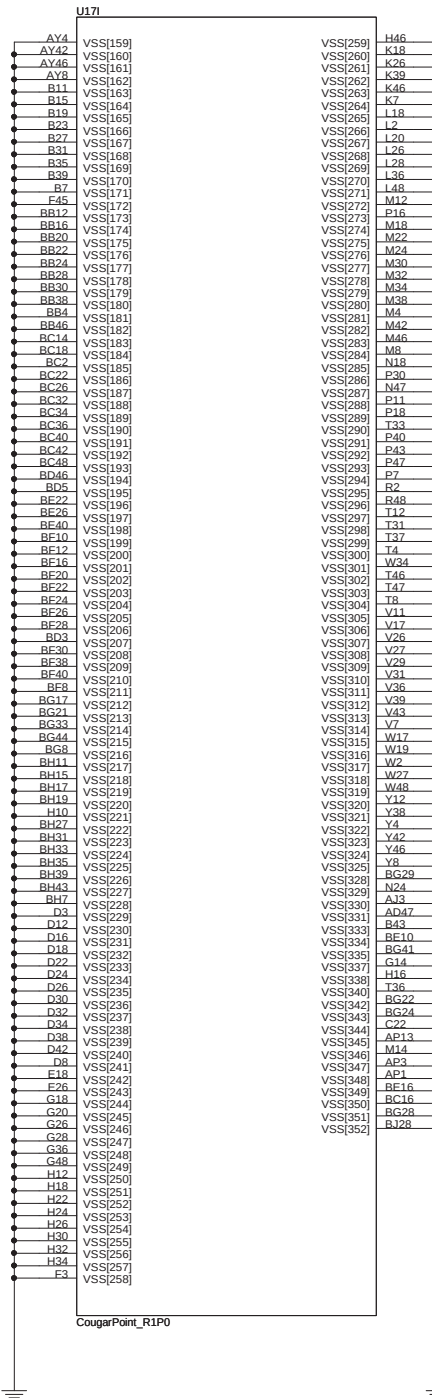
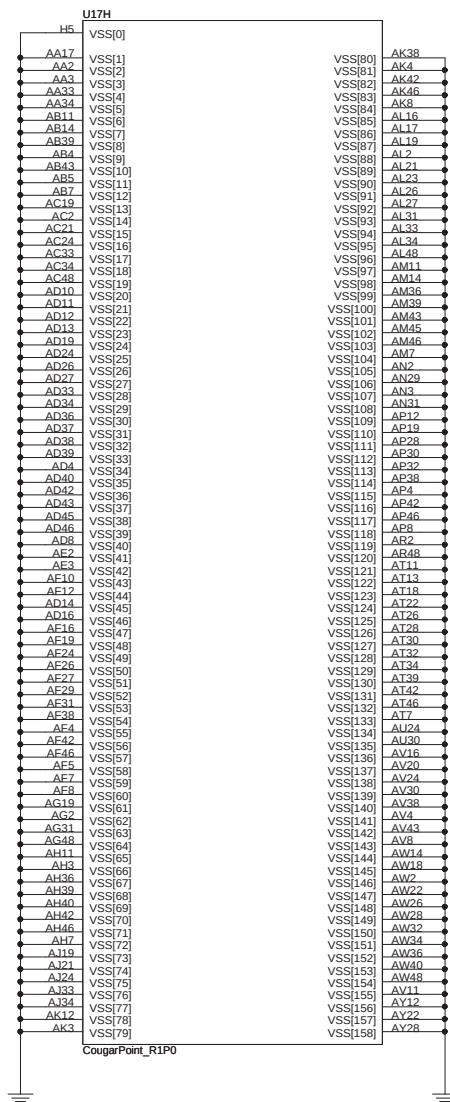


Board ID	ID1	ID2	ID3	ID4	ID6	ID7	ID9	GPIO1
UMA SKU	H	L						
VGA SKU								
W/O 3G		H	L					
W/ 3G								
W/O LED KB			H	L				
W/ LED KB								
14"				H	L			
15"								
W/ MDC				H	L			
W/O MDC								
W/ HDMI						H	L	
W/O HDMI								
USB3.0							H	L
USB2.0								
W/ G-sensor								H
W/O G-sensor								L





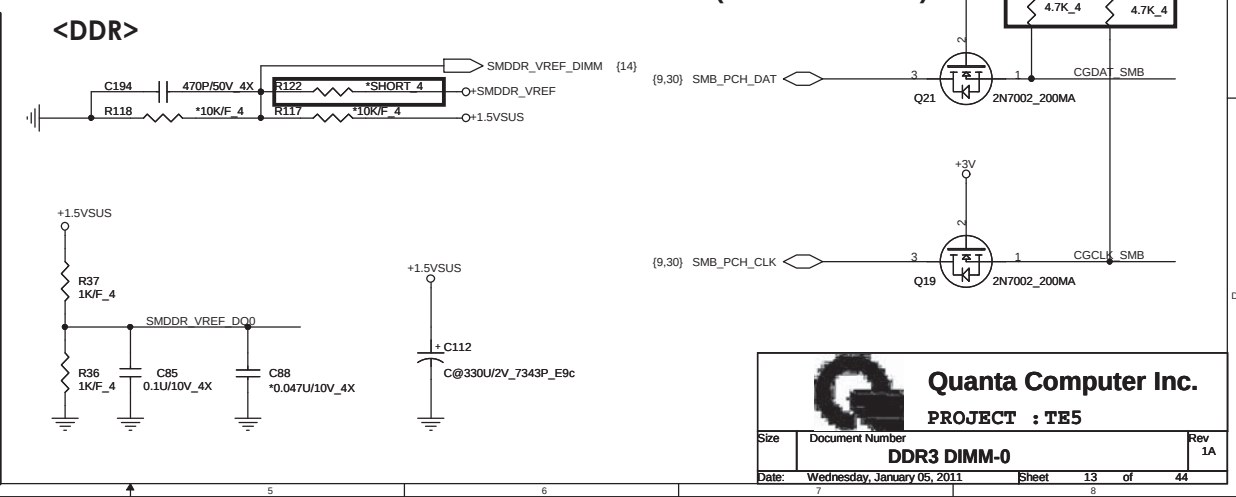
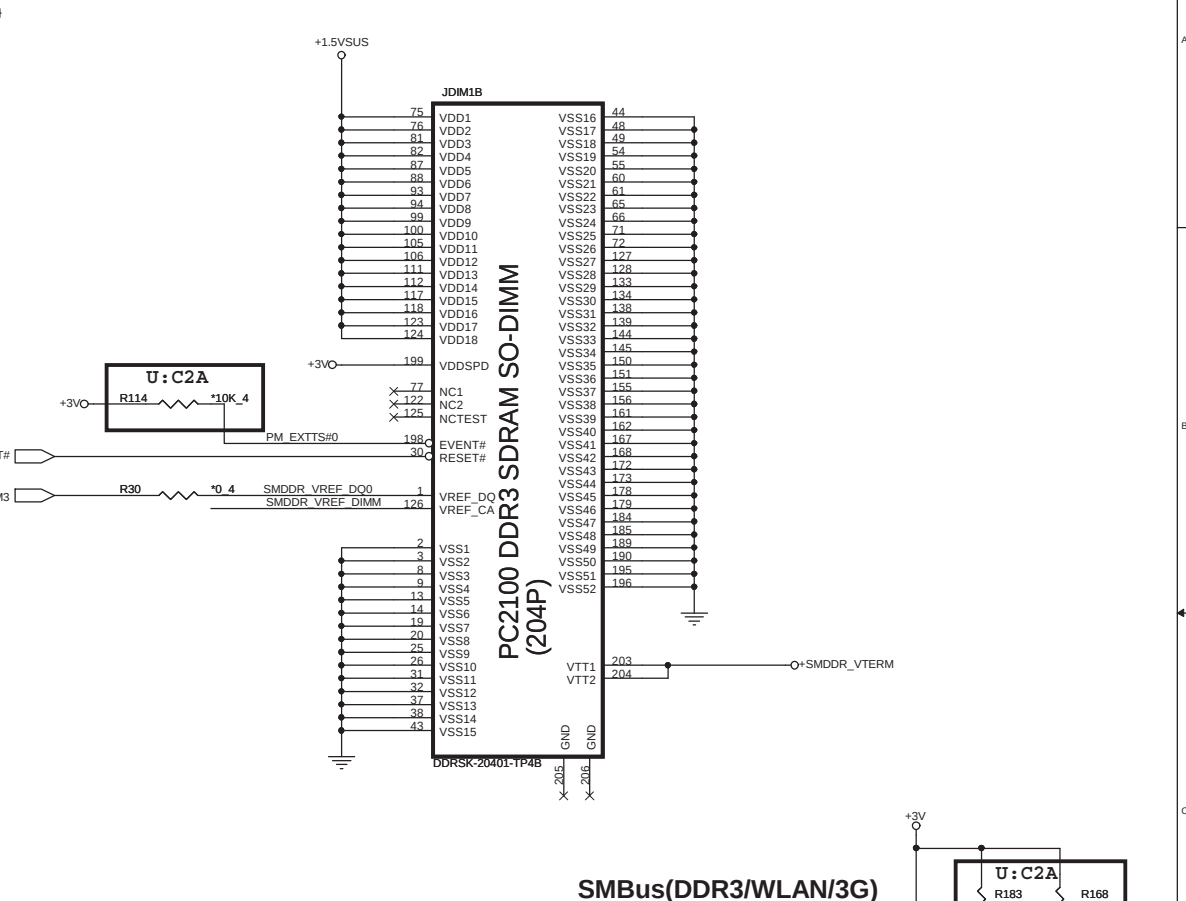
IBEX PEAK-M (GND)

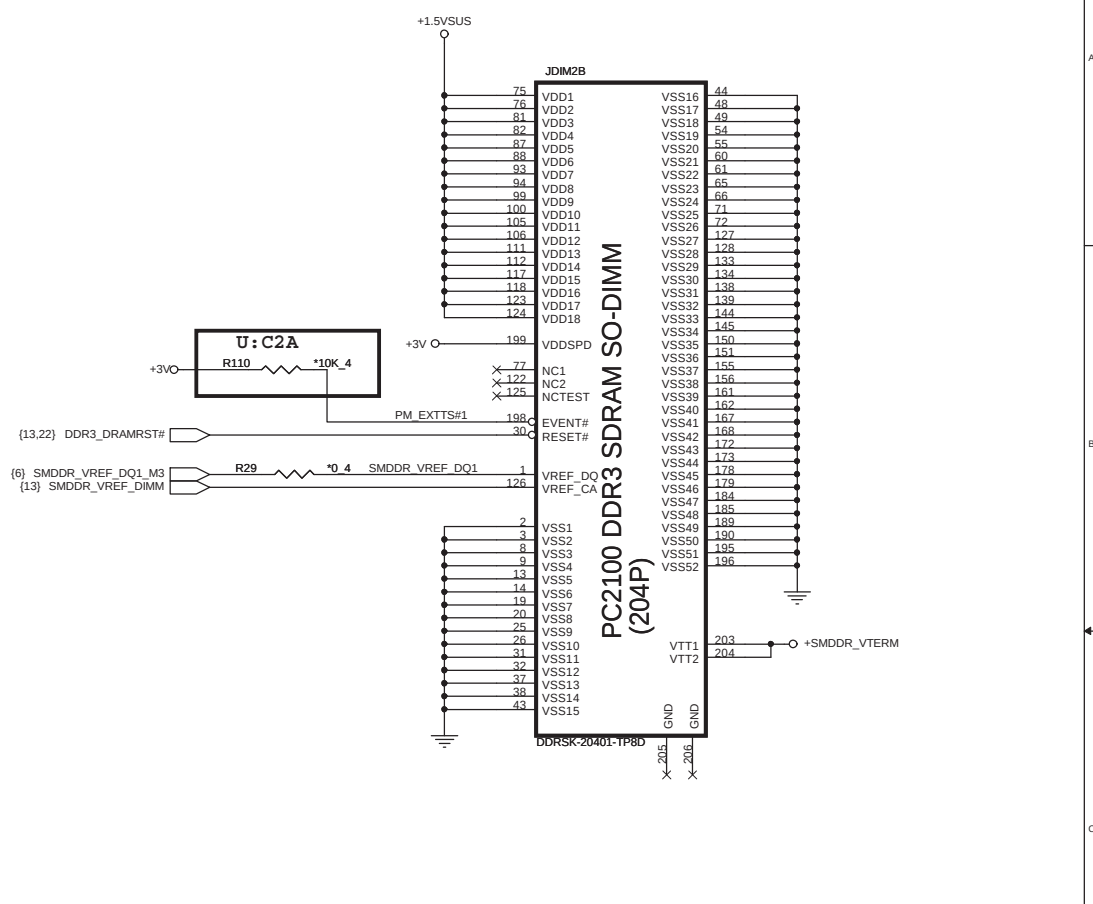
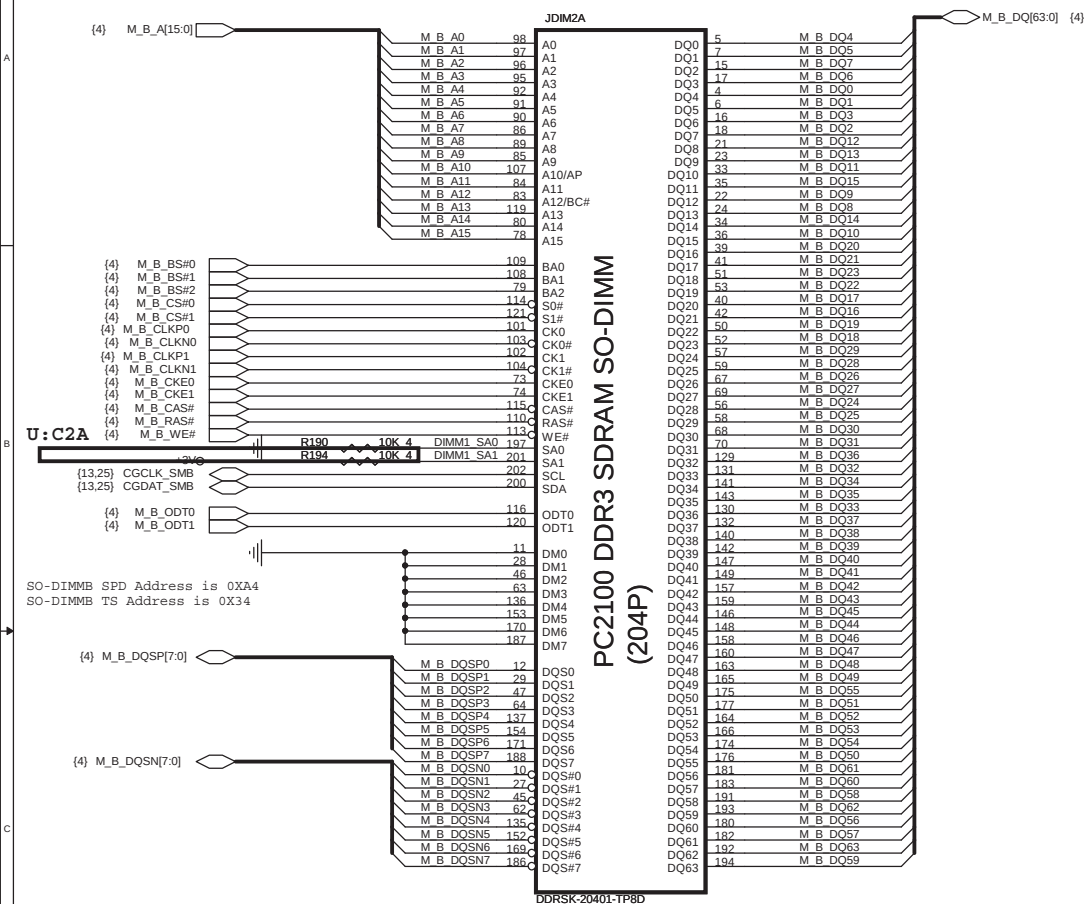


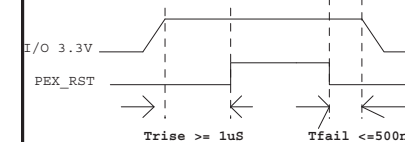
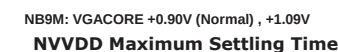
Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Rev
	Cougar Point 6/6	1A
Date:	Wednesday, January 05, 2011	Sheet 12 of 44



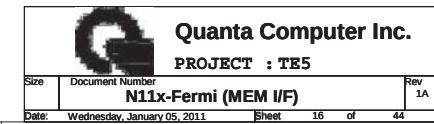




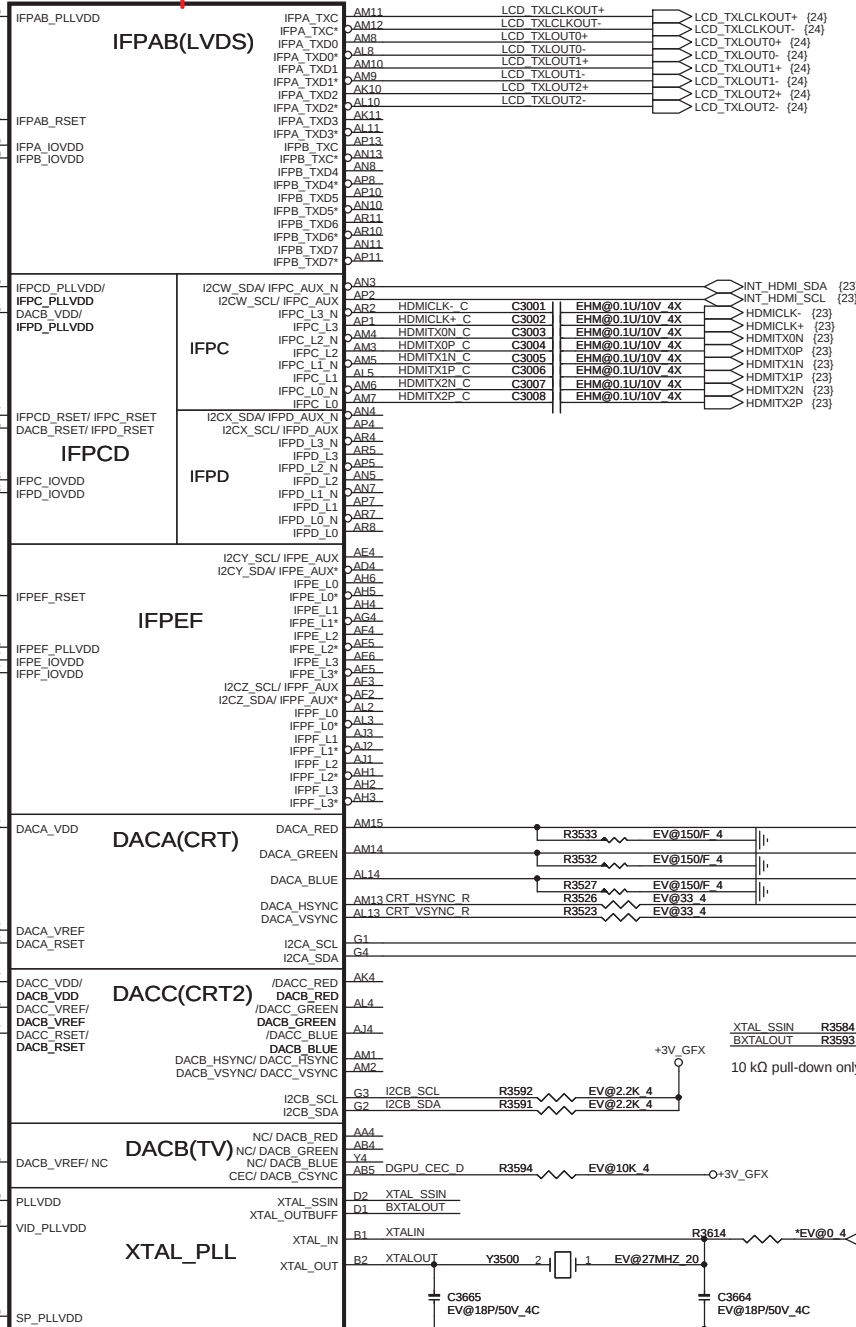
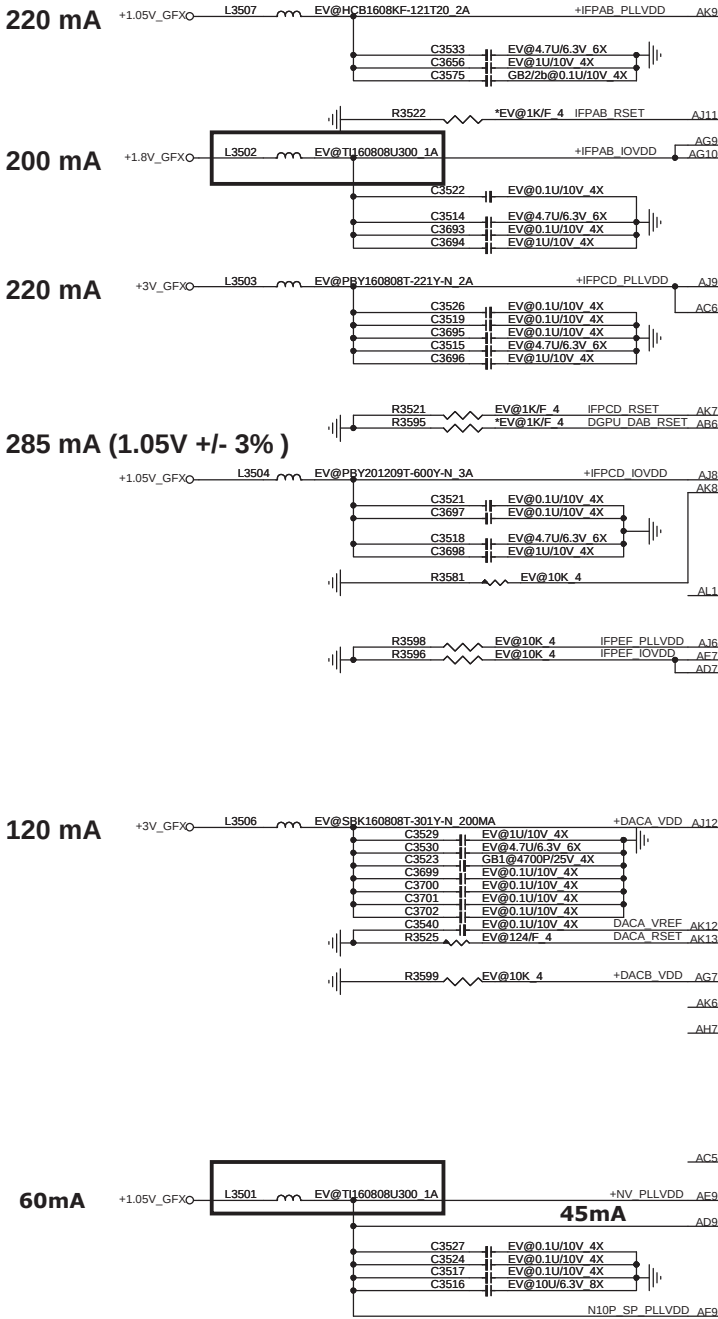
Quanta Computer Inc.

PROJECT : TE5

Size	Document Number	Revision
	N11x-Fermi PCIE	
Date:	Wednesday, January 05, 2011	Sheet 15 of 44



GPU3500D
fcbg973-nvidia-n11p-es-4
COMMON



STUFF PDs on XTALSSIN and
XTALOUTBUFF WHEN EXT_SS
IS NOT
USED

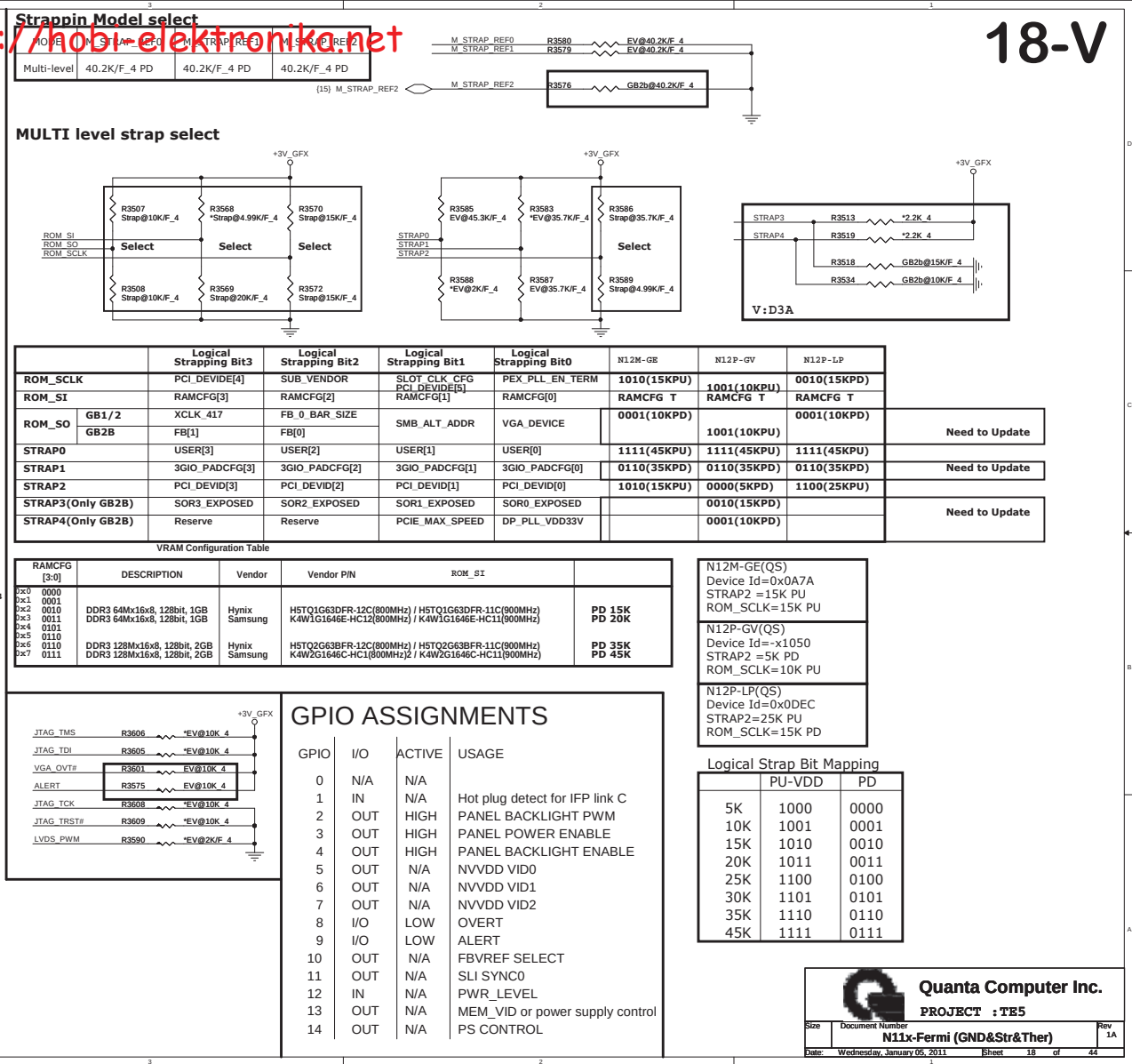
Quanta Computer Inc.

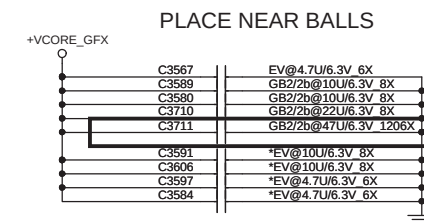
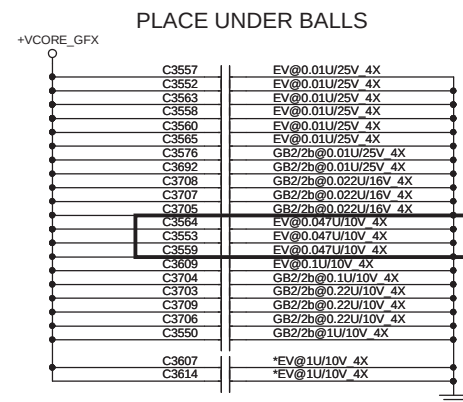
PROJECT : TE5

Size Document Number Rev 1A

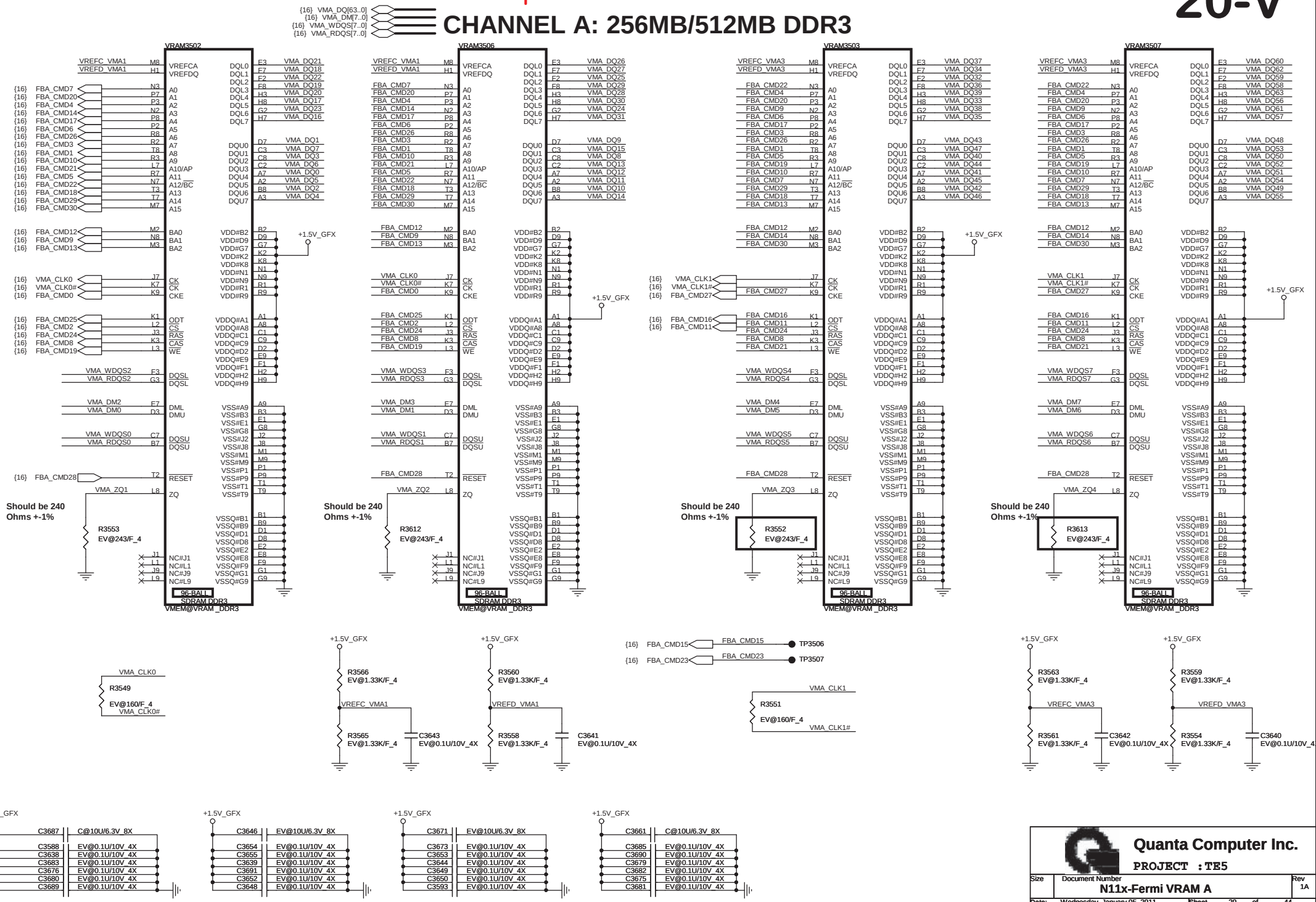
N11x-Fermi (DISPLAY)

Date: Wednesday, January 05, 2011 Sheet 17 of 44





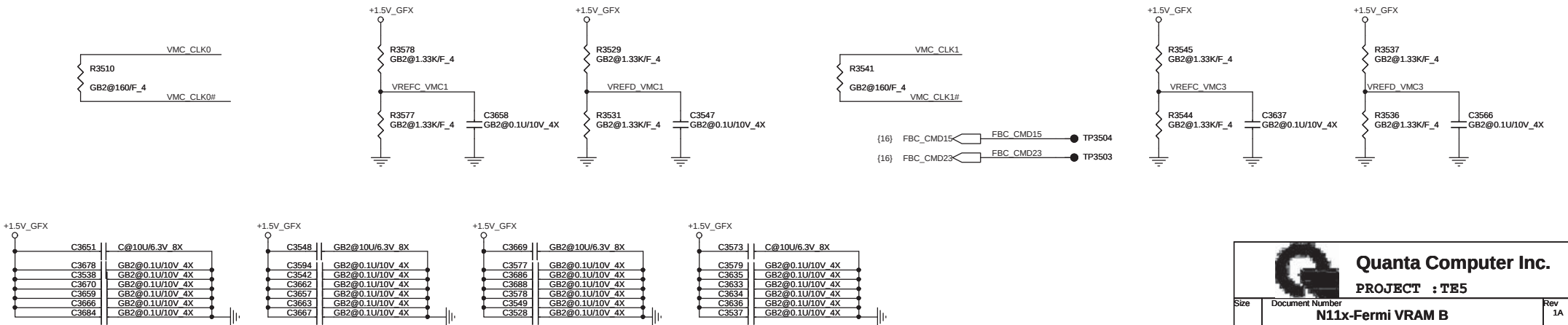
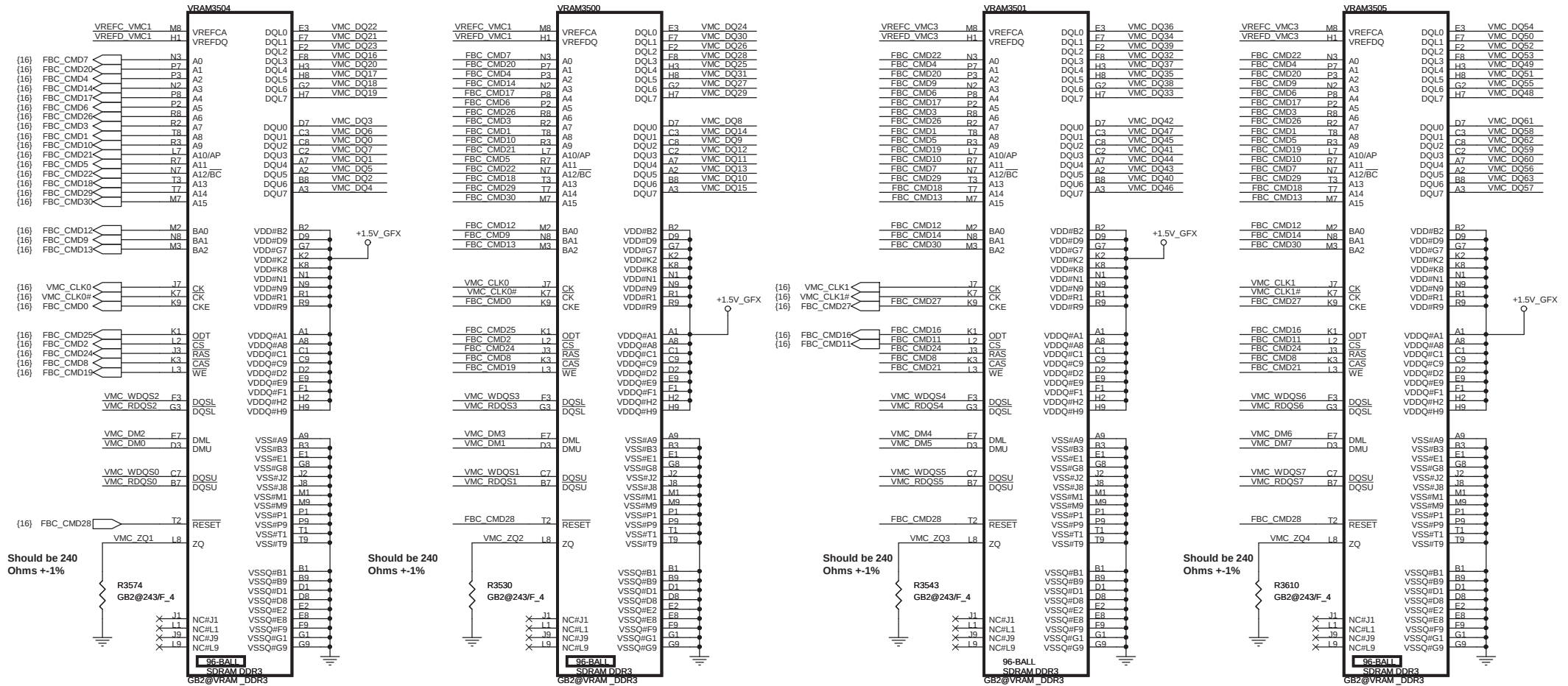
CHANNEL A: 256MB/512MB DDR3

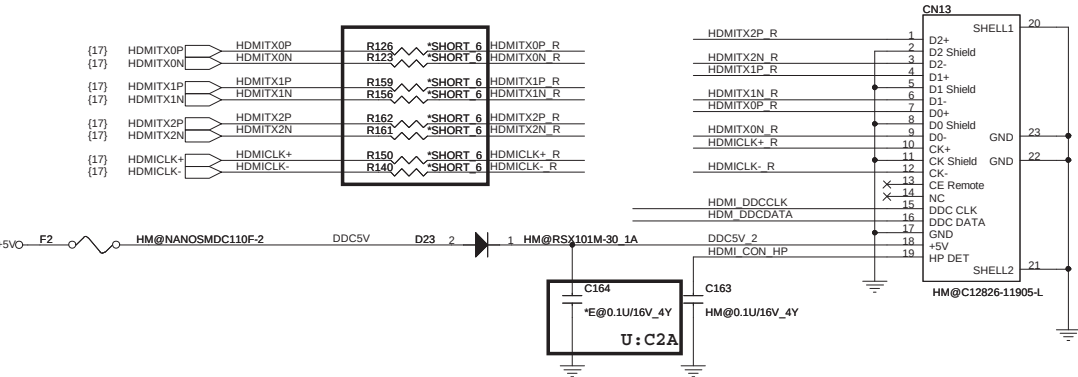


http://hobi-elektronika.net
CHANNEL B: 256MB/512MB DDR3

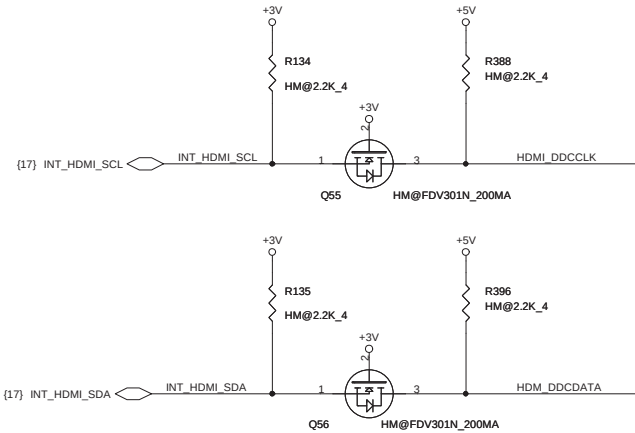
21-V

(16) VMC_DQ[63..0]
(16) VMC_DM[7..0]
(16) VMC_WDQS[7..0]
(16) VMC_RDQS[7..0]

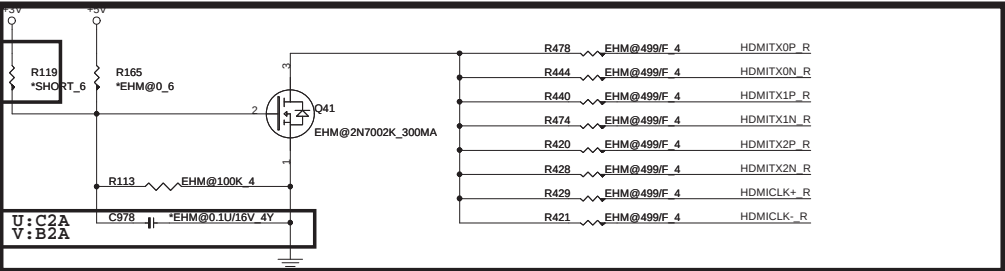




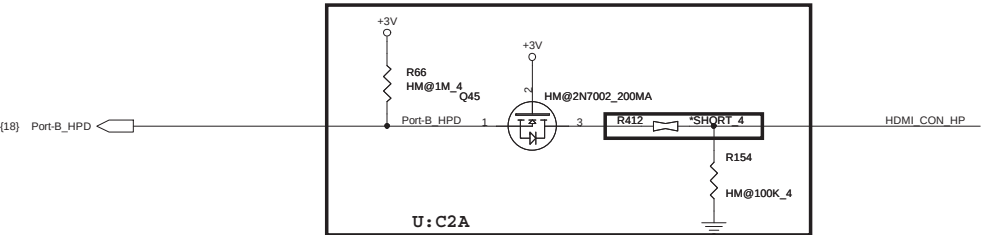
HDMI-SMBus <HDM>

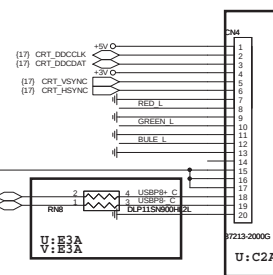
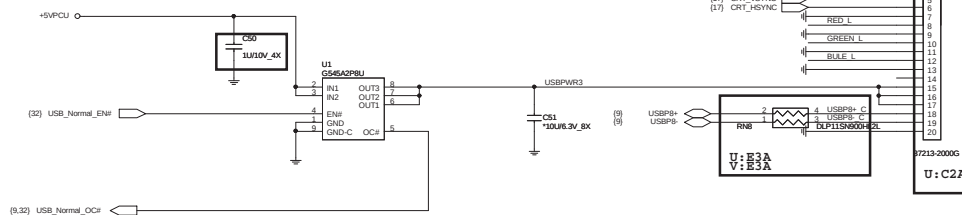
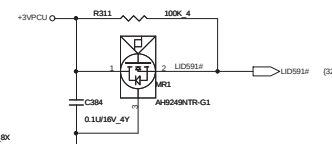


HDMI-passive level shift <HMP/HMG>



HDMI-HPD <HMP/HMG>





(32) BT_FCCTRL

WIMAX_FO

R63

10K 4

R69

*SHORT_4

BT_FCCTRL_BT#

C42

DTC144EUBTL_30MA

SERIRQ debug

R186

PLTRST#

(8,32) SERIRQ LDRQ#1

R292

R66

*NMP#Q0_4 SERIRQ debug

NMP#RX02 LDRQ#1 debug

PLTRST# debug

(9) CLK_PCI_LPC

R284

NMP#Q0_4 PCLK debug

(9) PCIE_TXP6

(9) PCIE_TXN6

(9) PCIE_RXP6

(9) PCIE_RXN6

(9) CLK_PCIE_MINI

(9) CLK_PCIE_MINI#

(9) PCIE_CLK_MINI_REQ#

BY_CTLSTR_B#

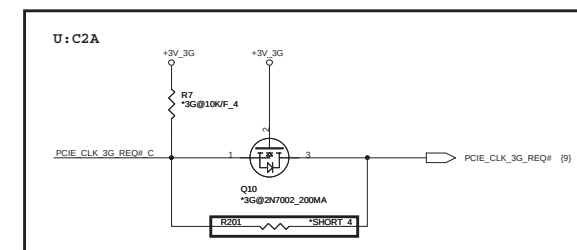
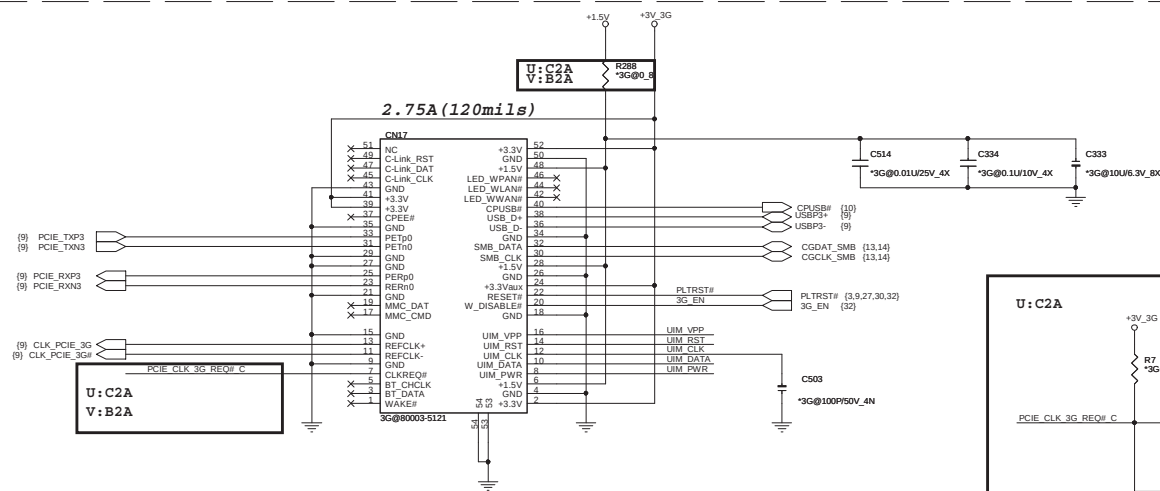
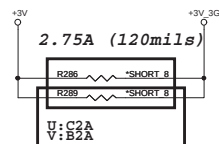
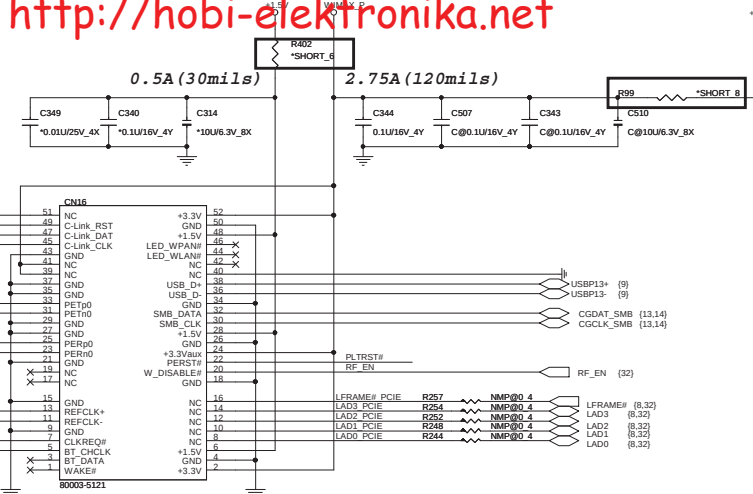
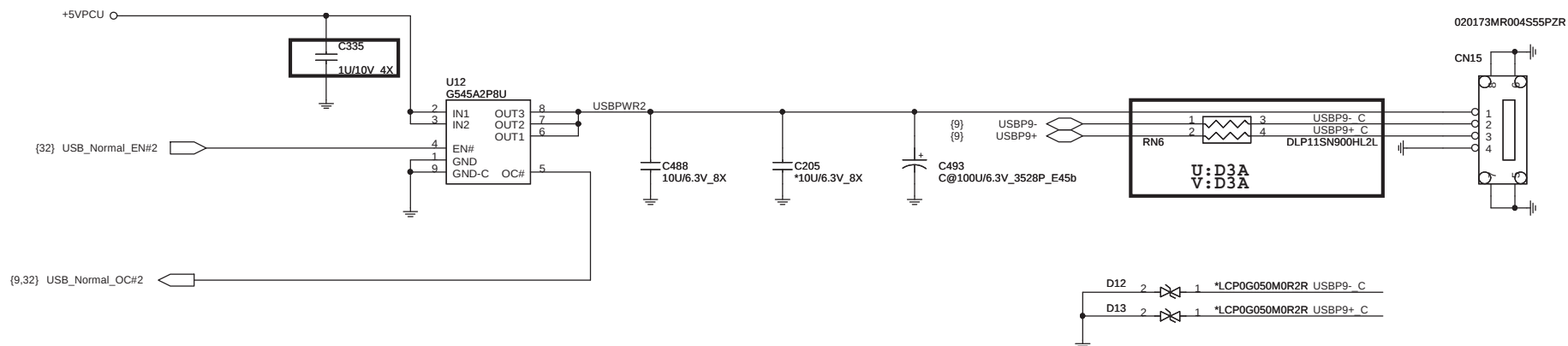
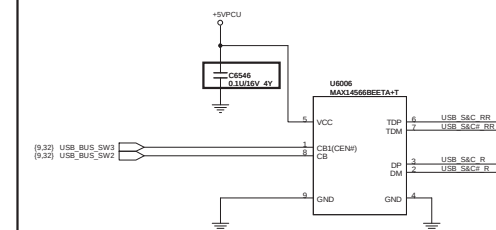


Figure 1: USB2.0 PHY connection diagram. The diagram shows a JSM1 component connected to a USB2.0 PHY. The JSM1 pins are: 1 (UIM_CLK), 2 (UIM_DATA), 3 (UIM_DATA), 4 (UIM_RST), 5 (UIM_VPP), 6 (UIM_PWR), 7 (UIM_PWR), 8 (X), 9 (1411), 10 (1312). The PHY pins are: C294 (3G00.1U/0V_4), 9 (USBP5+), 9 (USBP5-). The PHY is connected to a 3G08511-120N component.



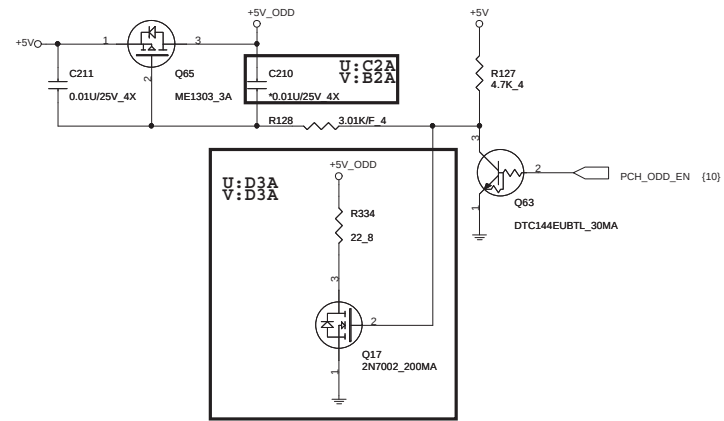
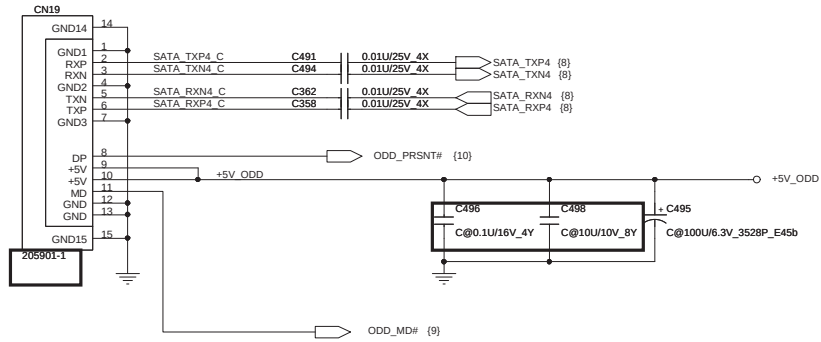
U:C2A



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

SATA ODD

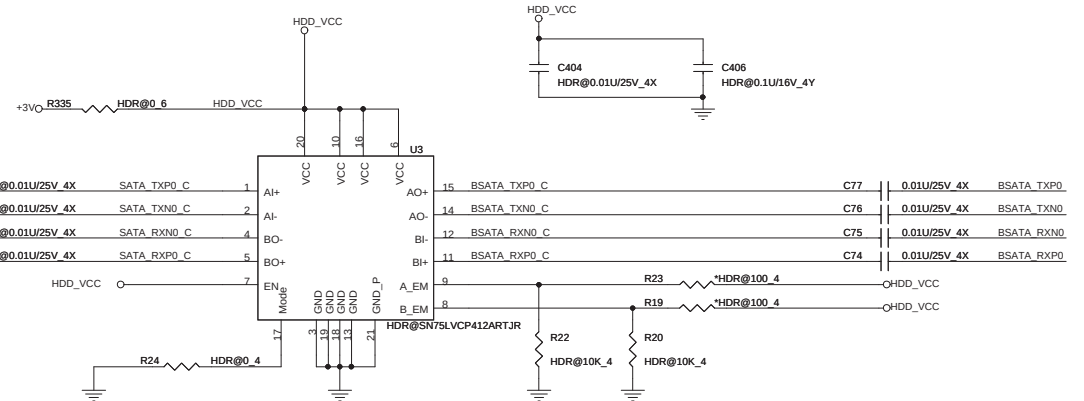
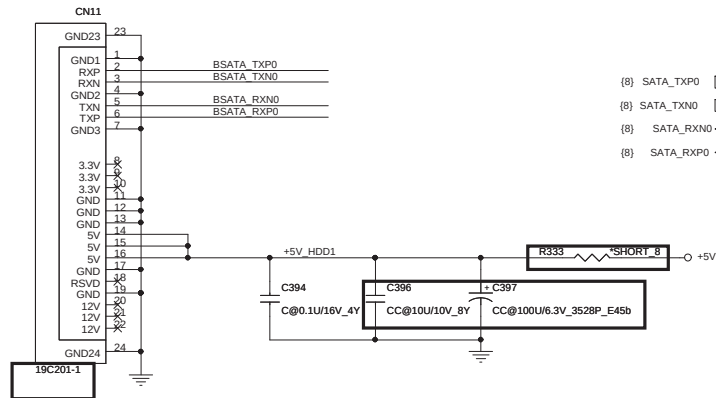
[ODD]



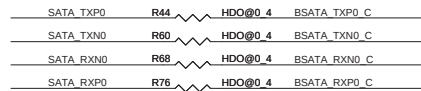
SATA HDD

[HDD]

SATA HDD Re-driver IC



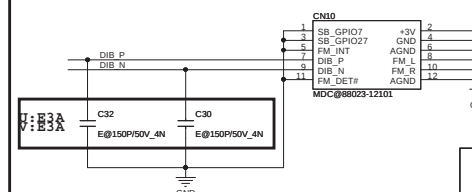
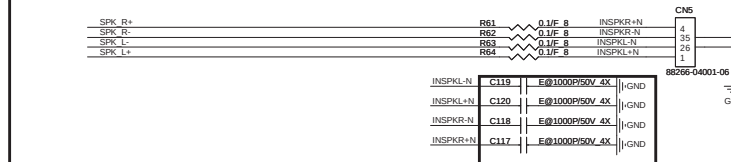
Colay with Redriver IC



SATA Re-driver Bypass

Quanta Computer Inc.
PROJECT : TE5

Size: Document Number
HDD/ODD/MDC
Date: Wednesday, January 05, 2011 Sheet 28 of 44 Rev 1A

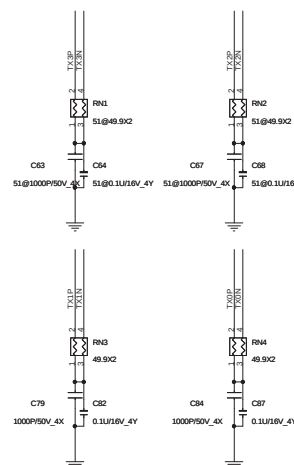


PCIE_WAKE# PCIE_WAKE# (7.27)

SB SMBDATA1 LAN R16 0.4 SMB_PCH_DAT (9.13)

SB SMBCLK1 LAN R18 0.4 SMB_PCH_CLK (9.13)

PLACE NEAR LAN IC SIDE



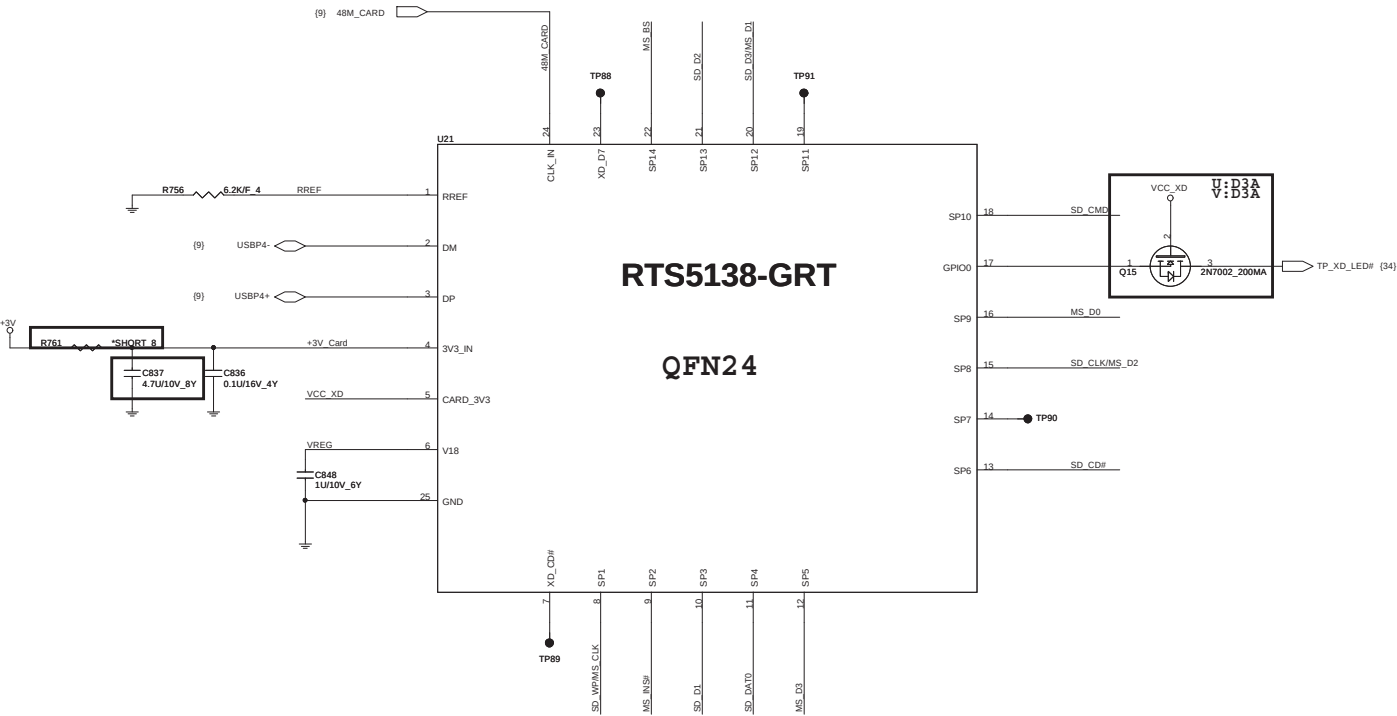
LEDO = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

[illegible]

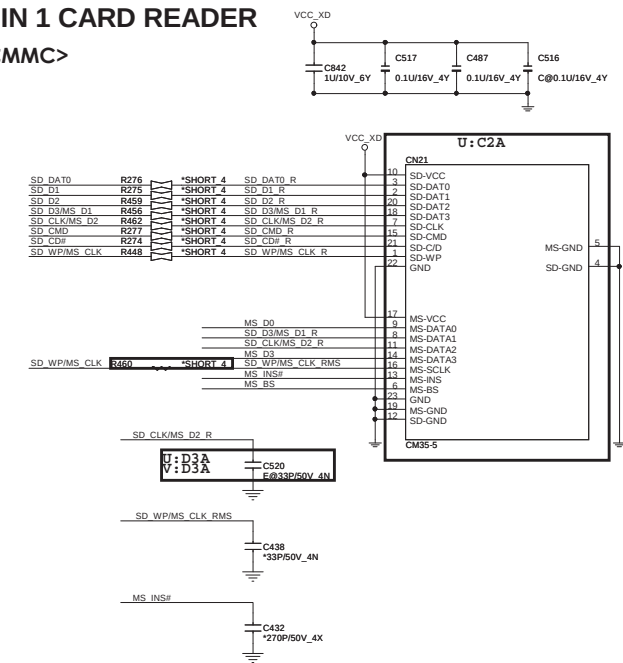
 Quanta Computer Inc. PROJECT : TE5	
Size	Document Number Atheros Lan
Date:	Wednesday, January 05, 2001 Sheet 30 of 44

3 IN 1 CARD READER
Card reader controller <MMC>

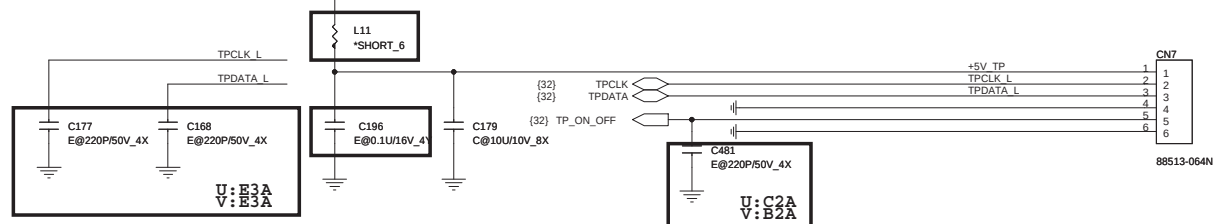
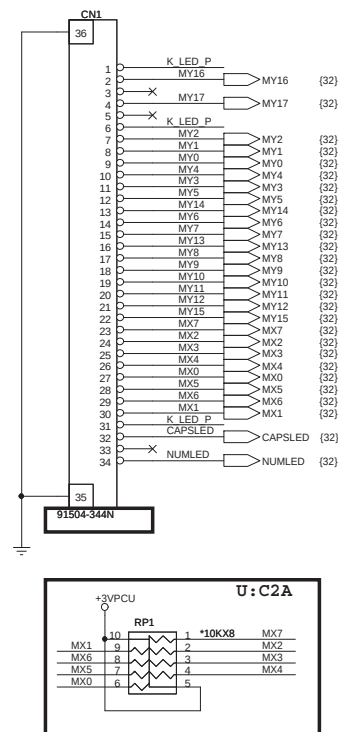
<http://hobi-elektronika.net>



3 IN 1 CARD READER
<MMC>



TP board <TRD

[illegible]

CPU

HOLE29
h-tc315bc217d142p2

HOLE30
h-tc315bc217d142p2

HOLE31
h-tc315bc217d142p2

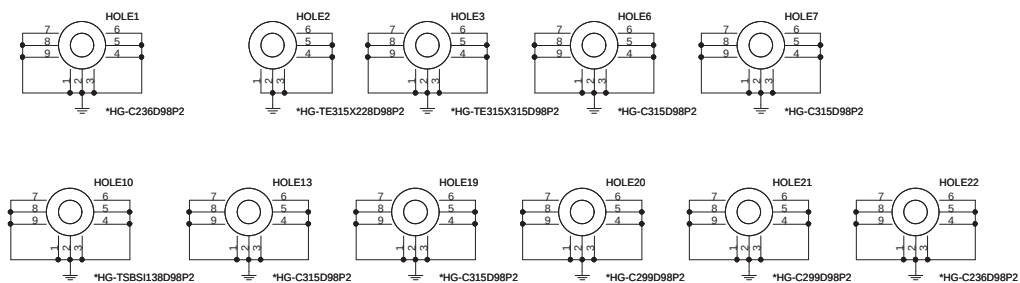
HOLE32
h-tc315bc217d142p2

Diagram illustrating the connection of the HOLE9, HOLE24, HOLE8, and HOLE12 to the ground plane using the *H-C131D91P2 component.

MINI CARD

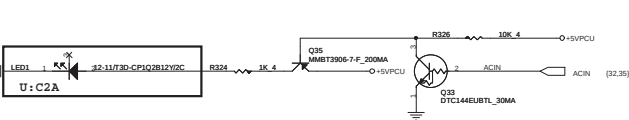
Diagram illustrating the pin configurations for four Mini Card modules, each with a central circular connector and two side connectors. The pin numbers are indicated by the numbers 7, 8, 9, 4, and 6.

- HOLE15:** *HG-C236D15P2
- HOLE18:** *HG-C236D15P2
- HOLE16:** *HG-C236D15P2
- HOLE17:** *HG-C236D15P2

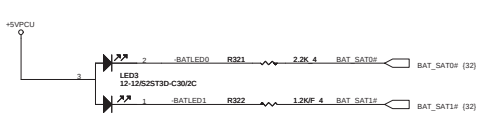


LED <LED>

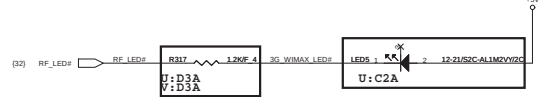
AC-IN



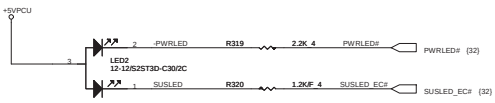
BATTERY



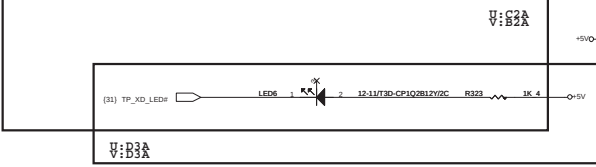
RF LED



POWER



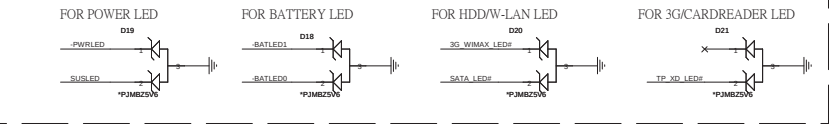
CARDREADER



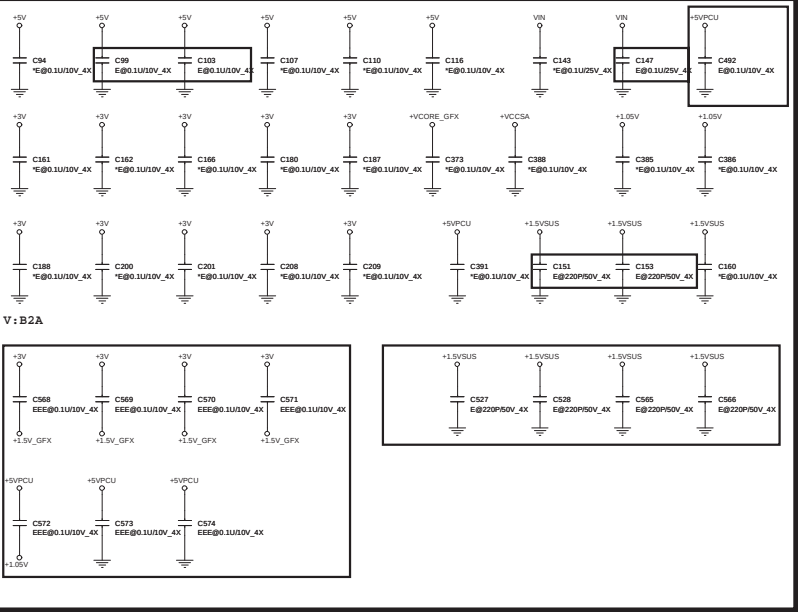
HDD/ODD



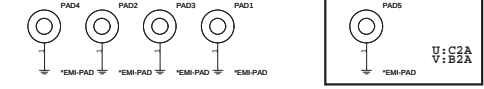
ESD Protect

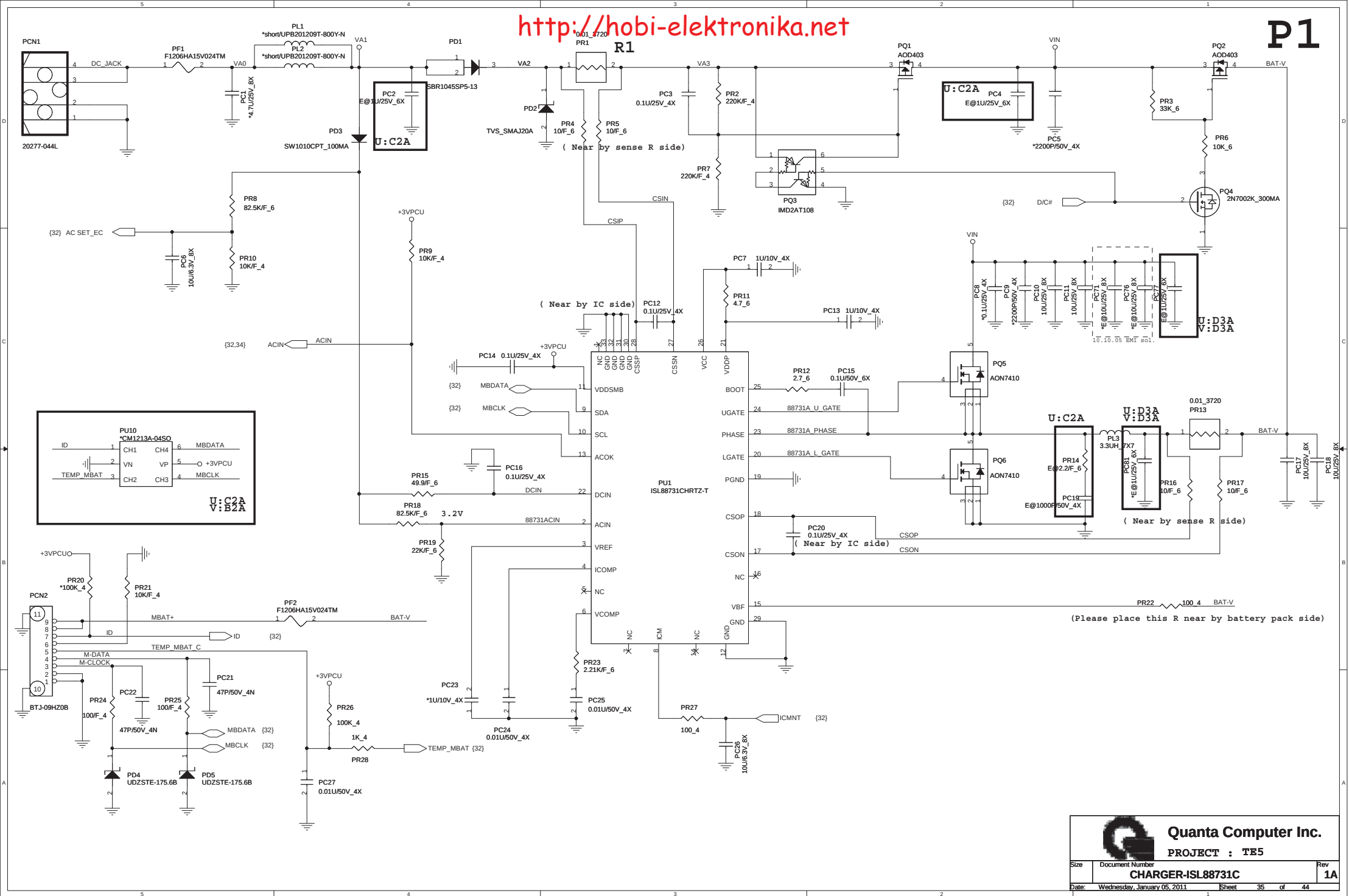


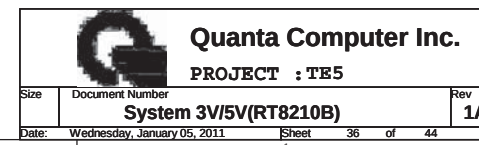
EMI

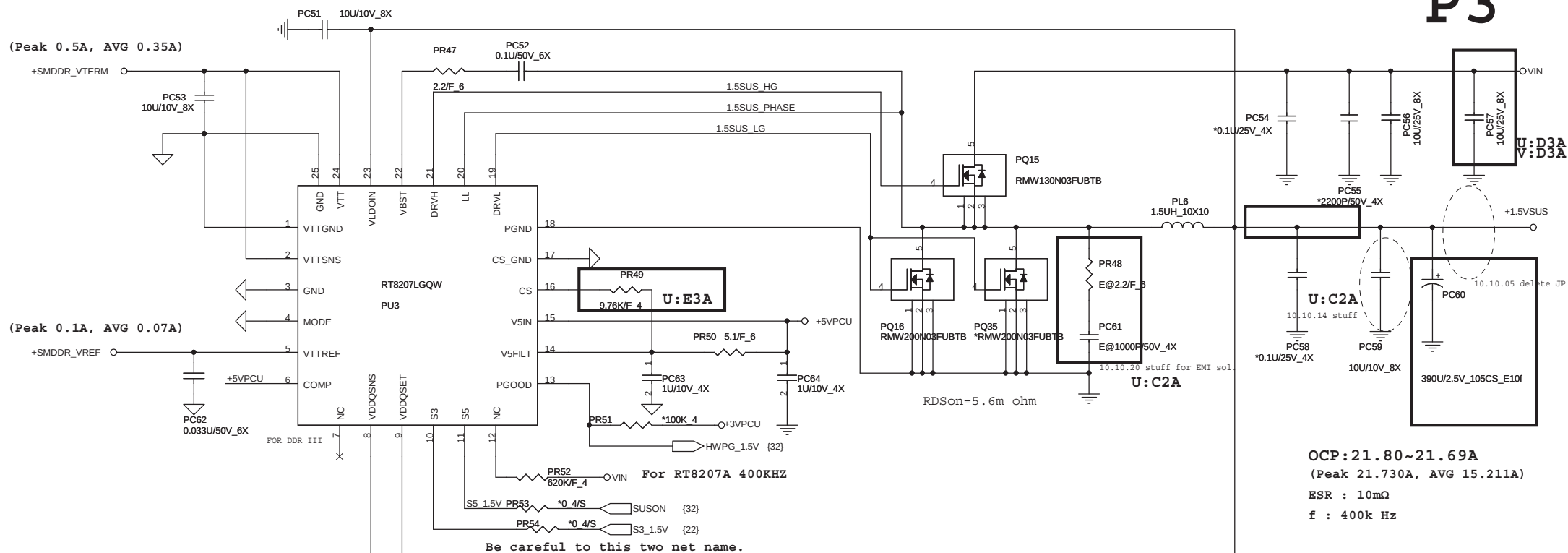


EMI PAD

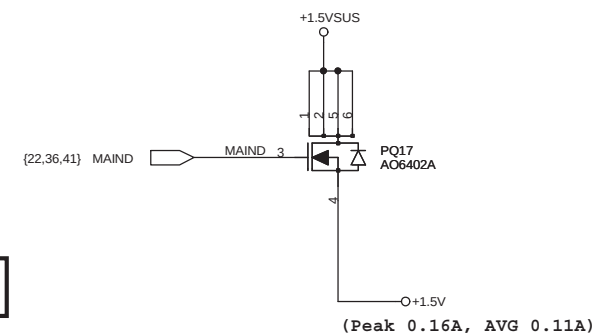
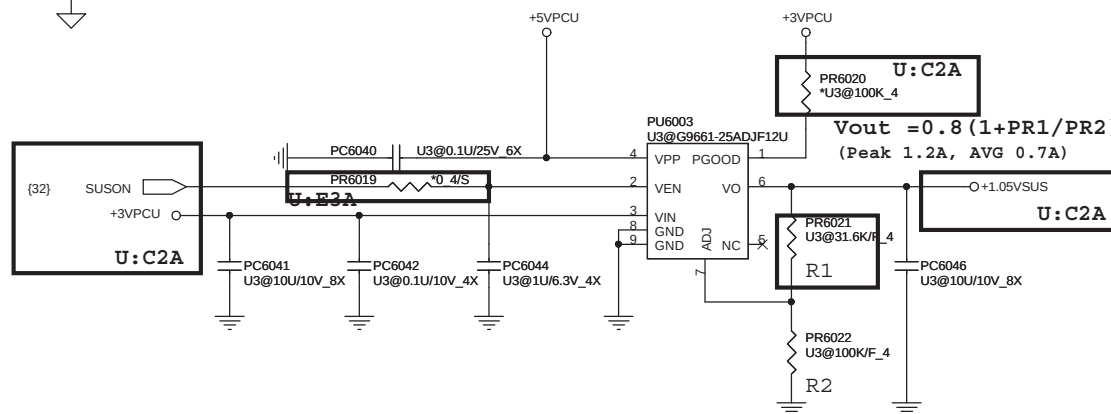
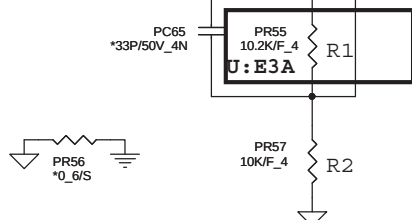


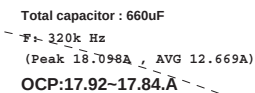




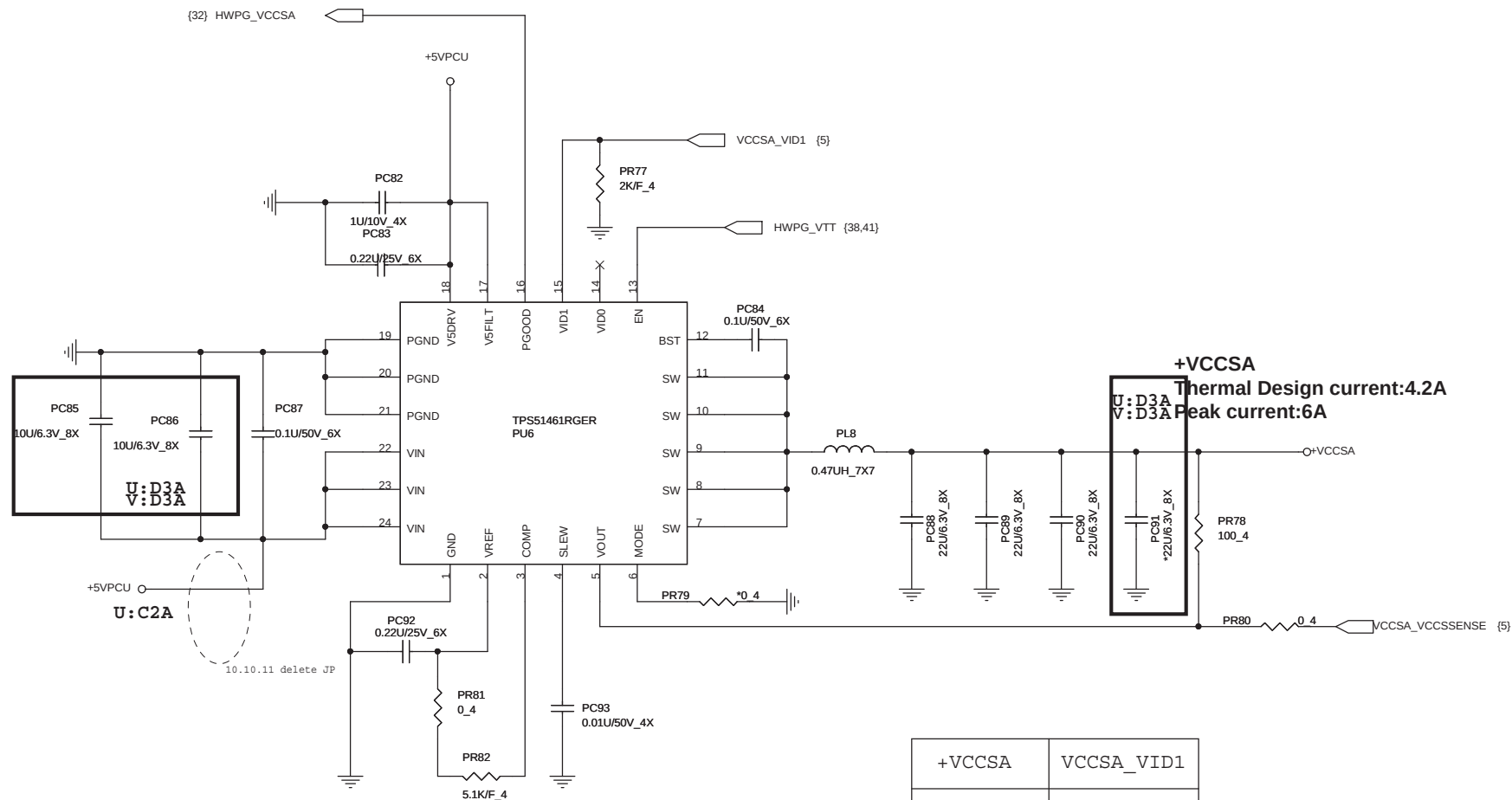


$$V_{out} = (R1/R2) \times 0.75 + 0.75$$





 Quanta Computer Inc. PROJECT : TE5		Rev 1/
Size	Document Number +VTT /+1.05V(RT8238A)	
Date:	Wednesday, January 05, 2011	Sheet 38 of 44

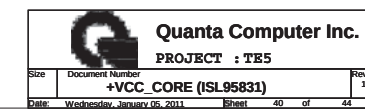


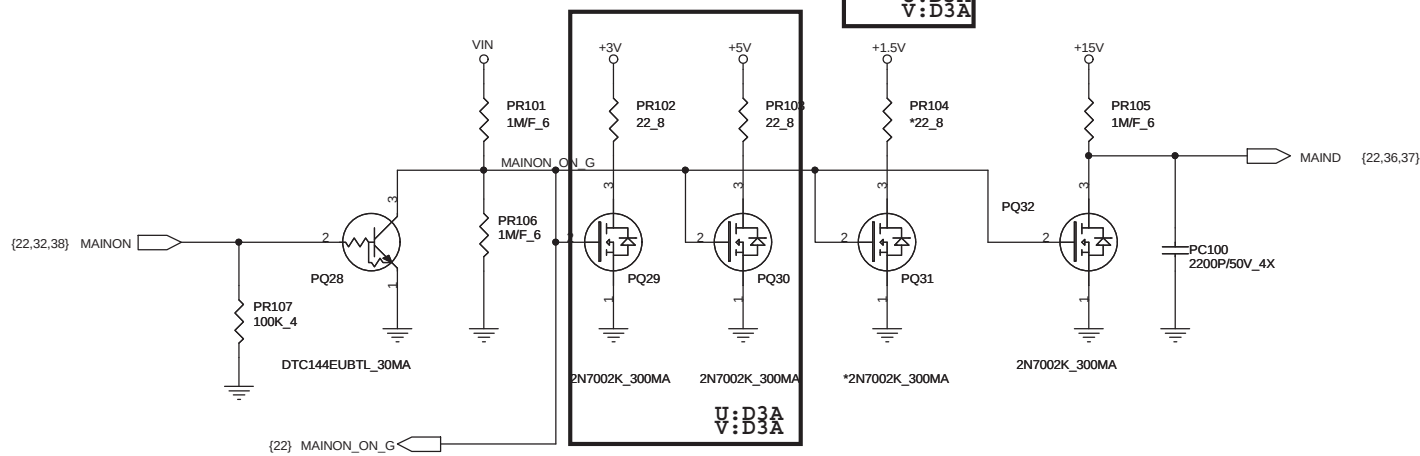
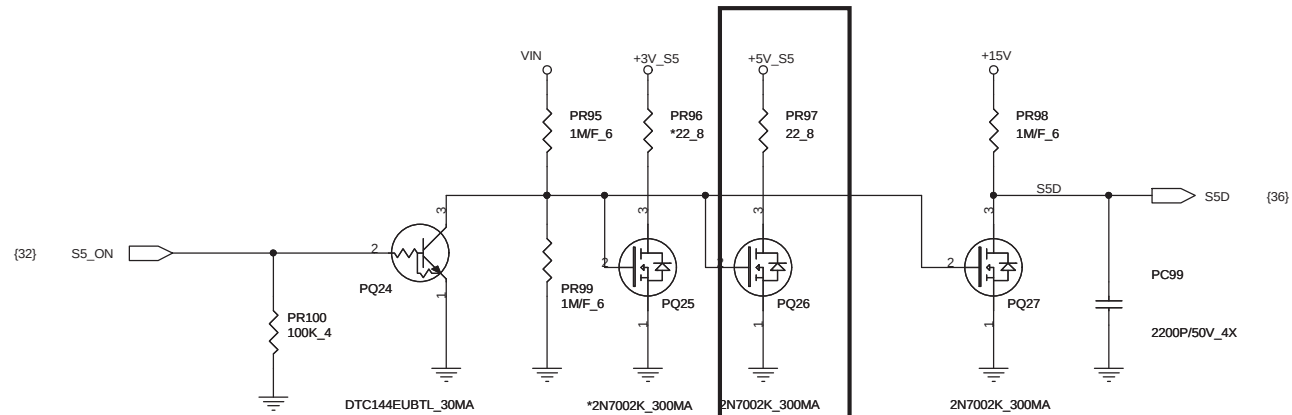
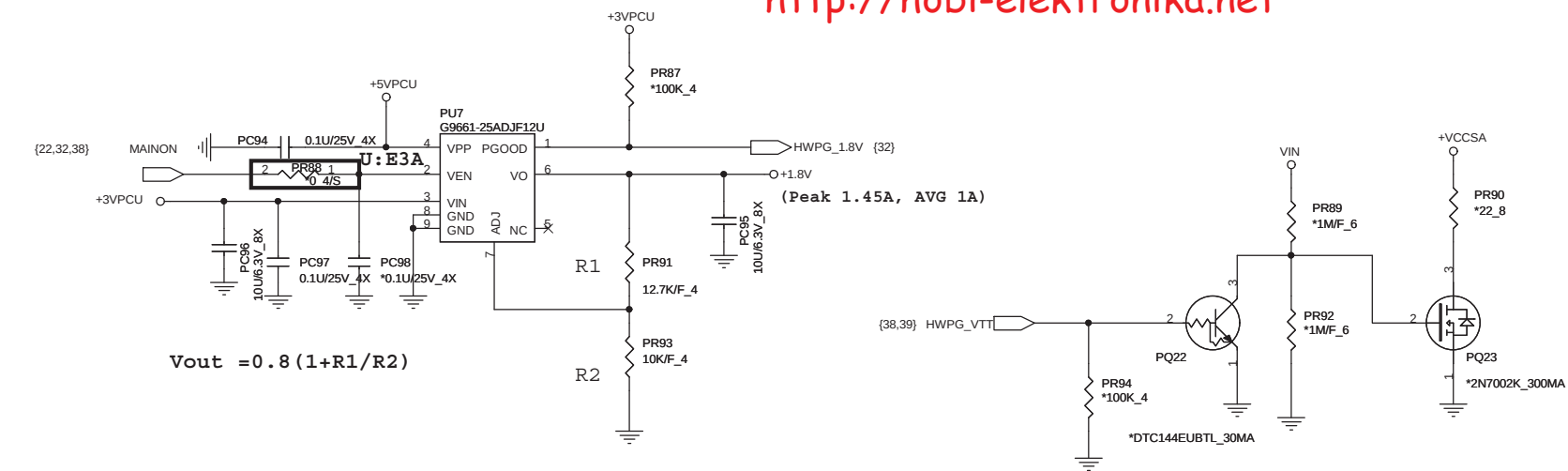
U: C2A



Quanta Computer Inc.

PROJECT : TE5



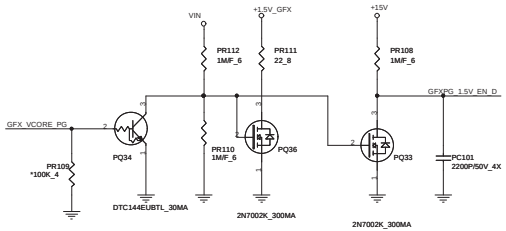
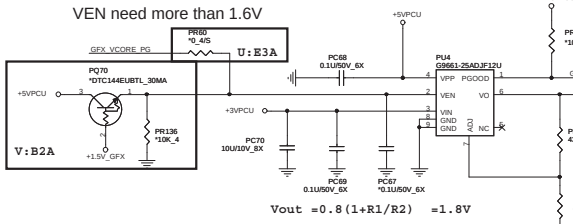


Need to consider DOS mode

Default	N12M-GE	N12P-LP	N12P-GV
PR131 R5 NC	10K	CS31002JB28	10K
PR113 R6 10K	CS31002JB28	NC	NC
PR121 R7 10K	CS31002JB28	NC	10K
PR134 R8 NC	10K	CS31002JB28	NC

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12M-GE	N12P-LP	N12P-GV
LOW	LOW	1.0V	0.925V	1.025V
LOW	HIGH	1.0V	0.90V Default	1.0V
HIGH	LOW	1.0V Default	0.9V	1.0V
HIGH	HIGH	0.85V	0.825V	0.85V Default

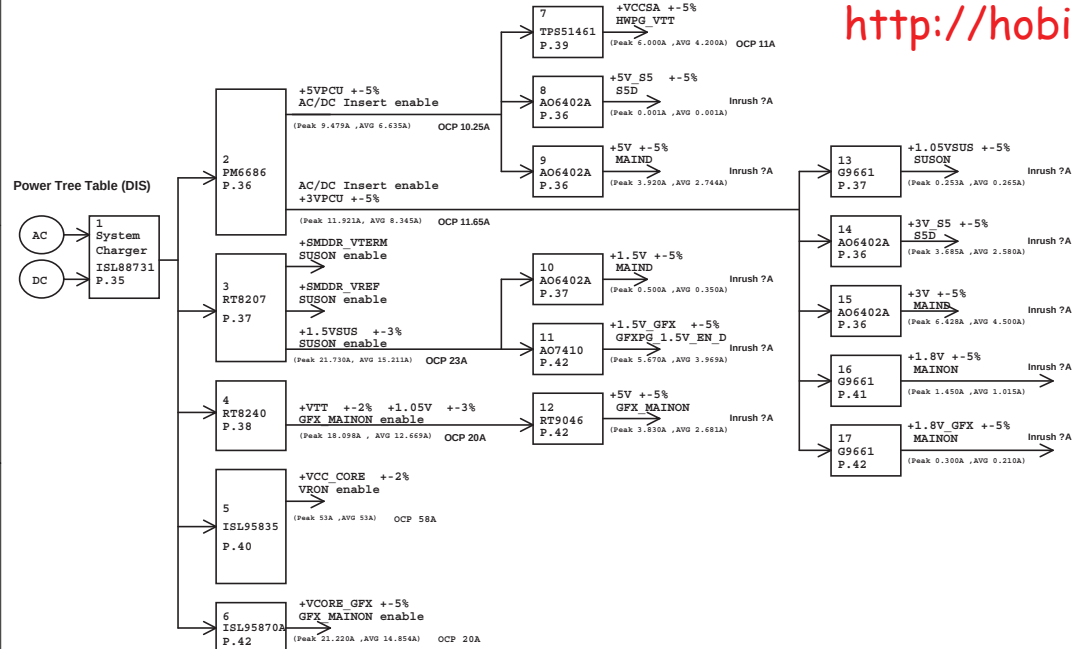
	N12M-GE	N12P-LP	N12P-GV
R1 PR117	47.5K/F_4	CS34752FB14	22.6K/F_4
R2 PR124	0_4	CS00002JB38	0_4
R3 PR119	270K/F_4	CS42702JB10	243K/F_4
R4 PR114	1M/F_4	CS51002FB11	750K/F_4
R5 PR118,PR123	2.32K/F_4	CS22322FB01	2.10K/F_4
R6 PR128,PR129	3.3K/F_4	CS23302FB12	3.24K/F_4



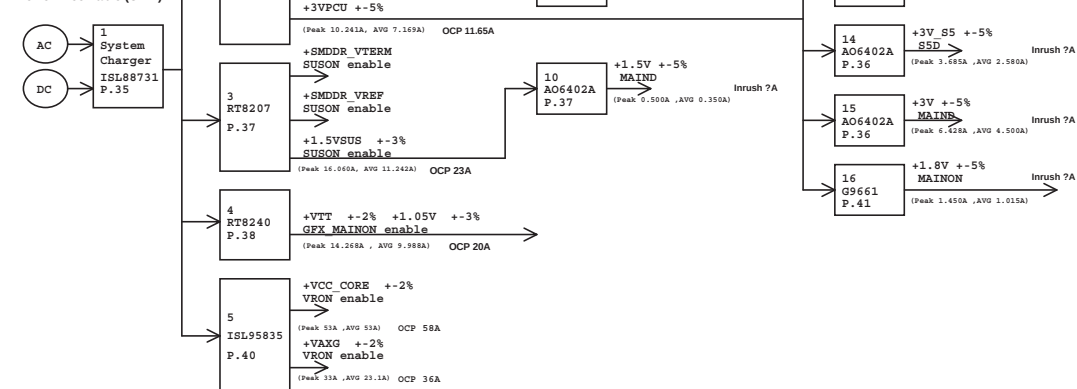
- +3VPCU change to +3V
+5VPCU change to +5V
- Power On Sequence
1. +3V_GFX connect +3V
 2. +1.05V_GFX connect +1.05V
 3. GFX_Mainon Enable +VCORE_GFX
 4. GFX_VCORE_PG Enable(Delay) +1.5V_GFX
 5. +1.5V_GFX Enable +1.8V_GFX
 6. GFX_V18_PG connect GFX_PG
- Power Off Sequence
- compare +VCC3_GFX with +V1.8_GFX

OCP: 25A
(Peak 21A)
Total capacitor: 660 uF
ESR : 4.5mΩ
f : 300k Hz

Power Tree Table (DIS)



Power Tree Table (UMA)



Power Distribution List

Power	Distribution

