

PWA : P835D
PWB : R983D
SCH : M854D

RM2 Paltrow Intel Discrete Block Diagram

VER : 3A

POWER

AC/BATT CONNECTOR	PG 54
BATT CHARGER	PG 47

CLOCK
SLG8SP513V
(QFN-64) PG 17

FAN & THERMAL
EMC1423
(10P TSSOP) PG 39

Penryn
(478 Micro-FCPGA)
PG 3,4

667 / 800 / 1066 MHz FSB

DDR3-SODIMM1
PG 15

800 / 1066 MHZ DDR III

DDR3-SODIMM2
PG 16

800 / 1066 MHZ DDR III

Cantiga
(1299 uFCBGA)
PG 5,6,7,8,9,10

DMI interface

Subwoofer
CONN PG 42

Subwoofer AMP
MAXIM MAX9759
(16 Pin TQFN) PG 42

AUDIO
IDT 92HD73C
(56 LQFP)
9 x 9 mm
PG 40

IHDA

MIC PG 42 & IB

Internal Speaker
PG 37 & DB

Amplifier
TI TPA6040A4
(32 Pin QFN) PG 41

HP2 PG 42 & IB

Amplifier
TI TPA4411MRTJR
(20 Pin QFN) PG 41

HP1 PG 42 & IB

Camera + D-MIC
PG 37

TV CONN PG 35

USB CONN
PG 42 & IB

USB/eSATA Combo
PG 35 & eSATA board

SATA-ODD PG 36

SATA-HDD PG 36

1394 CONN
PG 29 & 1394 board

CardReader
CONN PG 29

PC Card/1394
RICOH R5C833T
(128 Pin TQFP)
14 x 14 mm PG 28,29

Debug Port
(Mini PCI)
PG 56

SIO
ITE ITE8512E
(128 Pin LQFP)
16 x 16 mm PG 31

LPC



RM2 MB PCB (rev F)

SPI ROM
2MB
(8 Pin SO8W) PG 32

Keyboard
PG 37

CIR
PG 32

Touchpad
PG 37 & DB

Media Button
PG 37 & DB

LED
PG 38

RTC
PG 32

SYSTEM POWER

REGULATOR +1.5V_RUN/+1.05V_VCCP PG 48	SYS VR +5V_ALW2/+3.3V_ALW +5V_ALW/+15V_ALW PG 50	VGA Core +VCC_GFX_CORE +1.1V_GFX_PCIE PG 52
DDR3 VR +1.5V_DDR/+0.75V_DDR_VTT +V_DDR_MCH_REF PG 49	CPU VR +VCC_CORE PG 51	REGULATOR +1.8V_SUS PG 53
Load Switch +5V_SUS/+3.3V_SUS/+5V_RUN/+3.3V_RUN/+1.8V_RUN PG 55		

PCIEx16

AMD M86ME-XT
PCI EXPRESS GFX
(880 BGA)
PG 18,19,20,21,22,26

HDMI

HDMI CONN. PG 25

DP

DISPLAYPORT PG 25

LVDS

Panel Connector PG 26

VGA

CRT CONN. PG 27

GDDR3 x 4 (512M)
(136P FBGA)
PG 23,24

GPU THERMAL
ANALOG DEVICES ADM1032
(8 MSOP) 3 x 3 mm PG 22

PCIE [1]

USB2.0 [5]

WWAN MINI-CARD PG 34

PCIE [2]

USB2.0 [4]

WLAN Half MINI-CARD PG 33

PCIE [3]

USB2.0 [6]

UWB/BT MINI-CARD PG 34

PCIE [4]

USB2.0 [7]

Express Card PG 30

PCIE [6]

LAN
Broadcom BCM5784M
(68P QFN) PG 43

Express Switch
RICOH R5538D001
(20 QFN) 4 x 4 mm PG 30

Magnetic
PG 44

RJ45
PG 44

PAD &
SCREW &
SPRING PG 46

System
Reset
Circuit PG 45

To IO Board
(USB*2/ MIC/
HP2/ HP1/ LED) PG 42

To Daughter Board
(Power Button/Speaker/
KB LED/Touch PAD/
Media Button) PG 37



Title BLOCK DIAGRAM		
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30	Express card
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35	USB & eSATA & TV
36	SATA HDD & ODD
37	KB/CCD/UI
38	LED
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40-42	Audio/CONN/Subwoofer (92HD73C).
43-44	LAN/RJ45 (BCM5784M)
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52	VGA_M86 (MAX8632)
53	1.8V_SUS (TPS51117)
54	DCIN & Batt
55	Load Switch
56	Debug Port (Mini PCI)
57	SMBUS BLOCK
58	Power statu
59	Power Block Diagram

<http://hobi-elektronika.net>

Power States

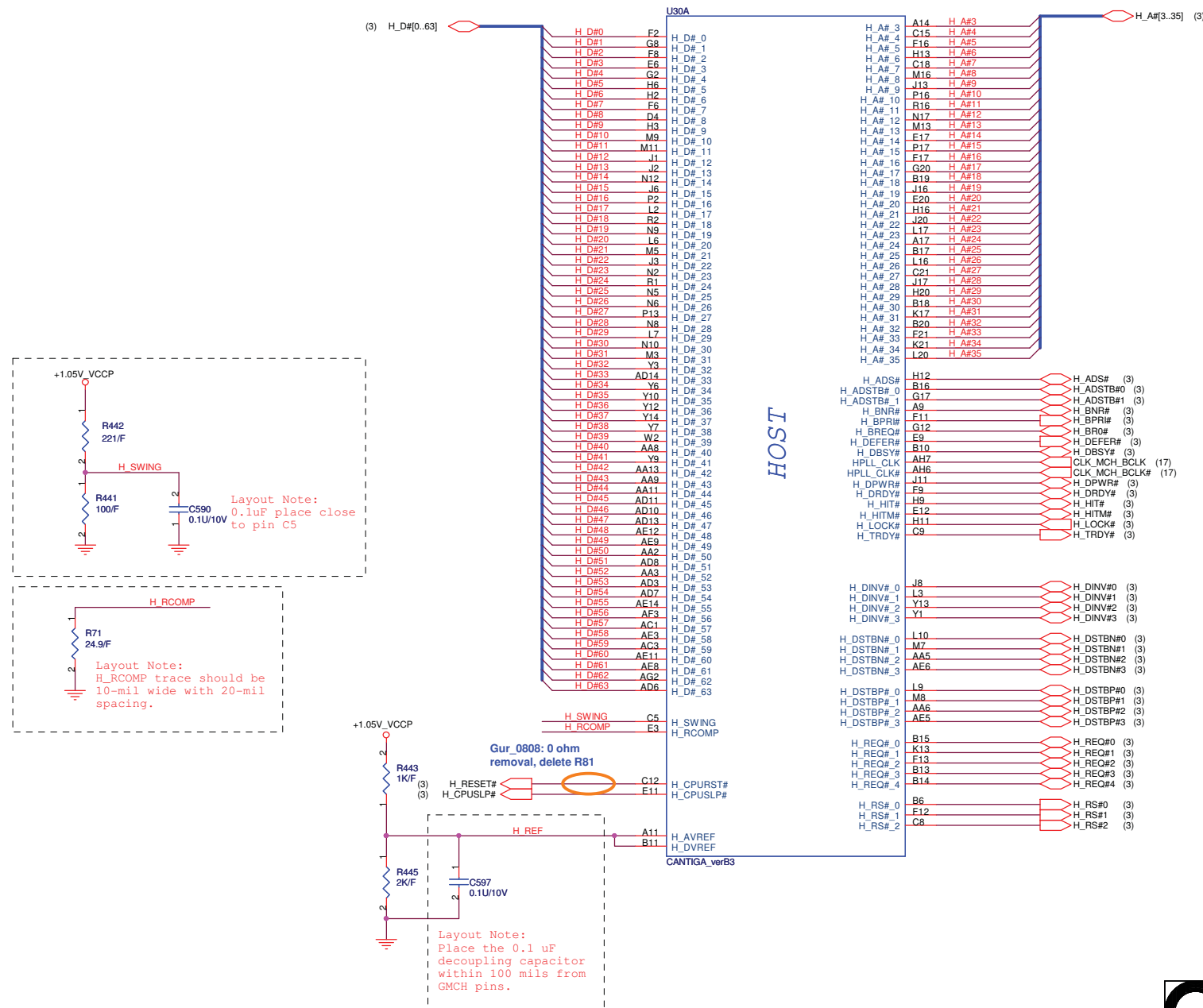
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28,30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38,52,53	LED power source	LDO output	

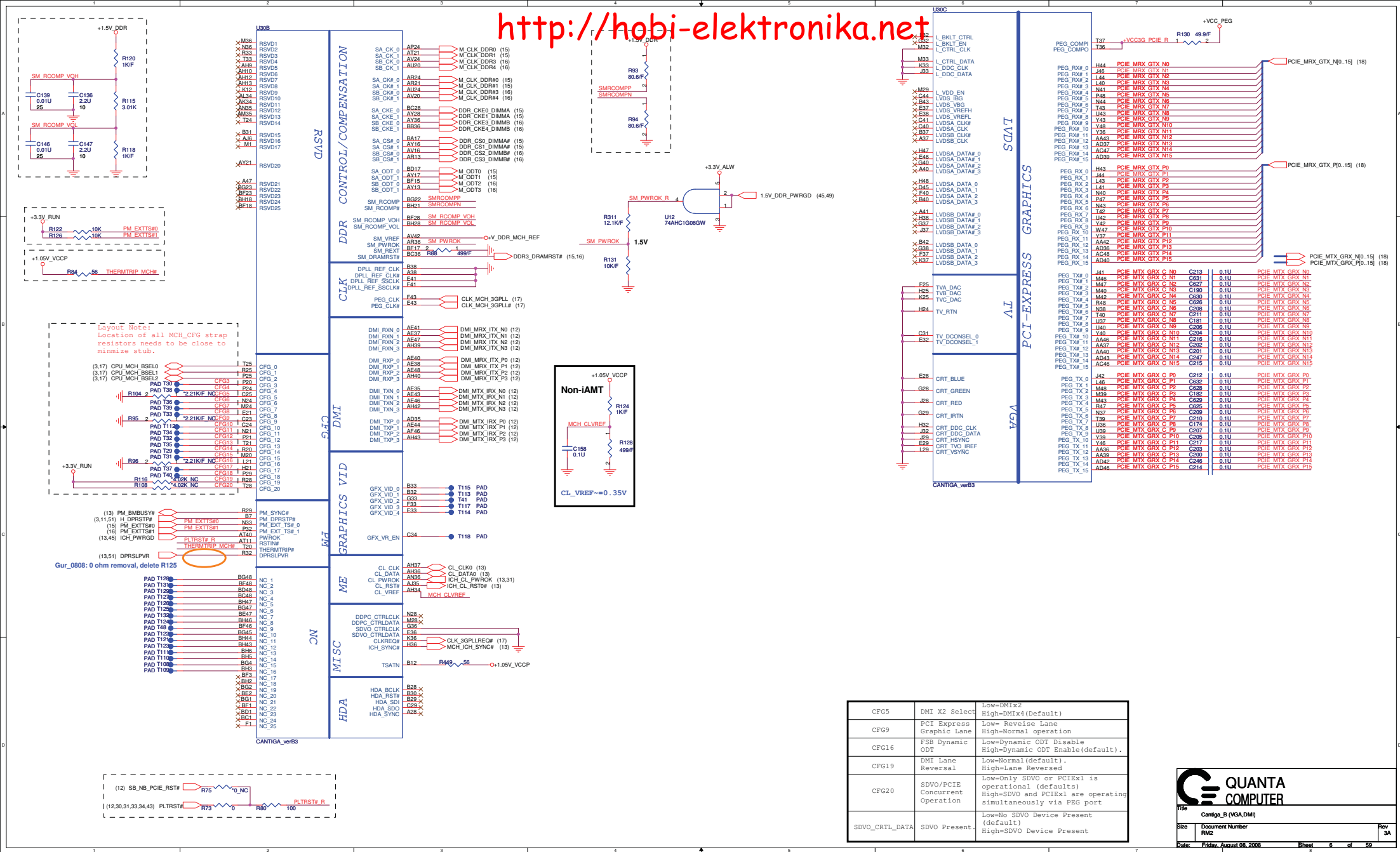
GND PLANE	PAGE	DESCRIPTION
⏏ 8731AGND	46	
⏏ AGND_0.9V	49	
⏏ AGND_DC/DC	52	
⏏ AGND_DC2	48	
⏏ AGND_DDR	49	
⏏ AGND_ISL6260	51	
⏏ GND	ALL	

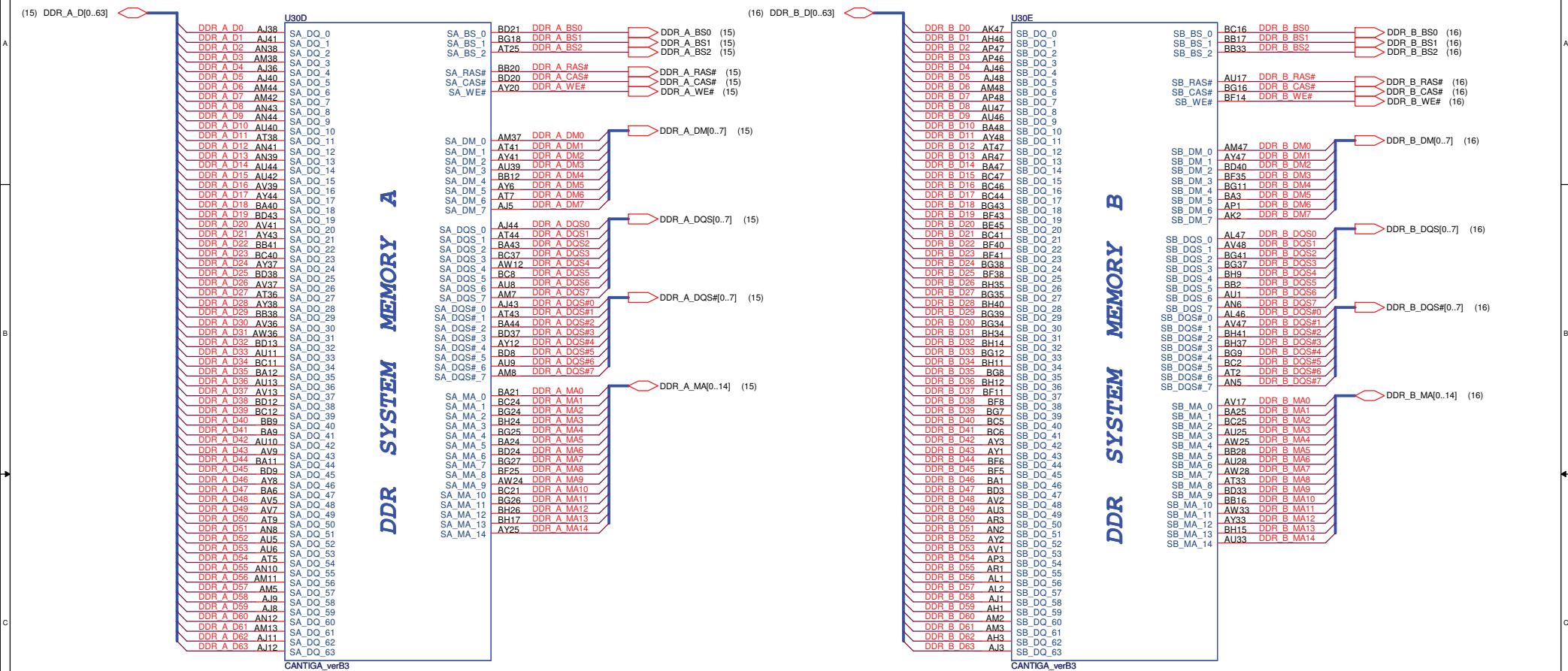
QUANTA
COMPUTER

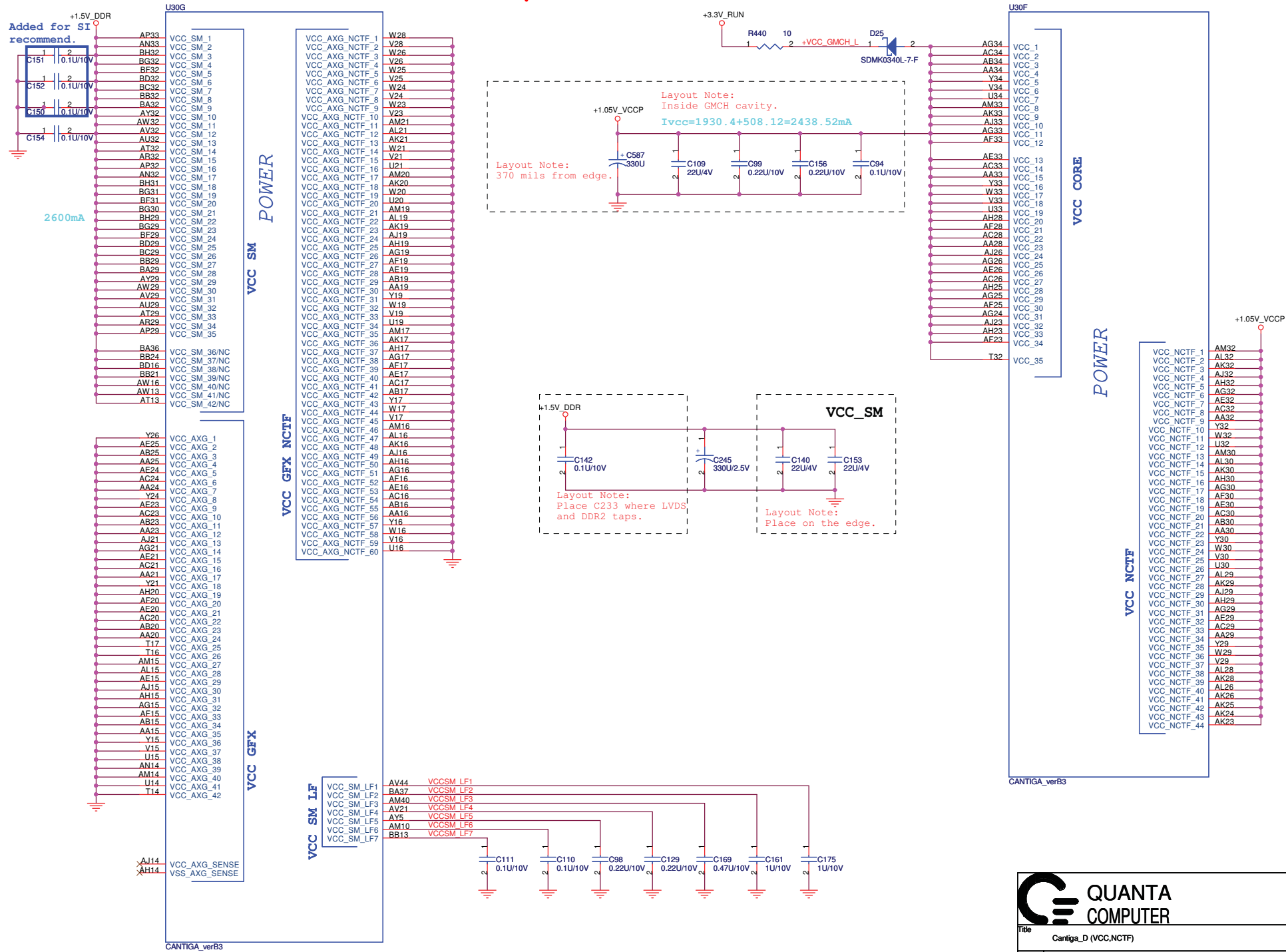
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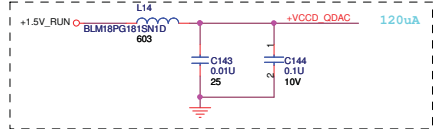
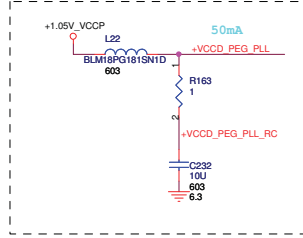
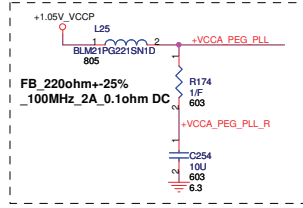
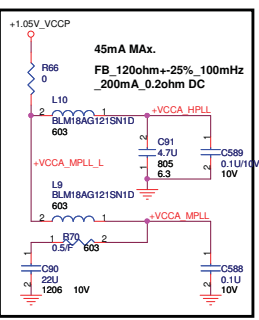




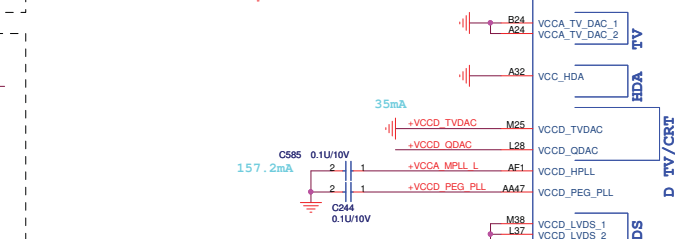
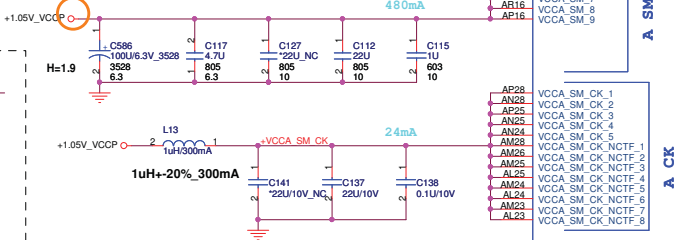








Gur_0808: 0 ohm removal, delete R99



24mA
139.2mA

1.5V_RUN

414uA

50mA

480mA

24mA

1uH+-20%_300mA

157.2mA

414uA

50mA

480mA

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1uH+-20%_300mA

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1uH+-20%_300mA

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1uH+-20%_300mA

157.2mA

414uA

50mA

480mA

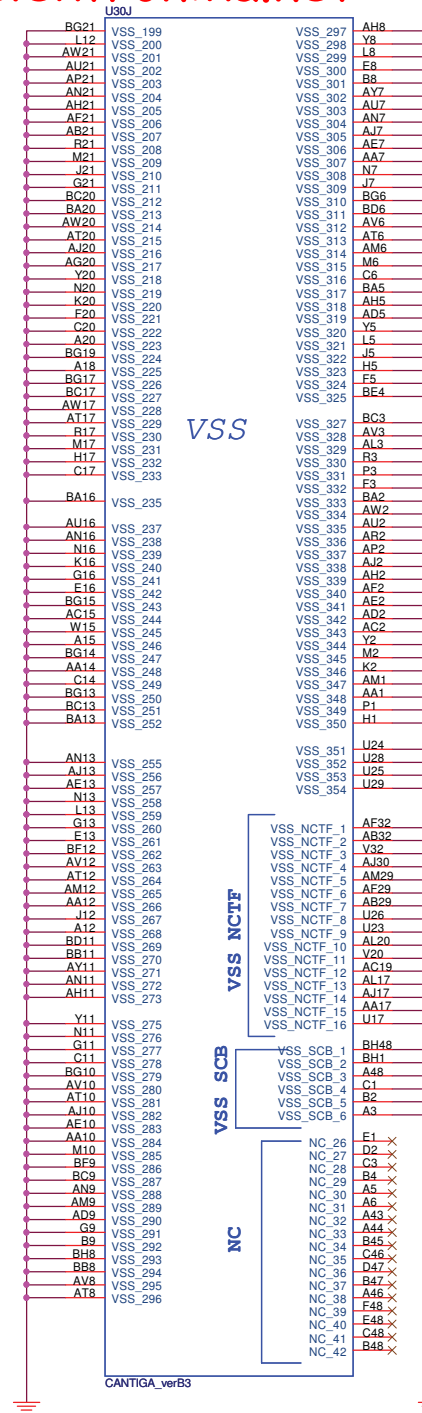
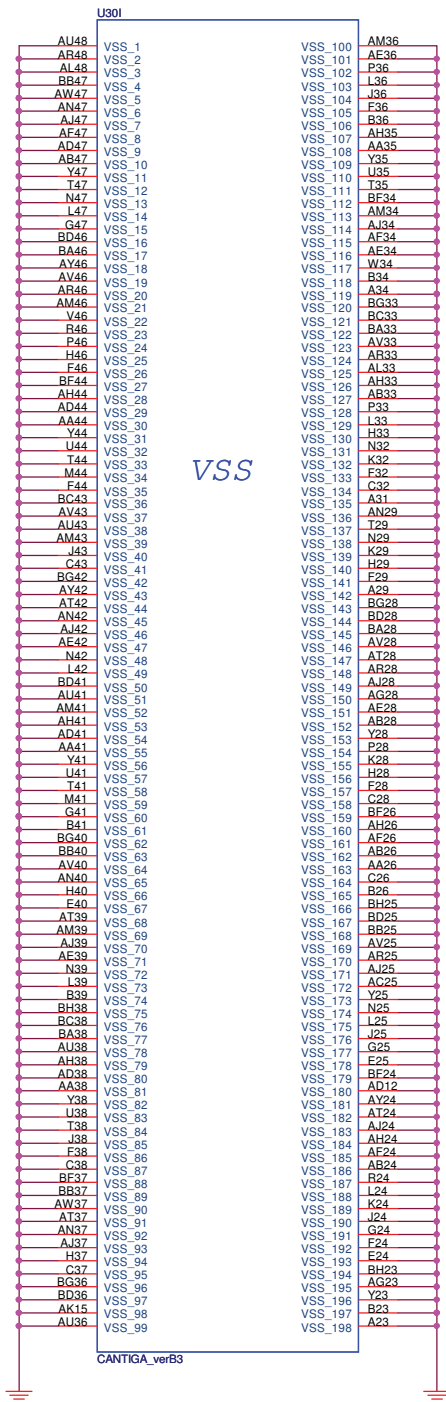
24mA

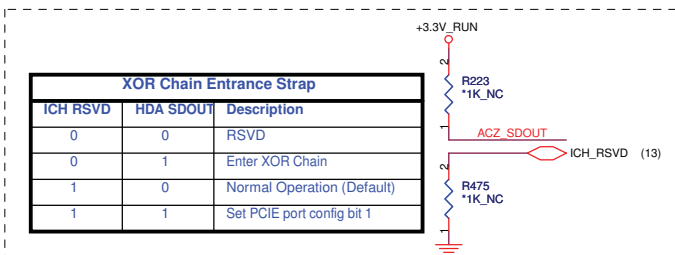
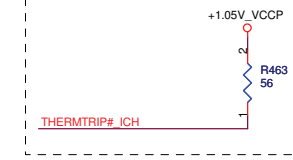
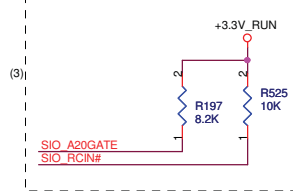
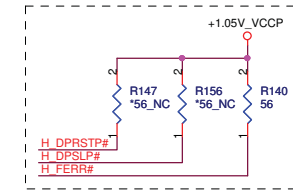
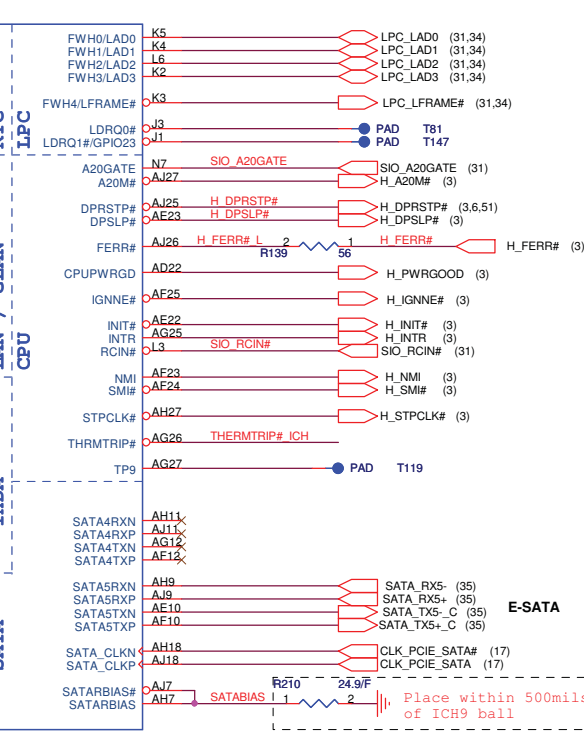
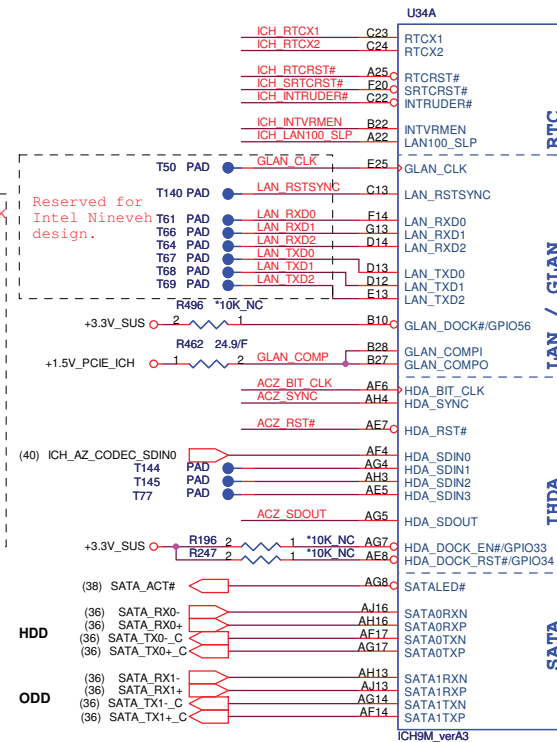
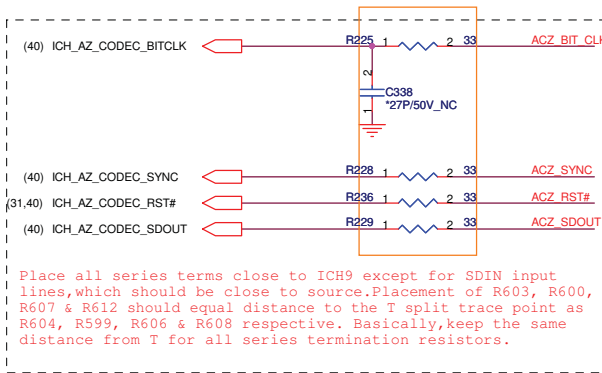
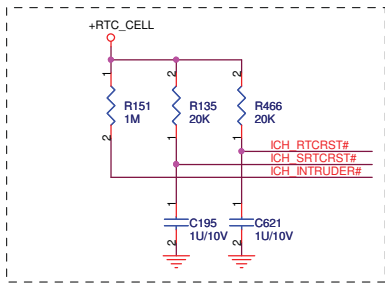
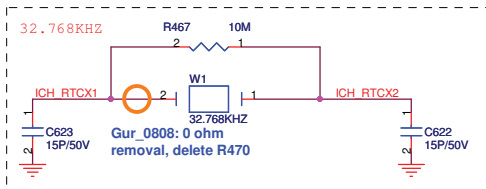
1uH+-20%_300mA

157.2mA

414uA

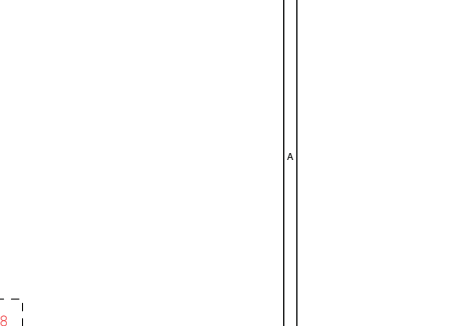
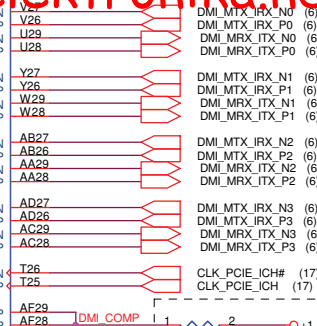
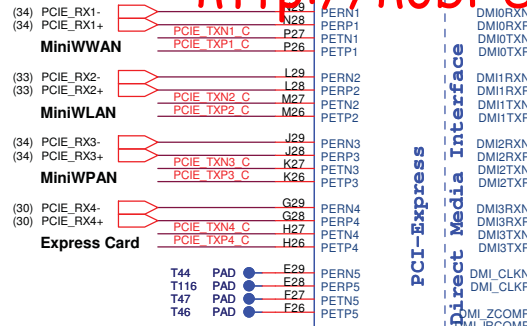
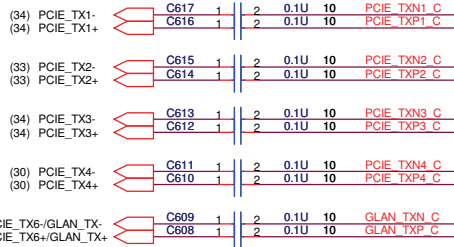
50mA





ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

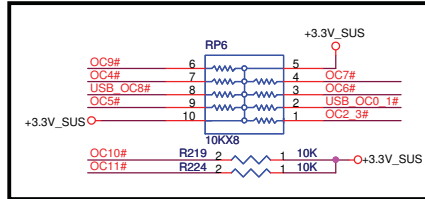
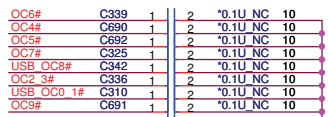
Place TX DC blocking caps close ICH8.

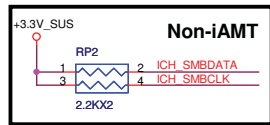


Boot BIOS Strap			
	LPC	GNT0#	SPI_CS1#
PCI	11	No stuff	No stuff
SPI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

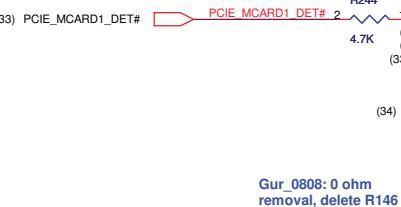
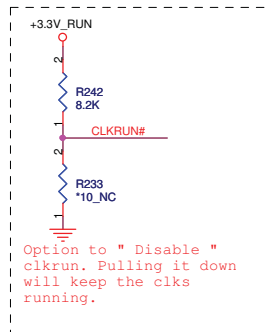
Places within 500 mils of the ICH9

WWAN Noise - ICH improvements

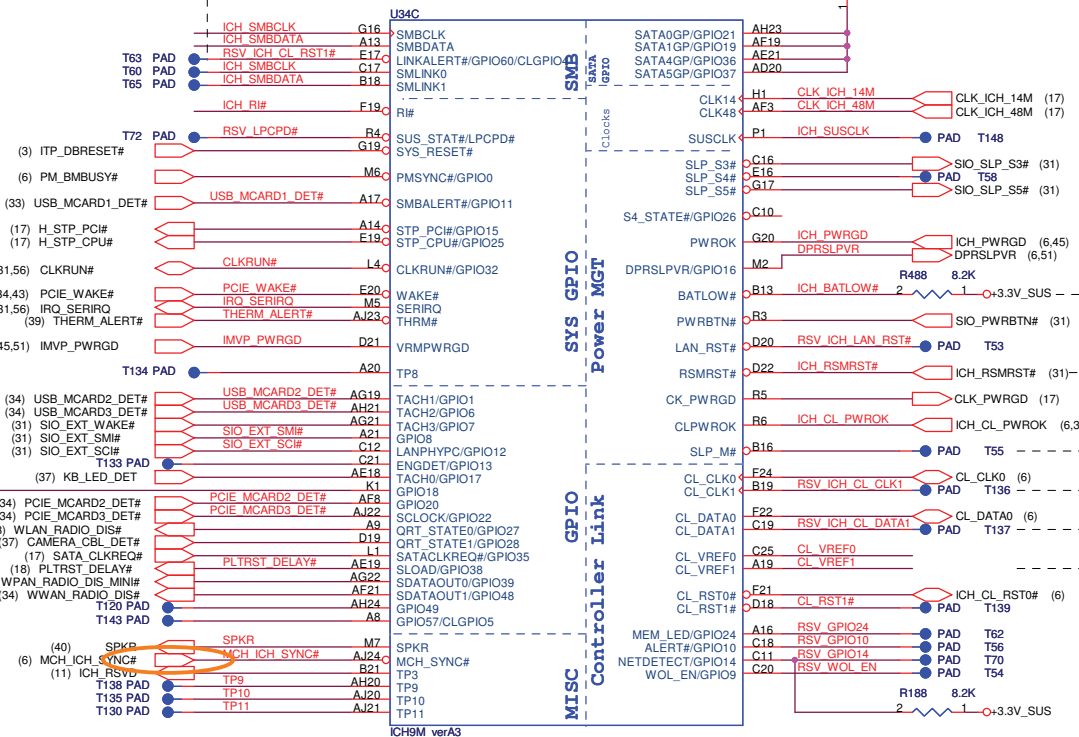
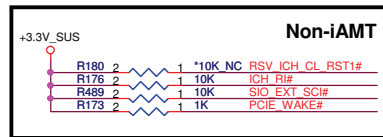
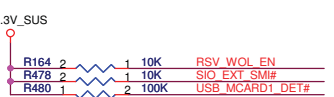
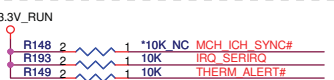
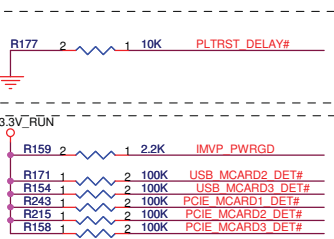


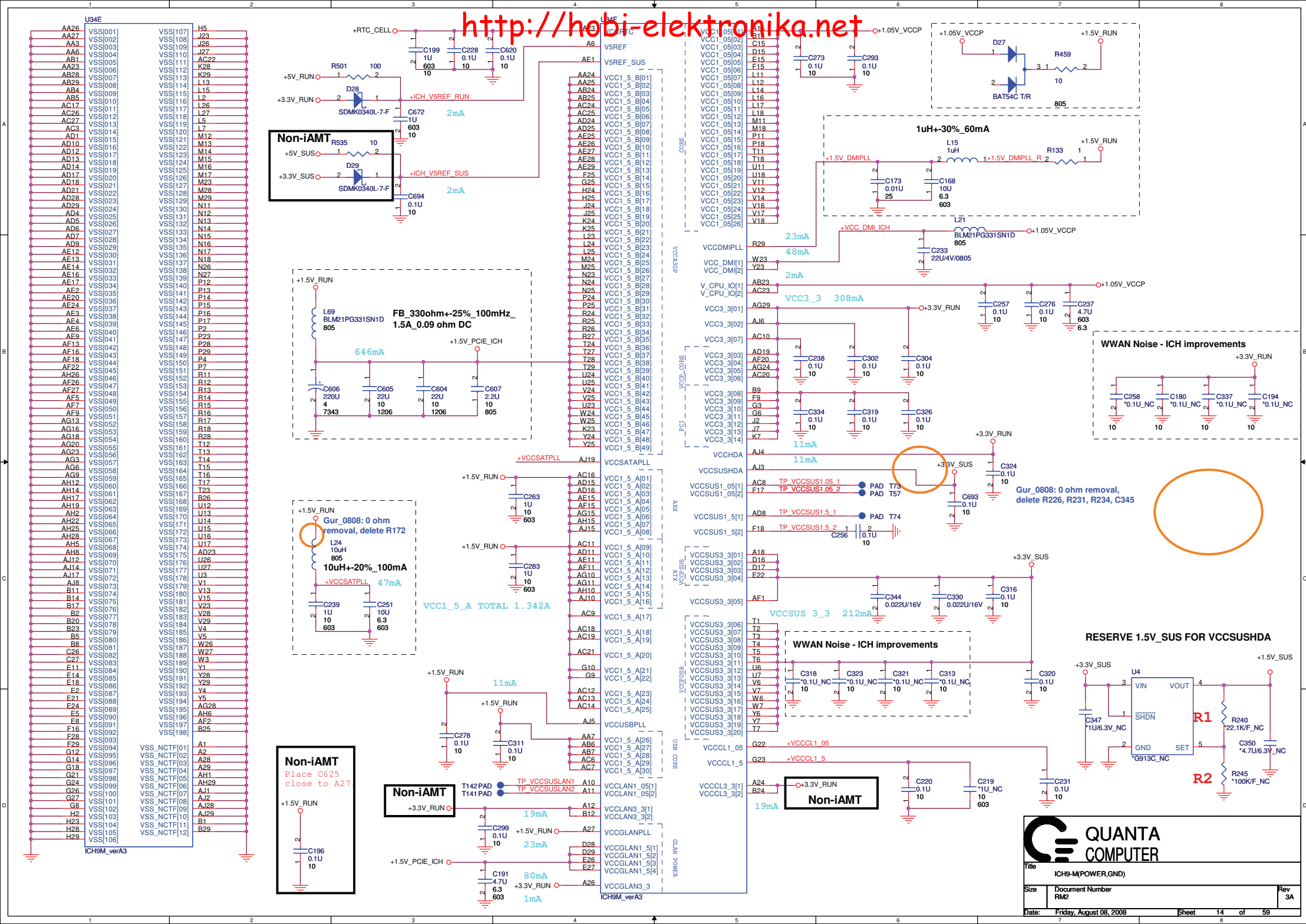


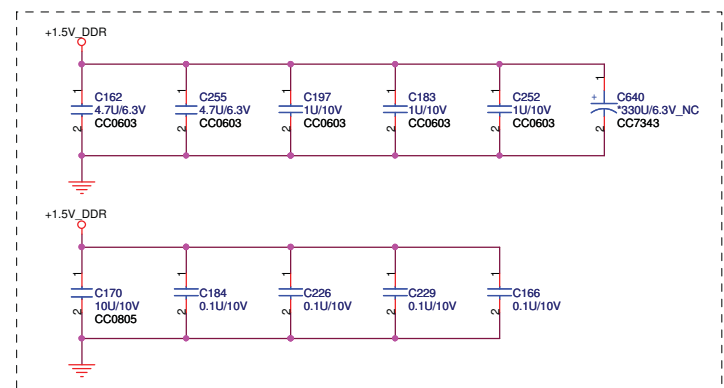
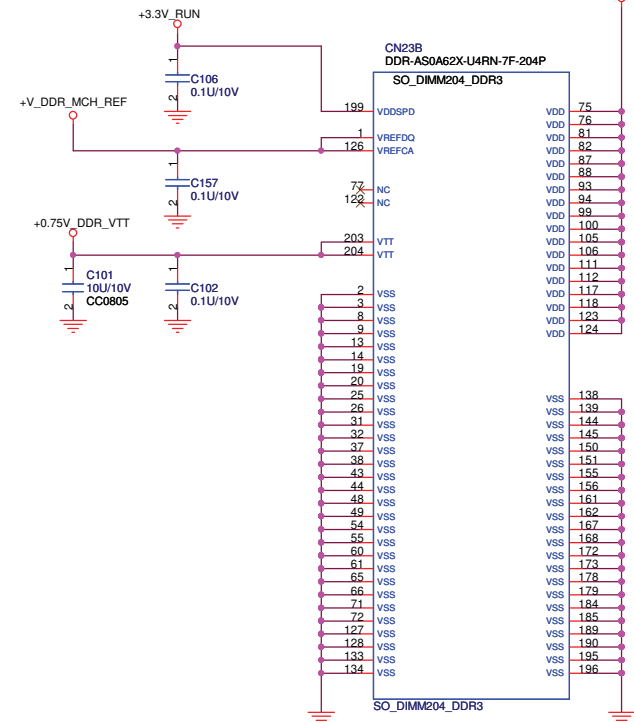
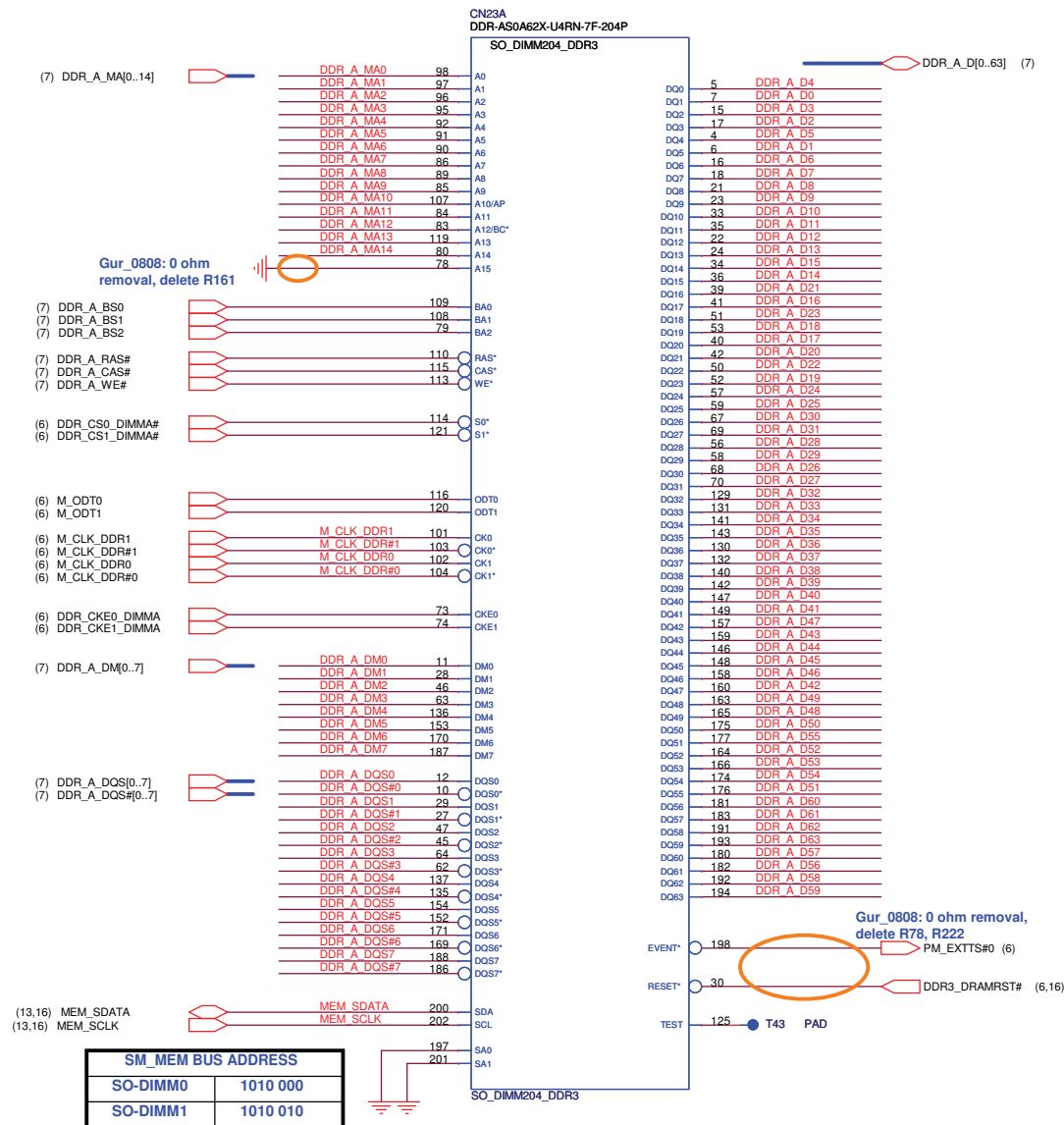
Gur_0808: 0 ohm removal,
delete R178, R186, RP14



Gur_0808: 0 ohm
removal, delete R146



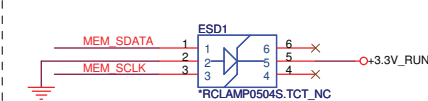


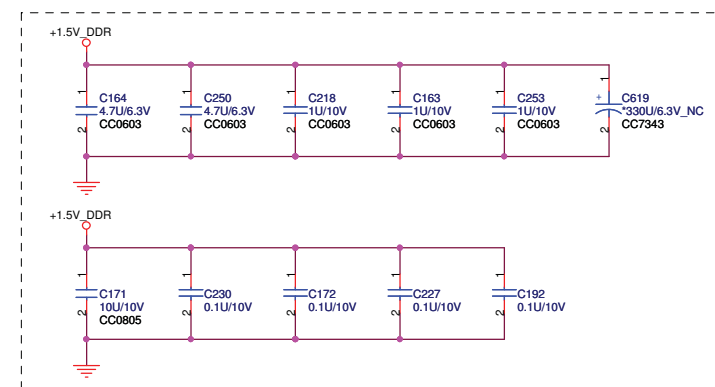
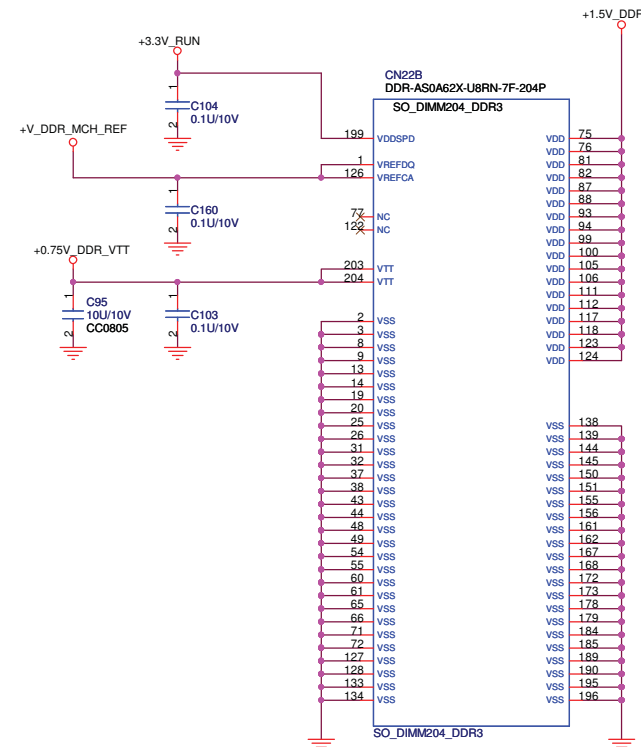


For EMI Reserved



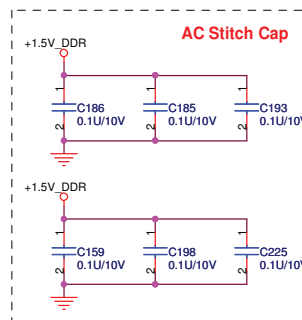
Place ESD Protection diodes.





For EMI Reserved

M CLK DDR4	R138	1	2	*200/F NC	M CLK DDR4
M CLK DDR3	R142	1	2	*200/F NC	M CLK DDR3



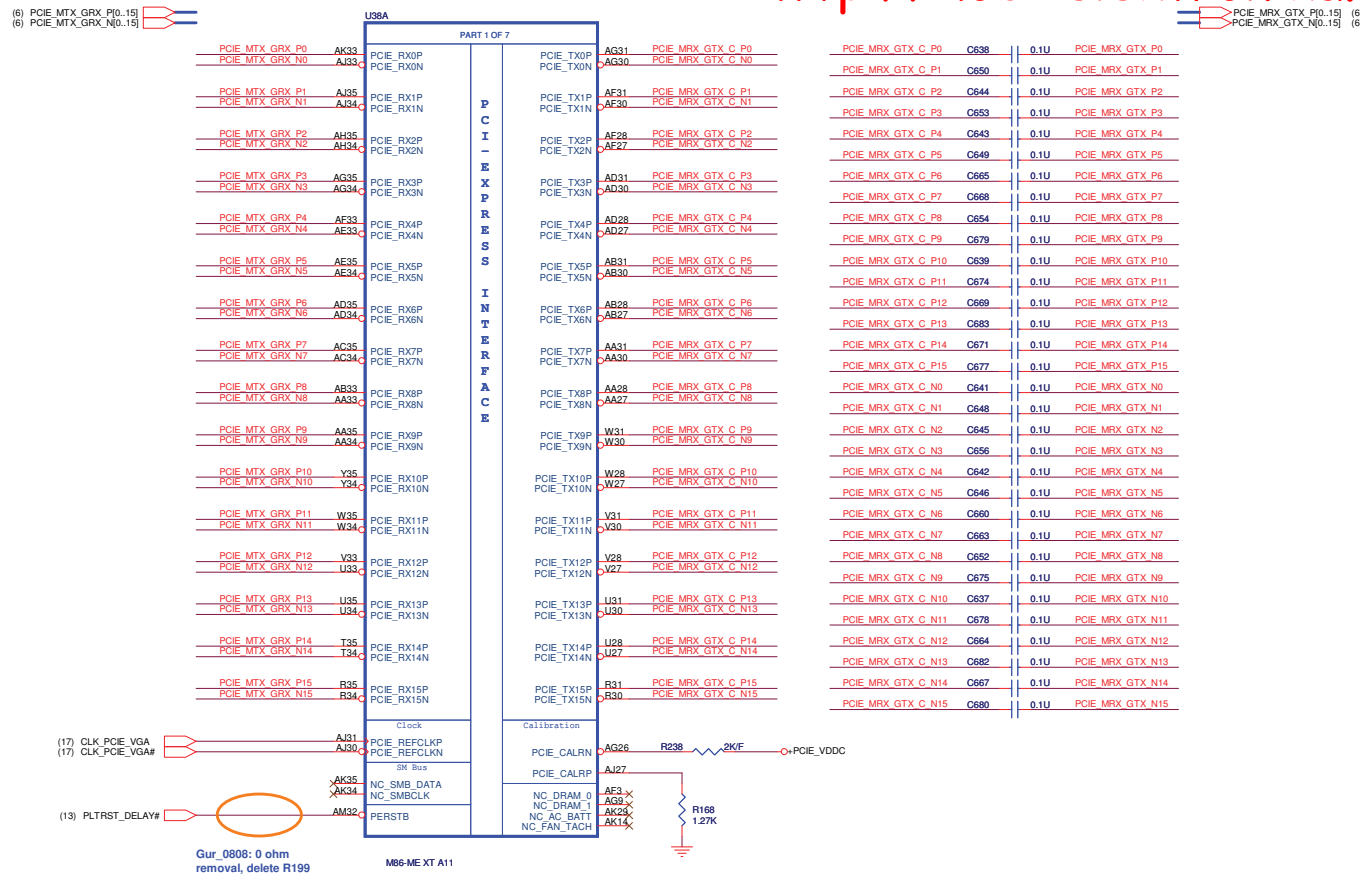
Title	DDR3 SO-DIMM2 (204P)
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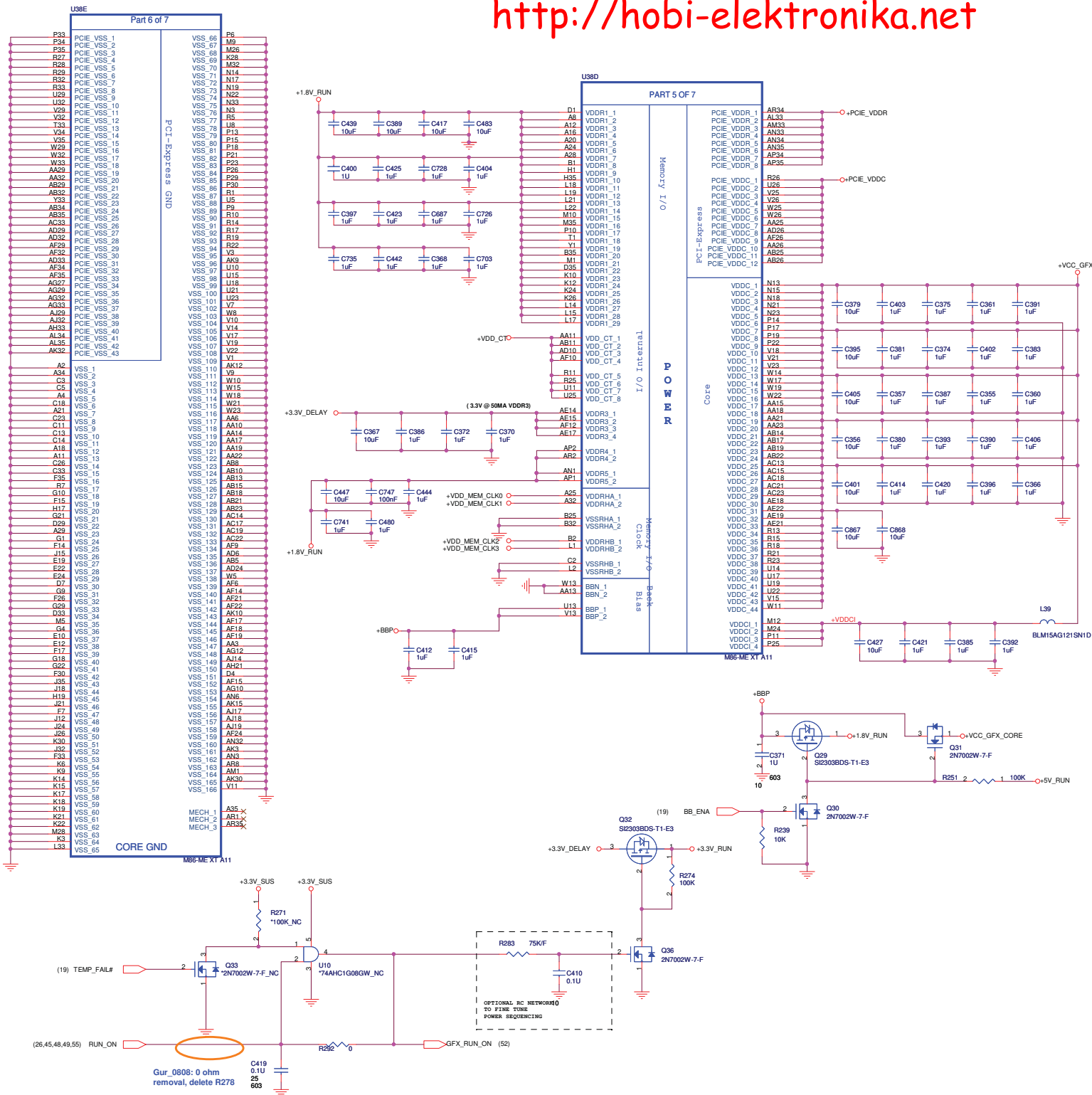
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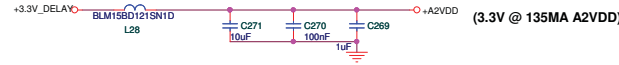
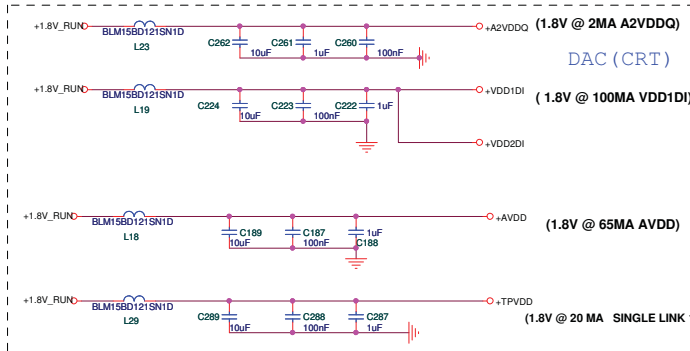
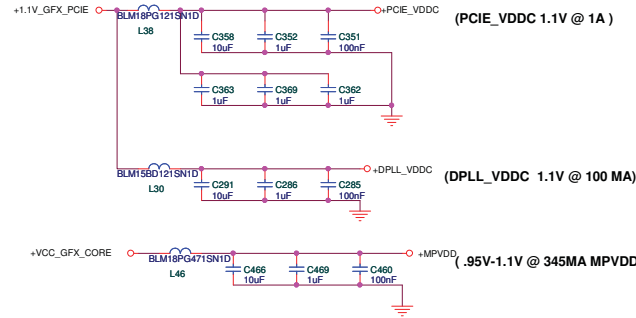
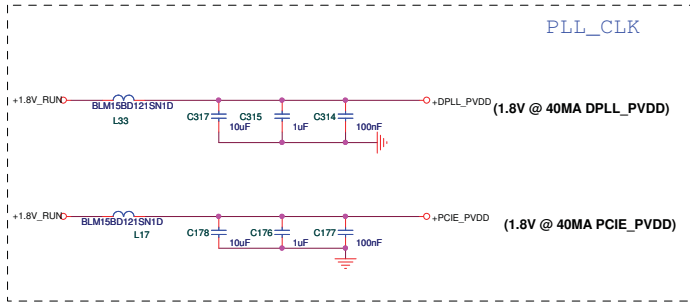
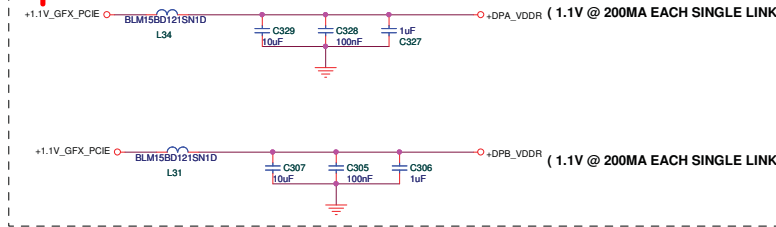
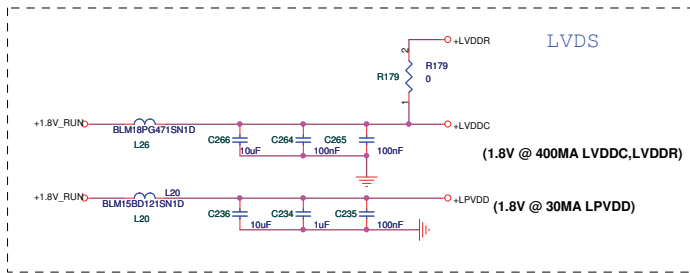
Document Number	BM2
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Date: Thursday, August 14, 2008

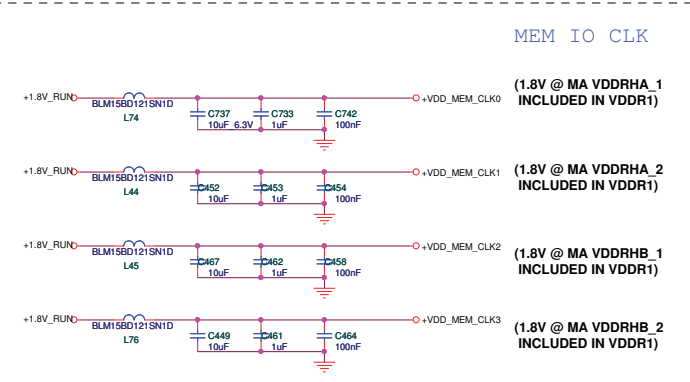
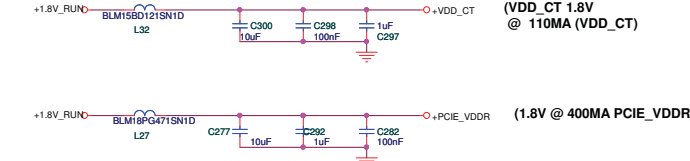
Sheet 16 of 59

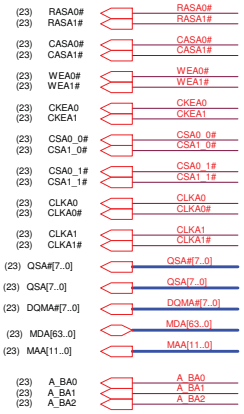


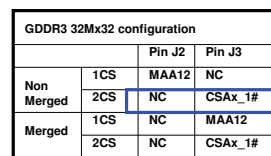


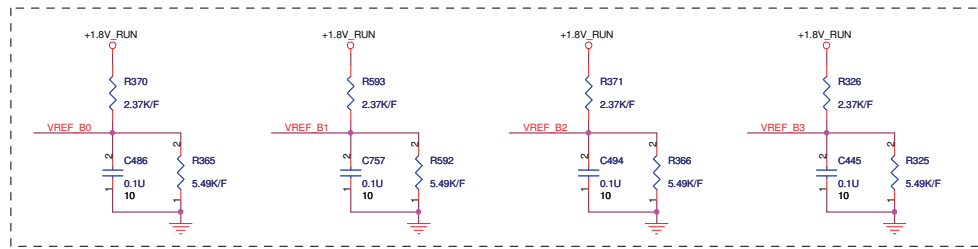
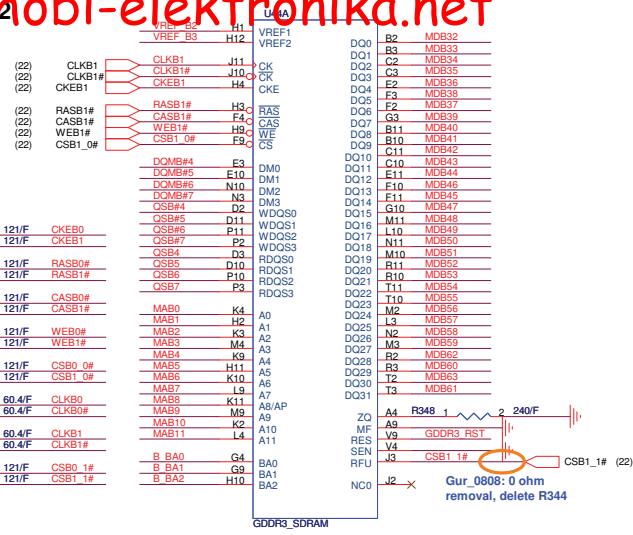
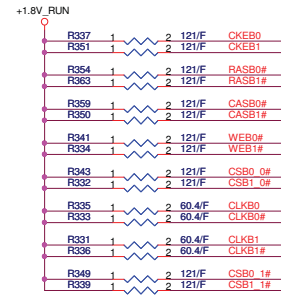
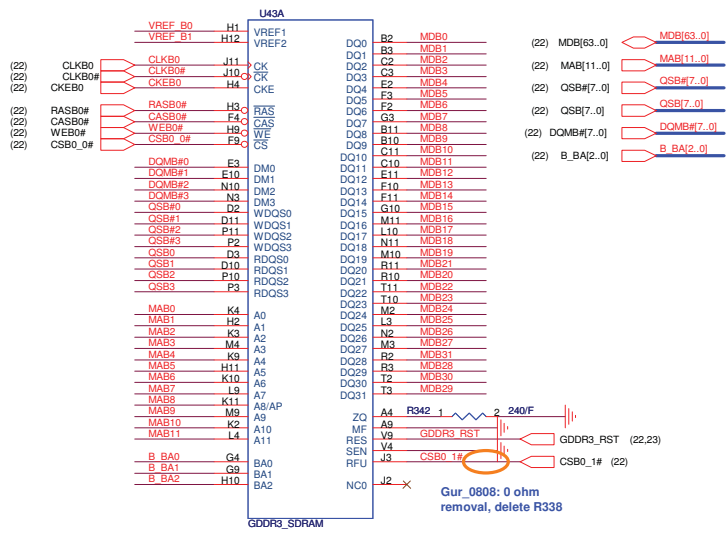


PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

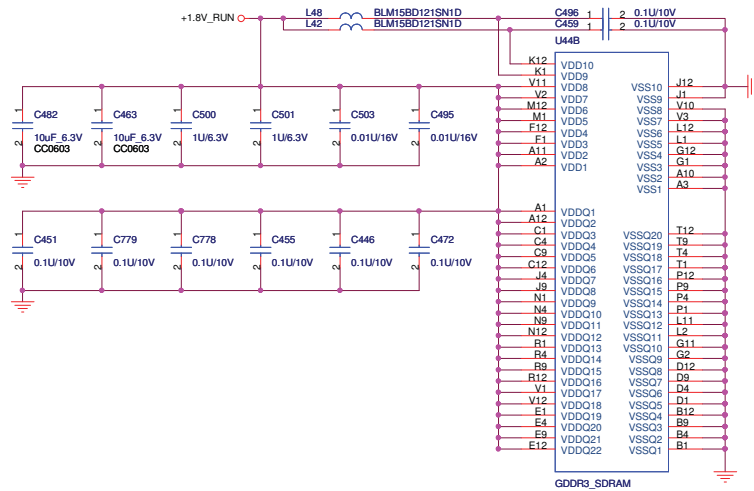
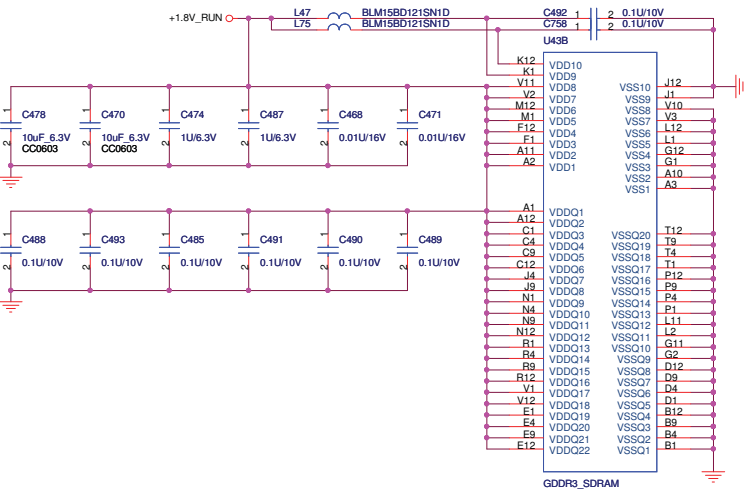


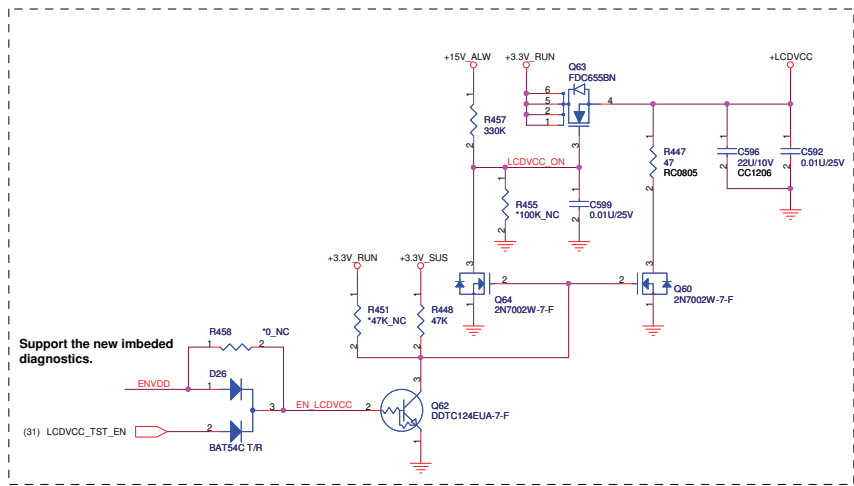
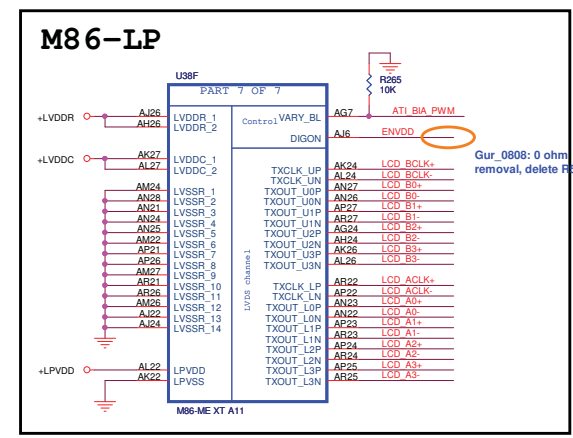
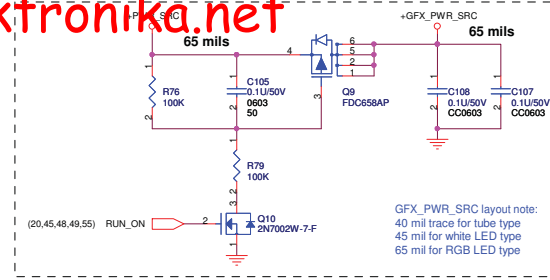
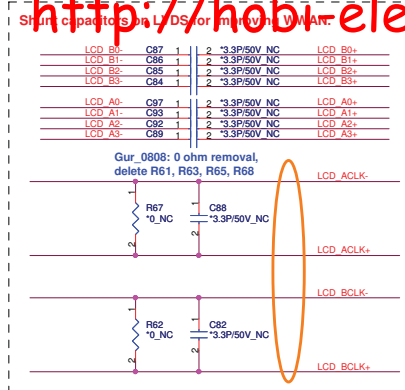
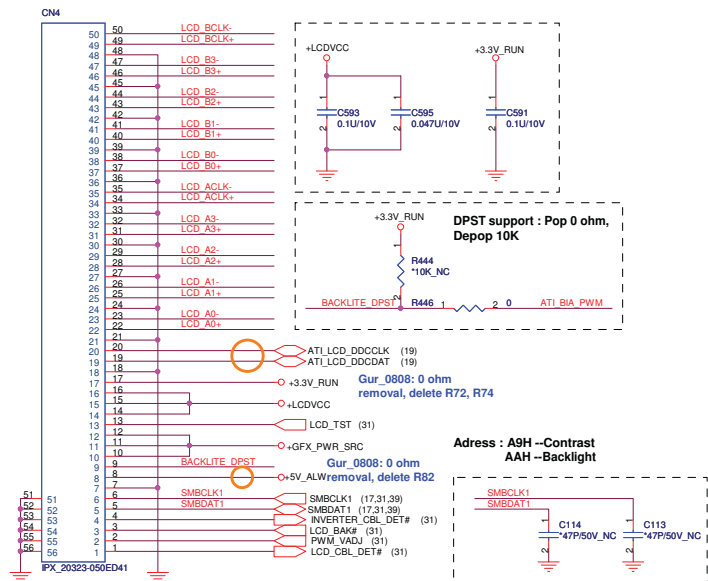


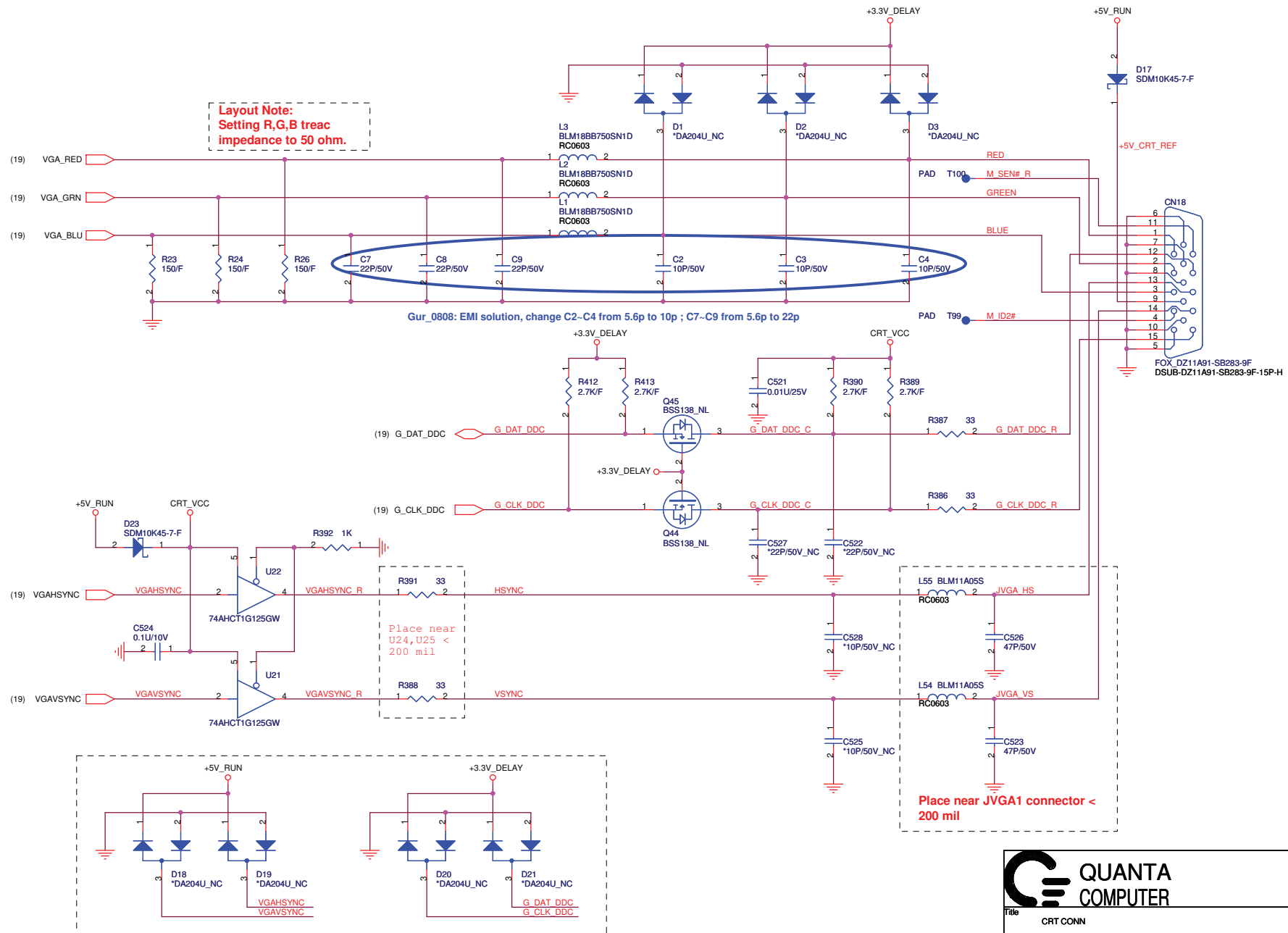




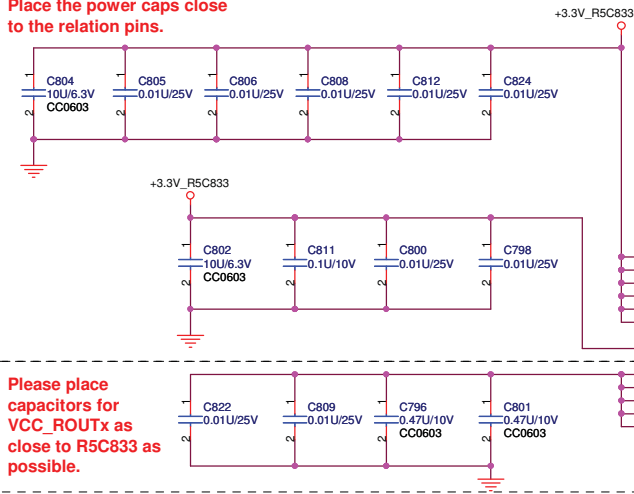
		Pin J2	Pin J3
Non Merged	1CS	MAB12	NC
	2CS	NC	CSBx_1#
Merged	1CS	NC	MAB12
	2CS	NC	CSBx_1#



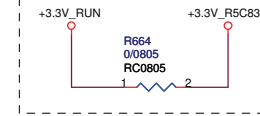




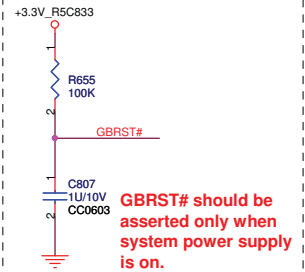
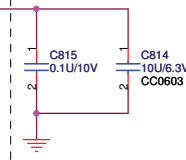
Place the power caps close to the relation pins.



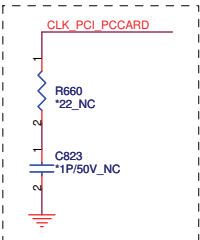
Please place capacitors for VCC_ROUTx as close to R5C833 as possible.



Place the power caps close to the relation pins.



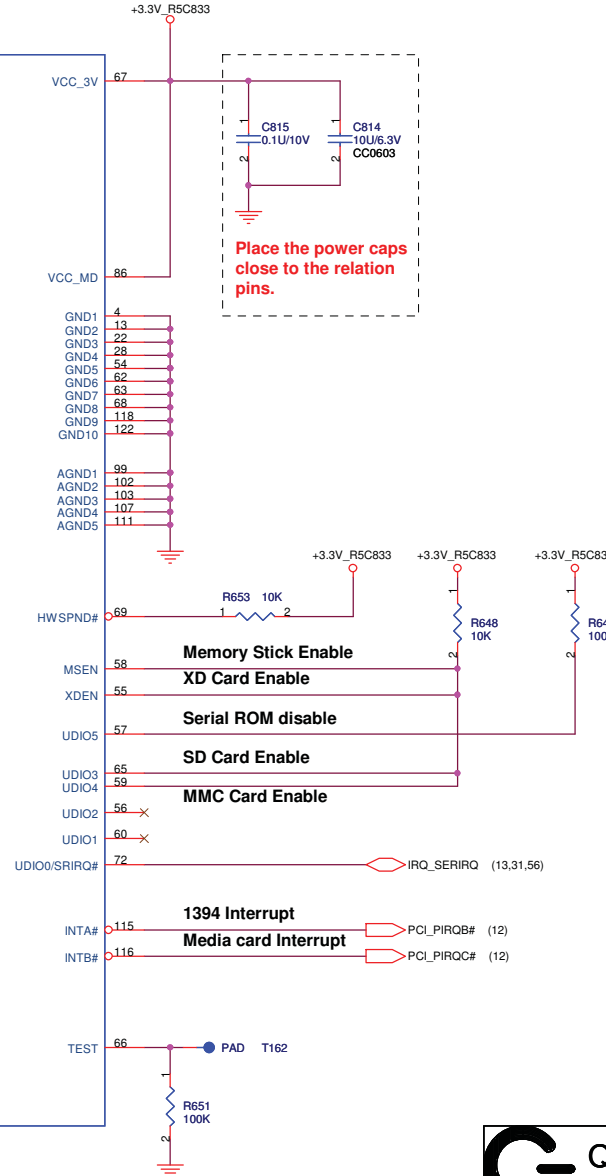
GBRST# should be asserted only when system power supply is on.

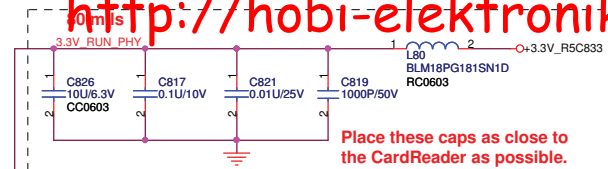
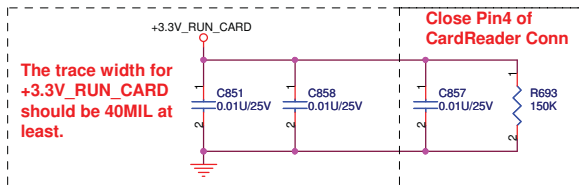
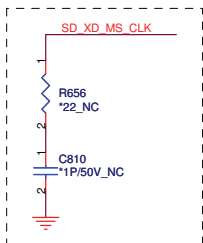
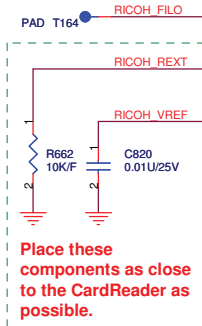
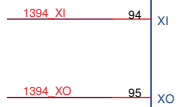
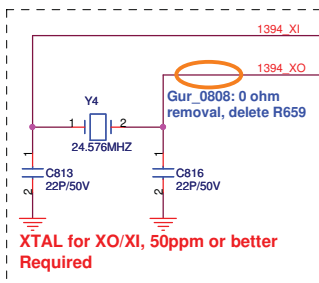


- (12,56) PCI_PAR
- (12,56) PCI_C_BE3#
- (12,56) PCI_C_BE2#
- (12,56) PCI_C_BE1#
- (12,56) PCI_C_BE0#
- (12) PCI_REQ0#
- (12) PCI_GNT0#
- (12,56) PCI_FRAME#
- (12,56) PCI_IRDY#
- (12,56) PCI_TRDY#
- (12,56) PCI_DEVSEL#
- (12,56) PCI_STOP#
- (12,56) PCI_PERR#
- (12,56) PCI_SERR#
- (12,56) PCI_RST#
- (17) CLK_PCCARD
- (12,56) ICH_PME#
- (13,31,56) CLKRUN#

- PCI AD31
- PCI AD30
- PCI AD29
- PCI AD28
- PCI AD27
- PCI AD26
- PCI AD25
- PCI AD24
- PCI AD23
- PCI AD22
- PCI AD21
- PCI AD20
- PCI AD19
- PCI AD18
- PCI AD17
- PCI AD16
- PCI AD15
- PCI AD14
- PCI AD13
- PCI AD12
- PCI AD11
- PCI AD10
- PCI AD9
- PCI AD8
- PCI AD7
- PCI AD6
- PCI AD5
- PCI AD4
- PCI AD3
- PCI AD2
- PCI AD1
- PCI AD0
- PAR
- C/BE3#
- C/BE2#
- C/BE1#
- C/BE0#
- IDSEL
- REQ#
- GNT#
- FRAME#
- IRDY#
- TRDY#
- DEVSEL#
- STOP#
- PERR#
- SERR#
- GBRST#
- GBRST#
- PCIRST#
- PCICLK
- PME#
- CLKRUN#

PCI / OTHER



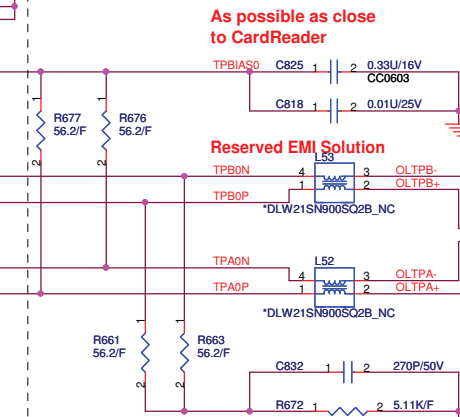


AVCC_PHY1
AVCC_PHY2
AVCC_PHY3
AVCC_PHY4

TPBIAS0
TPB0N
TPBP0
TPAN0
TPAP0

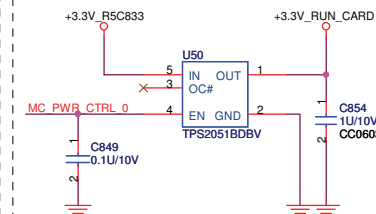
IEEE1394/SD

MDIO17 87 XD_MMS_DATA7
MDIO16 92 XD_MMS_DATA6
MDIO15 89 XD_MMS_DATA5
MDIO14 91 XD_MMS_DATA4
MDIO13 90 SD_XD_MS_DATA3
MDIO12 93 SD_XD_MS_DATA2
MDIO11 81 SD_XD_MS_DATA1
MDIO10 82 SD_XD_MS_DATA0
MDIO05 75 SD_WP#
MDIO08 88 SD_XD_MS_CMD
MDIO19 83 XD_ALE
MDIO18 85 XD_CLE
MDIO02 78 XD_CE#
MDIO03 77 SD_WP#_XDR_B#
MDIO00 80 SD_CD#
MDIO01 79 MS_INS#
MDIO09 84 SD_XD_MS_CLK
MDIO04 76 MC_PWR_CTRL_0
MDIO06 74 T163PAD
MDIO07 73

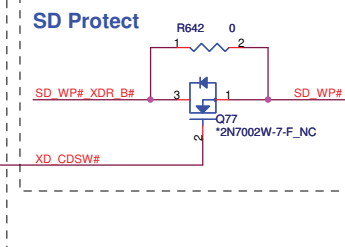
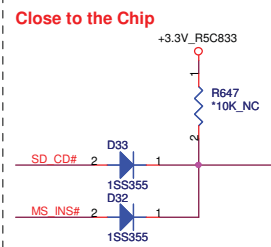
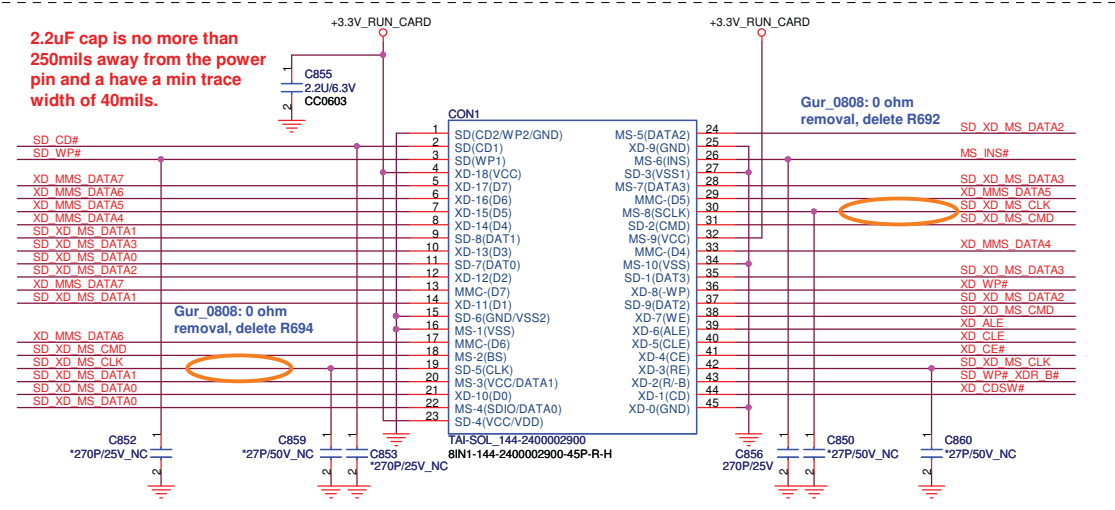


1. TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
2. TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
3. Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

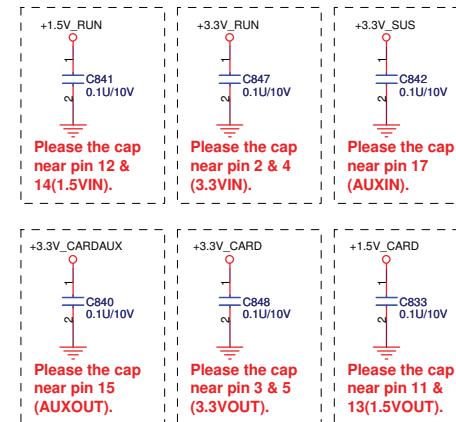
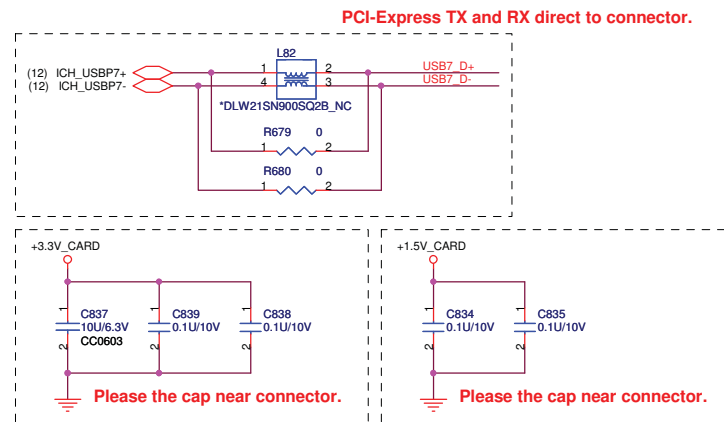
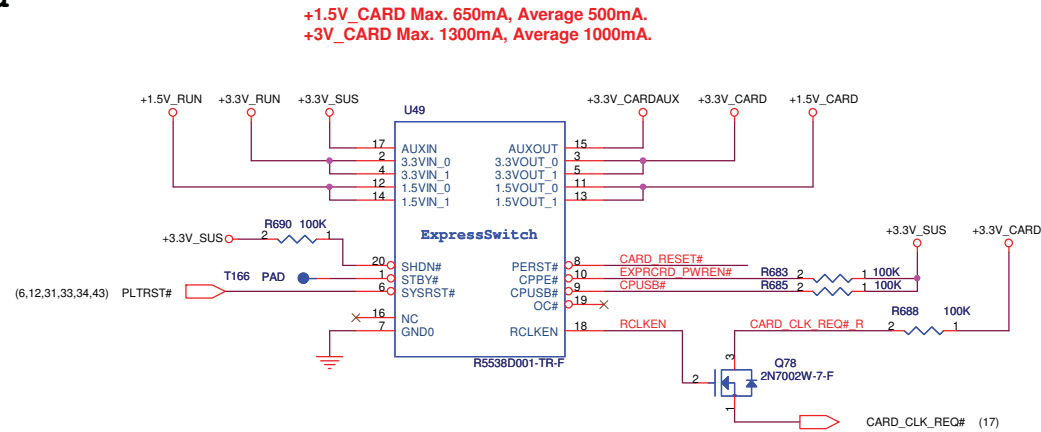
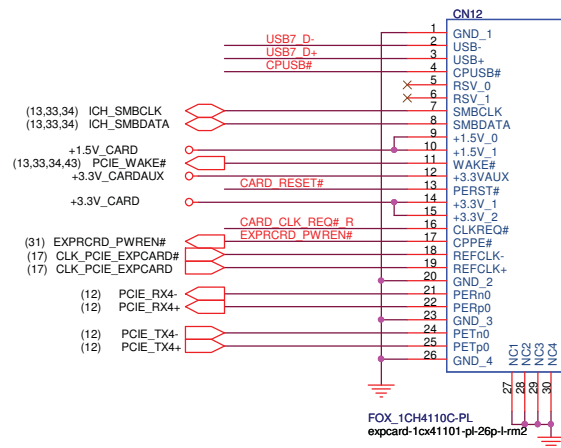
- Layout Note:**
- 1). The distance between Media Card Power Switch and Media Socket should be less than 2-inches.
 - 2). The trace width for +3.3V_RUN_CARD should be 40MIL at least.
 - 3). The GND trace for Media Card Socket should be 40MIL at least.

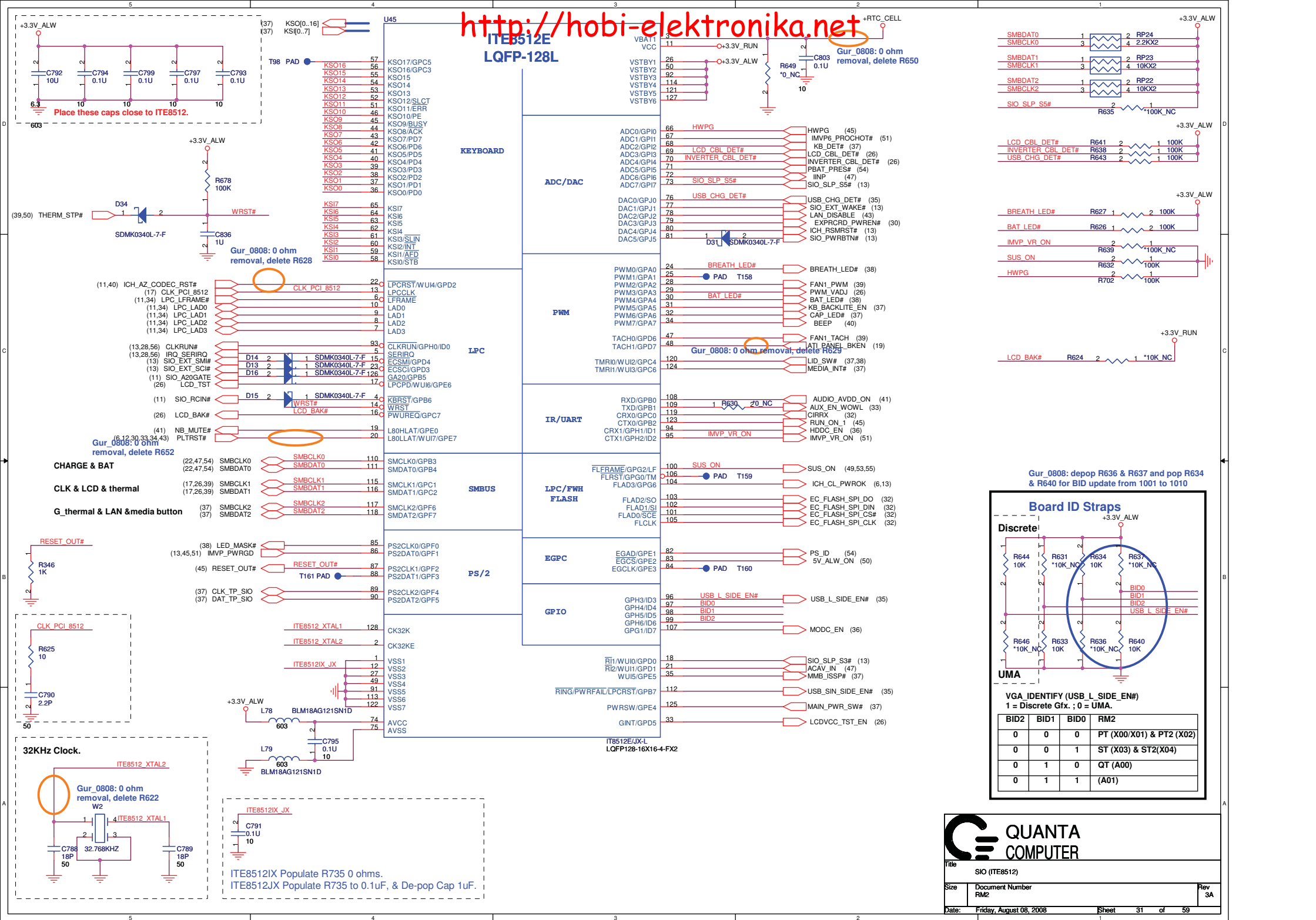


2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.

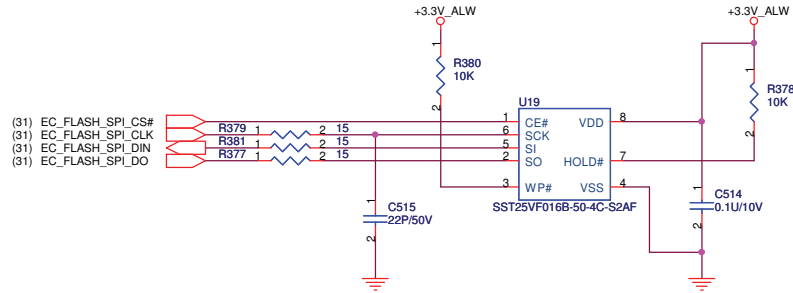


Express Card

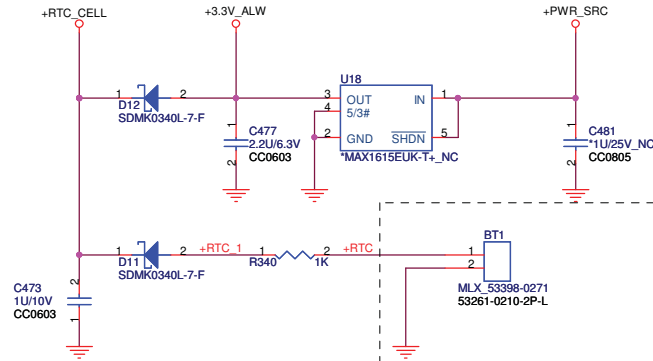




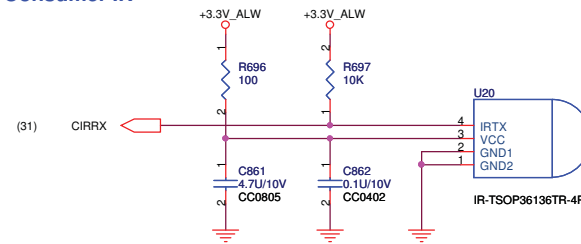
16Mbit (2M Byte), SPI

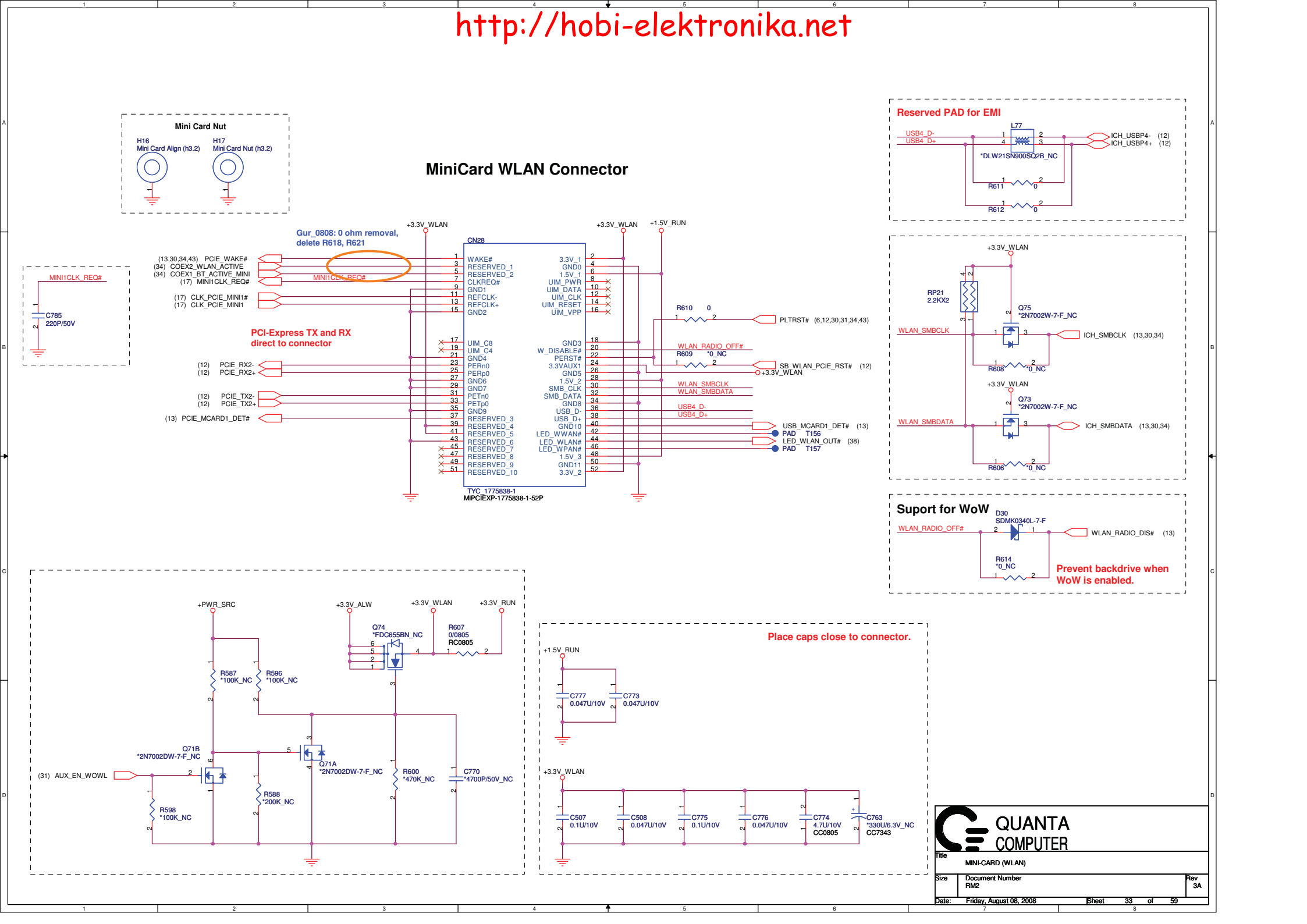


RTC BATTERY



Consumer IR





http://hobi-elektronika.net

Mini Card Nut

H16 Mini Card Align (h3.2) H17 Mini Card Nut (h3.2)

MiniCard WLAN Connector

Gur_0808: 0 ohm removal, delete R618, R621

MINI1CLK_REQ#

C785 220P/50V

PCI-Express TX and RX direct to connector

PCIE_WAKE# (13,30,34,43) COEX2_WLAN_ACTIVE (34) COEX1_BT_ACTIVE_MINI (17) MINI1CLK_REQ# (17) CLK_PCIE_MINI# (17) CLK_PCIE_MINI# (17)

PCIE_RX2- (12) PCIE_RX2+ (12) PCIE_TX2- (12) PCIE_TX2+ (12) PCIE_MCARD1_DET# (13)

WAKE# 1 RESERVED_1 3 RESERVED_2 5 CLKREQ# 7 GND1 9 REFCLK+ 11 REFCLK- 13 UIM_RESET 15 UIM_C8 17 UIM_C4 19 GND4 21 PERn0 23 PERp0 25 GND5 27 1.5V_2 29 PETn0 31 PETp0 33 GND6 35 GND9 37 RESERVED_3 39 RESERVED_4 41 RESERVED_5 43 RESERVED_6 45 RESERVED_7 47 RESERVED_8 49 RESERVED_9 51 RESERVED_10

3.3V_1 2 GND0 4 1.5V_1 6 UIM_PWR 8 UIM_DATA 10 UIM_CLK 12 UIM_RESET 14 UIM_VPP 16

W_DISABLE# 18 PERST# 20 3.3VAUX1 22 GND5 24 1.5V_2 26 SMB_CLK 28 SMB_DATA 30 USB_D- 32 USB_D+ 34 GND8 36 GND10 38 LED_WWAN# 40 LED_WLAN# 42 LED_WLAN# 44 1.5V_3 46 GND11 48 3.3V_2 50 RESERVED_10 52

PLTRST# (6,12,30,31,34,43) WLAN_RADIO_OFF# (12) SB_WLAN_PCIE_RST# (12) WLAN_SMBCLK (13,30,34) WLAN_SMBDATA (13,30,34) USB_MCARD1_DET# (13) LED_WLAN_OUT# (38)

ICL_USB4P4- (12) ICH_USB4P4+ (12)

ICL_SMBCLK (13,30,34) ICH_SMBCLK (13,30,34)

WLAN_RADIO_DIS# (13)

Prevent backdrive when WoW is enabled.

Place caps close to connector.

QUANTA COMPUTER

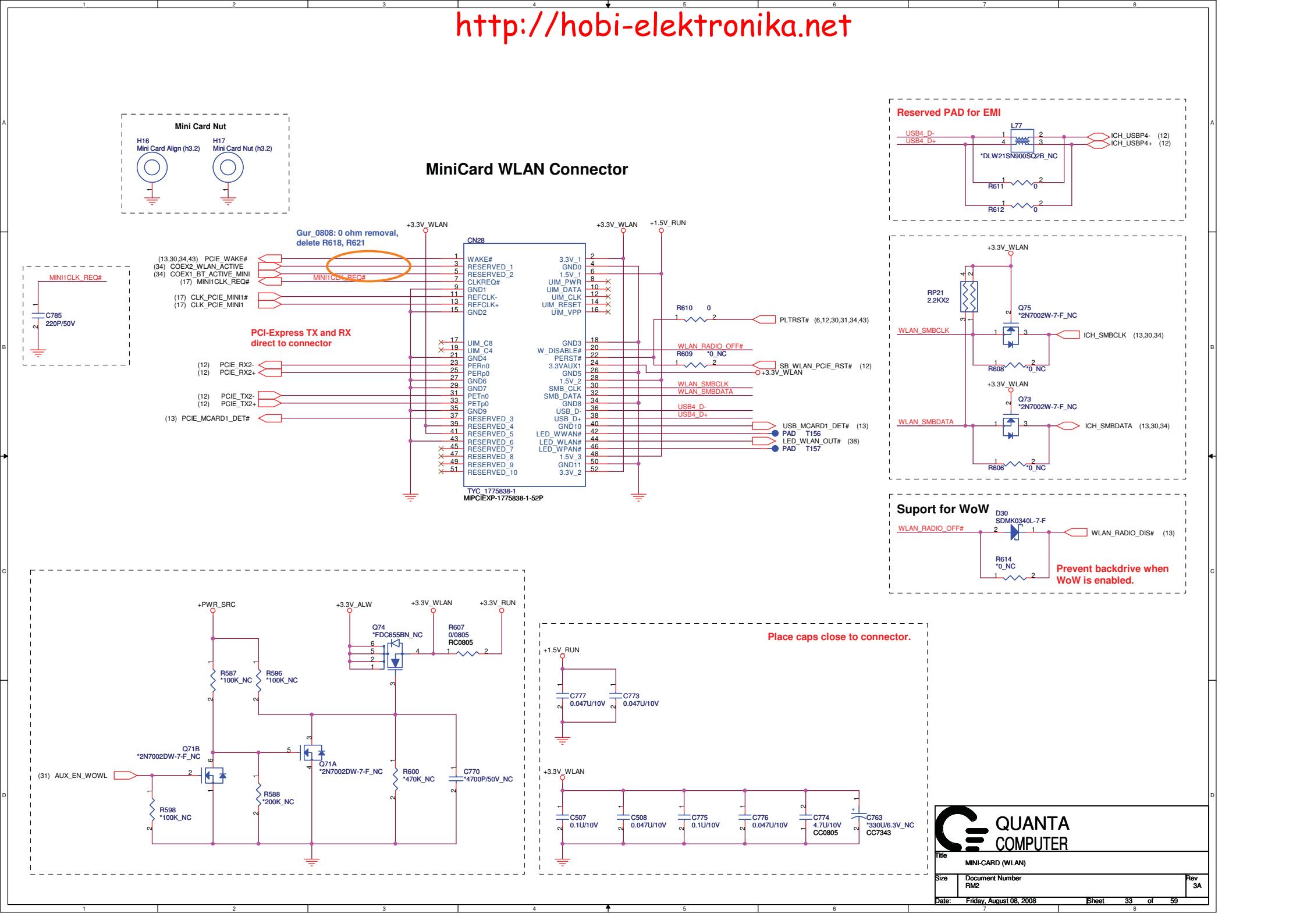
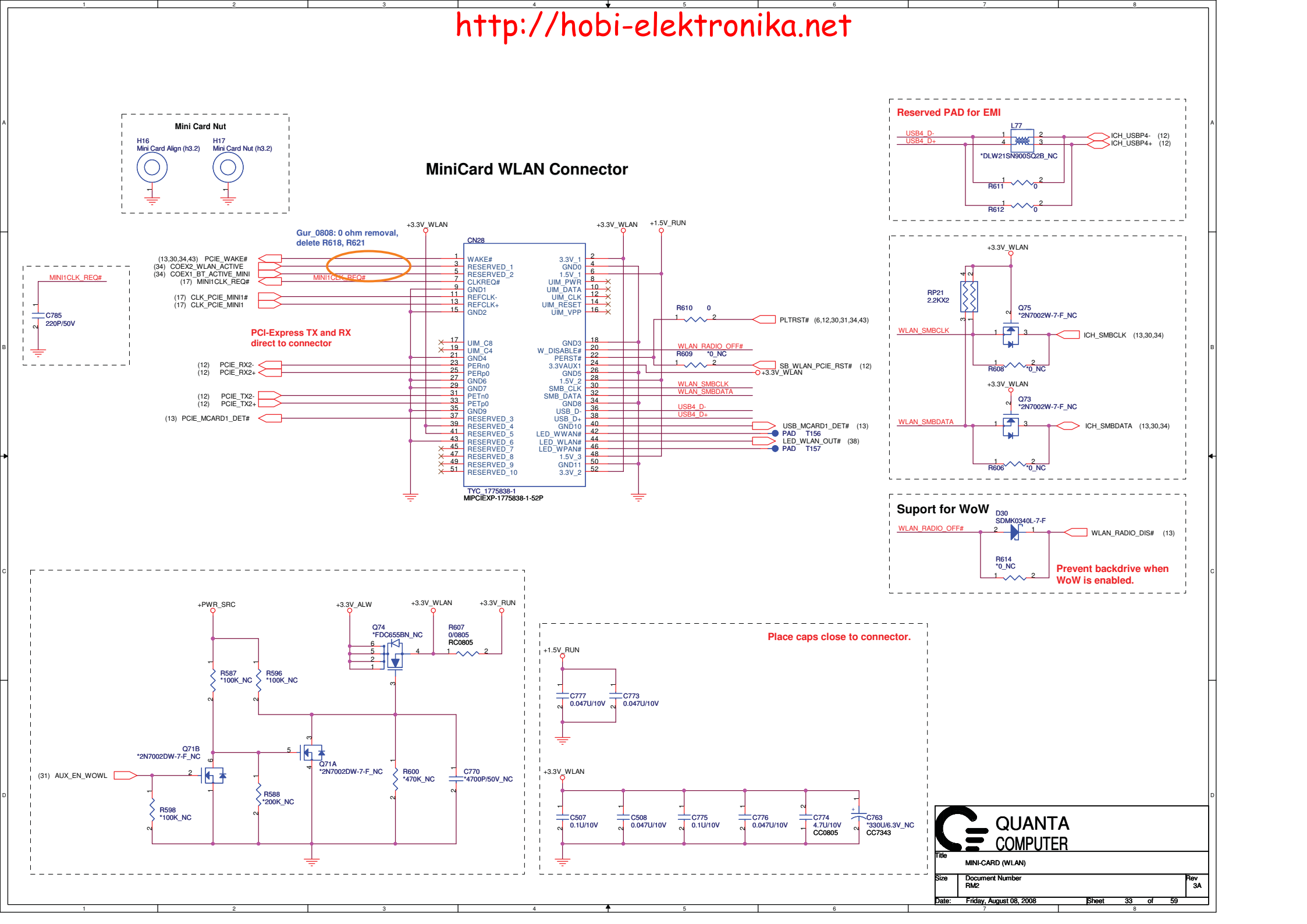
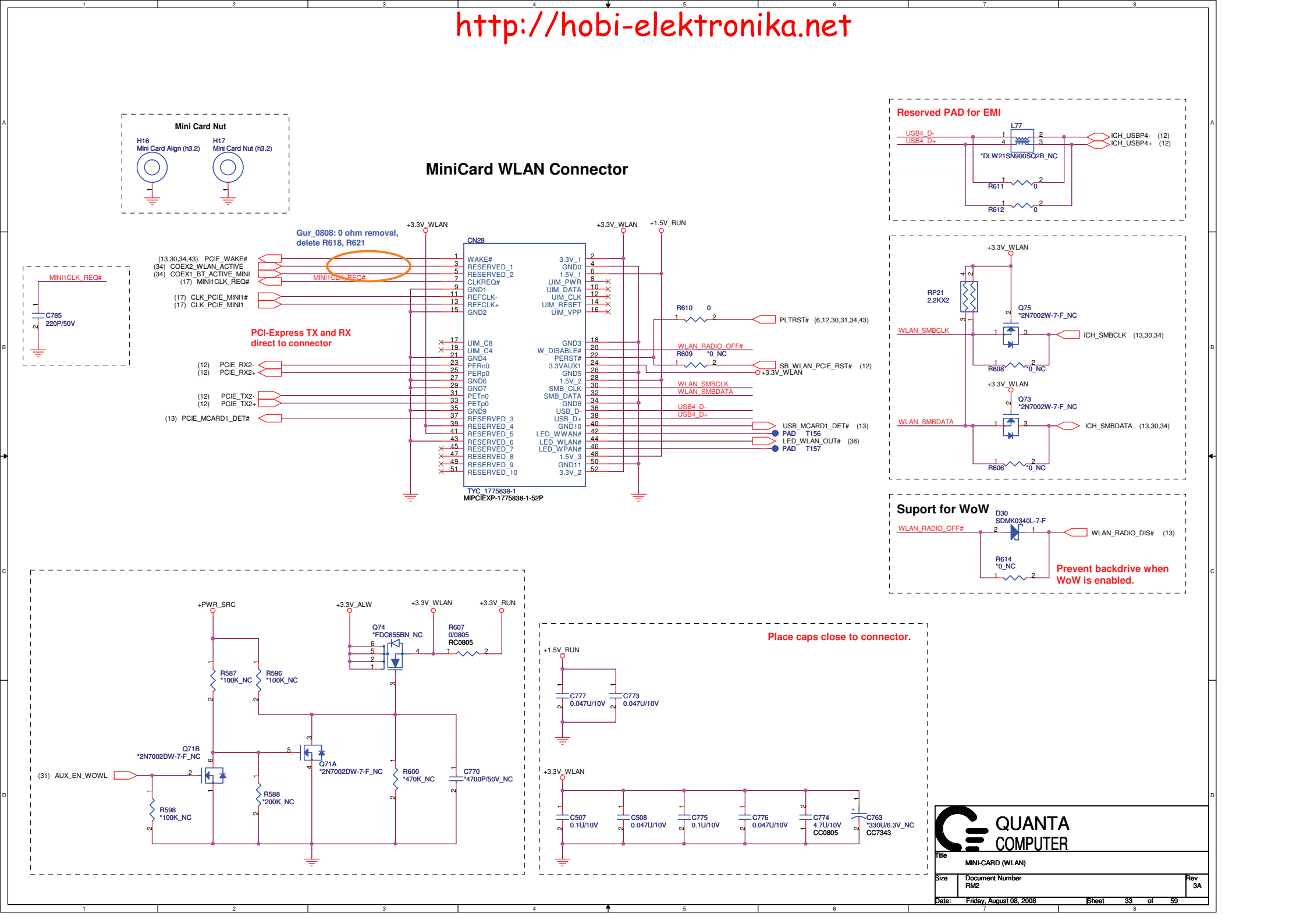
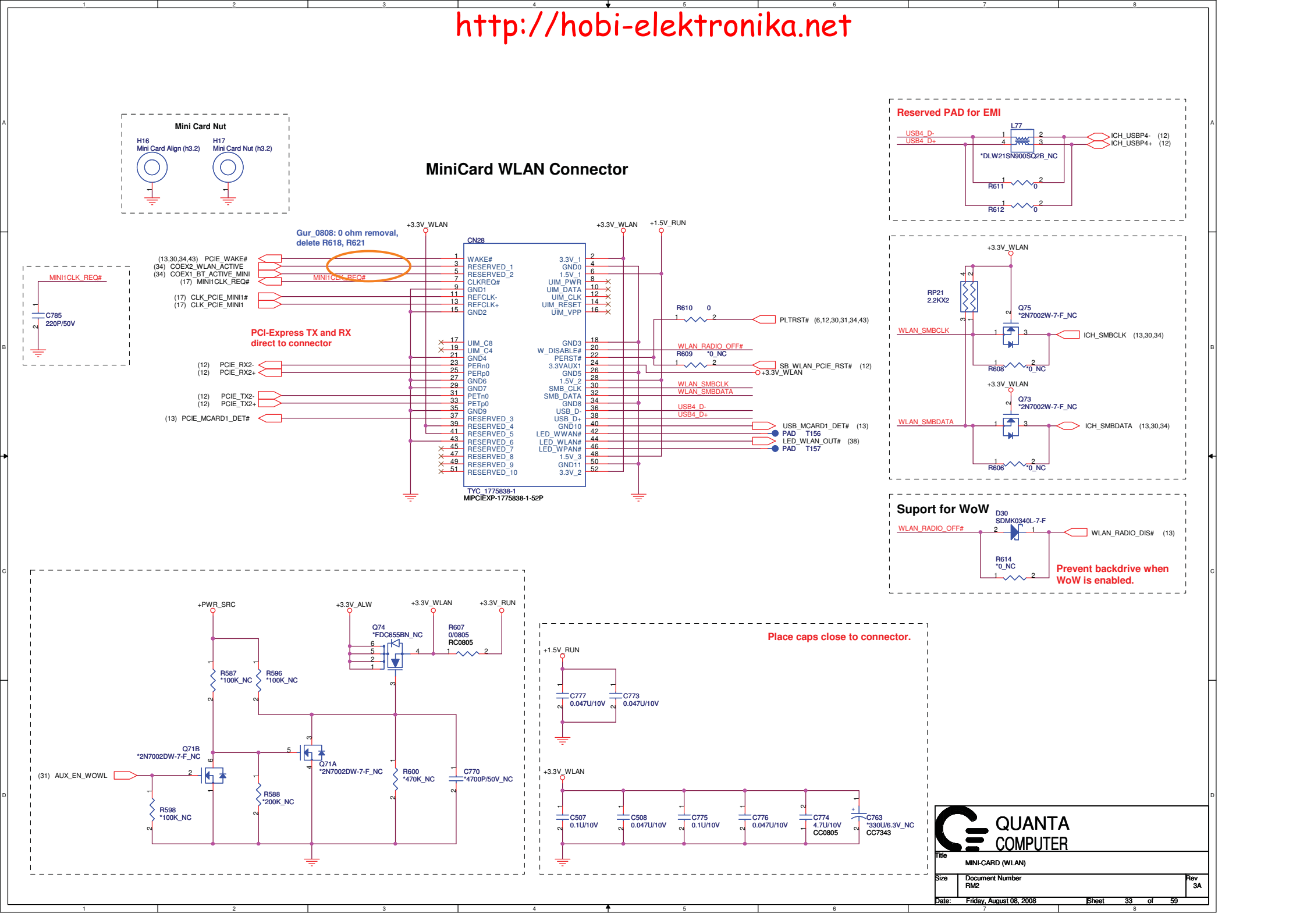
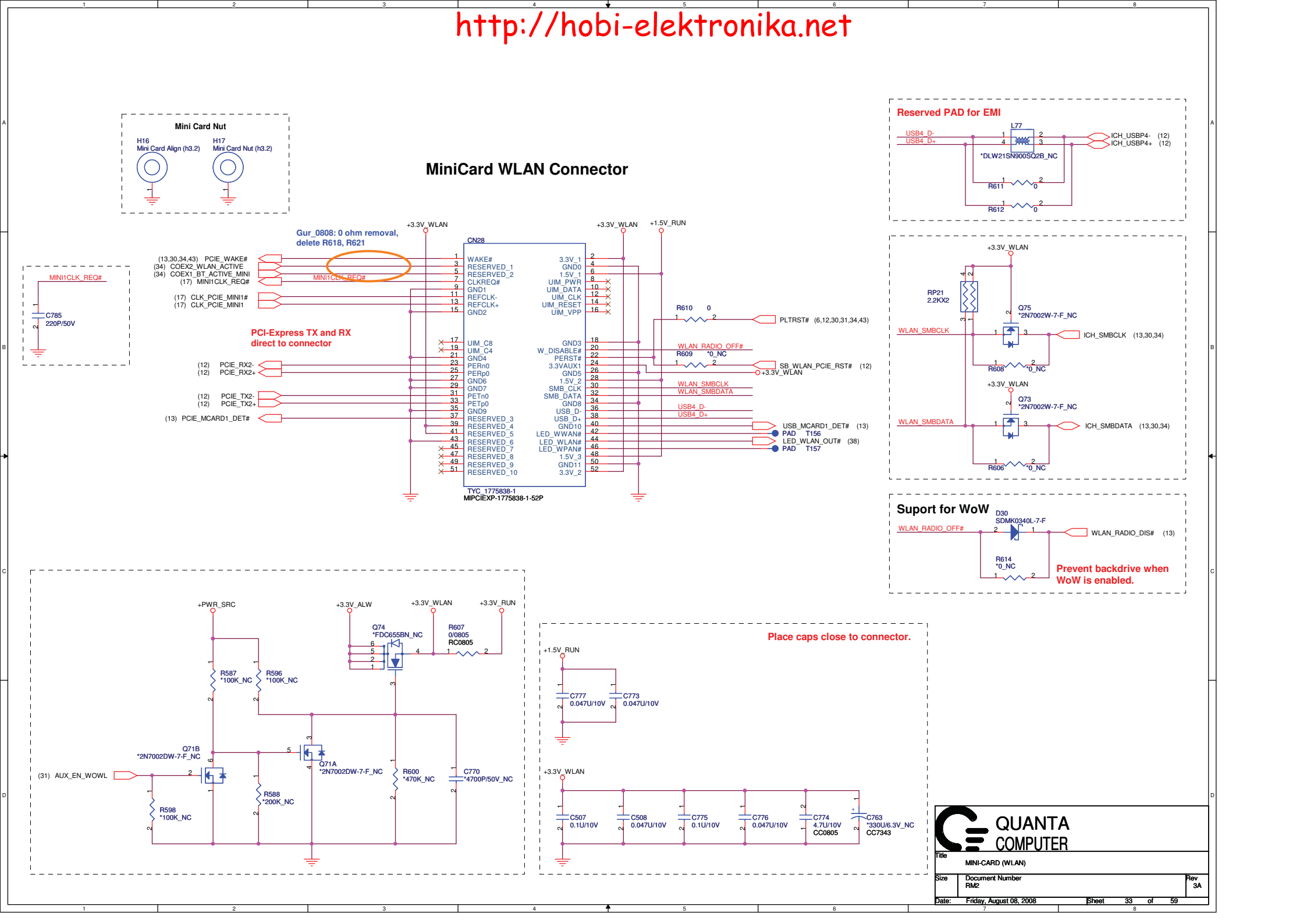
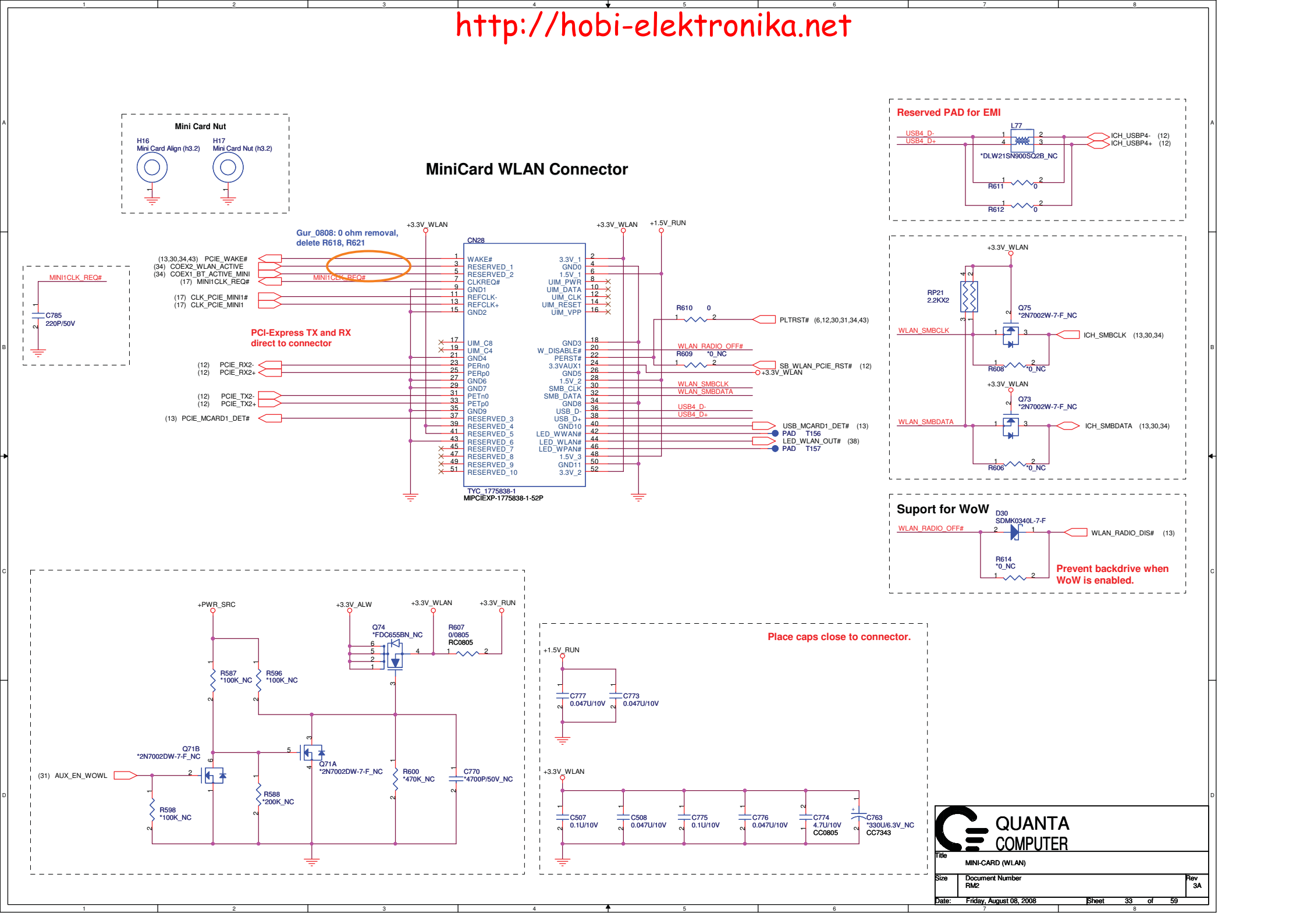
MINI-CARD (WLAN)

Document Number RM2

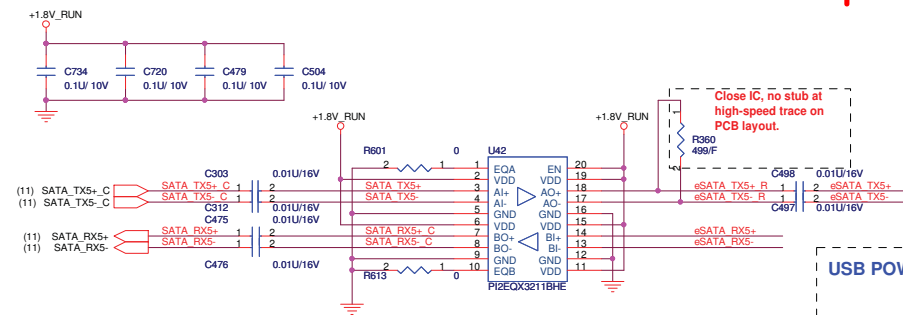
Rev 3A

Date: Friday, August 08, 2008

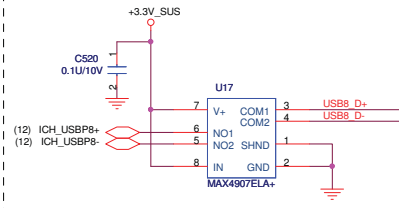
Sheet 33 of 59



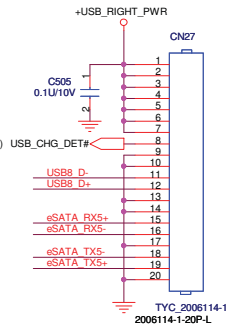
eSATA Re-driver IC



USB BUS SW

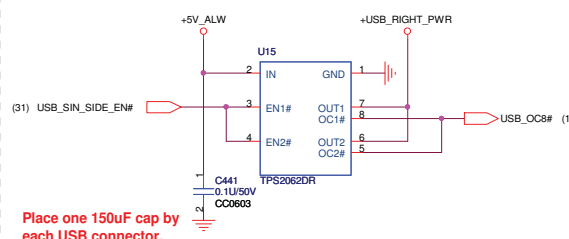


eSATA CONN



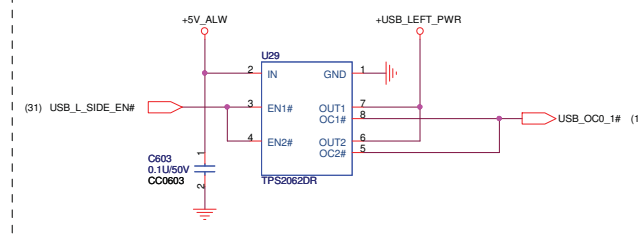
USB POWER SW

Each channel is 1A

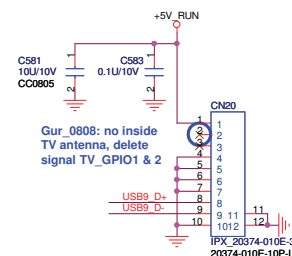
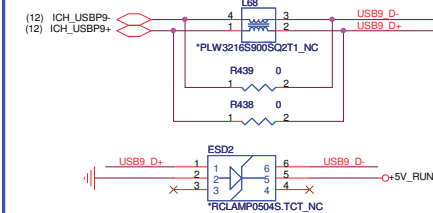


USB POWER SW

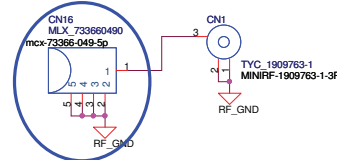
Each channel is 1A



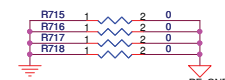
TV module



TV RF Jack & Microwave connector



Gur_0814: change P/N & footprint & library for non-switch RF Jack



To Daughter Board connector

Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White" = System in Standby (S3);

Power Button

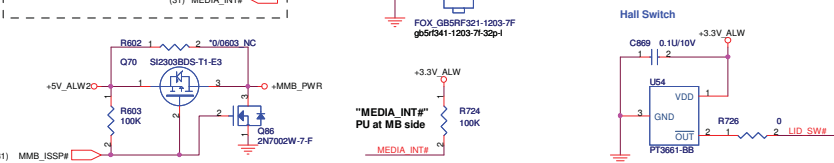
Speaker

Gur_0614: change
R722 to connect to
R721 from pin1 to pin2

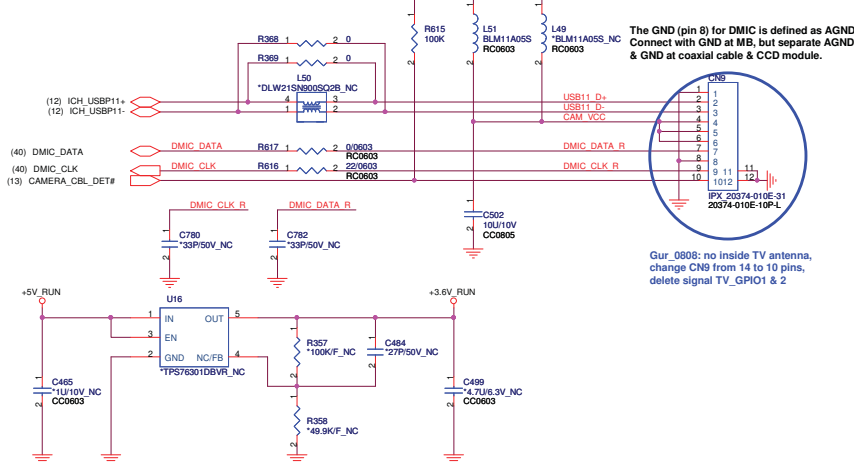
KB LED

Touch Pad

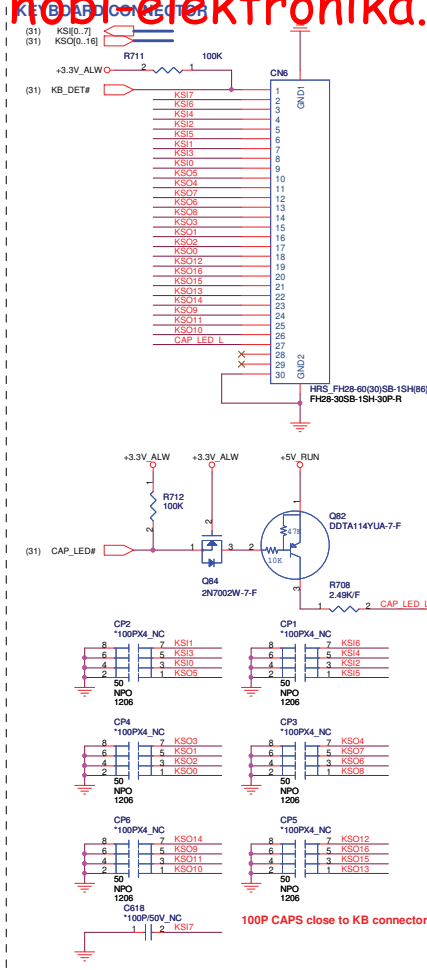
Media Button



Array Microphone & Camera



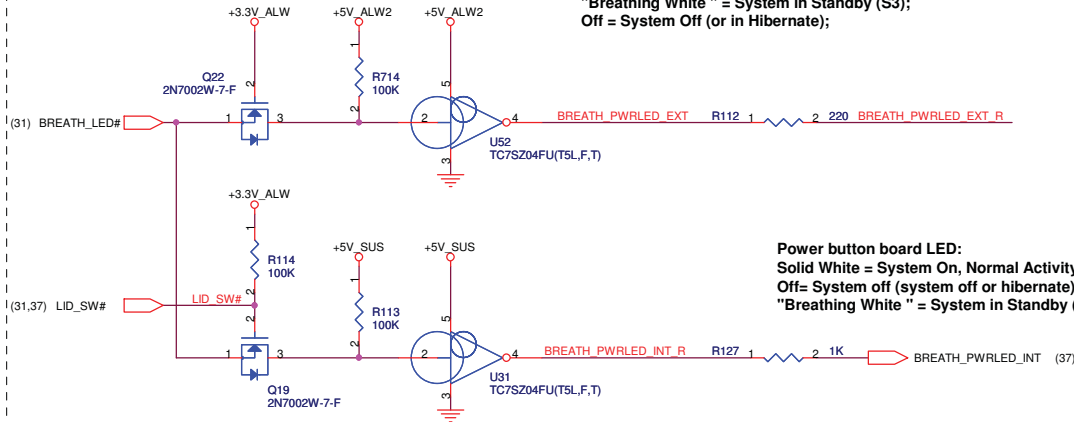
KB Board connector



Hinge & Power Button board LED (PWR/Battery indicator)

Hinge LED

Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

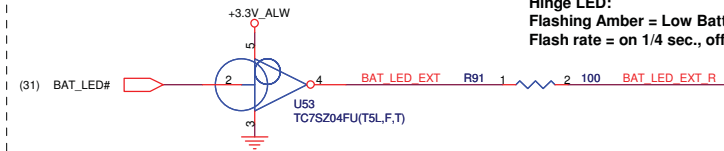


Power button board LED:

Solid White = System On, Normal Activity
Off= System off (system off or hibernate);
"Breathing White " = System in Standby (S3)

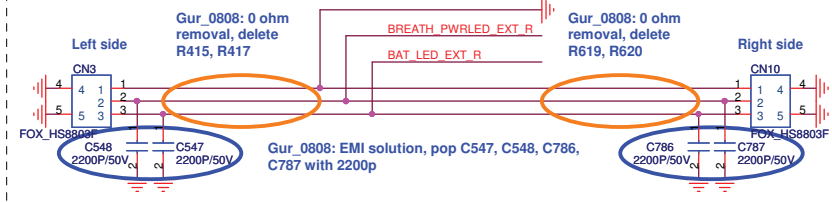
Hinge LED:

Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.



Hinge LED (PWR/Battery indicator)

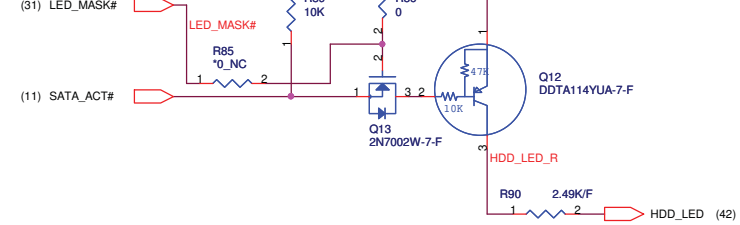
L-C filter (reserve R-C) for EMI



Solid White= System On, Normal Activity
Solid White= Charging (system on);
Solid White= Charging (system off or hibernate and battery charge <90%);
Off= Charging (system off or hibernate and battery charge > 90%);
"Breathing White " = System in Standby (S3);
Off = System Off (or in Hibernate);

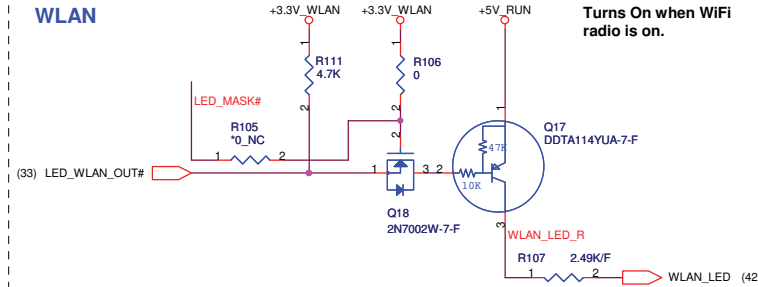
Flashing Amber = Low Battery (S0 and S3 and no AC) when battery charge <10%
Flash rate = on 1/4 sec., off 3/4 sec.

HDD Activity LED



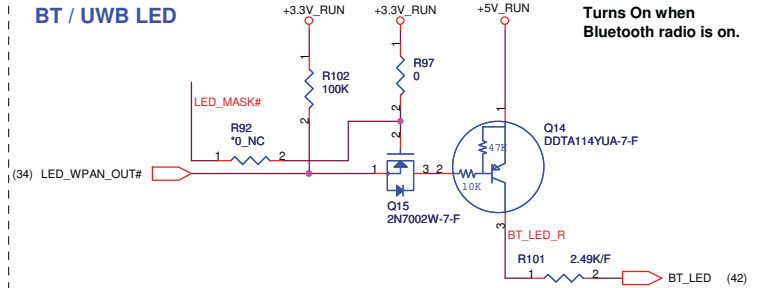
Flicker with HDD activity.

WLAN



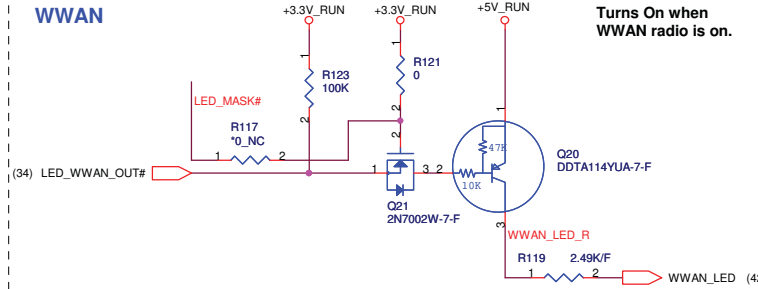
Turns On when WiFi radio is on.

BT / UWB LED



Turns On when Bluetooth radio is on.

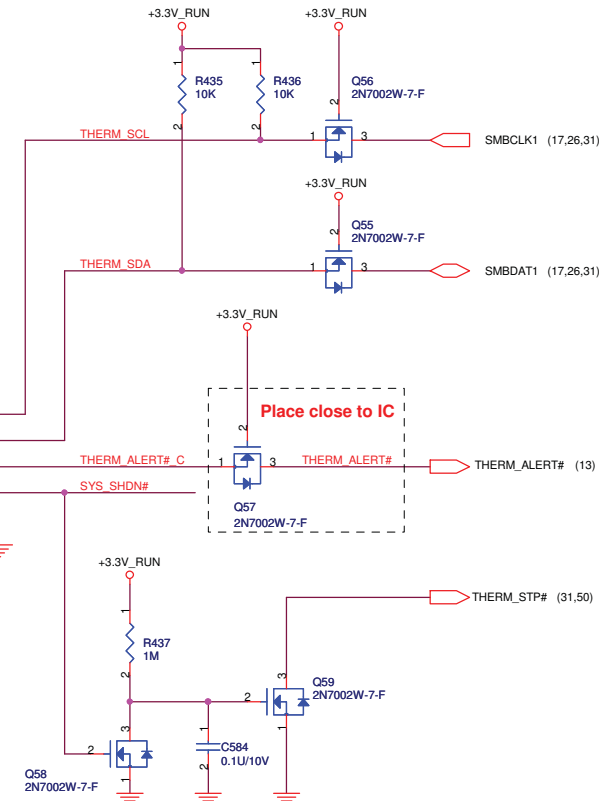
WWAN



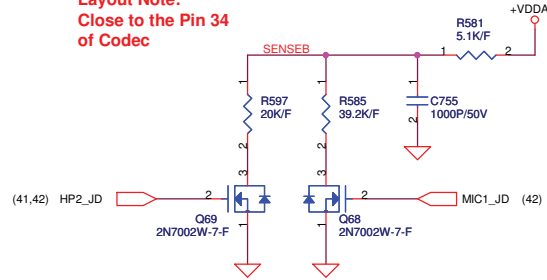
Turns On when WWAN radio is on.



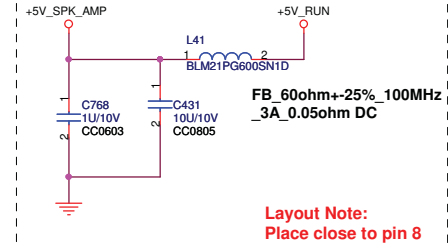
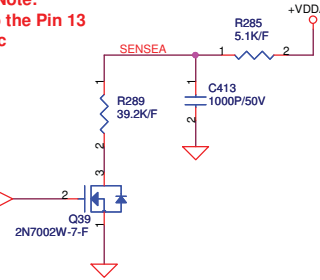
Title			LED
Size	Document Number	Rev	
	RM2	3A	
Date:	Friday, August 08, 2008	Sheet	38 of 59



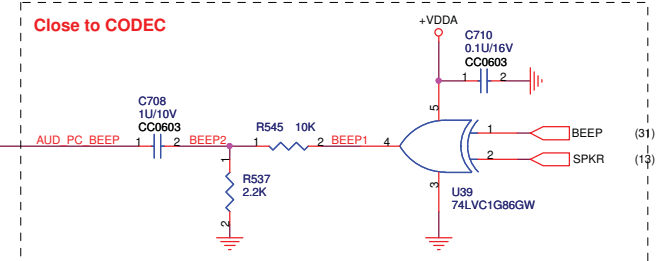
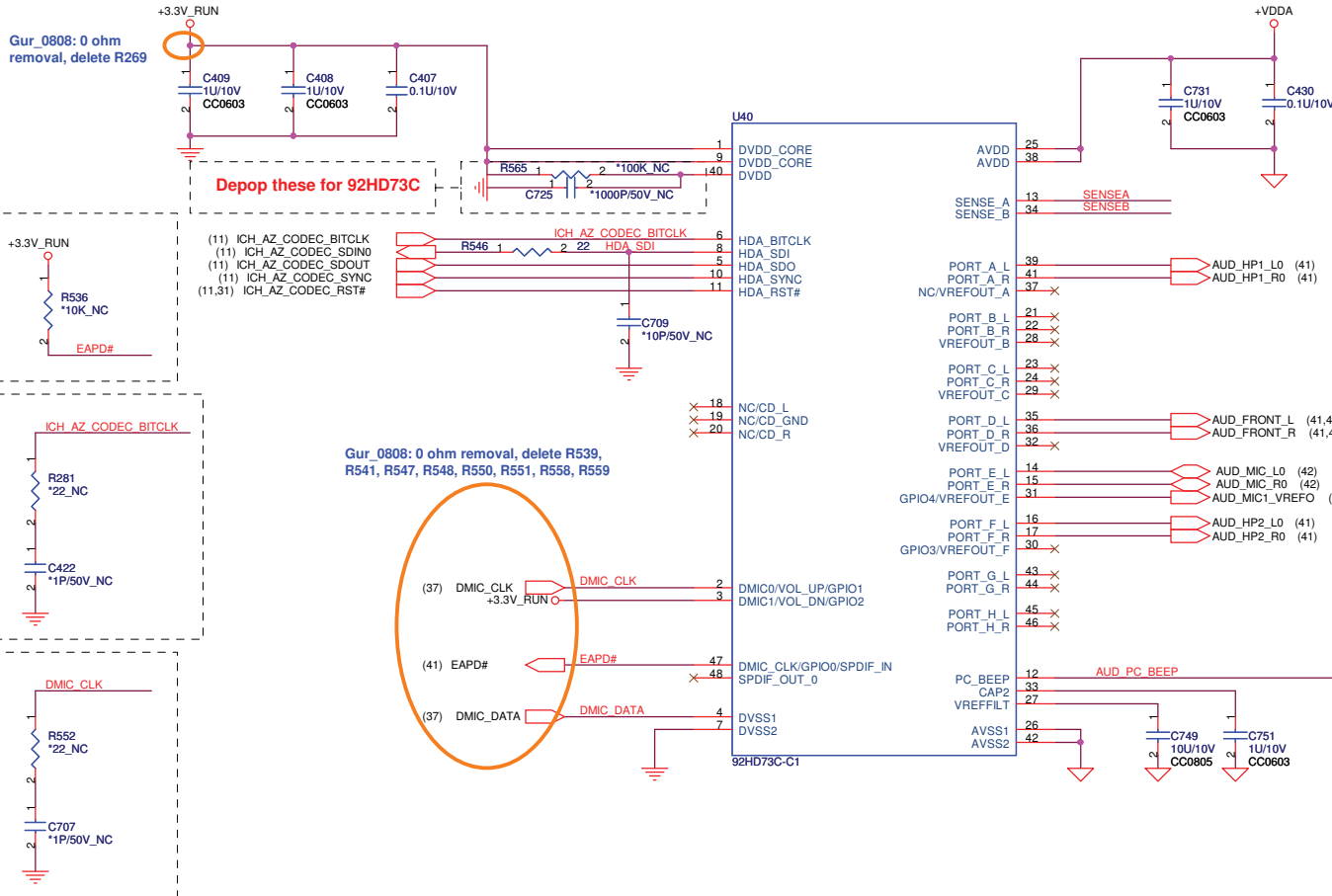
Layout Note:
Close to the Pin 34
of Codec

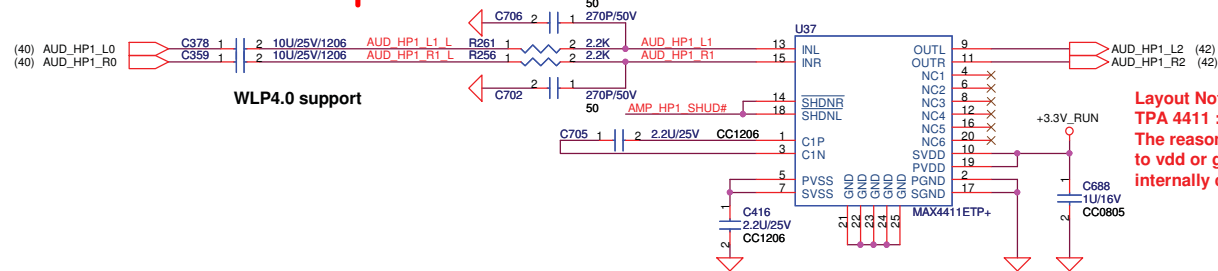


Layout Note:
Close to the Pin 13
of Codec

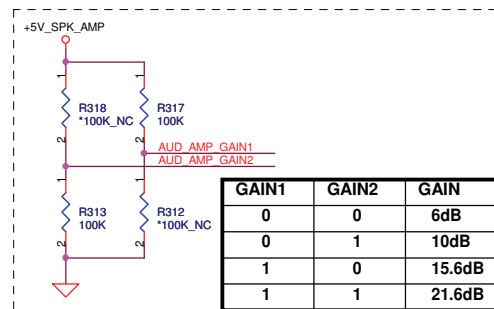
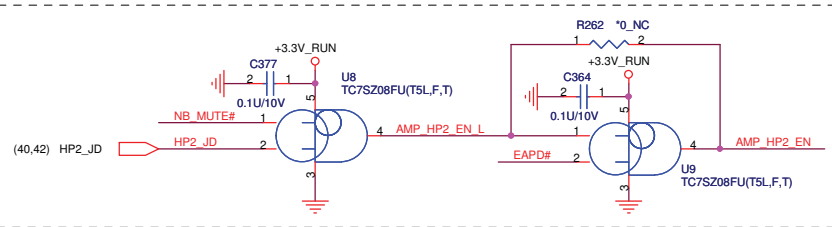


AZALIA (HD) CODEC

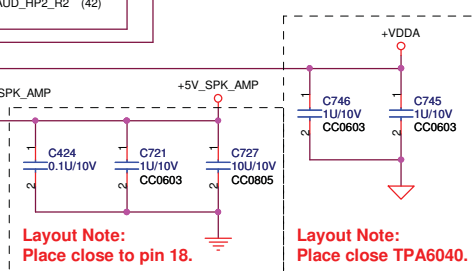
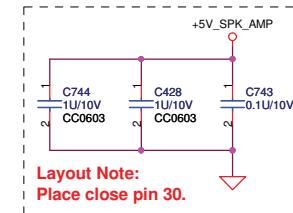
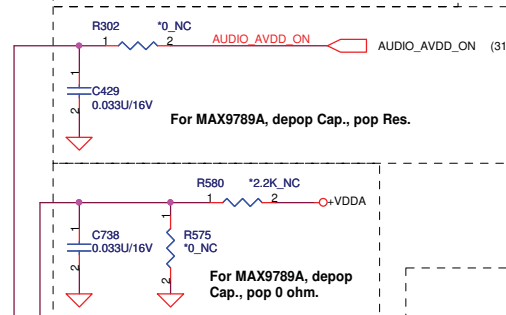
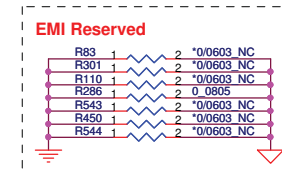
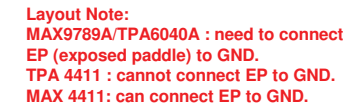




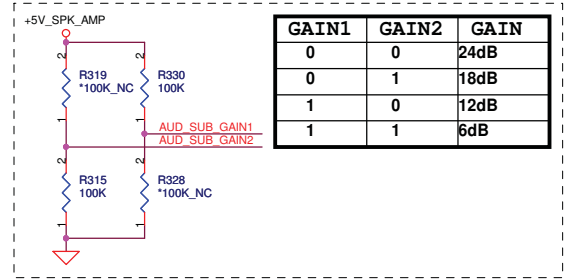
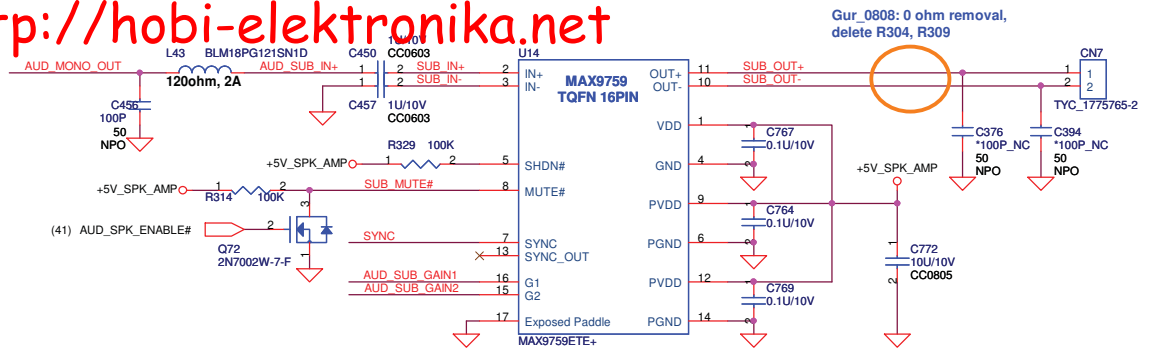
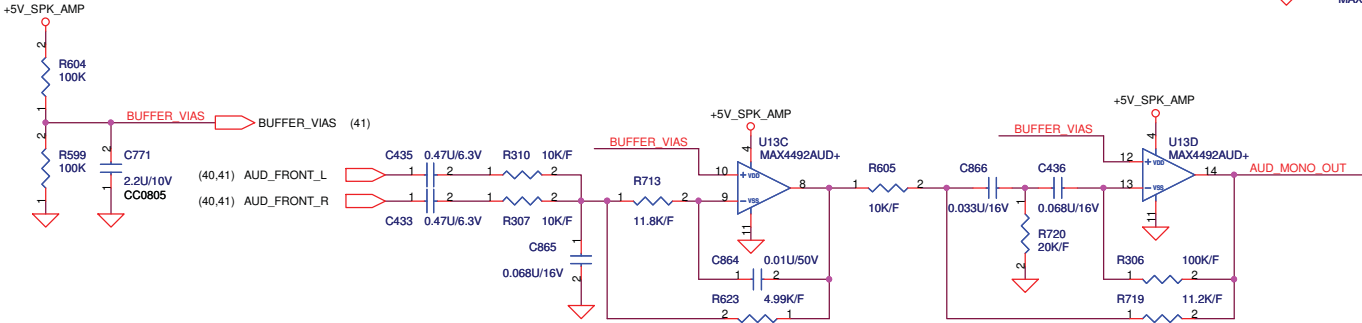
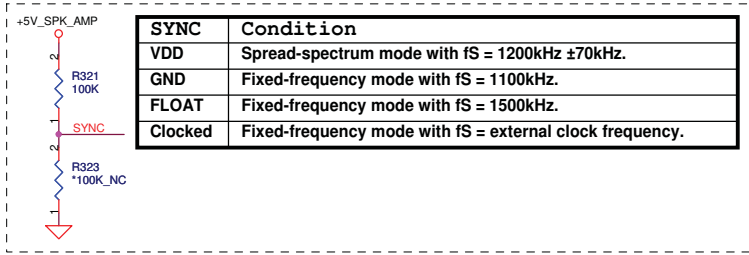
Layout Note:
TPA 4411 : cannot connect EP to GND.
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



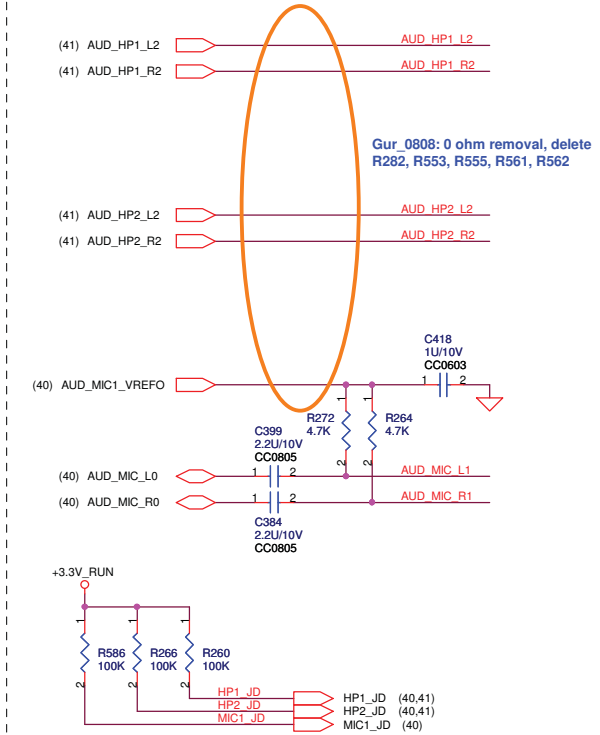
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



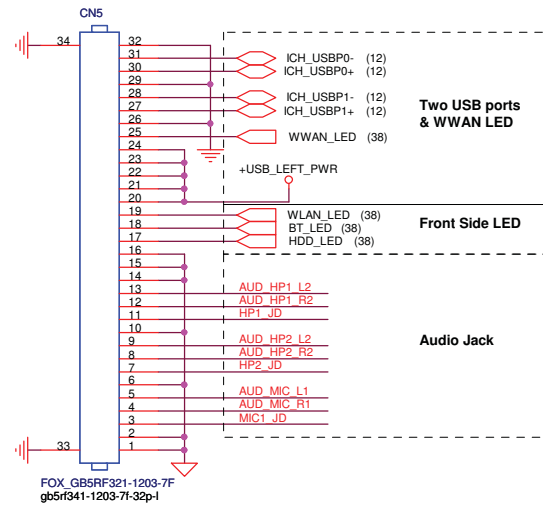
INTERNAL SUBWOOFER AMP



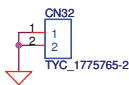
Ambient Parts of Headphone & MIC Jack



To IB(IO Board) connector

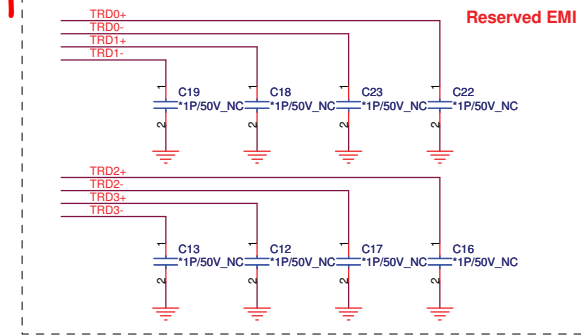
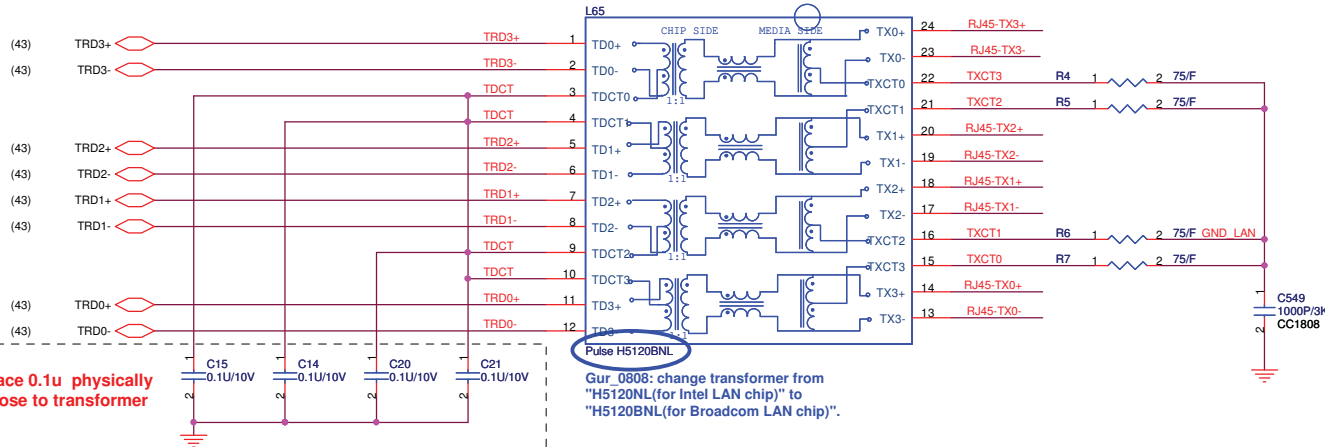


Adding additional AGND

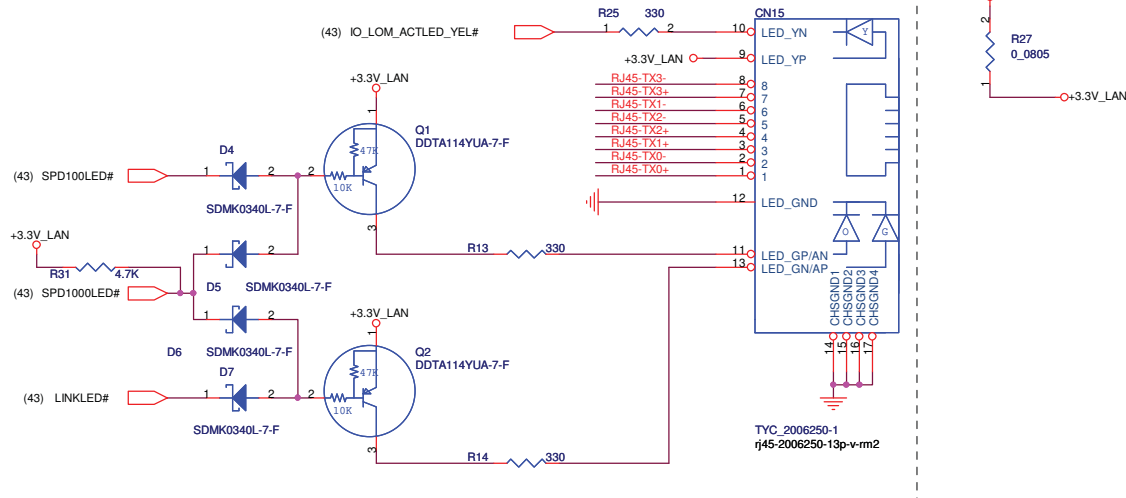


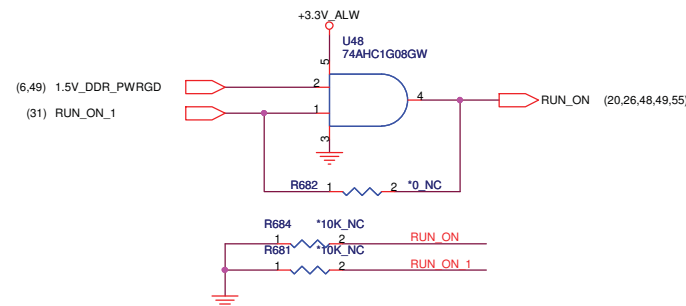
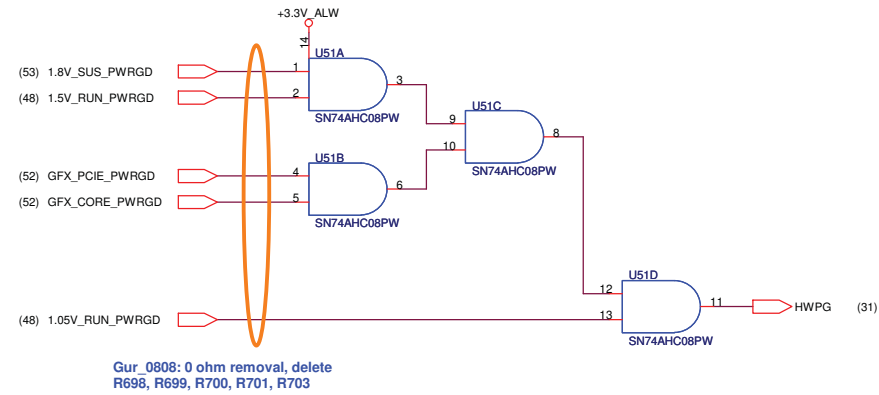
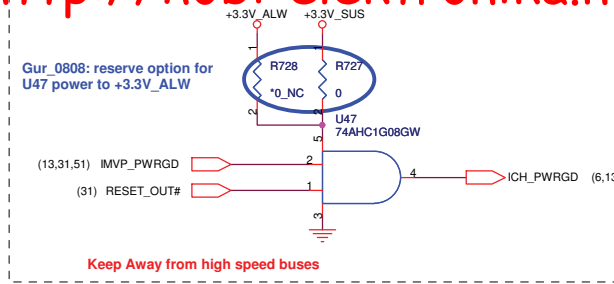
TRANSFORMER

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.

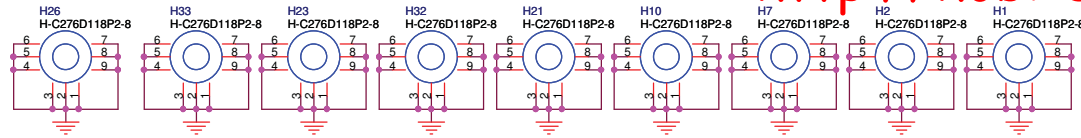


RJ-45 Connector

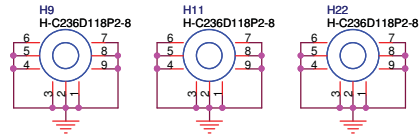




H-C276D118P2-8 * 9



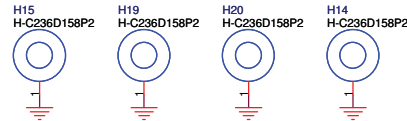
H-C236D118P2-8 * 3



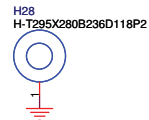
h-c236d197p2 * 1



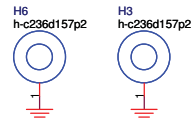
H-C236D158P2 * 4



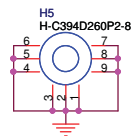
H-T295X280B236D118P2 * 1



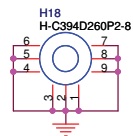
h-c236d157p2 * 2



h-c394d260p2 * 1



H-C394D260P2-8 * 1

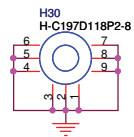


h-c236d236n * 2

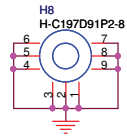


Gur_0814: delete H27

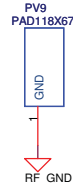
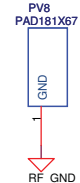
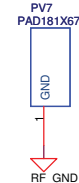
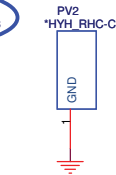
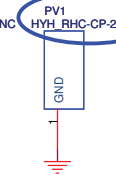
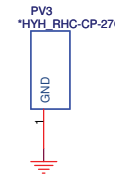
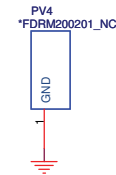
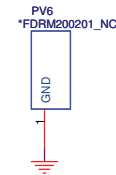
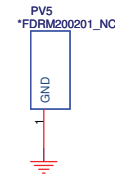
H-C197D118P2-8 * 1

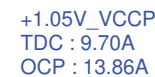


H-C197D91P2-8 * 1

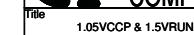


h-o205x157d138x91p2 * 1

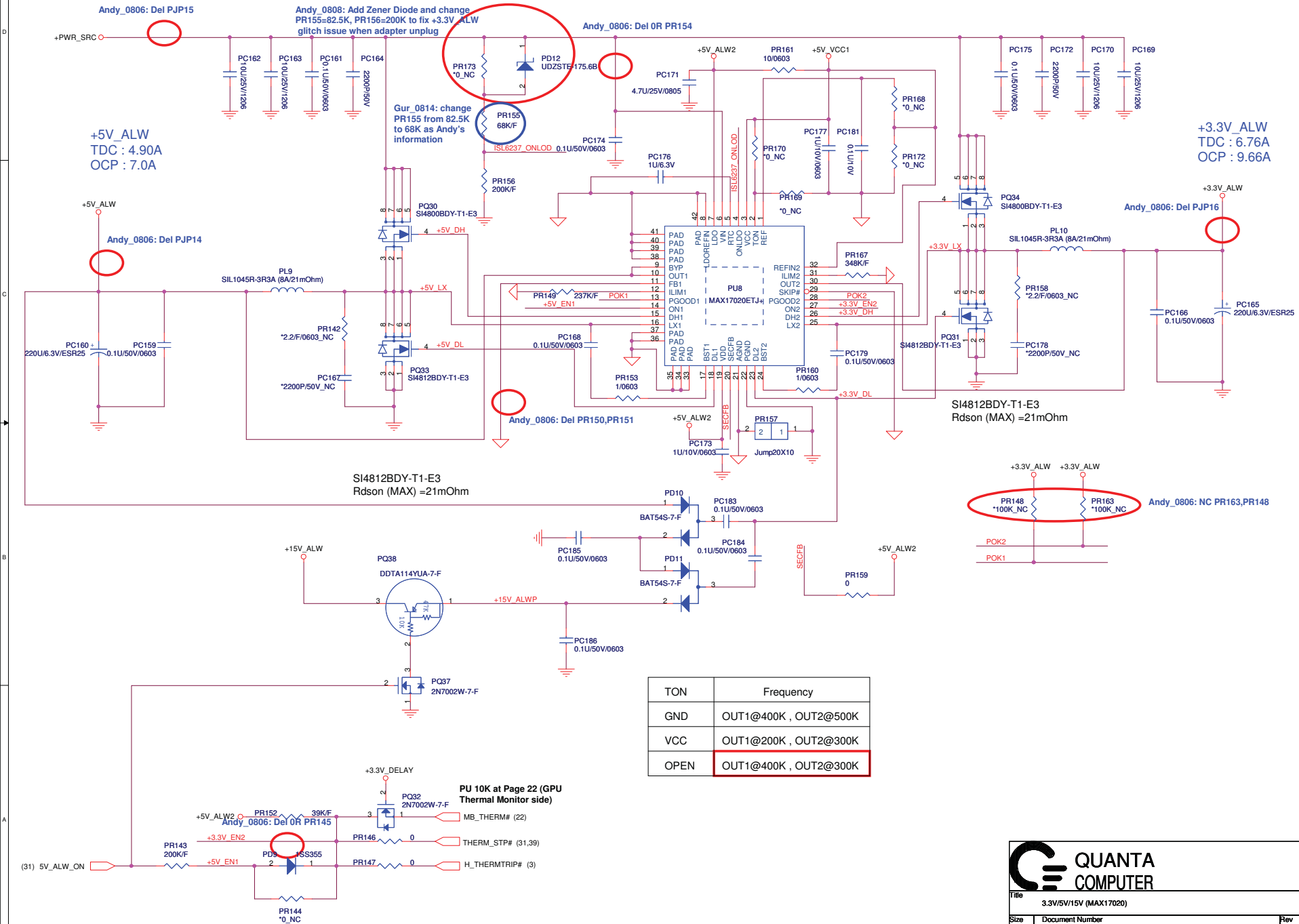


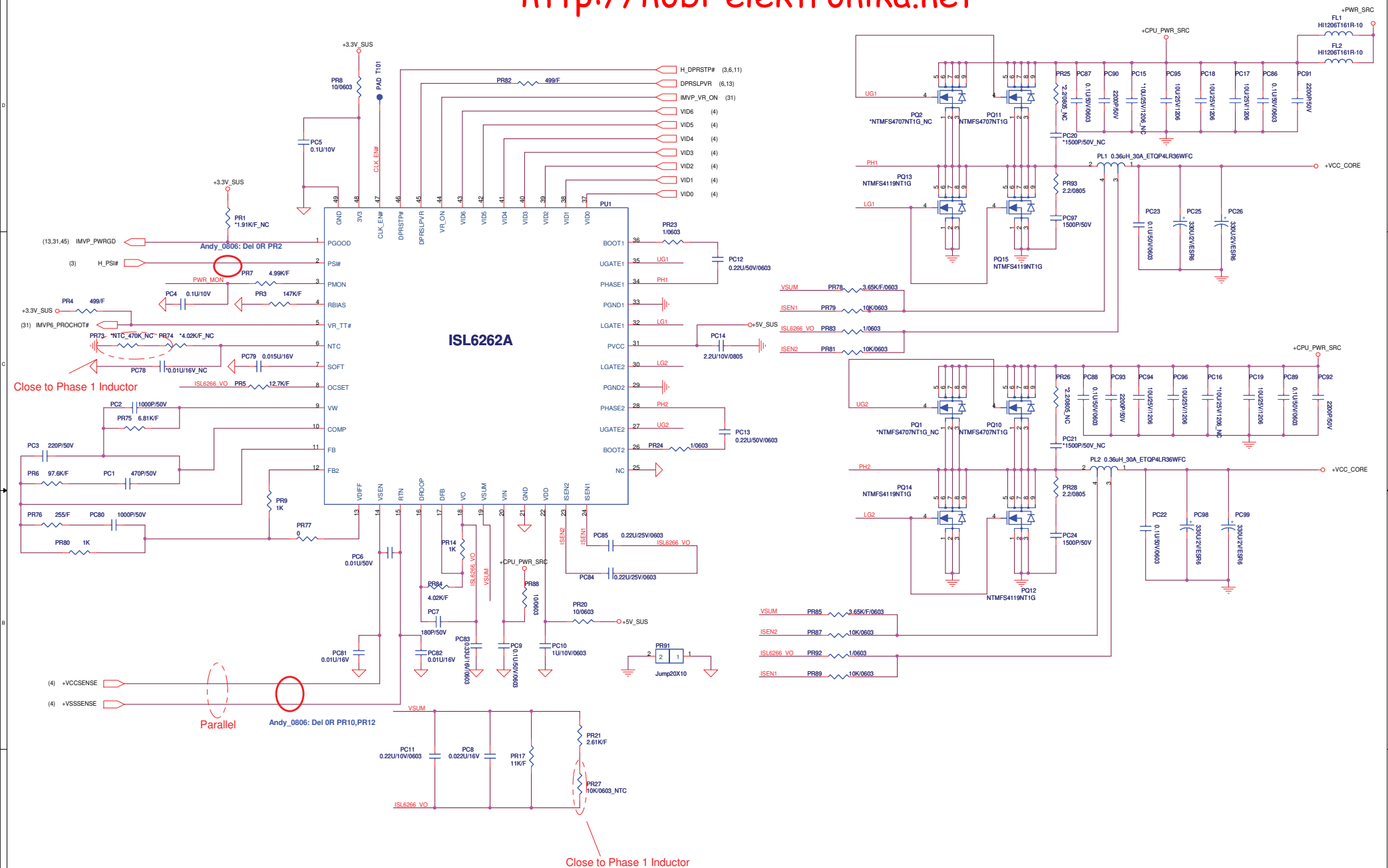


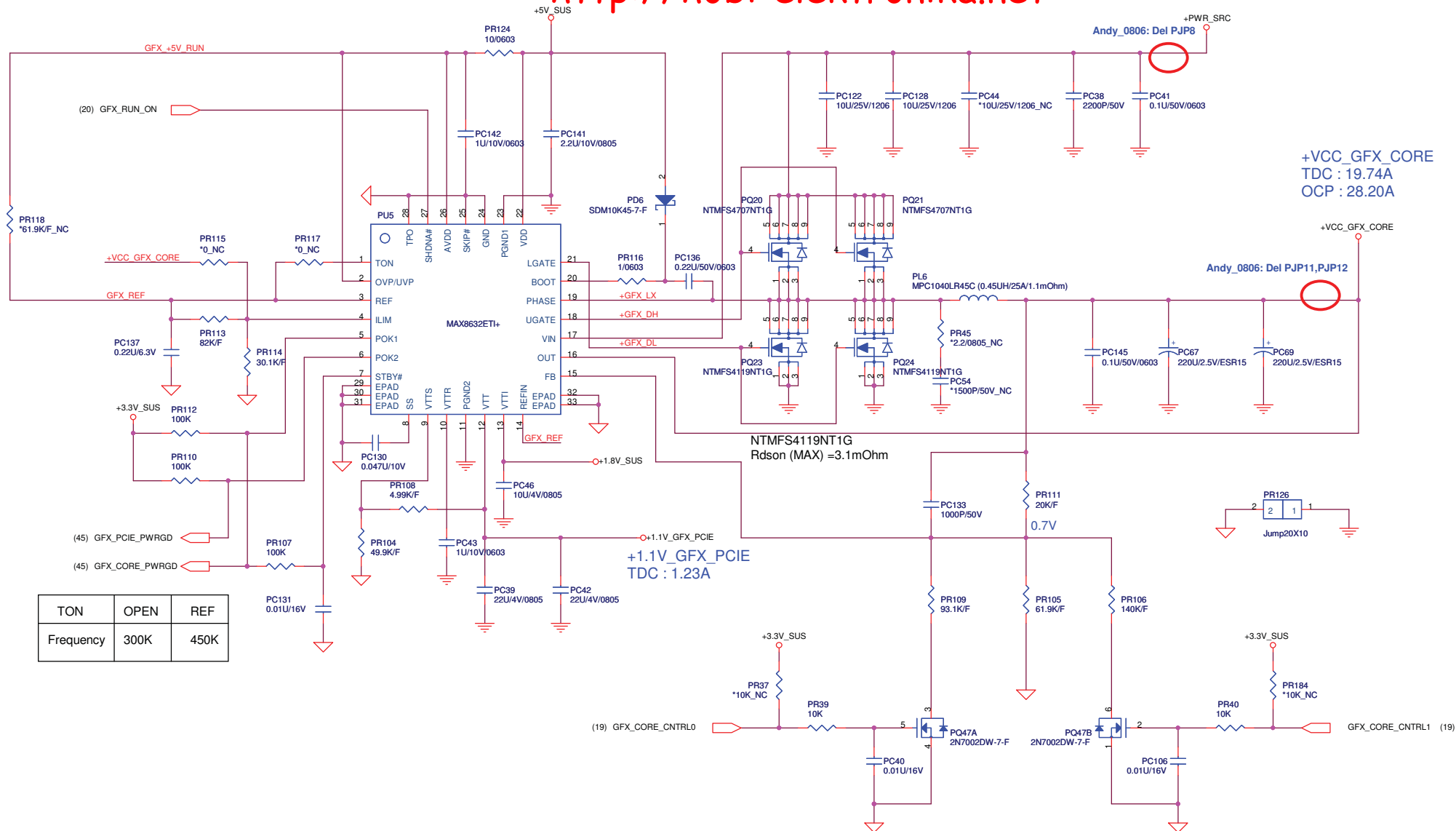
FDS6680AS
Rdson (MAX) =12.5mOhm



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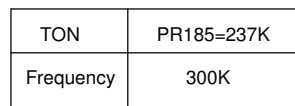


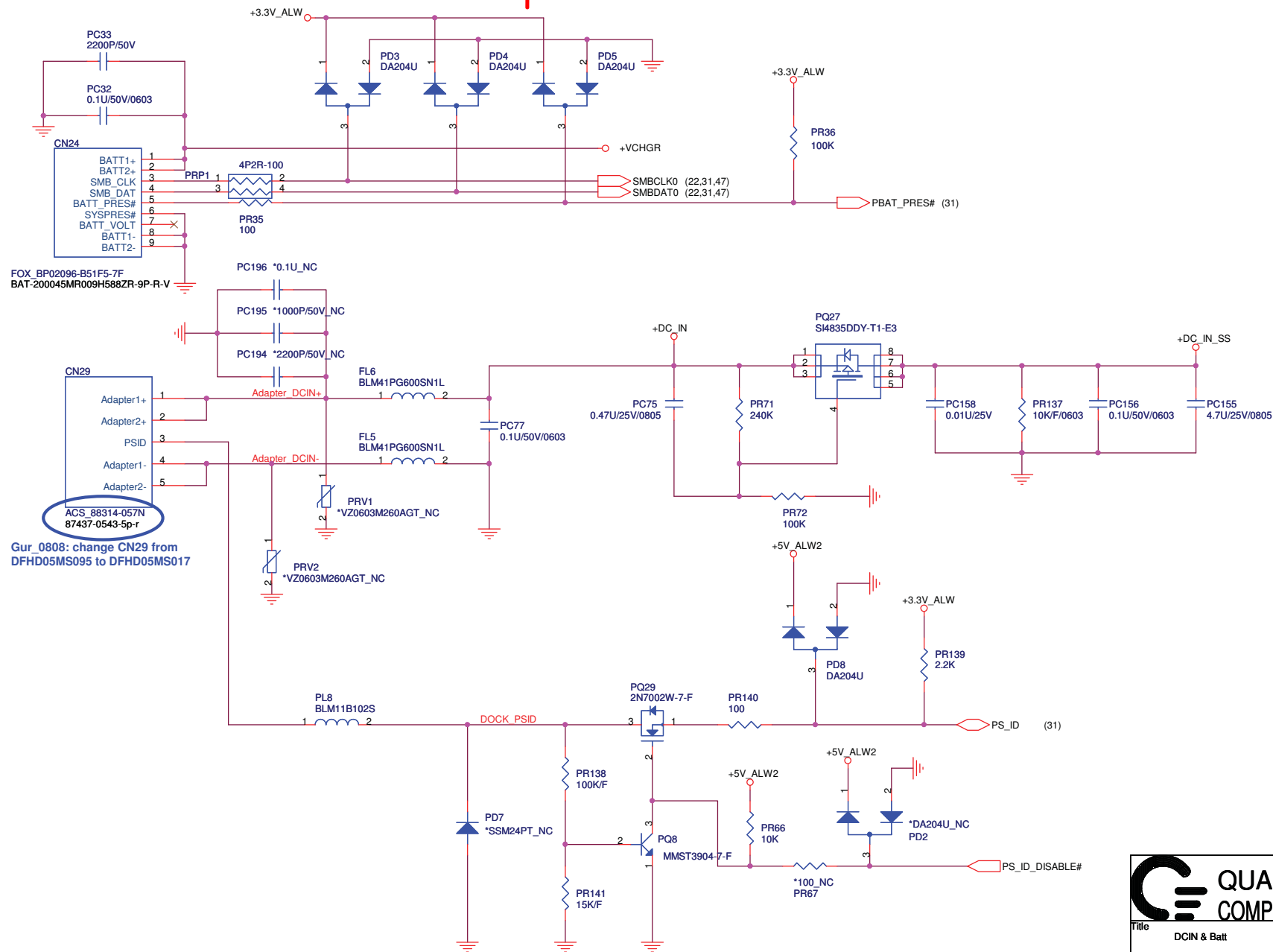


TON	OPEN	REF
Frequency	300K	450K

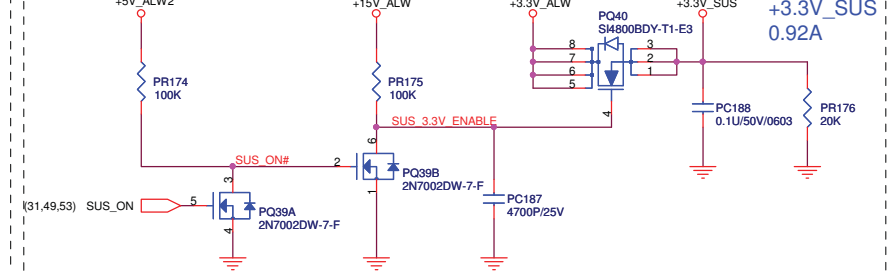
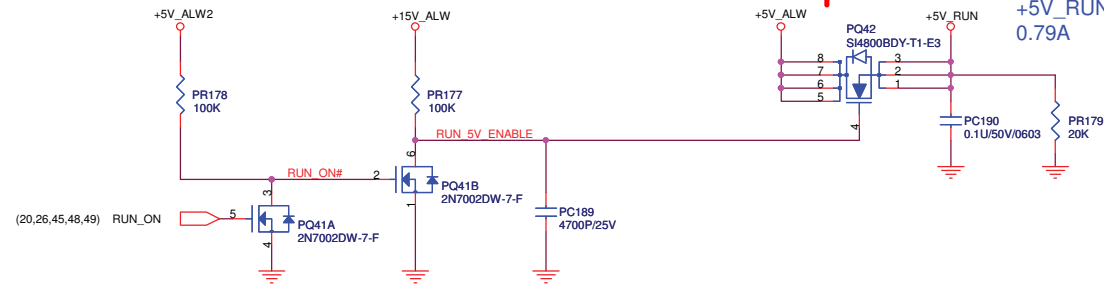
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.95
HIGH	LOW	1.1V
HIGH	HIGH	1.2V

ILIM	$I_{OVP} = (2 * R_b / (R_a + R_b)) * 0.1 * (1 / R_{DS(on)}) + (I_{\Delta} / 2)$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVP	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

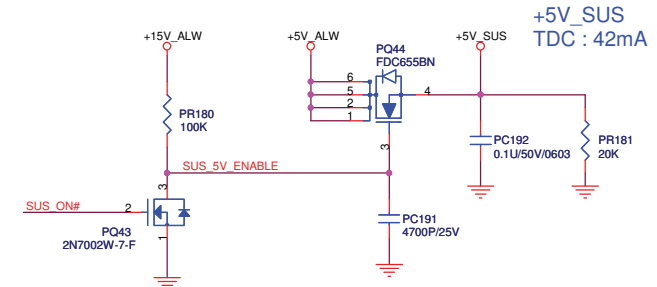
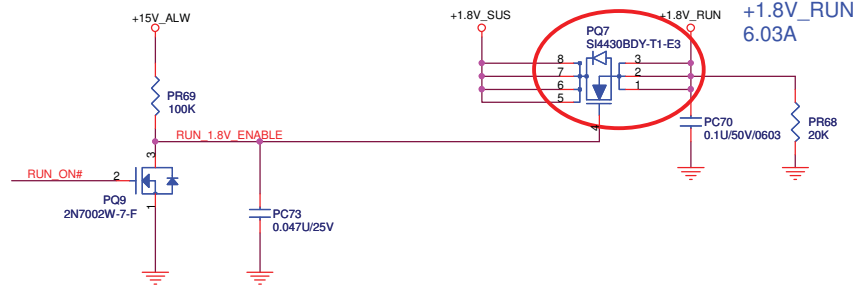




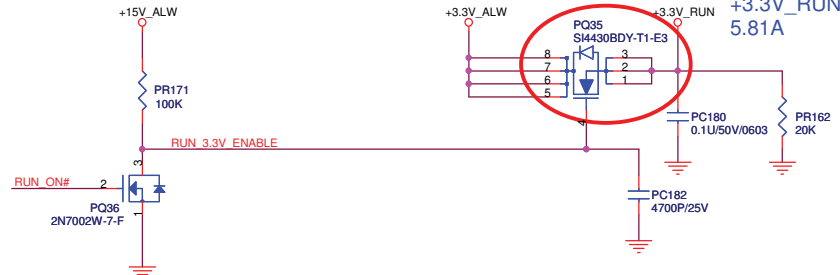
Title			DCIN & Batt
Size	Document Number	Rev	
	RM2	3A	
Date:	Friday, August 08, 2008	Sheet	54 of 59



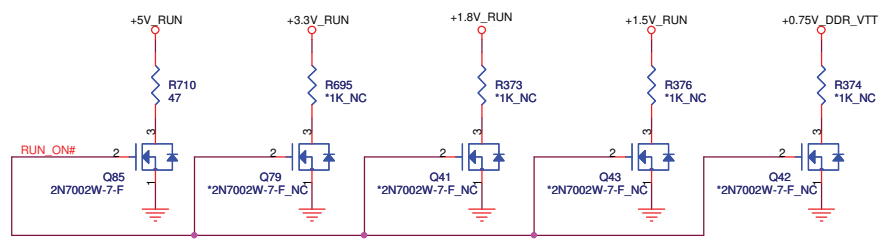
Andy_0807: Change to SI4430BDY-T1-E3
due to SI4336DY-T1-E3 EOL



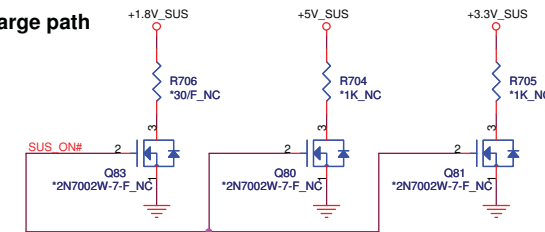
Andy_0807: Change to SI4430BDY-T1-E3
due to SI4336DY-T1-E3 EOL



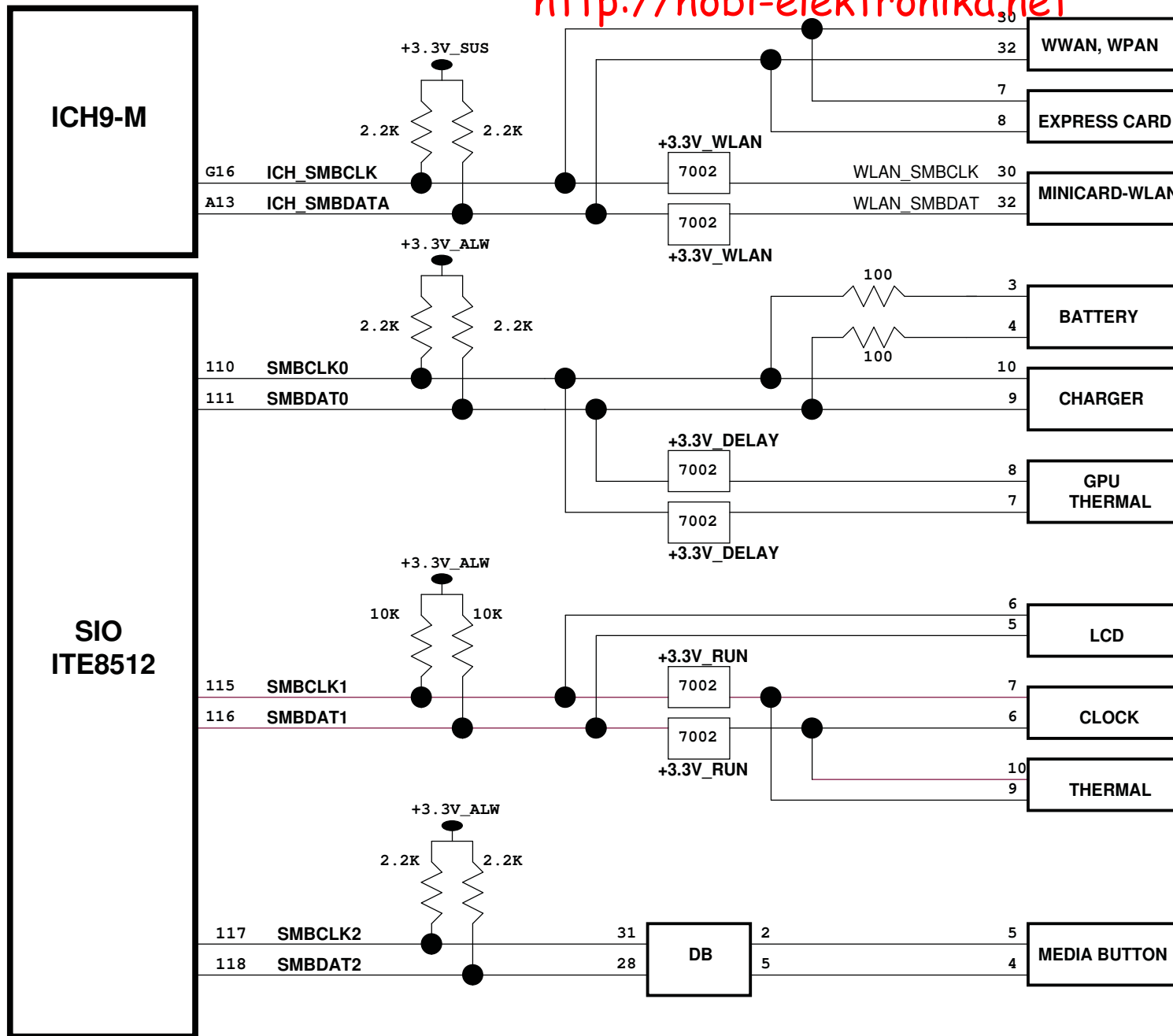
Reserve discharge path



Reserve discharge path



Title			Load Switch
Size	Document Number	Rev	
	RM2	3A	
Date:	Thursday, August 07, 2008	Sheet	55 of 59



POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH					
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH					
S5 (SOFT OFF) / M1	LOW	HIGH	LOW					
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH					
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW					

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	OFF	ON
S5 S4/AC	ON	OFF	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	ON

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD23	REQ#0 / GNT#0	PIRQB: 1394 PIEQC: Card reader

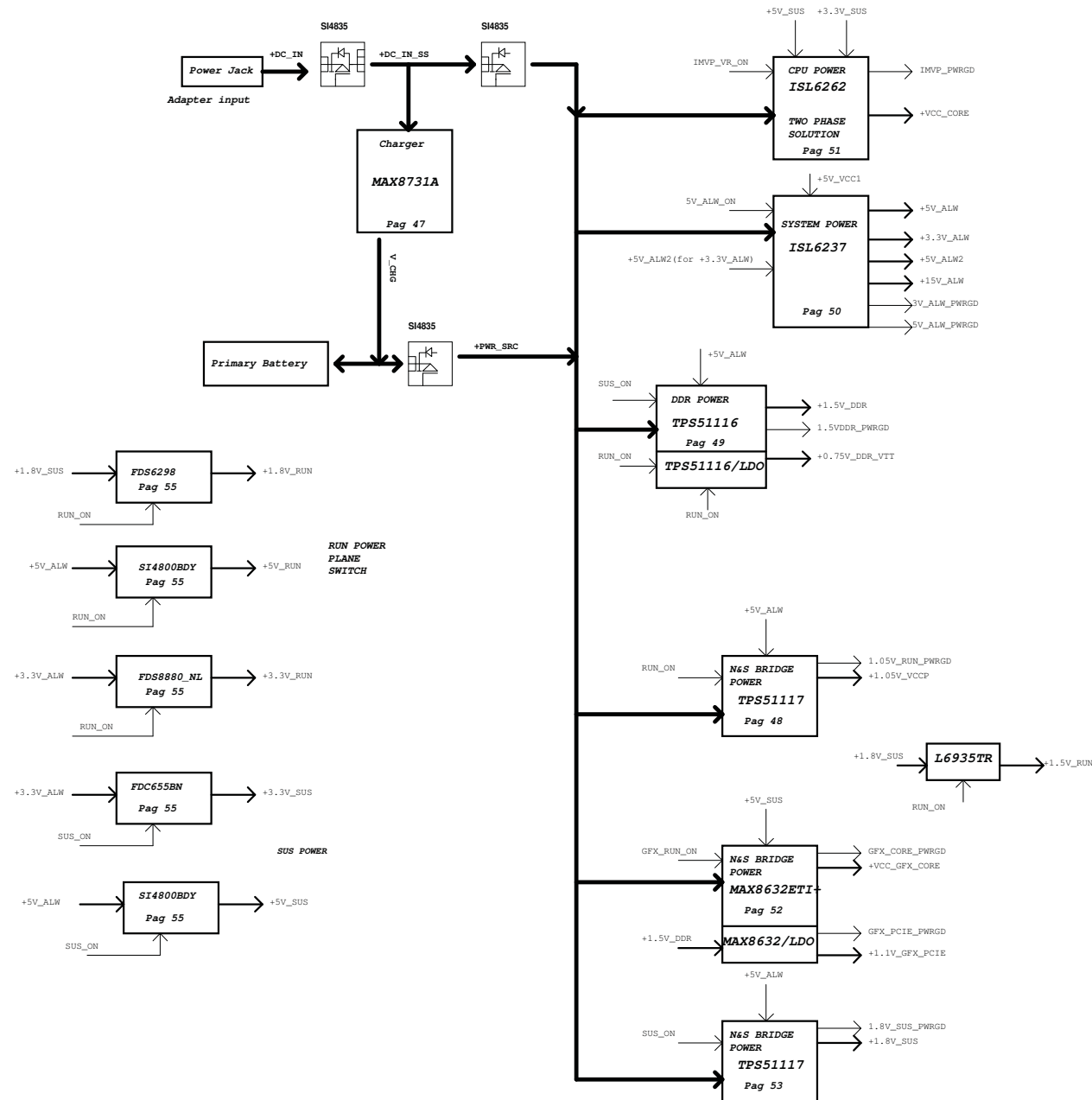
ICH9-M	USB PORT#	DESTINATION
	0	Side pair Top / left
	1	Side pair bottom / left
	2	Reserved
	3	Reserved
	4	WLAN
	5	Mini Card (WWAN)
	6	Mini Card (WPAN)
	7	Express Card
	8	USB W/ E-SATA port
	9	TV
	10	Reserved
ECE 5011	11	Camera
	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	LOM

RM1 Power Design Block Diagram

2008/03/014

<http://hobi-elektronika.net>



MODEL	REV	DATE	CHANGE LOG	Model		
				Page	FROM	TO
RM2 MB with MV	Pre	2008/03/05	Base on the schematic of "GM5-0226-3.DSN" CPU socket P3,P4 use RM1(NV) CPU socket DIMM from DDR2 to DDR3 P6,P15,P16 DIMM from DDR2 to DDR3 as RM1(NV) VRAM from DDR2 to DDR3 P23,P24 VRAM from DDR2 to DDR3 as RM1(NV) HDMI function P6,P25 delete parts of HDMI for UMA option, use RM1(NV) connector DP function P25 adding DP related part from RM1(NV), need to connect all signals LCD panel P6,P26 delete UMA option, use RM1(NV) connector & related parts CRT P6,P27 delete UMA option, use RM1(NV) connector and adding sync & SMBus ESD parts 1394 P29 use RM1(NV) connector Card Reader P30 use RM1(NV) connector, need re-connect signals Express Card P30 use RM1(NV) connector FLASH/ RTC/ CIR P32 use RM1(NV) parts, CIR need On/Off control (CIR-ON/OFF#) ? WPAN, WWAN, WLAN P33, P34 use RM1(NV) connector & nut, add WWAN LED as RM1(NV) USB & eSATA & TV P35 all the same with RM1(NV), need to re-connect all signals HDD & ODD (SATA) P11, P36 all the same with RM1(NV), delete SATA 4 for original 2nd HDD	1	2A	
				2	2A	
				3	2A	
				4	2A	
				5	2A	
				6	2A	
				7	2A	
				8	2A	
				9	2A	
				10	2A	
				11	2A	
				12	2A	
				13	2A	
				14	2A	
				15	2A	
	2008/03/06		KB/CCD/ UI P31, 37 use the same KB/CCD/Daughter Board with RM1, delete KSO17 & KSO18 & NUM_LED#, remember to re-connect all signals LED P31,P37,P38 delete original BATLED#; need to add BAT LED on Power Button board through DB; base on RM1's LED circuit & change Barrel LED from active low to active high FAN/THERMAL P39 use the same parts with RM1 Audio & Subwoofer & IB connector P40~42 follow original RM1's; remember to add LED function on IB connector & board and re-connect USB signals LAN P43, P44 use RM1's transformer & RJ45 & related parts	16	2A	
				17	2A	
				18	2A	
				19	2A	
				20	2A	
				21	2A	
	2008/03/10		Card Reader P28~30 use RM1(NV) schematic, need re-connect signals Express Card P28~30 use RM1(NV) schematic, need re-connect signals WPAN, WWAN, WLAN P33~34 use RM1(NV) schematic, need re-connect signals CRT P27 use RM1(NV) schematic, need re-connect signals remove reserved UMA circuit P05~P10 remove reserved UMA circuit with "FM7MB_A1A_0227_DIS.DSN" reference	22	2A	
				23	2A	
				24	2A	
				25	2A	
				26	2A	
				27	2A	
	2008/03/11		P31 depop Cap 1uF of "ITE8512IX_JX" for IT8512E/JX as ITE's review P26 pop 0 ohm for DPST support from GPU remove reserved UMA circuit P31 remove reserved UMA circuit with "FM7MB_A1A_0227_DIS.DSN" reference Codec update & WLP4.0 support from IDT suggestion P40,41, update Codec to "AL73C1X5B01(rev B1)"; add 2.2K & 220p for HP as WLP4.0 from IDT suggestion traces re-connect P19, P28, P30, P33, P34, P35, P37, P42	28	2A	
				29	2A	
				30	2A	
				31	2A	
	2008/03/12		P45, change power of ICH_PWRGD AND Gate from +3.3V_ALW to +3.3V_SUS for its glitch issue P9, add 0 ohm, move "+VCCA_MPLL_L" as Intel CRB(373319, Rev 1.0) P35, change eSATA traces name from SATA 2 to SATA 5 as GM5 P31, delete unused "USB_R_SIDE_EN#" Power circuit update P55, P56, rename Page 56 to Page 59; rename Page 55 to Page 56 P47~P55, update power circuit as "RM1 WITH MV_0312.DSN" DIMM from DDR2 to DDR3 P6,P8,P9 change +1.8V_SUS to +1.5V_DDR of NB for DDR3 from DDR2 GM5-0311 schematic update for issue fix P25, change HDMI_DE-1 serial Res. from 0 ohm to 10K P31, delete 1U for the backdrive issue of IT8512E/JX when initial	32	2A	
				33	2A	
				34	2A	
				35	2A	
				36	2A	
				37	2A	
				38	2A	
	2008/03/14		P47~P55, update power circuit as "RM1MB_M86_A1A_0312 FOR 256MB(MV)_A.DSN" P45, change Res of PWRGD logic power from 10K to 0 ohm VRAM from DDR2 to DDR3 P22~P24, update circuit as AMD M86 CRB "ref133-8.pdf"	39	2A	
				40	2A	
	2008/03/17		P9, change C1020 from 7343(ESR=18m) to 3528(ESR=45m) P47~P55, update power circuit as "RM1MB_M86_A1A_0314 FOR 256MB(MV)_2.DSN" P44, reserve EMI Cap for LAN signals HDMI & DP P19, P25, update circuit by referring AMD M86 CRB "ref133-8.pdf"	41	2A	
				42	2A	
				43	2A	
	2008/03/18		P6, no UMA, delete HDA for UMA HDMI P6, P15 PM_EXTTS#0 for DIMM1 event, PM_EXTTS#1 for DIMM2 event Intel review P3, P6, P8, P9, P14, P15, P17, P38, P51, update as Intel review list "Customer_schematics_review_DELL_0318.XLS"	44	2A	
				45	2A	
	2008/03/20		P34, add trace name of debug Mini card P47~P55, update power circuit as "RM2MB_M86_A1A_0318 FOR 256MB_1.DSN" P19,P25, DP update & refer XM1(Nike) schematic for DP power issue P11, delete IHDA for UMA HDMI P12,P17,P57~P60, add Mini PCI debug at P57, original P57~P59 renamed with plus one page P11, P35, P36, move SATA_TX Cap from ICH to device side as Intel CRB Spec P45, replace 1.25V_RUN_PWRGD by 1.8V_SUS_PWRGD; 1.5V_SUS_PWRGD by 1.5V_RUN_PWRGD P31, delete GPIO_ADAPT_TRIP_SEL & CIR_ON/OFF# & ADAPT_OC P48, P50~P53 update power circuit as "RM2MB_M86_A1A_0320 FOR 256MB_1.DSN"	46	2A	
				47	2A	
				48	2A	
				49	2A	
				50	2A	
				51	2A	
	2008/03/21		P31, BID update, change CHIPSET_ID1 to BID2; del DIS & UMA select ID update connector P/N & footprint as "Patrow_GGCL_EE_032108_Gur.xls" P35, change eSATA re-driver IC from 3201 to 3211 as FM7 P37, change pin definition of to DB connector as IM3 P31, replace WIRELESS_ON/OFF# by AUDIO_AVDD_ON at EC pin 108 P42, add Front Side LED at IB connector (MB side) pin 15~18 TV tuner P35, change CN19 from 4 to 10 pins for adding TV GPIO P37, change CN7 from 20 to 14 pins for deleting LED & adding TV GPIO USB charge P35, add "USB_CHG_DET#" at CN29 pin 8 for USB charge detect P31, add "USB_CHG_DET#" at EC pin 76 AMD review (update as "Dell_Patrow_RM2_M86XT_Review_Mar20_2008_Gur.doc") P25, change CN14 to pin14 from GND to test PAD; add 499 ohm to GND for AUX_SINK_P P27, +3.3V_RUN to +3.3V_DELAY for CRT RGB & DDC	52	2A	
				53	2A	
				54	2A	
				55	2A	
				56	2A	
				57	2A	
				58	2A	
				59	2A	
	2008/03/24		P31, add DIS & UMA select ID back ; add test PAD for NC pins P22~24, add MAA12 & MAB12 to reserve 32Mx32 GDDR usage P48~P50, P53, P55, update power circuit as "RM2MB_M86_A1A_0321 FOR 256MB_1.DSN" P29, change 1394_CONN for 1394 board, remember to update footprint Intel review P14, update as Intel review list "Customer_schematics_review_DELL_rev2.2_Gur.xls"			



QUANTA
COMPUTER

PROJECT : RM2

DOC. NO. 204

REV: 2A

ASSY: 31RM2MB0000

APPROVED BY : Roger Chen

CHECKED BY : Roger Chen

DRAWN BY : Guresu Lo

DATE : Mar., 24, 2008

SHEET 1 OF 4

MODEL	REV	DATE	CHANGE LOG	Model		
				Page	FROM	TO
RM2 MB with MV	Pre	2008/03/25	P56, remove original GM5 stitching Cap*5 & Spring*3 P46, update screw hole as mail "rm2 hole footprint (0325, 6:15PM)" P11, change as RM1's for layout space limitation update connector P/N & footprint as "Paltrow_GGCL_EE_032508_Gur.xls" TV tuner module P35, change bulk Cap of TV power from 1U to 10U P35, as TV tuner vendor suggestion, exchange GPIO1 & 2 ; exchange USB signals ; connect pin 9 & 10 to GND	1	2A	
				2	2A	
				3	2A	
				4	2A	
		2008/03/26	P18~P22, change AMD GPU from M86 LP to M86-ME XT A11 P15, P16, delete stitch Cap used for RM1 layout P47~P55, update power circuit as "RM2MB_M86_A1A_0325 FOR 256MB_1.DSN" P09, add trace name "+VCCA_SM" for layout LAN from 5787 to 5784 P43, P44, update from 5787 to 5784, check support items	5	2A	
				6	2A	
				7	2A	
				8	2A	
		2008/03/27	All page, change CC0402-FM6 to CC0402; RC0402-FM6 to RC0402; change R738, R741, R748 from CC0402-C to RC0402-C P34, change SIM card back as RM1's P20, add trace name +VDDCI P19, update VRAM table & set configuration to 1111 P31, delete R1134 & "ADP_OC" for "IINP" for double reserved 0 ohm Biometric de-feature P12, P37, del USB 10, check re-arrange pin of DB connector	9	2A	
				10	2A	
				11	2A	
				12	2A	
		2008/03/28	P47~P55, update power circuit as "RM2MB_M86_A1A_0327A FOR 256MB_1.DSN" P22~P24, reserve MAA12, MAB12, CSAx_1# & CSBx_1# for 32Mx32 GDDR3, default set Non Merged & 1CS mode Biometric de-feature P28, del USB 10 & power of Biometric for de-feature, and re-arrange pin H/P HDMI failure, follow "FM6-HDMI DDC test issue 0326.ppt" P25, change D47 to 0_0805, change PU Res to 2.2K from 6.8K P55, H/P HDMI failure, change R1261 from 1K to 47 ohm, and pop R1261 & Q121 for back drive solution	13	2A	
				14	2A	
				15	2A	
				16	2A	
		2008/03/31	P31, P43, change "LAN_DISABLE#" to "LAN_DISABLE" for high active P46, delete H23, H24, H27, H28, H29, H30 P52, update power circuit as "RM2MB_M86_A1A_0328 FOR 256MB_1.DSN" P22, change GPU thermal SMBus from 2 to 0 for MMB FW ISSP Flash support P19, R23, R24 update VRAM table & P/N to set Hynix(16Mx32) as default Change by layout requirement P15, P16, swap as "a788.1257a_ddr_swap_0331.xls" P23, swap as "a788.1257a_vrma_swap_0329.xls" Silego review P17, update as "RM2_Silego Suggestion.pdf" P17, delete R927, double reserved PD of PCI_ICH	17	2A	
				18	2A	
				19	2A	
				20	2A	
				21	2A	
				22	2A	
		2008/04/01	P33, P34, change footprint of Mini Card nut from "MININUT-5028HB25" to "h-tc138bc236d55p2" P38, change BAT_LED Power from +5V_ALW2 to +3.3V_ALW ; add L-C filter (R-C) as EMI request P25, reserve level shift for HDMI as HDMI issue on H/P Intel review P14, update as Intel review list "Customer_schematics_review_DELL_rev2.3_Gur.xls" IDT review P41, change C1456, C1457, C1458 and C1459 to 270P from 220P; change C675, C676, C718, C719 from 2.2U to 10U AMD review P23, P24, update to 2CS, non-Merged mode for 32Mx32 GDDR3 change LAN to 5784 only P43, P44, delete option for 5787, use 5784 only	23	2A	
				24	2A	
				25	2A	
				26	2A	
				27	2A	
				28	2A	
		2008/04/02	P12, P13, swap as "a788.1257a_swap_0402_Gur.xls" P35, change pin definition of CN19 for cable making process concern P19, update VRAM table & config default GDDR3 is Samsung 32Mx32 ; VRAM size from 256M to 512M as default Ricoh review P29, delete reserved C839 (0.01u), not necessary	29	2A	
				30	2A	
		2008/04/03	P1, update Block Diagram update connector P/N & footprint as "Paltrow_GGCL_EE_040308_Gur.xls" P35, update library of RF Jack	31	2A	
				32	2A	
		2008/04/07	P22~24, delete reserved MAA12/B12 for 2CS mode only. P43, connect SUPER_IDDO to GND directly P26, delete Pin 59~62 of CN2 for footprint change P31, change PU of "BREATH_LED#" & "BAT_LED#" from +5V_ALW2 to +3.3V_ALW Intel review P09, delete reserved +1.5V circuit, connect +VCCD_TVDDAC directly to GND ; delete reserved R798 PD Res of +VCCD_QDAC Broadcom review P43, update as "RM2_schematic_review_0407_Gur.doc"	33	2A	
				34	2A	
				35	2A	
				36	2A	
				37	2A	
		2008/04/08	P13, 25, 29, 35, swap as "a788.1257a_swap_0407.xls" P34, update library as SIM card pin definition P48, 49, 50, 52, 53, 55, update power circuit as "RM2MB_M86_A1A_0407 FOR 512MB_1.DSN" P22, P50, add MOS to shutdown system 3/5V by GPU thermal trip P46, P56, P57, P60, delete P56 "EMI CAP (blank page)", move P57 (Mini PCI) to P56 and P60 (SMBus) to P57; add 6 spring at P46 P29, P33, P34, P46, update connector P/N & footprint as "Paltrow_GGCL_EE_040808_Gur.xls"	38	2A	
				39	2A	
				40	2A	
				41	2A	
		2008/04/09	P29, change CN35 library (to 1394 board) from 4 to 8 pins MMB ISSP support P31, P37 reserve circuit for MMB ISSP support	42	2A	
				43	2A	
				44	2A	
		2008/04/10	P23, P24 swap as "a788.1257a-vrma-swap-0410_Gur.xls" P35, add hi-pot Cap for RF signal P46, change from h-236d118p2 to h-tc197bc236d118p2 Internal review P48, P50, P52, change 3V/5V_ALW_PWRGD to GFX_PWRGD for PWRGD monitor change P14, del reserve +1.5V_RUN and 0 ohm*1 & 0.1u*1 P23, P24, pop R1299, R1302, R1307, R1310 for 32Mx32 P28, del R605, connect CLK_PCI_PCCARD directly P36, del R583, R474 for double PU to +3.3V_SUS with ICH P01, P57, update Block Diagram & SMBus Block	45	2A	
				46	2A	
				47	2A	
				48	2A	
				49	2A	
				50	2A	
		2008/04/11	P37, IDT check, change series Res of DMIC_CLK from 0 to 22 ohm P17, add bead on BSEL0 & BSEL2 for EMI noise of 48M & 14M P47, 48, 49, 50, 52, 54, update power circuit as "RM2MB_M86_A1A_0410A FOR 512MB_1.DSN" P27, update library of CN7 to add shield GND P46, delete R1220 0 ohm to connect directly; change U87 & U92 from 74AHCT1G08GW to 74AHCT1G08GW for working power issue, AHCT is 4.5~5.5V, AHC is 2~5.5V P36, delete reserved 0_0805 to +5V_RUN of HDD & ODD power for layout concern Intel review P14, change back to 1U_0603_X5R from 0.1u_0402_X7R for V5REF decoupling Cap; change series Res from 100 to 10 ohm for V5REF_SUS Add temporary DP dongle support circuit for DP function test P25, add temporary DP dongle support circuit for DP function test at PT stage	51	2A	
				52	2A	
				53	2A	
				54	2A	
				55	2A	
		2008/04/14	P47, 49, 52, 53, 55, update power circuit as "RM2MB_M86_A1A_0411 FOR 512MB_1.DSN" P29, update connector P/N & footprint as "Paltrow_GGCL_EE_041108_Gur.xls" Delete all test PAD which footprint is "PAD-VIA20D10A25TMP"; T65,T70,T71,T72,T73,T74,T75,T76,T83,T84,T85,T86,T87,T88,T89,T90,T127,T128,T129,T130,T131,T132,T133,T134,T135,T136,T149,T150,T151,T152,T153,T154,T155,T156,T160,T161,T163,T164,T175,T176,T177,T178,T179,T180,T181,T182,T183,T184,T185,T186,T187,T188,T189,T190,T191,T192,T193,T194,T196,T197,T198,T199,T200,T201,T204,T205,T266,T285,T286,T287,T288,T289 P19, P36 delete repeat Res, R977 (series 0 ohm) with Page 31; R1181 (PU, 100K) with Page 38 GM5 update (0411 schematic) P3, update BSEL table P6, del R751 to prevent back driver(from +5V_ALW2 to +1.05_VCCP) when stuffed	56	2A	
				57	2A	
				58	2A	
				59	2A	
		2008/04/15	P28, change IDSEL from PCI_AD23 to AD17 as FM7 & GM5 P41, pop 100K, depop 0 ohm for "AUD_AMP_MUTE#" as FM7 & GM5 Intel review P03, Intel review, change R660 from 68 to 56 ohm as check list 2.0 P06, add circuit for SM_PWROK of DDR3 Broadcom review P43, BCM review, delete R1185 & R1187 by power directly connecting to save cost			



MODEL	REV	DATE	CHANGE LOG	Model		
				Page	FROM	TO
RM2 MB with MV	Pre	2008/04/16	P17, remove bead of BSEL0 & 2 for layout space concern	1	2E	
		2008/04/17	P1, update Block Diagram P29, update library of CON1 to delete pin 48 & 49 (to GND) P51 (alter rename), pop PQ10 & PQ11, depop PQ1 & PQ2 Rename	2	2A	
				3	2D	
				4	2B	
		2008/04/18	P48, update power circuit as "RM2MB_M86_A1A_0417 FOR 512MB_1.DSN" P31, BOM change for RP23 from "CJ310042N02" to "CJ310042N11" P32, delete RTC battery "UBM2" for assembly process change	5	2D	
				6	2D	
	2A(PT)	2008/04/18	First Release All pages, change revision form 1A to 2A for RM2 start from PT stage P44, change footprint of RJ45 from "rj45-2006250-13p-v-rm2" to "rj45-2006250-13p-h-rm2."	7	2D	
				8	2D	
	2B(PT)	2008/04/23	P01, change Ver. from 2A to 2B; adding Dell PWA, PWB, SCH P/N P26, delete Pin 57, 58 of CN4 for new footprint Update for AMD PowerPlay P52, update power circuit as "RM2MB_M86_A1A_0418A FOR 512MB_1.DSN" P19, pop R287 and separate "GFX_CORE_CNTRL" to "GFX_CORE_CNTRL0" & "GFX_CORE_CNTRL1"	9	2D	
				10	2D	
				11	2D	
		2008/04/24	P48, update power circuit as "RM2MB_M86_B2B_0423 FOR 512MB_1.DSN" P20, change reserved U10 from "74AHC1T1G08GW" to "74AHC1G08GW" for logic power level issue	12	2D	
		2008/04/28	P4, pop C558 & depop C562 for mechanical interference concern	13	2E	
		2008/05/02	Badge LED don't light enough issue P38, change R112 from 100K (CS41002JB20) to 220 (CS12202JB24) ; change R91 from 100K (CS41002JB20) to 150 (CS11502JB22) ; change R416 & R418 from 220 (CS12202JB24) to 0 ohm (CS000002JB38)	14	2D	
	2C(PT)	2008/05/14	P1, change ver. from 2B to 2C P14, change L15 from "CV-1008MZ14" to "CV-1001TN09" P35, delete bypass Res. of eSATA MMB ISSP backdrive issue P37, reserve a MOS for +MMB, PWR backdrive when ISSP LAN 10M & 100M LED reversed and LAN footprint update P44, exchange CN15 pin 11 & 13 for LAN 10M & 100M LED reversed; change RJ45 footprint from "rj45-2006250-13p-h-rm2" to "rj45-2006250-13p-v-rm2."	15	2E	
				16	2A	
				17	2A	
		2008/05/29	P46, change H14, H15, H19, H20 from "h-c236d197p2" to "H-C236D158P2"; change from "h-tc197bc236d118p2" to "H-T295X280B236D118P2"; change H30 from "h-c157d157n" to "H-C197D118P2" for IB cable cost down from coaxial to FFC type P42, change CN5 from 30 to 32 pin for cable cost down from coaxial to FFC type	18	2A	
				19	2B	
				20	2E	
	2D(ST)	2008/06/16	P1, change ver. from 2C to 2D P31, pop R637 & depop R640 for BID update from 1000 to 1001 P11, change C622 & C623 from 10pF to 15pF as TXC's validation. P40, change U40 from AL73C1X3B03 for Rev. from B2 to C1. P43, change +2.5V_L0M to +1.2V_VDDC_IO & LAN_REGCTL25 to LAN_REGOUT12_IO to avoid confusion. P46, change PV4-PV6 from FDZD3002010 to FDRM2002010 as ME's request S3S5 leakage P28, R31, depop R654 for S3 leakage issue, and supplier indicate it's no need for R5C833; pop R652 as GM5, no leakage concern as test P49, change PR121 PU from +3.3V_ALW to +3.3V_SUS for S5 leakage issue P38, change design, add U52, R714 & U53, delete Q11, R416 & R418 Derating issue P9, change L70(91nH, 1.5A) to 0_0805	21	2E	
				22	2A	
				23	2A	
				24	2A	
				25	2E	
				26	2D	
		2008/06/19	P42, change CN5 from 32 FFC to 32 coaxial connector for IB cable change P35, del JP1, FS1, JP2, FS3 for direct USB SW power P35, del C520 & add R715-R718 & change GND to RF_GND for TV layout ; del CN2 to disable internal antenna support P46, depop PV2 & PV4 as ME request XPS_Premium_LED colors behavior v3 3.xIs P38, depop Q16, R100, U2, R109 of Power button board Amber LED as "XPS_Premium_LED_colors_behavior v3 3.xIs" MMB ISSP fail P31, change RP22 from 2.2K to 10K for ISSP fail Power issue (update as "RM2MB_M86_D2D_0616 FOR 512MB_1.DSN") P47, Change P018,P025 to SI4835DDY-T1-E3 due to SI4835BDY-T1-E3 EOL; Change PL4 to SIL104R-5R8B due to SIL104R-5R8PF EOL; Change PR47 to short jumper; Remove 0R PR58 P48, Change PR97 from 15.8K to 13.3K for WCEPTA; Remove PR65 and PR64, directly connect pins to GND; Change PR31 to short jumper P49, Remove PR65 and PR64, dire GND to connect pins to GND; Depop PC56,PC57; Change PR46 from 15.4K to 11.32K for WCEPTA; Change PR56 to short jumper; Change PL5 to SIL104R-1R5B due to SIL104R-1R5PF EOL P50, Remove 0R PR173; Change PR157 to short jumper; Remove 0R PR164; Remove 0R PR165 and PR166; P51, Remove 0R PR11,PR13,PR15,PR16,PR18,PR19,PR22,PR30; Change PR84 to 4.02K; Change PR91 to short jumper; Andy_0617: Depop PC15,PC16 P52, Remove 0R PR125; Change PR113 to 82K; Change PR105 to 61.9K; Change PR126 to short jumper P53, Change PR61 to short jumper; Change PL7 to SIL104R-1R5B due to SIL104R-1R5PF EOL P54, Change to SI4835DDY-T1-E3 due to SI4835BDY-T1-E3 EOL	27	2D	
				28	2D	
				29	2A	
				30	2D	
				31	2D	
				32	2A	
	2008/06/20	2008/06/20	EMI Solution for Power as "RM2MB_M86_D2D_0619 FOR 512MB_1.DSN" P47, Add FL8 for EMI solution P50, Change PC176 from 0_1u to 1u by FEA suggestion P54, Add PC194,PC195,PC196 for EMI solution Derating issue P9, as EMI request, change from R713 0_0805 to L70 "CX31P121001(120 ohm, 3A)"	33	2A	
				34	2E	
				35	2E	
				36	2A	
				37	2E	
				38	2E	
	2008/06/24	2008/06/24	P31, del R623 & "ICH_PME#" to connect "PLTRST#" to R652; add PD 1K for RESET_OUT# P46, depop PV3, PV5 & PV6 as ME request; add PAD PV7, PV8 & PV9 & hole H34; change screw hole from " " " to " " " for H26, H33, G23, H32, H21, H10, H7, H2, H1, H9, H22, H11, H18, H30 & H8 P41, change R286 from 0_0603 to 0_0805, depop R83, R301, R110, R543, R450 & R544 P38, add pin 4 & 5 for CN3 & CN10 to connect to GND P42, change CN5 from 32 to 30 pin & change pin assignment for cable manufacture P30, change CN12 from "EXPCARD-1CX41101-PL-26P-L" to "expcard-1cx41101-pl-26p-l-rm2" P54, change CN24 from "DFHD09MR017(SUYIN)" to "DFHD09MR024(FOXCONN)" as ME's information P9, P11, P13, P20, change footprint from RC0402-C to RC0402 or CC0402-C to CC0402 for R247, R496, R489, R524, R525, C726, C728, C741, C624, C689 P3, depop R56 for abnormal H_RESET# Combo USB EA fail - change USB Bus SW P35, change U17 from "ALU5S31003" to "AL004907000"; del R345 & add C520 for support item NB(Cantiga) & SB(CH9M) P/N change P5-P14, change NB from "AJQ0T780T08" to "AJSLB970T13(ver B3)"; change SB from "AJQ0T090T06" to "AJSLB8Q0T16(ver A3)" For 2nd source BOM creation problem P9, P26, P27, P38, P44, change Q83 from "BAM06550025" to "BAM06550025"; change D17 from "BCRB500VZ02" to "BC010K45004"; change D10 from "BC000501Z09" to "BC010K45004"; change D4 & D7 from "BC000751Z05" to "BC000340033"; change Q20 from "BA001140Z08" to "BA001140001"	39	2A	
				40	2D	
				41	2E	
				42	2E	
				43	2D	
				44	2D	
	2E(ST)	2008/07/10	P1, change ver. from 2D to 2E P47, update power circuit as "RM2MB_M86_D2D_0624 FOR 512MB_1.DSN" P13,P51 depop PR1 & pop R159 for change IMVP_PWRGD PU from +3.3V_SUS & +3.3V_RUN P42, change back CN5 from 30 pin coaxial to 32 pin FFC & change pin assignment for FFC implement; add CN32 for additional AGND P20, add two more 10uF for +VCC_GFX_CORE ripple P15,P34,P35, change ESD1-3 from ALSRV054011 to AL000504000 for EOL concern P34, change SIM card connector to push-push type, CN26 from DG006001404 to DG006000020 P25, reserve R723 for option when remove DP dongle support ST Internal Doc, 0703-1 update P48, change PU3 from AL009194000 to AL009024000. P38, change R127 from 220 to 1K; R90,R107,R101,R119 from 220 to 3 3K as IM3 XPS_Premium_LED colors behavior v3 7.xIs (no Amber LED & change indicator on power button LED) P37, del "BAT_LED_INT" as "XPS_Premium_LED colors_behavior v3 7.xIs" P38, change power of R113 & U31 from +5V_ALW2 to +5V_SUS, no change indicator ; del Q16, R100, U2, R109 of Power button board Amber LED Subwoofer overload & band filter EQ is main SPK EQ issue P41, circuit change for main SPK EQ as "PALTROW EQ CIRCUIT rev 3.pptx" P42, circuit change for subwoofer overload & band filter issue as "PALTROW EQ CIRCUIT rev 3.pptx" add KB LED detect pin P13, del L59 & add "KB_LED_DET" P37, del +15V_ALW, add KB_LED_DET & R721, R722	45	2A	
				46	2E	
				47	2E	
				48	2E	
				49	2D	
				50	2D	
				51	2E	
				52	2D	
				53	2D	
				54	2D	
				55	2A	
				56	2A	
				57	2A	
				58	2A	
				59	2A	
	2008/07/14	2008/07/14	P25, change DP connector footprint from "DP-47644-0001-20P-L-H" to "dp-rsd-47644-001-20p-l-h" P20,P21, add "-C" on footprint for C867,C868,C427,C417,C405,C395,C401,C379,C367,L38,C356,C358,L39,C389 P46, update library for " " " for H26, H33, G23, H32, H21, H10, H7, H2, H1, H9, H22, H11, H18, H30 & H8 debug port code "52" issue when "MEDIA_INT#" isn't high at system boot P37, add R724, move PU of "MEDIA_INT#" to MB side reserve Hall IC on MB side for option & study P37, add U54, C869, R726 & reserve R725 for study of Hall IC on MB			



PROJECT : RM2

DOC. NO. 204

REV: 2E

ASSY: 31RM2MB0000

APPROVED BY : Roger Chen

CHECKED BY : Roger Chen

DRAWN BY : Guresu Lo

DATE : Jul., 14, 2008

SHEET 3 OF 4



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