

# QL1 BLOCK DIAGRAM

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01

## PCB STACK UP 6L HDI

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : BOT

## POWER

CPU Core  
RT8152D P29

VCCP 1.05V  
RT8209 P27

DDR Power  
RT8207 P28

SYSTEM 5V/3V  
RT8206 P26

Charger  
ISL6251A P30

Discharge  
P31

1.5V  
RT9025 P27

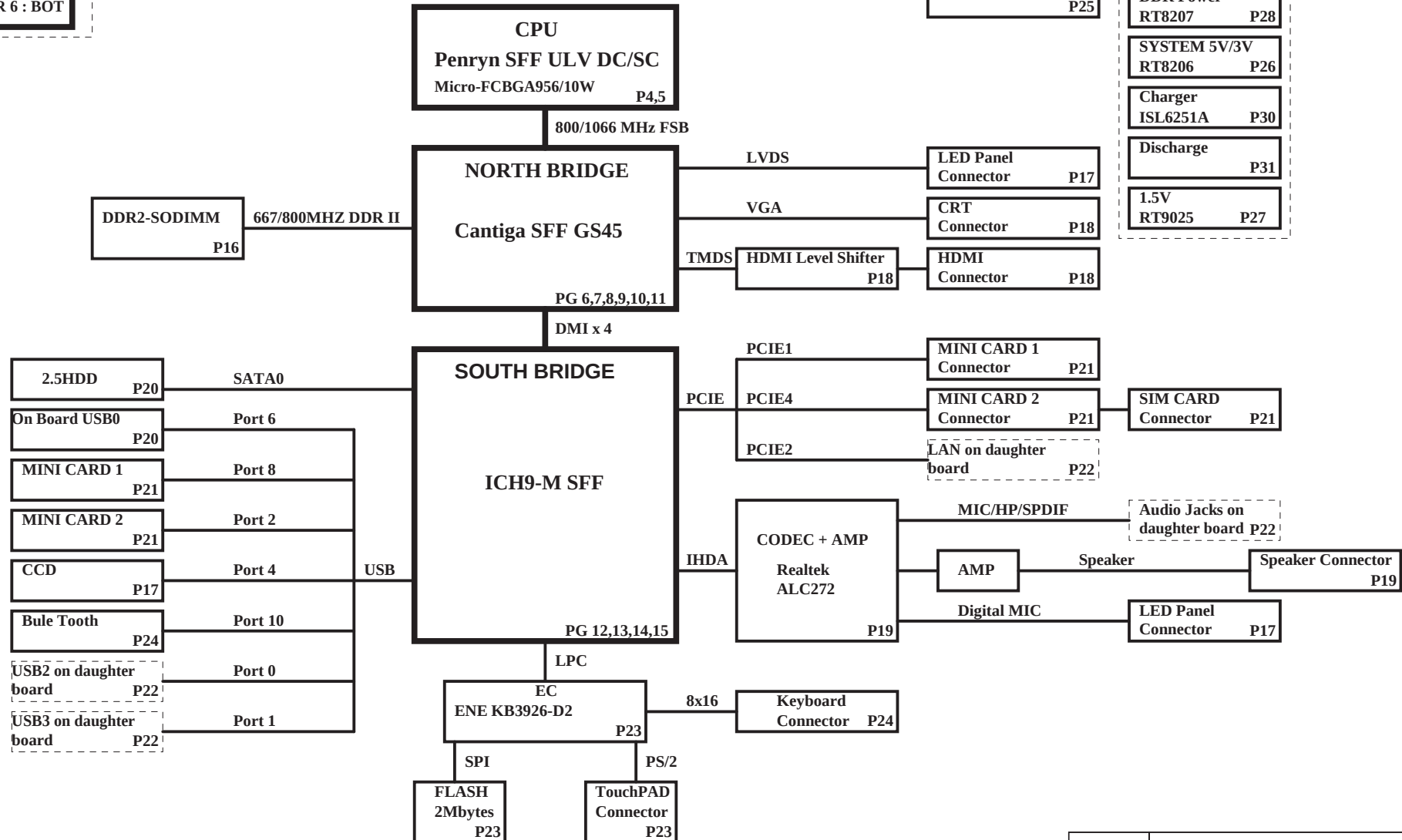
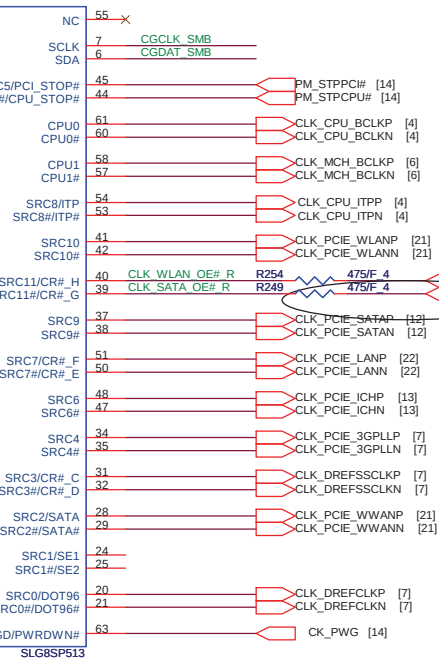
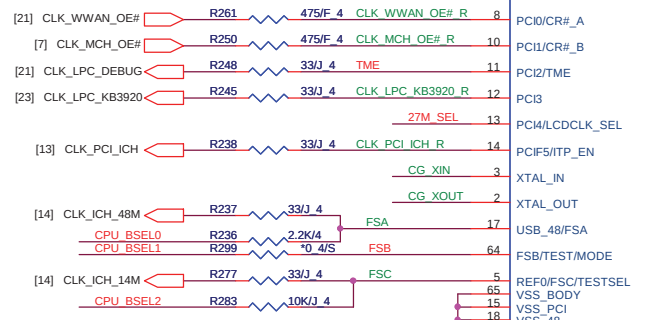
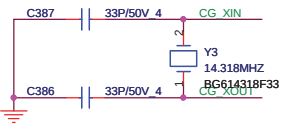


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| 06-11 | Cantiga North Bridge        |
| 12-15 | ICH9-M South Bridge         |
| 16    | DDR2 SO-DIMM                |
| 17    | LED Panel/CCD               |
| 18    | CRT / HDMI                  |
| 19    | Azalia ALC272               |
| 20    | USB/ HDD                    |
| 21    | MINI PCIE(WLAN/WIMAX/3G)    |
| 22    | LED/B2B conn/ HOLE          |
| 23    | KB3926/ROM                  |
| 24    | KB/BT/TPD                   |
| 25    | FAN/THERMAL                 |
| 26    | SYSTEM 5V/3V (RT8206)       |
| 27    | 1.05V (RT8209)/1.5V         |
| 28    | DDR 1.8VSUS(RT8207)         |
| 29    | VCore( RT8152D)             |
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| 32    | MODIFY LIST                 |
|       |                             |
|       |                             |
|       |                             |
|       |                             |
|       |                             |
|       |                             |
|       |                             |
|       |                             |
|       |                             |

Clock Generator (CLK)



CK505 QFN64

|         |                   |             |
|---------|-------------------|-------------|
| ICS     | ICS9LPRS355BKL    | ALPRS355000 |
| Silego  | SLG8SP513VTR      | AL8SP513000 |
| Realtek | RTM875N-606-VD-GR | AL000875000 |

Change U18 footprint 8/20

0=overclocking of CPU and SRC Allowed  
1 = overclocking of CPU and SRC not Allowed

TIME

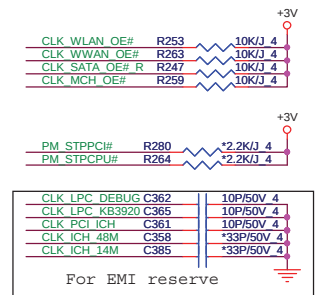
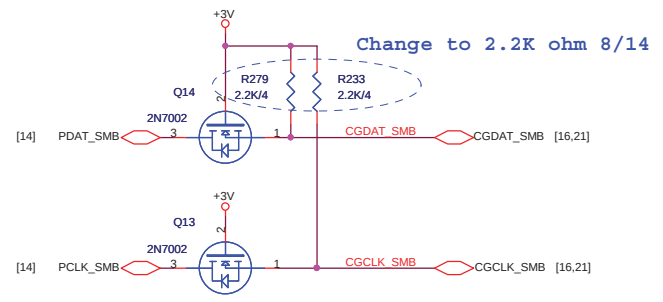
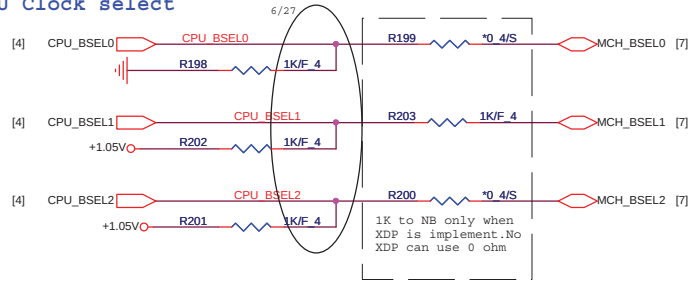
| ITP_EN | Pin 53/54    |
|--------|--------------|
| 0      | SRC_0/SRC_0# |
| 1      | ITP/ITP#     |

| LCDCLK_SEL | Pin 20/21      | Pin 24/25      |
|------------|----------------|----------------|
| 0          | DOT_96/DOT196# | LCDCLK/LCDCLK# |
| 1          | SRC_0/SRC_0#   | 27M/27M_SS     |

| FSC | FSB | FSA | CPU (MHz) | SRC (MHz) | PCI (MHz) | REF (MHz) | DOT96 (MHz) | USB (MHz) |
|-----|-----|-----|-----------|-----------|-----------|-----------|-------------|-----------|
| 0   | 0   | 0   | 266.6     | 100.0     | 33.3      | 14.318    | 96.0        | 48.0      |
| 0   | 0   | 1   | 133.3     | 100.0     | 33.3      | 14.318    | 96.0        | 48.0      |
| 0   | 1   | 0   | 200.0     | 100.0     | 33.3      | 14.318    | 96.0        | 48.0      |
| 0   | 1   | 1   | 166.6     | 100.0     | 33.3      | 14.318    | 96.0        | 48.0      |
| 1   | 0   | 0   | 333.3     | 100.0     | 33.3      | 14.318    | 96.0        | 48.0      |
| 1   | 0   | 1   | 100.0     | 100.0     | 33.3      | 14.318    | 96.0        | 48.0      |
| 1   | 1   | 0   | 400.0     | 100.0     | 33.3      | 14.318    | 96.0        | 48.0      |
| 1   | 1   | 1   |           |           |           |           |             |           |

Reserved

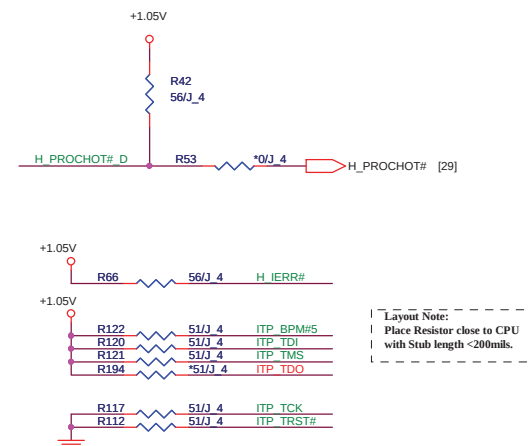
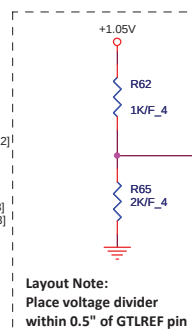
CPU Clock select



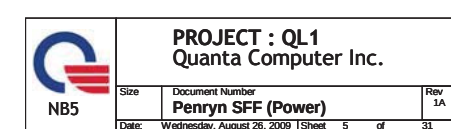
**PROJECT : QL1**  
Quanta Computer Inc.

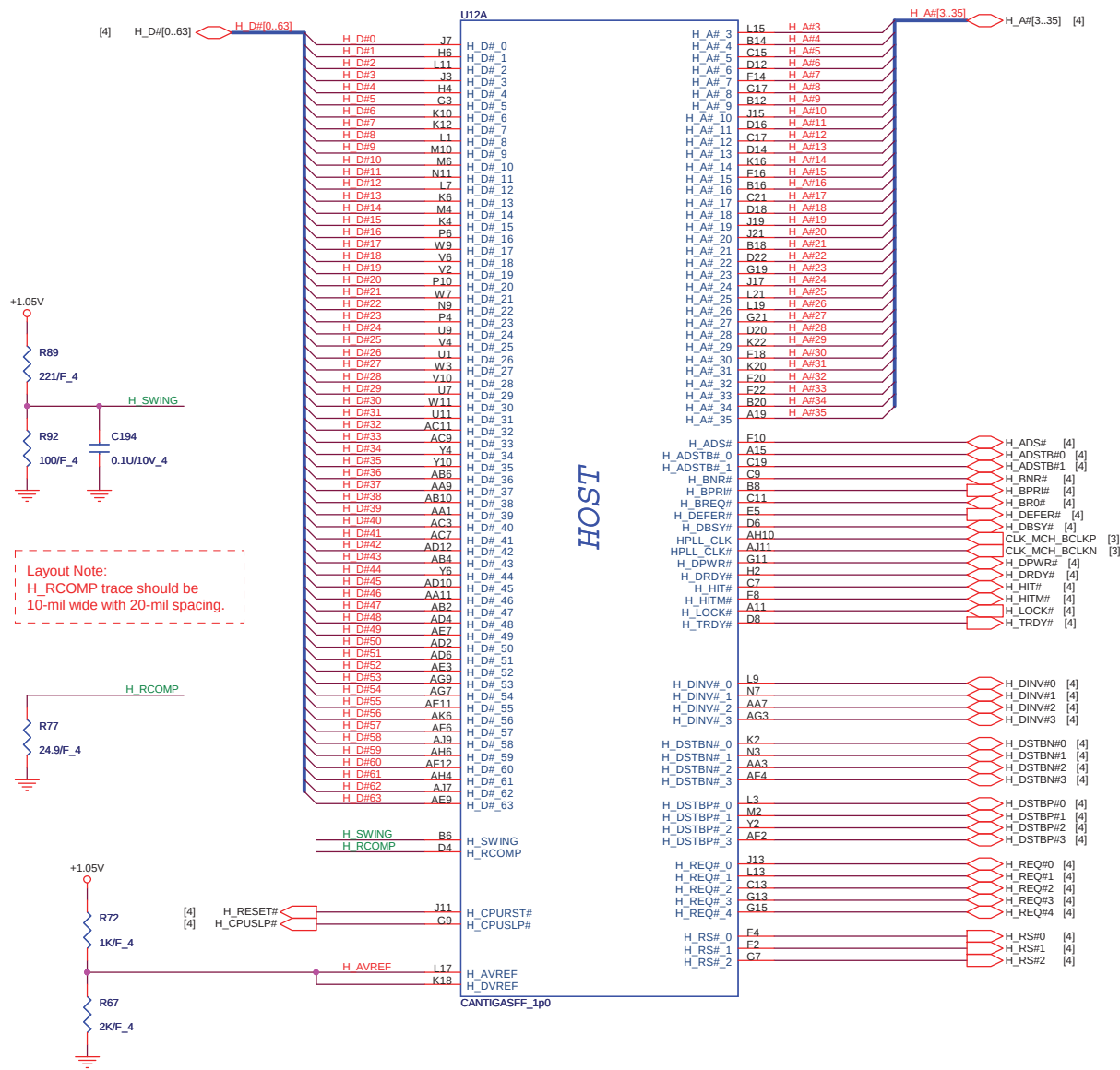
NB5

|                        |                            |               |
|------------------------|----------------------------|---------------|
| Size                   | Document Number            | Rev 1A        |
| <b>CLOCK GENERATOR</b> |                            |               |
| Date:                  | Wednesday, August 26, 2009 | Sheet 3 of 31 |



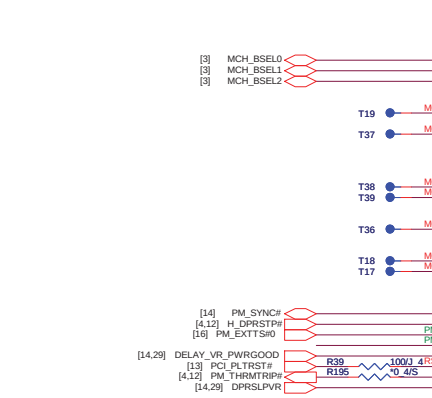
<http://hobi-elektronika.net>



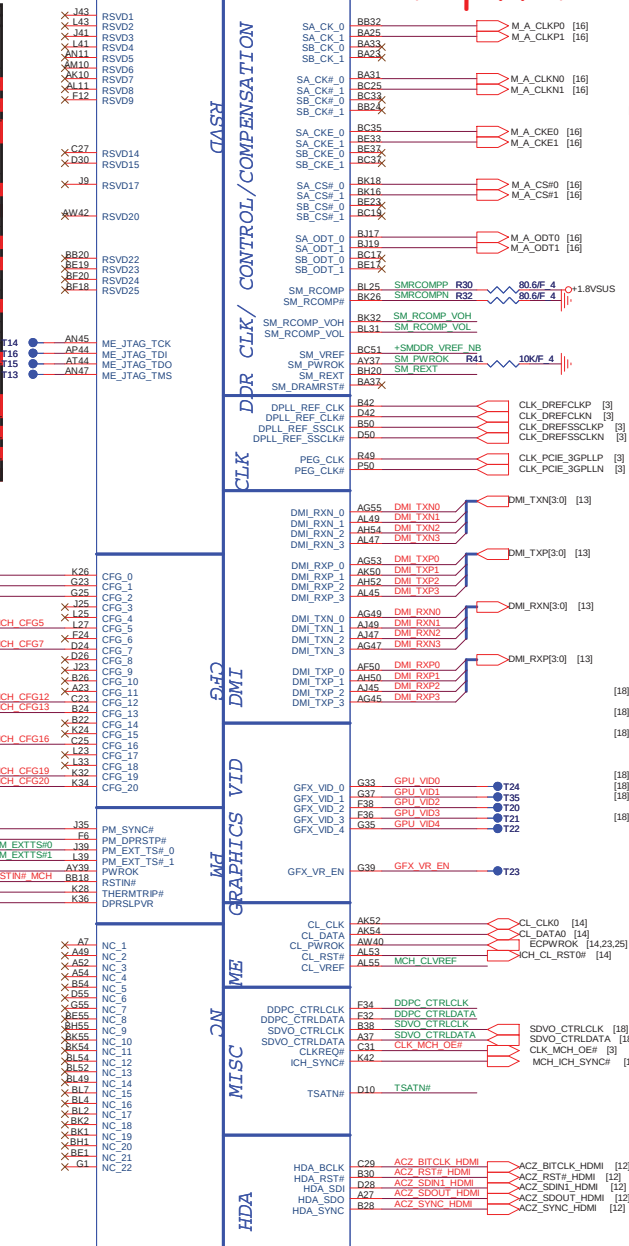
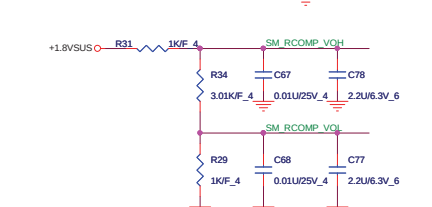
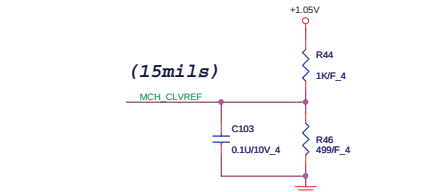


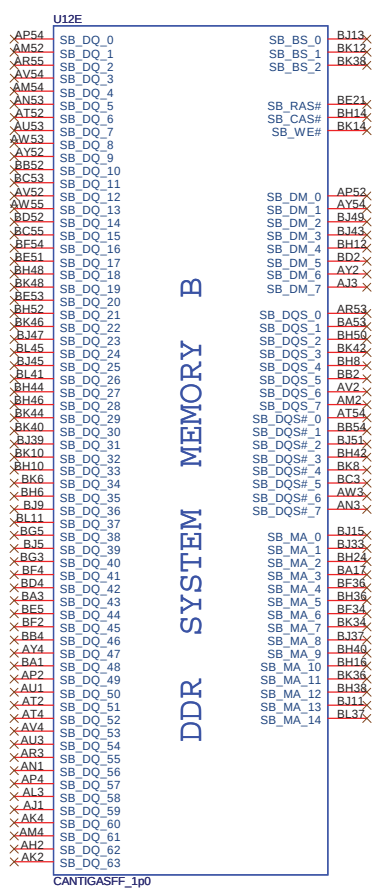
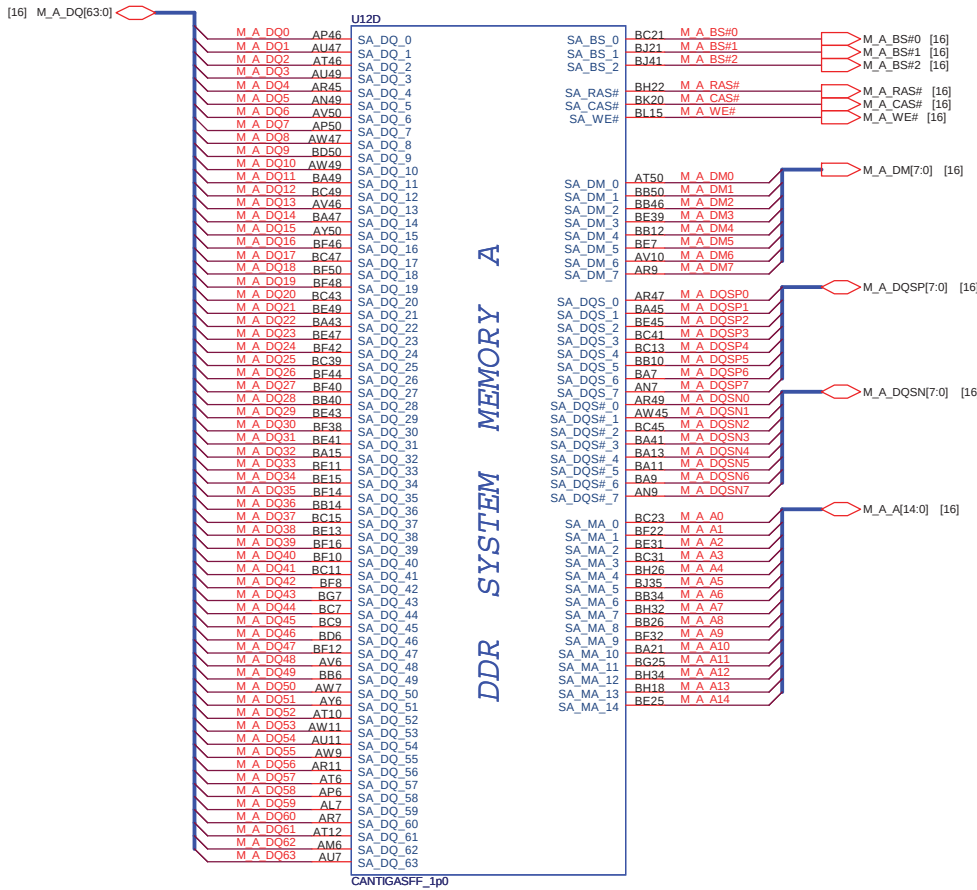
| Pin Name      | Strap Description                                                    | Configuration                                                                                                                                                   |
|---------------|----------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG2:0        | FSB Frequency                                                        | 000 = FSB1066<br>010 = FSB800<br>011 = FSB667<br>Other = Reserved                                                                                               |
| CFG4:3        | Reserved                                                             |                                                                                                                                                                 |
| CFG5          | DMI x2 Select                                                        | 1 = DMI x4<br>0 = DMI x2                                                                                                                                        |
| CFG6          | ITPM Host Interface                                                  | 1 = ITPM disabled<br>0 = ITPM enabled                                                                                                                           |
| CFG7          | Intel Management Engine Crypto TLS cipher suite with confidentiality | 1 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality                                                          |
| CFG8          | Reserved                                                             |                                                                                                                                                                 |
| CFG9          | PCIe Graphics Lane                                                   | 1 = Normal operation : Lane Numbered in Order<br>0 = Reverse Lanes                                                                                              |
| CFG10         | PCIe Loopback enable                                                 | 1 = Disabled<br>0 = Enabled                                                                                                                                     |
| CFG11         | Reserved                                                             |                                                                                                                                                                 |
| CFG12         | ALLZ                                                                 | 1 = Disabled<br>0 = ALLZ mode enabled                                                                                                                           |
| CFG13         | XOR                                                                  | 1 = Disabled<br>0 = XOR mode enabled                                                                                                                            |
| CFG14         | Reserved                                                             |                                                                                                                                                                 |
| CFG15         | Reserved                                                             |                                                                                                                                                                 |
| CFG16         | FSB Dynamic ODT                                                      | 1 = Dynamic ODT enabled<br>0 = Dynamic ODT disabled                                                                                                             |
| CFG17         | Reserved                                                             |                                                                                                                                                                 |
| CFG18         | Reserved                                                             |                                                                                                                                                                 |
| CFG19         | DMI Lane Reversal                                                    | 1 = Reverse Lanes<br>0 = Normal operation : Lane Numbered in Order                                                                                              |
| CFG20         | Digital DisplayPort (SDVO/DP/HDIM) Concurrent with PCIe              | 1 = Digital DisplayPort (SDVO/DP/HDIM) and PCIe are operating simultaneously via the PEG port<br>0 = Digital DisplayPort (SDVO/DP/HDIM) or PCIe are operational |
| SDVO_CTRLDATA | SDVO Present                                                         | 1 = SDVO/HDIM/DP interface enabled<br>0 = No SDVO/HDIM/DP interface disabled                                                                                    |
| L_DDC_DATA    | Local Flat Panel (LFP) Present                                       | 1 = LFP Card Present; PCIe disabled<br>0 = LFP Disable                                                                                                          |
| DDPC_CTRLDATA | Digital Display (HDIM/UDP) device present                            | 1 = Digital display (HDIM/UDP) device present<br>0 = Digital display (HDIM/UDP) interface absent                                                                |

- The recommended pull-up resistor value is 4.02 kΩ ±1%.
- The recommended pull-down resistor value is 2.21 kΩ ±1%.



Check list note : CL\_REF=0.35V





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|       |                            |               |
|-------|----------------------------|---------------|
| Size  | Document Number            | Rev           |
|       | Cantiga SFF (DDRII)        | 1A            |
| Date: | Wednesday, August 26, 2009 | Sheet 8 of 31 |

## 09

VCC 2200mA

U12F

VCC CORE

## POWER

VCC NCTF

+1.8VSUS

VCC SM : 3000mA

+VCC\_SM\_I

VCC AXG 7700mA

POWER

VCC GFX NCTF

VCC GFX

VCC GFX

CC MS LF

UMA 9.6A(GM45)  
(Plane or shape)

Layout Note:  
Inside GMCH cavity.

10mil

CANTIGASFF\_1p0

1. Route VCC\_AXG\_SENSE and VSS\_AXG\_SENSE differentially
2. VCC\_AXG\_SENSE PU to +VGFY\_CORE\_INT with 10ohm and VSS\_AXG\_SENSE PD with 10ohm for Intel suggest

CANTIGASFF 1p0

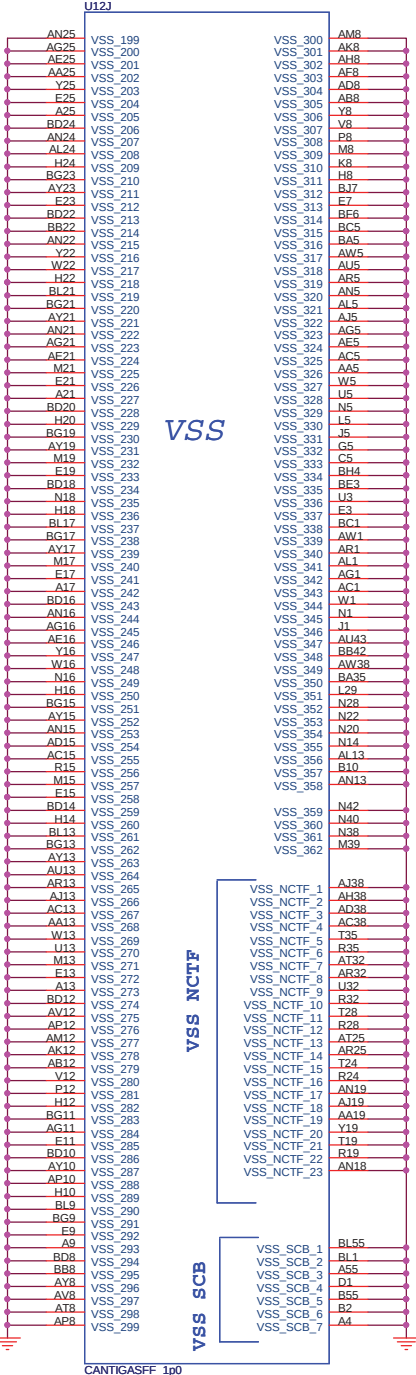
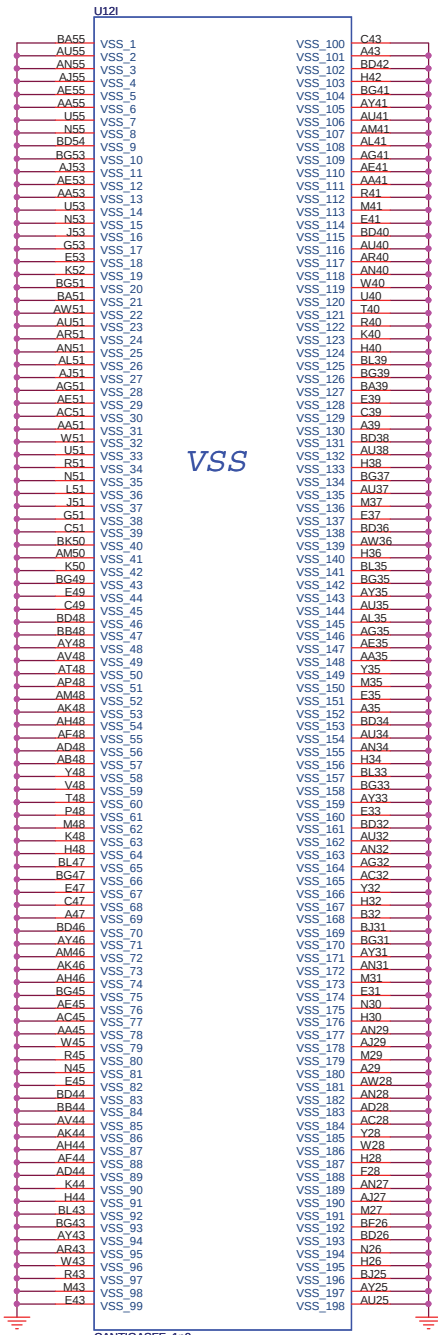


NB5

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|       |                               |               |
|-------|-------------------------------|---------------|
| Size  | Document Number               | Rev           |
|       | <b>Cantiga SFF (VCC/NCTF)</b> | 1             |
| Date: | Wednesday, August 26, 2009    | Sheet 9 of 31 |

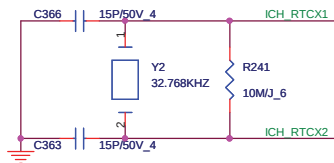




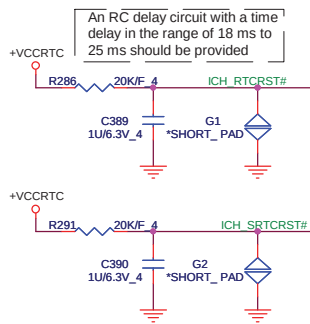
PROJECT : QL1  
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|       |                            |                |
|-------|----------------------------|----------------|
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|       | Cantiga SFF (GND)          | 1A             |
| Date: | Wednesday, August 26, 2009 | Sheet 11 of 31 |

## RTC CRYSTAL

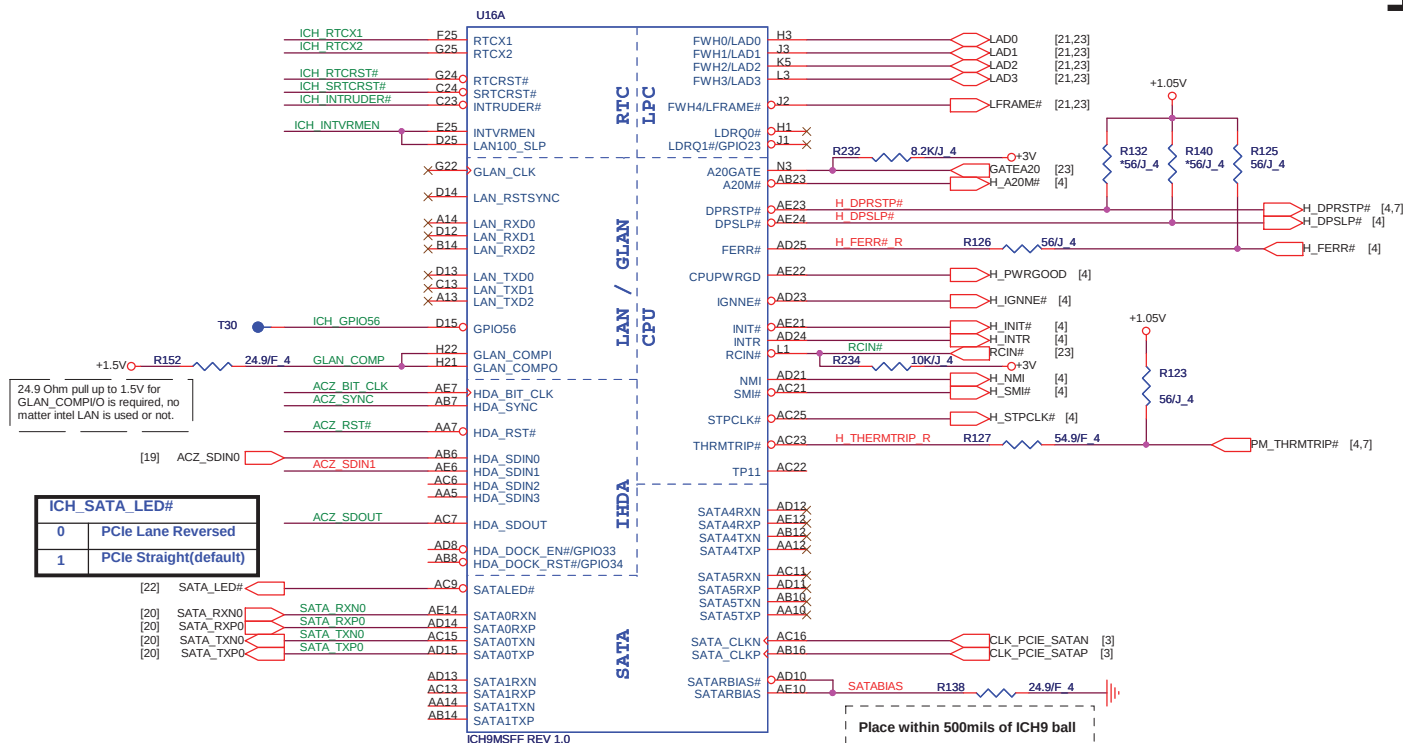


## RESET JUMP

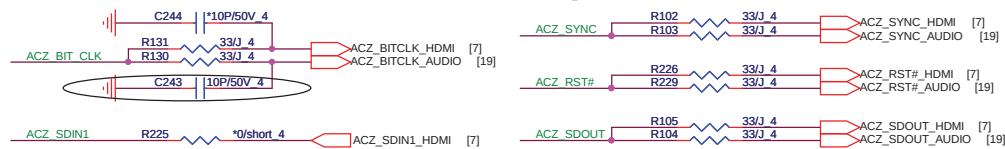


<http://hot-electronics.net> (CLG)

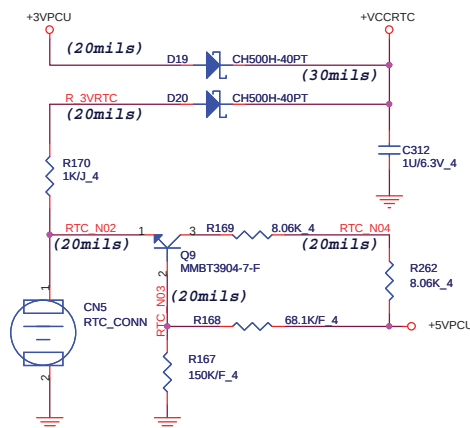
12



## HD Audio Interface



## RTC BATTERY (RTC)



### South Bridge Strap Pin (1/3)

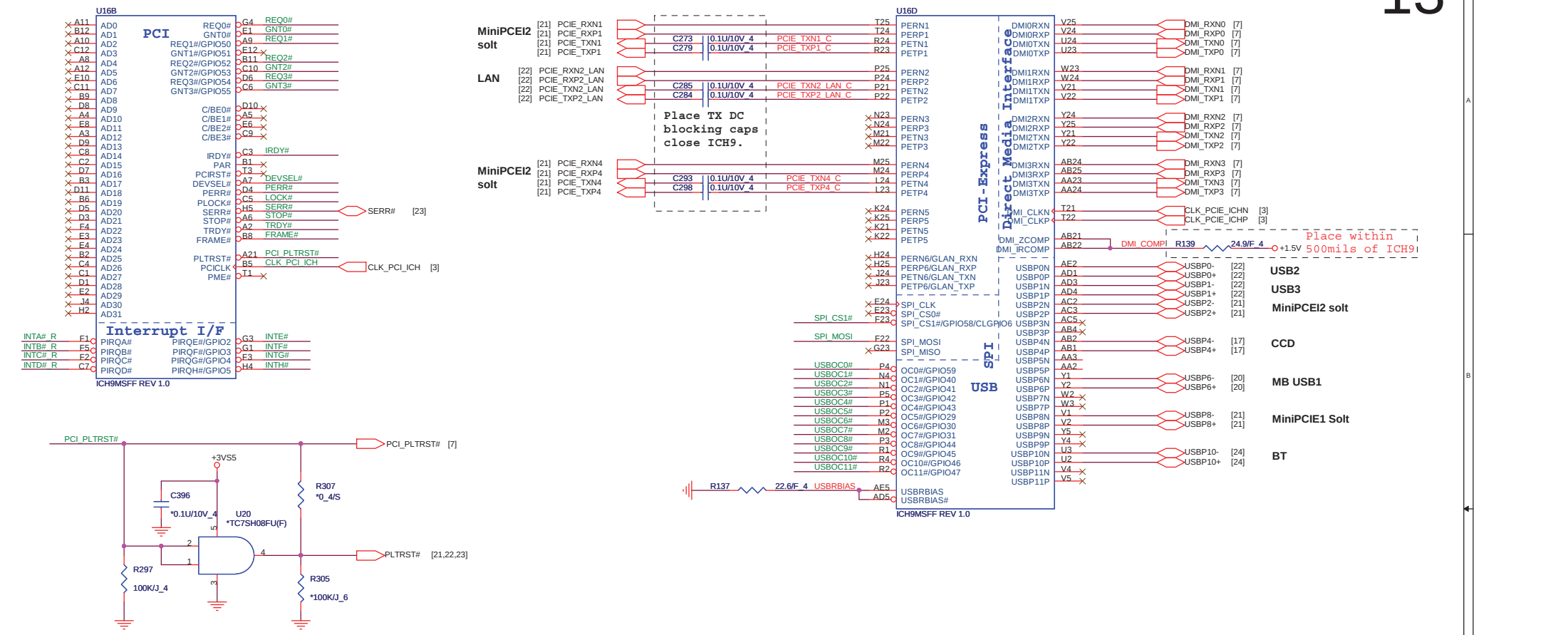
| Pin Name               | Strap description                                                 | Sampled | Configuration                                                                                                                           |           |                            | PU/PD                                                                                                  |
|------------------------|-------------------------------------------------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------|-----------|----------------------------|--------------------------------------------------------------------------------------------------------|
| HDA_DOCK_EN/<br>GPIO33 | Flash Descriptor Security<br>Override Strap                       | PWROK   | 0 = The Flash Descriptor Security will be overridden.<br>1 = The security measures defined<br>in the Flash Descriptor will be in effect |           |                            | This strap should only be enabled in manufacturing<br>environments using an external pull-up resistor. |
| SATALED#               | PCI Express Lane Reversal<br>(Lanes 1-4)                          | PWROK   | Internal PU                                                                                                                             |           |                            |                                                                                                        |
|                        | XOR Chain Entrance                                                | PWROK   | ICH_TP3                                                                                                                                 | ACZ_SDOUT | Description                | [14]              |
|                        |                                                                   |         | 0                                                                                                                                       | 0         | RSVD                       |                                                                                                        |
| HDA_SDOUT              | XOR Chain Entrance /PCI Express*<br>Port Config 1 bit 1(Port 1-4) | PWROK   | 0                                                                                                                                       | 1         | Enter XOR Chain            |                   |
|                        |                                                                   |         | 1                                                                                                                                       | 0         | Normal opration(Default)   |                                                                                                        |
|                        |                                                                   |         | 1                                                                                                                                       | 1         | Set PCIe port config bit 1 |                                                                                                        |



**PROJECT : QL1**  
**Quanta Computer Inc.**  
**MV CULV**

Size Document Number  
**ICH9M SFF (Host/SATA/HDA)**

Date: Wednesday, August 26, 2009 | Sheet 12 of 31



South Bridge Strap Pin (2/3)

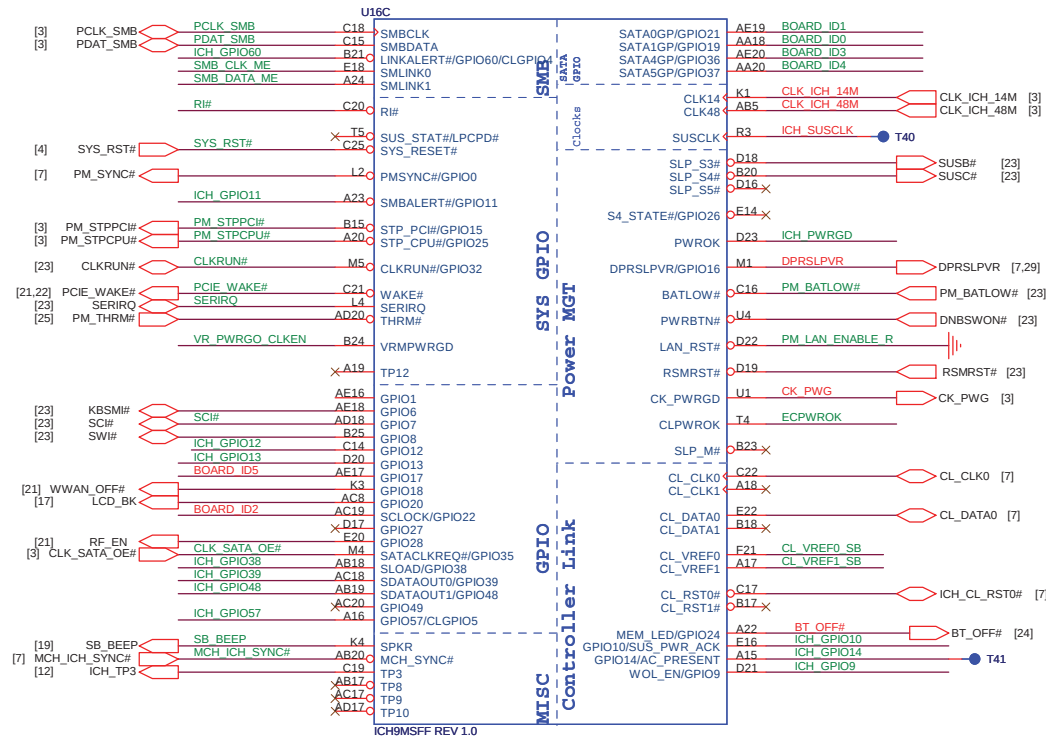
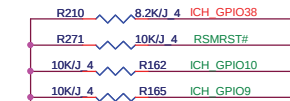
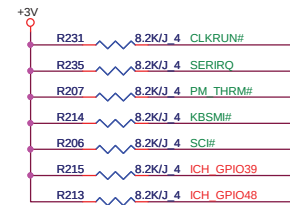
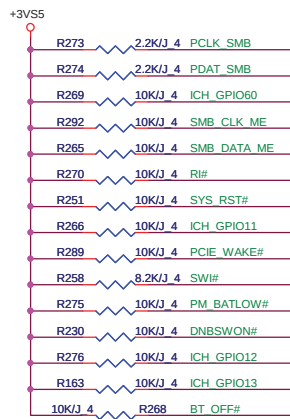
| Pin Name                                                                                                   | Strap description                             | Sampled      | Configuration                                                                                                              | PU/PD                                                                                |               |               |                                                                                      |   |     |                                                                                      |
|------------------------------------------------------------------------------------------------------------|-----------------------------------------------|--------------|----------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------|---------------|--------------------------------------------------------------------------------------|---|-----|--------------------------------------------------------------------------------------|
| HDA_SYNC                                                                                                   | PCI Express Port<br>Config 1 bit 0 (Port 1-4) | PWROK        | 0 = Default<br>1 = Setting bit 0                                                                                           |                                                                                      |               |               |                                                                                      |   |     |                                                                                      |
| GNT2# / GPIO53                                                                                             | PCI Express Port<br>Config 2 bit 2 (Port 5-6) | PWROK        | 0 = Setting bit 2<br>1 = Default                                                                                           |  |               |               |                                                                                      |   |     |                                                                                      |
| GNT1# / GPIO51                                                                                             | ESI Strap(Server Only)                        | PWROK        | 0 = DMI for ESI-compatible<br>1 = Default                                                                                  |                                                                                      |               |               |                                                                                      |   |     |                                                                                      |
| GNT3# / GPIO55                                                                                             | Top-Block Swap Override                       | PWROK        | 0 = "top-block swap" mode<br>1 = Default                                                                                   |  |               |               |                                                                                      |   |     |                                                                                      |
| SPI_MOSI                                                                                                   | Integrated TPM Enable                         | CLPWROK      | 0 = INT TPM disable(Default)<br>1 = INT TPM enable                                                                         |  |               |               |                                                                                      |   |     |                                                                                      |
| GNT0#                                                                                                      | Boot BIOS Selection 0                         | PWROK        | <table><tr><th>PCI_GNT#0</th><th>SPI_CS#1</th><th>Boot Location</th></tr><tr><td>0</td><td>1</td><td>SPI</td></tr></table> | PCI_GNT#0                                                                            | SPI_CS#1      | Boot Location | 0                                                                                    | 1 | SPI |  |
|                                                                                                            |                                               |              | PCI_GNT#0                                                                                                                  | SPI_CS#1                                                                             | Boot Location |               |                                                                                      |   |     |                                                                                      |
| 0                                                                                                          | 1                                             | SPI          |                                                                                                                            |                                                                                      |               |               |                                                                                      |   |     |                                                                                      |
| <table><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>1</td><td>1</td><td>LPC(Default)</td></tr></table> | 1                                             | 0            | PCI                                                                                                                        | 1                                                                                    | 1             | LPC(Default)  |                                                                                      |   |     |                                                                                      |
| 1                                                                                                          | 0                                             | PCI          |                                                                                                                            |                                                                                      |               |               |                                                                                      |   |     |                                                                                      |
| 1                                                                                                          | 1                                             | LPC(Default) |                                                                                                                            |                                                                                      |               |               |                                                                                      |   |     |                                                                                      |
| SPI_CS1# /<br>GPIO58 / CLGPIO6                                                                             | Boot BIOS Selection 1                         | CLPWROK      | <table><tr><td>1</td><td>1</td><td>LPC(Default)</td></tr></table>                                                          | 1                                                                                    | 1             | LPC(Default)  |  |   |     |                                                                                      |
| 1                                                                                                          | 1                                             | LPC(Default) |                                                                                                                            |                                                                                      |               |               |                                                                                      |   |     |                                                                                      |

### PCI PULL-UP

### USBOC# PULL-UP

**PROJECT : QL1**  
Quanta Computer Inc.

|       |                                 |                |
|-------|---------------------------------|----------------|
| Size  | Document Number                 | Rev            |
|       | <b>ICH9M SFF (USB/PCIE/DMI)</b> | 1A             |
| Date: | Wednesday, August 26, 2009      | Sheet 13 of 31 |



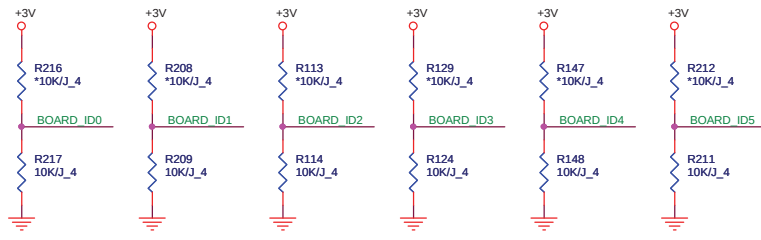
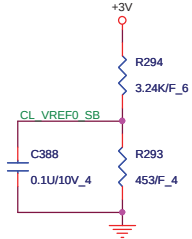
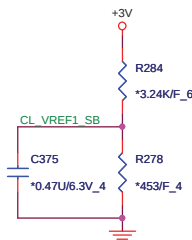
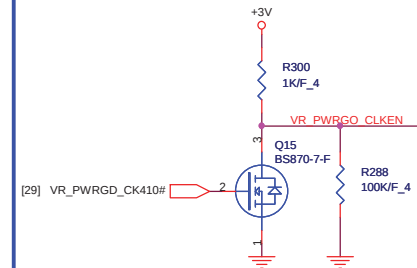
No Reboot Strap

SB\_BEEP Low: Default  
Hi: No reboot

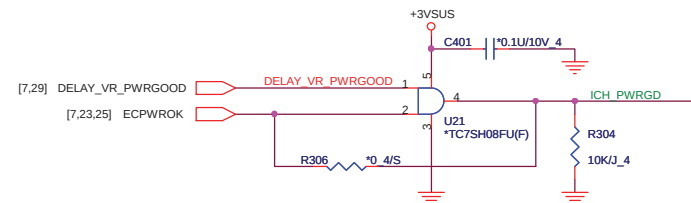


TPM physical presence

ICH\_GPIO57 Low: Default



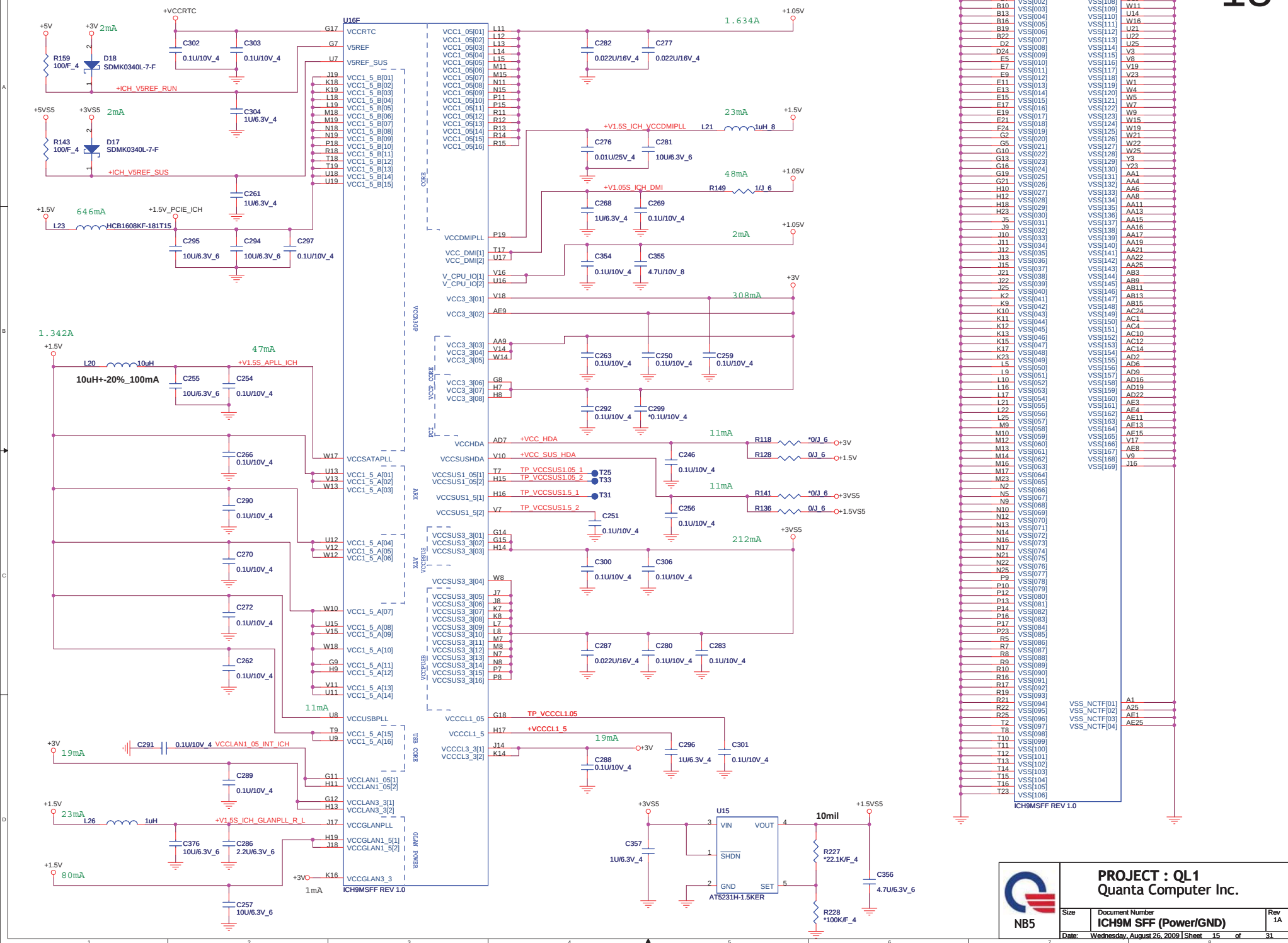
| BOARD ID | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | NOTE |
|----------|-----|-----|-----|-----|-----|-----|------|
| GS40     | 0   | 0   | 0   | 0   | 0   | 0   |      |
| GS45     | 0   | 0   | 0   | 0   | 0   | 1   |      |
|          |     |     |     |     |     |     |      |
|          |     |     |     |     |     |     |      |
|          |     |     |     |     |     |     |      |
|          |     |     |     |     |     |     |      |
|          |     |     |     |     |     |     |      |
|          |     |     |     |     |     |     |      |



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MV CULV

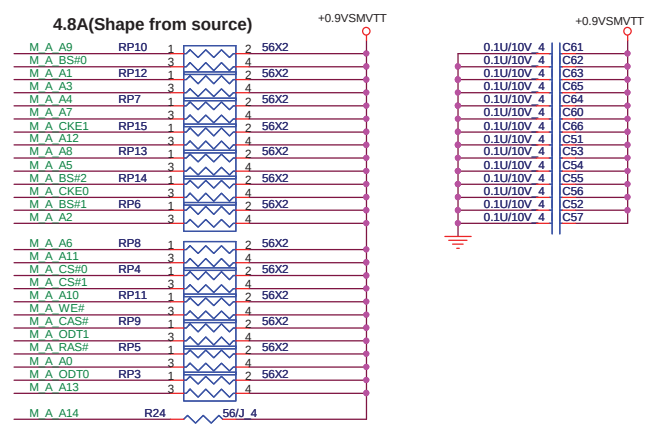
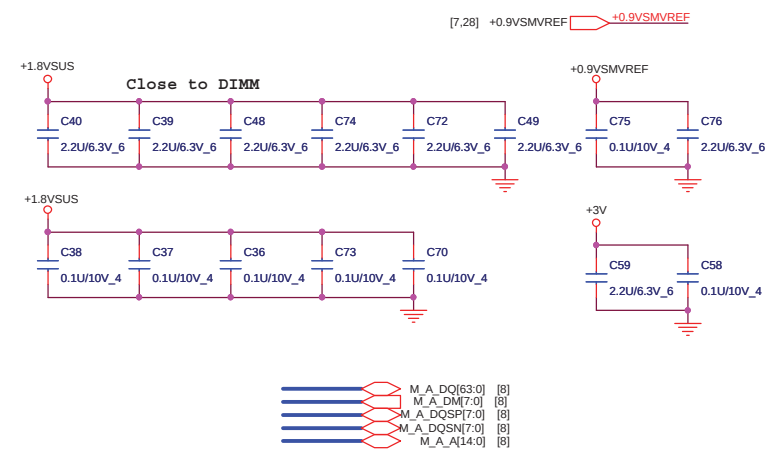
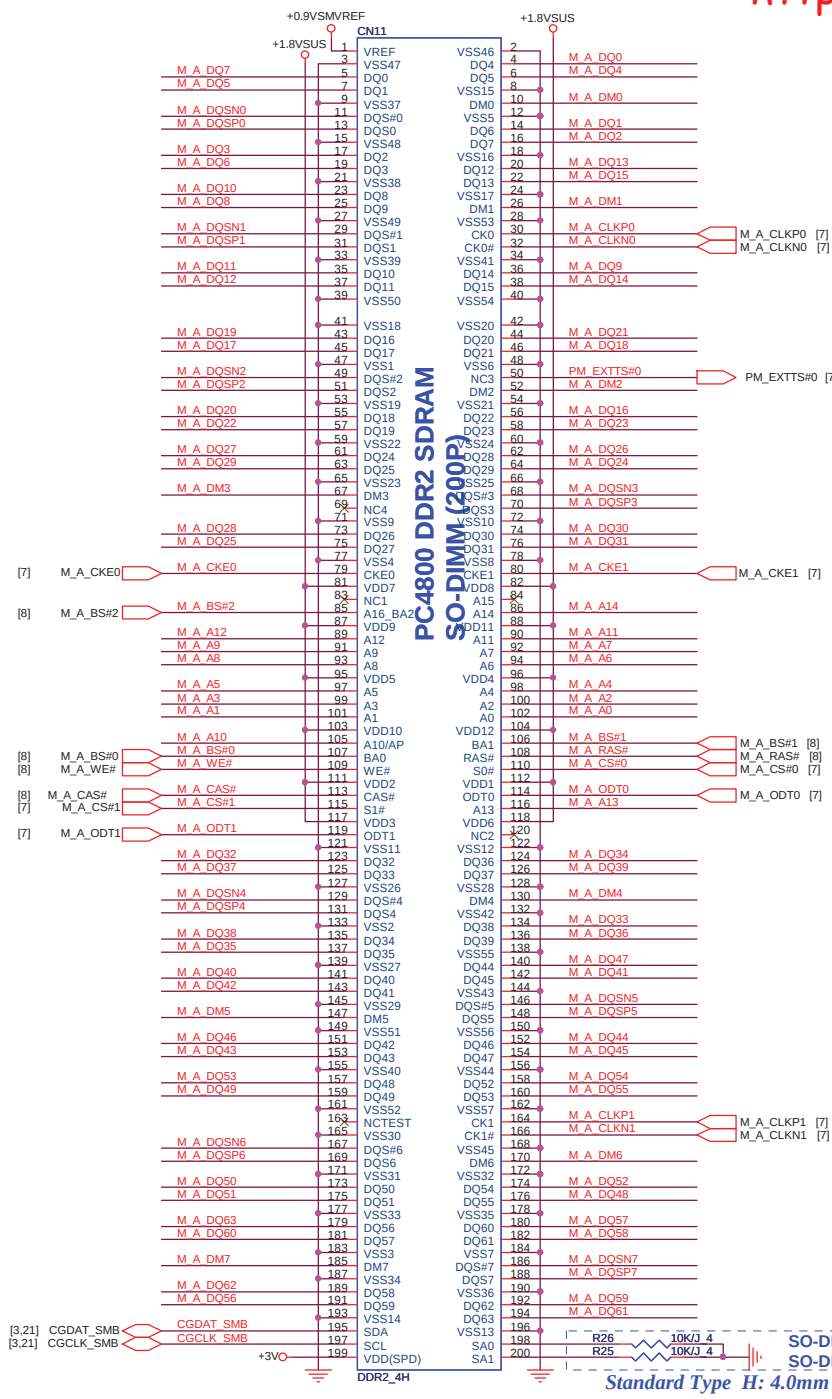
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**PROJECT : QL1**  
Quanta Computer Inc.

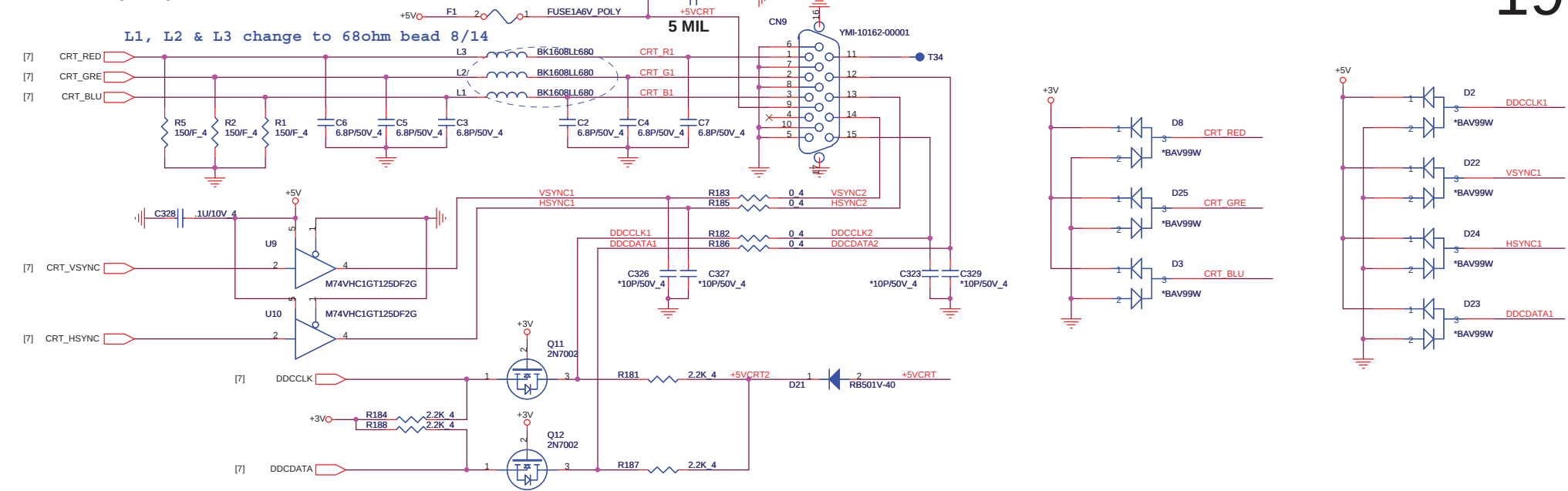
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| Size  | Document Number              | Rev            |
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| Date: | Wednesday, August 26, 2009   | Sheet 15 of 31 |



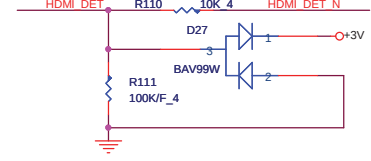
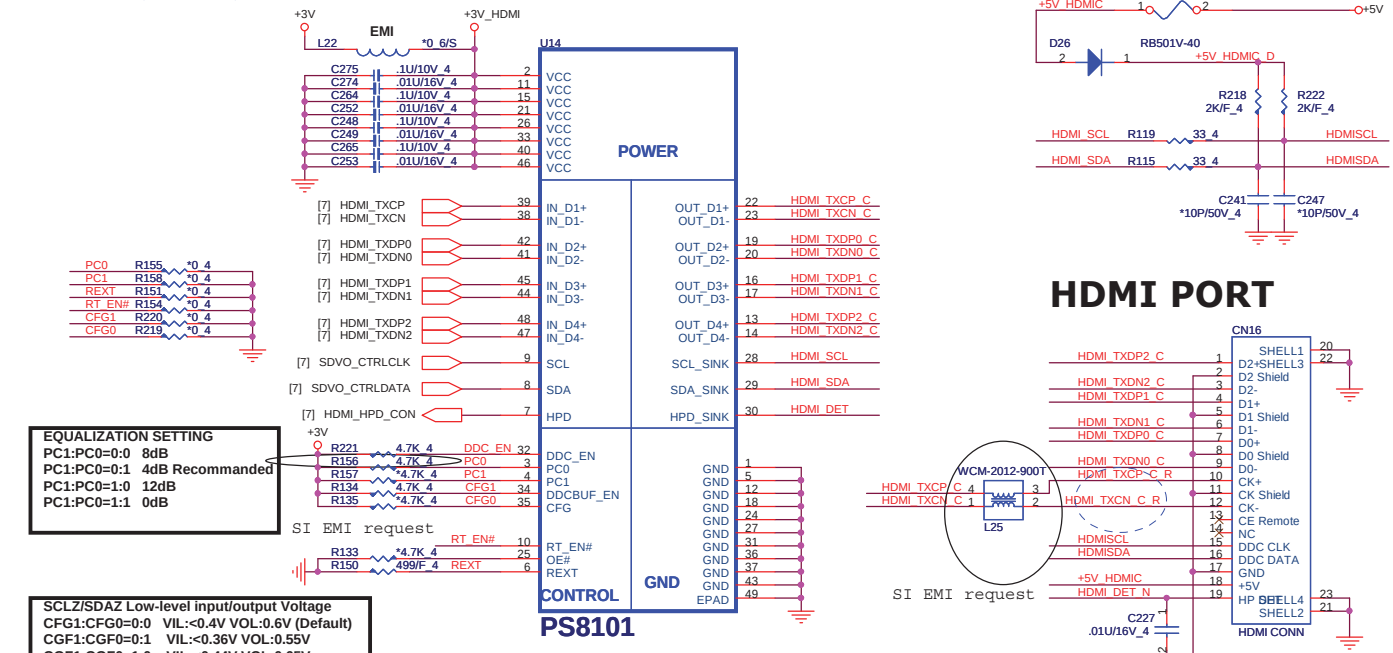
SMbus address A0  
SO-DIMM1 SPD Address is 0xA4  
SO-DIMM1 TS Address is 0x34  
Standard Type H: 4.0mm



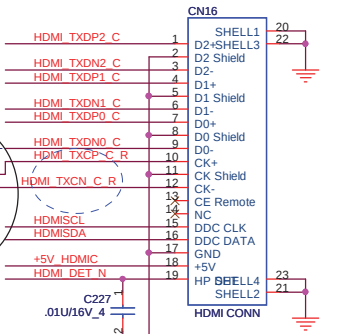
CRT PORT (CRT)



HDMI(HDM)



HDMI PORT



|      | PDT    | CHR  | PIM  |
|------|--------|------|------|
| R631 | NC     | 0    | 0    |
| R596 | NC     | 4.7K | NC   |
| R605 | NC     | NC   | NC   |
| R608 | 4.7K   | NC   | NC   |
| R558 | 100K   | NC   | NC   |
| R594 | 499    | 1.2K | 4.7K |
| R550 | 7.5K   | 7.5K | NC   |
| R552 | 20K    | 20K  | NC   |
| R595 | NC     | NC   | 4.7K |
| Q31  | 2N7002 | NC   | NC   |
| R606 | NC     | 4.7K | NC   |

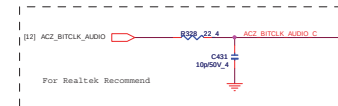
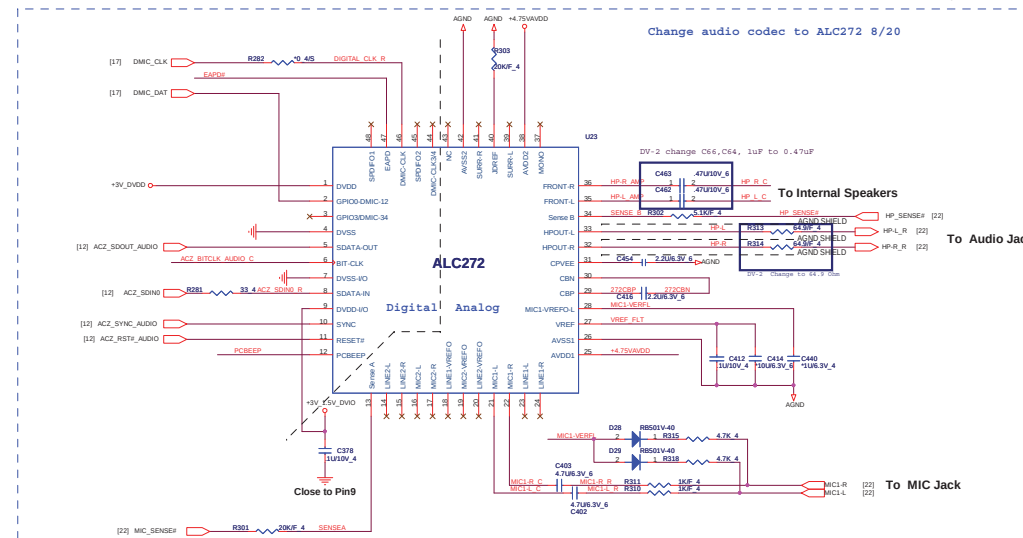
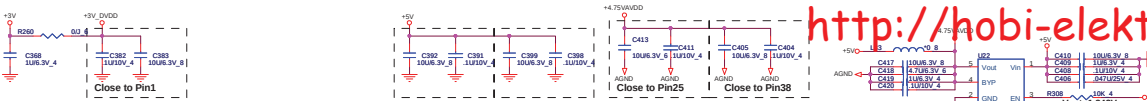
Vendor:PDT P/N:AL008101000  
Vendor:CHR P/N:AL007318001  
Vendor:PIM P/N:ALP411LS001



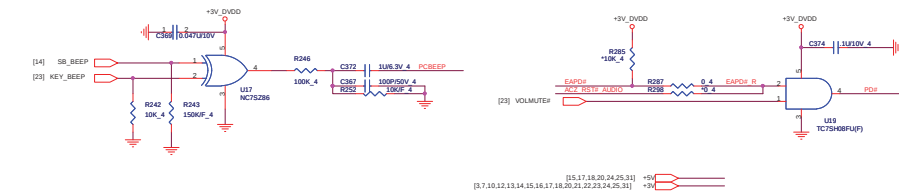
PROJECT : QL1  
Quanta Computer Inc.

| Size  | Document Number            | Rev            |
|-------|----------------------------|----------------|
|       | CRT                        | 1A             |
| Date: | Wednesday, August 26, 2009 | Sheet 18 of 31 |

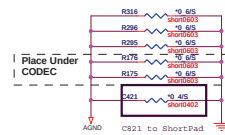
Change to HDMI\_TXCN\_C\_R & HDMI\_TXCP\_C\_R 8/14



| PORT     | PLACE TO             |
|----------|----------------------|
| MONO OUT | X                    |
| PORT A   | AUDIO OUT            |
| PORT B   | MIC                  |
| PORT C   | X                    |
| PORT D   | Internal Speakers    |
| PORT E   | X                    |
| PORT F   | X                    |
| DM       | Internal DIGITAL MIC |



SA\_A# -->EXT Audio  
SA\_B# -->EXT MIC  
Audio JACK: Normal Open



## AUDIO AMPLIFIER

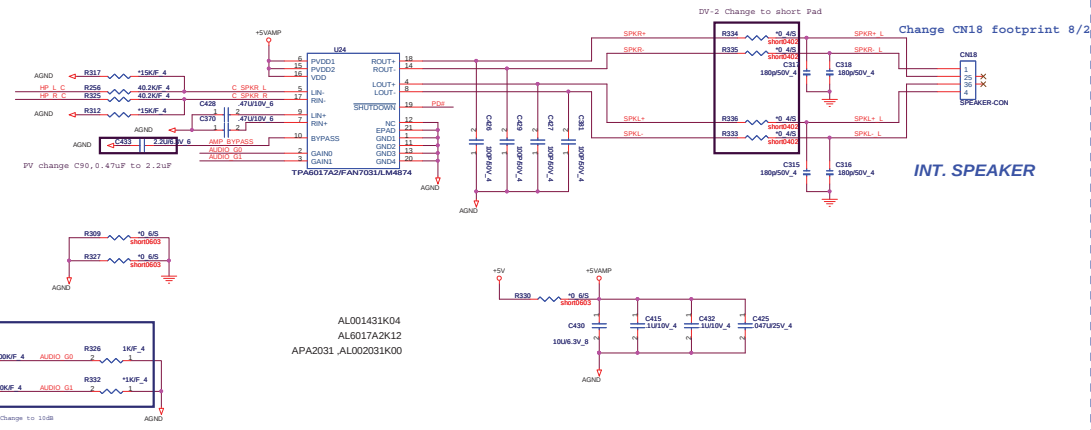
Add amplifier 8/20

6017A2 Gain Table

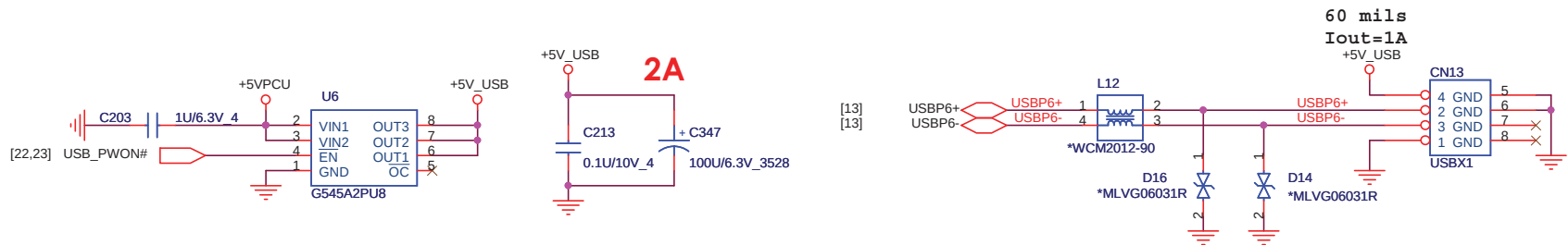
| GAIN0 | GAIN1 | AV(INV) |
|-------|-------|---------|
| 0     | 0     | 6dB     |
| 0     | 1     | 10dB    |
| 1     | 0     | 15.6dB  |
| 1     | 1     | 21.6dB  |



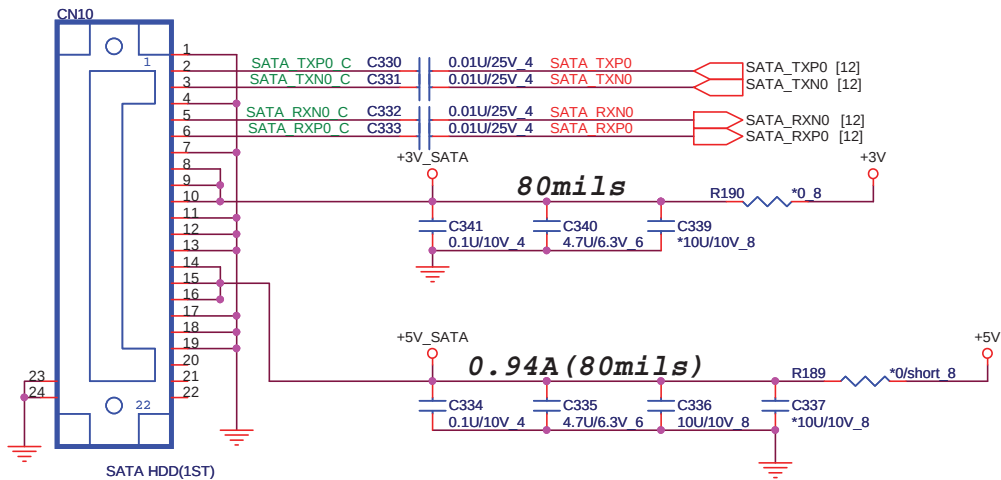
AL001A31K04  
AL6017A2K12  
APA2031 AL002031K00



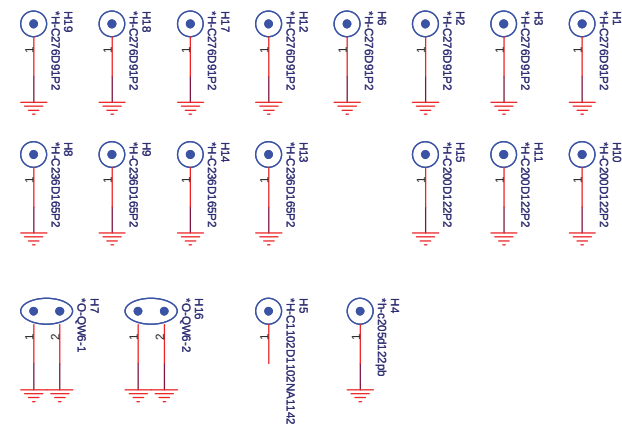
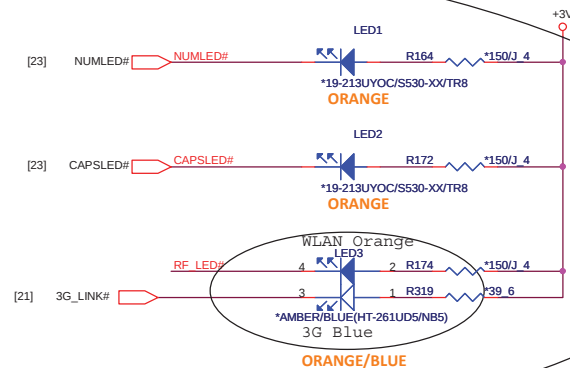
INT. SPEAKER



2.5" SATA HDD(HDD)

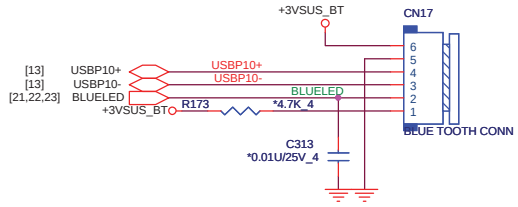
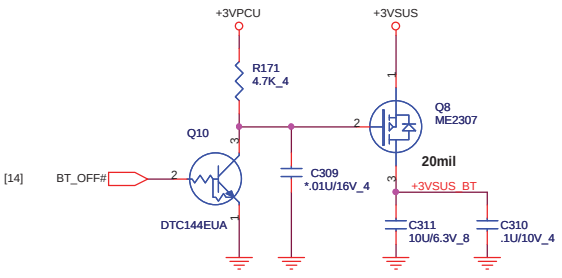
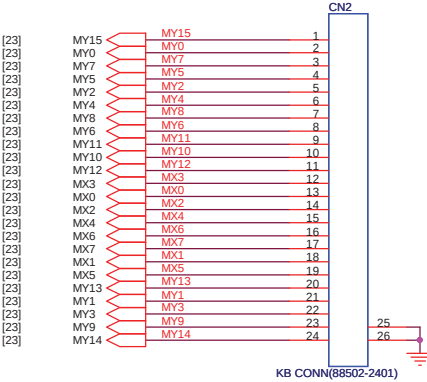






Pin 134-40 RI-TAND connector pinout diagram. The diagram shows a 40-pin connector with pins numbered 1 to 40. Pins 1-13 are on the left, and pins 14-40 are on the right. The diagram includes labels for various signals such as HP\_SENSE#, HP\_L\_R, HP\_R\_R, RF\_LINK#, USBP1, USBP1+, PCIE\_RXN2\_LAN, PCIE\_RXP2\_LAN, PCIE\_TXN2\_LAN, PCIE\_TXP2\_LAN, SMART\_LED#, MBATLED#, BATLOW#, USB\_PWON#, MIC\_SENSE#, MIC1-L, MIC1-R, SMART\_BTN#, USBP0, USBP0+, CLK\_PCIE\_LANN, CLK\_PCIE\_LANP, PCIE\_WAKE#, PLTRST#, NBSWON1#, PWR\_LED#, +5VPCU, +3V, +3VPCU, and +3VLAVCC. The diagram also shows a ground symbol and a +5VPCU symbol.

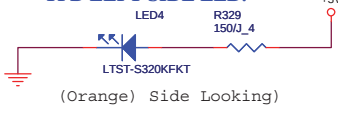




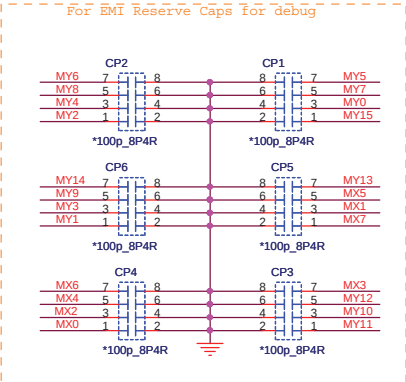
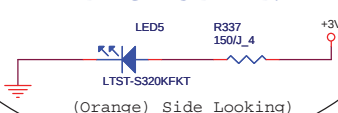
Touch Pad D/B (TPD)

20090821:  
Add TPD Right / Left side LED

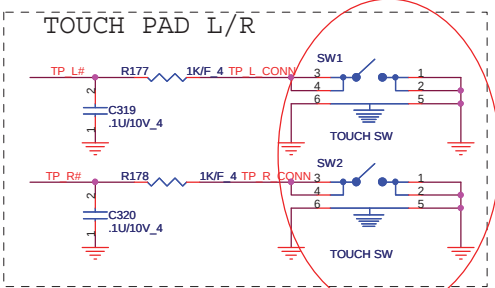
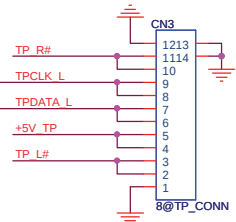
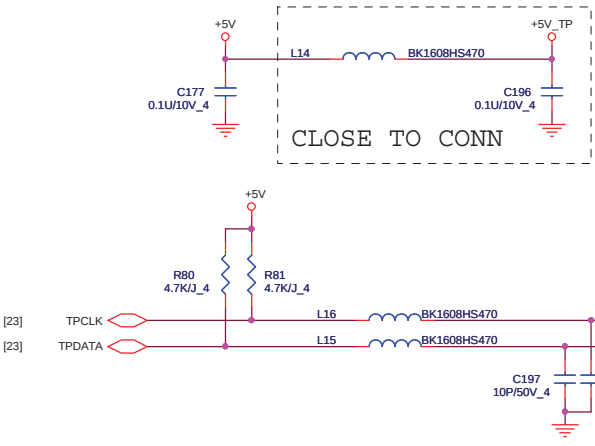
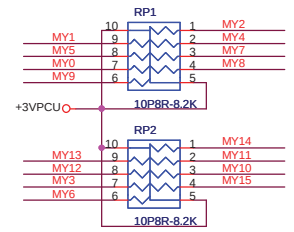
TPD LEFT SIDE LED.



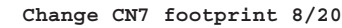
TPD RIGHT SIDE LED.



KEYBOARD PULL-UP

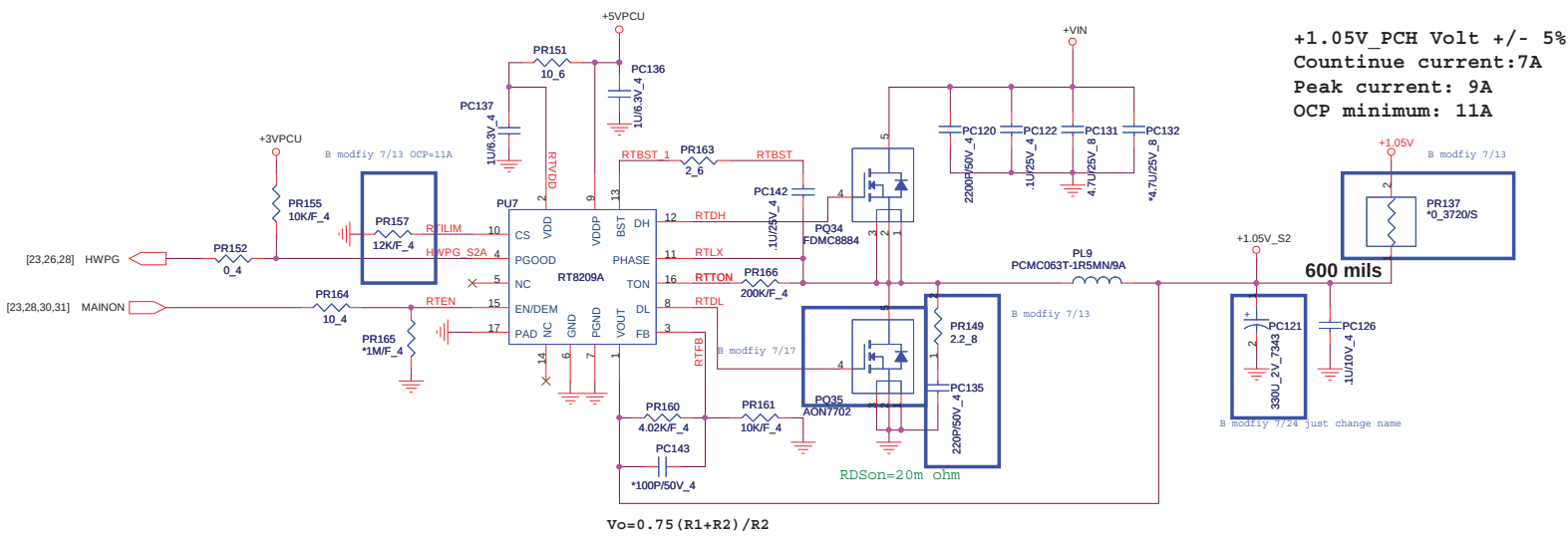


PROJECT : QL1  
Quanta Computer Inc.



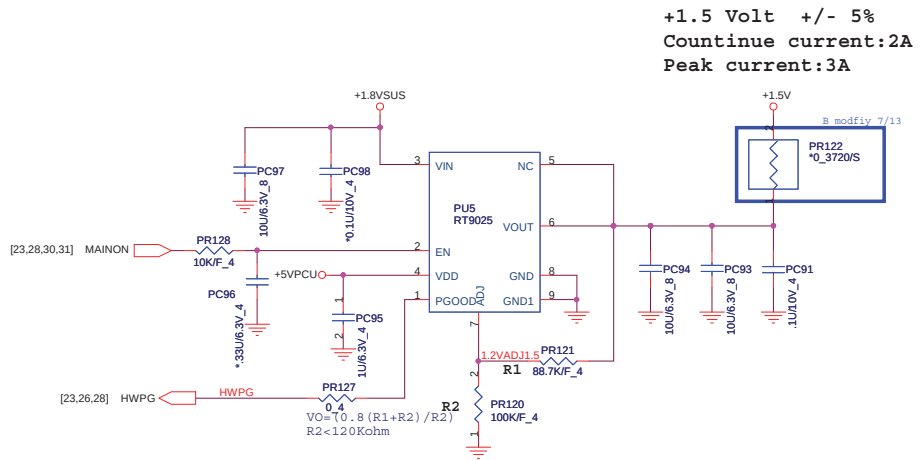
|                                                                                              |                                                     |                                       |                  |          |
|----------------------------------------------------------------------------------------------|-----------------------------------------------------|---------------------------------------|------------------|----------|
| <br>NB5 | <b>PROJECT : QL1</b><br><b>Quanta Computer Inc.</b> |                                       |                  |          |
|                                                                                              | Size                                                | Document Number<br><b>FAN/THERMAL</b> | Rev<br><b>1A</b> |          |
| Date:                                                                                        | Wednesday, August 26, 2009                          | Sheet                                 | 25               | of<br>31 |



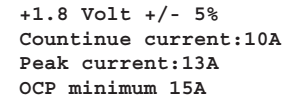


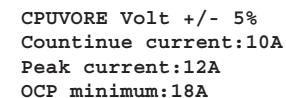
+1.05V\_PCH Volt +/- 5%  
Countinue current:7A  
Peak current: 9A  
OCP minimum: 11A

Add two cap for EMI 8/6

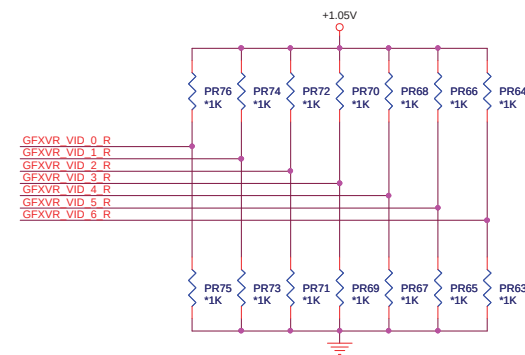


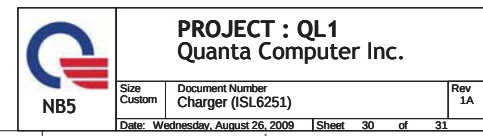
+1.5 Volt +/- 5%  
Countinue current:2A  
Peak current:3A

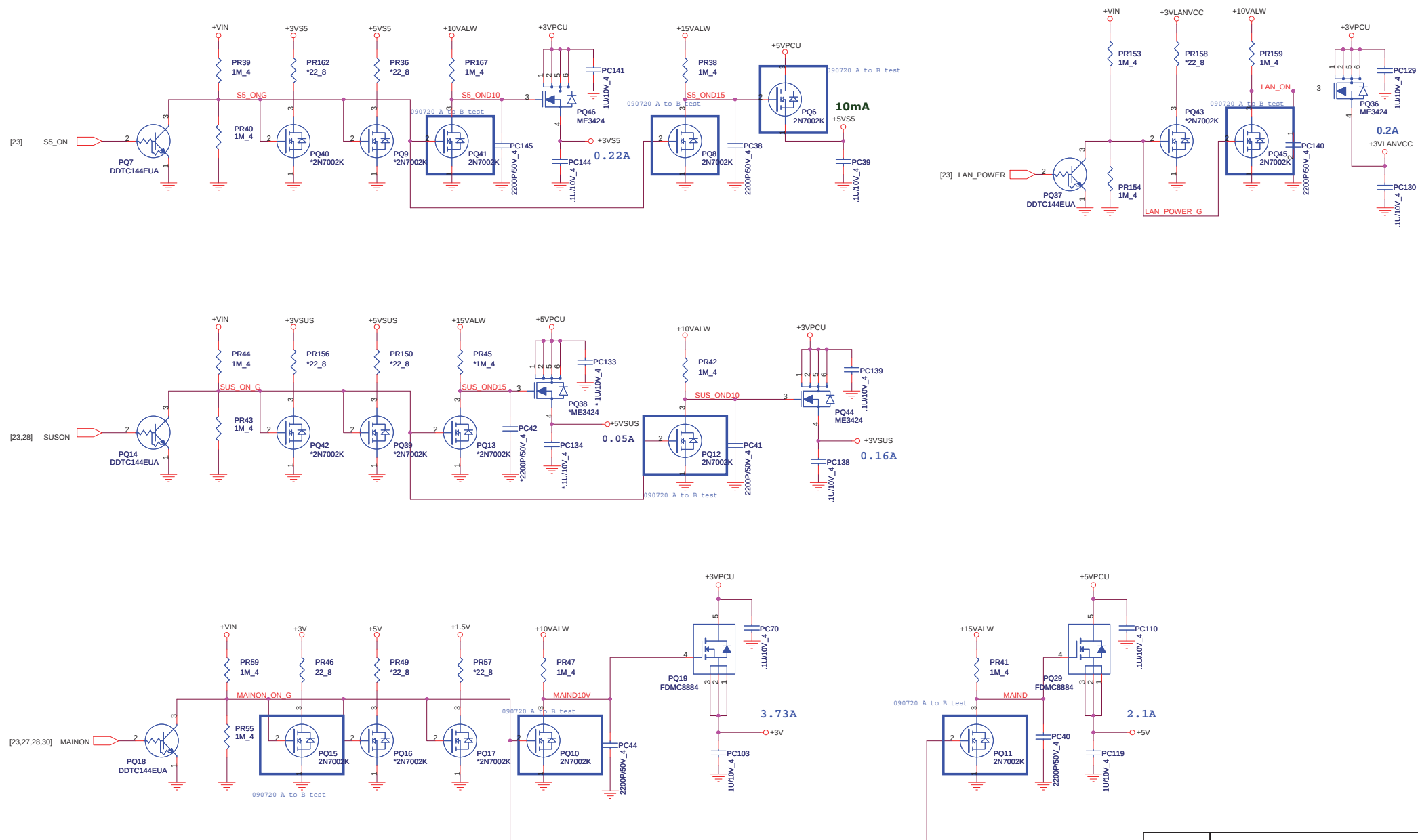




Change PL6 footprint CHOKE-ETQP4L 8/18







QW6 DV1 to QL1 DV1 modify list:

- Page 3 : 1. ADD BOM R249 475ohm.  
2. Change BOM R233,R279 2.2Kohm.  
3. Link NET PU\_BSEL0,CPU\_BSEL1,CPU\_BSEL2  
4. C361, C362, C365 stuff 10pF for EMI.
- Page 12: 1. C243 modify 10pF for EMI.
- Page 17: 1. Change U1 footprint 6pin to 5pin.  
2. C422, C423 modify for EMI.
- Page 18: 1. ADD BOM R156 4.7kohm.  
2. Stuff L25 for EMI.  
3. L1, L2, L3 modify BK1608LL680 for EMI.
- Page 19: 1. Audio CODEC modify to ALC272 + AMP from ALC269 for LG request.
- Page 21: 1. Add WLAN module power switch circuit.  
2. Add 3G module power switch.  
3. Use one 0 ohm for JSIM1 pin 10 (CD) contact with CN15 pin 7 (CLKREQ#) , but not stuff 0 ohm.
- Page 22: 1. Change LED Color (ORANGE/BLUE) .  
2. LED circuit modify no stuff.  
3. Add SMART Button & LED & RF LED line for CN4.
- Page 23: 1. Add Smart Button line contact with EC.
- Page 24: 1. Add TPD Right/ Left side LED.
- All page: 81,C88,C89,C148,C167,C348,C351,C353 footprint from Ecap3\_5x2\_8-3-1\_1h change to cc3528-1\_1h.