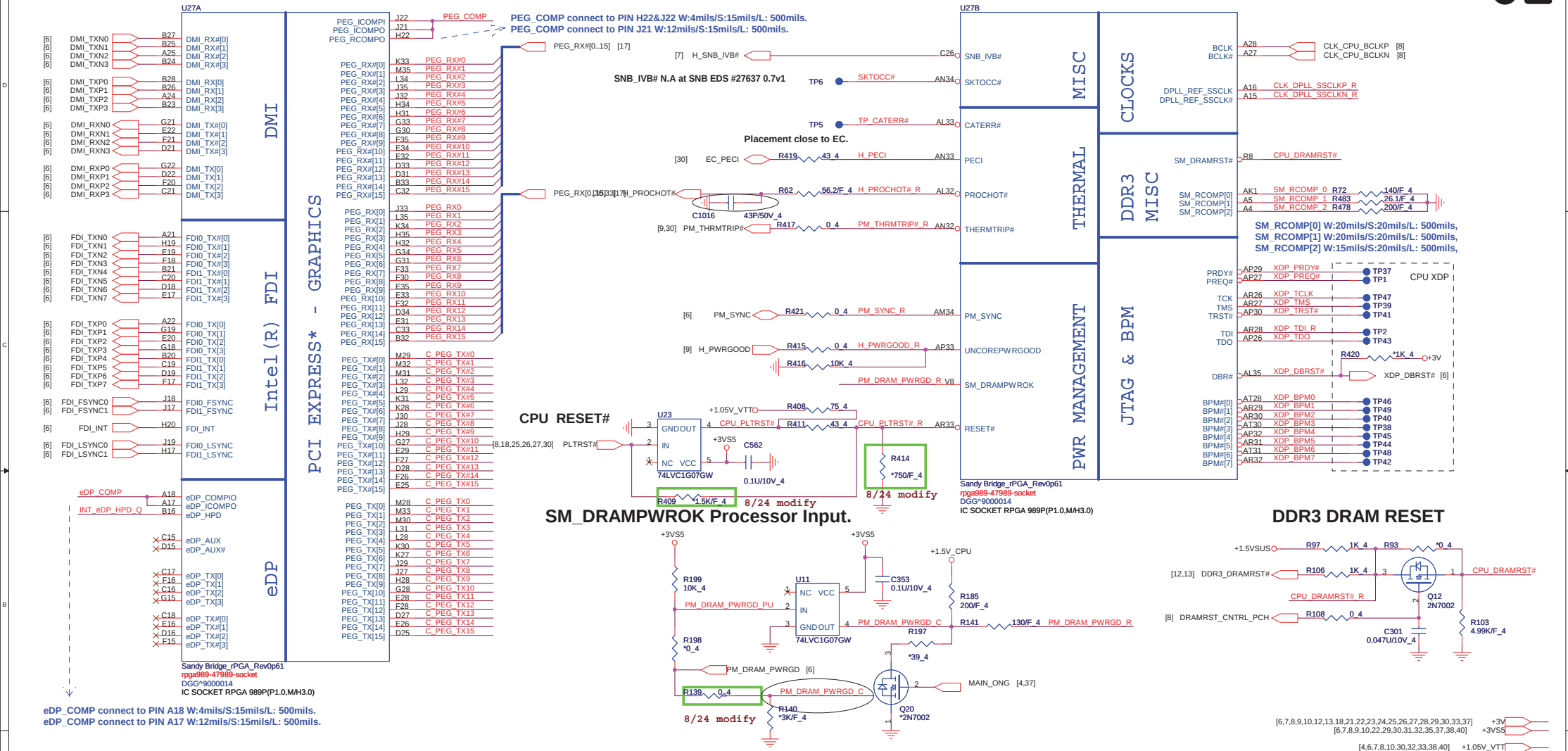


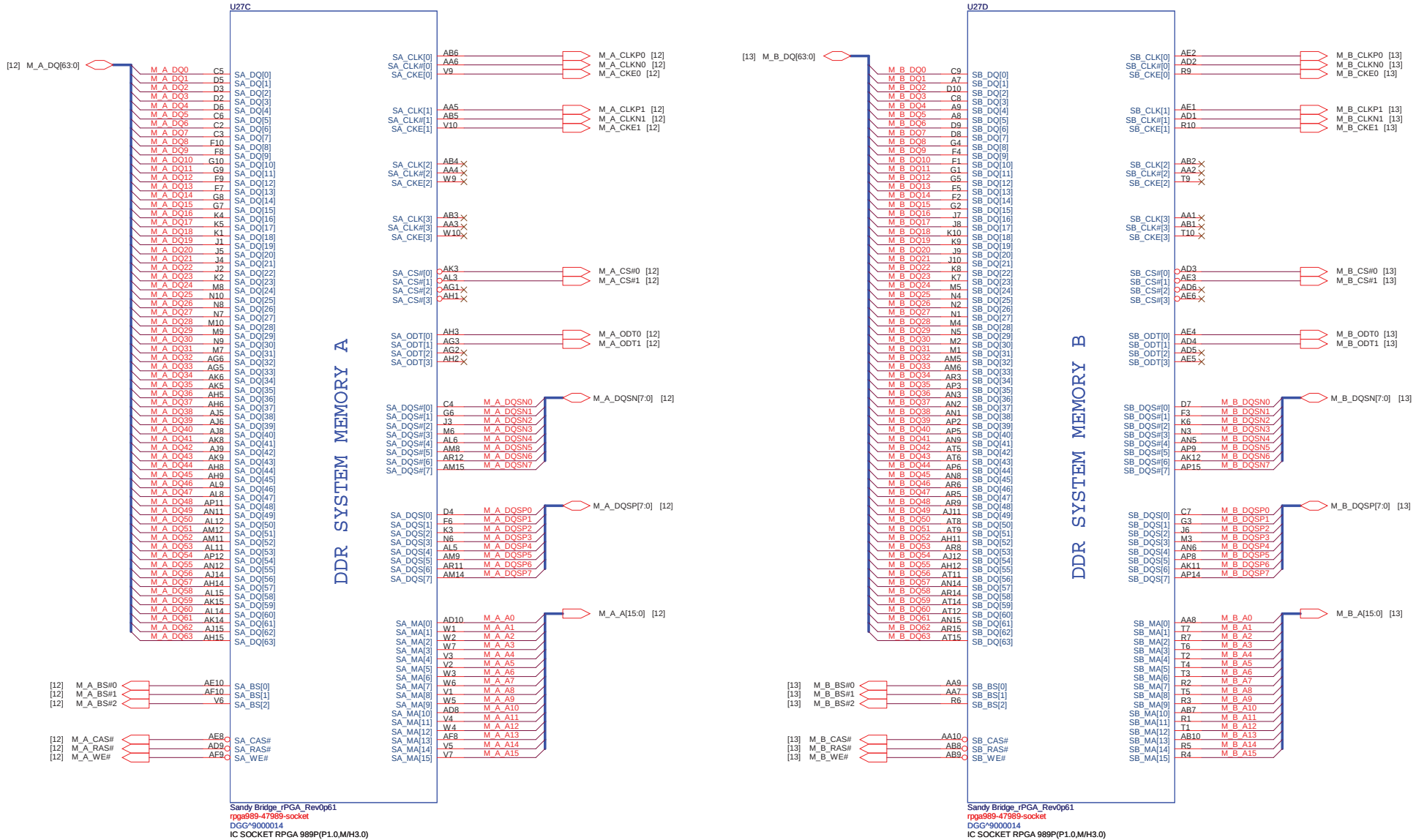
	PROJECT : SWH Quanta Computer Inc.		
	Size Custom	Document Number	Rev 1A
	Block Diagram		
Date: Tuesday, October 26, 2010	Sheet	1 of	41

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)



Sandy Bridge Processor (DDR3)



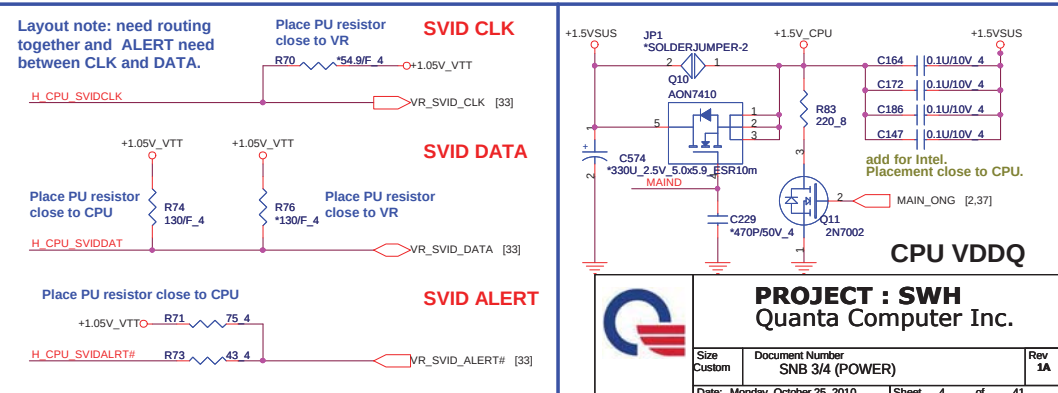
Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)

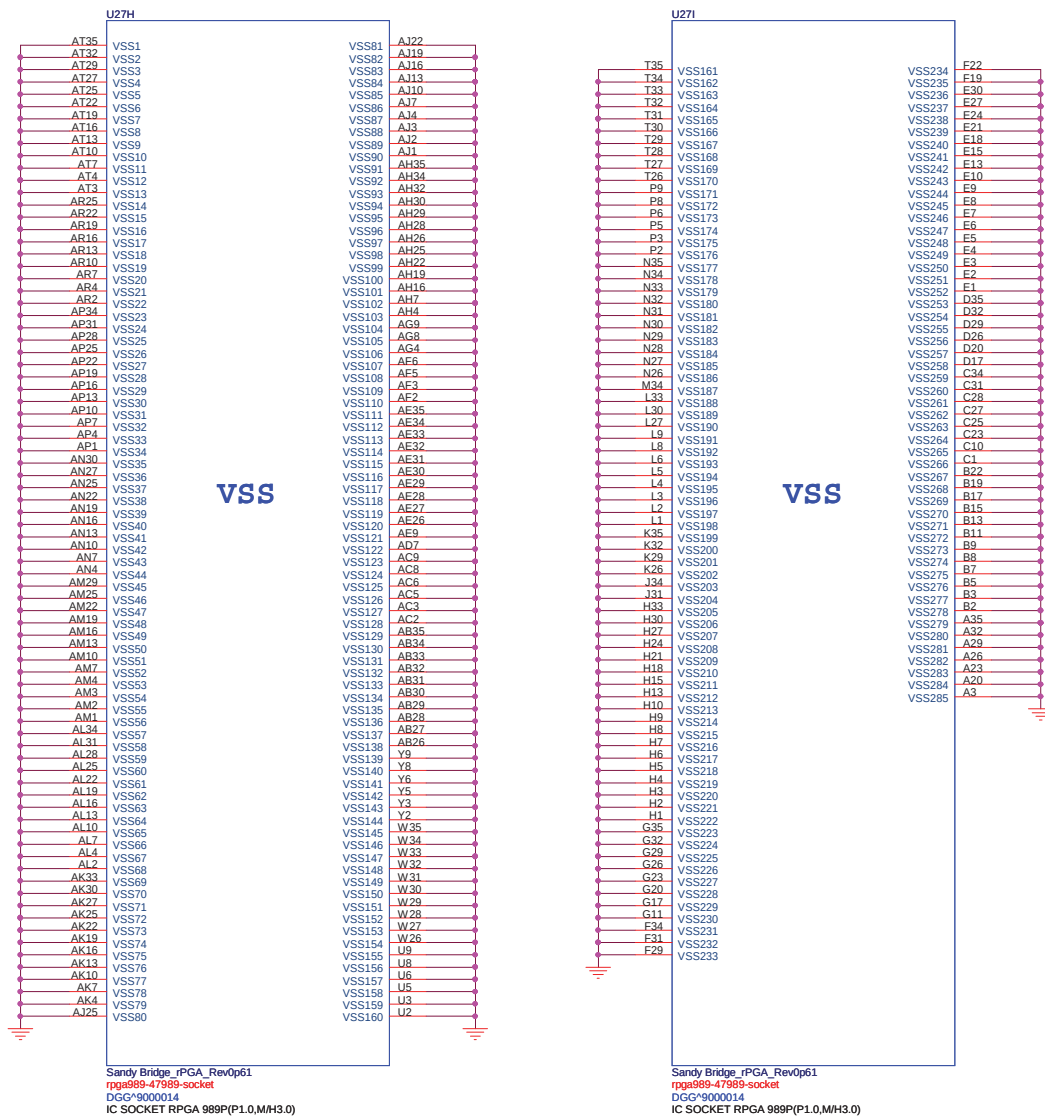


PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A
Date:	Monday, October 25, 2010	Sheet 3 of 41



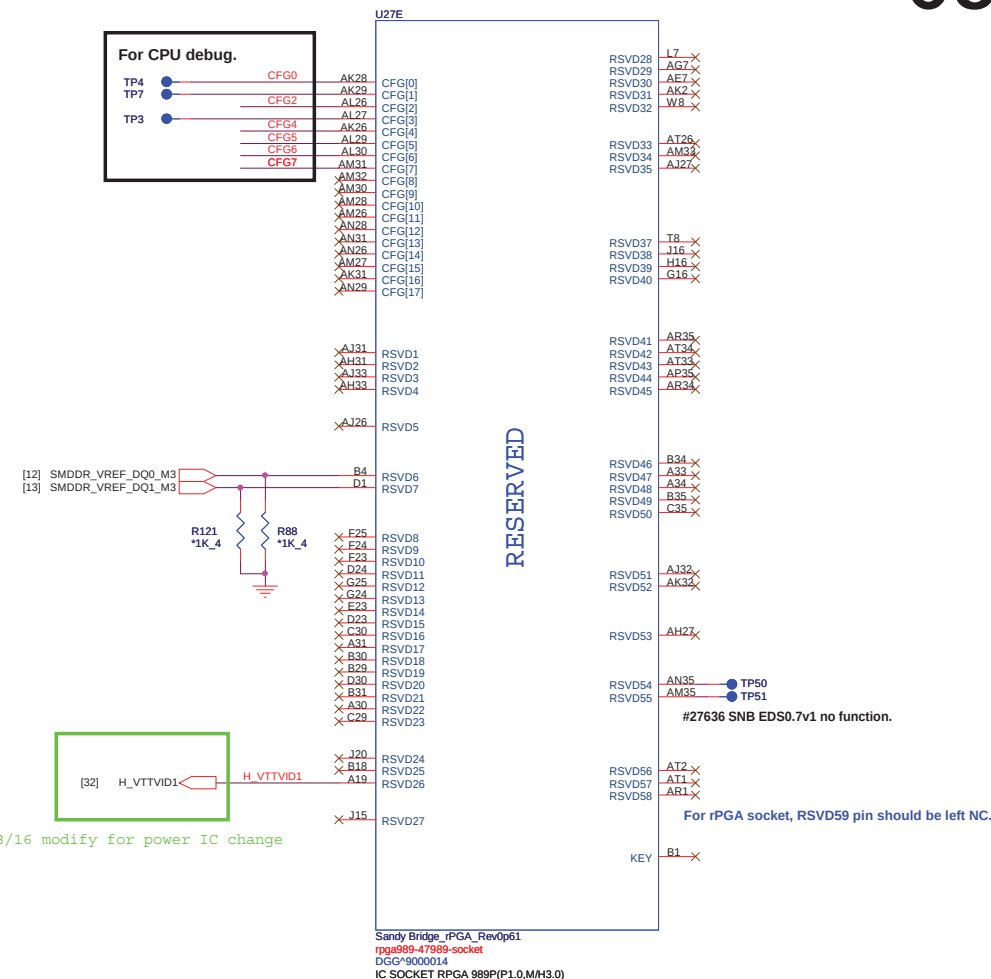
Sandy Bridge Processor (GND)



Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

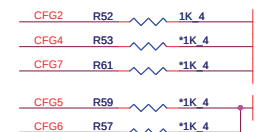
Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge Processor (RESERVED, CFG)



```
CFG[6:5] (PCIe Port Bifurcation Straps)
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

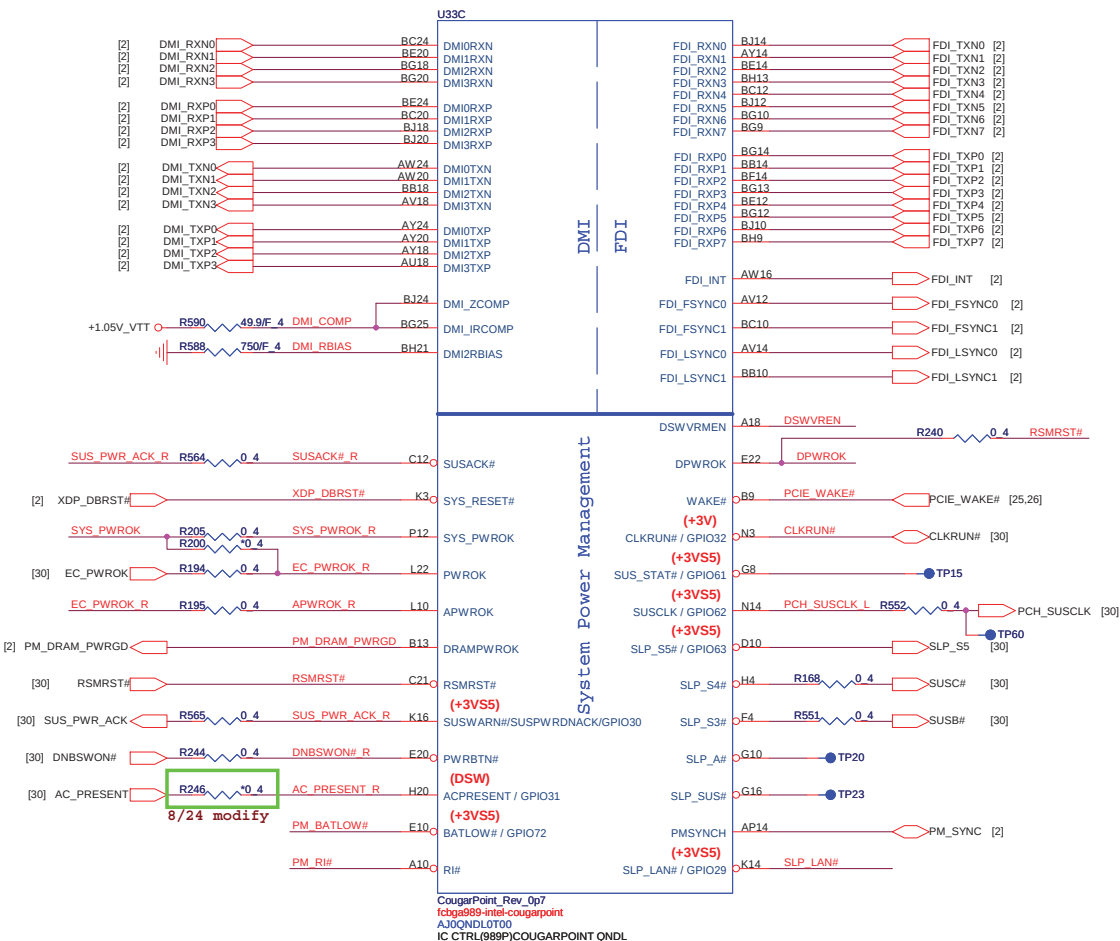
Processor Strapping		
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



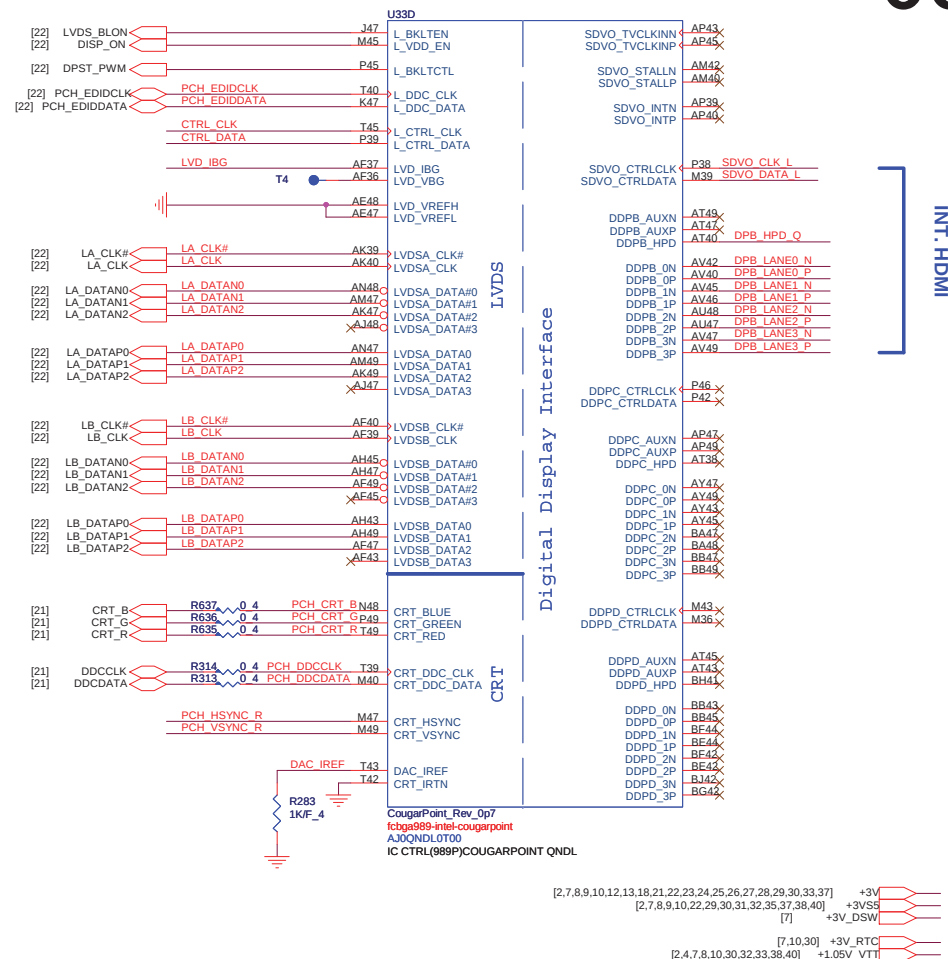
PROJECT : SWH
Quanta Computer Inc.

Size Custom	Document Number SNB 4/4 (GND)	Rev 1A
Date: Monday, October 25, 2010		Sheet 5 of 41

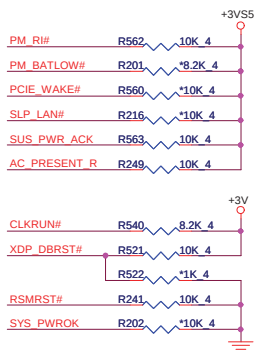
Cougar Point (DMI, FDI, PM)



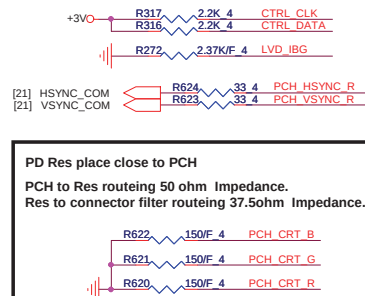
Cougar Point (LVDS, DDI)



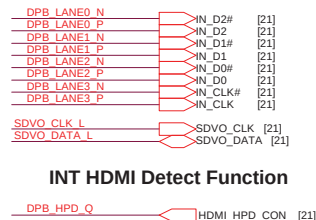
PCH Pull-high/low(CLG)



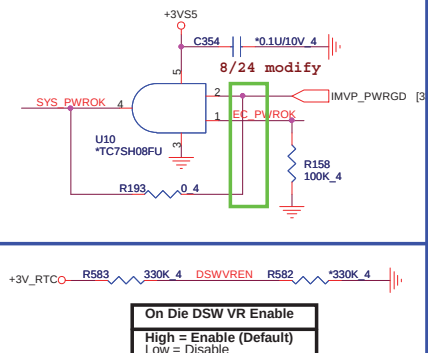
**INT LVDS & CRT disable
(DIS only remove)**



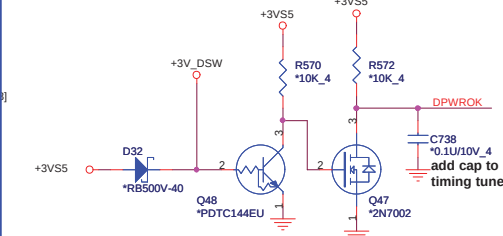
INT HDMI disable (DIS only remove)



System PWR_OK(CLG)



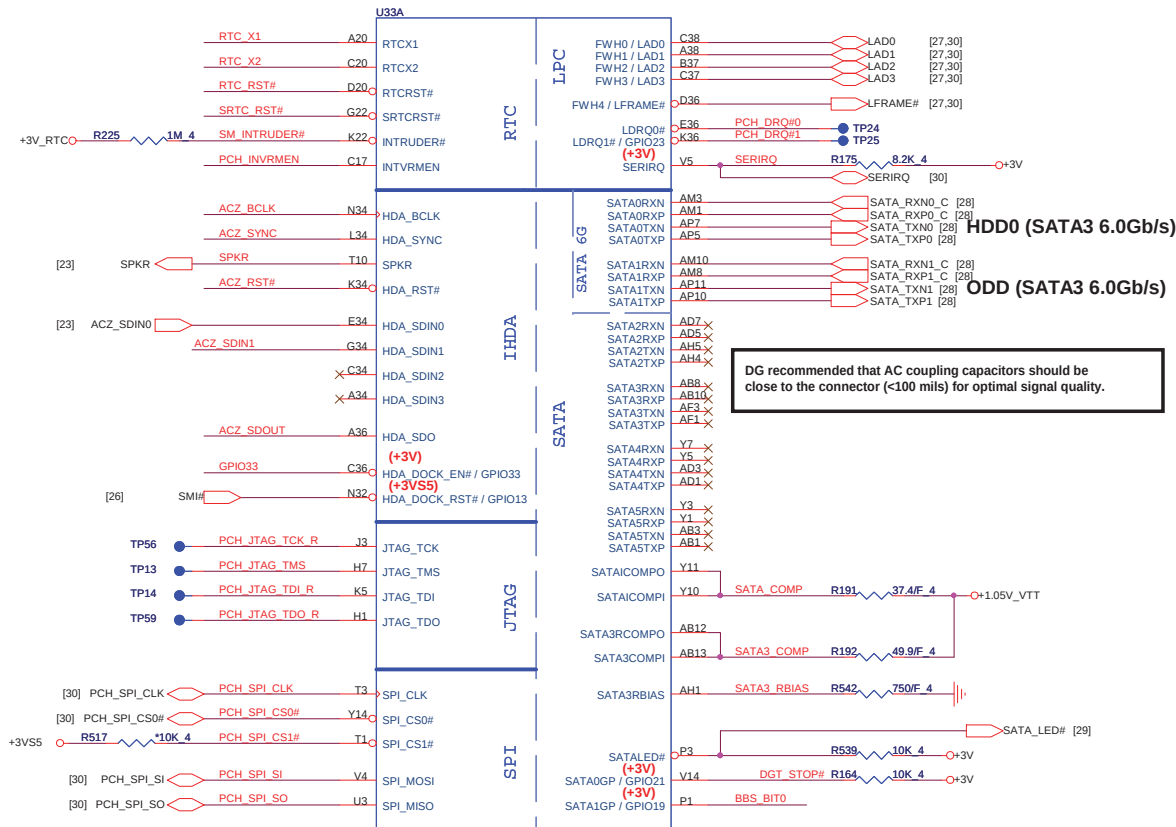
DPWROK FOR DSW



PROJECT : SWH
Quanta Computer Inc.

Size Custom	Document Number PCH 1/6 (DMI/FDI/VIDEO)	Rev 1A
Date: Monday, October 25, 2010		Sheet 6 of 41

Cougar Point (HDA, JTAG, SATA)

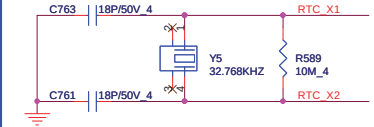


PCH Strap Table

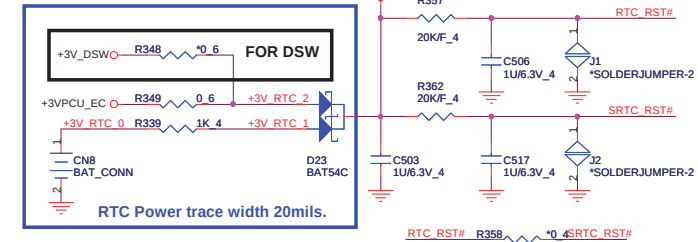
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R174 1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R617 1K 4 R627 10K 4 +3V PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R581 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R597 1K 4 8/24 modify GPIO33_E [30]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R518 1K 4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R615 1K 4 BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R190 1K 4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R533 2.2K 4 R553 4.7K 4 NV_CLE [8] N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5 R277 1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	8/24 modify GPIO33_E ACZ_SDOUT R598 1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R561 1K 4 ICC_EN# [9]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R157 1K 4 PLL_ODVR_EN [9]
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R251 1K 4 +3V

RTC Clock 32.768KHz

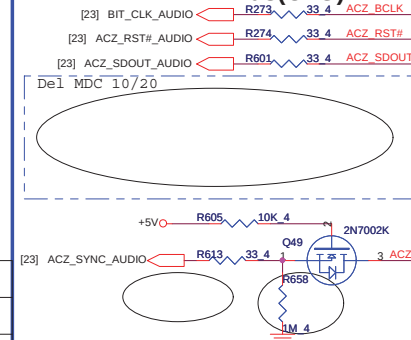
07



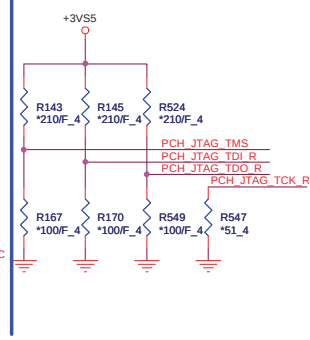
RTC Circuitry(RTC)



HDA Bus(CLG)

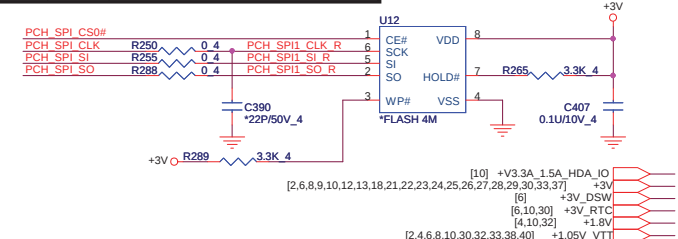


PCH JTAG Debug(CLG)



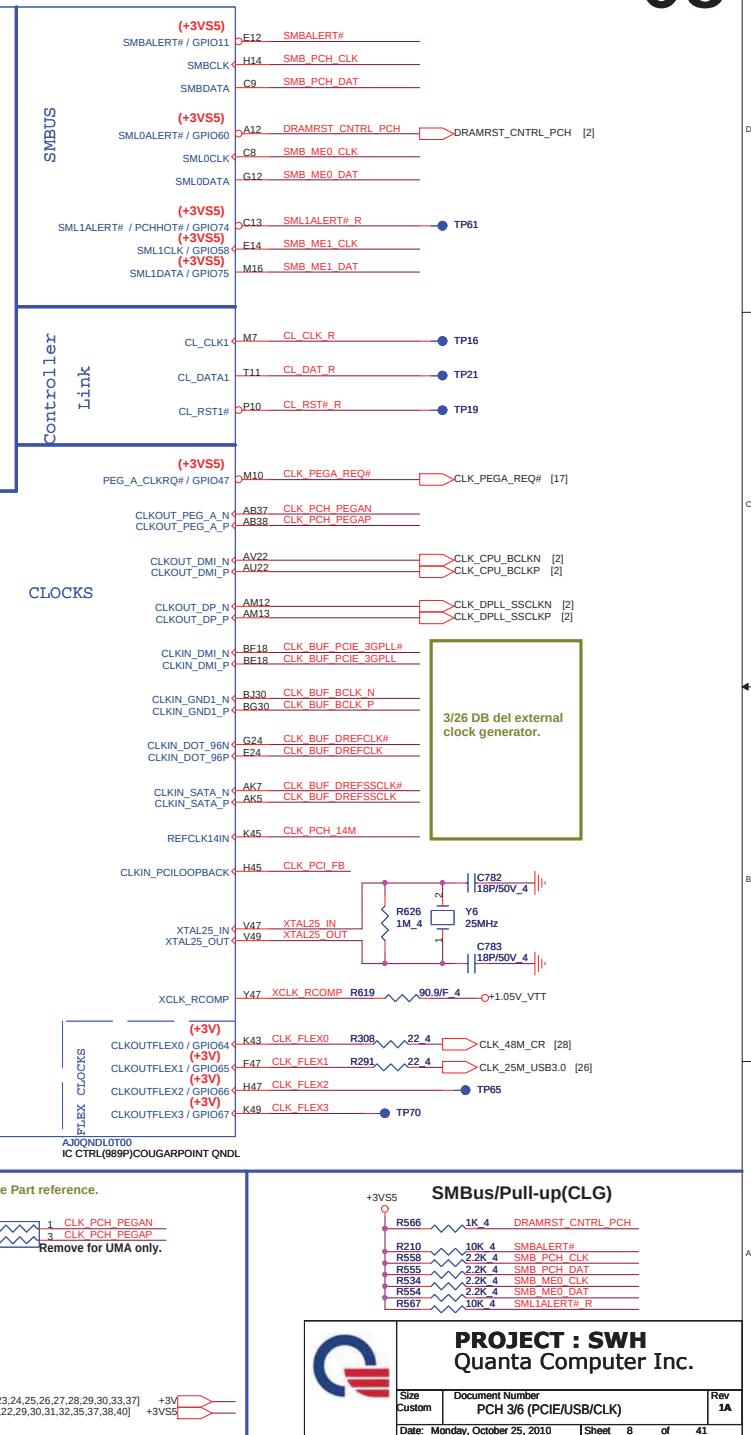
Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH SPI ROM(CLG)

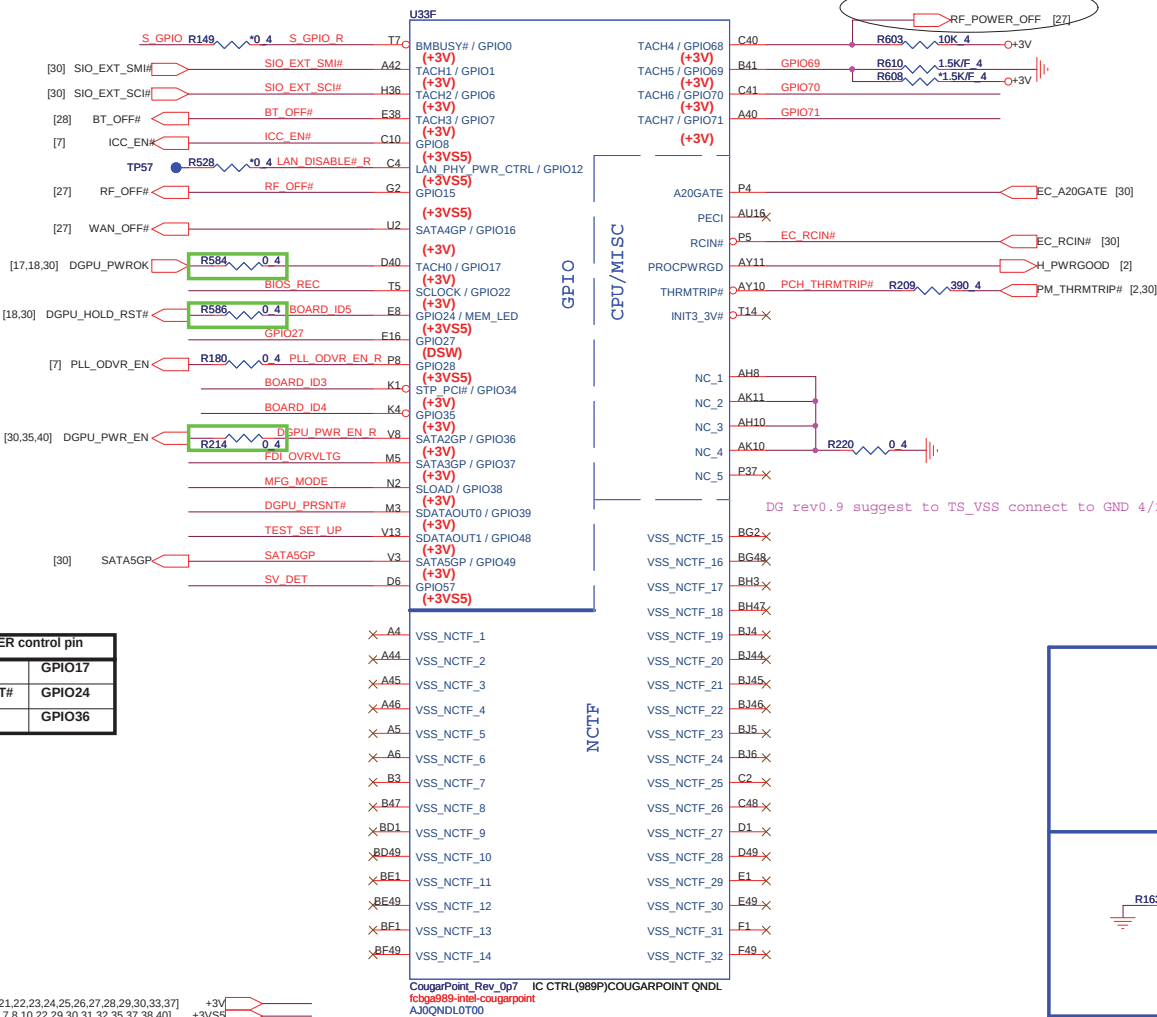


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Quanta Computer Inc.

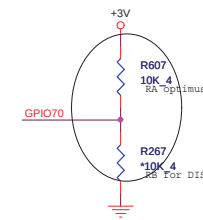
Size	Custom	Document Number	PCH 2/6 (SATA/HDA/SPI)	Rev	1A
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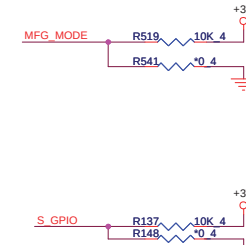
Cougar Point (GPIO,VSS_NCTF,RSVD)



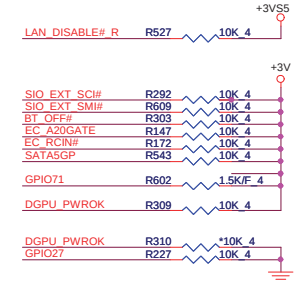
Clock Gen Power OK (CLG)



MFG-TEST



GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TLS) cipher suite
 Low = Disable (Default)
 High = Enable

BIOS RECOVERY High = Disable (Default)
 Low = Enable

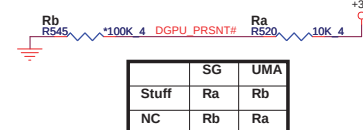
TEST SET UP
 High = Strong (Default)

TEST DETECT
 Low = Default

DGPU_PWR_EN R
 DMI TERMINATION VOLTAGE OVERRIDE
 Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI OVRVLTG
 FDI TERMINATION VOLTAGE OVERRIDE
 LOW - Tx, Rx terminated to same voltage

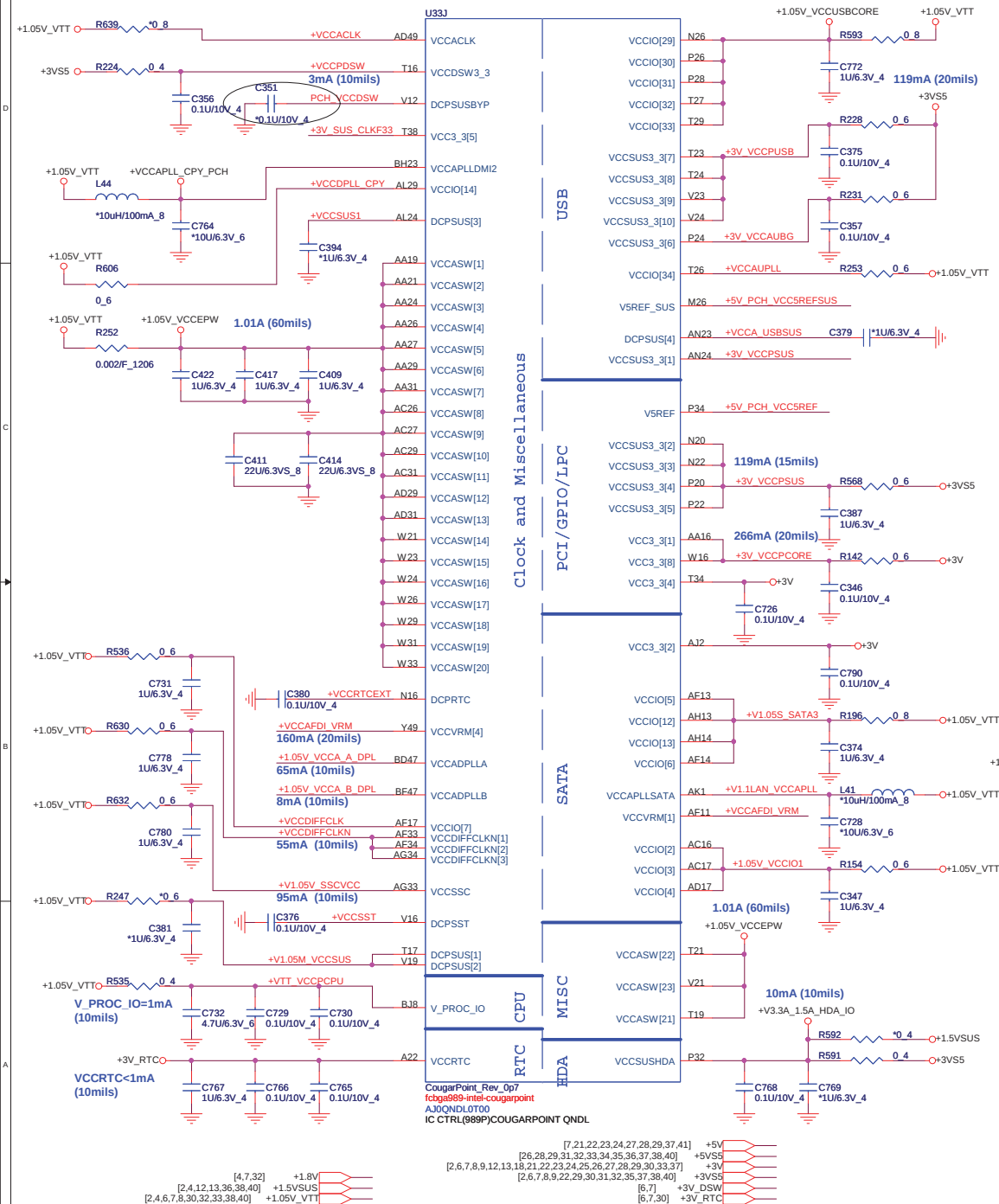
GFX Present



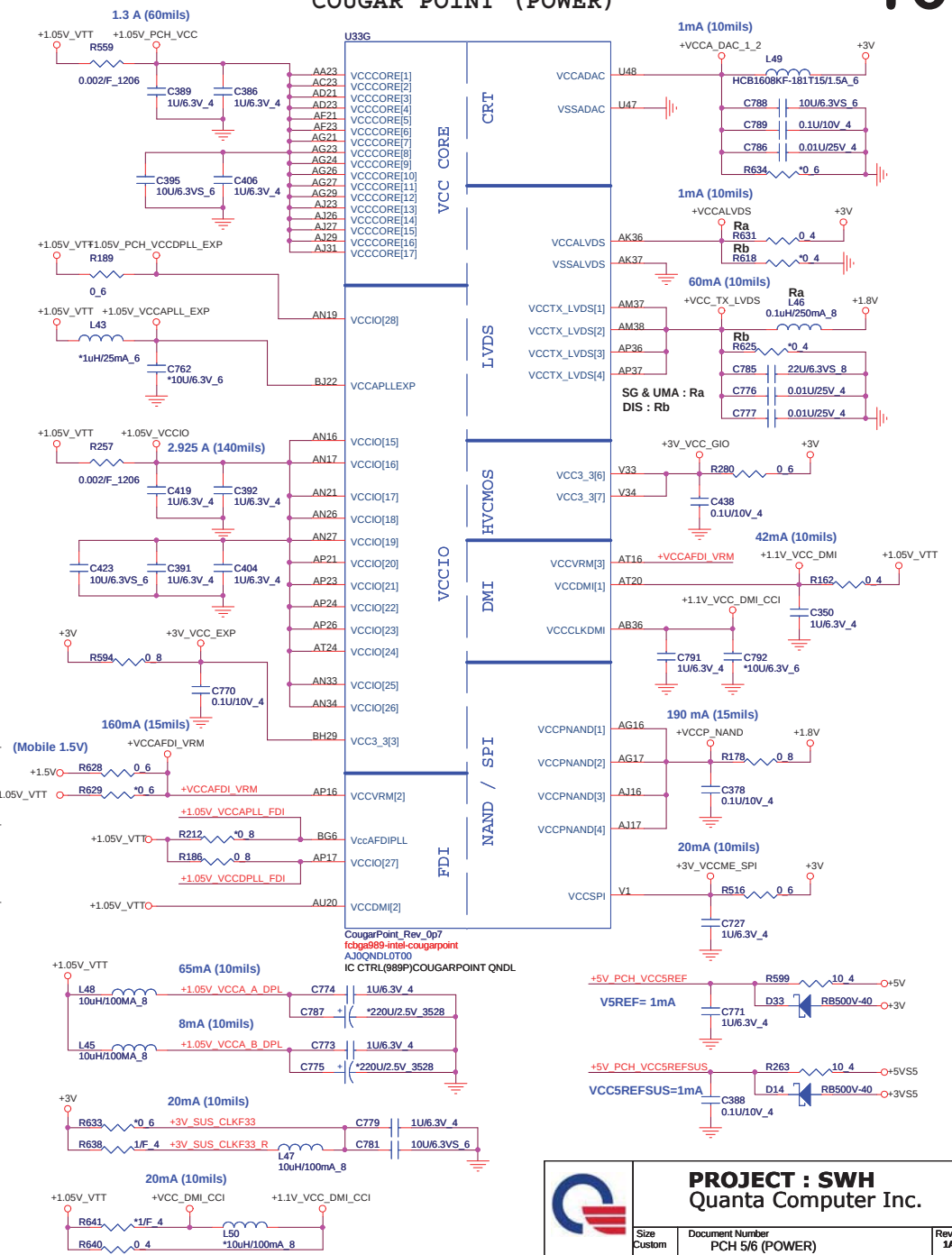
PROJECT : SWH
Quanta Computer Inc.

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
Date: Monday, October 25, 2010	Sheet 9 of 41	

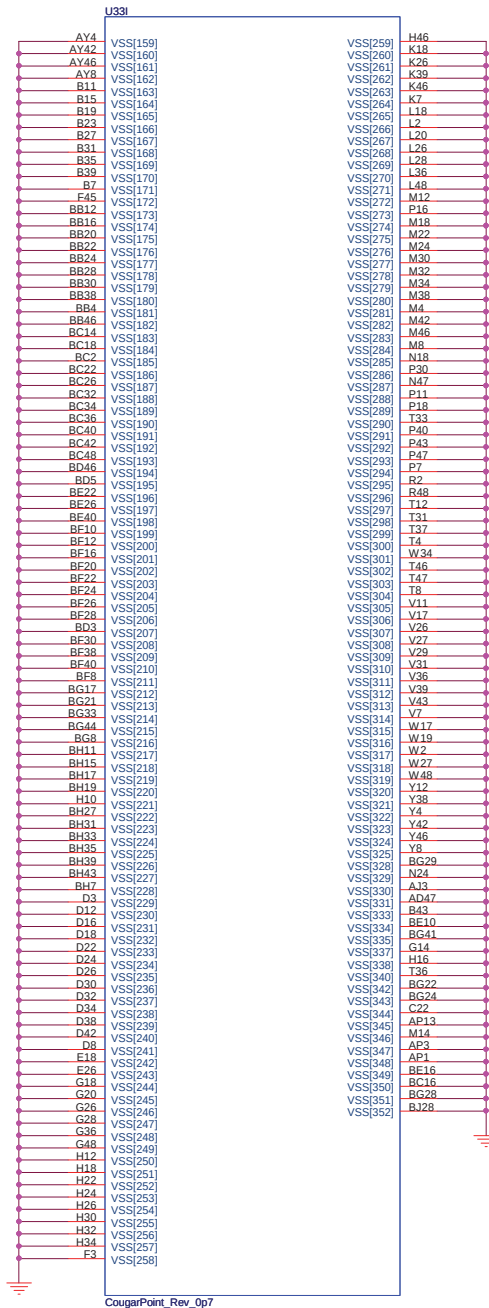
Cougar Point-M (POWER)



COUGAR POINT (POWER)

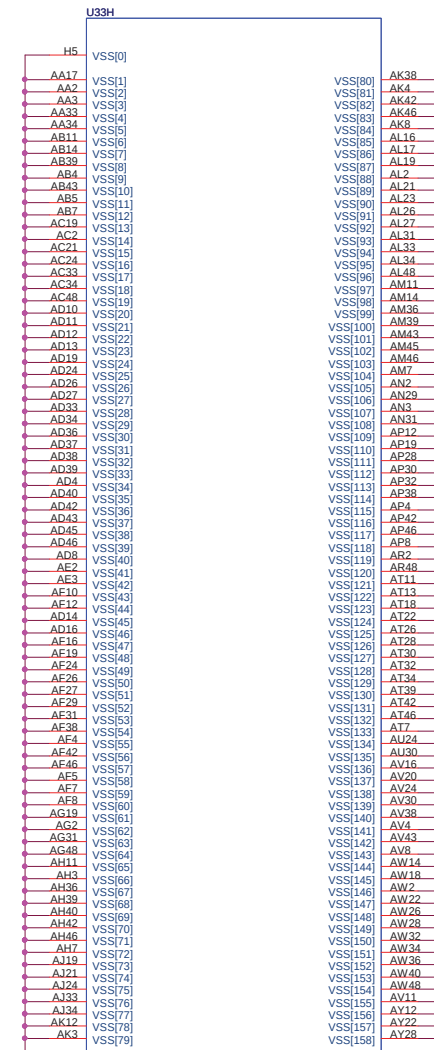


IBEX PEAK-M (GND)

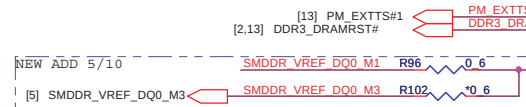
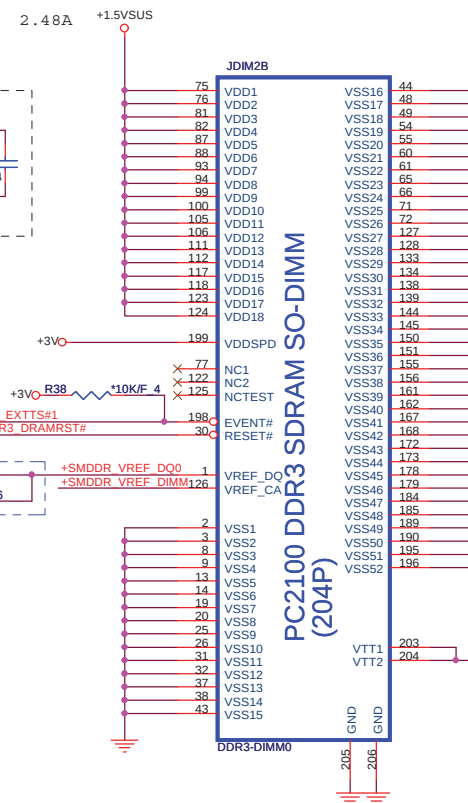
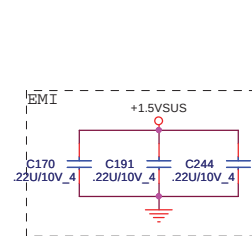
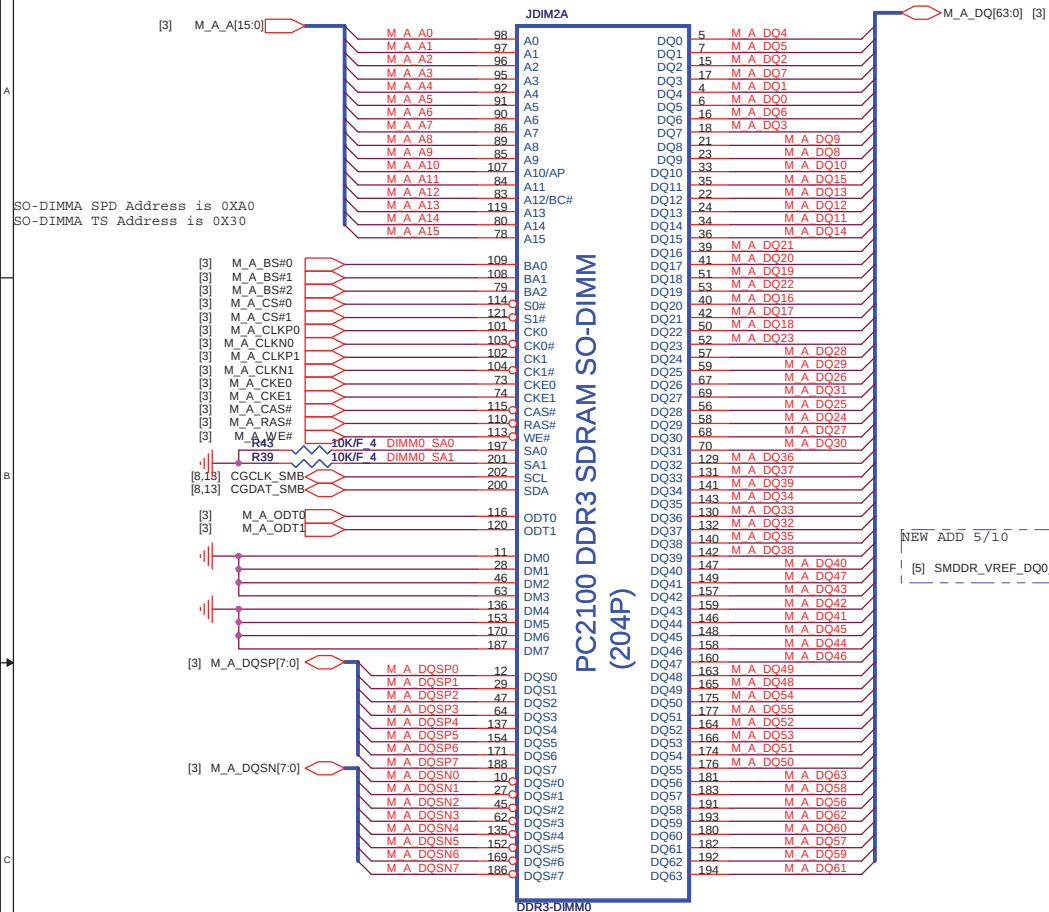


CougarPoint_Rev_0p7

IBEX PEAK-M (GND)

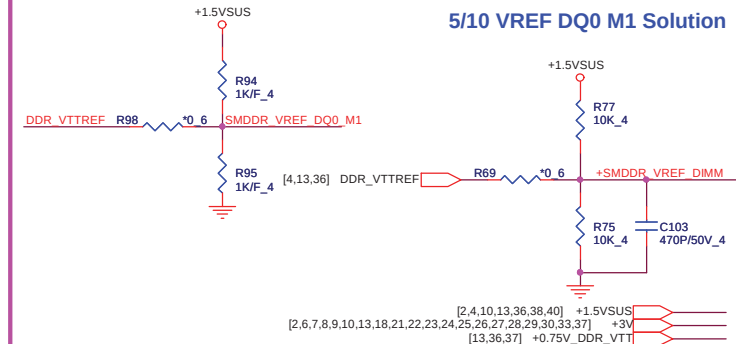


CougarPoint_Rev_0p7

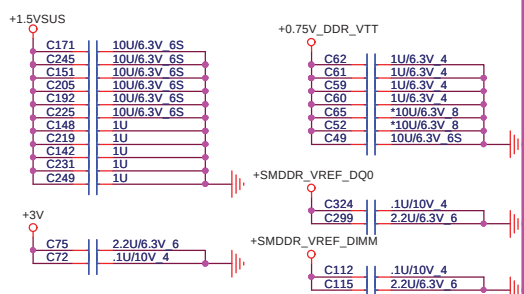


6/22:Document Number: 436996
Intel remove the DDR3 verf M2
circuitry

VREF DQ0 M2 Solution



Place these Caps near So-Dimm0.^{11/6}

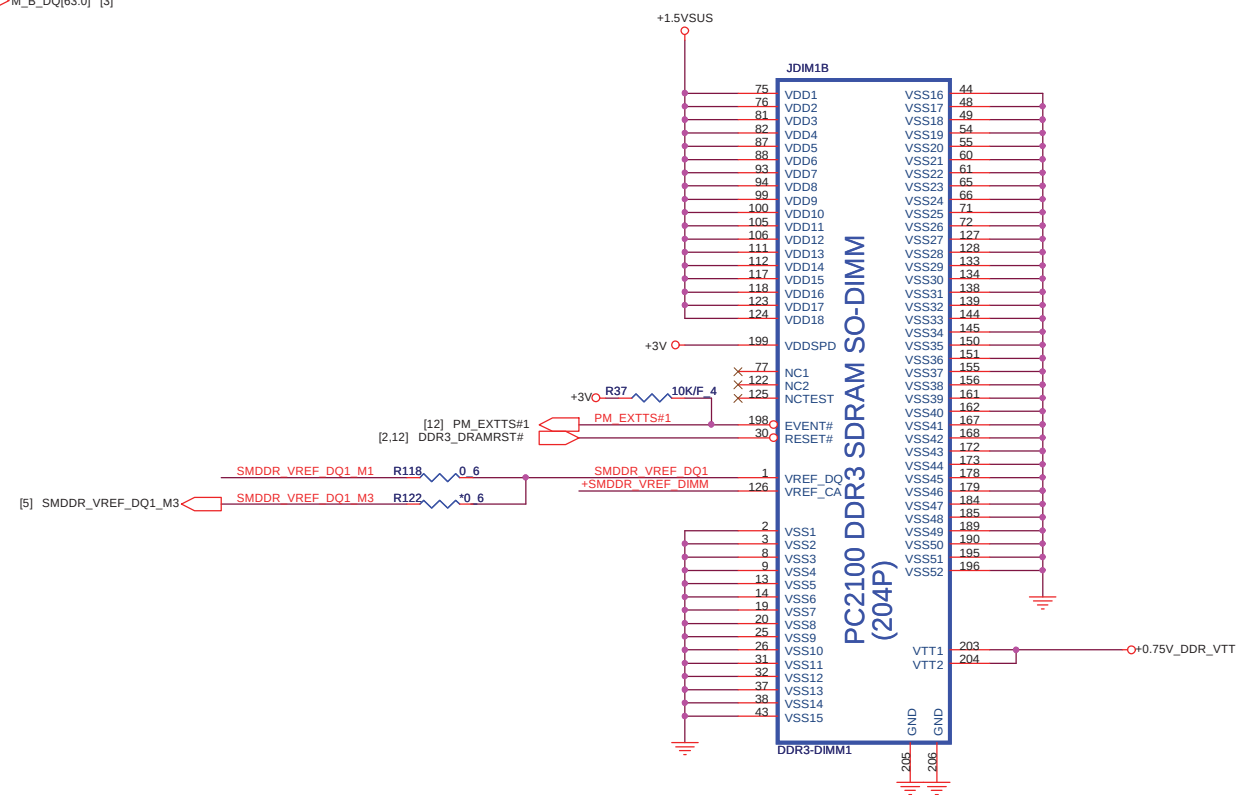
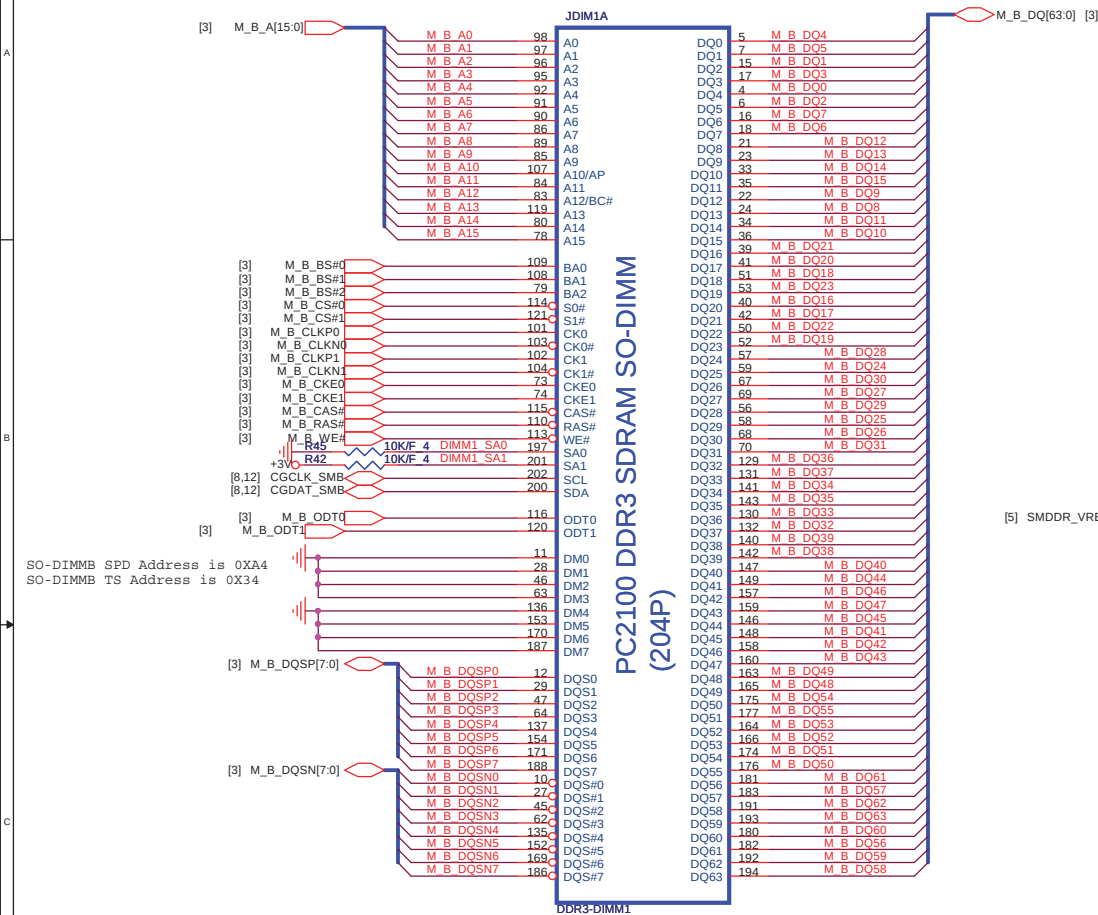


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PROJECT : SWH
Quanta Computer Inc.

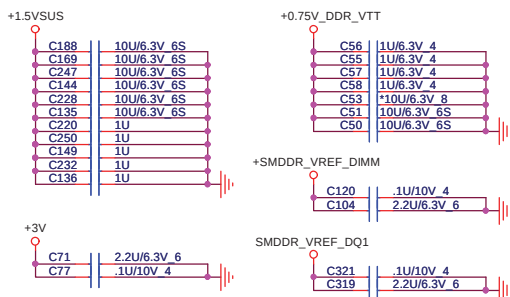
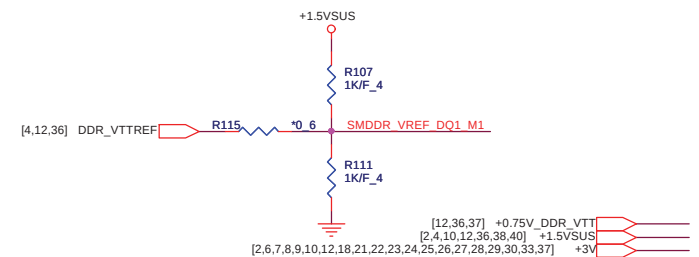
Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A
Date: Monday, October 25, 2010	Sheet 12 of 41	



6/22:Document Number: 436996
Intel remove the DDR3 verf M2
circuitry

VREF DQ1 M2 Solution

VREF DQ1 M1 Solution

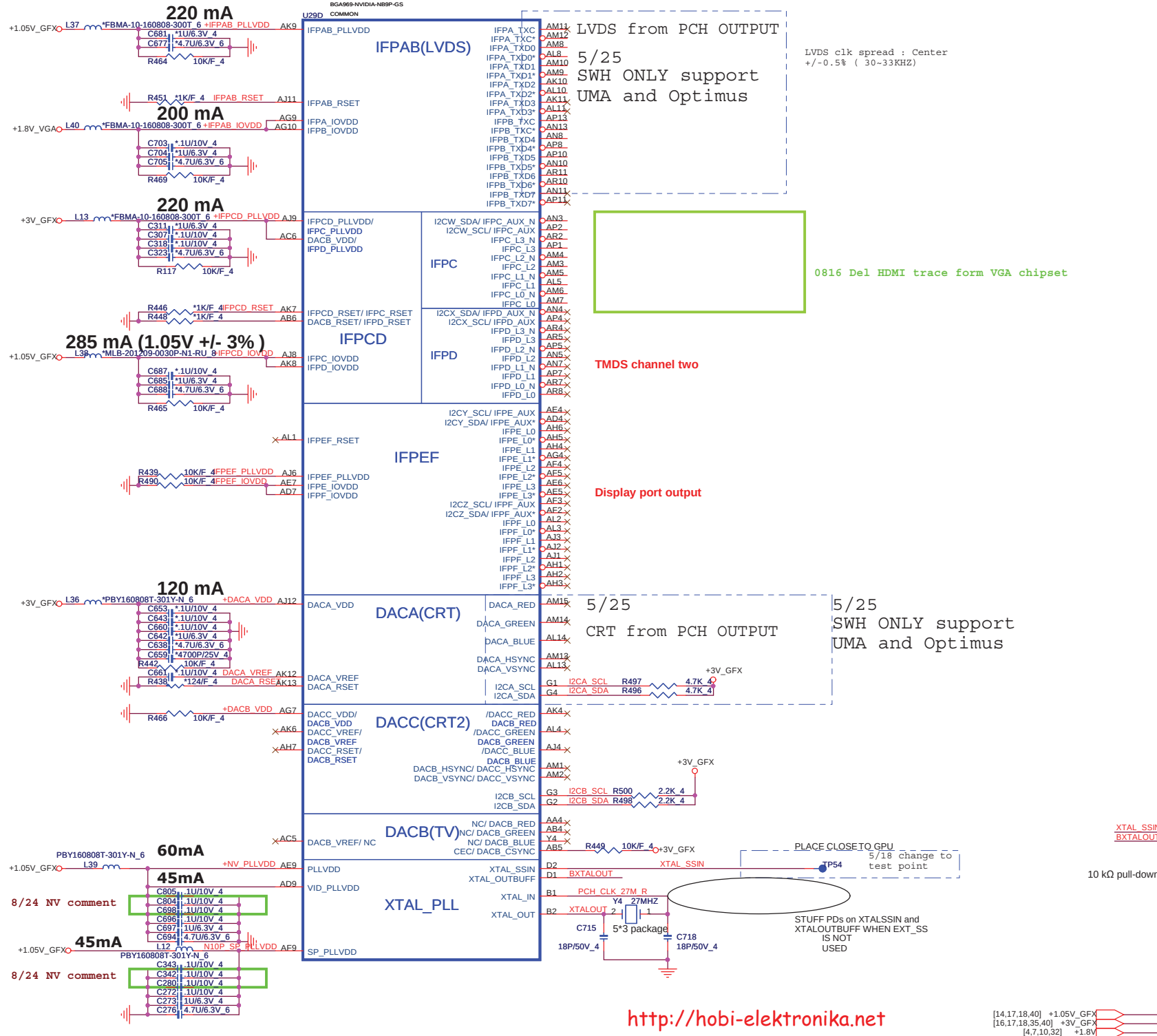


<http://hobi-elektronika.net>



PROJECT : SWH
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM-1	Rev 1A
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Fermi :
1 : C149 , C80 stuff 0 ohm
2 : R151 , R172 unstuff

8/25 NV comment

8/25 NV comment

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Default: Hynix VRAM

4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK 417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	Reserved	Reserved	Reserved	PD 10K
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 15K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 20K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	
0101	Reserved	Reserved	Reserved	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 ^{11/13}
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL ^{11/13}
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

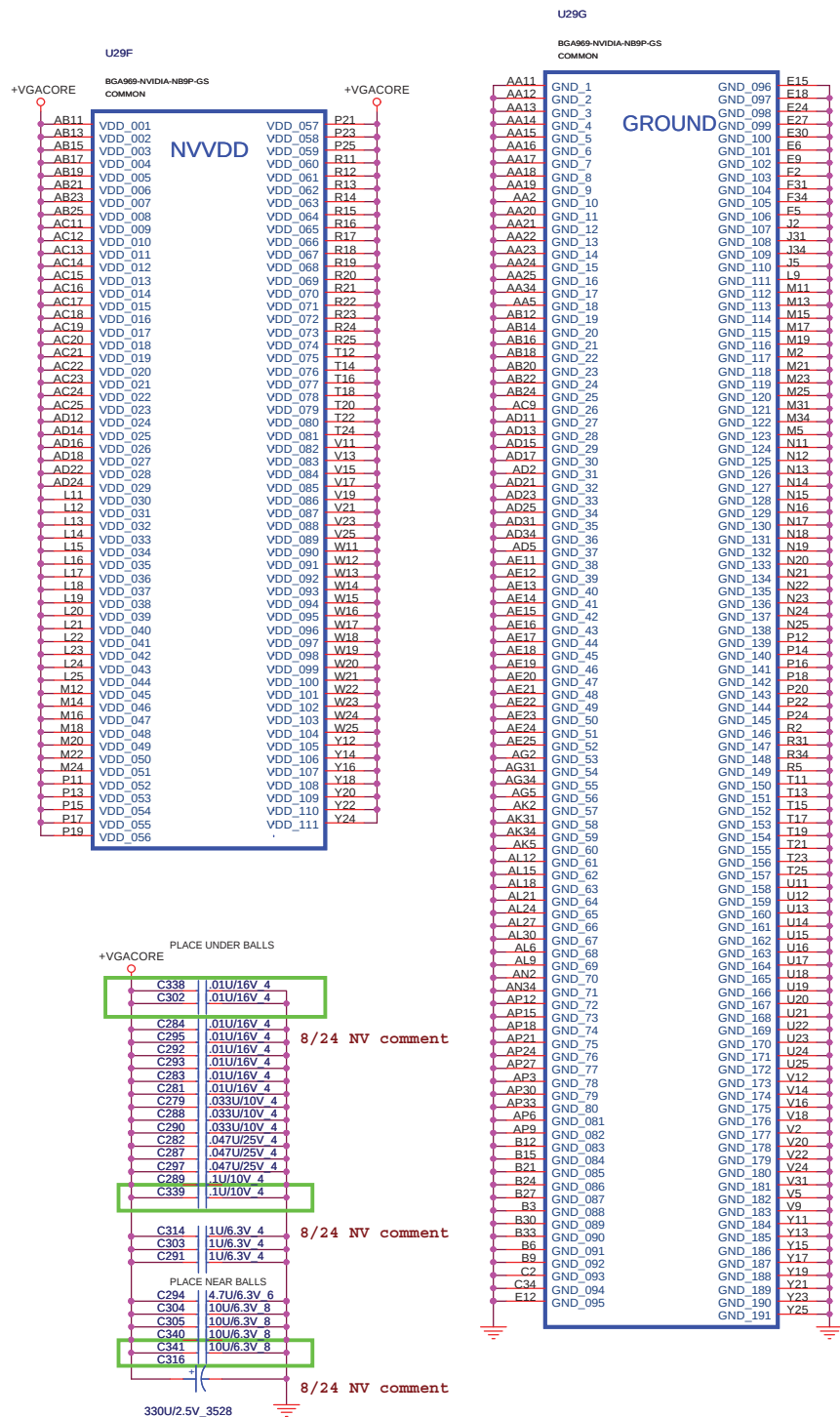


PROJECT : SWH
Quanta Computer Inc.

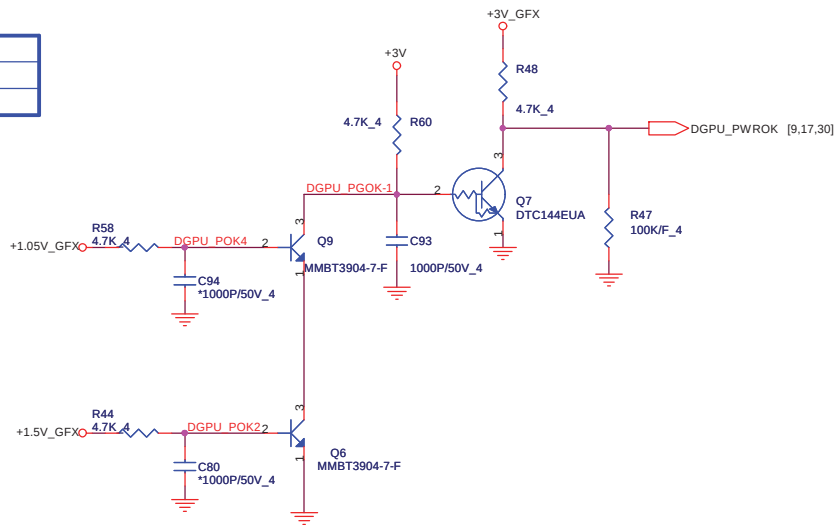
Size	Document Number	Rev
Custom	N11x-Fermi	1A
Date: Monday, October 25, 2010	Sheet 16 of 41	

<http://hobi-elektronika.net>
[15,17,18,35,40] +3V_GFX

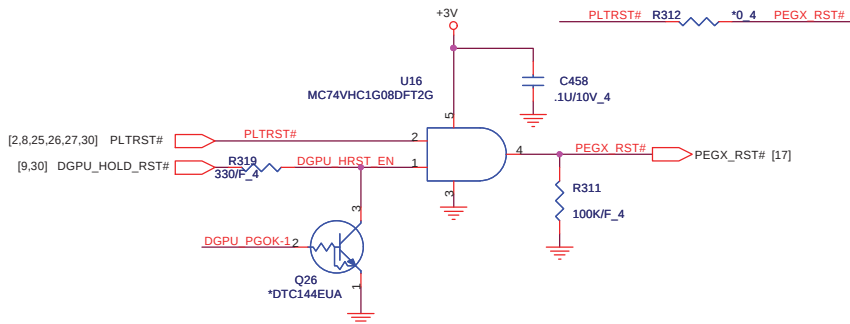




SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

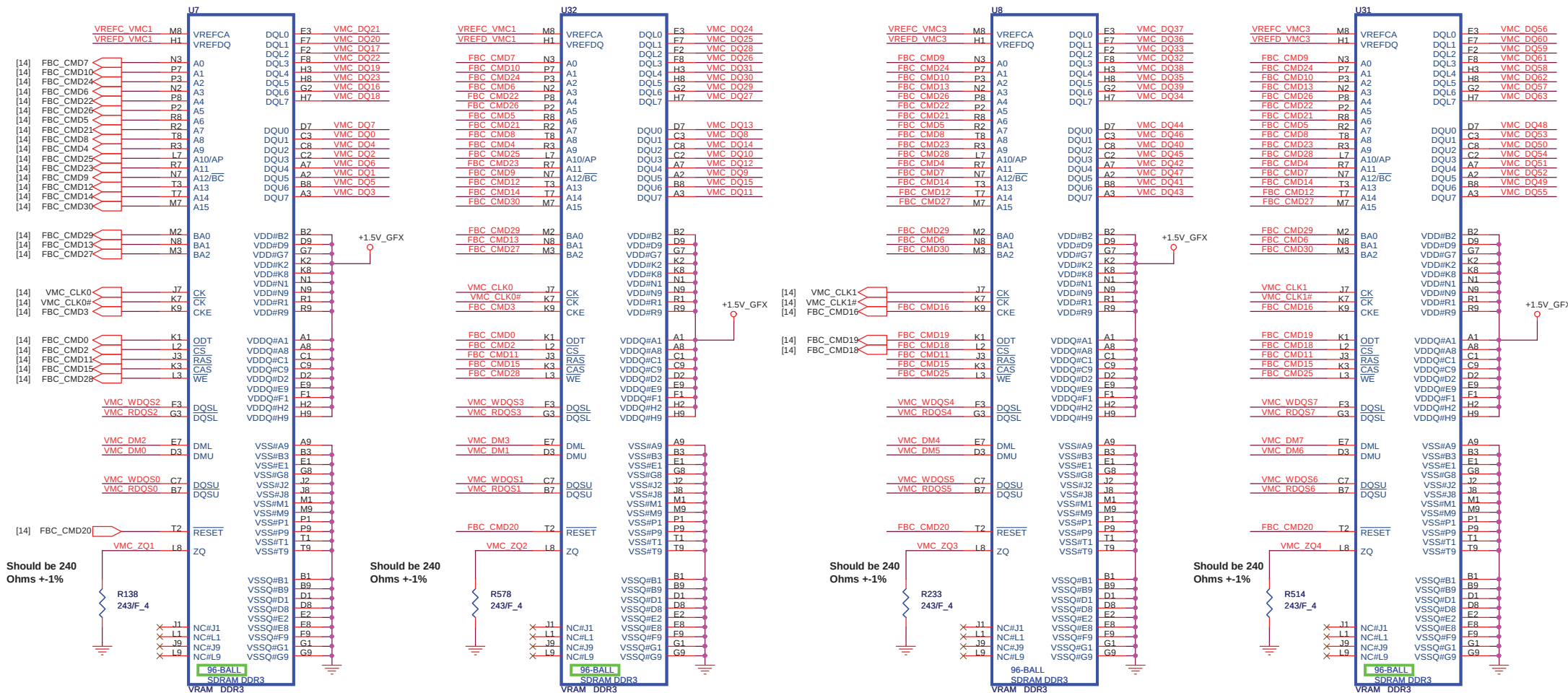


Discrete Only



[14] VMC_DQ[63..0]
[14] VMC_DM[7..0]
[14] VMC_WDQS[7..0]
[14] VMC_RDQS[7..0]

CHANNEL B: 256MB/512MB DDR3



Should be 240 Ohms +-1%

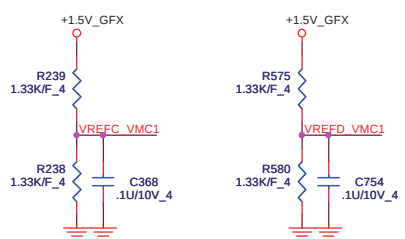
VMC_CLK0

R230 162/F_4

Fermi : Change to 160 ohm

1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)

2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)



Should be 240 Ohms +-1%

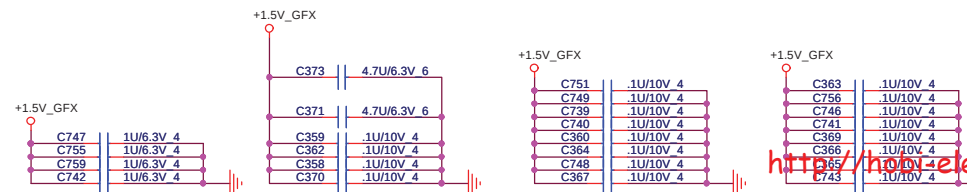
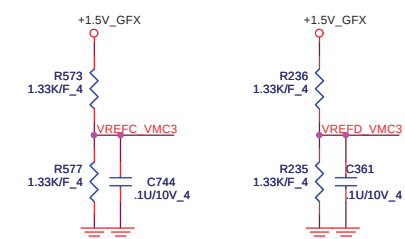
VMC_CLK1

R229 162/F_4

Fermi : Change to 160 ohm

1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)

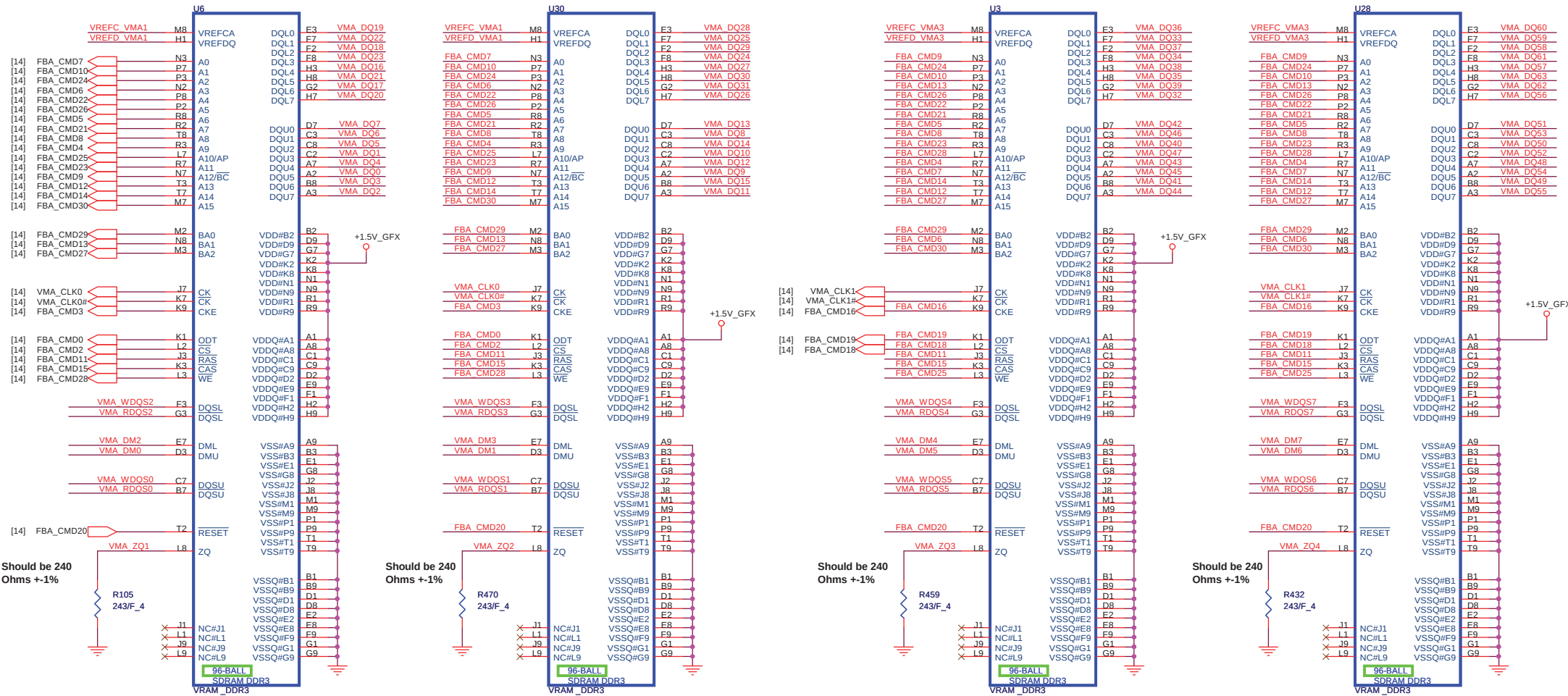
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)



[14] FBC_CMD17 FBC_CMD17 TP11

[14] FBC_CMD1 FBC_CMD1 TP10

CHANNEL A: 256MB/512MB DDR3



VMA CLK0

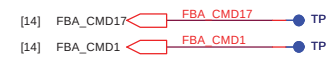
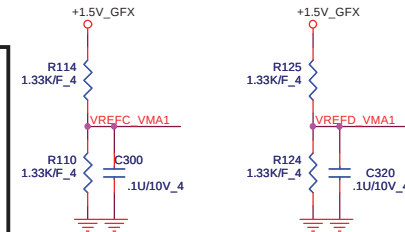
R119 162F_4 VMA CLK0#

Fermi : Change to 160 ohm

1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)

2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)

CS11622FB15 RES CHIP 162 1/16W +-1% (0402) EP (V1)



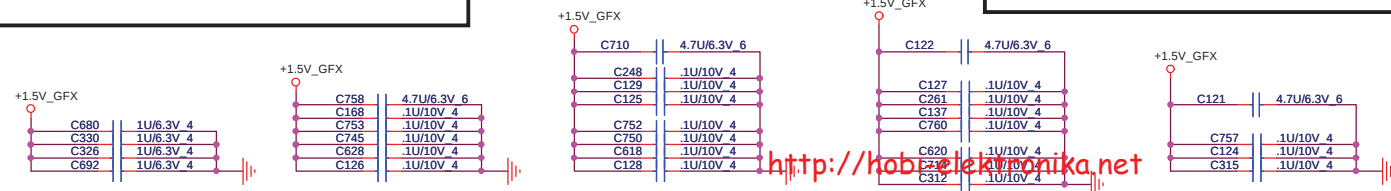
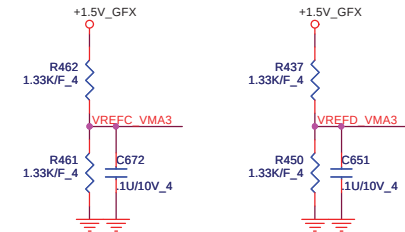
VMA CLK1

R79 162F_4 VMA CLK1#

Fermi : Change to 160 ohm

1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)

2 : CS11622FB07 ,RES CHIP 162 1/16W +-1% (0402)



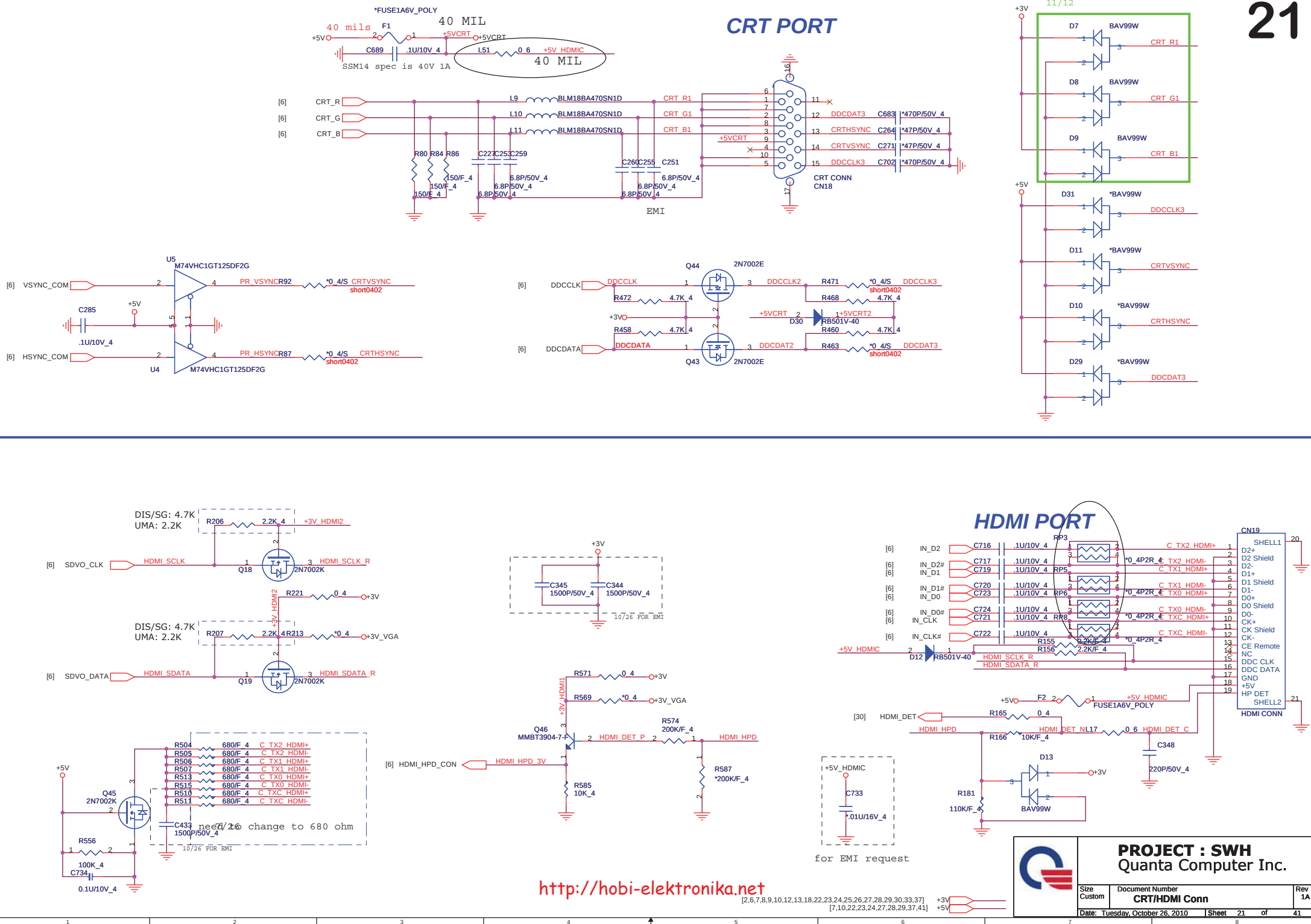
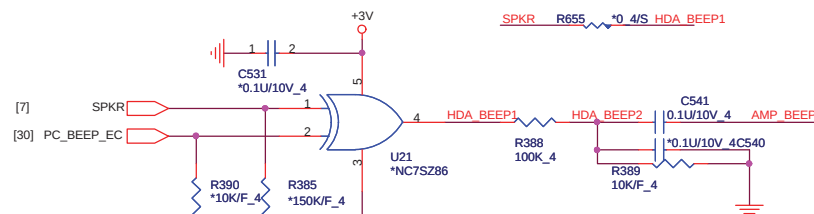
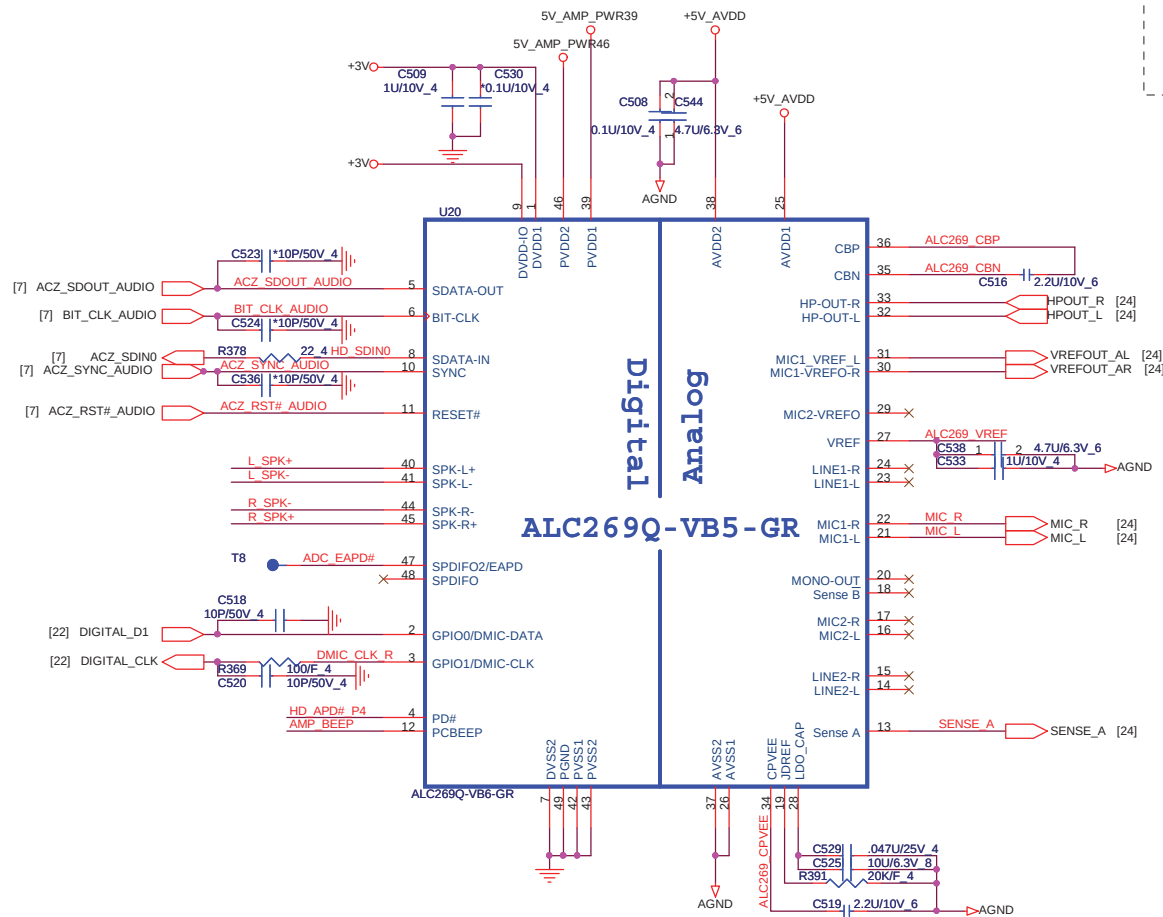
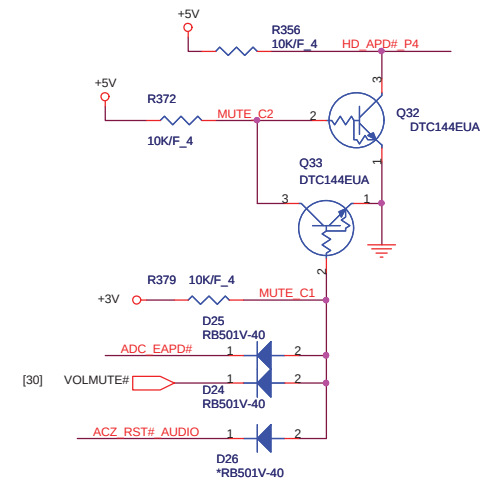
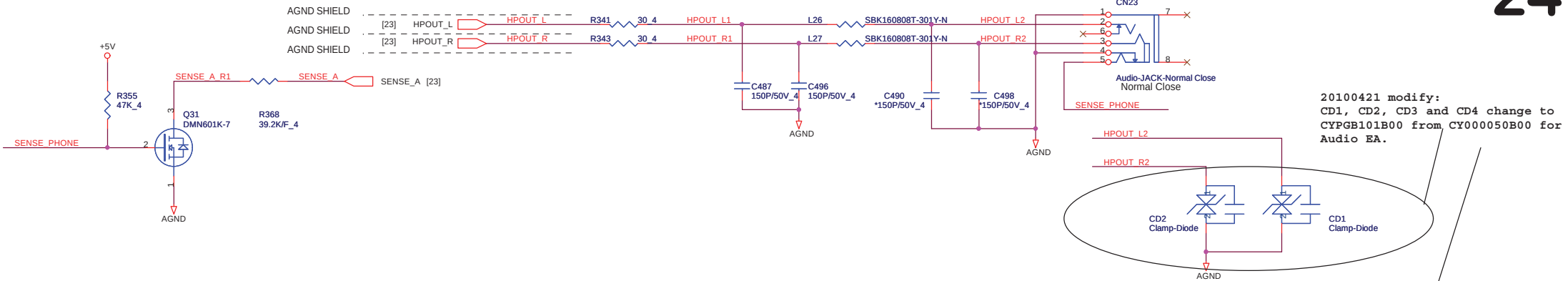


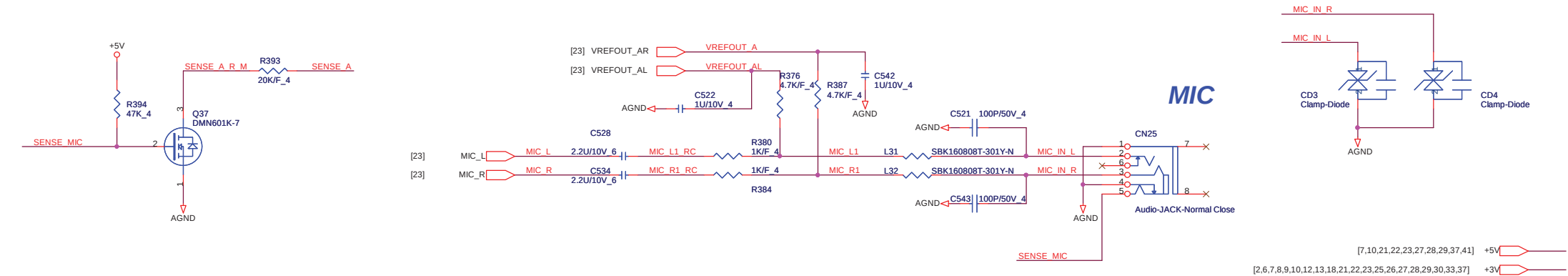
Diagram illustrating the speaker connection for the SBK160808T-221Y-N components. The components are connected to a common ground through capacitors C382, C383, C384, and C385. The output is connected to a 4-pin connector labeled CN6, with pins 1, 2, 3, and 4 labeled L SPK-, L SPK+, R SPK-, and R SPK+ respectively. The connector is also labeled INT SPEAKER CONN.



Line out



MIC

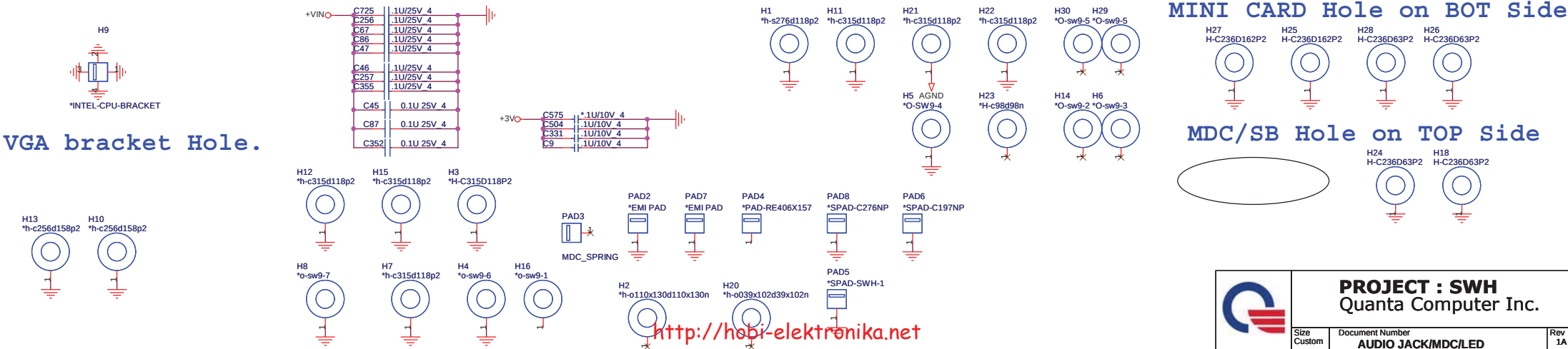


CPU bracket Hole. EMI capacitive

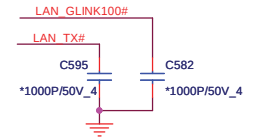
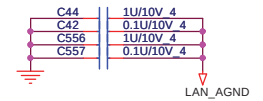
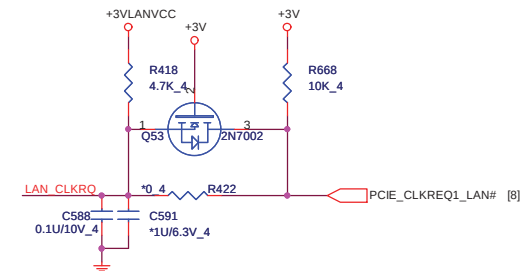
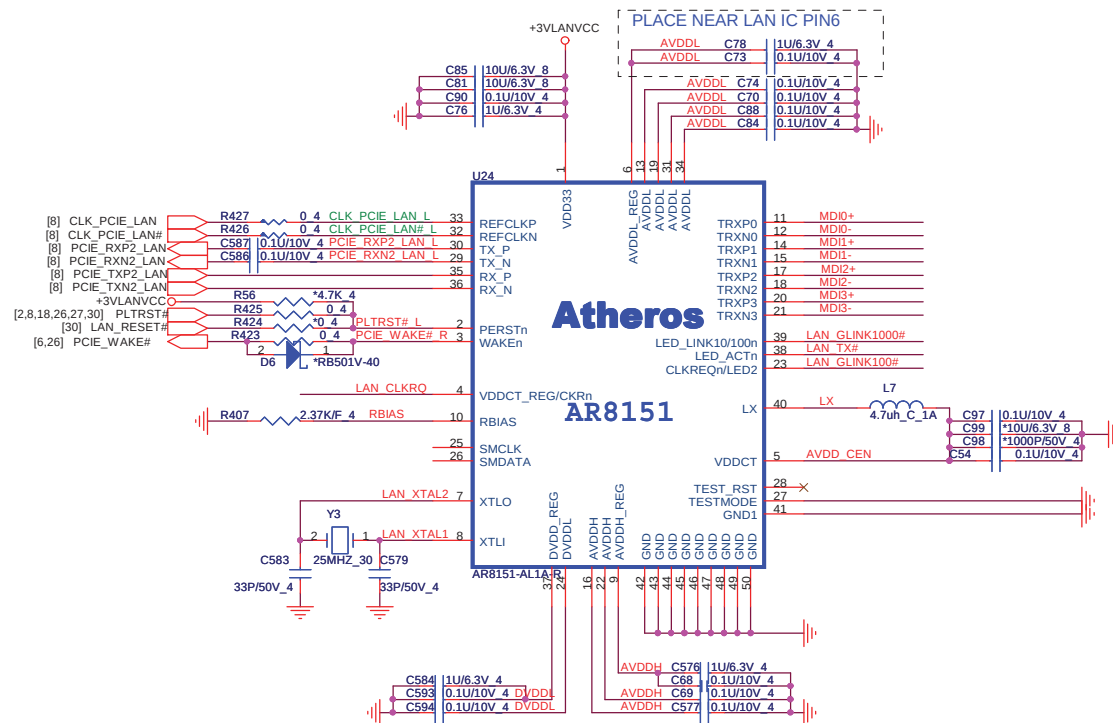
PAD and HOLE

MINI CARD Hole on BOT Side

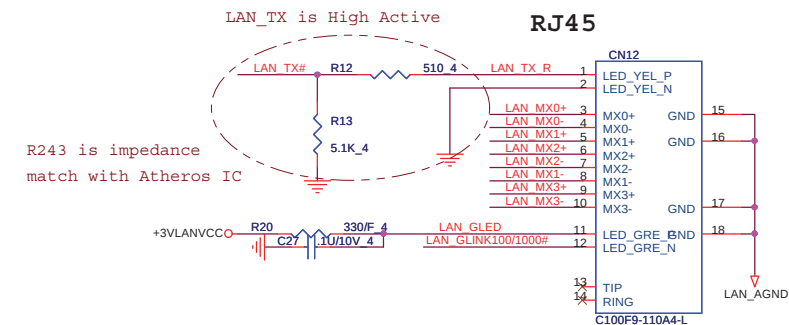
MDC/SB Hole on TOP Side



		PROJECT : SWH	
		Quanta Computer Inc.	
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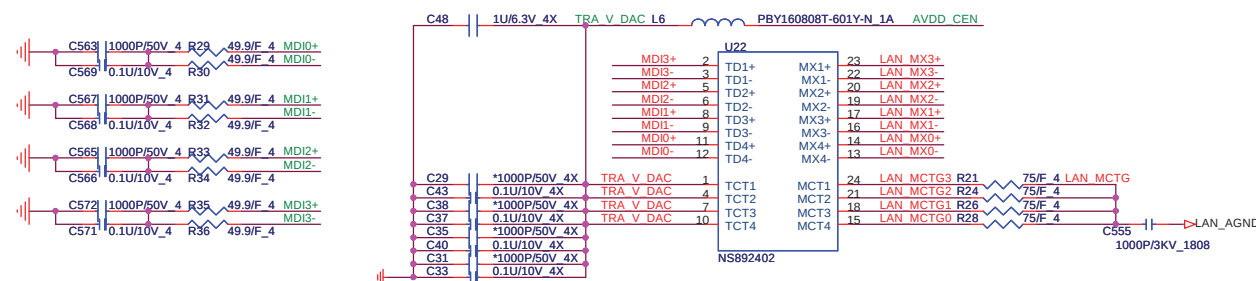


Lan Connector



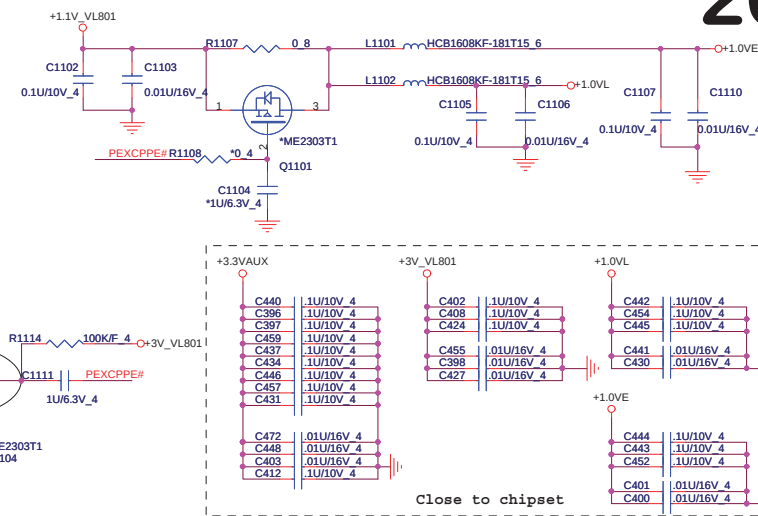
PLACE NEAR LAN IC SIDE

Transformer for 10/100/1000

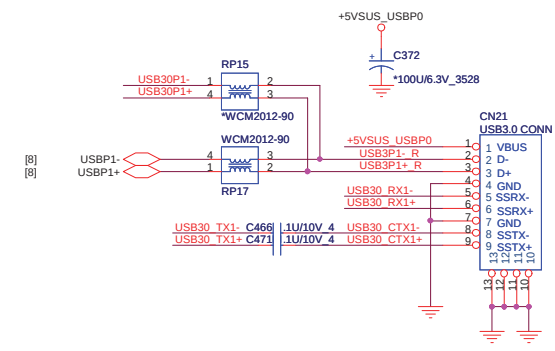


for Atheros

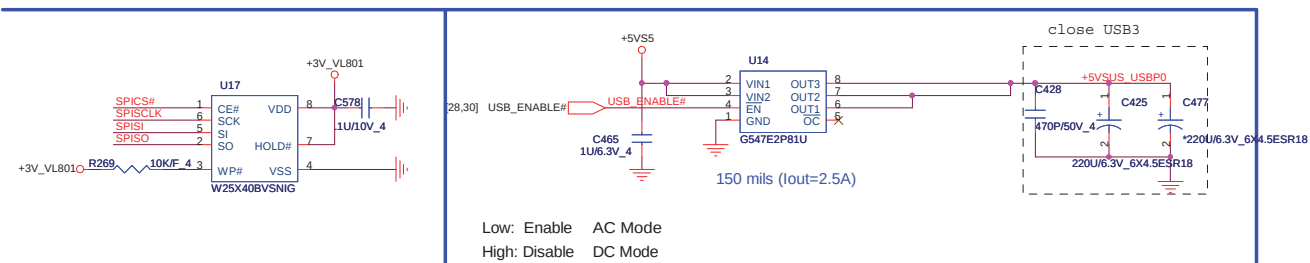
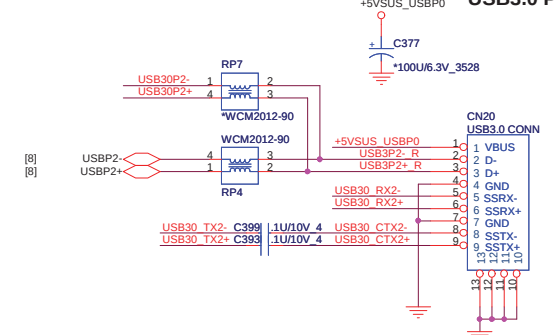
NS892402: GIGABIT DB0ZB1LAN04
NS892405: 10/100 DB0ZB1LAN04



USB3.0 PORT1

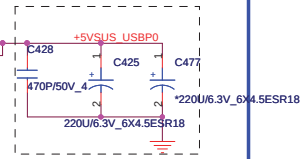


USB3.0 PORT2



Low: Enable	AC Mode
High: Disable	DC Mode

```
close USB3
```

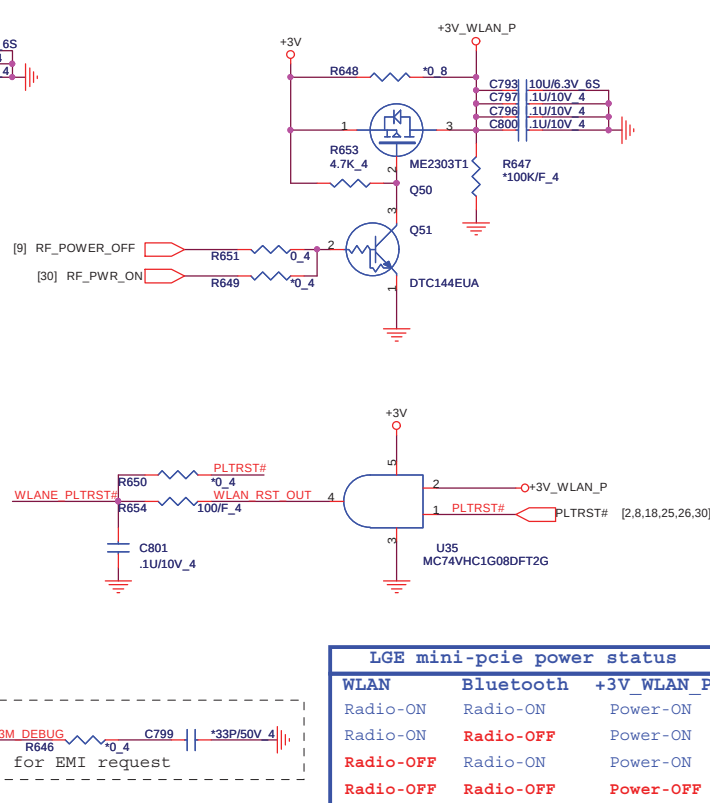


150 mils (I_{out}=2.5A)



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The image contains three separate circuit diagrams, each for a different pin on the WLAN module. Each diagram shows a 2N7002 MOSFET used as a switch, controlled by a 3V3 signal from the module.

- PIN44:** The 3V3_WLAN_P signal is connected to the gate of the MOSFET. The drain is connected to the WLAN_LED# signal line. The source is connected to ground.
- PIN7:** The 3V3_WLAN_P signal is connected to the gate of the MOSFET. The drain is connected to the REQ_WLAN# signal line. The source is connected to ground.
- PIN5:** The 3V3_WLAN_P signal is connected to the gate of the MOSFET. The drain is connected to the BT_COMBO_EN# signal line. The source is connected to ground.

FOR KBC DEBUG

+5V $\rightarrow$ R404 $\rightarrow$ 0 6 MINIEC 5V

1208 EC add debug pin

EC_DEBUG1 R405 $\rightarrow$ 0 4

Robson

[8] PCIE_TXP4

[8] PCIE_TXN4

[8] PCIE_RXP4

[8] PCIE_RXN4

[8] CLK_PCIE_WWAN

[8] CLK_PCIE_WWAN#

[8] PCIE_CLK_REQ#

MINICAR_PME#

TP35

TP36

PLTRST#

R40

*10K/F

*0 4/S

+3V

WAN_OFF# [9]

C585

*1U/10V_4

C590

*1U/10V_4

C592

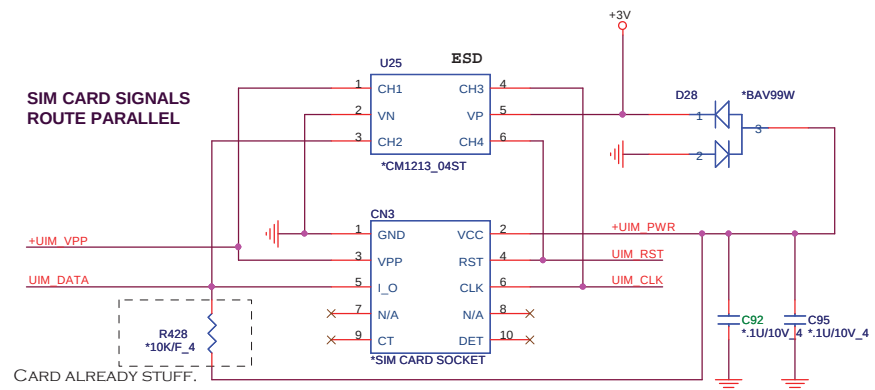
*4.7U/6.3V_6

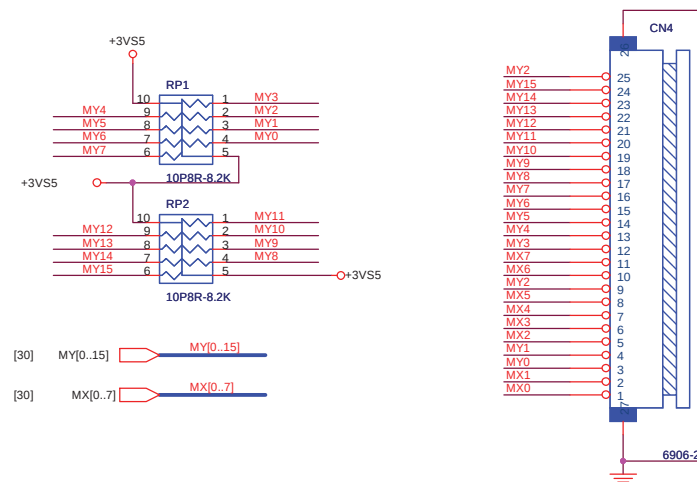
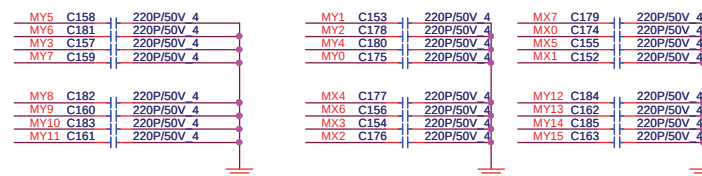
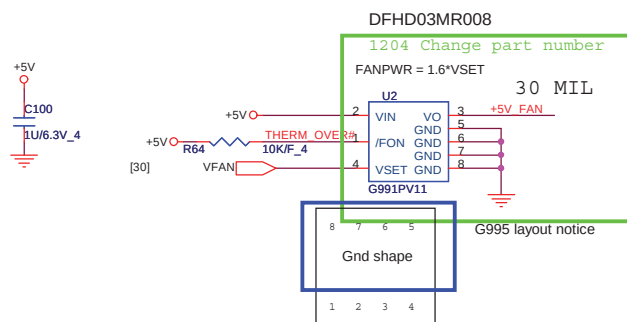
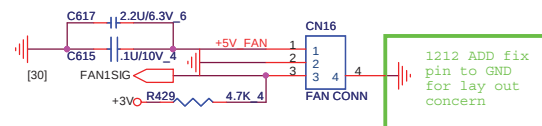
C631 close to CN7

C596

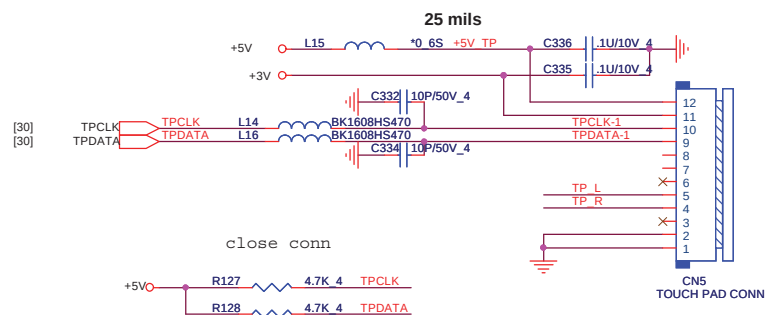
*1U/10V_4

http://hobi-elektronika

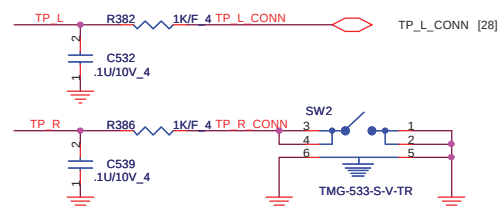




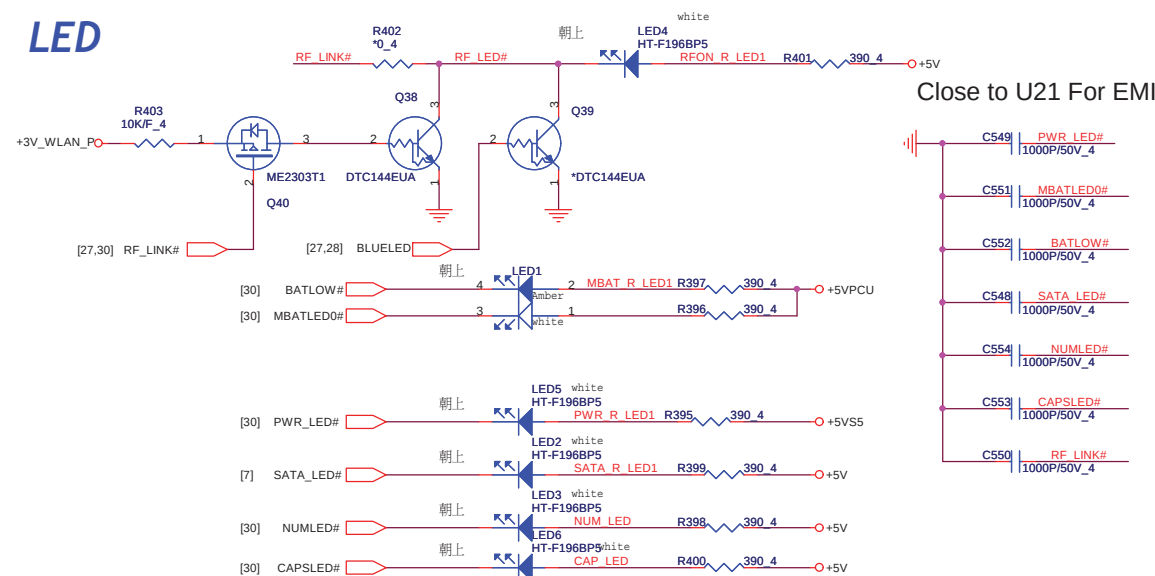
TOUCH PAD CONNECTOR

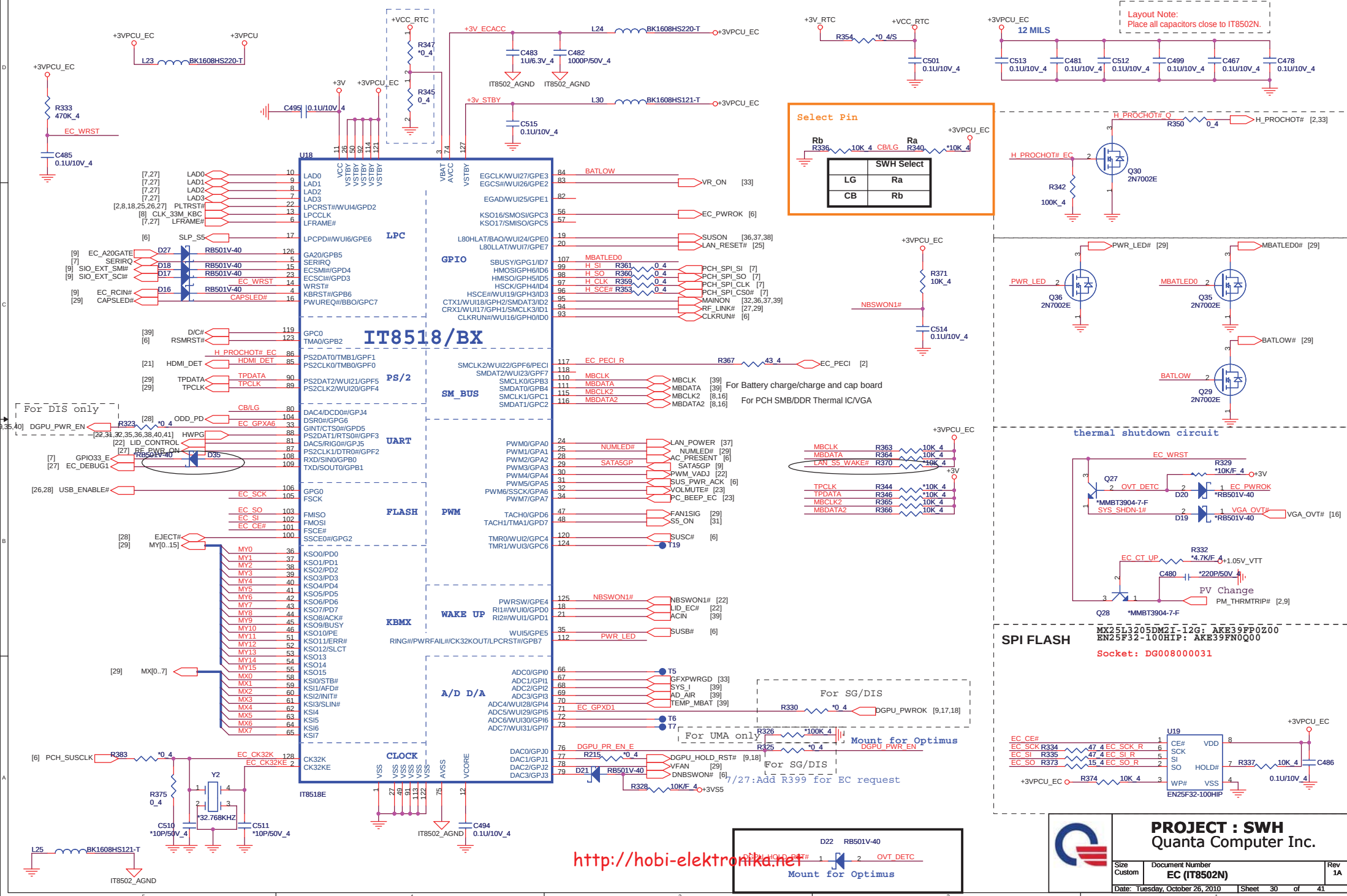


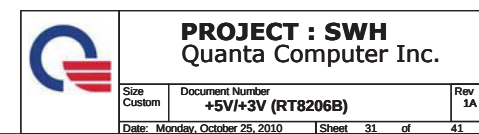
TOUCH PAD L/R SW1,SW2 in QL2 use, SW3,SW4 in SW9 use

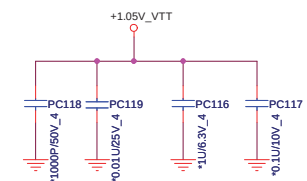
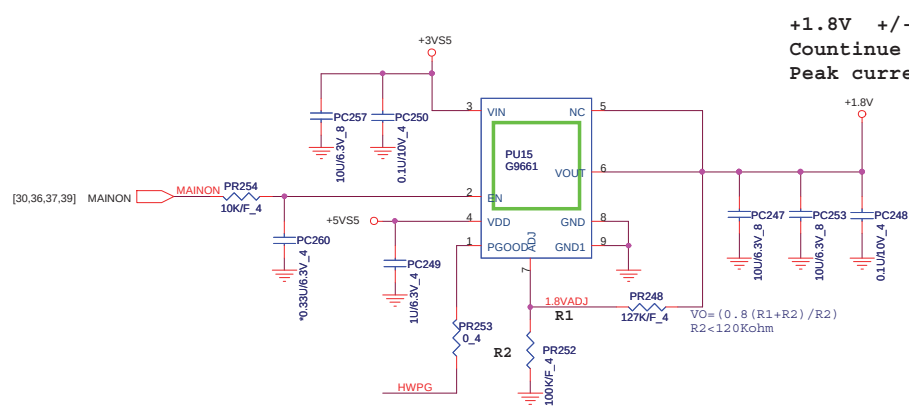
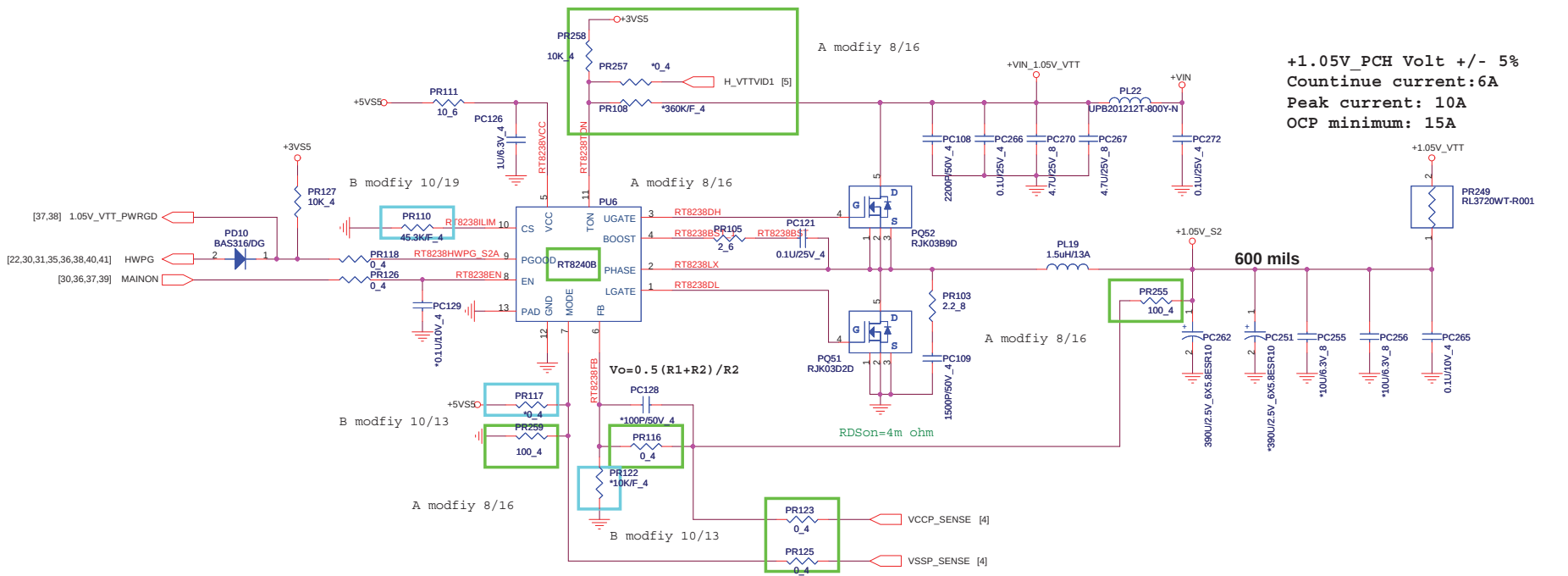


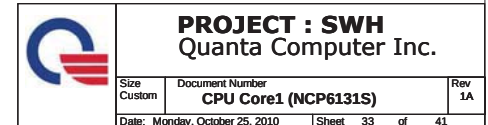
LED

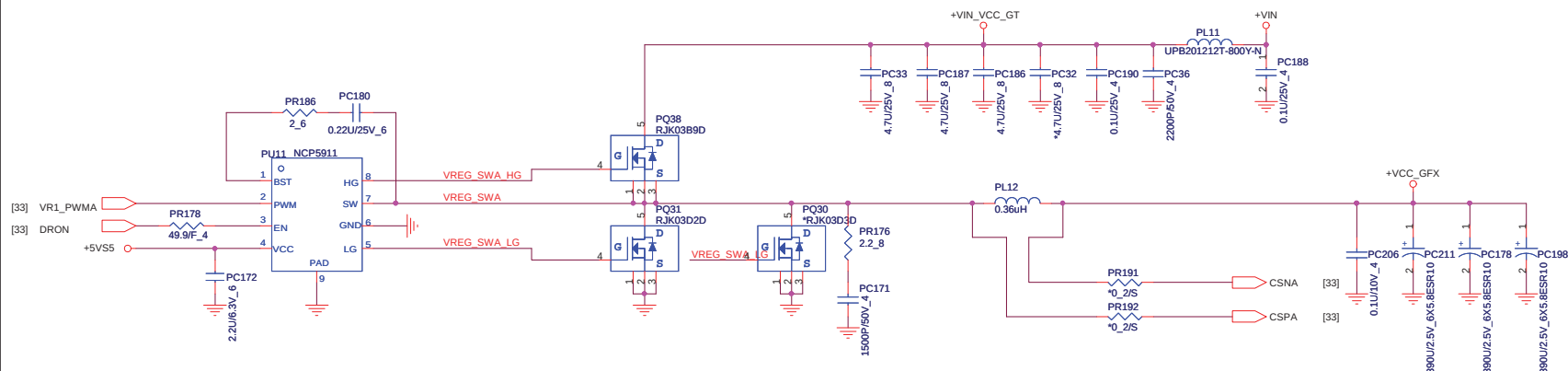
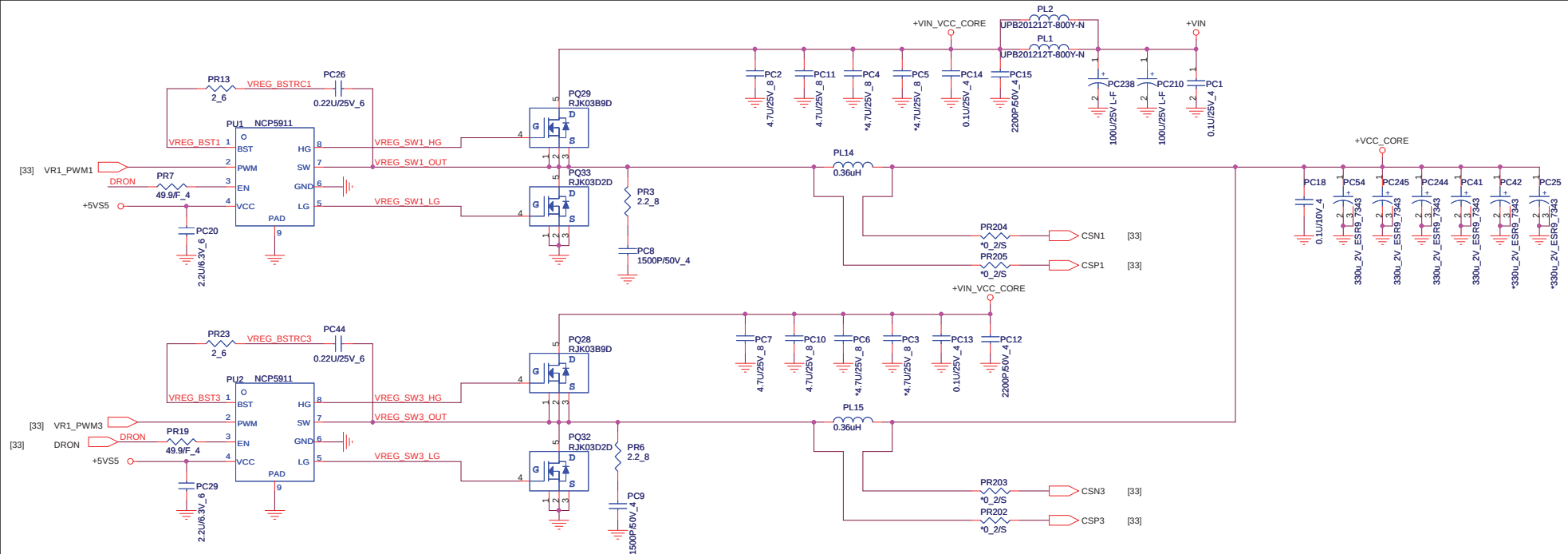




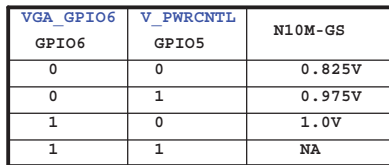




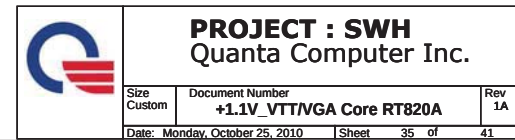


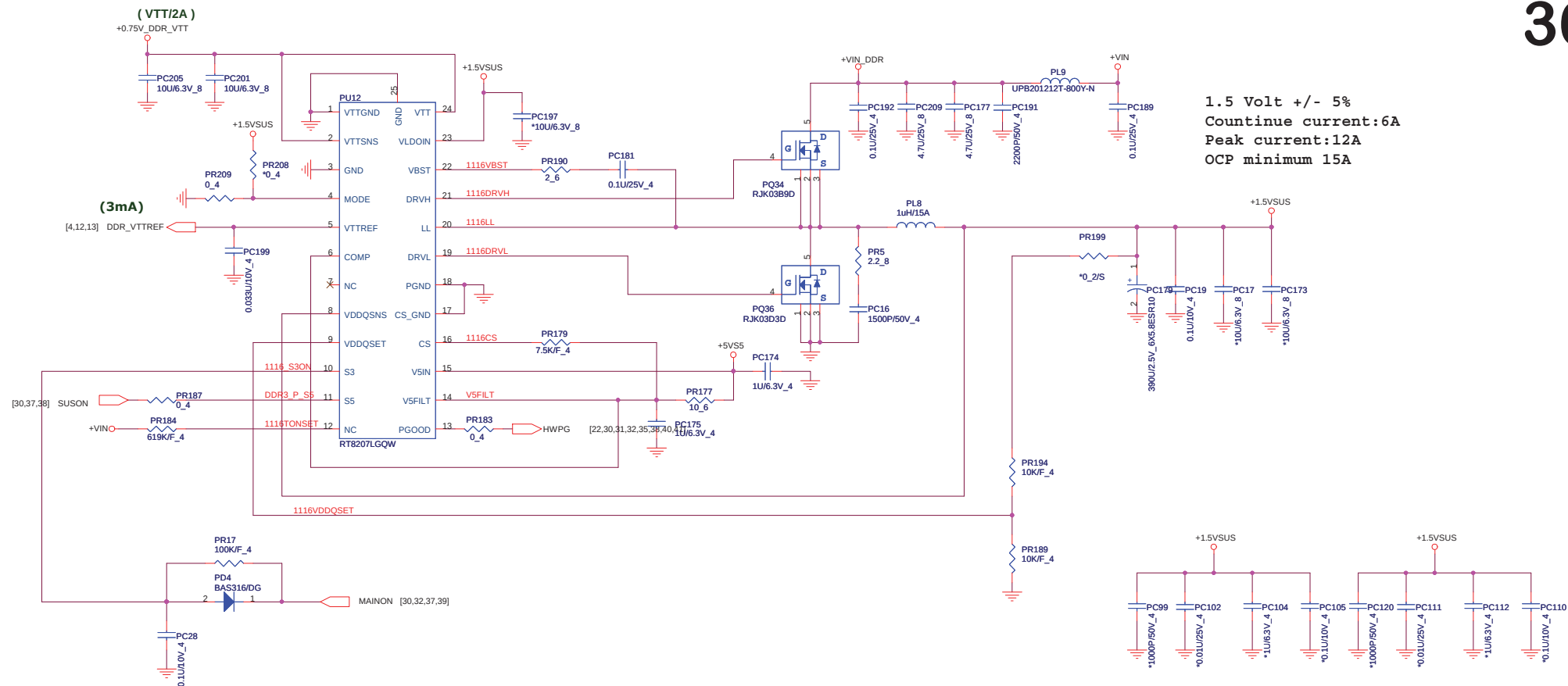


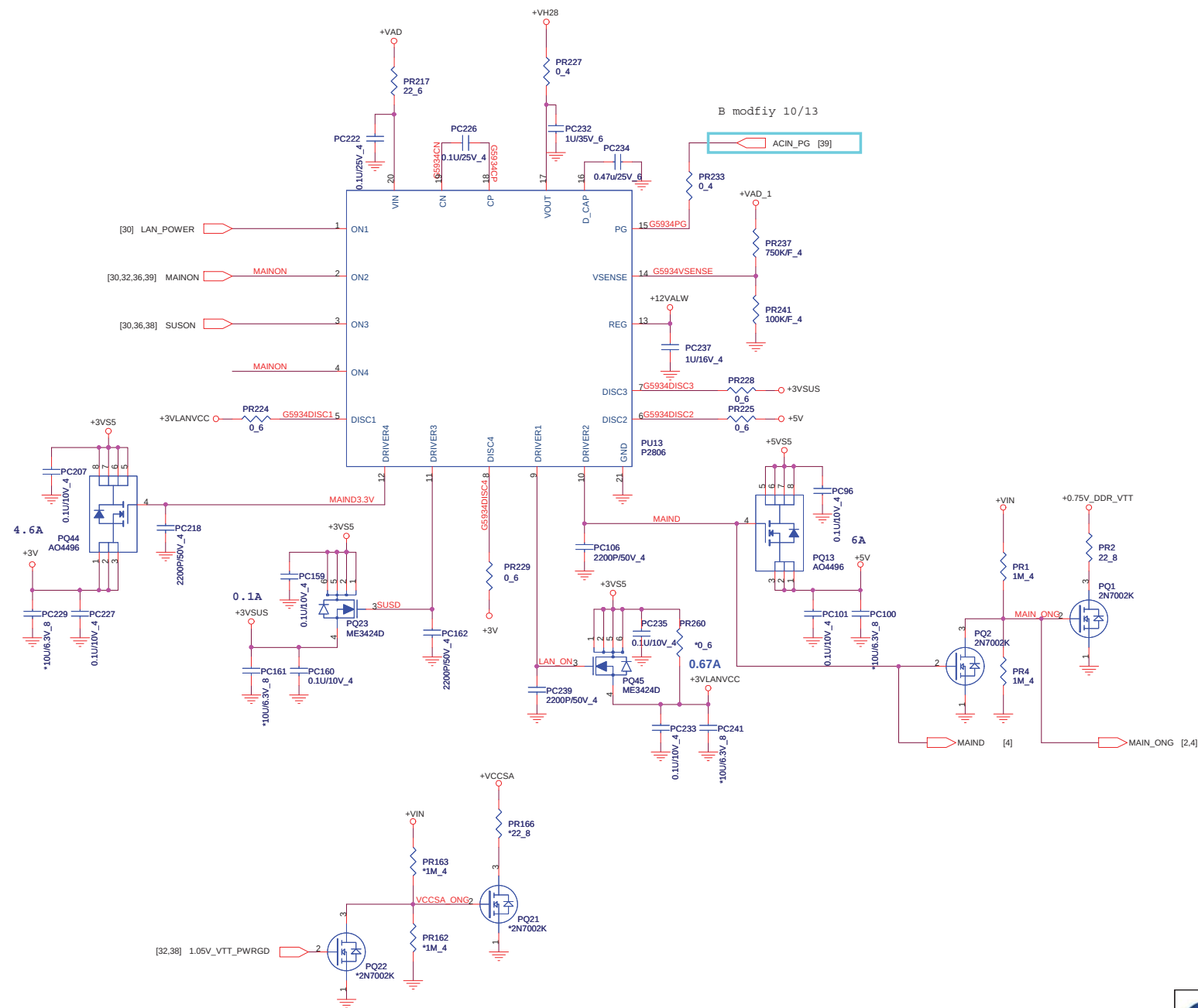
 PROJECT : SWH Quanta Computer Inc.		
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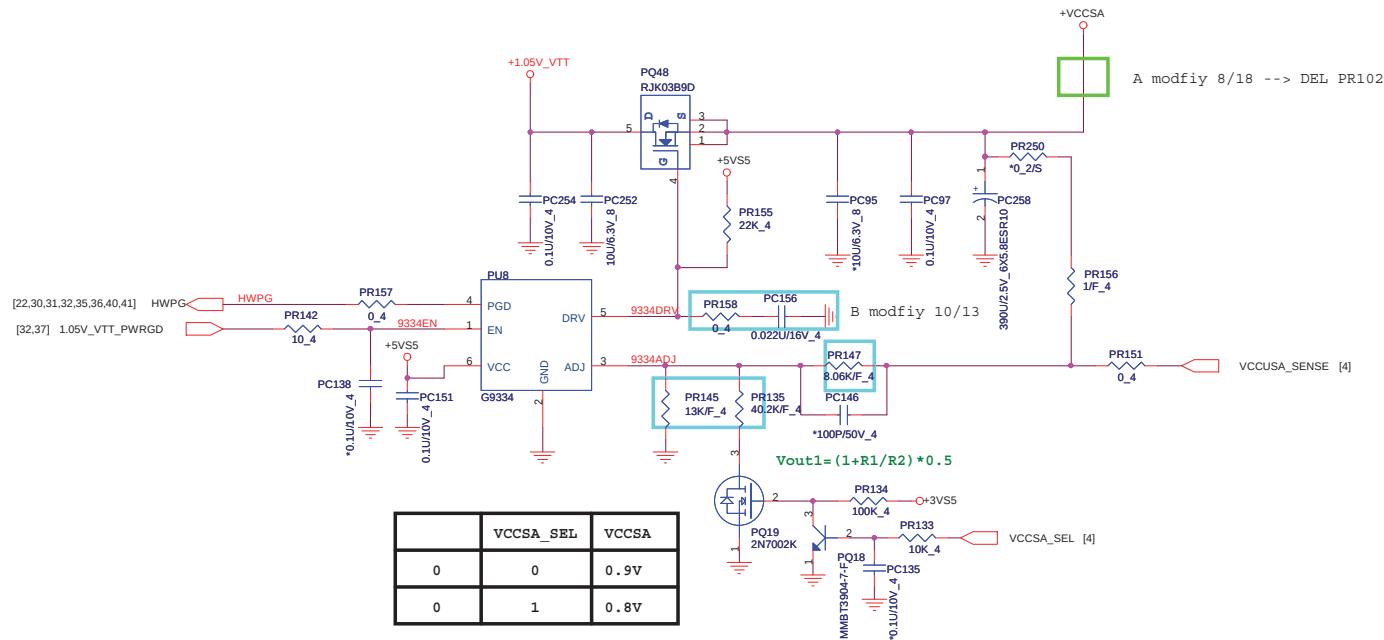
<http://hobi-elektronika.net>



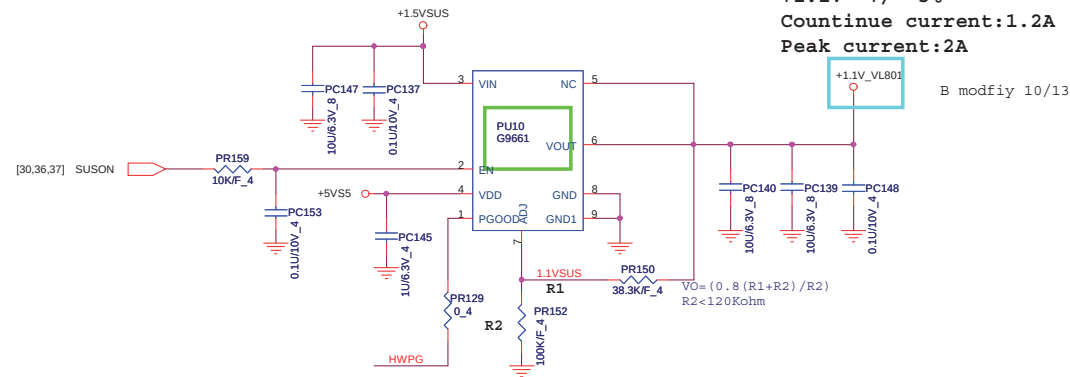




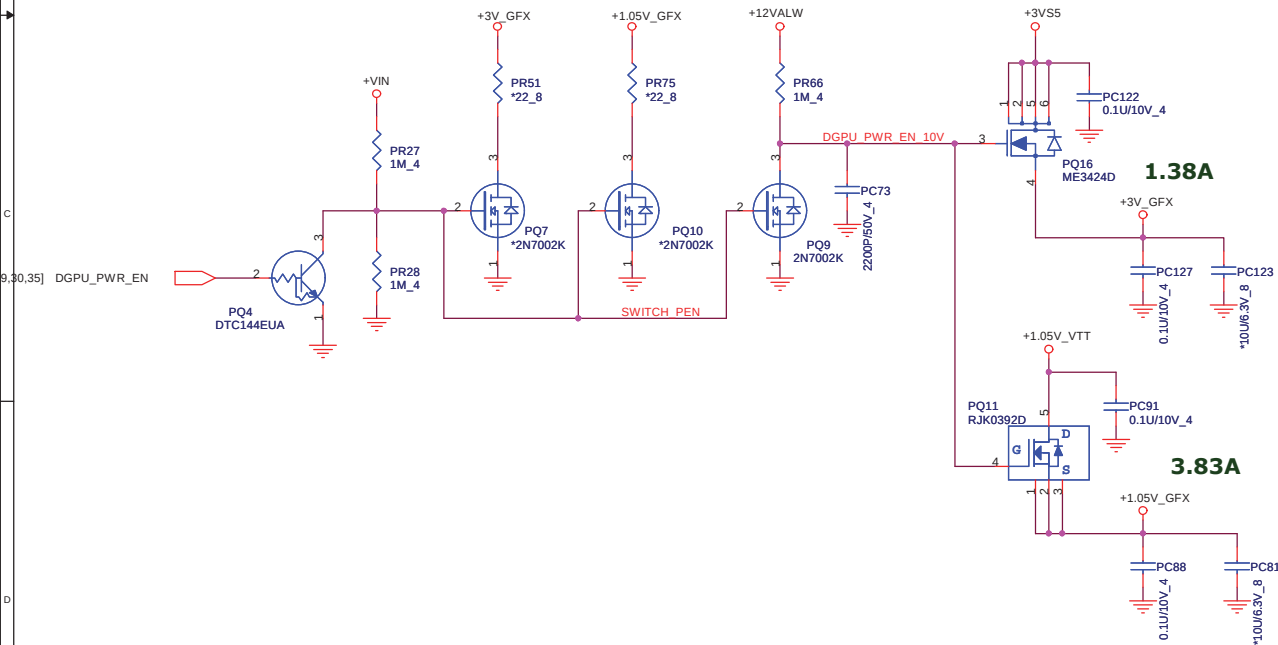
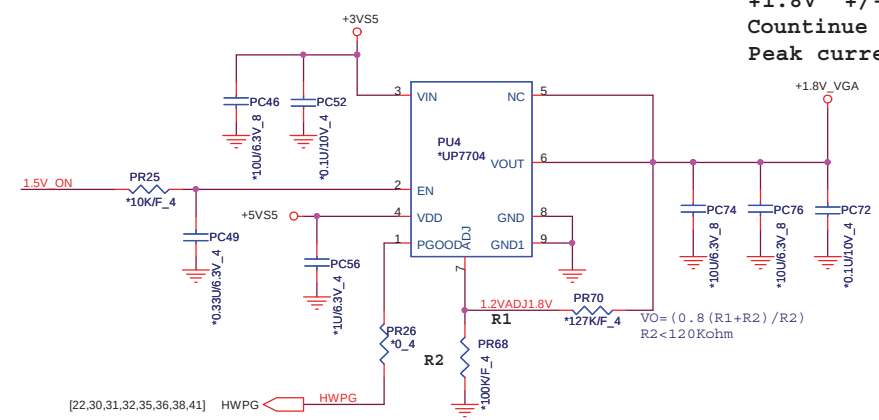
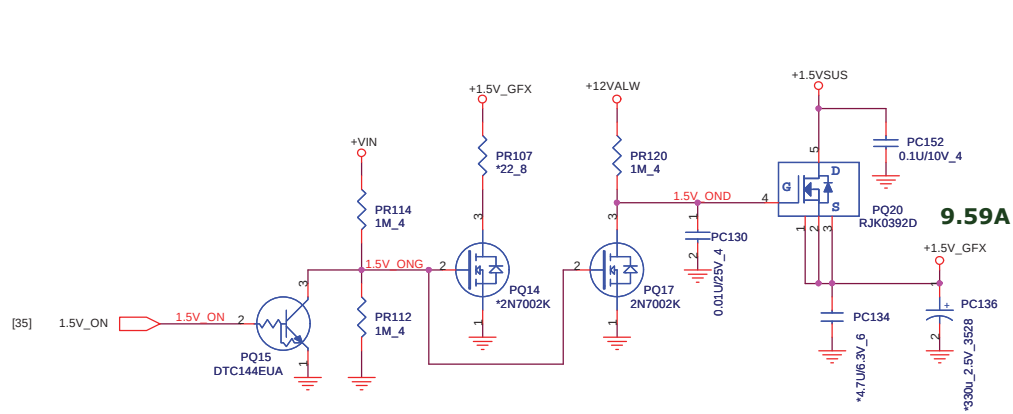
0.85V Volt +/- 5%
Countinue current 3A~6A



+1.1V +/- 5%
Countinue current:1.2A
Peak current:2A







Vender	Size	P/N
EON	128KB 512KB	AKE37ZN0Q01 (EN25F40-100HIP
Winbond	128KB 512KB	AKE35FN0N00 (W25X10BVSNIG) AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031

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