

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3(High)
LAYER 7 : SGND
LAYER 8 : BOT



4/7 DB del for PDC update.

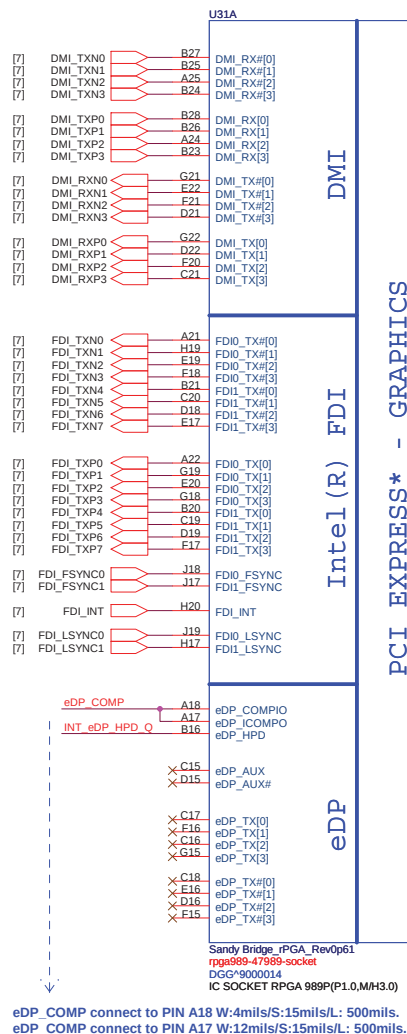


PROJECT : LX3/5(Huron River)

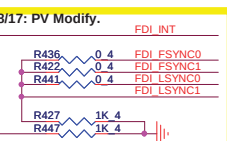
Quanta Computer Inc.

Size Custom	Document Number Clock Gen(9LRS3197)/HOLES	Rev 1A
Date: Friday, October 01, 2010		Sheet 2 of 47

Sandy Bridge Processor (DMI, PEG, FDI)

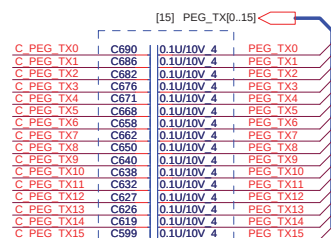


**FDI disable
(DIS only stuff)**



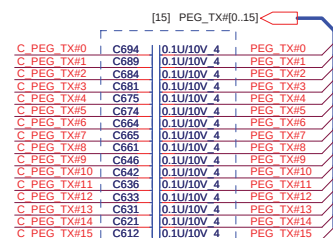
FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)



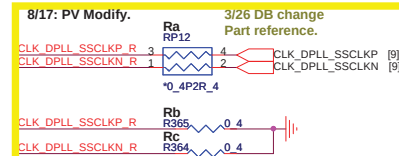
0.22uF AC coupling Caps for PCIE GEN1/2/3

remove)



0.22uF AC coupling Caps for PCIE GEN1/2/3

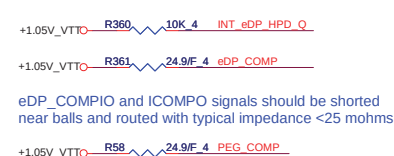
Embedded Display PLL Clock



	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

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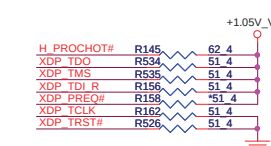
DP & PEG Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

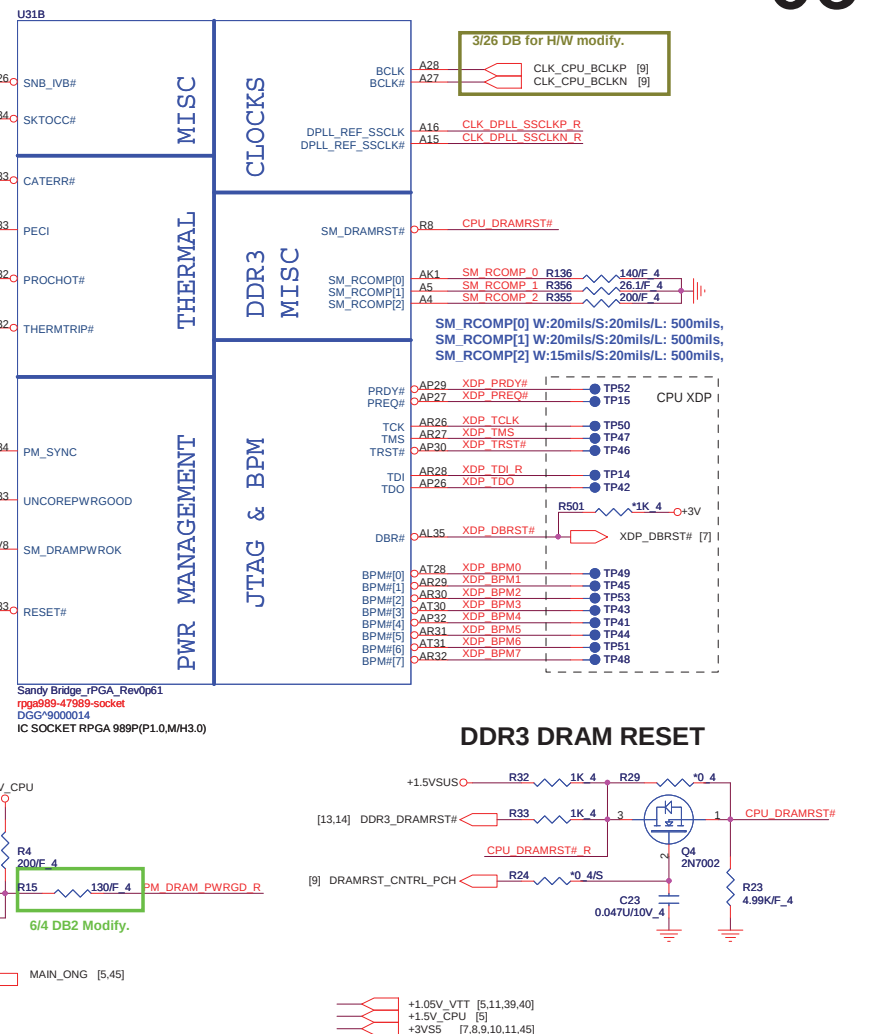
Processor pull-up (CPU)



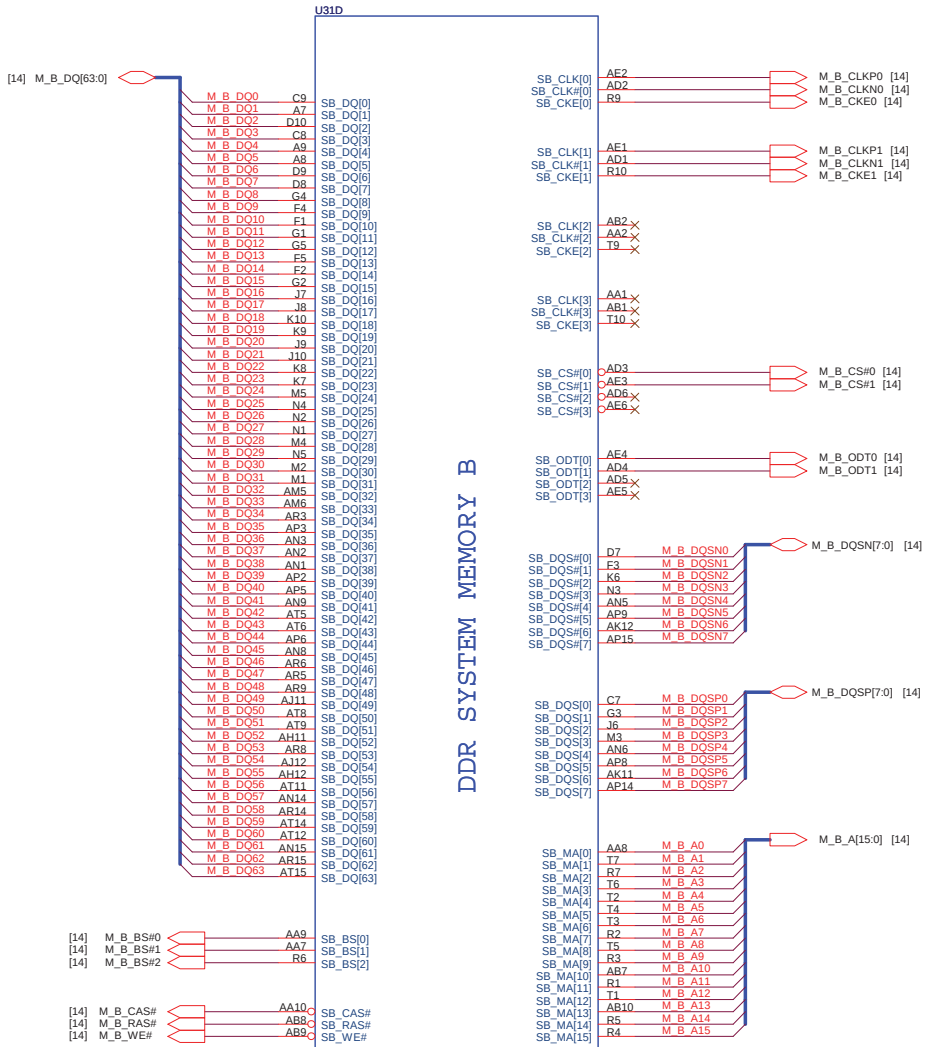
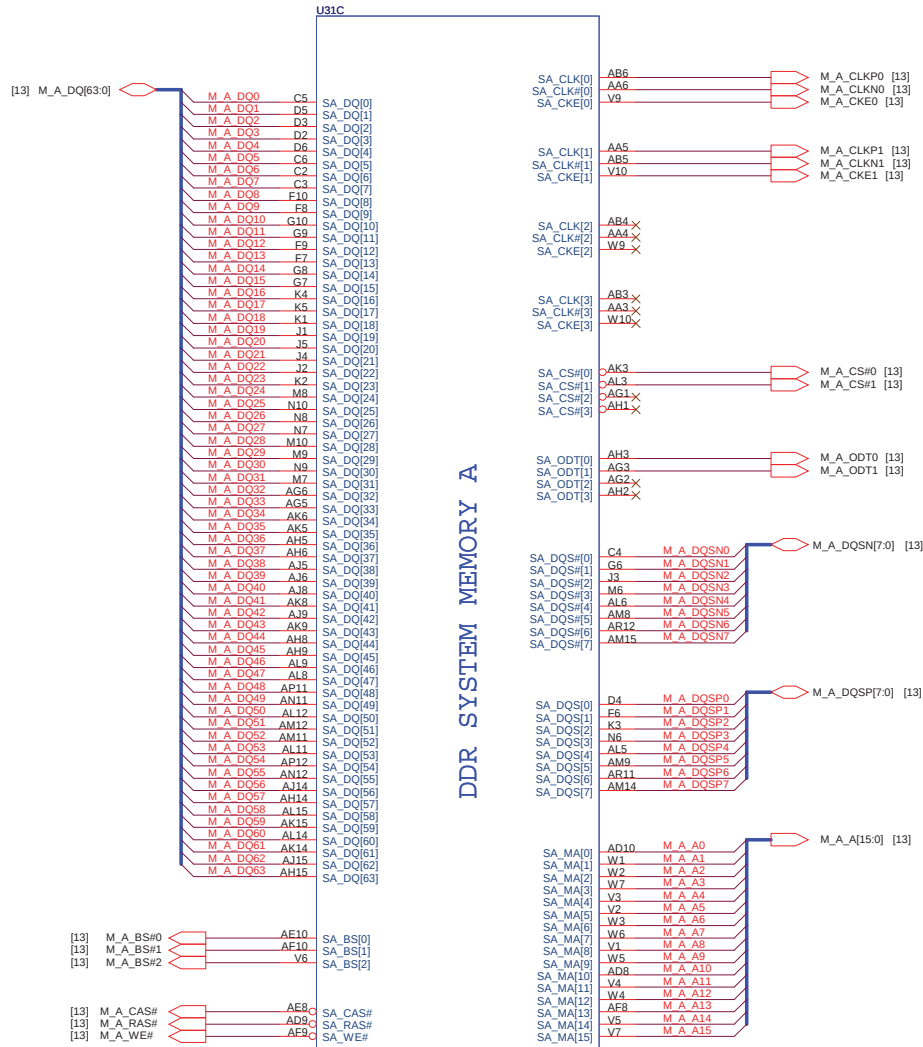
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size Custom	Document Number SNB 1/4 (PCIE&DMI&FDI)	Rev 1A
Date: Wednesday, October 13, 2010	Sheet 3 of 47	

Sandy Bridge Processor (CLK,MISC,JTAG)

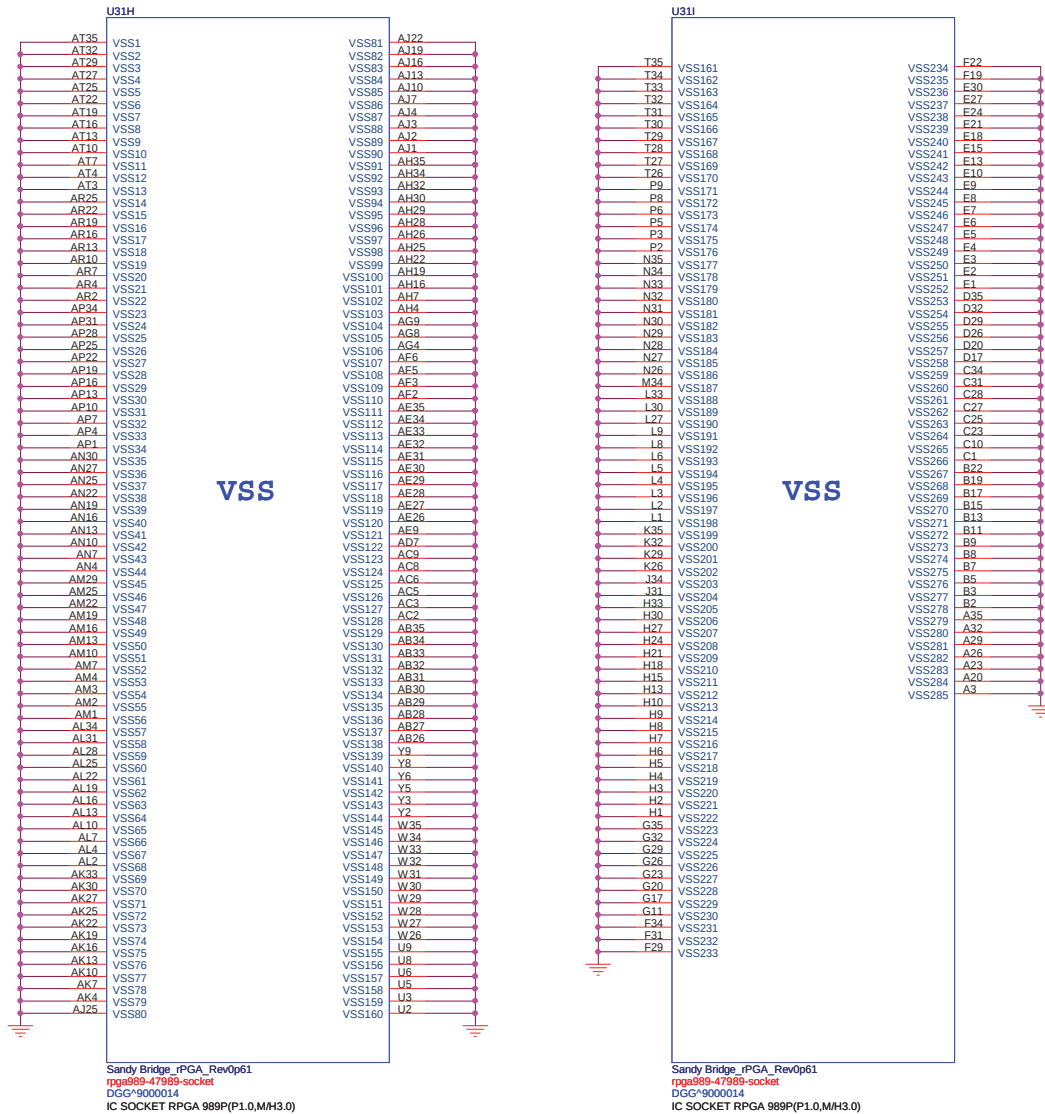


Sandy Bridge Processor (DDR3)

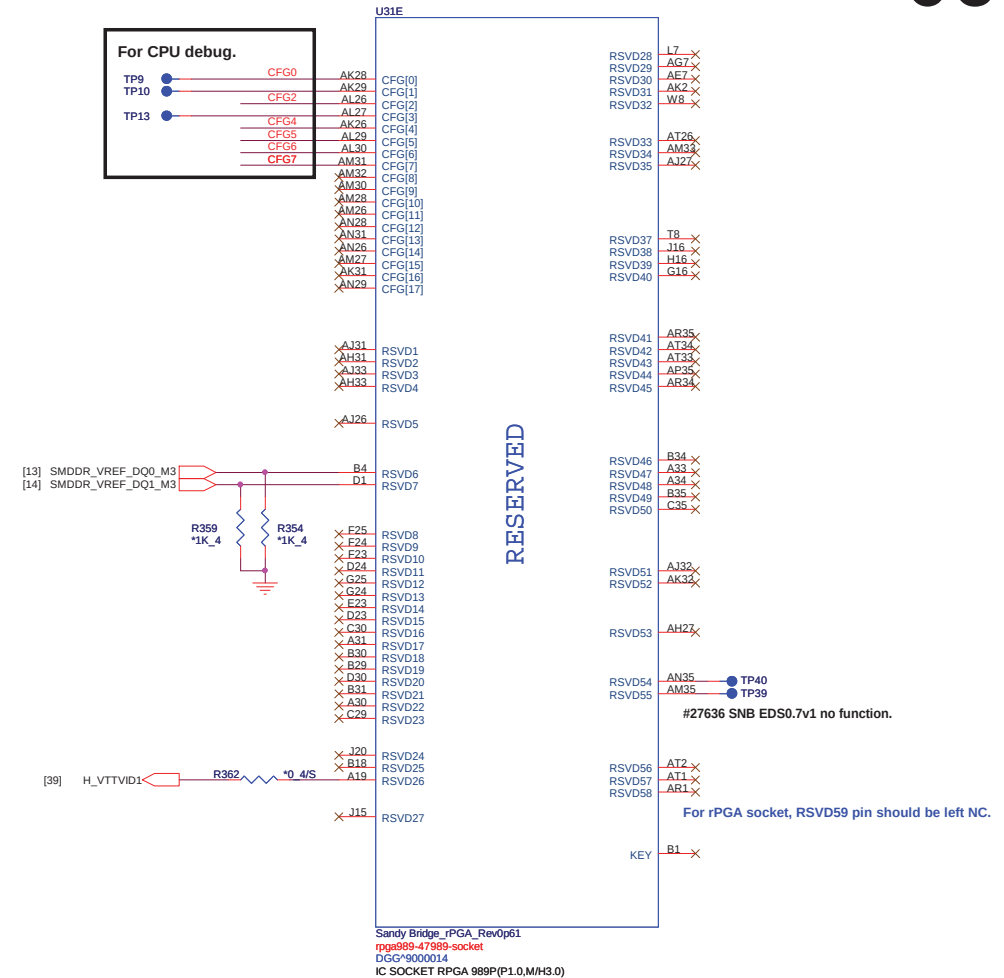




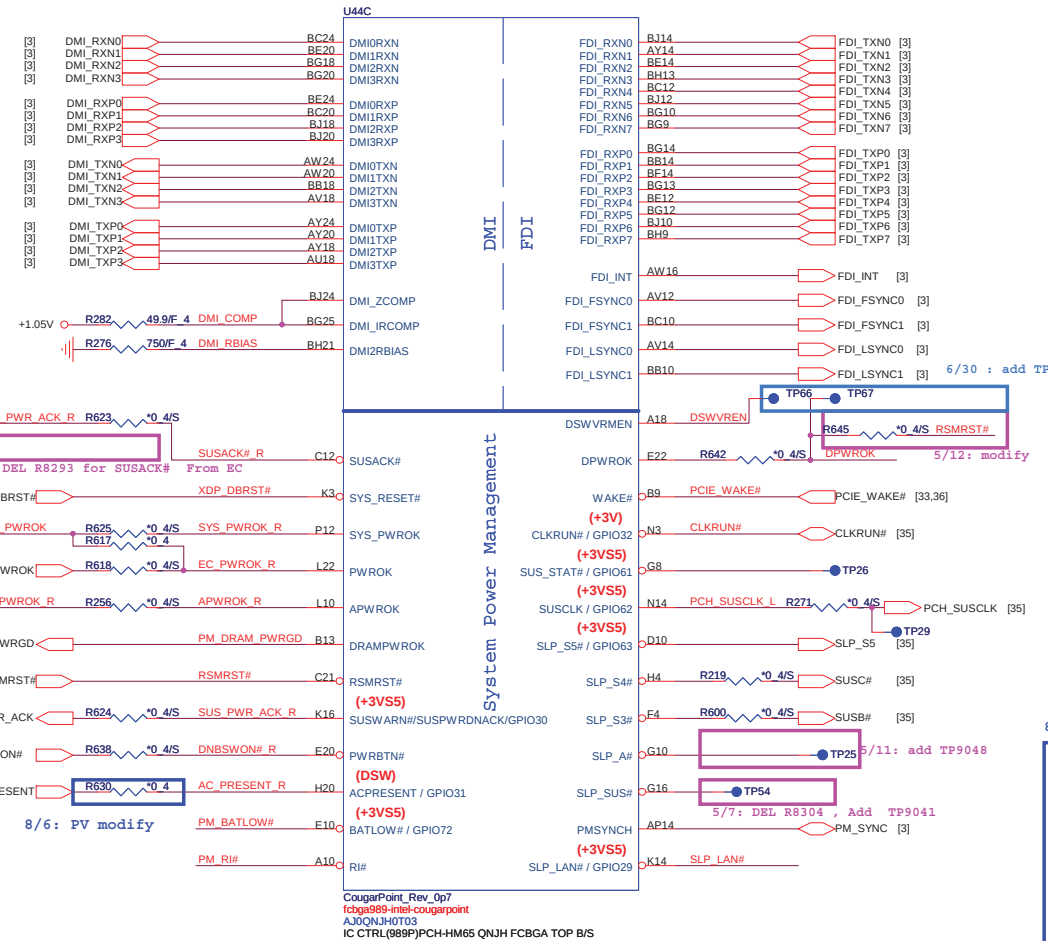
Sandy Bridge Processor (GND)



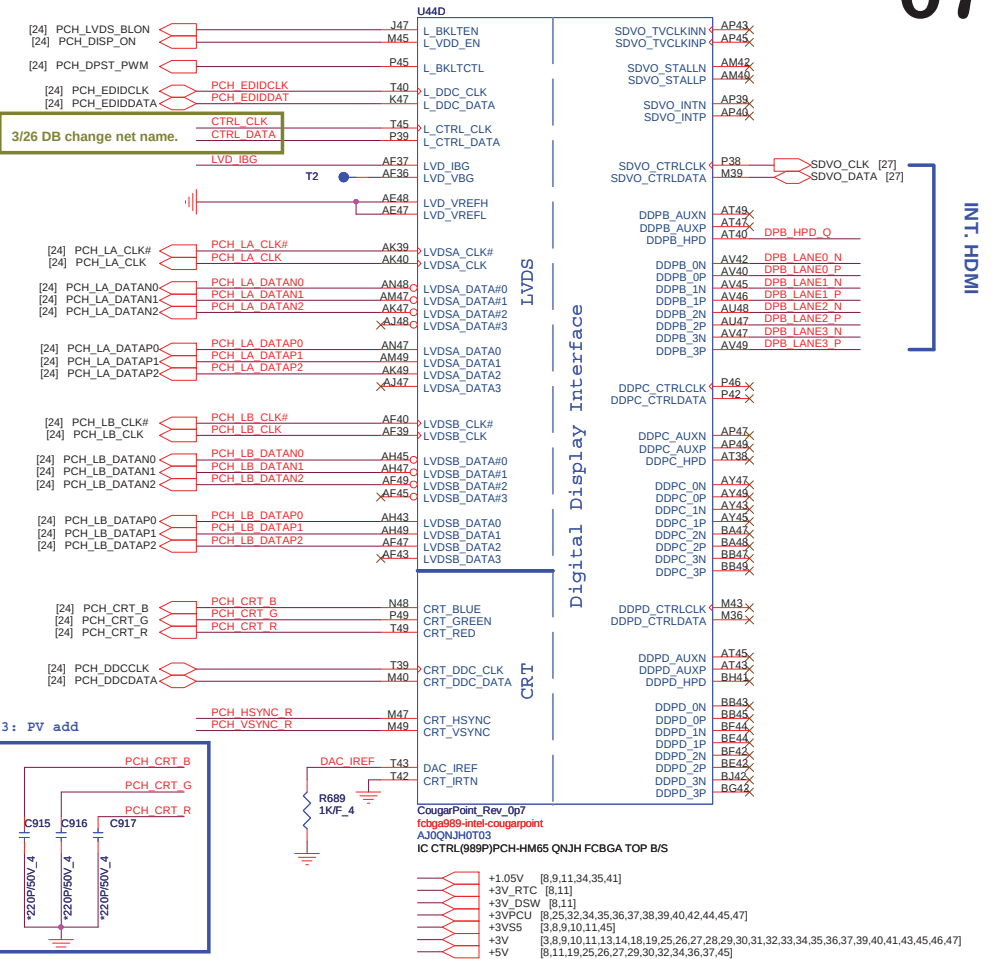
Sandy Bridge Processor (RESERVED, CFG)



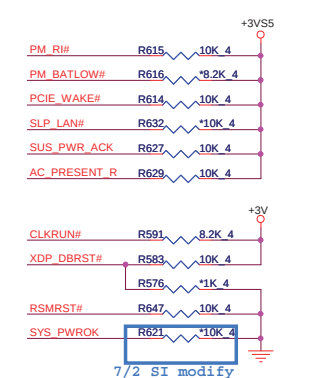
Cougar Point (DMI, FDI, PM)



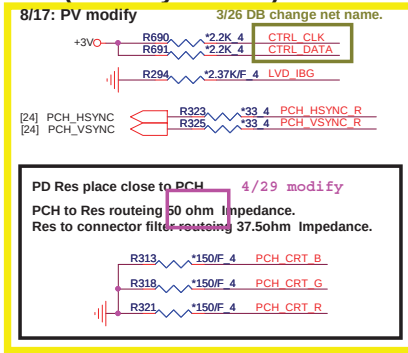
Cougar Point (LVDS, DDI)



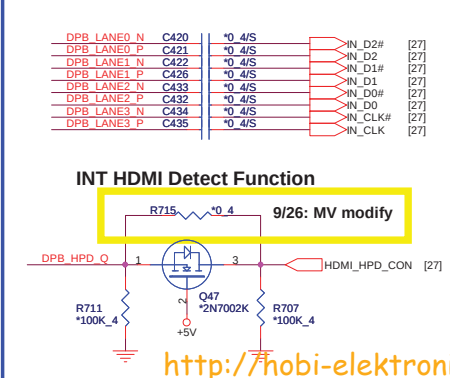
PCH Pull-high/low(CLG)



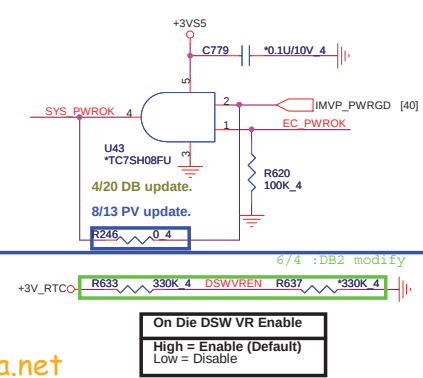
**INT LVDS & CRT disable
(DIS only remove)**



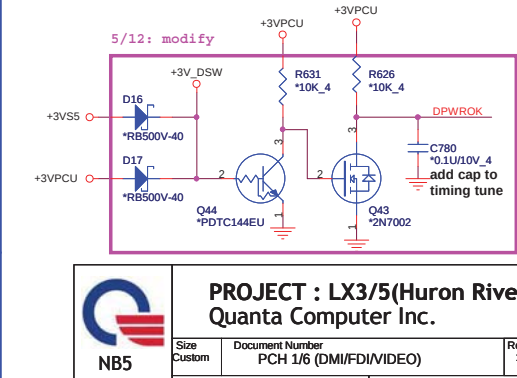
INT HDMI disable (DIS only remove)

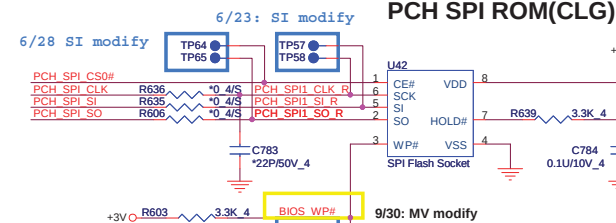
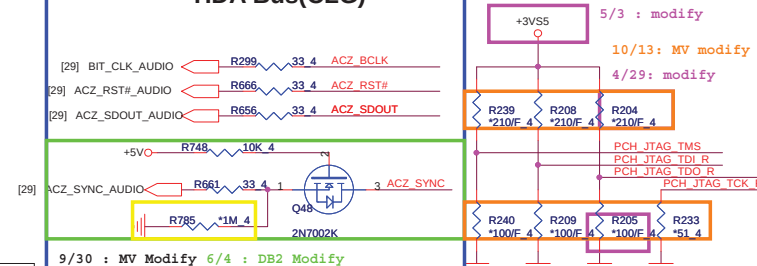
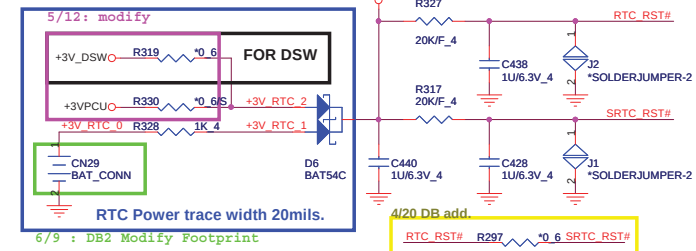
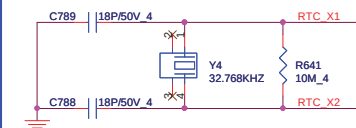


System PWR_OK(CLG)



DPWROK FOR DSW





NB5

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A
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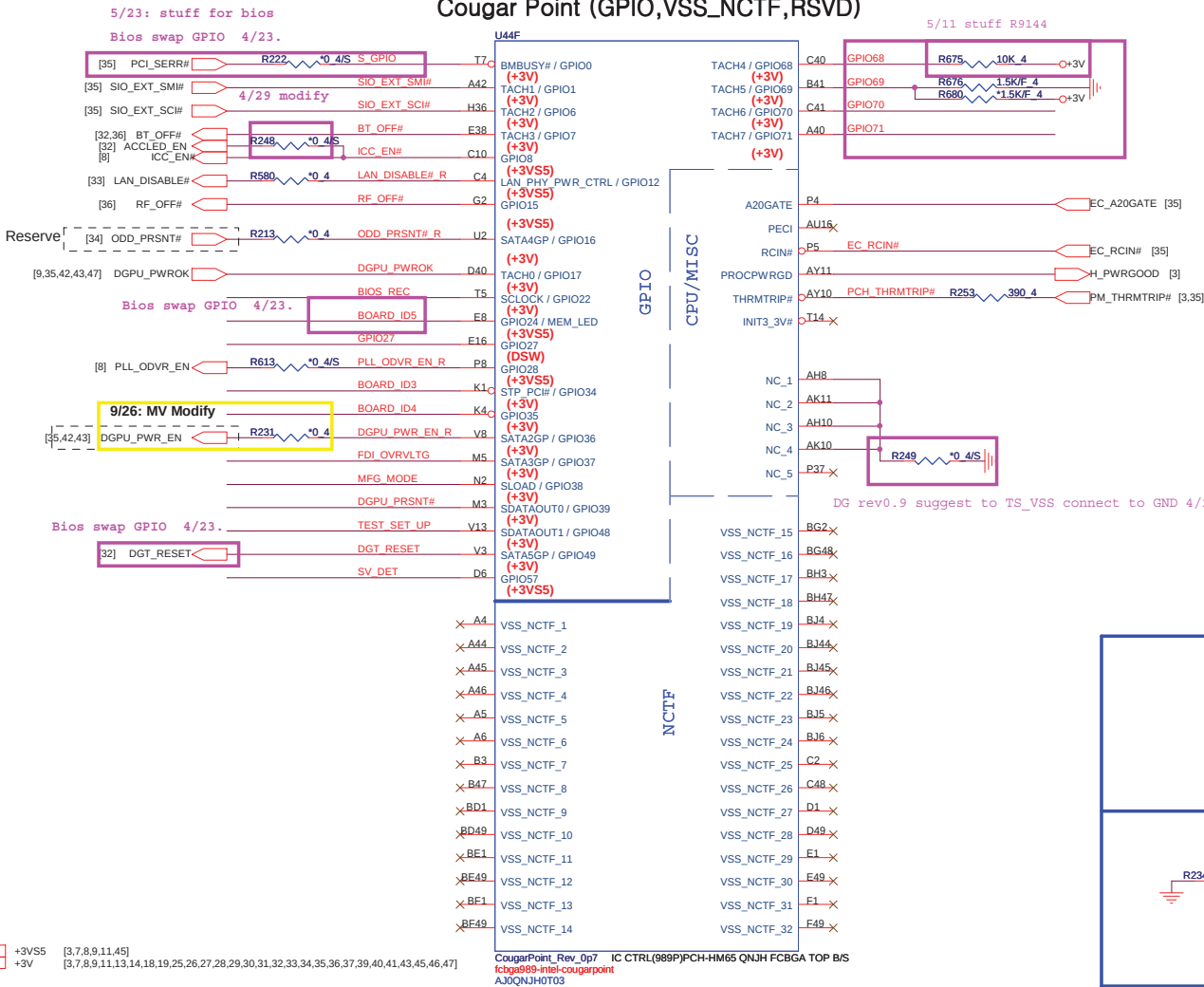
Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	9/30: MV modify									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	0	LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	0	LPC											
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/29 modify										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

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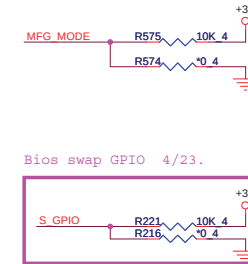
Cougar Point (GPIO,VSS_NCTF,RSVD)

Clock Gen Power OK (CLG)

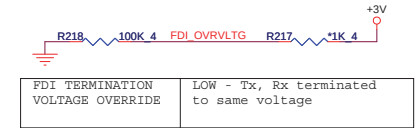
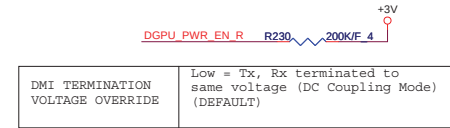
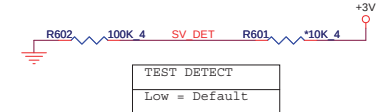
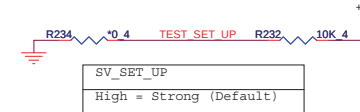
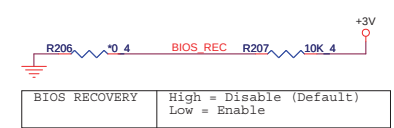
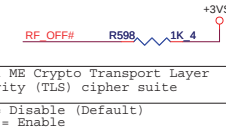
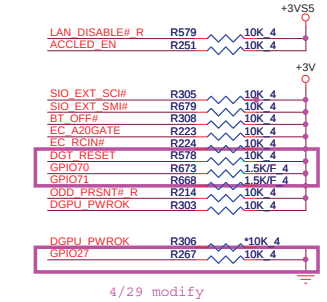
3/26 DB del external clock generator.



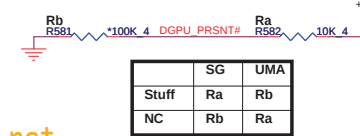
MFG-TEST



GPIO Pull-up/Pull-down(CLG)

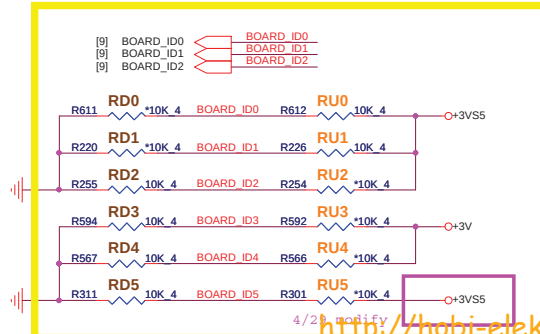


GFX Present

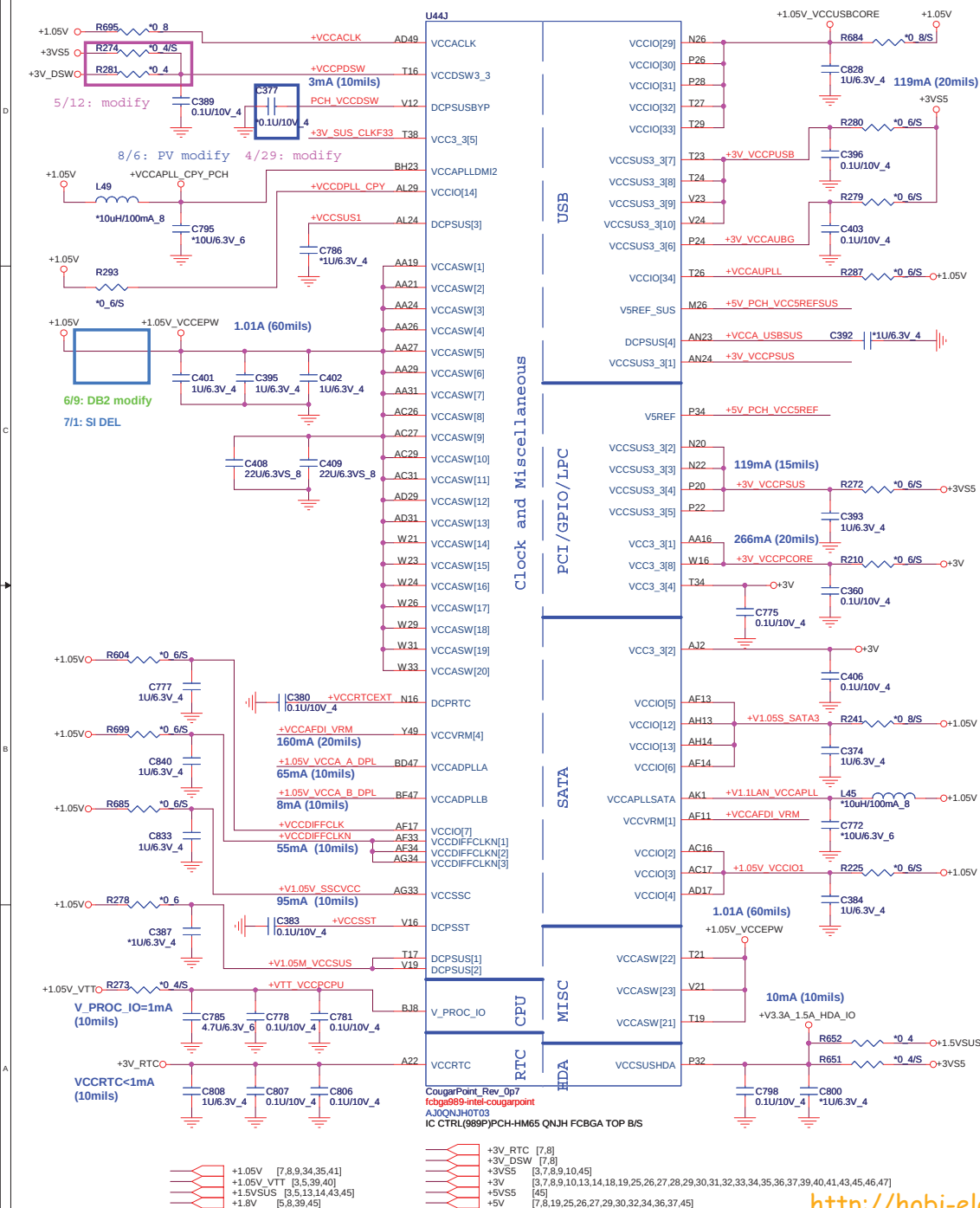


BOARD ID SETTING

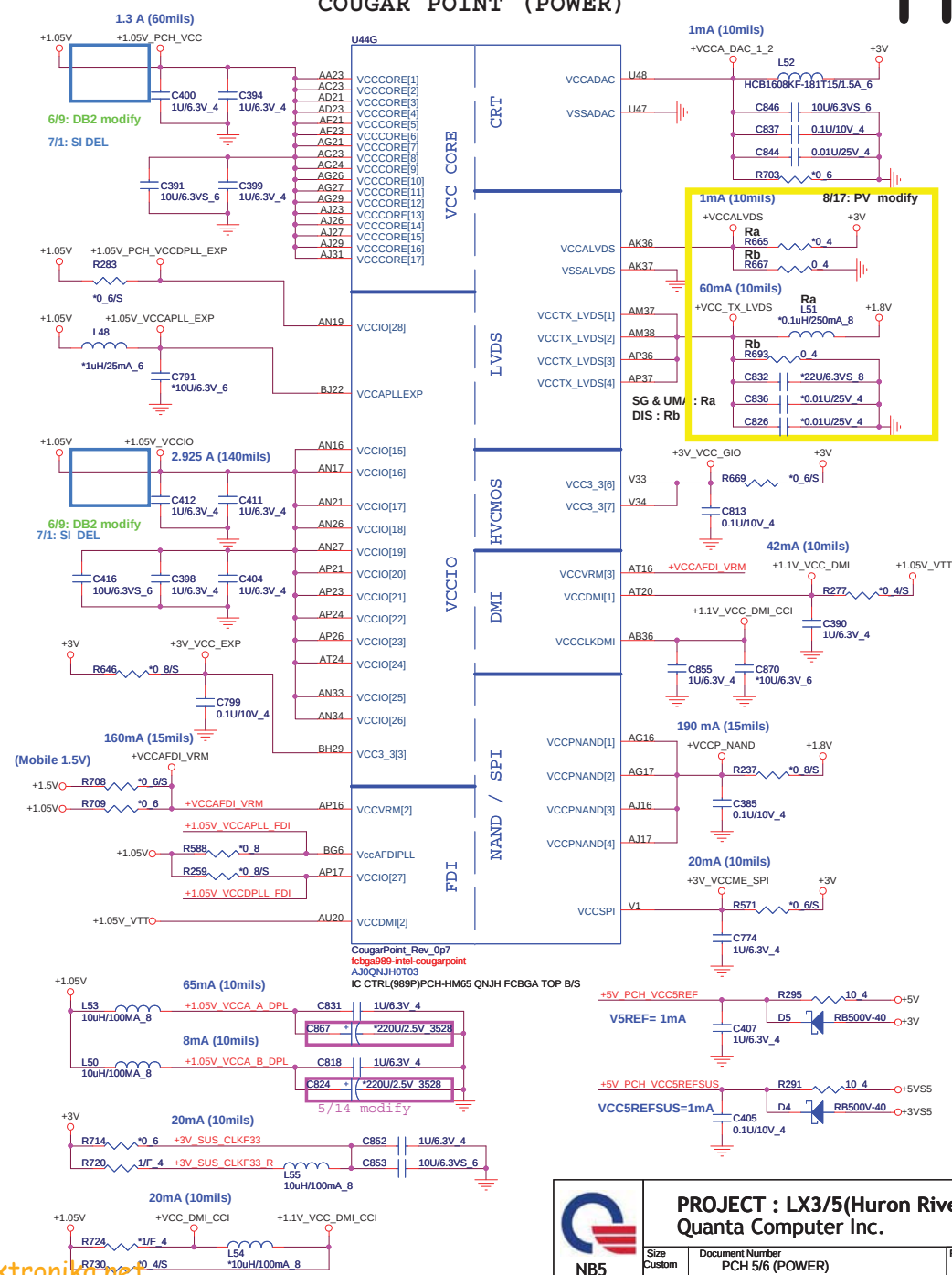
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
LX3 UMA	0	0	0	0	0	0
LX5 UMA	0	0	0	0	0	1
L	0	0	0	0	1	0
X	0	0	0	0	1	1
LX3 Capilano	0	0	0	1	0	0
LX5 Capilano	0	0	0	1	0	1
LX5 Capilano XT	0	0	0	1	1	0
LX5 DISCRETE	0	0	0	1	1	1



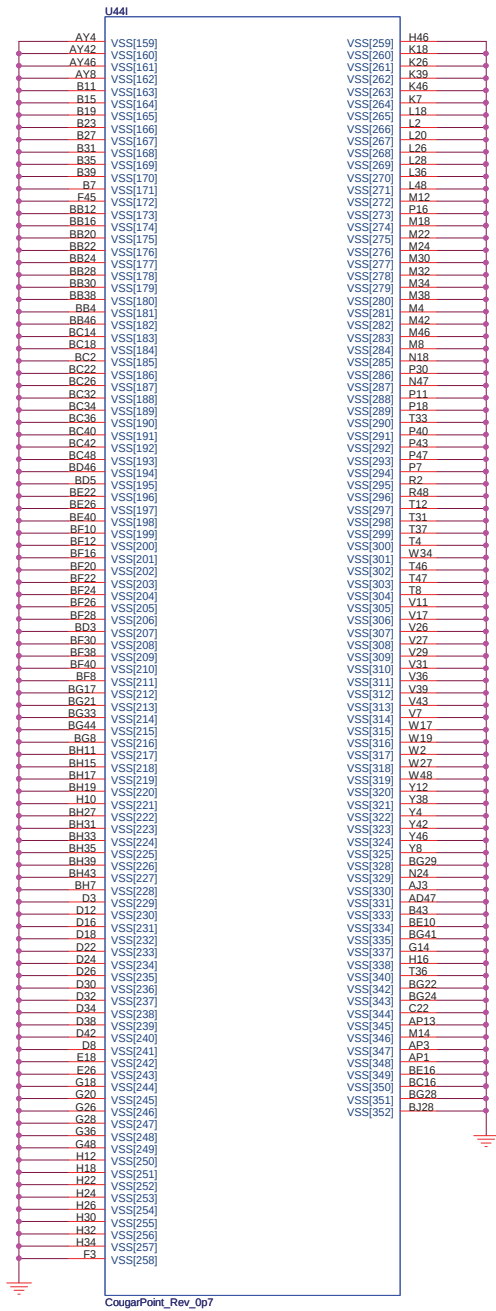
Cougar Point-M (POWER)



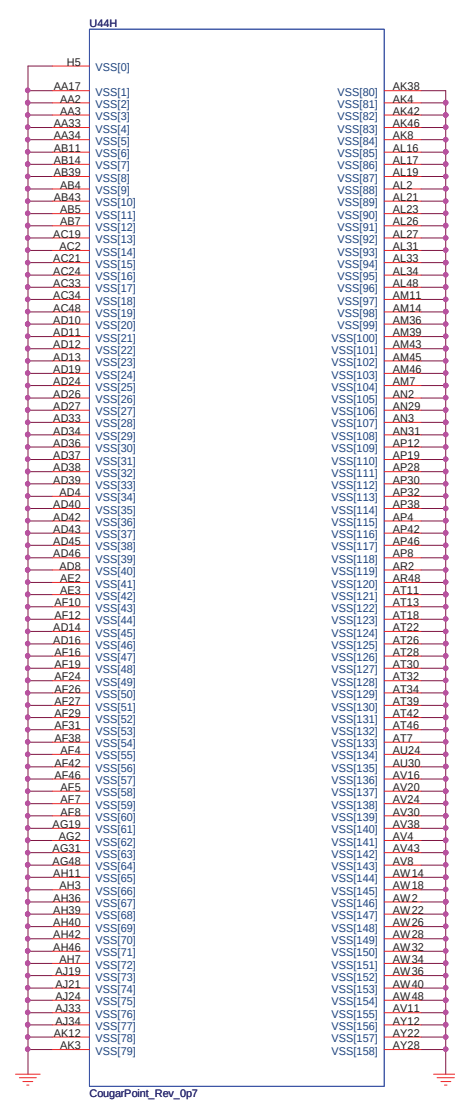
COUGAR POINT (POWER)



IBEX PEAK-M (GND)



IBEX PEAK-M (GND)

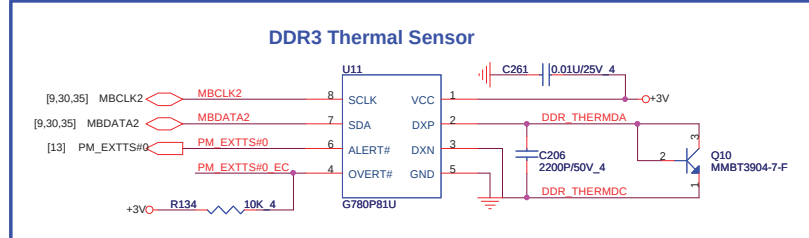
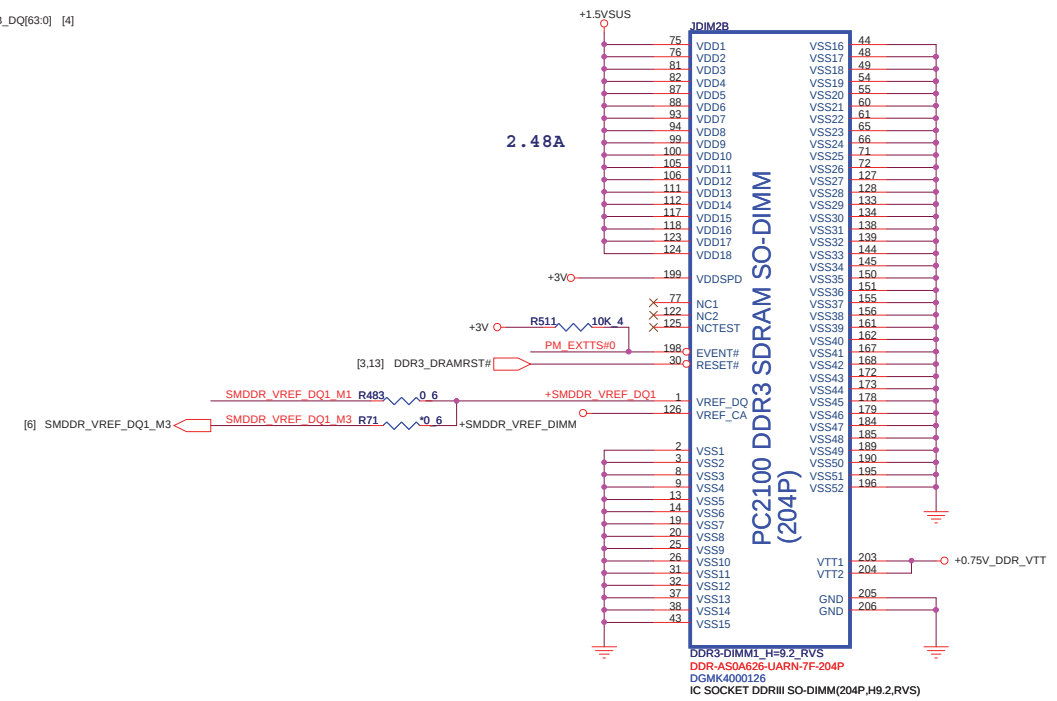
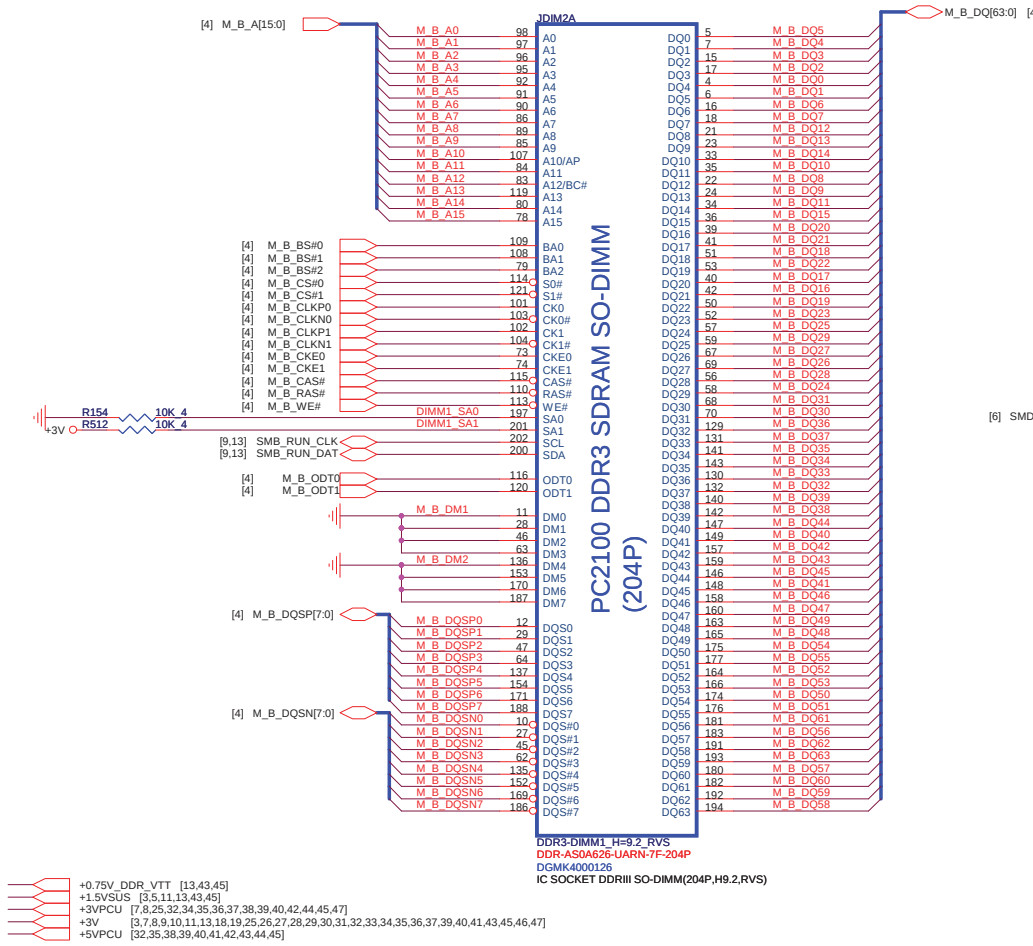




1

[illegible][illegible]

100



VREF DQ1 M2 Solution

Place these Caps near So-Dimm1.

VREF DQ1 M1 Solution

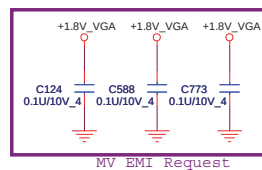
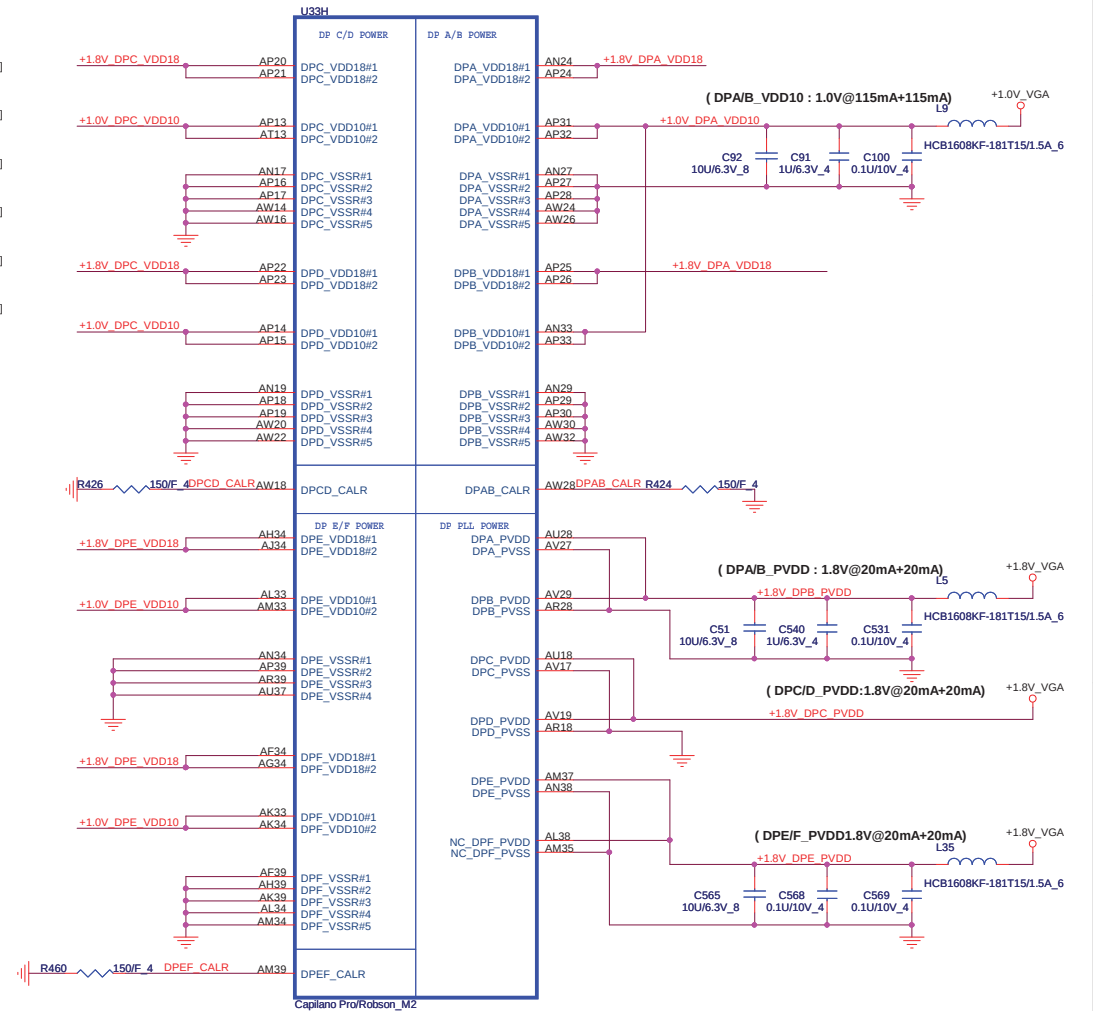
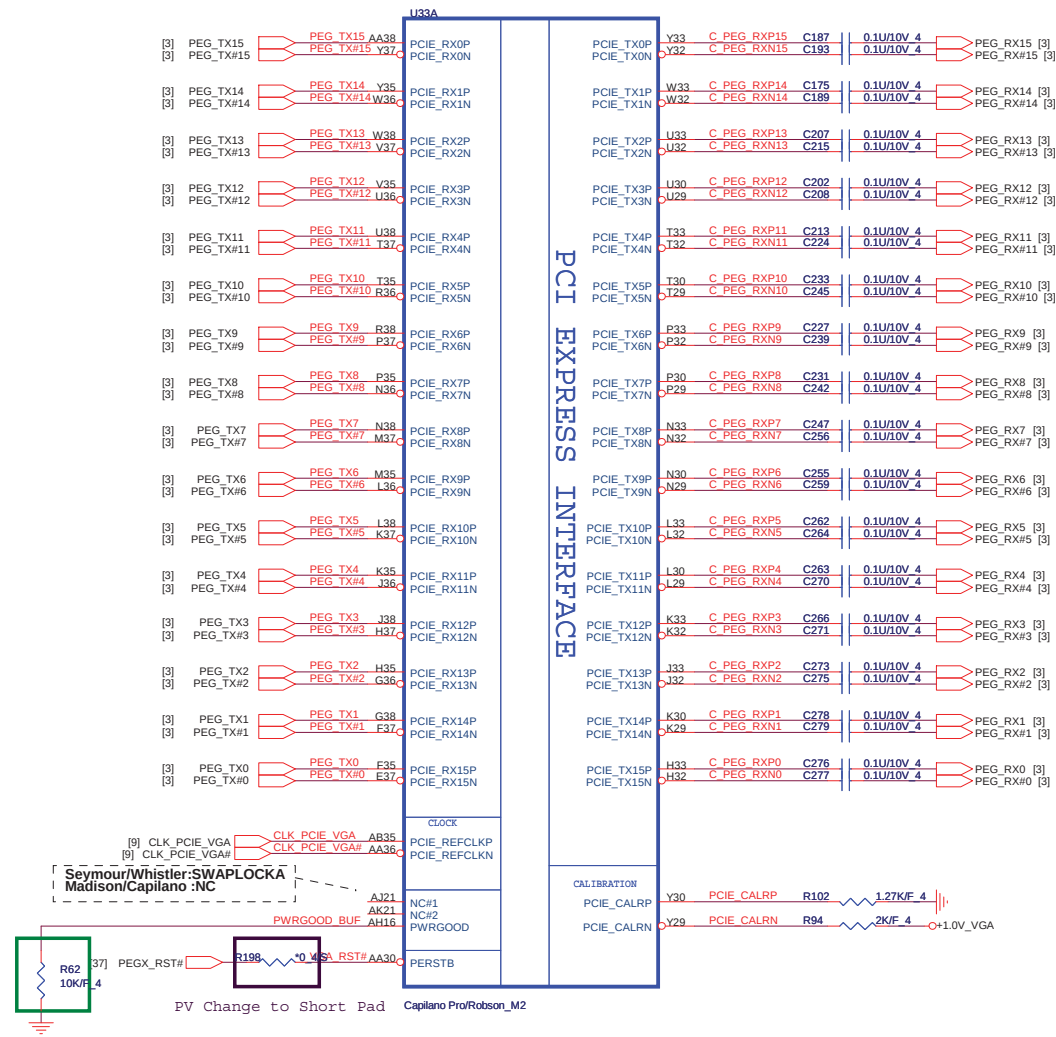
6/23 : Del M2 solution

4/29 reserve M2 solution

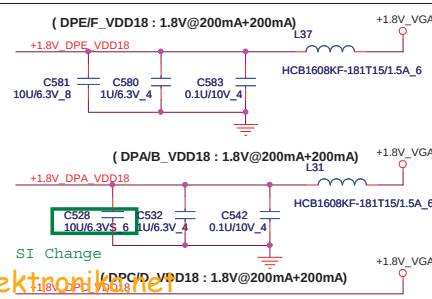
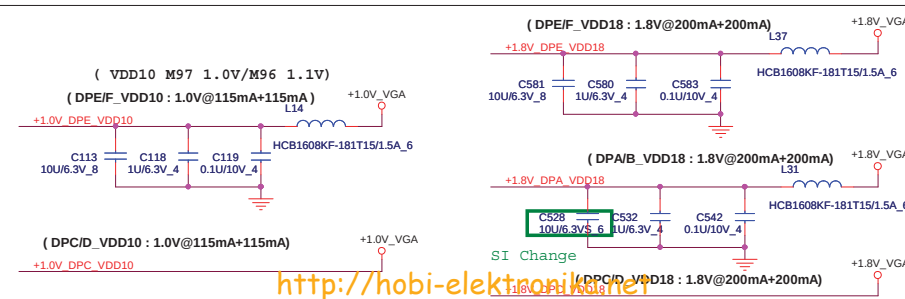
<http://hobi-elektronika.net>

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

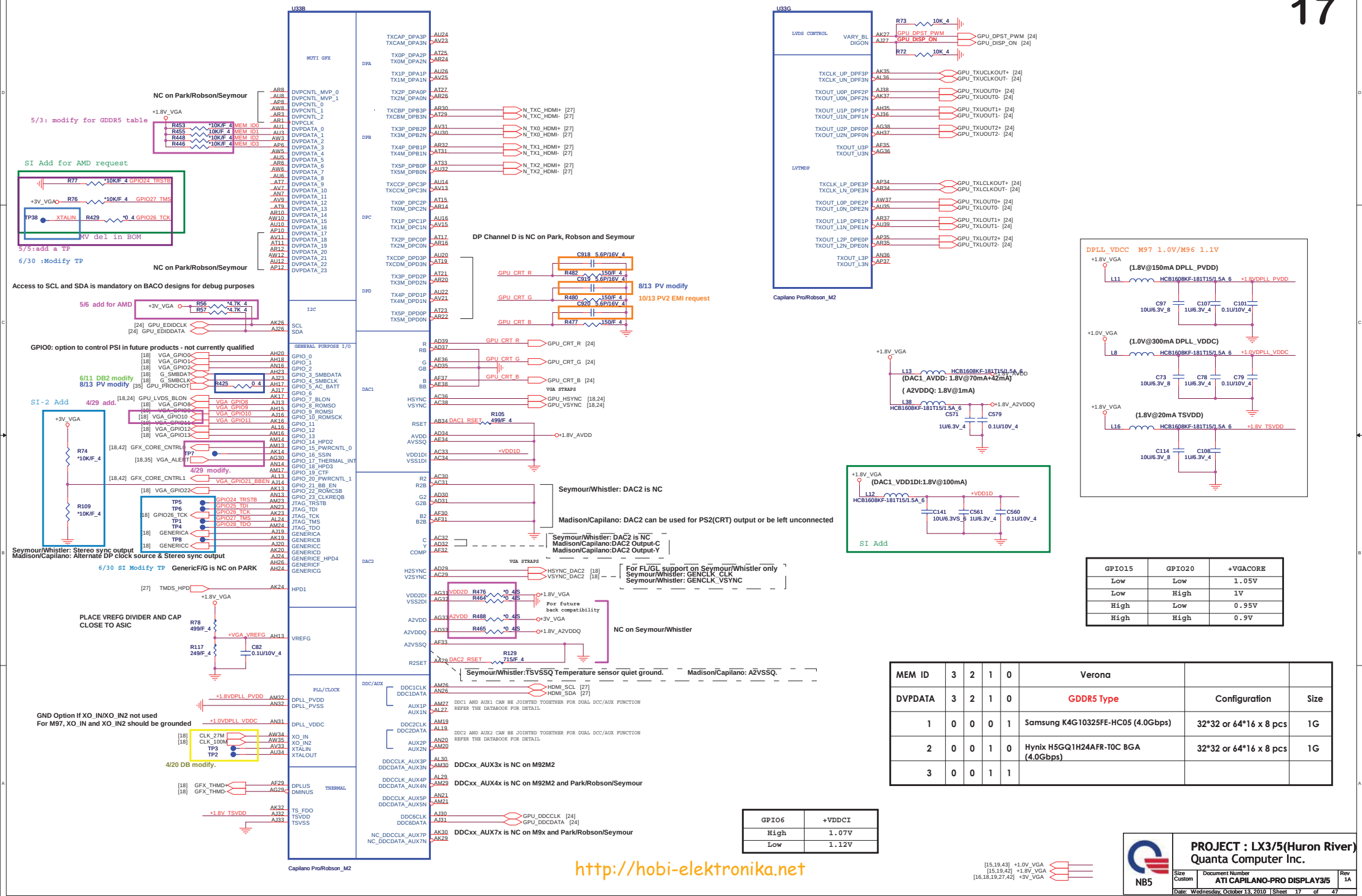
Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A
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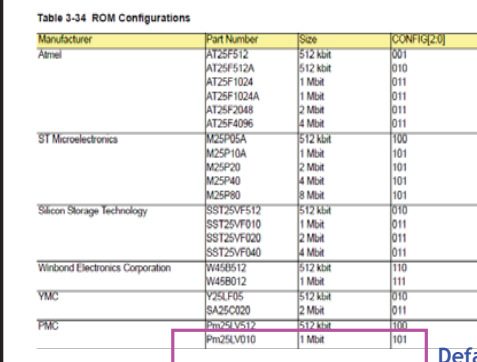


SI Del R43,R38,C57

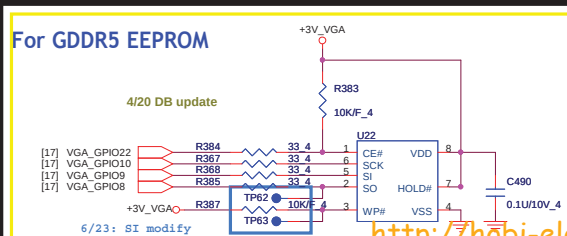
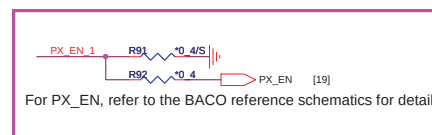




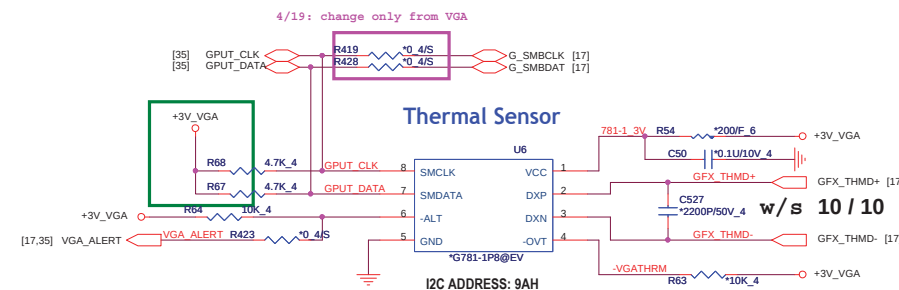
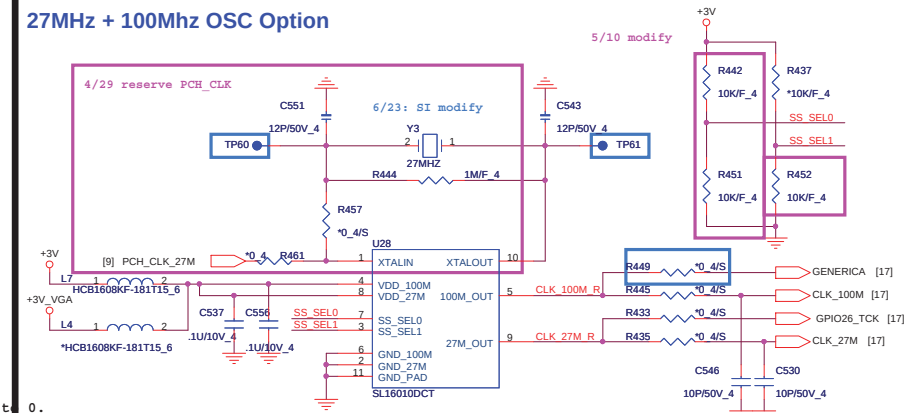




Reserve for support BACO mode



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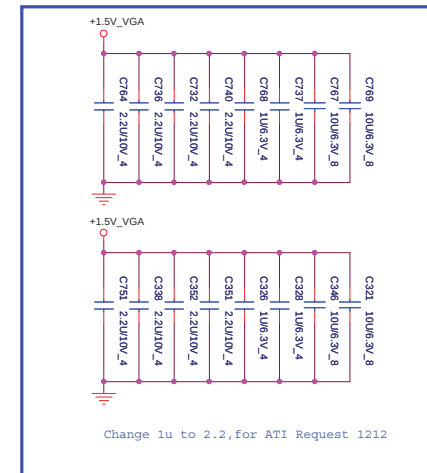
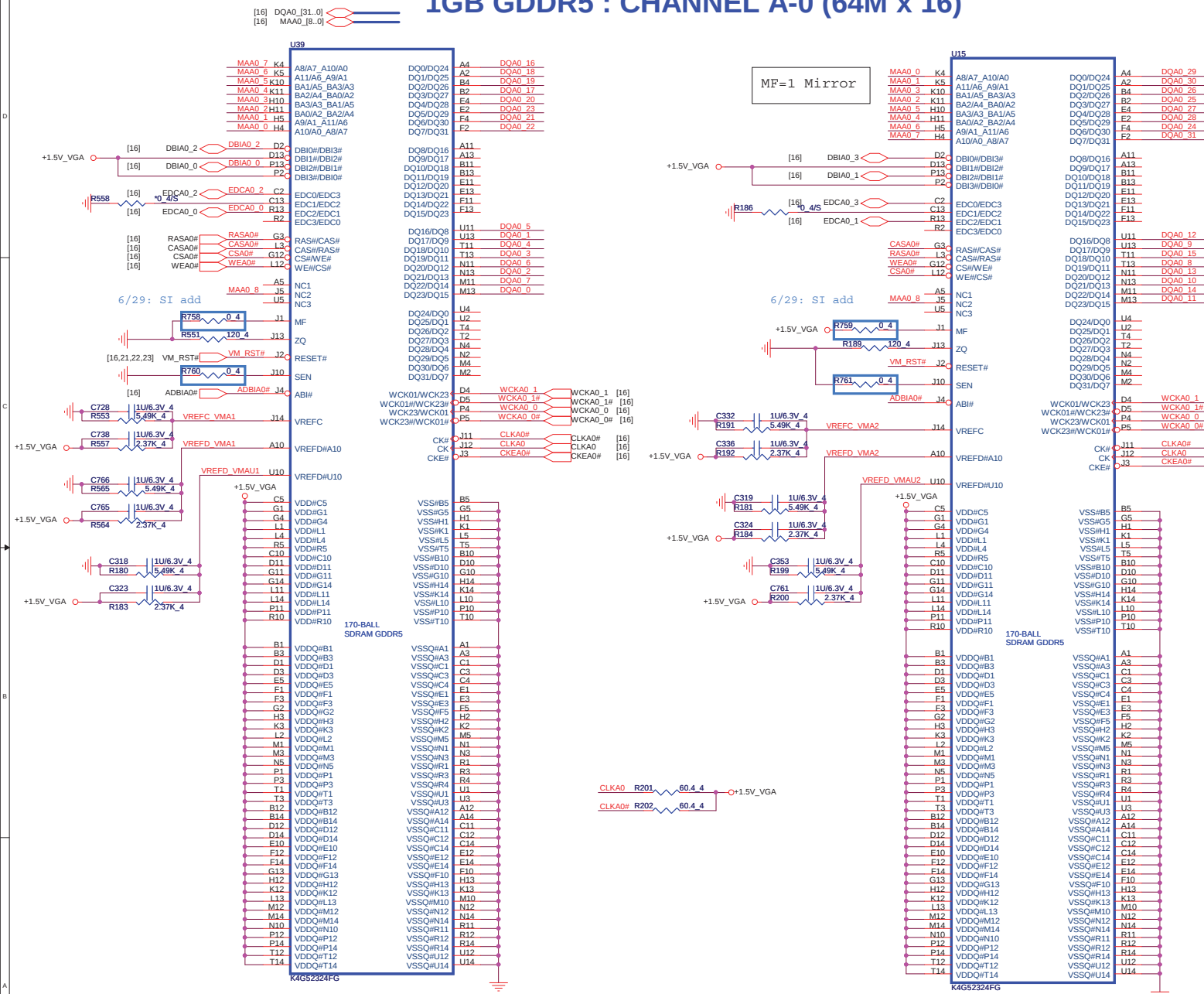
 NB5	PROJECT : LX3/5(Huron River) Quanta Computer Inc.		
	Size Custom	Document Number ATI CAPILANO-PRO(GD&Str)4/5	Rev 1A
Date: Wednesday, October 13, 2010 Sheet 18 of 47			



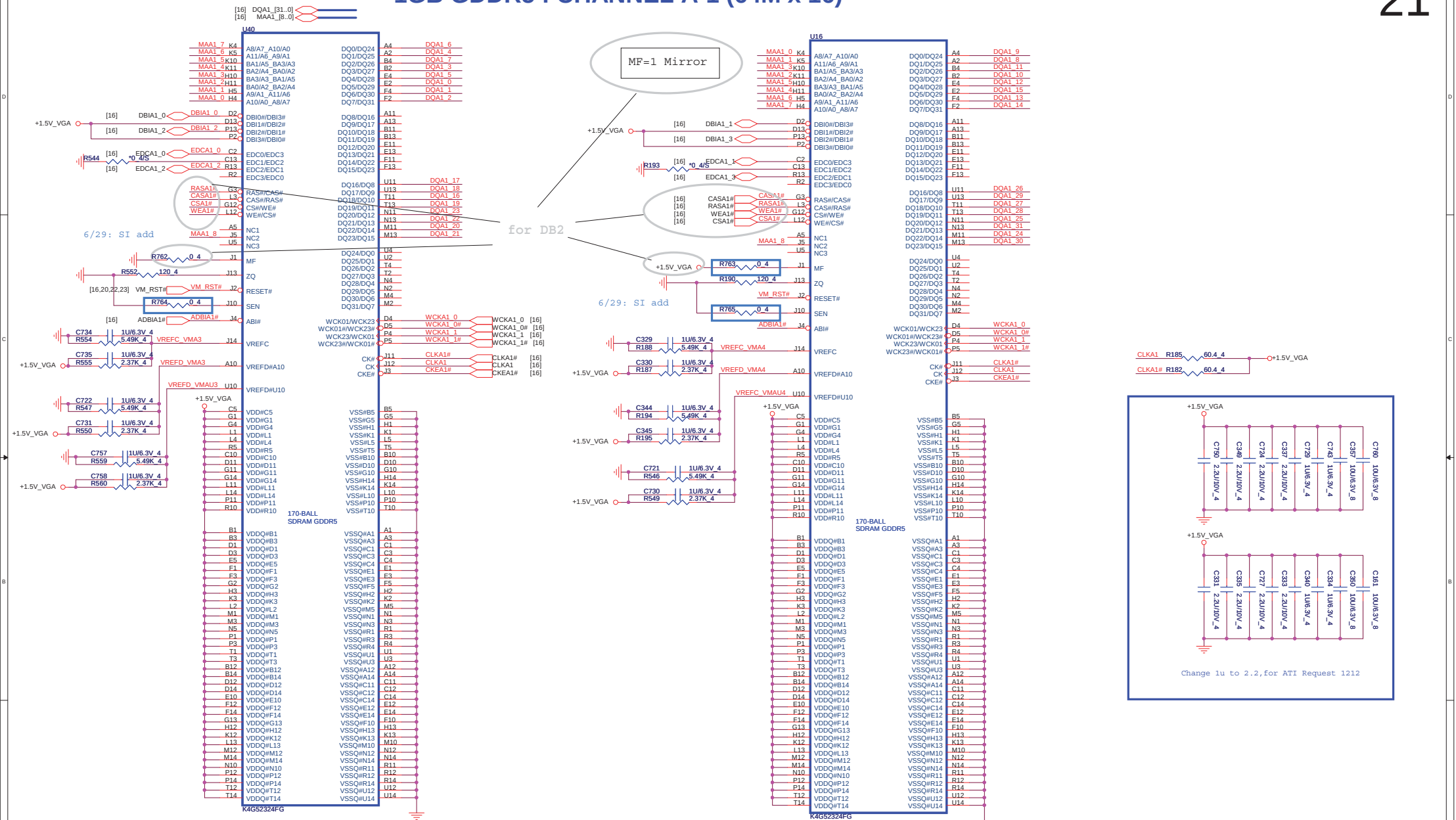
NB5

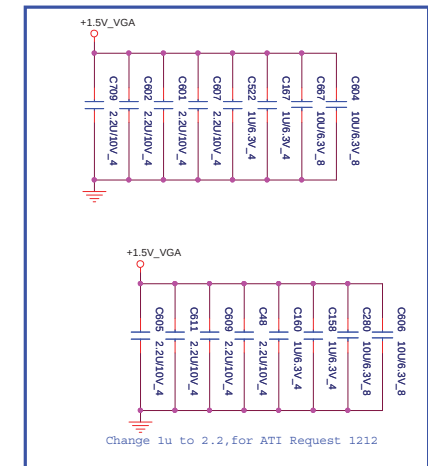
Size Custom	Document Number ATI CAPILANO-PRO(POWER) 5/5	Rev 1A
Date: Wednesday, October 13, 2010		Sheet 19 of 47

1GB GDDR5 : CHANNEL A-0 (64M x 16)

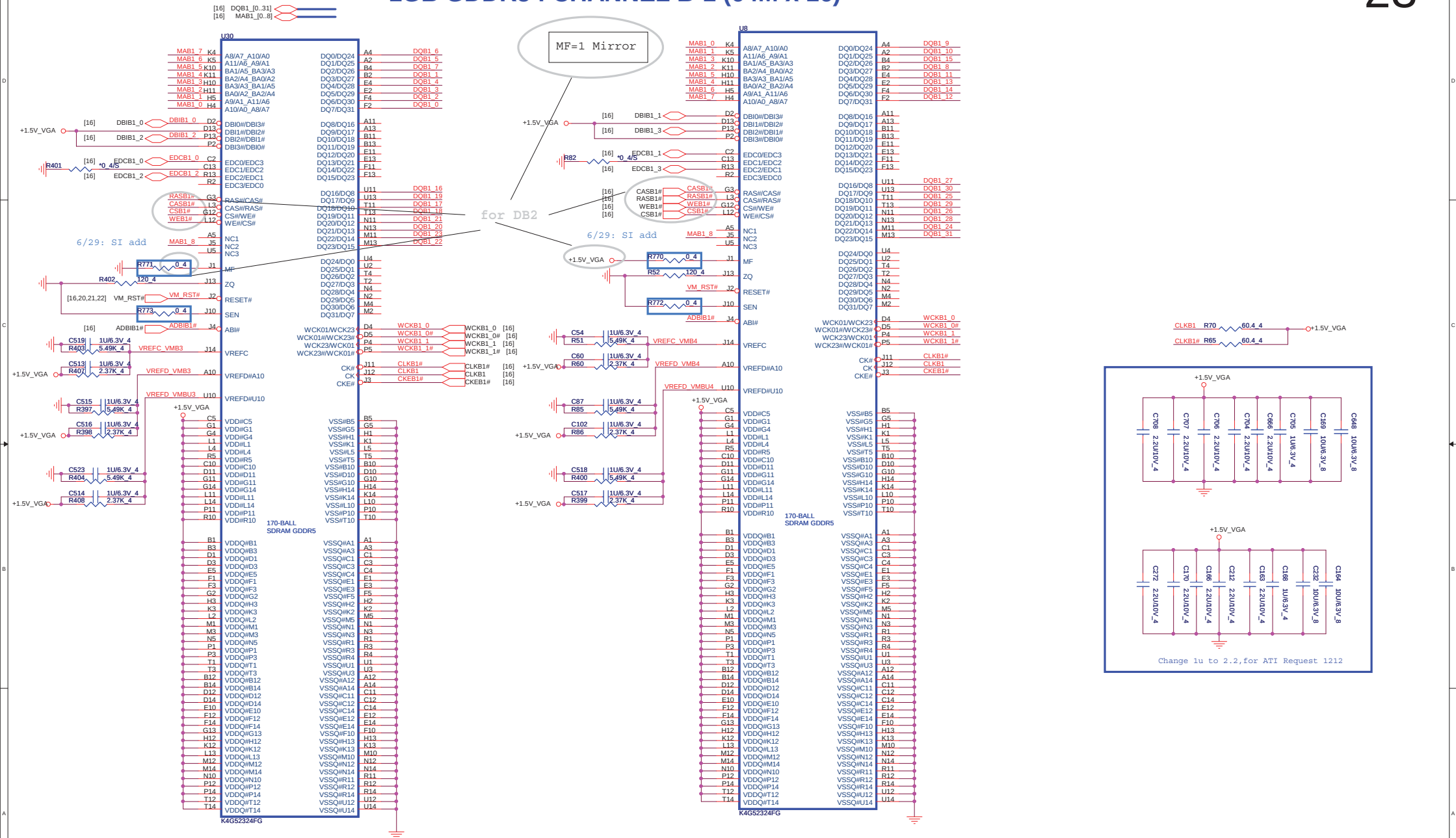


1GB GDDR5 : CHANNEL A-1 (64M x 16)


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1GB GDDR5 : CHANNEL B-1 (64M x 16)



[illegible]

RP27 0_4P2R_4

[17,18] GPU_LVDS_BLON 1 2 LVDS_BLON [25]
[17] GPU_DISP_ON 3 4 DISP_ON [25]

RP29 0_4P2R_4

[17] GPU_EDIDCLK 3 4 EDIDCLK [25]
[17] GPU_EDIDDATA 1 2 EDIDDATA [25]

[17] GPU_DPST_PWM [25] DPST_PWM

[35] PWM_VADJ

0.4

R752

R779

	PCH_LA_CLK	PCH_LA_CLK#	PCH_LA_DATA0P	PCH_LA_DATA0N	PCH_LA_DATA1P	PCH_LA_DATA1N	PCH_LA_DATA2P	PCH_LA_DATA2N
[7]	PCH_LA_CLK	PCH_LA_CLK#	PCH_LA_DATA0P	PCH_LA_DATA0N	PCH_LA_DATA1P	PCH_LA_DATA1N	PCH_LA_DATA2P	PCH_LA_DATA2N
[7]	PCH_LA_CLK#	PCH_LA_CLK	PCH_LA_DATA0N	PCH_LA_DATA0P	PCH_LA_DATA1N	PCH_LA_DATA1P	PCH_LA_DATA2N	PCH_LA_DATA2P
[7]	PCH_LA_DATA0P	PCH_LA_DATA0N	PCH_LA_DATA1P	PCH_LA_DATA1N	PCH_LA_DATA2P	PCH_LA_DATA2N	PCH_LA_DATA3P	PCH_LA_DATA3N
[7]	PCH_LA_DATA0N	PCH_LA_DATA0P	PCH_LA_DATA1N	PCH_LA_DATA1P	PCH_LA_DATA2N	PCH_LA_DATA2P	PCH_LA_DATA3N	PCH_LA_DATA3P
[7]	PCH_LA_DATA1P	PCH_LA_DATA1N	PCH_LA_DATA2P	PCH_LA_DATA2N	PCH_LA_DATA3P	PCH_LA_DATA3N	PCH_LA_DATA4P	PCH_LA_DATA4N
[7]	PCH_LA_DATA1N	PCH_LA_DATA1P	PCH_LA_DATA2N	PCH_LA_DATA2P	PCH_LA_DATA3N	PCH_LA_DATA3P	PCH_LA_DATA4N	PCH_LA_DATA4P
[7]	PCH_LA_DATA2P	PCH_LA_DATA2N	PCH_LA_DATA3P	PCH_LA_DATA3N	PCH_LA_DATA4P	PCH_LA_DATA4N	PCH_LA_DATA5P	PCH_LA_DATA5N
[7]	PCH_LA_DATA2N	PCH_LA_DATA2P	PCH_LA_DATA3N	PCH_LA_DATA3P	PCH_LA_DATA4N	PCH_LA_DATA4P	PCH_LA_DATA5N	PCH_LA_DATA5P

RP1

*0_4P2R_4

[7] PCH_LVDS_BLON

[7] PCH_DISP_ON

PCH LVDS BLON

PCH_DISP_ON

3

4

1

2

LVDS_BLON

DISP_ON

[7] PCH_DPST_PWM

[35] PWM_VADJ

PCH_DPST_PWM R353 *0.4 DPST_PWM

*0.4 R780

[17] GPU_TXCLKOUT+	GPU_TXCLKOUT+ RP30	3	4	0 4P2R 4	TXCLKOUT+	TXCLKOUT+	[25]
[17] GPU_TXCLKOUT-	GPU_TXCLKOUT-	1	4	0 4P2R 4	TXCLKOUT-	TXCLKOUT-	[25]
[17] GPU_TXCLKOUT0+	GPU_TXCLKOUT0+	1	2	TXCLKOUT0	TXCLKOUT0	TXCLKOUT0	[25]
[17] GPU_TXCLKOUT0-	GPU_TXCLKOUT0-	1	2	TXCLKOUT0	TXCLKOUT0	TXCLKOUT0	[25]
[17] GPU_TXCLKOUT1+	GPU_TXCLKOUT1+	1	4	0 4P2R 4	TXCLKOUT1+	TXCLKOUT1+	[25]
[17] GPU_TXCLKOUT1-	GPU_TXCLKOUT1-	1	2	TXCLKOUT1	TXCLKOUT1	TXCLKOUT1	[25]
[17] GPU_TXCLKOUT2+	GPU_TXCLKOUT2+	1	4	0 4P2R 4	TXCLKOUT2+	TXCLKOUT2+	[25]
[17] GPU_TXCLKOUT2-	GPU_TXCLKOUT2-	1	2	TXCLKOUT2	TXCLKOUT2	TXCLKOUT2	[25]

[illegible]

[17] GPU_CRT_R GPU_CRT_R R776 0.4 CRT_R_CON [26]

[17] GPU_CRT_G GPU_CRT_G R777 0.4 CRT_G_CON [26]

[17] GPU_CRT_B GPU_CRT_B R778 0.4 CRT_B_CON [26]

RP26 0_4P2R_4

[17,18] GPU_HSYNC 3 HSYNC COM [26]
[17,18] GPU_VSYNC 1 VSYNC COM [26]

RP28 0_4P2R_4

[17] GPU_DDCCLK 3 DDCCLK COM 4 DDCCLK COM [26]
[17] GPU_DDCDATA 1 DDCDATA COM 2 DDCDATA COM [26]

[7] PCH_CRT_R PCH_CRT_R R389 *0.4 CRT_R_CON

[7] PCH_CRT_G PCH_CRT_G R388 *0.4 CRT_G_CON

[7] PCH_CRT_B PCH_CRT_B R377 *0.4 CRT_B_CON

[7] PCH_HSYNC PCH_HSYNC
 [7] PCH_VSYNC PCH_VSYNC

1 2
 3 4

HSYNC_COM
 VSYNC_COM

BB16 #0_4B2B_4

5/11:for Layout modify

RP17

*0_4P2R_4

[7] PCH_DDCCLK

[7] PCH_DDCDATA

1

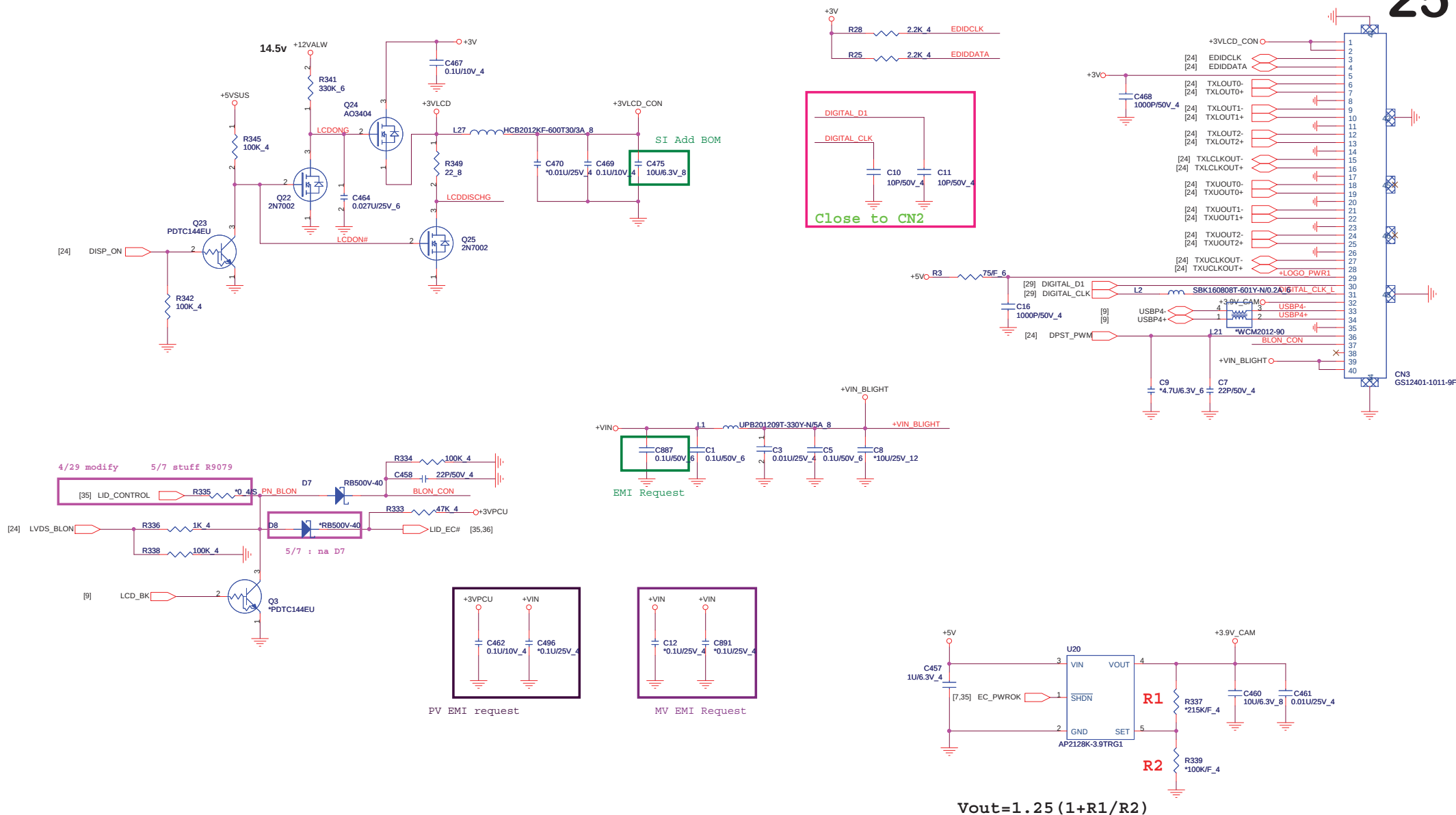
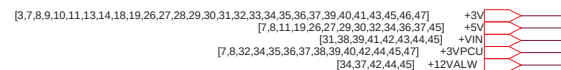
2

3

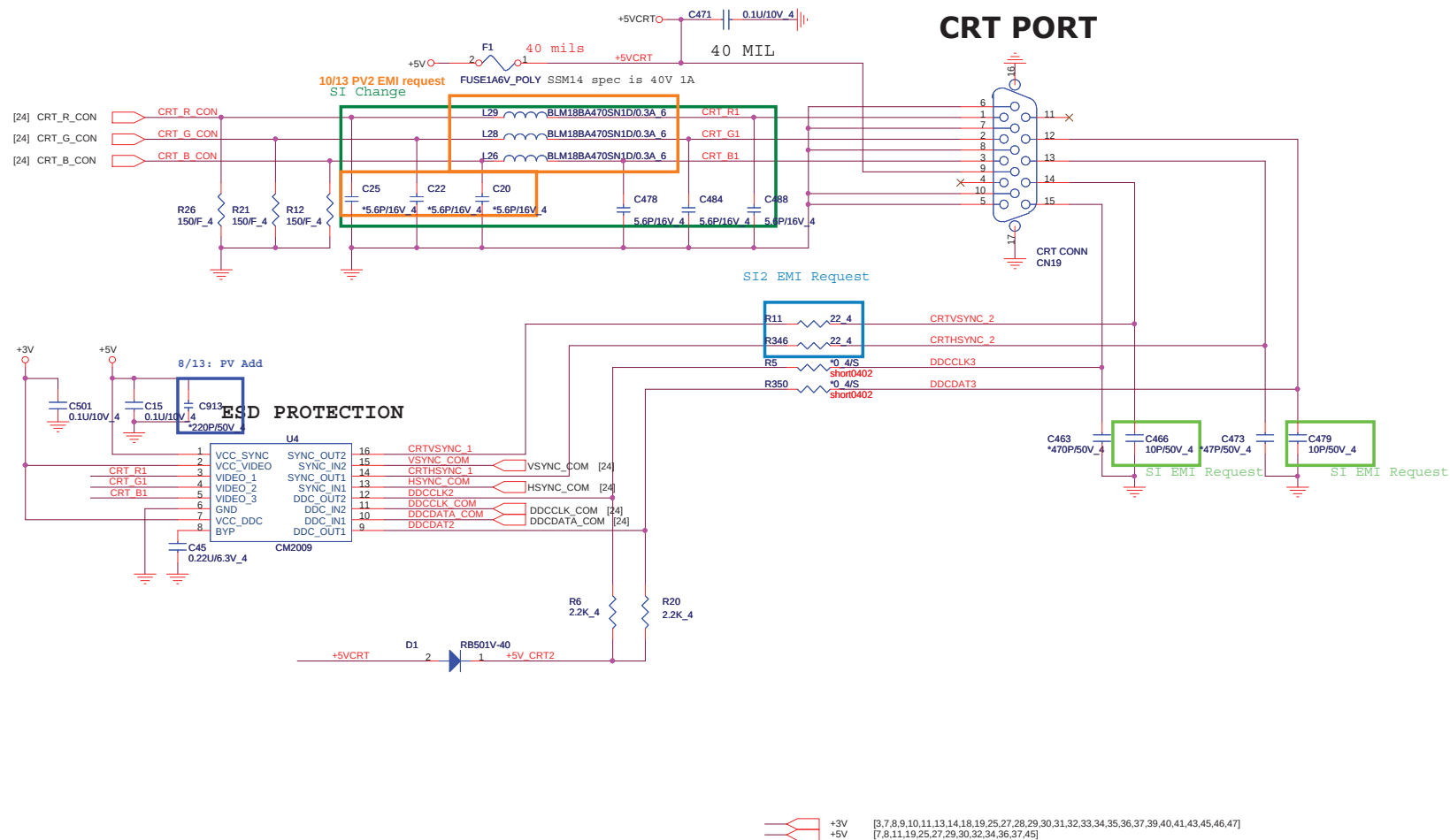
4

DDCCLK_COM

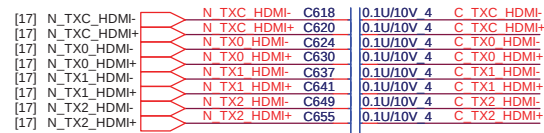
DDCDATA_COM


$$V_{out} = 1.25 (1 + R_1/R_2)$$


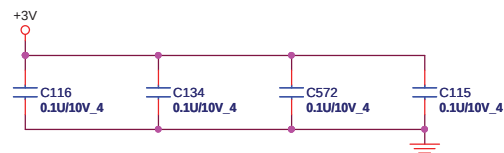
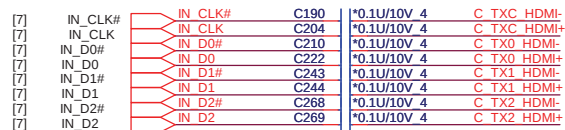
<http://hobi-elektronika.net>



DIS/SG HDMI



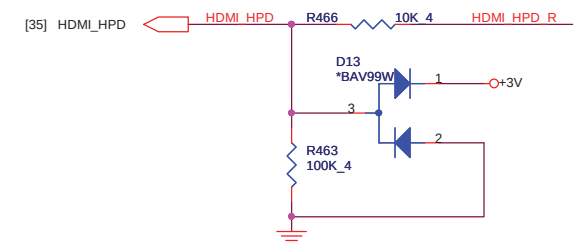
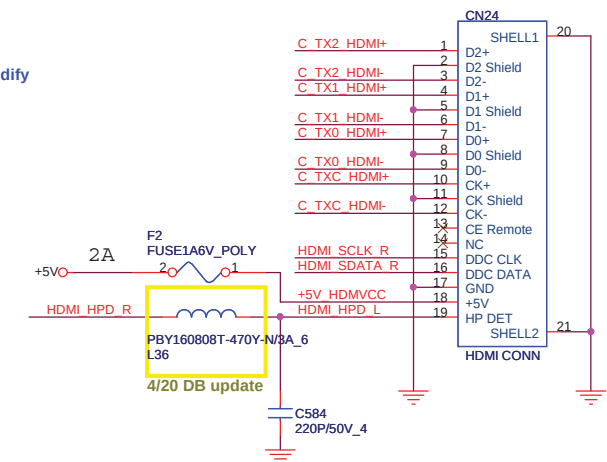
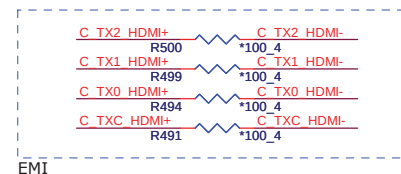
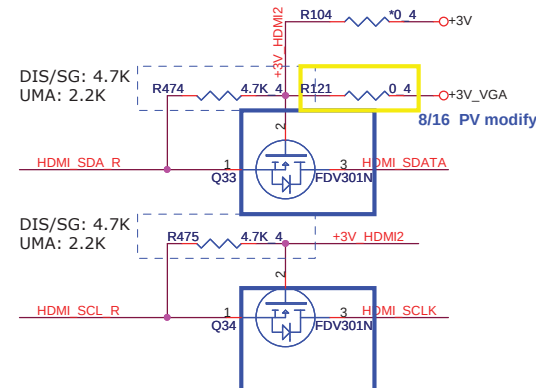
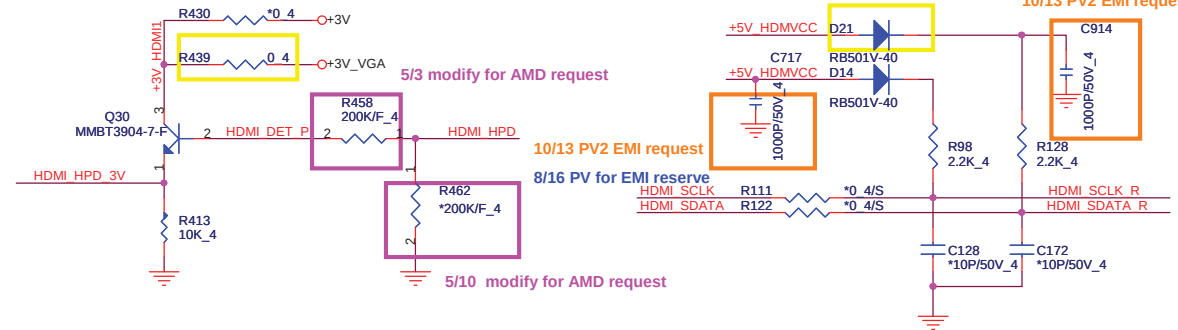
UMA ONLY HDMI



HDMI CON_COM

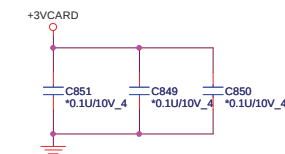
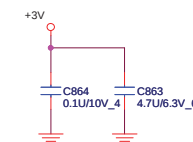
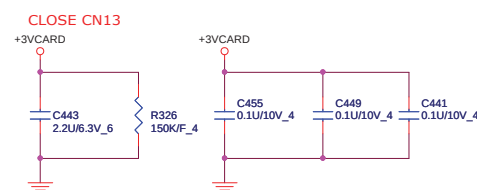
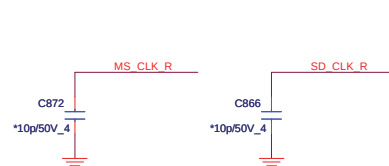
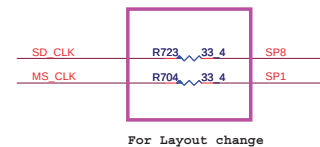
9/26: MV Del C906,C914
9/26: MV Add D21

10/13 PV2 EMI request

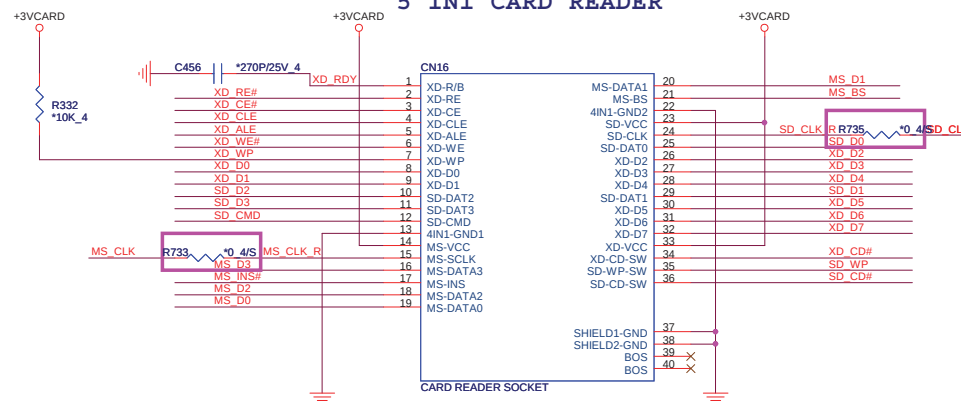


PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size Custom	Document Number KB/POWER CONN	Rev 1A
Date: Wednesday, October 13, 2010 Sheet 27 of 47		



XD,MMC/SD,MS/MSP
5 IN1 CARD READER



5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

<http://hobi-elektronika.net>



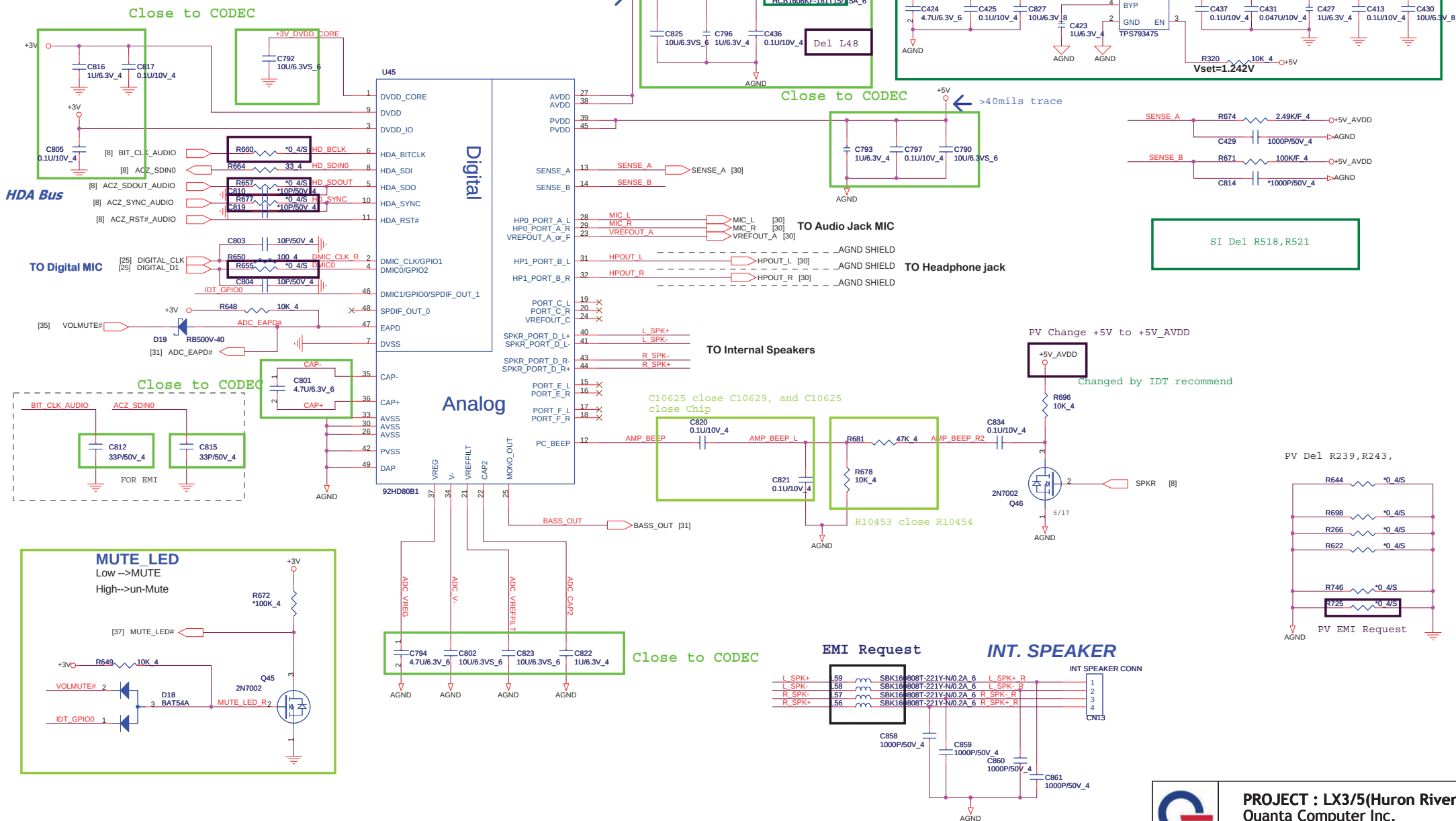
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size Custom	Document Number DTSE138 & CD SOCKET
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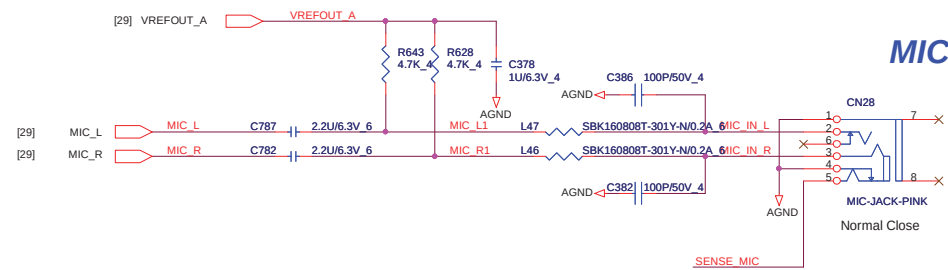
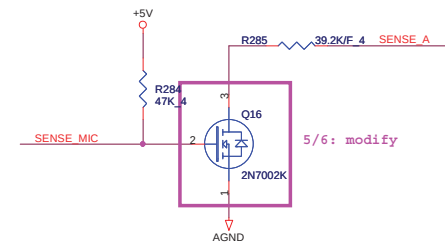
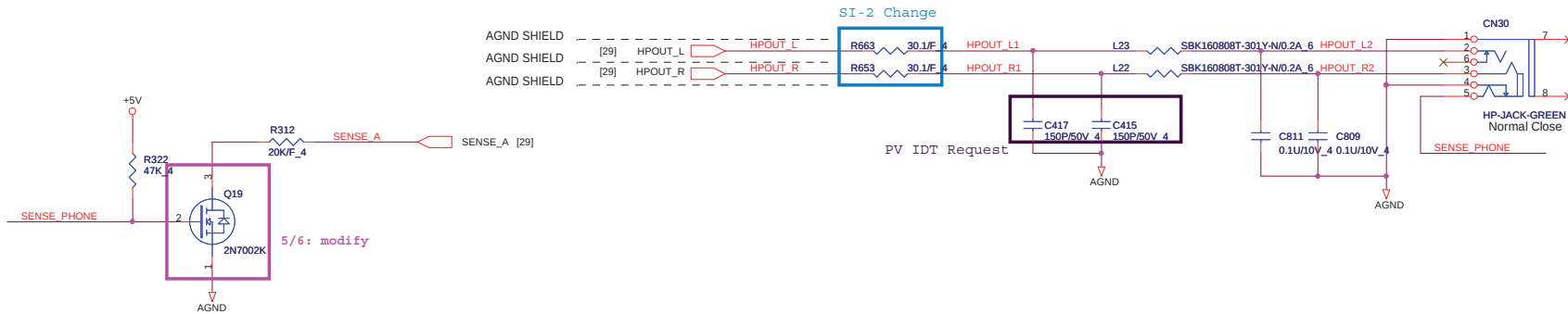
Custom	RTS5138 & CR SOCKET	
Date: Wednesday, October 13, 2010	Sheet	28

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1A

[3,7,8,9,10,11,13,14,18,19,25,26,27,28,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47] +3V
[31] +4.75VAVDD
[7,8,11,19,25,26,27,30,32,34,36,37,45] +5V

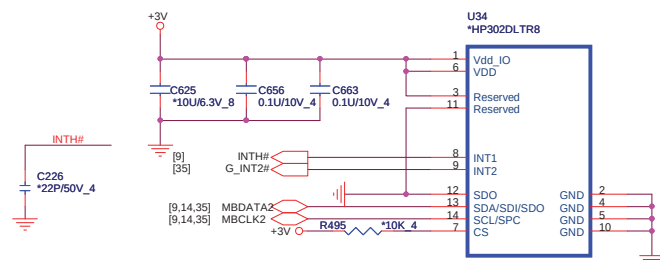


Line out

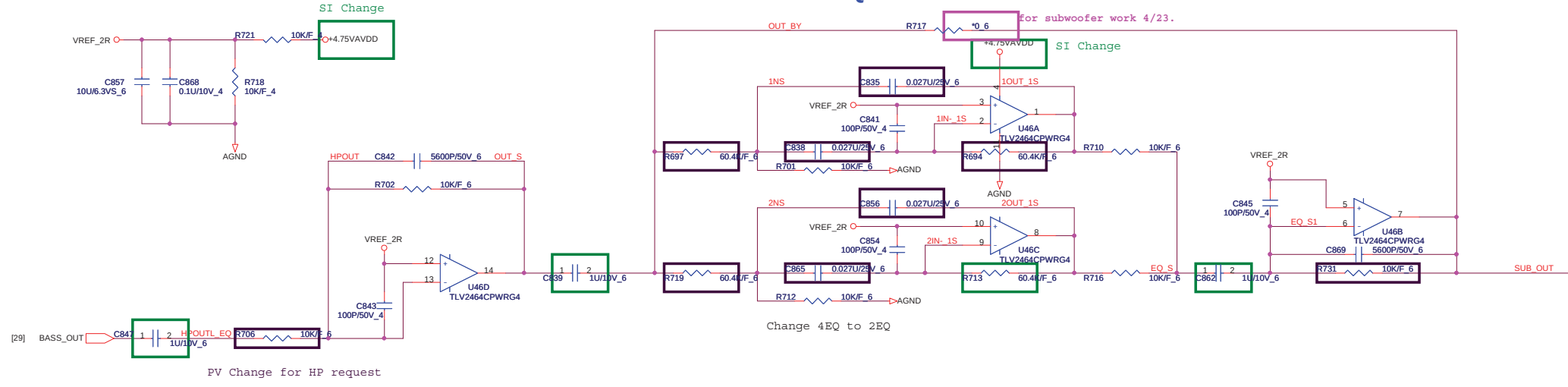


MIC

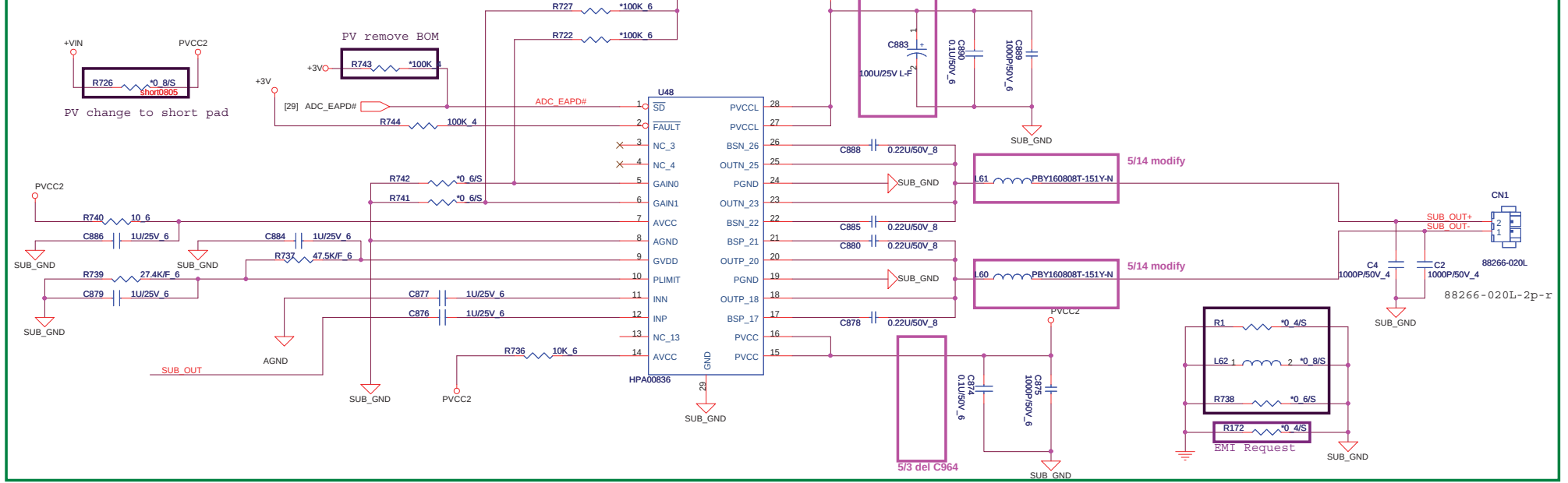
Accelerometer Sensor



EQ FOR SUBWOOFER



Sub-Woofer power



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

<http://hobi-elektronika.net>

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

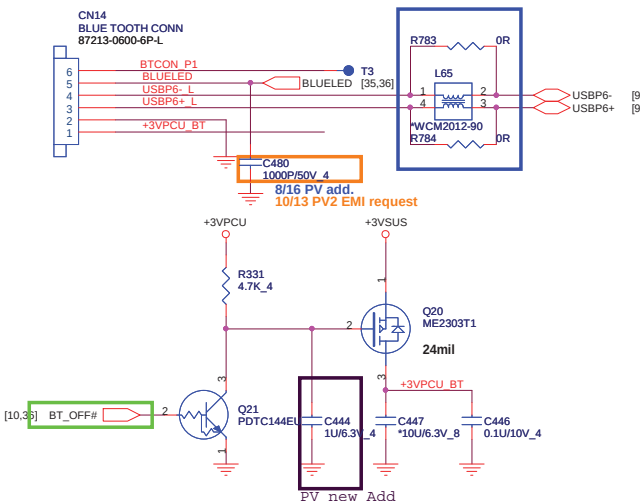
Size Custom

Document Number SUBWOOFER (EQ & AMP.)

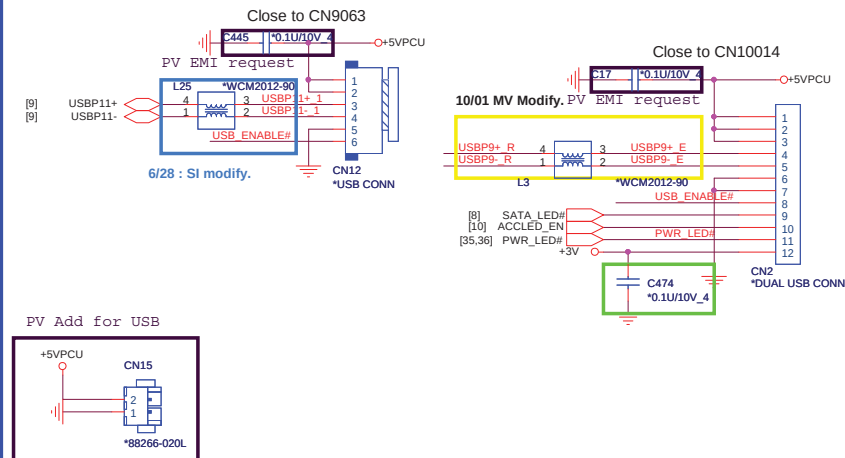
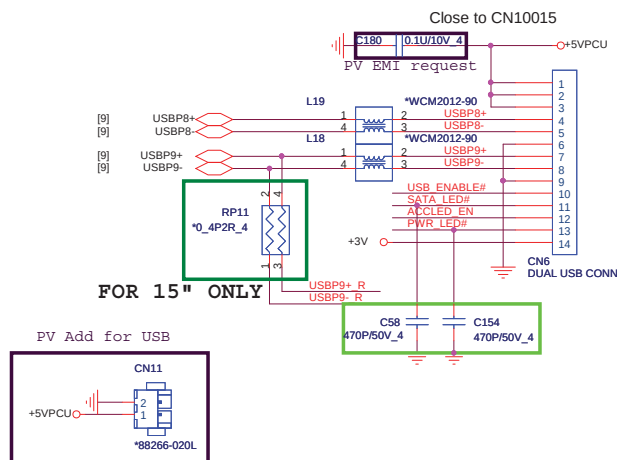
Date: Wednesday, October 13, 2010

Rev 1A

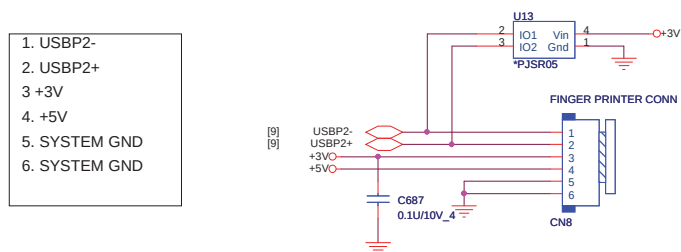
Sheet 31 of 47



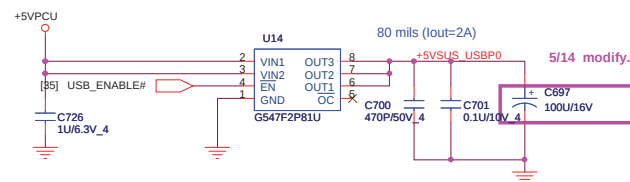
RIGHT SIDE USB for 15"



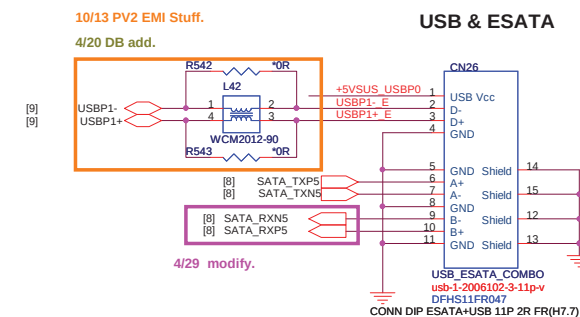
USB fingerprint CON



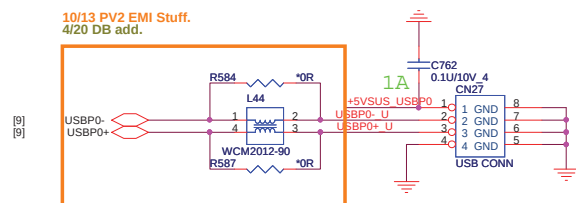
E-SATA



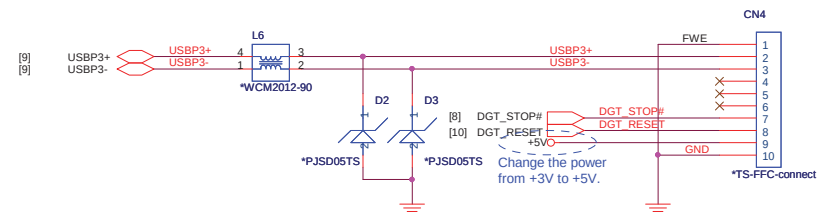
USB & ESATA



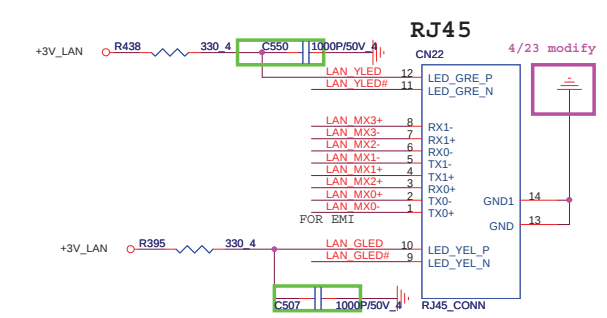
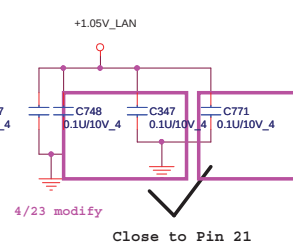
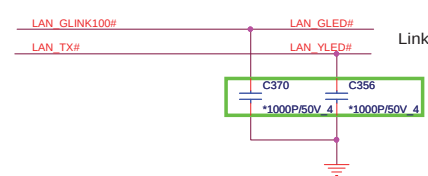
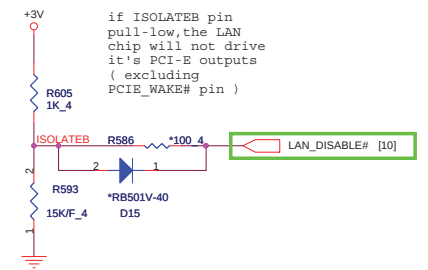
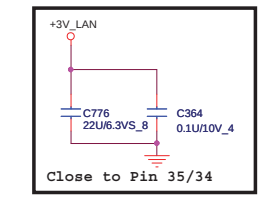
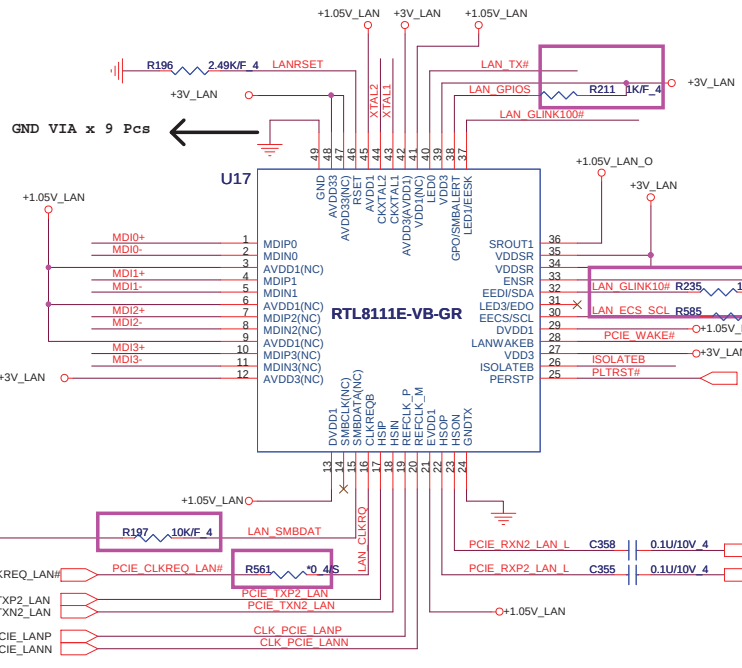
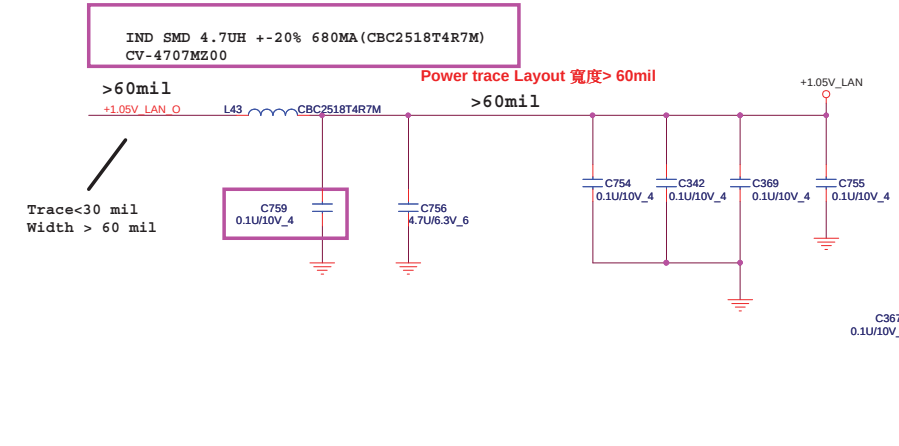
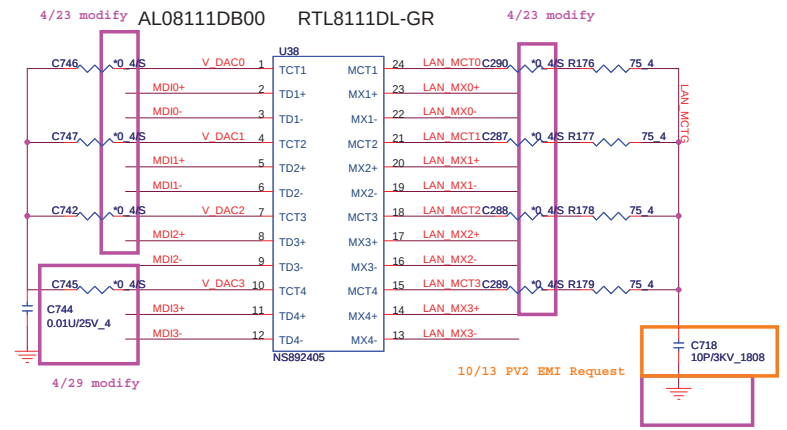
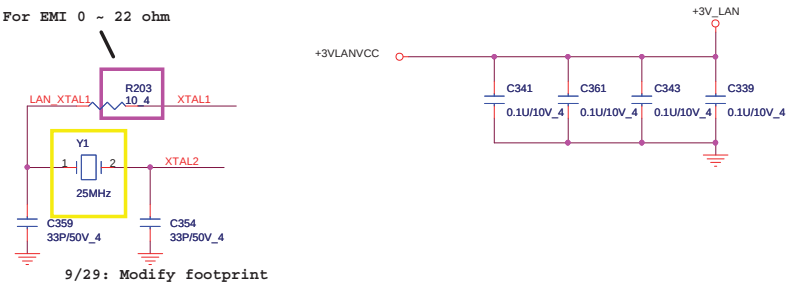
LEFT USB PORT



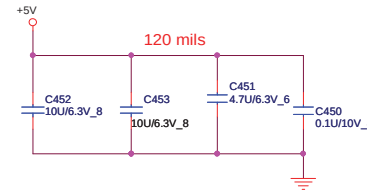
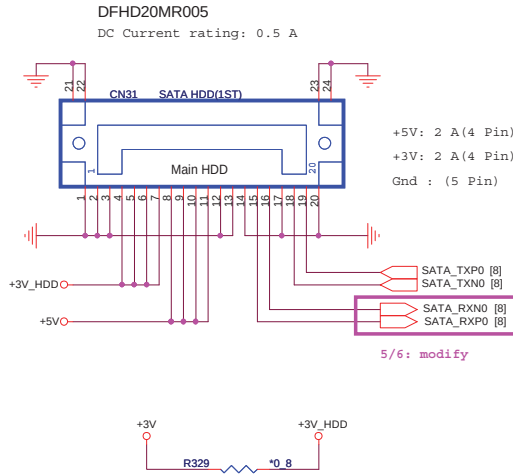
Touch screen for 15"



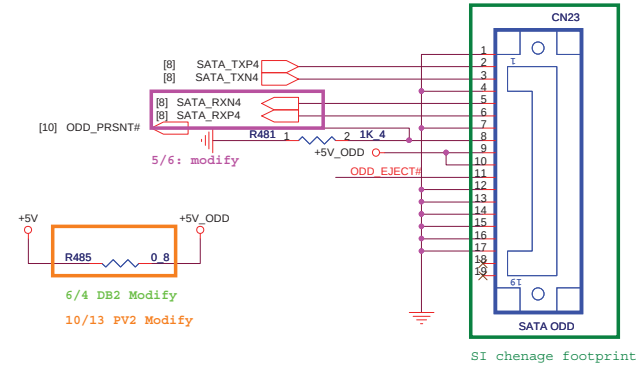
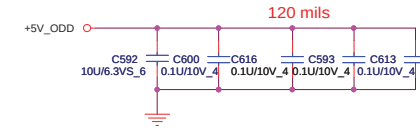
For EMI 0 ~ 22 ohm



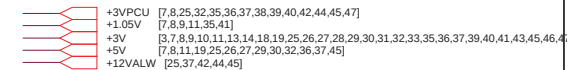
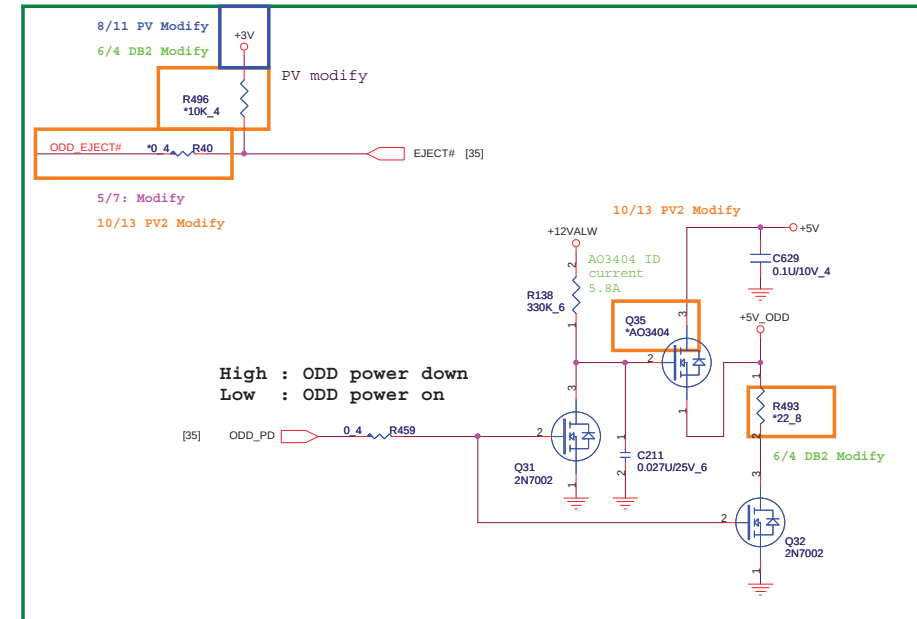
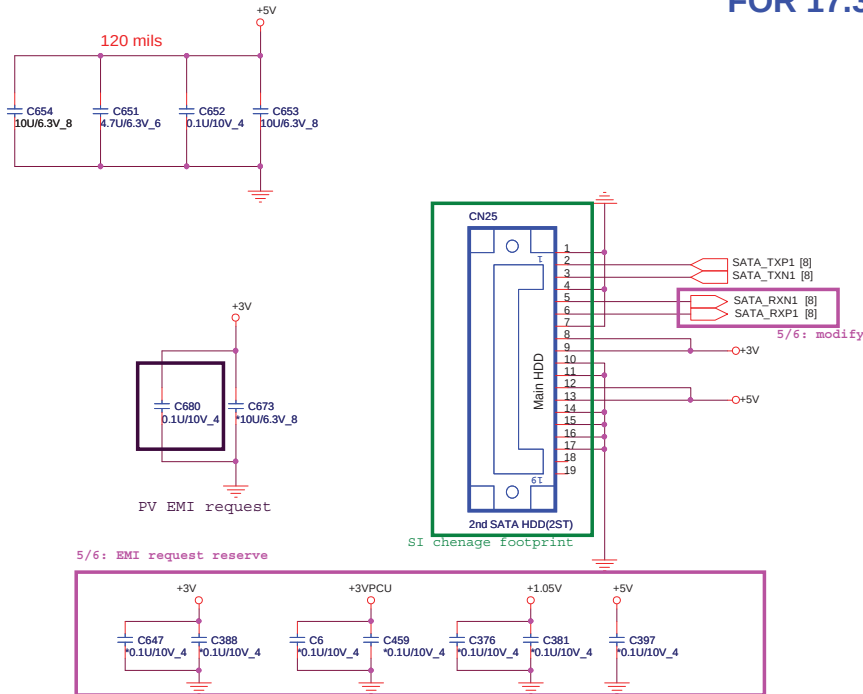
SATA HDD CONNECTOR



SATA CD-ROM

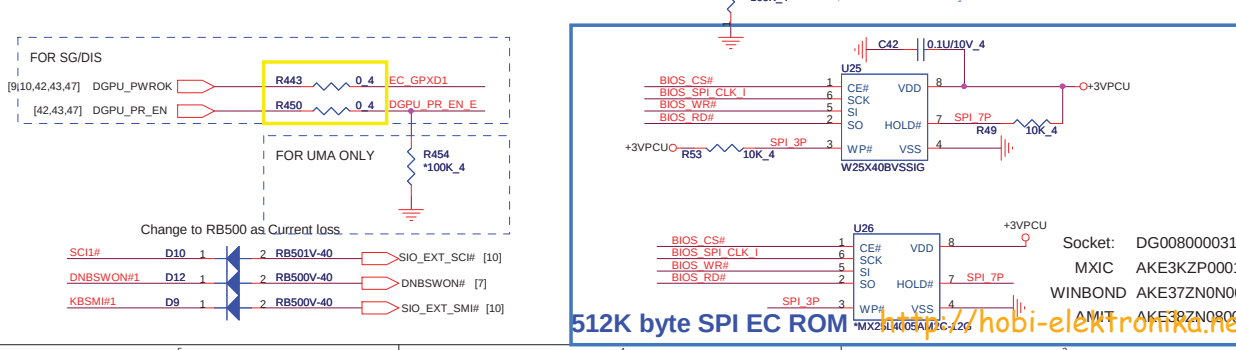
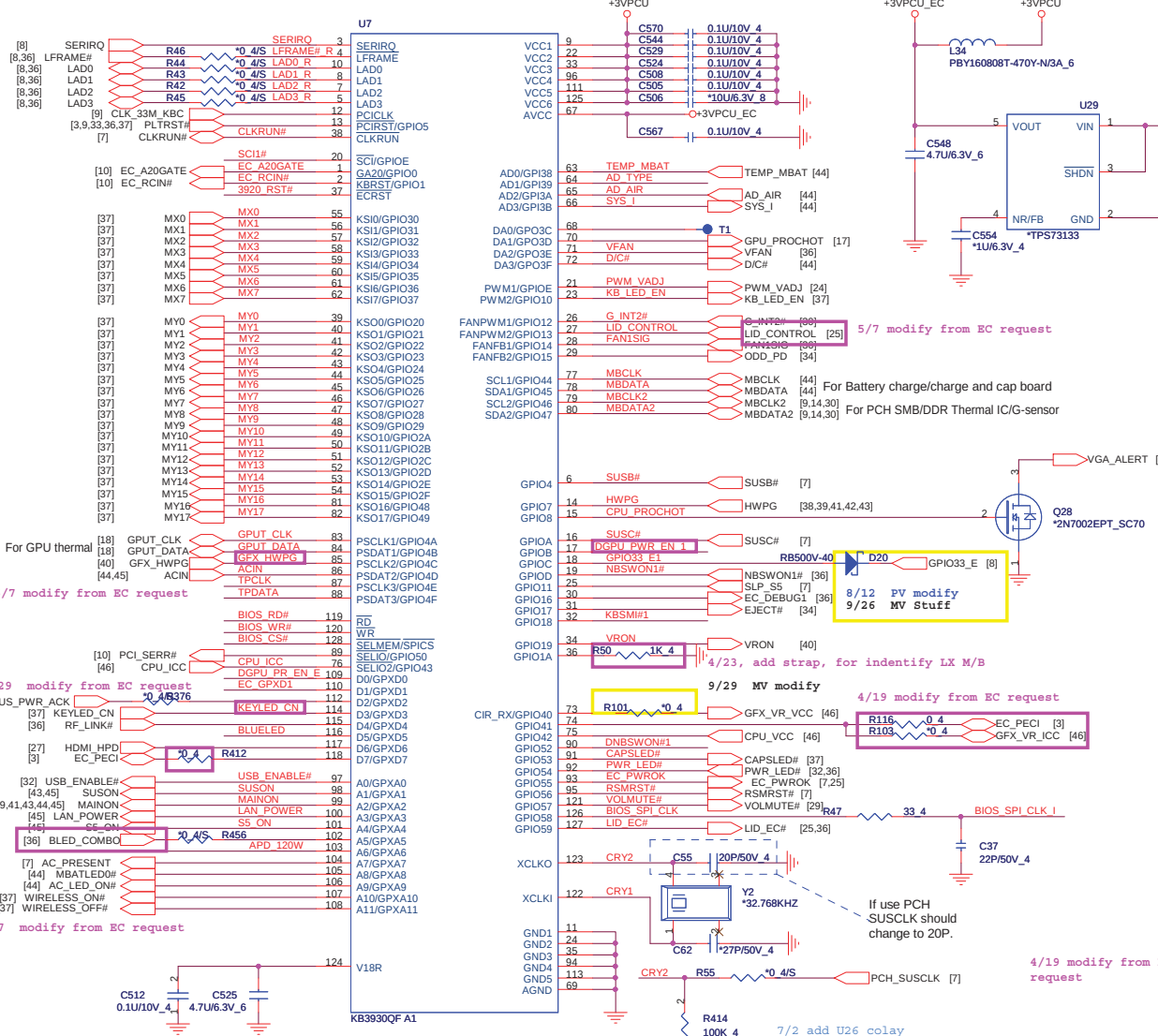
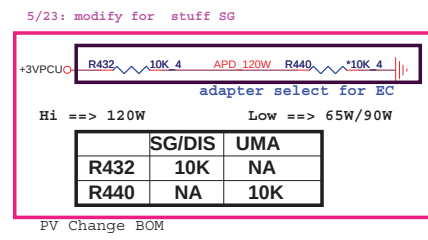
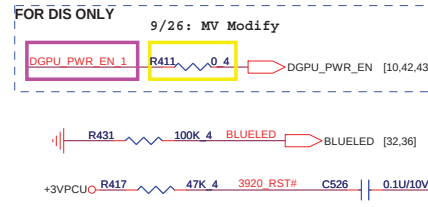
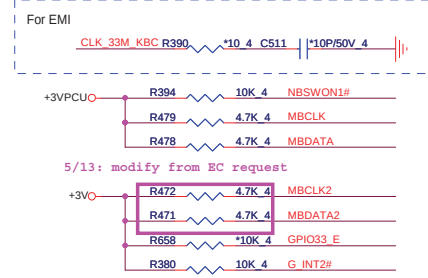
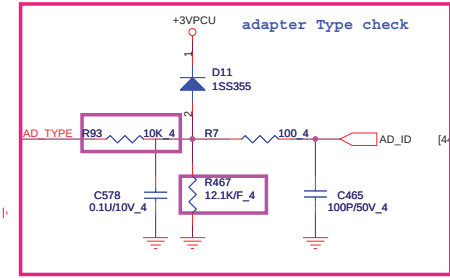
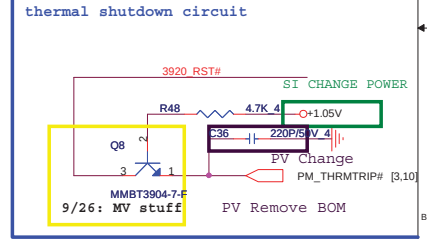
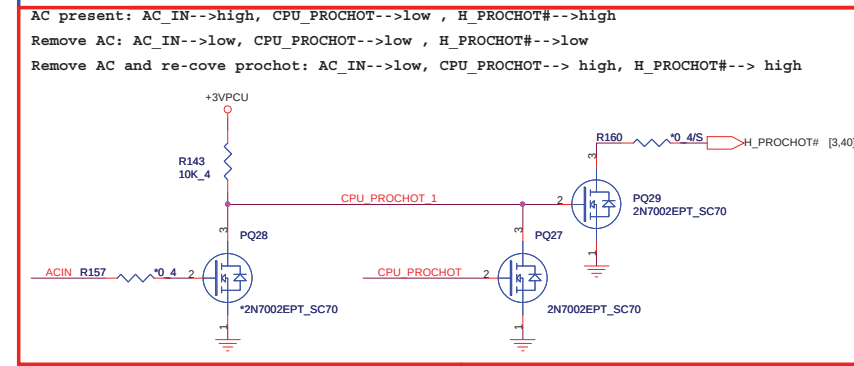
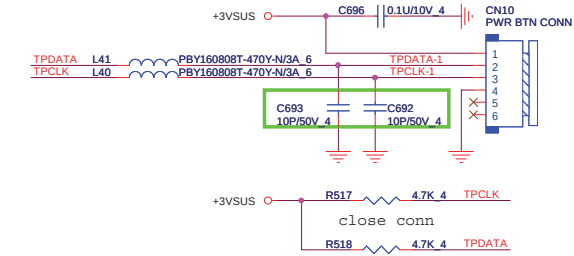


SATA_2 CONNECTOR FOR 17.3"

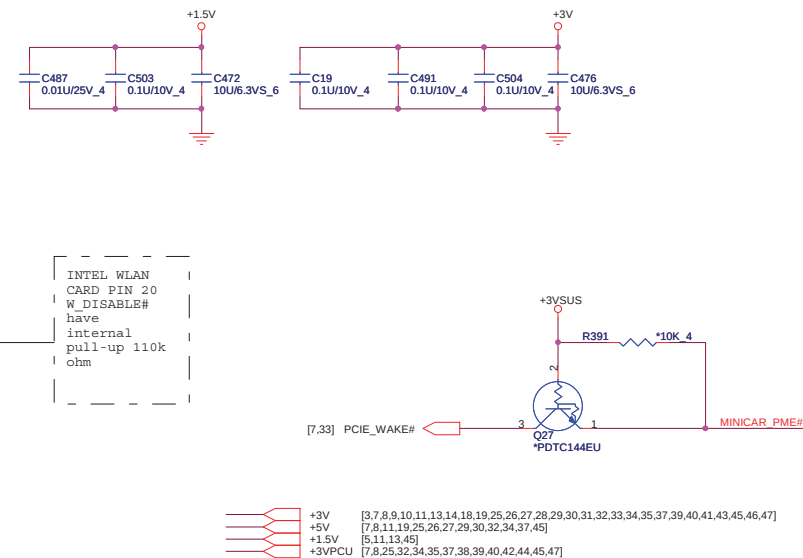
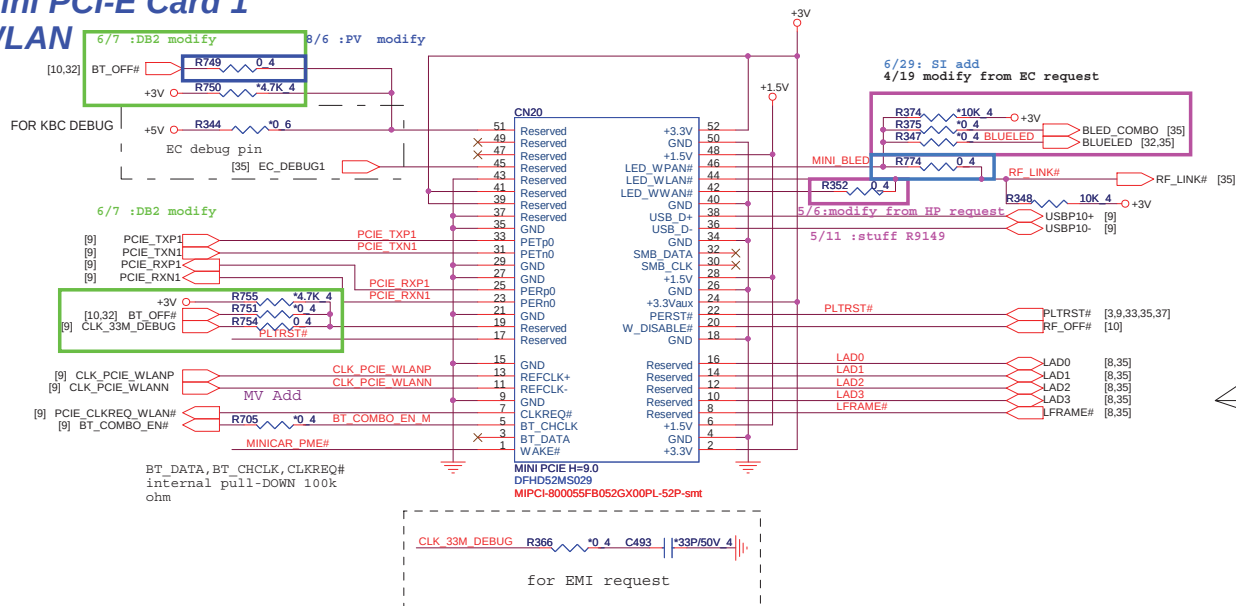


<http://hobi-elektronika.net>

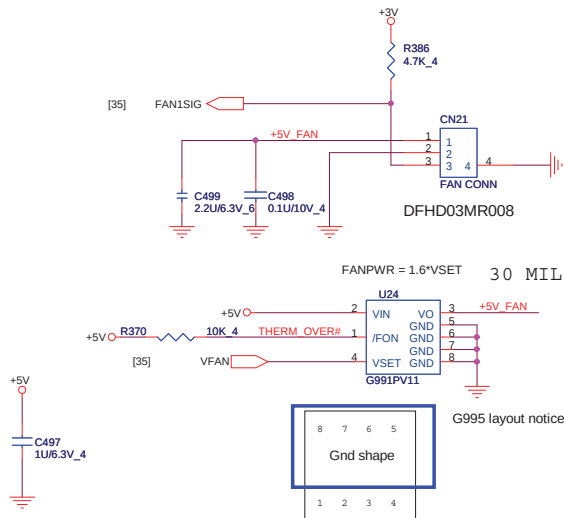
TOUCH PAD CONNECTOR & ON/OFF BOTTOM



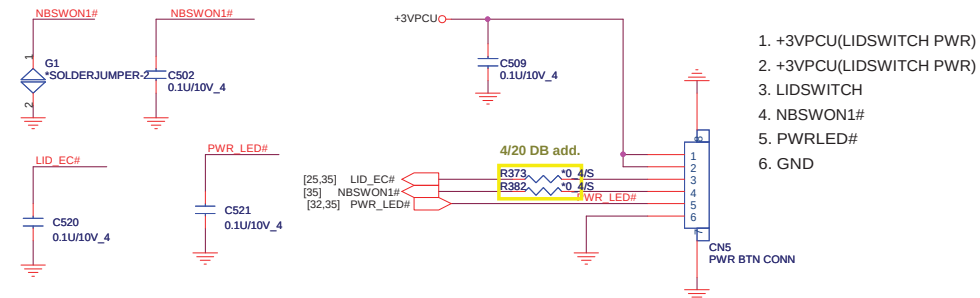
Mini PCI-E Card 1



CPU FAN

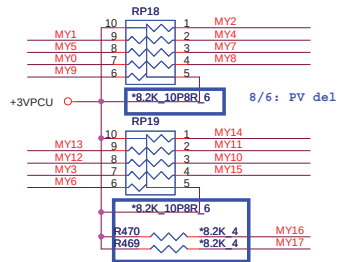


POWER BOTTON CONNECT



1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. NBSWON1#
5. PWRLED#
6. GND

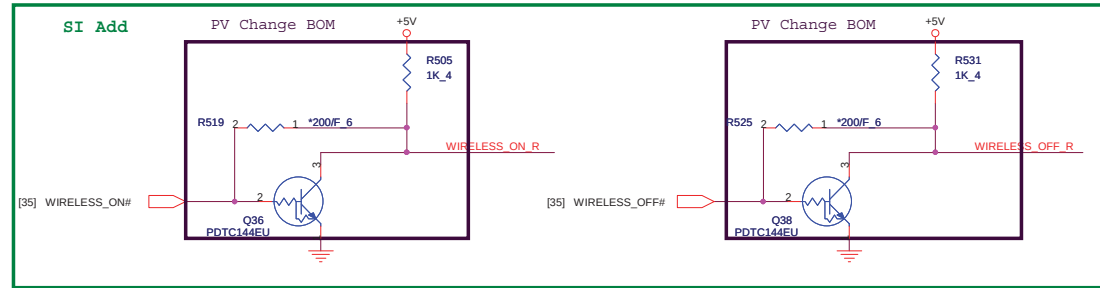
KEYBOARD PULL-UP



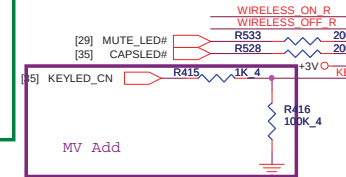
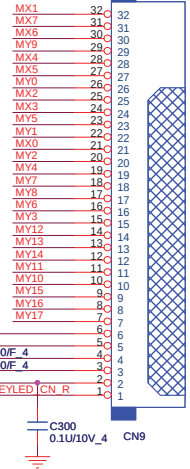
clear ABS 758 resin for key cap.

7 LEDs for 15.4" (total LED current 140mA)

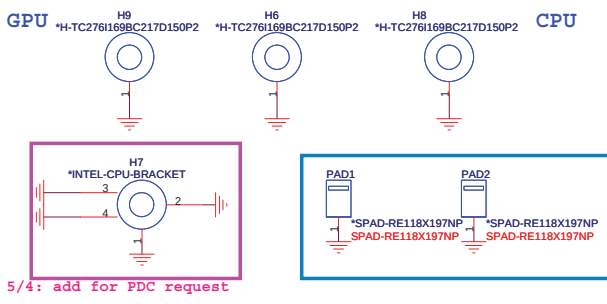
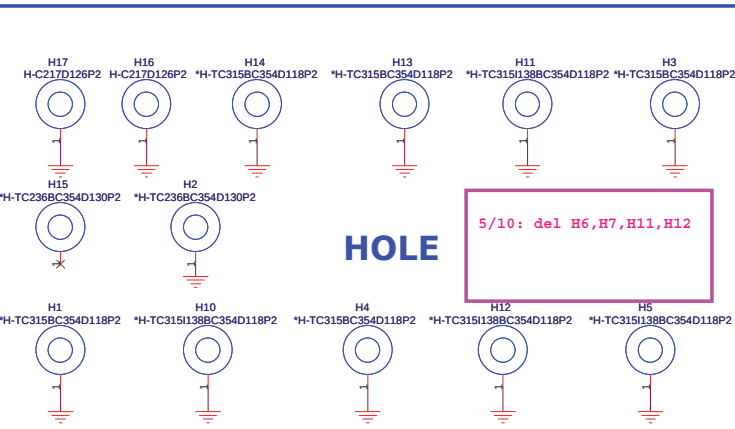
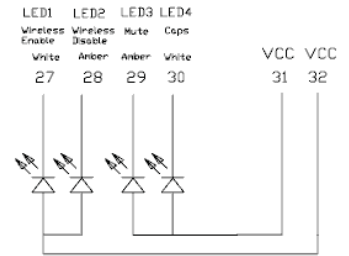
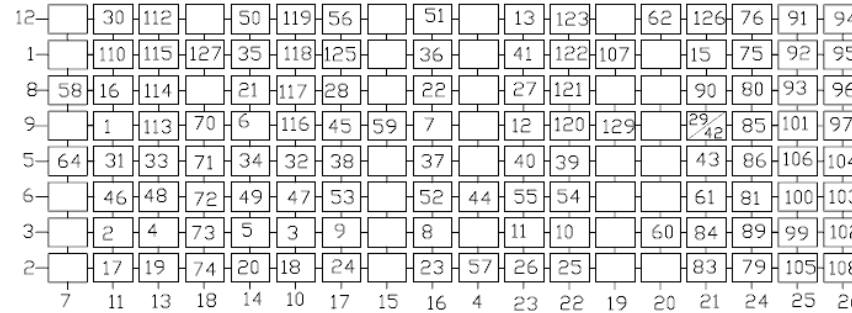
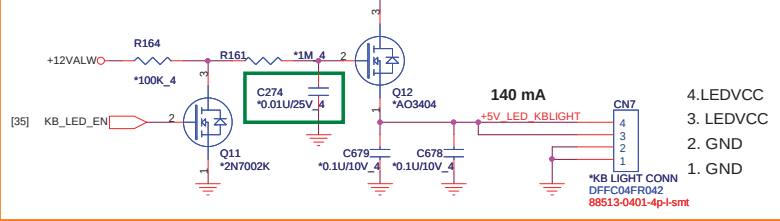
11 LEDs for 17" (Total LED current 220mA)



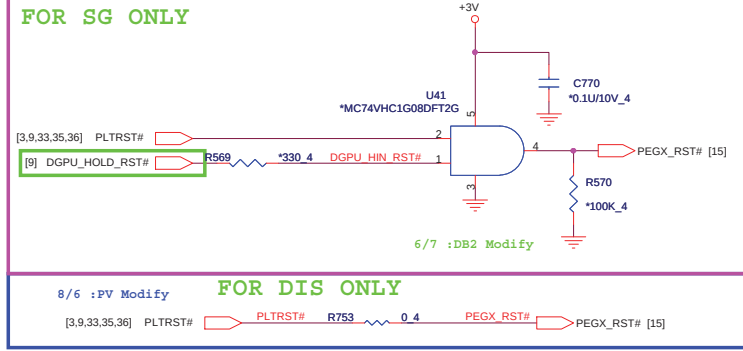
KB CONN



KB backlight for 15"



FOR SG ONLY



FOR DIS ONLY



PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

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Custom	KB	1A

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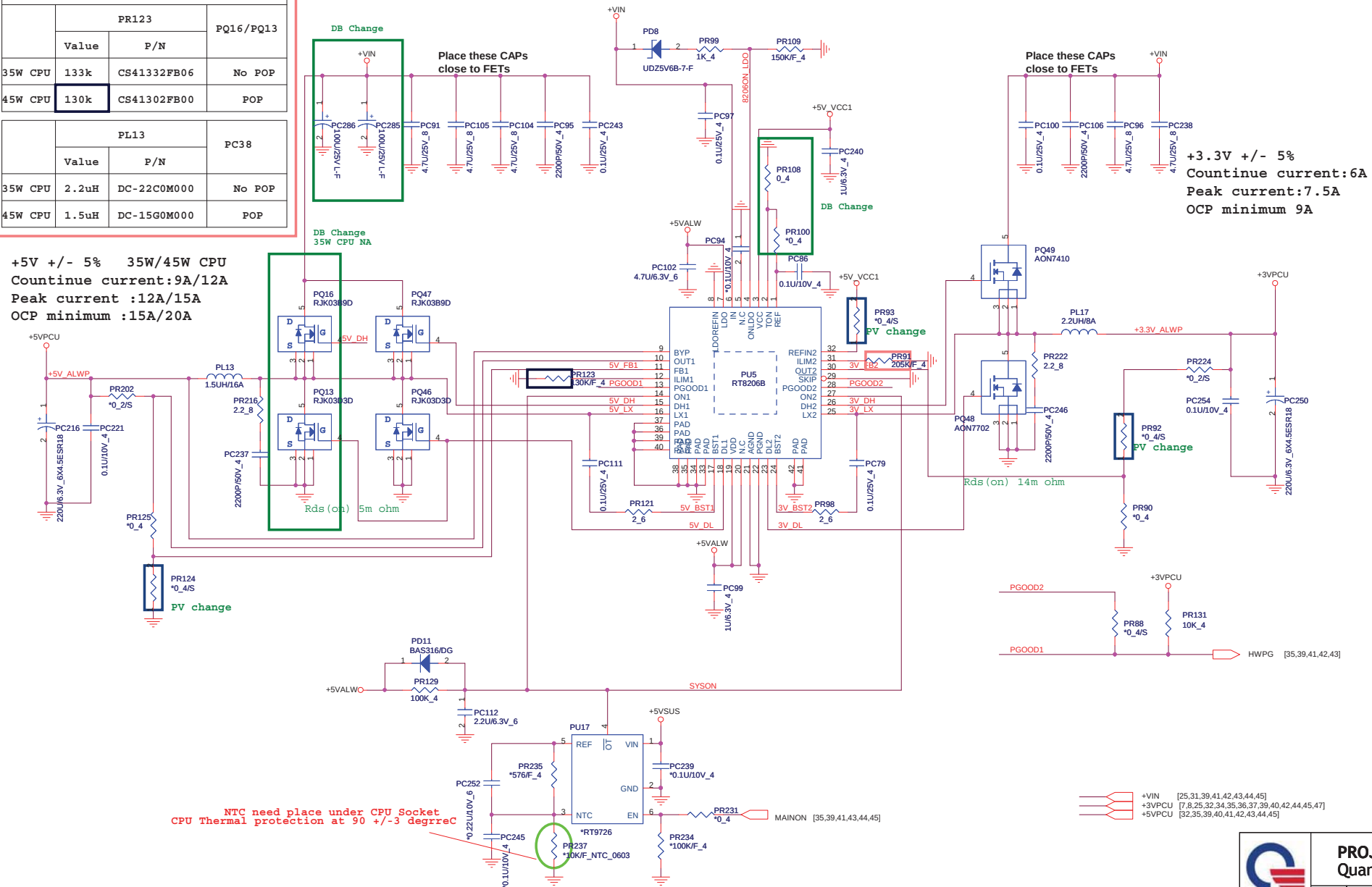
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

5VPCU setting

	PR123		PQ16/PQ13
	Value	P/N	
35W CPU	133k	CS41332FB06	No POP
45W CPU	130k	CS41302FB00	POP

	PL13		PC38
	Value	P/N	
35W CPU	2.2uH	DC-22C0M000	No POP
45W CPU	1.5uH	DC-15G0M000	POP

+5V +/- 5% 35W/45W CPU
 Countinue current:9A/12A
 Peak current :12A/15A
 OCP minimum :15A/20A

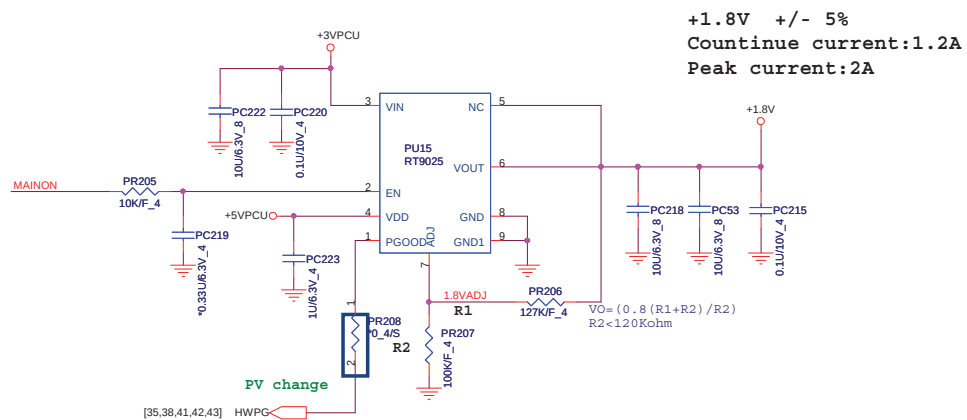
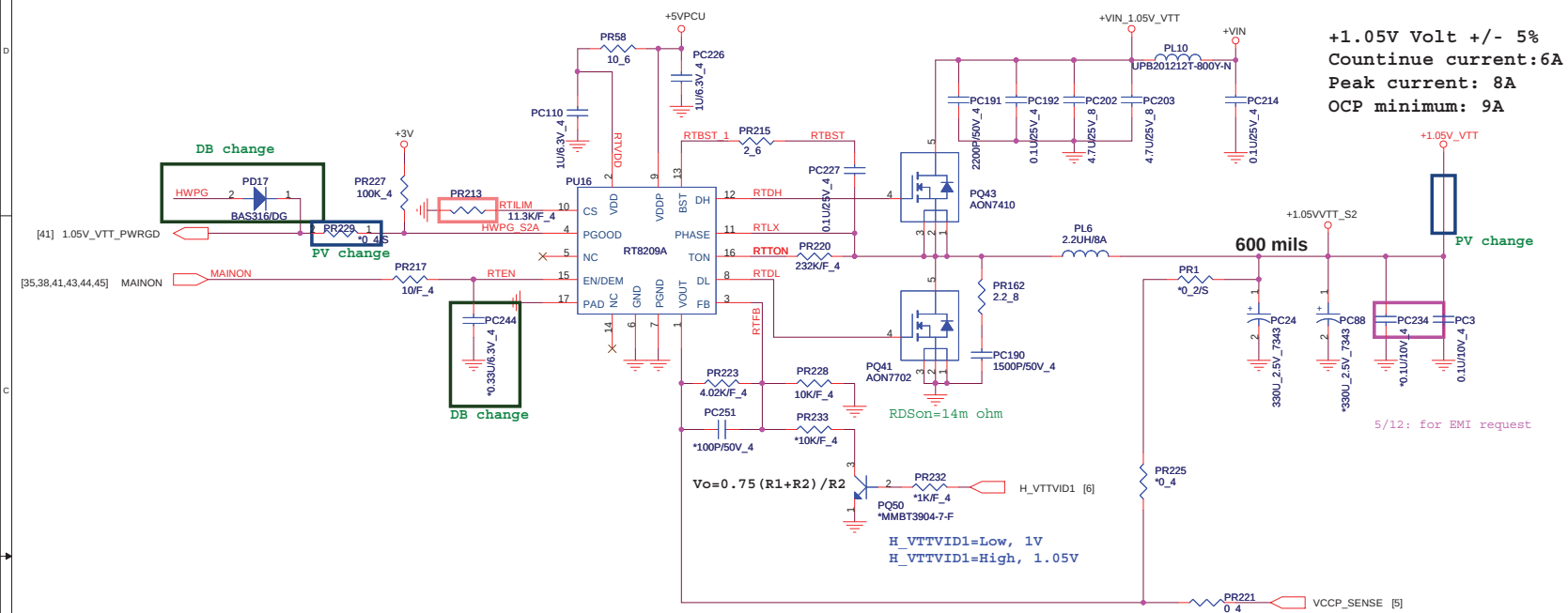


<http://hobi-elektronika.net>



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A
Date: Wednesday, October 13, 2010 Sheet 38 of 47		

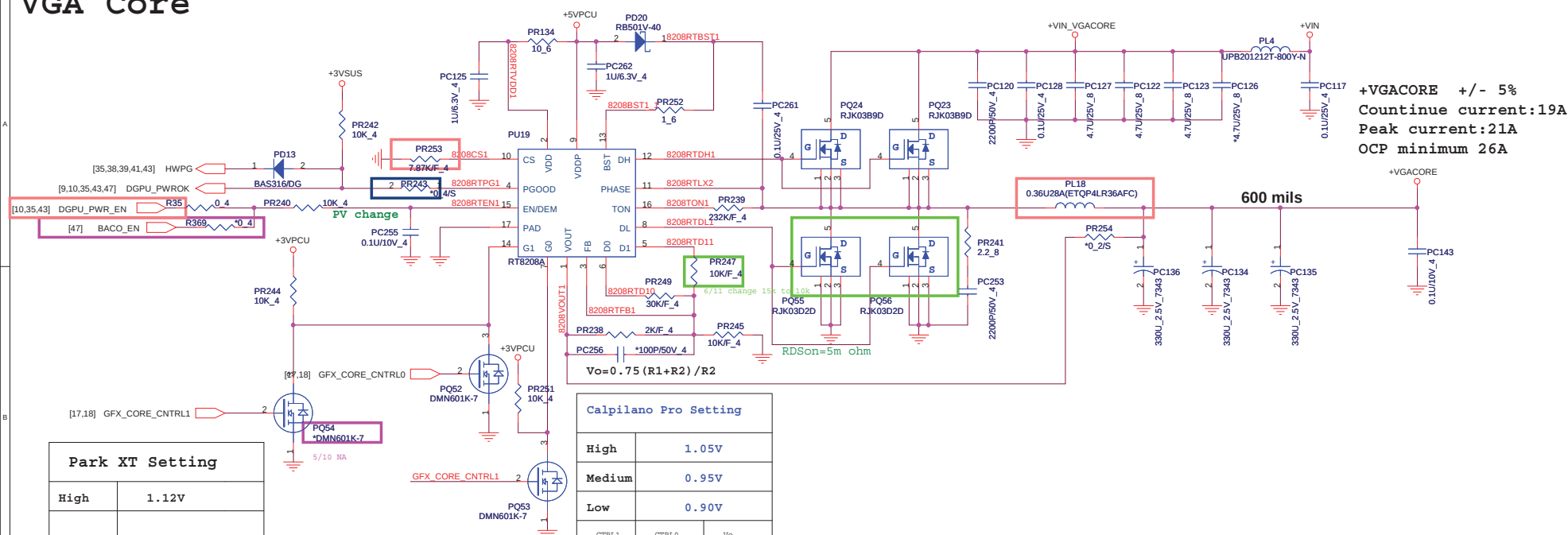






	VCCSA_SEL	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.8V
1	1	0.8V

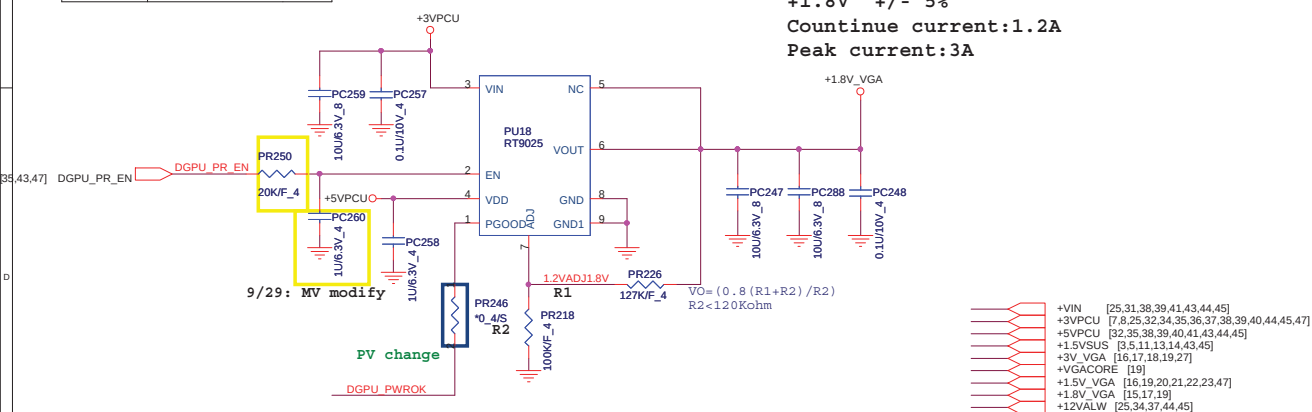




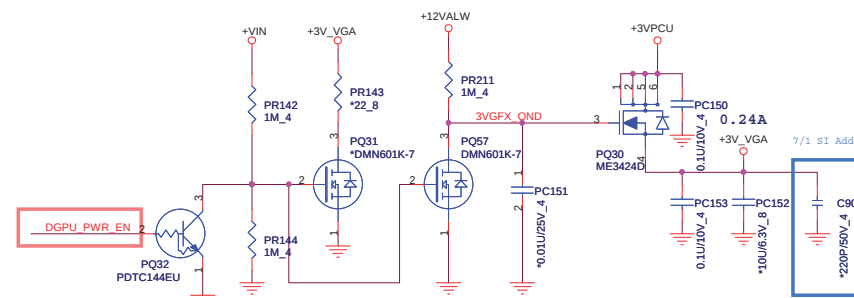
Park XT Setting		
High	1.12V	
Low	0.90V	
CTRL0	CTRL1	Vo
0	0	1.12
0	1	0.9
不上位	PR187 PR188 PQ58 PQ59 PQ61 PQ25 PC122 PC121	
改科	PR190=6.81k (CS26812FB01) PR195=9.09k (CS29092FB02) PQ24=RJX01B9D(BAW01B90000) PQ60=RJX03D3D(BAW03D30000)	

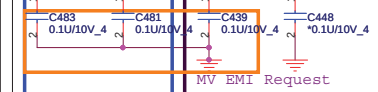
Calpilano Pro Setting		
High	1.05V	
Medium	0.95V	
Low	0.90V	
CTRL1	CTRL0	Vo
0	0	1.05
0	1	1
1	0	0.95
1	1	0.9
不上件	PC122	
改料	PC120 PC121=CH7338M8631	

+1.8V +/- 5%
Continue current:1.2A
Peak current:3A



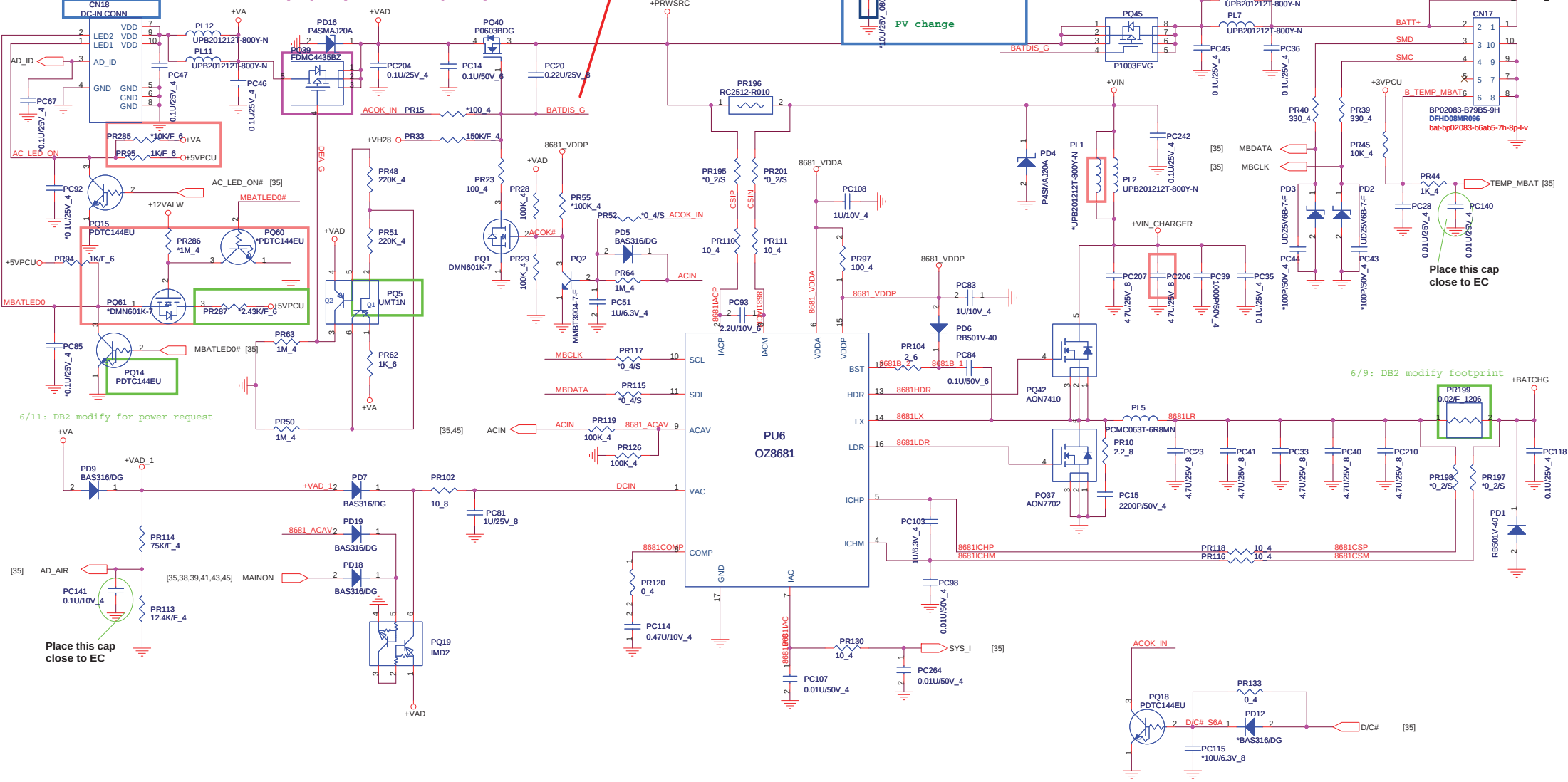
<http://hobi-elektronika.net>



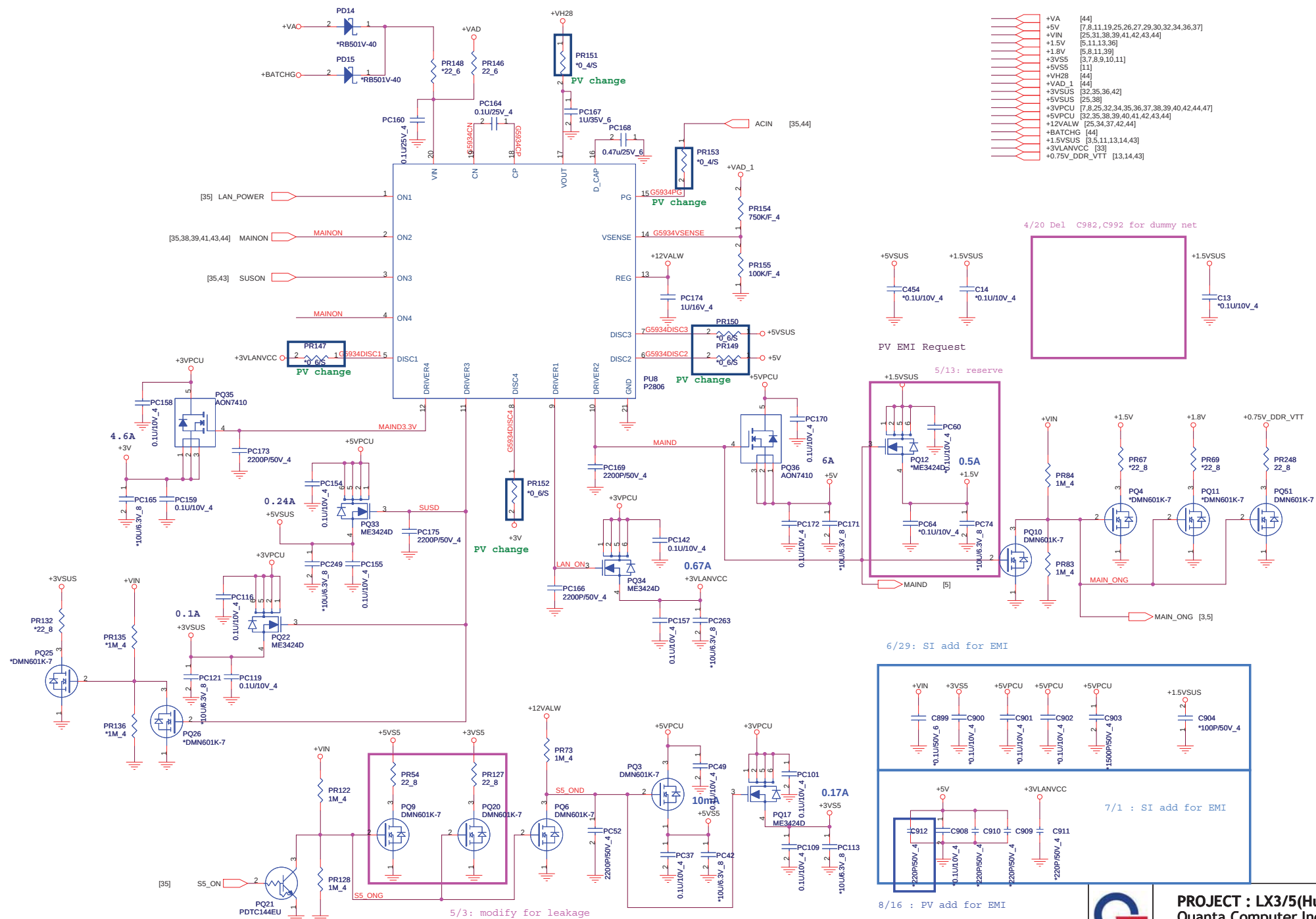


Do Not add test pad on BATDIS_G signal

PV change



- +VA [45]
- +VH28 [45]
- +VAD_1 [45]
- +3VPCU [7,8,25,32,34,35,36,37,38,39,40,42,45,47]
- +5VPCU [32,35,38,39,40,41,42,43,45]
- +BATCHG [45]

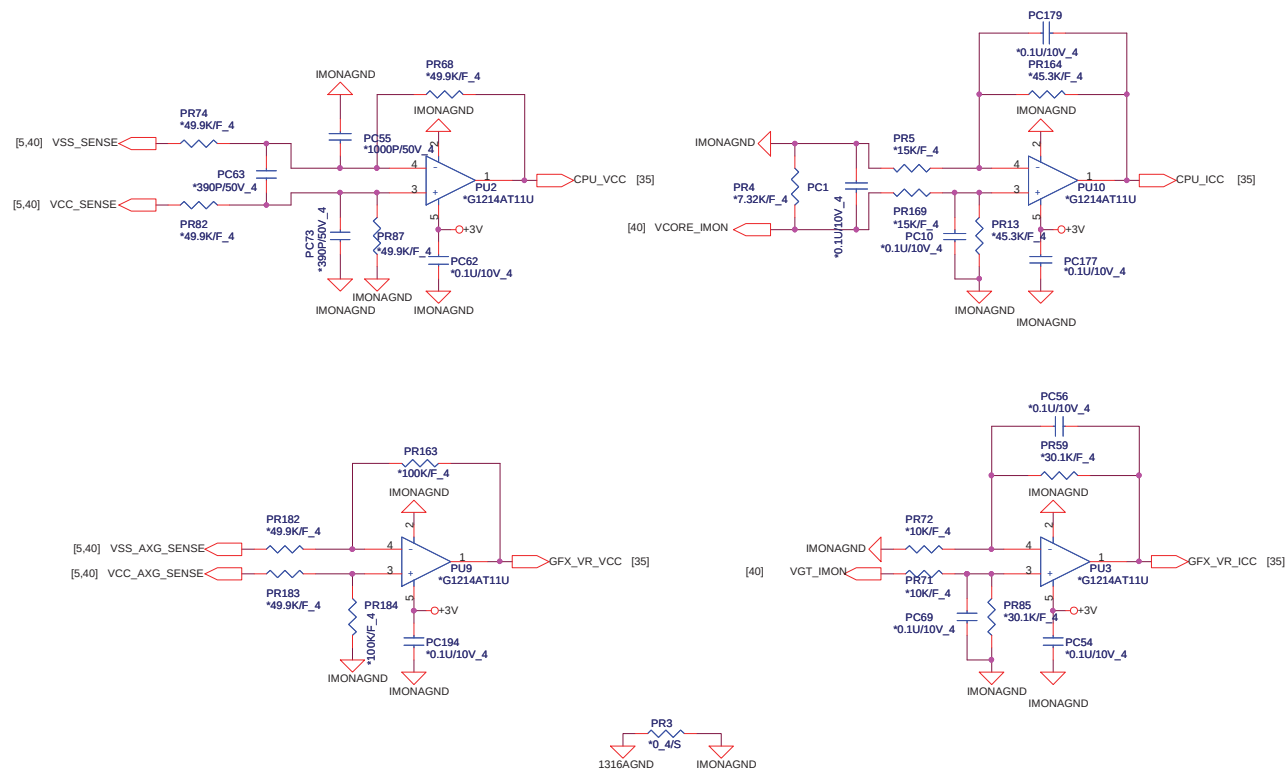


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**PROJECT : LX3/5(Huron River)
Quanta Computer Inc.**

Size	Document Number	Rev
Custom	Dis-charge IC (P2806)	1A
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Vender	Size	P/N
EON	128KB	AKE37ZN0Q01 (EN25F40-100HIP)
Winbond	128KB	AKE35FN0N00 (W25X10BVSNIG)
	512KB	AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031

<http://hobi-elektronika.net>

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		Quanta Computer Inc.	
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