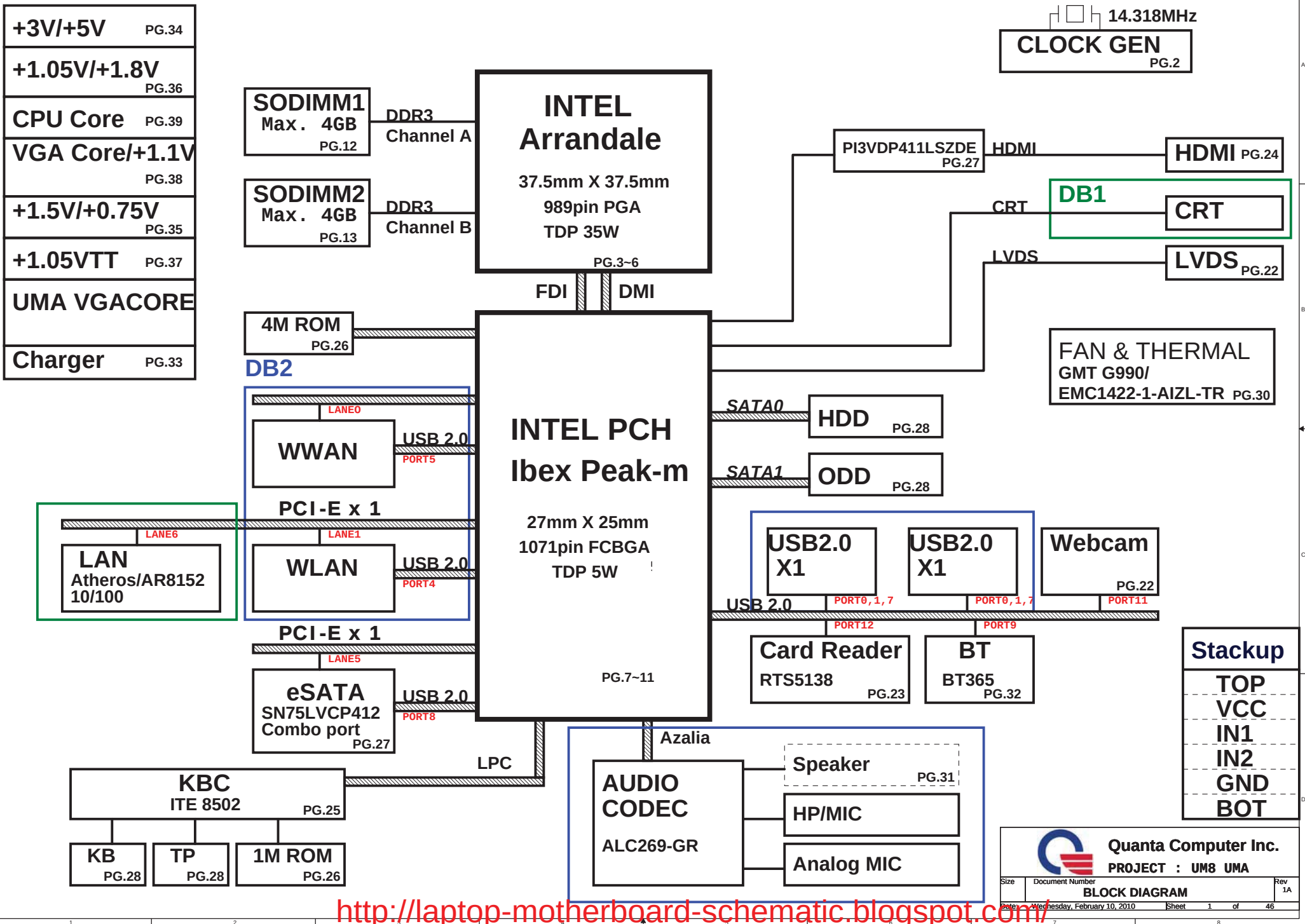
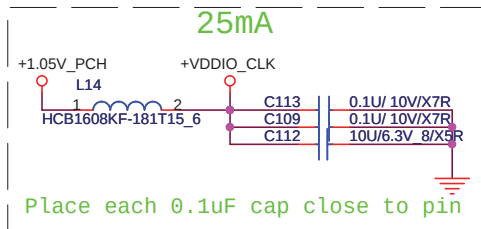
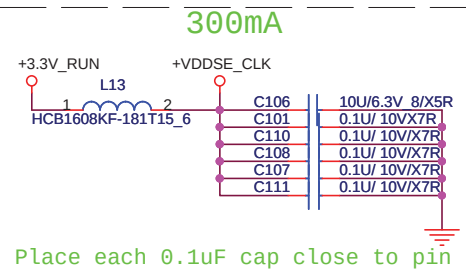


UM8 UMA SYSTEM DIAGRAM



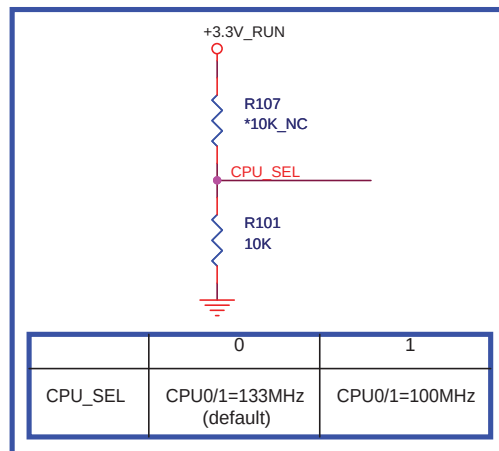
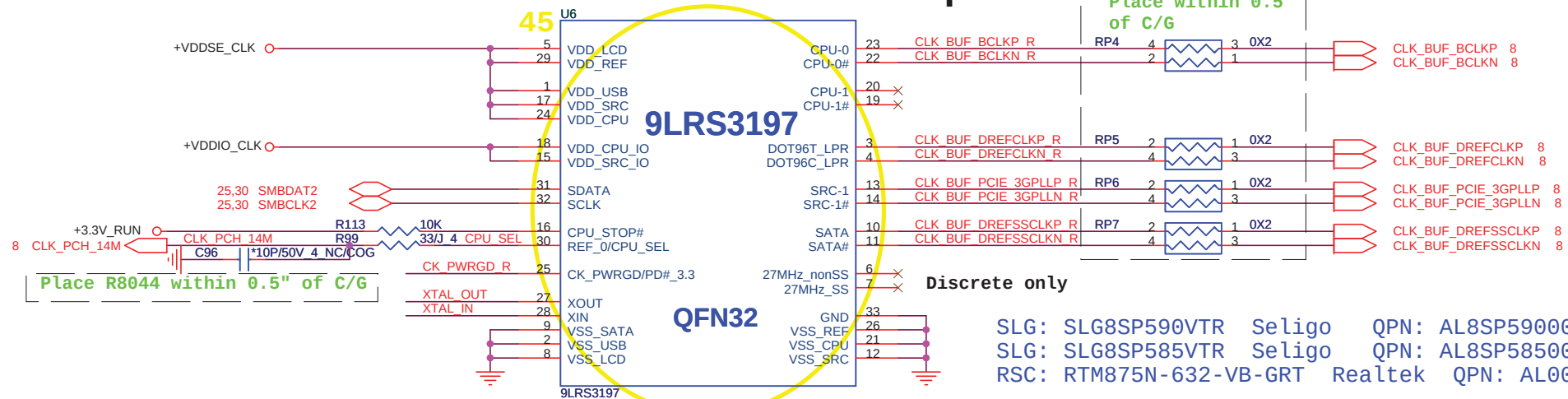


8/20 Wait Victor check

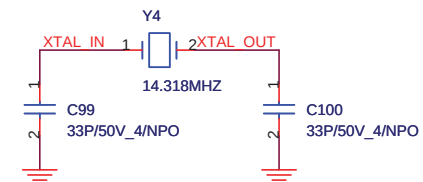
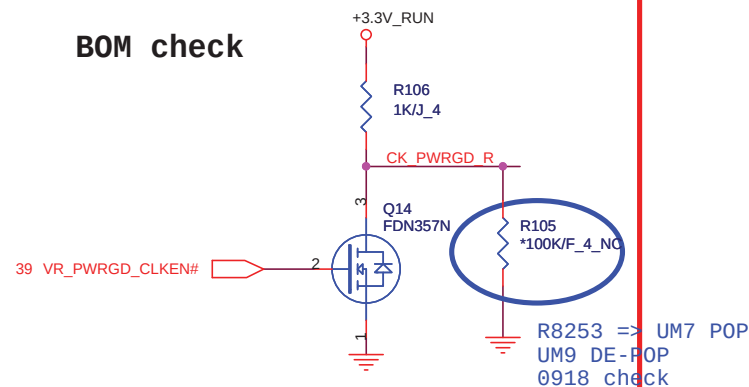


PDC (Power Cap quantities follow UM3)

Check CLK P/N and footprint

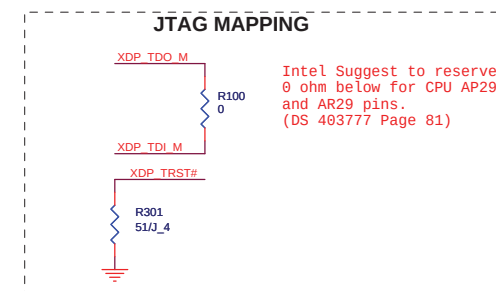
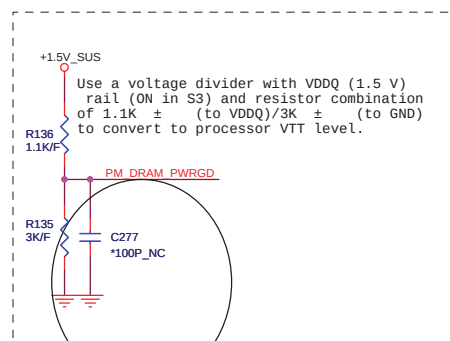
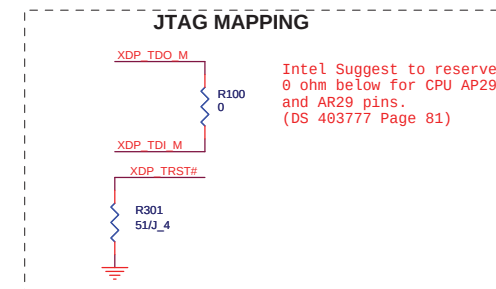


BOM check

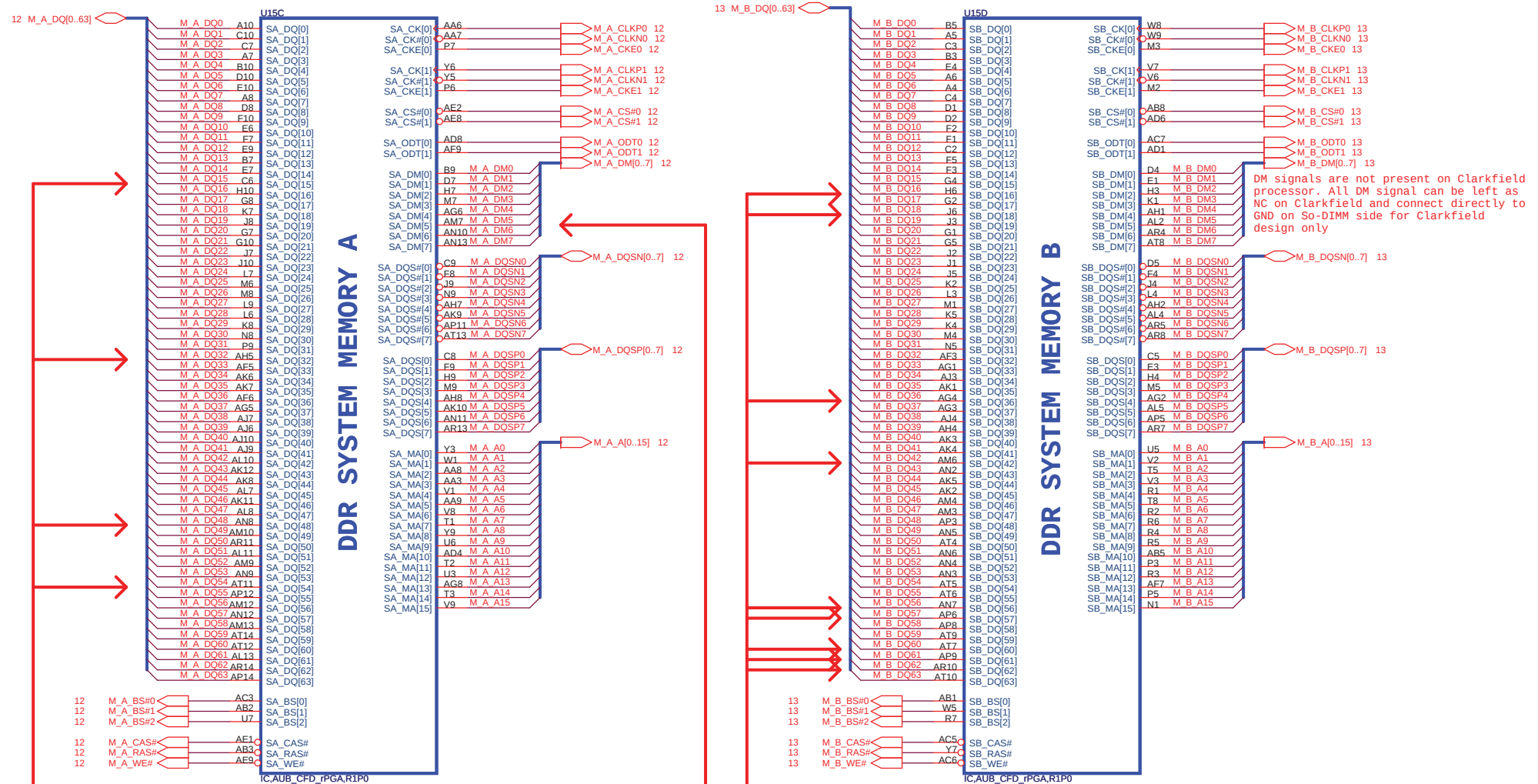


Quanta Computer Inc.
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AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

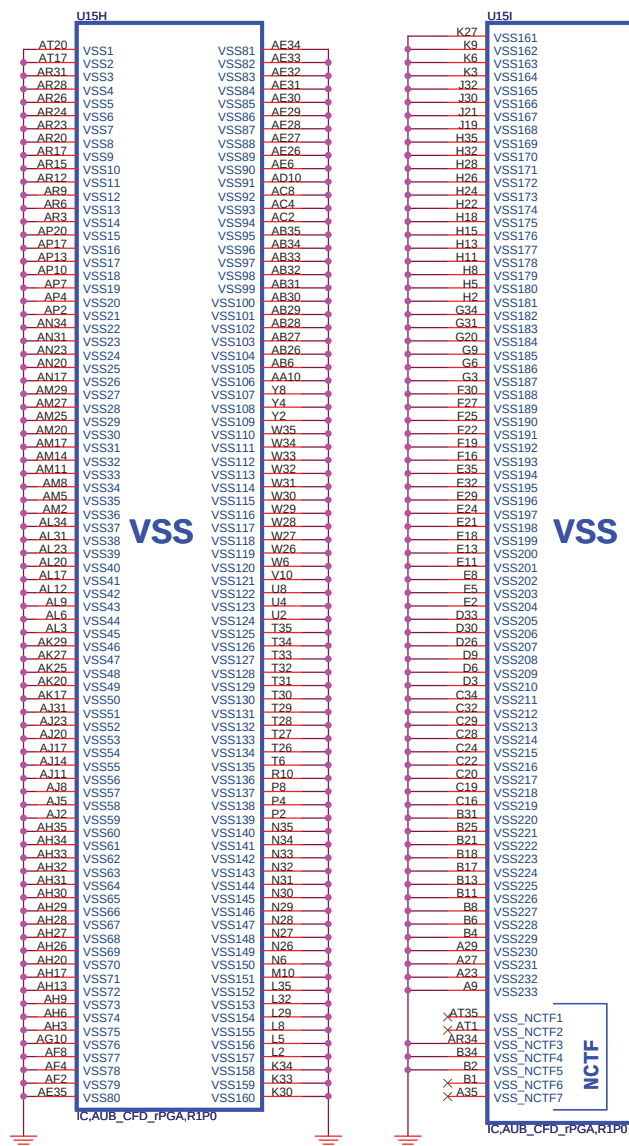


0525 Steg : As an option, VTT_SENSE pin on the processor can be left floating. But the platform needs to have the FB (feedback) pin of the VR tied to the VTT plane regulation.

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

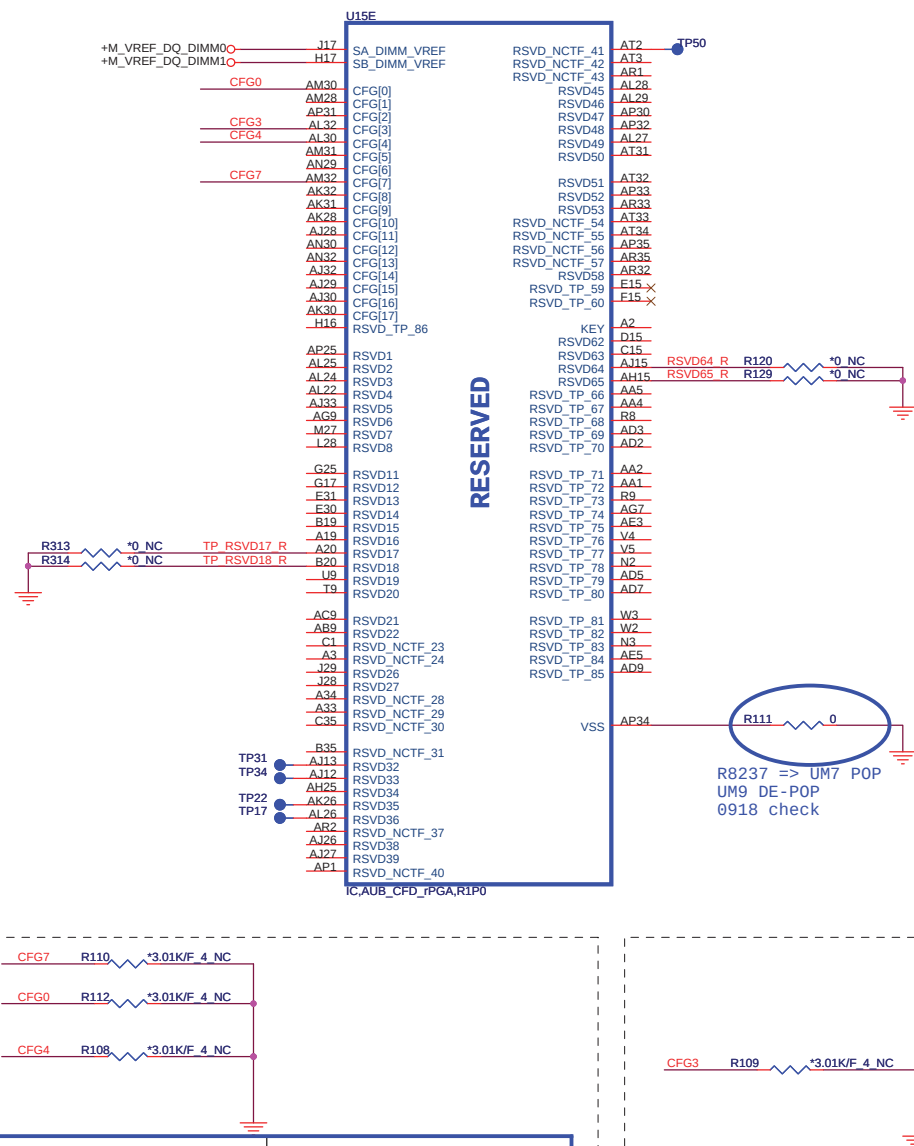
AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

06



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

<http://laptop-motherboard-schematic.blogspot.com/>

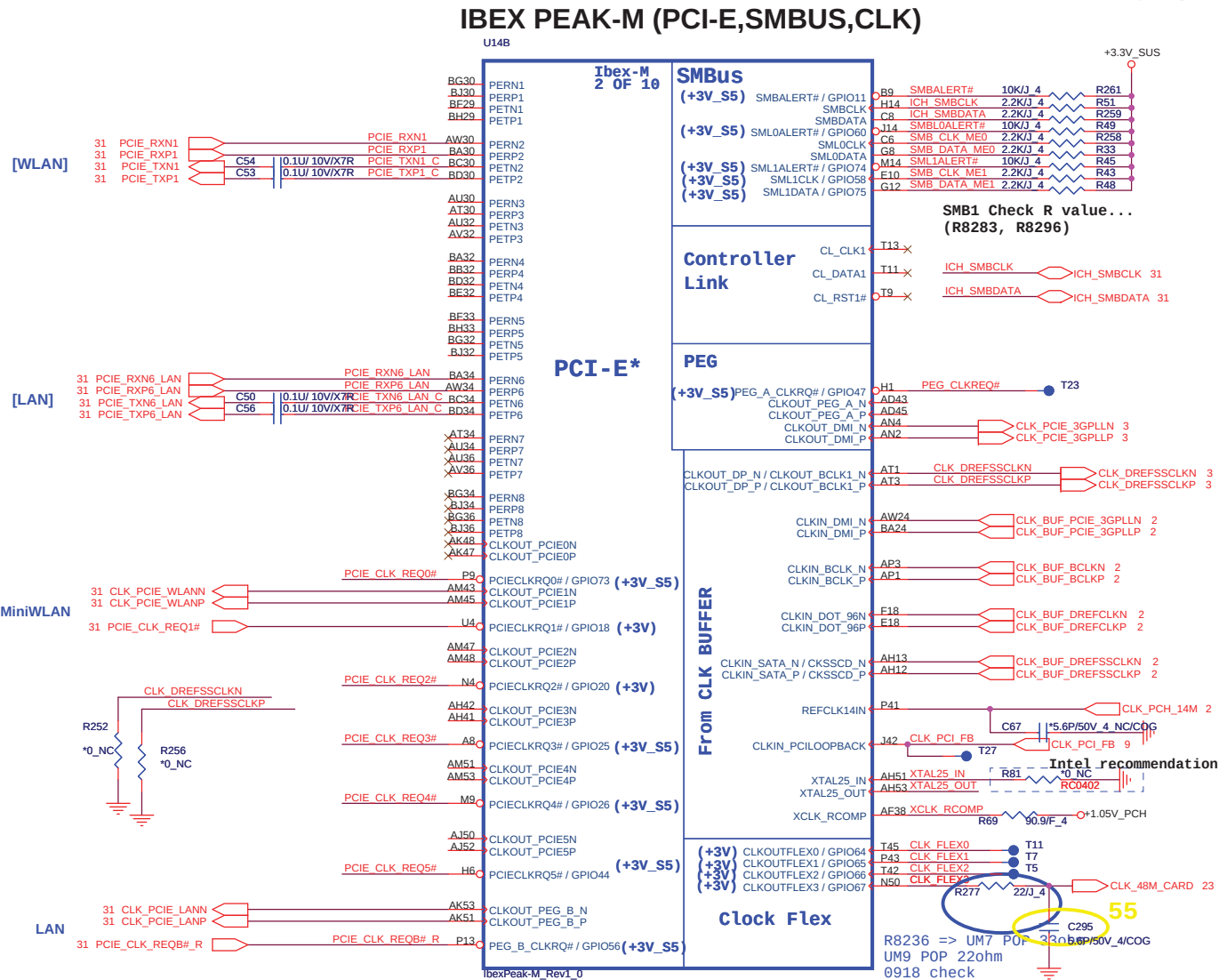
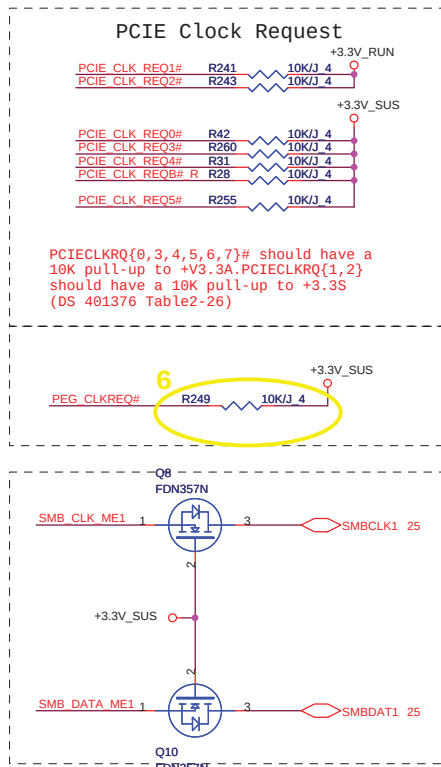
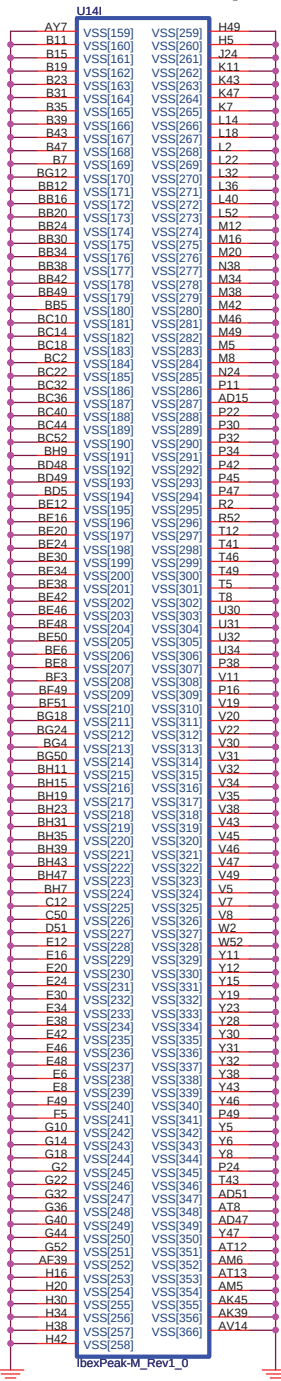


	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

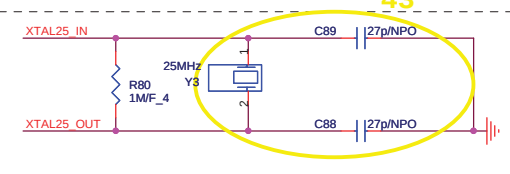
IBEX PEAK-M (HDA,JTAG,SATA)



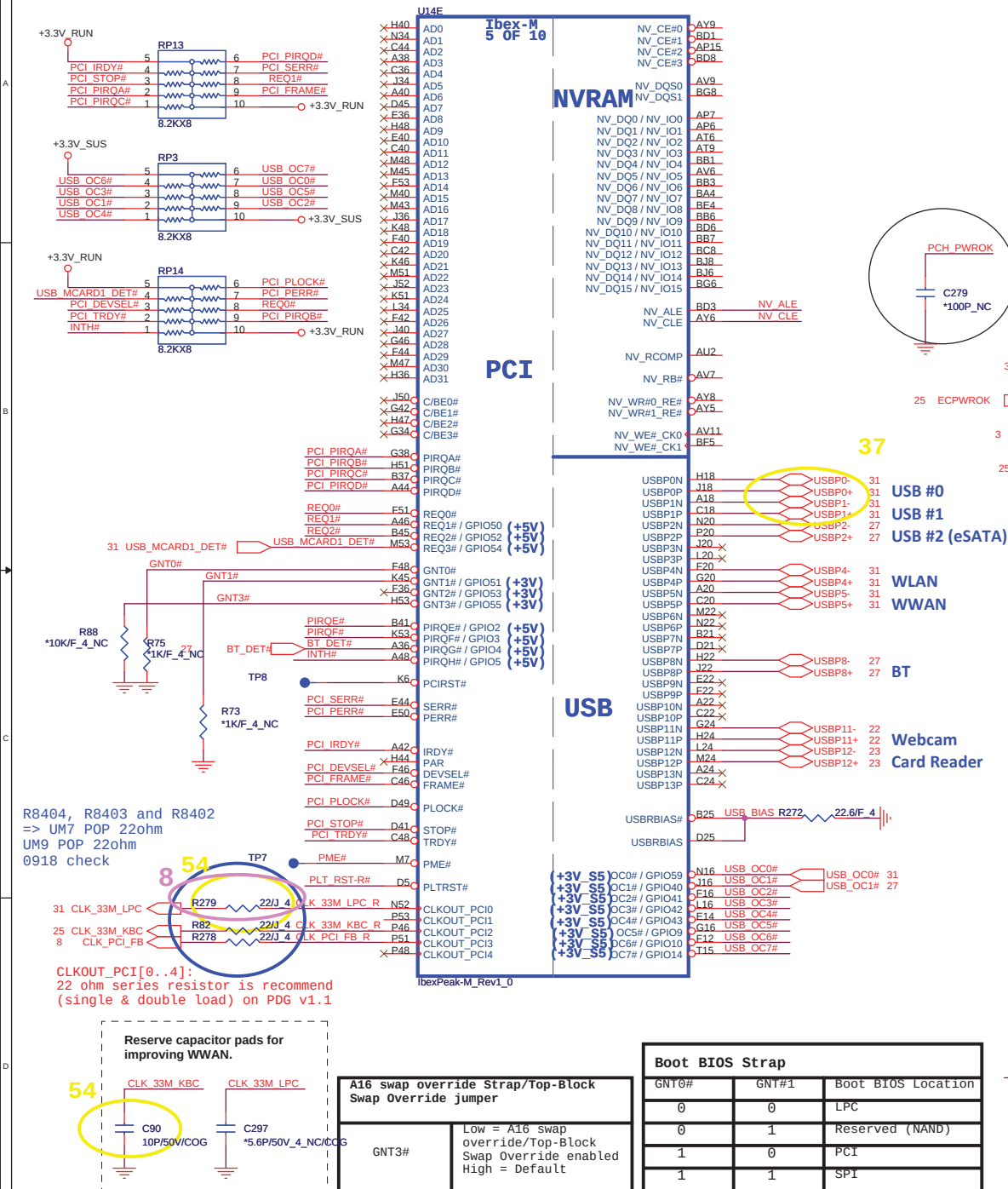
IBEX PEAK-M (GND)



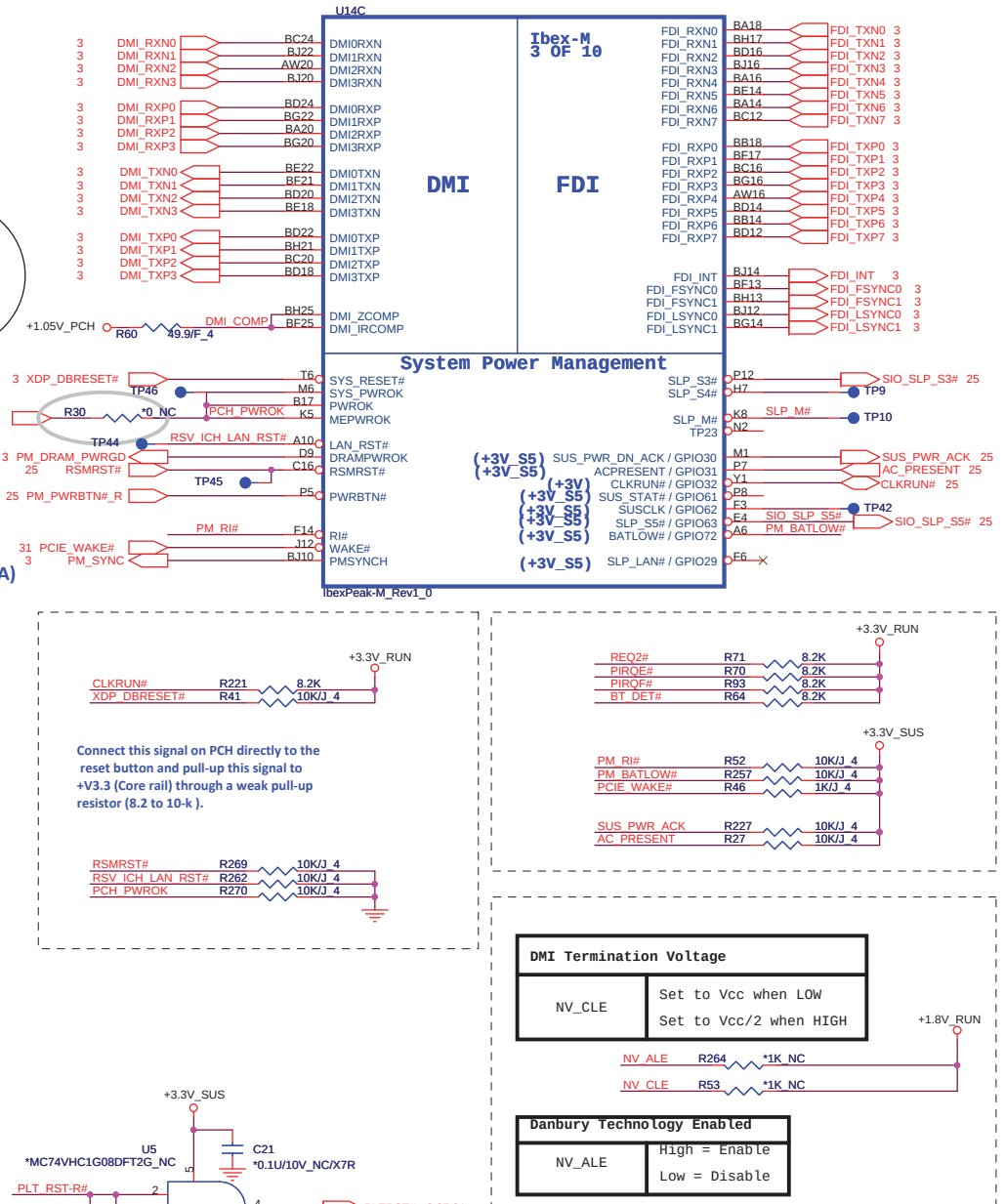
UMA	POP Y8201, C8411, C8412 and R8401, de-POP R89 for Internal GFX
DIS	de-POP Y8201, C8411, C8412 and R8401, POP R89 for Internal GFX



IBEX PEAK-M (PCI,USB,NVRAM)

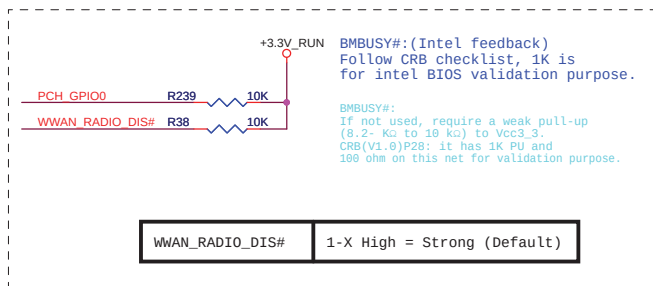
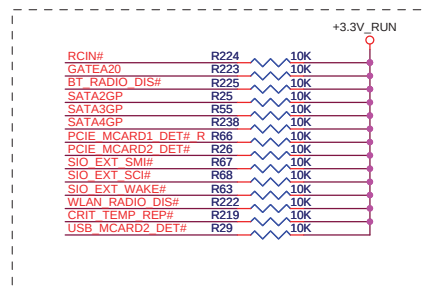
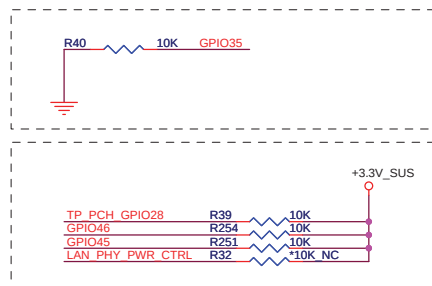
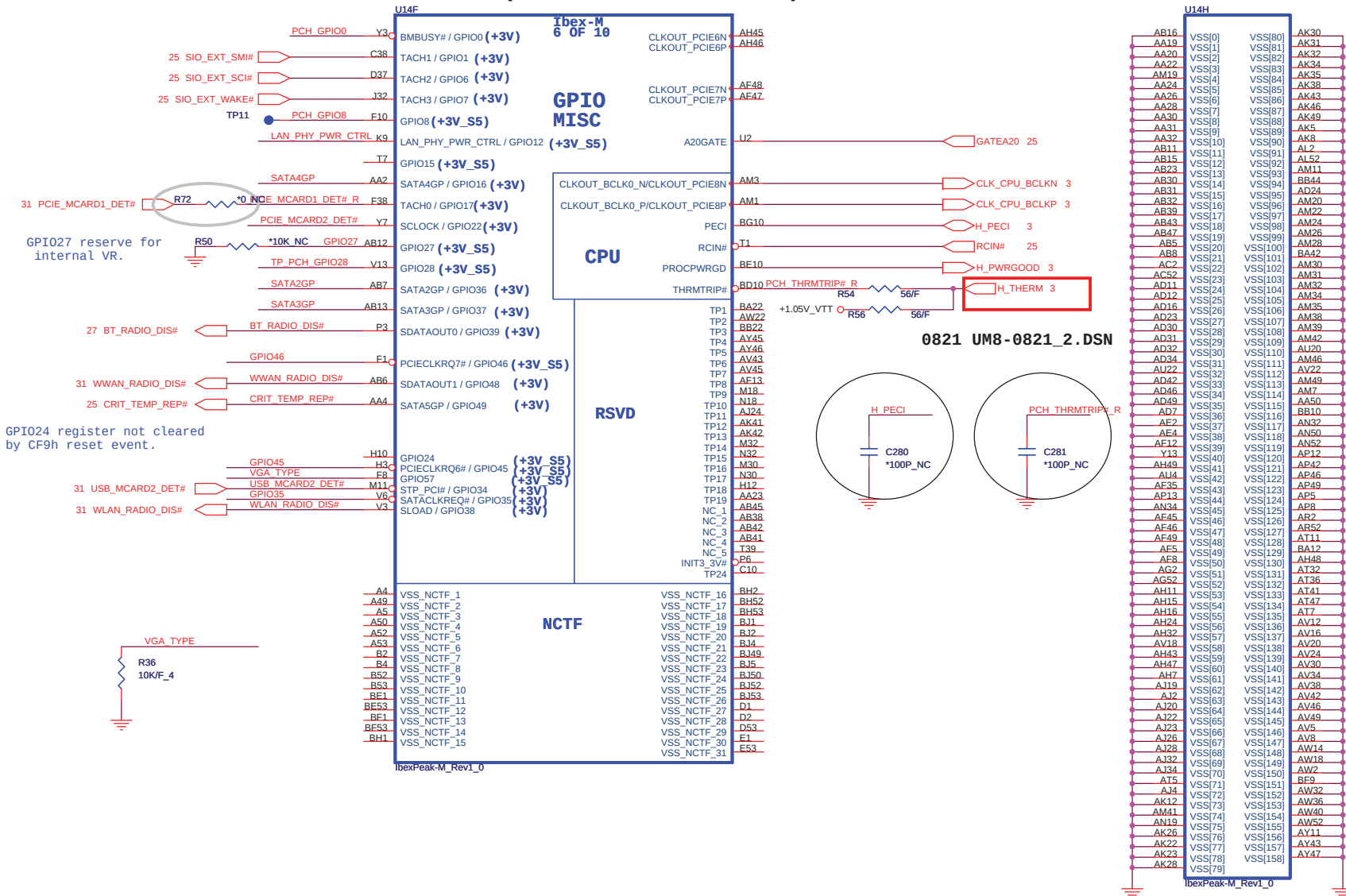


IBEX PEAK-M (DMI,FDI,GPIO)



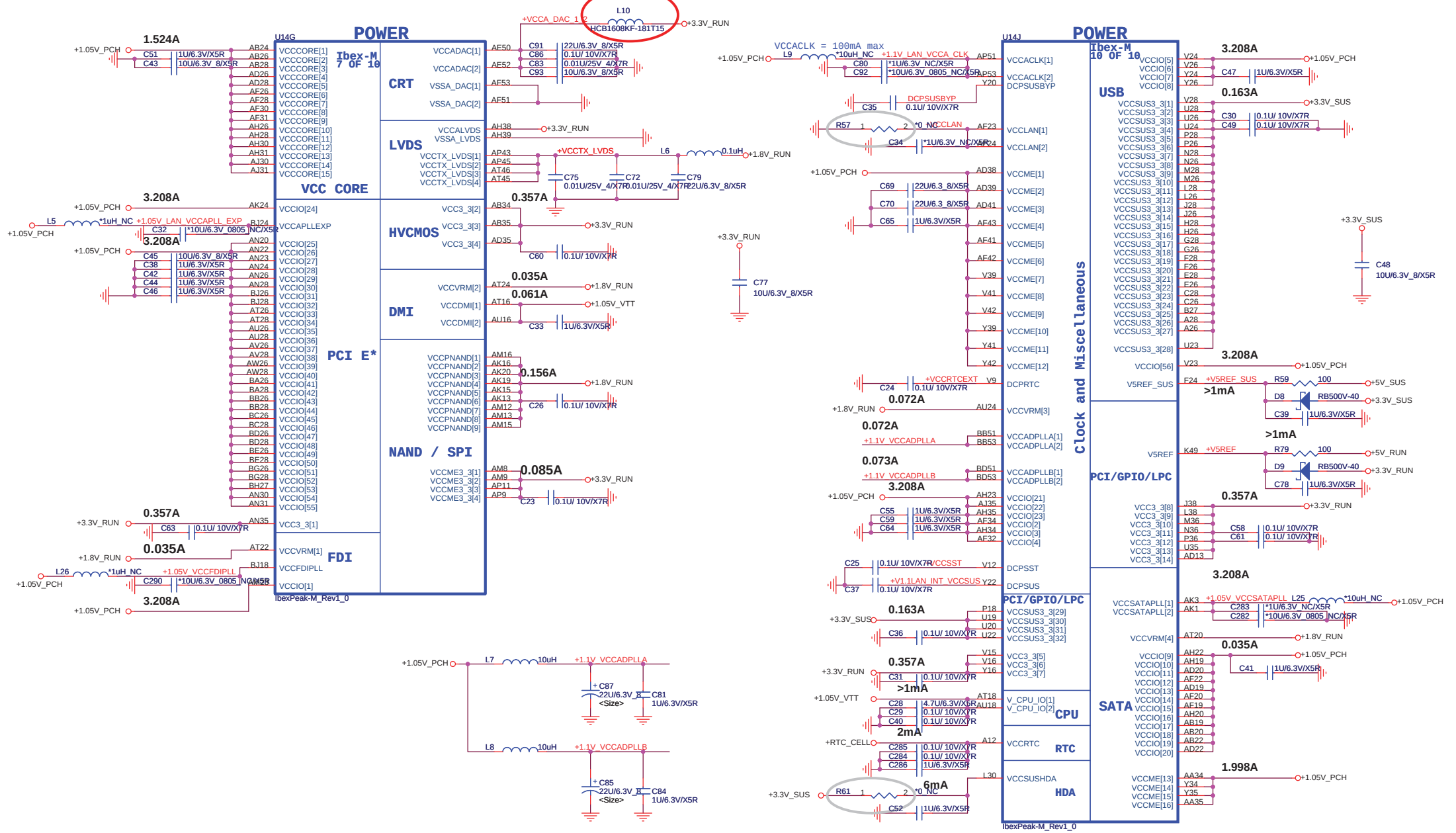
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

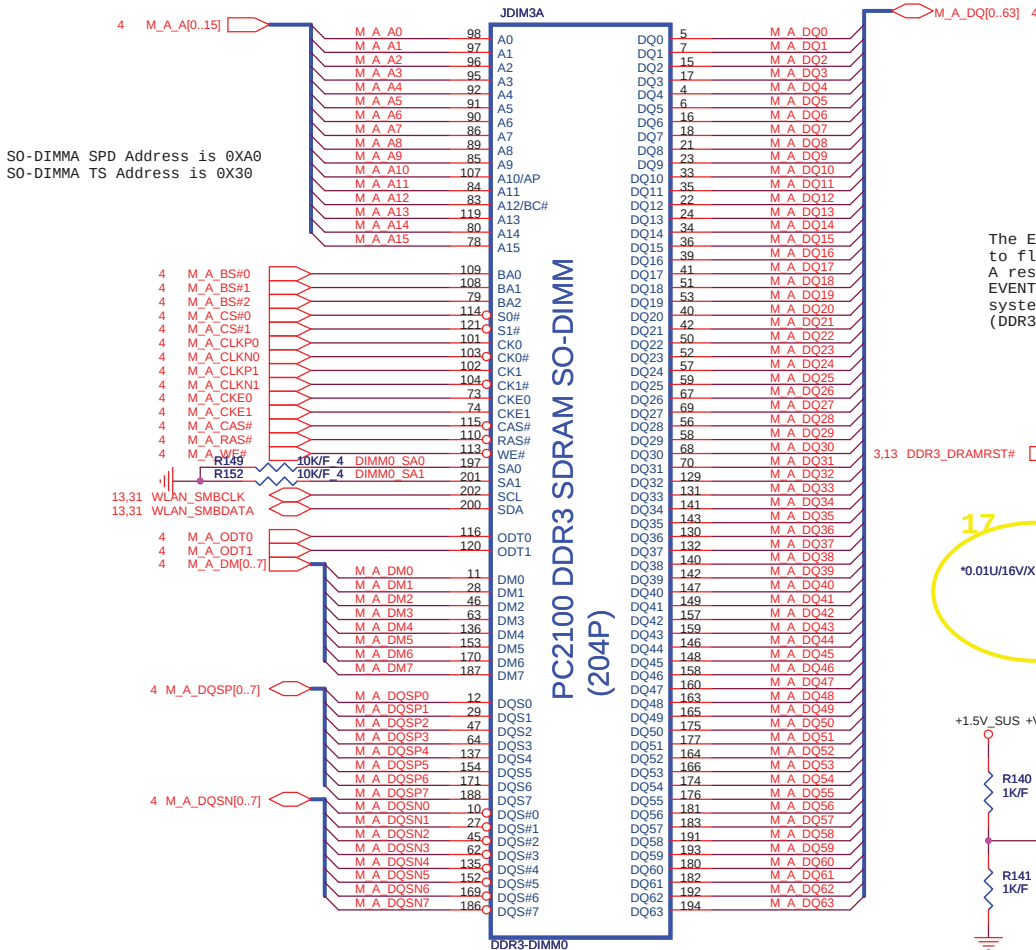


Cap quantities follow UM3

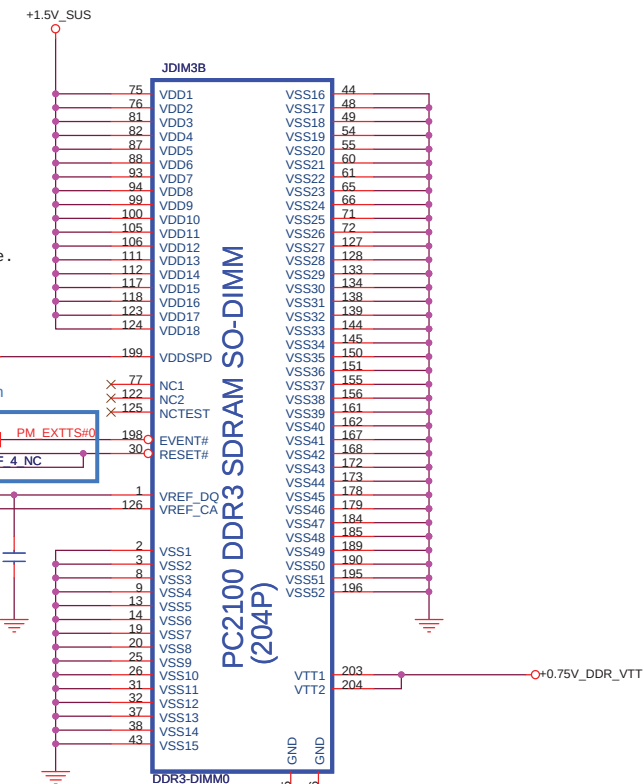
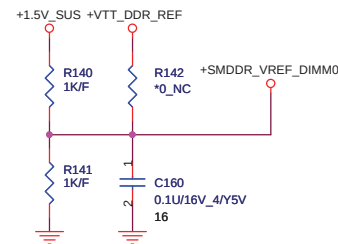
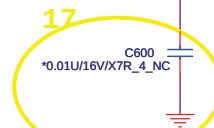
need check to change to 470 ohm



```
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30
```



The EVENT# pin is reserved for use to flag critical module temperature. A resistor may be connected from EVENT# bus line to Vddspd on the system planer to act as a pullup. (DDR3 DS REV0.5)

3,13 DDR3_DRAMRST# ☐

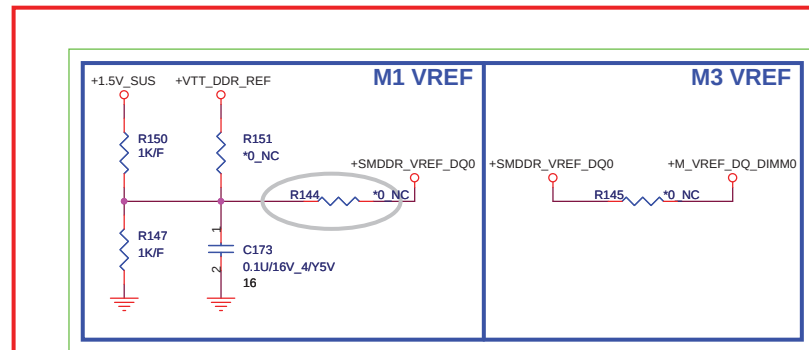
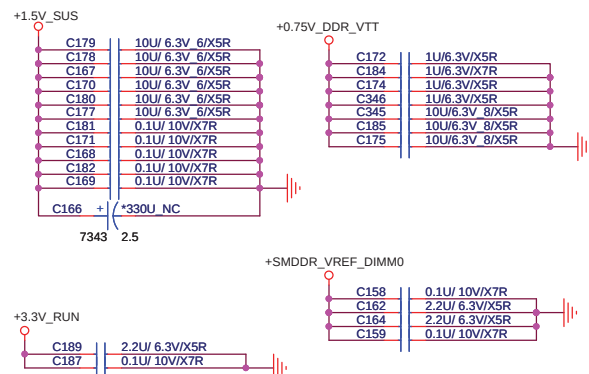
M2 VREF

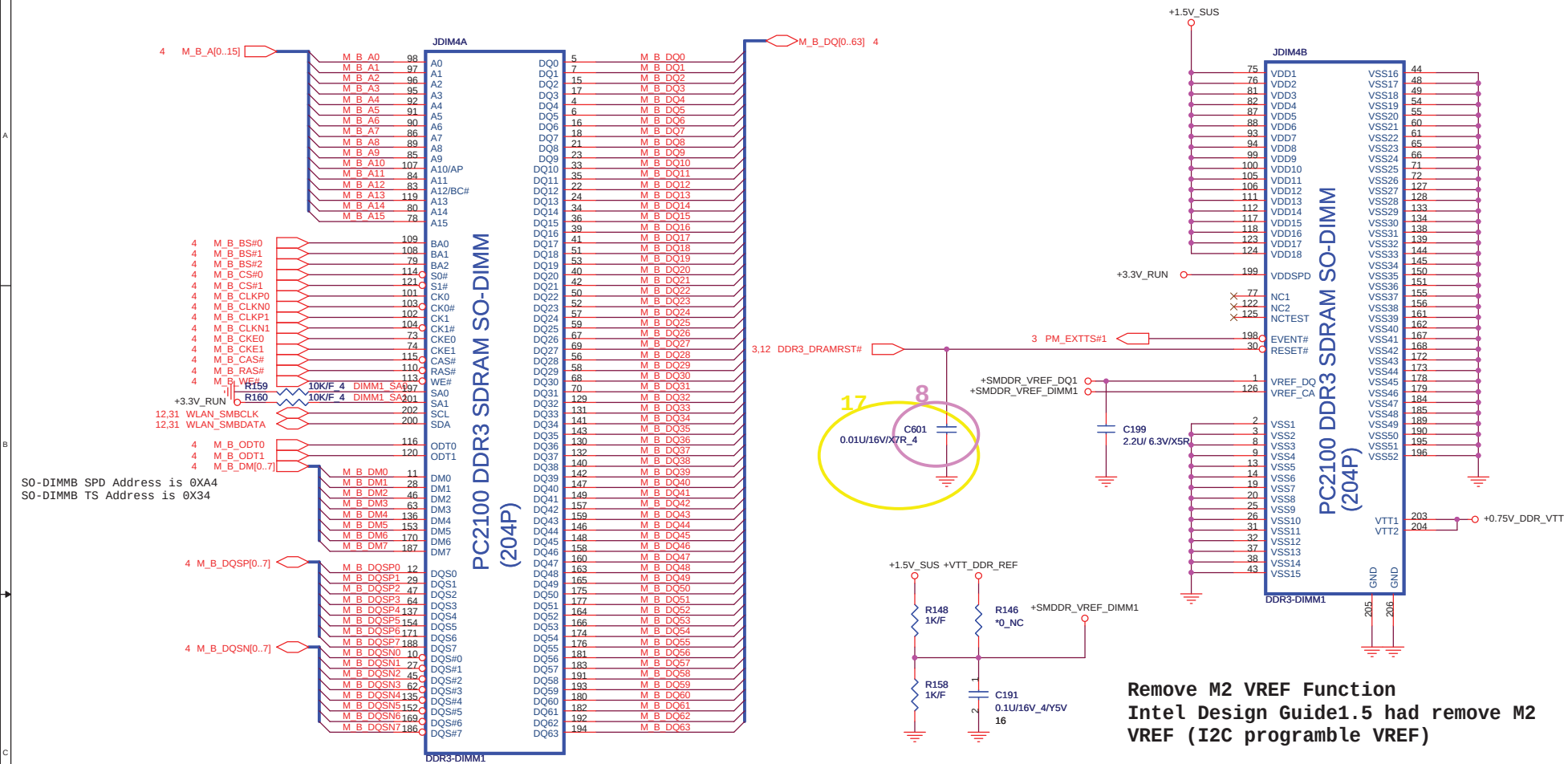
Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

Place these Caps near So-Dimm0.

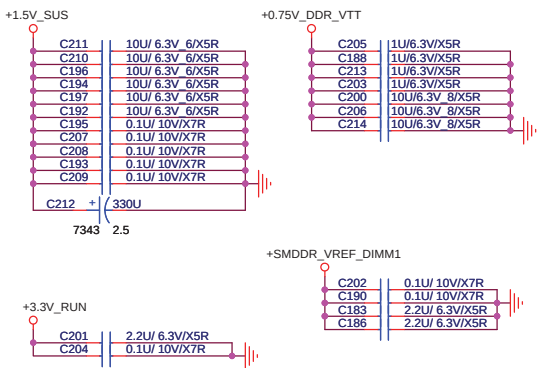
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%





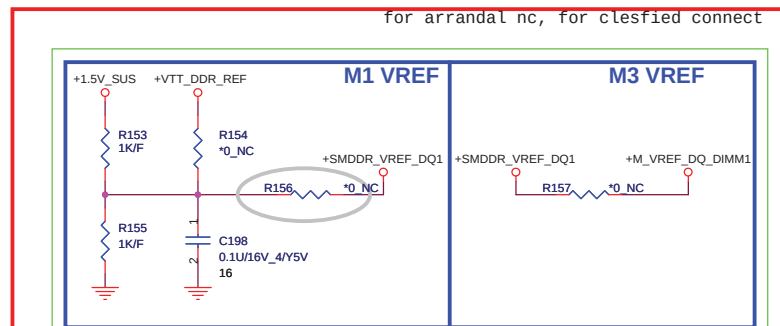
Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



Wait Victor check

for arrandal nc, for clesfied connect



Quanta Computer Inc.
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	DDR3 DIMM-1	1A
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<http://laptop-motherboard-schematic.blogspot.com/>

		Quanta Computer Inc.	
		PROJECT : UM8 UMA	
Size	Document Number		Rev
	Blank		1A
Date:	Wednesday, February 10, 2010	Sheet	14 of 46



<http://laptop-motherboard-schematic.blogspot.com/>

		Quanta Computer Inc.	
		PROJECT : UM8 UMA	
Size	Document Number		Rev
	Blank		1A
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<http://laptop-motherboard-schematic.blogspot.com/>

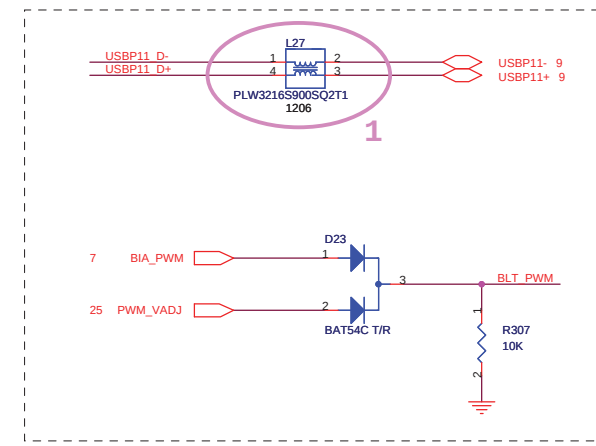
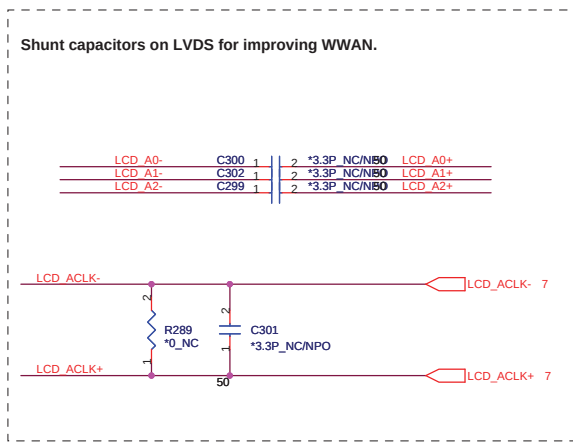
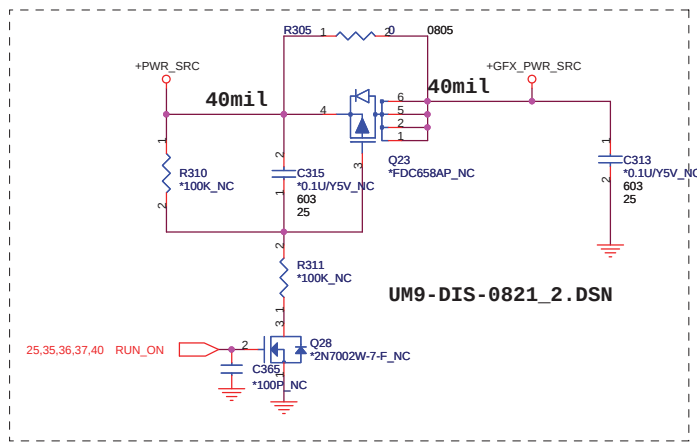
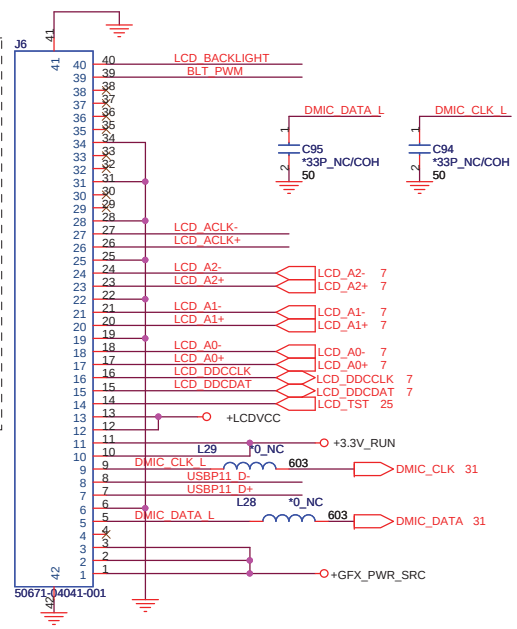
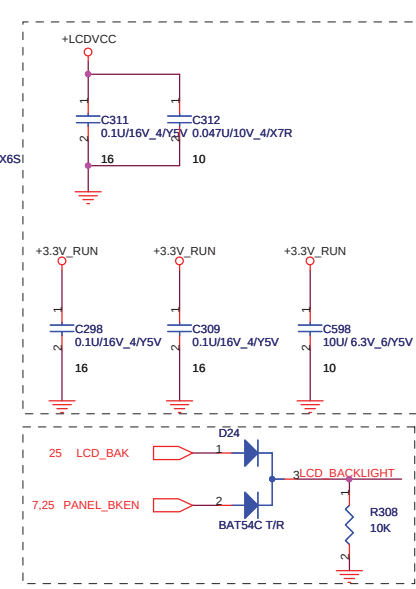
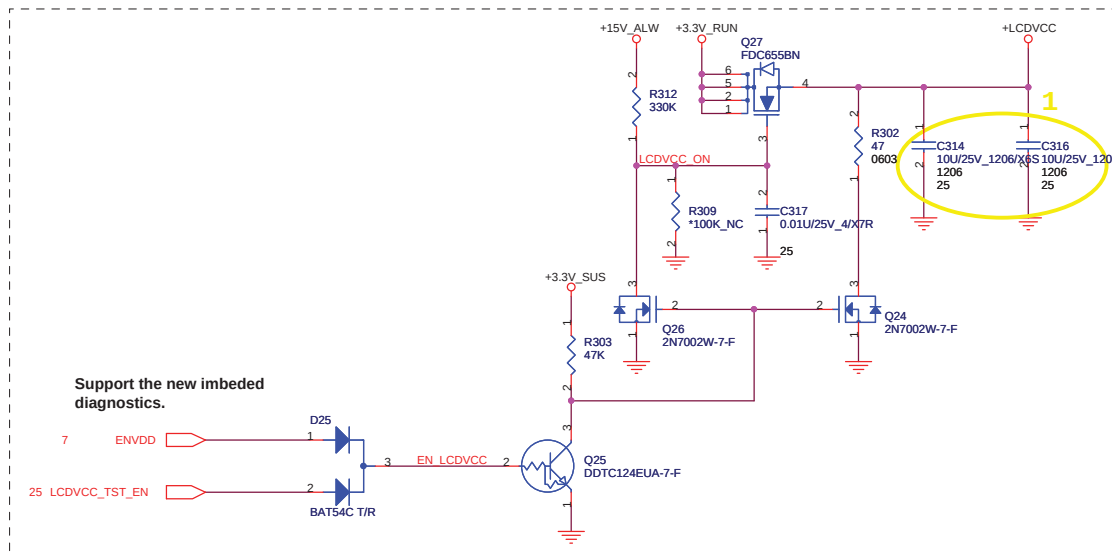


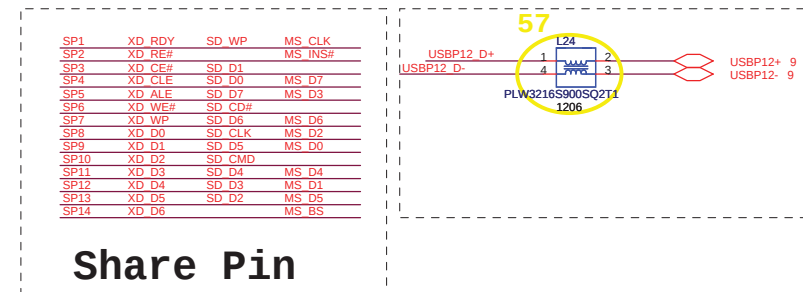
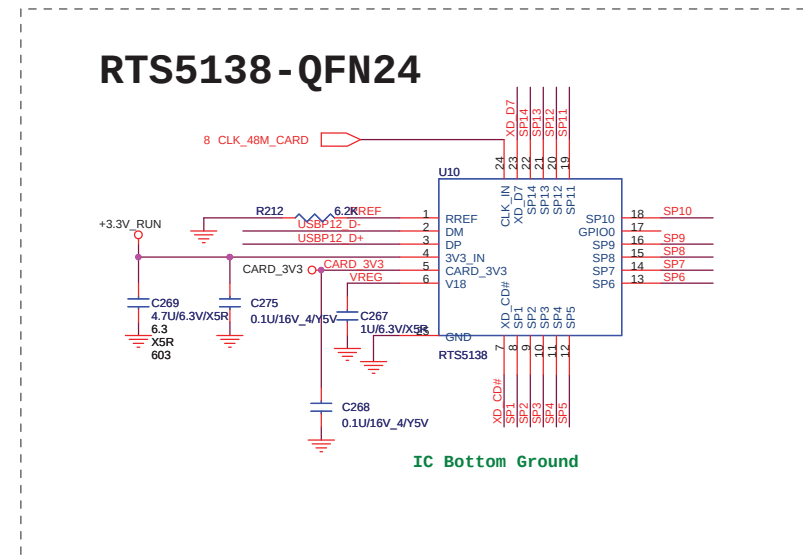
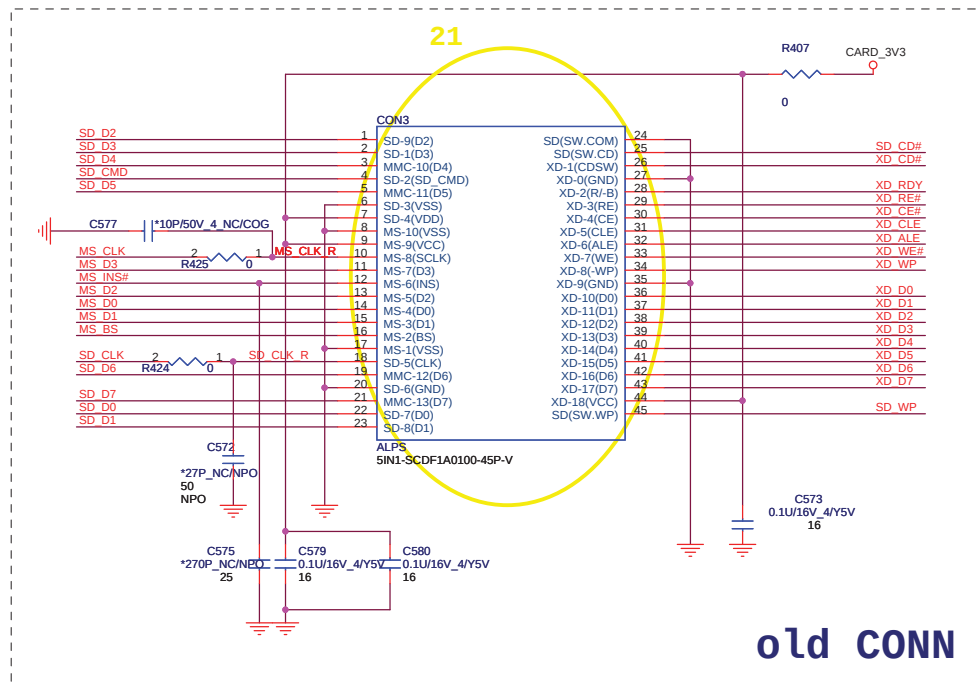




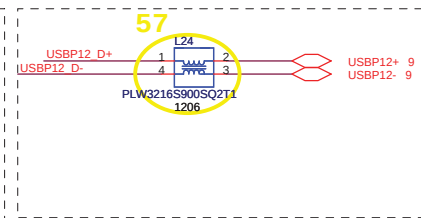
<http://laptop-motherboard-schematic.blogspot.com/>

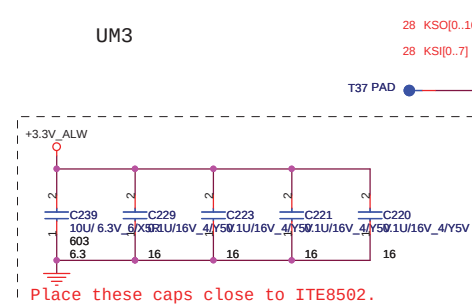
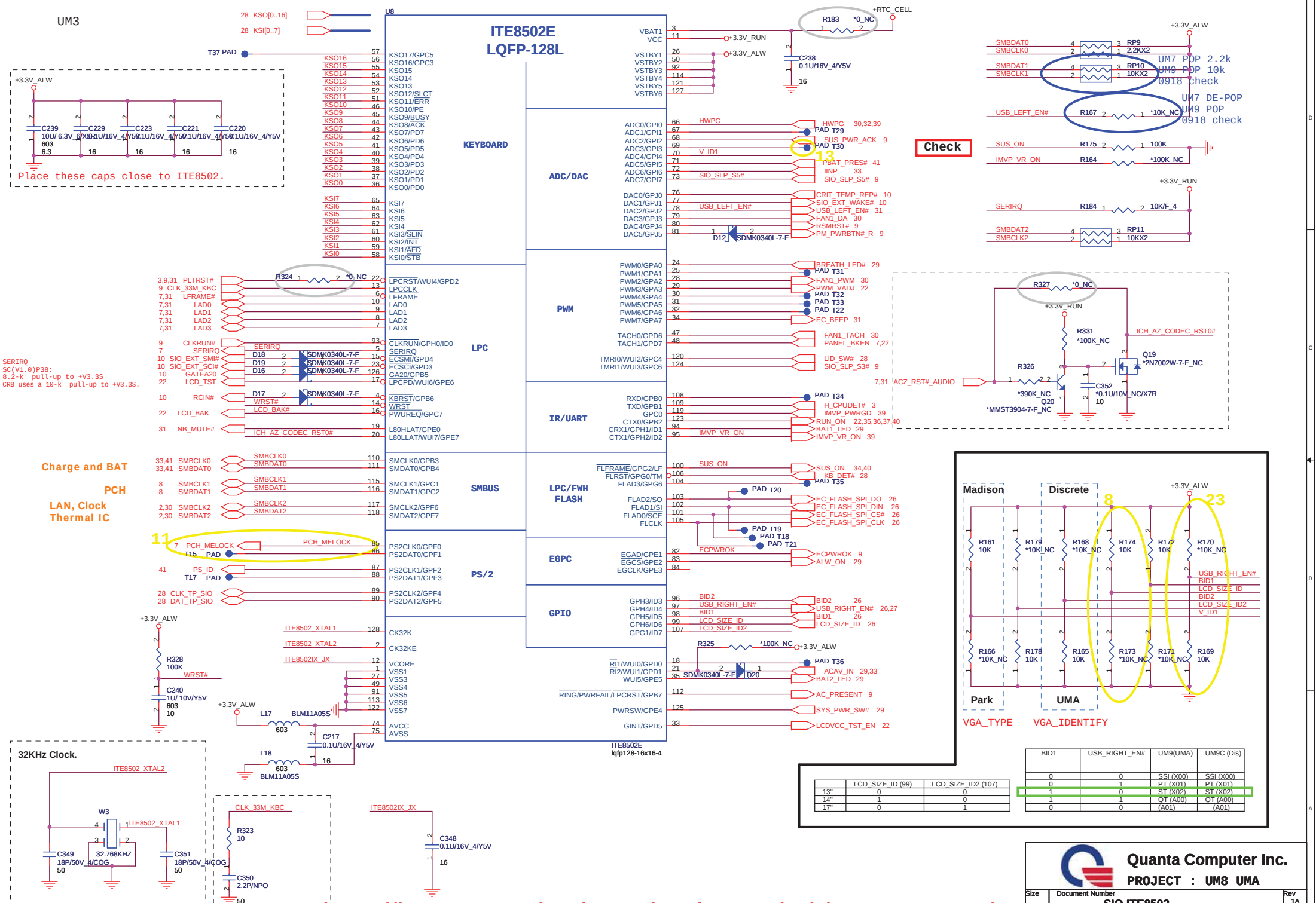
		Quanta Computer Inc.	
		PROJECT : UM8 UMA	
Size	Document Number		Rev
	Blank		1A
Date:	Wednesday, February 10, 2010	Sheet	21 of 46





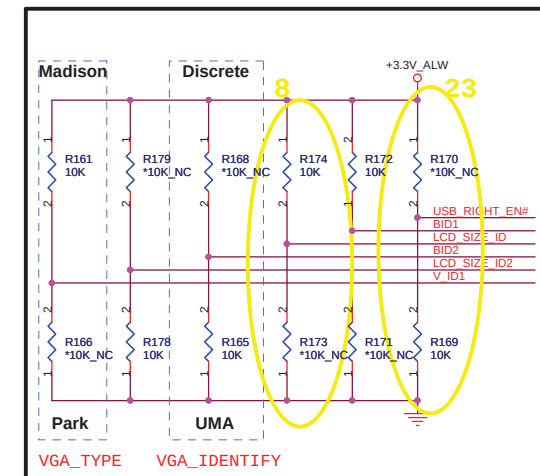
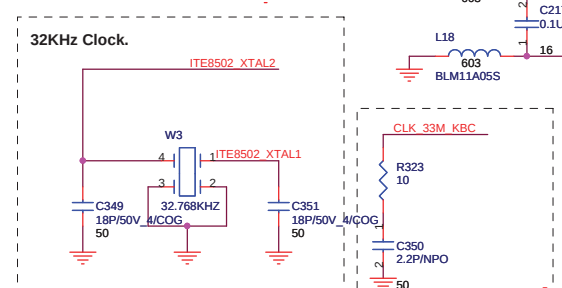
SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD INS#	MS INS#
SP3	XD CE#	SD D1	MS D7
SP4	XD CLE	SD D0	MS D3
SP5	XD ALE	SD D7	MS D3
SP6	XD WE#	SD CD#	MS D6
SP7	XD WP	SD D6	MS D6
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	MS D0
SP11	XD D3	SD D4	MS D4
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	MS D5
SP14	XD D6	MS BS	





SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

Charge and BAT
PCH
LAN, Clock
Thermal IC



	BID1	USB_RIGHT_EN#	UM9(UMA)	UM9C (Dis)
	0	0	SSI (X00)	SSI (X00)
	0	1	PT (X01)	PT (X01)
	1	0	ST (X02)	ST (X02)
	1	1	QT (A00)	QT (A00)
	0	0	(A01)	(A01)

	LCD_SIZE_ID(99)	LCD_SIZE_ID2(107)
13"	0	0
14"	1	0
17"	0	1

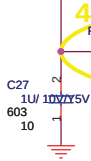
For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



MACRONIX: MX25L3205DM2I-12G QPN: AKE39FP0Z00
WINBOND: W25X32VSSIG QPN: AKE39ZP0N00

RTC BATTERY



Check P/N & Footprint

需加COIN BATTERY 料號IN BOM
need modify the location of this portions

13



For PCH

32Mbit (4M Byte)

MACRONIX: MX25L8005M2C-15G QPN: AKE5GFK0Z09
WINBOND: W25X80AVSSIG QPN: AKE39ZP0N00



close to PCH

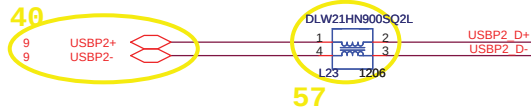
20

Close to U

For HSPI Function

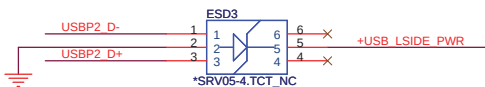
eSATA and USB To DB

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



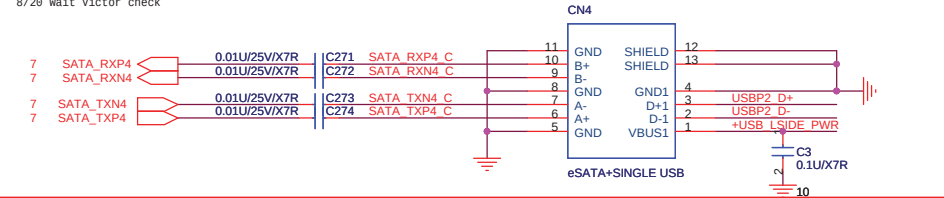
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



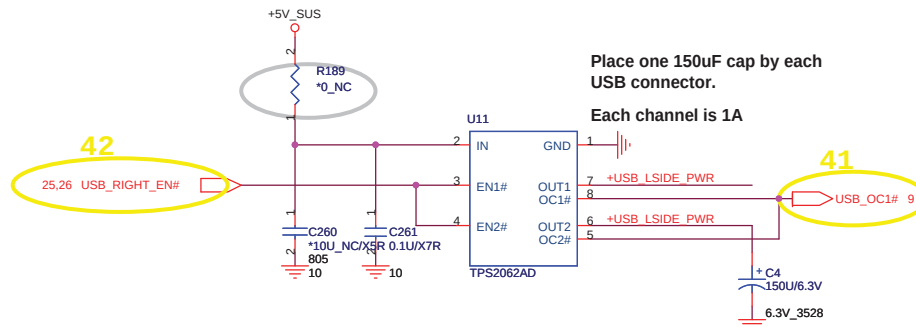
USB and eSATA Conn.

8/20 Wait Victor check

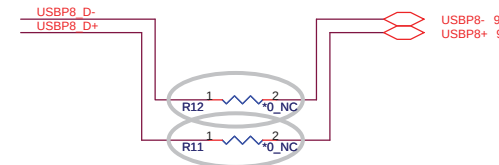
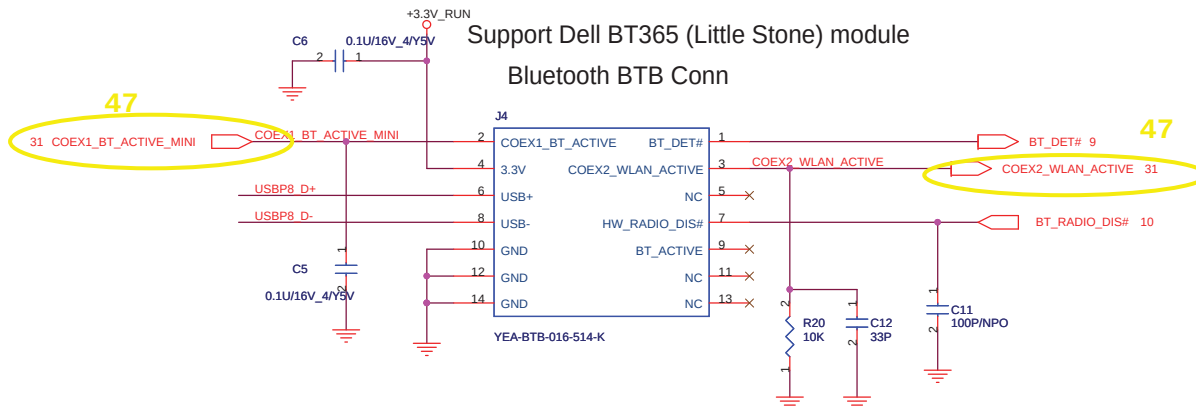


Place one 150uF cap by each USB connector.

Each channel is 1A

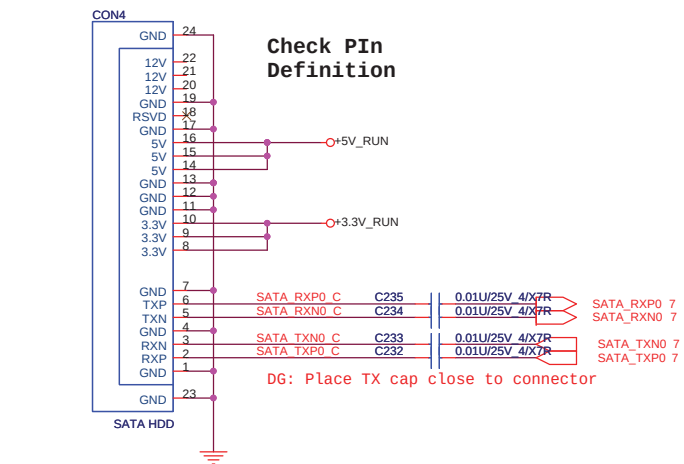


Support Dell BT365 (Little Stone) module Bluetooth BTB Conn



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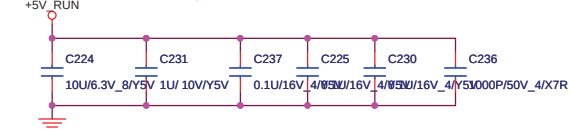
SATA Connector.



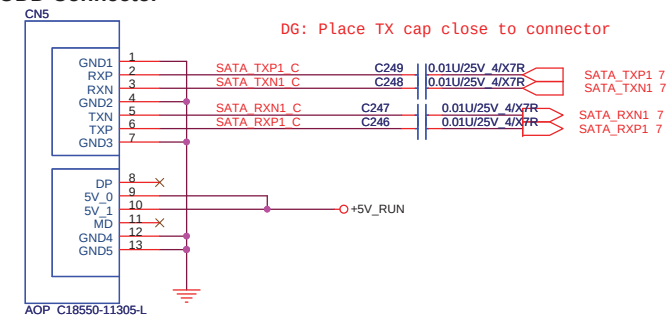
Place caps close to connector.



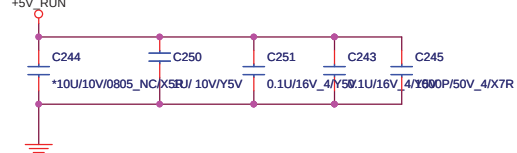
Place caps close to connector.



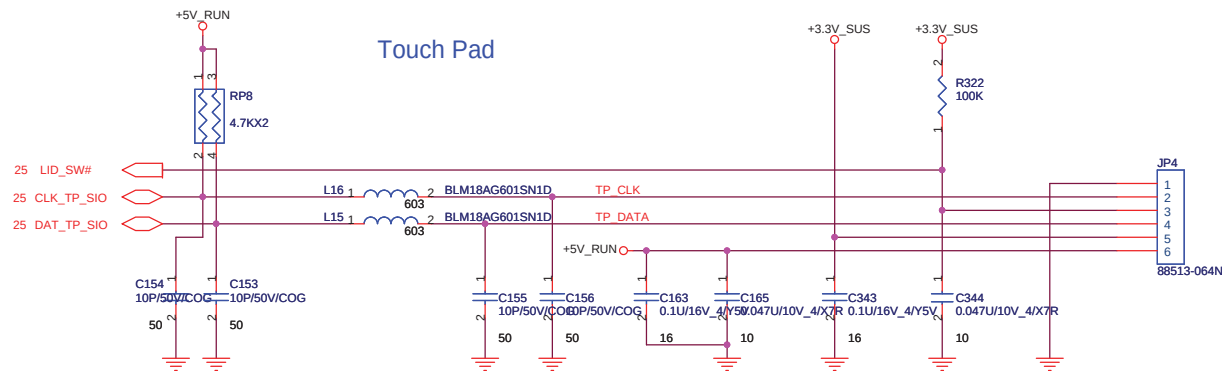
ODD Connector



Place caps close to connector.



Touch Pad

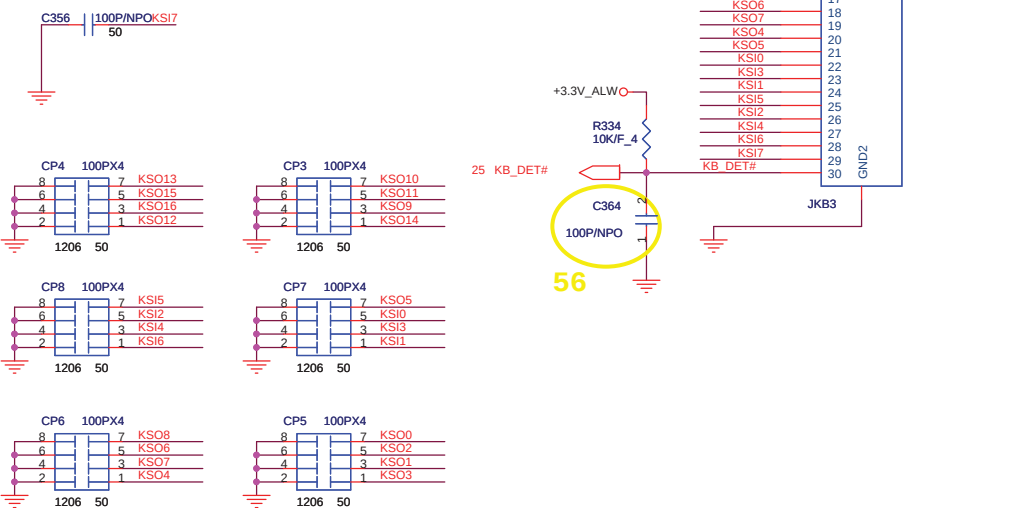


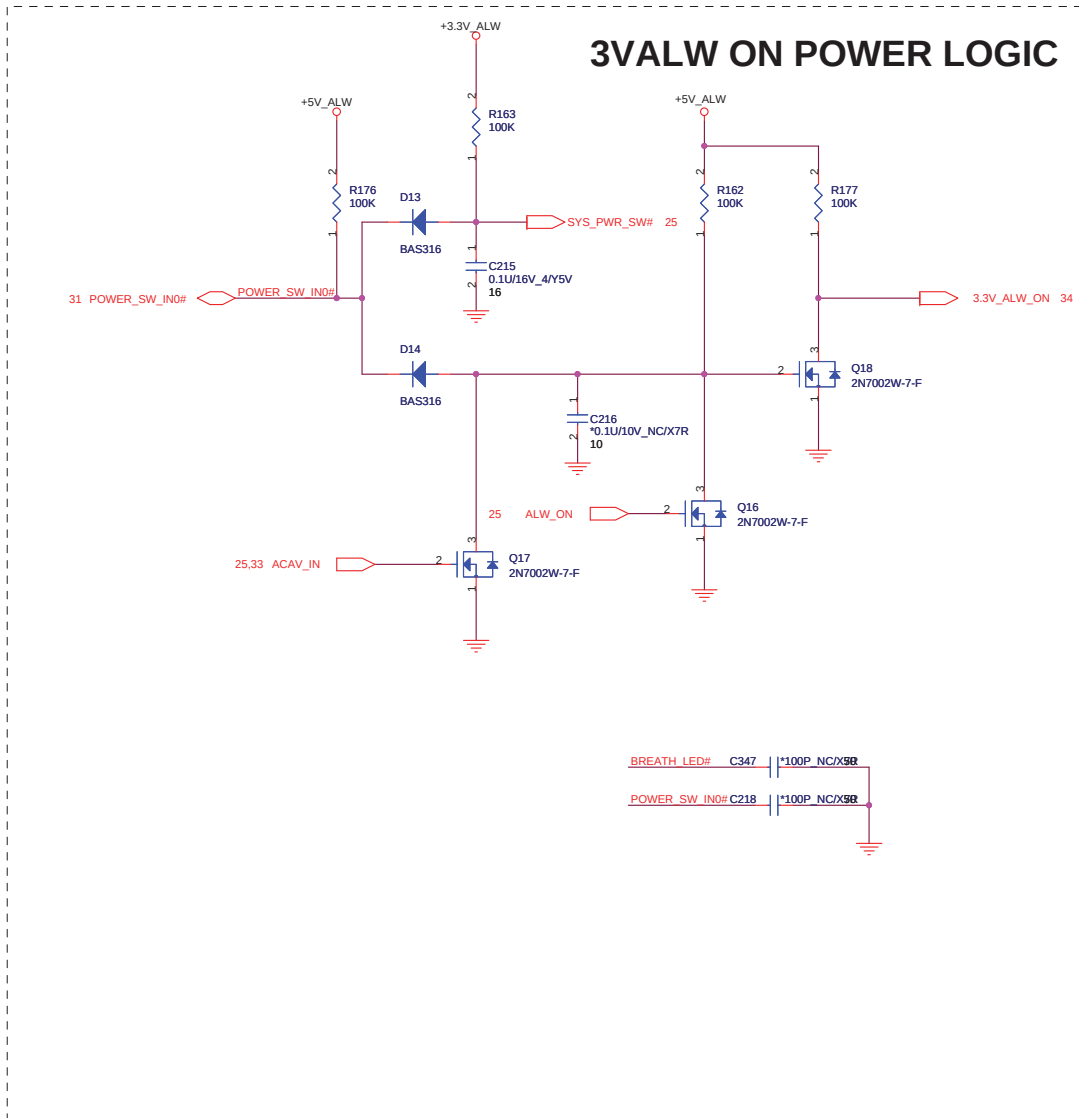
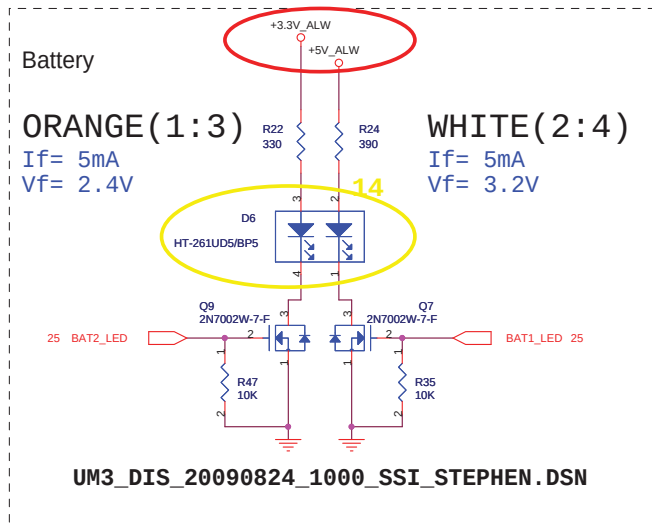
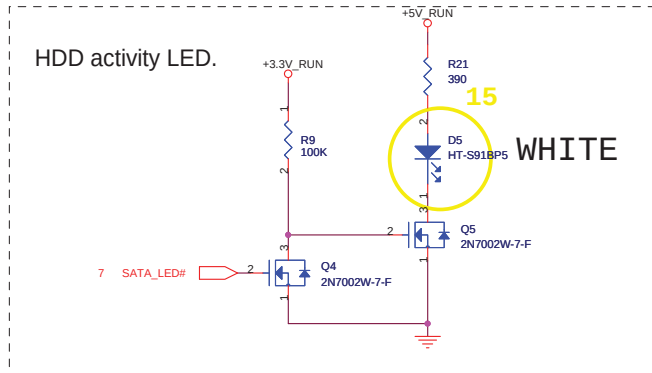
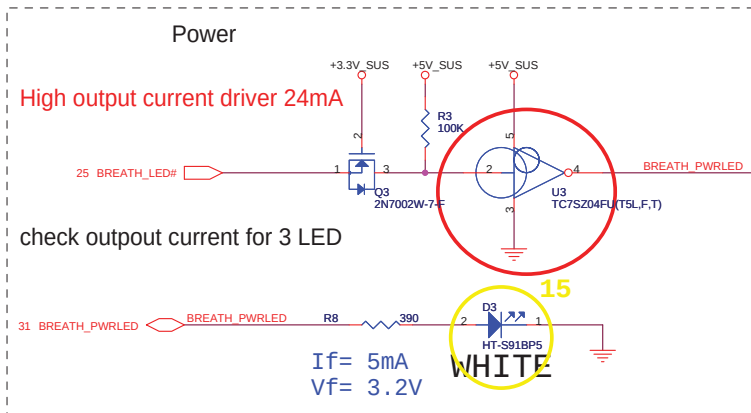
KEYBOARD CONNECTOR

Top side

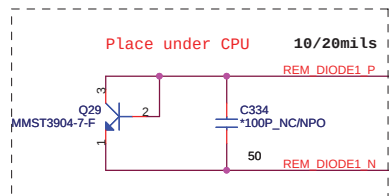
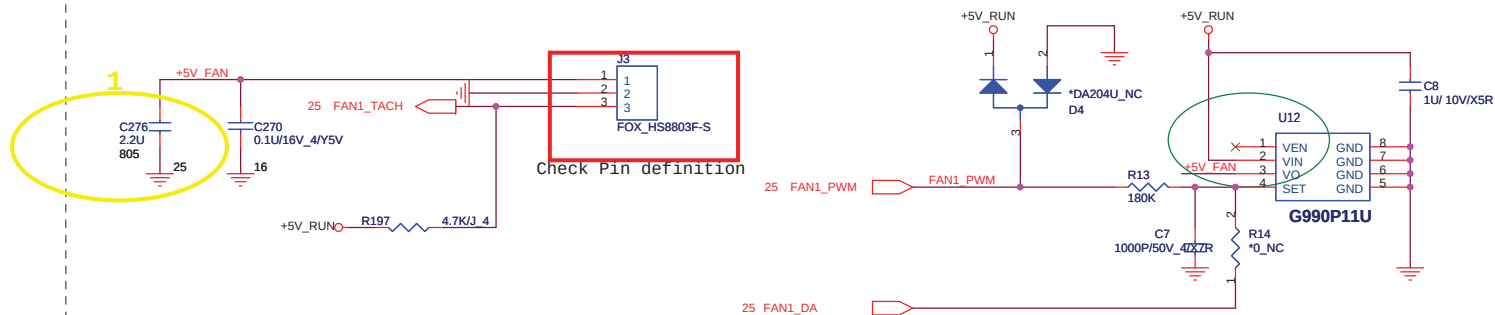
25 KSO[0..16]

25 KSI[0..7]



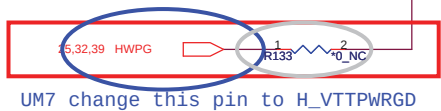
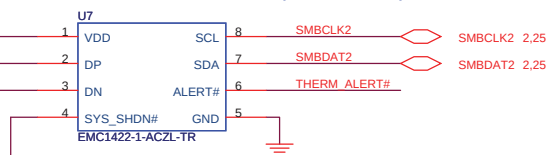


FAN CONTROL



1. Place C160 close to EMC1422
 2. Place C518 to be close to Q51
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy

ADM1032-1 => Hex 4C (1001 100) AL001032001
ADM1032-2 => Hex 4D (1001 101) AL001032002



Follow UM3 to change Q11
PIN2 gate control to avoid
abnormal shutdown?

UM7 change this pin to H_VTTPWRGD

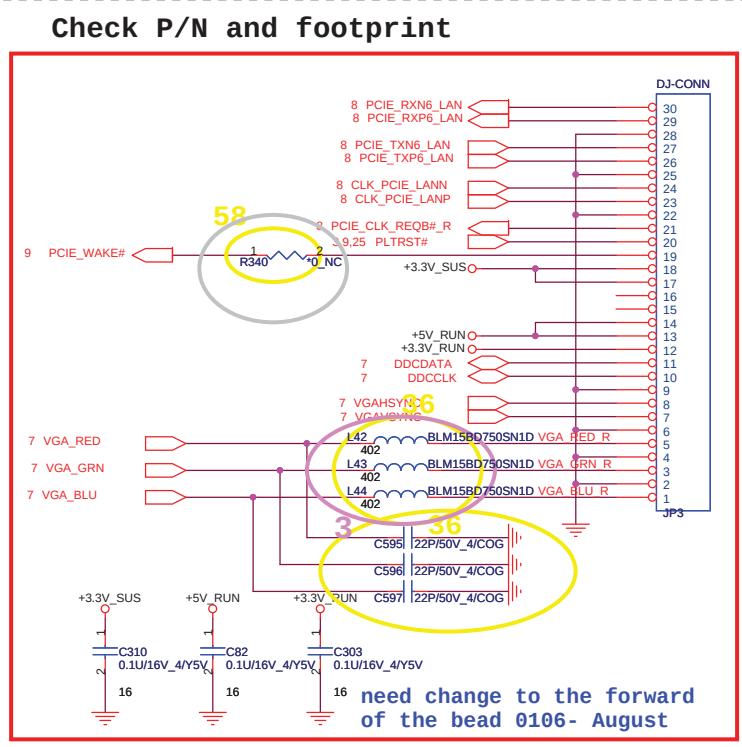
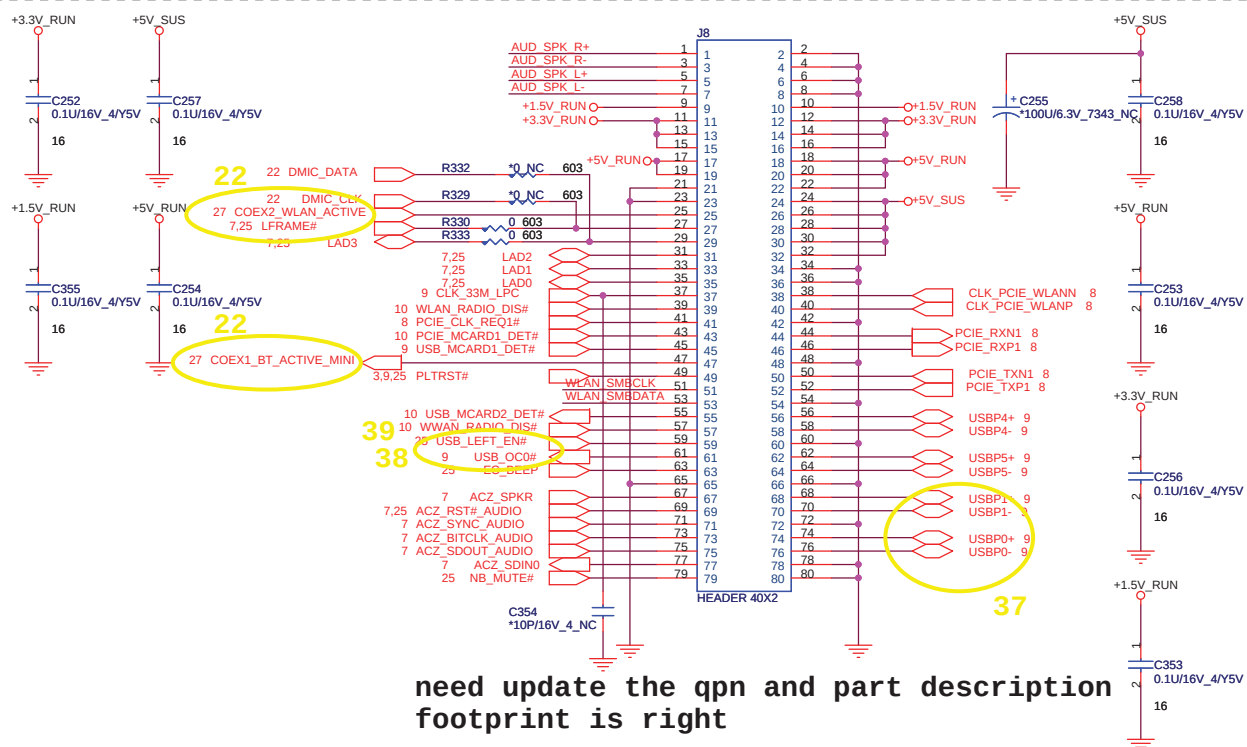
OTP 85 degree C



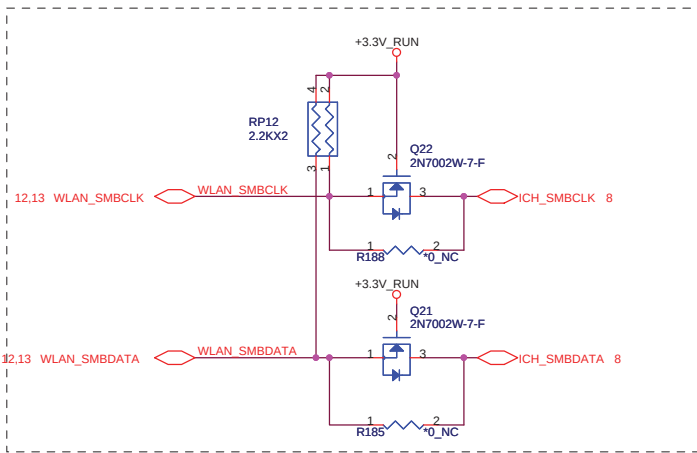
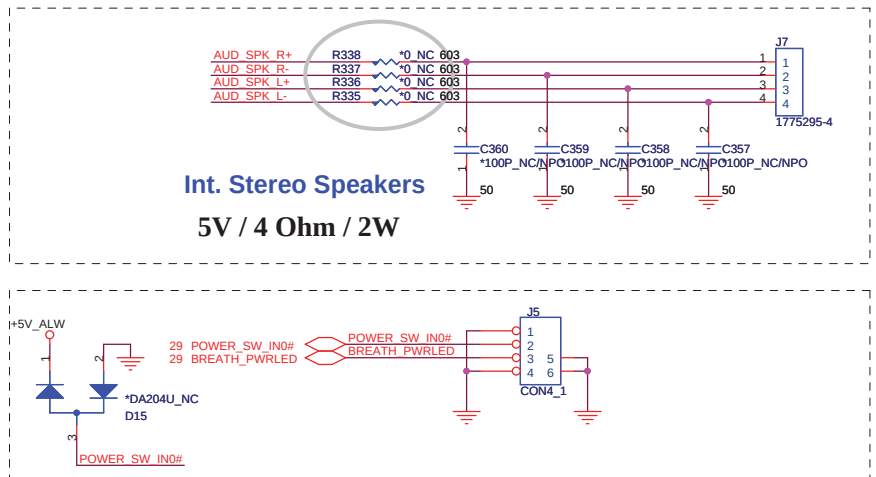
SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#						
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C



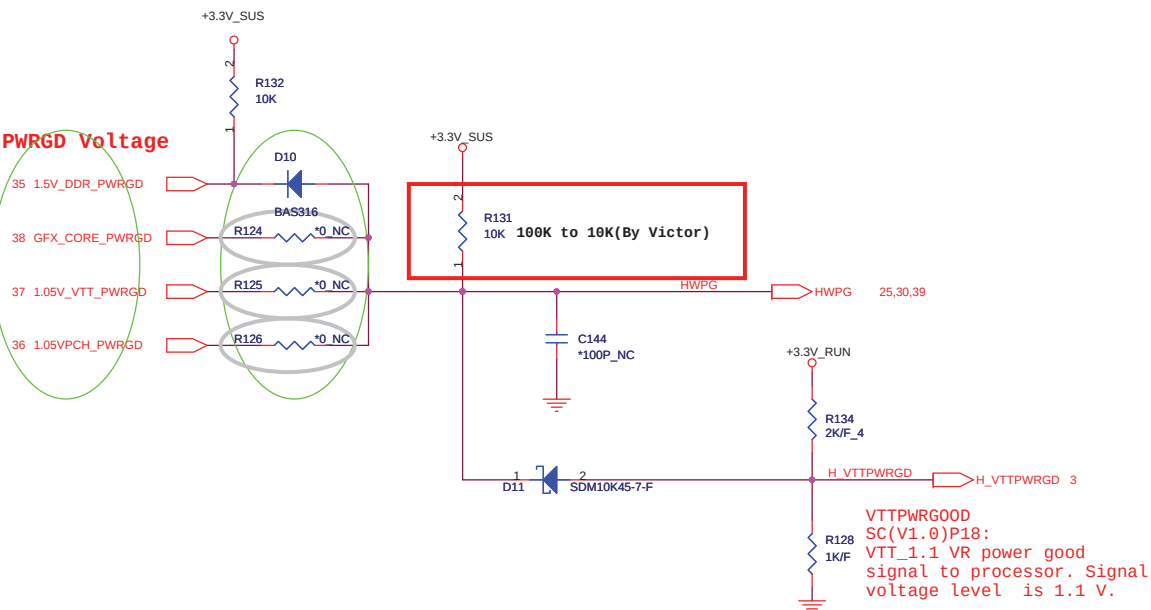
Quanta Computer Inc.
PROJECT : UM8 UMA



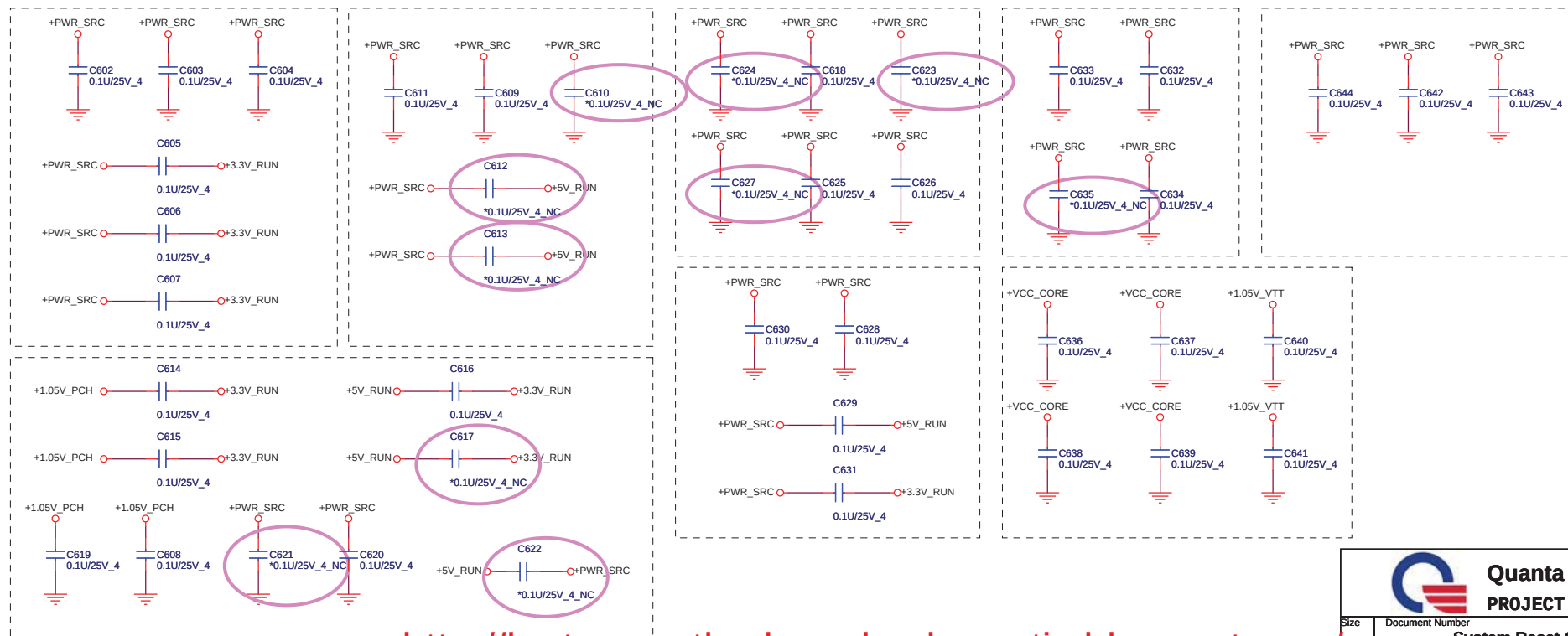
To CRT board



Check PWRGD Voltage



VTT_PWRGOOD
SC(V1.0)P18:
VTT_1.1 VR power good
signal to processor. Signal
voltage level is 1.1 V.



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		1A
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+5V_SUS
Fs=200K
TDC : 7.8A
OCP : 11.1A

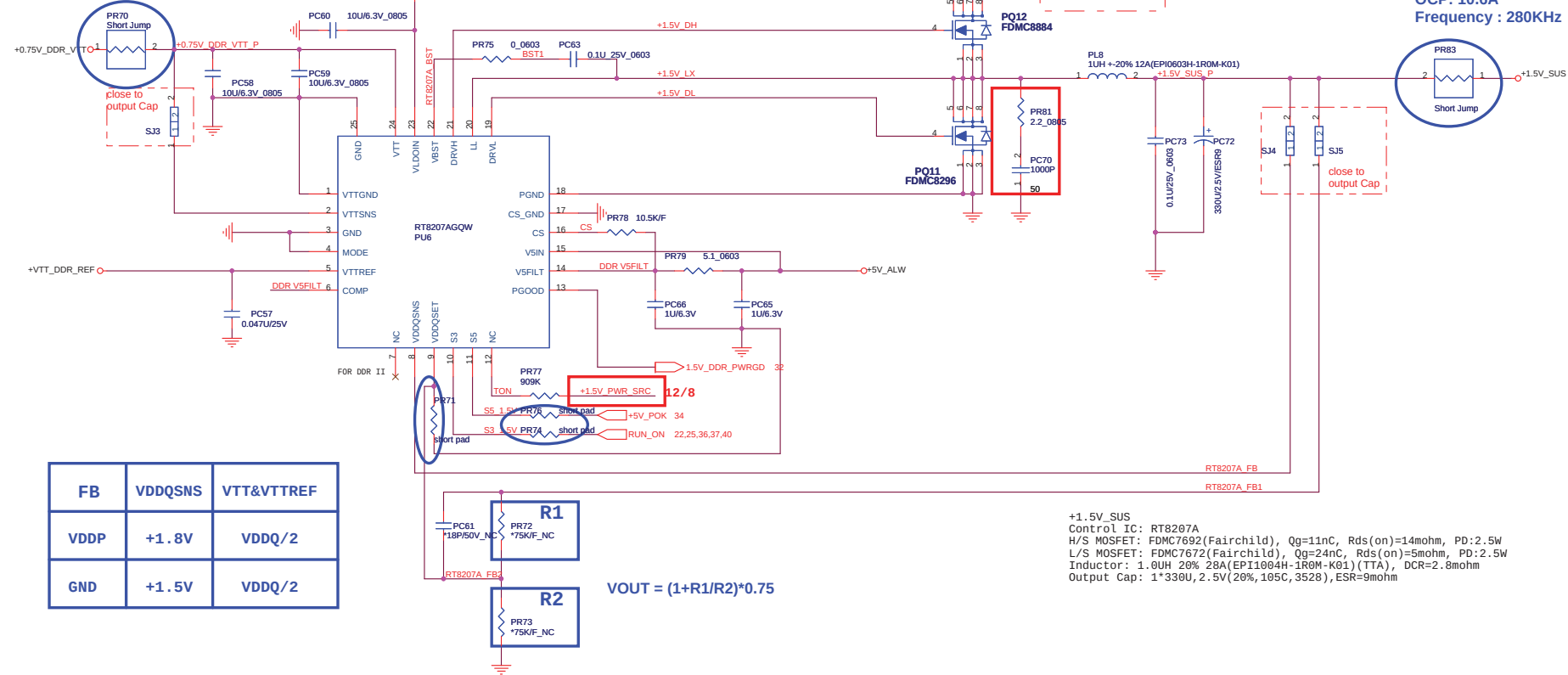
+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884(Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296(Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3uH, 30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330u, 6.3V(20%ESR17,7343)

+3.3V_ALW
Fs=250K
TDC : 6.38(UMA) ; 7.6A(DIS)
OCP : 9.11(UMA) ; 10.9A(DIS)

+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884(Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296(Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3uH, 30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330u, 6.3V(20%ESR17,7343)

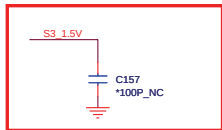
Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

+0.75V_DDR_VTT
TDC : 0.7A

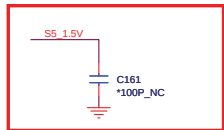


FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

$$VOUT = (1+R1/R2)*0.75$$

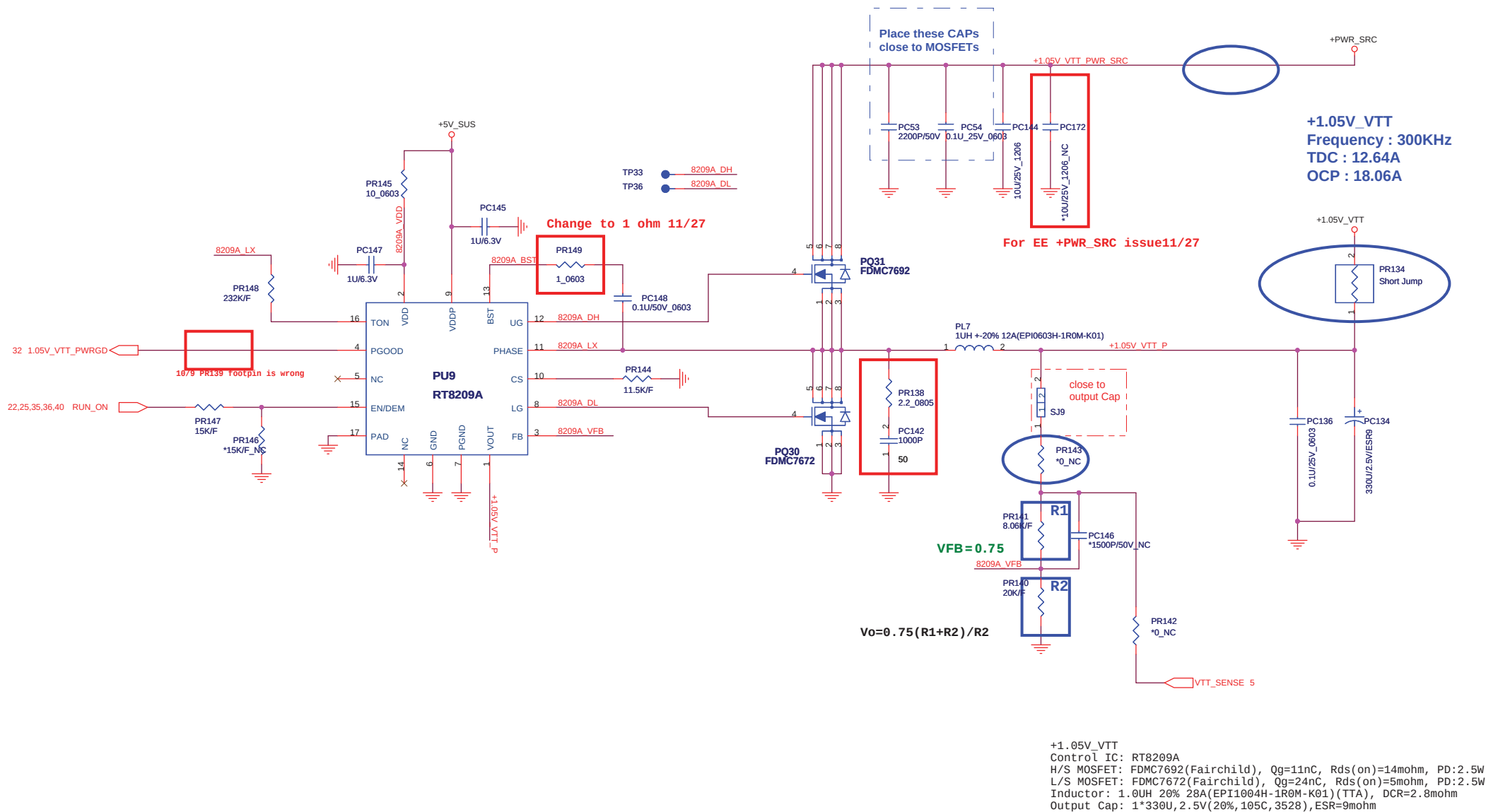


close to PR56



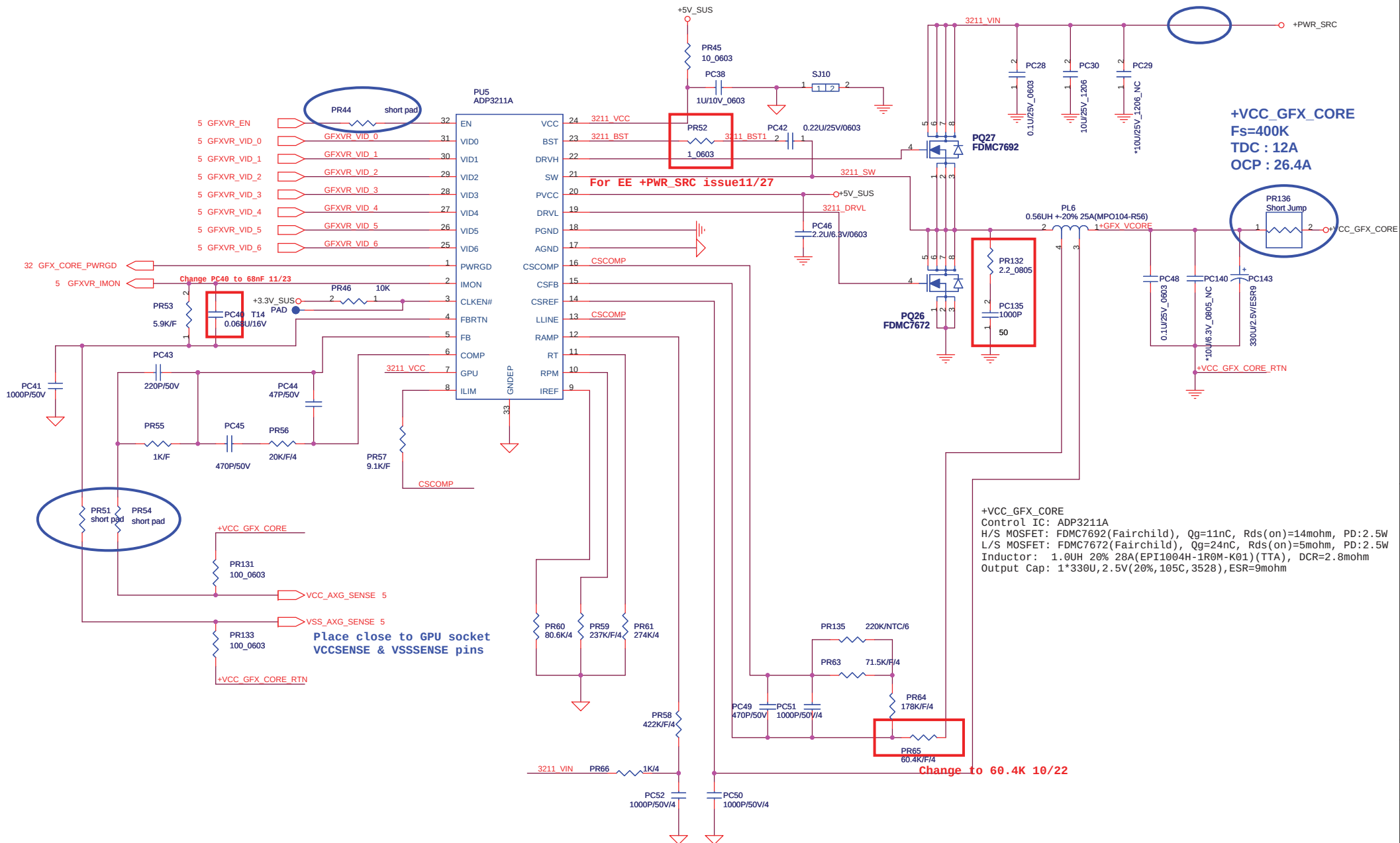
close to PR55

+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMC7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD=2.5W
L/S MOSFET: FDMC7672(Fairchild), Qg=24nC, Rds(on)=5mohm, PD=2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*330U, 2.5V(20%, 105C, 3528), ESR=9mohm



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	1.05_VTT	1A
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	GFX_CORE	1A
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Change to RUN_ON

22,25,35,36,37 RUN_ON

12/31 change to 0.01u for
Touch PAD issue - August

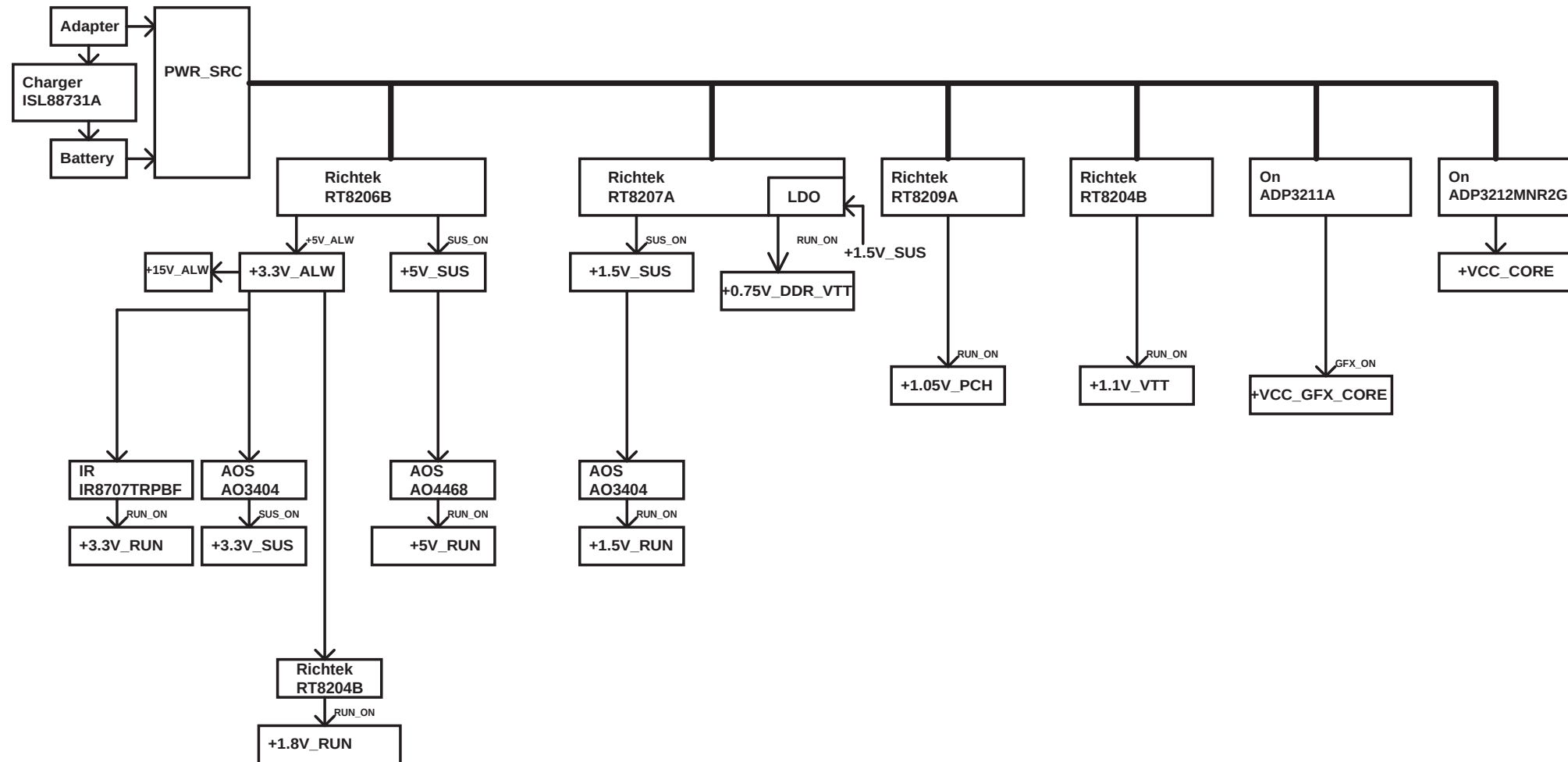
+5V_RUN
TDC : 5A

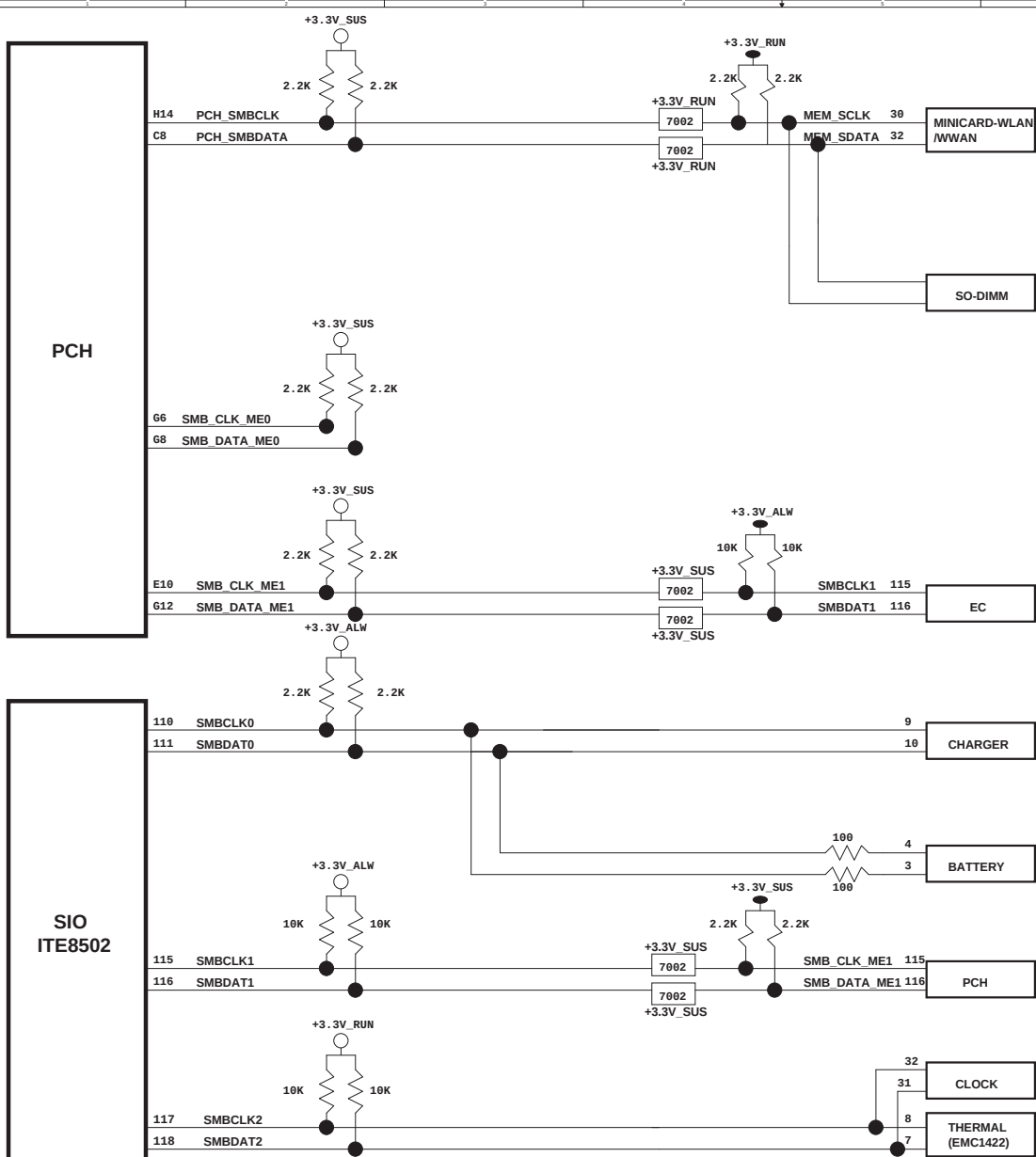
+3.3V_SUS
TDC : 0.26A

+1.5V_RUN
TDC : 0.35A

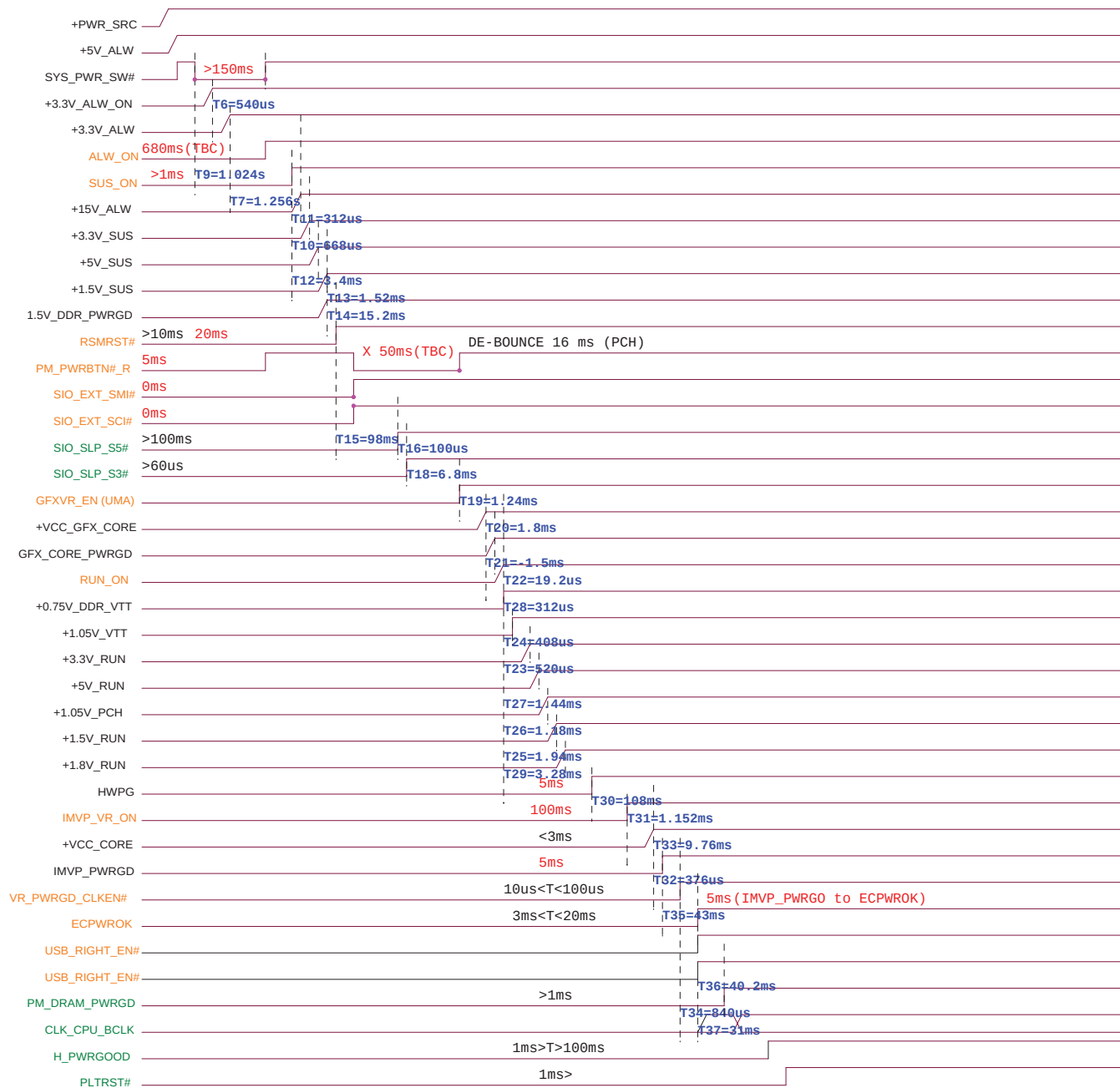
+3.3V_RUN
TDC : 4.9A

12/31 change to 0.01u for
Touch PAD issue - August





UM8_X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



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Power Design Block Diagram

