5 4 3 2 1

D

UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

C

Intel PCH(Panther Point)

DY :NotInstalled
UMA:UMA platform installed
OPS:Optimus
HR:Huron River
CR:Chief River
V: V-Series installed

B

A

<Core Design>

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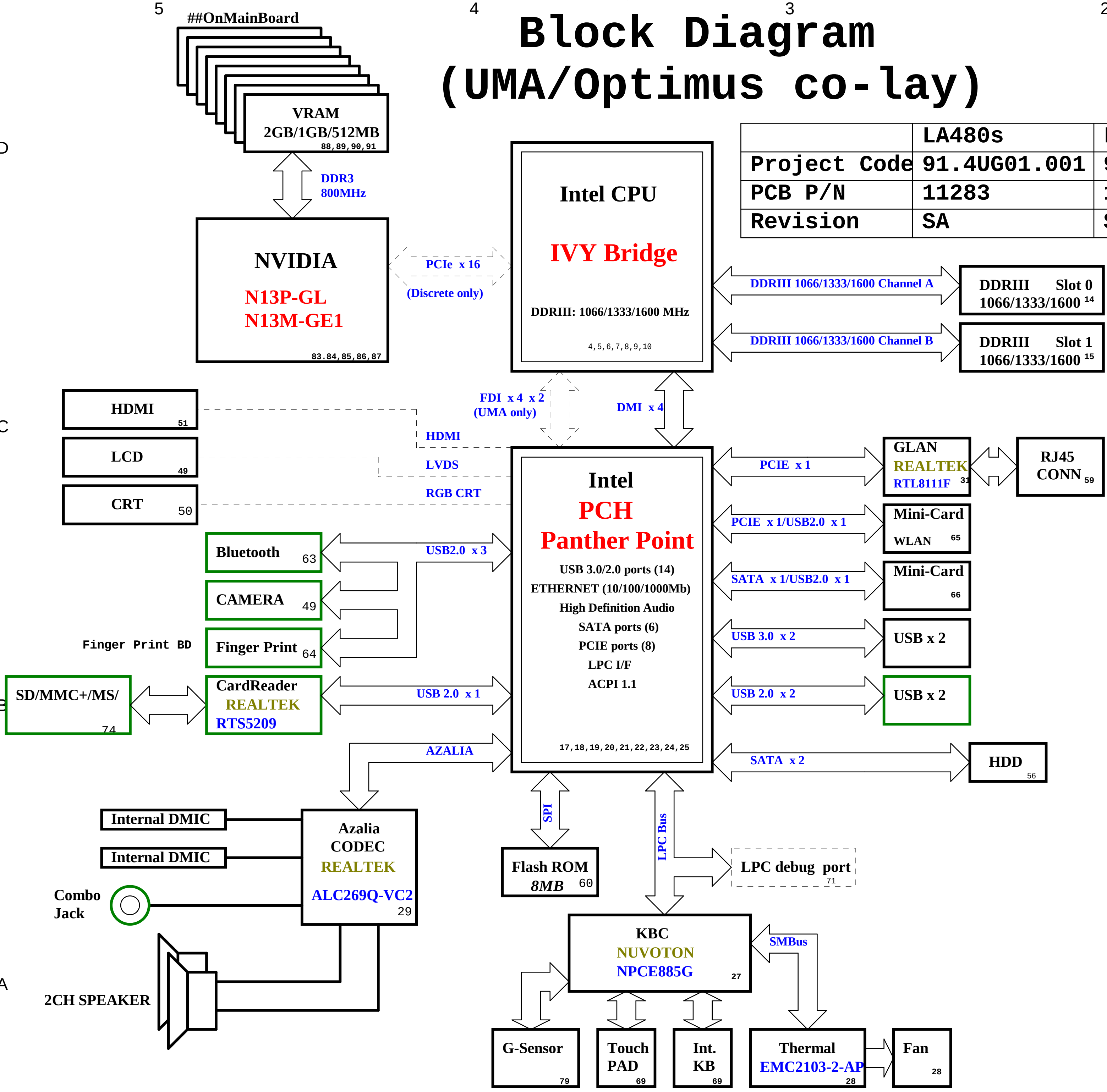
Title	**Cover Page**		
Size A4	Document Number **LA480s**		Rev SA
Date: Tuesday, March 06, 2012	Sheet 1 of 103		

Block Diagram
(UMA/Optimus co-lay)

	LA480s	LPR-1
Project Code	91.4UG01.001	91.4UH01.001
PCB P/N	11283	11284
Revision	SA	SA



CPU DC/DC TPS51640 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51219 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207M 46	
INPUTS	OUTPUTS
DCBATOUT	0D75V_S0 1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC TPS51640 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA TPS51728 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24737 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT8207 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

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Title		
Block Diagram		
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 2 of 103	

PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	X
LANE2	WLAN
LANE3	Card Reader
LANE4	LAN
LANE5	X
LANE6	X
LANE7	X
LANE8	X

USB Table

port9 is debug port

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 3
3	USB3.0 ext port 2
4	BLUETOOTH (USB1.1)
5	Card Reader
6	X
7	X
8	WWAN
9	USB2.0 ext port 4
10	FingerPrint
11	WLAN
12	CCD
13	X

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SMBus ADDRESSES

I^2C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA	
Pair	Device
0	mSATA
1	HDD1
2	N/A
3	N/A
4	ODD
5	N/A

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Title: Table of Content		
Size: A3	Document Number: LA480s	Rev: SA
Date: Tuesday, March 06, 2012	Sheet 3 of 103	

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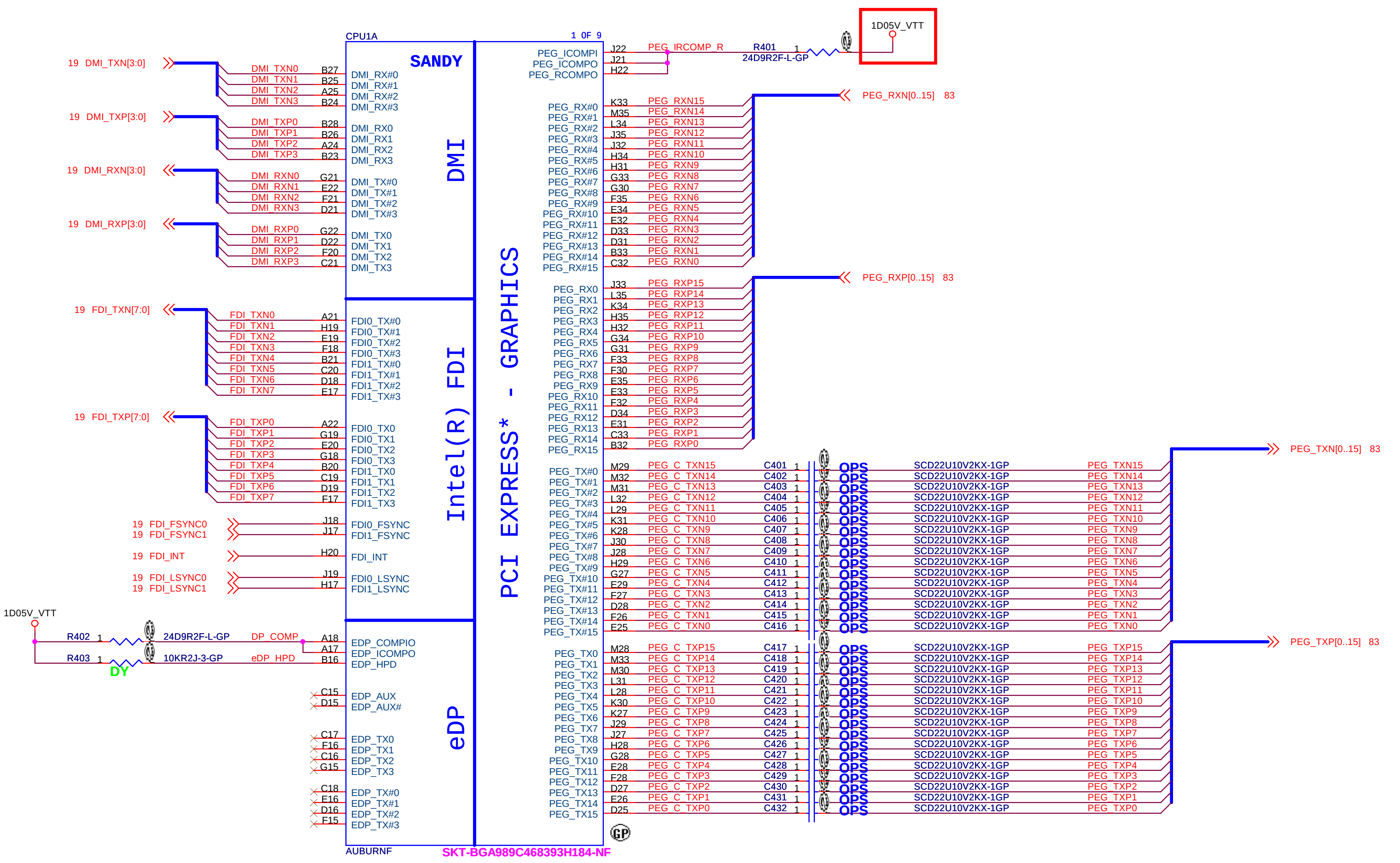

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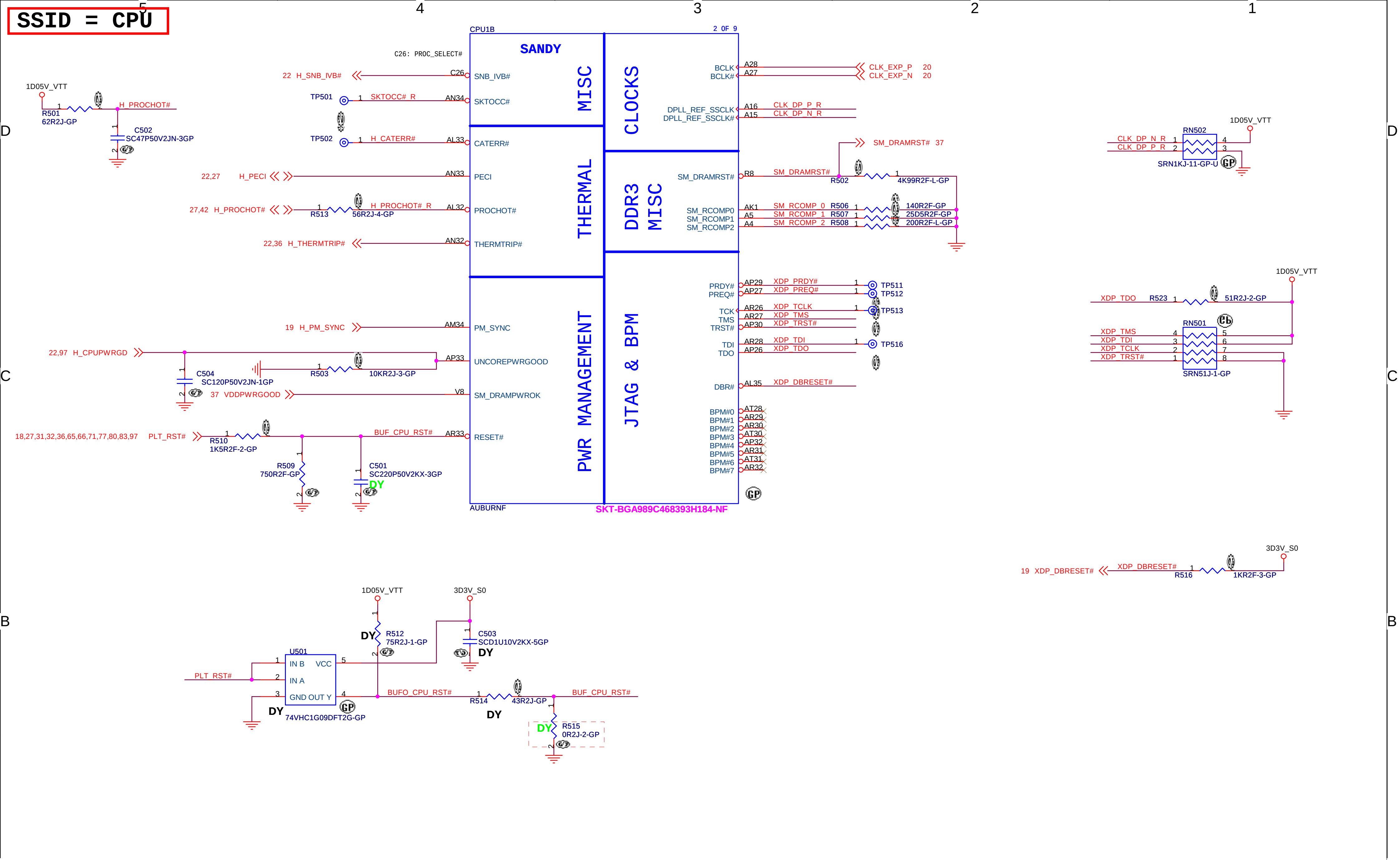
Title	CPU (PCIE/DMI/FDI)	
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 4 of 103	



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Title	CPU (THERMAL/CLOCK/PM)	
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 5 of 103	

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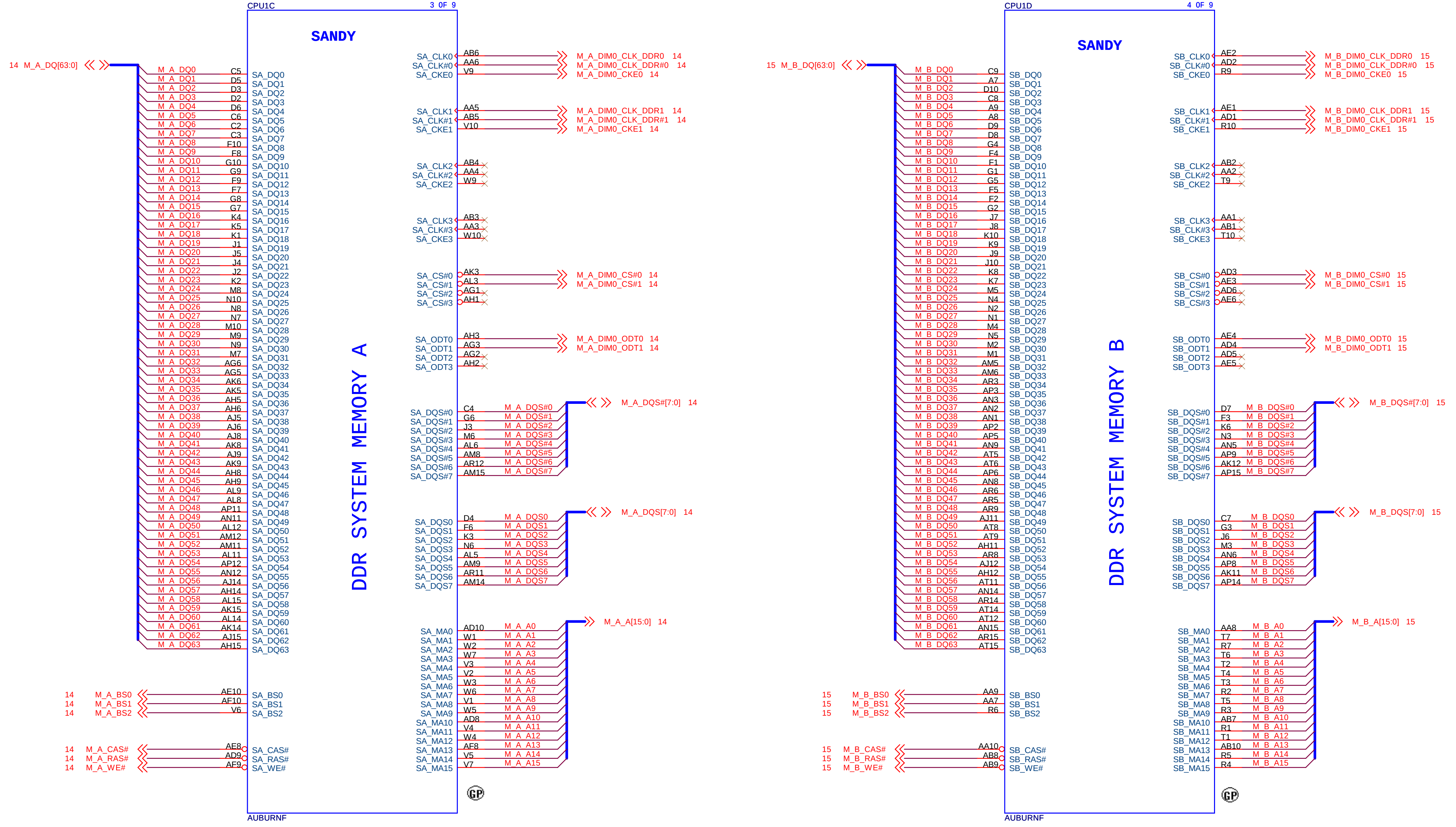

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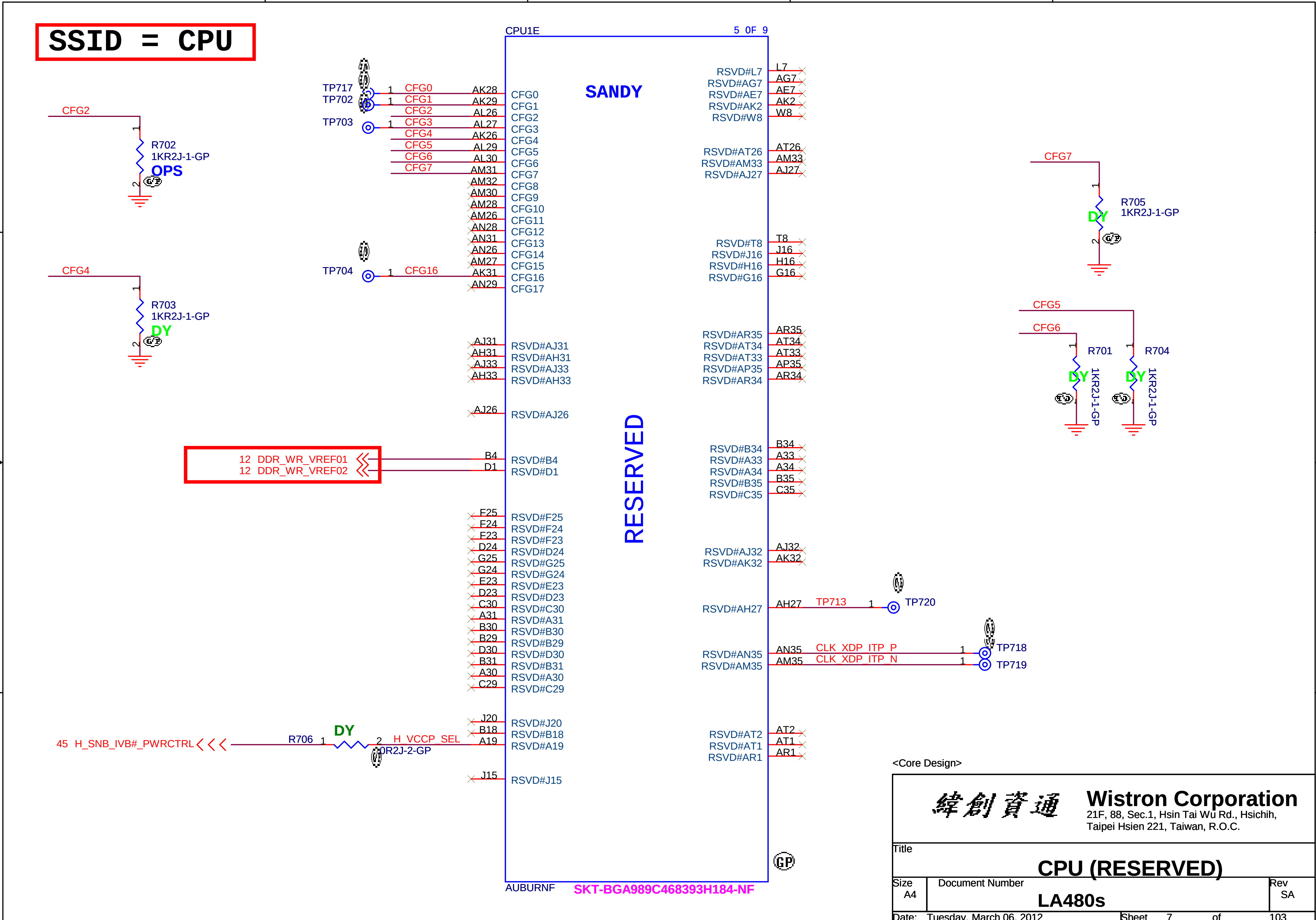
Title	CPU (DDR)	
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 6 of 103	



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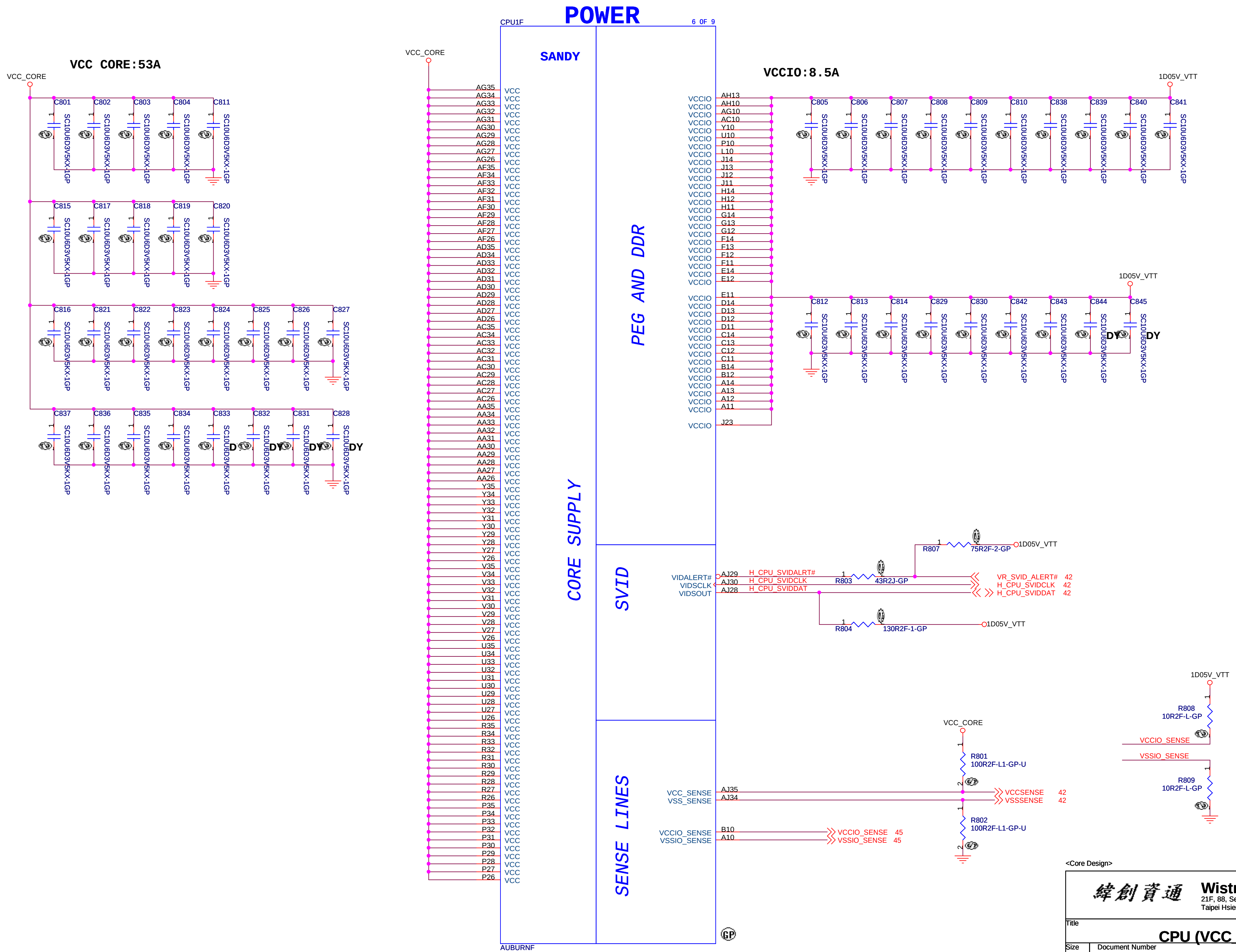
Title	CPU (RESERVED)		
Size A4	Document Number LA480s		Rev SA
Date: Tuesday, March 06, 2012		Sheet 7	of 103



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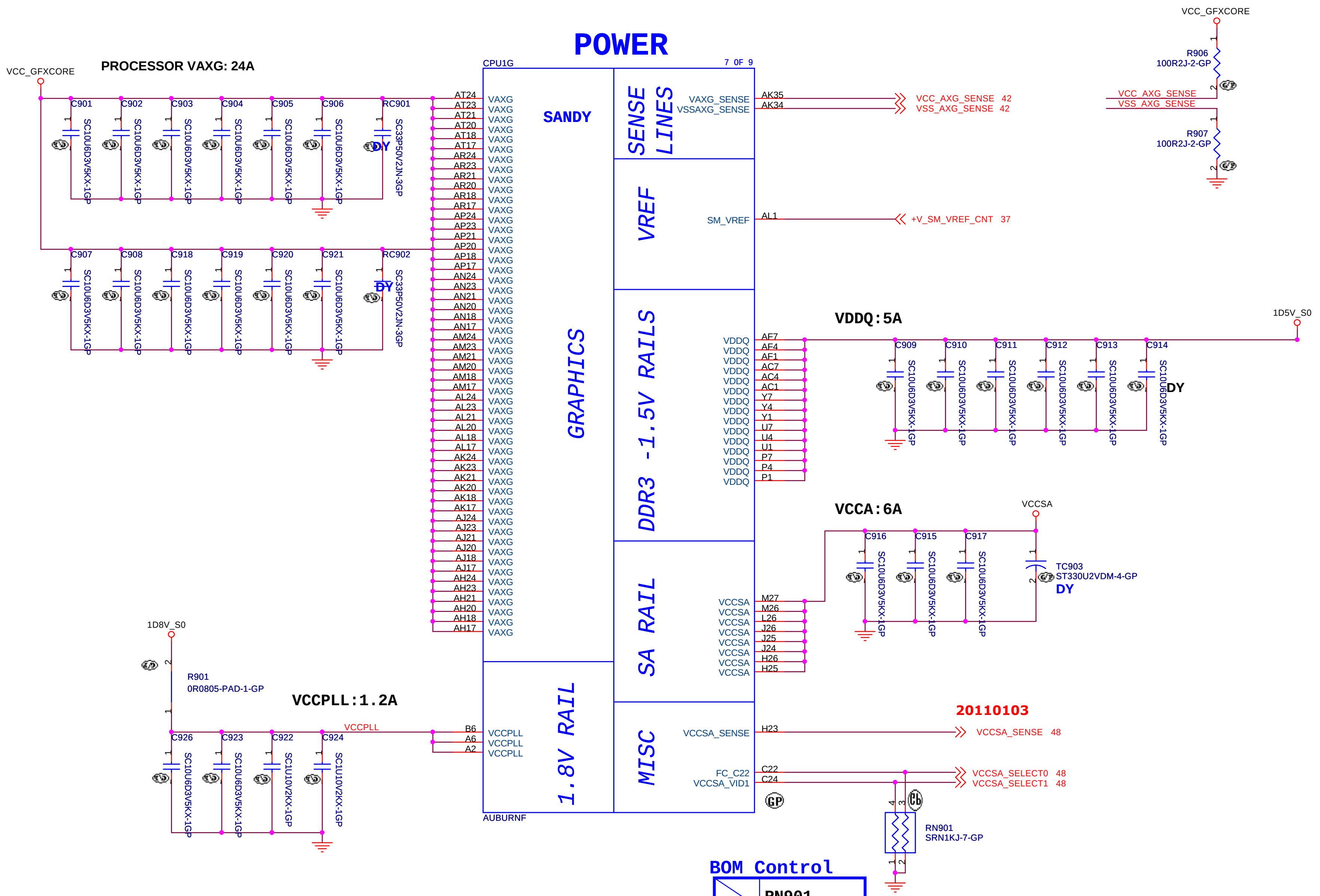
Title	CPU (VCC_CORE)	
Size: Custom	Document Number: LA480s	Rev: SA
Date: Wednesday, March 07, 2012	Sheet 8 of 103	



BOM Control

	R906/R907
CRV	100 ohm
HR	10 ohm

BOM Control

	RN901
HR	10K ohm --------------
CRV	1K ohm 66.10236.04L

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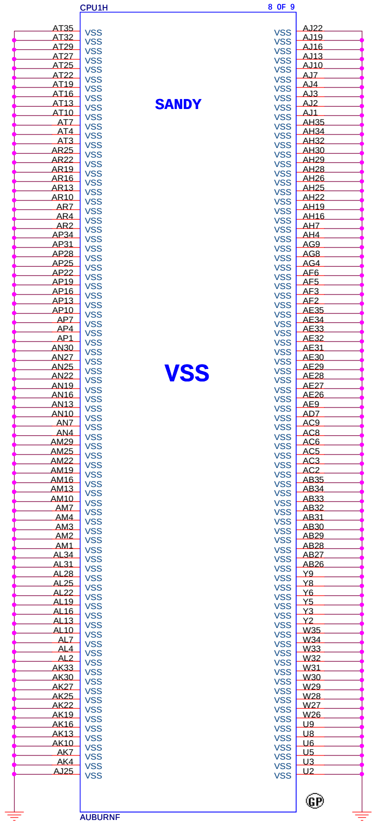
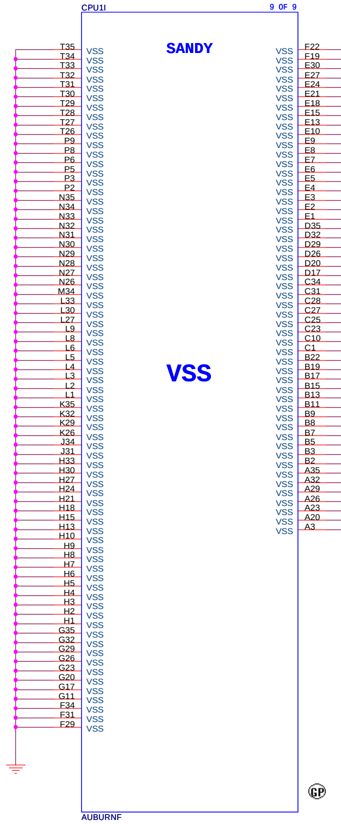
Title
CPU (VCC_GFXCORE)

Size	Document Number	Rev
A3	LA480s	SA

Date: Wednesday, March 07, 2012 Sheet 9 of 103

SSID = CPU





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Title	CPU (VSS)	
Size A2	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 10 of 103	

5 4 3 2 1

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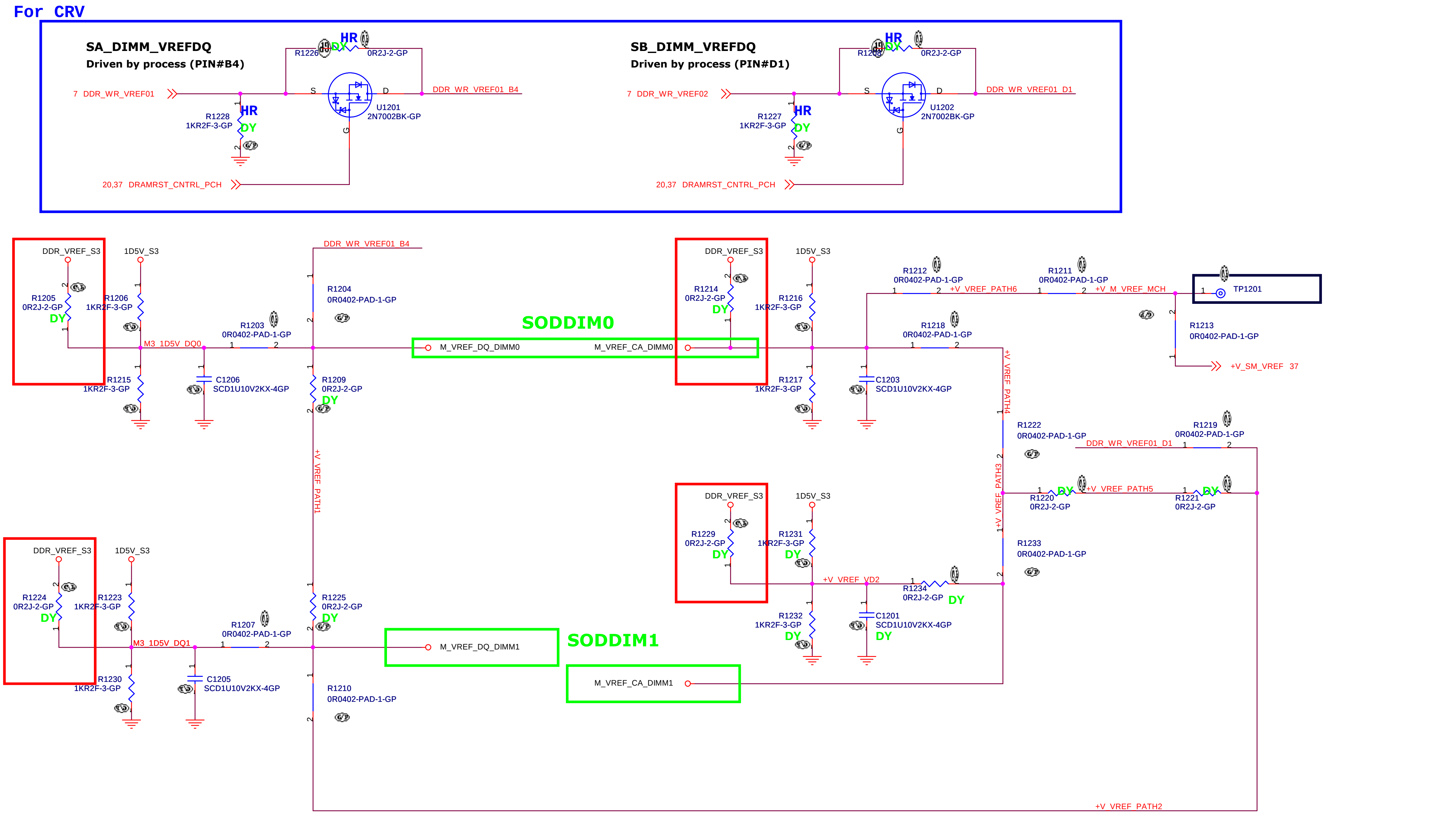
Title: <Title>		
Size: A4	Document Number: **LA480s**	Rev: SA
Date: Tuesday, March 06, 2012	Sheet 11 of 103	

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

CAD Note: All VREF traces should have 20:20 mil trace geometry. Note that while 20 mil trace width is optimal, short violations is acceptable if required due to tight routing constraints.



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Title	M3	
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 12 of 103	

5 4 3 2 1

D

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<Core Design>

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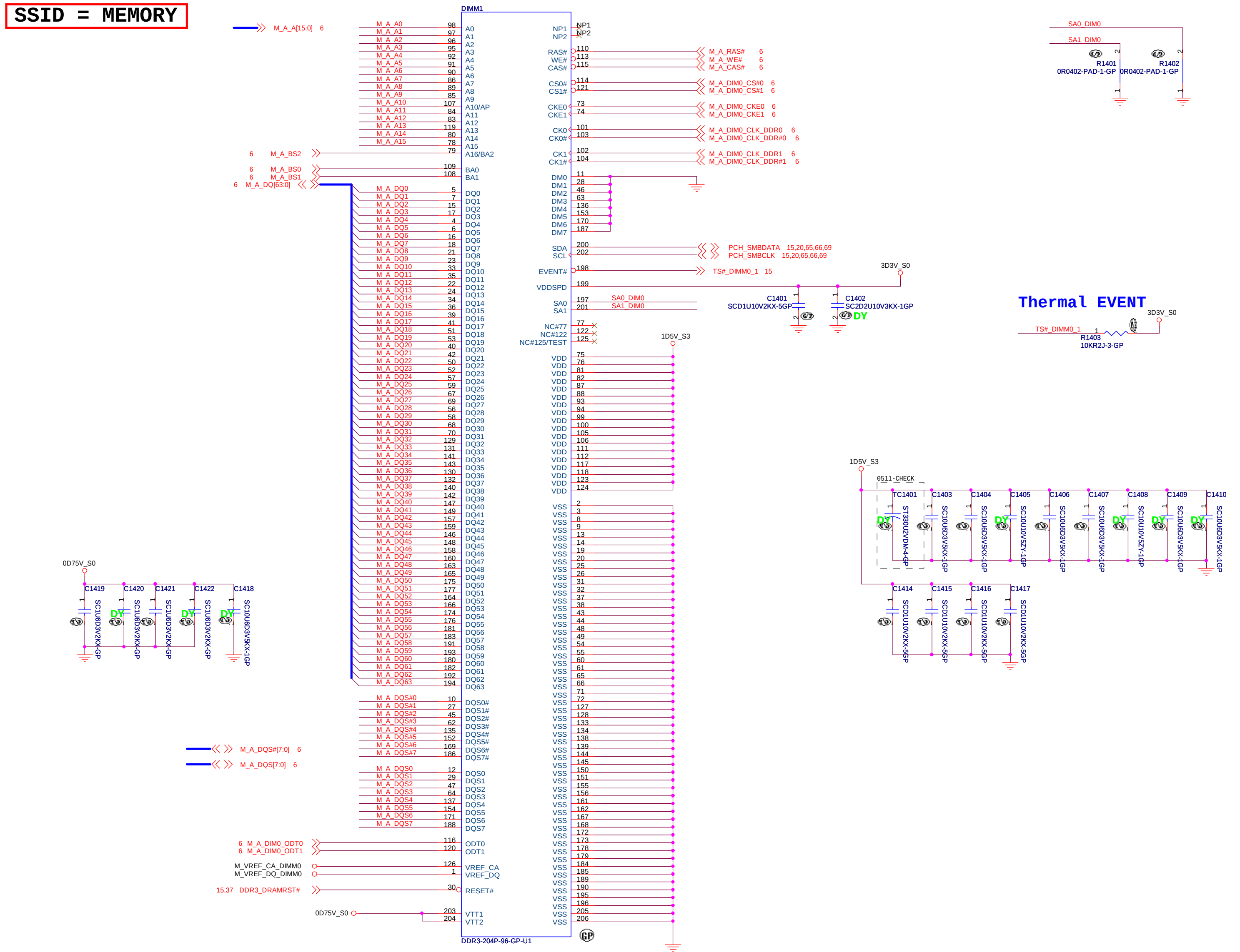
Title	<Title>
Size A4	Document Number **LA480s** — Rev SA
Date: Tuesday, March 06, 2012	Sheet 13 of 103



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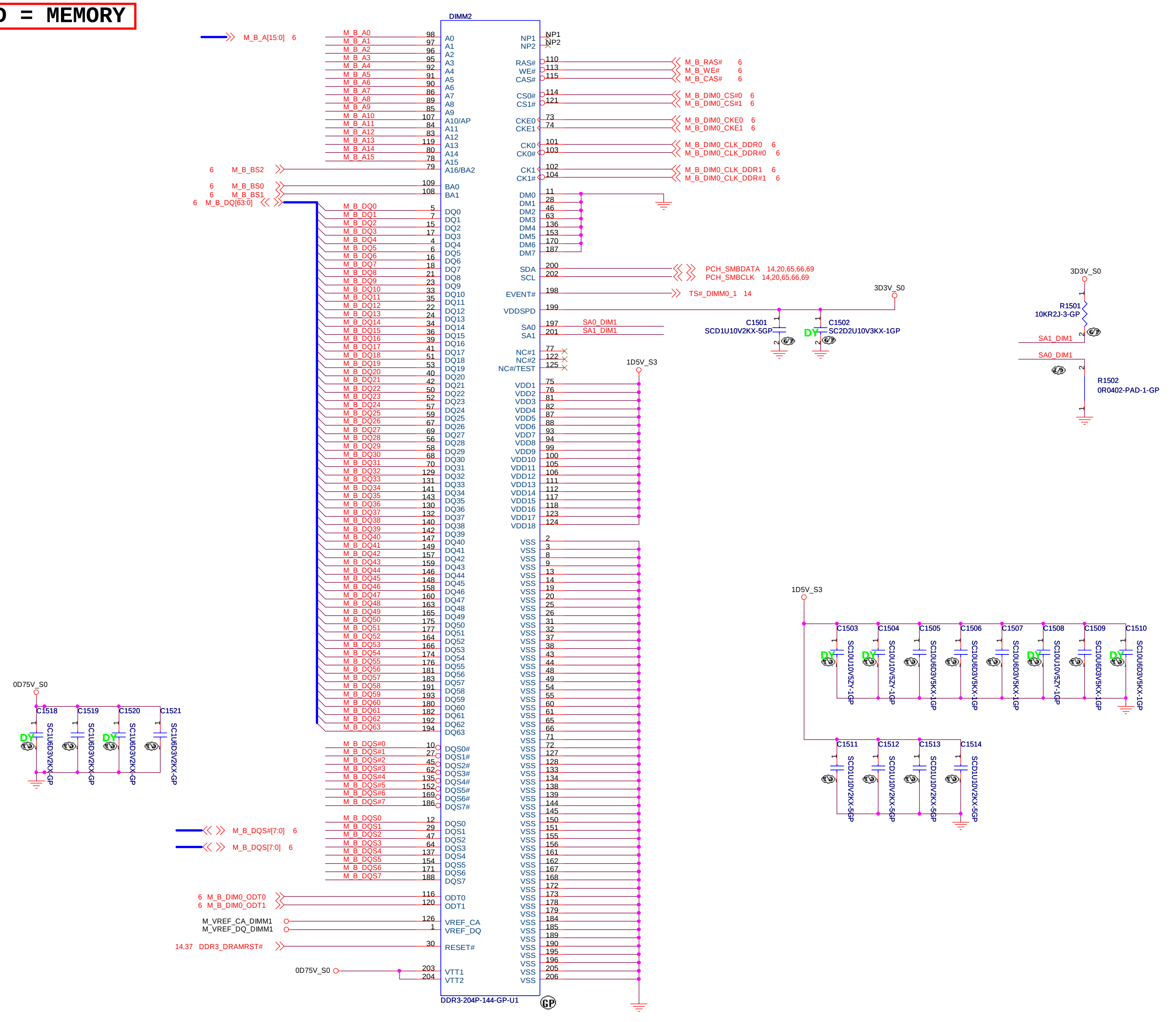
Title		
DDR3-SODIMM1		
Size: A2	Document Number: LA480s	Rev: SA
Date: Tuesday, March 06, 2012	Sheet 14 of 103	

SSID = MEMORY



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Title	DDR3-SODIMM2	
Size A2	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 15 of 103	

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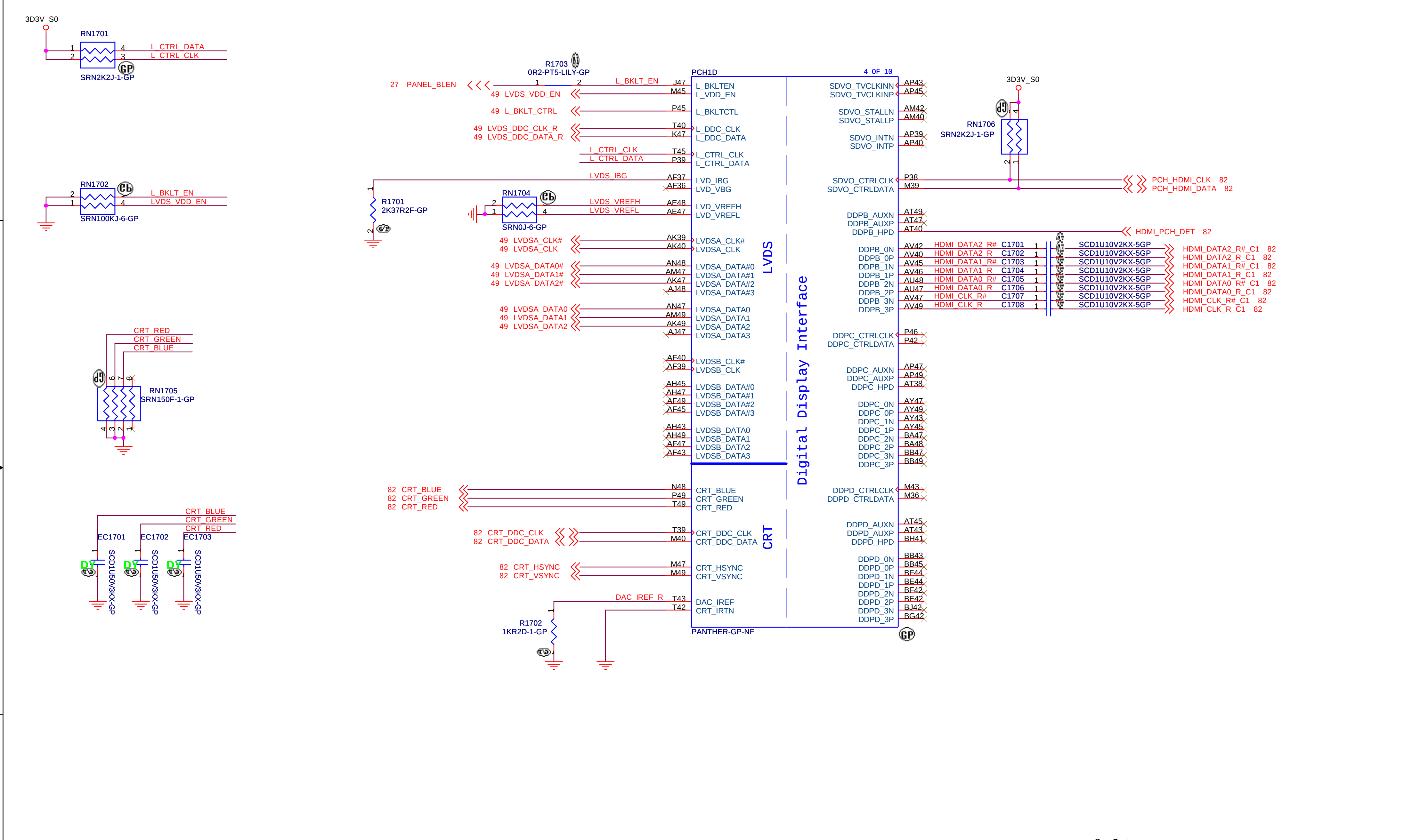
Title	**DDR3-SODIMM2**
Size A4	Document Number **LA480s** Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 16 of 103



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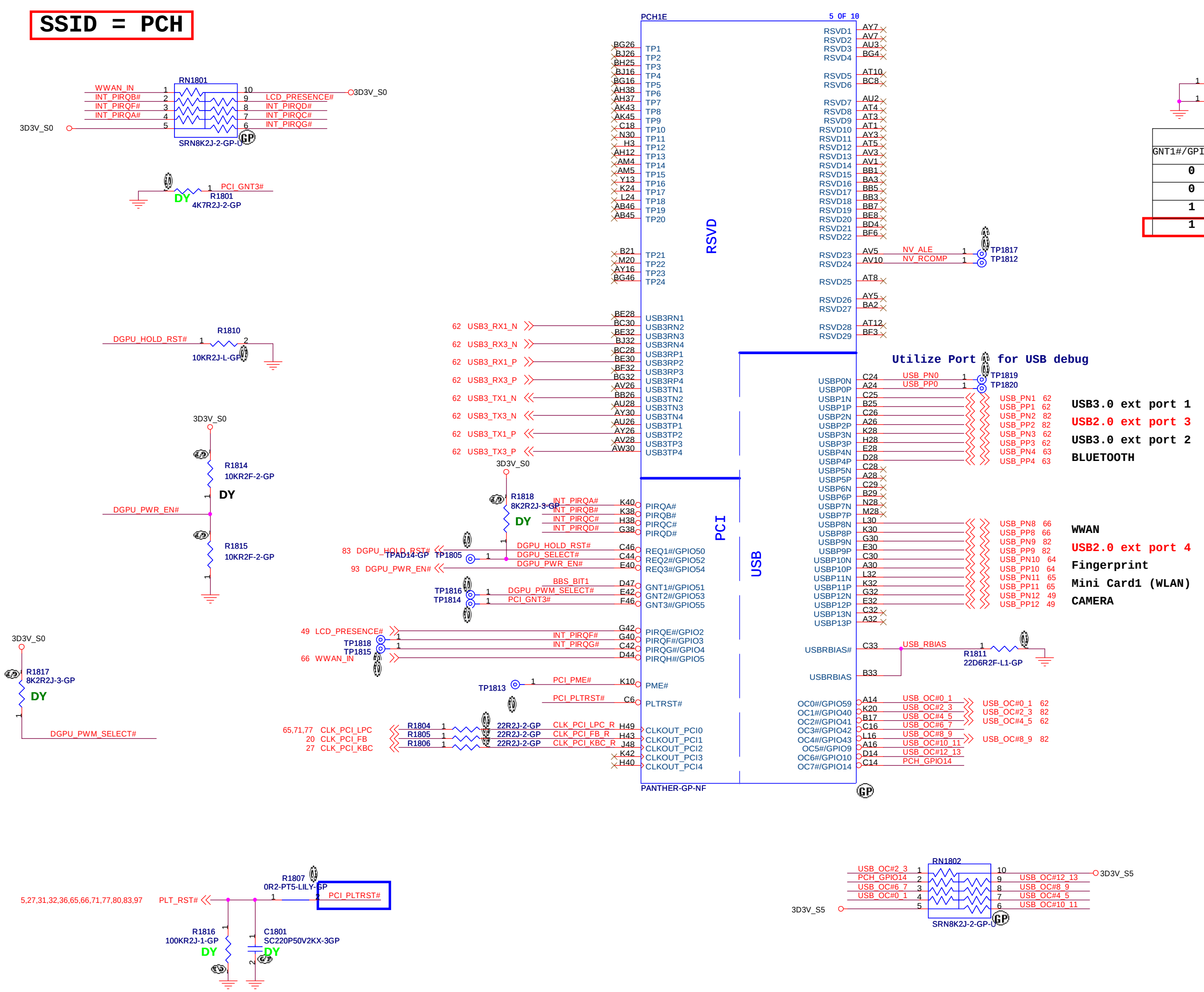
Title
PCH : LVDS/CRT/DDI

Size	Document Number	Rev
A3	LA480s	SA

Date: Tuesday, March 06, 2012 Sheet 17 of 103



BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

Gx8 USB Table

Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext. port 3
3	USB3.0, ext port2
4	Bluetooth
5	X
6	X
7	X
8	3G
9	USB2.0, ext port4
10	Finger Print
11	Mini Card1 (WLAN)
12	CAMERA
13	X

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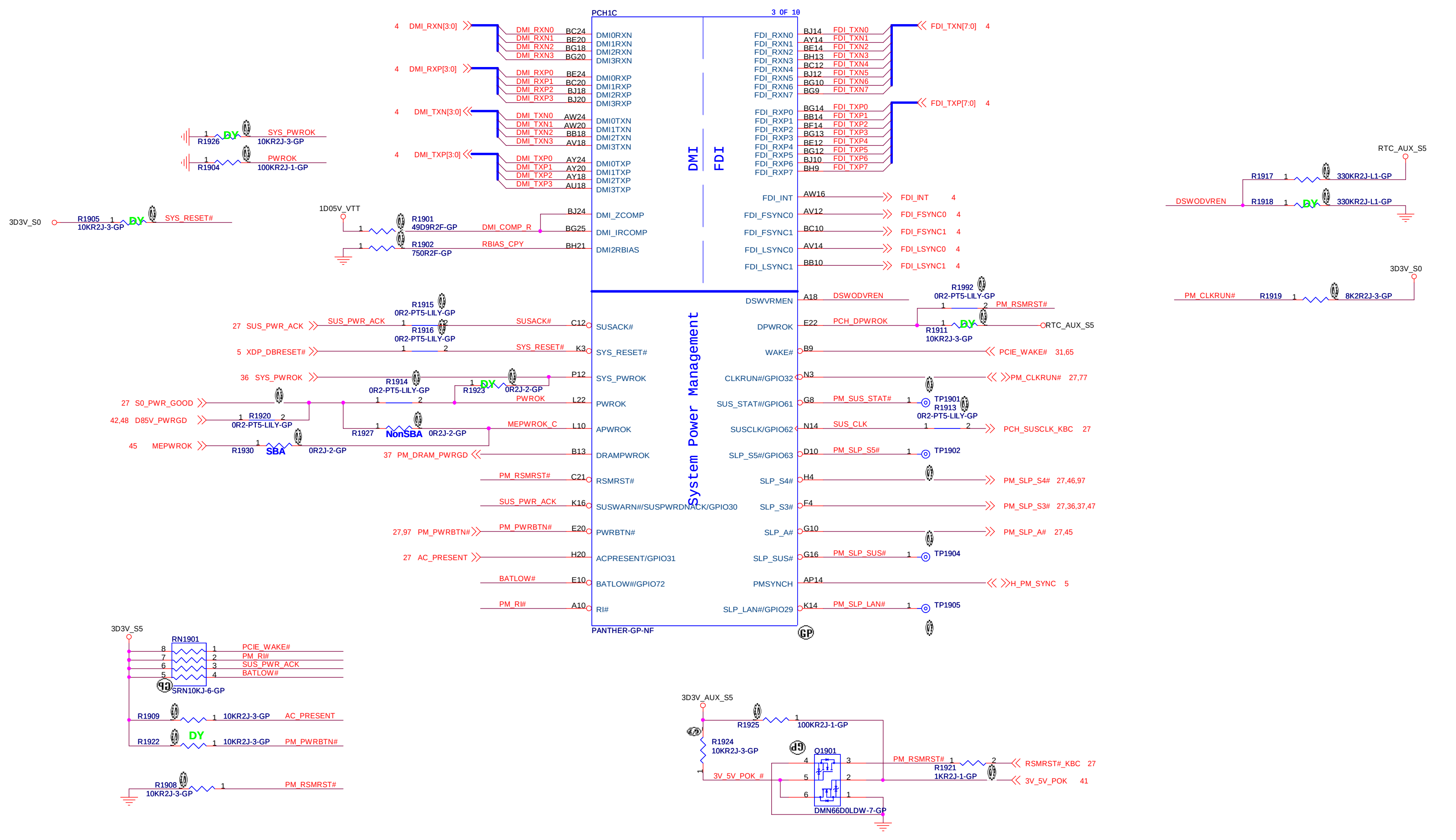
Title: PCH : PCI/USB/NVRAM/RSVD

Size: A2 | Document Number: LA480s | Rev: SA

Date: Tuesday, March 06, 2012 | Sheet 18 of 103

SSID = PCH



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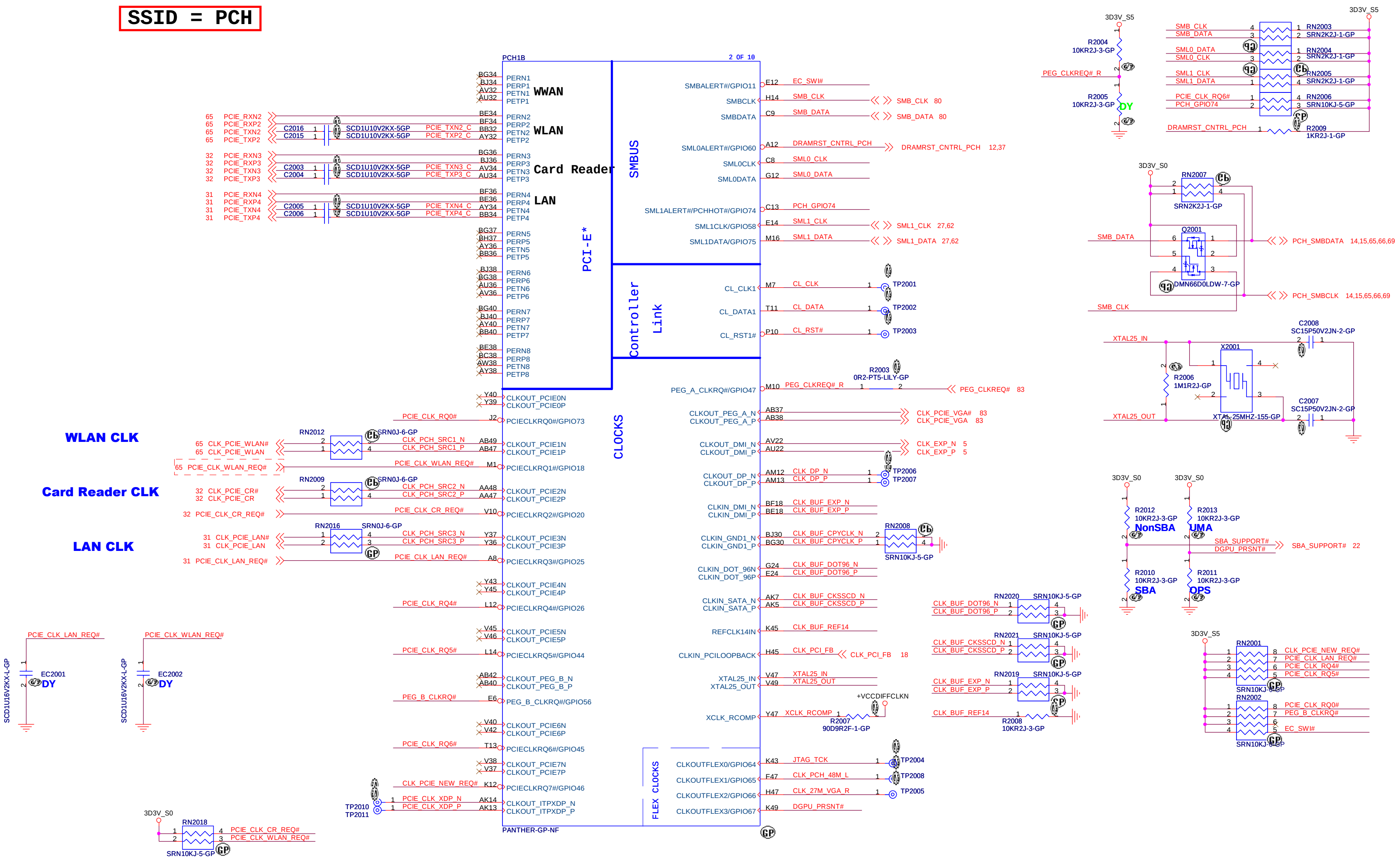
Title	PCH : DMI/FDI/PM	
Size A2	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 19 of 103	



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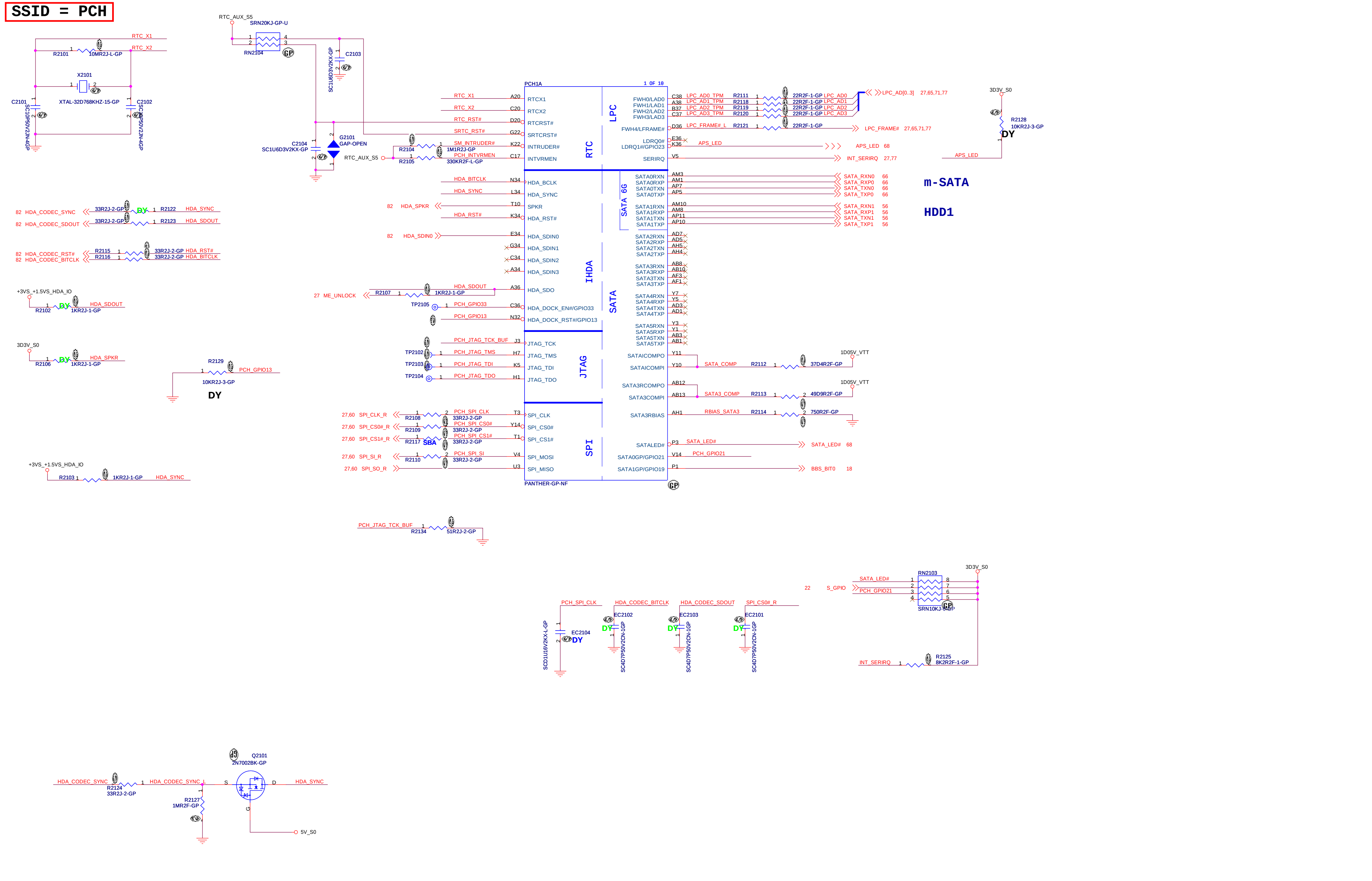
Title		
PCH : PCIE/SMBUS/CLK		
Size A2	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 20 of 103	



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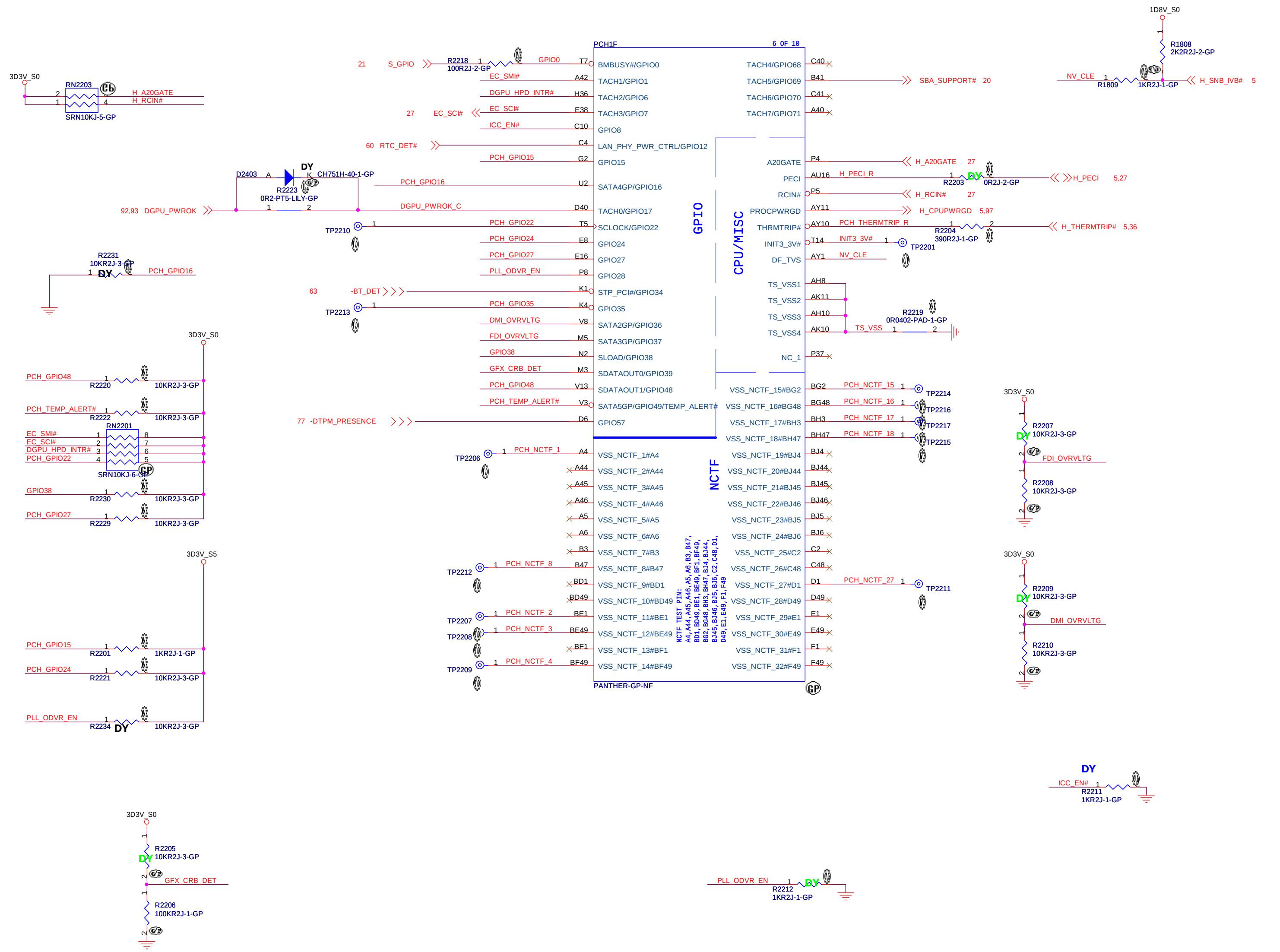
Title: **PCH : HDA/JTAG/SATA**

Size	Document Number	Rev
A2	LA480s	SA

Date: Tuesday, March 06, 2012 Sheet 21 of 103



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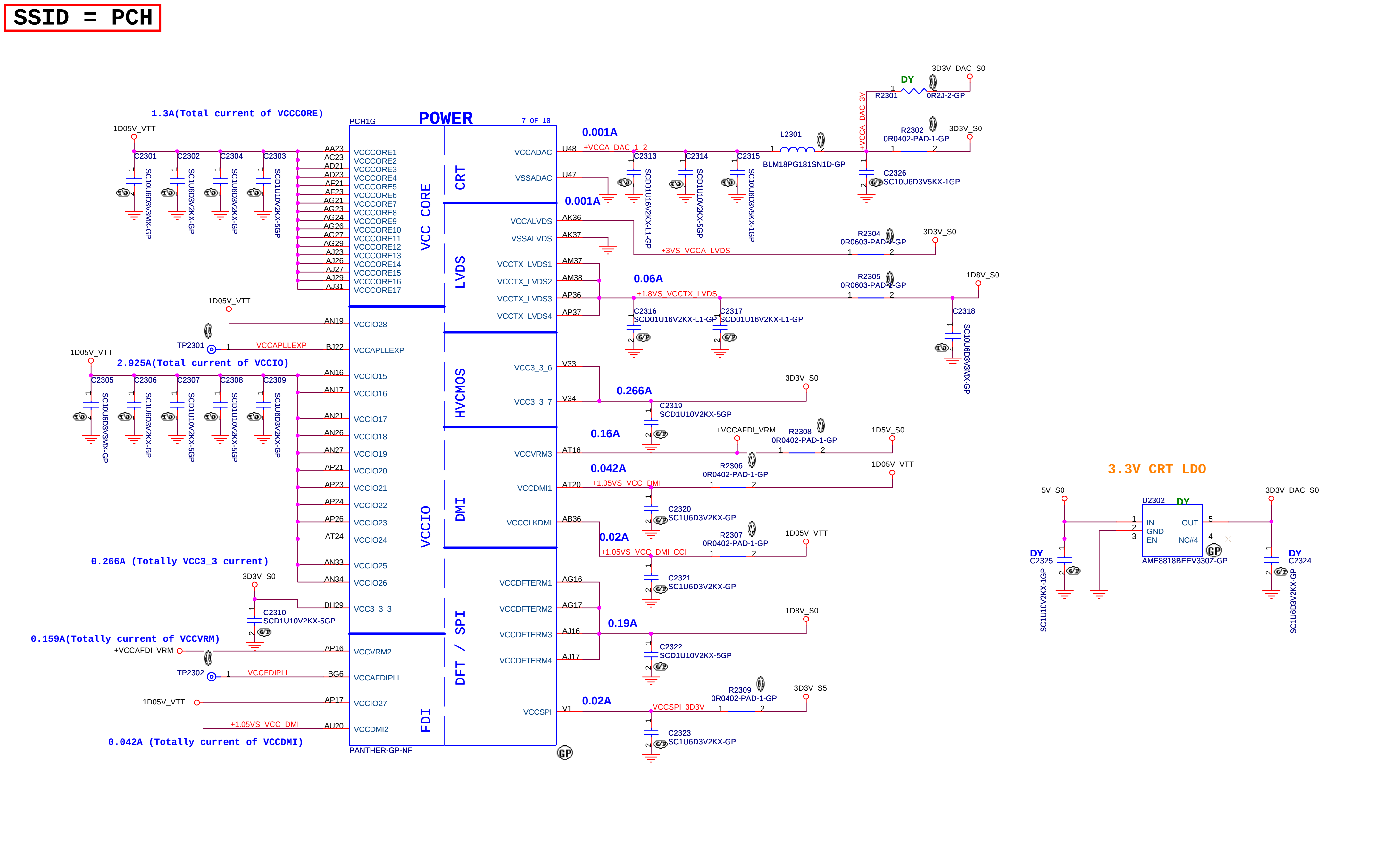
Title		
PCH : GPIO/NTCF/MISC		
Size A2	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 22 of 103	



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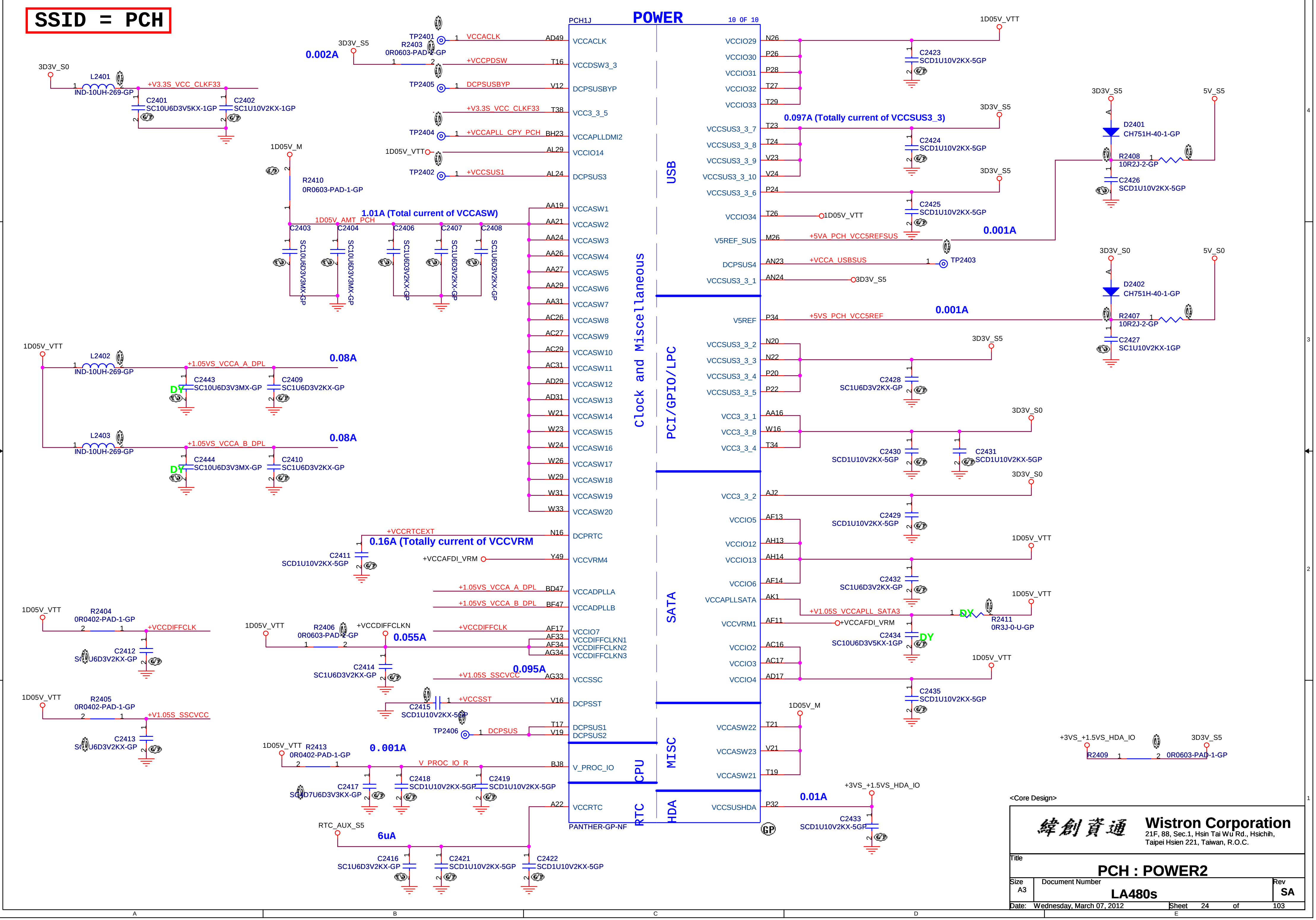
Title		
PCH : POWER1		
Size A3	Document Number LA480s	Rev SB
Date: Wednesday, March 07, 2012	Sheet 23 of 103	

SSID = PCH



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Title	**PCH : POWER2**
Size A3	Document Number **LA480s** — Rev **SA**
Date: Wednesday, March 07, 2012	Sheet 24 of 103

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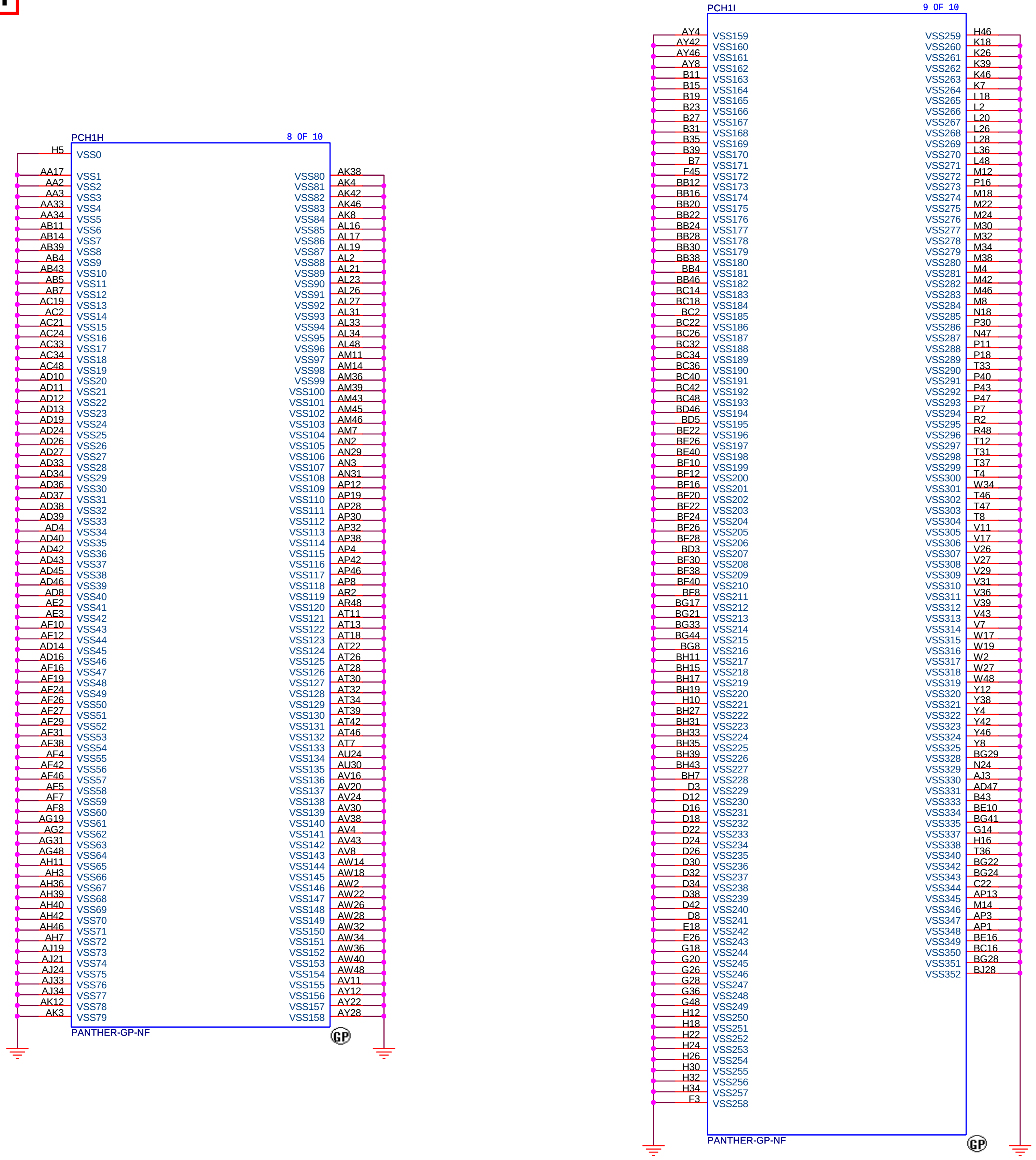

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Title	**PCH : VSS**	
Size A3	Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 25 of 103	

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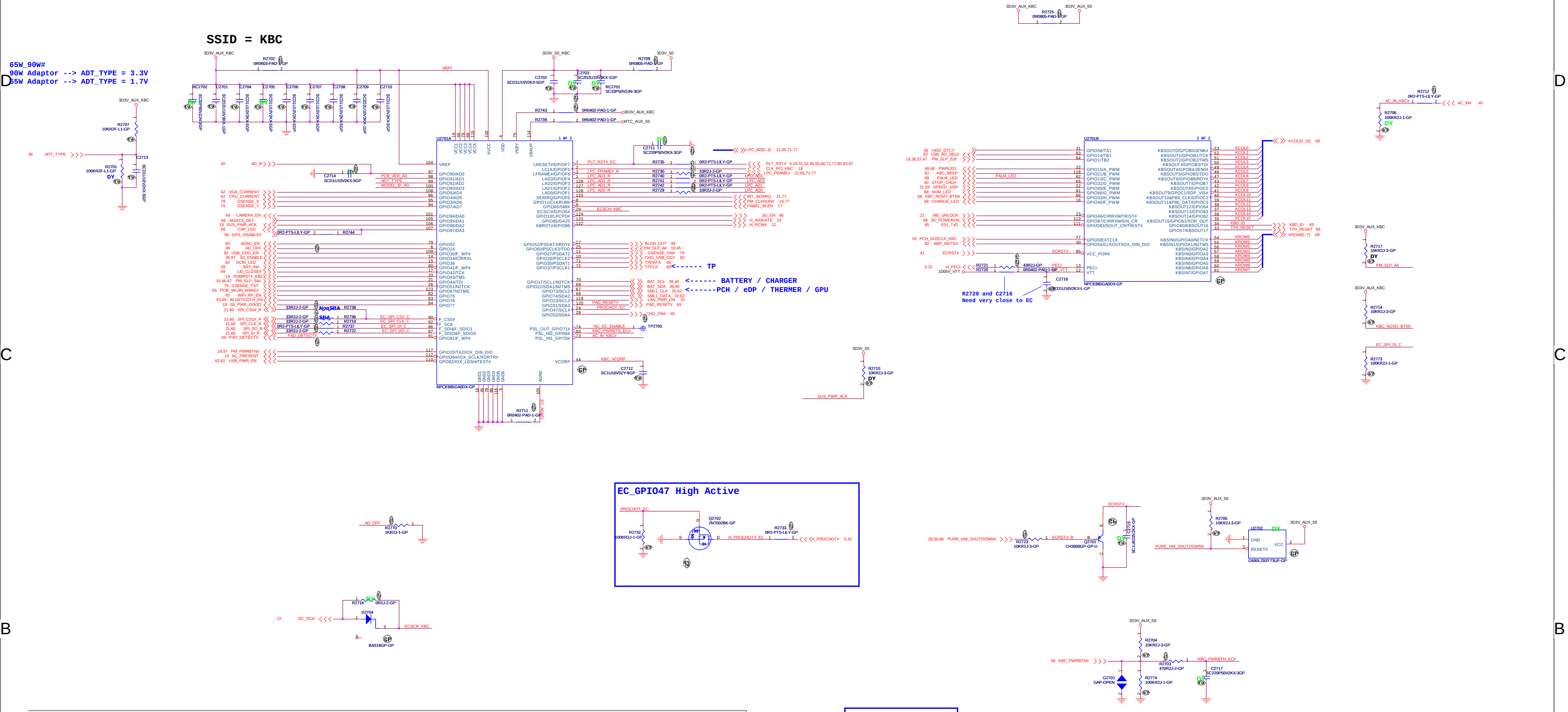
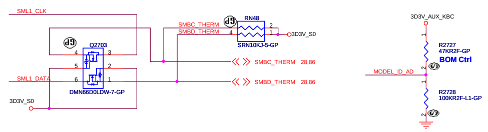
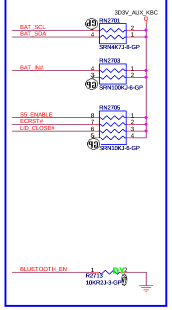
Title: **Reserved**		
Size: A4	Document Number: **LA480s**	Rev: **SA**
Date: Tuesday, March 06, 2012	Sheet 26 of 103	

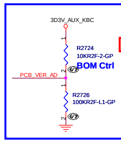




MODEL_ID_AD(Pin100)	Pull-Low Register	Pull-High Register	Voltage
V480s UMA	100.0 K	147 K 64.14735.6DL	1.336 V
V480s PX	100.0 K	215 K 64.21535.6DL	1.048 V
LPR-1 UMA	100.0 K	280 K 64.28035.6DL	0.868 V
LPR-1 PX	100.0 K	392 K 64.39235.6DL	0.671 V

EC GPIO standard PH/PL





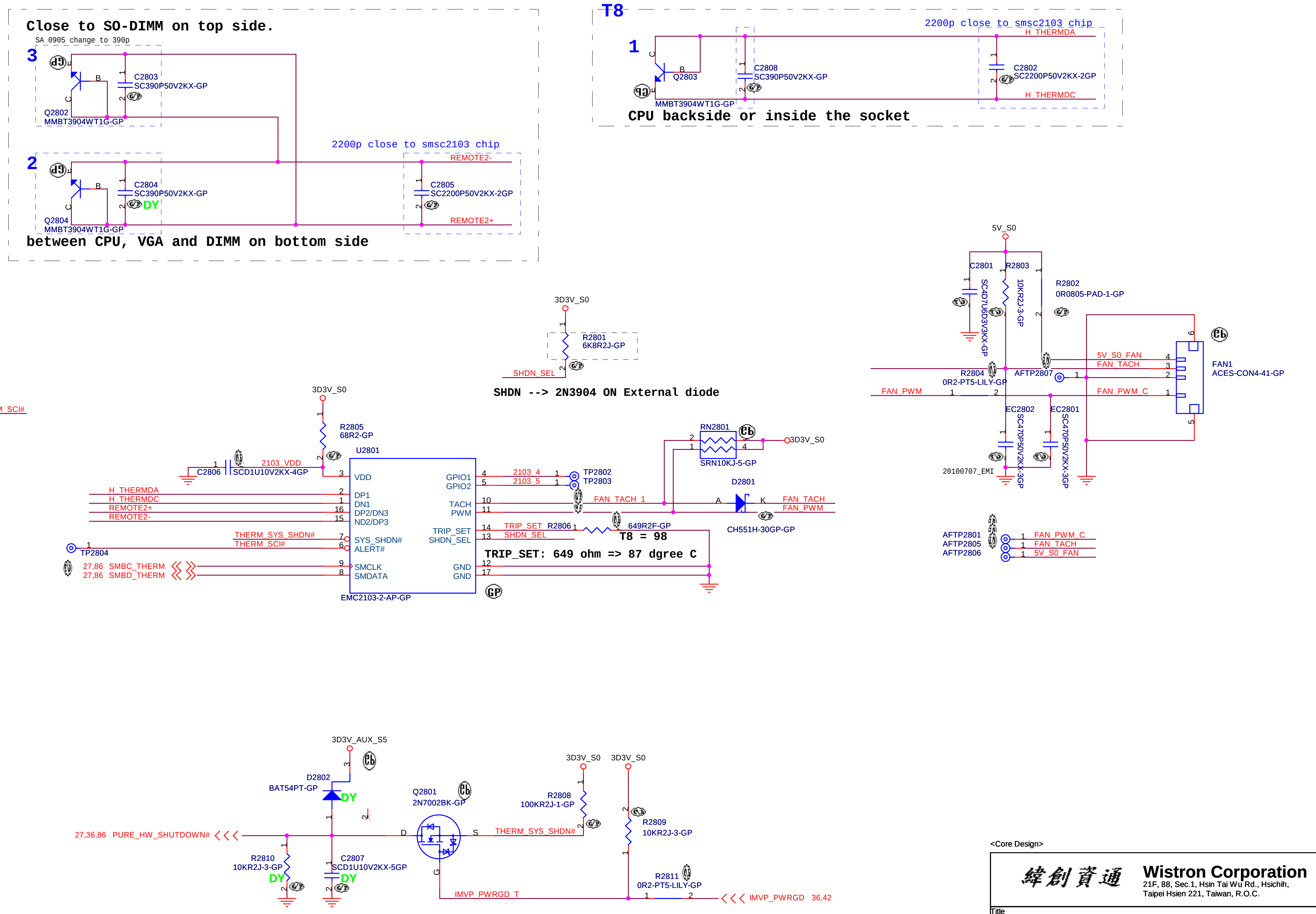
PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

<Core Design>

緯創資通	Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C
Title	<Title>
Size A1	Document Number LA480s — Rev SA
Date: Tuesday, March 06, 2012	Sheet 27 of 103

SSID = Thermal

Thermal sensor



<Core Design>

緯創資通 **Wistron Corporation**
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Title: **THERMAL SENSOR SMSC EMC2103**		
Size: A3	Document Number: **LA480s**	Rev: **SA**
Date: Tuesday, March 06, 2012	Sheet 28 of 103	

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

AUDIO CODEC

Size	Document Number	Rev
A4	**LA480s**	**SA**

Date: Tuesday, March 06, 2012 Sheet 29 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
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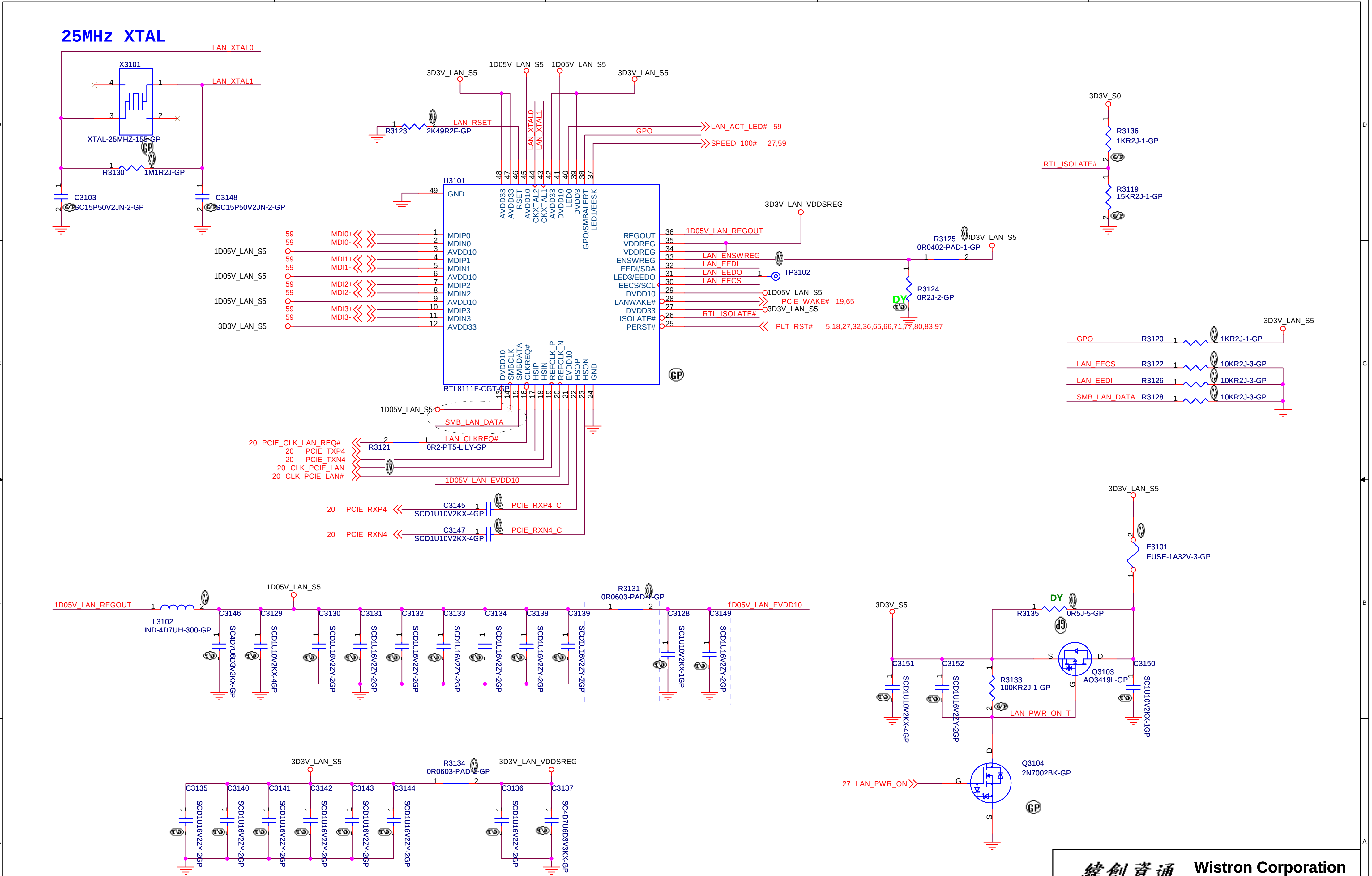
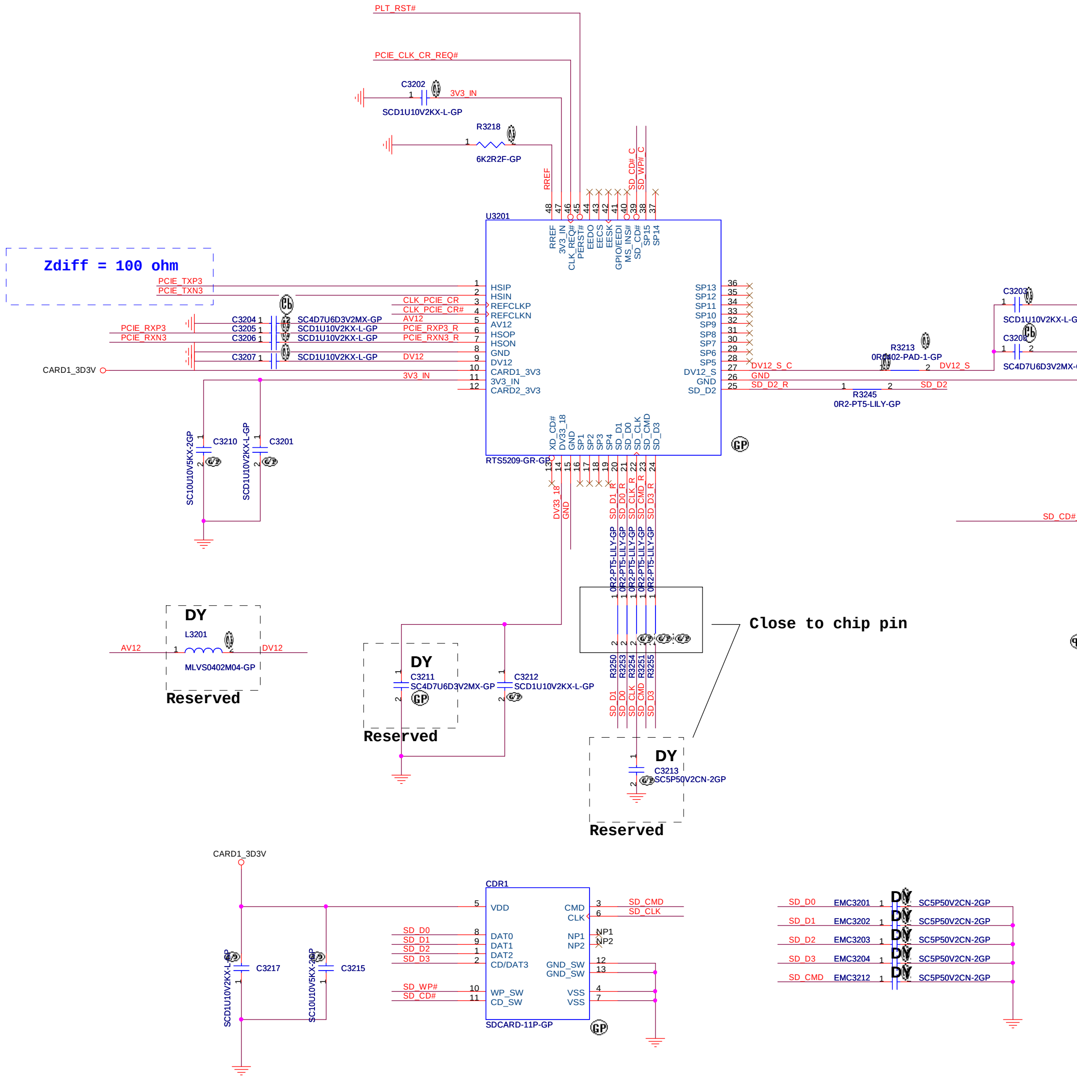
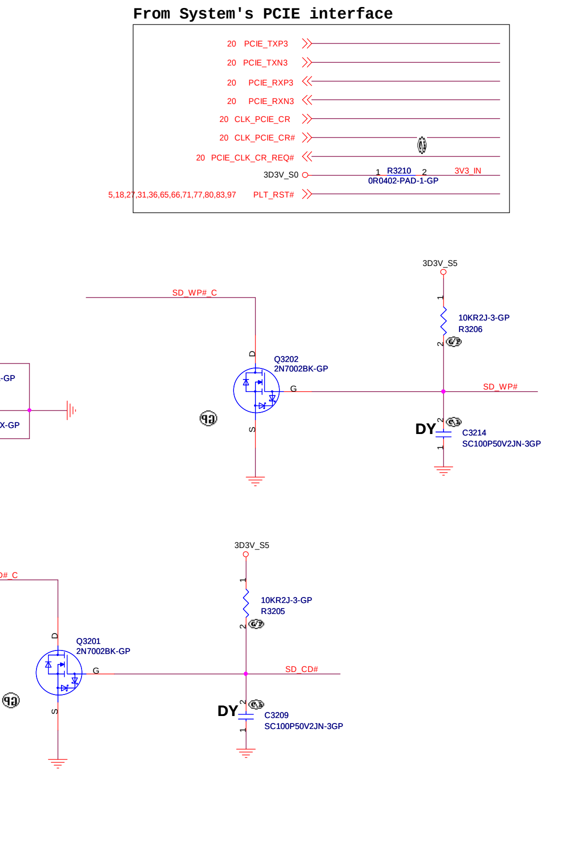
Title	**Reserved**	
Size A4	Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 30 of 103	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
<Core Design>

Title	LAN_RTL8111F	
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 31 of 103	





Common Net

SP1	SD_D7		XD_RDY
SP2	SD_D6		XD_RE#
SP3	SD_D5		XD_CE#
SP4	SD_D4		XD_WE#
SP5		MS_BS	XD_CLE
SP6		MS_D5	XD_ALE
SP7		MS_D1	XD_WP#
SP8		MS_D4	XD_D0
SP9		MS_D0	XD_D1
SP10		MS_D2	XD_D2
SP11		MS_D6	XD_D3
SP12		MS_D3	XD_D4
SP13		MS_D7	XD_D5
SP14			XD_D6
SP15	SD_WP		XD_D7

<Core Design>

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Title	RTS5209/5139	
Size A2	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 32 of 103	

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<Core Design>

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Title	**Reserved**	
Size A4	Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 33 of 103	

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<Core Design>

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Title **Reserved**		
Size A4	Document Number **LA480s**	Rev **SA**
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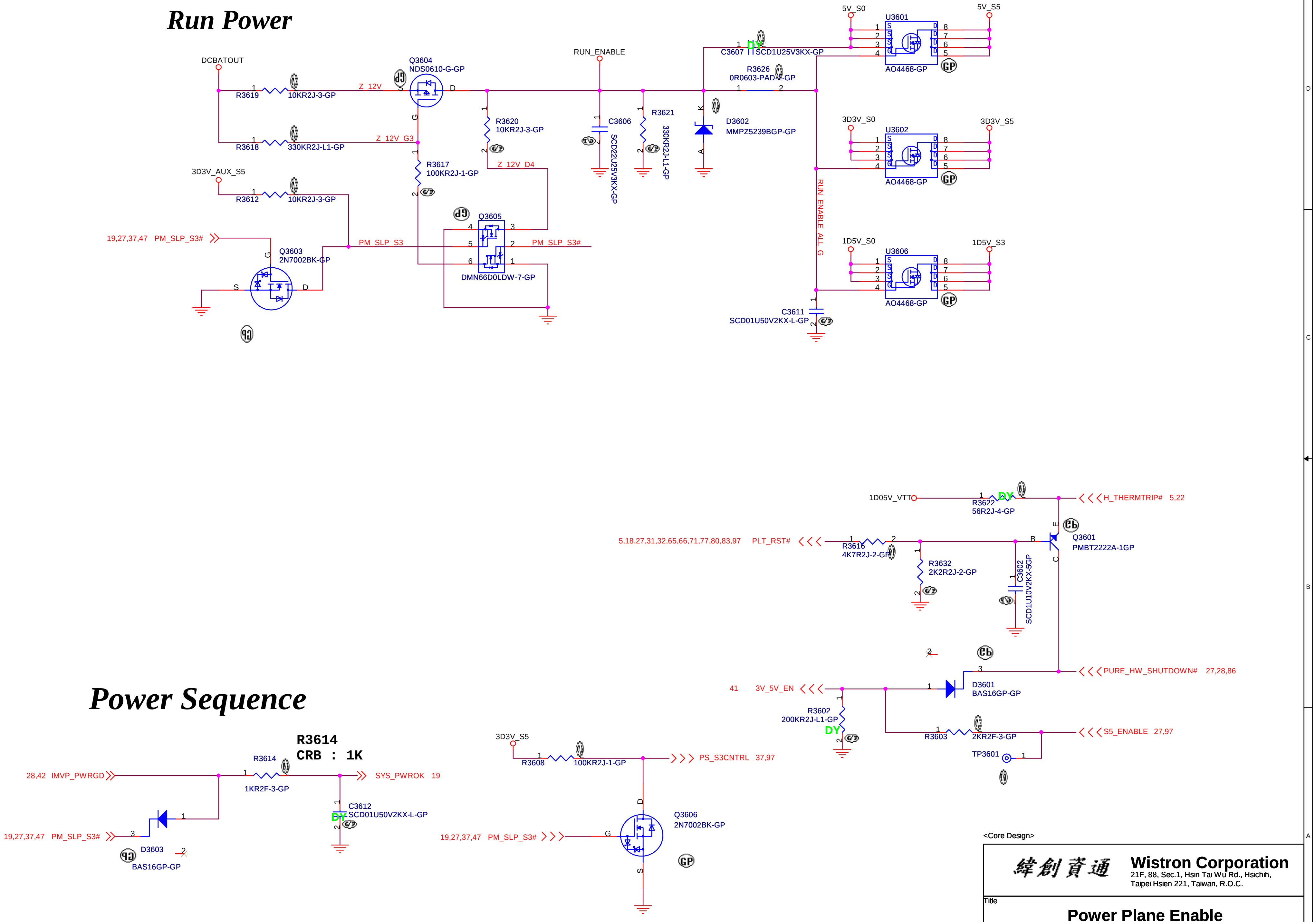
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0 Controller**		
Size: A4	Document Number: **LA480s**	Rev: **SA**
Date: Tuesday, March 06, 2012	Sheet 35 of 103	

Run Power

Power Sequence



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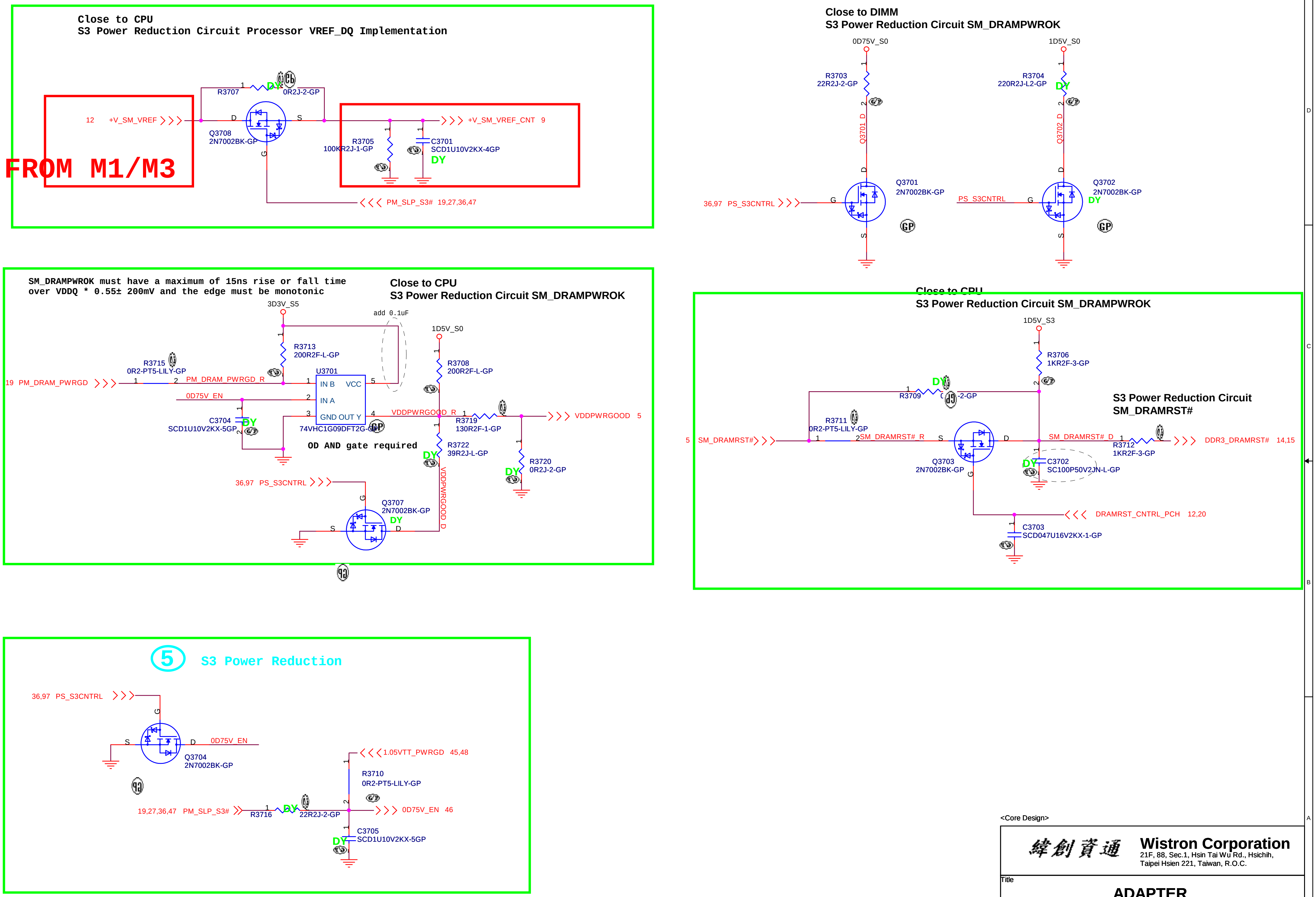
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Power Plane Enable**
Size A3 / Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 36 of 103

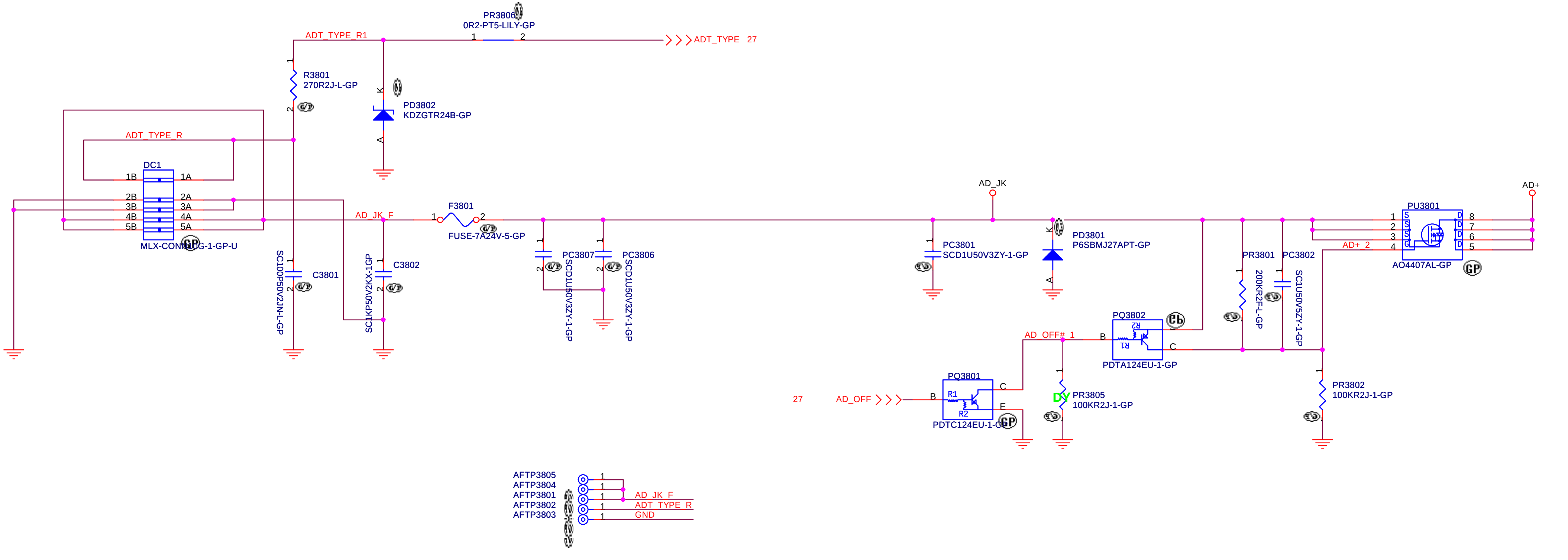


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ADAPTER		
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 37 of 103	

Adaptor in to generate DCBATOUT



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN_JACK	
Size A3	Document Number LA480s	Rev SA
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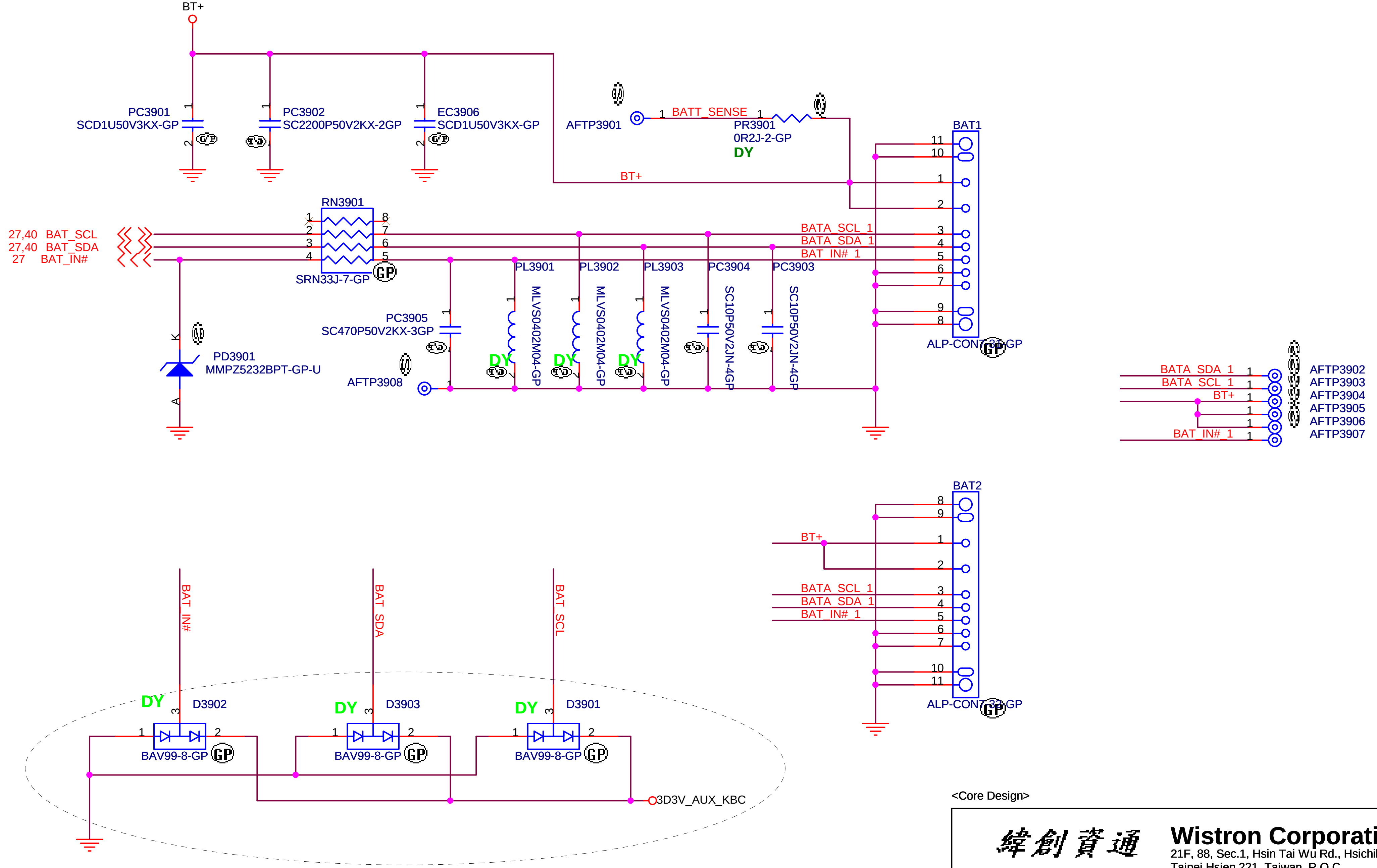
BATTERY CONNECTOR



<Core Design>

緯創資通 **Wistron Corporation**

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Title	BATT_CONN	
Size	Document Number: LA480s	Rev: SA
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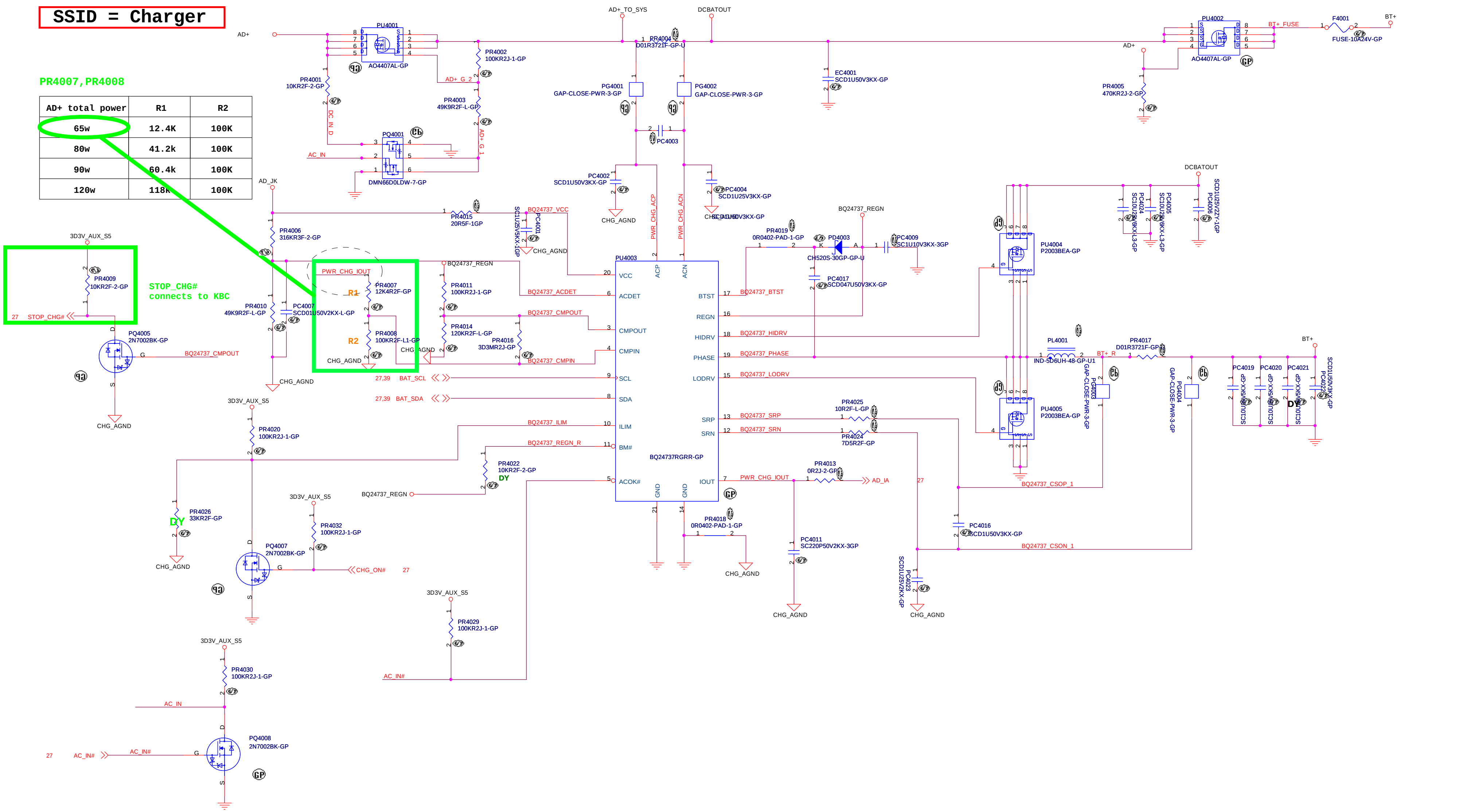
SSID = Charger

PR4007,PR4008

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K

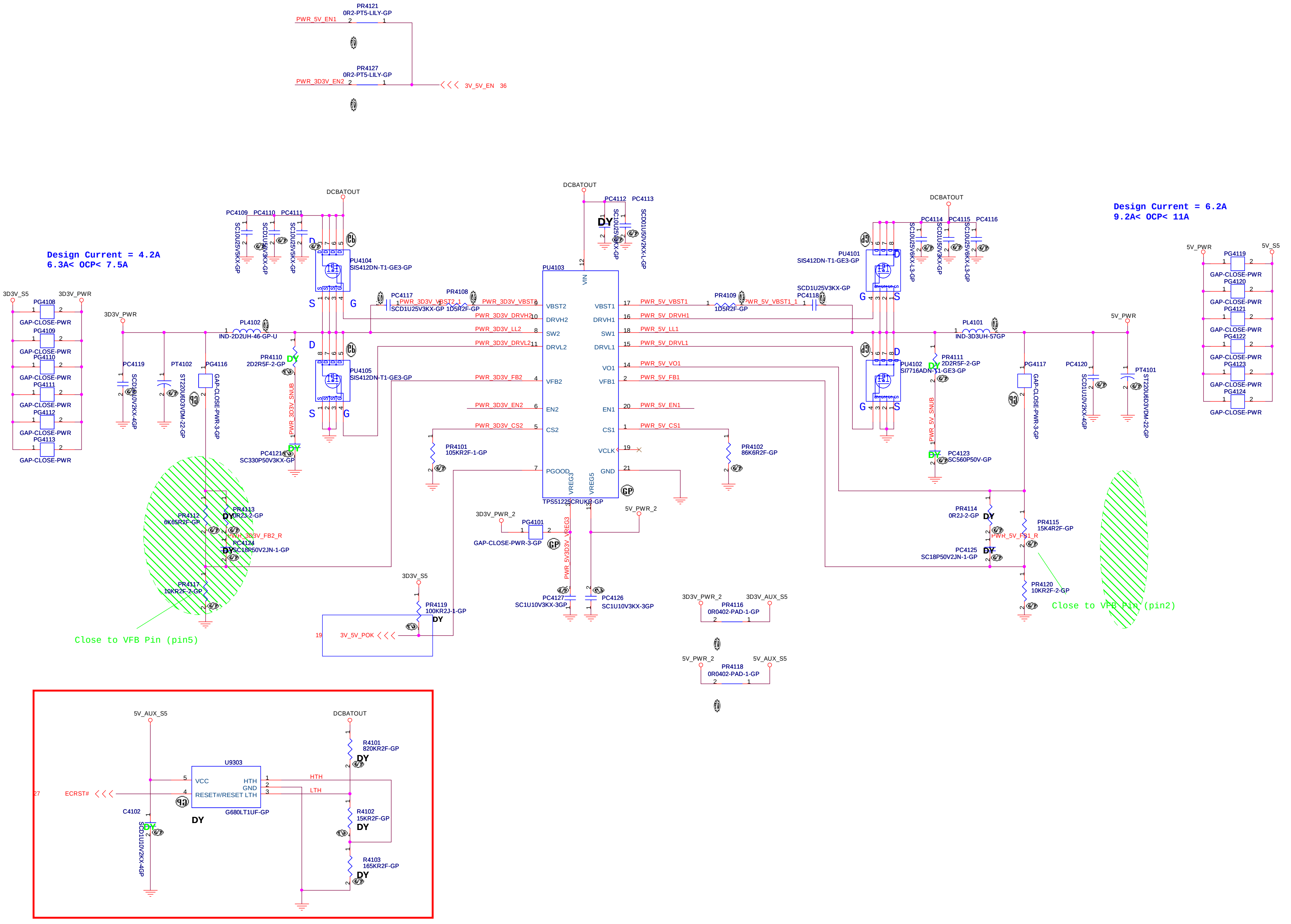


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CHARGER_BQ24737	
Size A2	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 40 of 103	

SSID = PWR.Plane.Regulator_5v3p3v



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
TPS51225_5V_3D3V		
Size A2	Document Number LA480s	Rev SA
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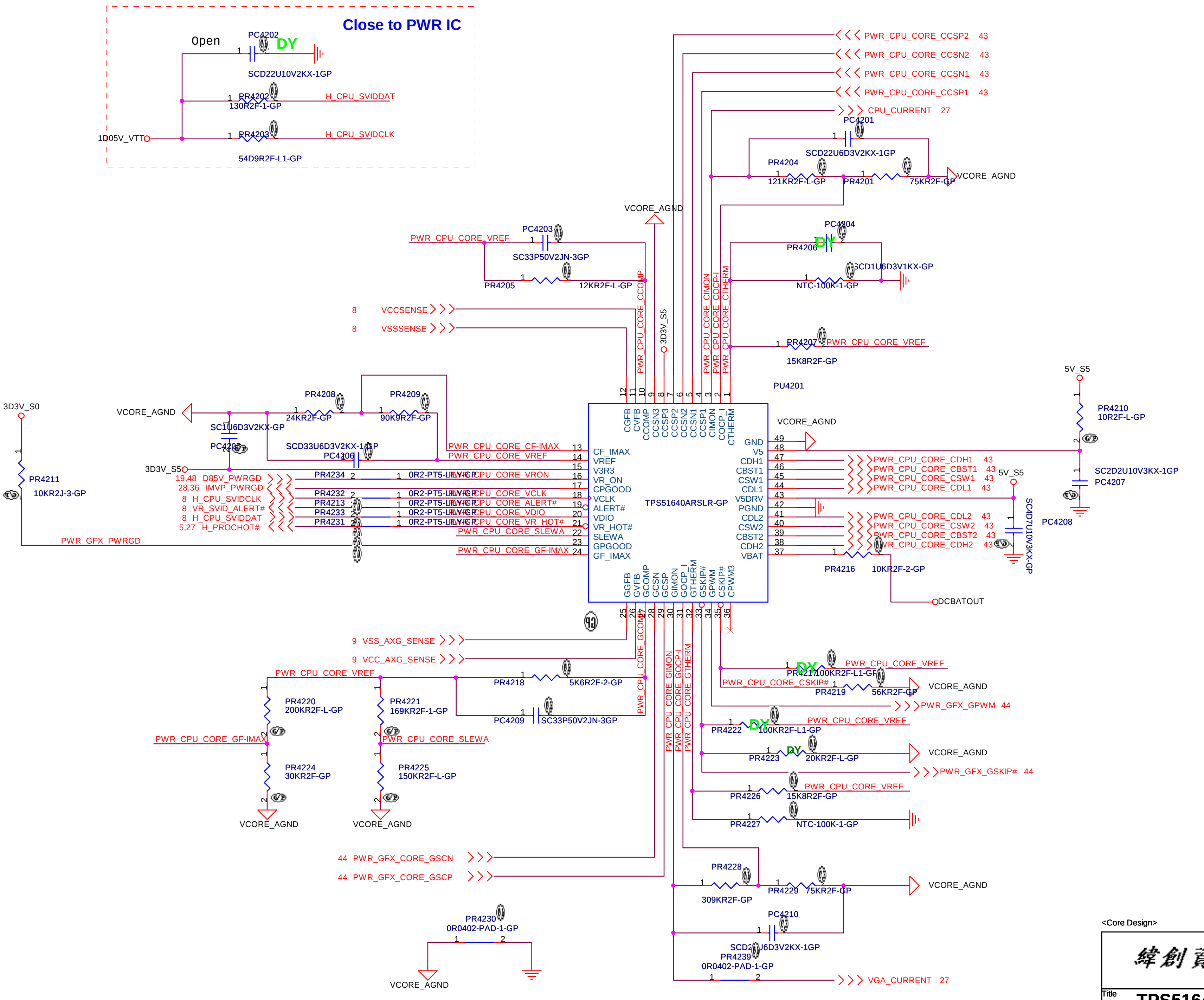

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	**TPS51640_CPU_CORE(1/3)**	
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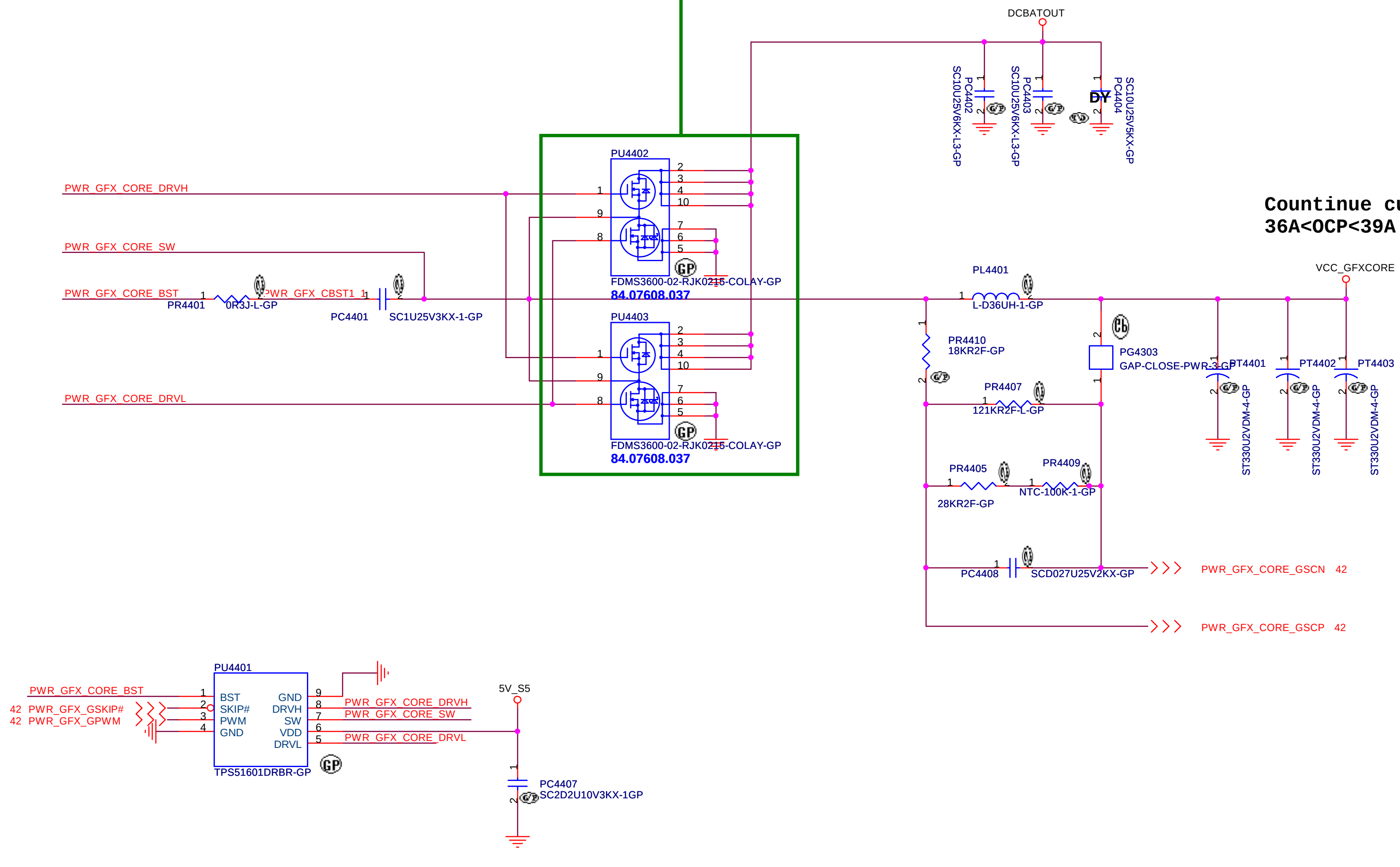
	Main source	2nd source
PU4402	84.03668.037 FDMS3668S	84.00031.037 RJK03P1DPA
PU4403	84.03668.037 FDMS3668S	84.00031.037 RJK03P1DPA

BOM control

Countinue current=21.5A
36A<OCP<39A



<Core Design>

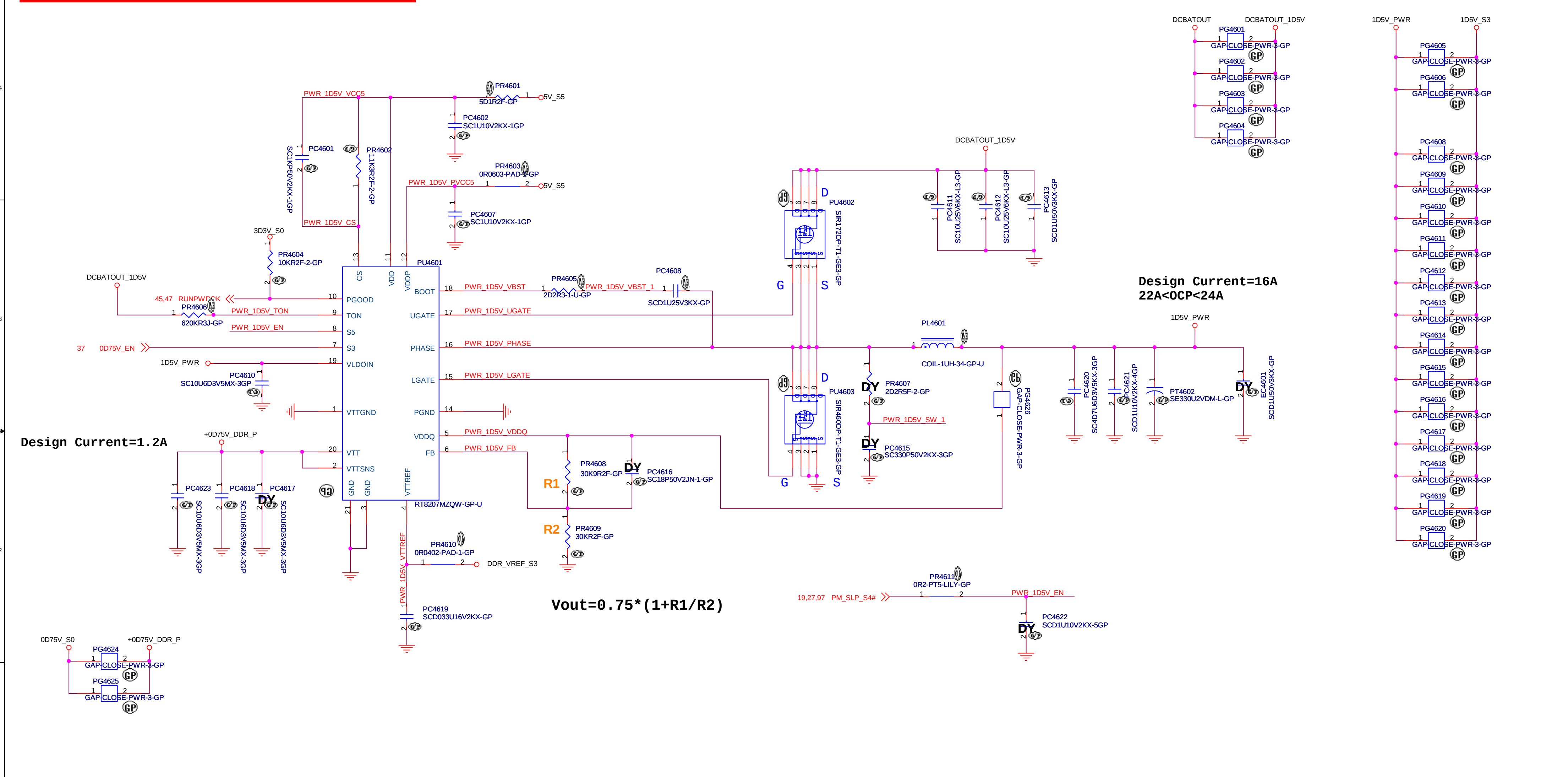
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51640_CPU_CORE(3/3)**

Size | Document Number: **LA480s** | Rev: **SA**

Date: Tuesday, March 06, 2012 | Sheet 44 of 103

SSID = PWR.Plane.Regulator_1p5v0p75v



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8207M_1D5V_0D75V
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Date:	Tuesday, March 06, 2012
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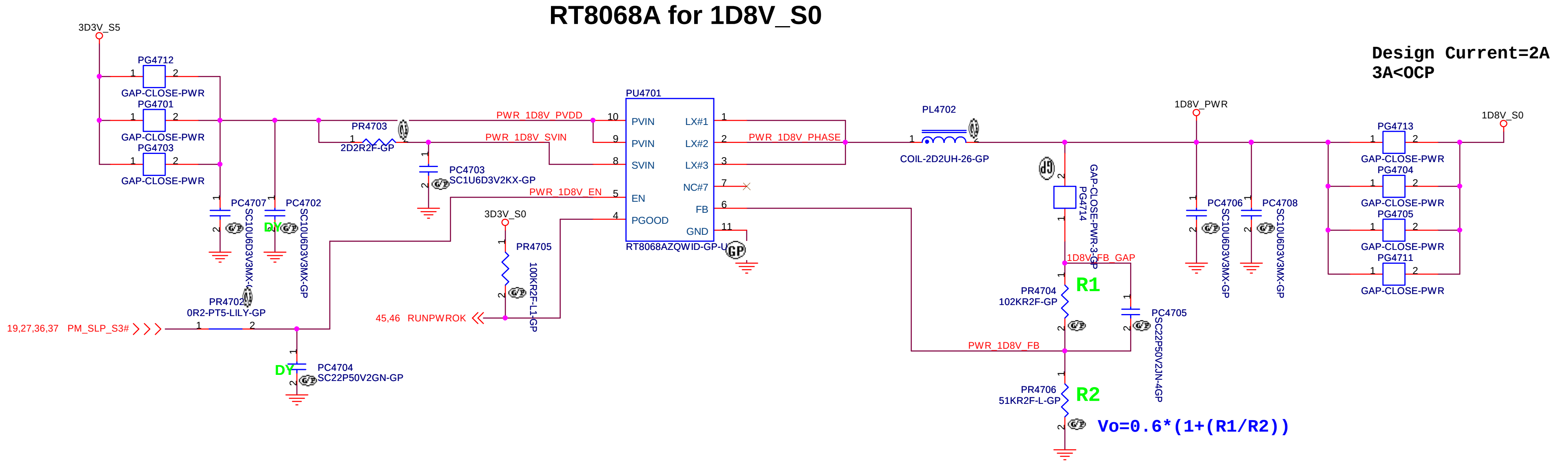
SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0

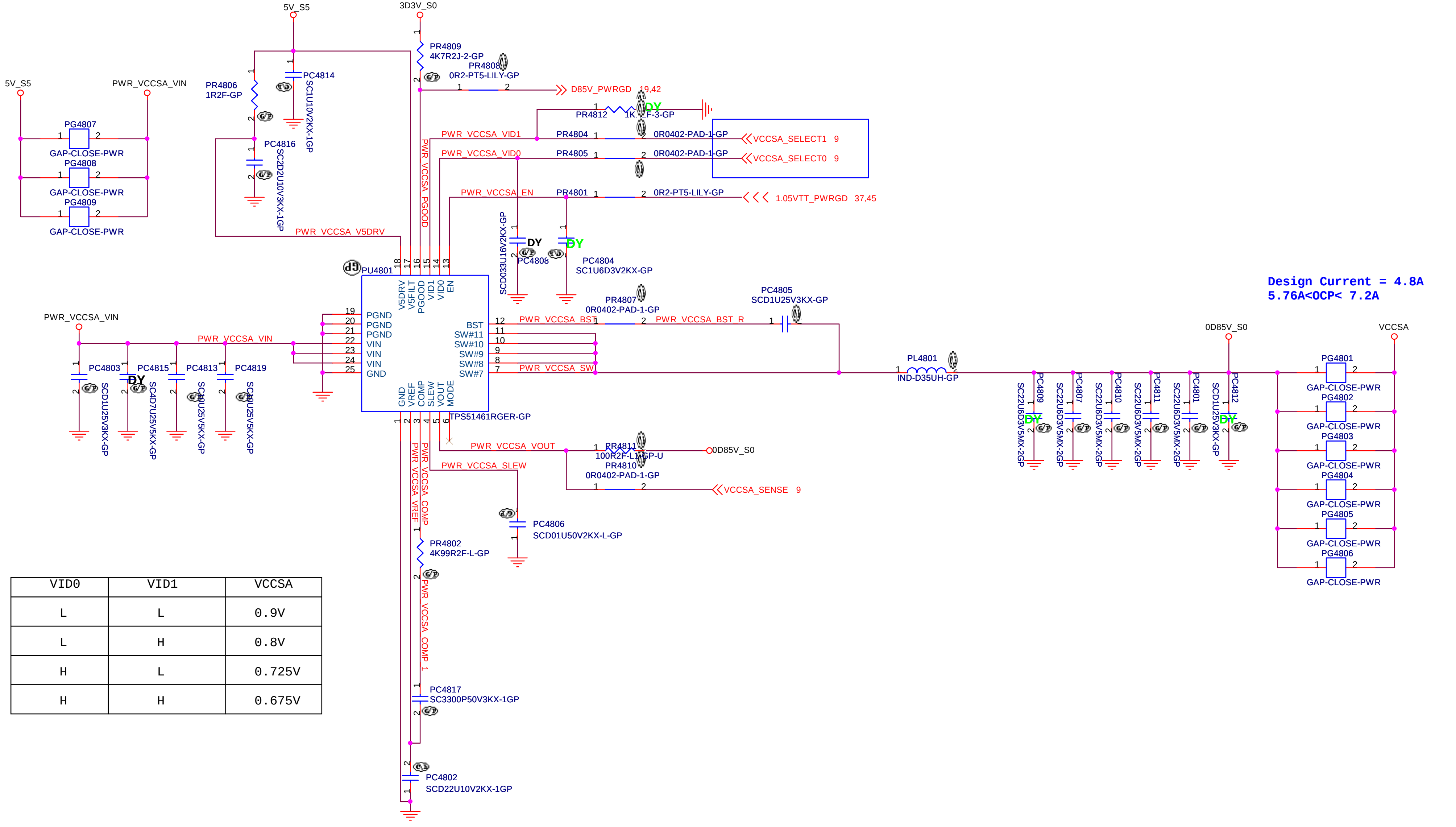


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWM_1D8V_RT8068		
Size	Document Number: LA480s		Rev: SA
Date: Tuesday, March 06, 2012		Sheet 47 of 103	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Core Design>

緯創資通 **Wistron Corporation**
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Title: VCCSA_TPS51461

Size | Document Number: LA480s | Rev: SA

Date: Tuesday, March 06, 2012 | Sheet 48 of 103

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Connector	
Size A4	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 50 of 103	

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**HDMI**	
Size A4	Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 51 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	eDP	
Size A4	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 52 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**S-VIDEO**	
Size A4	Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 53 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**		
Size A4	Document Number **LA480s**	Rev **SA**
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SSID = User.Interface

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**ITP**	
Size A4	Document Number **LA480s**	Rev **SA**
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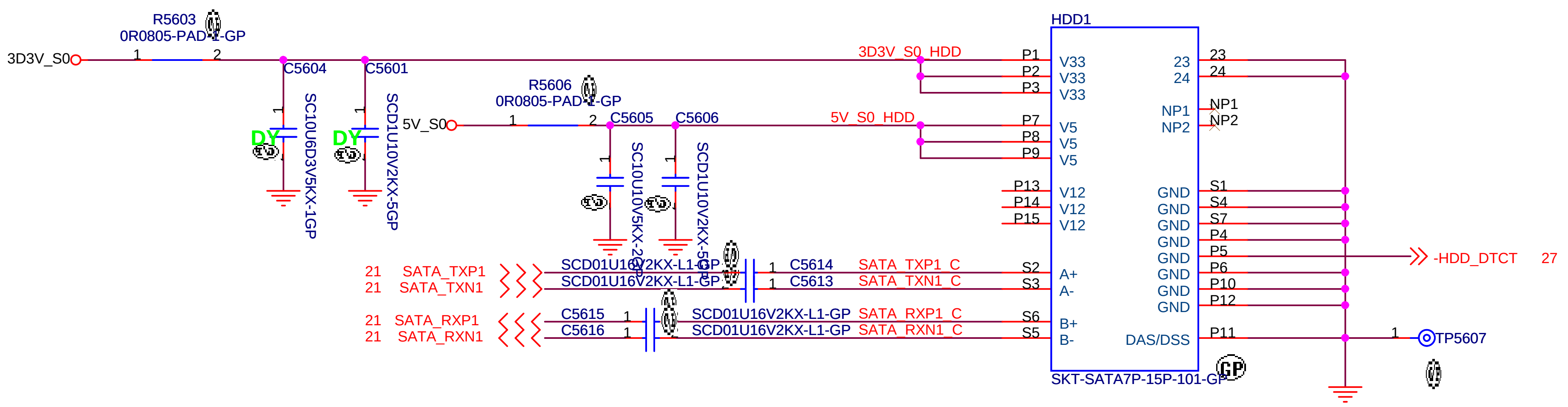
SATA HDD Connector



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD/ODD
Size	A4
Document Number	LA480s
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Date:	Tuesday, March 06, 2012
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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: E-SATA+USB		
Size: A4	Document Number: LA480s	Rev: SA
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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	**Audio Jack**	
Size A4	Document Number **LA480s**	Rev **SA**
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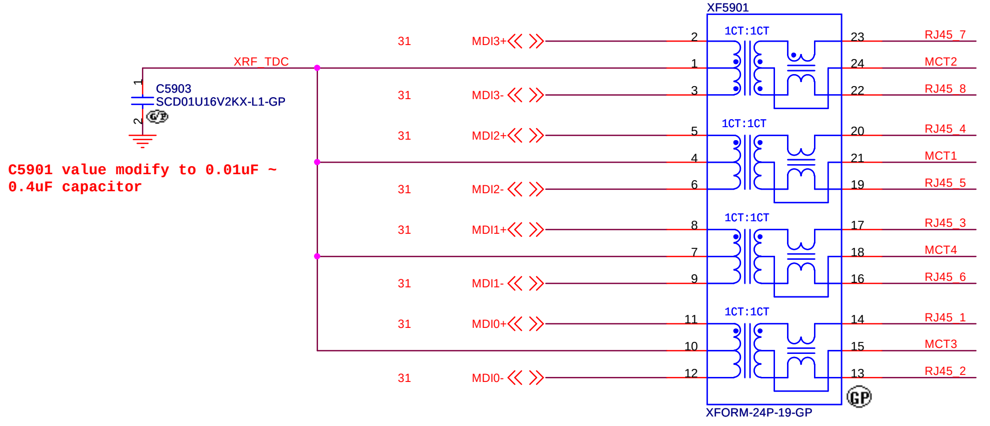
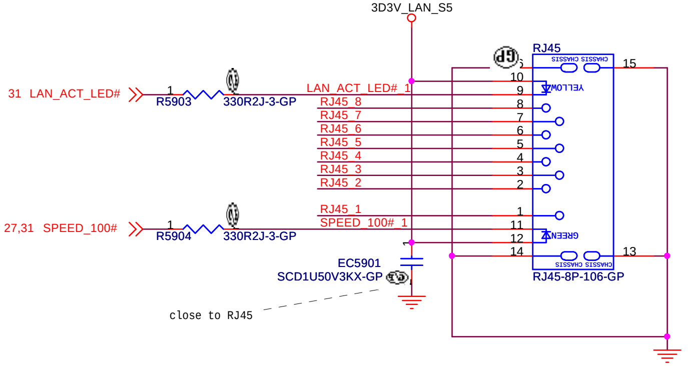
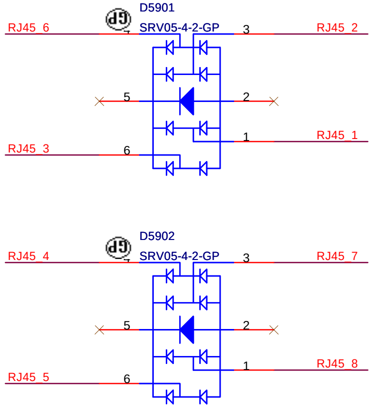
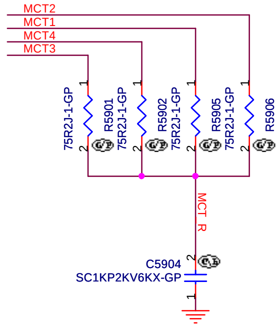
GIGA Lan Transformer

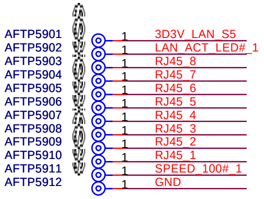


LAN Connector









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緯創資通 **Wistron Corporation**
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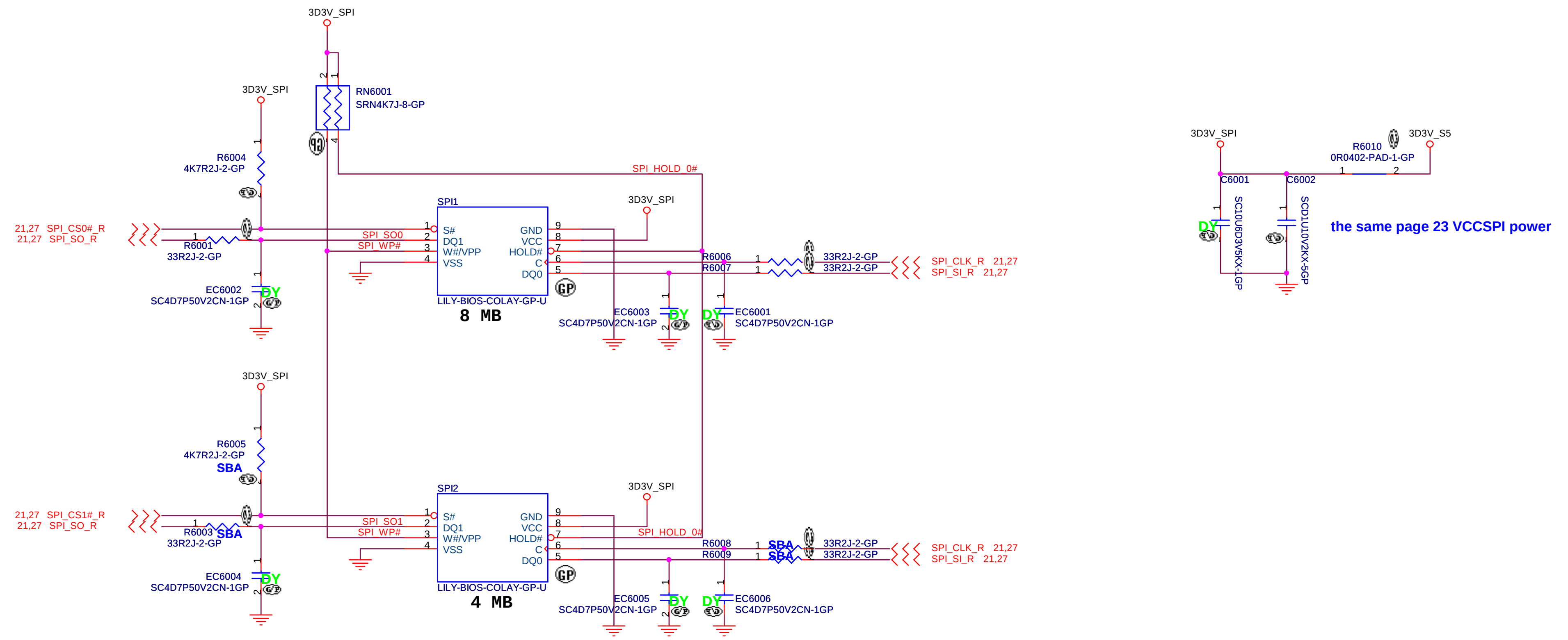
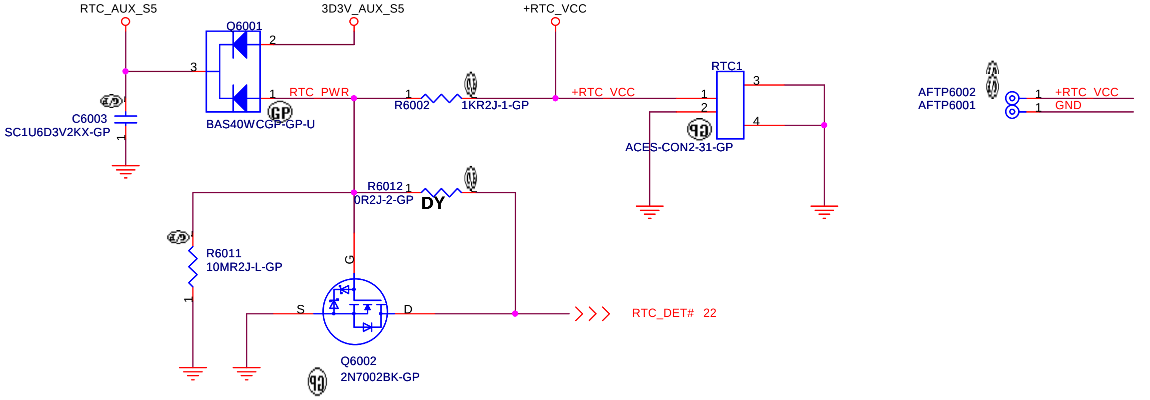
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RJ45 / Transformer		
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 59 of 103	

SSID = Flash.ROM



SSID = RBATT



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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash/RTC		
Size A3	Document Number LA480s		Rev SA
Date: Tuesday, March 06, 2012	Sheet 60 of 103		

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Connector**		
Size: A4	Document Number: **LA480s**	Rev: **SA**
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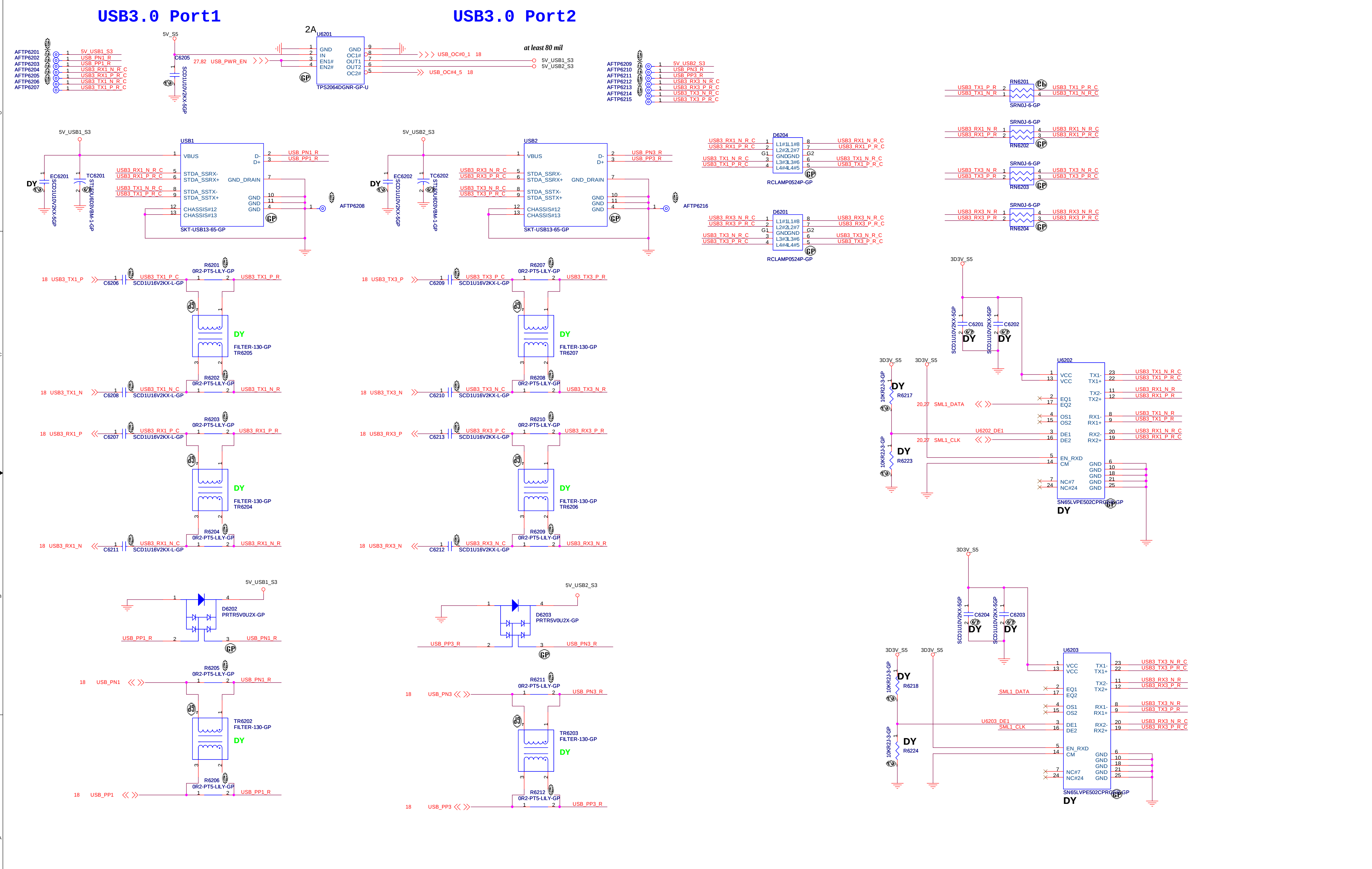

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB 3.0 Port*2		
Size A2	Document Number LA480s	Rev SA
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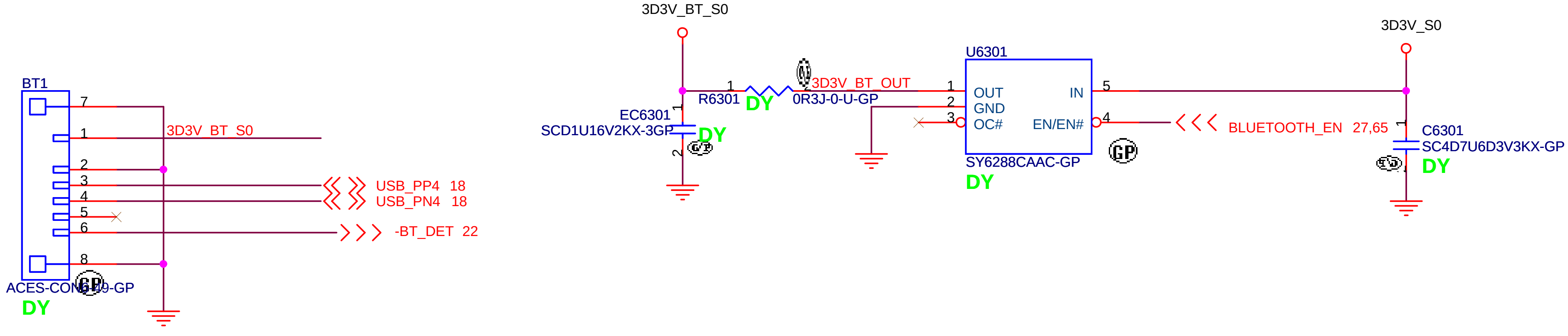
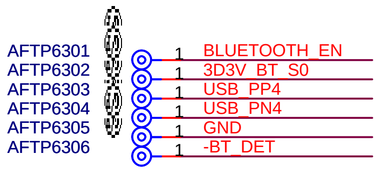
SSID = User.Interface

Bluetooth conn.





	BT CONN.	WLAN CONN.
BT1	**ASM**	**DY**
R6301	**ASM**	**DY**
U6301	**ASM**	**DY**
C6301	**ASM**	**DY**

<Core Design>

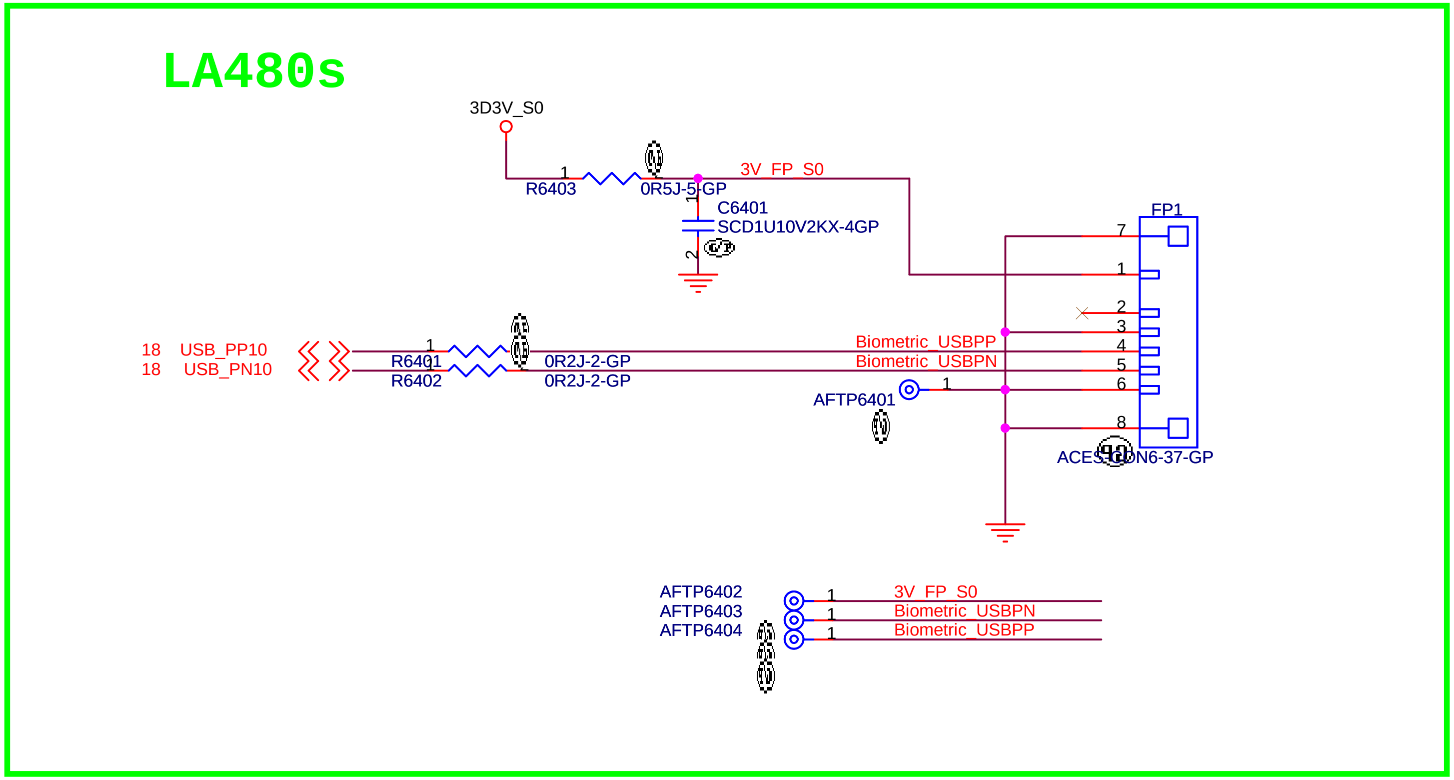
緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Bluetooth**

Size: A4 | Document Number: **LA480s** | Rev: **SA**

Date: Tuesday, March 06, 2012 | Sheet 63 of 103



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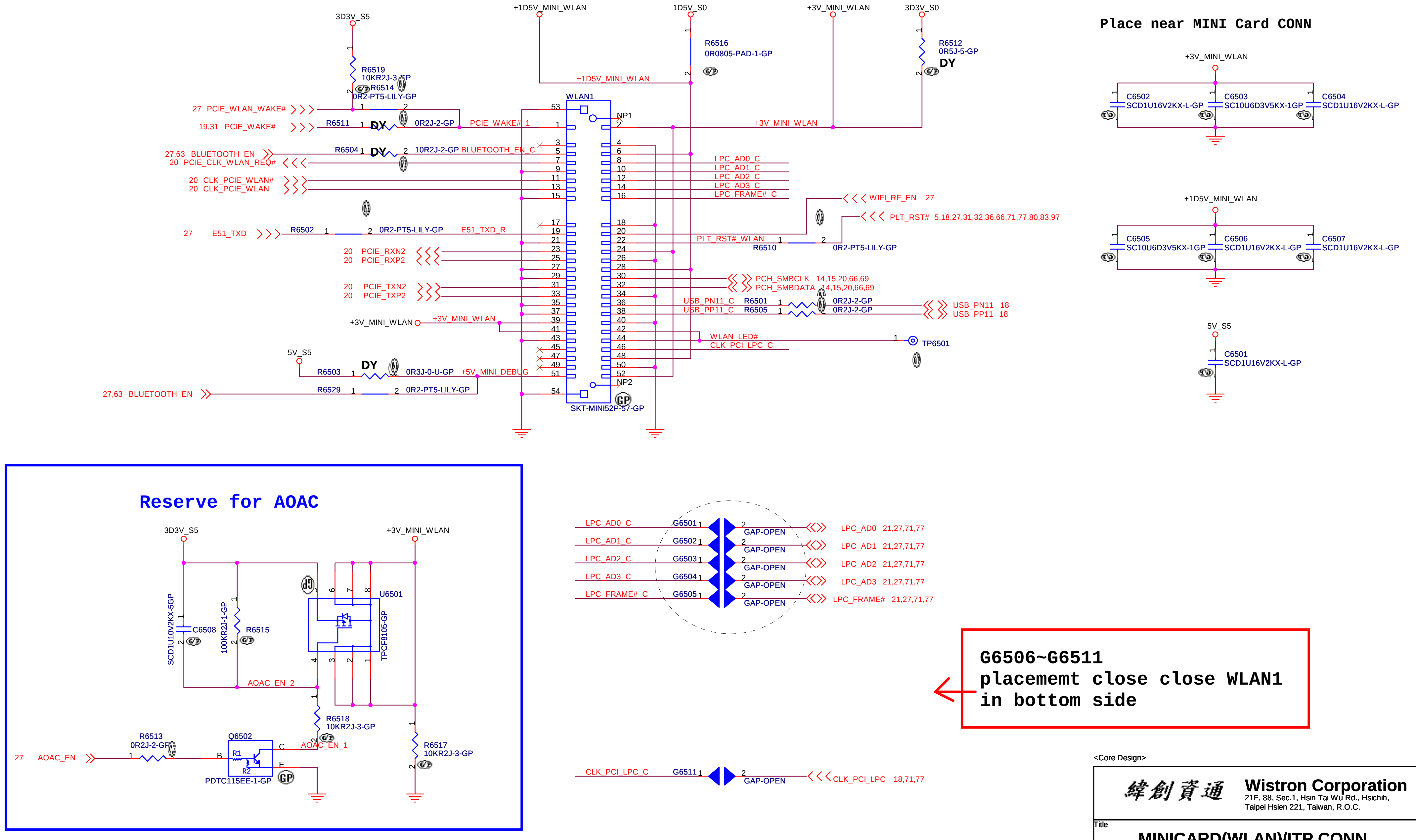
緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Finger Printer Connector**	
Size A4	Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 64 of 103	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



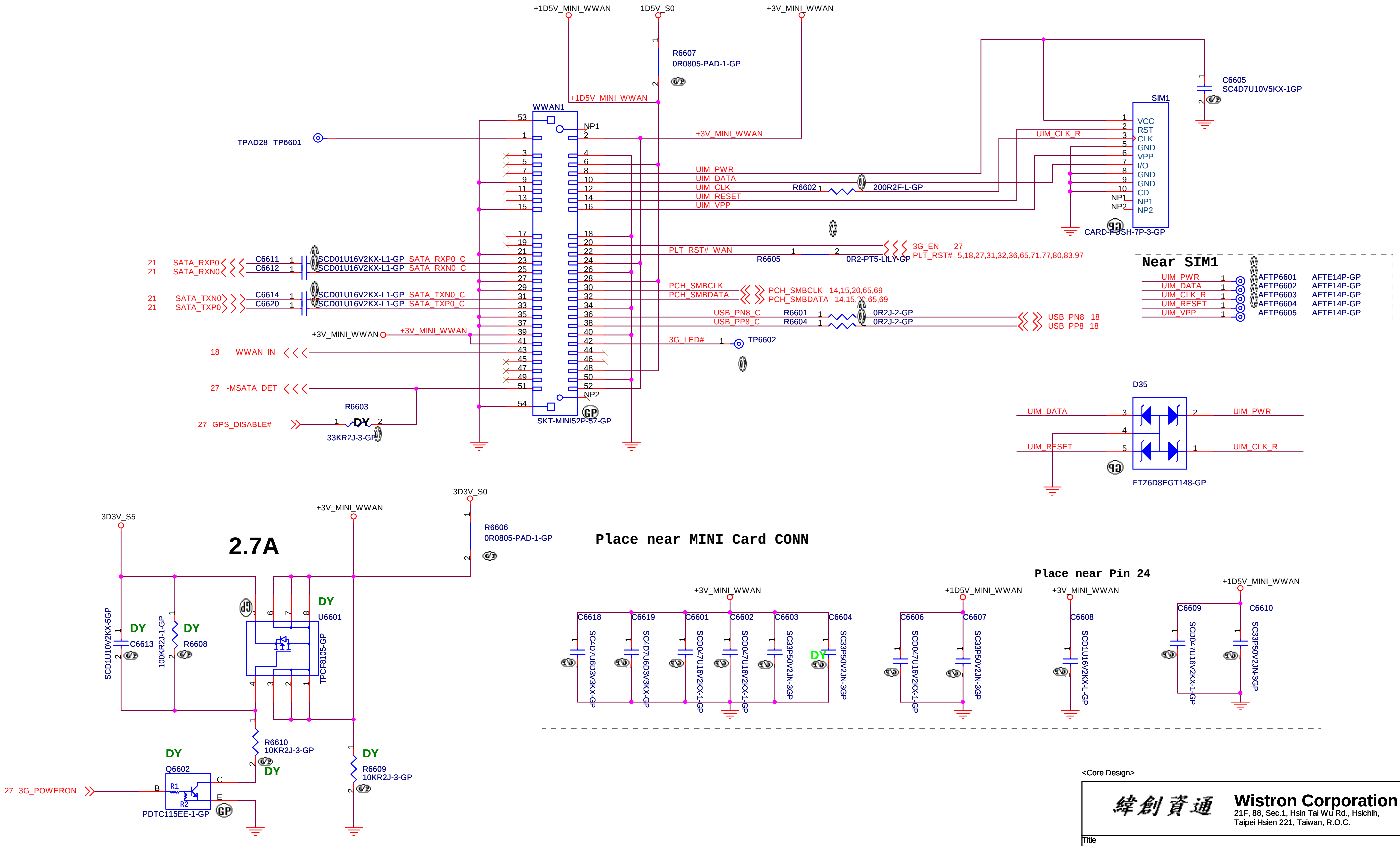
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINICARD(WLAN)/ITP CONN	
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 65 of 103	

SSID = Wireless

Mini Card Connector(Full Card)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**WWAN Connector**	
Size A3	Document Number **LA480s**	Rev **SA**
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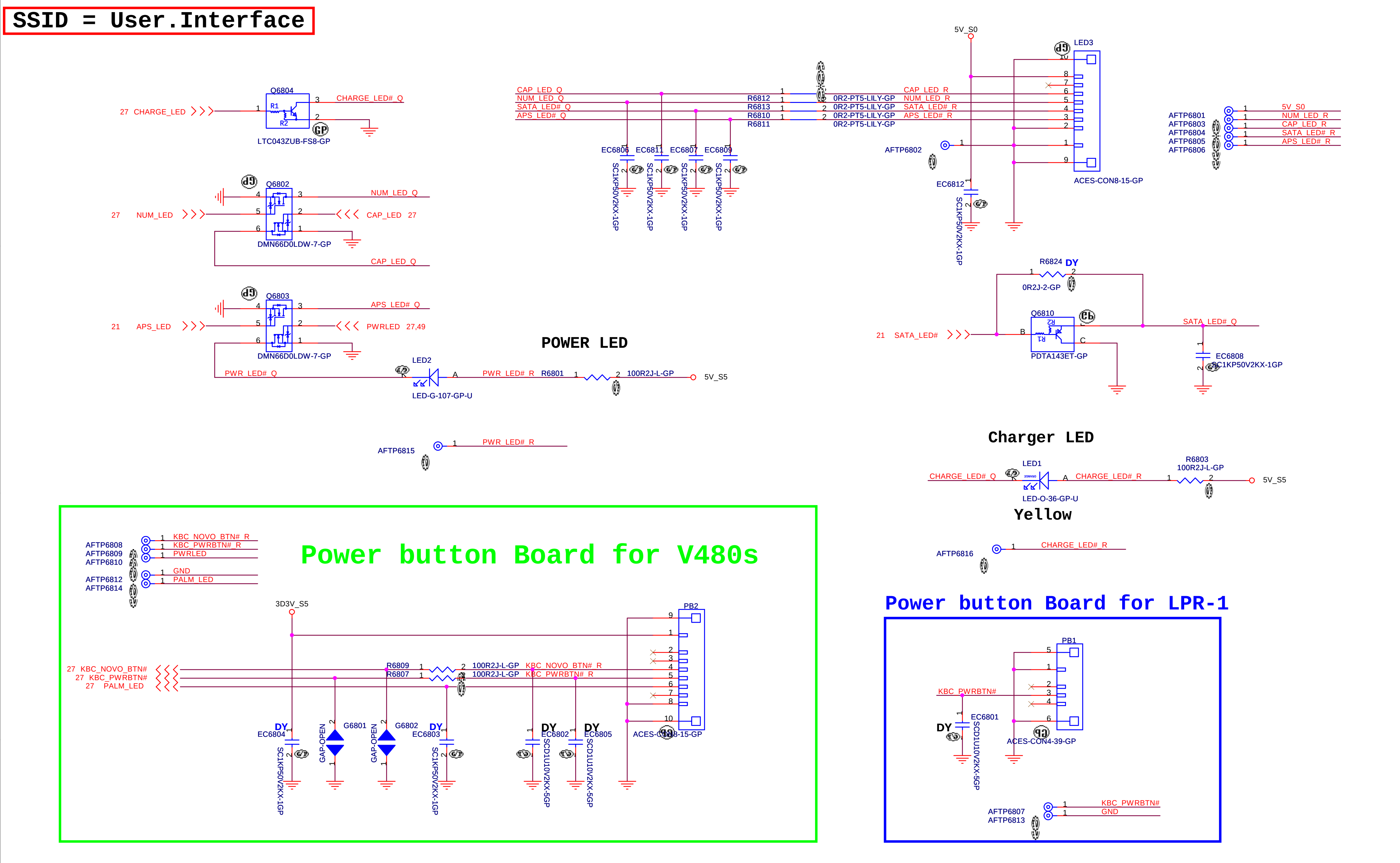
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Reserved**	
Size A4	Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 67 of 103	



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緯創資通 **Wistron Corporation**
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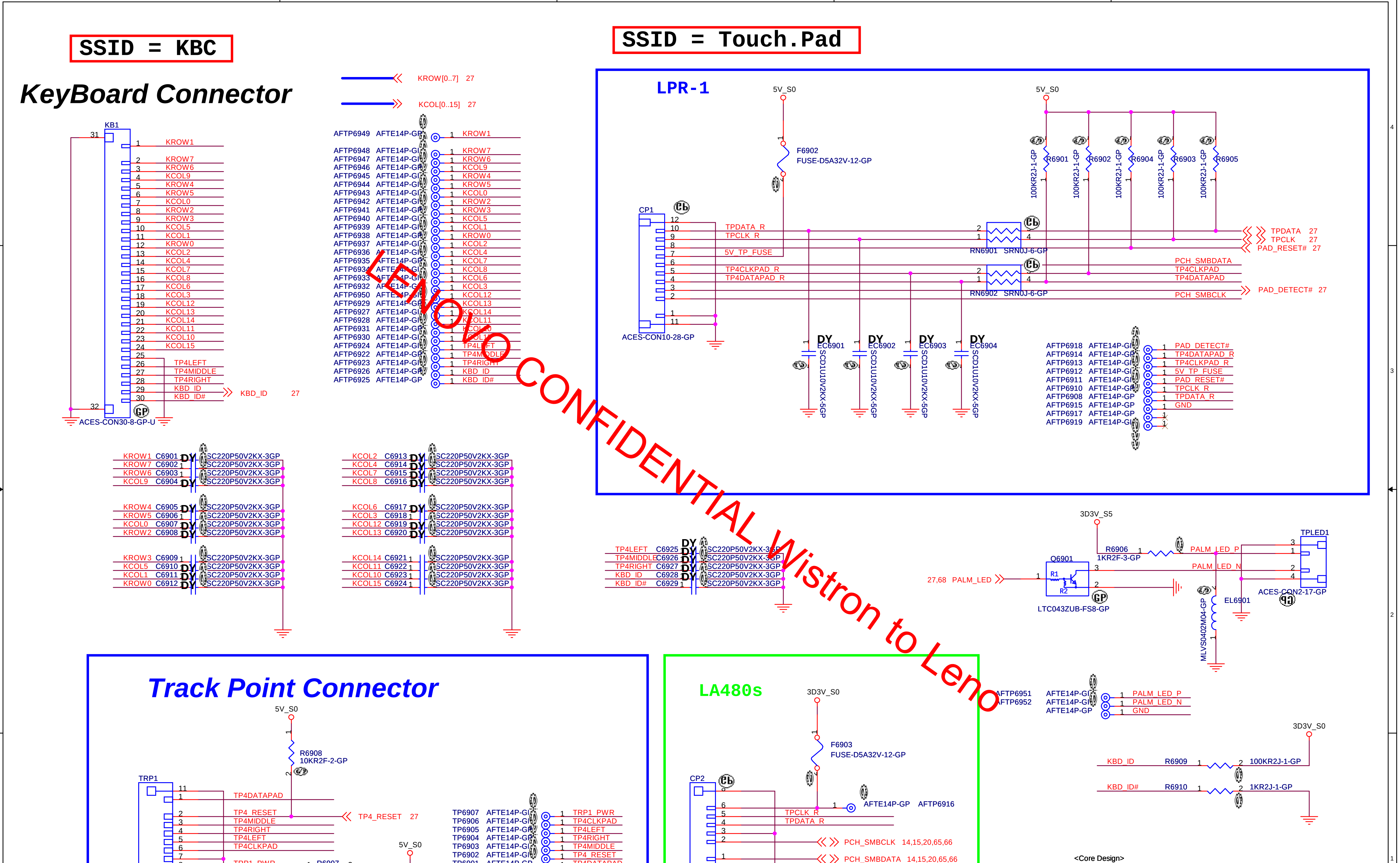
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED Bard/Power Button		
Size A3	Document Number LA480s		Rev SA
Date: Wednesday, March 07, 2012		Sheet 68 of 103	



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	TOUCH PAD CONNECTOR	
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 69 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**

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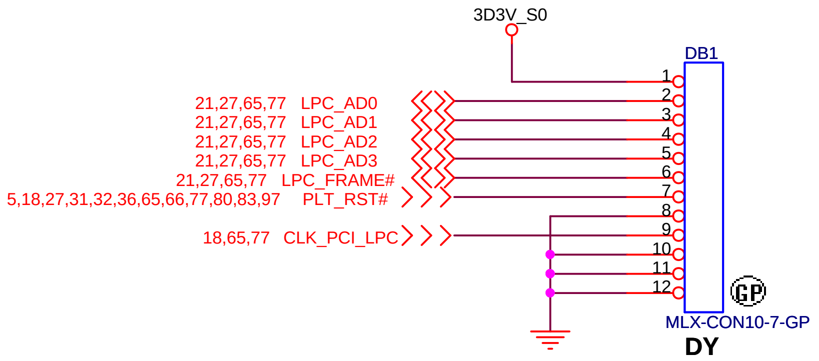
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Hall Sensor**	
Size A4	Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 70 of 103	

5 4 3 2 1



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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	**Dubug connector**	
Size A4	Document Number **LA480s**	Rev **SA**
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Title: **Reserved**		
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size A4	Document Number LA480s	Rev SA
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<Core Design>

緯創資通 **Wistron Corporation**
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Title	**CARD Reader CONN**	
Size A4	Document Number **LA480s**	Rev **SA**
Date: Tuesday, March 06, 2012	Sheet 74 of 103	

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	New Card	
Size A4	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 75 of 103	

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size A4	Document Number LA480s	Rev SA
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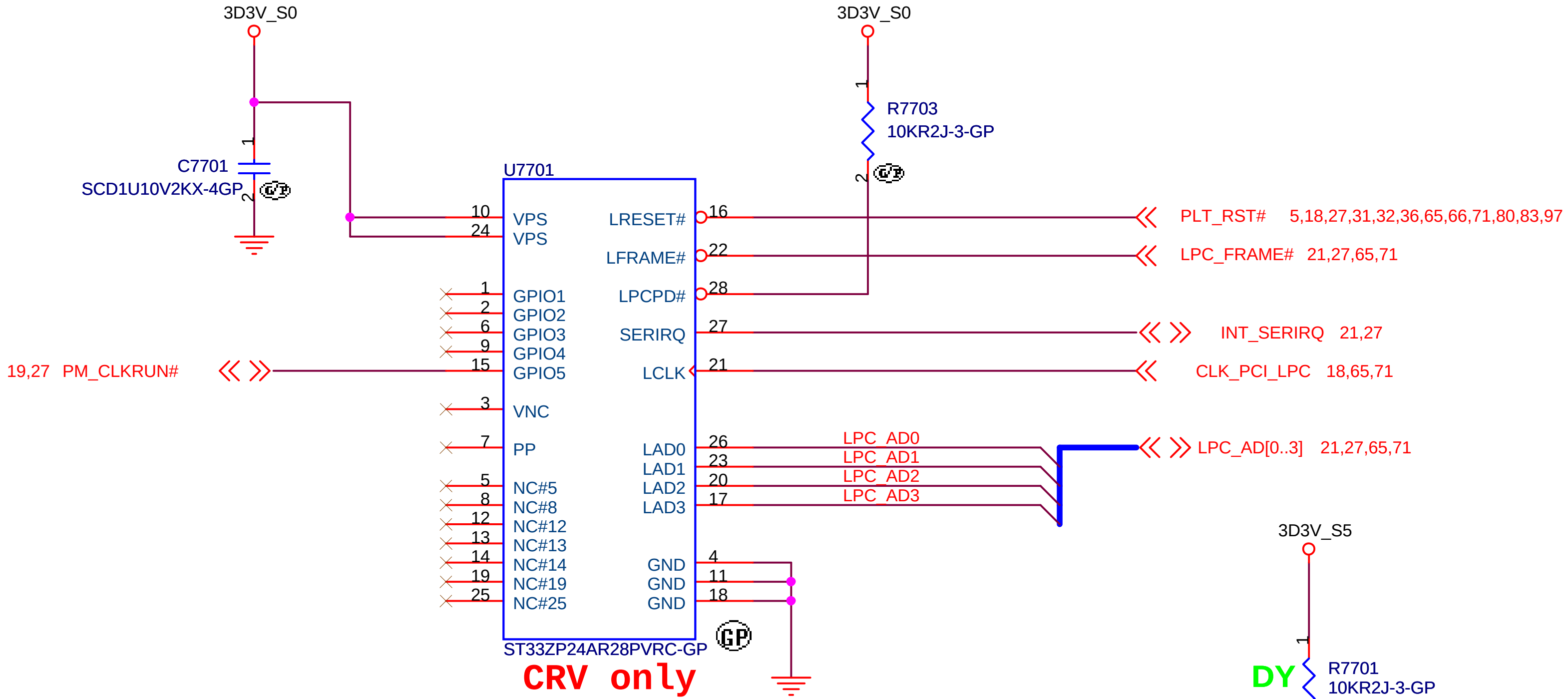

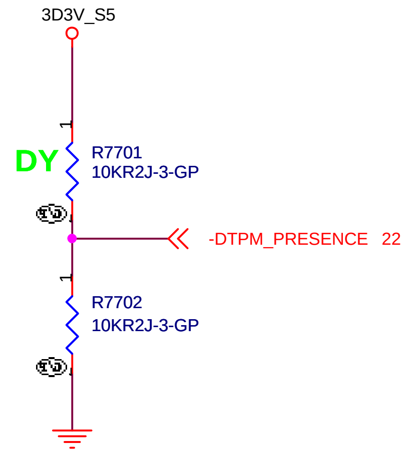

	NO TPM	ST Micro ST33ZP24AR28PVRC
U7701	DY	ASM
C7701	DY	ASM
R7703	DY	ASM
R7701	ASM	DY
R7702	DY	ASM

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Title: **Reserved**

Size: A4 | Document Number: **LA480s** | Rev: **SA**

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	**Reserved**		
Size A4	Document Number **LA480s**		Rev **SA**
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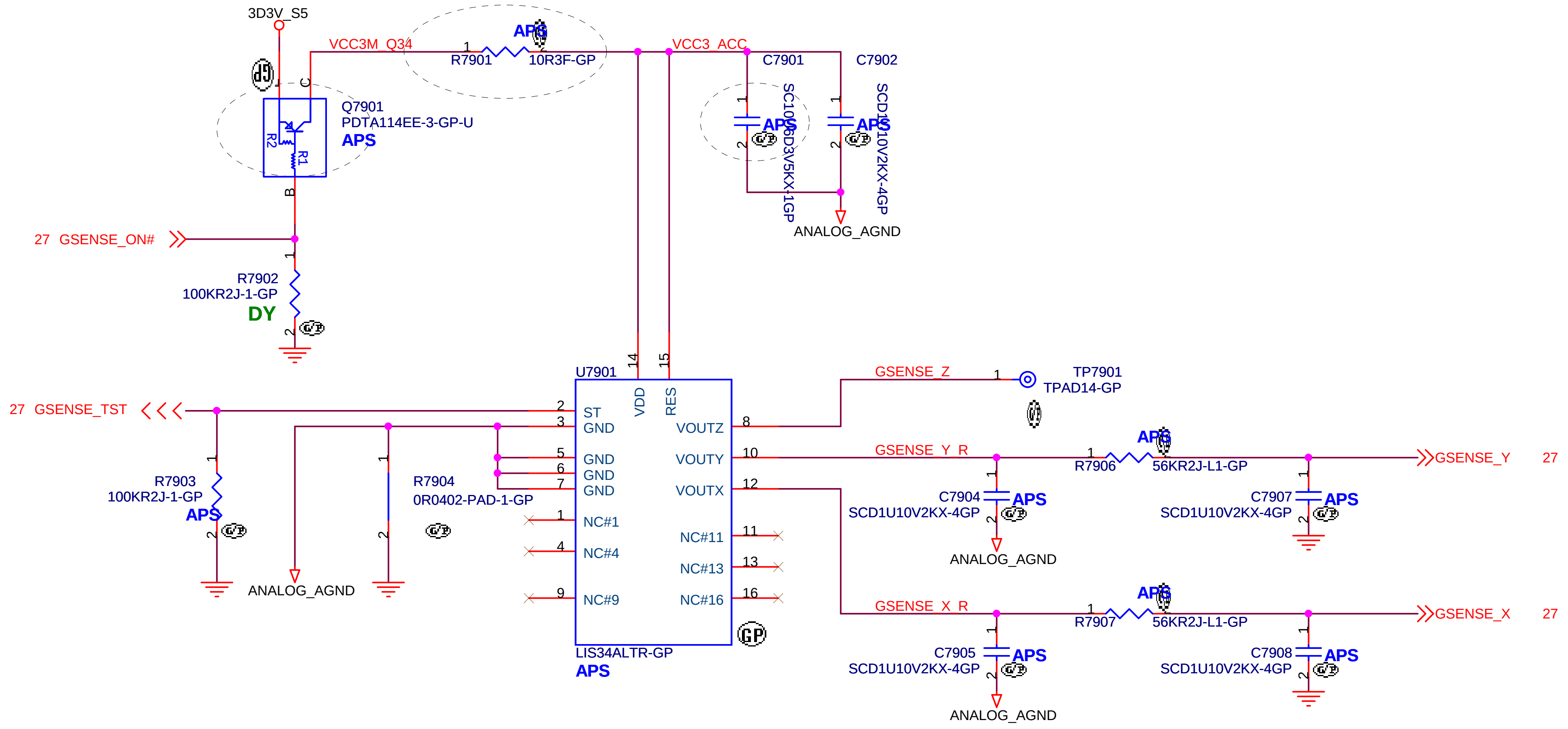

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Title		
G-Sensor		
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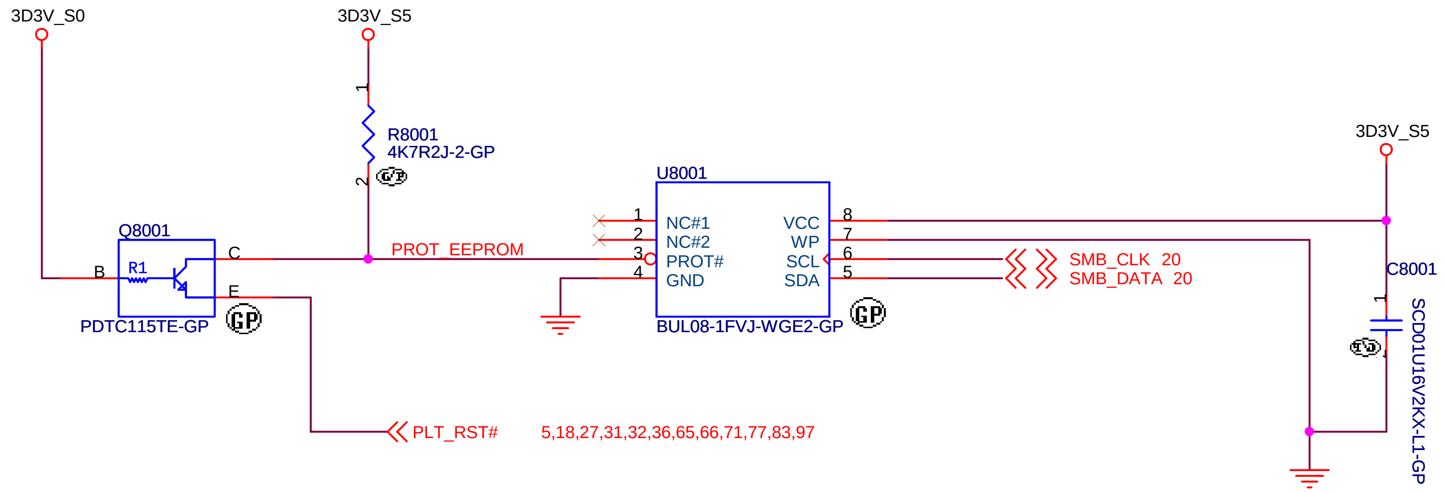
RFID



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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	**Reserved**	
Size A4	Document Number **LA480s**	Rev **SA**
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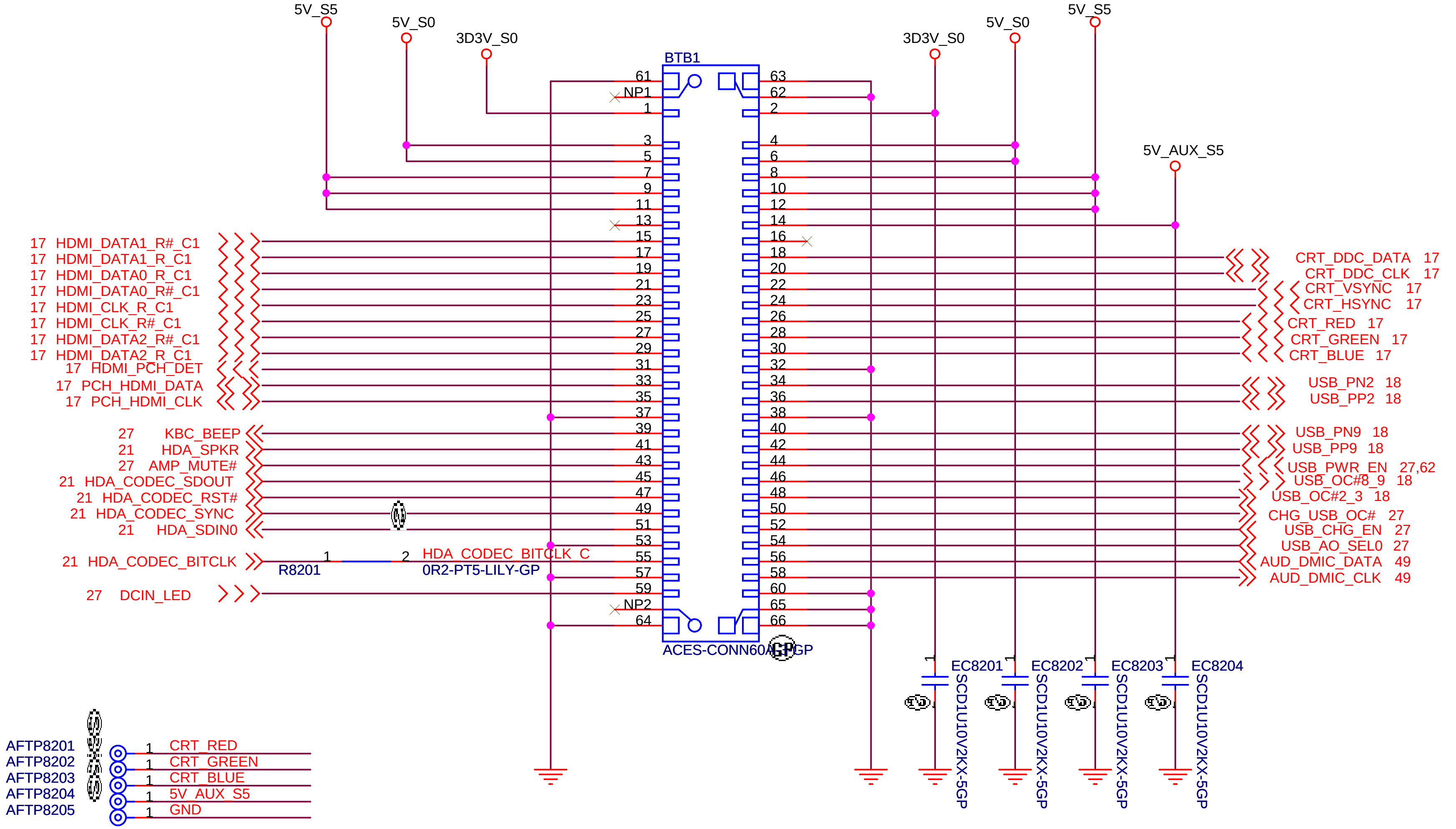
Title: **Reserved**		
Size: A4	Document Number: **LA480s**	Rev: **SA**
Date: Tuesday, March 06, 2012	Sheet 81 of 103	



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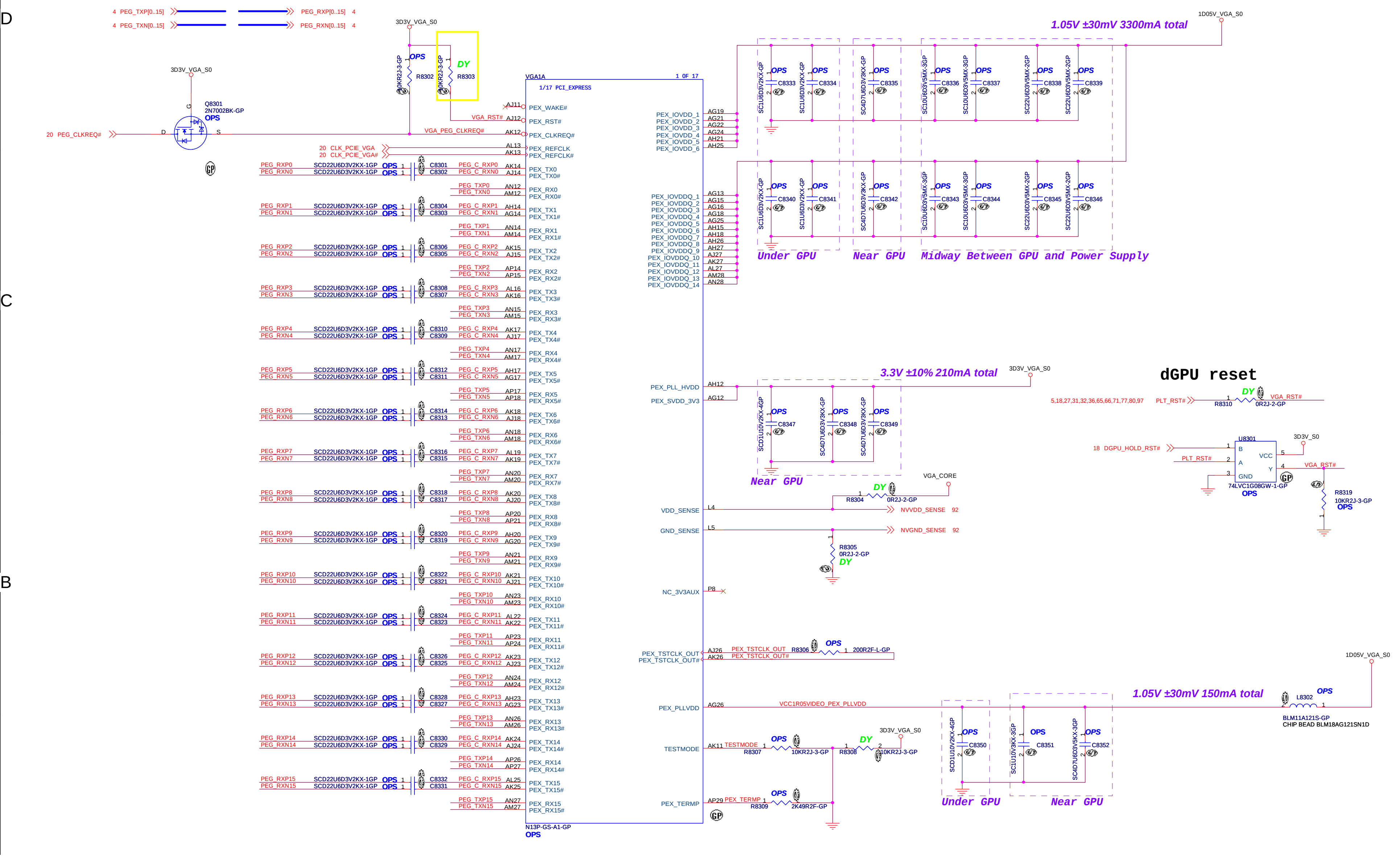
Taipei Hsien 221, Taiwan, R.O.C.

Title		
IO Board Connector		
Size A4	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 82 of 103	



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緯創資通 **Wistron Corporation**
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	**N13P_GPU (1/5): PEG**	
Size A2	Document Number **LA480s**	Rev **SA**
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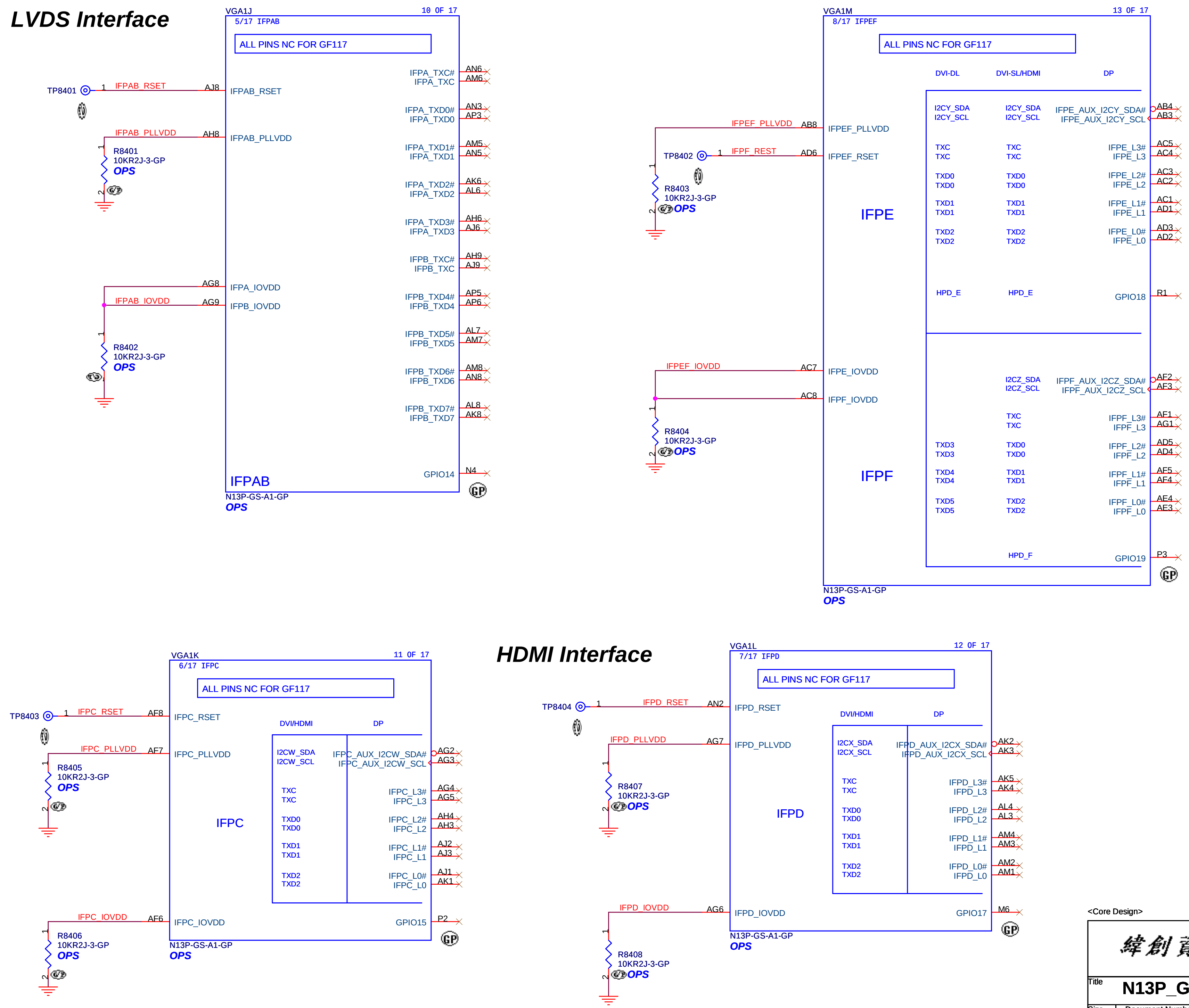

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緯創資通 **Wistron Corporation**
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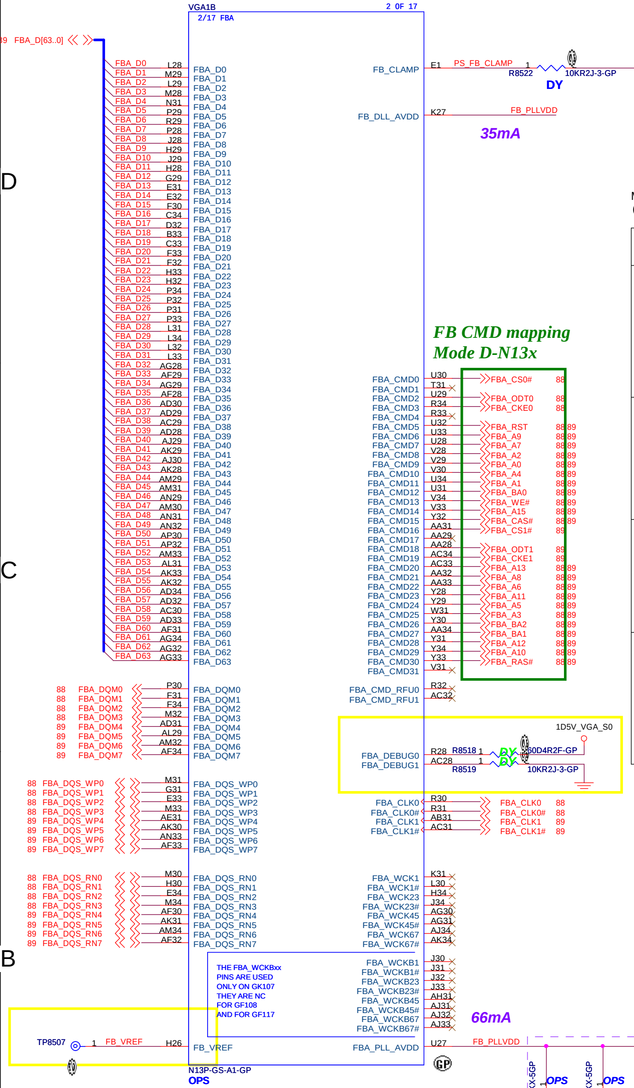
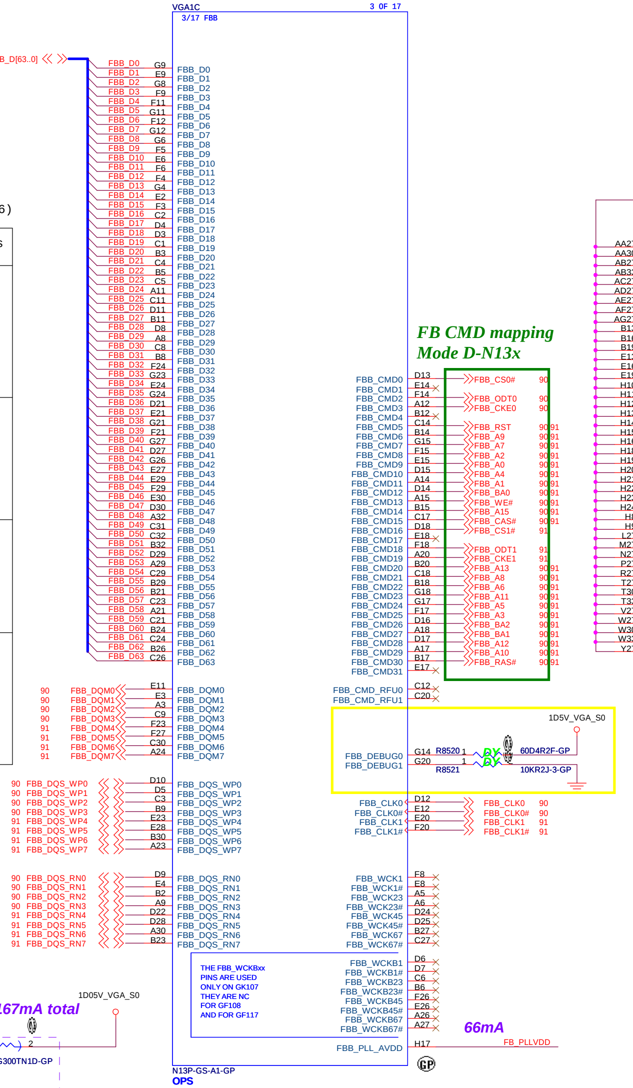
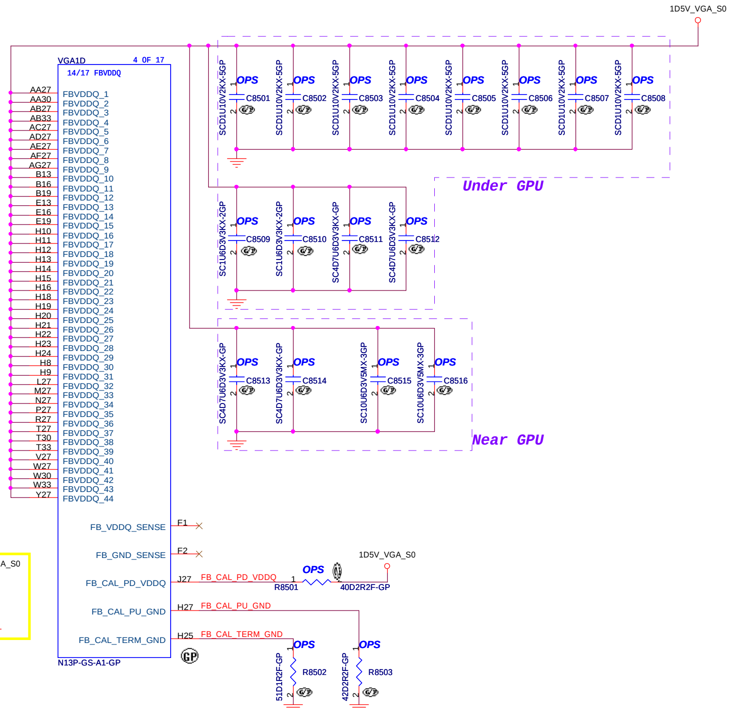
Title	N13P_GPU (2/5): DIGITALOUT	
Size A3	Document Number LA480s	Rev SA
Date: Tuesday, March 06, 2012	Sheet 84 of 103	



Mode D Command Mapping
(DG-05587-001_v03_p.78_Table 16)

N13x DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		

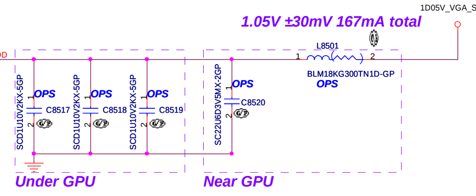


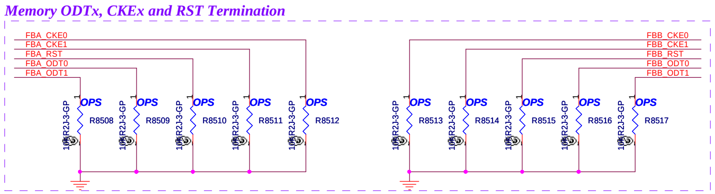


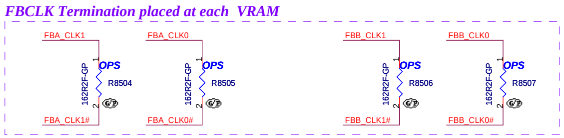
Default GPU Drive Calibration for DDR3 (DG-05587-001_v03_p.82_Table 17)

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PU_VDDQ	FBCAL_TERM_GND
DDR3	1.5V	42.2Ω	40.2Ω	51.1Ω

*Use only 1% resistors for driver calibration.







<Core Design>

Wistron Corporation
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Title: N13P_GPU (3/5): VRAM I/F

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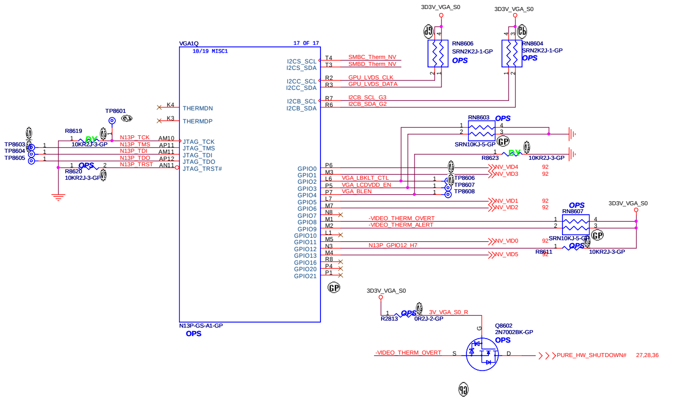
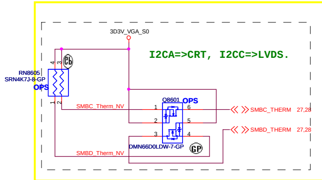
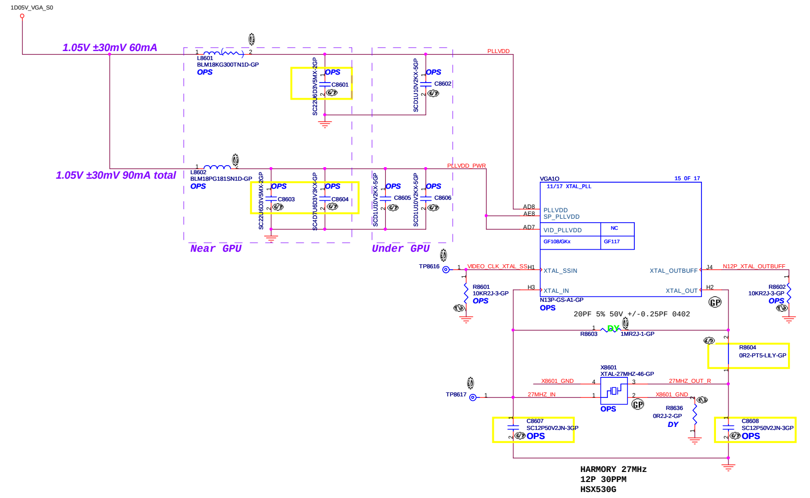
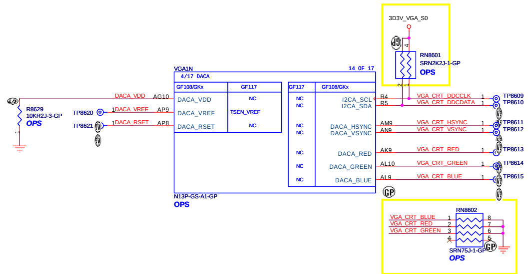






GPIO Description (DG-05587-001_v03_p.82_Tale 98)

GPIO pin Name	Normal Function	I/O	Function Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlught PWM Brightness Control
GPIO3	LCD_VCC	O	Panel Power Enable
GPIO4	LCD_BLEN	O	panel Backlight Enale
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC Power Detect Input. High = AC, Low = Battery
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plog Detect for IFPAB
GPIO15	HPD_C	I	Hot Plog Detect for IFPC
GPIO16	MEM_VDD_CTL	O	Memory VDD VID
GPIO17	HPD_D	I	Hot Plog Detect for IFPD
GPIO18	HPD_E	I	Hot Plog Detect for IFPE
GPIO19	HPD_F	I	Hot Plog Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		



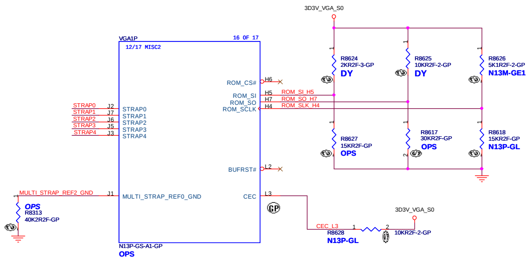


	TABLE NVIDIA	N12P-GL DEV ID: 0x0DE9	N12M-GE1 DEV ID: 0x1058
ROM_SO	R8617	10Kohm 64.10025.6DL	30Kohm 64.30025.6DL

	TABLE NVIDIA	N12P-GL DEV ID: 0x0DE9	N12M-GE1 DEV ID: 0x1058
ROM_SCLK	R8626	DY	5Kohm 64.51015.6DL
	R8618	15Kohm 64.15025.6DL	DY

TABLE VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
900MHz	72.52G63.A0U	72.42164.D0U	72.51G63.H0U	72.41646.Q0U
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

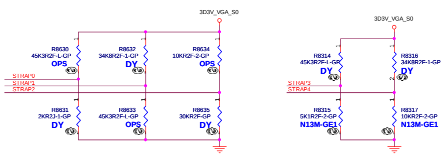


	TABLE NVIDIA	N12P-GL DEV ID: 0x0DE9	N12M-GE1 DEV ID: 0x1058
STRAP1	R8632	DY	DY
	R8633	45Kohm 64.45325.6DL	35Kohm 64.34825.6DL
STRAP2	R8634	10Kohm 64.10025.6DL	5Kohm 64.51015.6DL
	R8635	DY	DY
STRAP3	R8314	DY	DY
	R8315	DY	5Kohm 64.51015.6DL
STRAP4	R8316	DY	DY
	R8317	DY	10Kohm 64.10025.6DL

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21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: **N13P_GPU (4/5): GPIO/STRAP**

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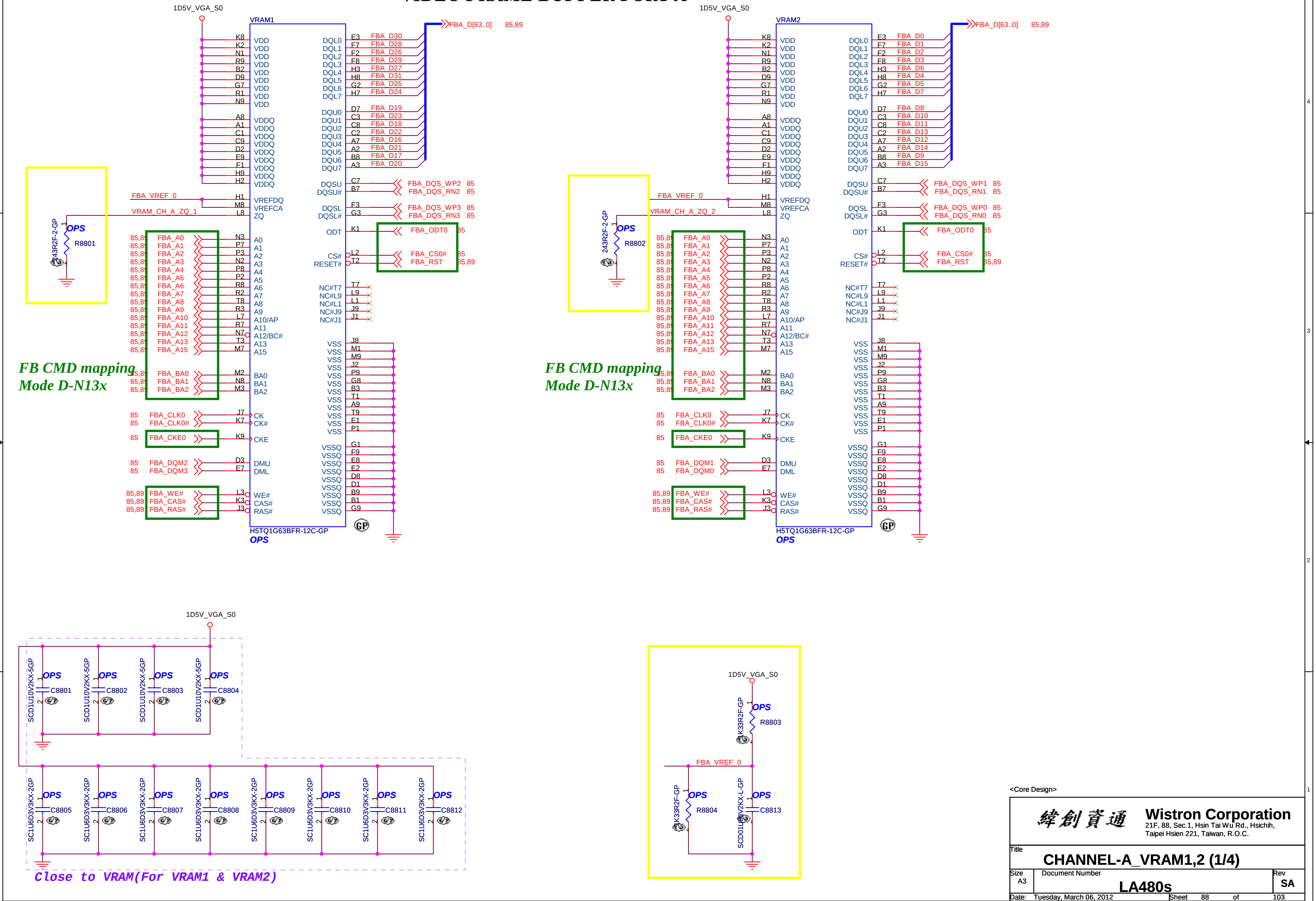
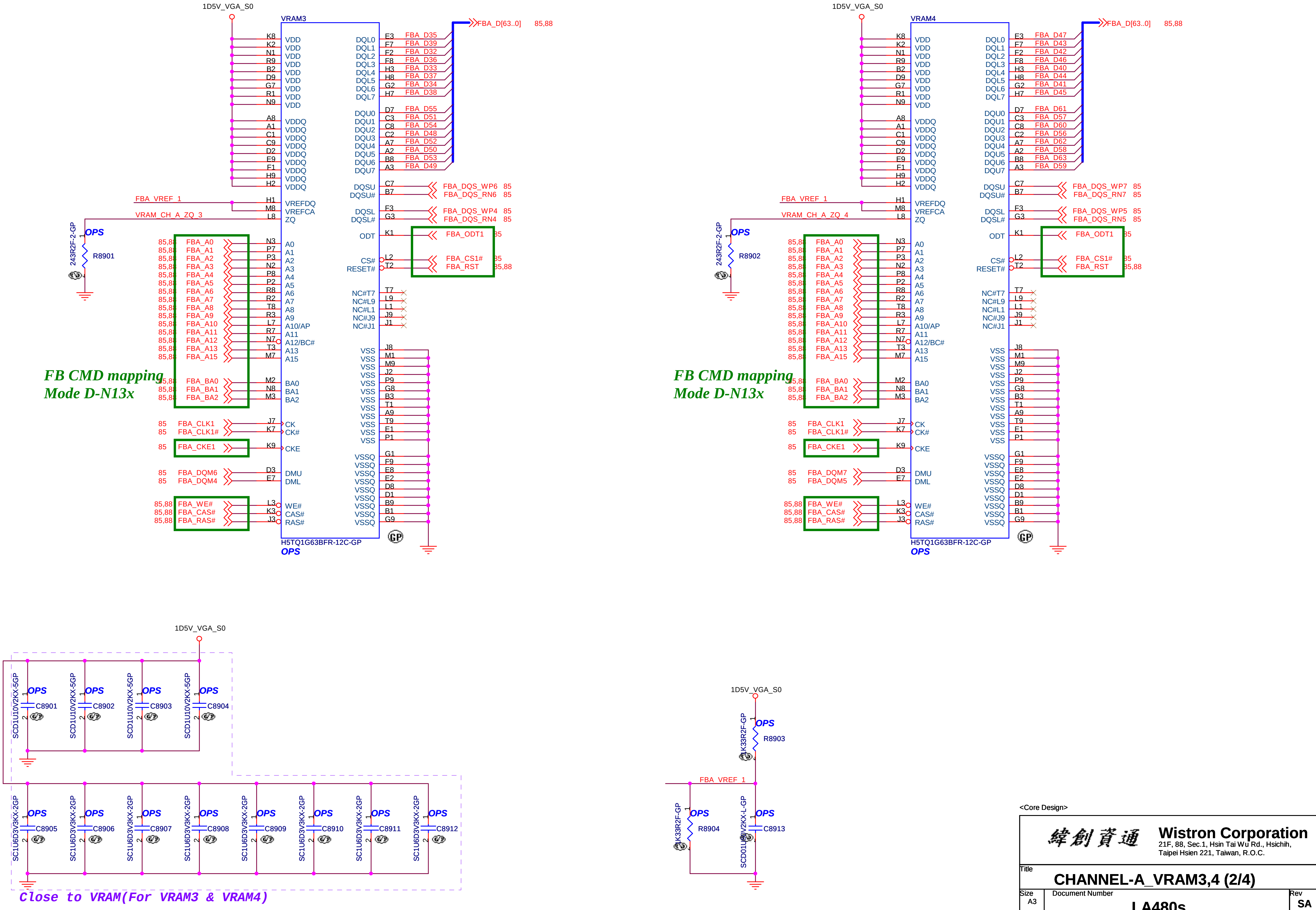
VIDEO FRAME BUFFER PORT A



VIDEO FRAME BUFFER PORT A



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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CHANNEL-A_VRAM3,4 (2/4)		
Size: A3	Document Number: LA480s	Rev: SA
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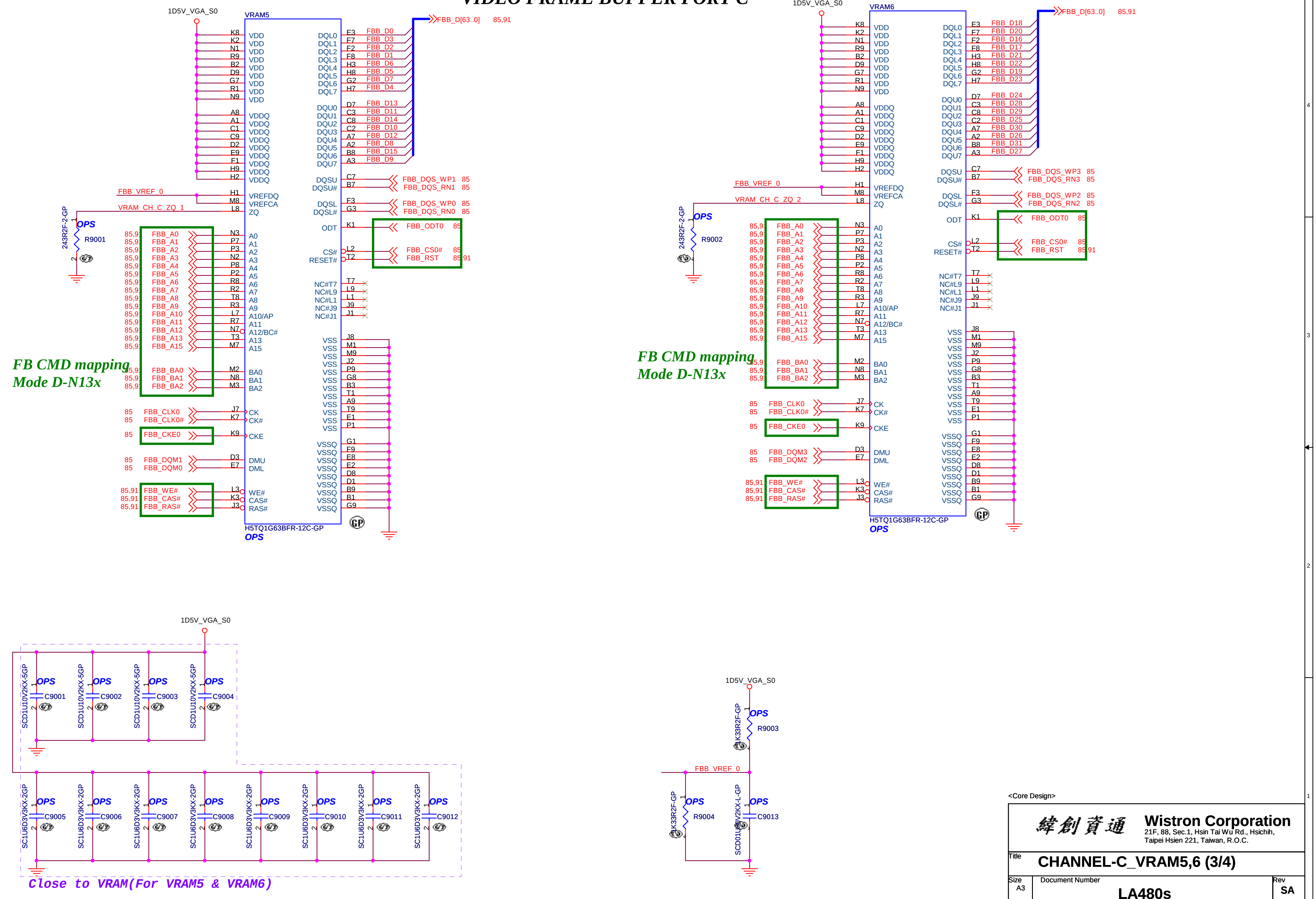
VIDEO FRAME BUFFER PORT C



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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CHANNEL-C_VRAM5,6 (3/4)
Size A3	Document Number LA480s — Rev SA
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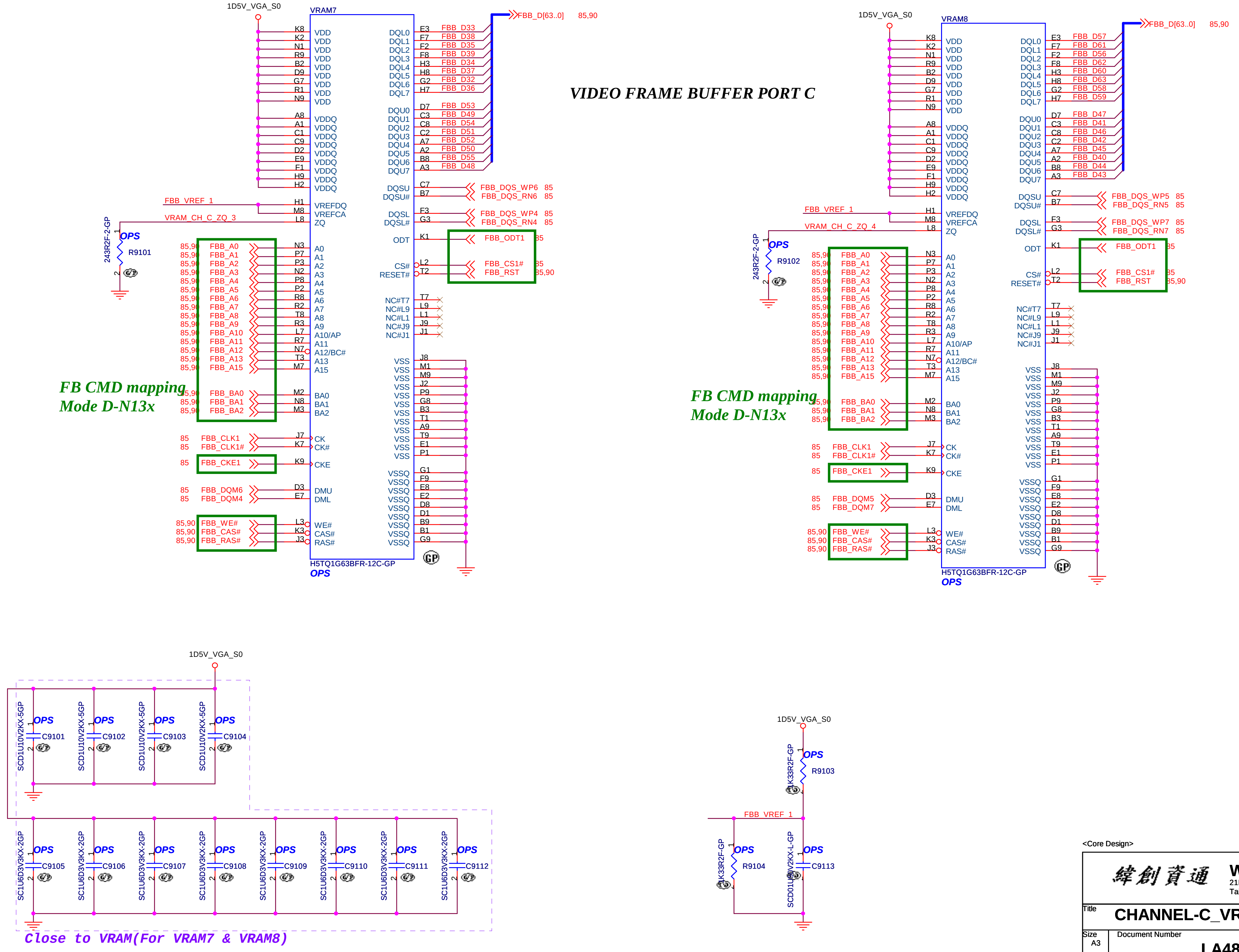

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Title	CHANNEL-C_VRAM7,8 (4/4)	
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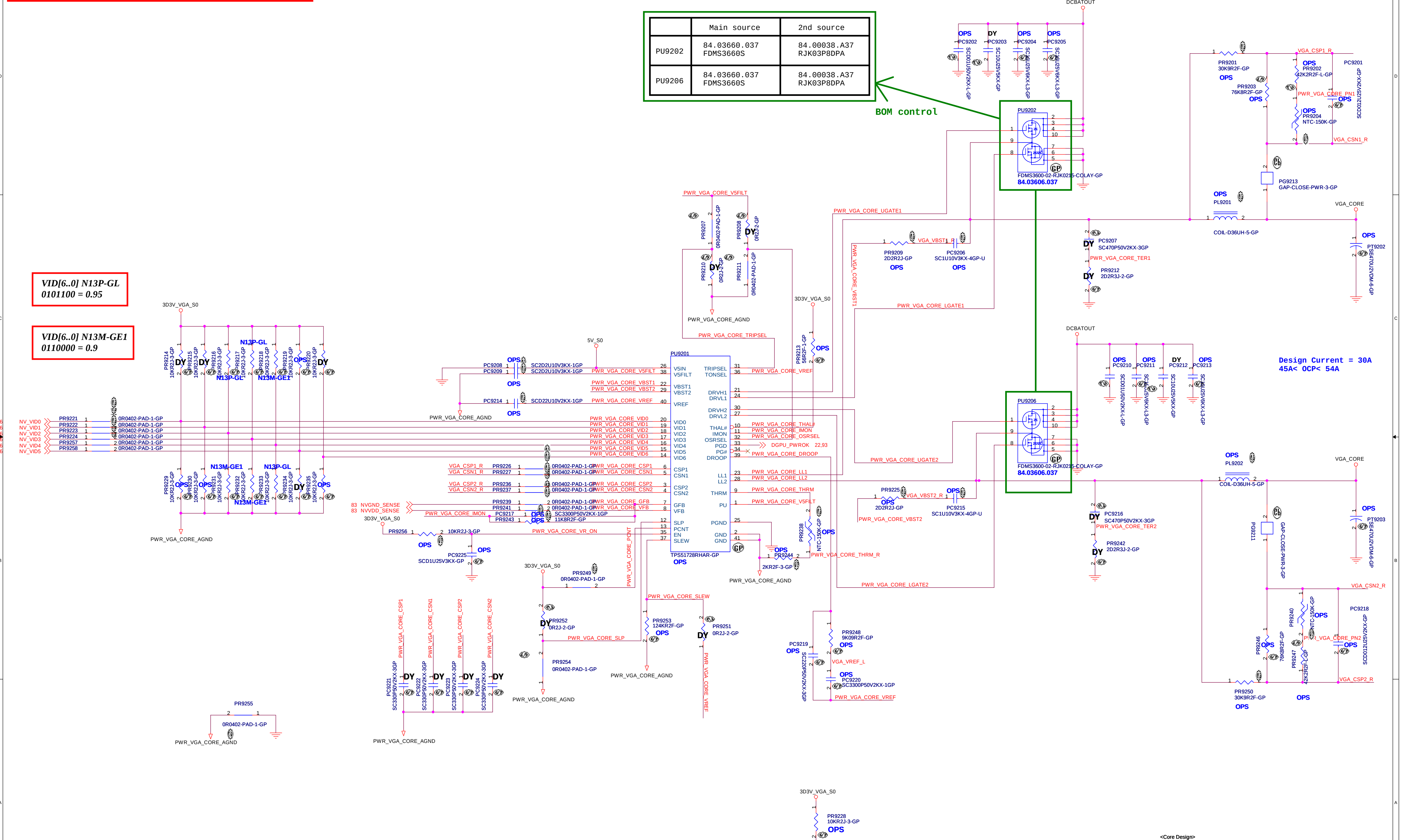
SSID = PWR.Plane.Regulator_GFX

	Main source	2nd source
PU9202	84.03660.037 FDMS3660S	84.00038.A37 RJK03P8DPA
PU9206	84.03660.037 FDMS3660S	84.00038.A37 RJK03P8DPA

BOM control



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51728_VGA_CORE

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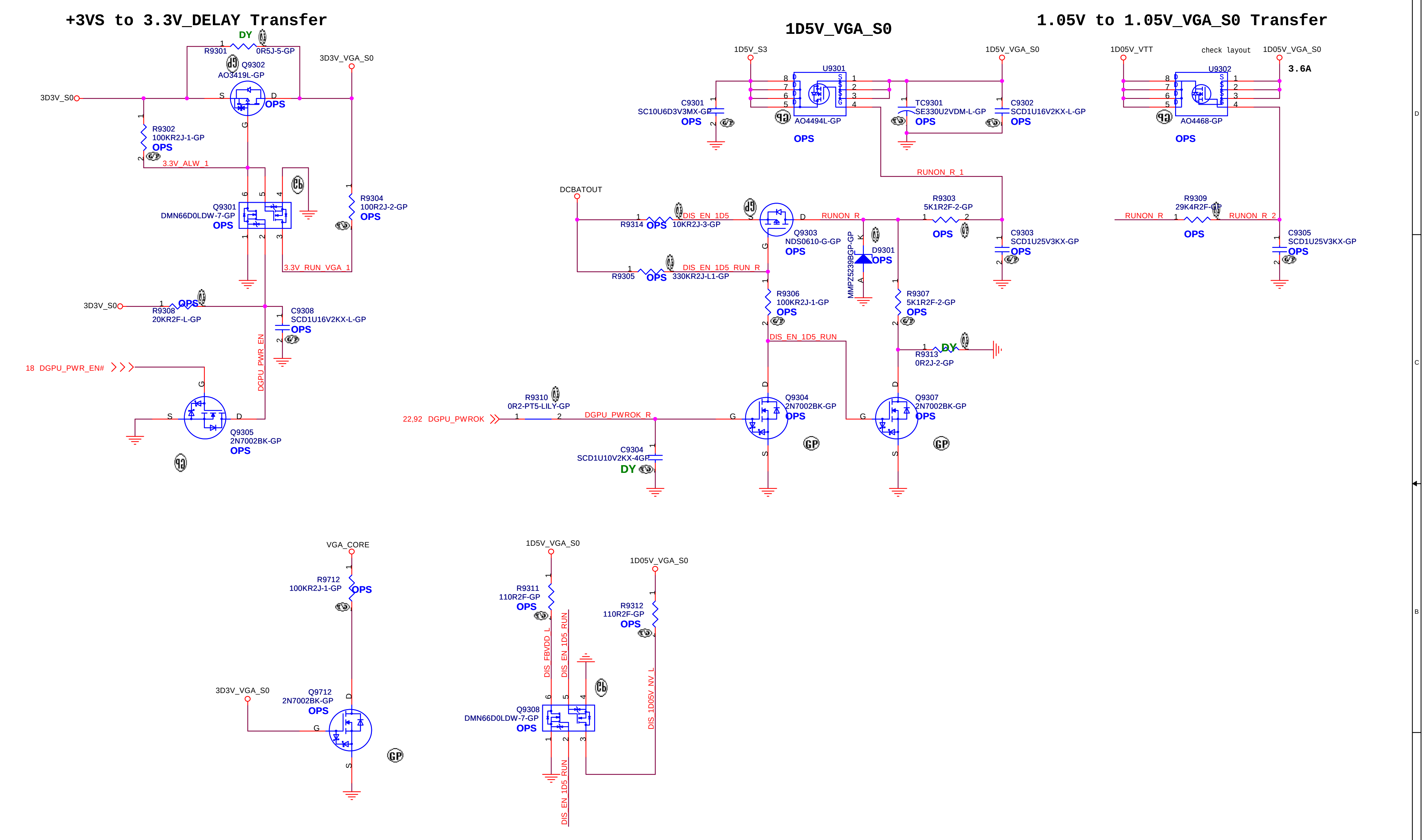

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緯創資通 **Wistron Corporation**
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Title	DISCRETE VGA POWER		
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Title <Title>	
Size A4	Document Number **LA480s** Rev SA
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Taipei Hsien 221, Taiwan, R.O.C.

Title	**Reserved**	
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Taipei Hsien 221, Taiwan, R.O.C.

Title	TOUCH PANEL	
Size A4	Document Number LA480s	Rev SA
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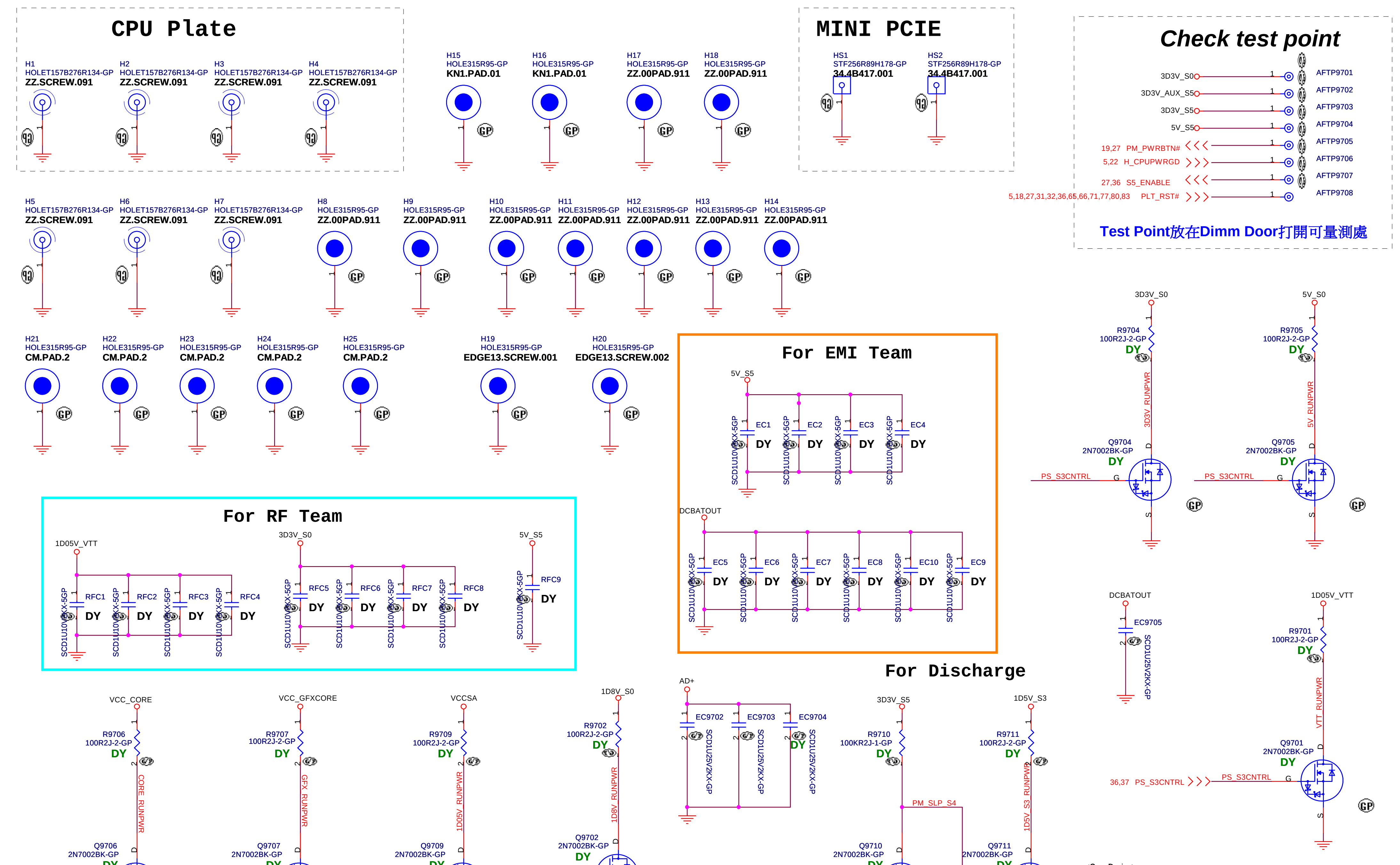

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **UNUSED PARTS/EMI Capacitors**

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A3	LA480s	SA

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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	Change History		
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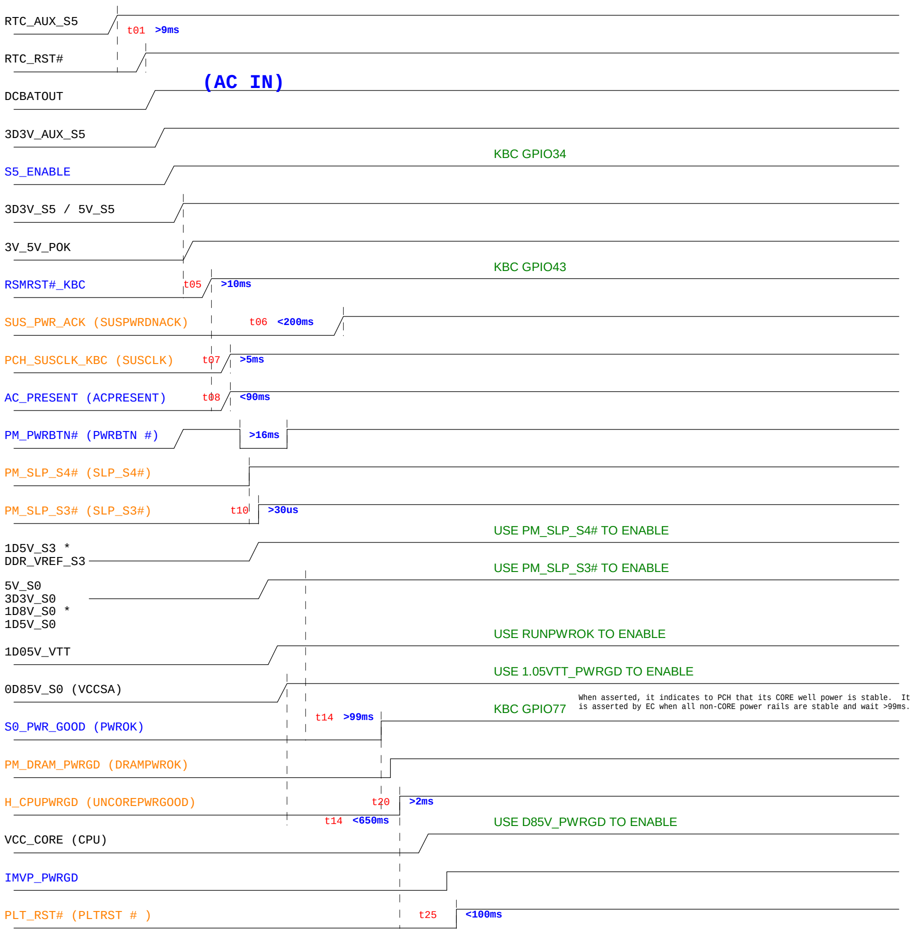
(AC mode)

red word: KBC GPIO
red word: PCH / CPU



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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	<Title>	
Size A2	Document Number LA480s	Rev SA
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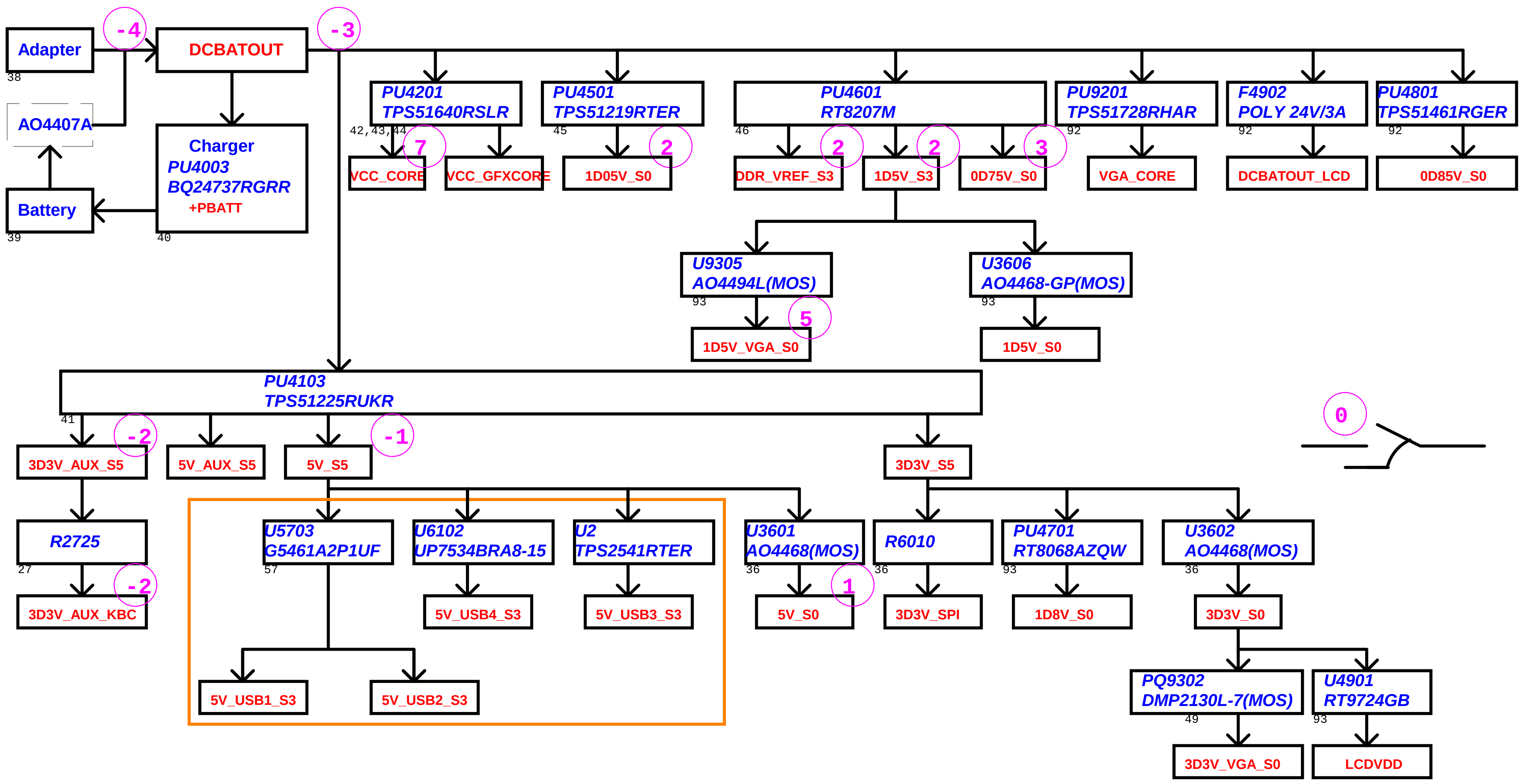

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Title			
Power Block Diagram			
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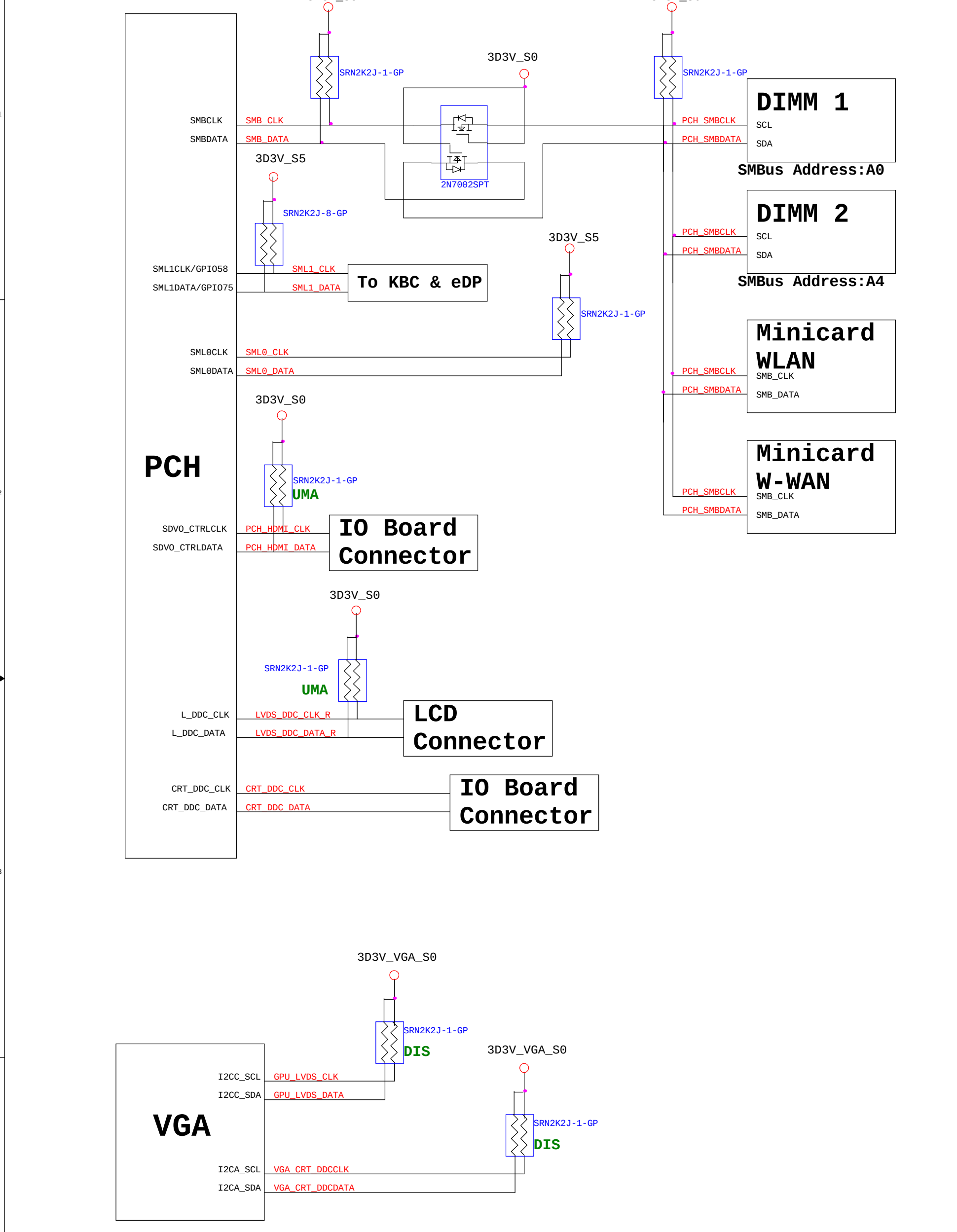
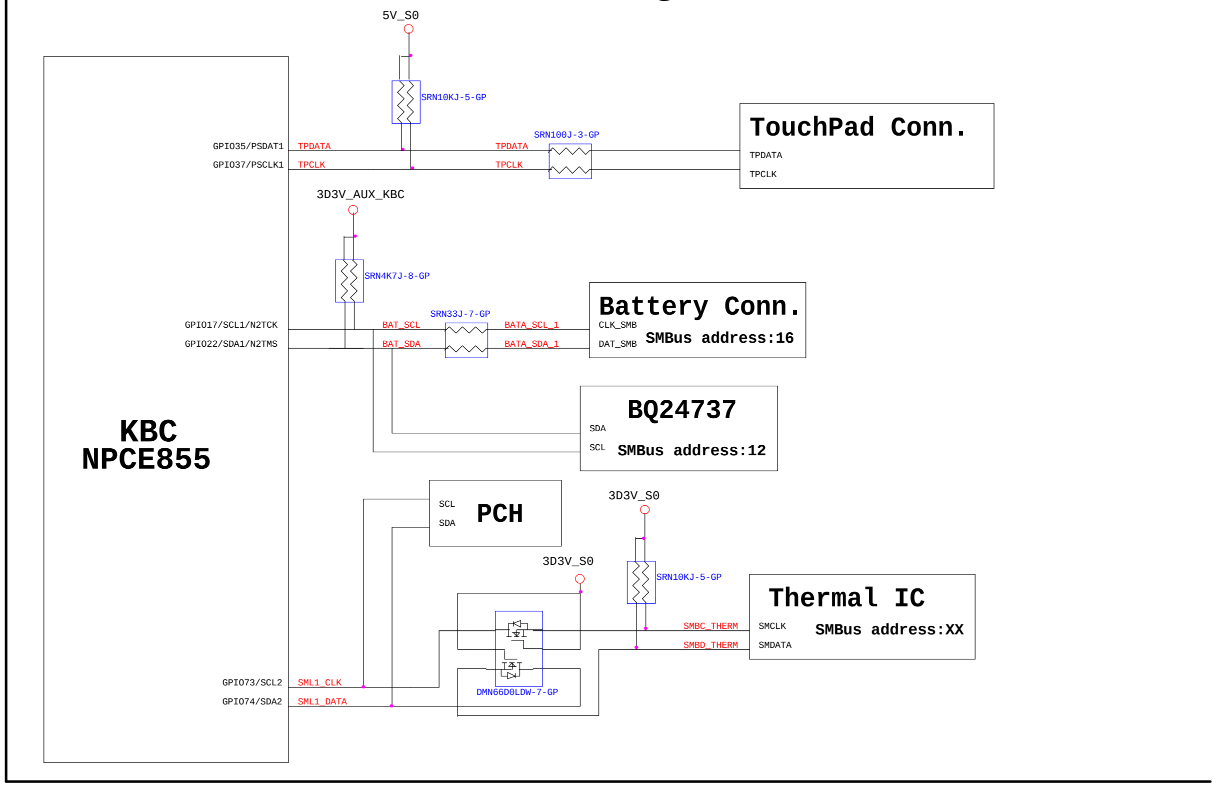
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title	SMBUS Block Diagram	
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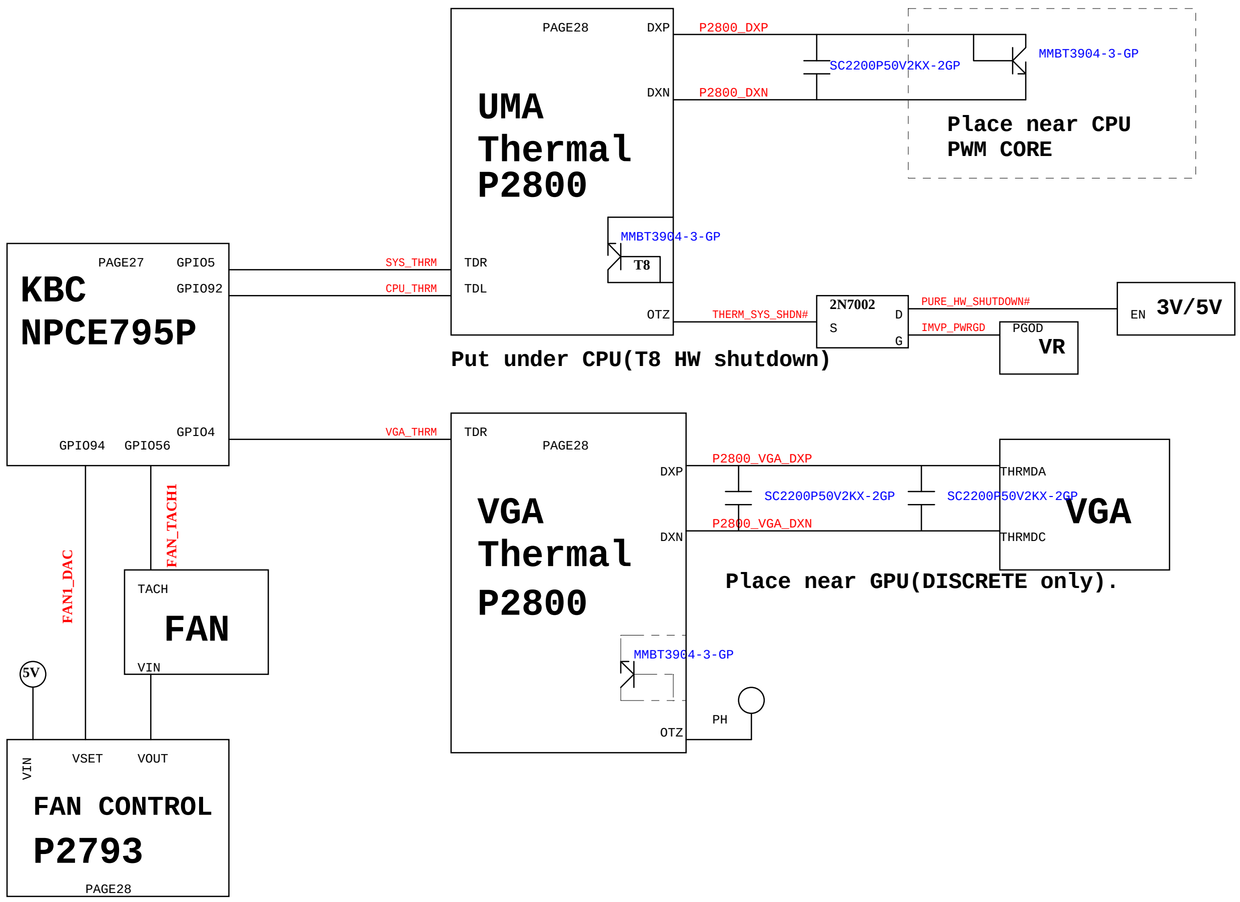
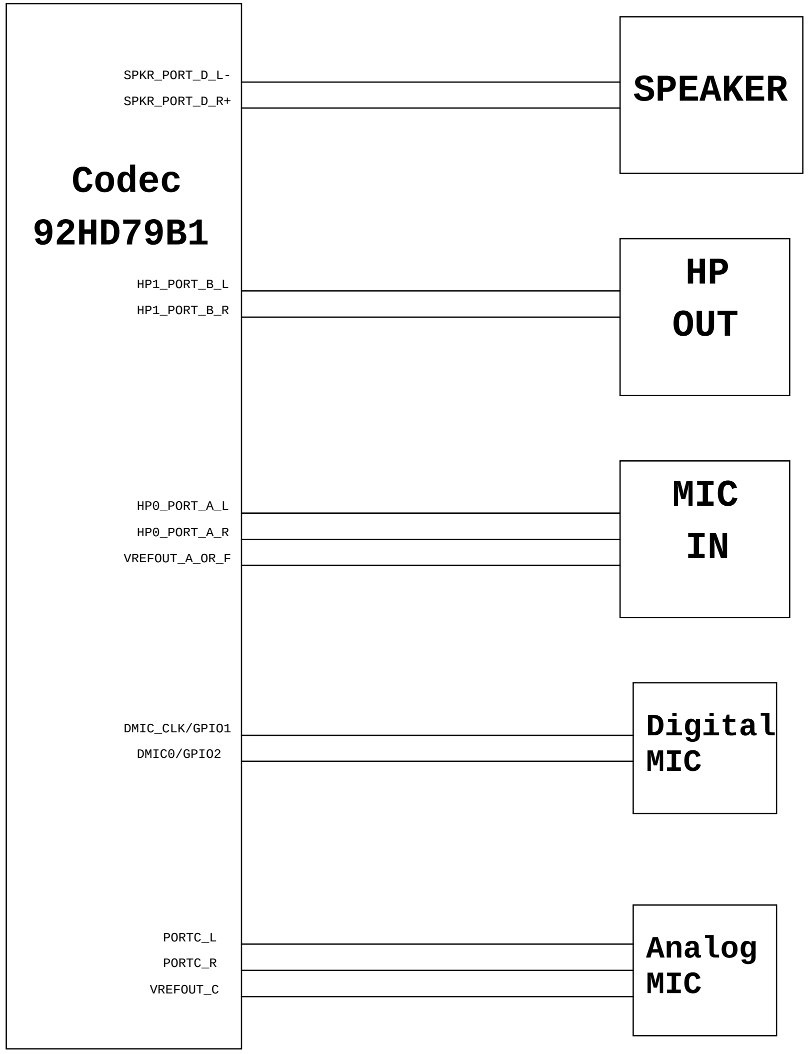
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram		
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Title: Change History		
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