Compal Confidential

NAV51 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII

2010-03-31

REV: 1.0

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

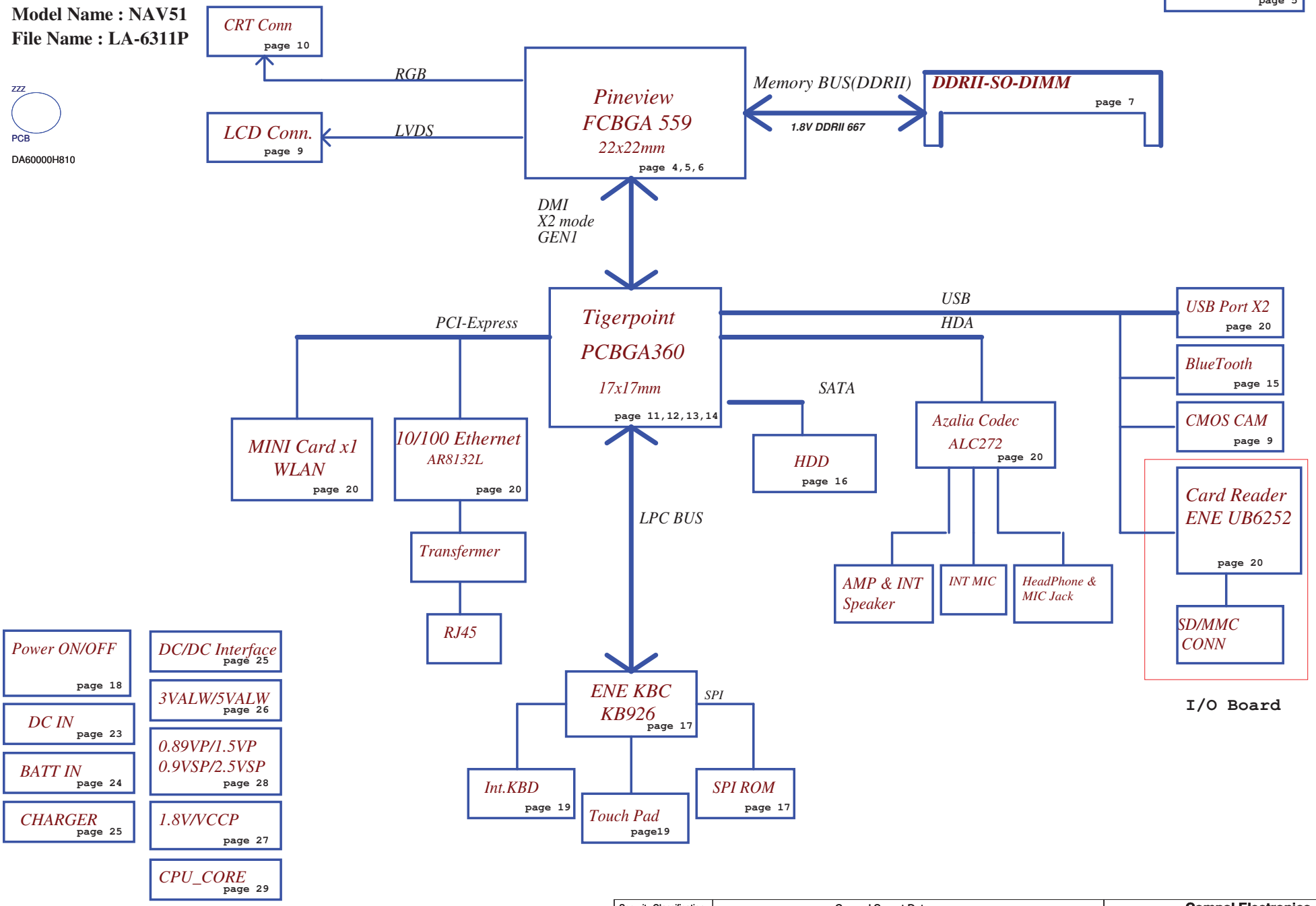
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Title: Cover Page		
Size: B	Document Number: NAV51 LA-6311P	Rev: 1.0
Date: Tuesday, April 13, 2010	Sheet 1 of 33	

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Model Name : NAV51
File Name : LA-6311P

ZZZ
PCB
DA60000H810



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Title: Block Diagrams			
Size: B	Document Number: NAV51 LA-6311P		Rev: 1.0
Date: Tuesday, April 13, 2010		Sheet 2 of 33	

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 17)

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0(EVT)	0	0 V	0 V	0 V
1(DVT)	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2(PVT)	18K +/- 5%	0.436 V	0.503 V	0.538 V
3(MP)	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
EMC1402	100_1100

Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

USB table

EHCI1	UHCI1	Port0	MB USB Conn1.
		Port1	MB USB Conn2.
	UHCI2	Port2	
		Port3	CMOS
	UHCI3	Port4	Card Reader
		Port5	
EHCI2	UHCI4	Port6	BT
		Port7	WLAN
	UHCI5	Port8	
		Port9	
	UHCI6	Port10	
		Port11	

PCIE table

PCIE port1	LAN
PCIE port2	Wireless Card
PCIE port3	
PCIE port4	
PCIE port5	
PCIE port6	

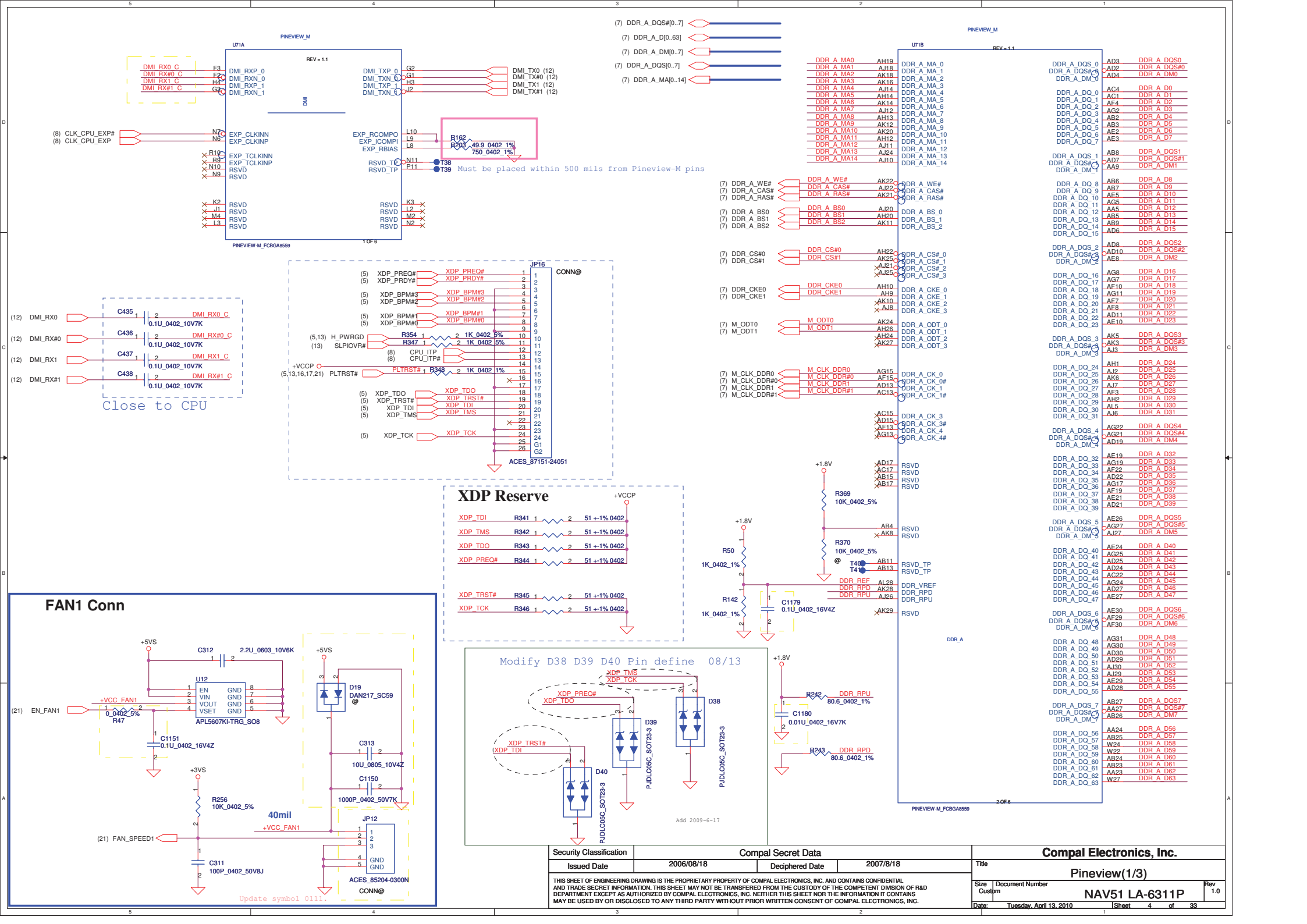
SATA table

SATA port0	HDD
SATA port1	
SATA port2	
SATA port3	
SATA port4	
SATA port5	

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Title	Notes List		
Size B	Document Number	NAV51 LA-6311P	Rev 1.0
Date: Tuesday, April 13, 2010	Sheet 3 of 33		



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Pineview(1/3)

Size	Document Number	Rev
Custom	NAV51 LA-6311P	1.0

Date: Tuesday, April 13, 2010 | Sheet 4 of 33

R249 be placed <750 mils to U71.M30
R247 be placed <750 mils to U71.M29

R201 be placed <500 mils to U71.P28

R151 be placed U71.R22

To be placed <250 mils to U71 ball

To be placed <500 mils to U71 ball

Modify 08/04

Add 470PF on H_SMI# for known issue 07/08

H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

CPU THERMAL SENSOR

EMC1402-1-ACZL-TR MSOP 8P SENSOR
Address:100_1100

Close to Processor pin

Close to Processor pin

placed within 0.5" of processor pin and 5mils spacing.

placed within 0.5" of processor pin and 5mils spacing.

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Compal Electronics, Inc.

Title	Pineview(2/3)	
Size B	Document Number NAV51 LA-6311P	Rev 1.0
Date: Tuesday, April 13, 2010	Sheet 5 of 33	

GFX supply current: 1.38A
Sustained GFX supply current: 1.05A

DDR supply current 2.27A

DDR analog supply current: 1.32A

Display PLL SFR and CRT DAC supply current: 0.154A

GIO supply current: 0.006A

DAC, GIO, LVDS, & LGIO, DPLL, HMPLL supply current: 0.33A

Processor core analog supply current: 0.08A

LVDS supply current: 0.06A

DMI analog supply current: 0.48A

SFR & DMIHMPLL supply current: 0.104A

Please closed U71

Please closed U71.Y2

Please closed U71.D4

C243 to closed U71.U10

Close Chipset pin

Modify to 2.2U 05/11

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Compal Electronics, Inc.

Title: Pineview(3/3)

Size	Document Number	Rev
Custom	NAV51 LA-6311P	1.0

Date: Tuesday, April 13, 2010 | Sheet 6 of 33

09/03

Change to SP07F001720 04/30

(4) DDR_A_DQS#[0..7]
(4) DDR_A_D[0..63]
(4) DDR_A_DM[0..7]
(4) DDR_A_DQS[0..7]
(4) DDR_A_MA[0..14]

Layout Note:
Place near JDIM1

+1.8V

C128 2.2U_0603_6.3V4Z
C129 2.2U_0603_6.3V4Z
C110 2.2U_0603_6.3V4Z
C109 2.2U_0603_6.3V4Z
C130 2.2U_0603_6.3V4Z

@ C94 220U_B2_2.5VM_R35
C106 0.1U_0402_16V4Z
C105 0.1U_0402_16V4Z
C108 0.1U_0402_16V4Z
C107 0.1U_0402_16V4Z

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS

C119 C117 C86 C121 C87 C88 C122 C115 C91 C90 C120 C118 C89 C439 C440 C441 C442 C443 C444 C445 C446
0.1U_0402_16V4Z

+0.9VS

RP6: DDR_A_MA13, M_ODT0, DDR_CS#0, DDR_A_RAS# → DDR_A_BS1, DDR_A_MA0, DDR_A_MA2, DDR_A_MA4
RP5: 47_0804_8P4R_5%
RP2: DDR_A_BS0, DDR_A_MA10, DDR_A_MA1, DDR_A_MA3 → DDR_A_MA6, DDR_A_MA7, DDR_A_MA11, DDR_A_MA14
RP4: 47_0804_8P4R_5%
RP3: M_ODT1, DDR_CS#1, DDR_A_CAS#, DDR_A_WE# → DDR_A_MA5, DDR_A_MA8, DDR_A_MA9, DDR_A_MA12
RP1: 47_0804_8P4R_5%

Layout Note:
Place these resistor closely DIMMA,all trace length<1000 mil

DDR_CKE1 — R163 47_0402_5%
DDR_A_BS2 — R60 47_0402_5%
DDR_CKE0 — R59 47_0402_5%

Layout Note:
Place these resistor closely DIMMA,all trace length Max=1000 mil

+DIMM_VREF — 20mils — C111 0.1U_0402_16V4Z — C112 2.2U 6.3V M X5R 0402

+1.8V — R61 1K_0402_1% — +DIMM_VREF — R62 1K_0402_1%

Share +DIMM_VREF for
1.DDRII VREF
2.GMCH SM_VREF_0
SM_VREF_1

+3VS — C116 0.1U_0402_16V4Z — C141 0.1U_0402_16V4Z

CONN@ JDIM1

	VREF	1	2	VSS	
	VSS	3	4	DQ4	DDR_A_D4
DDR_A_D0	DQ0	5	6	DQ5	DDR_A_D5
DDR_A_D1	DQ1	7	8	VSS	
	VSS	9	10	DM0	DDR_A_DM0
DDR_A_DQS#0	DQS0#	11	12	VSS	
DDR_A_DQS0	DQS0	13	14	DQ6	DDR_A_D6
	VSS	15	16	DQ7	DDR_A_D7
DDR_A_D2	DQ2	17	18	VSS	
DDR_A_D3	DQ3	19	20	DQ12	DDR_A_D12
	VSS	21	22	DQ13	DDR_A_D13
DDR_A_D8	DQ8	23	24	VSS	
DDR_A_D9	DQ9	25	26	DM1	DDR_A_DM1
	VSS	27	28	VSS	
DDR_A_DQS#1	DQS1#	29	30	CK0	M_CLK_DDR0 (4)
DDR_A_DQS1	DQS1	31	32	CK0#	M_CLK_DDR#0 (4)
	VSS	33	34	VSS	
DDR_A_D10	DQ10	35	36	DQ14	DDR_A_D14
DDR_A_D11	DQ11	37	38	DQ15	DDR_A_D15
	VSS	39	40	VSS	
	VSS	41	42	VSS	
DDR_A_D16	DQ16	43	44	DQ20	DDR_A_D20
DDR_A_D17	DQ17	45	46	DQ21	DDR_A_D21
	VSS	47	48	VSS	
DDR_A_DQS#2	DQS2#	49	50	NC	R64 1 2 0_0402_5% PM_EXTTS#0 (5)
DDR_A_DQS2	DQS2	51	52	DM2	DDR_A_DM2
	VSS	53	54	VSS	
DDR_A_D18	DQ18	55	56	DQ22	DDR_A_D22
DDR_A_D19	DQ19	57	58	DQ23	DDR_A_D23
	VSS	59	60	VSS	
DDR_A_D24	DQ24	61	62	DQ28	DDR_A_D28
DDR_A_D25	DQ25	63	64	DQ29	DDR_A_D29
	VSS	65	66	VSS	
DDR_A_DM3	DM3	67	68	DQS3#	DDR_A_DQS#3
	NC	69	70	DQS3	DDR_A_DQS3
	VSS	71	72	VSS	
DDR_A_D26	DQ26	73	74	DQ30	DDR_A_D30
DDR_A_D27	DQ27	75	76	DQ31	DDR_A_D31
	VSS	77	78	VSS	
(4) DDR_CKE0	CKE0	79	80	NC/CKE1	DDR_CKE1 (4)
	VDD	81	82	VDD	
	NC	83	84	NC/A15	
(4) DDR_A_BS2	BA2	85	86	NC/A14	DDR_A_MA14
	VDD	87	88	VDD	
DDR_A_MA12	A12	89	90	A11	DDR_A_MA11
DDR_A_MA9	A9	91	92	A7	DDR_A_MA7
DDR_A_MA8	A8	93	94	A6	DDR_A_MA6
	VDD	95	96	VDD	
DDR_A_MA5	A5	97	98	A4	DDR_A_MA4
DDR_A_MA3	A3	99	100	A2	DDR_A_MA2
DDR_A_MA1	A1	101	102	A0	DDR_A_MA0
	VDD	103	104	VDD	
DDR_A_MA10	A10/AP	105	106	BA1	DDR_A_BS1 (4)
(4) DDR_A_BS0 DDR_A_BS0	BA0	107	108	RAS#	DDR_A_RAS# (4)
(4) DDR_A_WE# DDR_A_WE#	WE#	109	110	S0#	DDR_CS#0 (4)
	VDD	111	112	VDD	
(4) DDR_A_CAS# DDR_A_CAS#	CAS#	113	114	ODT0	M_ODT0 (4)
(4) DDR_CS#1 DDR_CS#1	NC/S1#	115	116	NC/A13	DDR_A_MA13
	VDD	117	118	VDD	
(4) M_ODT1 M_ODT1	NC/ODT1	119	120	NC	
	VSS	121	122	VSS	
DDR_A_D32	DQ32	123	124	DQ36	DDR_A_D36
DDR_A_D33	DQ33	125	126	DQ37	DDR_A_D37
	VSS	127	128	VSS	
DDR_A_DQS#4	DQS4#	129	130	DM4	DDR_A_DM4
DDR_A_DQS4	DQS4	131	132	VSS	
	VSS	133	134	DQ38	DDR_A_D38
DDR_A_D34	DQ34	135	136	DQ39	DDR_A_D39
DDR_A_D35	DQ35	137	138	VSS	
	VSS	139	140	DQ44	DDR_A_D44
DDR_A_D40	DQ40	141	142	DQ45	DDR_A_D45
DDR_A_D41	DQ41	143	144	VSS	
	VSS	145	146	DQS5#	DDR_A_DQS#5
DDR_A_DM5	DM5	147	148	DQS5	DDR_A_DQS5
	VSS	149	150	VSS	
DDR_A_D42	DQ42	151	152	DQ46	DDR_A_D46
DDR_A_D43	DQ43	153	154	DQ47	DDR_A_D47
	VSS	155	156	VSS	
DDR_A_D48	DQ48	157	158	DQ52	DDR_A_D52
DDR_A_D49	DQ49	159	160	DQ53	DDR_A_D53
	VSS	161	162	VSS	
	NC,TEST	163	164	CK1	M_CLK_DDR1 (4)
	VSS	165	166	CK1#	M_CLK_DDR#1 (4)
DDR_A_DQS#6	DQS6#	167	168	VSS	
DDR_A_DQS6	DQS6	169	170	DM6	DDR_A_DM6
	VSS	171	172	VSS	
DDR_A_D50	DQ50	173	174	DQ54	DDR_A_D54
DDR_A_D51	DQ51	175	176	DQ55	DDR_A_D55
	VSS	177	178	VSS	
DDR_A_D56	DQ56	179	180	DQ60	DDR_A_D60
DDR_A_D57	DQ57	181	182	DQ61	DDR_A_D61
	VSS	183	184	VSS	
DDR_A_DM7	DM7	185	186	DQS7#	DDR_A_DQS#7
	VSS	187	188	DQS7	DDR_A_DQS7
DDR_A_D58	DQ58	189	190	VSS	
DDR_A_D59	DQ59	191	192	DQ62	DDR_A_D62
	VSS	193	194	DQ63	DDR_A_D63
(8,17) CLK_SMBDATA CLK_SMBDATA	SDA	195	196	VSS	
(8,17) CLK_SMBCLK CLK_SMBCLK	SCL	197	198	SA0	R66 1 2 10K_0402_5%
	VDDSPD	199	200	SA1	R65 1 2 10K_0402_5%
	G1	201	202	G2	

FOX_AS0A426-N4RN-7F

For EMI's request add it.021110.

DIMMA

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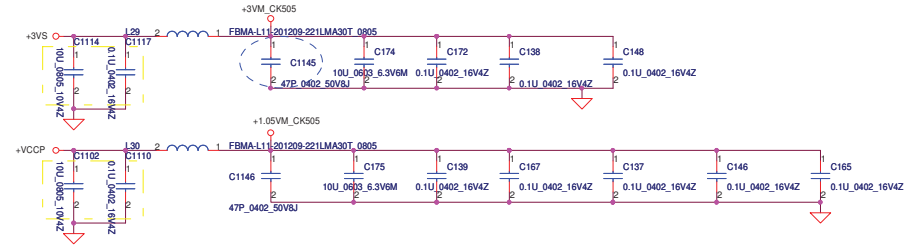
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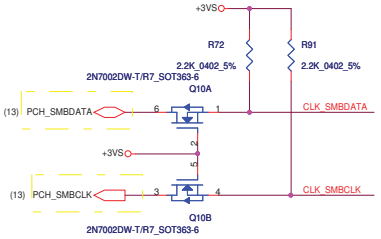
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Size	Document Number	Rev
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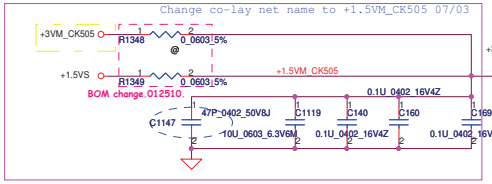
Date: Tuesday, April 13, 2010 Sheet 7 of 33

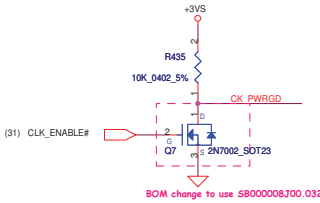
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0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
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1	1	1	Reserved					

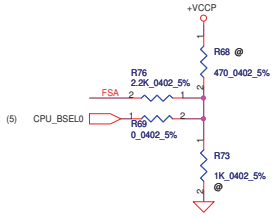


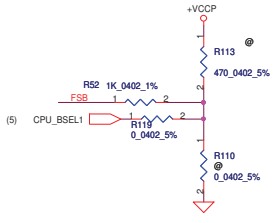


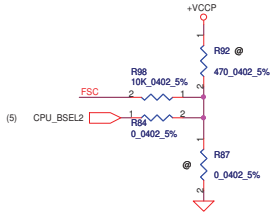
SA00003H730 (Realtek :RTM890N-397-VC-GRT)

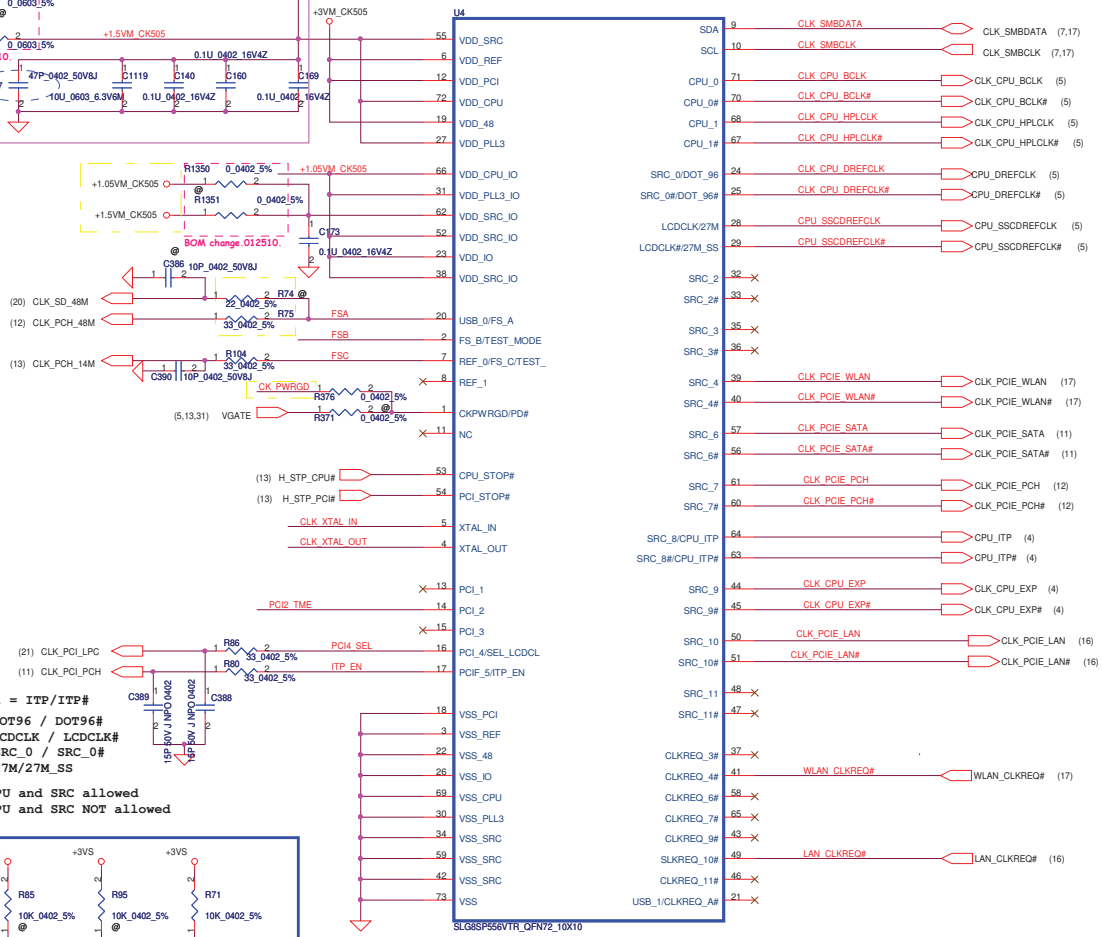






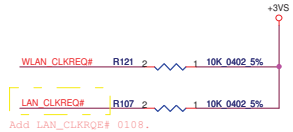






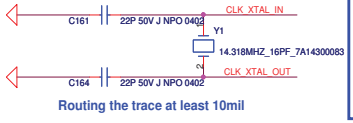
PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_LAN
REQ_11#	
REQ_A#	

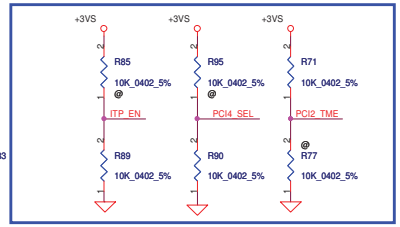


For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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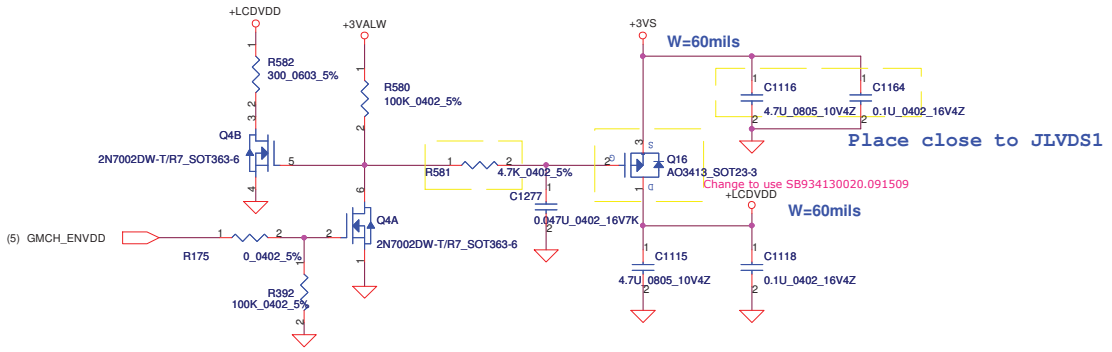
Compal Electronics, Inc.

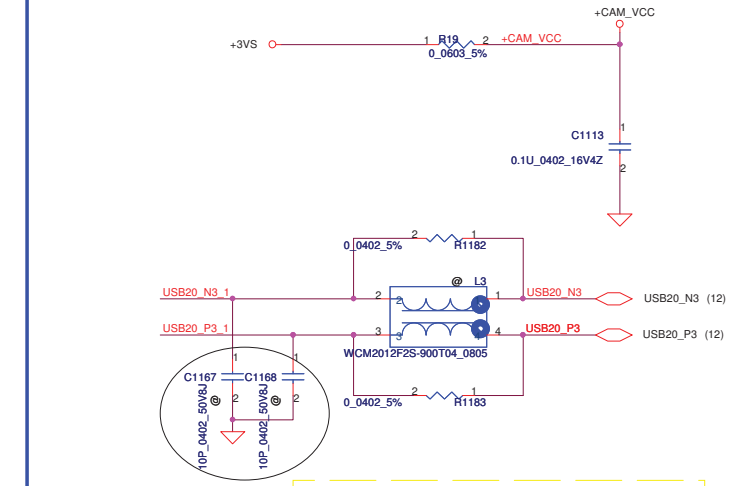
Title: Clock Generator CK505

Size | Document Number: NAV51 LA-6311P | Rev: 1.0

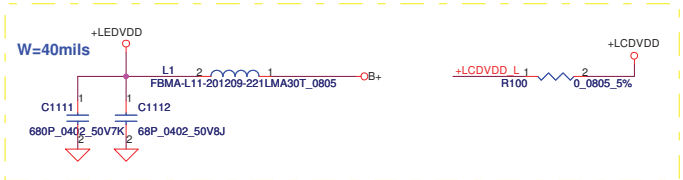
Date: Tuesday, April 13, 2010 | Sheet 8 of 33

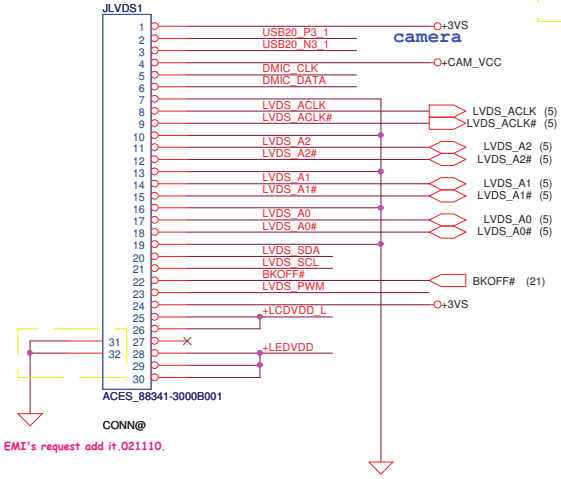
LCD POWER CIRCUIT

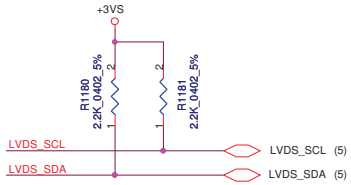


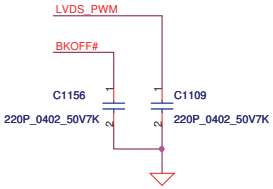


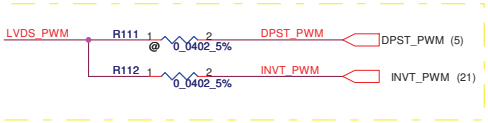
CMOS & LCD/PANEL BD. Conn.

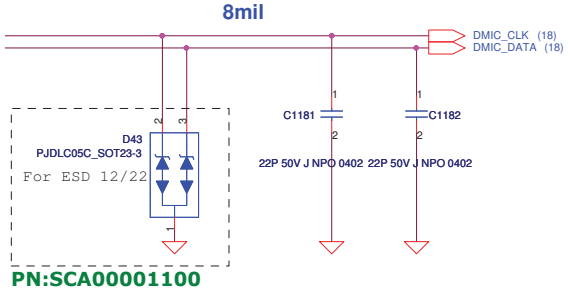












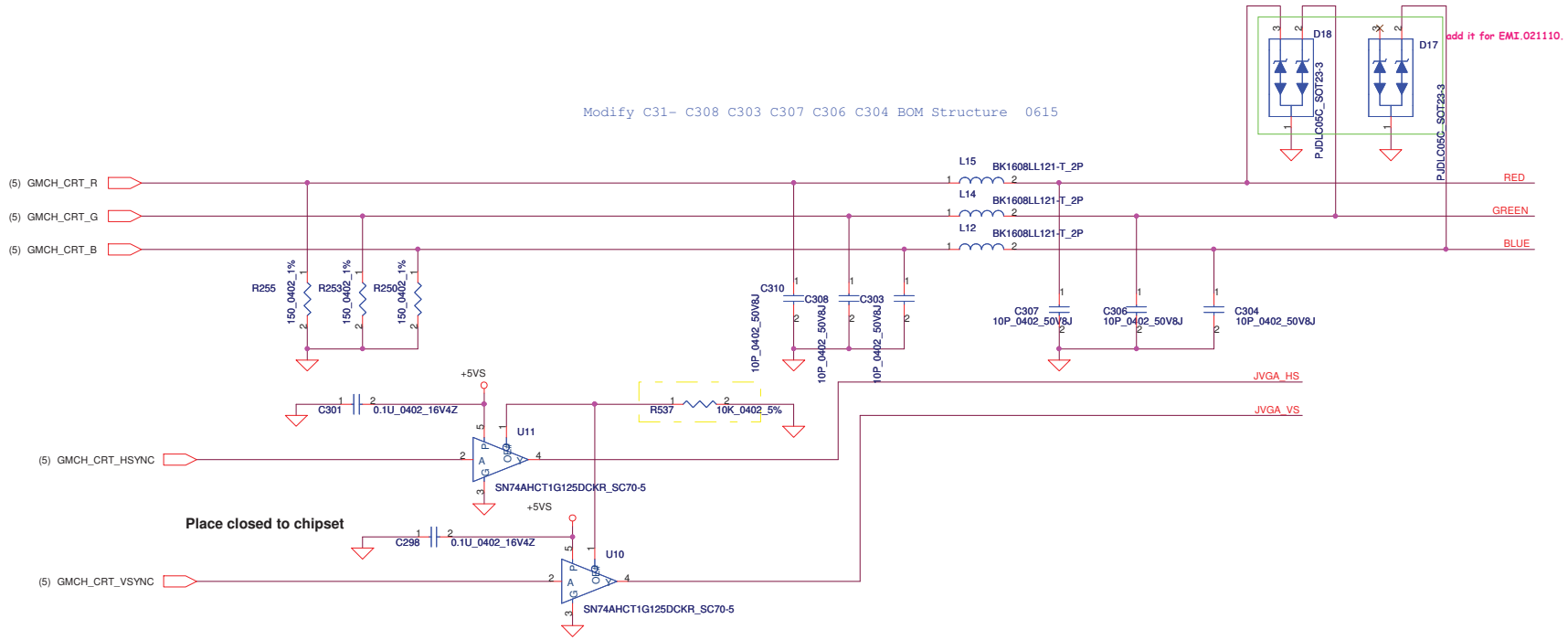
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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Compal Electronics, Inc.	
Title	LVDS /INVERTER
Size B	Document Number NAV51 LA-6311P
Rev	1.0
Date: Tuesday, April 13, 2010	Sheet 9 of 33

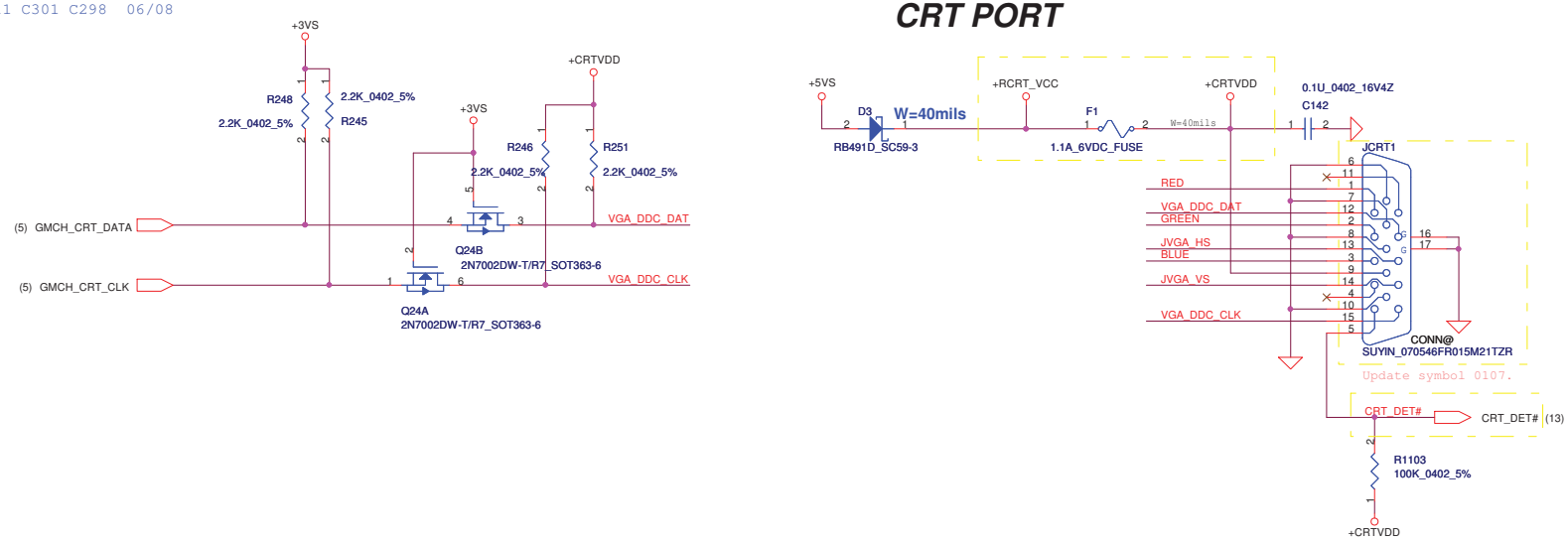
Close to CRT CONN for ESD.

Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615



Add R1283 R1284
Change R247 R249 to 10 ohm
Add @ on U10 U11 C301 C298 06/08

CRT PORT



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

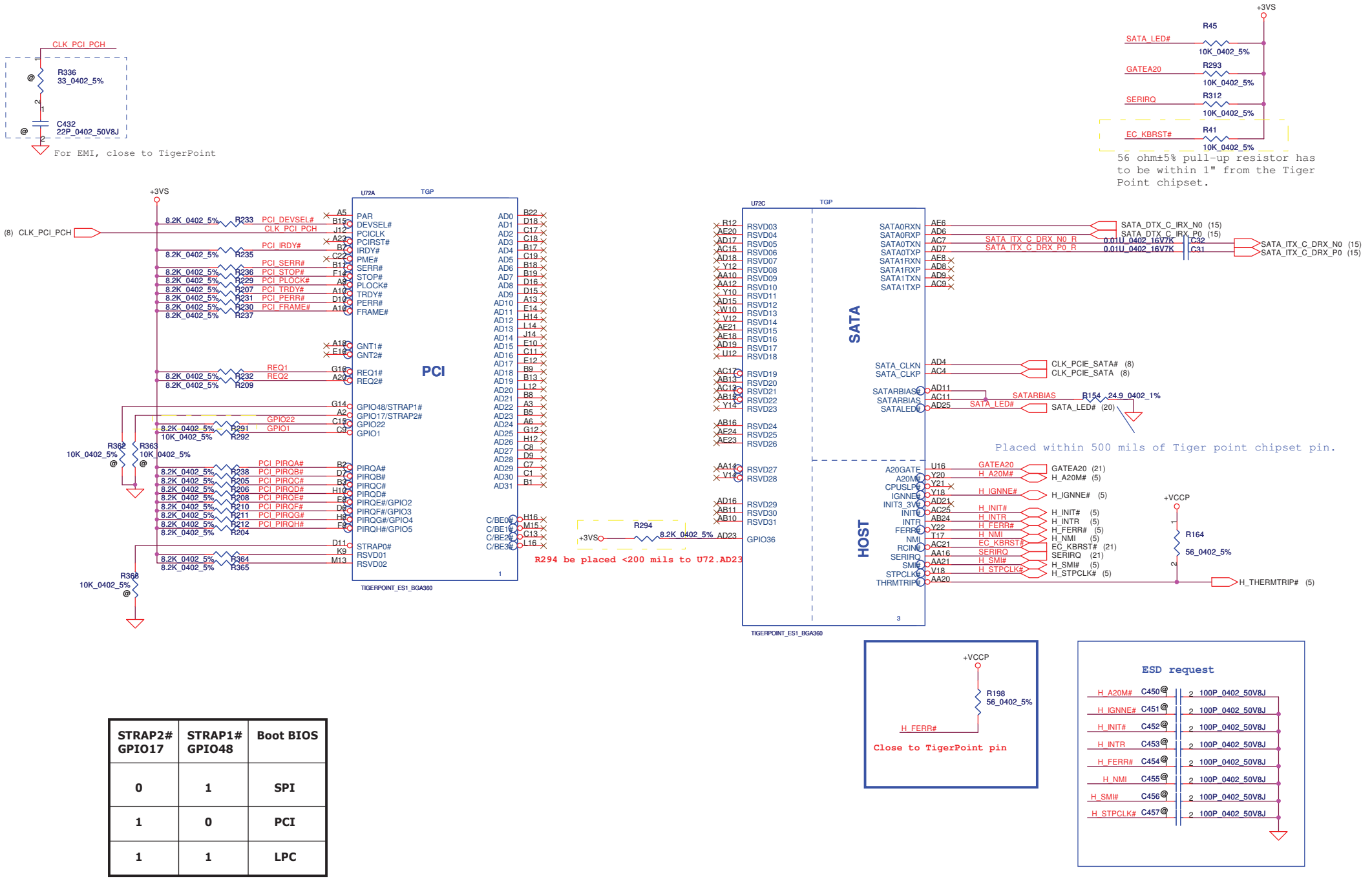
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Compal Electronics, Inc.

Title: CRT PORT

Size	Document Number	Rev
B	NAV51 LA-6311P	0.2

Date: Tuesday, April 13, 2010 Sheet 10 of 33



STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

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Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

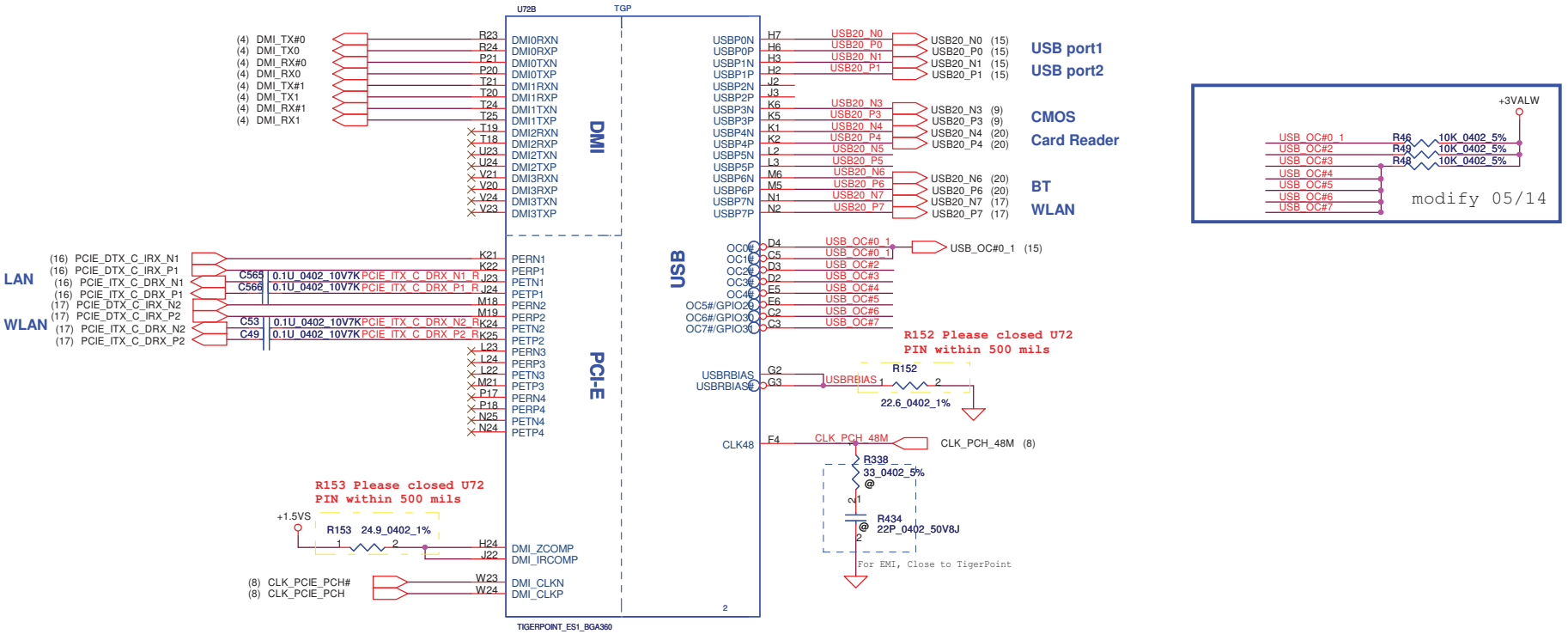
Title: Tigerpoint(1/4)

Size | Document Number: NAV51 LA-6311P | Rev: 1.0

Date: Tuesday, April 13, 2010 | Sheet 11 of 33

PCIE Port List	
1	LAN
2	WLAN
3	
4	

USB Port List	
0	USB Left1
1	USB Left2
2	
3	CMOS
4	CardReader
5	
6	BT
7	WLAN



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

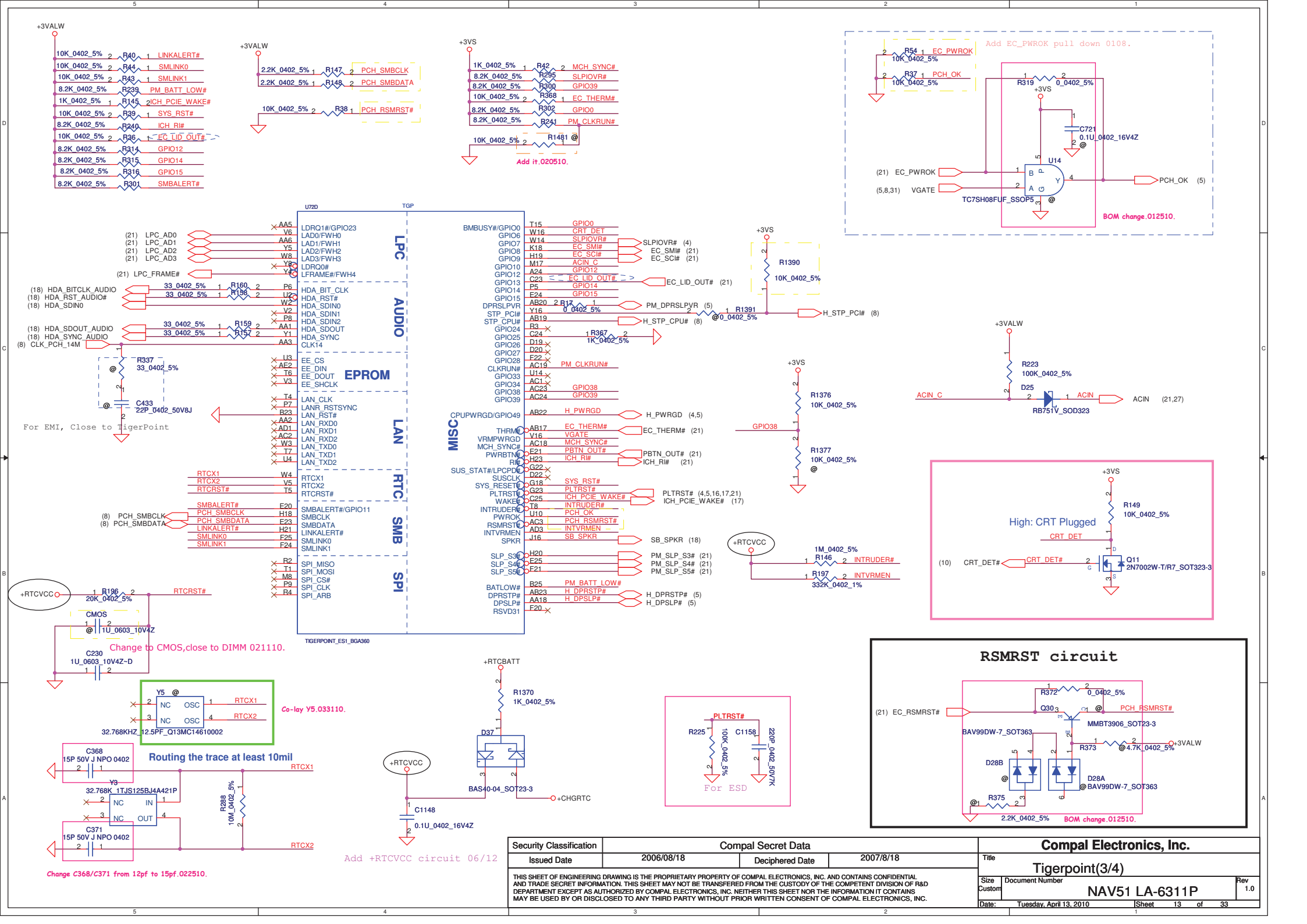
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Compal Electronics, Inc.

Title: Tigerpoint(2/4)

Size: Custom | Document Number: NAV51 LA-6311P | Rev: 1.0

Date: Tuesday, April 13, 2010 | Sheet 12 of 33



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

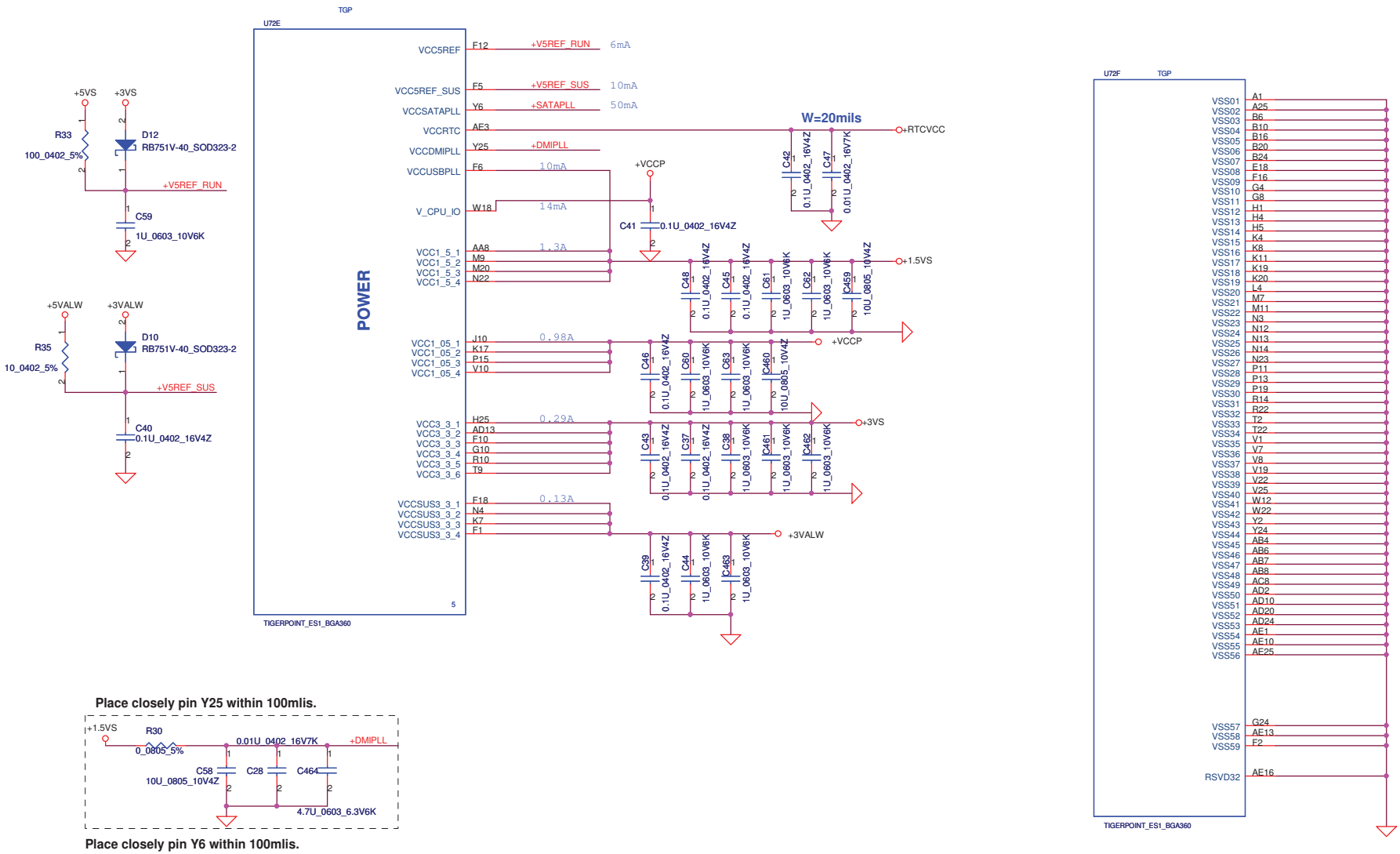
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Compal Electronics, Inc.

Title: Tigerpoint(3/4)

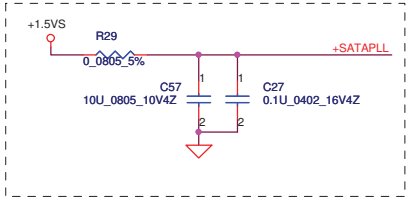
Size: Custom | Document Number: NAV51 LA-6311P | Rev: 1.0

Date: Tuesday, April 13, 2010 | Sheet 13 of 33



Place closely pin Y25 within 100mlis.

Place closely pin Y6 within 100mlis.



Security Classification	Compal Secret Data		
Issued Date	2009/04/15	Deciphered Date	2010/04/15

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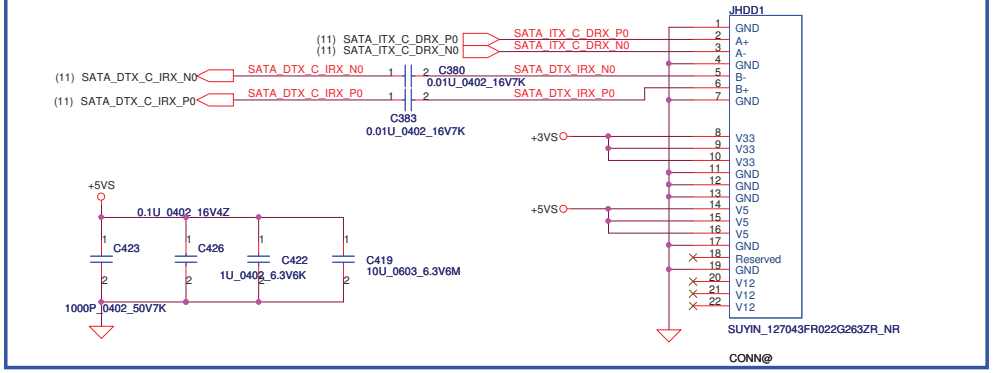
Compal Electronics, Inc.

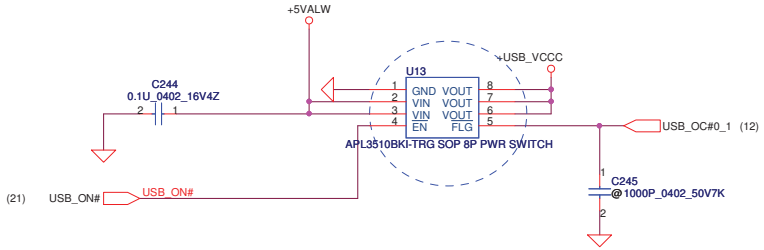
Title: Tigerpoint(4/4)

Size: Custom | Document Number: NAV51 LA-6311P | Rev: 0.1

Date: Tuesday, April 13, 2010 | Sheet 14 of 33

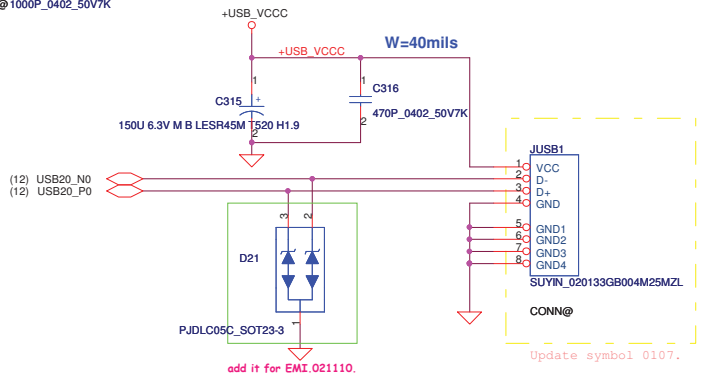
SATA HDD Conn.



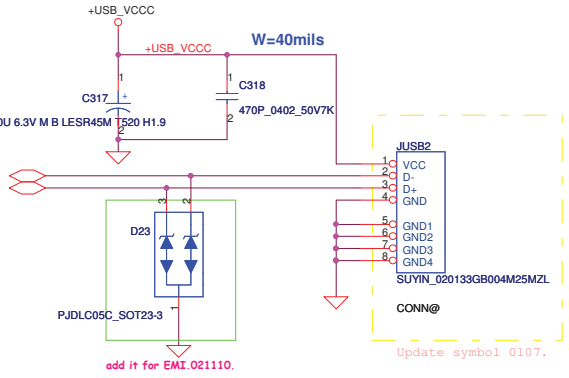


Change JUSB1 JUSB2 to NEW P/N SP010906181 06/23

USB CONN.1



USB CONN.2



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Issued Date	2006/08/18	Deciphered Date	2007/8/18

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Compal Electronics, Inc.

Title: SATA,CONN. / USB CONN.

Size	Document Number	Rev
B	NAV51 LA-6311P	0.2

Date: Tuesday, April 13, 2010 Sheet 15 of 33

L17 close to pin1

C1280 close to pin5

C1278 close to pin6

C1292 close to pin2

60mil

40mil

C1194 、C1195 close to L17

pin7 float -->25MHz

GND-->48MHz

Co-lay Y6.033110.

Change C1186/C1187 from 27pf to 15pf.022510.

the GND directly connect to GND layer

C1281 、C1282 close to pin38 、pin37

R1466 keep away other singal (25mil)

Add pull down R for no-overclocking mode 011710.

C1188 、C1189 close to pin2

close to pin11

close to pin42

If overclocking, R638, L30 stuffed and R637 removed.
If not overclocking, R637, L30 suffed and R638 removed.
AR8132:L30=0ohm,C856=0.1uF. remove C857

Place Close to Chip

20mil

the GND directly connect to GND layer

close to pin19 、pin25

close to pin15

close to pin16 、pin22 、pin36 、pin39

close to pin8

close to pin28 、pin32

close to pin45 、pin46

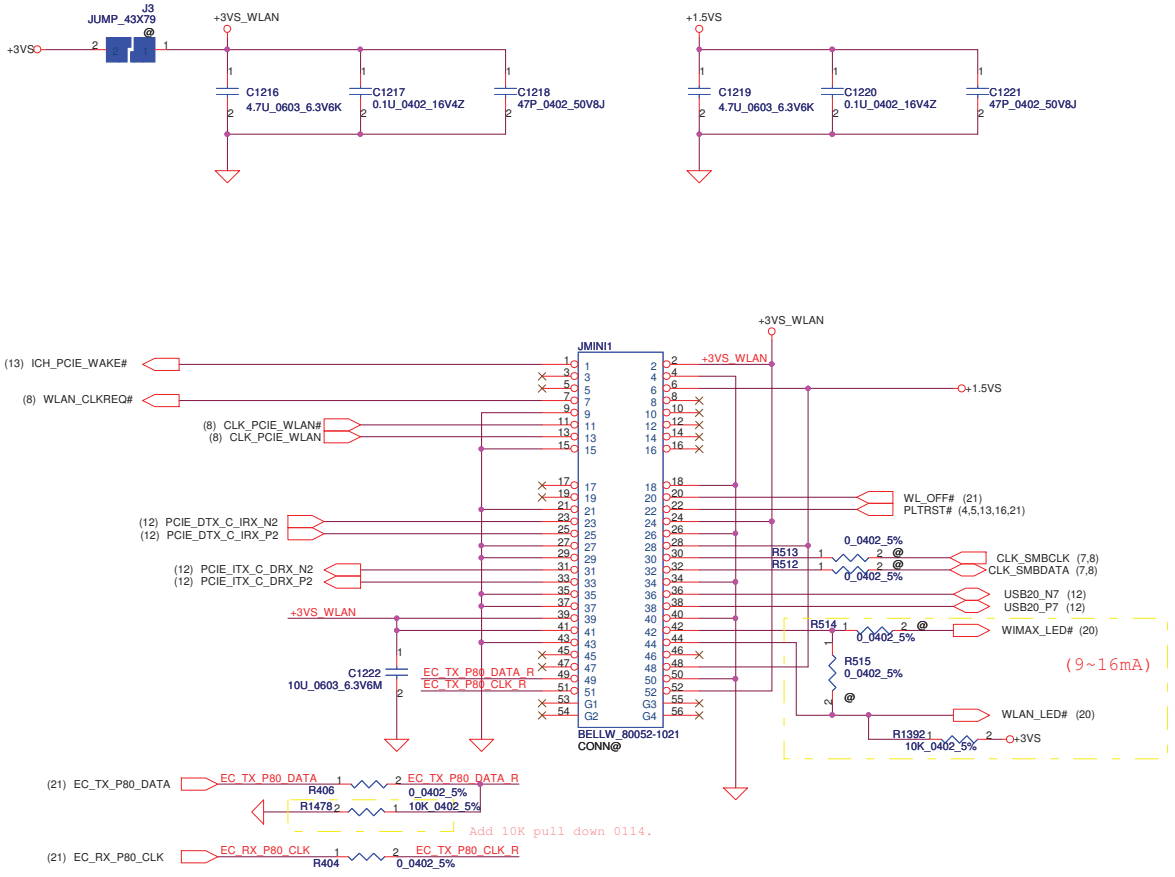
the GND directly connect to GND layer

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

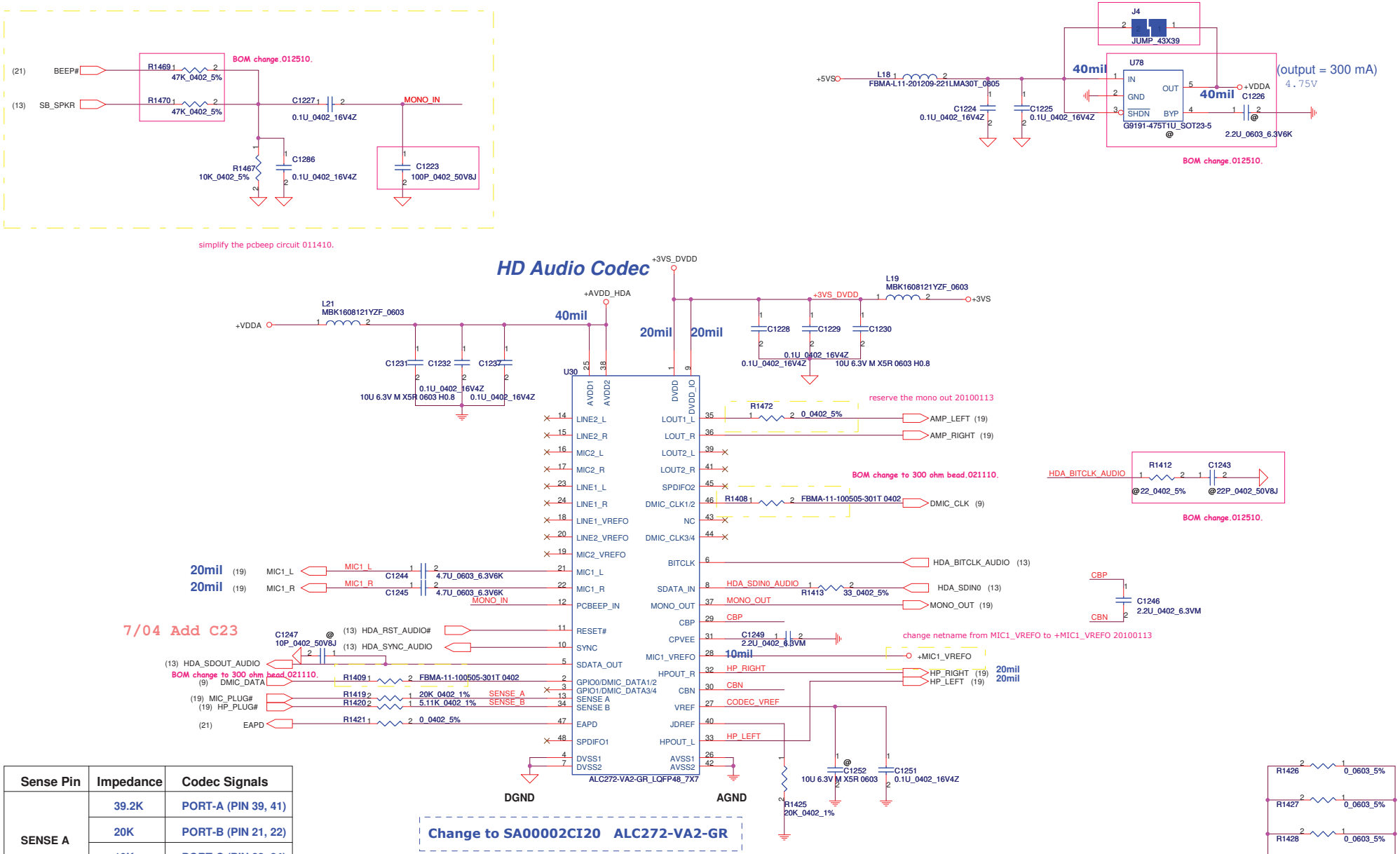
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Compal Electronics, Inc.			
Title	Atheros 8131		
Size: Custom	Document Number: NAV51 LA-6311P		Rev: 1.0
Date: Tuesday, April 13, 2010	Sheet 16 of 33		

Mini-Express Card for WLAN



Compal Electronics, Inc.			
Title	<Title>	WLAN	
Size	Document Number	NAV51 LA-6311P	Rev 0.1
Custom	NAV51 LA-6311P		
Date: Tuesday, April 13, 2010	Sheet 17 of 33		



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

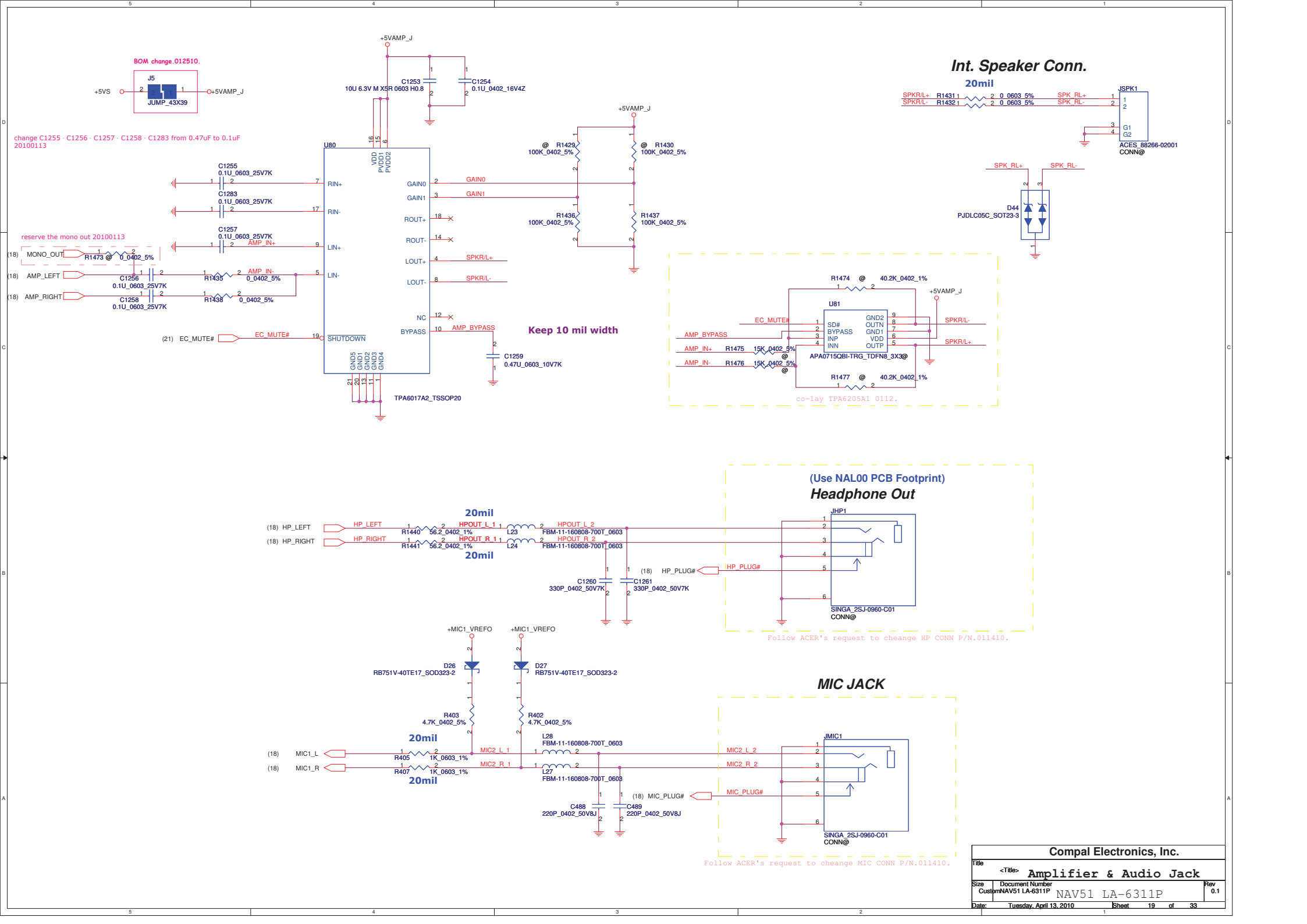
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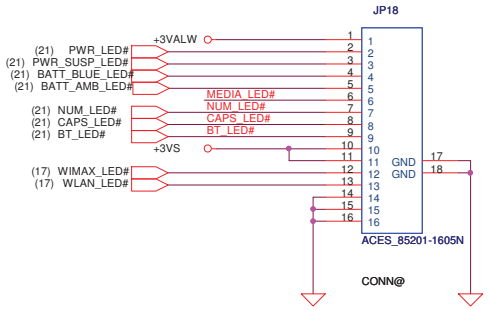
Title: HD Audio Codec ALC272

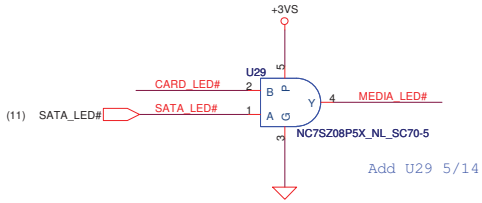
Size: Custom | Document Number: NAV51 LA-6311P | Rev: 1.0

Date: Tuesday, April 13, 2010 | Sheet 18 of 33

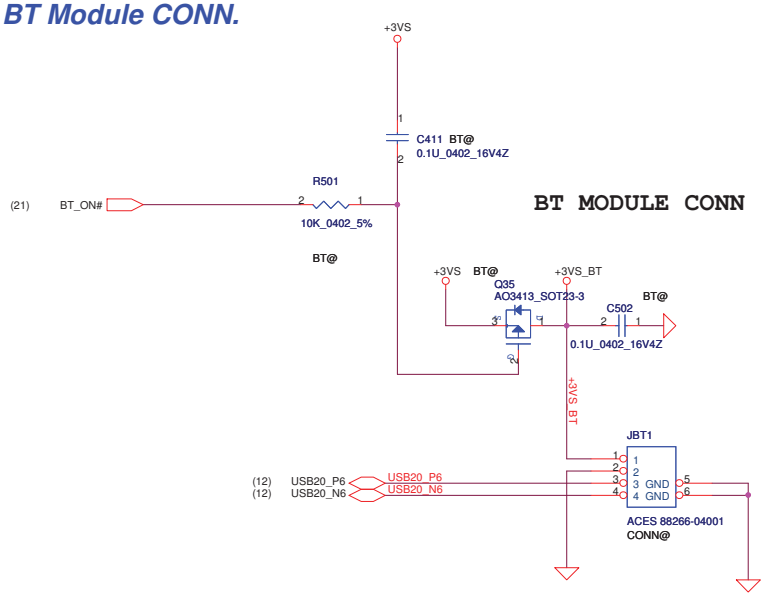

BOM change.012510.
J5
JUMP_43X39
+5VS
+5VAMP_J
change C1255 · C1256 · C1257 · C1258 · C1283 from 0.47uF to 0.1uF
20100113
U80
TPA6017A2_TSSOP20
C1253
10U 6.3V M X5R 0603 H0.8
C1254
0.1U_0402_16V4Z
C1255
0.1U_0603_25V7K
C1283
0.1U_0603_25V7K
C1257
0.1U_0603_25V7K
C1256
0.1U_0603_25V7K
C1258
0.1U_0603_25V7K
C1259
0.47U_0603_10V7K
reserve the mono out 20100113
MONO_OUT
AMP_LEFT
AMP_RIGHT
R1473 @ 0_0402_5%
R1435 0_0402_5%
R1438 0_0402_5%
AMP_IN+
AMP_IN-
EC_MUTE#
AMP_BYPASS
SPKR/L+
SPKR/L-
GAIN0
GAIN1
R1429 @ 100K_0402_5%
R1430 @ 100K_0402_5%
R1436 100K_0402_5%
R1437 100K_0402_5%
Keep 10 mil width
Int. Speaker Conn.
20mil
R1431 0_0603_5%
R1432 0_0603_5%
SPK_RL+
SPK_RL-
JSPK1
ACES_88266-02001
CONN@
D44
PJDLC05C_SOT23-3
R1474 @ 40.2K_0402_1%
R1475 15K_0402_5% @
R1476 15K_0402_5% @
R1477 @ 40.2K_0402_1%
U81
APA0715QBI-TRG_TDFN8_3X3@
co-lay TPA6205A1 0112.
(Use NAL00 PCB Footprint)
Headphone Out
HP_LEFT
HP_RIGHT
HPOUT_L_1
HPOUT_R_1
HPOUT_L_2
HPOUT_R_2
R1440 56.2_0402_1%
R1441 56.2_0402_1%
L23 FBM-11-160808-700T_0603
L24 FBM-11-160808-700T_0603
C1260 330P_0402_50V7K
C1261 330P_0402_50V7K
HP_PLUG#
JHP1
SINGA_2SJ-0960-C01
CONN@
Follow ACER's request to cheange HP CONN P/N.011410.
+MIC1_VREFO
D26 RB751V-40TE17_SOD323-2
D27 RB751V-40TE17_SOD323-2
R403 4.7K_0402_5%
R402 4.7K_0402_5%
MIC1_L
MIC1_R
MIC2_L_1
MIC2_R_1
MIC2_L_2
MIC2_R_2
R405 1K_0603_1%
R407 1K_0603_1%
L28 FBM-11-160808-700T_0603
L27 FBM-11-160808-700T_0603
C488 220P_0402_50V8J
C489 220P_0402_50V8J
MIC_PLUG#
MIC JACK
JMIC1
SINGA_2SJ-0960-C01
CONN@
Follow ACER's request to cheange MIC CONN P/N.011410.
Compal Electronics, Inc.
Title
<Title> Amplifier & Audio Jack
Size Custom
Document Number NAV51 LA-6311P
NAV51 LA-6311P
Rev 0.1
Date: Tuesday, April 13, 2010
Sheet 19 of 33

LED PCB CONN.

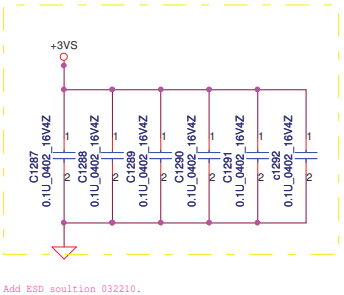




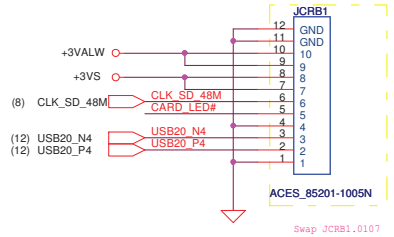
BT Module CONN.



ESD



Card Reader CONN.



Security Classification	Compal Secret Data		
Issued Date	2009/01/22	Deciphered Date	2009/11/20

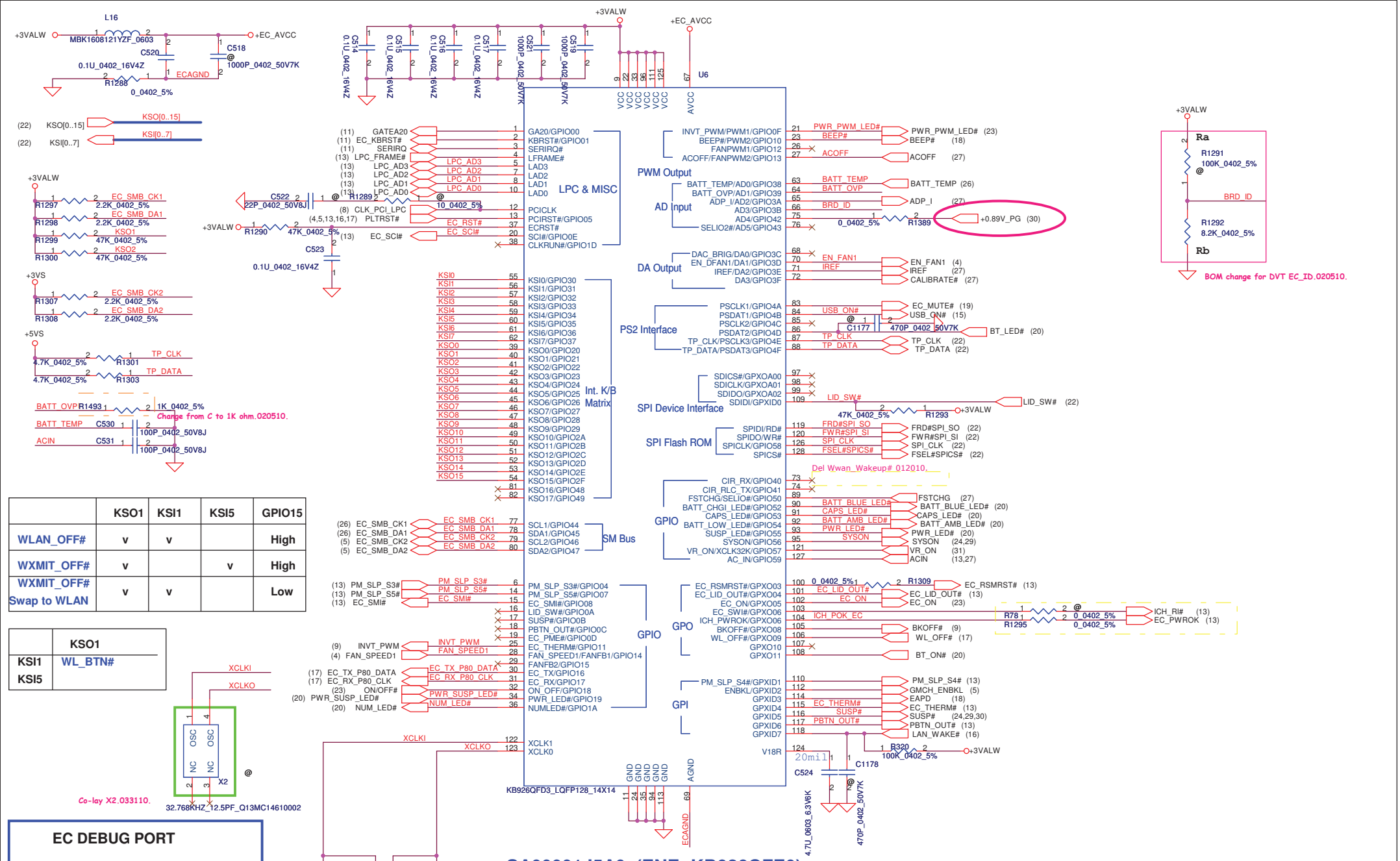
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Compal Electronics, Inc.

Title: **Card reader**

Size: Custom | Document Number: **NAV51 LA-6311P** | Rev: 0.1

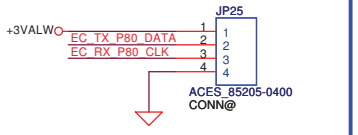
Date: Tuesday, April 13, 2010 | Sheet 20 of 33



	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_OFF# Swap to WLAN	v	v		Low

	KSO1
KSI1	WL_BTN#
KSI5	

EC DEBUG PORT



Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2007/8/18

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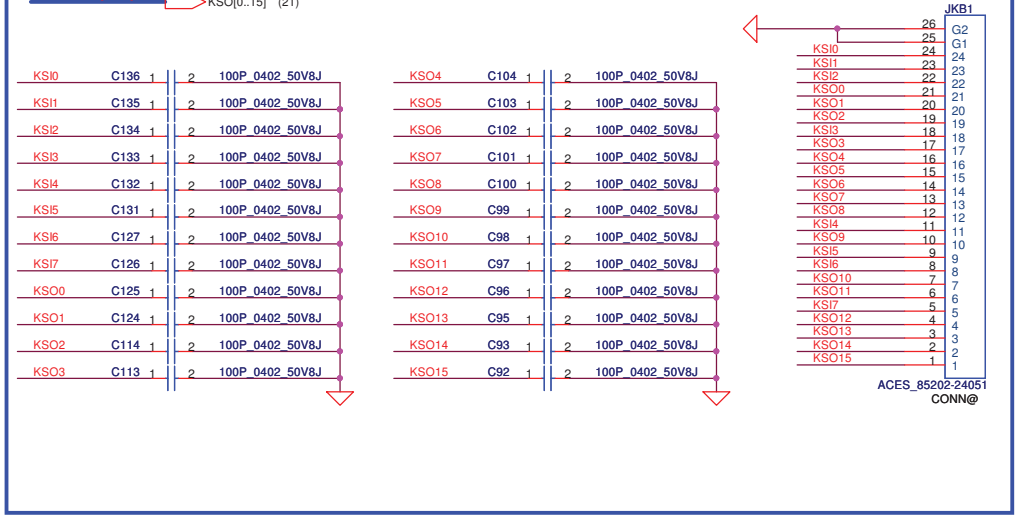
Compal Electronics, Inc.

Title: KB926/BIOS

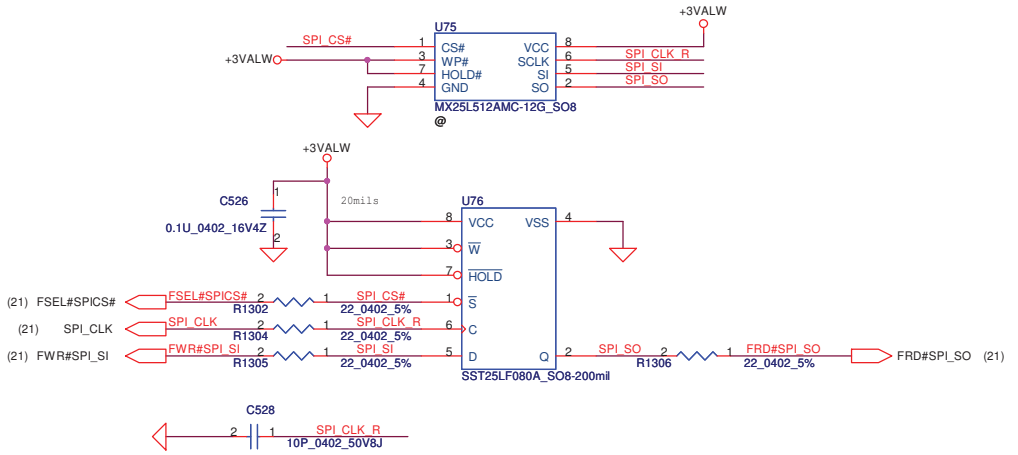
Size	Document Number	Rev
Custom	NAV51 LA-6311P	1.0

Date: Tuesday, April 13, 2010 | Sheet 21 of 33

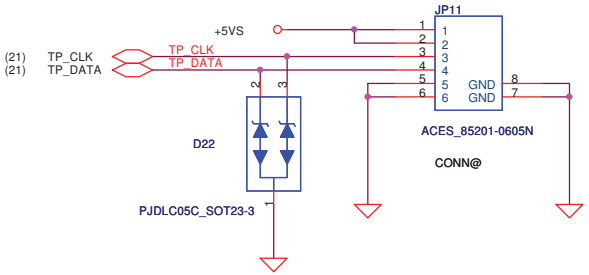
INT_KBD Conn.



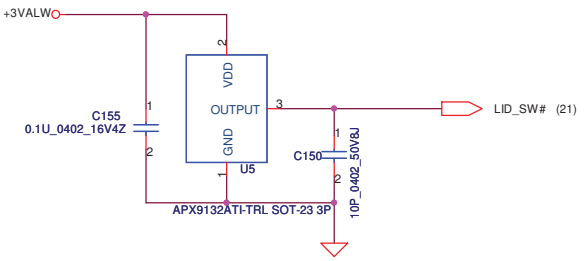
8M SPI ROM



To TP/B Conn.



LID Switch



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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Compal Electronics, Inc.

Title: KB CONN/TP/LID SW

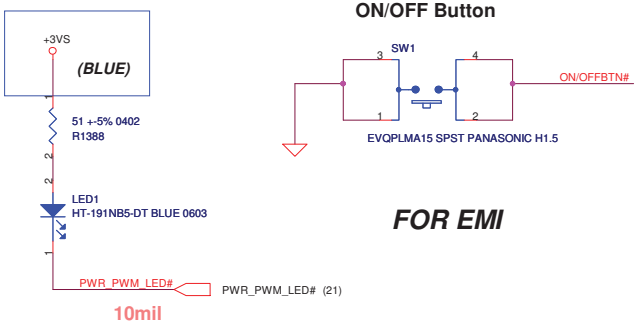
Size: B | Document Number: NAV51 LA-6311P | Rev: 0.2

Date: Tuesday, April 13, 2010 | Sheet 22 of 33

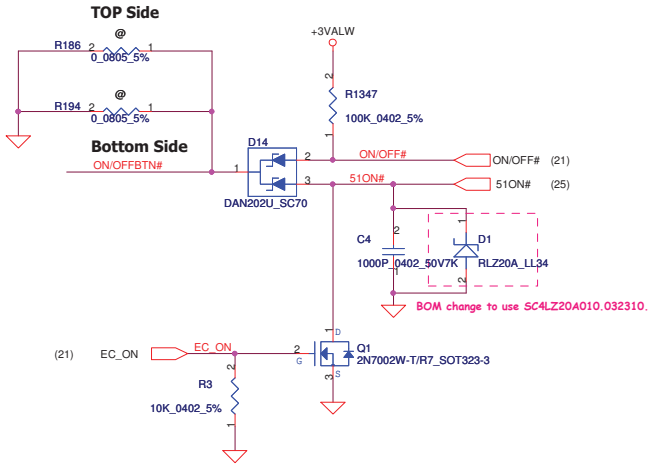
Add For NAV50 07/06

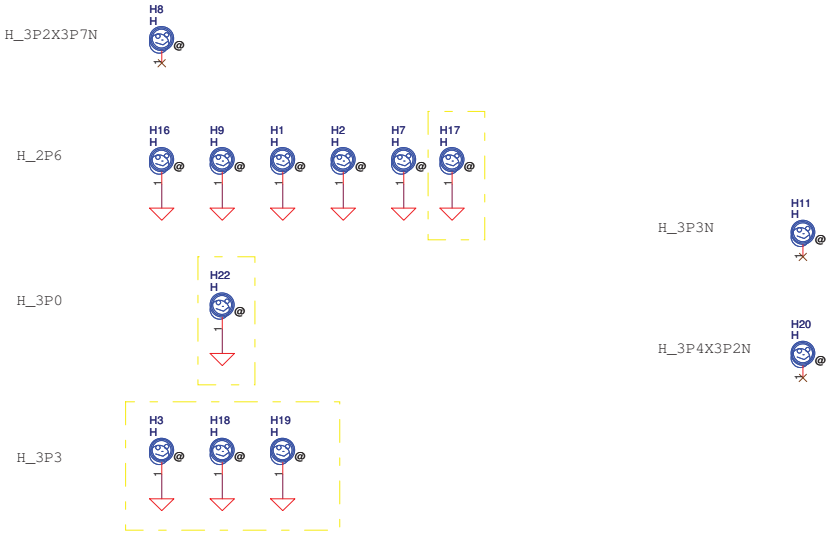
09/03 Change +5VS to +3VS

ON/OFF Button



Power Button Logic







Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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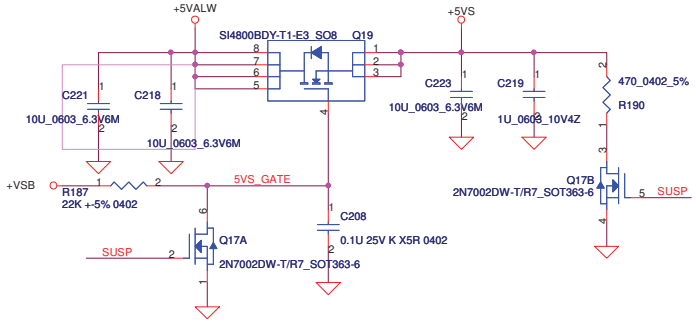
Compal Electronics, Inc.

Title: ON/OFF / LID SW

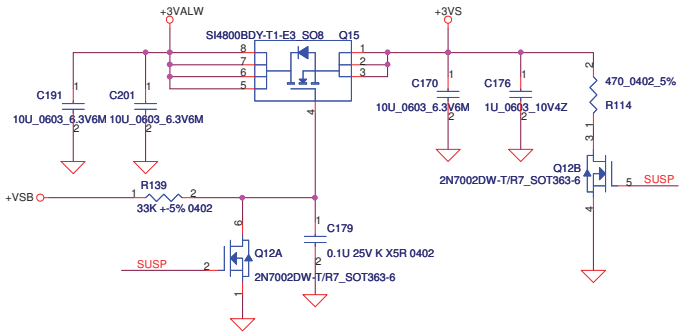
Size	Document Number	Rev
B	NAV51 LA-6311P	0.2

Date: Tuesday, April 13, 2010 Sheet 23 of 33

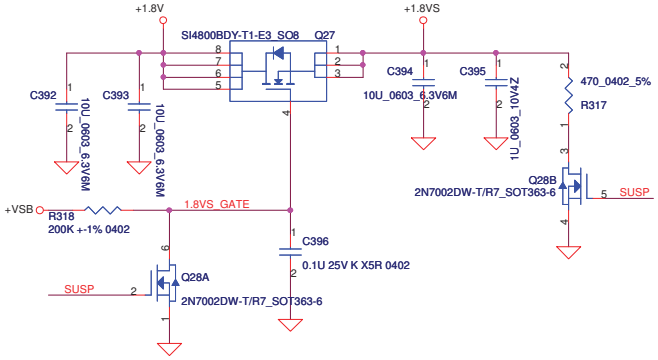
+5VALW TO +5VS

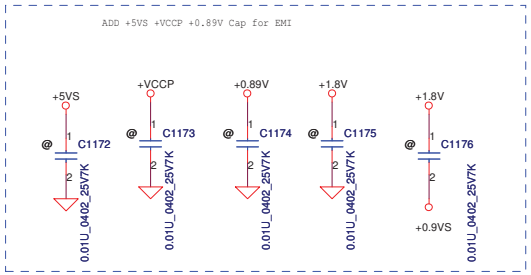


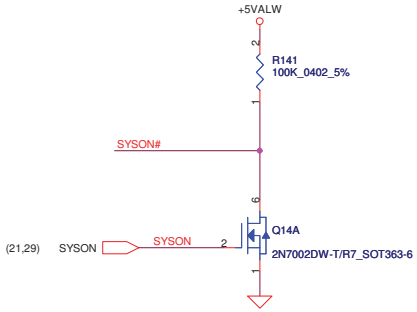
+3VALW TO +3VS

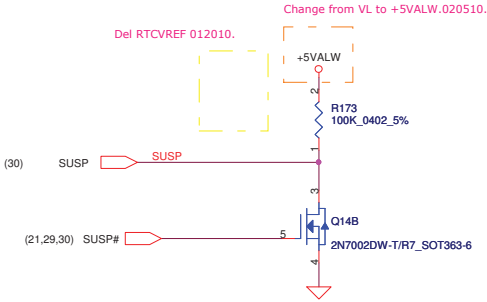


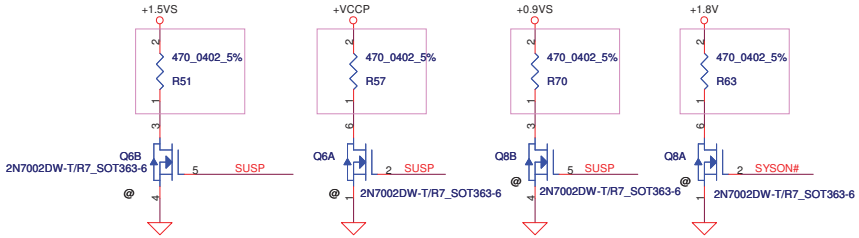
+1.8V to +1.8VS











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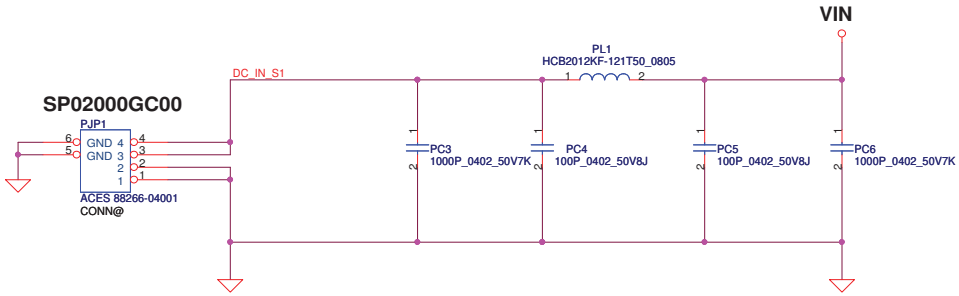
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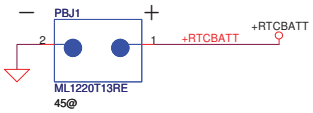
Compal Electronics, Inc.

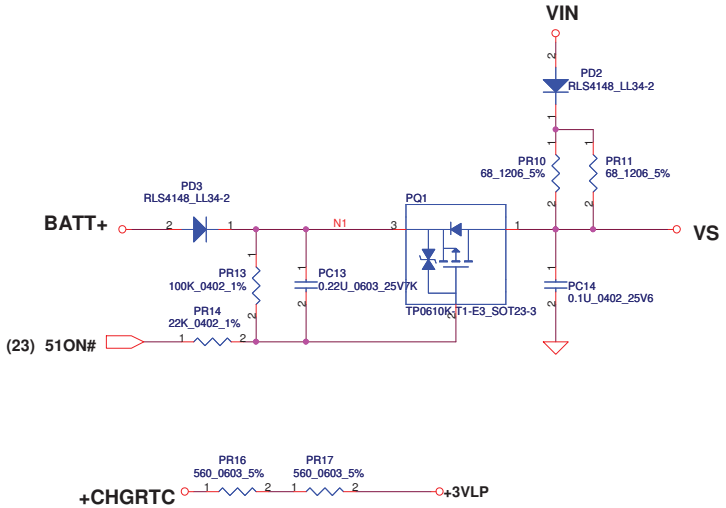
Title: DC INTERFACE

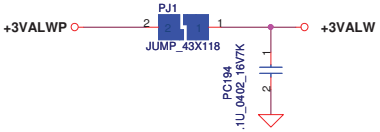
Size	Document Number	Rev
B	NAV51 LA-6311P	0.2

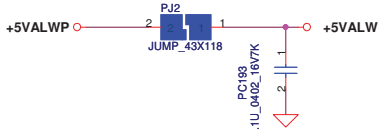
Date: Tuesday, April 13, 2010 Sheet 24 of 33

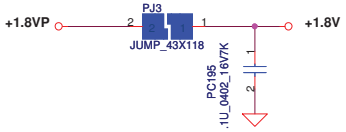


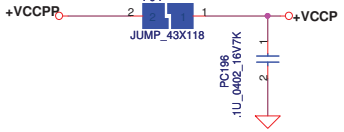


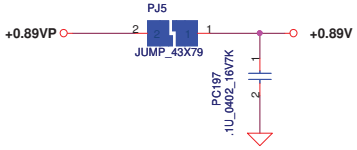












Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

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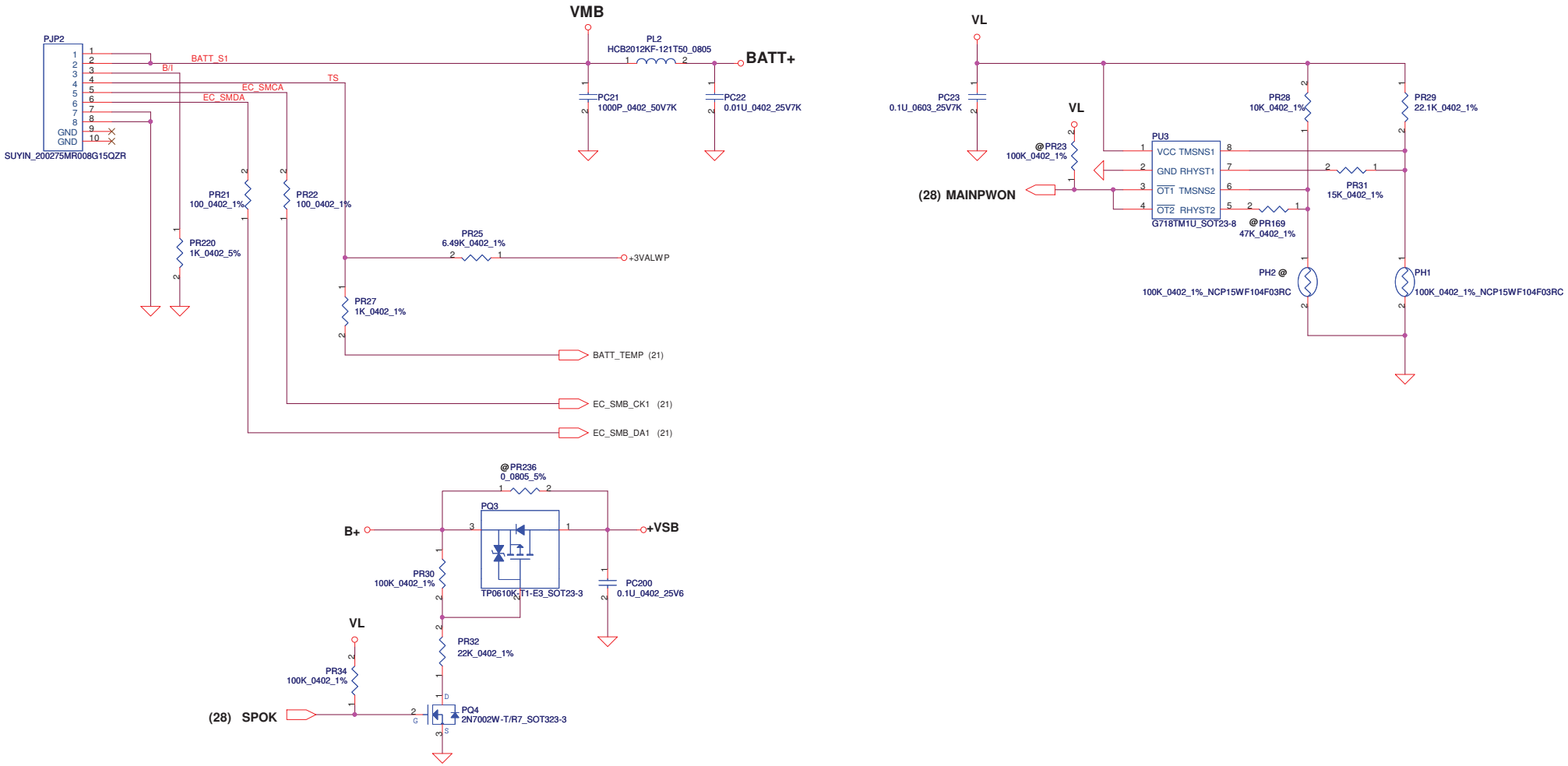
Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom	NAV51 LA-6311P	0.1

Date: Wednesday, April 14, 2010 | Sheet 25 of 32

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

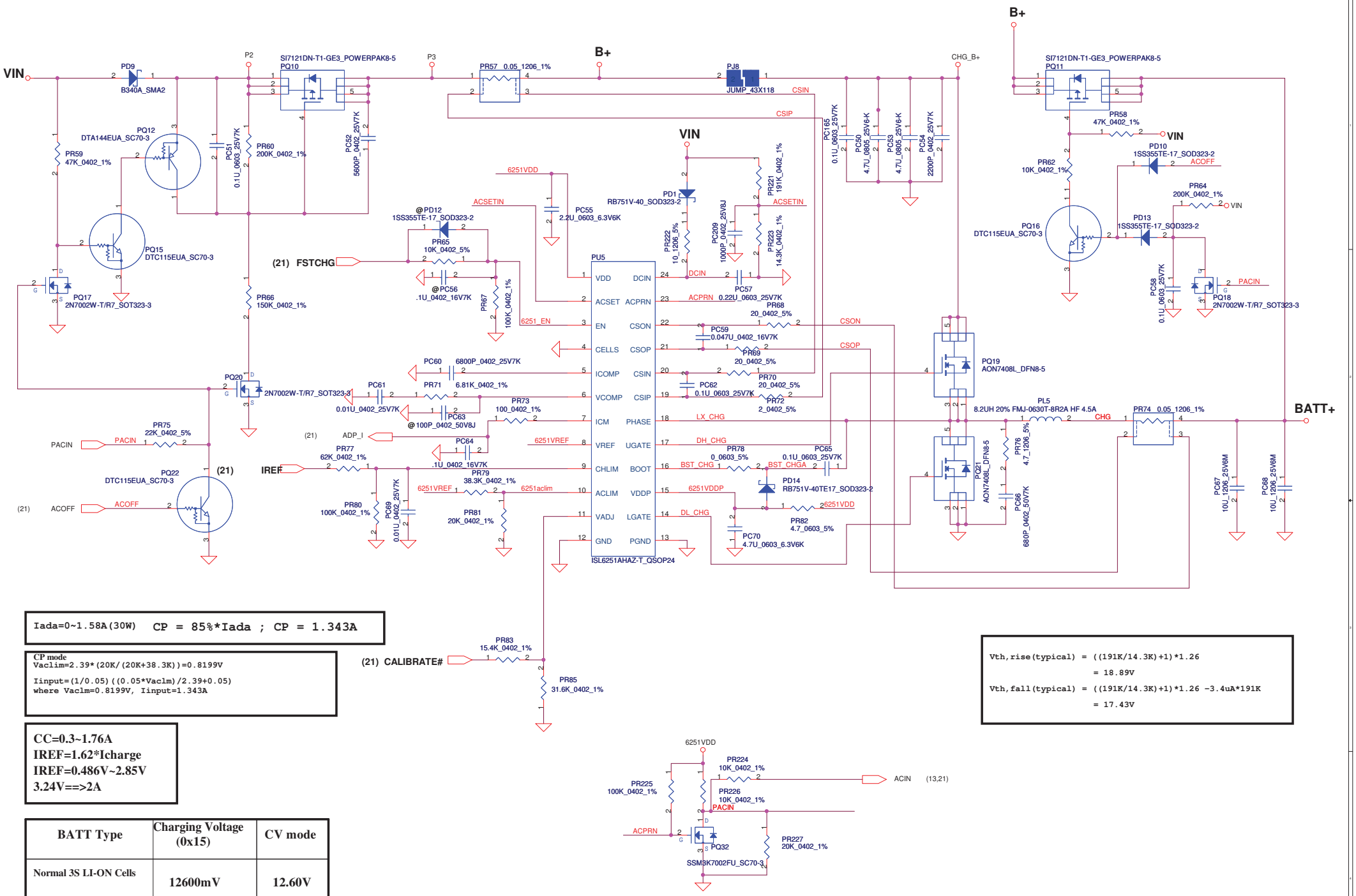
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Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
Custom	NAV51 LA-6311P	0.1

Date: Wednesday, April 14, 2010 | Sheet 26 of 33



Iada=0~1.58A(30W) CP = 85%*Iada ; CP = 1.343A

CP mode
Vaclim=2.39*(20K/(20K+38.3K))=0.8199V

Iinput=(1/0.05)((0.05*Vaclm)/2.39+0.05)
where Vaclm=0.8199V, Iinput=1.343A

CC=0.3~1.76A
IREF=1.62*Icharge
IREF=0.486V~2.85V
3.24V==>2A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

VADJ-->VREF-->4.41V

VADJ--->Ground--->3.99V

Vcell=(0.175*VADJ+3.99)

Vth,rise(typical) = ((191K/14.3K)+1)*1.26
= 18.89V

Vth,fall(typical) = ((191K/14.3K)+1)*1.26 -3.4uA*191K
= 17.43V

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

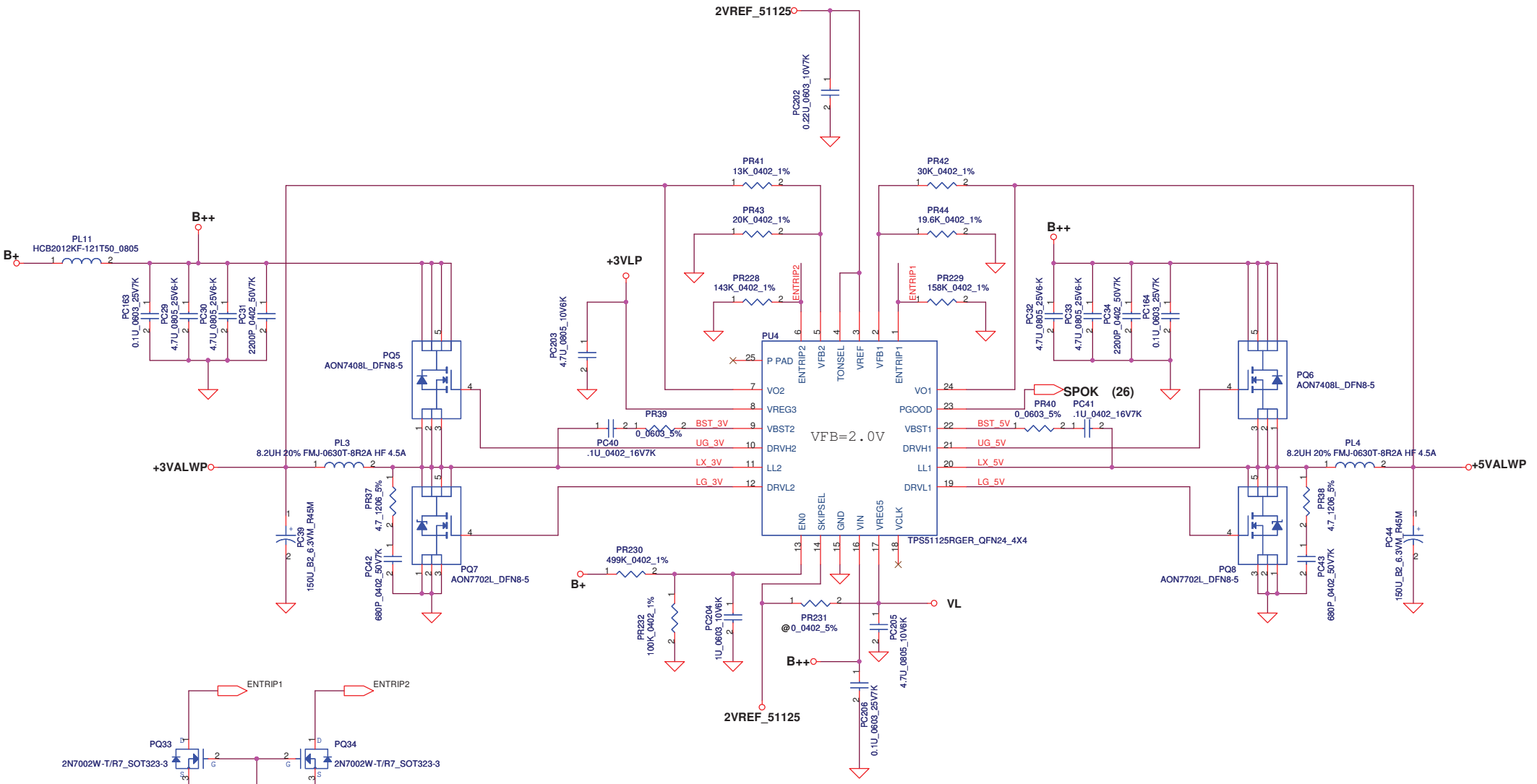
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Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NAV51 LA-6311P | Rev: 0.1

Date: Wednesday, April 14, 2010 | Sheet 27 of 33



+3.3VALWP Ipeak=5.731A Imax=4.012A
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vtrip=(10E-06 * 130K)/9-24mV=134.9mV
Ilimit=134.9mV/17.9m ~134.9mV/14.5m x 1.2
=7.536A ~ 7.752A
Iocp=Ilimit+Delta I/2
=8.081A ~ 8.297A
Delta I=1.090A (Freq=305KHz)

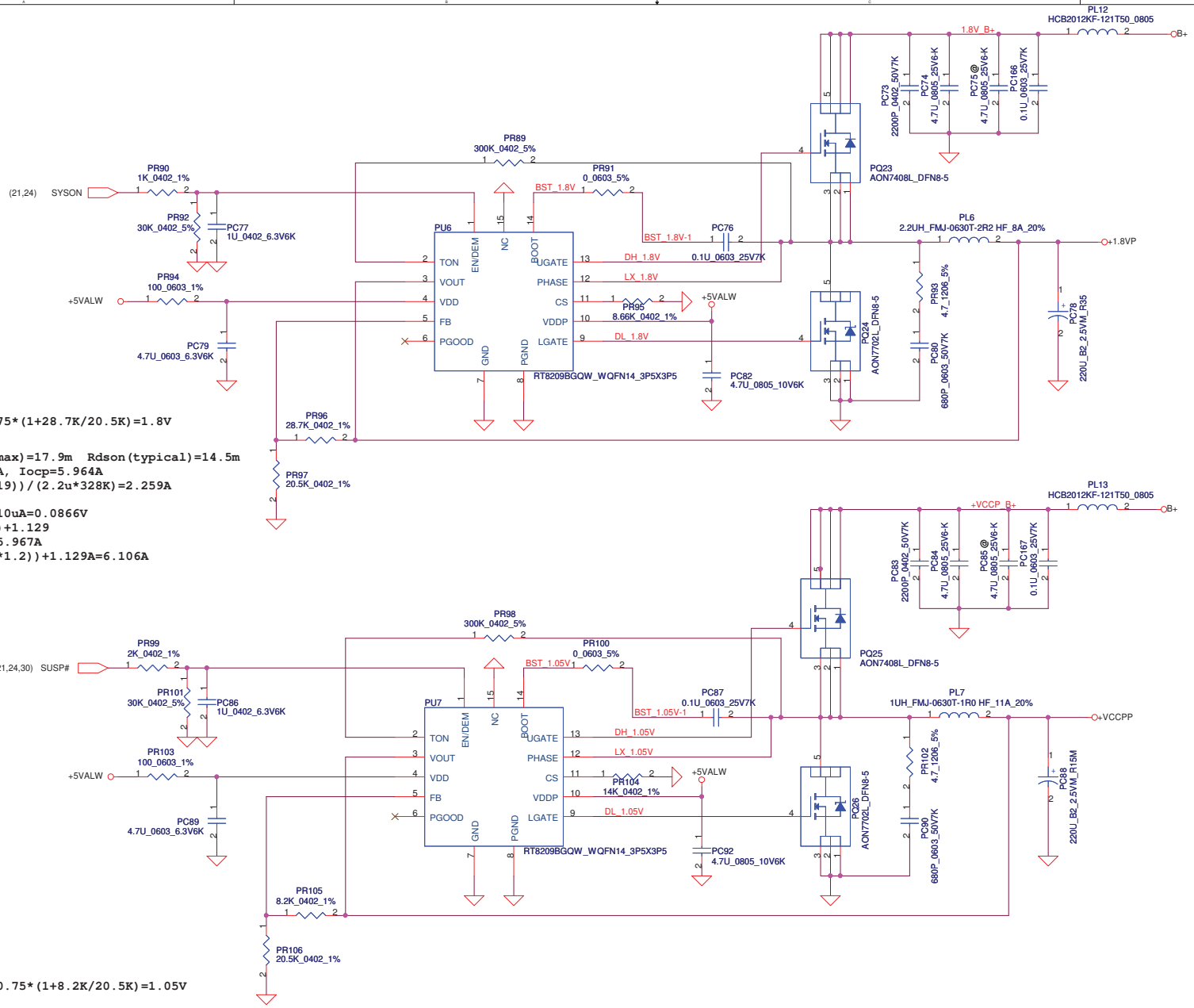
+5VALWP Ipeak=7.0A Imax=4.9A
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vtrip=(10E-06 * 147K)/9-24mV=151mV
Ilimit=151mV/17.9m ~151mV/14.5m x 1.2
=8.467A ~ 8.710A
Iocp=Ilimit+Delta I/2
=9.384A ~ 9.627A
Delta I=1.834A (Freq=245KHz)

Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

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Compal Electronics, Inc.

Title	+5V/+3V	
Size: Custom	Document Number: NAV50	Rev: 0.1
Date: Wednesday, April 14, 2010	Sheet 28 of 33	



<Vo=1.8V> VFB=0.75V
Vo=VFB*(1+PR96/PR97)=0.75*(1+28.7K/20.5K)=1.8V
Fsw=328KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(typical)=14.5m
Ipeak=4.97A, Imax=3.479A, Iocp=5.964A
Delta I=((19-1.8)*(1.8/19))/(2.2u*328K)=2.259A
=>1/2DeltaI=1.129A
Vtrip=Rtrip*10uA=8.66K*10uA=0.0866V
Iocpmin=Vtrip/(Rdsonmax)+1.129
=0.0866/(0.0179)+1.129=5.967A
Iocpmax=(0.0866/(0.0145*1.2))+1.129A=6.106A
Iocp=5.967A~6.106A

<Vo=1.05V> VFB=0.75V
Vo=VFB*(1+PR105/PR106)=0.75*(1+8.2K/20.5K)=1.05V
Fsw=280KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(typical)=14.5m
Ipeak=3.124A, Imax=2.187A, Iocp=3.749A
Delta I=((19-1.05)*(1.05/19))/(1.5u*280K)=3.549A
=>1/2DeltaI=1.774A
Vtrip=Rtrip*10uA=14K*10uA=0.14V
Iocpmin=Vtrip/(Rdsonmax)+1.774
=0.14/(0.0179)+1.774=9.596A
Iocpmax=(0.14/(0.0145*1.2))+1.774A=9.820A
Iocp=9.596A~9.820A

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

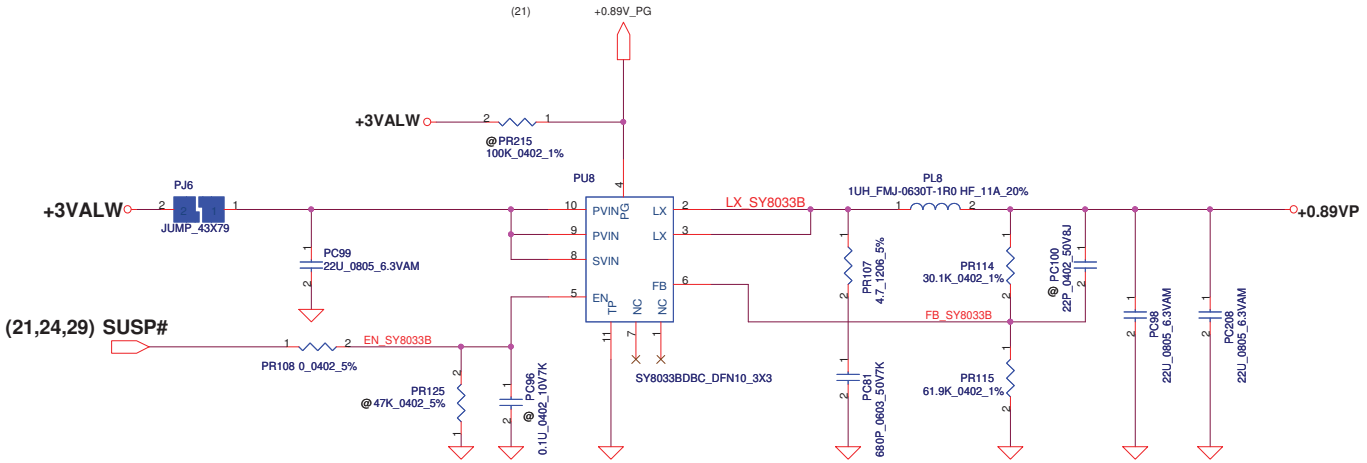
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Compal Electronics, Inc.

Title: 1.8VP / +VCCPP

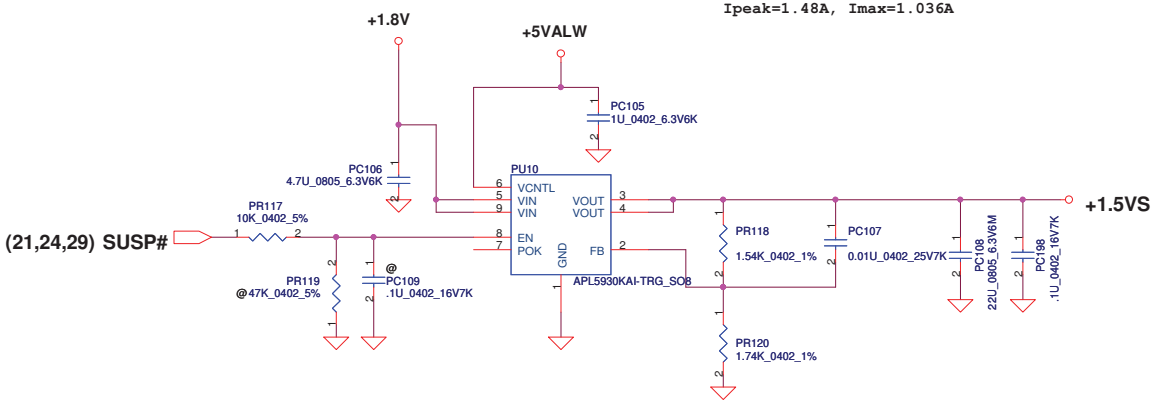
Size: Custom | Document Number: NAV51 LA-6311P | Rev: 0.1

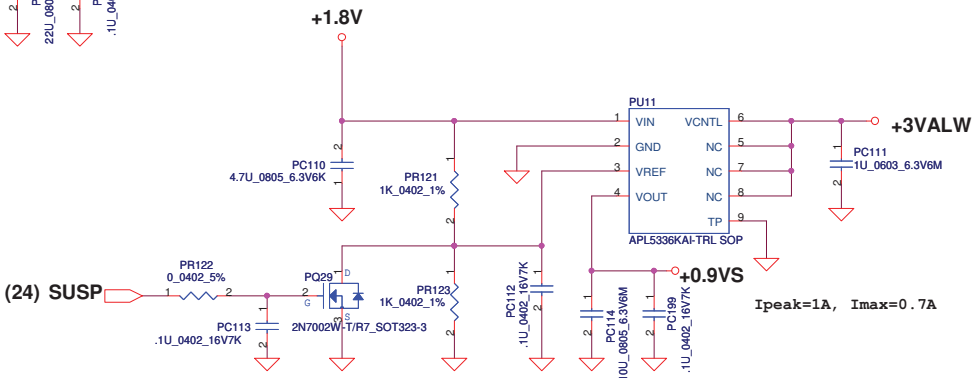
Date: Wednesday, April 14, 2010 | Sheet 29 of 33



<Vo=0.89V> VFB=0.6V
Vo=VFB*(1+PR114/PR115)=0.6*(1+30.1K/61.9)=0.89V
Ipeak=2.64A, Imax=1.848A

Ipeak=1.48A, Imax=1.036A





Ipeak=1A, Imax=0.7A

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

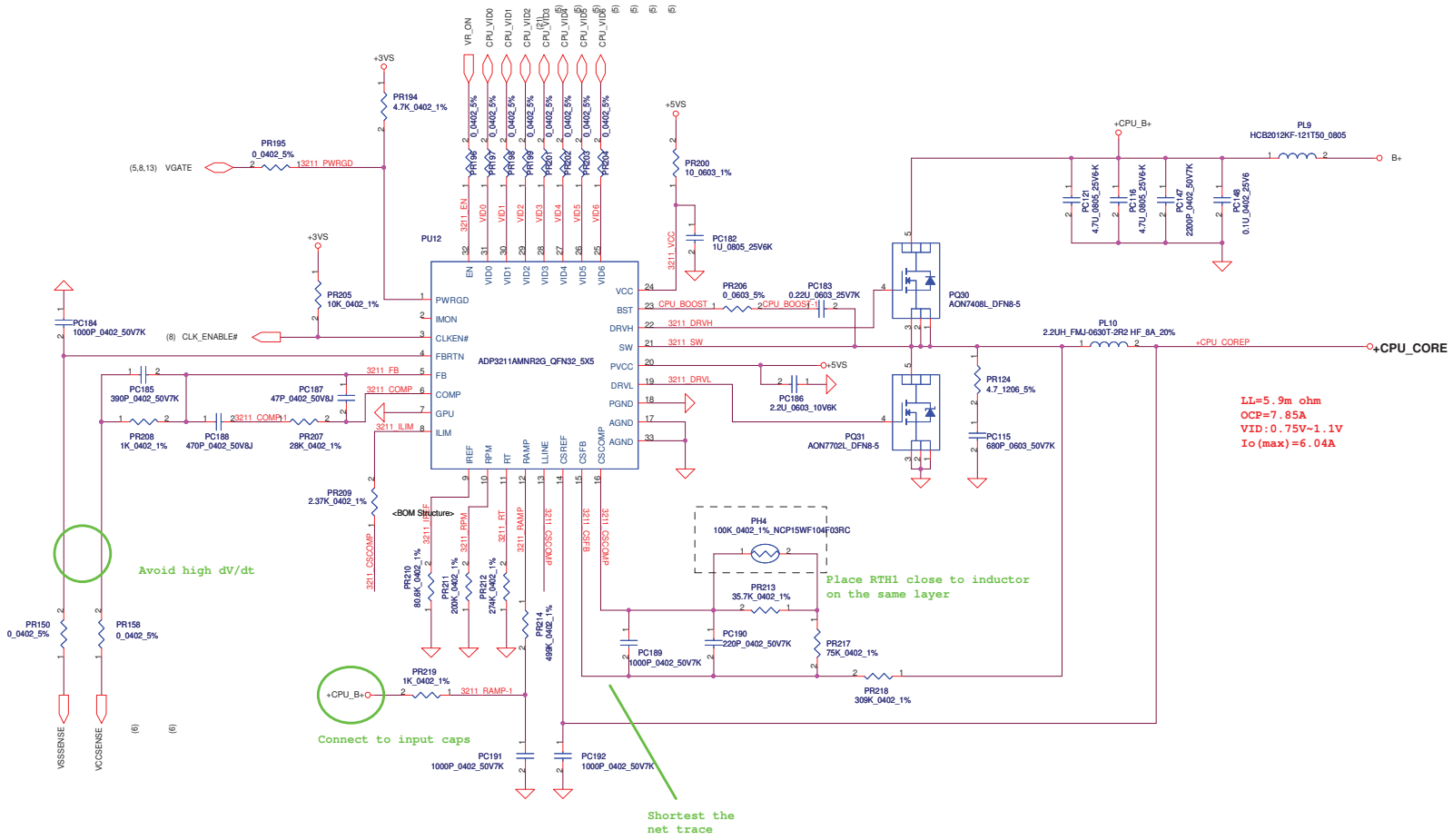
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Title: +0.89VP/+1.5VS/+0.9VSP

Size	Document Number	Rev
Custom	NAV51 LA-6311P	0.1

Date: Wednesday, April 14, 2010 | Sheet 30 of 33



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Title: +CPU_CORE

Size	Document Number	Rev
C	NAV51 LA-6311P	0.1

Date: Wednesday, April 14, 2010 Sheet 31 of 33

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1						2010.1.8	EVT
2						2010.1.11	EVT
3							
4							
5							
6							
7							
8							
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22							
23							

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2007/8/18

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Title	PIR_HW	
Size: Custom	Document Number: NAV51 LA-6311P	Rev: 1.0
Date: Wednesday, April 14, 2010	Sheet 32 of 33	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	PU8 Vin change to +3VALW	modify for HW layout request	0.1	30		2010.1.8	EVT
2	PU4 Pin25 change to no connect	modify for 3/5V load balance(TI FAE request)	0.1	28		2010.1.11	EVT
3							
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23							

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: NAV51 LA-6311P | Rev: 0.1

Date: Wednesday, April 14, 2010 | Sheet 33 of 33