Compal Confidential

PIQY0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
nVIDIA N12P-GT

2010-12-30

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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File Name : PIQY0

ZZZ1 DAZ0HA00100
ZZZ2 X7625738L01 X761G@
ZZZ3 X7625738L03 X762G@
ZZZ4 LS6881P DAZ@
ZZZ5 LS6882P DAZ@
ZZZ6 LS6883P DAZ@
ZZZ7 LA6881P DAZ@

POWER & ALS BOARD

CAP SENSOR & Slid bar BOARD

nVIDIA N12P-GT
VRAM 64*16 DDR3*8

PCI-E X16

Intel Sandy Bridge
Socket-rPGA988B
37.5mm*37.5mm

DDR3-SO-DIMM X2
BANK 0, 1, 2, 3
UP TO 8G

Dual Channel
DDR3-1066(1.5V)
DDR3-1333(1.5V)

100MHz 2.7GT/s
FDI *8
DMI *4

HDMI CONN
Passive level shift
CRT Connector
LVDS Connector
optimus 1.0
optimus 1.0

Intel Cougar Point
FCBGA 951
25mm*25mm

AZALIA
Audio Codec
RealTek ALC272/ALC5503
2Channel Speaker
Array Digital MIC
Audio Jacks
Stereo HeadPhone Output
Microphone Input

14*USB2.0
CMOS Camera
BlueTooth CONN
USB PORT 2.0 x2(Left)
Option3.0 x2
WLAN/WiMAX
USB PORT 2.0 x1(Right)

6*SATA serial
(port0,1 support SATA3)
ESATA HDD AND USB CONN (Right)
SATA3.0 HDD CONN
SATA3.0 HDD (SSD)
SATA ODD CONN

6*PCI-E BUS

PCI Express Mini card Slot 1
WLAN/WiMAX
USB(WiMAX)
PCI-E(WLAN)

PCI Express Mini card Slot 2
SSD
SATA(SSD)

USB3.0
RENESAS UPD720200

Card Reader
Jmicro JMB389
SD/MMC/MS/XD

WLAN/WiMAX

Broadcom
BCM57781/57780
10/100/1G LAN
RJ45 CONN

SPI ROM BIOS

LPC BUS

EC
ENE KB930

Int.KBD
SPI ROM
Touch Pad
Thermal Sensor
EMC1403

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	VENTURA@
Camera	CMOS@

VRAM BOM Config

X761G@: X7625738L01 Samsung 1GB
Sub: X7625738L02 Hynix 1GB
X762G@: X7625738L03 Samsung 2GB
Sub: X7625738L04 Hynix 2GB

GPU BOM Config

N12P SKU: OPTI@
GS SKU: GS@
GT SKU: GT@

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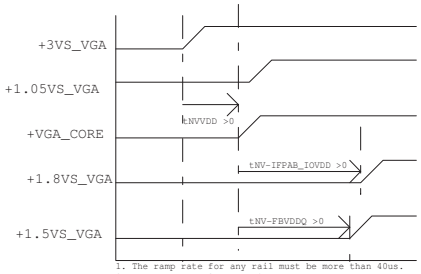
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Title: Notes List

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1. The ramp rate for any rail must be more than 40us.
2. +VGA_CORE <= +3VS_VGA +0.5V
3. +1.5VS_VGA <= +3VS_VGA +0.5V
4. Optimus follows power sequencing rules
   specified in discrete GPU design guide.

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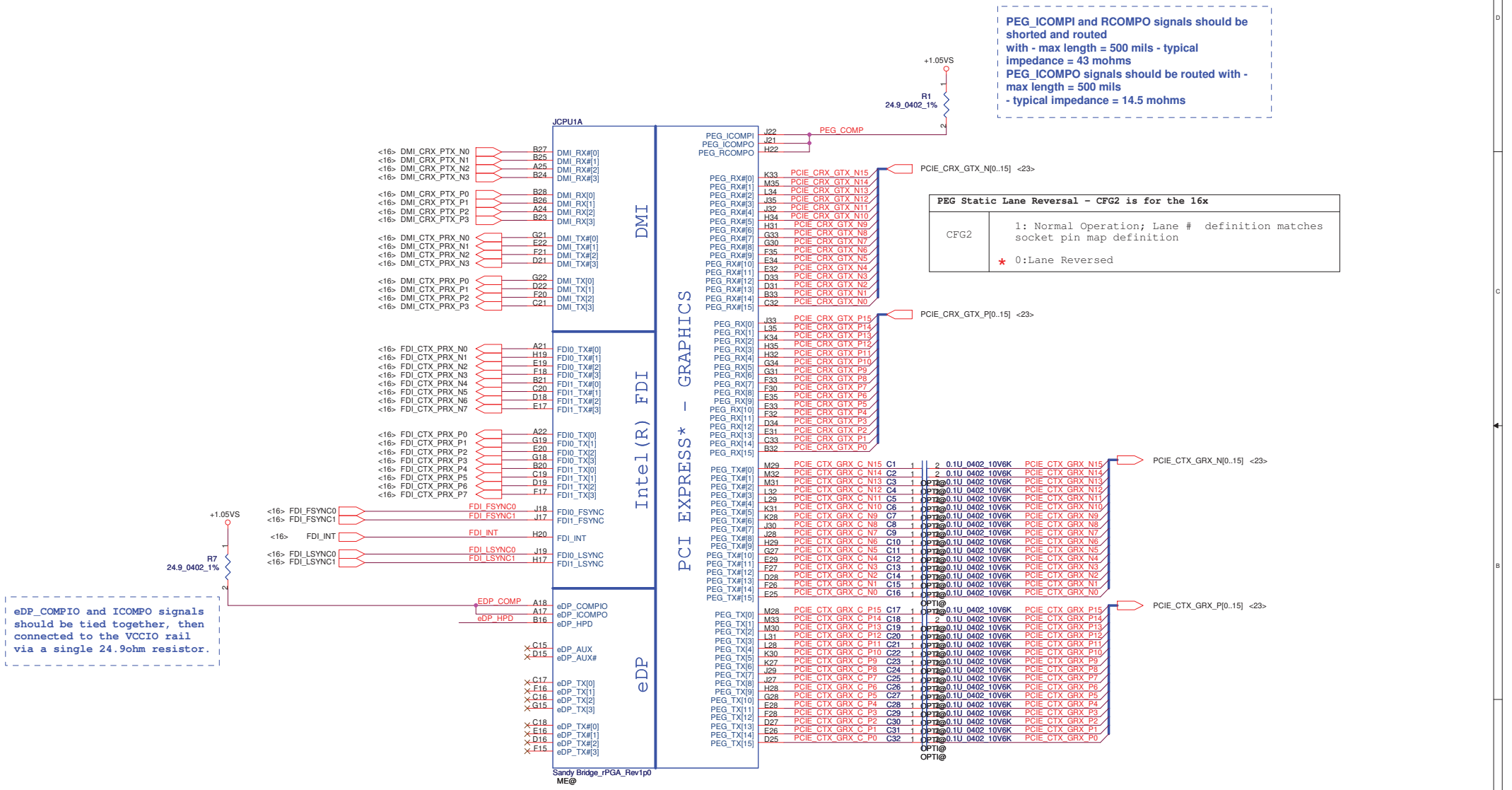
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Title: **VGA Notes List**

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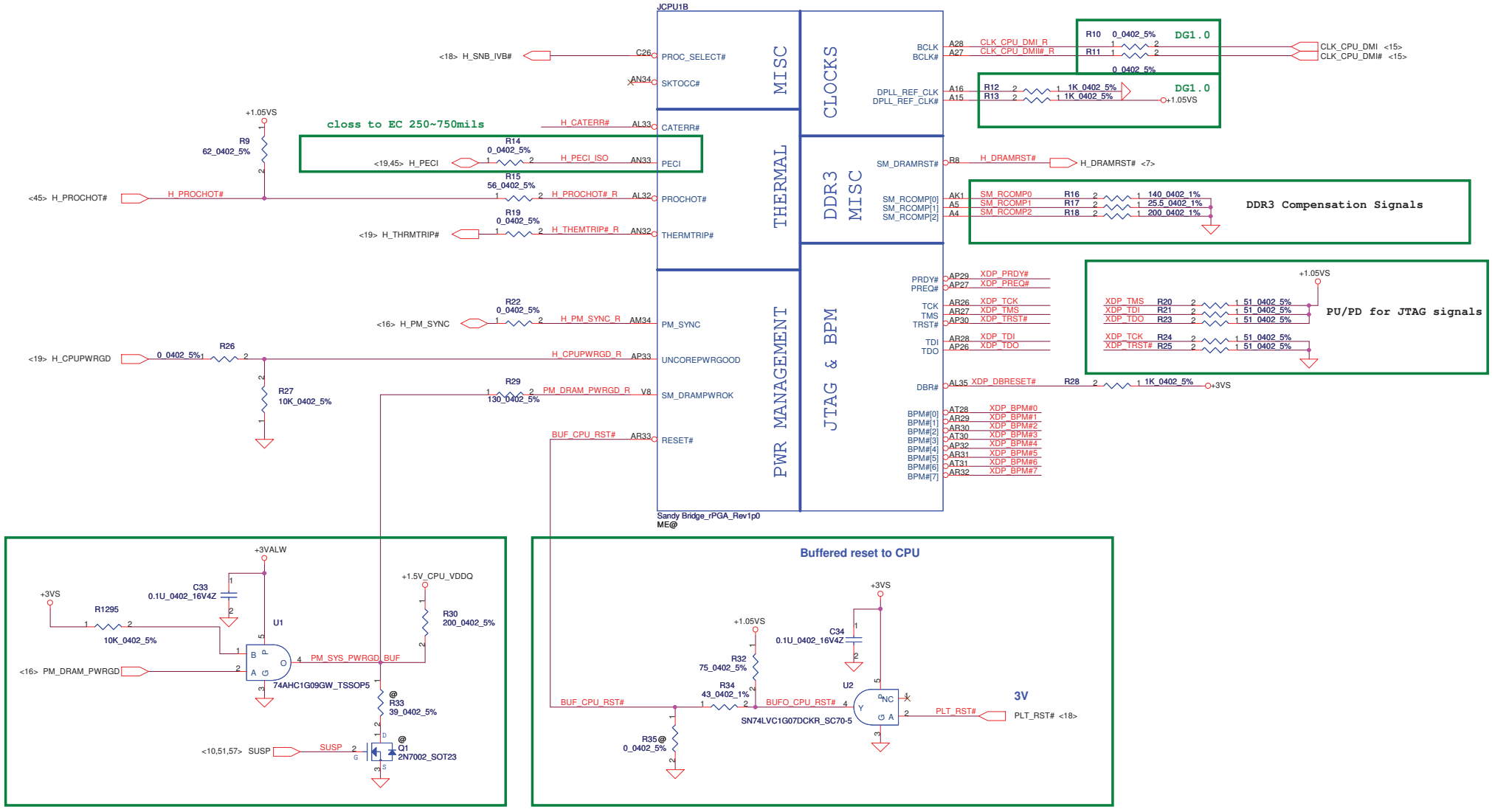
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Title: PROCESSOR(1/7) DMI,FDI,PEG

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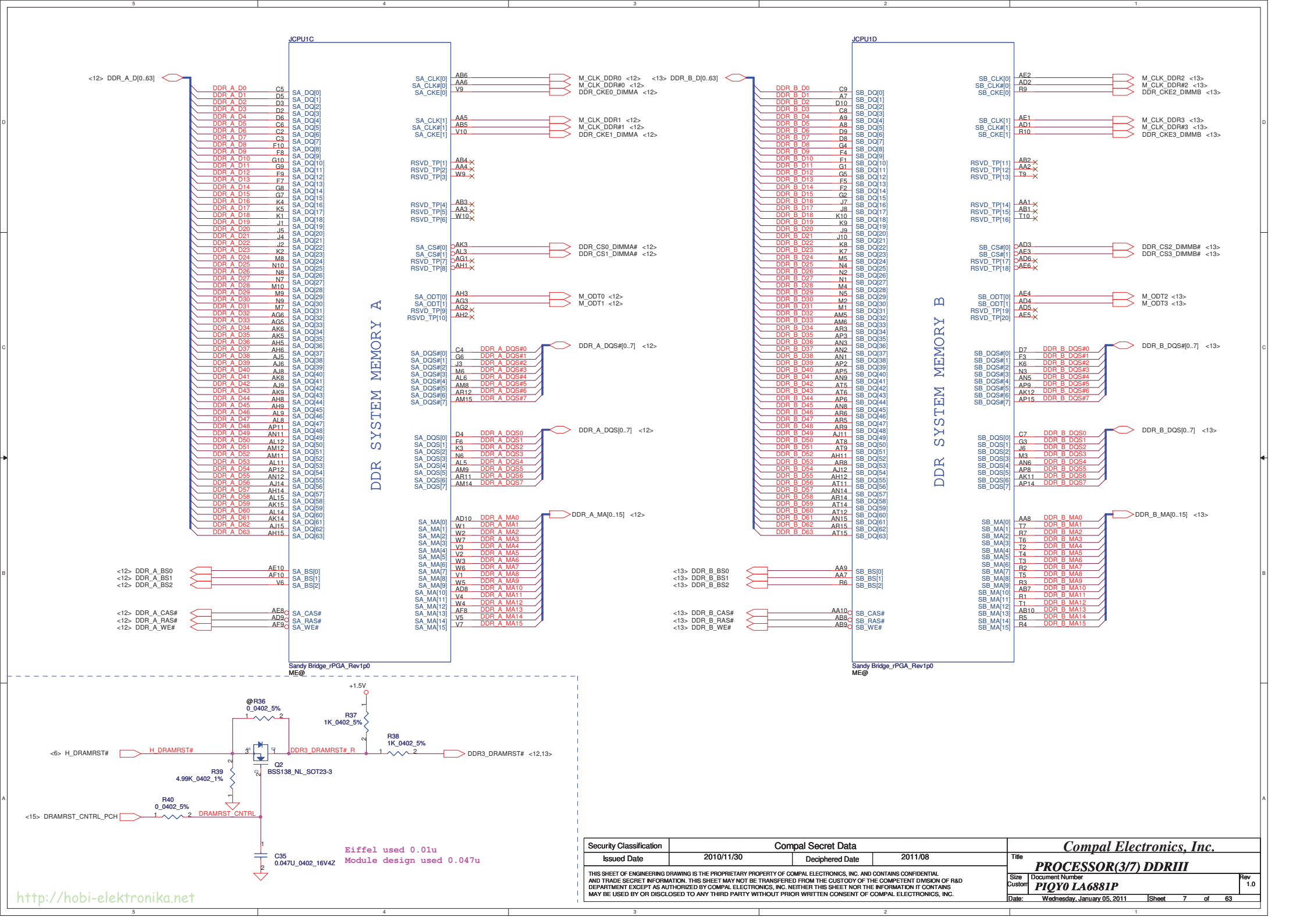


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Title: PROCESSOR(2/7) PM,XDP,CLK			
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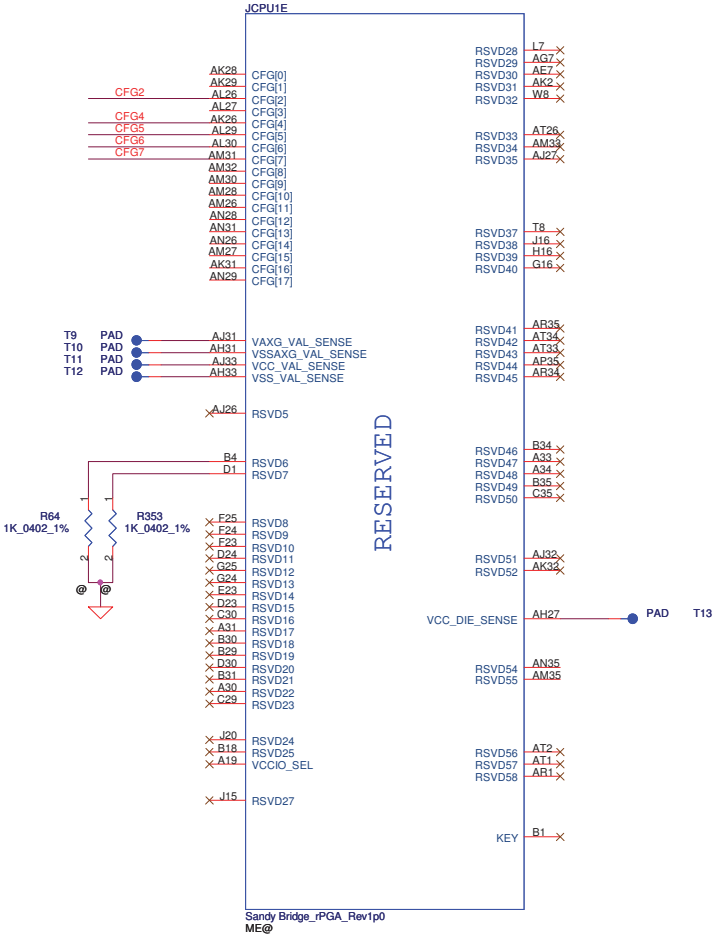
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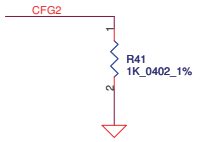
Title: **PROCESSOR(3/7) DDRIII**

Size	Document Number	Rev
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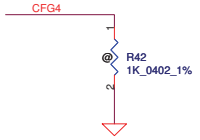
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CFG Straps for Processor

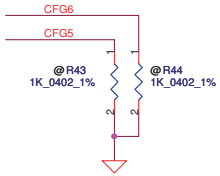




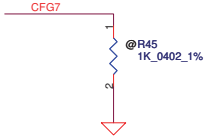
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

+CPU_CORE

(6/16 change 10uF_0603_6.3V)*5

C36 10U_0805_6.3V6M
C37 10U_0805_6.3V6M
C38 10U_0805_6.3V6M
C39 10U_0805_6.3V6M
C40 10U_0805_6.3V6M
C48 10U_0603_6.3V6M
C49 10U_0603_6.3V6M
C50 10U_0603_6.3V6M
C51 10U_0603_6.3V6M
C52 10U_0603_6.3V6M
C53 @ 10U_0603_6.3V6M

QC=94A
DC=53A

+CPU_CORE

(22uF_0805_6.3V)*16

C66 22U_0805_6.3V6M
C67 22U_0805_6.3V6M
C68 22U_0805_6.3V6M
C70 22U_0805_6.3V6M
C71 22U_0805_6.3V6M
C74 22U_0805_6.3V6M
C75 22U_0805_6.3V6M
C76 22U_0805_6.3V6M
C77 22U_0805_6.3V6M
C78 22U_0805_6.3V6M
C79 22U_0805_6.3V6M
C80 22U_0805_6.3V6M
C81 22U_0805_6.3V6M
C82 22U_0805_6.3V6M
C83 22U_0805_6.3V6M
C84 22U_0805_6.3V6M
C85 @ 22U_0805_6.3V6M
C86 @ 22U_0805_6.3V6M
C87 @ 22U_0805_6.3V6M

+CPU_CORE

(330uF)*4

C88 330U_X_2VM_R8M
C89 330U_X_2VM_R8M
C90 330U_X_2VM_R8M
C91 330U_X_2VM_R8M

DUAL@ DUAL@ DUAL@ DUAL@

C88 470U_D2_2VM_R4.5M QUAD@
C89 470U_D2_2VM_R4.5M QUAD@
C90 470U_D2_2VM_R4.5M QUAD@
C91 470U_D2_2VM_R4.5M QUAD@

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26
AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26
AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26
AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26
AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26
Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26
V35 V34 V33 V32 V31 V30 V29 V28 V27 V26
U35 U34 U33 U32 U31 U30 U29 U28 U27 U26
R35 R34 R33 R32 R31 R30 R29 R28 R27 R26
P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10
VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20
VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30
VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40
VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50
VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60
VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70
VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80
VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90
VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

Sandy Bridge_rPGA_Rev1p0
ME@

Cap quantity follow HR_PDDG_Rev07
22uF*7 NO-STUFF

18A

(22uF_0805_6.3V)*13

+1.05VS

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

C41 C42 C43 C44 C54 C45 C46 C55 C56 C47 22U_0805_6.3V6M
C57 C58 C59 @ C60 @ C61 @ C62 @ C63 @ C64 @ C65 @ 22U_0805_6.3V6M

C922 330U_2.5V_M @
C69 330U_D2_2.5VY_R9M
C72 330U_D2_2.5VY_R9M @
C918 330U_2.5V_M

+1.05VS

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# R47 43_0402_5%
VIDSCLK AJ30 H_CPU_SVIDCLK R48 BOM Structure 0402_5%
VIDSOUT AJ28 H_CPU_SVIDDAT R49 BOM Structure 0402_5%

VR_SVID_ALRT# <60>
VR_SVID_CLK <60>
VR_SVID_DAT <60>

R50 130_0402_5% +1.05VS

8/11 update: Add R1309, R1310.
PDDG1.21#439028

+CPU_CORE

R51 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R R52 0_0402_5%
VSS_SENSE AJ34 VSSSENSE_R R53 0_0402_5%

VCCSENSE <60>
VSSSENSE <60>

+1.05VS R1313 10_0402_1%

VCCIO_SENSE B10
VSSIO_SENSE A10 VSSIO_SENSE

VCCIO_SENSE <58>

R1314 10_0402_1%

R54 100_0402_1% @

R1309 27.4_0402_1% @
R1310 27.4_0402_1%

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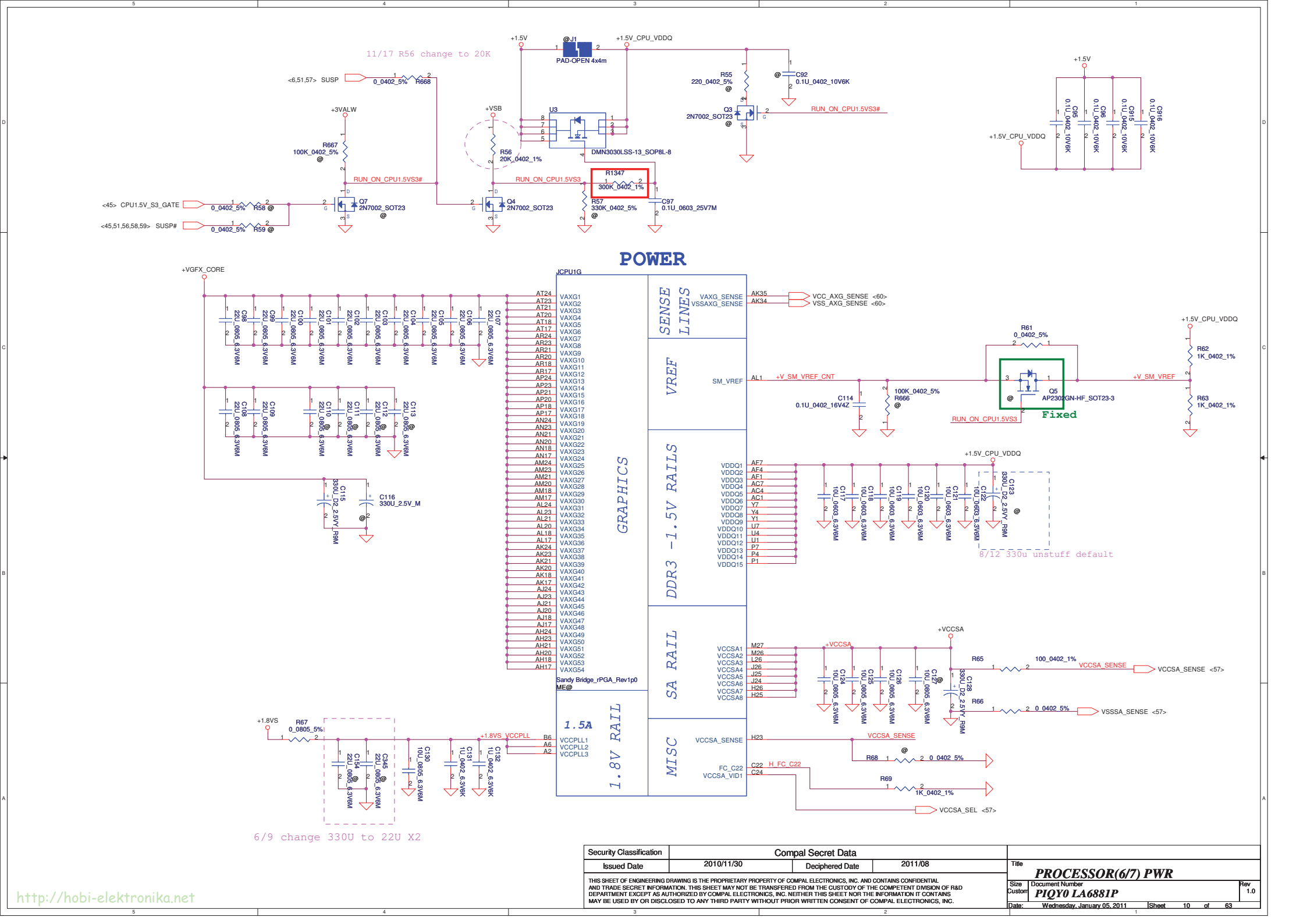
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Title: PROCESSOR(5/7) PWR,BYPASS

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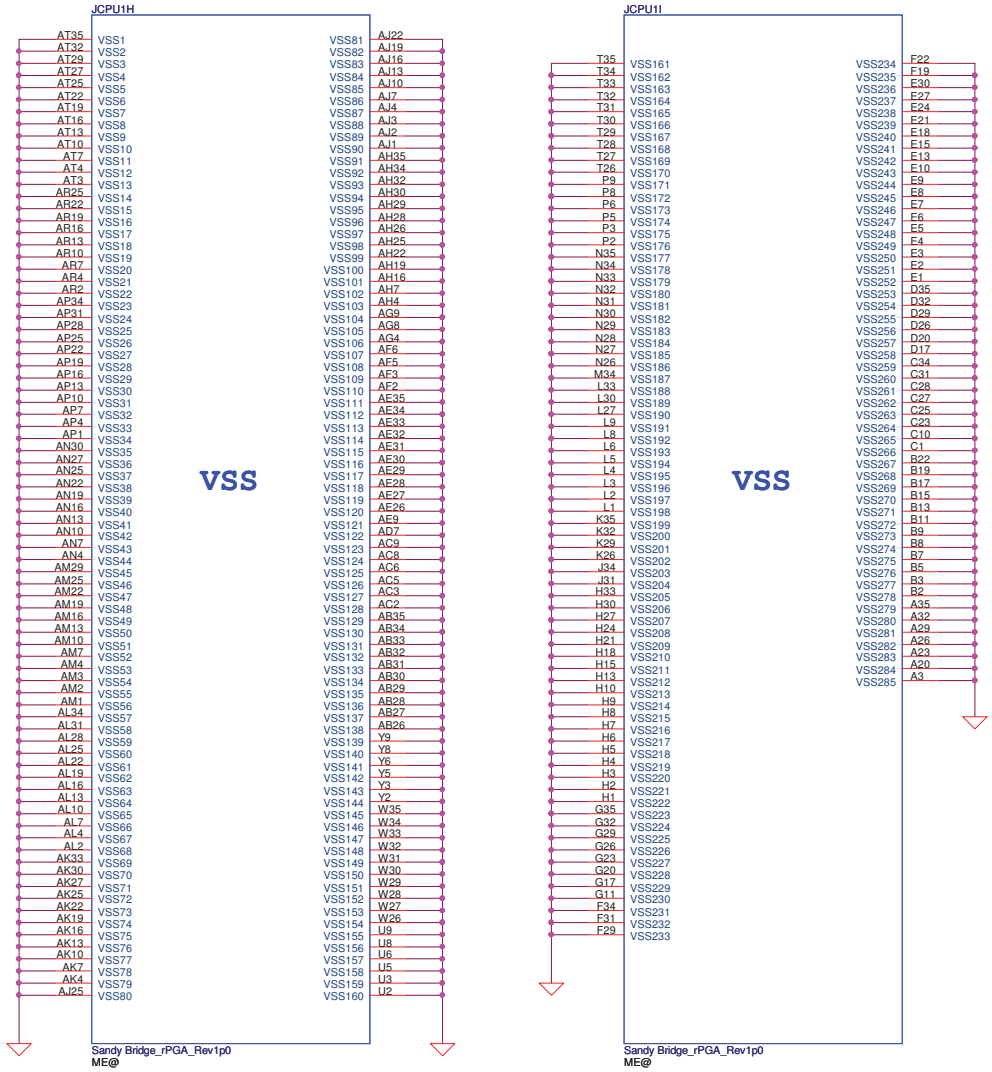
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Title: **PROCESSOR(6/7) PWR**

Size	Document Number	Rev
Custom	PIQY0 LA6881P	1.0

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Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
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DDR3 SO-DIMM A

JDIMM1

LCN_DAN06-K4526-0100

ME@

DDR3_DRAMRST# <7,13>

SMB_DATA_S3 <13,15,37>
SMB_CLK_S3 <13,15,37>

<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

R70 1K_0402_1%
R71 1K_0402_1%

R72 1K_0402_1%
R73 1K_0402_1%

C133 0.1U_0402_10V6K
C134 2.2U_0603_6.3V6K
C135 0.1U_0402_10V6K
C136 2.2U_0603_6.3V6K
C155 2.2U_0603_6.3V6K
C156 0.1U_0402_10V6K

R81 10K_0402_5%
R83 10K_0402_5%

Layout Note:
Place near DIMM

*(10uF_0603_6.3V)*8*

*(0.1uF_402_10V)*4*

C137 @
C138 @
C139
C140
C141
C142
C143
C144
C145 0.1U_0402_10V6K
C146 0.1U_0402_10V6K
C147 0.1U_0402_10V6K
C148 0.1U_0402_10V6K
C149 220U_B2_2.5VM_R35

Layout Note:
Place near DIMM

C150
C151 1U_0402_6.3V6K
C152 1U_0402_6.3V6K
C153 1U_0402_6.3V6K
1U_0402_6.3V6K

Layout Note:
Short to ground

```
VDDQ(1.5V) =
  3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
  6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
  3*0805 10uf  4*0402 1uf
VREF =
  1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
  1*0402 0.1uf  1*0402 2.2uf
```

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Issued Date	2010/11/30	Deciphered Date	2011/08

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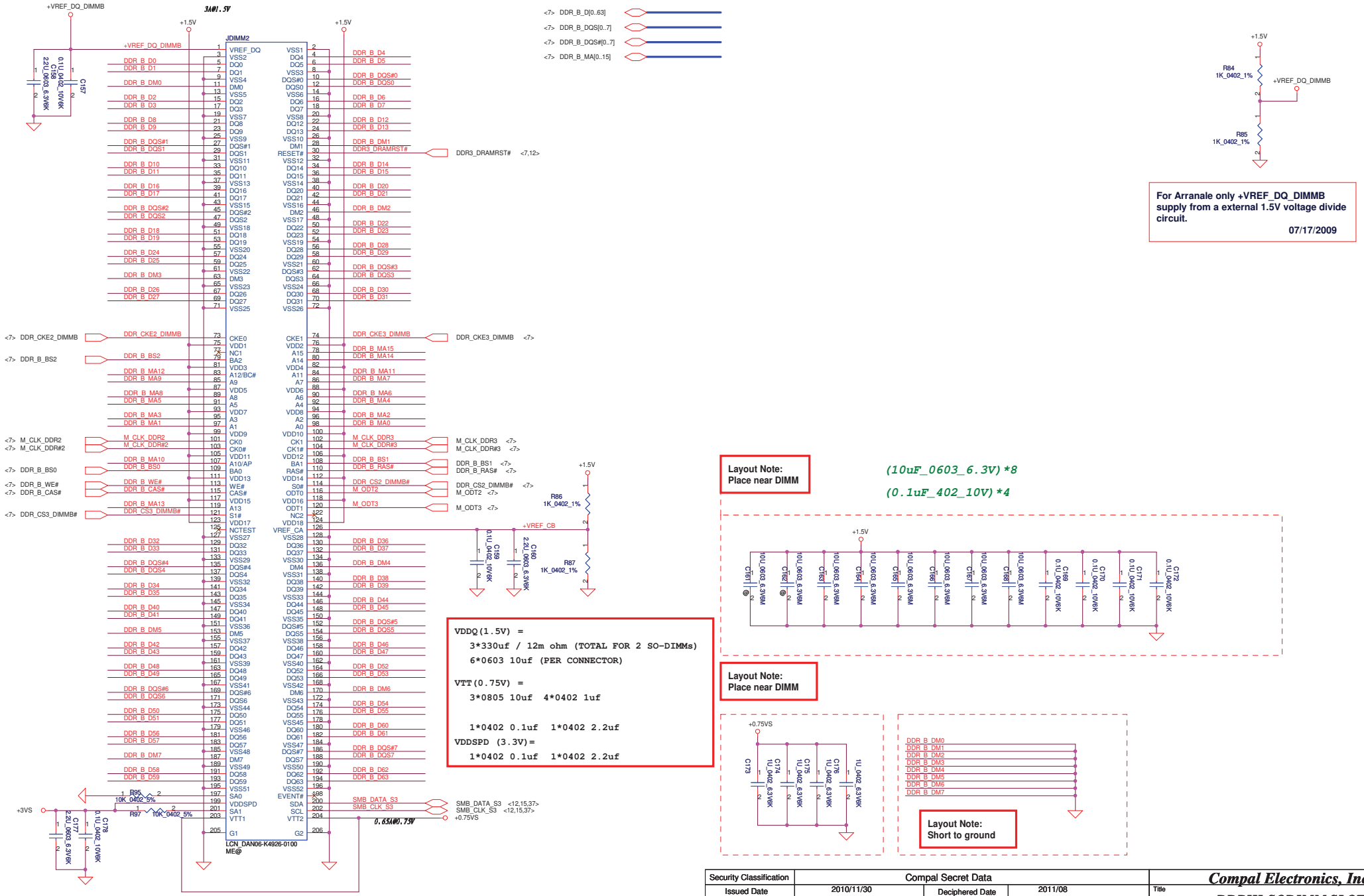
Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size: Custom | Document Number: **PIQY0 LA6881P** | Rev: 1.0

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<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_DQS#[0..7]
<7> DDR_B_MA[0..15]

For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.

07/17/2009

Layout Note:
Place near DIMM

(10uF_0603_6.3V)*8

(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

Layout Note:
Short to ground

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

Size | Document Number: PIQY0 LA6881P | Rev: 1.0

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W=20mils W=20mils
+RTCVCC +RTCBATT
R99 1K_0402_5%
C179 1U_0603_10V4Z
CLRP1 SHORT PADS
PCH_RTCX1 PCH_RTCX2
R98 10M_0402_5%
C180 15P_0402_50V8J
C181 15P_0402_50V8J
Y1 32.768KHZ_12.5PF_9H03200413
CMOS
+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN
R1330 330K_0402_5%
INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)
+3VS
R105 1K_0402_5% HDA_SPKR
* HIGH= Enable (No Reboot)
LOW= Disable (Default)
+3VALW
R106 1K_0402_5% HDA_SDOUT
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]
+3VALW
R108 1K_0402_5% HDA_SYNC
This signal has a weak internal pull-down
* On Die PLL VR Select is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom
<42> HDA_BITCLK_AUDIO R112 33_0402_5% HDA_BIT_CLK
<42> HDA_SYNC_AUDIO R114 33_0402_5% HDA_SYNC_R
<42> HDA_RST_AUDIO# R116 33_0402_5% HDA_RST#
<42> HDA_SDOUT_AUDIO R118 33_0402_5% HDA_SDOUT
+3VS Q10 BSS138_NL_SOT23-3 HDA_SYNC
R1348 1M_0402_5%
@R325 0_0402_5%
6/17 follow module design
+3VALW R121 200_0402_5% PCH_JTAG_TDO
+3VALW R122 200_0402_5% PCH_JTAG_TMS
+3VALW R123 200_0402_5% PCH_JTAG_TDI
R125 100_0402_1%
R126 100_0402_1%
R128 100_0402_1%
DPDG1.1
6/30 update R121, R122, R123
+RTCVCC
C183 1U_0603_10V4Z CLRP2 SHORT PADS
R103 20K_0402_5%
R100 20K_0402_5%
C182 1U_0603_10V4Z CLRP3 SHORT PADS
U4A
PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC
HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
<42> HDA_SPKR HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
<42> HDA_SDIN0 HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
IHDA
<45> ME_FLASH R109 0_0402_5% HDA_SDOUT A36 HDA_SDO
R107 1K_0402_1% PCH_GPIO33 C36 HDA_DOCK_EN# / GPIO33
<46> Kill_SW# Kill_SW# N32 HDA_DOCK_RST# / GPIO13
R110 51_0402_5%
PCH_JTAG_TCK J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG
SPI_CLK_PCH T3 SPI_CLK
SPI_SB_CS0# Y14 SPI_CS0#
T1 SPI_CS1#
SPI_SI V4 SPI_MOSI
SPI_SO_R U3 SPI_MISO
SPI
COUGARPOINT_FCBGA989
LPC
FWH0 / LAD0 C38 LPC_AD0
FWH1 / LAD1 A38 LPC_AD1
FWH2 / LAD2 B37 LPC_AD2
FWH3 / LAD3 C37 LPC_AD3
LPC_AD0 <37,45>
LPC_AD1 <37,45>
LPC_AD2 <37,45>
LPC_AD3 <37,45>
EC and Mini card debug port
FWH4 / LFRAME# D36 LPC_FRAME#
LPC_FRAME# <37,45>
LDRQ0# E36
LDRQ1# / GPIO23 K36
+3VS R104 10K_0402_5%
SERIRQ V5 SERIRQ
SERIRQ <45>
SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7 SATA_ITX_C_DRX_N0 0.01U_0402_16V7K C184 SATA_ITX_DRX_N0
SATA0TXP AP5 SATA_ITX_C_DRX_P0 0.01U_0402_16V7K C185 SATA_ITX_DRX_P0
SATA_DTX_C_IRX_N0 SATA_DTX_C_IRX_P0
SATA_DTX_C_IRX_N0 <37> SATA_DTX_C_IRX_P0 <37> SATA_ITX_DRX_N0 <37> SATA_ITX_DRX_P0 <37>
SSD
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11 SATA_ITX_C_DRX_N1 0.01U_0402_16V7K C273 SATA_ITX_DRX_N1
SATA1TXP AP10 SATA_ITX_C_DRX_P1 0.01U_0402_16V7K C272 SATA_ITX_DRX_P1
SATA_DTX_C_IRX_N1 SATA_DTX_C_IRX_P1
SATA_DTX_C_IRX_N1 <41> SATA_DTX_C_IRX_P1 <41> SATA_ITX_DRX_N1 <41> SATA_ITX_DRX_P1 <41>
HDD
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5 SATA_ITX_C_DRX_N2 0.01U_0402_16V7K C186 SATA_ITX_DRX_N2_CONN
SATA2TXP AH4 SATA_ITX_C_DRX_P2 0.01U_0402_16V7K C187 SATA_ITX_DRX_P2_CONN
SATA_DTX_C_IRX_N2 SATA_DTX_C_IRX_P2
SATA_DTX_C_IRX_N2 <41> SATA_DTX_C_IRX_P2 <41> SATA_ITX_DRX_N2_CONN <41> SATA_ITX_DRX_P2_CONN <41>
ODD
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3 SATA_ITX_C_DRX_N4 0.01U_0402_16V7K C188 SATA_ITX_DRX_N4
SATA4TXP AD1 SATA_ITX_C_DRX_P4 0.01U_0402_16V7K C189 SATA_ITX_DRX_P4
ESATA@
SATA_DTX_C_IRX_N4 SATA_DTX_C_IRX_P4
SATA_DTX_C_IRX_N4 <48> SATA_DTX_C_IRX_P4 <48> SATA_ITX_DRX_N4 <48> SATA_ITX_DRX_P4 <48>
ESATA
ESATA@
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP
R111 37.4_0402_1% +1.05VS_VCC_SATA
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP
R113 49.9_0402_1% +1.05VS_SATA3
SATA3RBIAS AH1 RBIAS_SATA3 R115 750_0402_1%
R117 10K_0402_5% +3VS
SATALED# P3 HDD_LED# HDD_LED# <50>
SATA0GP / GPIO21 V14 PCH_GPIO21 R119 10K_0402_5% +3VS
SATA1GP / GPIO19 P1 SATA_DET# SATA_DET# <37>
R316 10K_0402_5% +3VS
4MB SPI ROM FOR ME & Non-share ROM.
+3VS R127 3.3K_0402_5% SPI_WP#_0
R129 3.3K_0402_5% SPI_HOLD#_0
SPI_CLK_PCH R124 33_0402_5% @
C190 22P_0402_50V8J @
+3VS C191 0.1U_0402_16V4Z
R130 0_0402_5%
SPI_SB_CS0# SPI_SB_CS0#_R
SPI_SO_R SPI_SO_L0
SPI_WP#_0
R131 33_0402_5%
U5
CS# VCC
SO HOLD#
WP# SCLK
GND SI
SPI_HOLD#_0
SPI_CLK_PCH_0
SPI_SI_R0
S IC FL 32M W25Q32BVSSIG SOIC 8P
R1336 0_0402_5%
SPI_CLK_PCH
SPI_SI
R133 33_0402_5%

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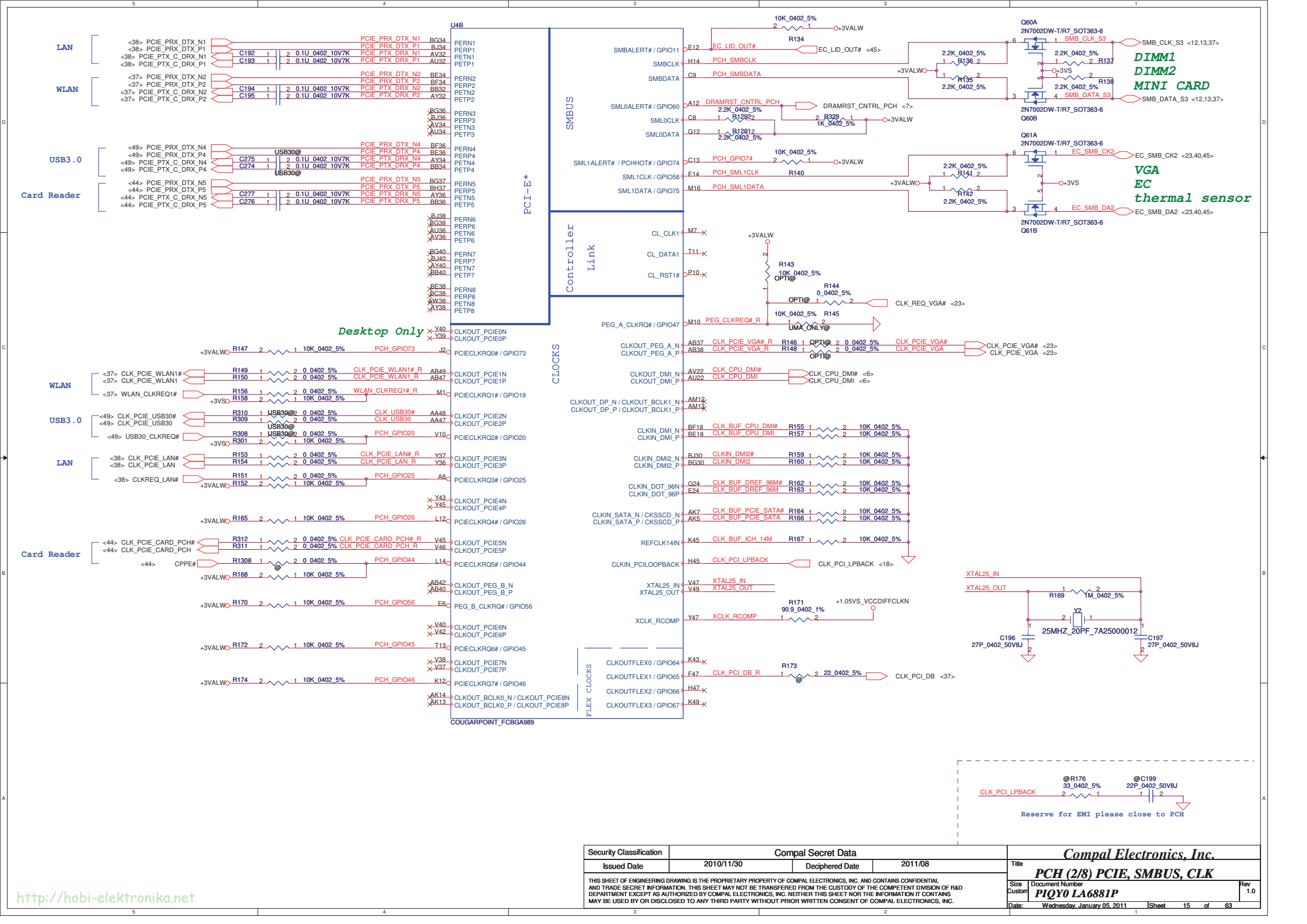
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Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

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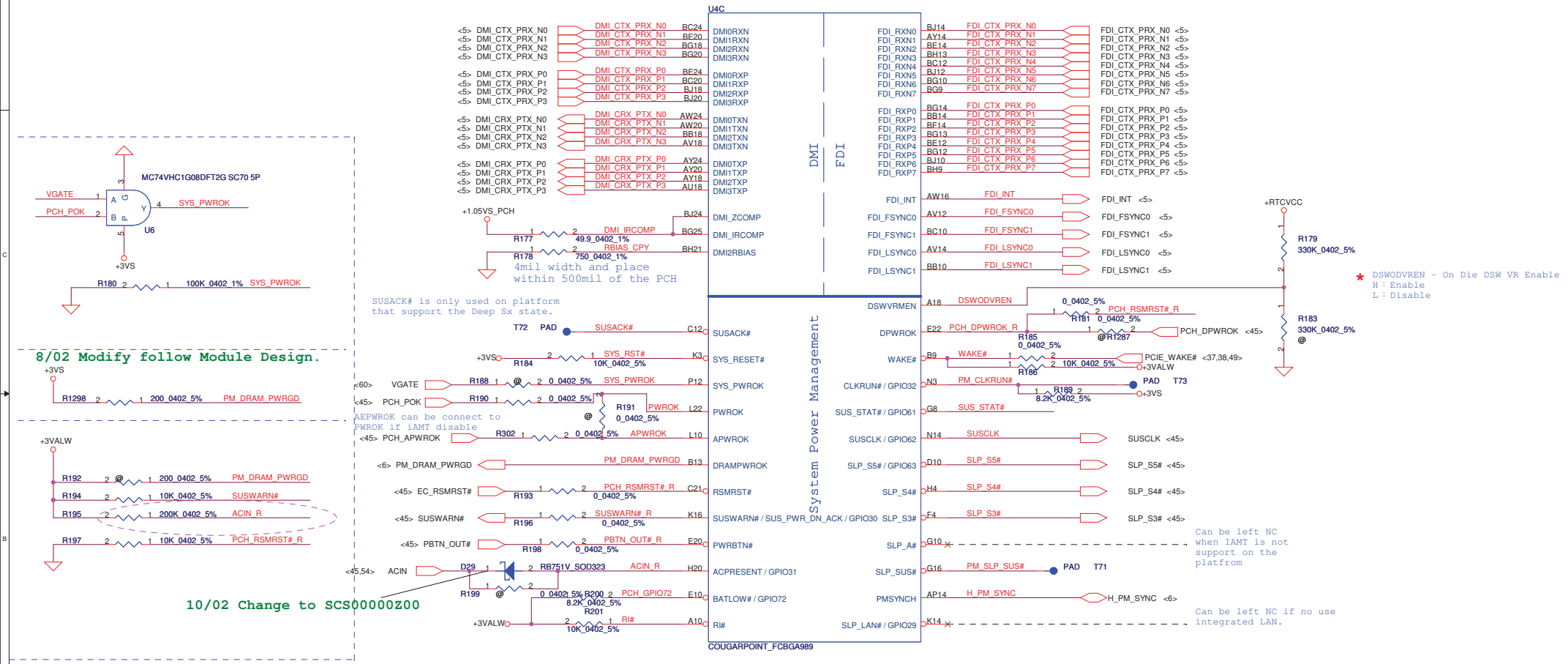
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Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

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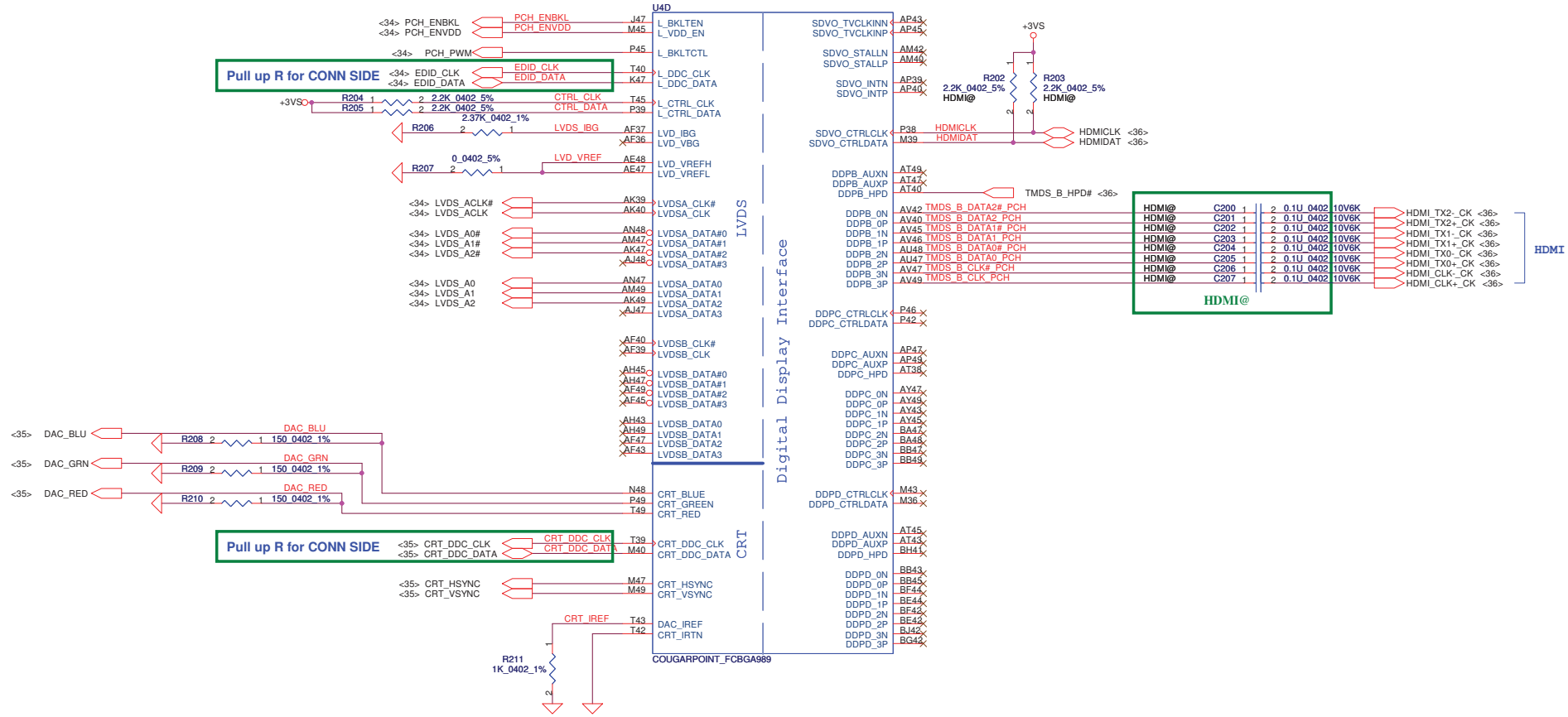
Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size: Custom | Document Number: PIQY0 LA6881P | Rev: 1.0

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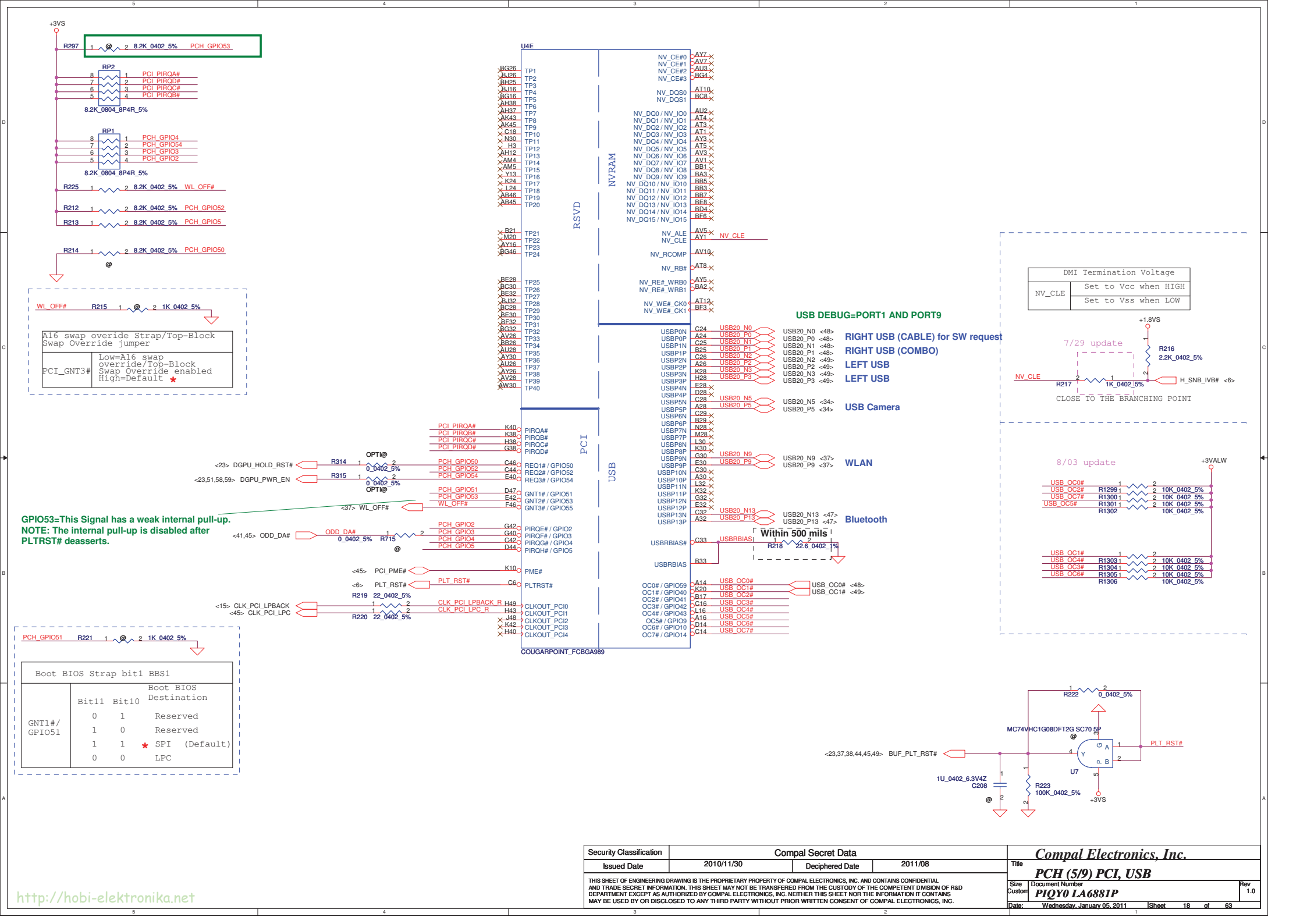
Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: Custom | Document Number: PIQY0 LA6881P | Rev: 1.0

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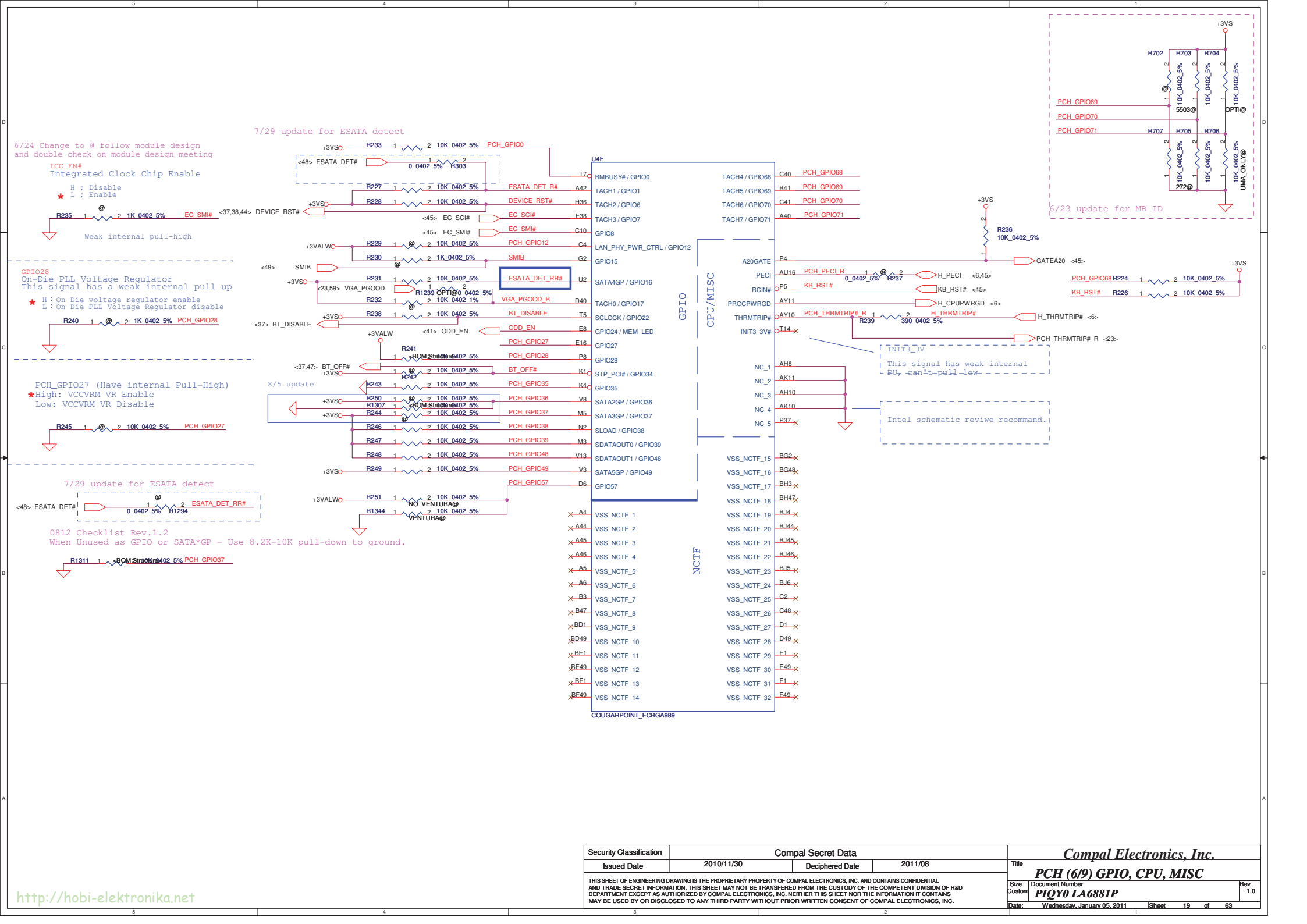
Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size	Document Number	Rev
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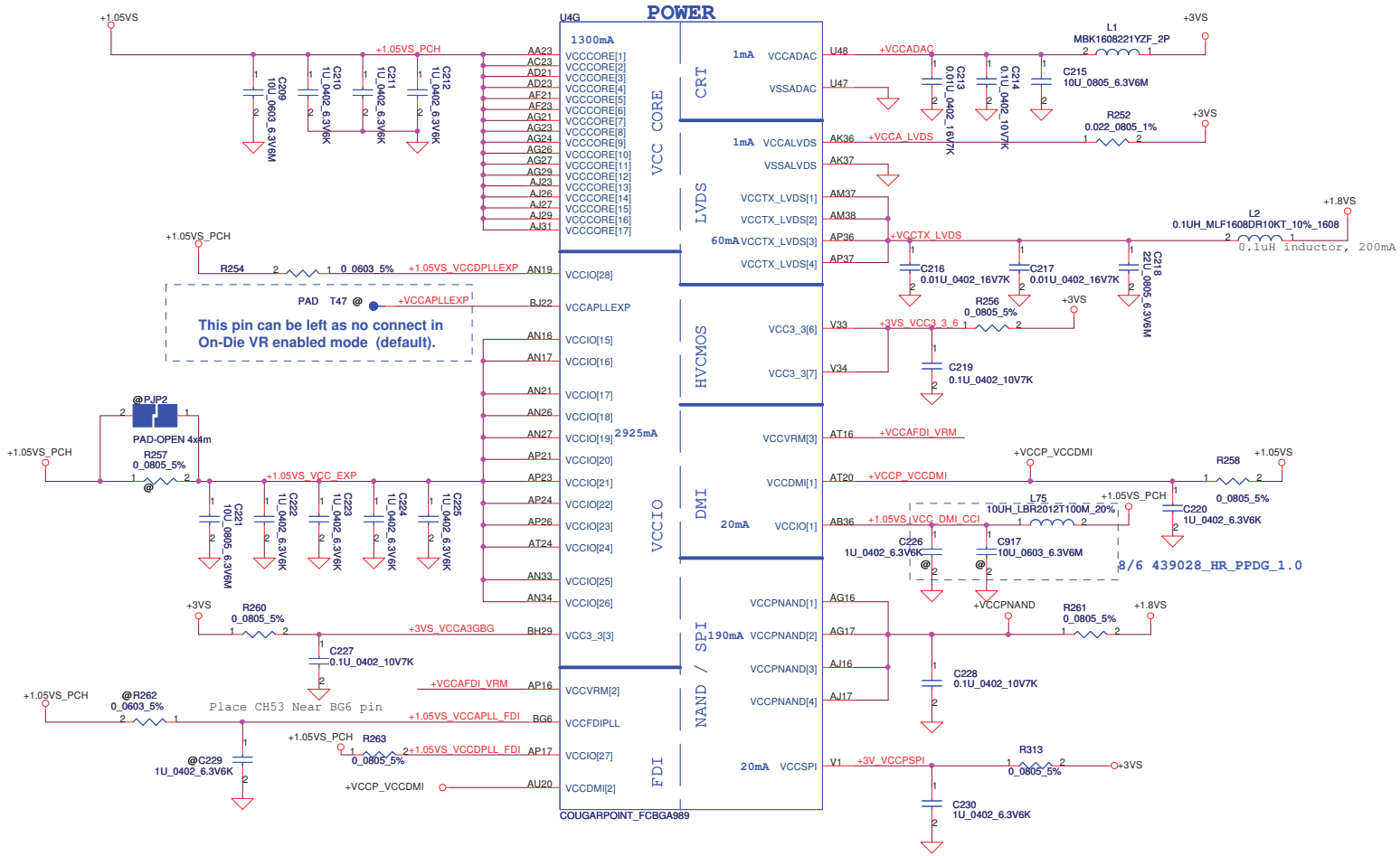
Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Intel HR_PDDG_1.21
1.5S rail. Default is to poppulate to enable VccVRM.

VCCVRM = 160mA detal waiting for newest spec

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Compal Electronics, Inc.

Title: PCH (7/9) PWR

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Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

U4J

COUGARPOINT_FCBGA989

USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA

11/25 0ohm deleted.

10/02 Change to SCS00000Z00.

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Issued Date	2010/11/30	Deciphered Date	2011/08

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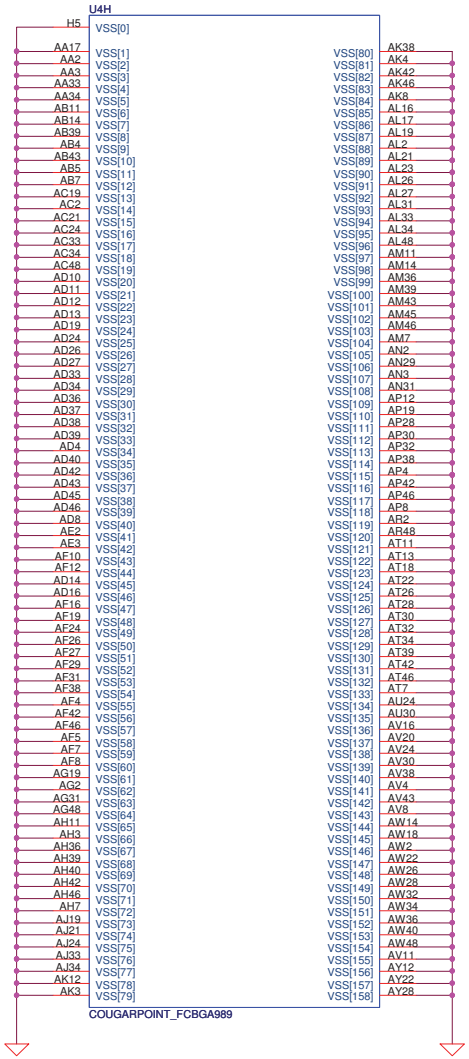
Compal Electronics, Inc.

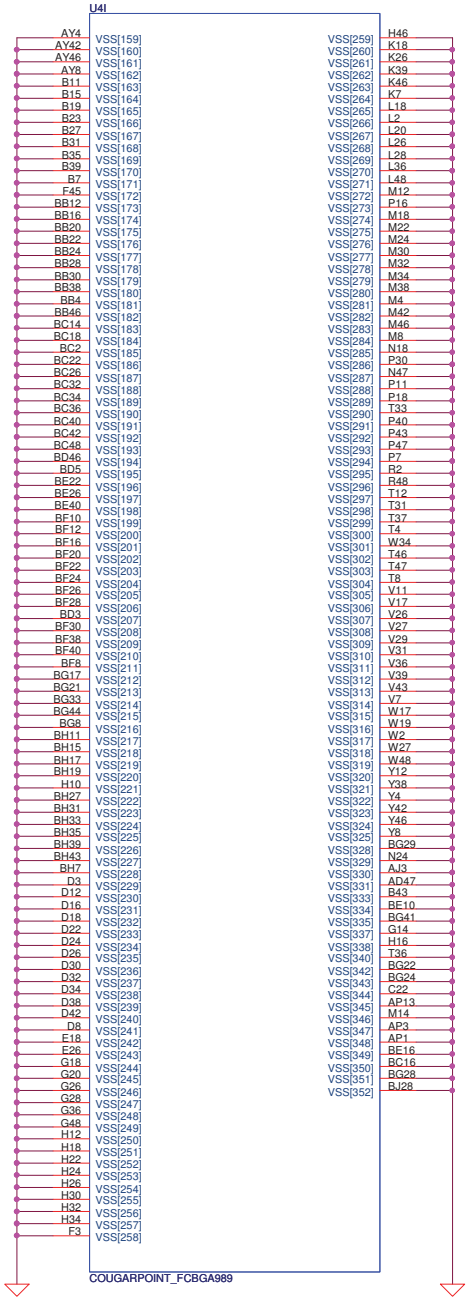
Title: PCH (8/9) PWR

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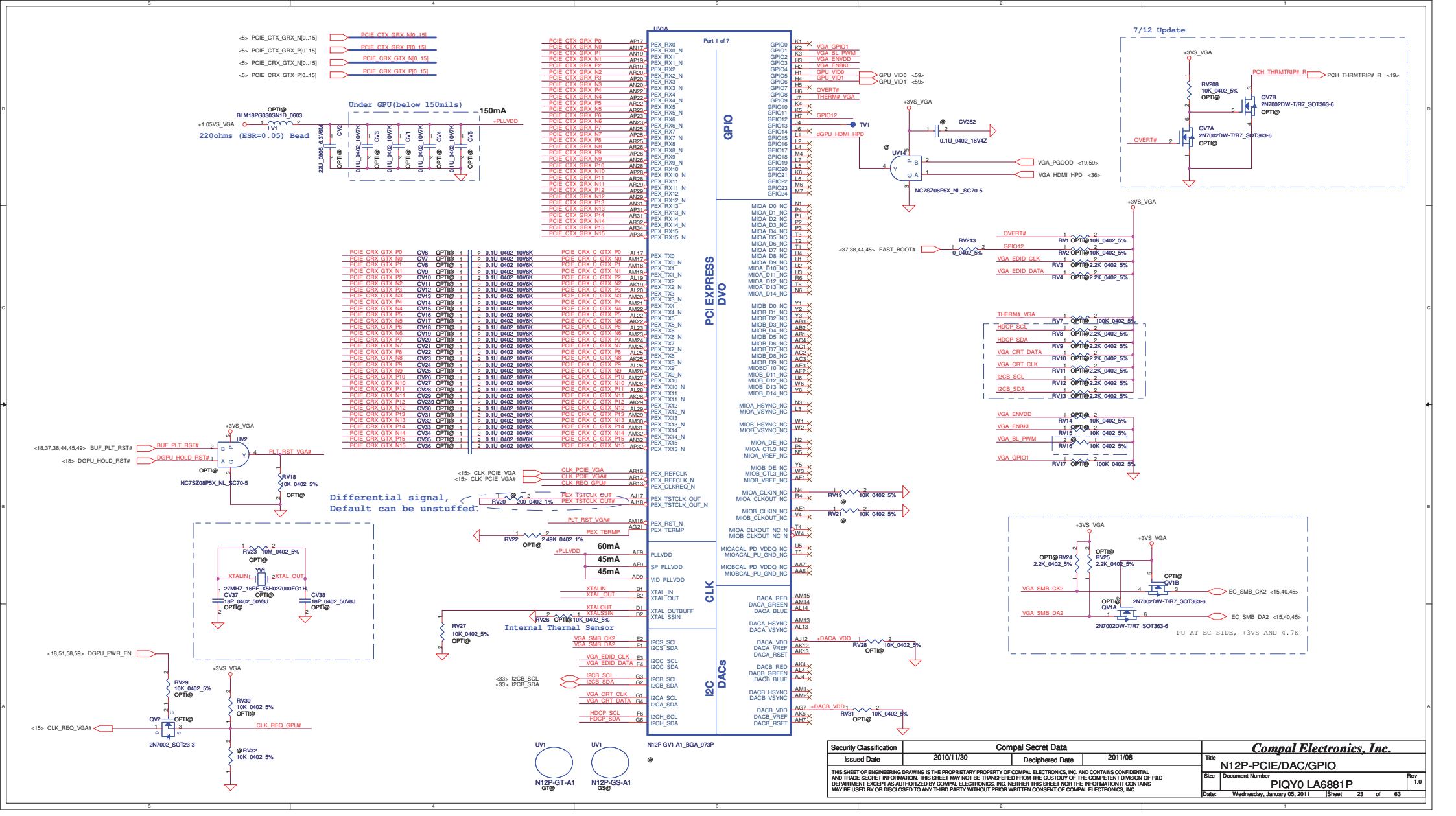
Compal Electronics, Inc.

Title: PCH (9/9) VSS

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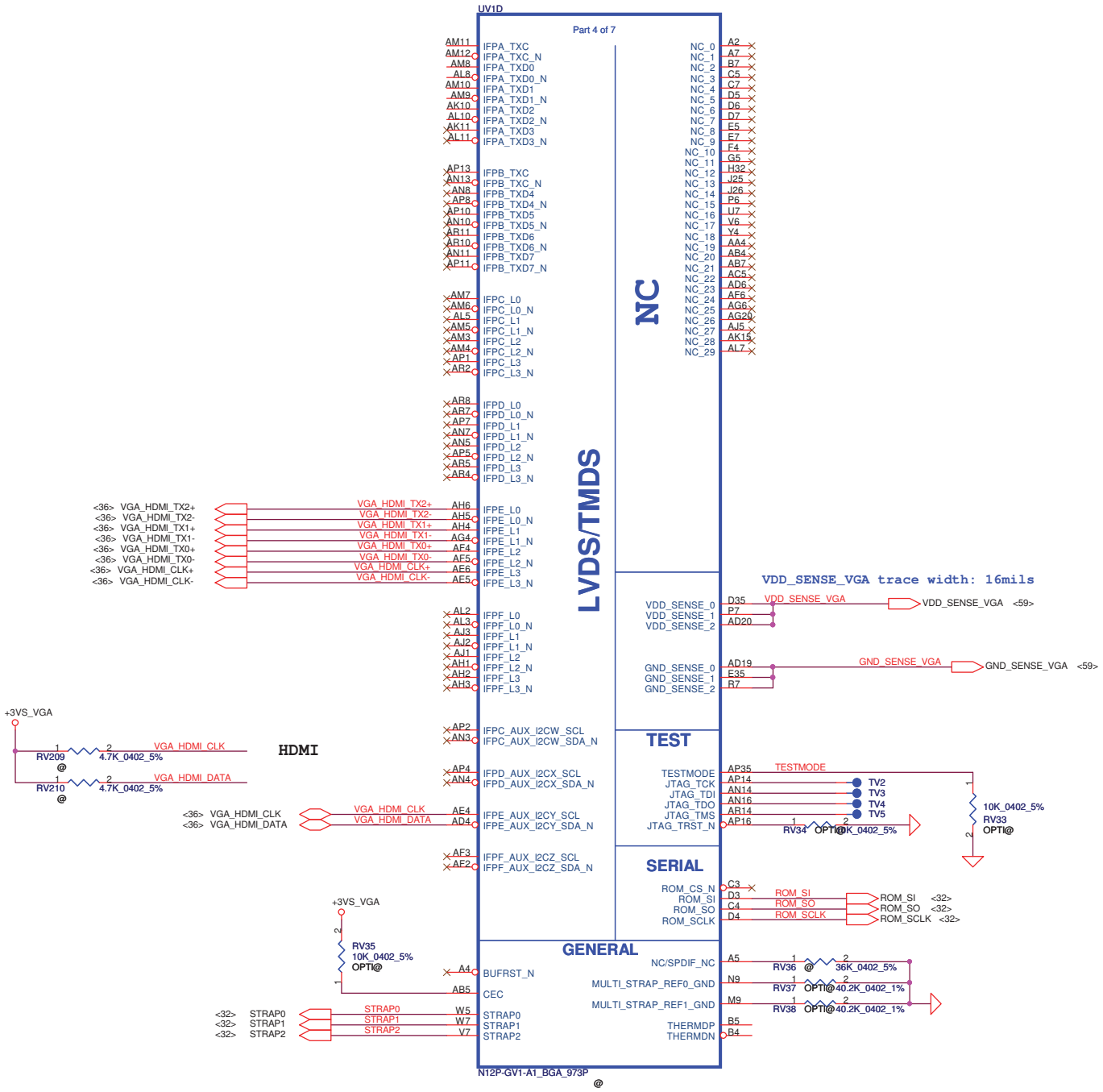
Compal Electronics, Inc.

Title: N12P-PCIE/DAC/GPIO

Size	Document Number	Rev
	PIQY0 LA6881P	1.0

Date: Wednesday, January 05, 2011 | Sheet 23 of 63

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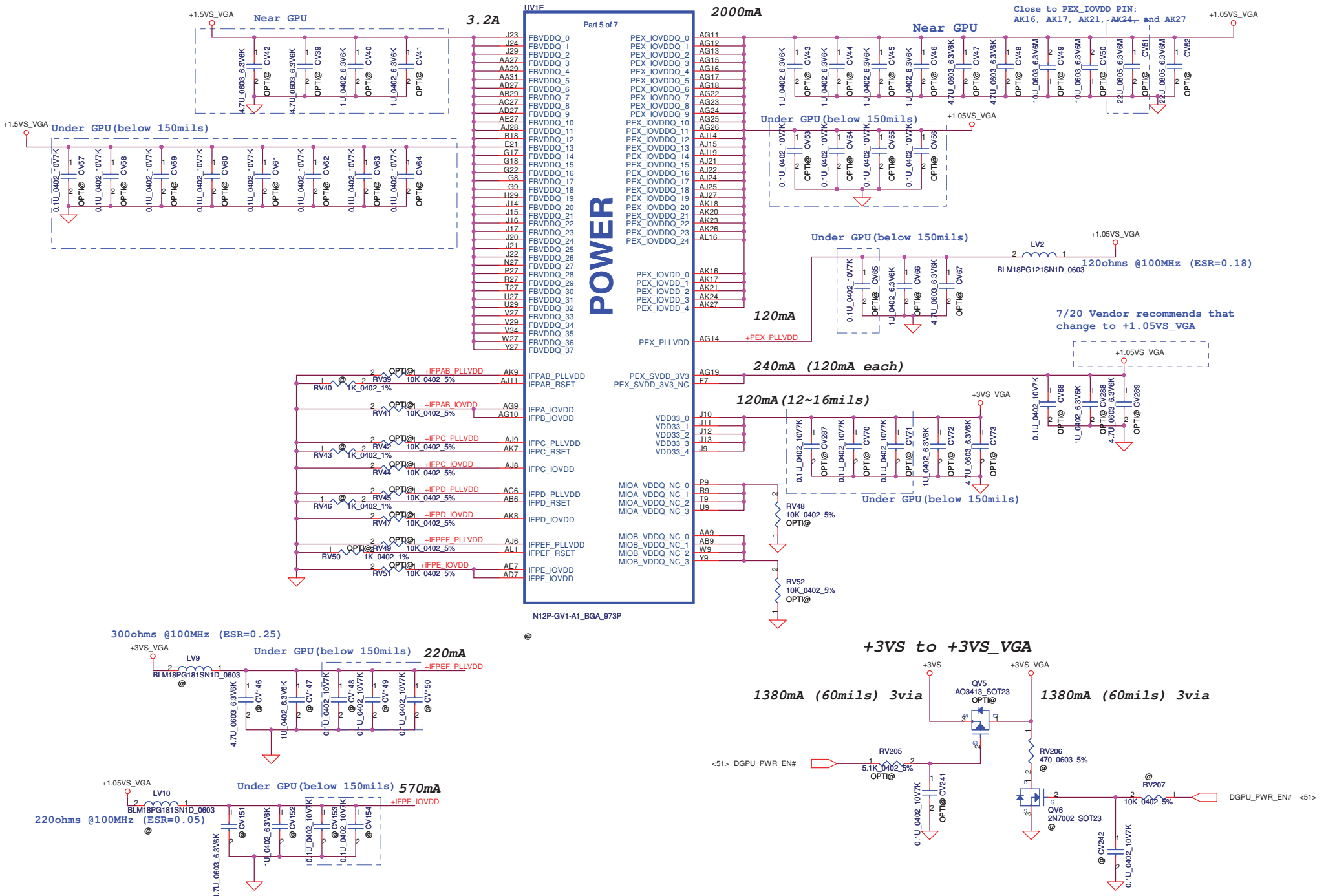
Compal Electronics, Inc.

Title: N12P-LVDS/HDMI/DP/THM

Size | Document Number: PIQY0 LA6881P | Rev: 1.0

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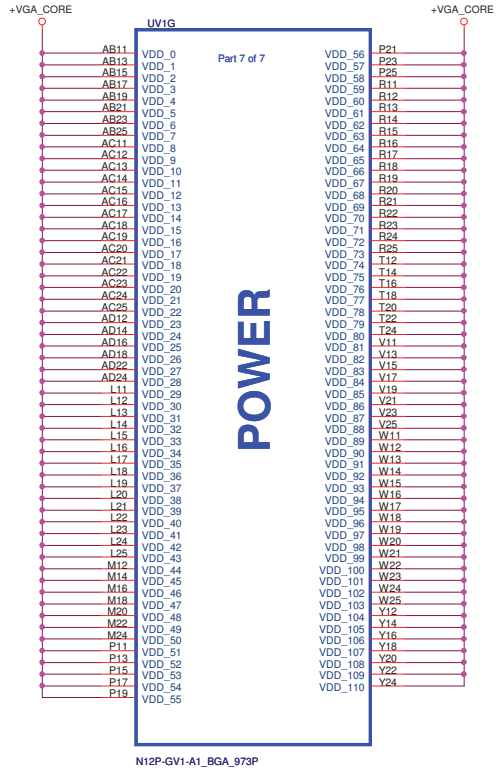
Title: N12P-POWER

Size | Document Number: PIQY0 LA6881P | Rev: 1.0

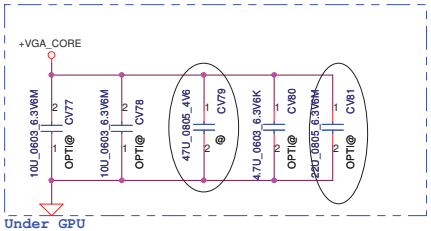
Date: Wednesday, January 05, 2011 | Sheet 25 of 63

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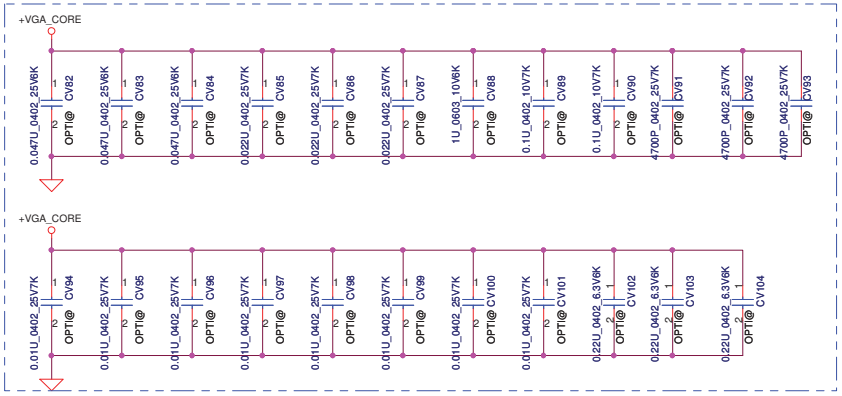
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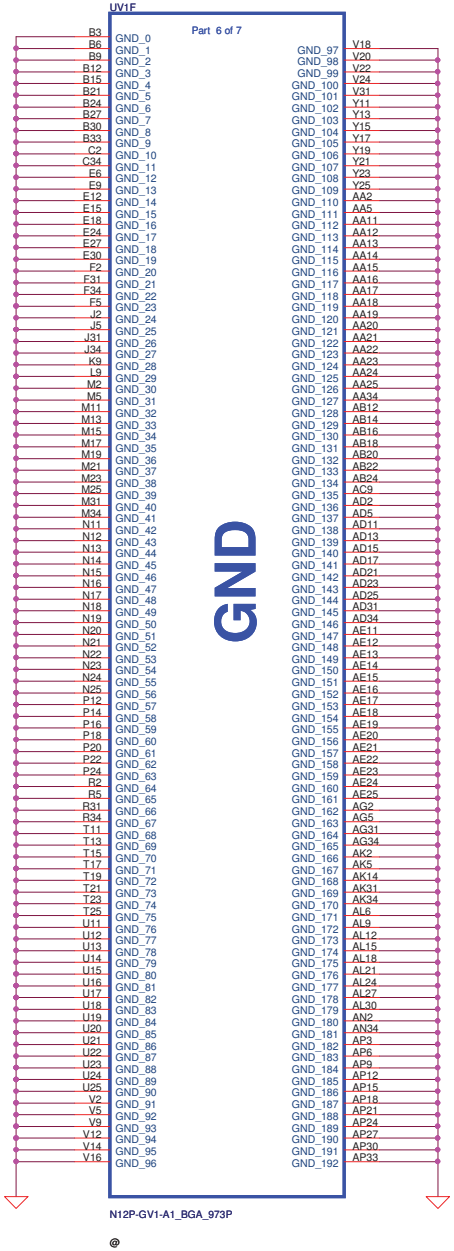


Near GPU



Under GPU





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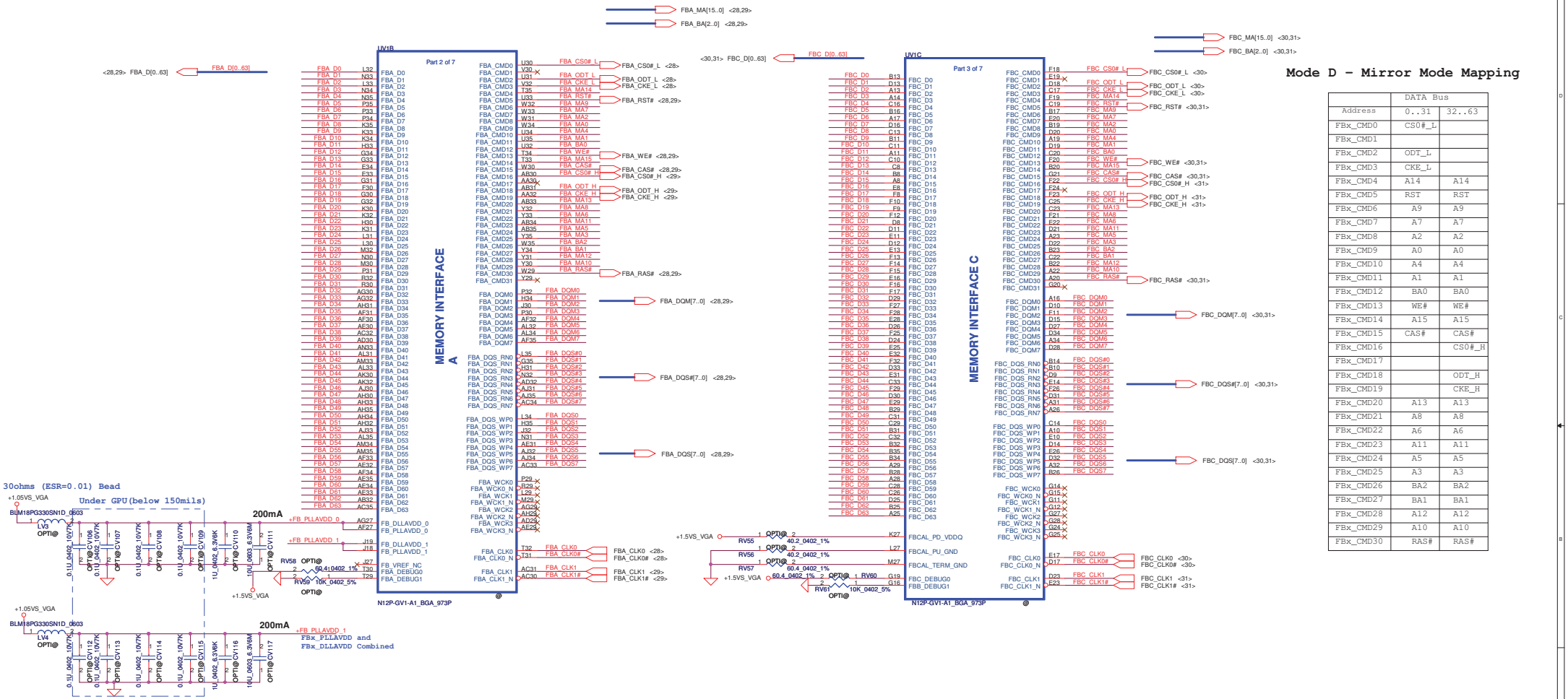
Compal Electronics, Inc.

Title: N12P-VGA CORE, GND

Size | Document Number: PIQY0 LA6881P | Rev: 1.0

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Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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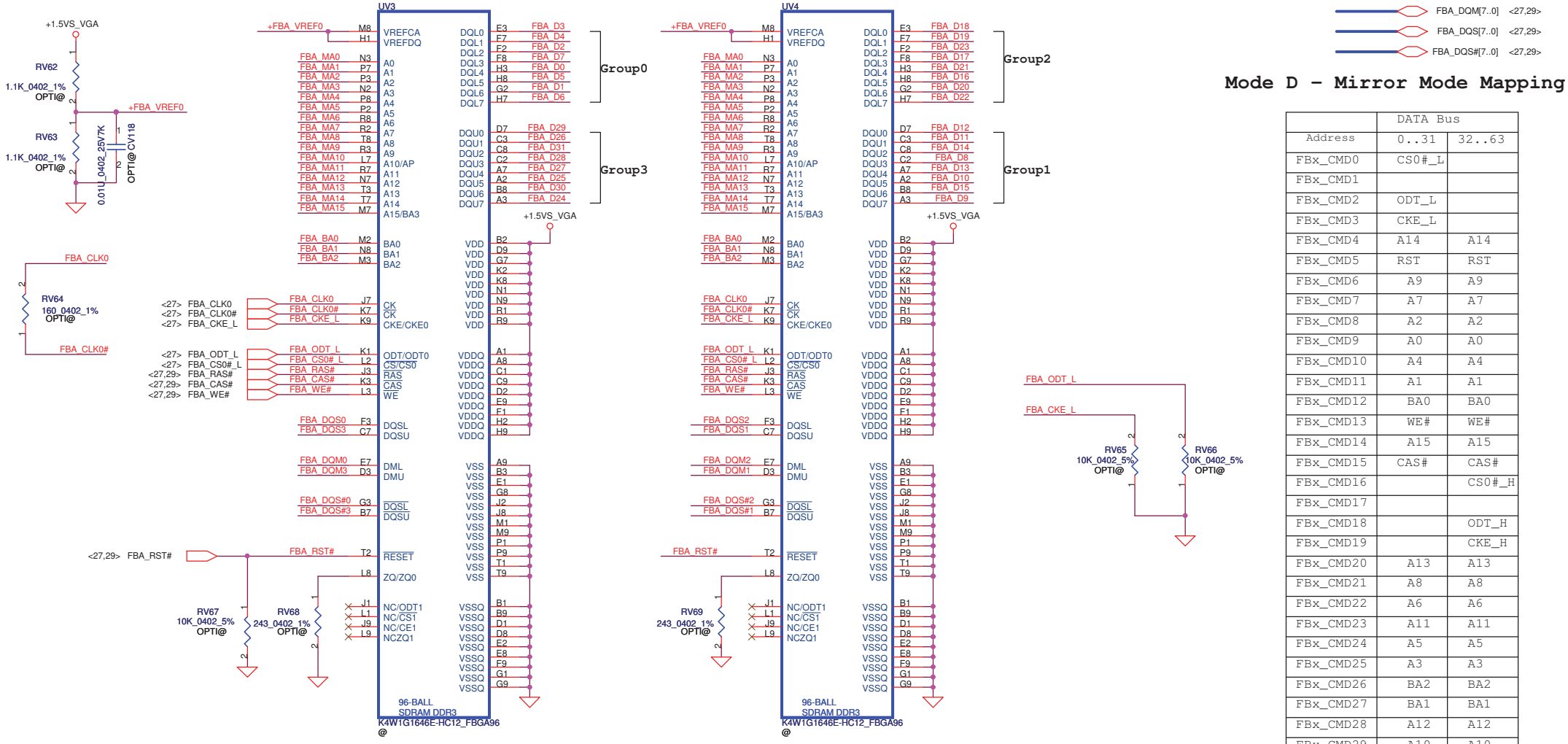
Title: N12P-MEM Interface

Size | Document Number: PIQY0 LA6881P | Rev: 1.0

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Memory Partition A - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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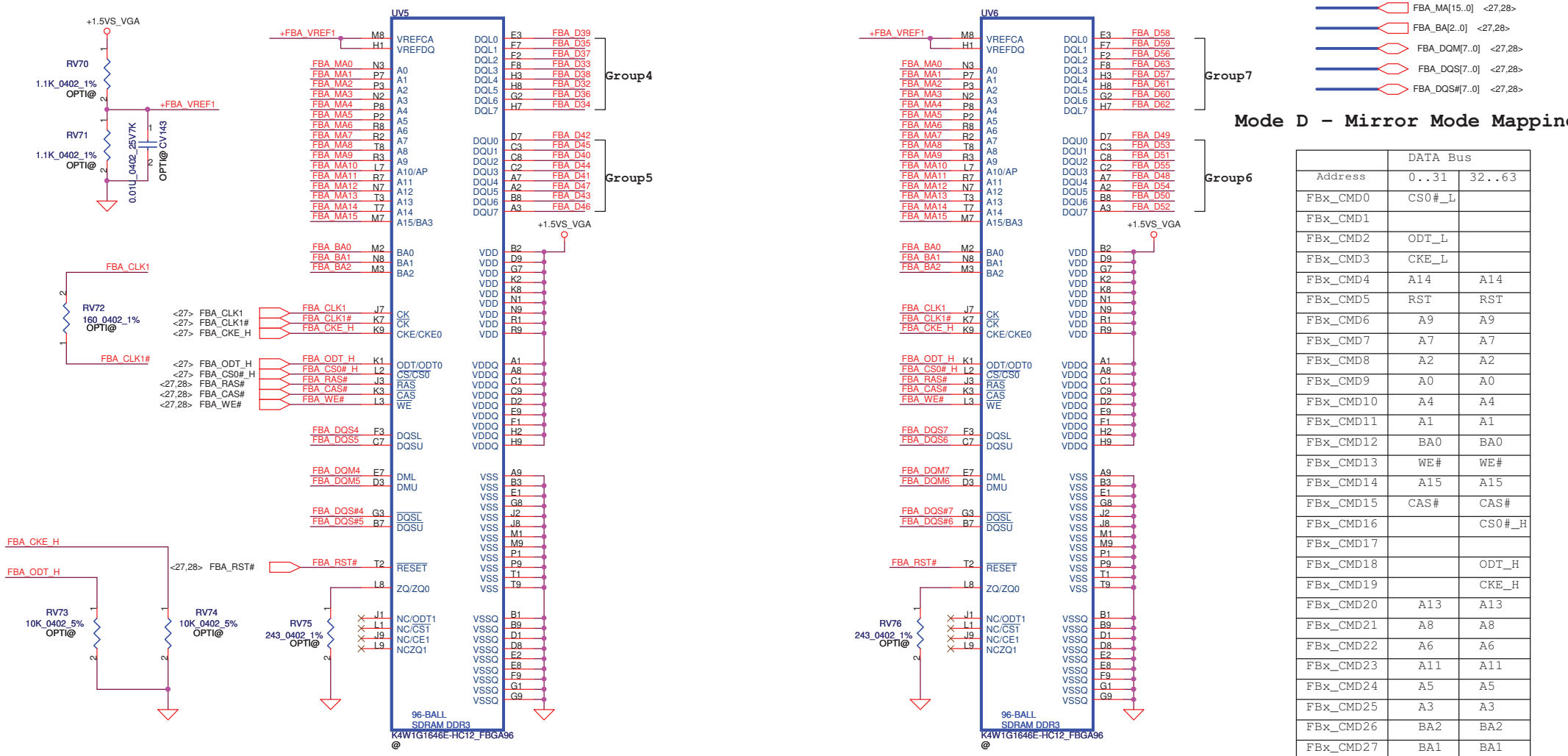
Title: N12P-VRAM A Lower

Size | Document Number: PIQY0 LA6881P | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 28 of 63

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Memory Partition A - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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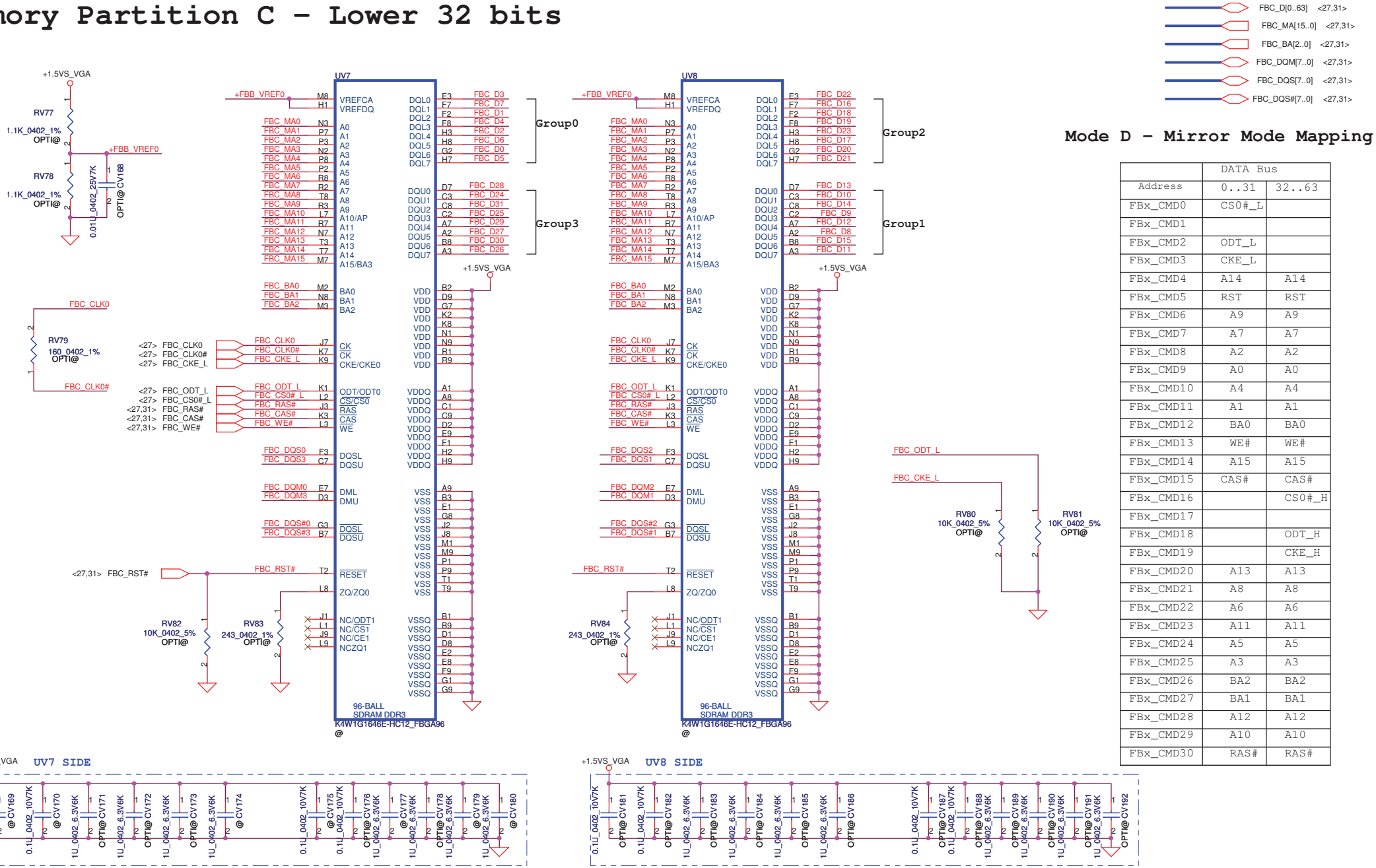
Title: N12P-VRAM A Upper

Size | Document Number: PIQY0 LA6881P | Rev: 1.0

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Memory Partition C - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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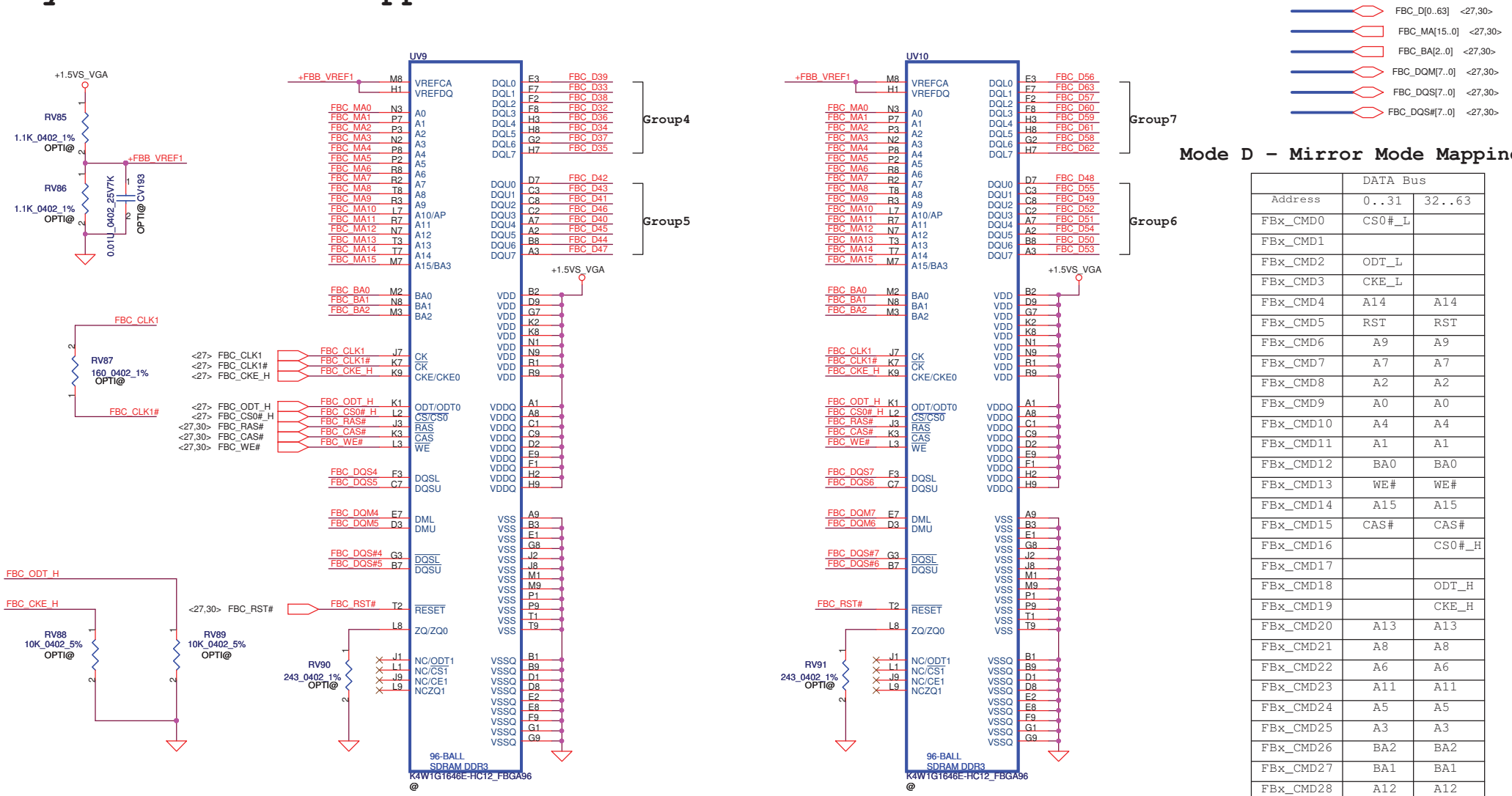
Title: N12P-VRAM C Lower

Size: Custom | Document Number: PIQY0 LA6881P | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 30 of 63

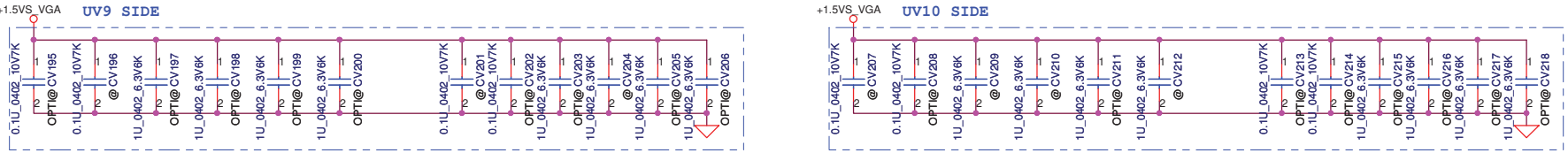
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Memory Partition C - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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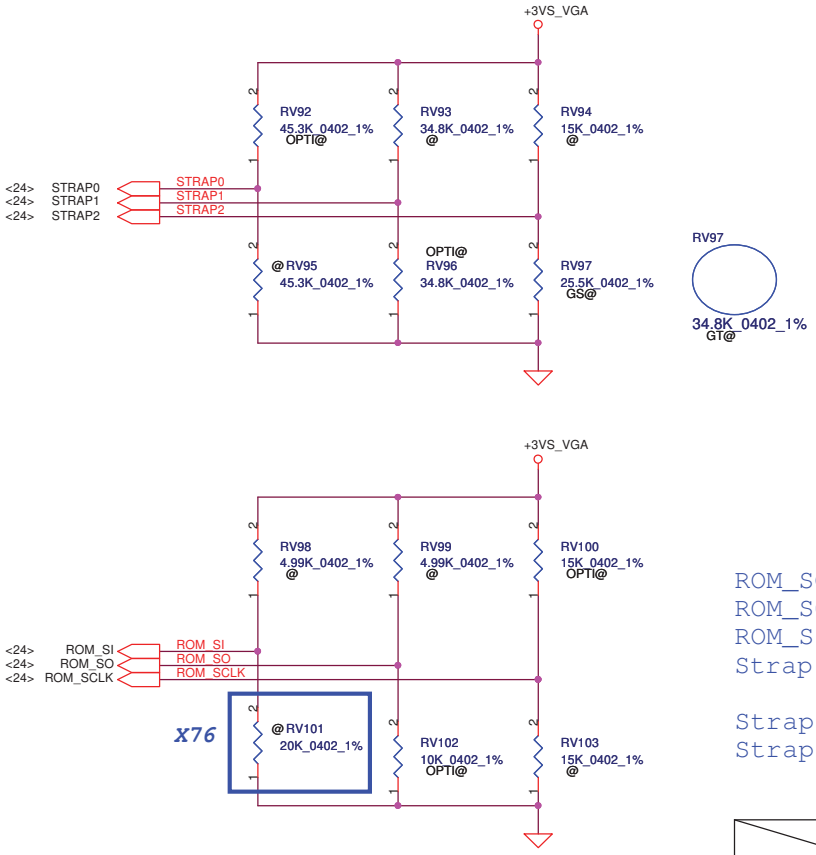
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Title: N12P-VRAM C Upper

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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

ROM_SO : PD-10K
ROM_SCLK : PH-15K
ROM_SI : PD20K (Samsung)
Strap 2 : N12P-GS, PD-25K,
N12P-GT, PD35K,
Strap 1 : PD-35K
Strap 0 : PH-45K

	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GT	0x0DF6	Pull up 15K	Pull down 35K

Hynix H5TQ1G63BFR-12C	64Mx16	0010	PD 15K	SA000041S30
	128Mx16	0110	PD 35K	SA00003YO00
Samsung K4W1G1646E-HC12	64Mx16	0011	PD 20K	SA000041T10
	128Mx16	0111	PD 45K	SA000047Q10

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

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Issued Date	2010/11/30	Deciphered Date	2011/08

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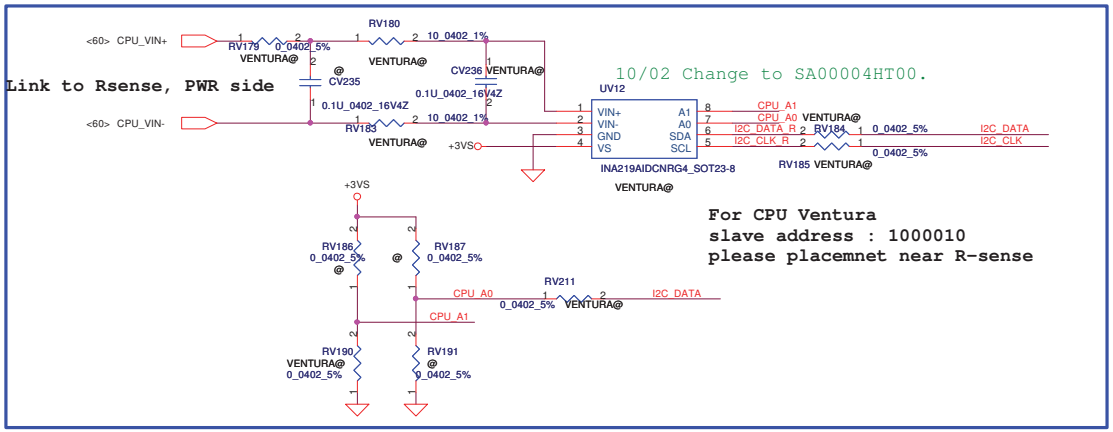
Title: N12P_MISC

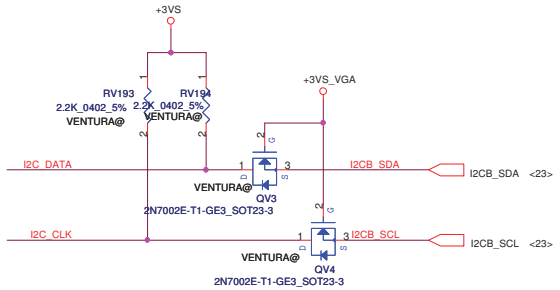
Size: Custom | Document Number: PIQY0 LA6881P | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 32 of 63

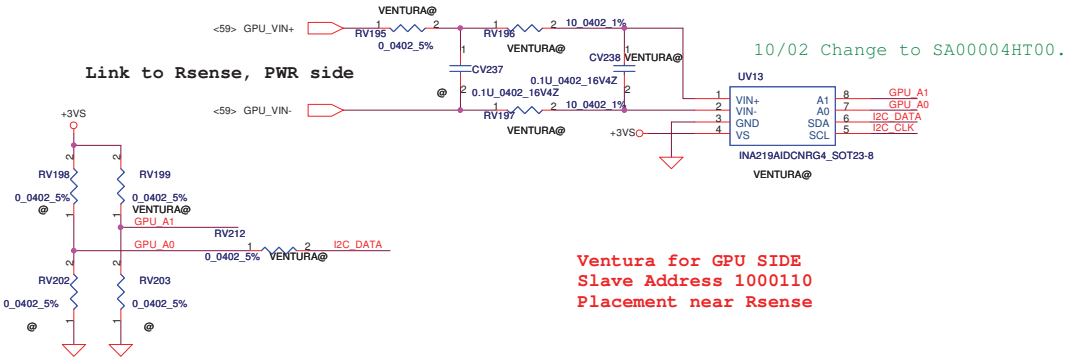
http://hobi-elektronika.net

TOP side (under inductor)





Link to GPU



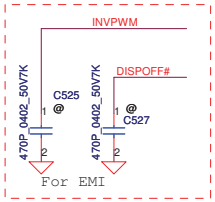
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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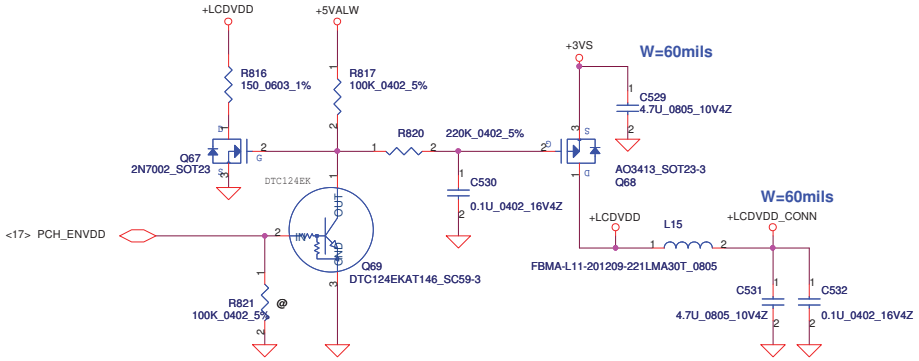
Compal Electronics, Inc.

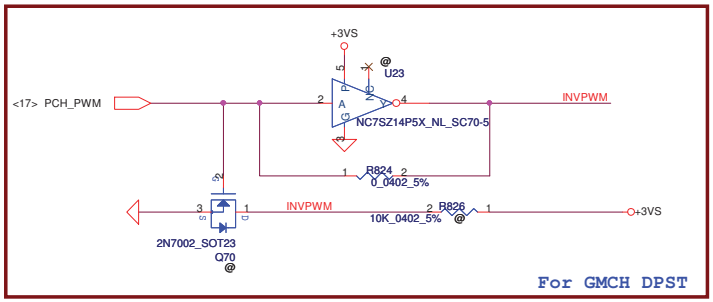
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Size	Document Number	Rev
	PIQY0 LA6881P	1.0
Date: Wednesday, January 05, 2011	Sheet 33 of 63	

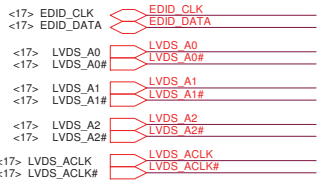
http://hobi-elektronika.net

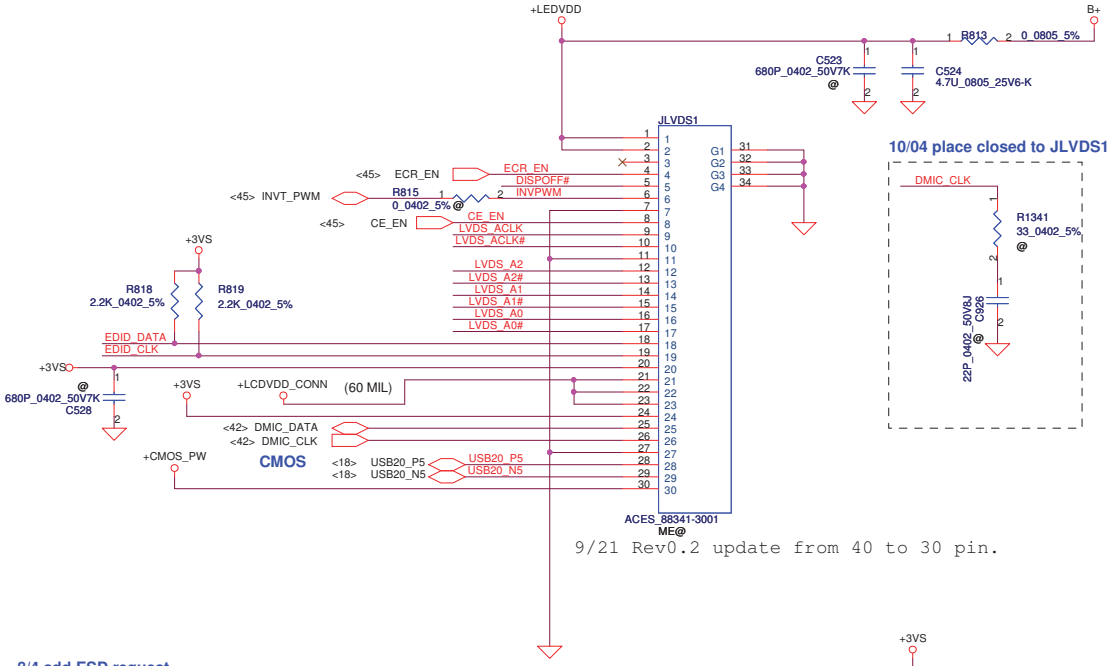


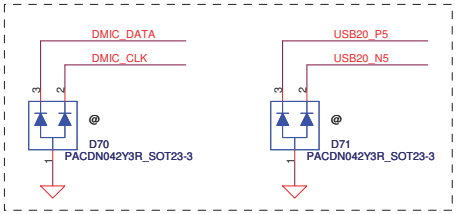
LCD POWER CIRCUIT

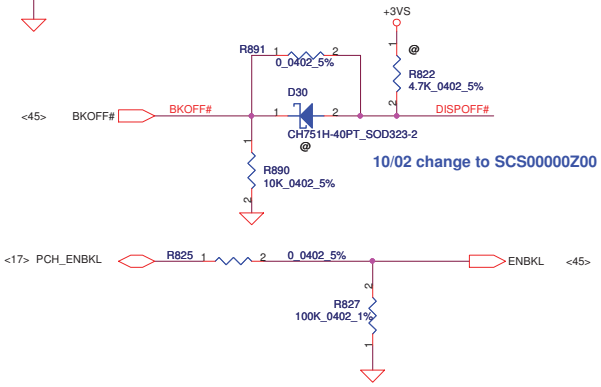


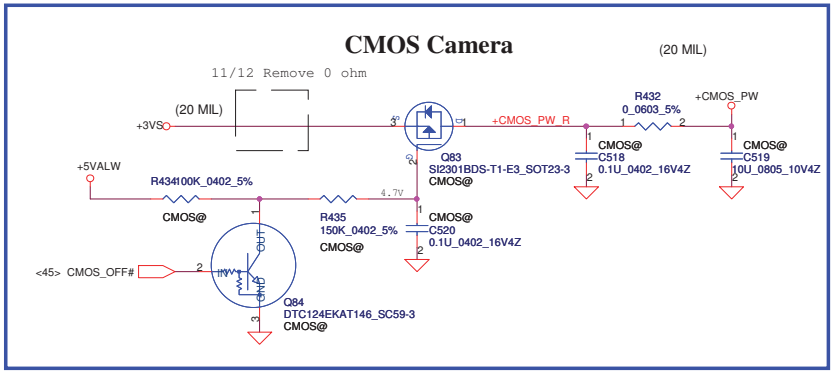










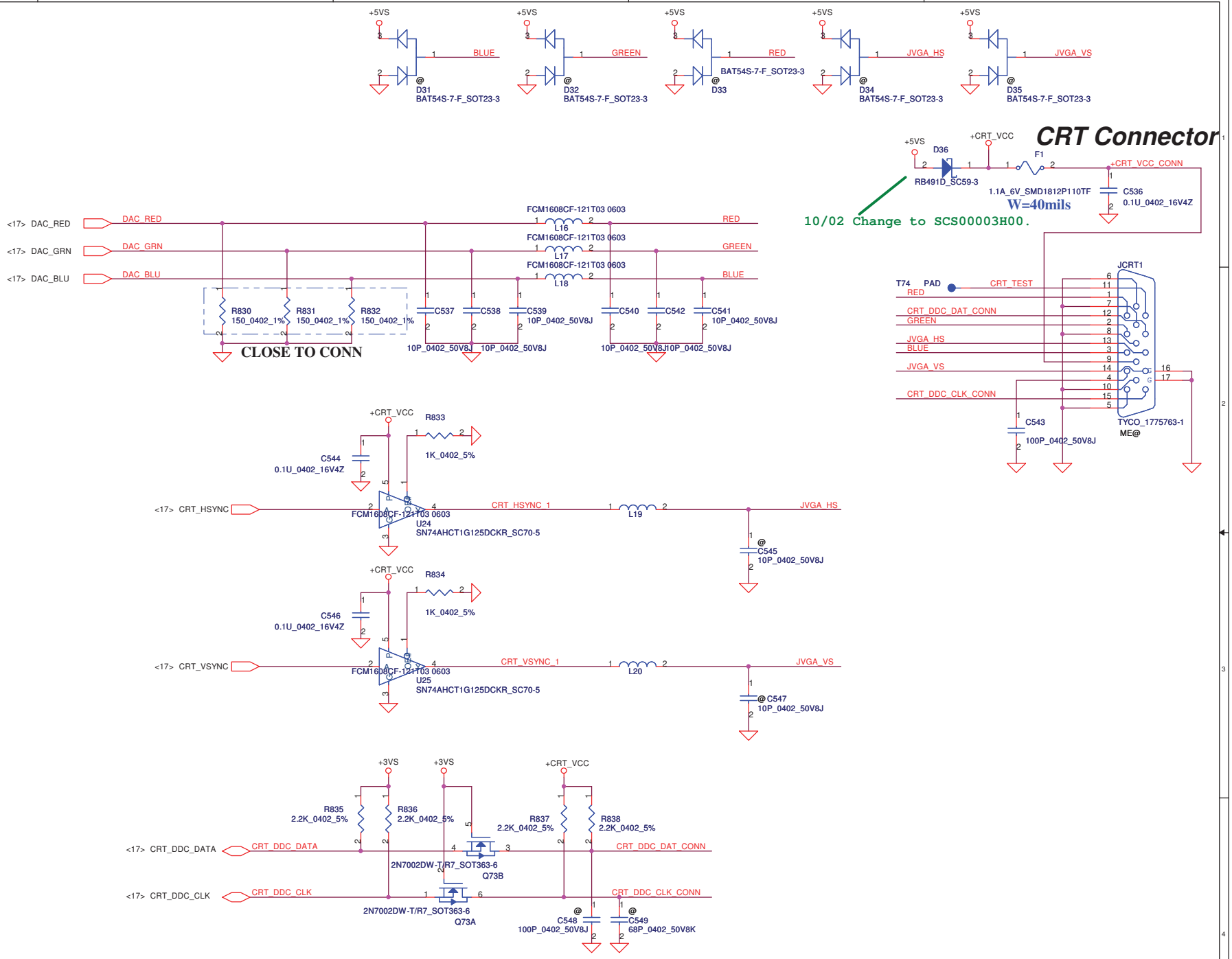


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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: B	Document Number: PIQY0 LA6881P		Rev: 1.0
Date: Wednesday, January 05, 2011	Sheet 34 of 63		

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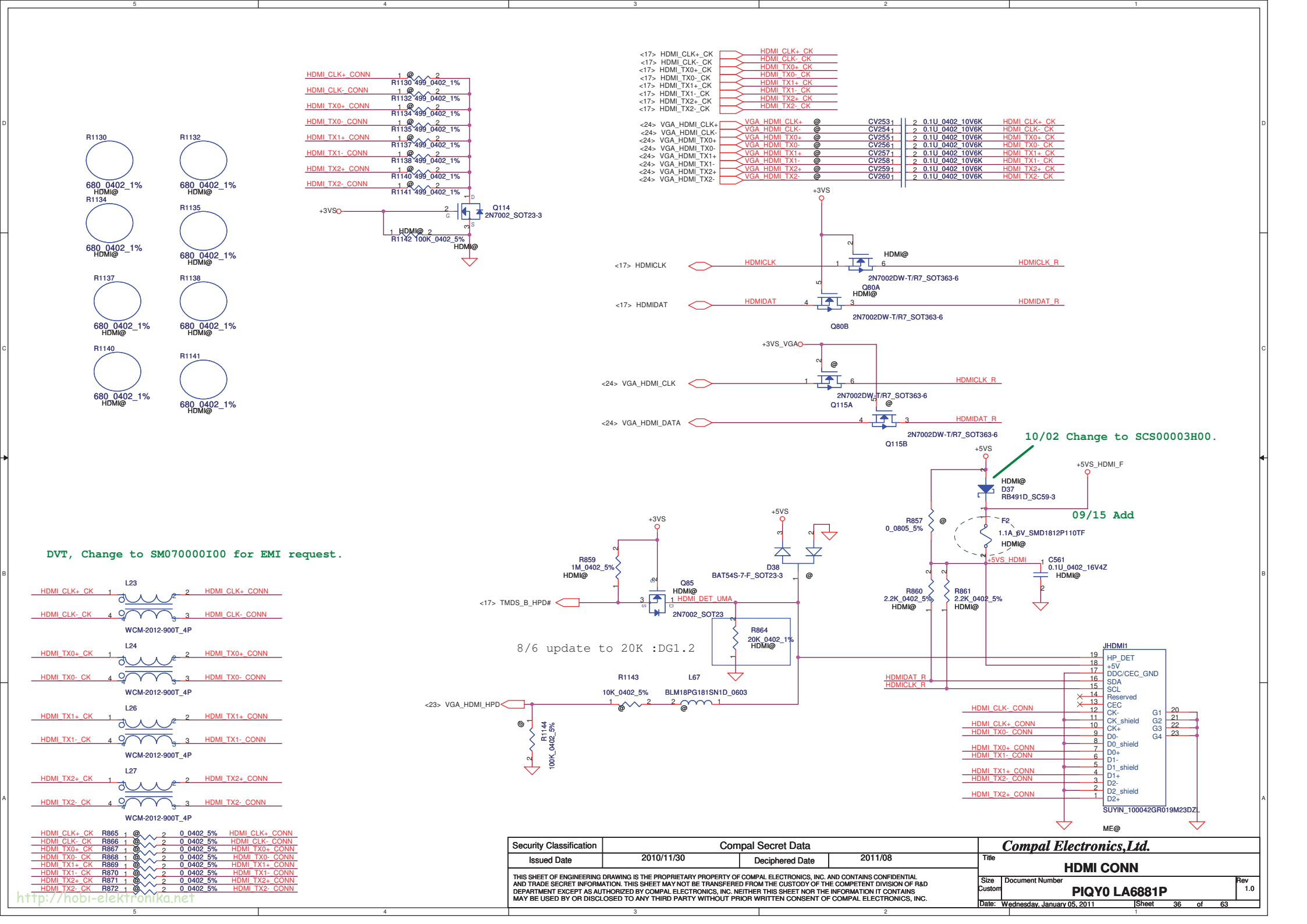
Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	PIQY0 LA6881P	1.0

Date: Wednesday, January 05, 2011 Sheet 35 of 63

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Compal Electronics, Ltd.

Title: HDMI CONN

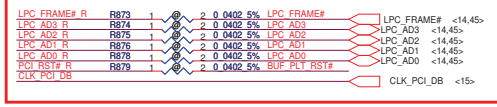
Size	Document Number	Rev
Custom	PIQY0 LA6881P	1.0

Date: Wednesday, January 05, 2011 Sheet 36 of 63

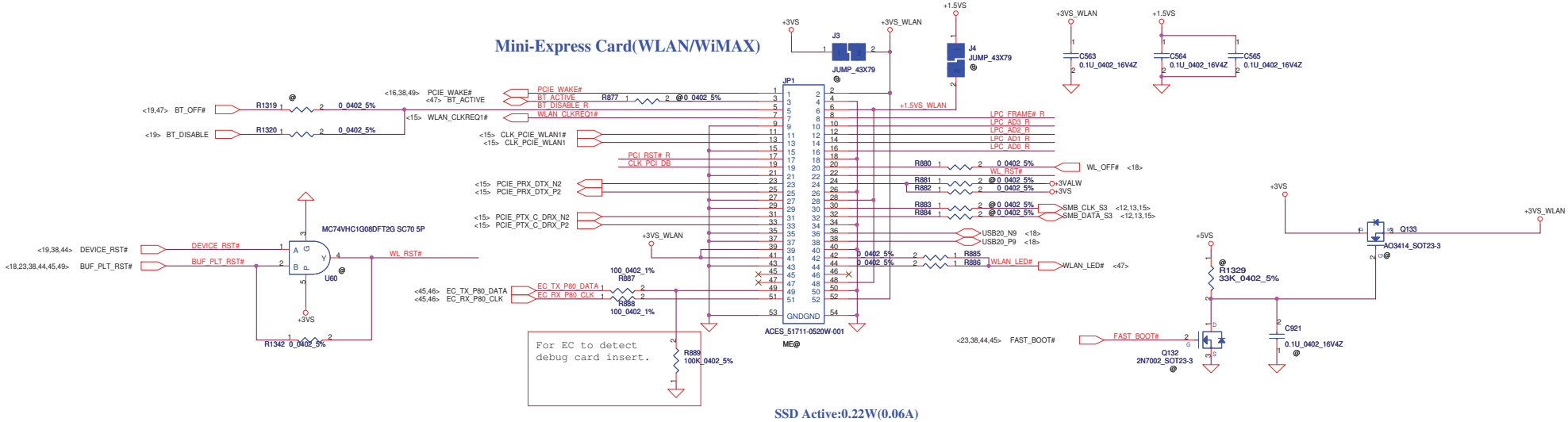
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Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

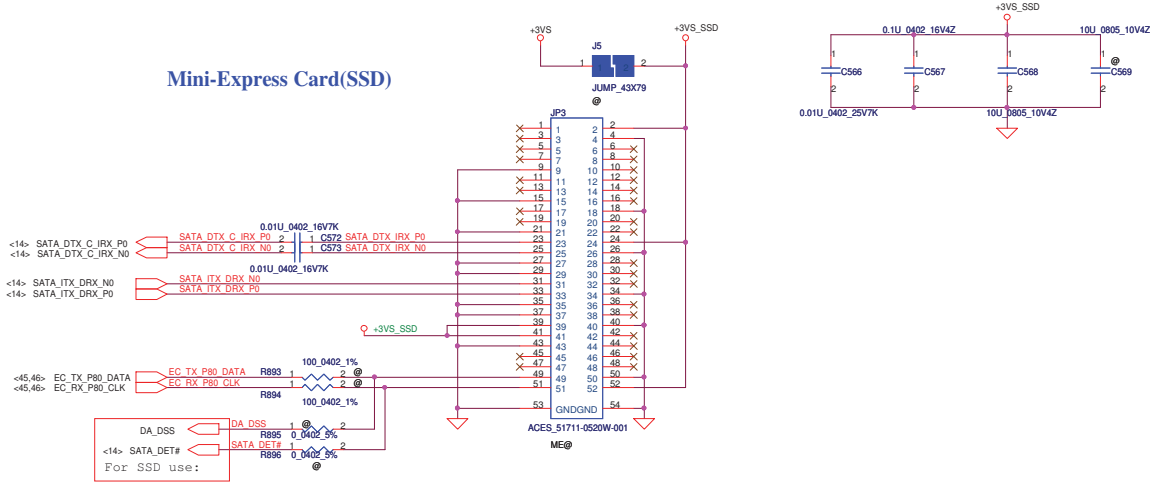


Mini-Express Card(WLAN/WiMAX)



SSD Active:0.22W(0.06A)

Mini-Express Card(SSD)

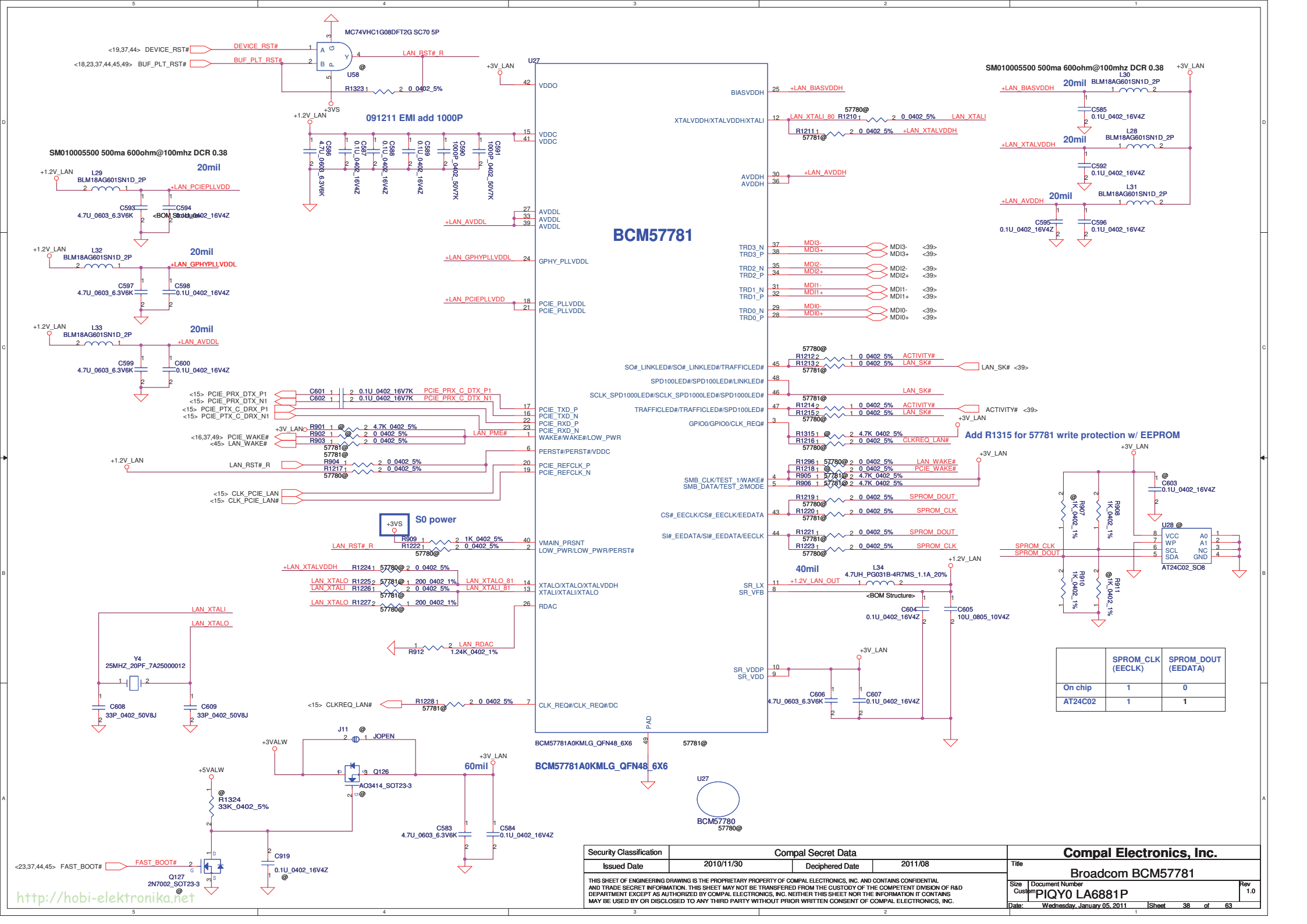


http://hobi-elektronika.net

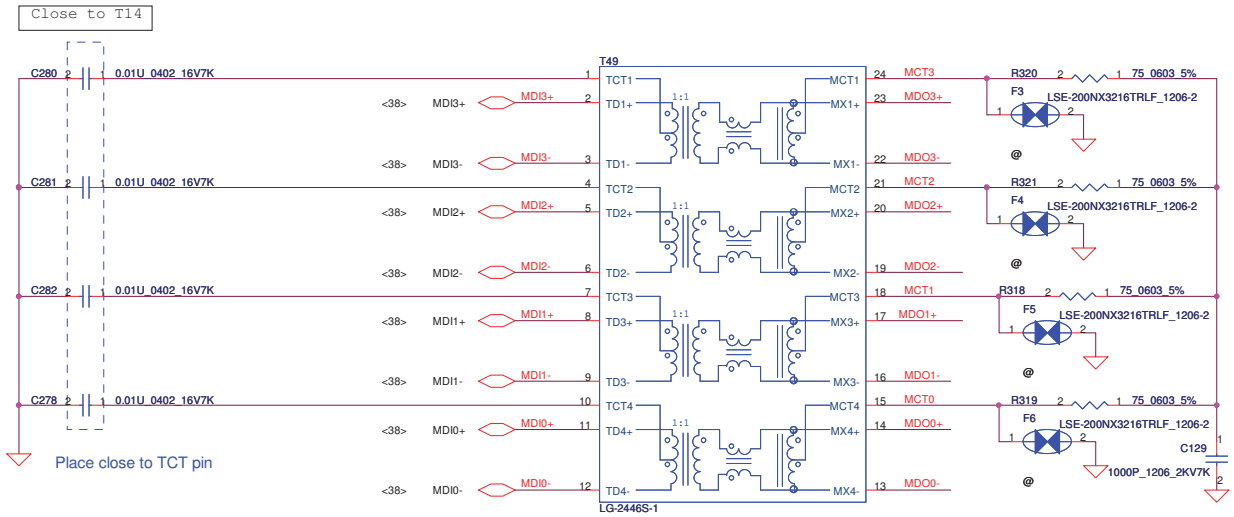
Security Classification	Compal Secret Data		
Issued Date	2010/11/30	Deciphered Date	2011/08

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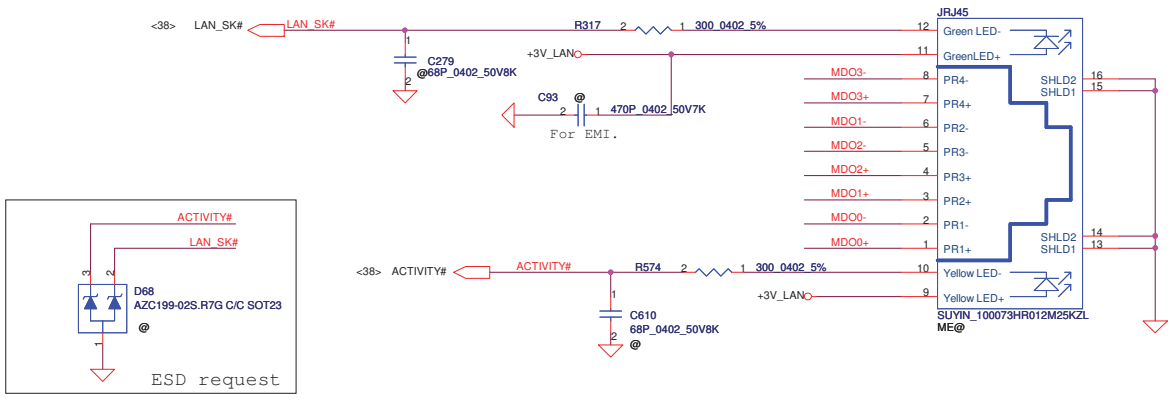
Compal Electronics, Inc.			
Title: Mini-Card			
Size	Document Number: PIQY0 LA6881P		Rev: 1.0
Date: Wednesday, January 05, 2011		Sheet 37 of 63	



	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1



RJ45 Conn.



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Issued Date	2010/11/30	Deciphered Date	2011/08

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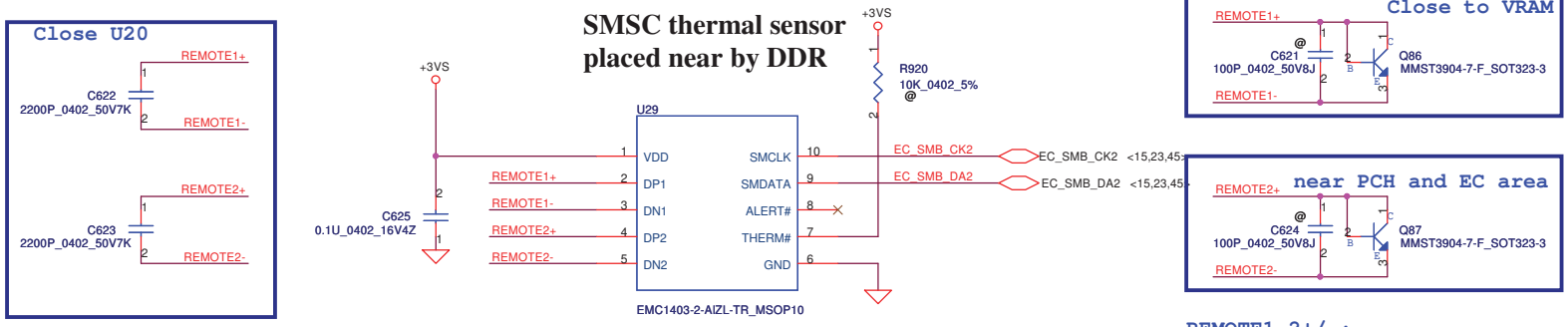
Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: PIQY0 LA6881P | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 39 of 63

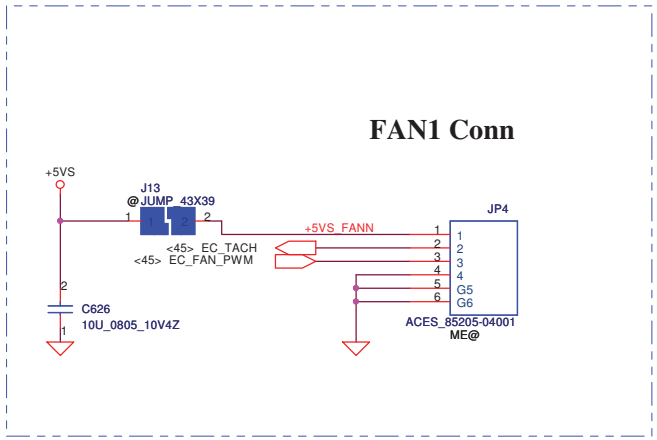
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Address 1001_101xb

8/02 Change PN to SA000046C00, Fintek.

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



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Compal Electronics,Ltd.

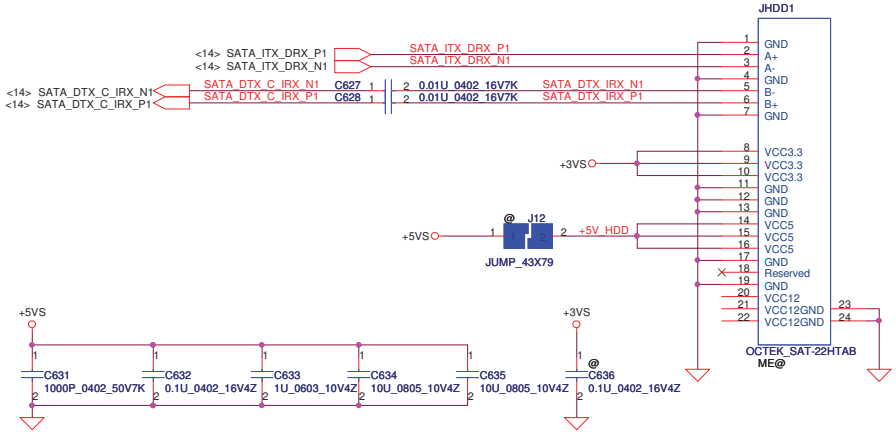
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Size	Document Number	Rev
Custom	PIQY0 LA6881P	1.0

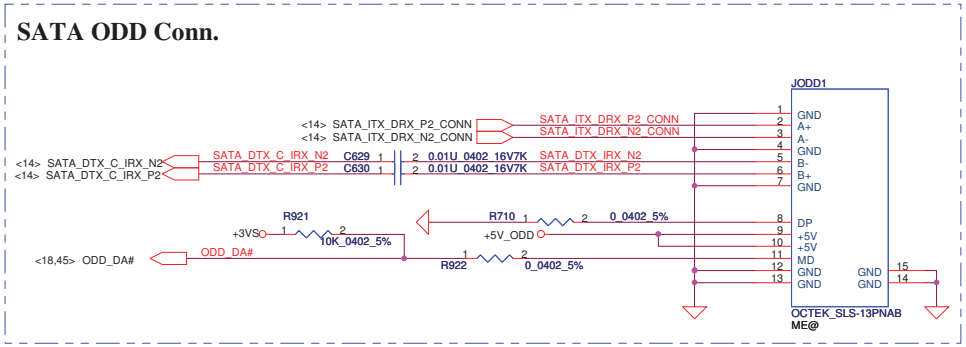
Date: Wednesday, January 05, 2011 Sheet 40 of 63

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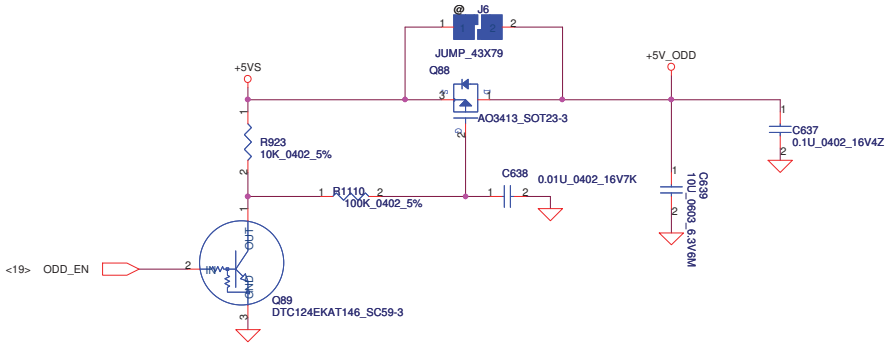
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control



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Issued Date	2010/11/30	Deciphered Date	2011/08

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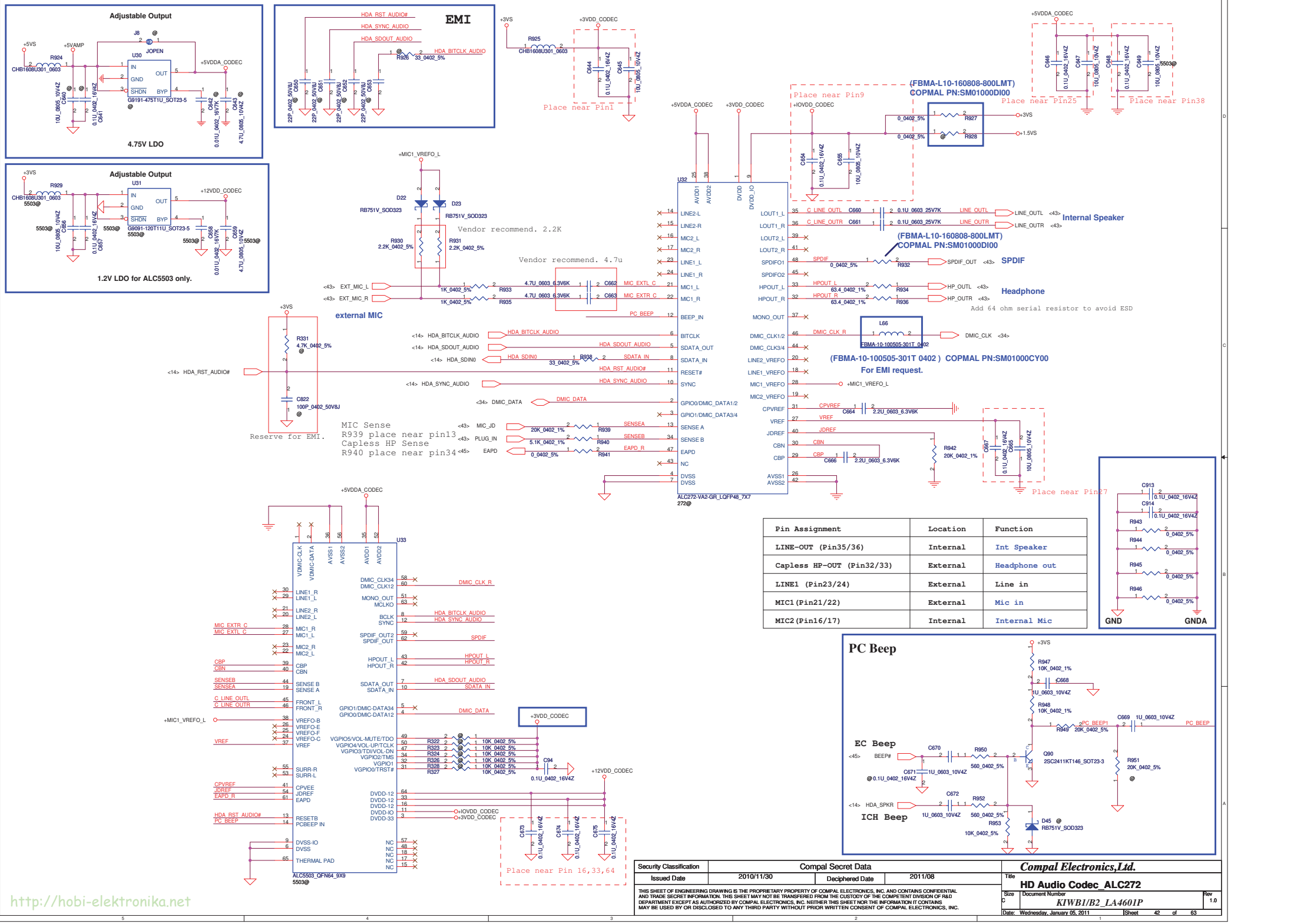
Compal Electronics, Inc.

Title: HDD/ODD Connector

Size: B | Document Number: PIQY0 LA6881P | Rev: 1.0

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Adjustable Output
4.75V LDO
Adjustable Output
1.2V LDO for ALC5503 only.
EMI
HDA_RST_AUDIO#
HDA_SYNC_AUDIO
HDA_SDOUT_AUDIO
HDA_BITCLK_AUDIO
Place near Pin1
Place near Pin9
Place near Pin25
Place near Pin38
(FBMA-L10-160808-800LMT)
COPMAL PN:SM01000DI00
Internal Speaker
SPDIF
Headphone
Add 64 ohm serial resistor to avoid ESD
external MIC
Vendor recommend. 2.2K
Vendor recommend. 4.7u
(FBMA-L10-100505-301T 0402) COPMAL PN:SM01000CY00
For EMI request.
Reserve for EMI.
MIC Sense
R939 place near pin13
Capless HP Sense
R940 place near pin34
ALC272-VA2-GR_LQFP48_7X7
272@
ALC5503_QFN64_9X9
5503@
Place near Pin 16,33,64
Place near Pin27
GND
GNDA
PC Beep
EC Beep
ICH Beep
Pin Assignment | Location | Function
LINE-OUT (Pin35/36) | Internal | Int Speaker
Capless HP-OUT (Pin32/33) | External | Headphone out
LINE1 (Pin23/24) | External | Line in
MIC1(Pin21/22) | External | Mic in
MIC2(Pin16/17) | Internal | Internal Mic
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Compal Electronics,Ltd.
Title: HD Audio Codec_ALC272
Size: C | Document Number: KIWB1/B2_LA4601P | Rev: 1.0
Date: Wednesday, January 05, 2011 | Sheet 42 of 63
http://hobi-elektronika.net

wide 20MIL

SPK_R1- 1 R1280 2 0_0805_5%
SPK_R2+ 1 R1281 2 0_0805_5%
SPK_L1- 1 R1282 2 0_0805_5%
SPK_L2+ 1 R1283 2 0_0805_5%

SPK_R1- CONN
SPK_R2+ CONN
SPK_L1- CONN
SPK_L2+ CONN

JSPK1
1
2
3 GND
4 GND
5
6
ACES_87213-0400G
ME@

C678 @ 1000P_0402_50V7K
C679 @ 1000P_0402_50V7K
C680 @ 1000P_0402_50V7K
C681 @ 1000P_0402_50V7K

SPK_R1- CONN
SPK_R2+ CONN
SPK_L1- CONN
SPK_L2+ CONN
HP_OUTR
HP_OUTL

D59 @ PACDN042Y3R_SOT23-3
D60 @ PACDN042Y3R_SOT23-3
D61 @ PACDN042Y3R_SOT23-3

Reserve for ESD request.

EXT_MIC_L-2
EXT_MIC_R-2

D69
ZEN ROW PJDLC05C 3P C/A SOT23
@
ESD request

Audio Jack
MIC IN

<42> EXT_MIC_L
EXT_MIC_L
L37
FBMA-L10-160808-121LMT_2P
EXT_MIC_L-2
C676 47P_0402_50V8J
@C677 10P_0402_50V8J
GNDA

<42> EXT_MIC_R
EXT_MIC_R
L40
FBMA-L10-160808-121LMT_2P
EXT_MIC_R-2
C682 47P_0402_50V8J
@C683 10P_0402_50V8J
GNDA

<42> MIC_JD
MIC_JD
10P_0402_50V8J C684 @
GNDA

JMIC1
GND GND GND GND
SUYIN_010168FR006G576ZL
ME@

220P_0402_50V7K C685
220P_0402_50V7K C686

Headphone

@R954 1K_0402_5%
@R955 1K_0402_5%
GNDA

<42> HP_OUTR
HP_OUTR
L41 FBMA-L10-160808-121LMT_2P
PR-OUT

<42> HP_OUTL
HP_OUTL
L42 FBMA-L10-160808-121LMT_2P
PL-OUT

JHP1

<42> PLUG_IN
PLUG_IN

+5VS

<42> SPDIF_OUT
SPDIF_OUT

C688 220P_0402_50V7K
C687 0.1U_0402_16V4Z

DRIVE IC
GND GND
SINGA_2SJ-A373-H03
ME@

+3VALW
R956 10K_0402_5% @
R957 0_0402_5%
AMP_OFF#
EC_MUTE#
EC_MUTE# <45>

+5VAMP
W=40mil

U34
VDD
PVDD
PVDD
GAIN0
GAIN1
LIN-
RIN-
LIN+
RIN+
NC
SHUTDOWN
LOUT-
ROUT-
LOUT+
ROUT+
GND GND GND GND GND
BYPASS
TPA6017A2PWPR_TSSOP20

SPK_L1-
SPK_R1-
SPK_L2+
SPK_R2+
20mil

<42> LINE_OUTL
LINE_OUTL
C924 0.033U_0402_16V7K
LIN

<42> LINE_OUTR
LINE_OUTR
C925 0.033U_0402_16V7K
RIN

R960 @ 10K_0402_5%
R961 @ 10K_0402_5%

C691 0.1U_0603_25V7K
C692 0.1U_0603_25V7K
C695 4.7U_0805_10V4Z

GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

+5VAMP
R962 @ 100K_0402_1%
GAIN0
R965 100K_0402_1%

+5VAMP
R963 100K_0402_1%
GAIN1
R966 100K_0402_1% @

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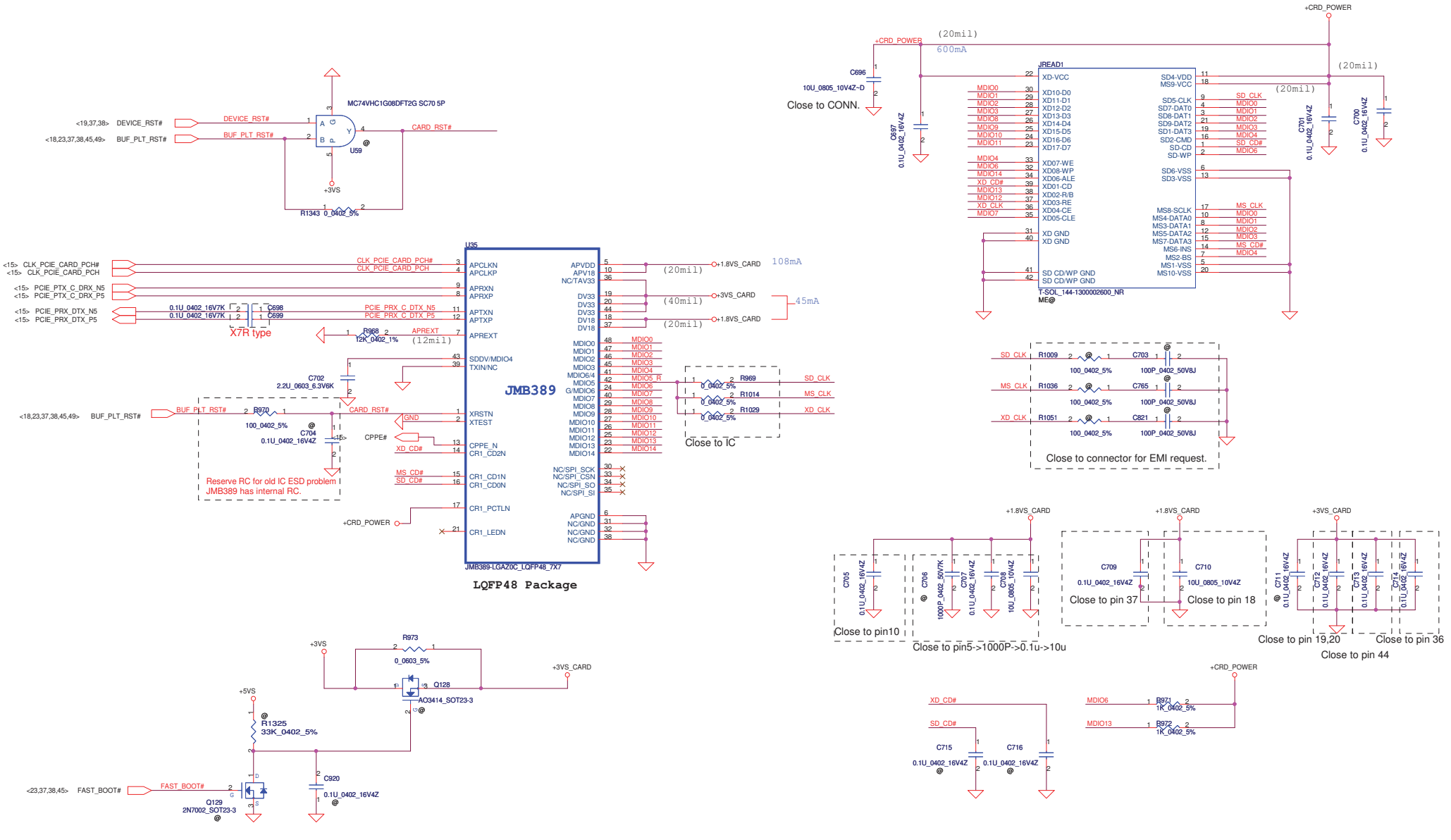
Compal Electronics,Ltd.

Title: AMP,Audio speaker CONN

Size: Custom | Document Number: KIWB1/B2_LA4601P | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 43 of 63

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Compal Electronics, Inc.

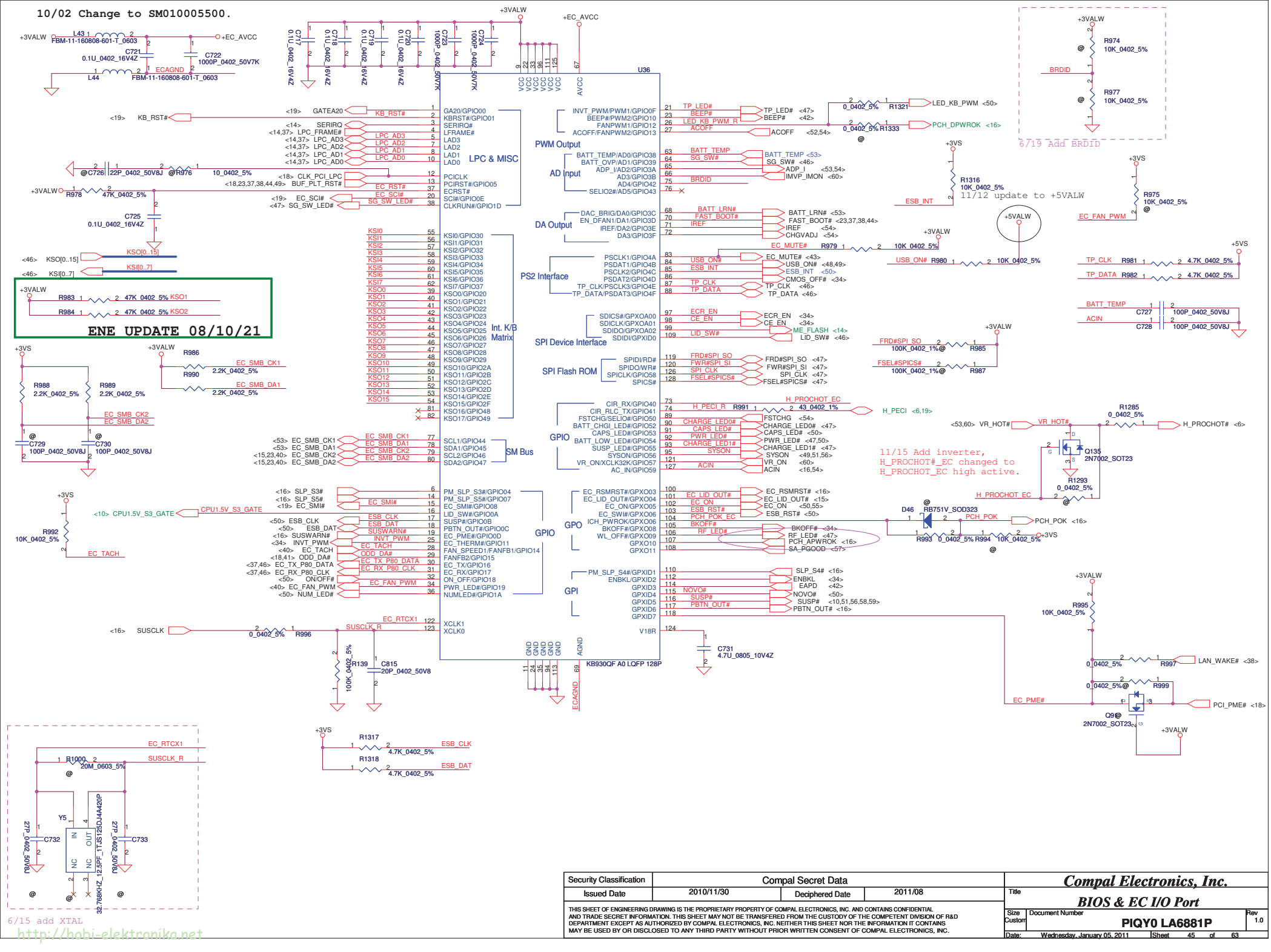
Title: Carder JMB389

Size	Document Number	Rev
Custom	PIQY0 LA6881P	1.0

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10/02 Change to SM010005500.



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Issued Date	2010/11/30	Deciphered Date	2011/08

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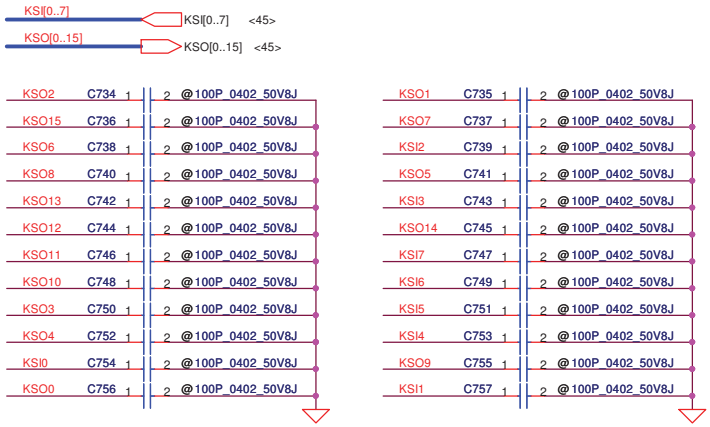
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

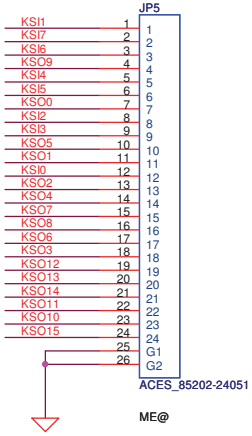
Size	Document Number	Rev
Custom	PIQY0 LA6881P	1.0

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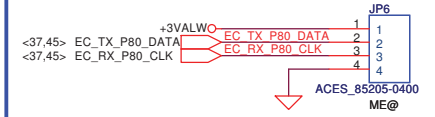
INT_KBD Conn.



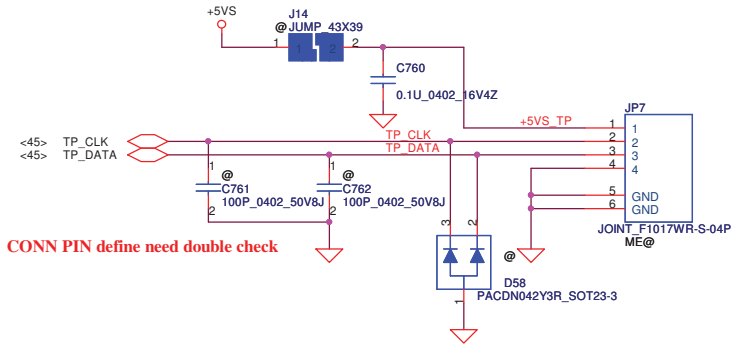
CONN PIN define need double check



EC DEBUG PORT

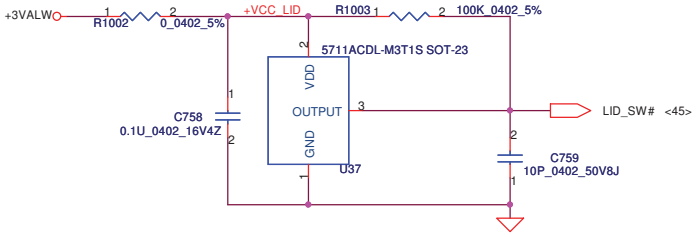


To TP/B Conn.

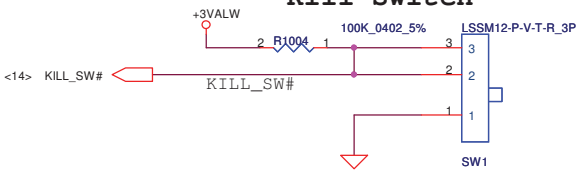


CONN PIN define need double check

Lid Switch

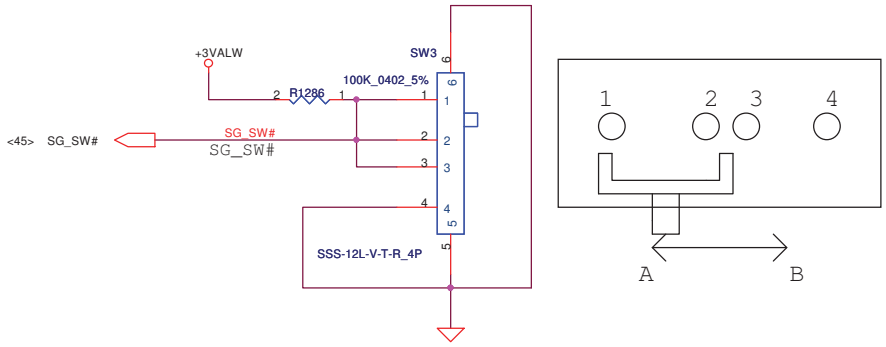


Kill Switch



Kill

STATUS	
1,2(LOW)	OFF
2,3(HI)	ON



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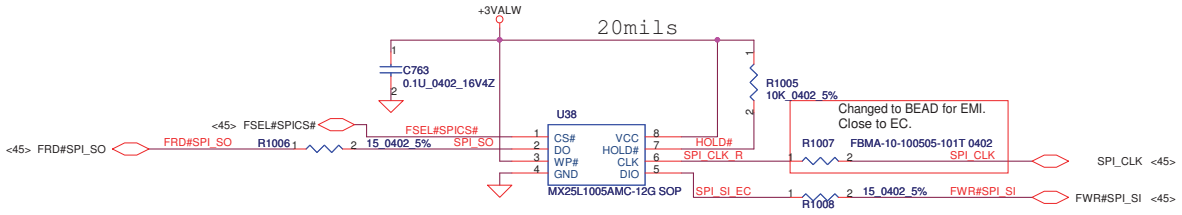
Compal Electronics, Inc.

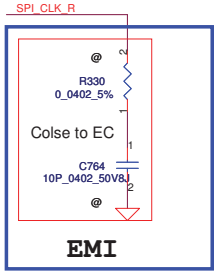
Title: KB /SW /LPC Debug Conn.

Size	Document Number	Rev
B	PIQY0 LA6881P	1.0

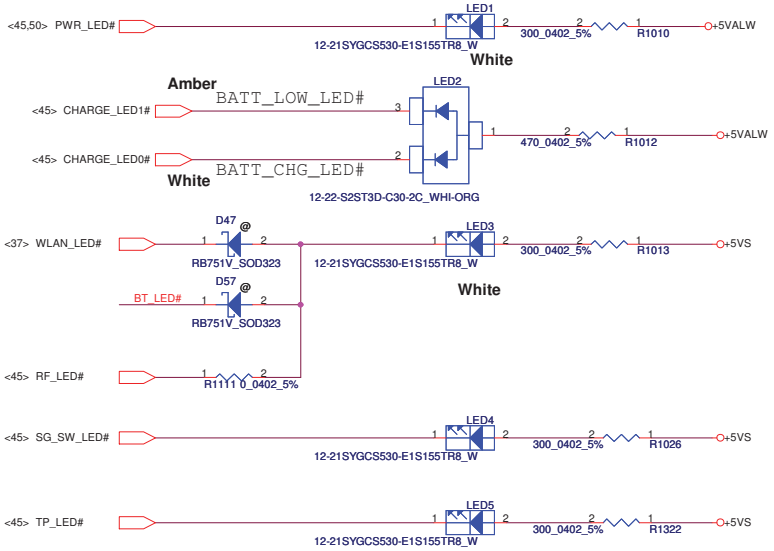
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FOR EC 128KB SPI ROM
(150mil PACKAGE)
P/N : SA00002C100

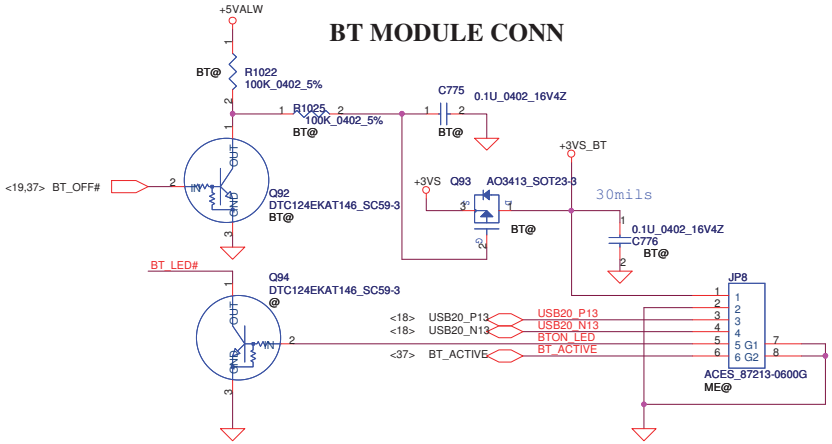


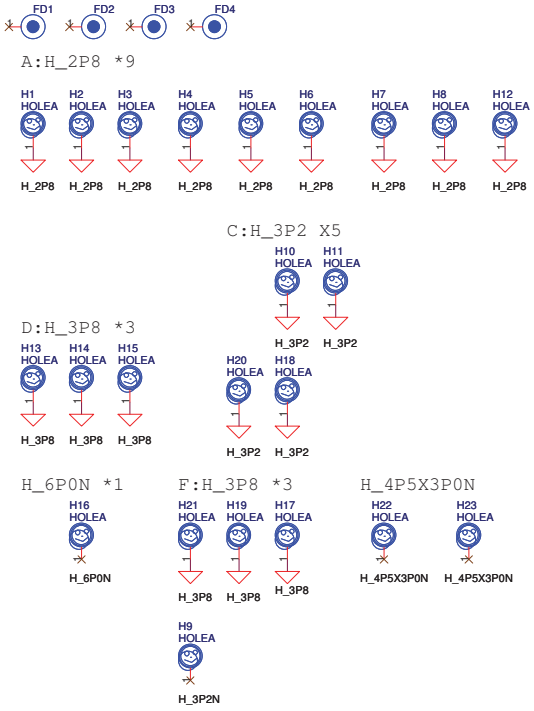


LED



BT MODULE CONN





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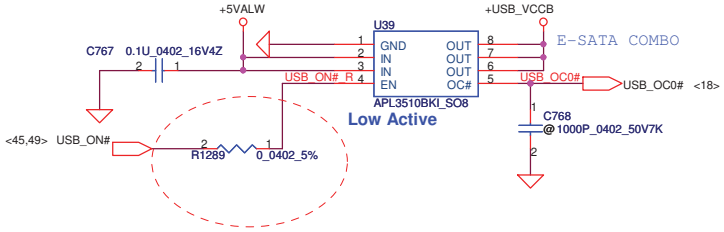
Compal Electronics, Inc.

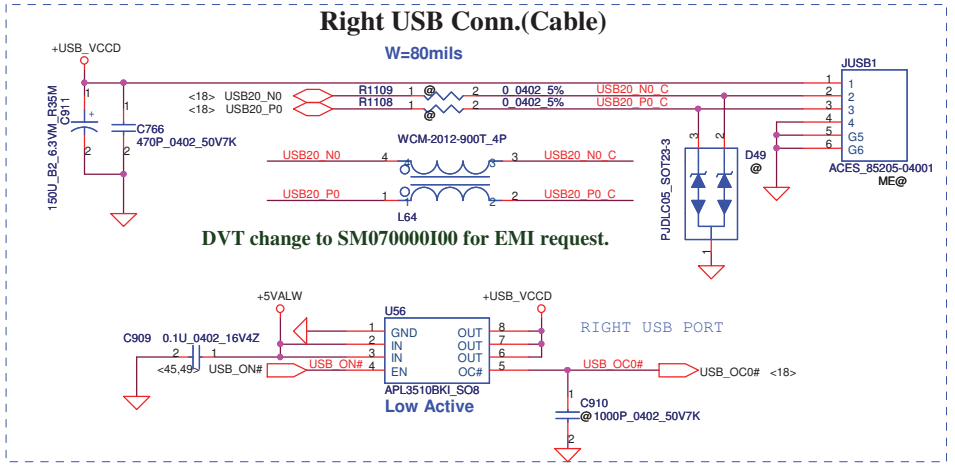
Title: **LED/EC SPI ROM/BT**

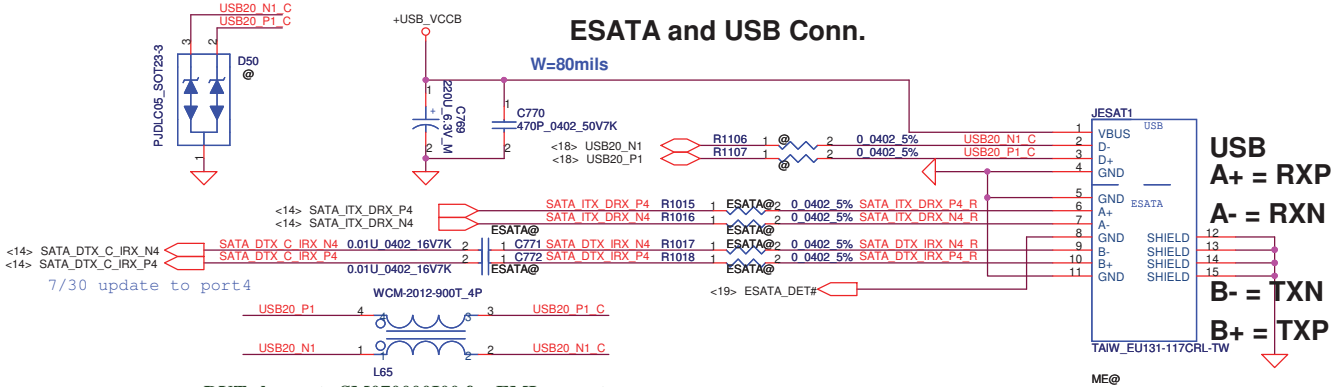
Size	Document Number	Rev
B	PIQY0 LA6881P	1.0

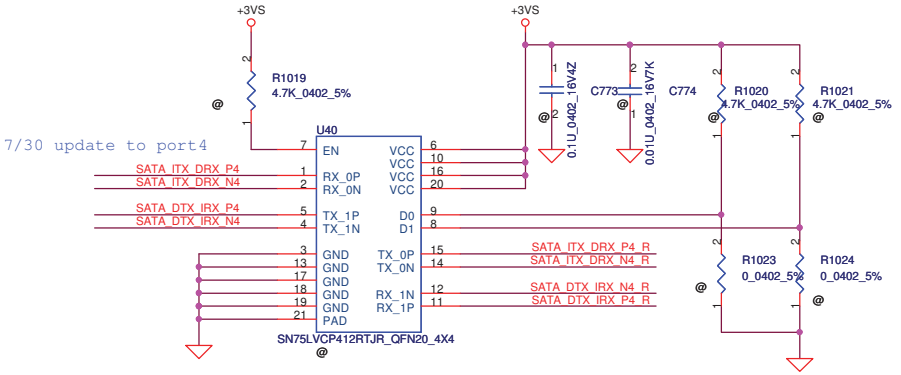
Date: Wednesday, January 05, 2011 Sheet 47 of 63

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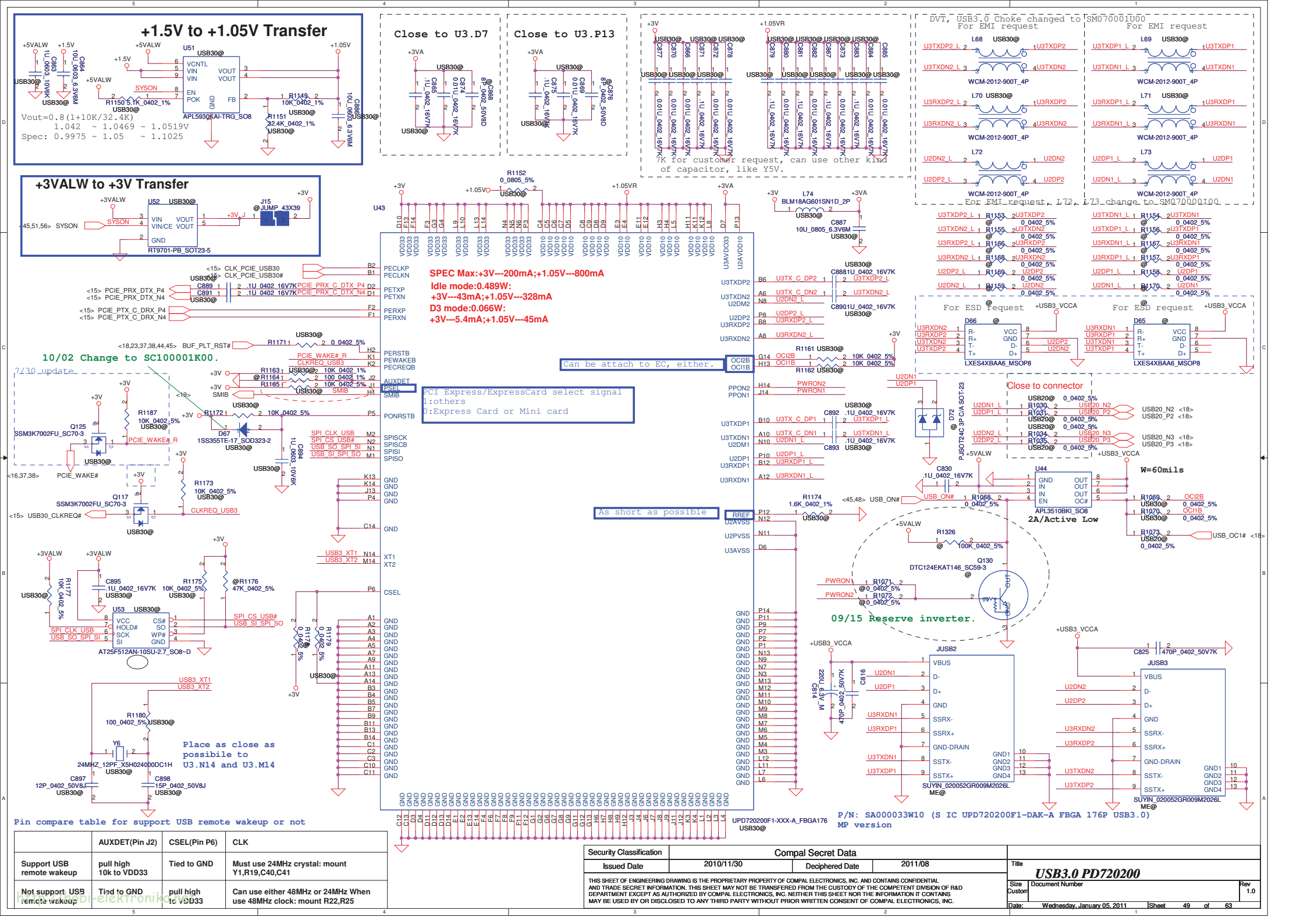


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Compal Electronics, Inc.			
Title	USB ports/E-SATA		
Size: Custom	Document Number: PIQY0 LA6881P		Rev: 1.0
Date: Wednesday, January 05, 2011	Sheet 48 of 63		

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	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

http://laptop-elektronika.pl

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Issued Date	2010/11/30	Deciphered Date	2011/08

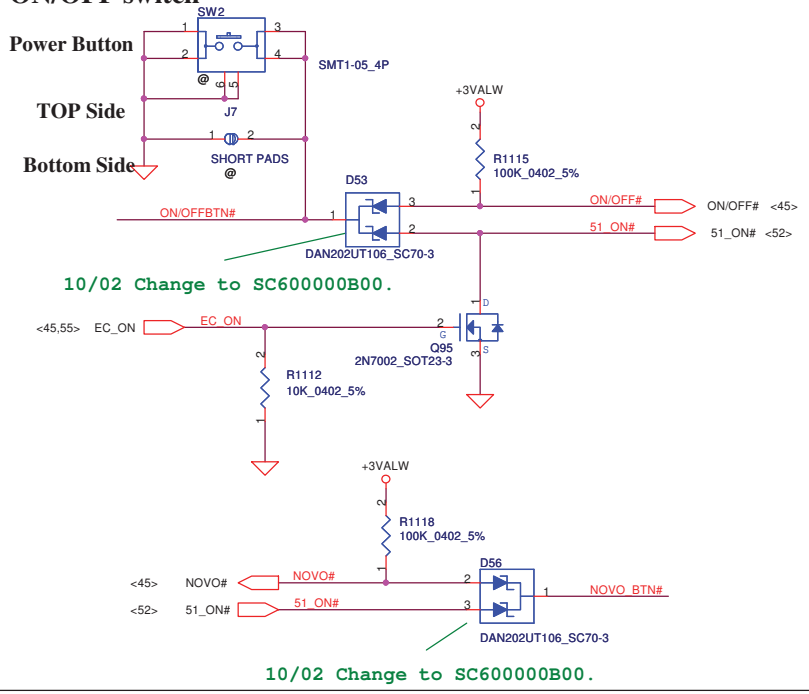
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Title: USB3.0 PD720200

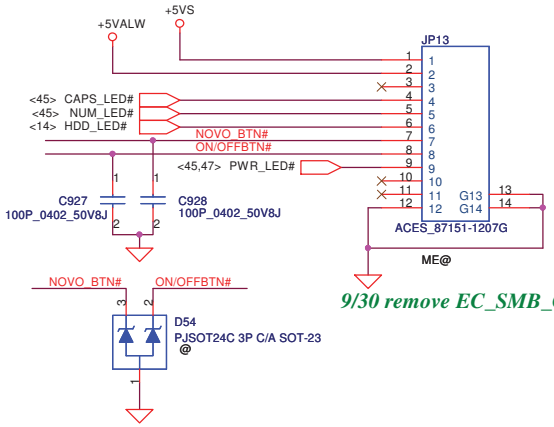
Size: Custom | Document Number | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 49 of 63

ON/OFF switch



Power Bottom Board Conn. 10pin



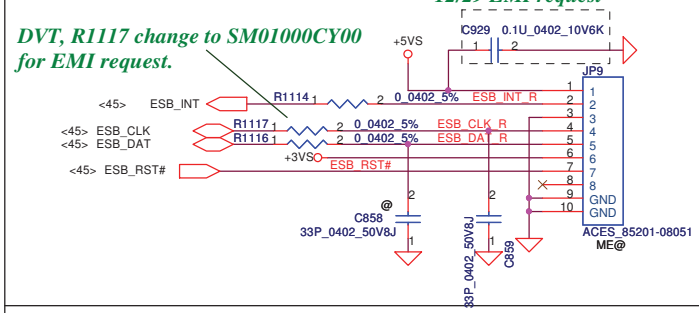
9/30 remove EC_SMB_CK2, EC_SMB_DA2

EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

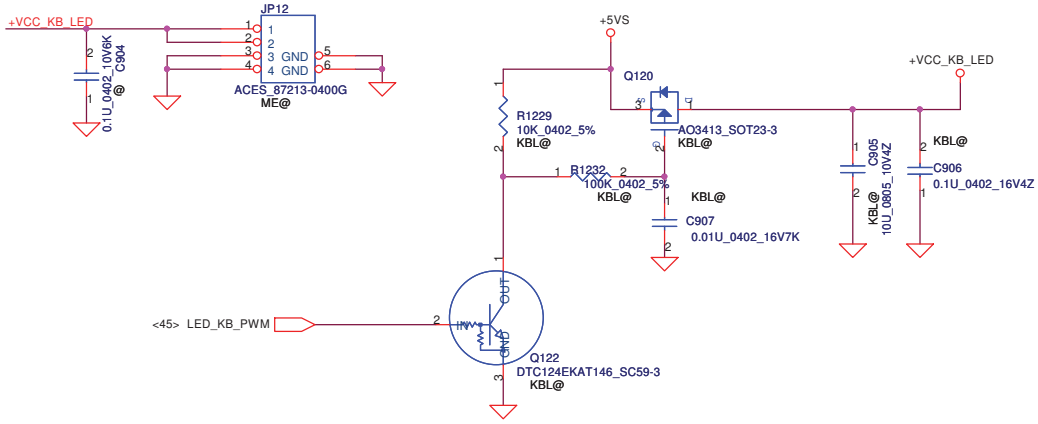
Silder Bar Board Mdule Conn. 6pin

12/29 EMI request

DVT, R1117 change to SM01000CY00 for EMI request.



KB Lighting CONN.4pin



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Issued Date	2010/11/30	Deciphered Date	2011/08

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Compal Electronics,Ltd.

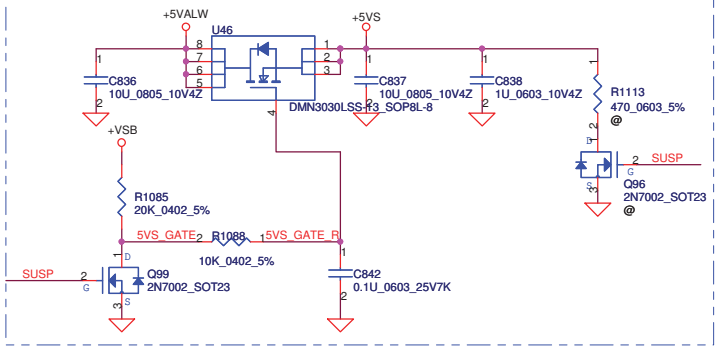
Title: **other IO connector**

Size	Document Number	Rev
Custom	PIQY0 LA6881P	1.0

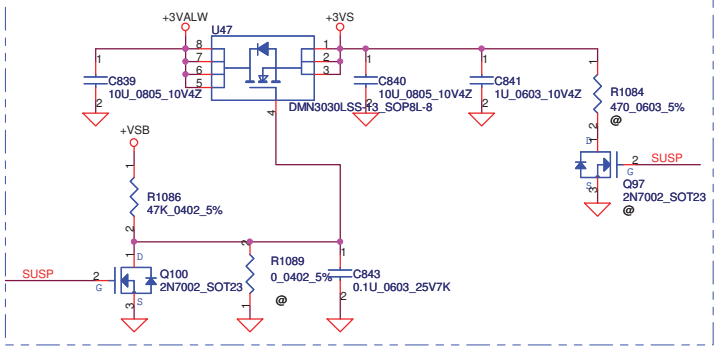
Date: Wednesday, January 05, 2011 | Sheet 50 of 63

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+5VALW TO +5VS

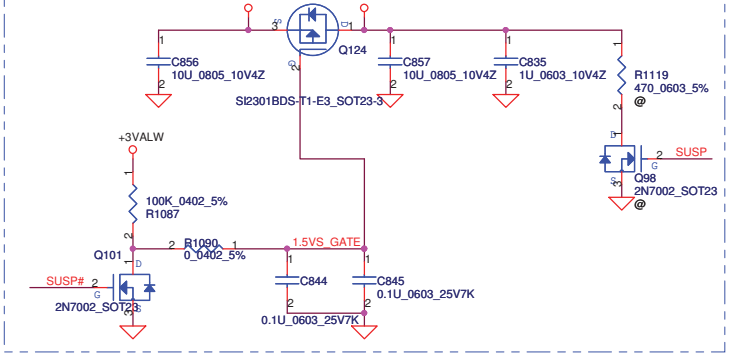


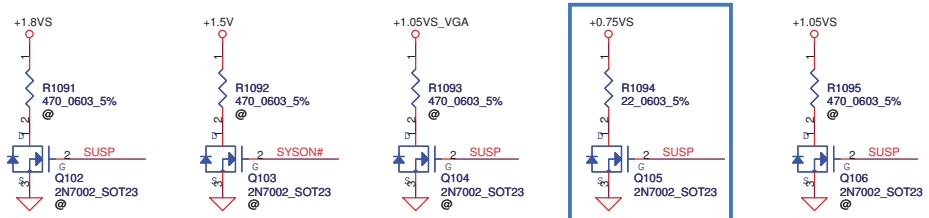
+3VALW TO +3VS



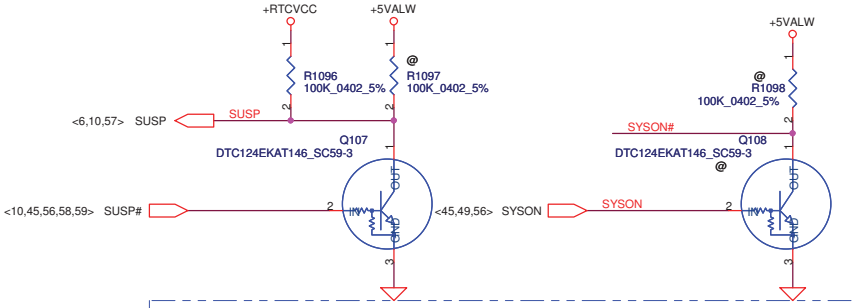
+1.5V to +1.5VS

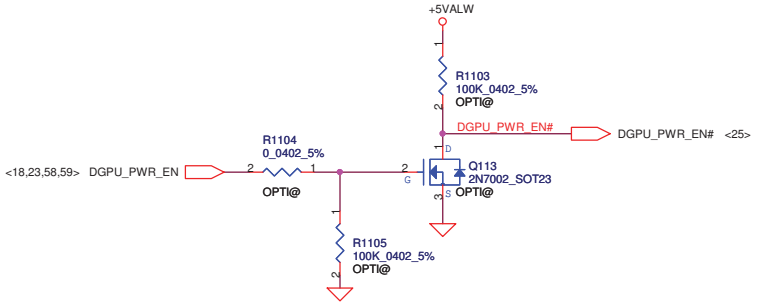
7/26 change SI4800 to SI2301



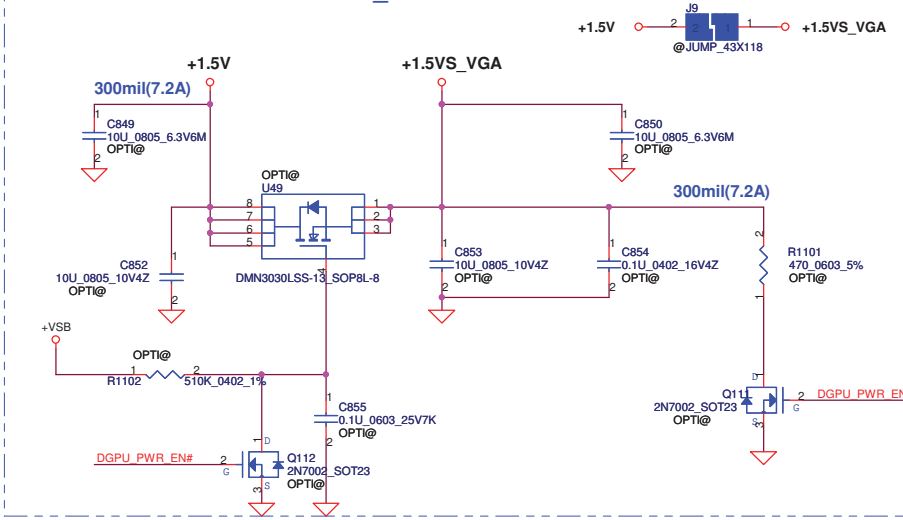


For Intel S3 Power Reduction.





+1.5V to +1.5VS_VGA Transfer



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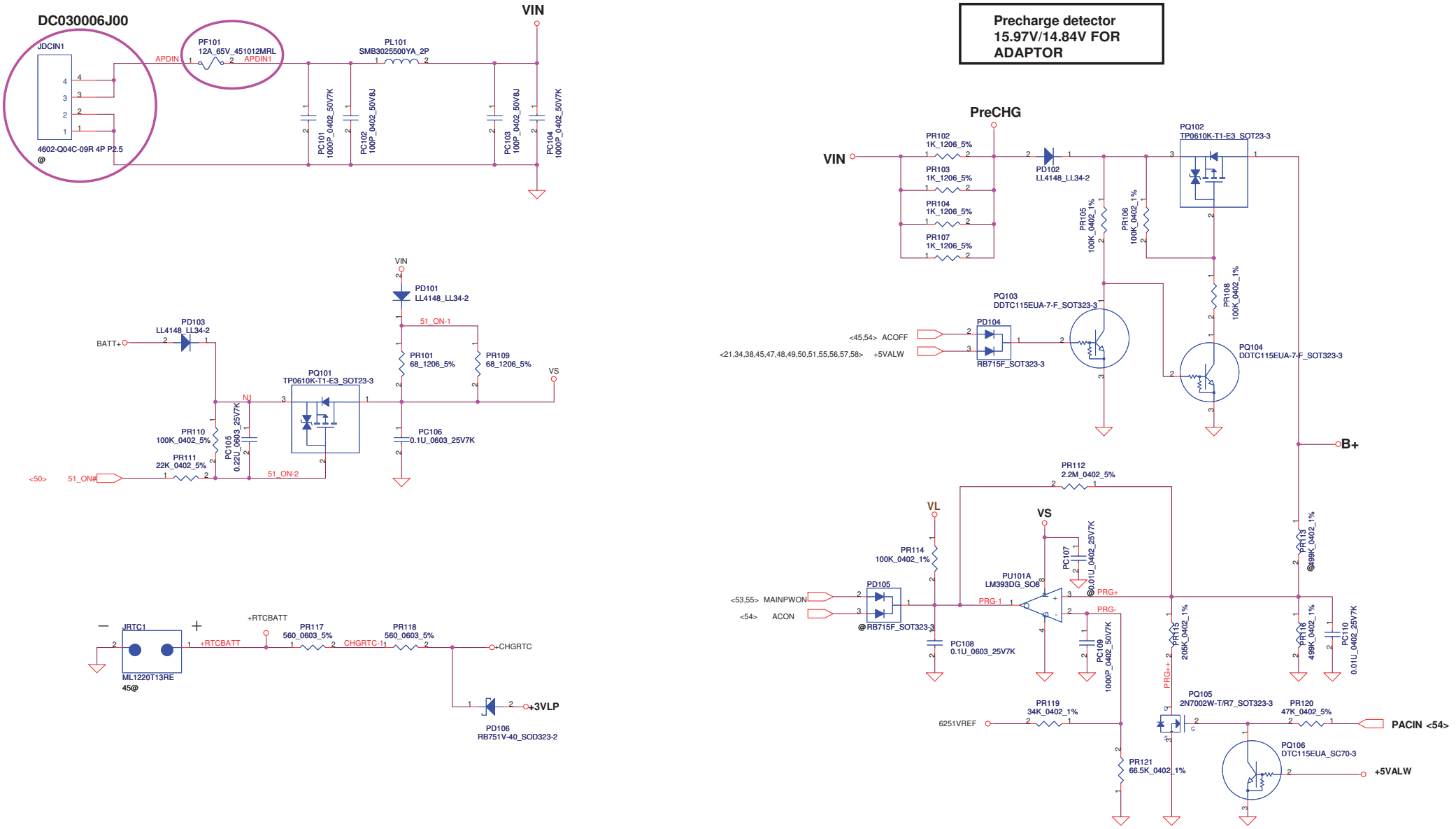
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Title: DC Interface

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ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

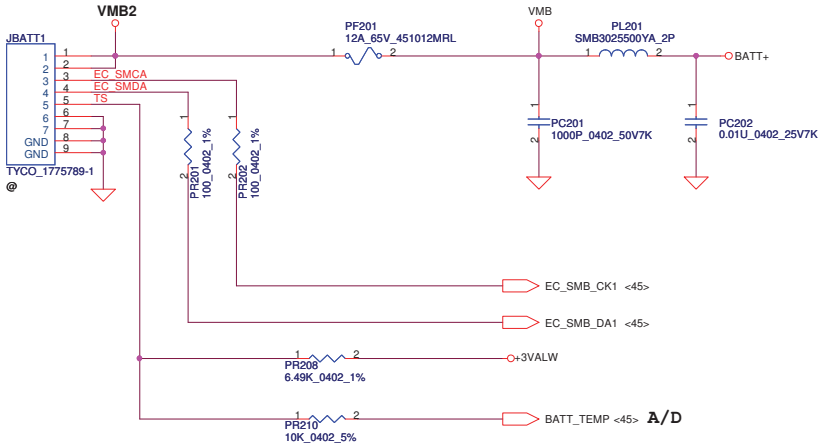
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

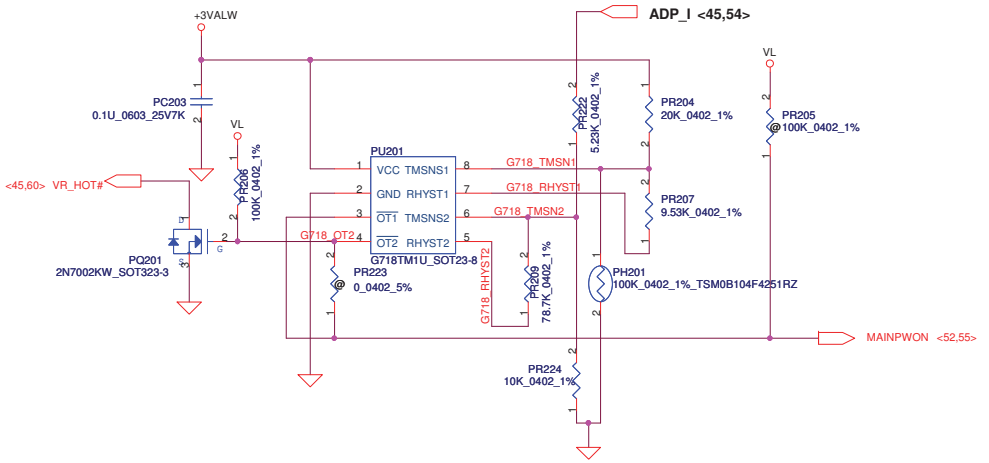
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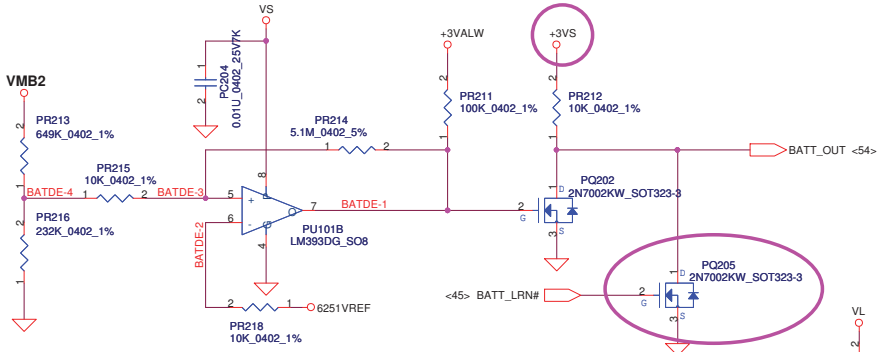
Compal Electronics, Inc.			
Title	PWR DCIN / Vin Detector /Pre-charge		
Size: Custom	Document Number: PIQY0/Y1		Rev: 1.0
Date: Wednesday, January 05, 2011	Sheet 52 of 63		

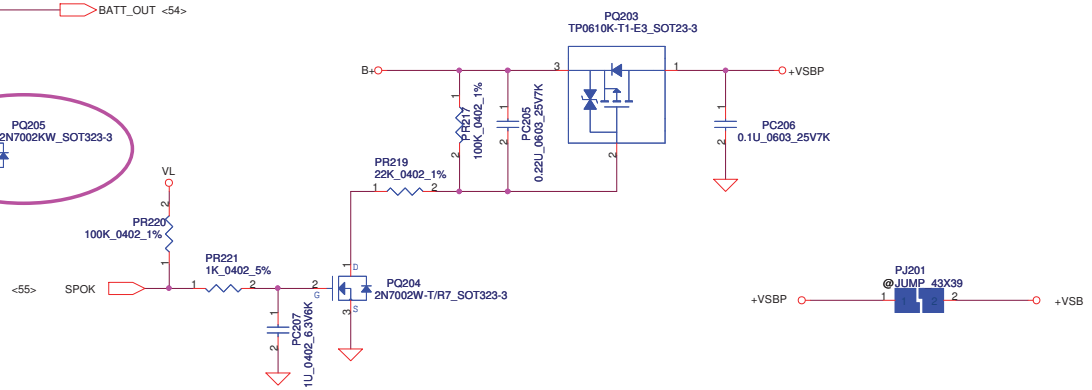
http://hobi-elektronika.net

PH201 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C







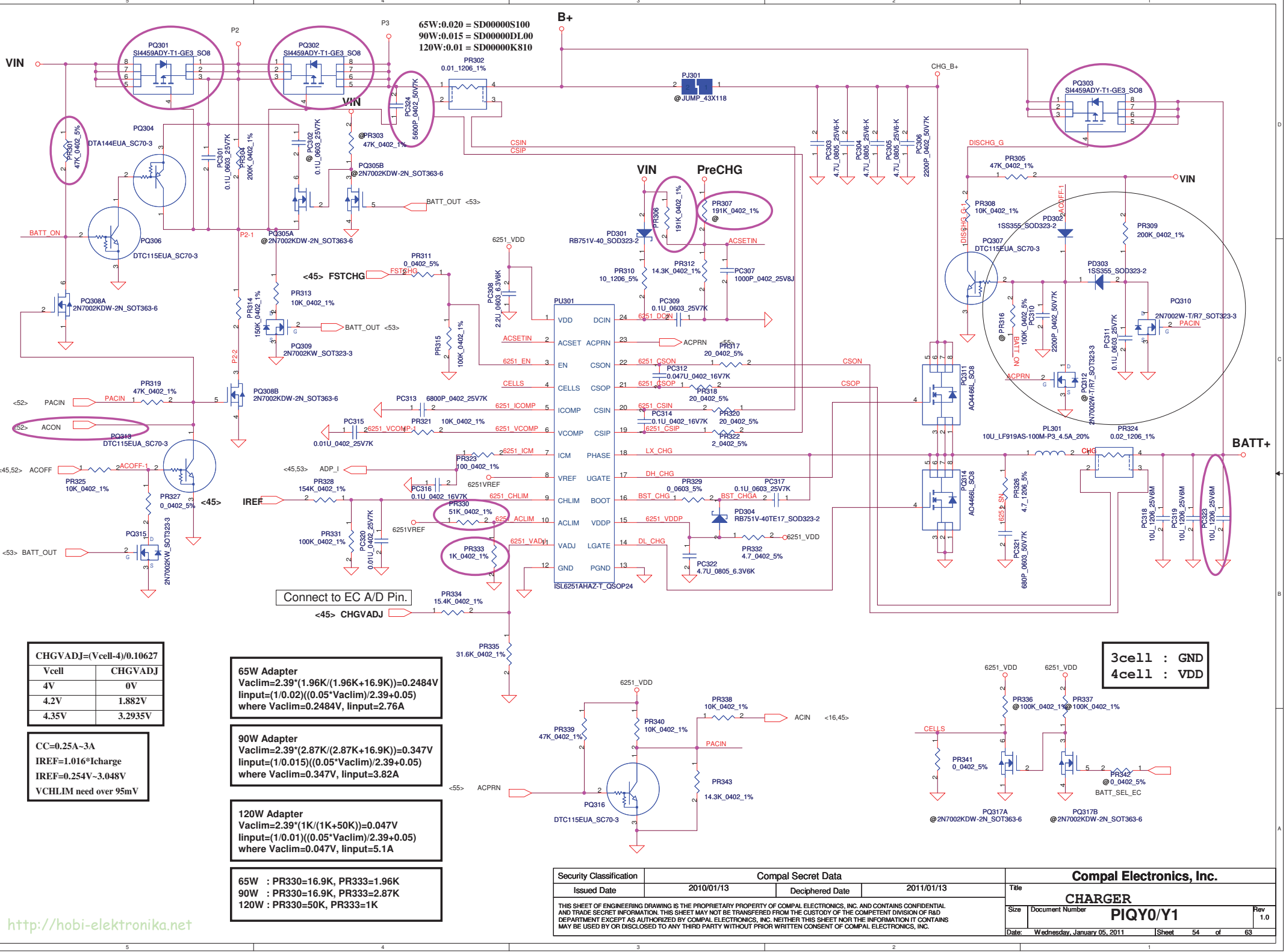


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Compal Electronics, Inc.			
Title: PWR-BATTERY CONN/OTP			
Size: Custom	Document Number: PIQY0/Y1		Rev: 1.0
Date: Wednesday, January 05, 2011	Sheet 53 of 63		

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CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

65W Adapter
Vaclim=2.39*(1.96K/(1.96K+16.9K))=0.2484V
linput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.2484V, linput=2.76A

90W Adapter
Vaclim=2.39*(2.87K/(2.87K+16.9K))=0.347V
linput=(1/0.015)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.347V, linput=3.82A

120W Adapter
Vaclim=2.39*(1K/(1K+50K))=0.047V
linput=(1/0.01)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.047V, linput=5.1A

65W : PR330=16.9K, PR333=1.96K
90W : PR330=16.9K, PR333=2.87K
120W : PR330=50K, PR333=1K

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Issued Date	2010/01/13	Deciphered Date	2011/01/13

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Compal Electronics, Inc.

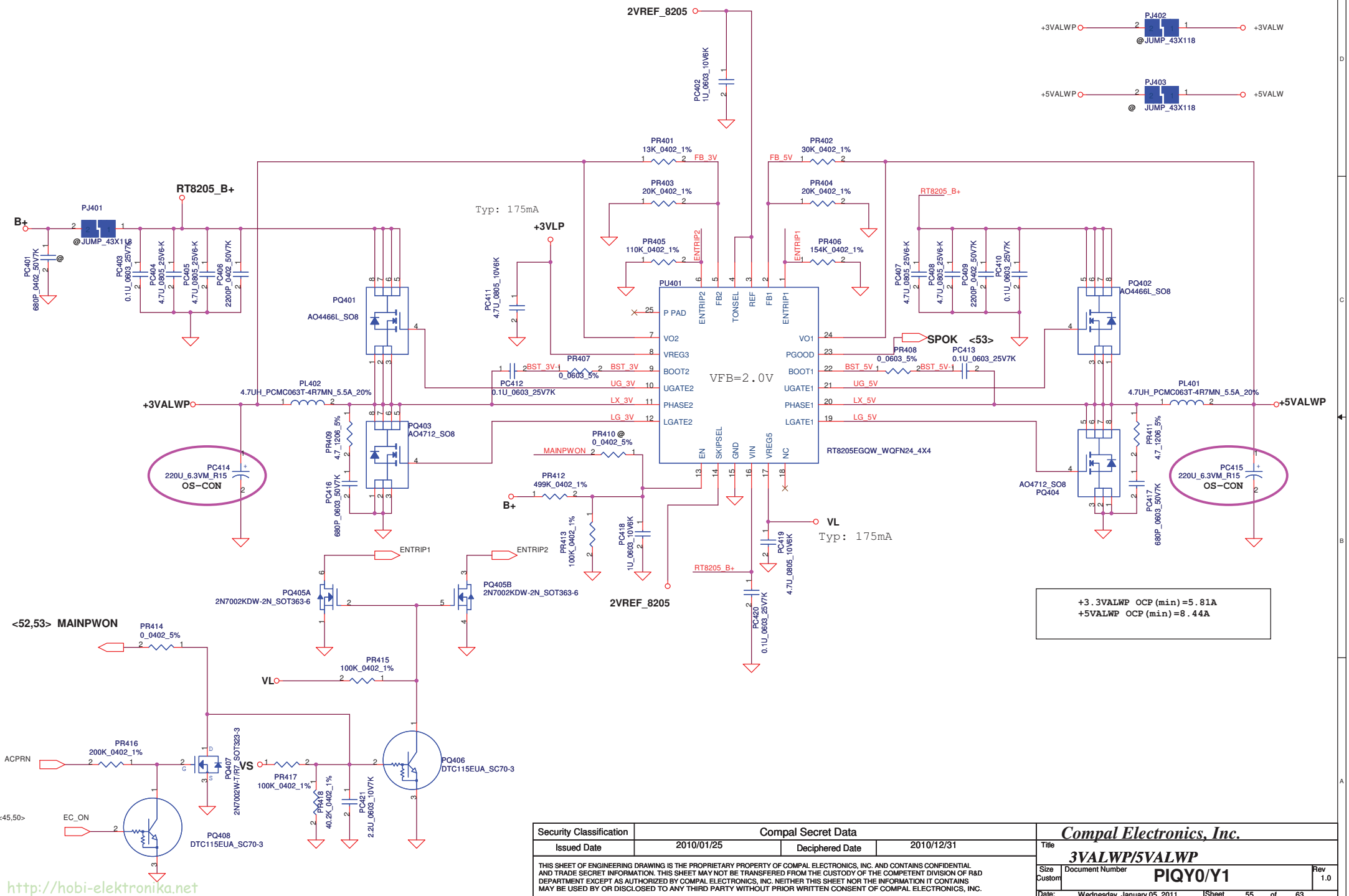
Title: CHARGER

Size	Document Number	Rev
	PIQY0/Y1	1.0

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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



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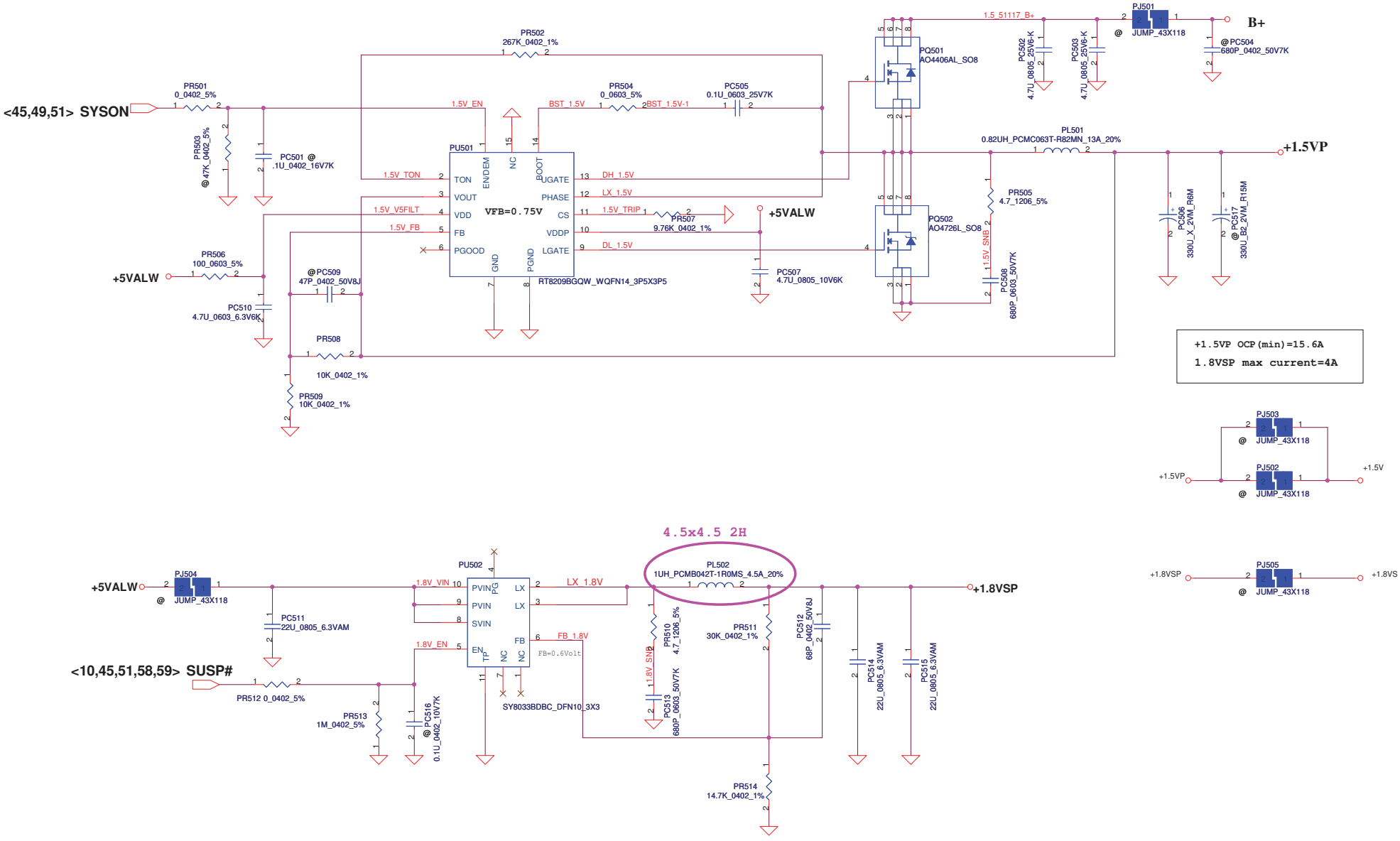
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	PIQY0/Y1	1.0

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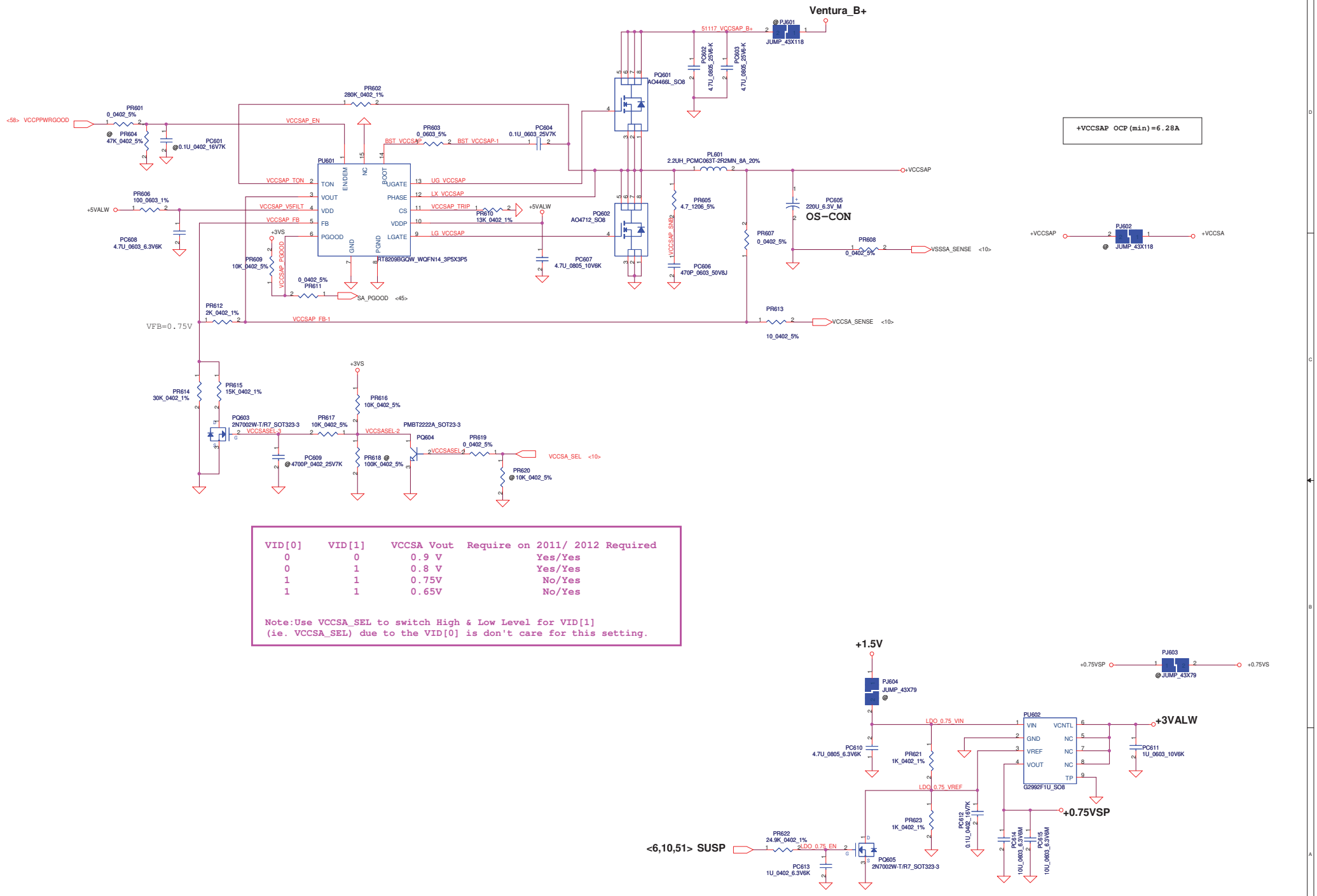
Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: PIQY0/Y1 | Rev: 1.0

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VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

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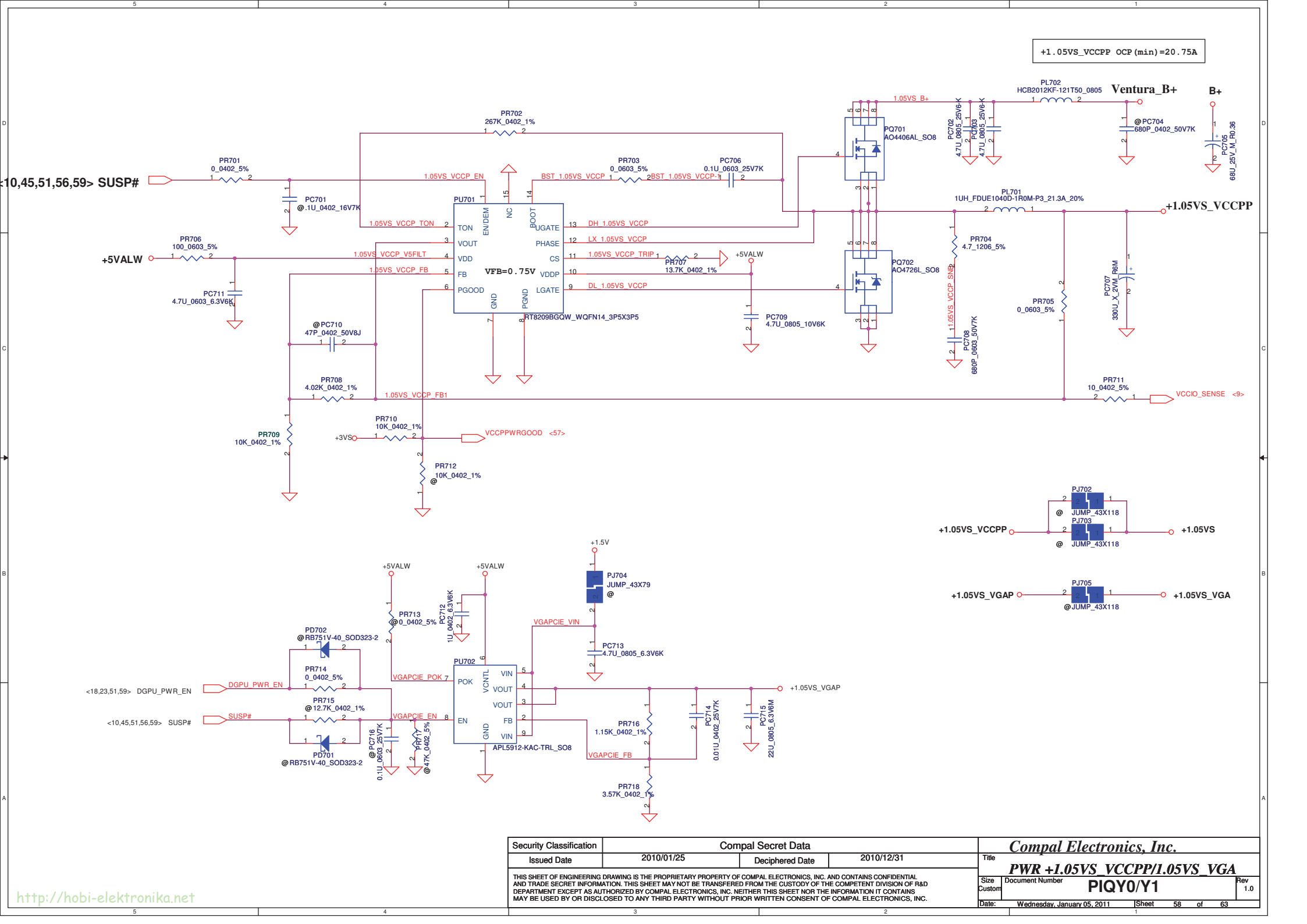
Compal Electronics, Inc.

Title: PWR +VCCSAP/+0.75VSP

Size: C | Document Number: PIQY0/Y1 | Rev: 1.0

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Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/1.05VS_VGA

Size: Custom | Document Number: PIQY0/Y1 | Rev: 1.0

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GS: PR840,PR845,PR847,PR853
GT/GT1:PR843,PR844.PR846,PR854

N12P-GS

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.0V
0	1	0.975V
1	1	0.825V

N12P-GT/GT1

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.075V
0	1	0.925V
1	1	0.825V

PU801 ISL6264CRZ-T_QFN40_6X6

PQ801 PQ802 PQ803 PQ804 TPCA8030-H_SOP-ADV8-5 / TPCA8028-H_SOP-ADVANCE8-5

PL801 HCB4532KF-800T90_1812

PL802 PL803 0.42UH_FDUE0640-R42M_20.2A_20%~D

7X7 4H_DCR=1.48mohm

B value=4300K

PH801 10K_0603_5%_TSM1A103J4302RE

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Compal Electronics, Inc.

Title: Power-VGA_CORE

Size: Custom | Document Number: PIQY0/Y1 | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 59 of 63

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

PR936
QC:19.1K
DC:19.6K

change from 43P to 47P
for shortage problem
2010-03-15

QC: PC935
DC: PC933

PR956
QC:3.724K
DC:2.15K

PR959
QC:1.54K=120A
DC:887=70A

PR943
0 ohm =>98A (Vboot=0v)
590 ohm=>91A (Vboot=0v)

B value=4700K

B value=4700K

B value=4250K

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71+5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

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Compal Electronics, Inc.			
Title	PWR +CPU_CORE/+VGFX_CORE		
Size: Custom	Document Number: PIQY0/Y1		Rev: 1.0
Date: Wednesday, January 05, 2011		Sheet 60 of 63	

Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2009/01/06

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Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: PIQY0/Y1 | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 61 of 63

PIQY0 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT
1		P18	Reserve R297	Reserve pull down for PCH GPIO53.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit Delete U55,C908,R1233,R1235,R1236,1238,R1230,R1231,Q121	Change KB light control from PWM to on/off.
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GPIO1.
6		P49	Stuff R1068, reserve R1326, Q130	Reserve USB3.0 power swicth control inverter circuit.
~~7~~		~~P48~~	~~Add R1327~~	~~For CHG_ON# pull down.~~
8		P45	Stuff R996,R139,C815, unstuff R1000,C732,C733,Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P34	Modify JLVDS1	Modify connector from 40pin to 30pin.
11		P09	Add C922	Add C922 to place at CPU sdie.
12		P21	Add R1330	Add for INTVREN control
13		P41	Modify C639	Modify type from 0805 to 0603
14		P45	Modify TP_LED#, PCH_DPWROK and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GPIO12.
15		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
16		P48		Remove USB charger function
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C924, C925 0.033u	For 100Hz High Pass filter
19		P14	Add one more SPI-ROM circuit	For dual BIOS function
20		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
21		P14	Add Q134, R1345, R1346	Add for Fast boot SPI ROM selection by EC.
22		P34	Add R1341, C926	Added for EMI request
23		P37, P44	Add R1342,R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1344	Added for VENTURA detection.
				DVT TO PVT
1		P10	Add R1347, Change R56 to 20K,	Modify S3 1.5V reduction sequence.
2		P45	Add Q135	Modify PROCHOT control circuit.
			Modify R980 link to +5VALW	Change USB_ON PU power rail
				PVT TO SVT
1		P23,P45	FAST_BOOT#	Link FAST_BOOT# to VGA GPIO12
2		P50	Add C929	EMI Request
2		P14	Add R1348	INTEL Design Guide update

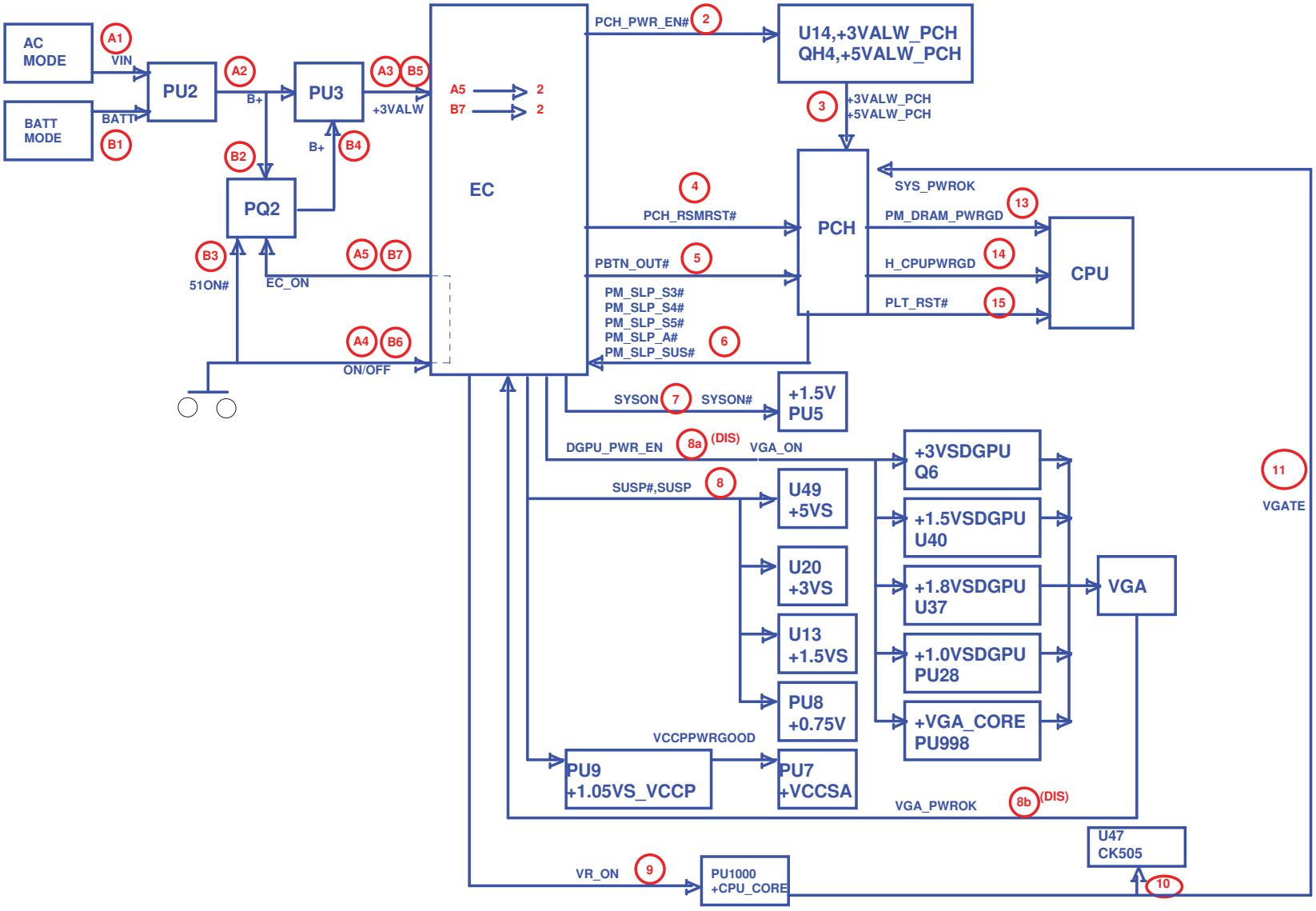
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Title	PIR (HW)	
Size: Custom	Document Number: LA-6882P	Rev: 1.0
Date: Wednesday, January 05, 2011	Sheet 62 of 63	



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Compal Electronics, Inc.

Title: Power sequence

Size	Document Number	Rev
Custom	PIQY0 LA6881P	1.0

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