PWWAA

LC Marseille

LA-6842P REV 0.2 Schematic

Intel Processor(ARD) /PCH(HM55)

2010-07-22 Rev 0.2

Security Classification	Compal Secret Data		
Issued Date	2010/06/21	Deciphered Date	2011/06/21

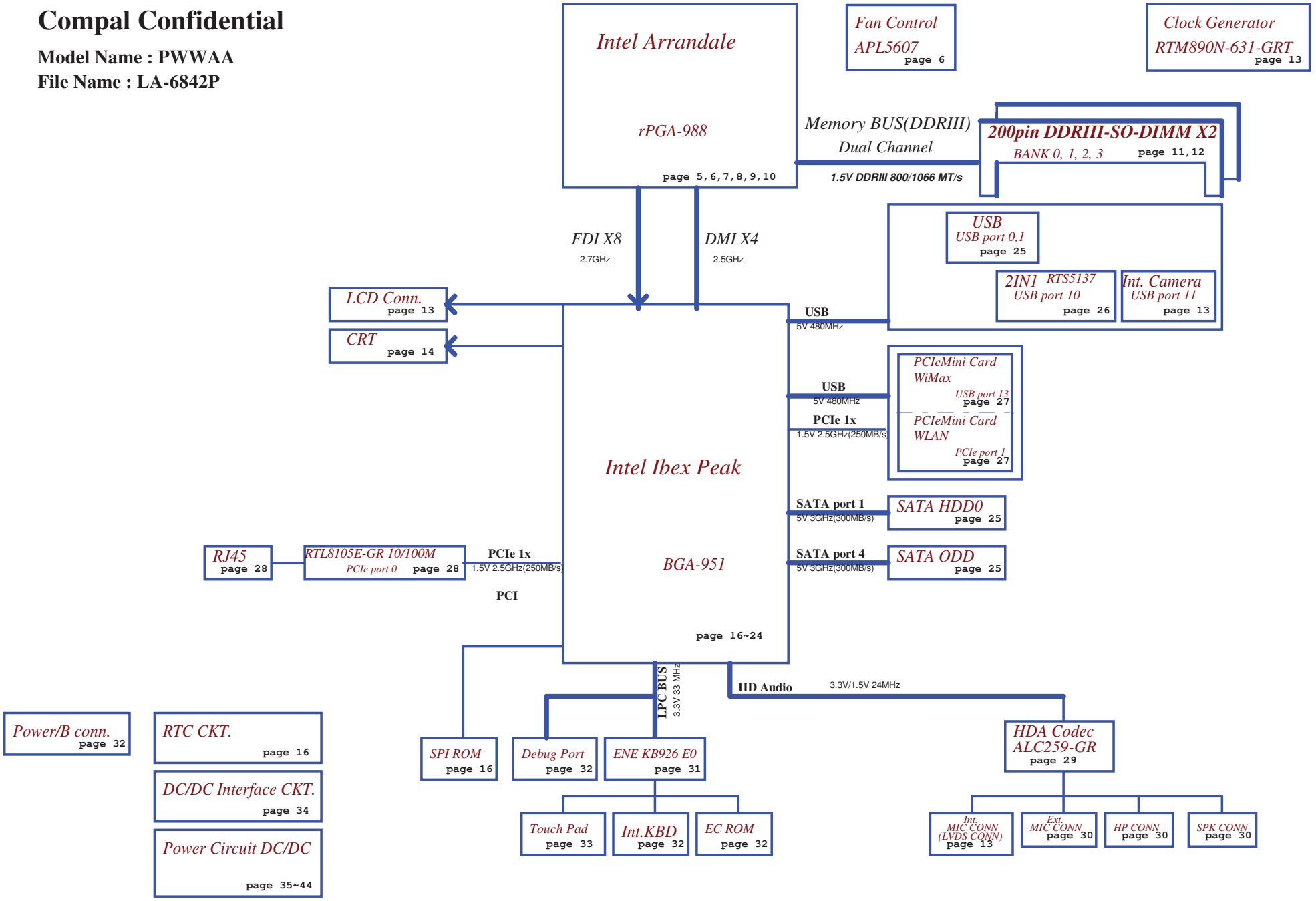
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Date: Wednesday, July 28, 2010	Sheet 1 of 45	

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Model Name : PWWAA
File Name : LA-6842P

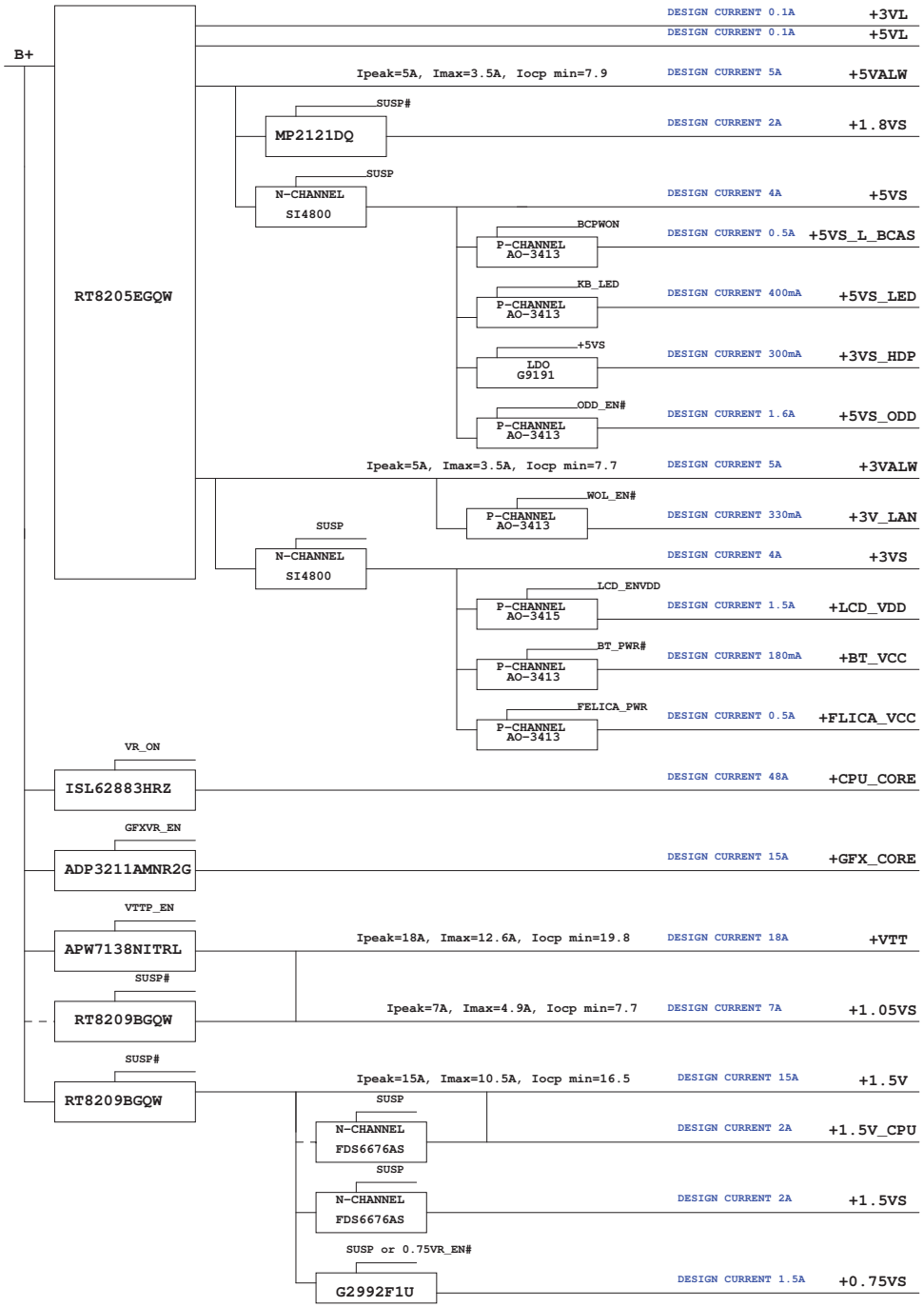


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Size	Document Number		Rev
	PWWAA LA6842P M/B		0.2
Date: Wednesday, July 28, 2010	Sheet 2 of 45		



Security Classification	Compal Secret Data		
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Size	Document Number	Rev
C	DWWA1 LA-6842P ME	0.2

Date: Wednesday, July 28, 2010 | Sheet 3 of 45

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	MINI PCI-E SLOT			LAN					
description			SLOT1	LAN					
explain			WLAN/BT	10/100M					
BTO									

Function				Camera & Mic			
description				Camera & Mic			
explain				Camera & Mic			
BTO				CAM@			

Function	S3 Power Saving		
description	S3 Power Saving		
explain		Power Saving	
BTO			

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

Power	Device	HEX	Address

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

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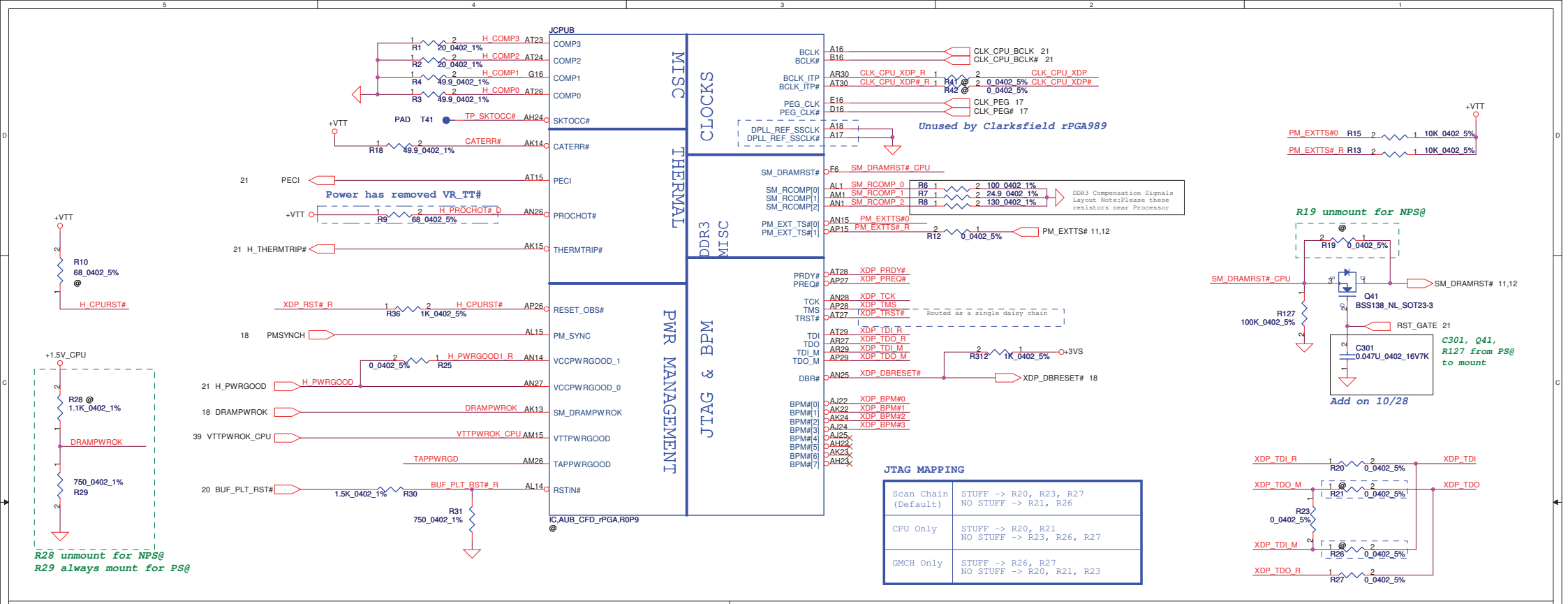
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Title: Notes List

Size: Custom | Document Number: PWWAA LA6842P M/B | Rev: 0.2

Date: Wednesday, July 28, 2010 | Sheet 4 of 45

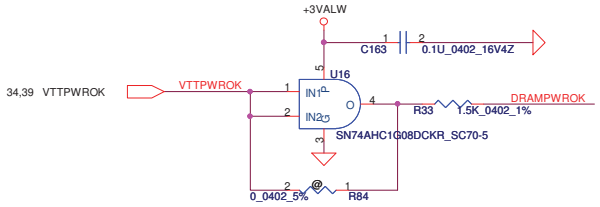


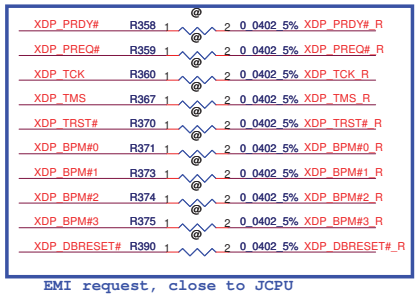
For S3 CPU Power Saving

place near JCPU

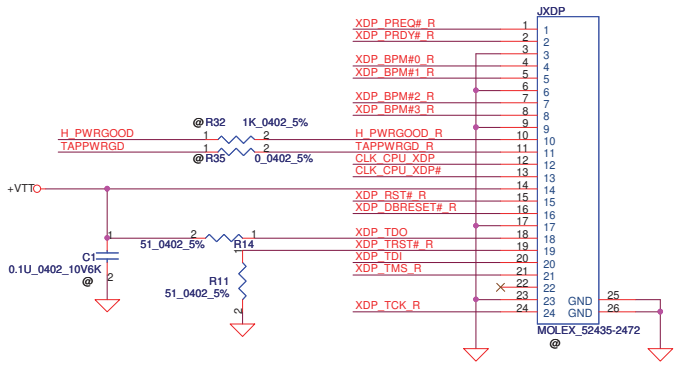
1000P_0402_50V7K C487 DRAMPWROK
1000P_0402_50V7K C488 VTTPWROK_CPU

0715 --> change BOM structure to mount





EMI request, close to JCPU



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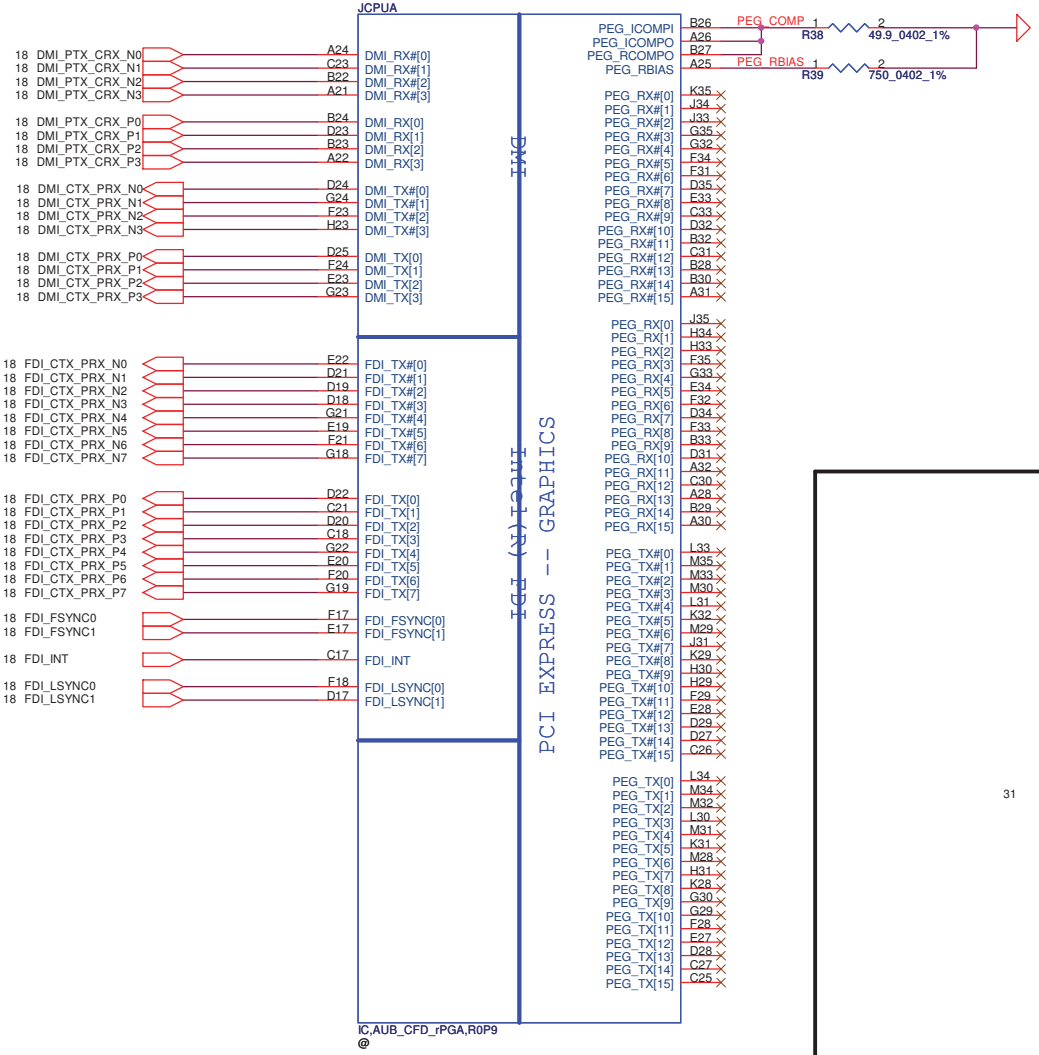
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Title: CPU CLK/MISC/JTAG

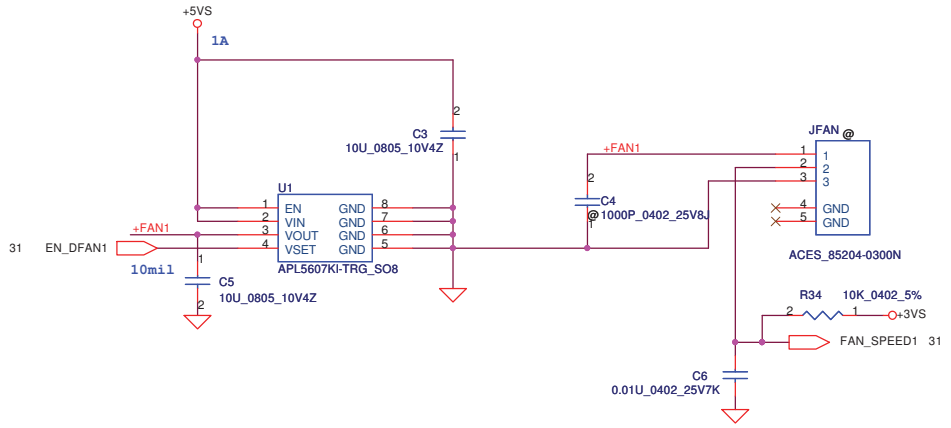
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Custom	PWWAA LA6842P M/B	0.2

Date: Wednesday, July 28, 2010 Sheet 5 of 45

http://laptop-motherboard-schematic.blogspot.com/



FAN Control Circuit



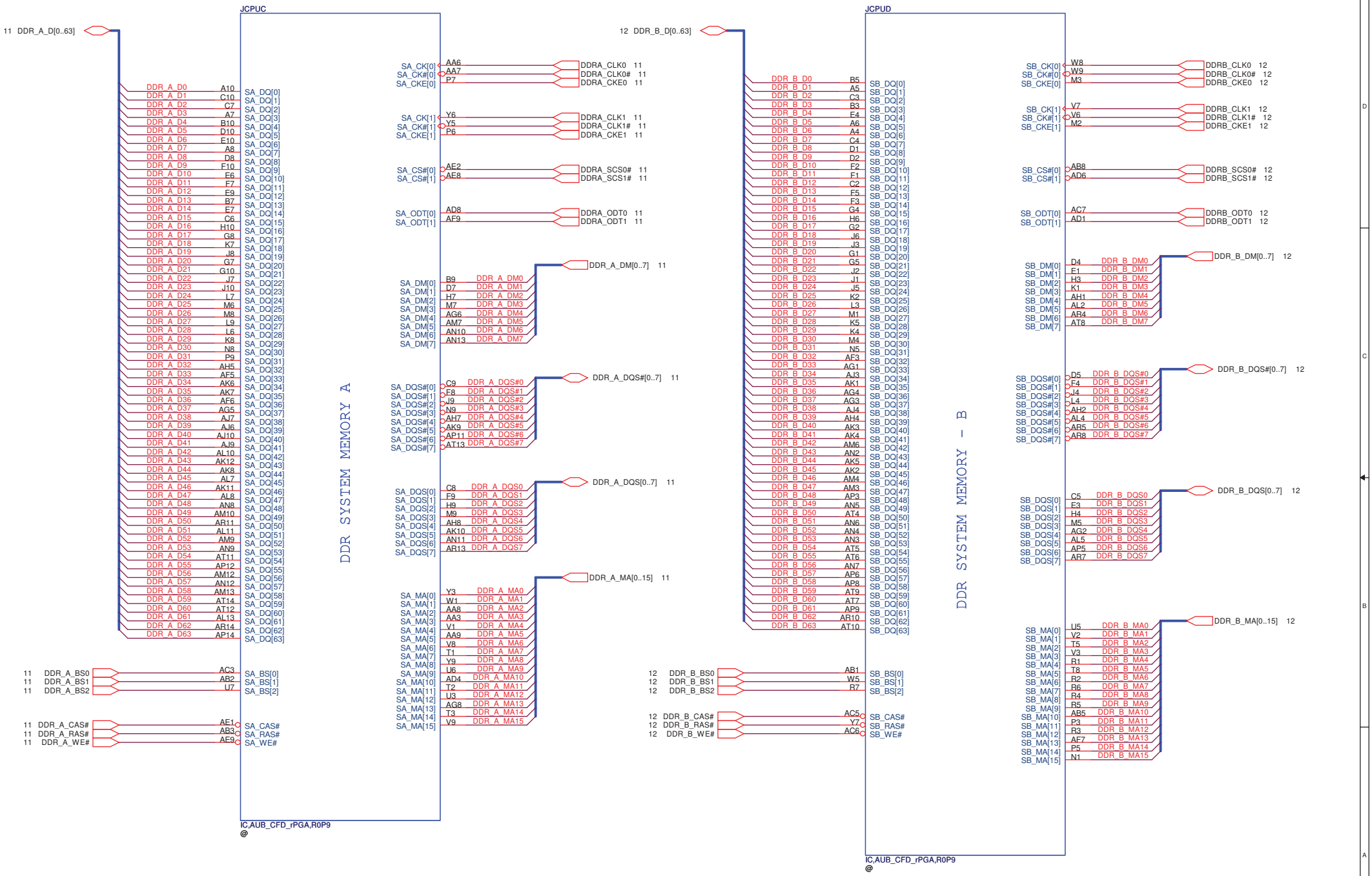
Remove Cap, for EMI

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Compal Electronics, Inc.			
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Size: B	Document Number: PWWAA LA6842P M/B		Rev: 0.2
Date: Wednesday, July 28, 2010	Sheet 6 of 45		

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Issued Date	2010/06/21	Deciphered Date	2011/06/21

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Title: CPU DDRIII

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Date: Wednesday, July 28, 2010 Sheet 7 of 45

http://laptop-motherboard-schematic.blogspot.com/

Material Note (+VTT):
390uF/ 10mohm, number are 3,
power x1, HW x2

JCPUF

+CPU_CORE

Clarksfield: 65A
Auburndale:48A

Clarksfield: 21A
Auburndale:18A

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

1.1V RAIL POWER

CPU CORE SUPPLY

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

(Place these capacitors under CPU socket Edge, top layer)

+VTT

C144 390U_2.5V_M_R10
C267 390U_2.5V_M_R10

C89 22U_0805_6.3V6M
C91 22U_0805_6.3V6M

C81 C83 C85 C87 C88 C90 C92 C94 10U_0805_10V4K

SF000002O00
ESR 10m-ohm
H6.3

Power team request for F-Din

+CPU_CORE

C114 C179 C131 C116 C132 C129 C149 22U_0805_6.3V6M

POWER

CPU VIDS

PSI# AN33 H_PSI# 42

VID[0] AK35 CPU_VID0 42
VID[1] AK33 CPU_VID1 42
VID[2] AK34 CPU_VID2 42
VID[3] AL35 CPU_VID3 42
VID[4] AL33 CPU_VID4 42
VID[5] AM33 CPU_VID5 42
VID[6] AM35 CPU_VID6 42

PROC_DPRSLPVR AM34 H_DPRSLPVR_R R62 0_0402_5% H_DPRSLPVR 42

VTT_SELECT G15 H_VTTSELECT T3 PAD

CRB default setting:
VID[6:0]=[0100111]

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V

SENSE LINES

ISENSE AN35 IMVP_IMON 42

VCC_SENSE AJ34 VCCSENSE_R R65 0_0402_5%
VSS_SENSE AJ35 VSSSENSE_R R66 0_0402_5%

R64 100_0402_1% VCCSENSE
R67 100_0402_1% VSSSENSE

+CPU_CORE

VCCSENSE 42
VSSSENSE 42

VTT_SENSE B15 VTT_SENSE 39
VSS_SENSE_VTT A15 VSS_SENSE_VTT 39

near CPU

IC,AUB_CFD_rPGA,R0P9
@

(Place these capacitors between inductor and socket on Bottom)

+CPU_CORE

10U_0805_10V4K

C71 C72 C73 C74 C75 C76 C77 C78 C79

(Place these capacitors under CPU socket, top layer)

+CPU_CORE

C98 C99 C100 C101 C102 C103 C104 10U_0805_10V4K

(Place these capacitors on CPU cavity, Bottom Layer)

+CPU_CORE

C105 C106 C107 C108 C109 C110 22U_0805_6.3V6M

+CPU_CORE

C111 C112 C113 C130 C115 C148 22U_0805_6.3V6M

TOP side (under inductor)

+CPU_CORE

C121 C122 C123 C124 330U_D2_2.5VM_R9M

Check list:

+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF

+VTT: 4x 330uF, 7x 22uF, 8x 10uF

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Title: CPU POWER-1

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Date: Wednesday, July 28, 2010 | Sheet 8 of 45

http://laptop-motherboard-schematic.blogspot.com/

For EMI request

+GFX_CORE
47P_0402_50V8J
C97 @
C118 @
C119 @
C93 @
47P_0402_50V8J
47P_0402_50V8J

+1.5V_CPU
PJ32 @
+1.5VS
JUMP_43X79

7/22 modified for cost down.

+1.5V_CPU
3A
Q33
+1.5V
form PS@ to mount
R424
470_0805_5%
C273
10U_0805_10V4K
FDS6676AS_SO8
R418
220K_0402_5%
+VSB
Q46B
SUSP
2N7002DW-T/R7_SOT363-6
C472
0.1U_0402_25V6
R417
820K_0402_5%
Q46A
SUSP
SUSP 34,41
2N7002DW-T/R7_SOT363-6

Change C271 to 4.5mm height OS-CON at PVT

+GFX_CORE
C271
330U_2.5V_M_R17
22U_0805_6.3V6M
C95
C127
C117
C96
C120
C86
10U_0805_6.3V6M
22U_0805_6.3V6M
1U_0402_6.3V4Z
10U_0805_6.3V6M

Add C496 Co-Layout with C271

+GFX_CORE
@
C496
330U_D2_2VM_R6M
For POLY Cap.

0714 --> C271 mount,
C496 unmount

JCPUG

AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

GRAPHICS

Auburndale:22A

SENSE LINES
VAXG_SENSE
VSSAXG_SENSE
AR22 VCC_AXG_SENSE_R
AT22 VSS_AXG_SENSE_R
R365 0_0402_5%
R384 0_0402_5%
R69 100_0402_1%
+GFX_CORE
VCC_AXG_SENSE 43
VSS_AXG_SENSE 43
For Power request
R82 100_0402_1%
near CPU

GRAPHICS VIDS
GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24
GFXVR_VID_0 43
GFXVR_VID_1 43
GFXVR_VID_2 43
GFXVR_VID_3 43
GFXVR_VID_4 43
GFXVR_VID_5 43
GFXVR_VID_6 43
Change R136 to 470 ohm for GFX issue
R50 470_0402_5%

GFXVR_EN
GFX_VR_EN AR25
GFX_DPRSLPVR AT25 GFXVR_DPRSLPVR
GFX_IMON AM24 GFXVR_IMON
GFXVR_EN 43
T8 PAD
GFXVR_IMON 43
R687 1K_0402_5%

C230 C314 C205 C186 0.1U_0402_16V4Z
remove PJ30

POWER

DDR3 - 1.5V RAILS
VDDQ1 AJ1
VDDQ2 AE1
VDDQ3 AE7
VDDQ4 AE4
VDDQ5 AC1
VDDQ6 AB7
VDDQ7 AB4
VDDQ8 Y1
VDDQ9 W7
VDDQ10 W4
VDDQ11 U1
VDDQ12 T7
VDDQ13 T4
VDDQ14 P1
VDDQ15 N7
VDDQ16 N4
VDDQ17 L1
VDDQ18 H1
+1.5V_CPU
1U_0402_6.3V4Z 1U_0402_6.3V4Z 22U_0805_6.3V6M
C133 C134 C135 C136 C137 C138 C139
C216 390U_2.5V_M_R10
1U_0402_6.3V4Z 1U_0402_6.3V4Z 1U_0402_6.3V4Z 22U_0805_6.3V6M
+1.5V
PJ31 @
JUMP_43X79
PJ31 need to open for S3 CPU Power Saving

Clarksfield: 5A
Auburndale:3A

FDI
+VTT
C141 C142
22U_0805_6.3V6M 22U_0805_6.3V6M
J24 J23 H25
VTT1_45 VTT1_46 VTT1_47

1.1V
VTT0_59 P10
VTT0_60 N10
VTT0_61 L10
VTT0_62 K10
+VTT
C143
10U_0805_10V4K
(Place these capacitors under CPU socket Edge, top layer)

Clarksfield: 21A
Auburndale:18A

PEG & DMI
+VTT
C146 C147
22U_0805_6.3V6M 22U_0805_6.3V6M
K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25
VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58
(Place these capacitors under CPU socket, top layer)

VTT1_63 J22
VTT1_64 J20
VTT1_65 J18
VTT1_66 H21
VTT1_67 H20
VTT1_68 H19
+VTT
C145
22U_0805_6.3V6M
(Place these capacitors under CPU socket, top layer)

1.8V
VCCPLL1 L26
VCCPLL2 L27
VCCPLL3 M26
+1.8VS_H_PLL
1U_0402_6.3V4Z 4.7U_0603_6.3V6K
+1.8VS
R71 0_0805_5%
C151 C152 C153 C154 C155
1U_0402_6.3V4Z 22U_0805_6.3V6M
2.2U_0603_6.3V4Z

Clarksfield: 0.6A
Auburndale:1.35A

IC,AUB_CFD_rPGA,R0P9
@

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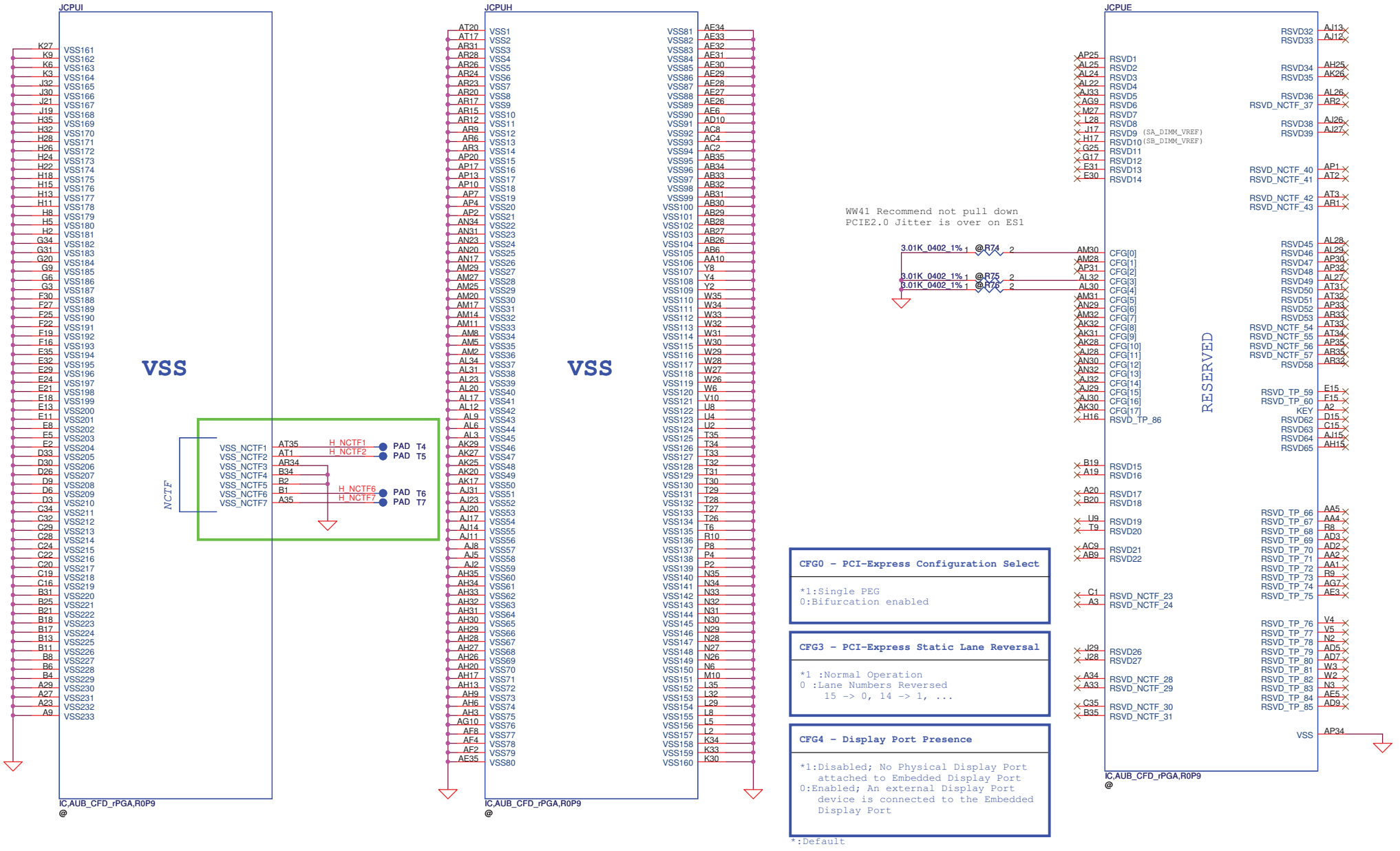
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Title: CPU POWER-2

Size	Document Number	Rev
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Date: Wednesday, July 28, 2010 Sheet 9 of 45

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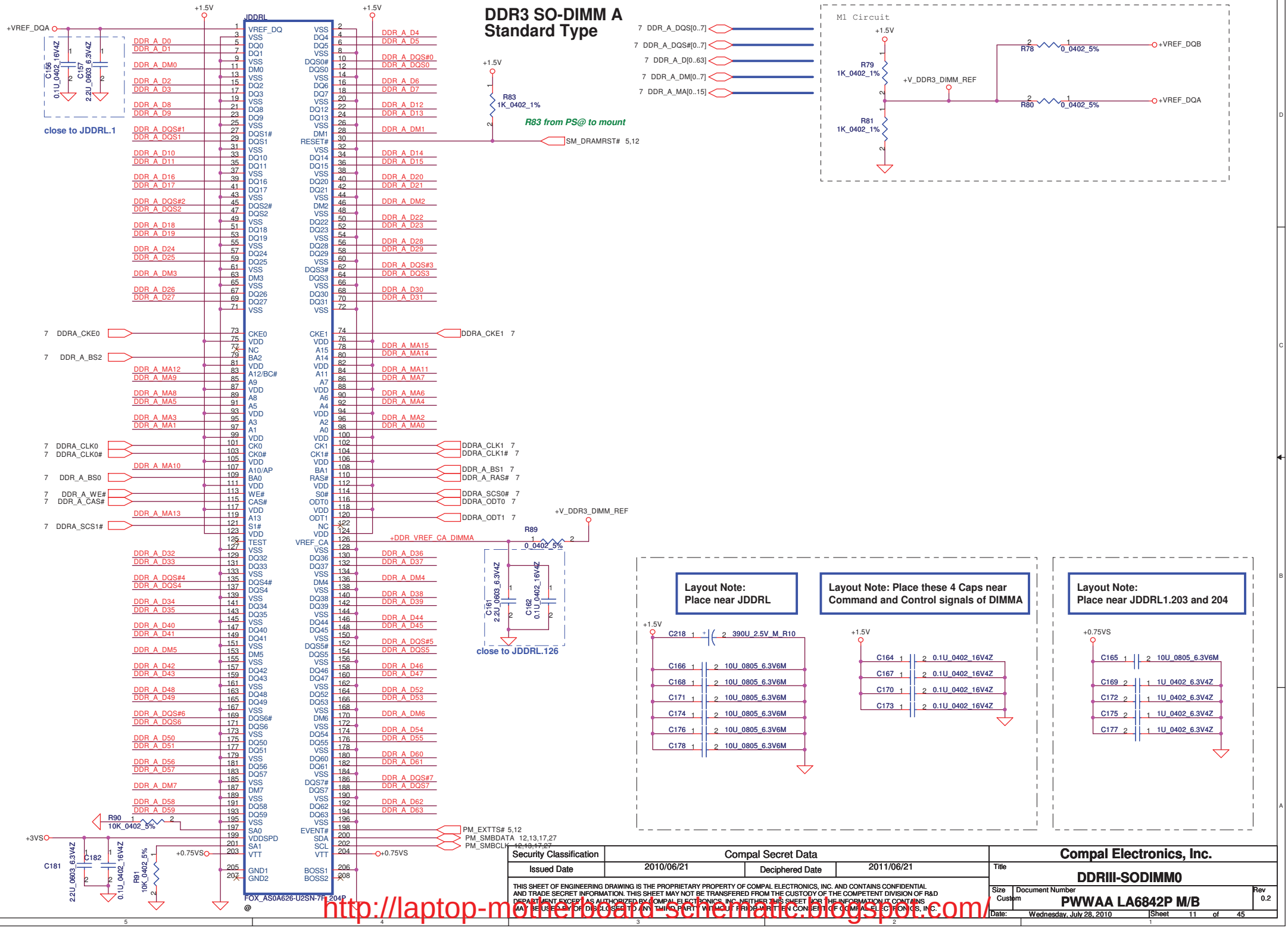
Security Classification	Compal Secret Data		
Issued Date	2010/06/21	Deciphered Date	2011/06/21

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Title	CPU GND/RESERVED/XDP		
Size: Custom	Document Number: PWWAA LA6842P M/B		Rev: 0.2
Date: Wednesday, July 28, 2010	Sheet 10 of 45		

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DDR3 SO-DIMM A
Standard Type



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Title: **DDRIII-SODIMM0**

Size	Document Number	Rev
Custom	PWWAA LA6842P M/B	0.2

Date: Wednesday, July 28, 2010 | Sheet 11 of 45

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Standard Type
DDR3 SO-DIMM B

7 DDR_B_DQS#[0..7]
7 DDR_B_DQS[0..7]
7 DDR_B_D[0..63]
7 DDR_B_DM[0..7]
7 DDR_B_MA[0..15]

JDDRH

+VREF_DQB	1	VREF_DQ	
DDR_B_D0	3	VSS	
DDR_B_D1	5	DQ0	
	7	DQ1	
DDR_B_DM0	9	VSS	
	11	DM0	
DDR_B_D2	13	VSS	
DDR_B_D3	15	DQ2	
	17	DQ3	
DDR_B_D8	19	VSS	
DDR_B_D9	21	DQ8	
	23	DQ9	
DDR_B_DQS#1	25	VSS	
DDR_B_DQS1	27	DQS1#	
	29	DQS1	
DDR_B_D10	31	VSS	
DDR_B_D11	33	DQ10	
	35	DQ11	
DDR_B_D16	37	VSS	
DDR_B_D17	39	DQ16	
	41	DQ17	
DDR_B_DQS#2	43	VSS	
DDR_B_DQS2	45	DQS2#	
	47	DQS2	
DDR_B_D18	49	VSS	
DDR_B_D19	51	DQ18	
	53	DQ19	
DDR_B_D24	55	VSS	
DDR_B_D25	57	DQ24	
	59	DQ25	
DDR_B_DM3	61	VSS	
	63	DM3	
DDR_B_D26	65	VSS	
DDR_B_D27	67	DQ26	
	69	DQ27	
	71	VSS	
7 DDRB_CKE0	73	CKE0	
	75	VDD	
	77	NC	
7 DDR_B_BS2	79	BA2	
	81	VDD	
DDR_B_MA12	83	A12/BC#	
DDR_B_MA9	85	A9	
	87	VDD	
DDR_B_MA8	89	A8	
DDR_B_MA5	91	A5	
	93	VDD	
DDR_B_MA3	95	A3	
DDR_B_MA1	97	A1	
	99	VDD	
7 DDRB_CLK0	101	CK0	
7 DDRB_CLK0#	103	CK0#	
	105	VDD	
DDR_B_MA10	107	A10/AP	
7 DDR_B_BS0	109	BA0	
	111	VDD	
7 DDR_B_WE#	113	WE#	
7 DDR_B_CAS#	115	CAS#	
	117	VDD	
DDR_B_MA13	119	A13	
7 DDRB_SCS1#	121	S1#	
	123	VDD	
	125	TEST	
	127	VSS	
DDR_B_D32	129	DQ32	
DDR_B_D33	131	DQ33	
	133	VSS	
DDR_B_DQS#4	135	DQS4#	
DDR_B_DQS4	137	DQS4	
	139	VSS	
DDR_B_D34	141	DQ34	
DDR_B_D35	143	DQ35	
	145	VSS	
DDR_B_D40	147	DQ40	
DDR_B_D41	149	DQ41	
	151	VSS	
DDR_B_DM5	153	DM5	
	155	VSS	
DDR_B_D42	157	DQ42	
DDR_B_D43	159	DQ43	
	161	VSS	
DDR_B_D48	163	DQ48	
DDR_B_D49	165	DQ49	
	167	VSS	
DDR_B_DQS#6	169	DQS6#	
DDR_B_DQS6	171	DQS6	
	173	VSS	
DDR_B_D50	175	DQ50	
DDR_B_D51	177	DQ51	
	179	VSS	
DDR_B_D56	181	DQ56	
DDR_B_D57	183	DQ57	
	185	VSS	
DDR_B_DM7	187	DM7	
	189	VSS	
DDR_B_D58	191	DQ58	
DDR_B_D59	193	DQ59	
	195	VSS	
	197	SA0	
	199	VDDSPD	
	201	SA1	
	203	VTT	
	205	GND1	
	207	GND2	

	2	VSS	
DDR_B_D4	4	DQ4	
DDR_B_D5	6	DQ5	
	8	VSS	
DDR_B_DQS#0	10	DQS0#	
DDR_B_DQS0	12	DQS0	
	14	VSS	
DDR_B_D6	16	DQ6	
DDR_B_D7	18	DQ7	
	20	VSS	
DDR_B_D12	22	DQ12	
DDR_B_D13	24	DQ13	
	26	VSS	
DDR_B_DM1	28	DM1	
SM_DRAMRST# 5,11	30	RESET#	
	32	VSS	
DDR_B_D14	34	DQ14	
DDR_B_D15	36	DQ15	
	38	VSS	
DDR_B_D20	40	DQ20	
DDR_B_D21	42	DQ21	
	44	VSS	
DDR_B_DM2	46	DM2	
	48	VSS	
DDR_B_D22	50	DQ22	
DDR_B_D23	52	DQ23	
	54	VSS	
DDR_B_D28	56	DQ28	
DDR_B_D29	58	DQ29	
	60	VSS	
DDR_B_DQS#3	62	DQS3#	
DDR_B_DQS3	64	DQS3	
	66	VSS	
DDR_B_D30	68	DQ30	
DDR_B_D31	70	DQ31	
	72	VSS	
DDRB_CKE1 7	74	CKE1	
	76	VDD	
DDR_B_MA15	78	A15	
DDR_B_MA14	80	A14	
	82	VDD	
DDR_B_MA11	84	A11	
DDR_B_MA7	86	A7	
	88	VDD	
DDR_B_MA6	90	A6	
DDR_B_MA4	92	A4	
	94	VDD	
DDR_B_MA2	96	A2	
DDR_B_MA0	98	A0	
	100	VDD	
DDRB_CLK1 7	102	CK1	
DDRB_CLK1# 7	104	CK1#	
	106	VDD	
DDR_B_BS1 7	108	BA1	
DDR_B_RAS# 7	110	RAS#	
	112	VDD	
DDRB_SCS0# 7	114	S0#	
DDRB_ODT0 7	116	ODT0	
	118	VDD	
DDRB_ODT1 7	120	ODT1	
	122	NC	
	124	VDD	
+DDR_VREF_CA_DIMMB	126	VREF_CA	
	128	VSS	
DDR_B_D36	130	DQ36	
DDR_B_D37	132	DQ37	
	134	VSS	
DDR_B_DM4	136	DM4	
	138	VSS	
DDR_B_D38	140	DQ38	
DDR_B_D39	142	DQ39	
	144	VSS	
DDR_B_D44	146	DQ44	
DDR_B_D45	148	DQ45	
	150	VSS	
DDR_B_DQS#5	152	DQS5#	
DDR_B_DQS5	154	DQS5	
	156	VSS	
DDR_B_D46	158	DQ46	
DDR_B_D47	160	DQ47	
	162	VSS	
DDR_B_D52	164	DQ52	
DDR_B_D53	166	DQ53	
	168	VSS	
DDR_B_DM6	170	DM6	
	172	VSS	
DDR_B_D54	174	DQ54	
DDR_B_D55	176	DQ55	
	178	VSS	
DDR_B_D60	180	DQ60	
DDR_B_D61	182	DQ61	
	184	VSS	
DDR_B_DQS#7	186	DQS7#	
DDR_B_DQS7	188	DQS7	
	190	VSS	
DDR_B_D62	192	DQ62	
DDR_B_D63	194	DQ63	
	196	VSS	
PM_EXTTS# 5,11	198	EVENT#	
PM_SMBDATA 11,13,17,27	200	SDA	
PM_SMBCLK 11,13,17,27	202	SCL	
+0.75VS	204	VTT	
	206	BOSS1	
	208	BOSS2	

FOX_AS0A626-UASN-7F 204P
@

+1.5V
+1.5V
+V_DDR3_DIMM_REF
+3VS
+0.75VS
+0.75VS

C183 2.2U_0603_6.3V4Z
C184 0.1U_0402_16V4Z
close to JDDRH.1

R97 1 2 0_0402_5%
C187 2.2U_0603_6.3V4Z
C188 0.1U_0402_16V4Z
close to JDDRH.126

R98 1 2 10K_0402_5%
R99 1 2 10K_0402_5%
2.2U_0603_6.3V4Z
C207
C208
0.1U_0402_16V4Z

Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

+1.5V
C189 @ 330U_B2_2.5VM_R15M
C192 10U_0805_6.3V6M
C194 10U_0805_6.3V6M
C197 10U_0805_6.3V6M
C200 10U_0805_6.3V6M
C202 10U_0805_6.3V6M
C204 10U_0805_6.3V6M

+1.5V
C190 0.1U_0402_16V4Z
C193 0.1U_0402_16V4Z
C196 0.1U_0402_16V4Z
C199 0.1U_0402_16V4Z

Layout Note:
Place near JDDRH.203 and 204

+0.75VS
C191 10U_0805_6.3V6M
C195 1U_0402_6.3V4Z
C198 1U_0402_6.3V4Z
C201 1U_0402_6.3V4Z
C203 1U_0402_6.3V4Z

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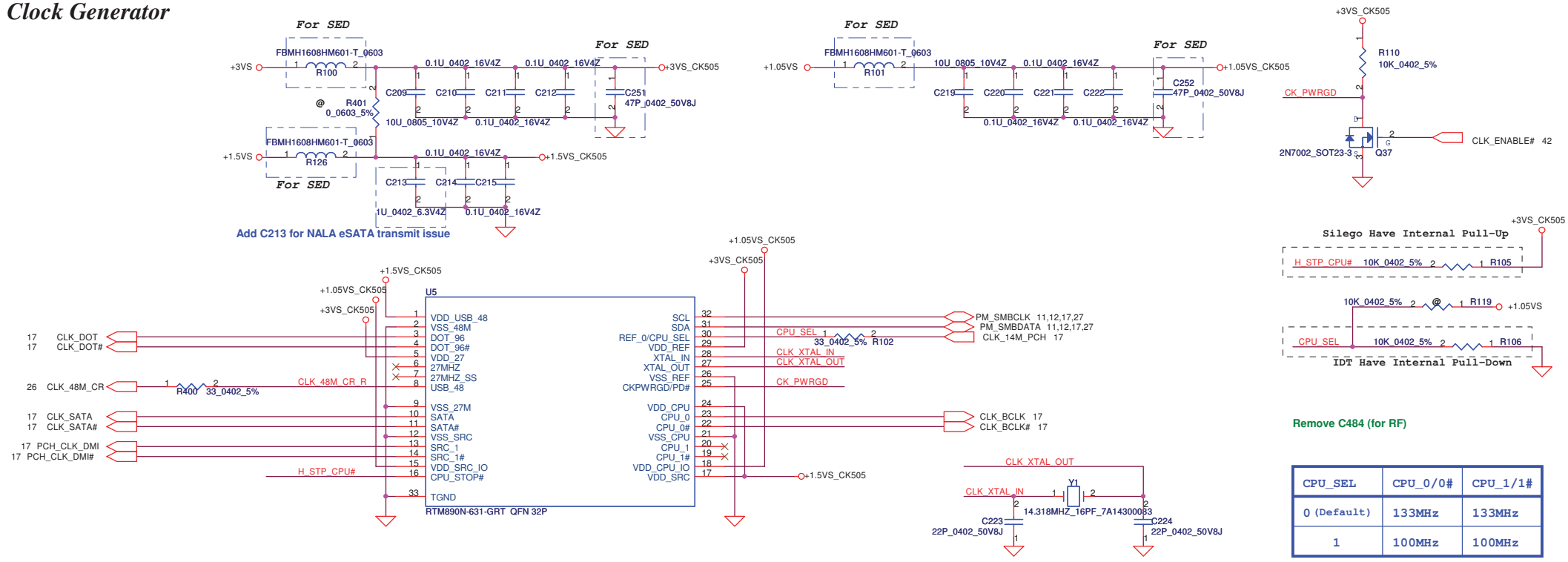
Title: **DDRIII-SODIMM1**

Size: Custom | Document Number: **PWWAA LA6842P M/B** | Rev: 0.2

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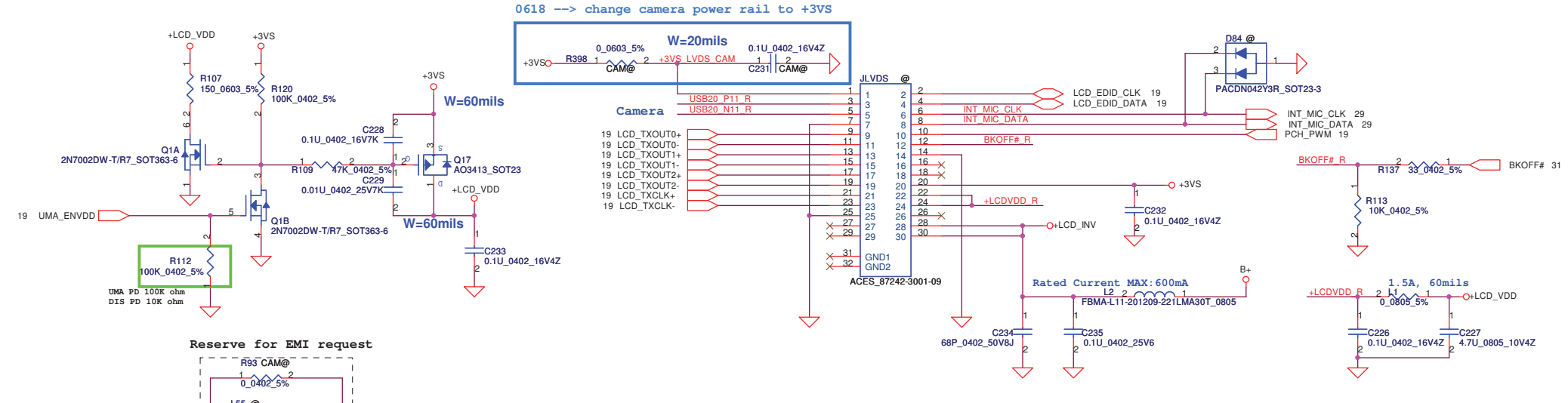
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Clock Generator



CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

LVDS / Int.Camera / Int.MIC Conn



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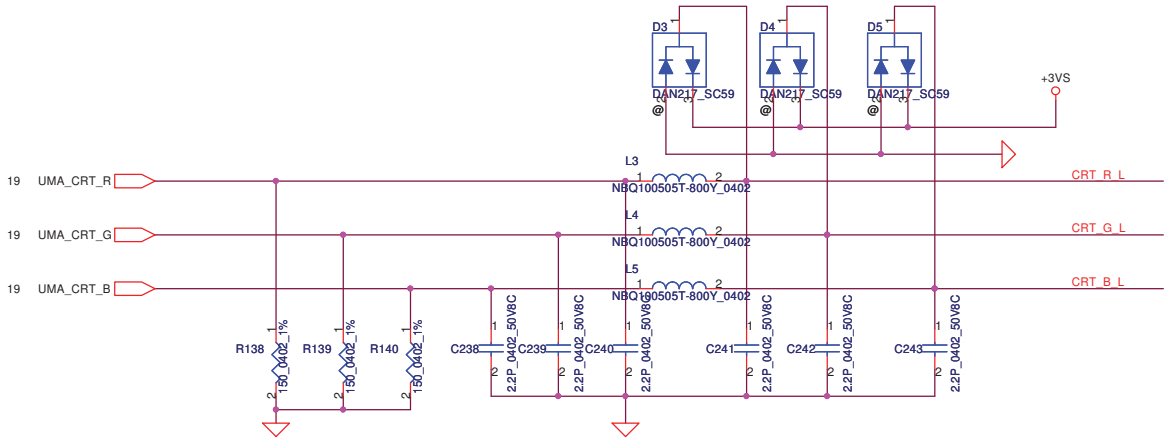
Title: Clock Generator (CK505)/ LVDS CONN

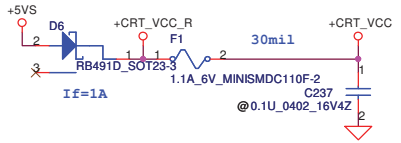
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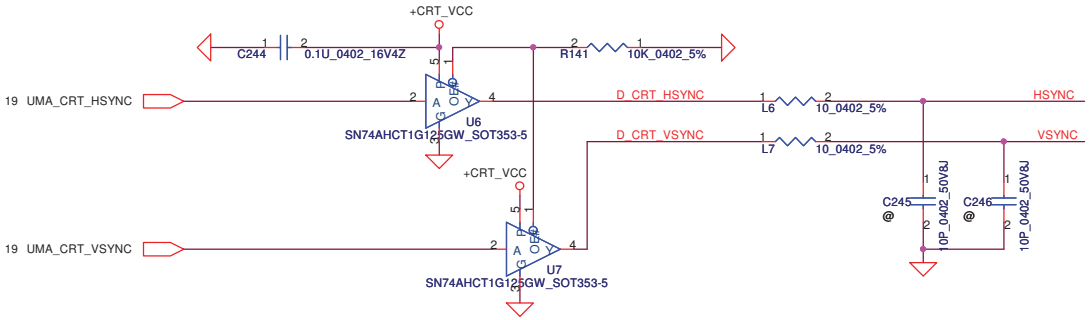
Date: Wednesday, July 28, 2010 | Sheet 13 of 45

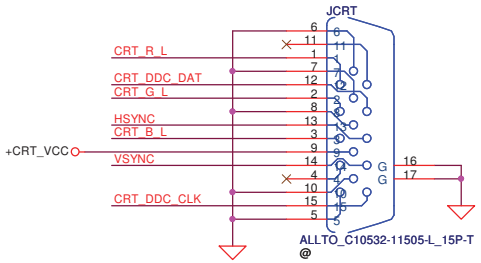
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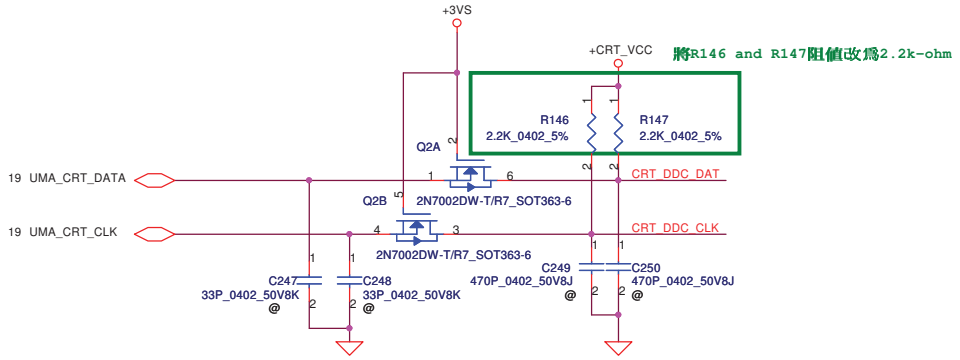
CRT CONNECTOR











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Title	CRT\TV\LVDS		
Size	Document Number	PWWAA LA6842P M/B	Rev 0.2
Date: Wednesday, July 28, 2010	Sheet 14 of 45		

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0624 --> Remove BIOS ROM Debug Circuit

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Compal Electronics, Inc.		
Title: BIOS ROM Debug		
Size	Document Number: PWWAA LA6842P M/B	Rev: 0.2
Date: Wednesday, July 28, 2010	Sheet 15 of 45	

CMOS Setting, near DDR Door

+RTCVCC — R282 20K_0402_1% — PCH_RTCRST# — JCMOS — C288 1U_0402_6.3V4Z

iME Setting.

R284 20K_0402_1% — PCH_SRTCRST# — J2 — C289 1U_0402_6.3V4Z

Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

HDA_SYNC

This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

HDA_SDO

This signal has a weak internal pull down.
This signal can't PU

Flash Descriptor Security Overide

HDA_DOCK_EN#	Low = Enabled High = Disabled *

ITPM Enabled — Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)

C287 15P_0402_50V8J — Y3 32.768KHZ_12.5PF_Q13MC14610002 — C290 15P_0402_50V8J — R283 10M_0402_5%

+RTCVCC — R285 1M_0402_5% — SM_INTRUDER# — R275 330K_0402_5% — PCH_INTVRMEN

U11A

RTC: RTCX1 (B13) — PCH_RTCX1; RTCX2 (D13) — PCH_RTCX2; RTCRST# (C14) — PCH_RTCRST#; SRTCRST# (D17) — PCH_SRTCRST#; INTRUDER# (A16) — SM_INTRUDER#; INTVRMEN (A14) — PCH_INTVRMEN

LPC: FWH0 / LAD0 (D33) — LPC_AD0 31,32; FWH1 / LAD1 (B33) — LPC_AD1 31,32; FWH2 / LAD2 (C32) — LPC_AD2 31,32; FWH3 / LAD3 (A32) — LPC_AD3 31,32; FWH4 / LFRAME# (C34) — LPC_FRAME# 31,32; LDRQ0# (A34); LDRQ1# / GPIO23 (F34) — remove FELICA_PWR#; SERIRQ (AB9) — SERIRQ 31,32 — R286 10K_0402_5% — +3VS

IHDA: HDA_BCLK (A30) — AZ_BITCLK; HDA_SYNC (D29) — AZ_SYNC; HDA_SPKR (P1) — 19,29 PCH_SPKR; HDA_RST# (C30) — AZ_RST#; HDA_SDIN0 (G30) — 29 AZ_SDIN0_HD; HDA_SDIN1 (F30); HDA_SDIN2 (E32); HDA_SDIN3 (F32); HDA_SDO (B29) — AZ_SDOUT — @R118 1K_0402_5%

remove SDN1 for MDC

SATA: HDA_DOCK_EN# / GPIO33 (H32) — 31 PWRME_CTRL#; HDA_DOCK_RST# / GPIO13 (J30)

remove CR_CPPE# for JM385

SATA0RXN (AK7) / SATA0RXP (AK6) / SATA0TXN (AK11) / SATA0TXP (AK9)

SATA1RXN (AH6) / SATA1RXP (AH5) / SATA1TXN (AH9) / SATA1TXP (AH8) — SATA_PRX_C_DTX_N1 25; SATA_PRX_C_DTX_P1 25; SATA_PTX_DRX_N1 25; SATA_PTX_DRX_P1 25

1ST HDD

SATA2RXN (AF11) / SATA2RXP (AF9) / SATA2TXN (AF7) / SATA2TXP (AF6)

SATA3RXN (AH3) / SATA3RXP (AH1) / SATA3TXN (AF3) / SATA3TXP (AF1)

Desktop Only

SATA4RXN (AD9) / SATA4RXP (AD8) / SATA4TXN (AD6) / SATA4TXP (AD5) — SATA_PRX_C_DTX_N4 25; SATA_PRX_C_DTX_P4 25; SATA_PTX_DRX_N4 25; SATA_PTX_DRX_P4 25

SATA ODD

SATA5RXN (AD3) / SATA5RXP (AD1) / SATA5TXN (AB3) / SATA5TXP (AB1)

remove eSATA SATA

SATAICOMPO (AF16); SATAICOMPI (AF15) — SATAICOMP — R295 37.4_0402_1% — +1.05VS

JTAG: JTAG_TCK (M3) — PCH_JTAG_TCK; JTAG_TMS (K3) — PCH_JTAG_TMS; JTAG_TDI (K1) — PCH_JTAG_TDI; JTAG_TDO (J2) — PCH_JTAG_TDO; TRST# (J4) — PCH_JTAG_RST#

SPI: SPI_CLK (BA2) — PCH_SPI_CLK; SPI_CS0# (AV3) — PCH_SPI_CS0#; SPI_CS1# (AY3); SPI_MOSI (AY1) — PCH_SPI_MOSI — R273 1K_0402_5% — +3VS; SPI_MISO (AV1) — PCH_SPI_MISO

SATALED# (T3) — SATA_LED#

SATA0GP / GPIO21 (Y9) — PCH_GPIO21

SATA1GP / GPIO19 (V1) — PCH_GPIO19

IBEXPEAK-M QV20 A0_FCBGA1071 — HM55R1@

RTC schematic for non-chargeable

+RTCVCC — D10 CHN202UPT SC-70 — +3VL — +RTCBATT — C291 0.1U_0402_16V4Z — @ JRTC LOTES_AAA-BAT-054-K01

29 AZ_BITCLK_HD — R288 33_0402_5% — AZ_BITCLK

29 AZ_SYNC_HD — R290 33_0402_5% — AZ_SYNC

29 AZ_RST_HD# — R292 33_0402_5% — AZ_RST#

29 AZ_SDOUT_HD — R294 33_0402_5% — AZ_SDOUT

+3VS — PCH_GPIO21 R302 10K_0402_5%; SATA_LED# R301 10K_0402_5%; PCH_GPIO19 R306 10K_0402_5%

+3VALW — @ R386 200_0402_5% — PCH_JTAG_TMS — @ R355 100_0402_5%

+3VALW — @ R363 200_0402_5% — PCH_JTAG_TDO — @ R535 100_0402_5%

+3VALW — @ R536 200_0402_5% — PCH_JTAG_TDI — @ R537 100_0402_5%

+3VALW — @ R643 20K_0402_5% — PCH_JTAG_RST# — @ R364 10K_0402_5%

R156 51_0402_5% — PCH_JTAG_TCK

06/01 change R125 from 4.7K to 51 ohm

PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable (Default) ES1	PCH JTAG Disable (Default) ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
	R353	10Kohm	10Kohm	No Install	No Install

For EMI Place near U13

PCH_SPI_CLK — R385 @ 10_0402_5% — @ C16 10P_0402_50V8J

4MB

+3VS — C293 0.1U_0402_16V4Z — U13 MX25L3205DM2I-12G SO8

PCH_SPI_CS0# — S
PCH_SPI_CLK — C
PCH_SPI_MOSI — D
PCH_SPI_MISO — Q

Security Classification	Compal Secret Data
Issued Date	2010/06/21
Deciphered Date	2011/06/21

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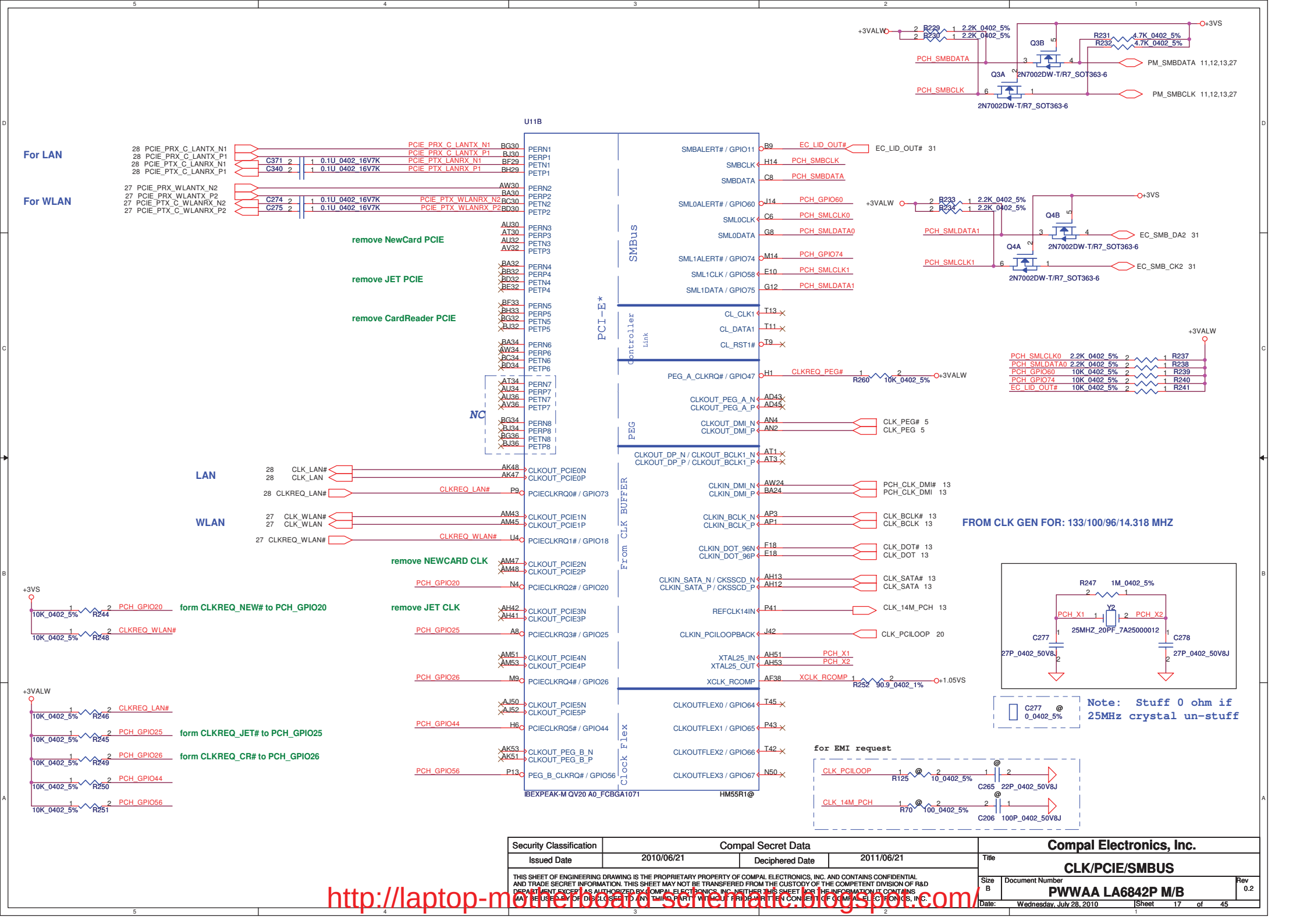
Compal Electronics, Inc.

Title: PCH-SPI/SATA/LPC/RTC/HDA

Size: B — Document Number: PWWAA LA6842P M/B — Rev: 0.2

Date: Wednesday, July 28, 2010 — Sheet 16 of 45

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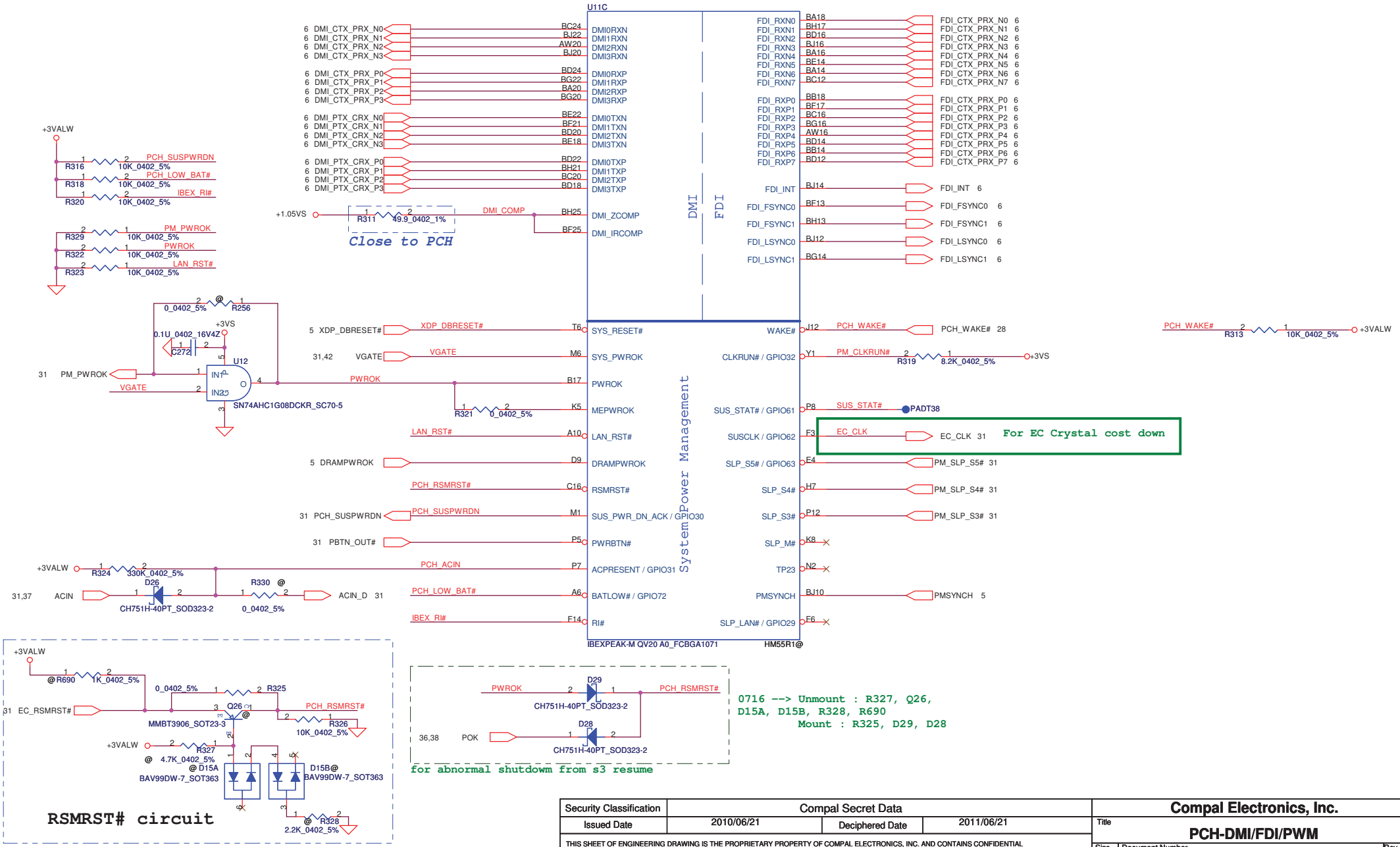
Compal Electronics, Inc.

Title: **CLK/PCIE/SMBUS**

Size	Document Number	Rev
B	PWWAA LA6842P M/B	0.2

Date: Wednesday, July 28, 2010 | Sheet 17 of 45

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Issued Date	2010/06/21	Deciphered Date	2011/06/21

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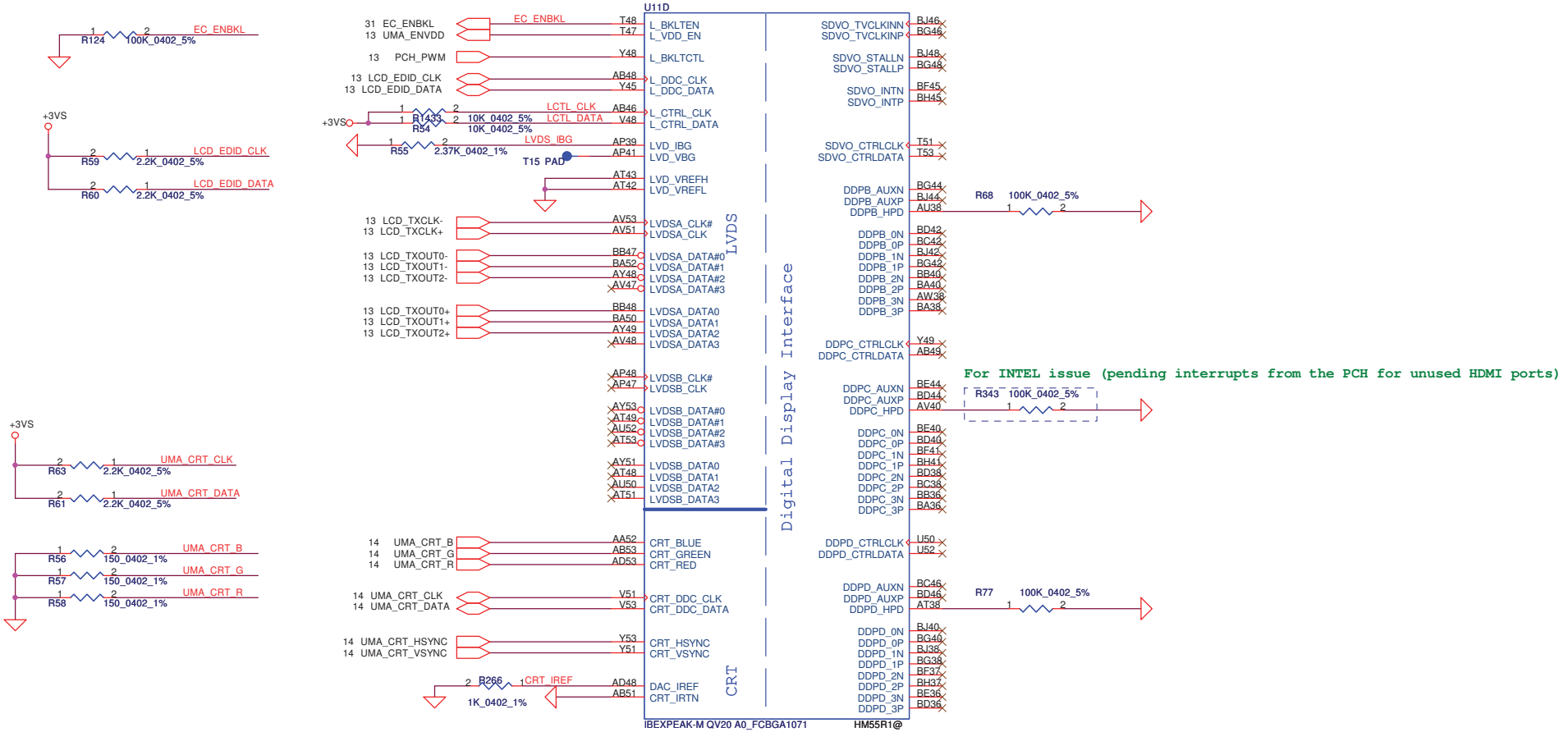
Compal Electronics, Inc.

Title: PCH-DMI/FDI/PWM

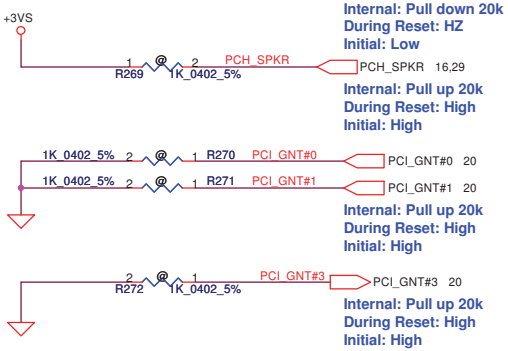
Size	Document Number	Rev
B	PWWAA LA6842P M/B	0.2

Date: Wednesday, July 28, 2010 Sheet 18 of 45

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PCH Strap Pin



Internal: Pull down 20k
During Reset: HZ
Initial: Low

Internal: Pull up 20k
During Reset: High
Initial: High

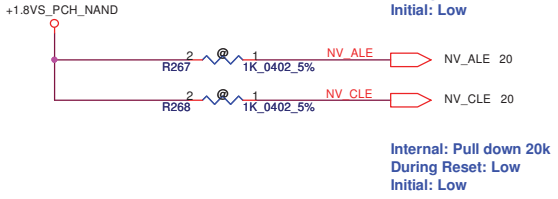
Internal: Pull up 20k
During Reset: High
Initial: High

Internal: Pull up 20k
During Reset: High
Initial: High

NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



Internal: Pull down 20k
During Reset: Low
Initial: Low

Internal: Pull down 20k
During Reset: Low
Initial: Low

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

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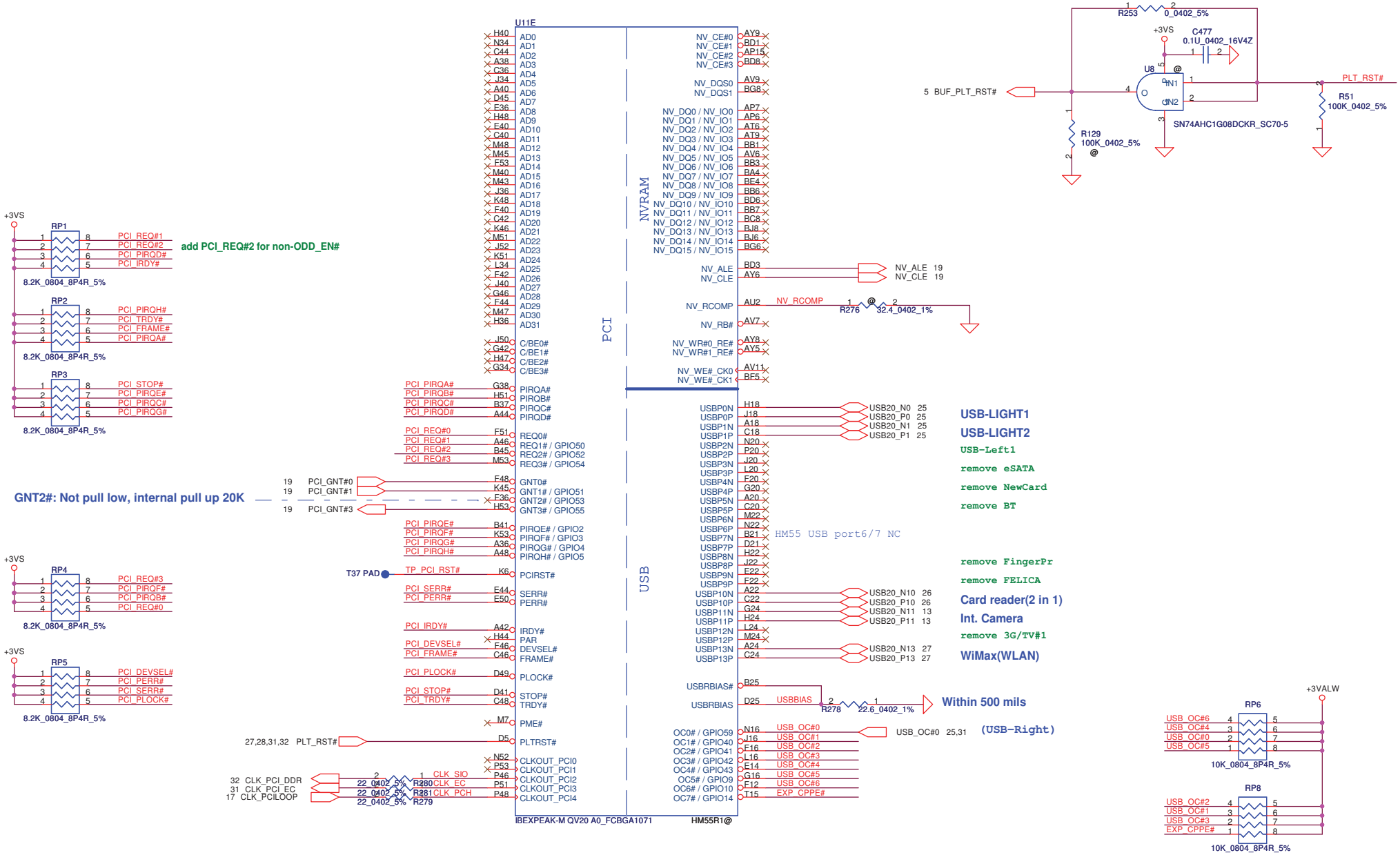
Compal Electronics, Inc.

Title: PCH-CRT/LVDS/HDMI

Size: Custom | Document Number: PWWAA LA6842P M/B | Rev: 0.2

Date: Wednesday, July 28, 2010 | Sheet 19 of 45

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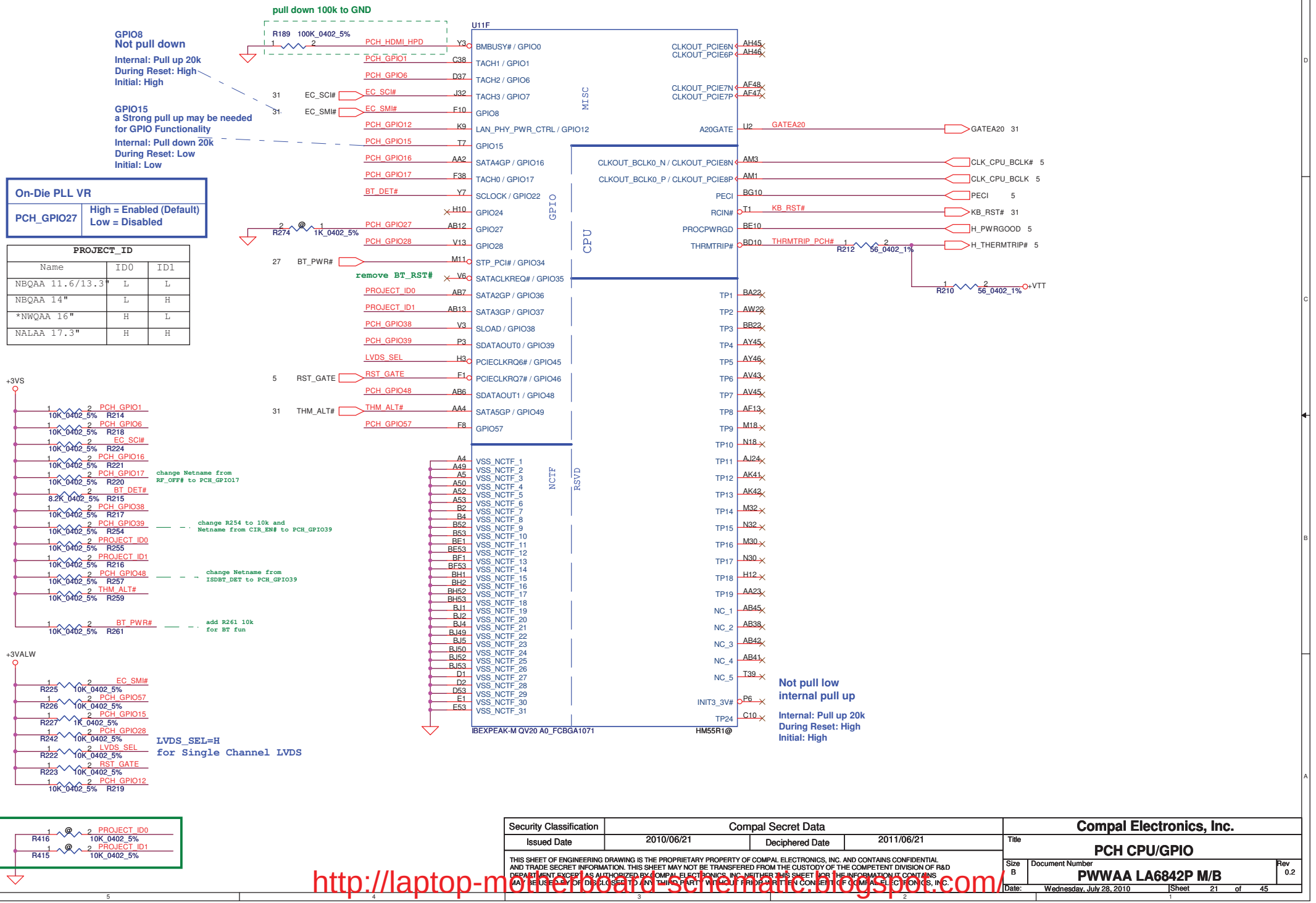
Compal Electronics, Inc.

Title: **PCH USB/PCI/NAND**

Size	Document Number	Rev
B	**PWWAA LA6842P M/B**	0.2

Date: Wednesday, July 28, 2010 | Sheet 20 of 45

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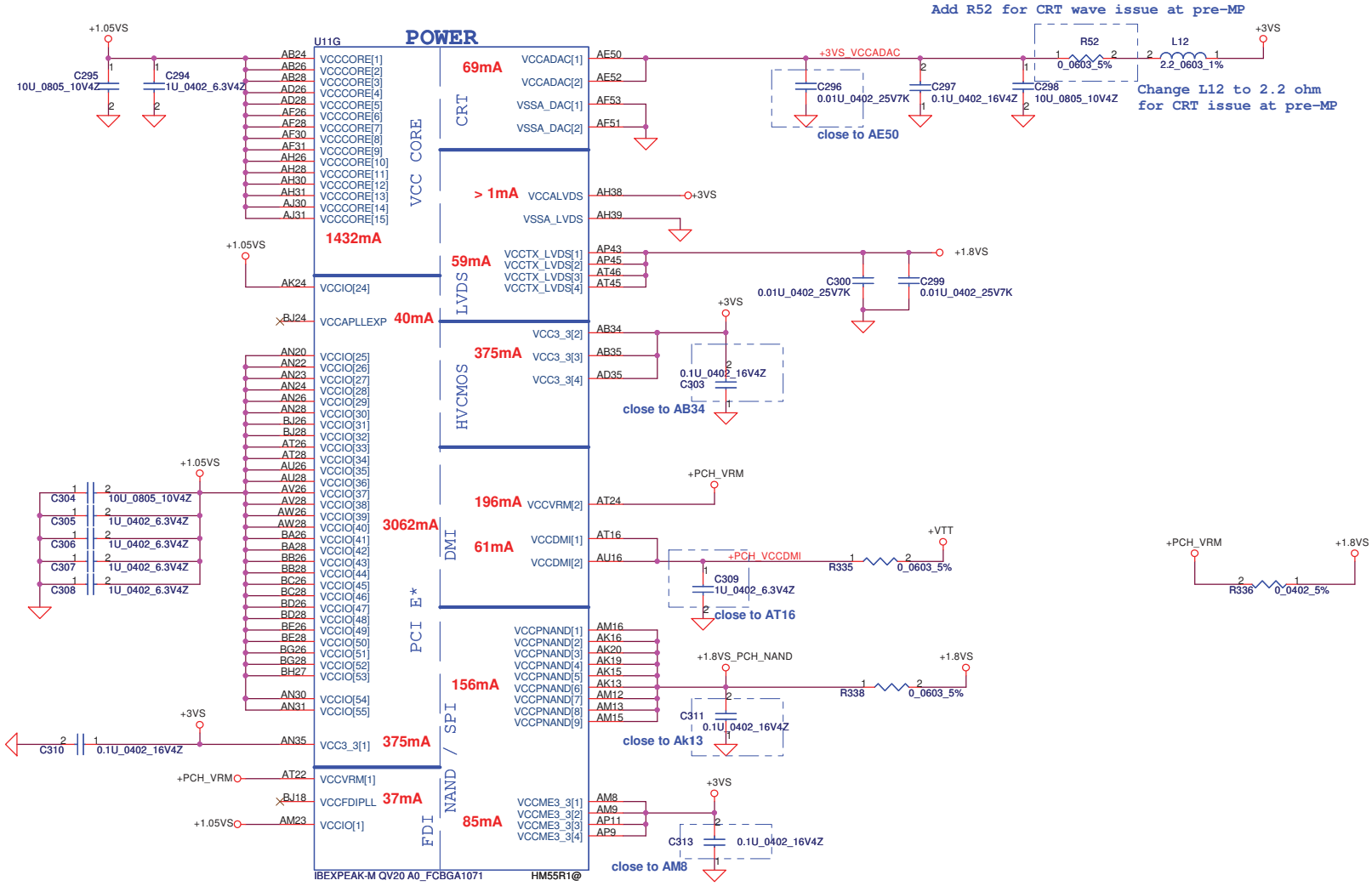
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Compal Electronics, Inc.

Title: PCH CPU/GPIO

Size: B | Document Number: PWWAA LA6842P M/B | Rev: 0.2

Date: Wednesday, July 28, 2010 | Sheet 21 of 45

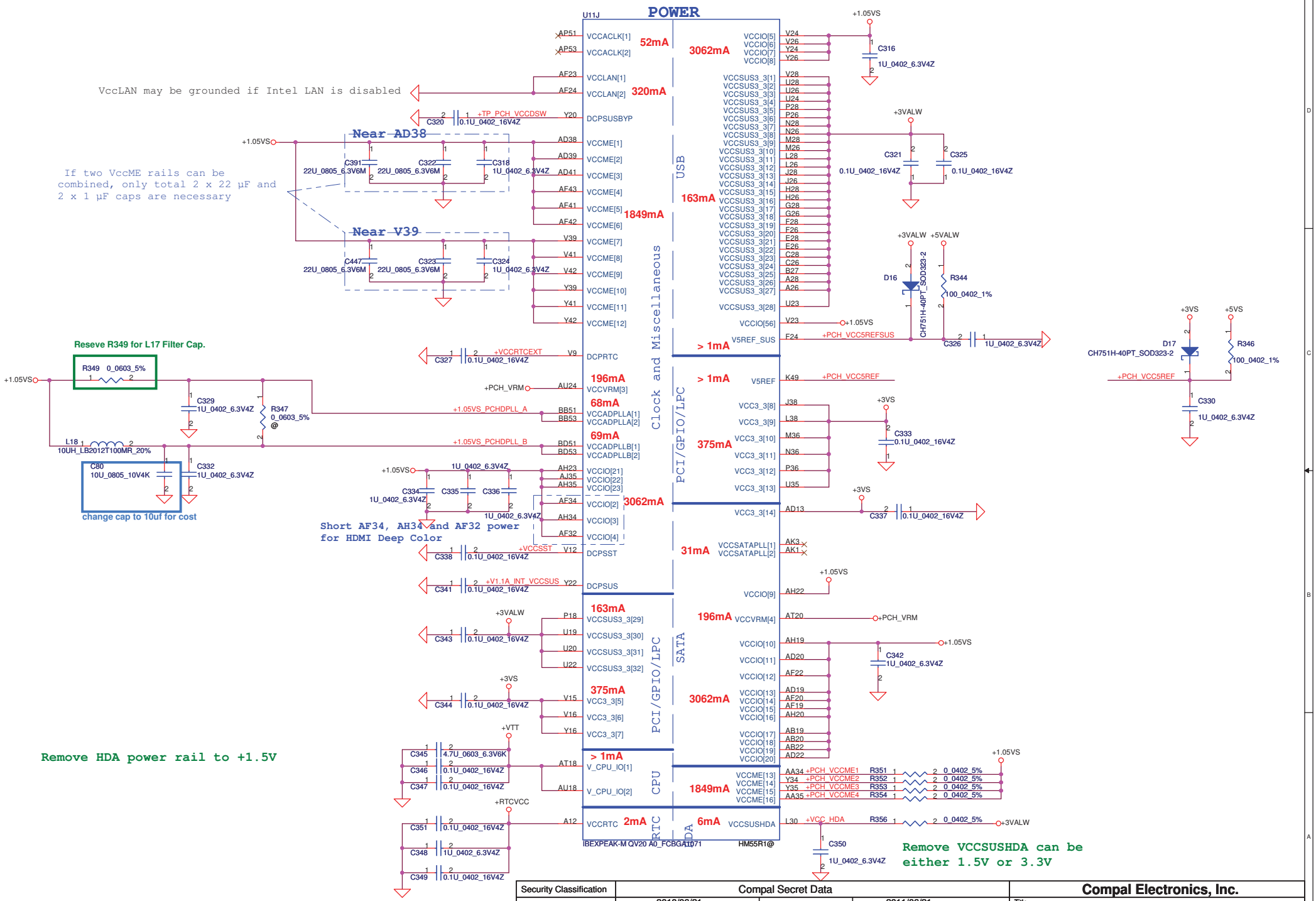


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Compal Electronics, Inc.			
Title: PCH POWER-1			
Size: B	Document Number: PWWAA LA6842P M/B		Rev: 0.2
Date: Wednesday, July 28, 2010	Sheet 22 of 45		

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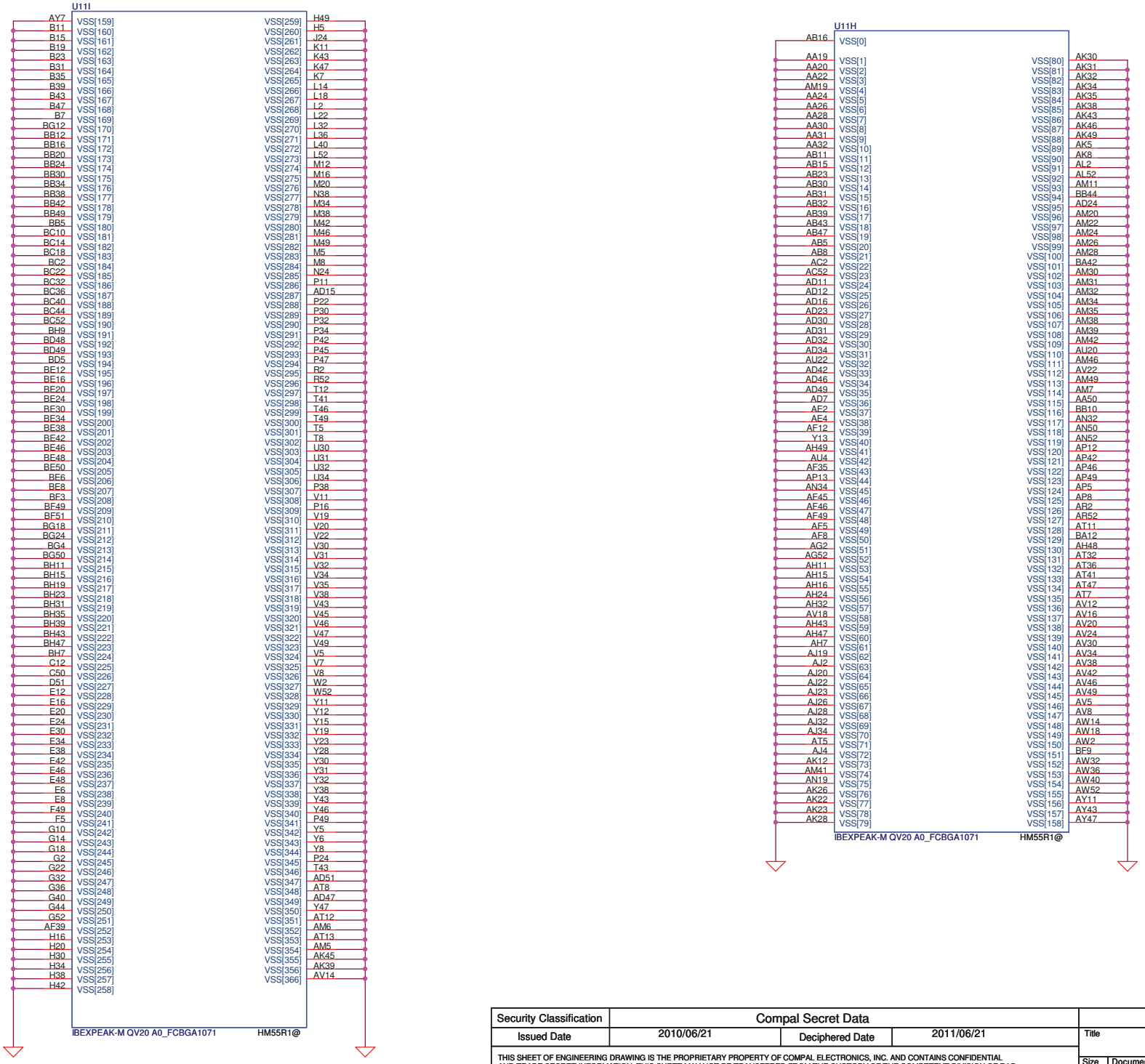


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Compal Electronics, Inc.			
Title	PCH POWER-2		
Size: Custom	Document Number: PWWAA LA6842P M/B		Rev: 0.2
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Compal Electronics, Inc.

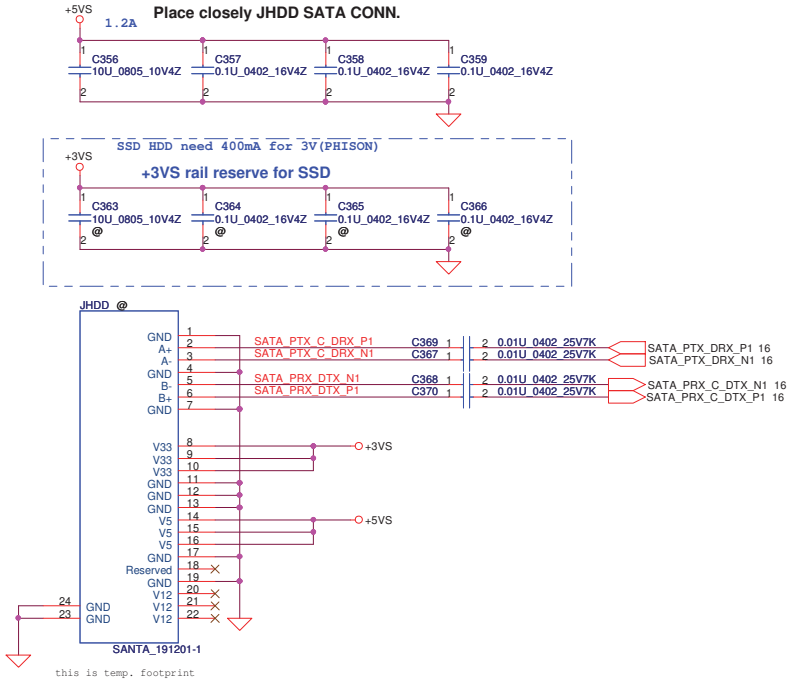
Title: **PCH-GND**

Size	Document Number	Rev
Custom	PWWAA LA6842P M/B	0.2

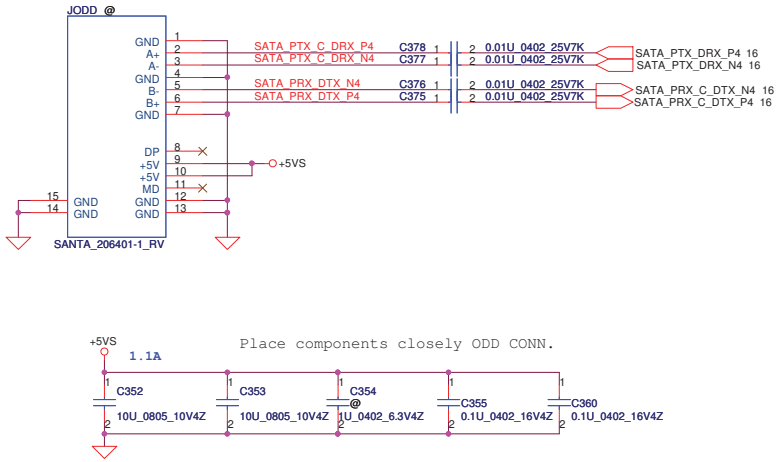
Date: Wednesday, July 28, 2010 Sheet 24 of 45

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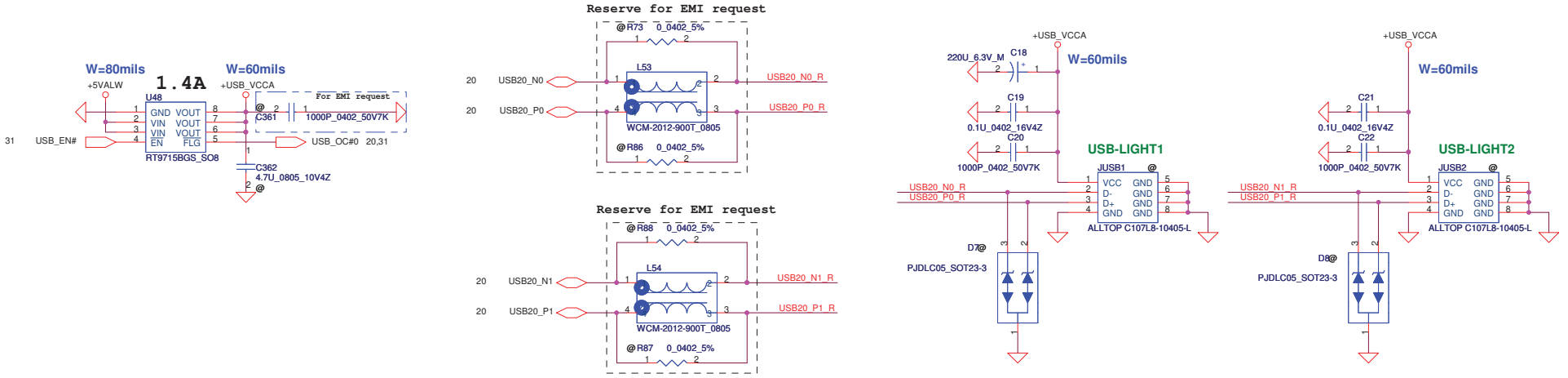
SATA HDD Conn.



SATA ODD Conn



USB Conn. (2 Port)



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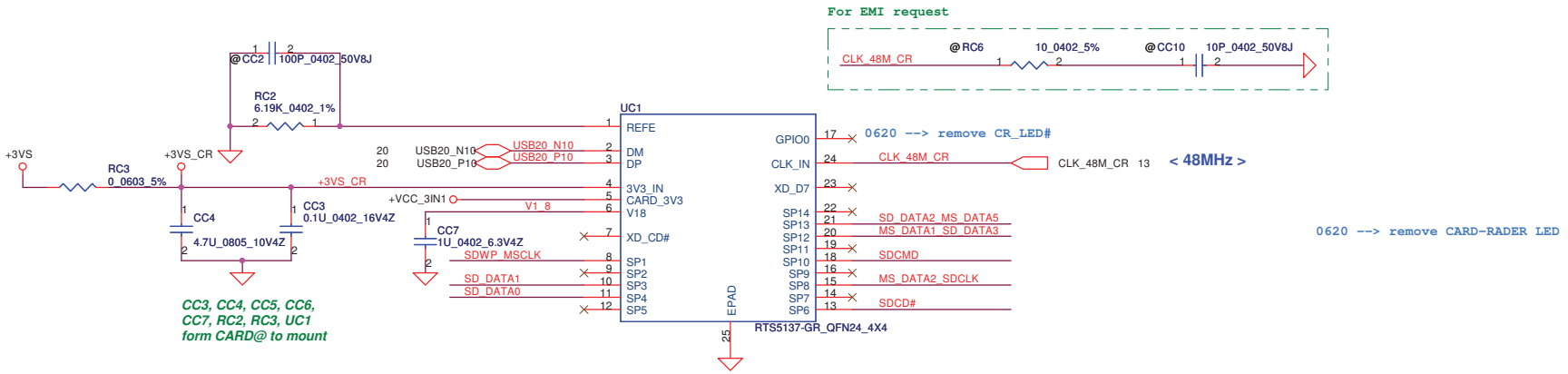
Compal Electronics, Inc.

Title: SATA-HDD/ODD/USB

Size	Document Number	Rev
	PWWAA LA6842P M/B	0.2

Date: Wednesday, July 28, 2010 Sheet 25 of 45

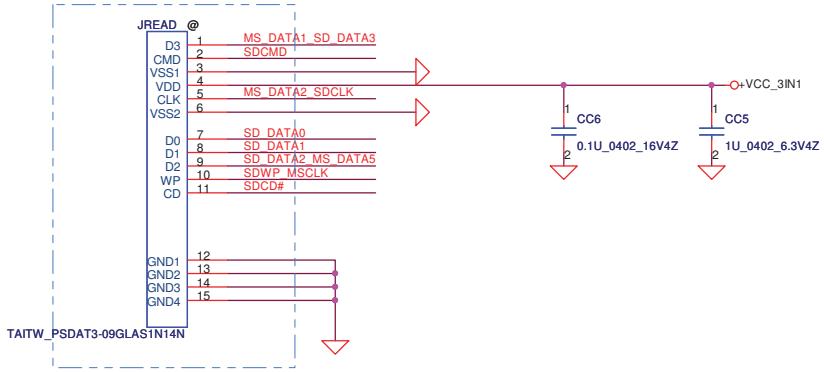
http://laptop-motherboard-schematic.blogspot.com/



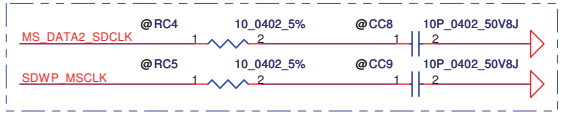
0715 --> change P/N to RTS5137 (SA000043500)

< 2 in 1 Card Reader >

0624 --> change CARDREADER conn.



For EMI request



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Compal Electronics, Inc.

Title: RTS5137 2in1 Card Reader

Size | Document Number: PWWAA LA6842P M/B | Rev: 0.2

Date: Wednesday, July 28, 2010 | Sheet 26 of 45

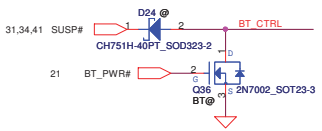
http://laptop-motherboard-schematic.blogspot.com/

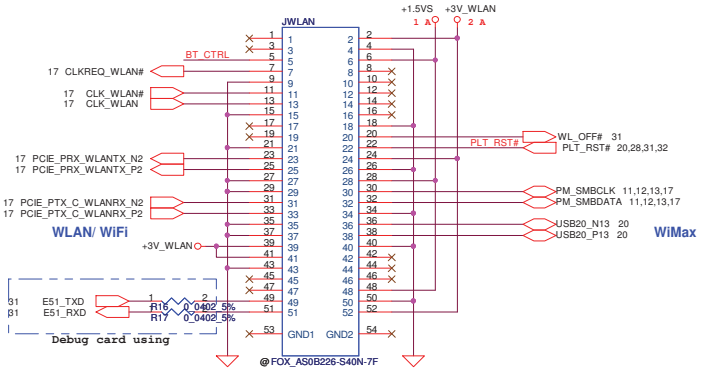
PCIe Mini Card-WLAN/WiMax

WLAN&BT Combo module circuits

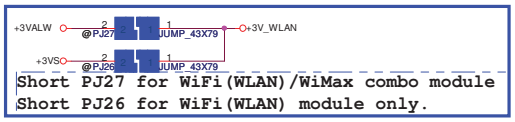
	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_PWR#	LO	HI

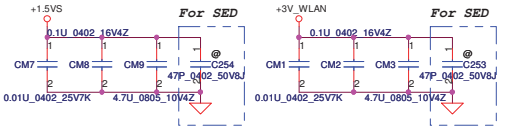
****If +3V_WLAN is +3VS, please remove D24.**





Slot#1 Half PCIe Mini Card-WLAN/WiMax





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Title	PCIe-WLAN		
Size	Document Number	PWWAA LA6842P M/B	Rev 0.2
Date: Wednesday, July 28, 2010	Sheet 27 of 45		

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3/19 --> Change JLAN for don't support LAN LED fuction
--> Pin40, 37 change to NC Pin

0715 --> LL1, CL13, CL9, LL3, CL28,
CL29 are unmount for RTL8105E-VC

C10,CL4,CL5,CL6,CL7 close to
Pin 27,39,12,47,48

CL19,CL20,CL21,CL22 close to
Pin 3,13,29,45

0715 --> change P/N to SA00003PO20 (RTL8105E-VC)

Add RL10 for +3V_LAN power enable signal
Add RL11 for wake on LAN function enable signal

0715 --> RL4 is unmount,
RL23 mount for
RTL8105E-VC

4/2->remove RL8, RL9, CL11

3/29 --> swap Line and PHY signal

Place these components
colsed to LAN chip

LAN Conn.

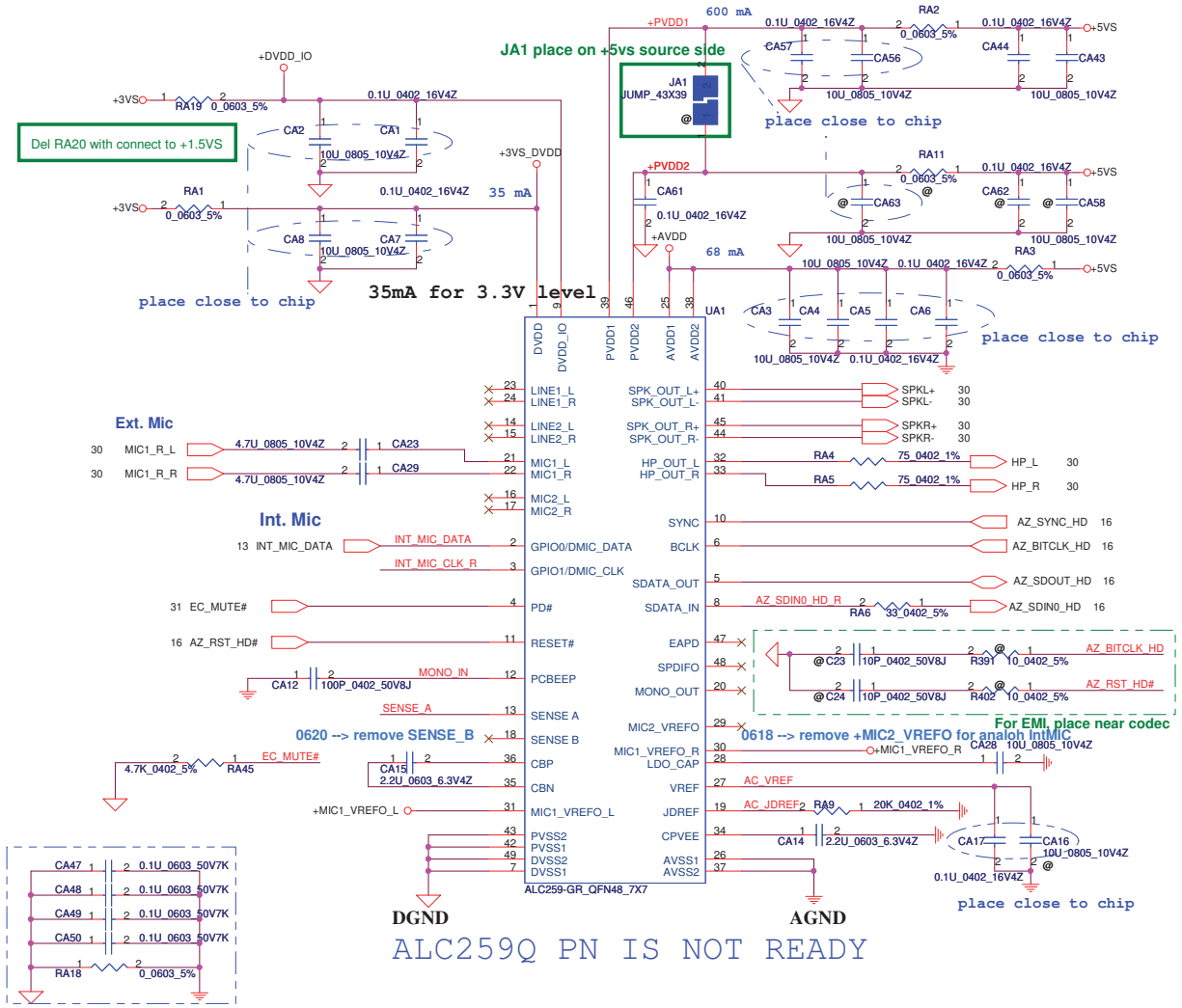
Security Classification	Compal Secret Data		
Issued Date	2010/06/21	Deciphered Date	2011/06/21

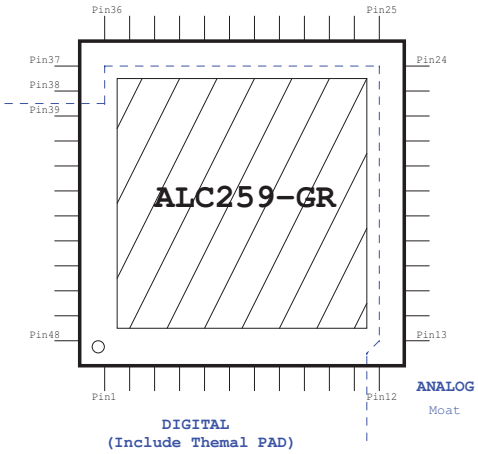
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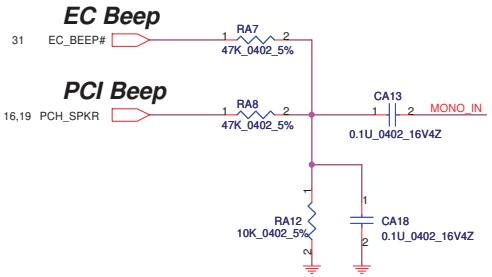
Compal Electronics, Inc.			
Title: RTL8105E 10/100 LAN			
Size: Custom	Document Number: PWWAA LA6842P M/B		Rev: 0.2
Date: Wednesday, July 28, 2010	Sheet 28 of 45		

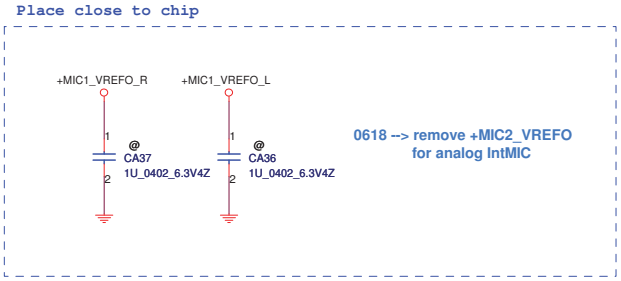
Codec

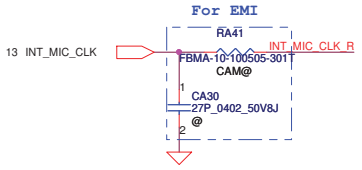




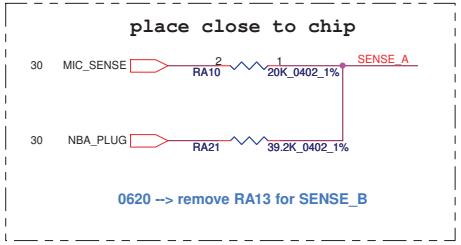
Beep sound







Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
	39.2K	PORT-E (PIN 14, 15)	



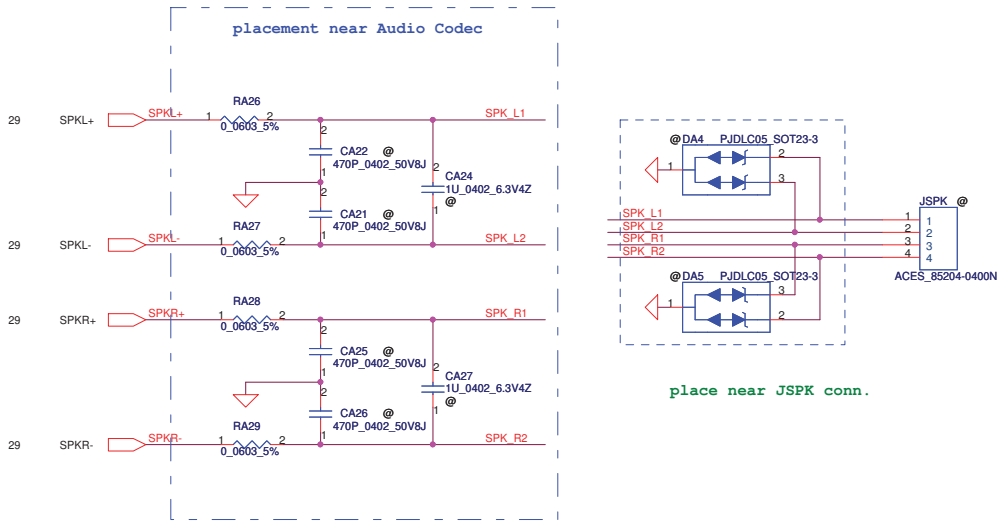
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Issued Date	2010/06/21	Deciphered Date	2011/06/21

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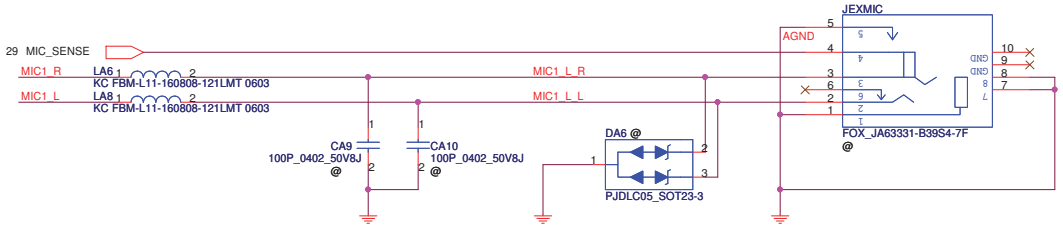
Title	HDA CODEC ALC259-GR		
Size	Document Number	PWWAA LA6842P M/B	Rev 0.2
Date: Wednesday, July 28, 2010	Sheet 29 of 45		

Speaker Connector

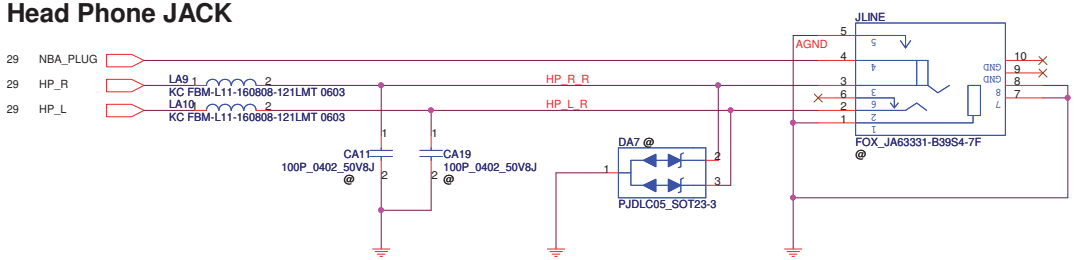


place near JSPK conn.

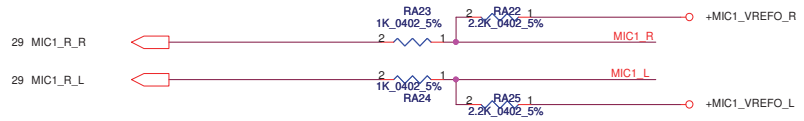
Ex.MIC JACK



Head Phone JACK



Ext.MIC/LINE IN



Int. Mic

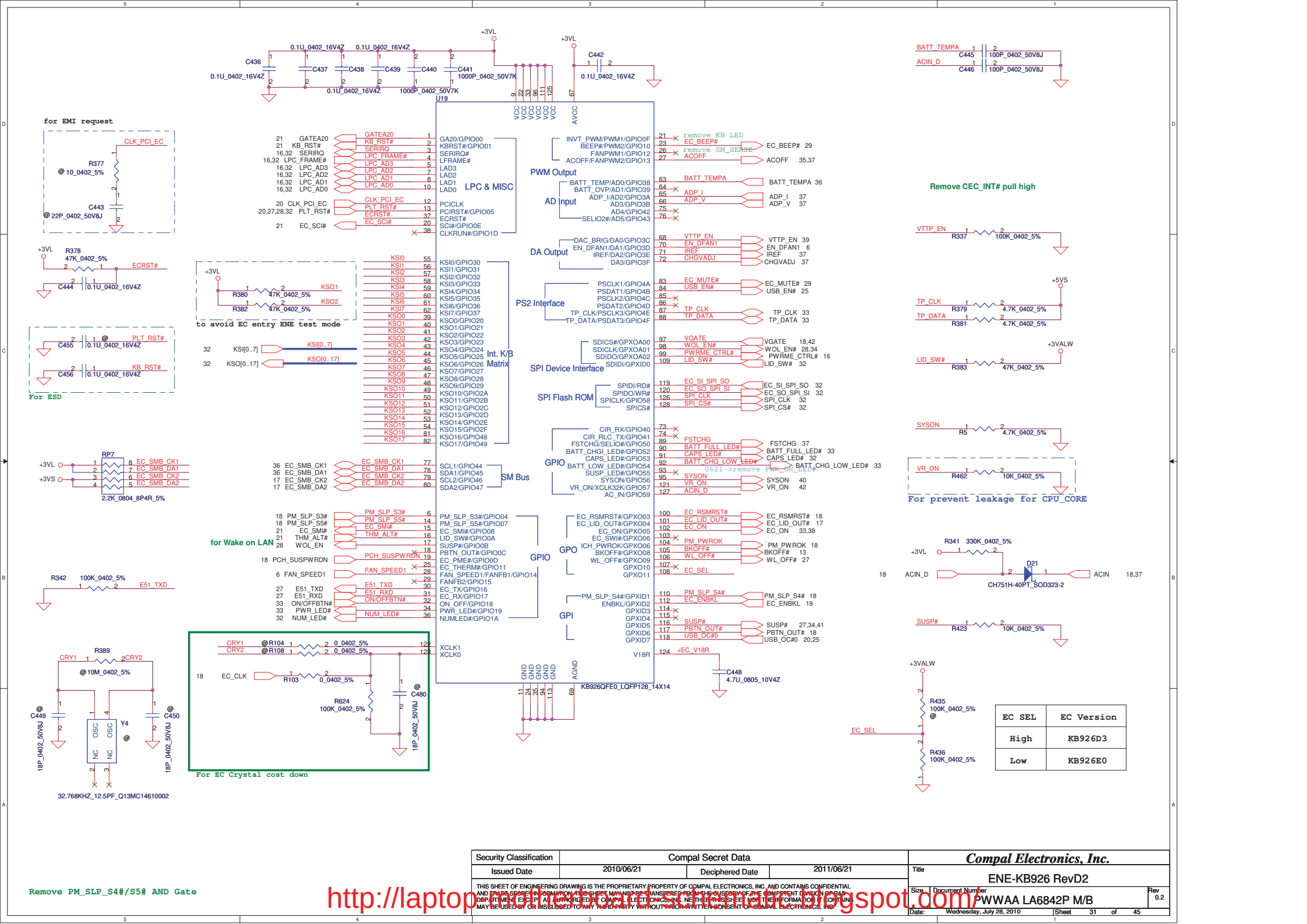
0618 --> remove Analog IntMIC, and change to DIGITAL MIC

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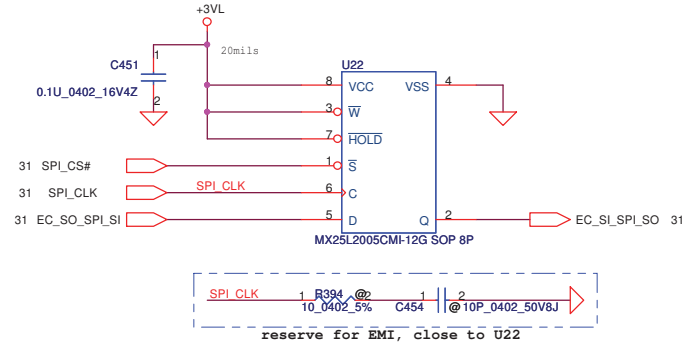
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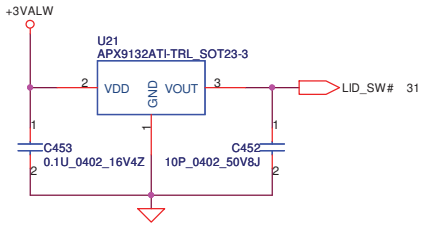
Compal Electronics, Inc.			
Title	HDA CODEC ALC259-GR		
Size	Document Number	PWWAA LA6842P M/B	Rev 0.2
Date:	Wednesday, July 28, 2010	Sheet 30 of 45	


U19
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
KB926QFE0_LQFP128_14X14
for EMI request
to avoid EC entry ENE test mode
for Wake on LAN
For ESD
For EC Crystal cost down
Remove CEC_INT# pull high
For prevent leakage for CPU_CORE
Remove PM_SLP_S4#/S5# AND Gate
32.768KHZ_12.5PF_Q13MC14610002
2.2K_0804_8P4R_5%
CH751H-40PT_SOD323-2
0621->remove PWR_ON_LED#
EC SEL | EC Version
High | KB926D3
Low | KB926E0
Compal Secret Data
Issued Date 2010/06/21
Deciphered Date 2011/06/21
Compal Electronics, Inc.
ENE-KB926 RevD2
PWWAA LA6842P M/B
Rev 0.2
Wednesday, July 28, 2010
Sheet 31 of 45

SPI Flash (256KB)

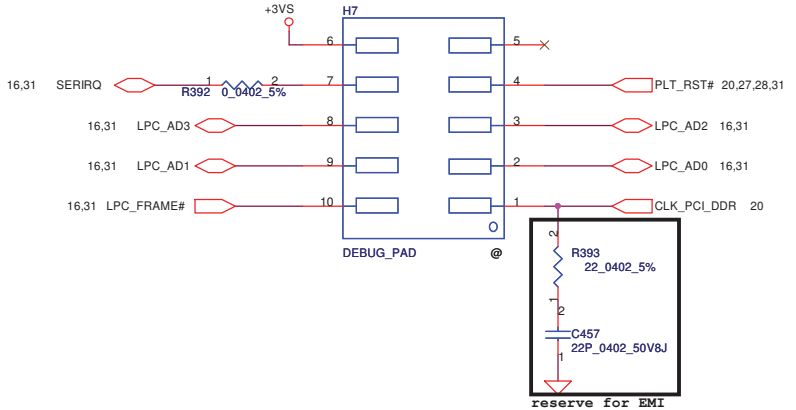


Lid SW

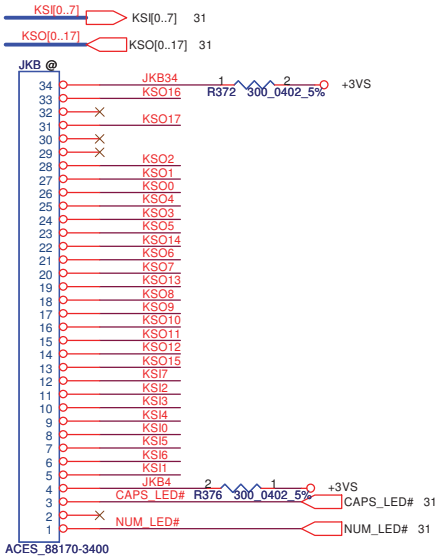


LPC Debug Port

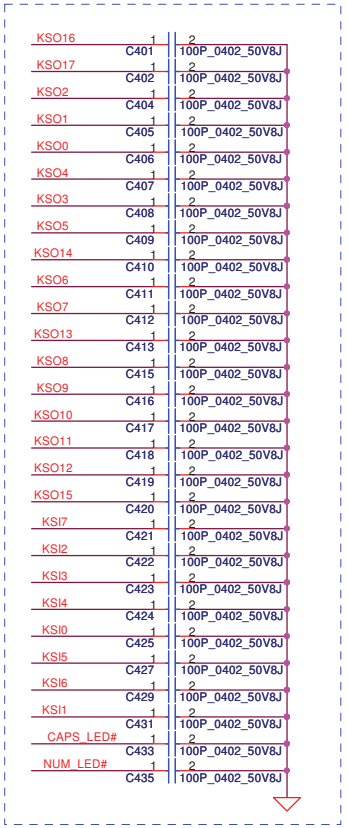
Please place the PAD under DDR DIMM.



KEYBOARD CONN.



please close to JKB



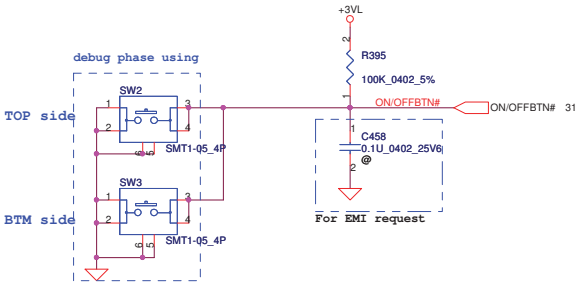
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Issued Date	2010/06/21	Deciphered Date	2011/06/21

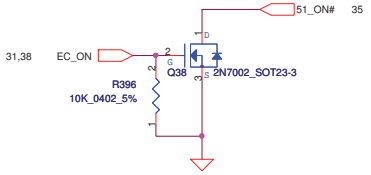
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Compal Electronics, Inc.		
Title	SPI ROM/TP/KB/Debug	
Size	Document Number PWWAA LA6842P M/B	Rev 0.2
Date: Wednesday, July 28, 2010	Sheet 32 of 45	

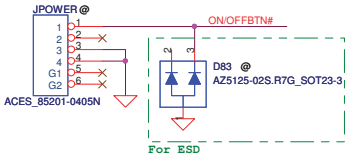
http://laptop-motherboard-schematic.blogspot.com/

Power Button

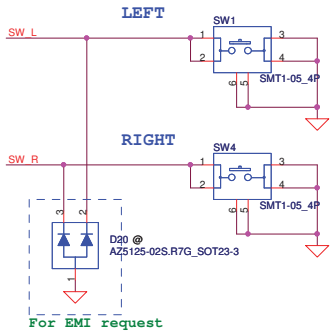


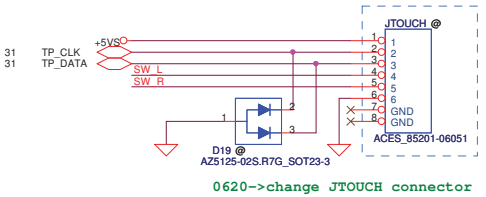


PWR/B to MB Conn.



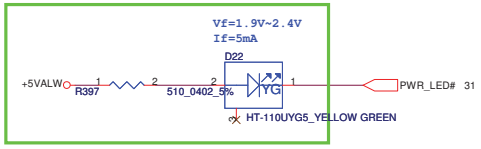
TP Button/Conn.



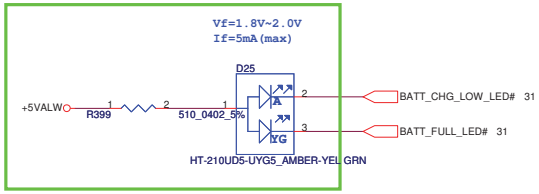


0620->change JTOUCH connector

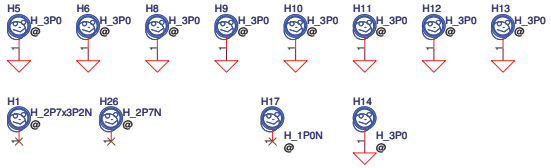
POWER/SUSPEND LED



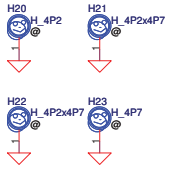
BATT CHARGE/FULL LED



Screw Hole



CPU



MINI CARD

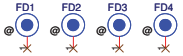


SB



For Codec AGND
Dummy
3G
MDC

PCB Fedical Mark PAD



ISPD

PCB ZZZ PCB LA-6842P REV0

DC-IN PJP1 PJP1 45@

PCH U11 PCH HM55R3@

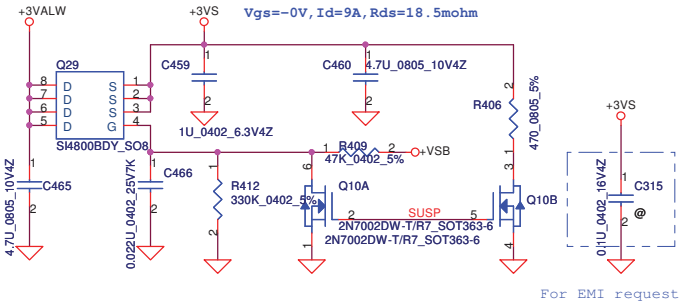
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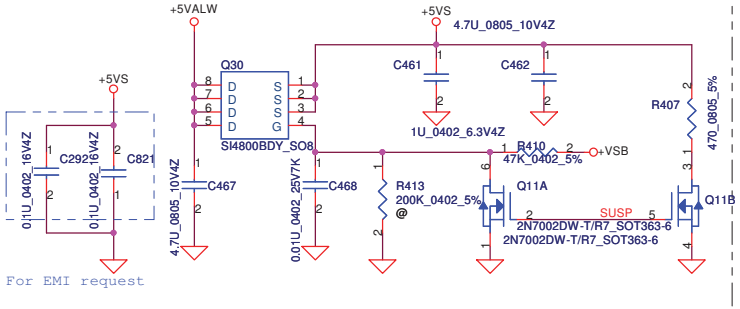
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Size	Document Number PWWAA LA6842P M/B	Rev 0.2
Date: Wednesday, July 28, 2010	Sheet 33 of 45	

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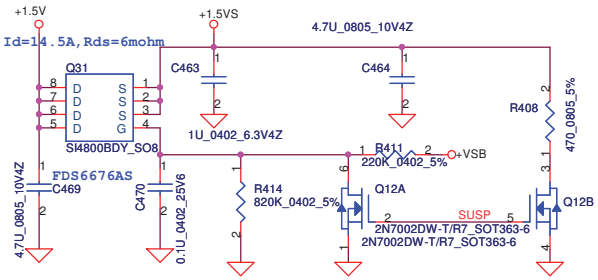
+3VALW TO +3VS



+5VALW TO +5VS

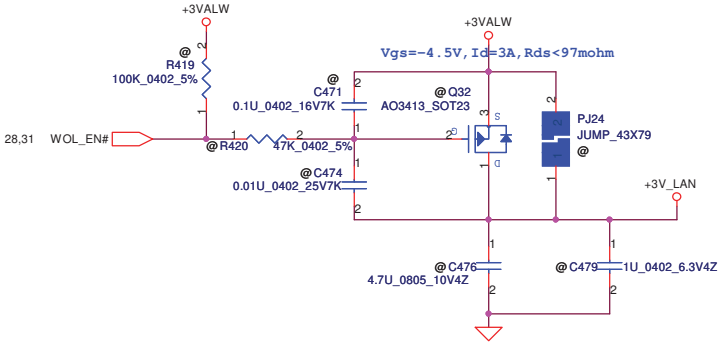


+1.5V to +1.5VS

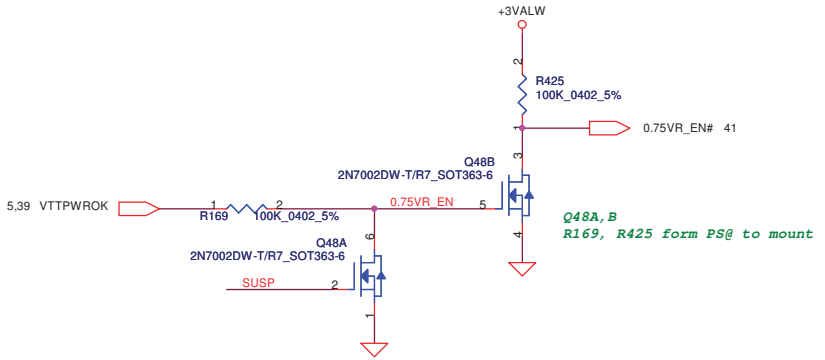


0715 --> Q31 change to SB548000310 the same as +5VS

+3VALW TO +3V_LAN

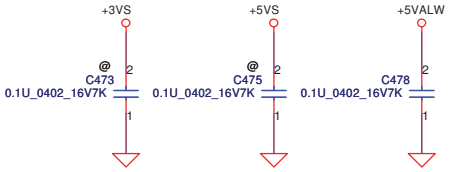


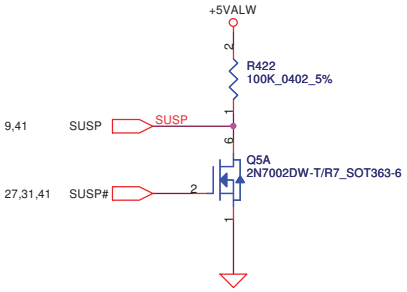
For S3 CPU Power Saving

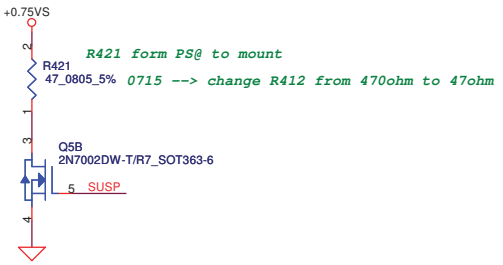


Q48A,B
R169, R425 form PS@ to mount

Reserve for EMI test







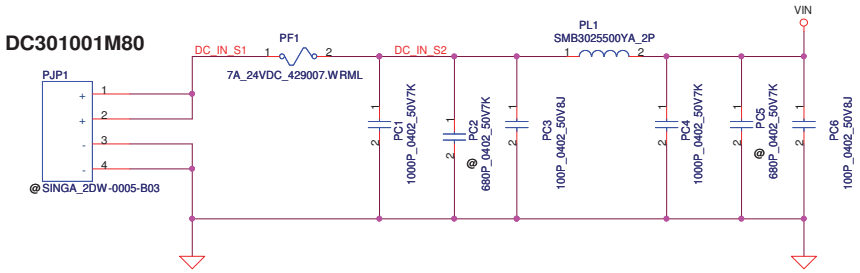
R421 form PS@ to mount
0715 --> change R412 from 470ohm to 47ohm

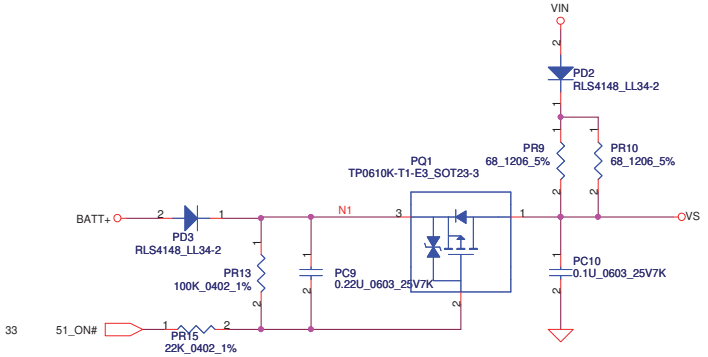
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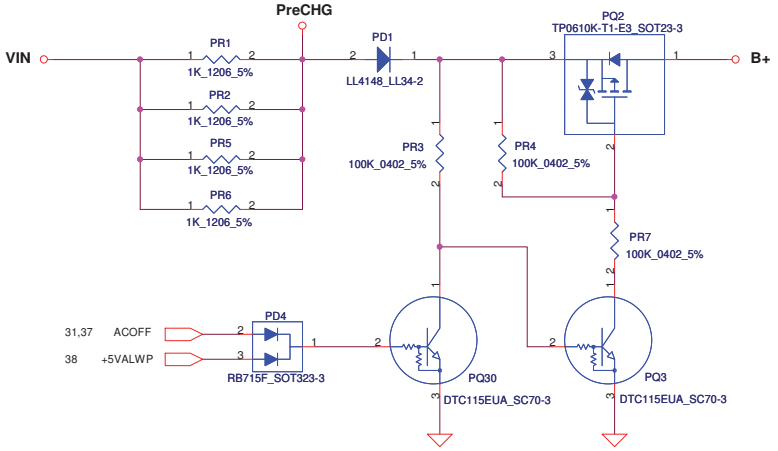
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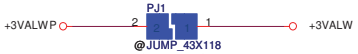
Compal Electronics, Inc.			
Title	DC-DC INTERFACE		
Size	Document Number	PWWAA LA6842P M/B	Rev 0.2
Date: Wednesday, July 28, 2010	Sheet 34 of 45		

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(5A,200mils ,Via NO.= 10)

OCP(min)=7.7A

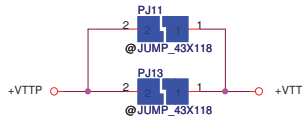


(5A,200mils ,Via NO.= 10)

OCP(min)=7.9A



(120mA,40mils ,Via NO.= 1)



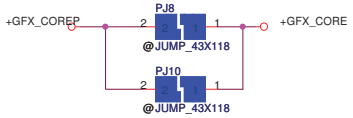
(20A,800mils ,Via NO.=40)

OCP(min)=27.49A



(9A,360mils ,Via NO.= 18)

OCP(min)=9.8A



(22A,880mils ,Via NO.=44)

OCP(min)=26A



(1.5A,60mils ,Via NO.= 4)



(2A,80mils ,Via NO.= 4)



(100mA,40mils ,Via NO.= 2)

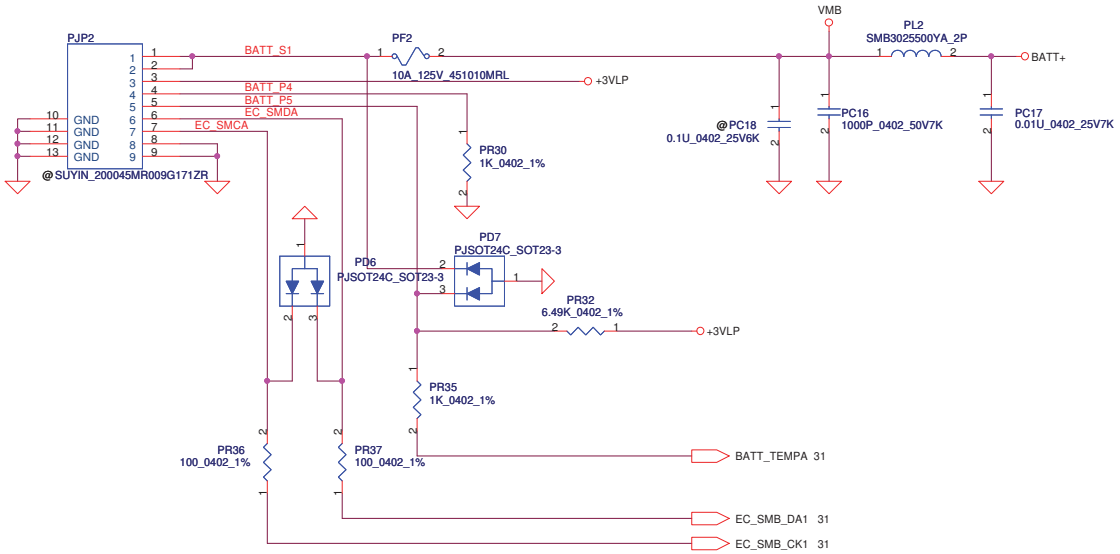
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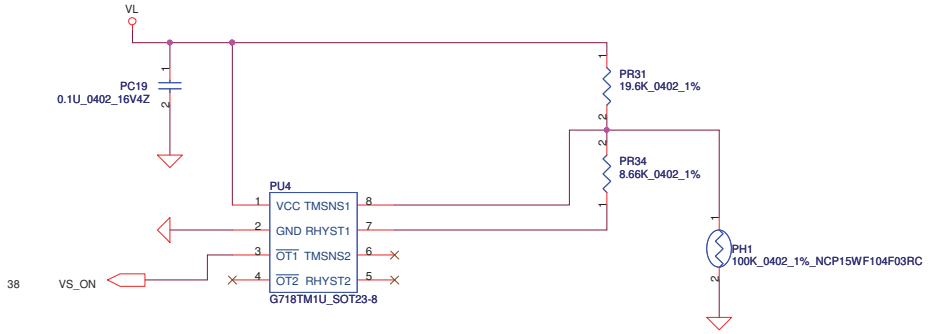
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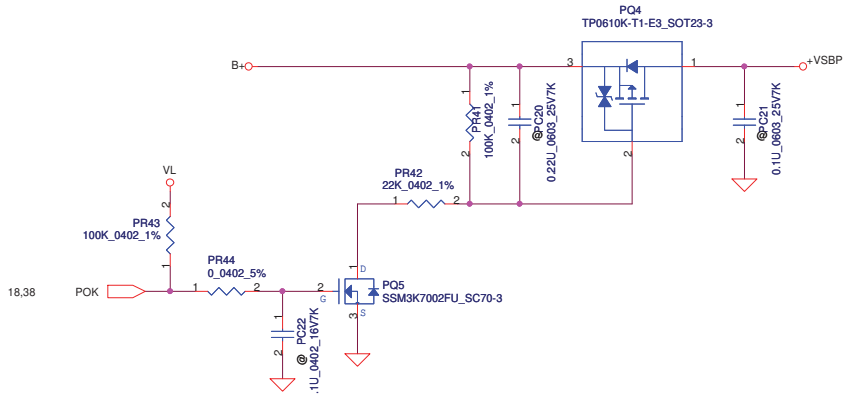
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Title	DCIN / DETECTOR		
Size	Document Number	PWWAA LA6842P M/B	Rev 0.2
Date: Wednesday, July 28, 2010	Sheet 35 of 45		

PH1 under CPU botten side :
CPU thermal protection at 95degree C
Recovery at 56 degree C





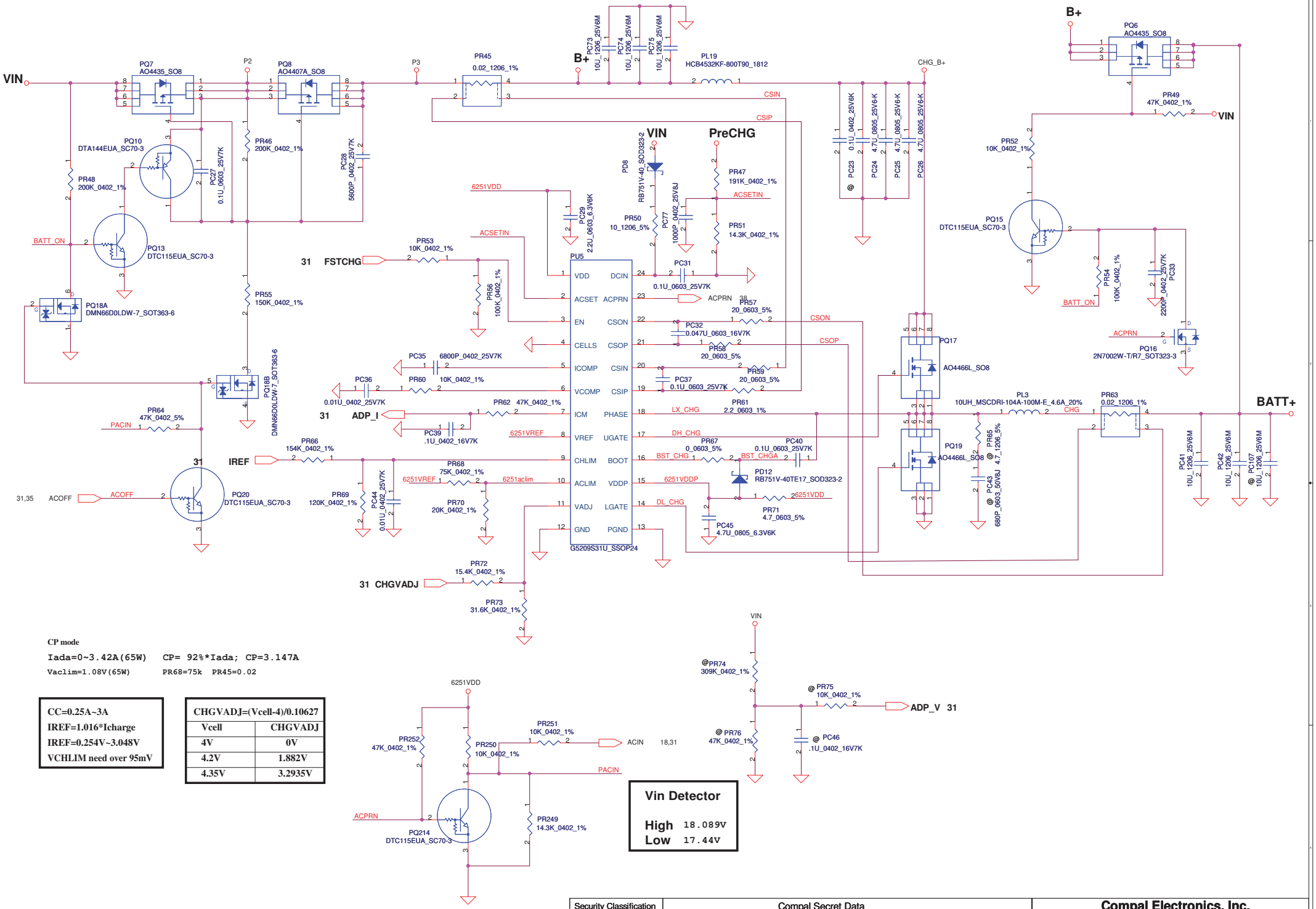


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Compal Electronics, Inc.	
Title	BATTERY CONN / OTP
Size	Document Number: PWWAA LA6842P M/B
Rev	0.2
Date: Wednesday, July 28, 2010	Sheet 36 of 45



CP mode

Iada=0~3.42A(65W) CP= 92%*Iada; CP=3.147A

Vaclim=1.08V(65W) PR68=75k PR45=0.02

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Vin Detector

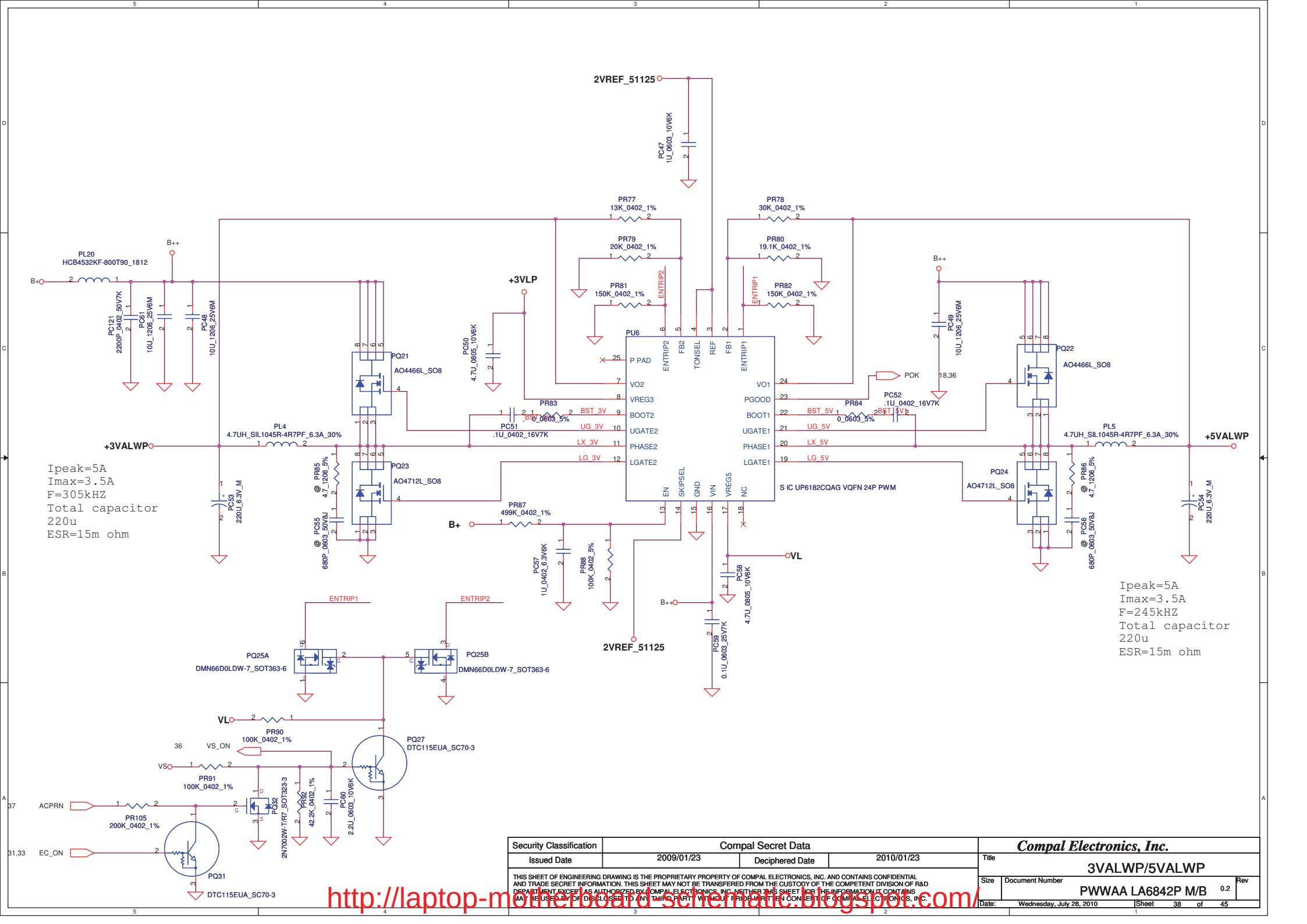
High 18.089V
Low 17.44V

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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Title	CHARGER		
Size	Document Number	PWWAA LA6842P M/B	Rev 0.2
Date: Wednesday, July 28, 2010	Sheet 37 of 45		



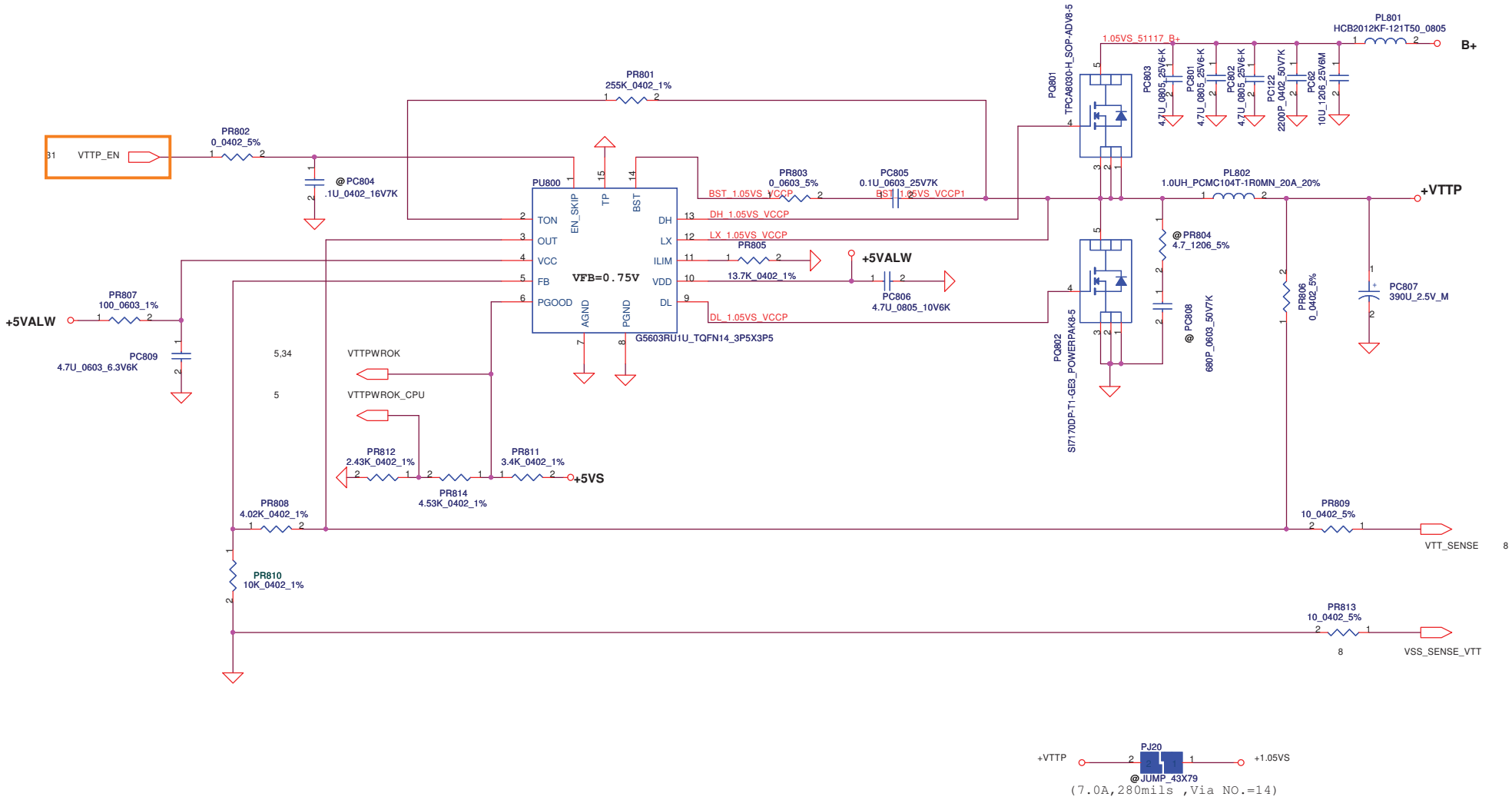
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Issued Date	2009/01/23	Deciphered Date	2010/01/23

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Title	3VALWP/5VALWP	
Size	Document Number	Rev
	PWWAA LA6842P M/B	0.2
Date: Wednesday, July 28, 2010	Sheet 38 of 45	

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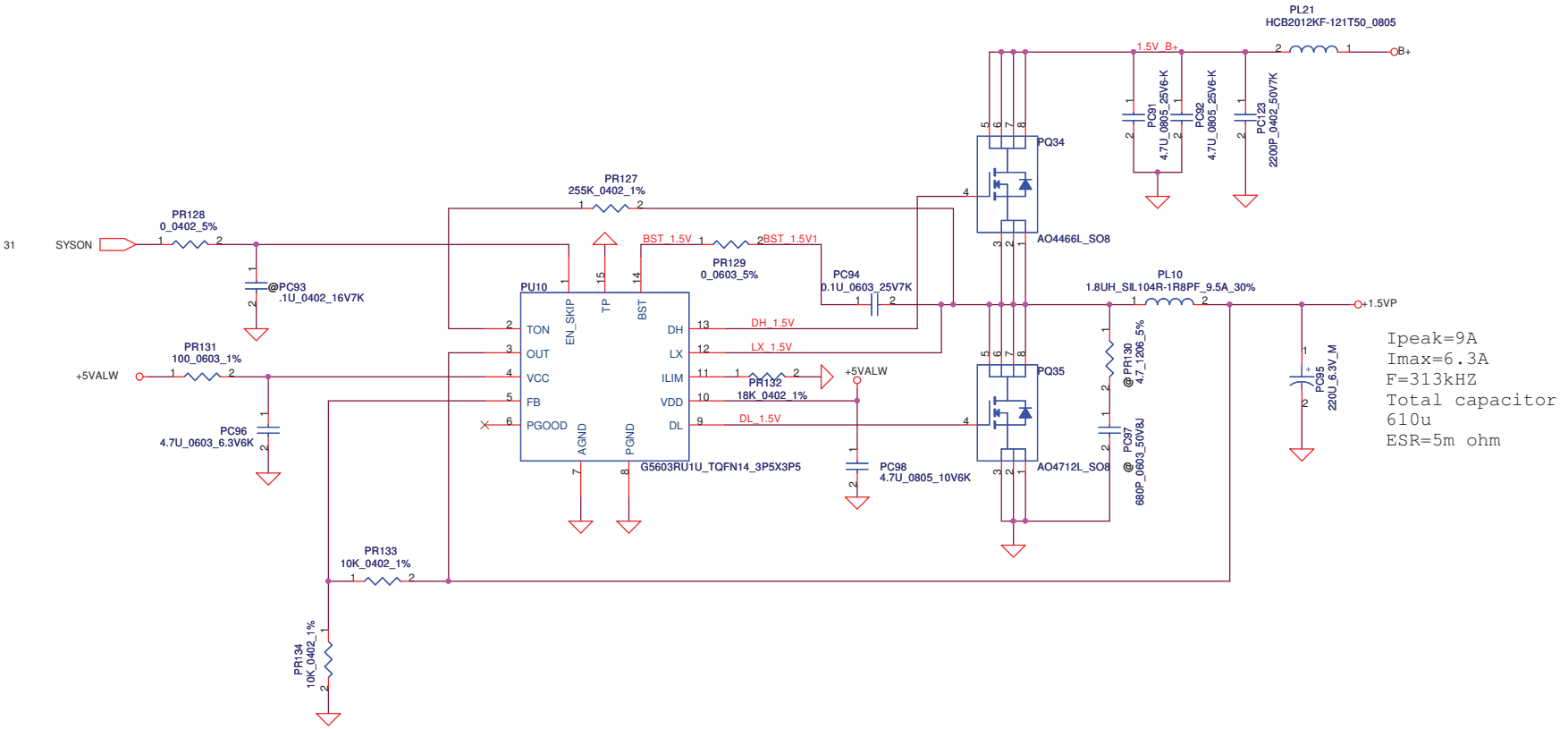
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Date: Wednesday, July 28, 2010	Sheet 39 of 45	

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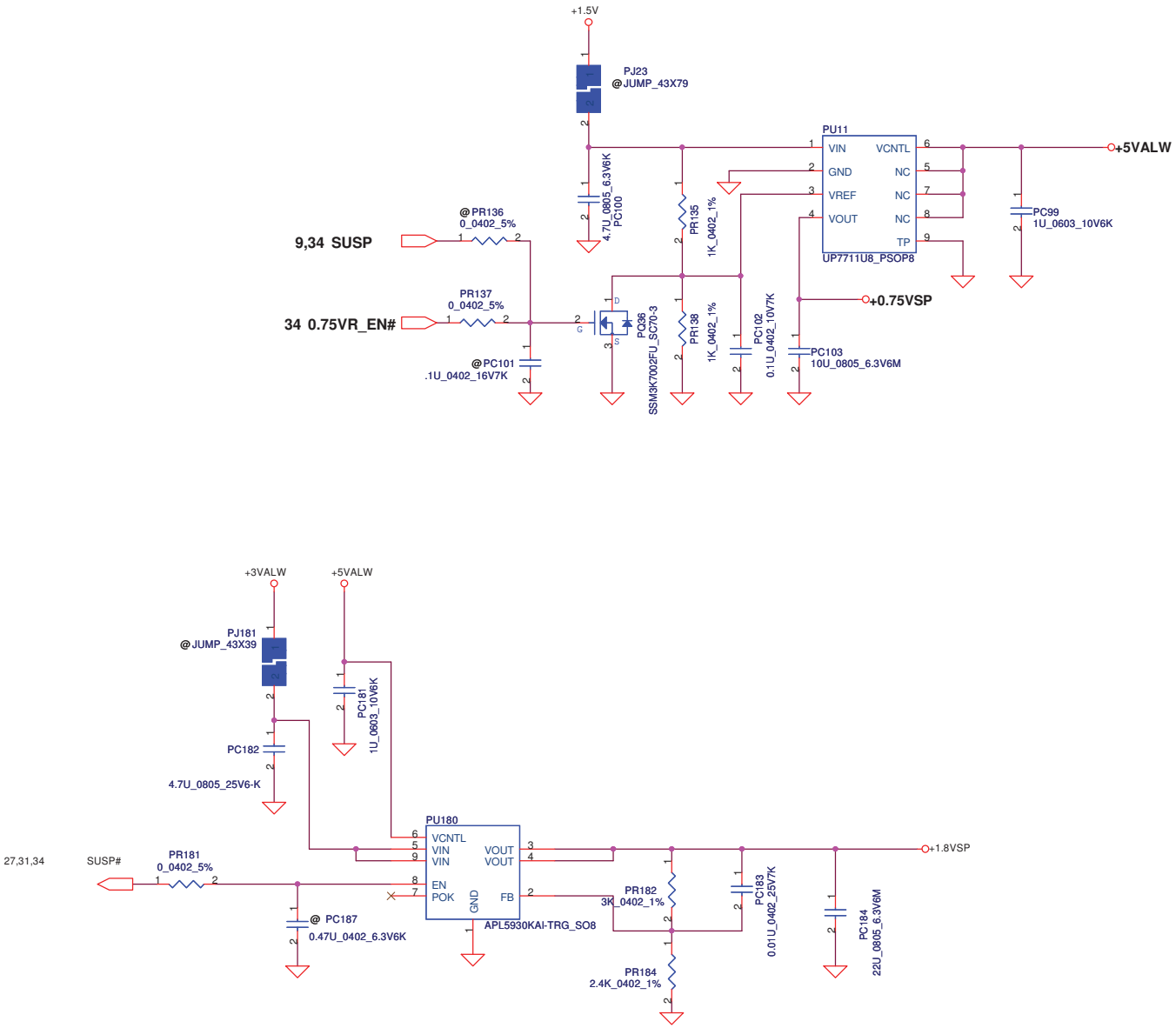
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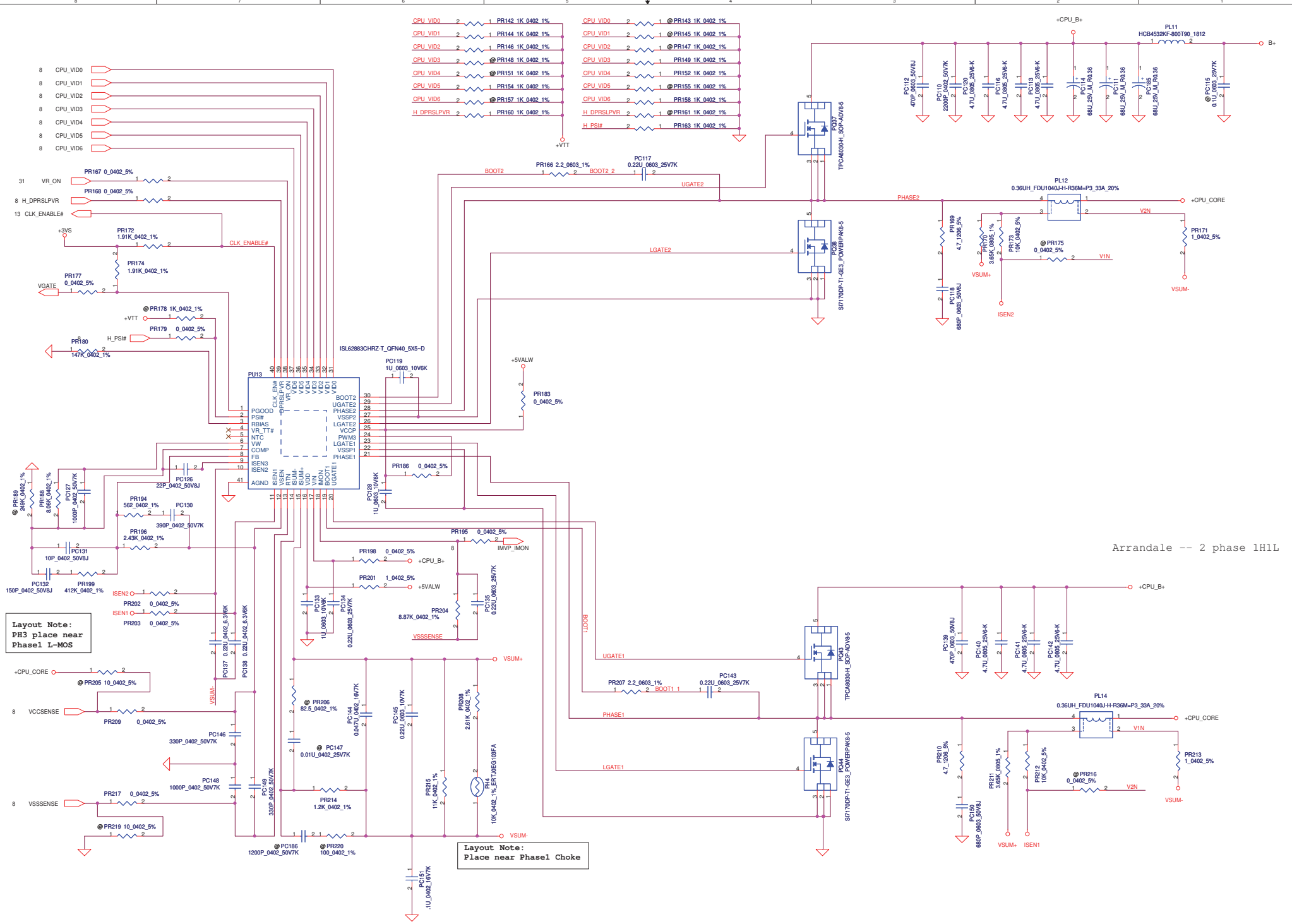


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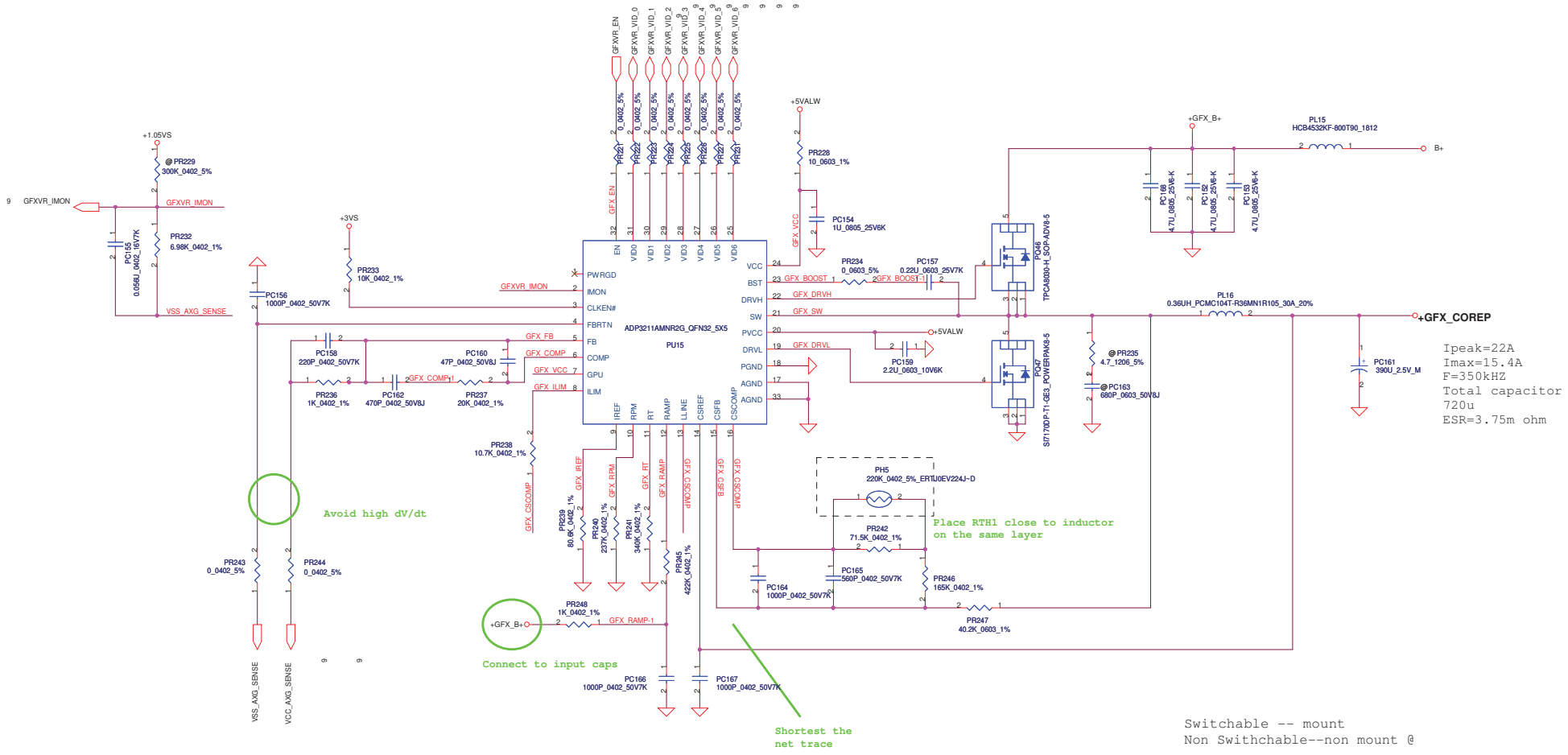
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Title	+CPU_CORE		
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Title	+GFX_COREP		
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Date: Wednesday, July 28, 2010	Sheet 43 of 45		

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	2010/07/13	42	Change PL12,PL14 to SH00000IN00	BOM modify
	2010/07/13	43	Change PL16 to SH00000IN00	BOM modify
	2010/07/23	36	Change PC19 to SE070104Z80	BOM modify
	2010/07/26	36	Add PD6,PD7	EMI request
	2010/07/26	37	Add PC73,PC74,PC75(10U_1206)	EMI request
	2010/07/26	38	Add PC121(2200P_0402),PC61(10U_1206)	EMI request
	2010/07/26	39	Add PC122(2200P_0402),PC62(10U_1206)	EMI request
	2010/07/26	40	Add PC123(2200P_0402)	EMI request

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Size	Document Number: PWWAA LA6842P M/B	Rev: 0.2
Date: Wednesday, July 28, 2010	Sheet 44 of 45	

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PIR (Product Improve Record)

PWWAA LA-6842P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2010/07/31

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

1. 20100714 / Page13 --> add 10u Cap to +1.5VS_CK505 For eSATA transmit issue ---> not add 10u Cap into schematic yet

NWQAA LA-6061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0 TO 2.0
GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/17	29	Change cardreader to JMB385/389	For customer request
2	3/18	31	Remove D86	For ESD request
3	3/18	22	Add R52	For CRT wave issue
4	3/19	22	Change L12 to 2.2 ohm	For CRT wave issue
5	3/22	15	Add D54	For HDMI CEC issue
6	3/24	13	Change C213 to 1U	For NALAA ESATA performance low issue

Security Classification	Compal Secret Data		
Issued Date	2010/06/21	Deciphered Date	2011/06/21

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Title: HW-PIR			
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Date: Wednesday, July 28, 2010	Sheet 45 of 45		