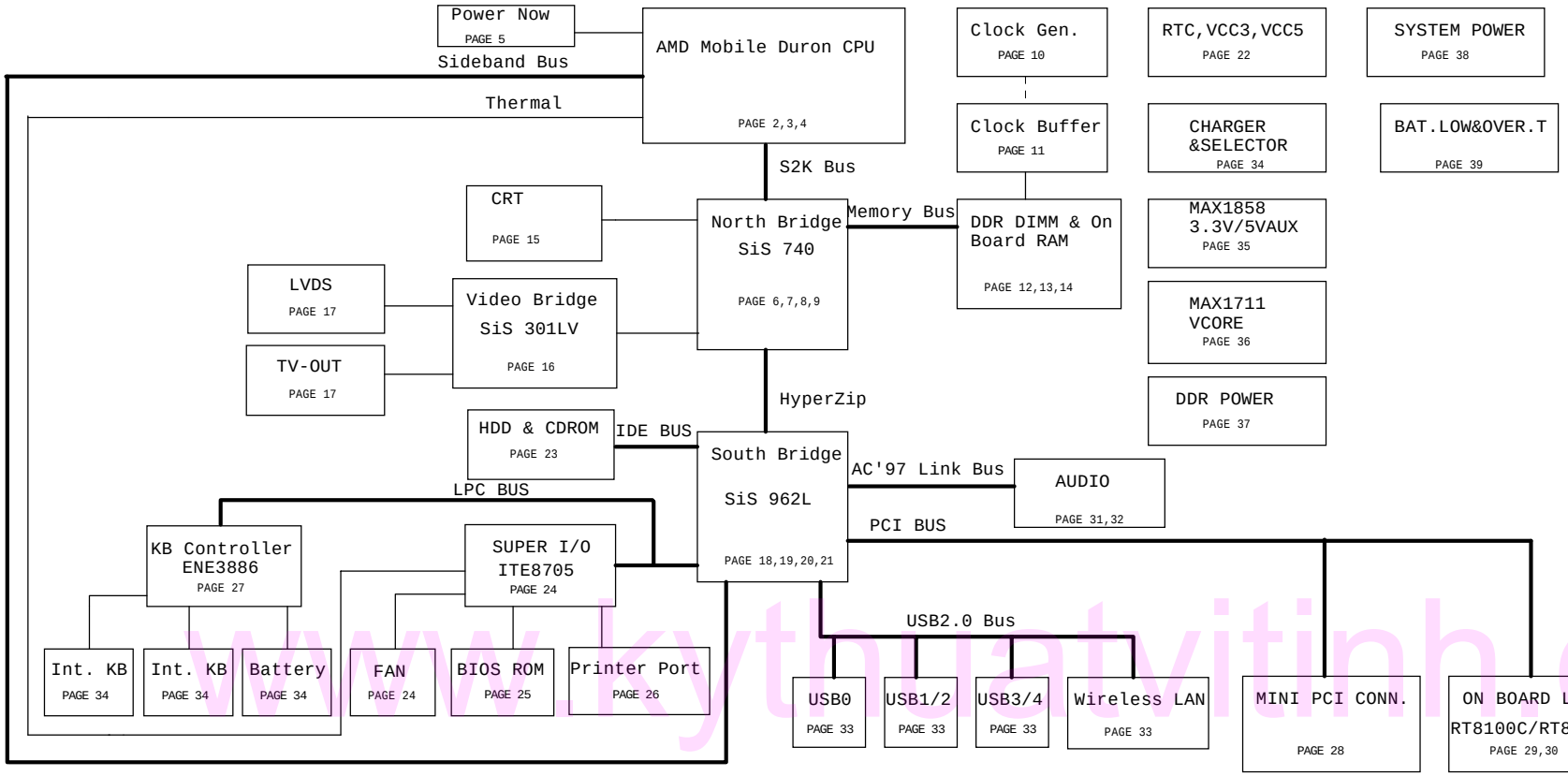


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DN: cn=fdsf, o=fsdfsd, ou=ffsdf, email=fdfsd@fsdff, c=US
Date: 2010.01.06 06:12:03 +07'00'

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P/N :
GERBER :

PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
REV																				
DATE																				

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REV																			
DATE																			

Designed by	Checked by	Approved by

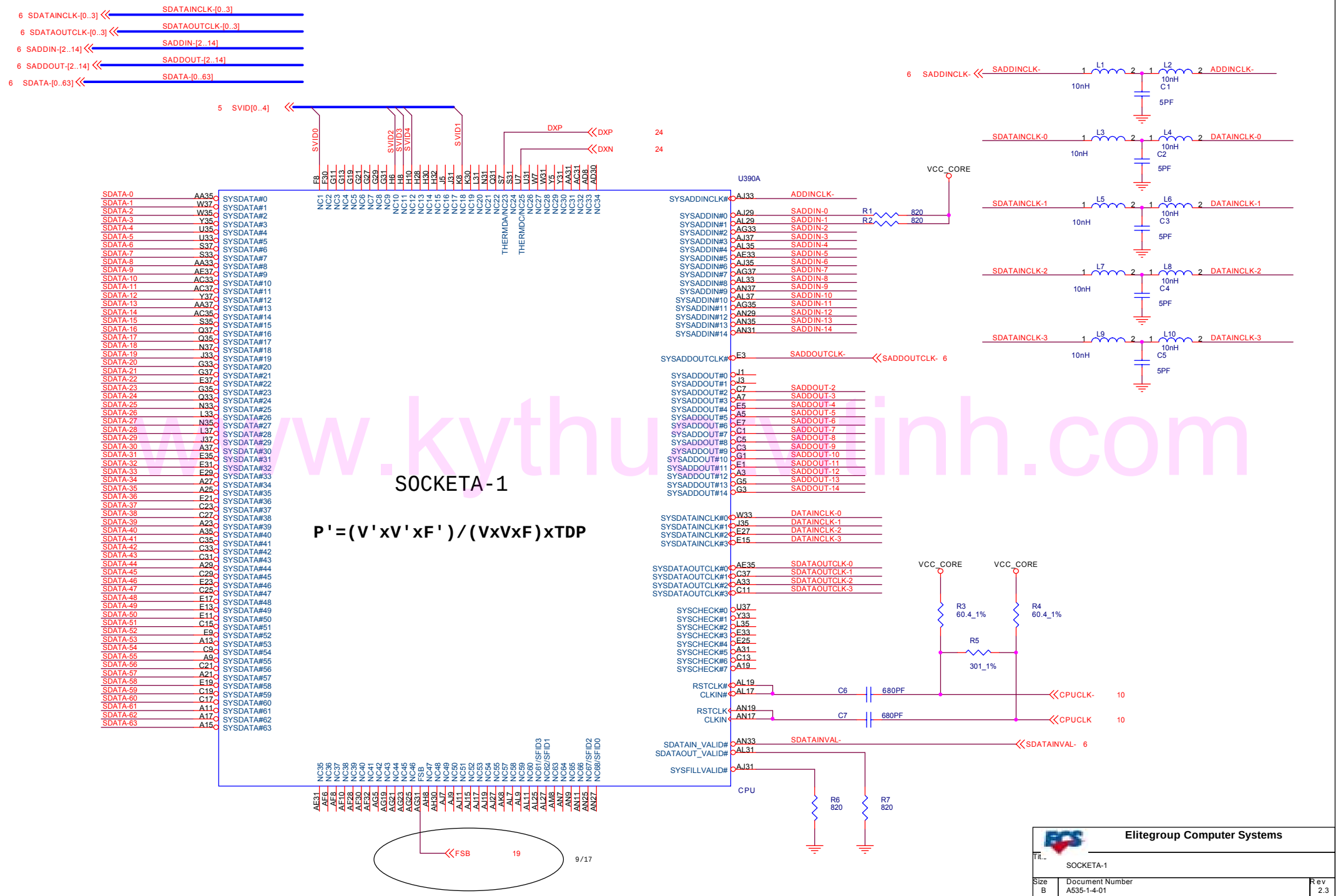
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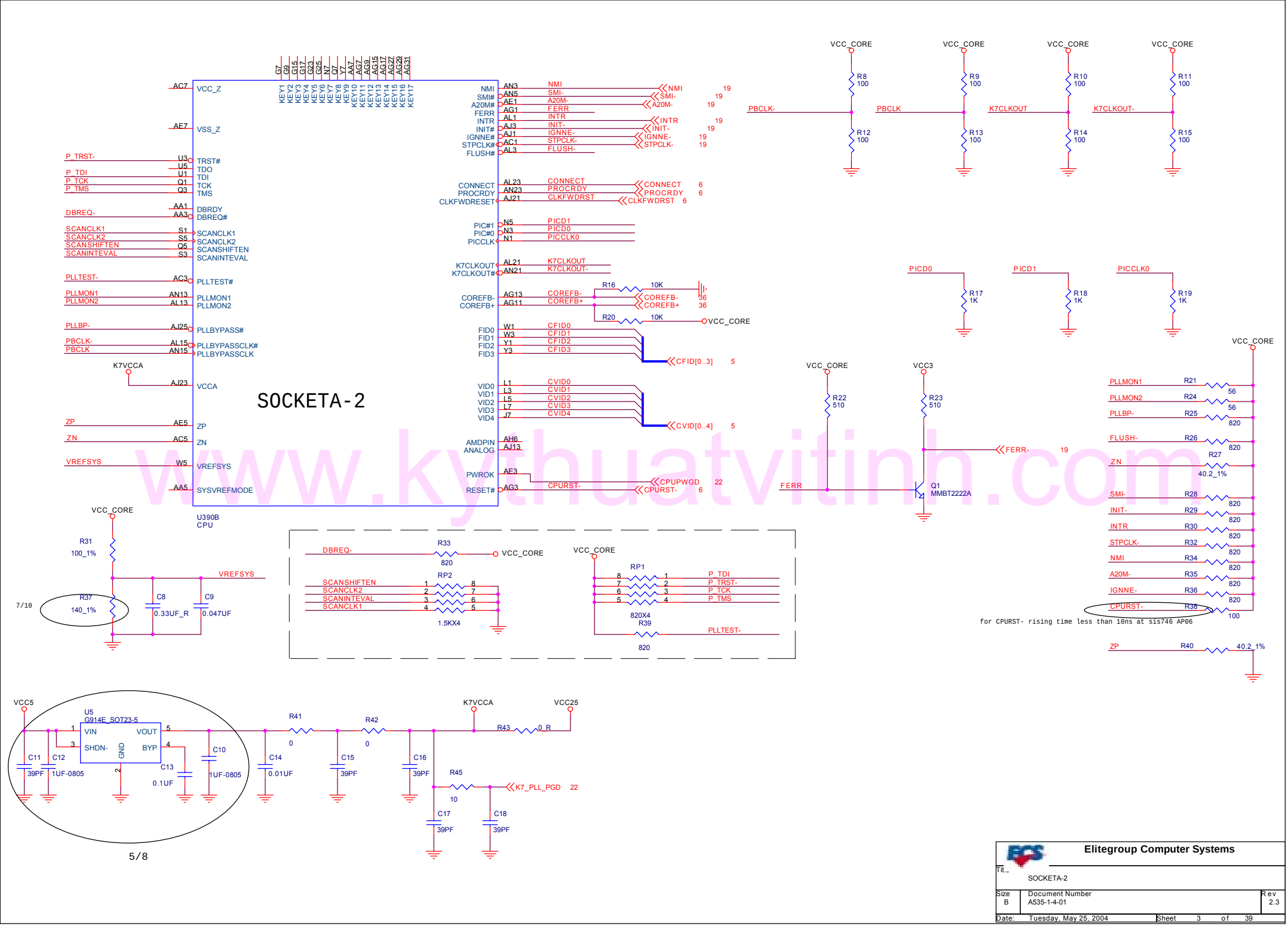
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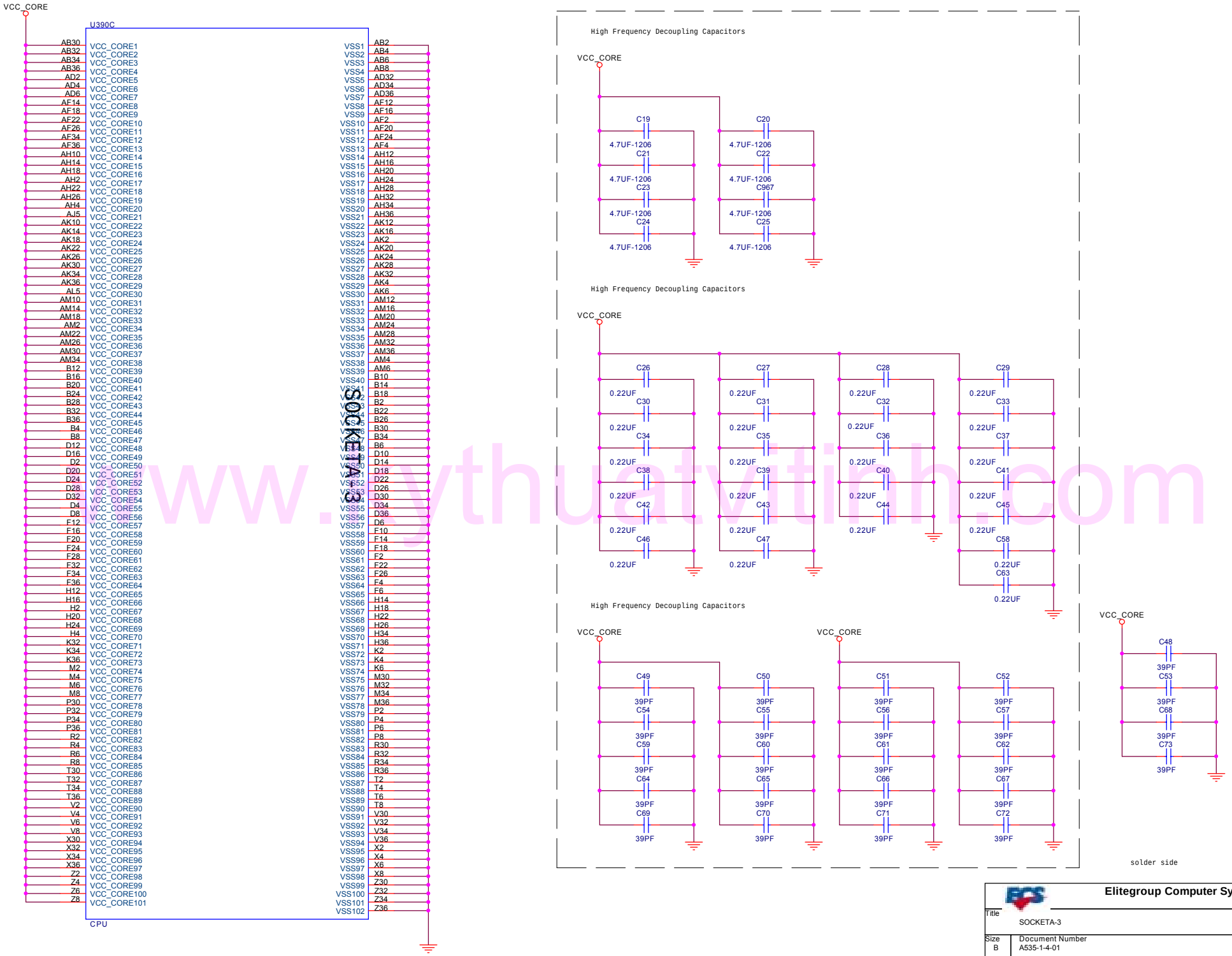
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Title: SOCKETA-2

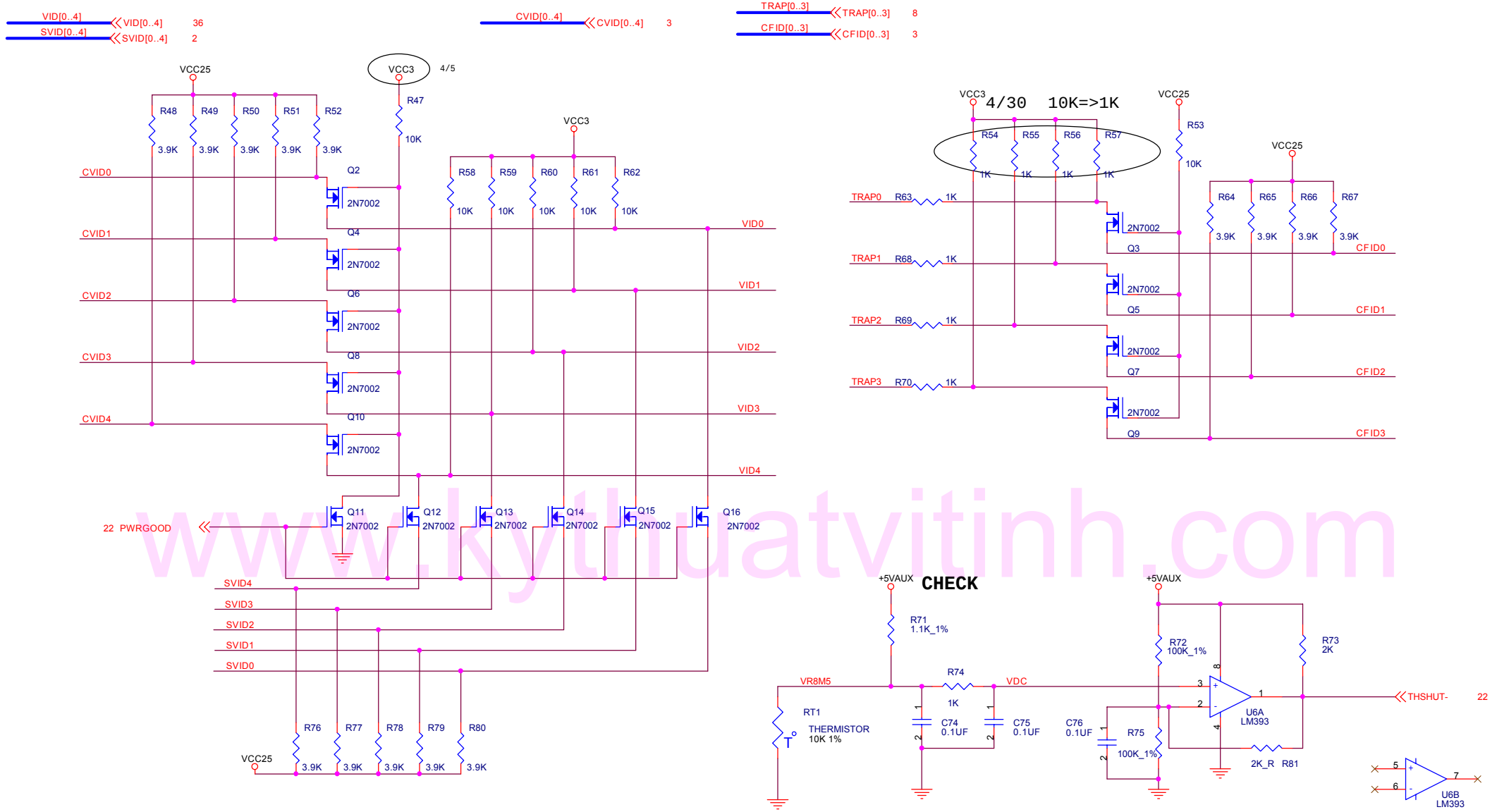
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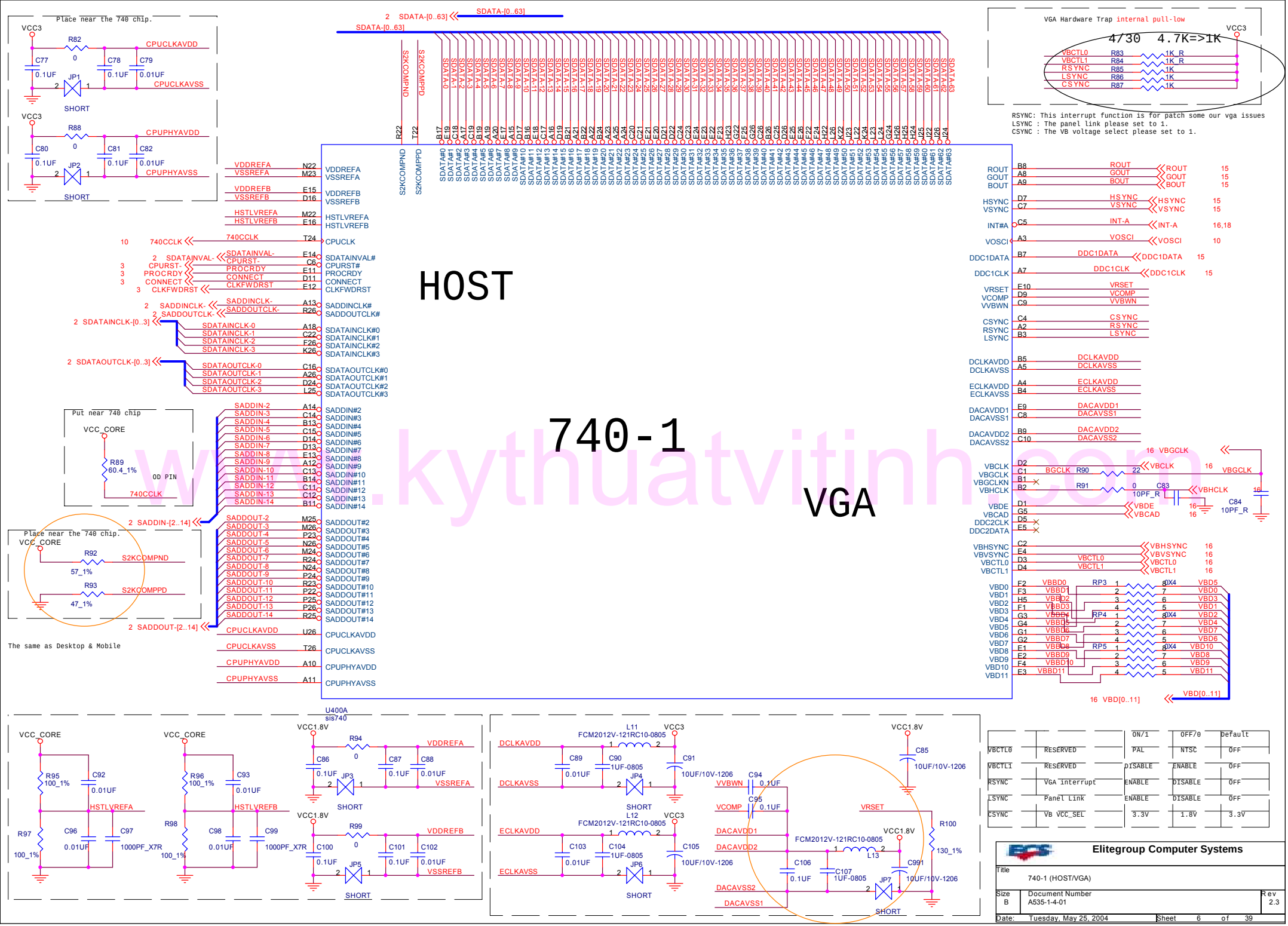
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Title: SOCKETA-3		
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		ON/1	OFF/0	Default
VBCTL0	ReSERVED	PAL	NTSC	OFF
VBCTL1	ReSERVED	DISABLE	ENABLE	OFF
RSYNC	VGa Interrupt	ENABLE	DISABLE	OFF
LSYNC	Panel Link	ENABLE	DISABLE	OFF
CSYNC	Vb VCC_SEL	3.3V	1.8V	3.3V

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Title	740-1 (HOST/VGA)	
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Near to DDR module

Series Resistances can swap by layout result

DDR MODULE TO DDR SELL ABOUT 2"

DMD[0..63] DMD[0..63] 12,13,14

DDQM[0..7] /RDQM[0..7] 12,13,14

DDQS[0..7] /RDQS[0..7] 12,13,14

DMAA[0..14] /RMA[0..14] 12,13,14

Near to DDR module

DDR MODULE TO DDR SELL ABOUT 2"

4/10

740-2

sis740

U400B

For SDR DRAM Clock input pin

Put near 740 chip.

Put near 740 chip.

SHORT

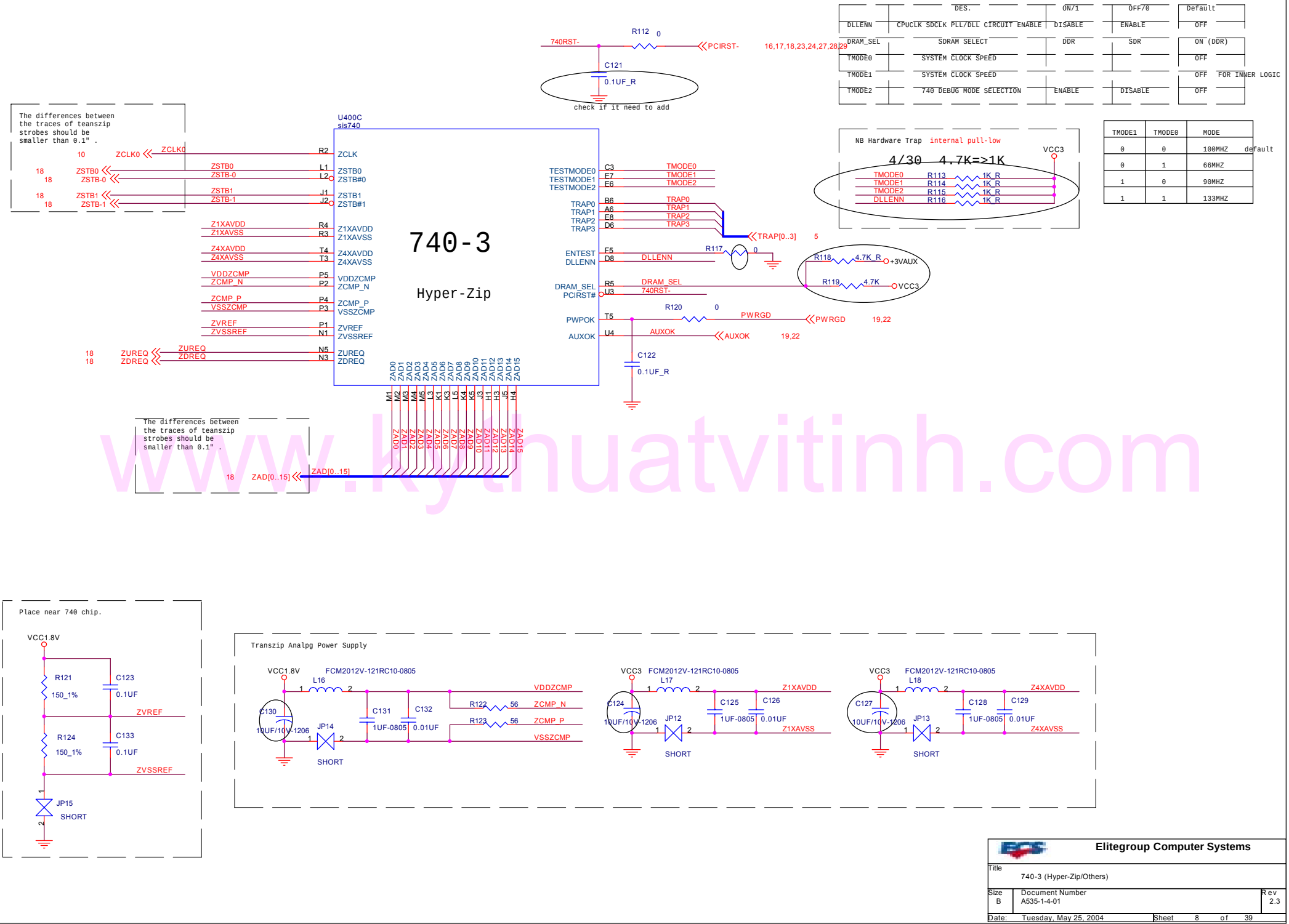
SHORT

SHORT

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Title	740-2 (MEMORY for DDR)	
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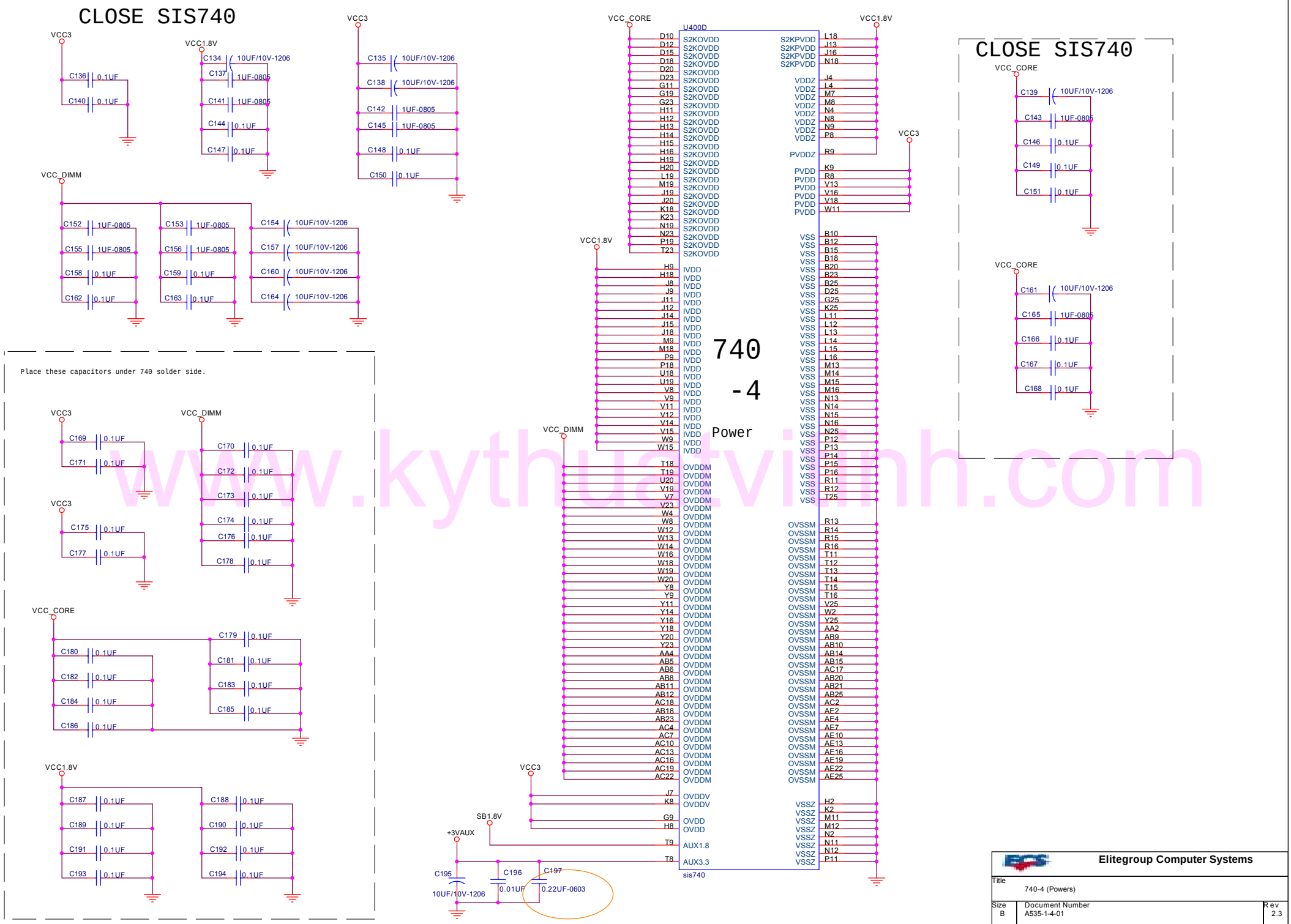
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Title: 740-3 (Hyper-Zip/Others)

Size: B | Document Number: A535-1-4-01 | Rev: 2.3

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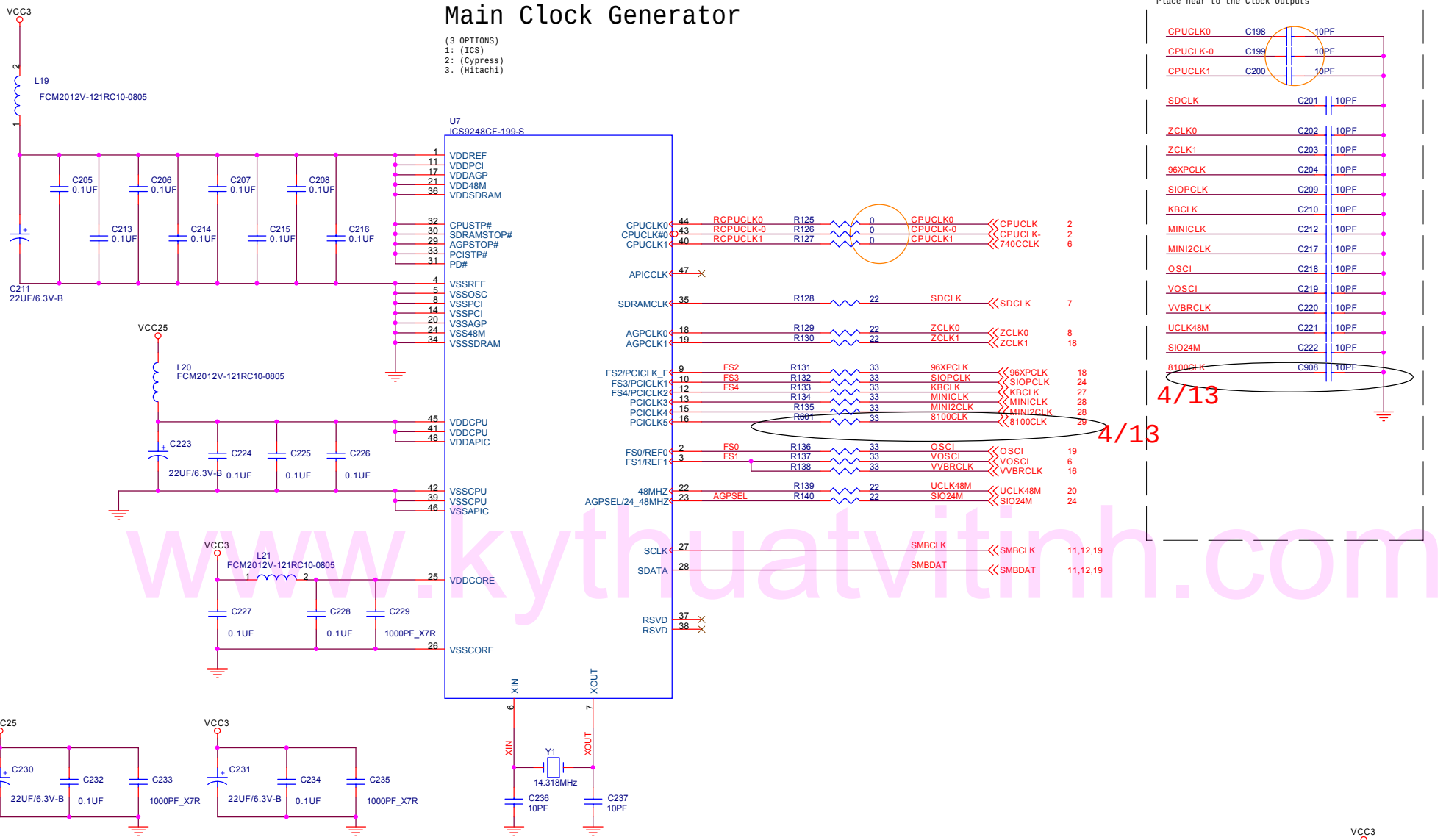


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Title: 740-4 (Powers)		
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Main Clock Generator

(3 OPTIONS)
1: (ICS)
2: (Cypress)
3. (Hitachi)



By-Pass Capacitors
Place near to the Clock Outputs

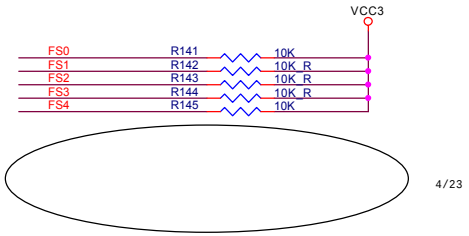
4/13

4/13

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24_48MHz has internal pull-up of 120K to VCC3

FS[0..4], AGPSEL, PCI_STOP#, CPU_STOP#, SDRAM_STOP#, AGP_STOP# have internal pull-down of 120K to GND



4/23

SIS740 CLOCK							AGPCLK (MHz)		
(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	AGPSEL=0	AGPSEL=1	
0	0	0	0	66.6	66.6	33.3	66.6	50	BIOS DEFAULT
0	0	0	1	100	100	33.3	66.6	50	
0	0	1	0	166	166	33.3	66.6	55.6	
0	0	1	1	133	133	33.3	66.6	50	
0	1	0	0	66.6	100	33.3	66.6	50	
0	1	0	1	100	66.6	33.3	66.6	50	
0	1	1	0	100	133	33.3	66.6	50	
0	1	1	1	133	100	33.3	66.6	50	
1	0	0	0	112	112	33.6	67.2	56	
1	0	0	1	124	124	31	62	46.5	
1	0	1	0	138	138	34.5	69	51.8	
1	0	1	1	150	150	30	60	50	
1	1	0	0	66.6	133	33.3	66.6	49.84	
1	1	0	1	133	166	33.3	66.6	55.3	
1	1	1	0	150	100	30	60	50	
1	1	1	1	160	120	30	60	48	

NOTE:
PCICLK<34.5MHz

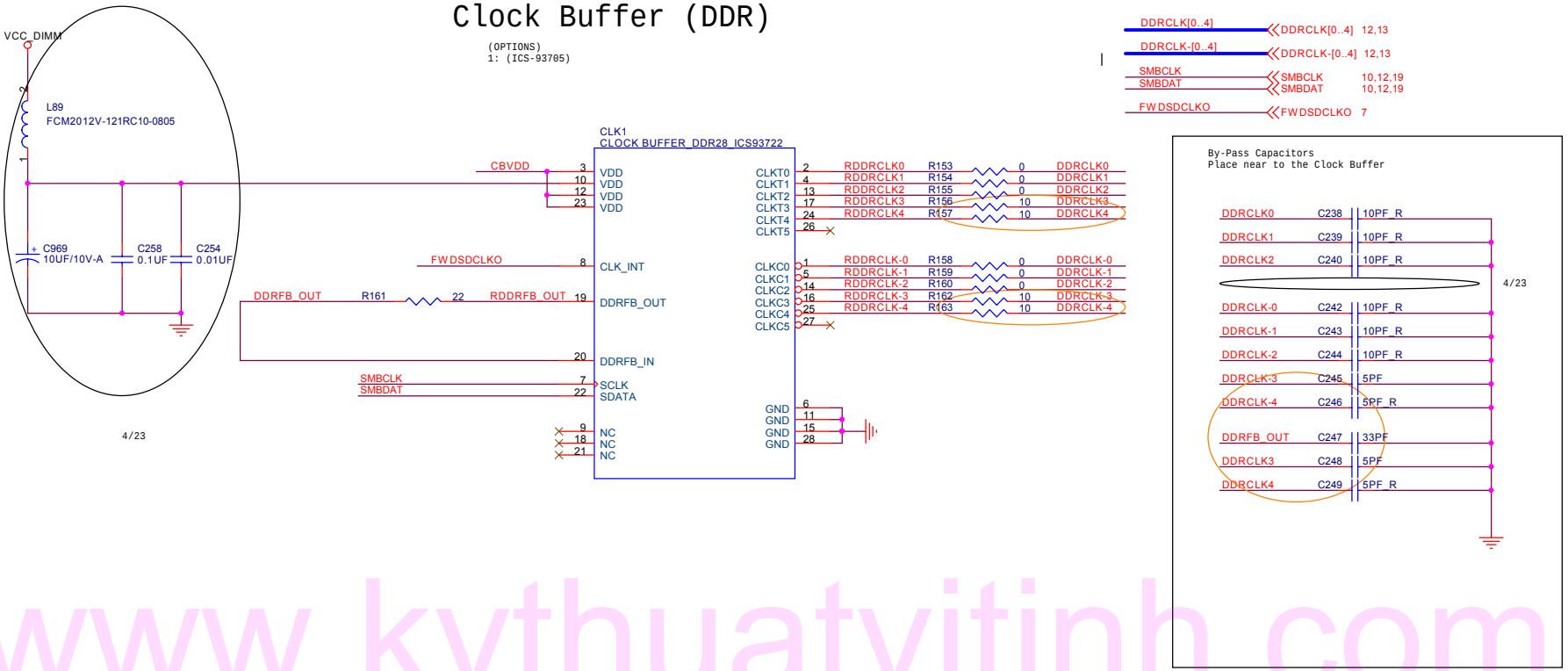
Elitegroup Computer SystemS

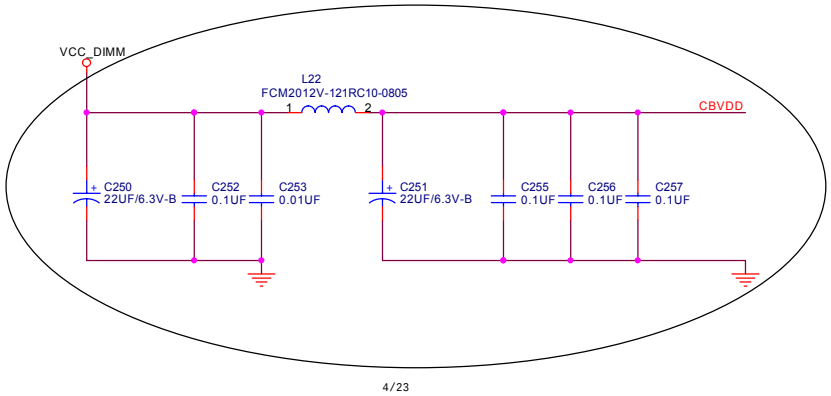
Title: CLOCK GENERATOR

Size: B | Document Number: A535-1-4-01 | Rev: 2.3

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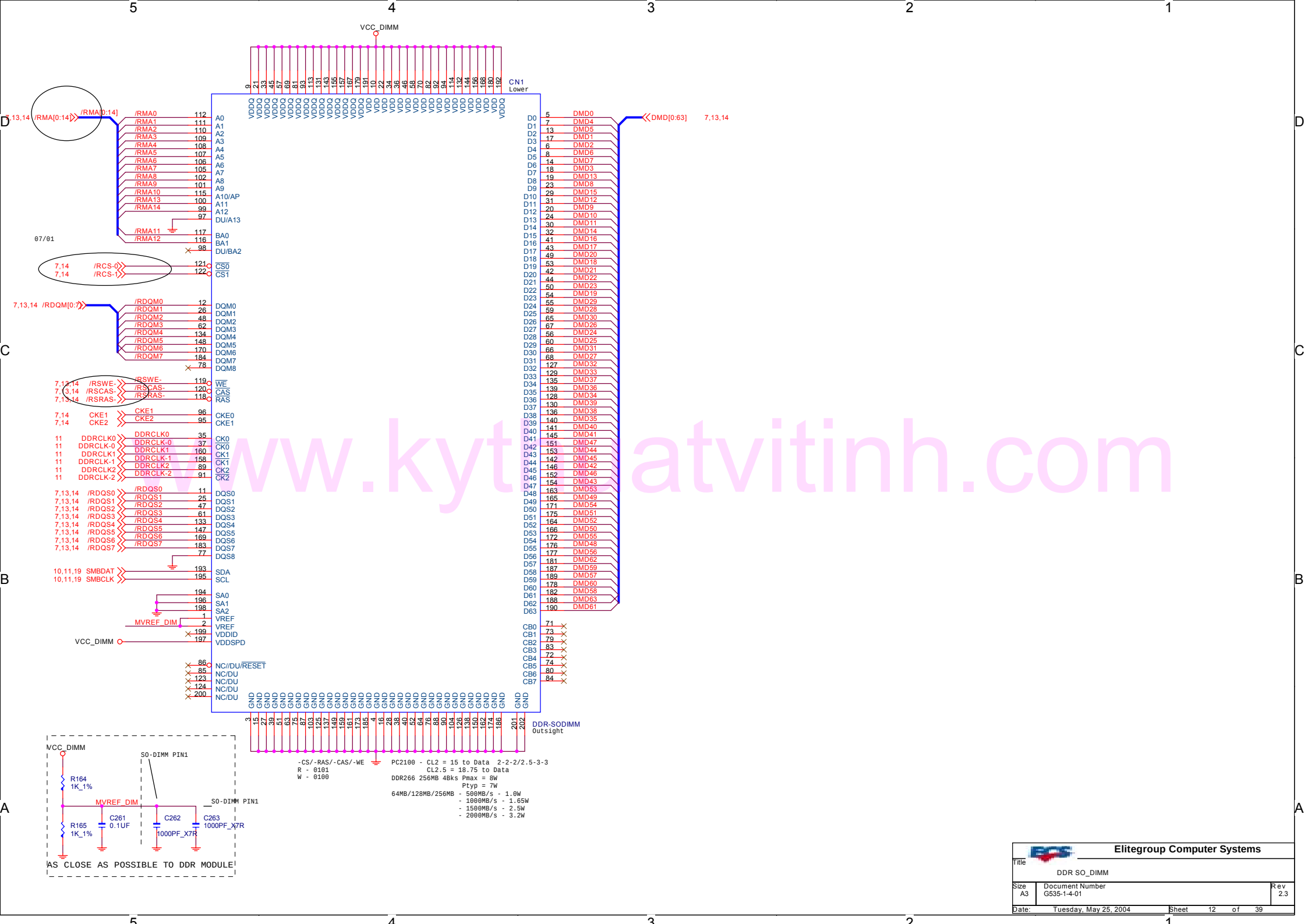
Clock Buffer (DDR)





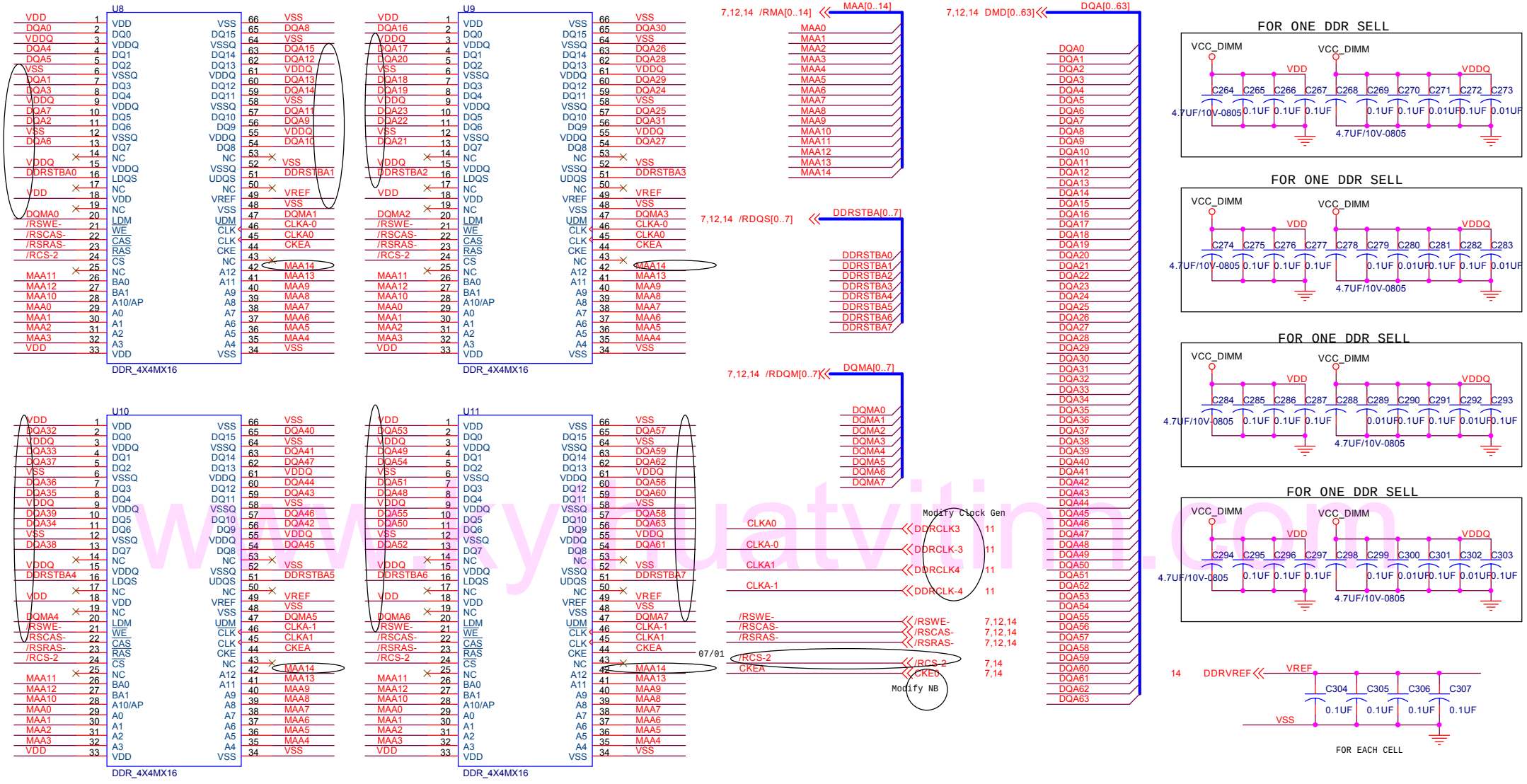
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Title: CLOCK BUFFER FOR DDR		
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Title: DDR SO_DIMM		
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SO-DIMM no "WP" pin

SSTL-2 Termination Resistors

	SDR	Rs	DDR	Rs	Rtt
MD/DQM(/DQS)	LV-CMOS	0/10/-	SSTL-2	10	47
MA/Control	LV-CMOS	10	SSTL-2	0	47
CS	LV-CMOS	0	SSTL-2	0	47
CKE	DD 3.3V		DD 2.5V		

Control signals can NOT be placed within the same RPs as data , strobe , or command signals

DMD[0..63] DMD[0..63] 7,12,13
/RDQM[0..7] /RDQM[0..7] 7,12,13
/RDQS[0..7] /RDQS[0..7] 7,12,13
/RMA[0..14] /RMA[0..14] 7,12,13
/RCS-[0..1] /RCS-[0..1] 7,12

DDR_VTT

RP33: DMD0 DMD4 DMD5 DMD1 — RP35: DMD3 DMD7 DMD2 DMD6 — RP36: DMD13 DMD12 DMD15 DMD8 — RP38: DMD10 DMD9 DMD11 DMD14 — RP41: DMD16 DMD17 DMD20 DMD18 — RP42: DMD19 DMD23 DMD22 DMD21 — RP44: DMD29 DMD28 DMD26 DMD30 — RP45: DMD27 DMD31 DMD25 DMD24 — RP47: DMD32 DMD33 DMD37 DMD36 — RP48: DMD35 DMD39 DMD34 DMD38 — RP50: DMD44 DMD47 DMD41 DMD40 — RP51: DMD45 DMD42 DMD46 DMD43 — RP52: DMD53 DMD49 DMD54 DMD51 — RP53: DMD48 DMD55 DMD50 DMD52 — RP55: DMD61 DMD63 DMD58 DMD60 — RP56: DMD56 DMD62 DMD59 DMD57

/DQM0 R663 47
/DQS0 R664 47
/DQM1 R665 47
/DQS1 R666 47
/DQM3 R667 47
/DQS3 R668 47
/DQM2 R669 47
/DQS2 R670 47
/DQM4 R671 47
/DQS4 R672 47
/DQM5 R673 47
/DQS5 R674 47
/DQS7 R675 47
/DQM7 R676 47
/DQM6 R677 47
/DQS6 R678 47

DDR_VTT

RP31: /RMA3 /RMA2 /RMA1 /RMA0
RP34: /RMA7 /RMA6 /RMA5 /RMA4
R659 47 /RMA11
R660 47 /RMA10
R661 47 /RMA12
RP39: /RMA14 /RMA13 /RMA9 /RMA8

R657 47 /RCS-2 7,13
R658 47 /RCS-1 7,12
R679 47 /RCS-0 7,12

R681 47 /RSRAS- /RSRAS- 7,12,13
R682 47 /RSCAS- /RSCAS- 7,12,13
R683 47 /RSWE- /RSWE- 7,12,13

7/10

VCC_DIMM

RP32: CKE2 CKE0 CKE1 — 470X4

7,12 CKE2
7,13 CKE0
7,12 CKE1

check if it need to change to resisters

DDR_VTT

ADD 13 PCS 0.1UF

C970 C973 C977 C971 C974 C978 C981 C972 C975 C979 C982 C976 C980 — 0.1UF

DDR_VTT

DECOUPLING CAPACITOR FOR SSTL-2 END TERMIANTION VTT ISLAND
0603 Package placed within 300mils of VTT Termination R-packs

C317 C321 C325 C329 C318 C322 C326 C330 C314 C315 C319 C323 C327 — 0.1UF

DDR_VTT

C316 C320 C324 C328 C331 C332 — 0.1UF

DDR_VTT

C333 C337 C341 C334 C338 C342 C345 C335 C339 C343 C346 C336 C340 C344 — 0.1UF

DDR_VTT

C308 C310 C312 C309 C311 C313 — 0.1UF

every one "RPs" put two CAPs

0.1UF X 39 pcs

VCC_DIMM

DIMM DECOUPLING ; CLOSE TO DIMM

C361 C366 C371 C375 C380 C385 C386 C387 C390 C391 C392 C393 C394 C362 C367 C372 C376 C381 C363 C368 C373 C364 C369 C374 C377 C382 C365 C370 — 0.1UF

VCC_DIMM

DDRVREF GEN. & DECOUPLING

R173 75_1%
R174 75_1%
C383 0.01UF
C384 0.01UF
C388 0.01UF
C389 0.01UF
DDRVREF 13

DDR on board RAM

Add island plane

DDR_VTT

C378 470UF/10V-D
C379 470UF/10V-D

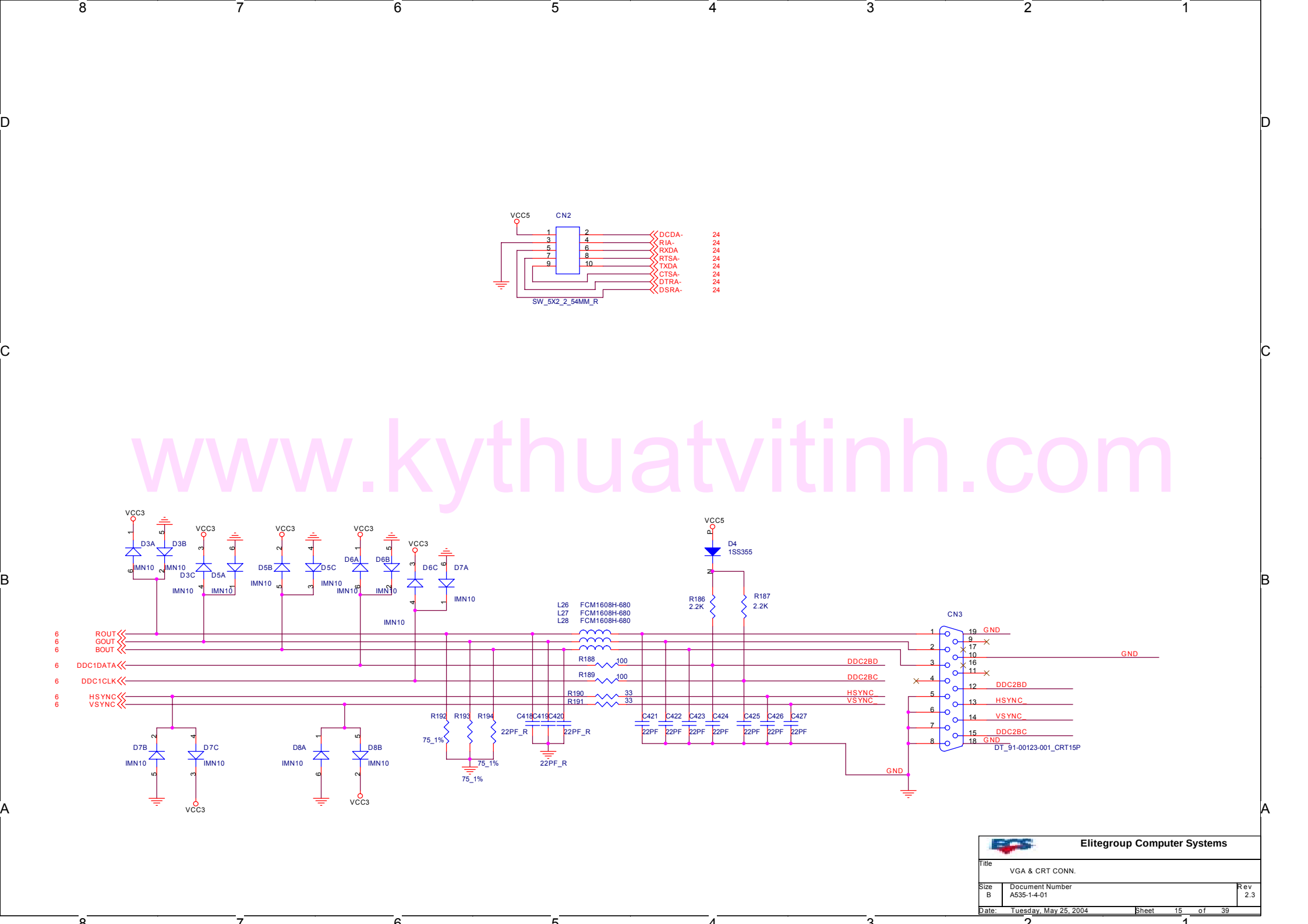
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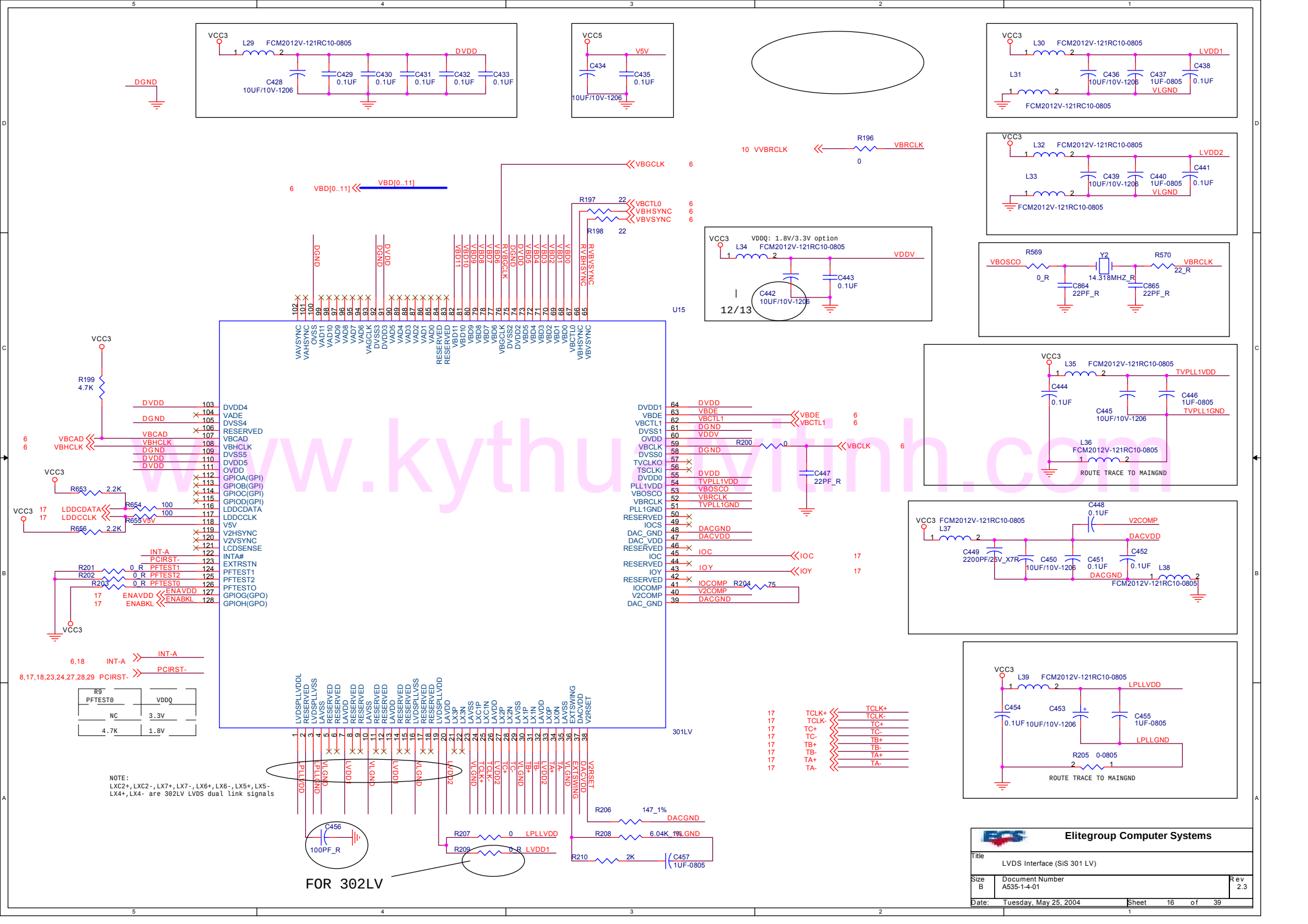
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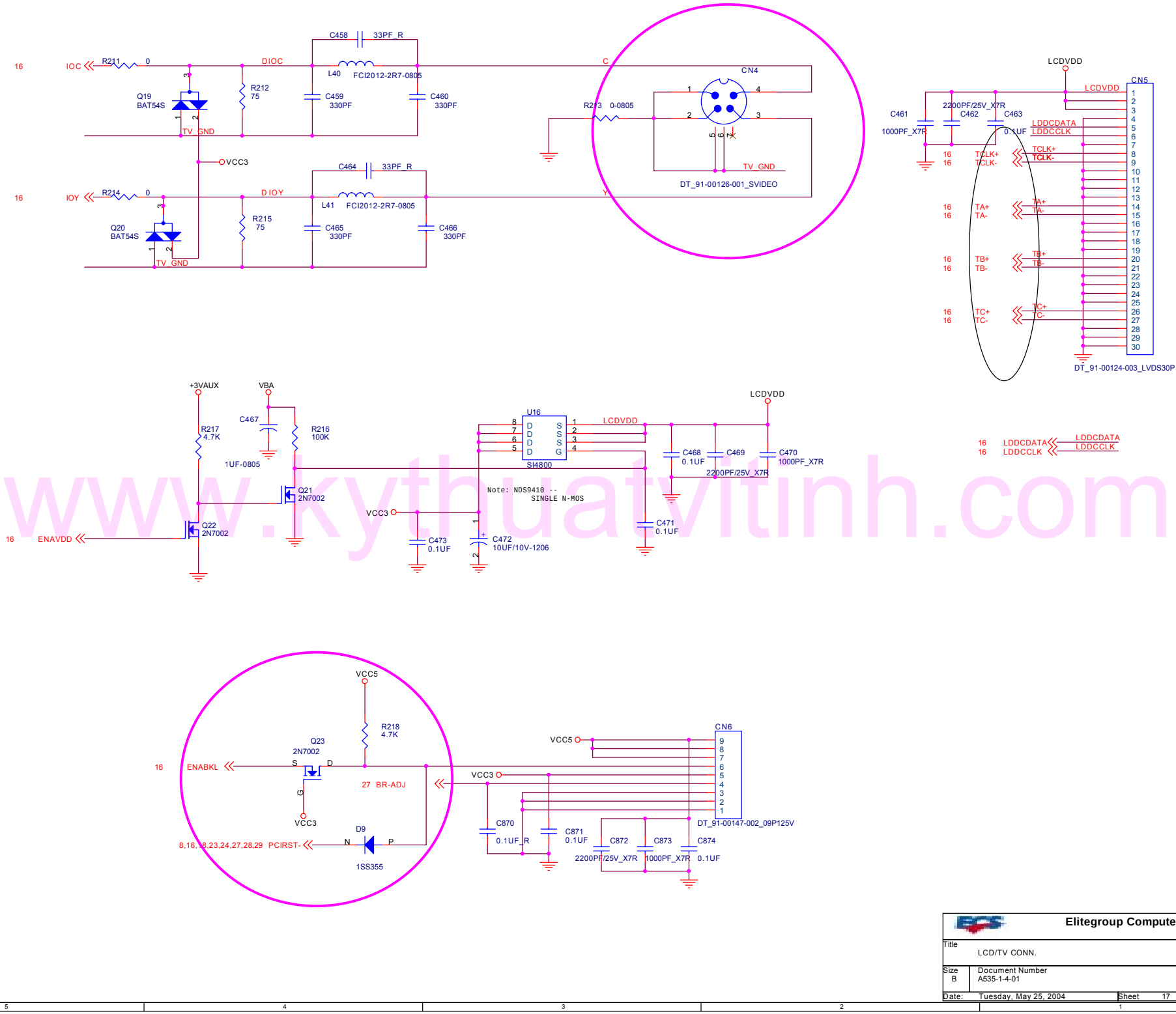


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Title: VGA & CRT CONN.		
Size: B	Document Number: A535-1-4-01	Rev: 2.3
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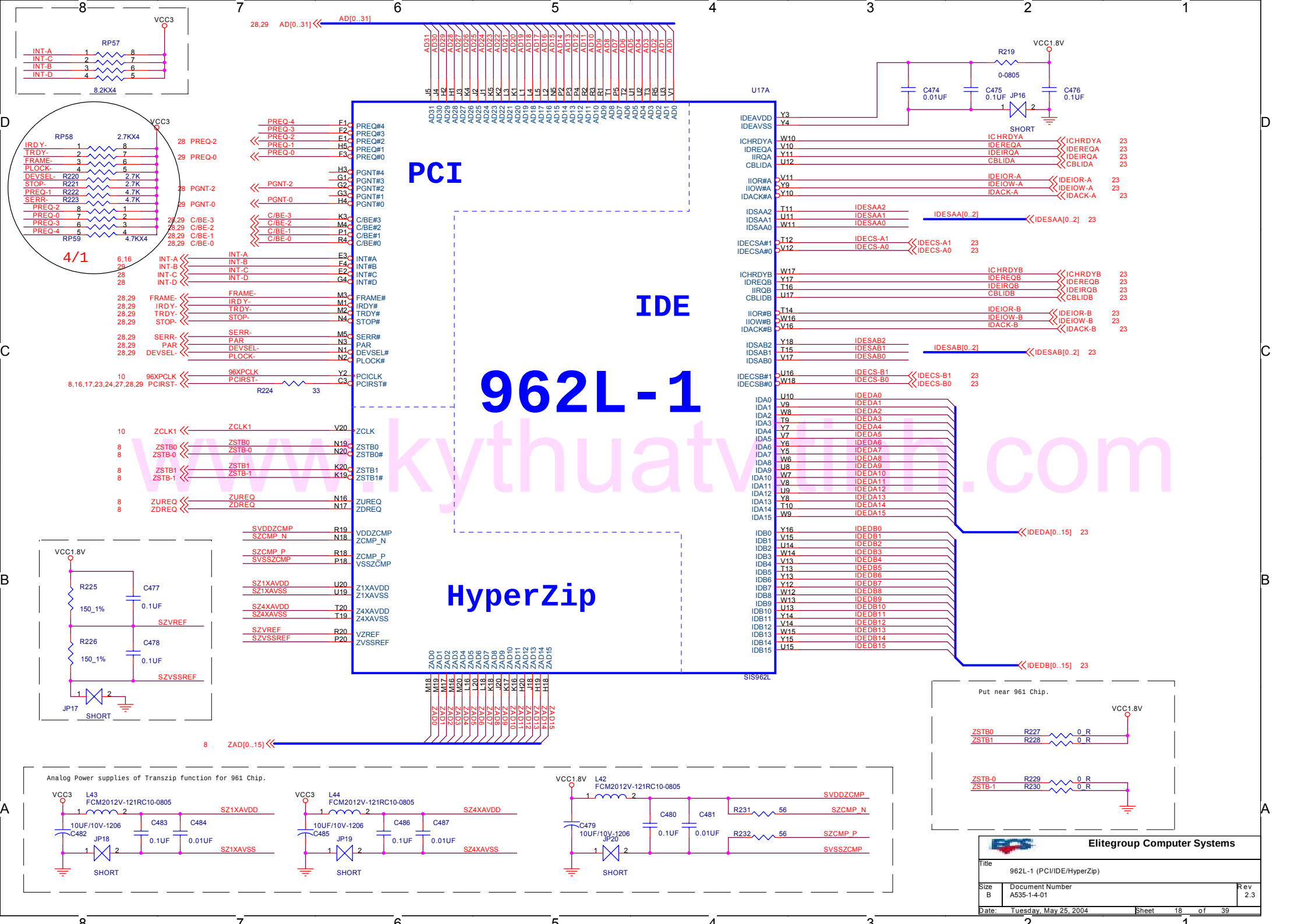


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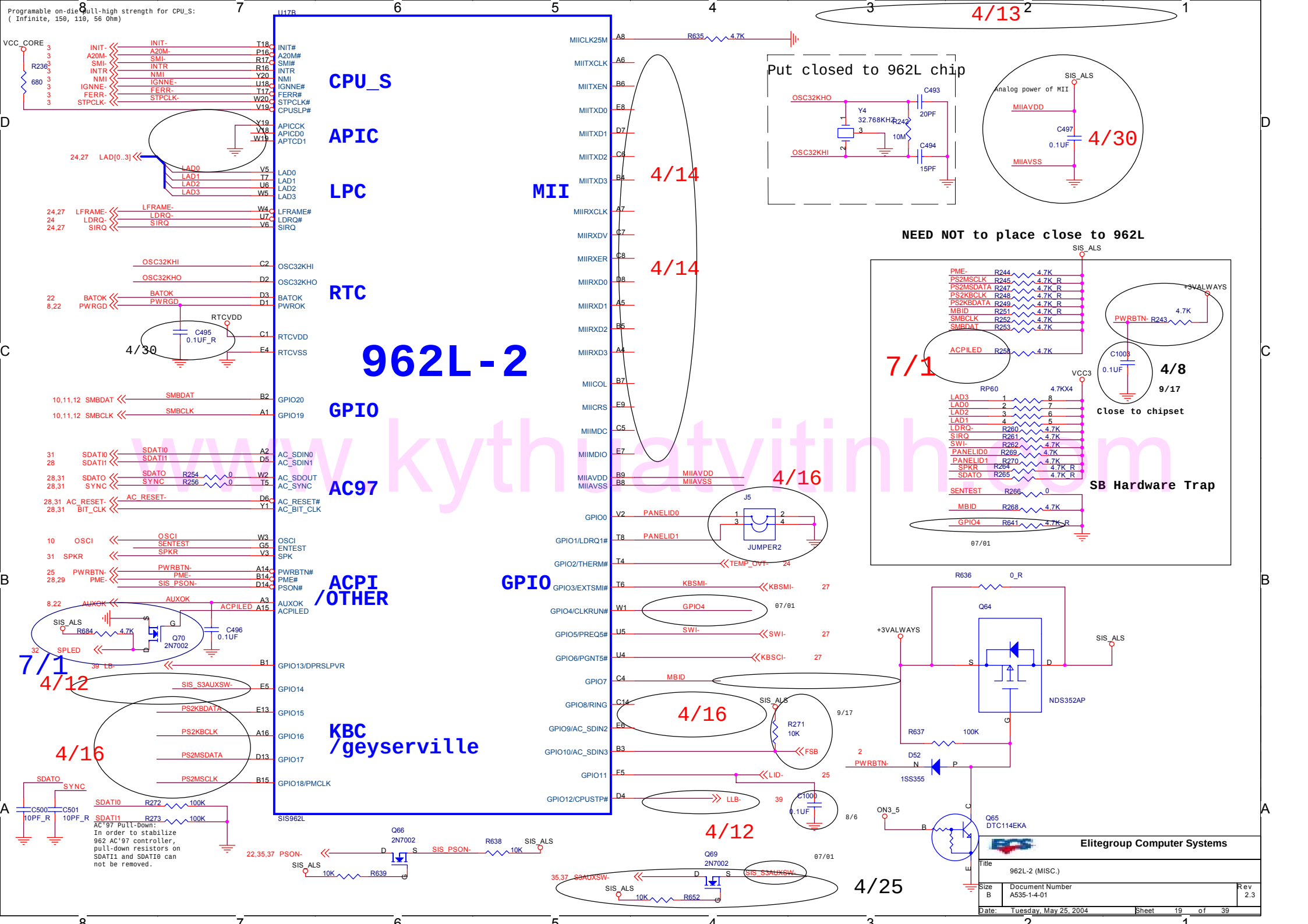


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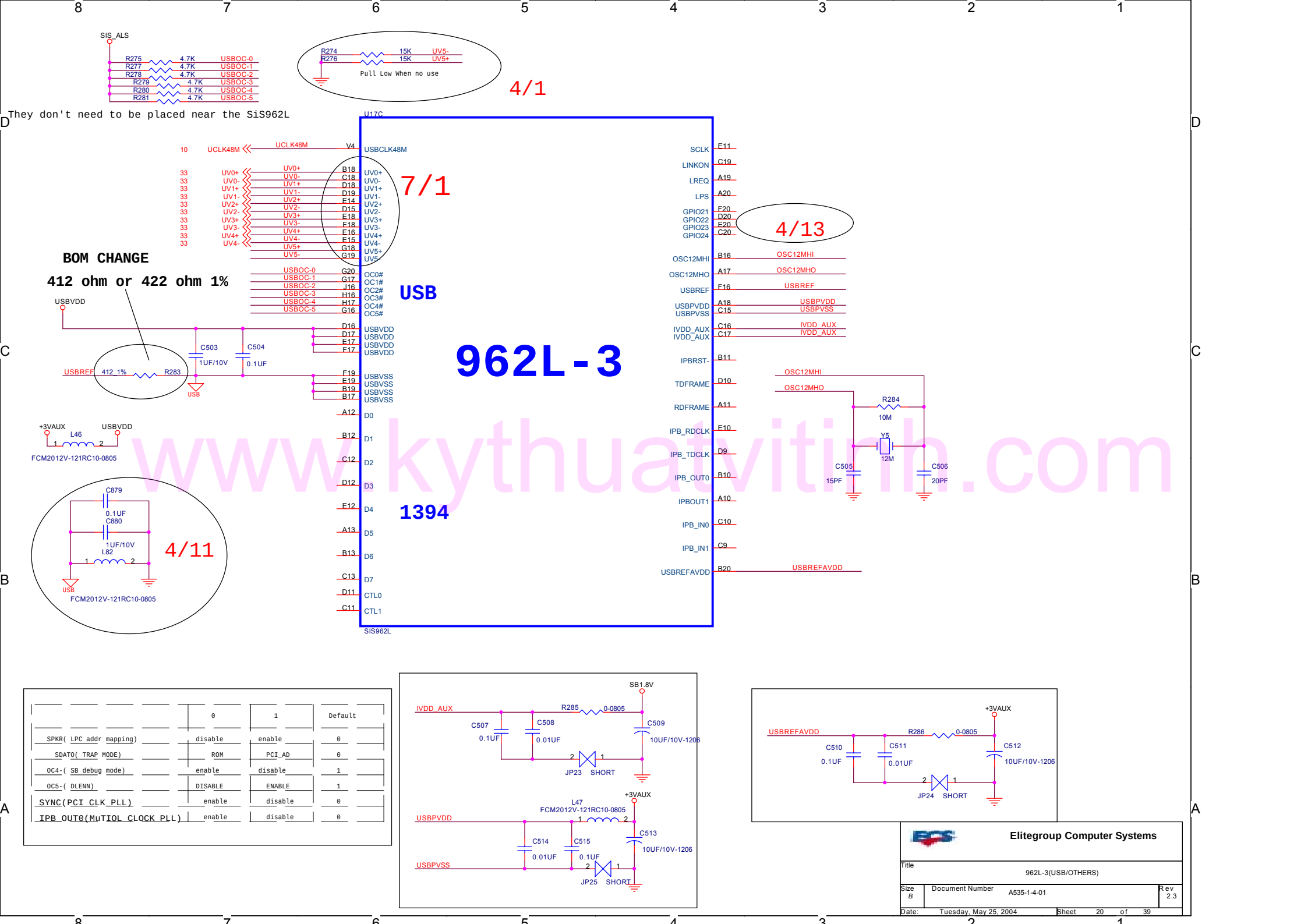
Elitegroup Computer Systems		
Title: LCD/TV CONN.		
Size: B	Document Number: A535-1-4-01	Rev: 2.3
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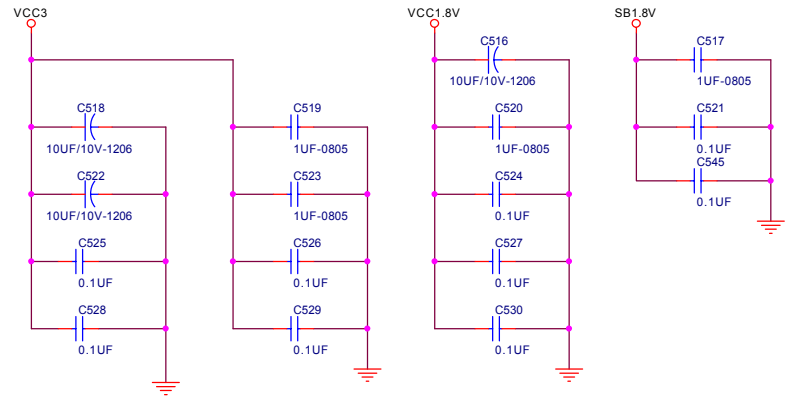


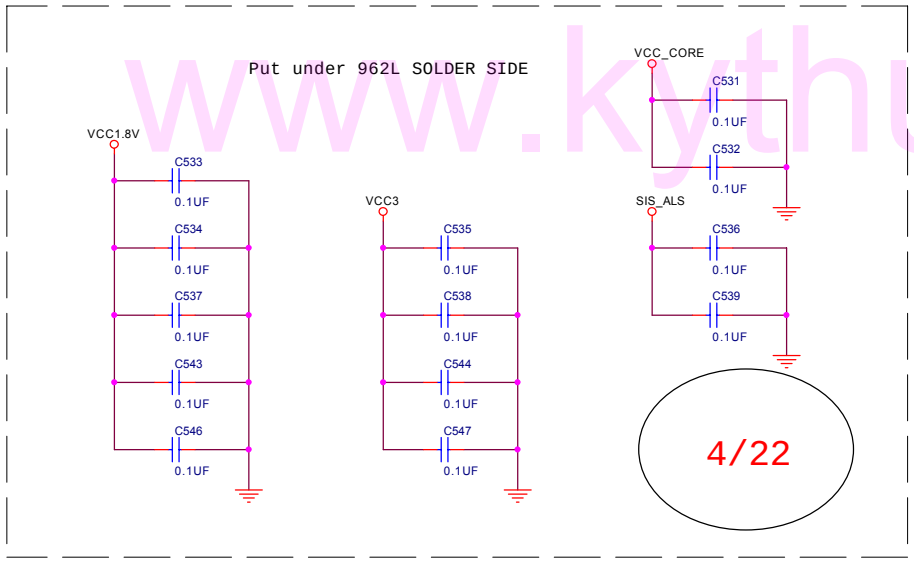
	0	1	Default
SPKR(LPC addr mapping)	disable	enable	0
SDAT0(TRAP MODE)	ROM	PCI_AD	0
OC4-(SB debug mode)	enable	disable	1
OC5-(DLENN)	DISABLE	ENABLE	1
SYNC(PCI CLK PLL)	enable	disable	0
IPB_OUT0(MuTIOL CLOCK PLL)	enable	disable	0

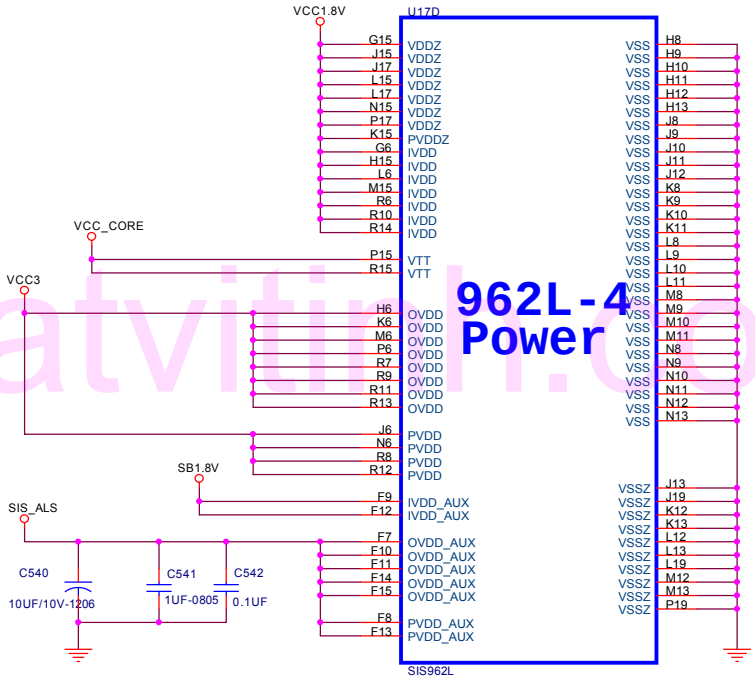
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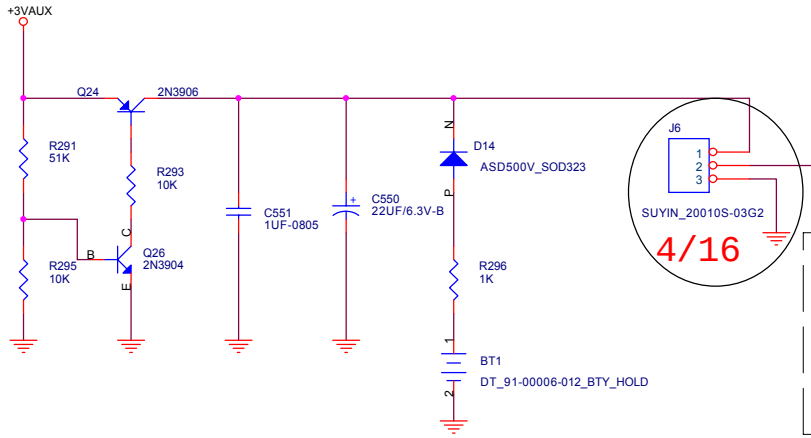


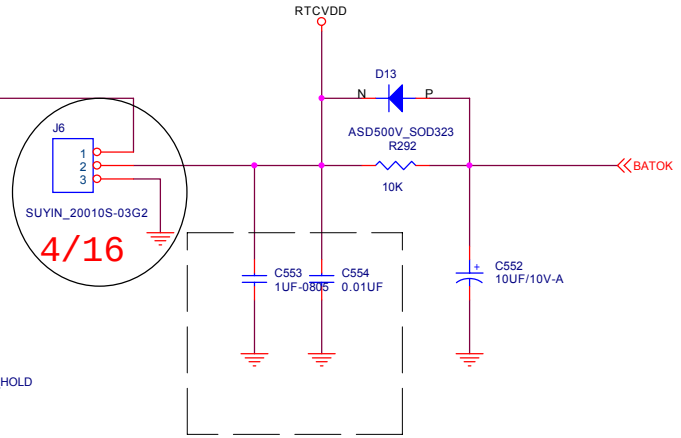
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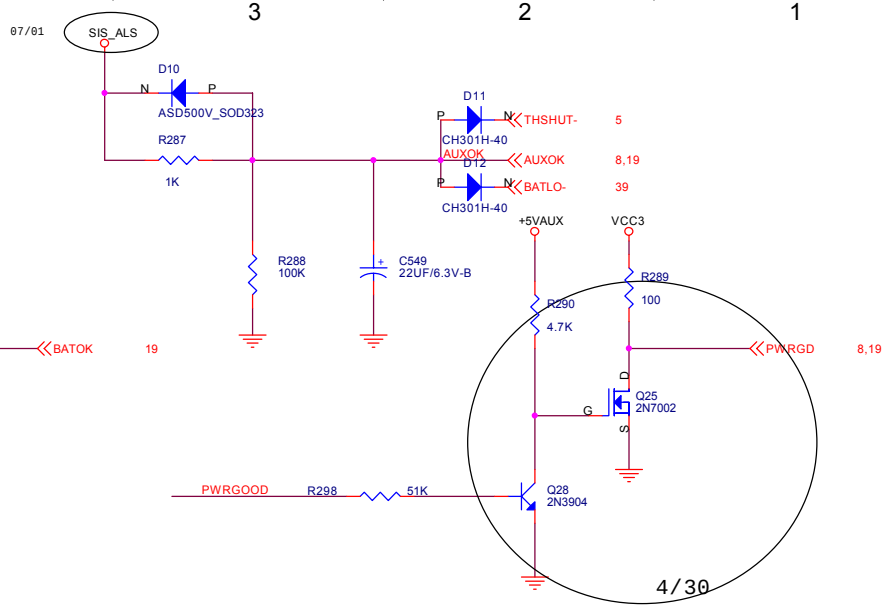
Elitegroup Computer Systems		
Title: 962L-4 (Powers)		
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RTC

NOTE!
1.The RTCVDD is 3V
2.Decoupling capacitor must be close to 962L RTCVDD pin.
3.RTC circuit must strictly follow SiS's recommended design
SiS is not responsible for RTC problems from foreign designs.

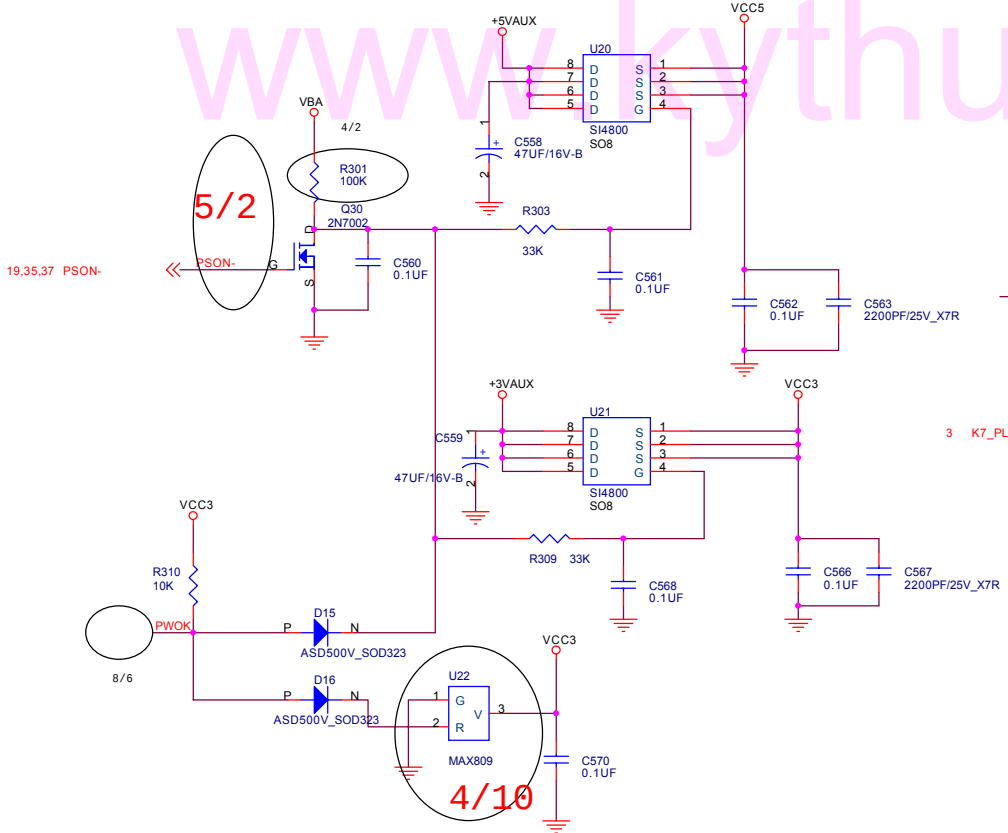


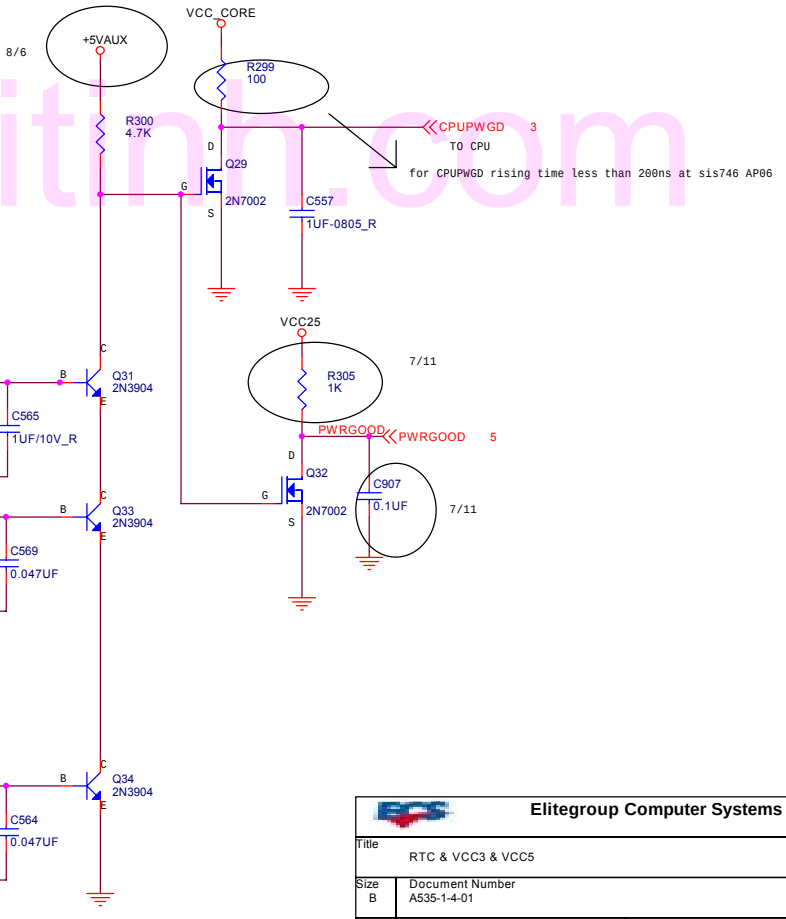




CONN---> LONGTRUMP_BH-8009G_RTC Place close to 962L

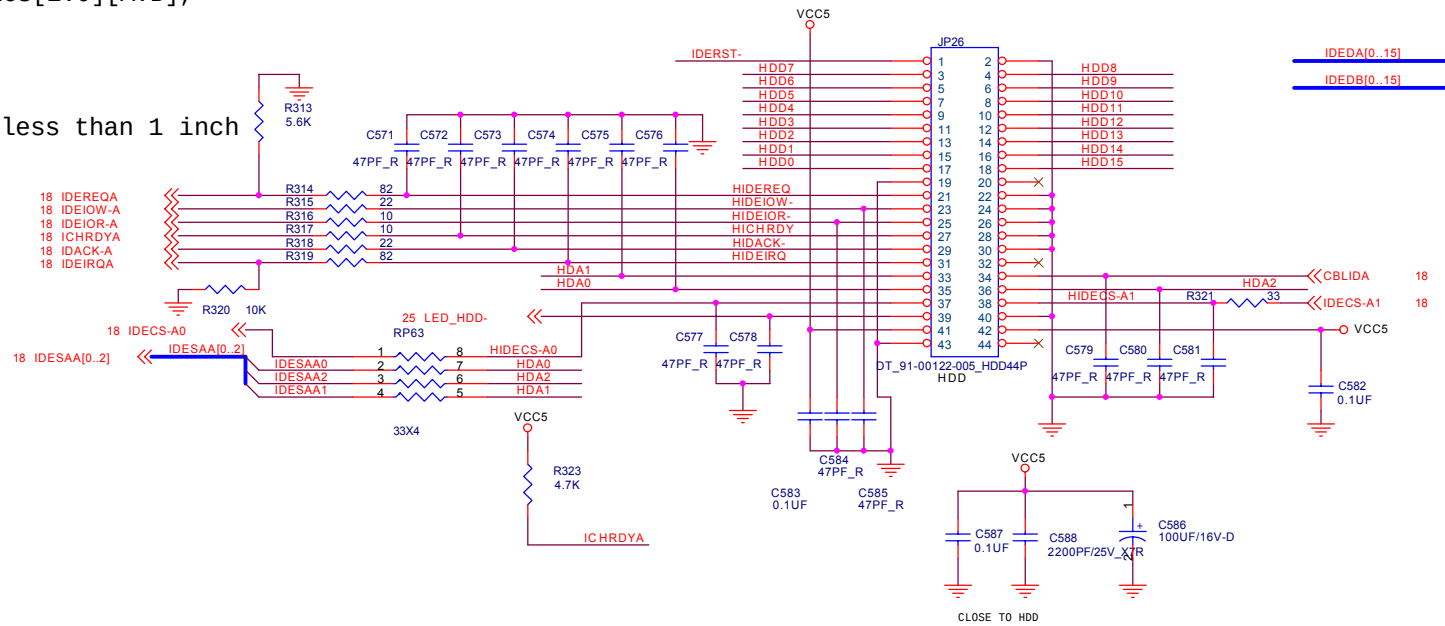
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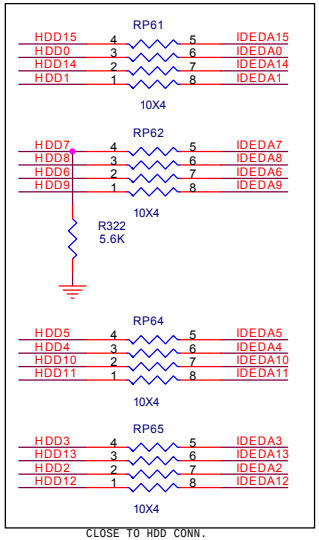




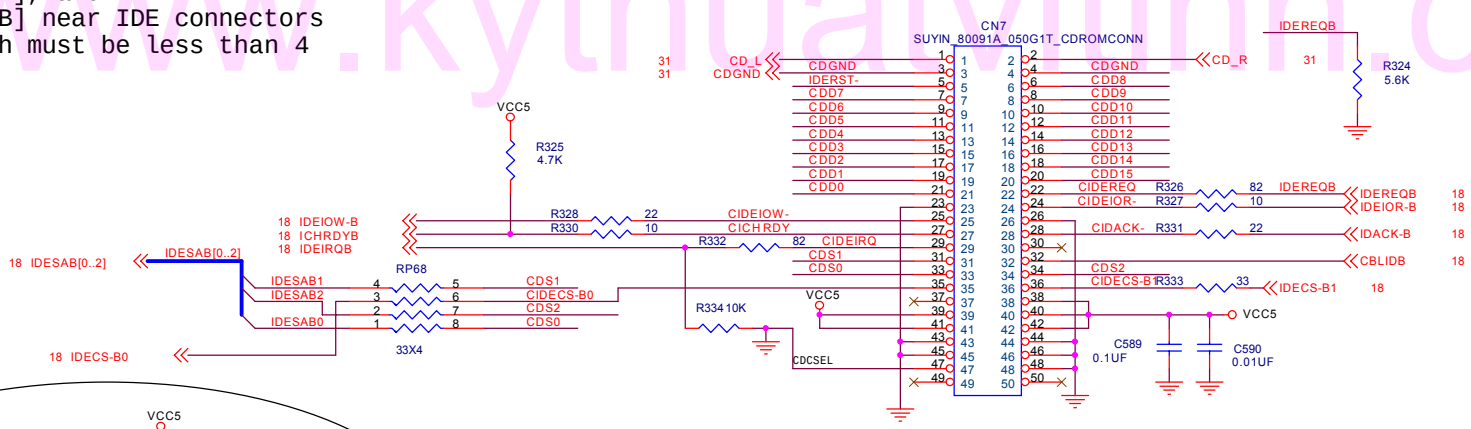
Elitegroup Computer Systems			
Title: RTC & VCC3 & VCC5			
Size: B	Document Number: A535-1-4-01		Rev: 2.3
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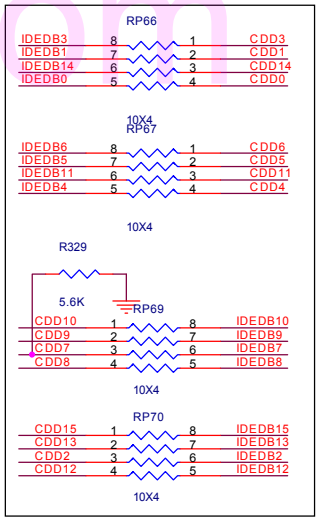
Place the damping resistors for
IDEA[2:0][A:B], IDECS[1:0][A:B],
IDEIOR[A:B]#,
IDEIOW[A:B]#, and
IDACK[A:B]# near
SiS962L
The length must be less than 1 inch

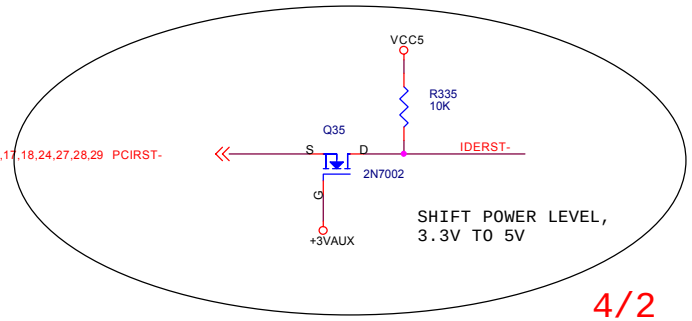




Place the damping resistors for
IDED[15:0][A:B], IDREQ[A:B],
ICHRDY[A:B], and
IDEIRQ[A:B] near IDE connectors
The length must be less than 4
inches

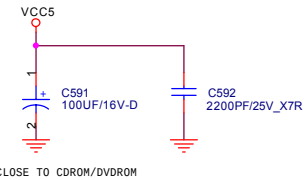






CSEL : "NC" ; "Hi" --> Master(CDROM)/Slave(DVDROM)

CSEL : "Low --> Slave(CDROM)/Master(DVDROM)



4/2

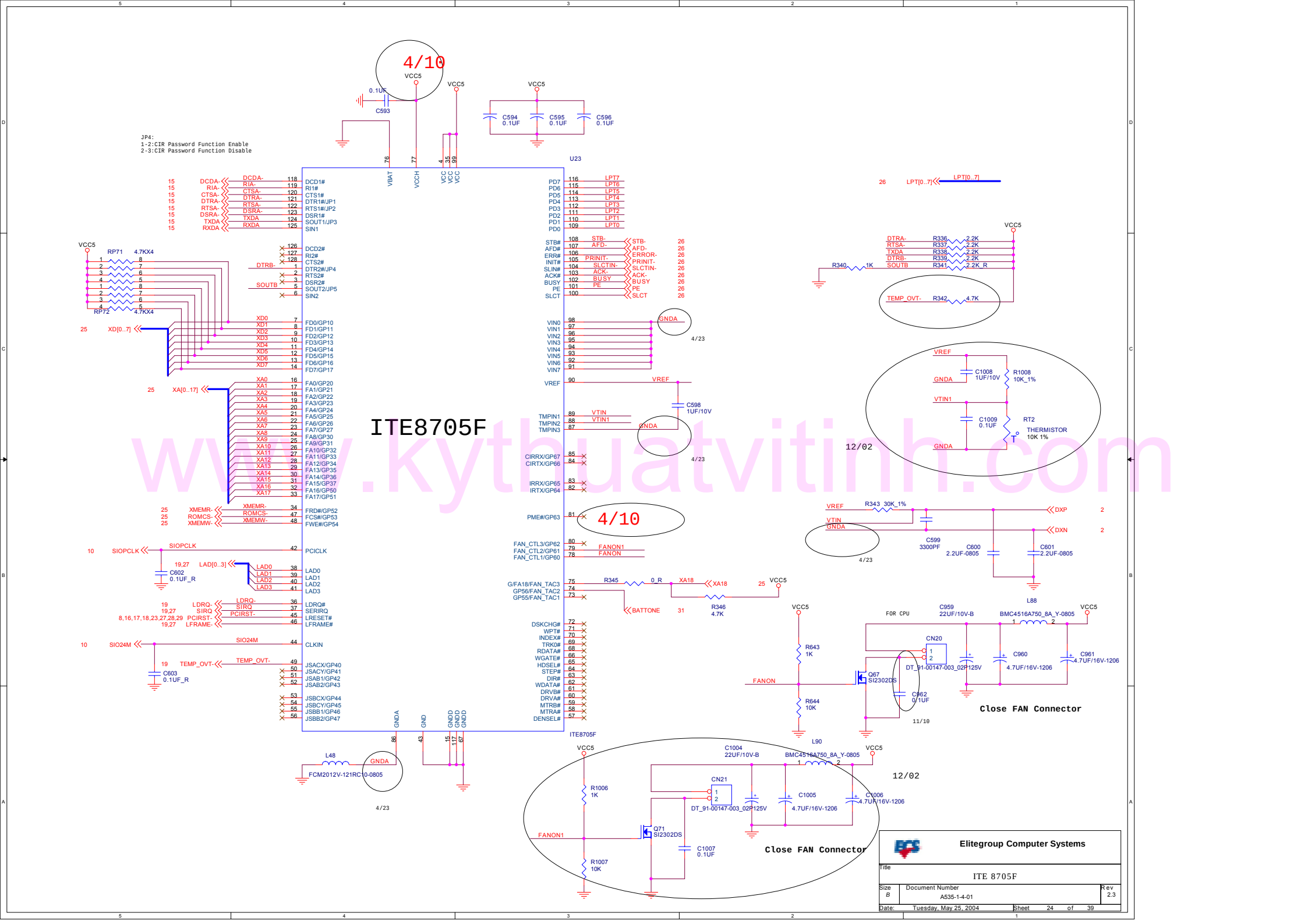
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Title: HDD & CDROM CONN.

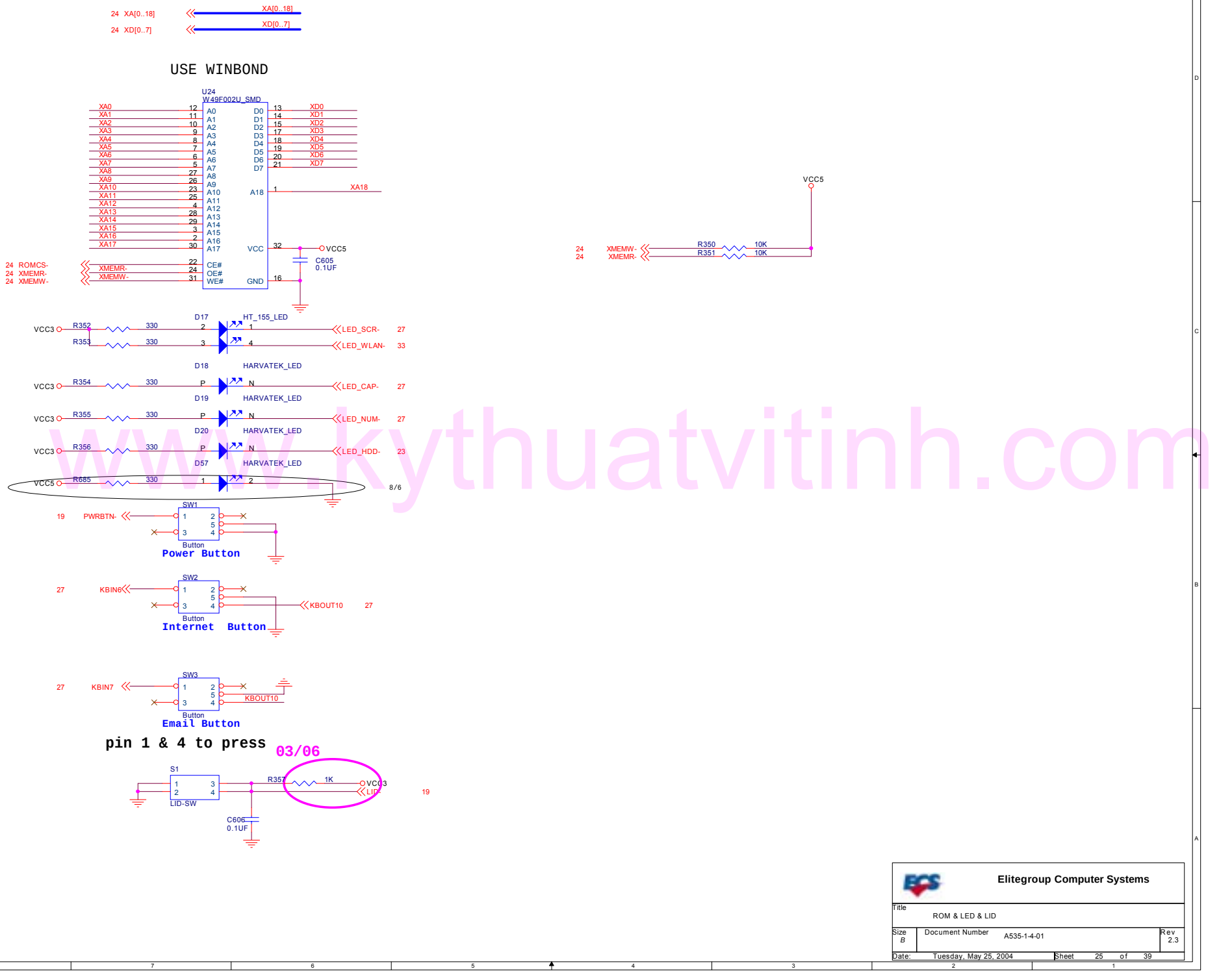
Size: B | Document Number: A535-1-4-01 | Rev: 2.3

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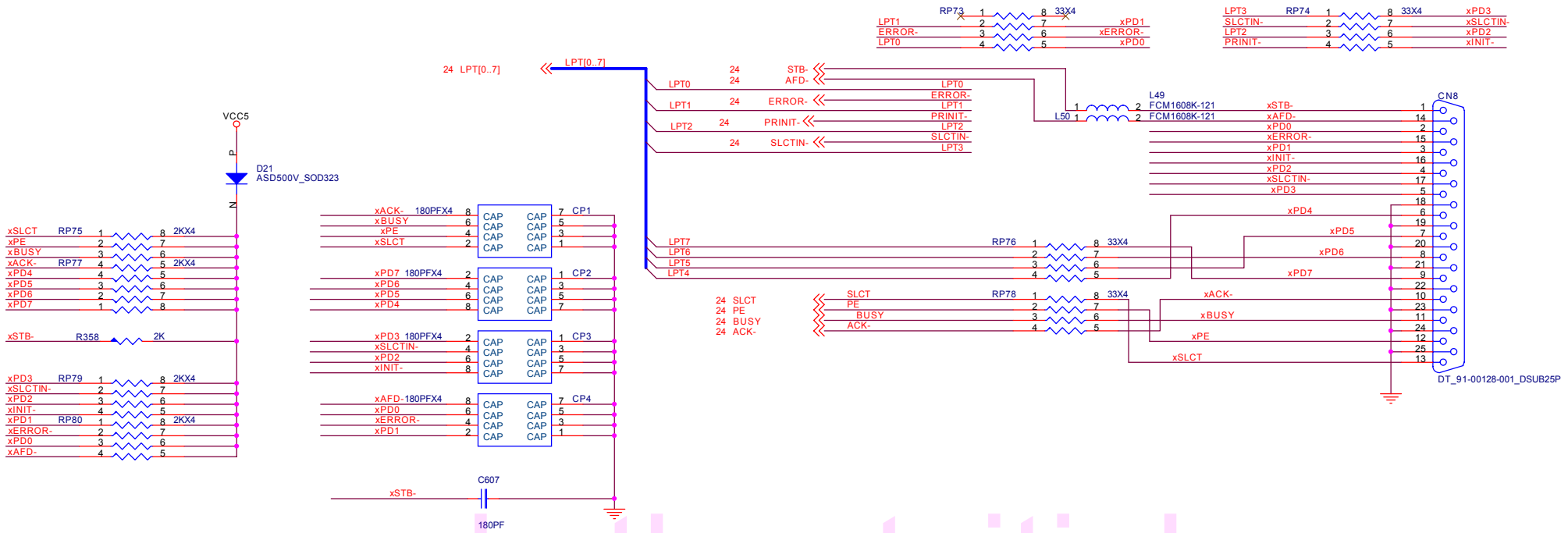


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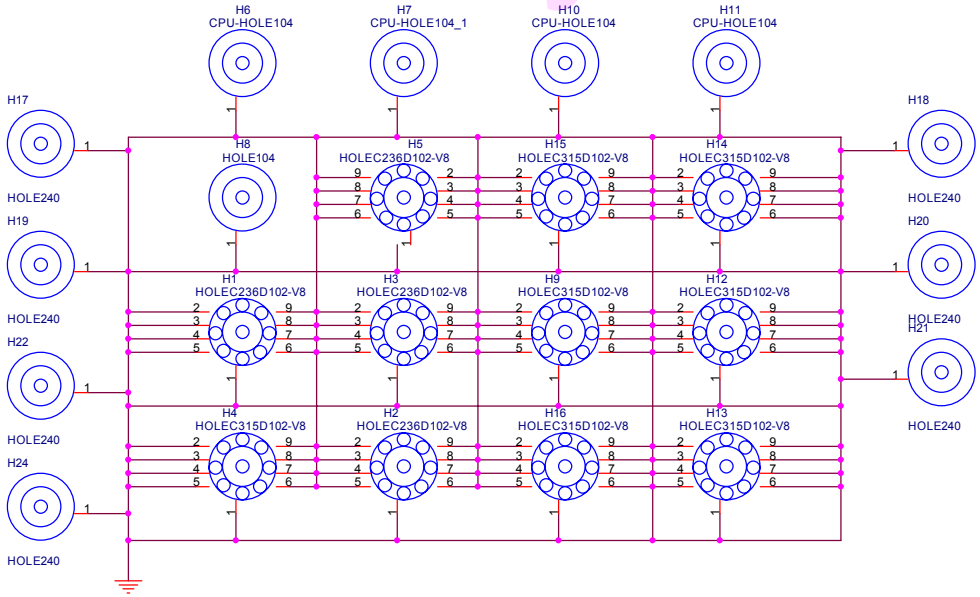


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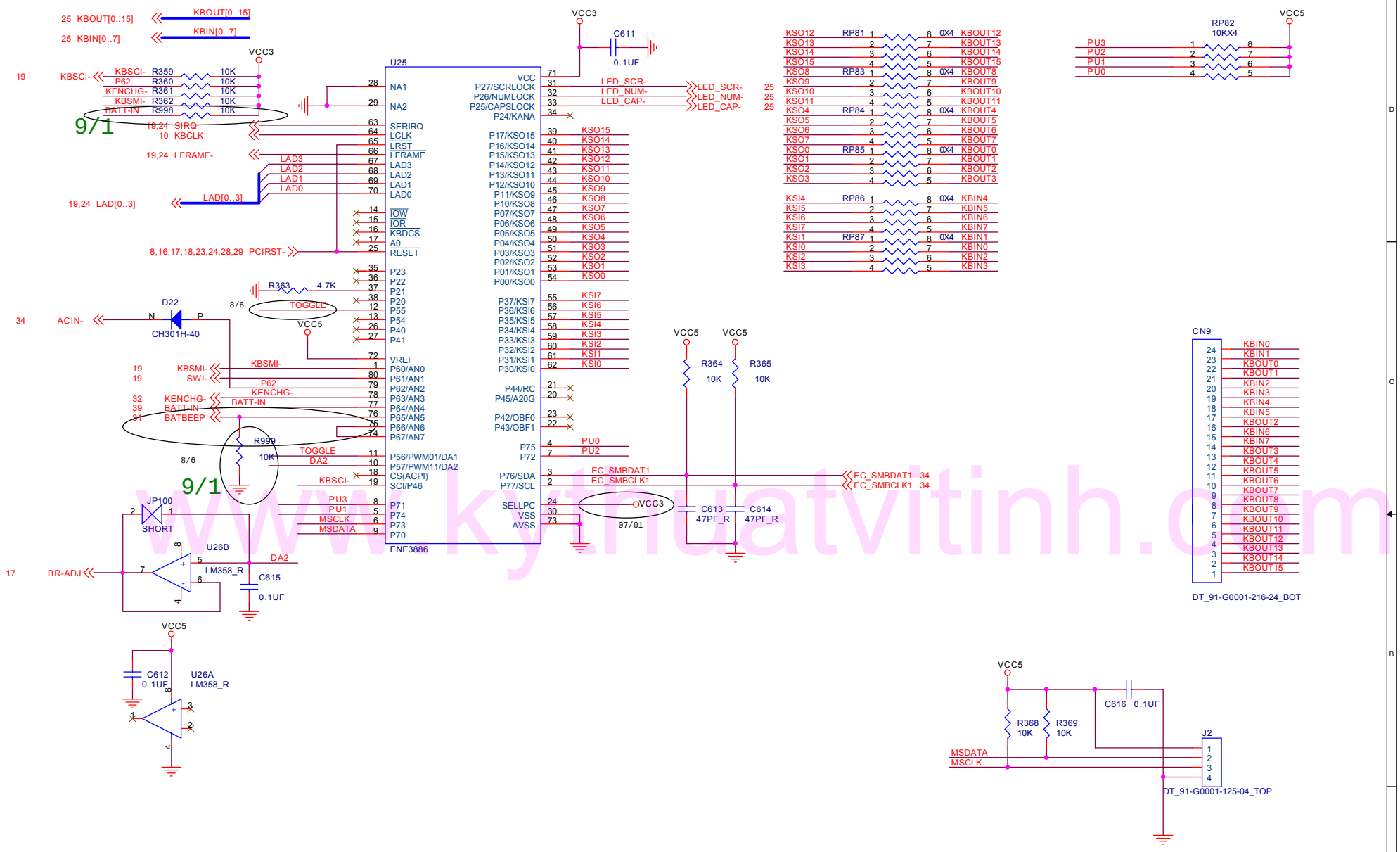
Elitegroup Computer Systems		
Title: ROM & LED & LID		
Size: B	Document Number: A535-1-4-01	Rev: 2.3
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Title: LPT PORT		
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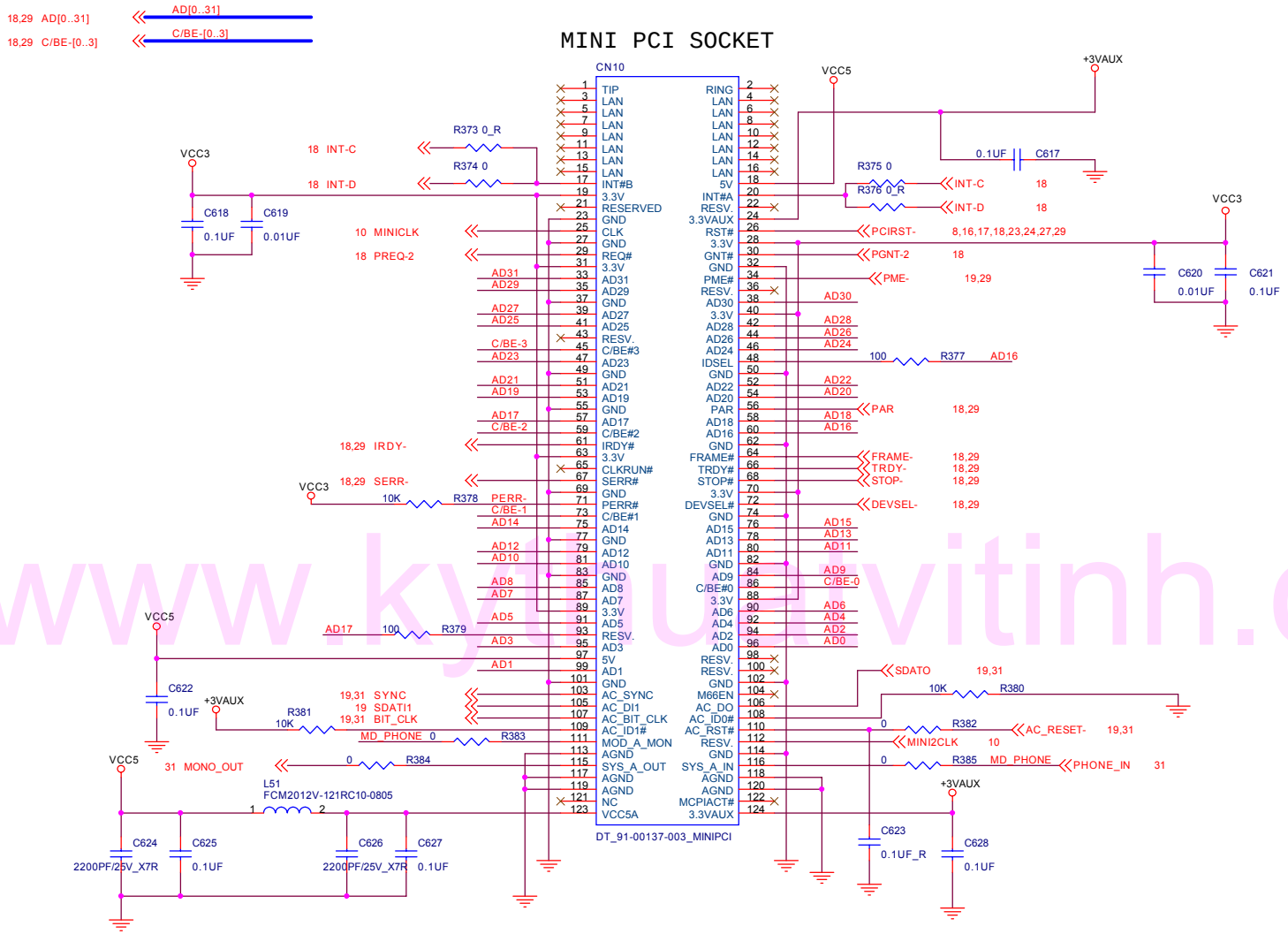
Elitegroup Computer Systems

Title: KBC & T/P

Size: Custom | Document Number: A535-1-4-01 | Rev: 2.3

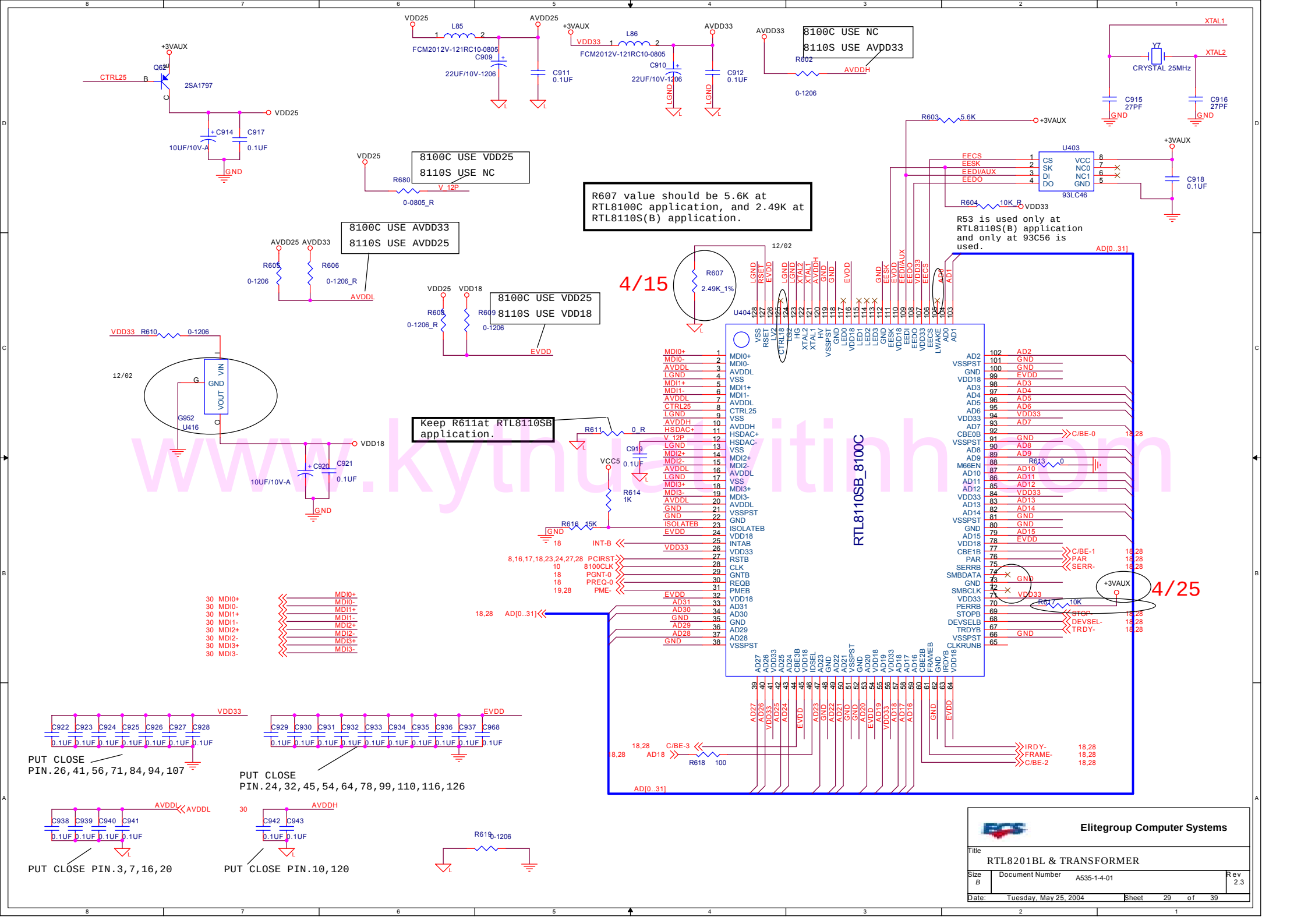
Date: Tuesday, May 25, 2004 | Sheet 27 of 39

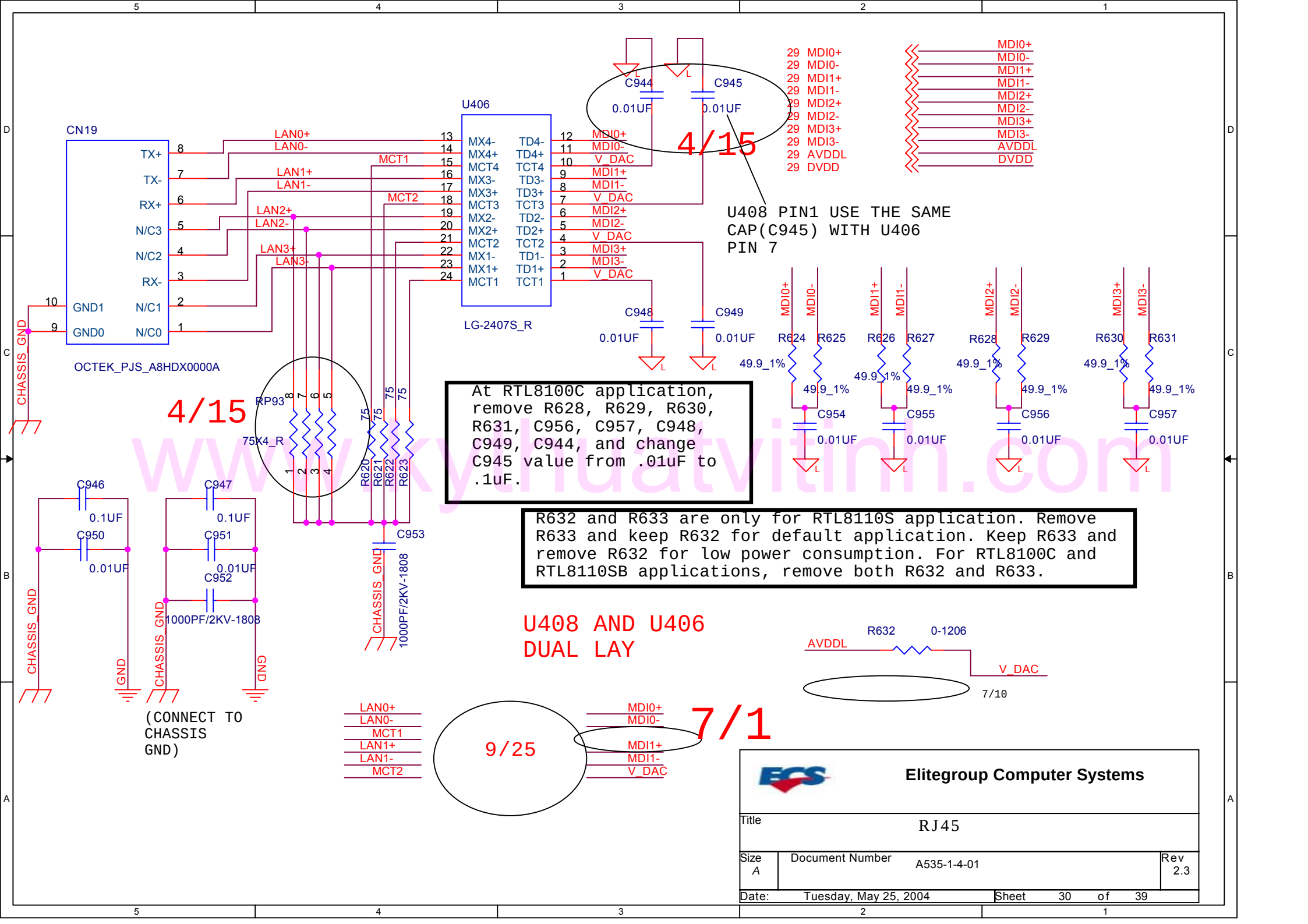
MINI PCI SOCKET

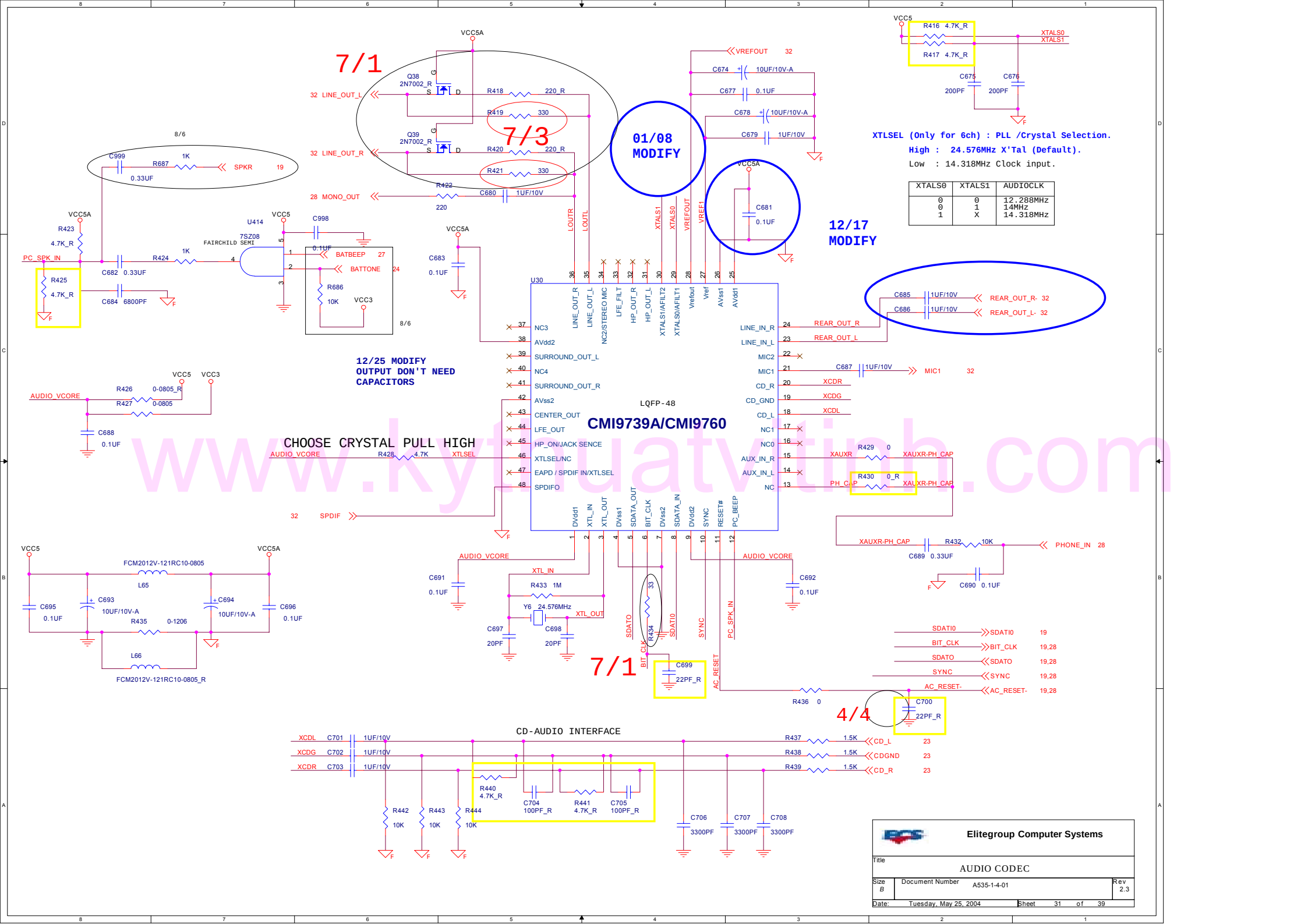


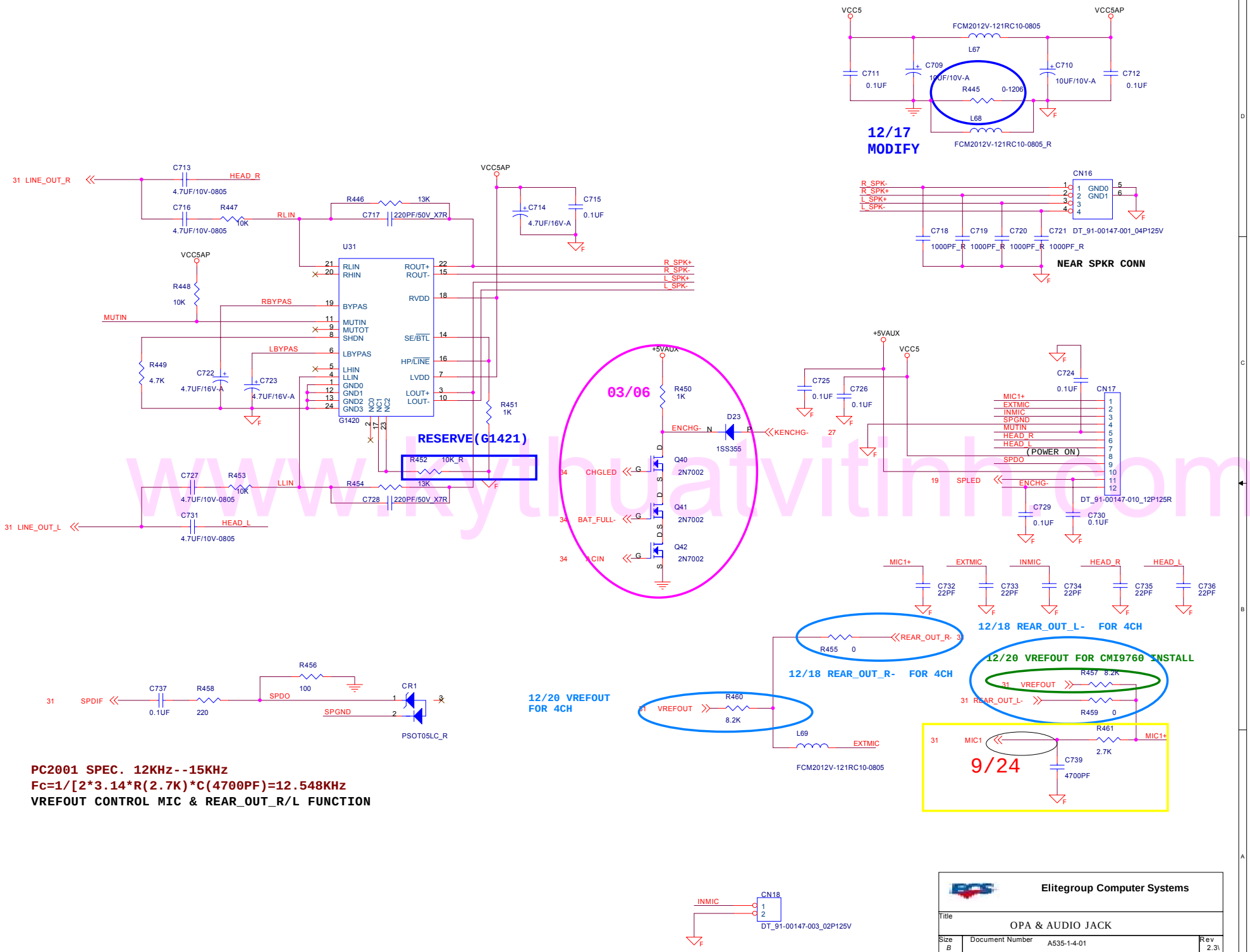
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Title: MINI PCI CONN.		
Size: B	Document Number: A535-1-4-01	Rev: 2.3
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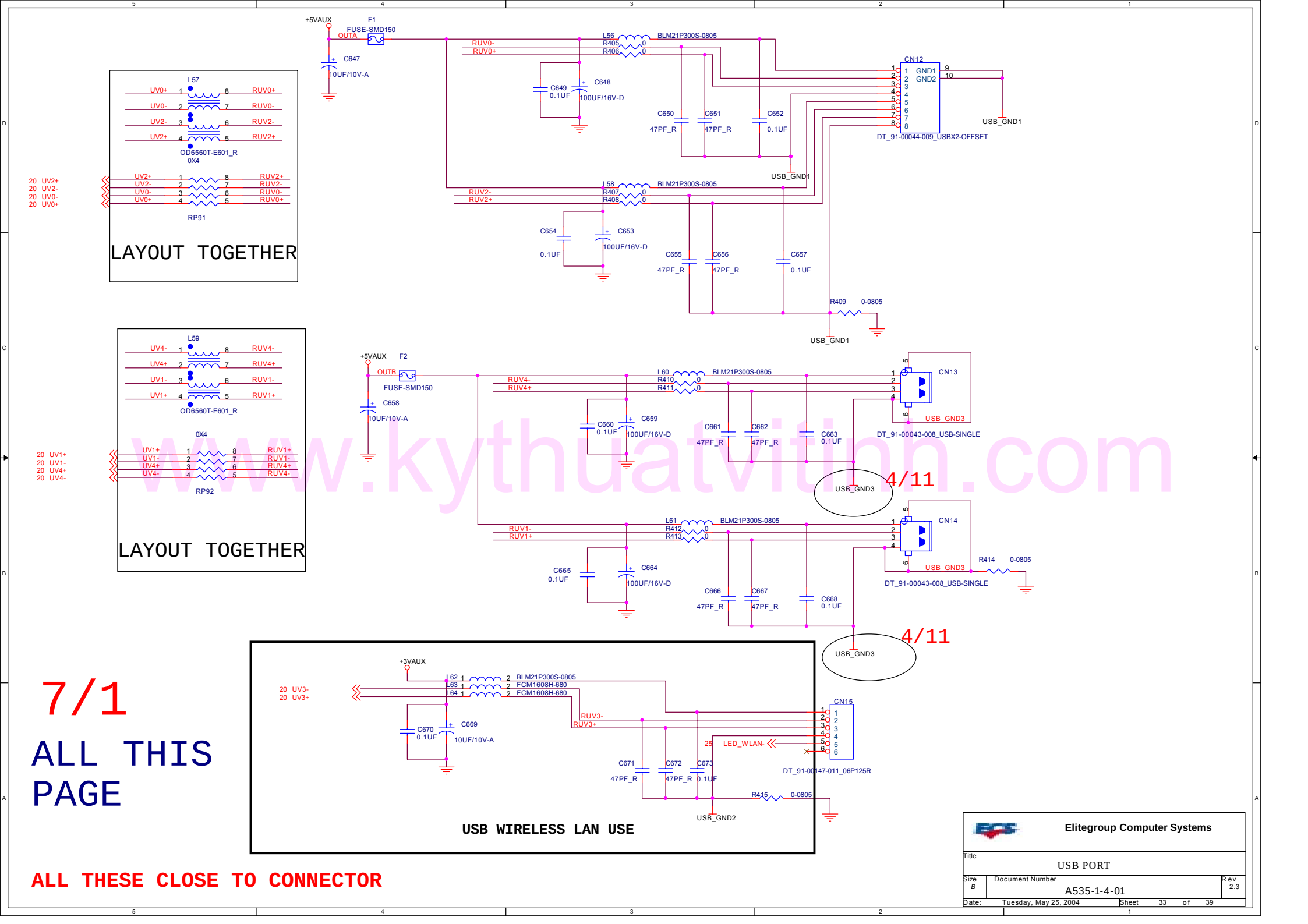

8100C USE NC
8110S USE AVDD33
8100C USE VDD25
8110S USE NC
8100C USE AVDD33
8110S USE AVDD25
8100C USE VDD25
8110S USE VDD18
R607 value should be 5.6K at RTL8100C application, and 2.49K at RTL8110S(B) application.
R53 is used only at RTL8110S(B) application and only at 93C56 is used.
Keep R611at RTL8110SB application.
RTL8110SB_8100C
93LC46
CRYSTAL 25MHz
PUT CLOSE PIN.26,41,56,71,84,94,107
PUT CLOSE PIN.24,32,45,54,64,78,99,110,116,126
PUT CLOSE PIN.3,7,16,20
PUT CLOSE PIN.10,120
4/15
4/25
Elitegroup Computer Systems
RTL8201BL & TRANSFORMER
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CN19
TX+
TX-
RX+
N/C3
N/C2
RX-
GND1
N/C1
GND0
N/C0
OCTEK_PJS_A8HDX0000A
CHASSIS_GND
LAN0+
LAN0-
LAN1+
LAN1-
LAN2+
LAN2-
LAN3+
LAN3-
MCT1
MCT2
U406
MX4-
MX4+
MCT4
MX3-
MX3+
MCT3
MX2-
MX2+
MCT2
MX1-
MX1+
MCT1
TD4-
TD4+
TCT4
TD3-
TD3+
TCT3
TD2-
TD2+
TCT2
TD1-
TD1+
TCT1
LG-2407S_R
MDI0+
MDI0-
V_DAC
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
AVDDL
DVDD
C944
C945
C948
C949
0.01UF
4/15
U408 PIN1 USE THE SAME CAP(C945) WITH U406 PIN 7
RP93
75X4_R
75
R620
R621
R622
R623
C946
C947
C950
C951
C952
C953
0.1UF
0.01UF
1000PF/2KV-1808
GND
(CONNECT TO CHASSIS GND)
R624
R625
R626
R627
R628
R629
R630
R631
49.9_1%
C954
C955
C956
C957
At RTL8100C application, remove R628, R629, R630, R631, C956, C957, C948, C949, C944, and change C945 value from .01uF to .1uF.
R632 and R633 are only for RTL8110S application. Remove R633 and keep R632 for default application. Keep R633 and remove R632 for low power consumption. For RTL8100C and RTL8110SB applications, remove both R632 and R633.
U408 AND U406 DUAL LAY
R632
0-1206
7/10
9/25
7/1
Elitegroup Computer Systems
Title
RJ45
Size
A
Document Number
A535-1-4-01
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2.3
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39


7/1
7/3
01/08 MODIFY
12/17 MODIFY
12/25 MODIFY OUTPUT DON'T NEED CAPACITORS
CHOOSE CRYSTAL PULL HIGH
CMI9739A/CMI9760
LQFP-48
U30
XTLSEL (Only for 6ch) : PLL /Crystal Selection.
High : 24.576MHz X'Tal (Default).
Low : 14.318MHz Clock input.
XTALS0 XTALS1 AUDIOCLK
0 0 12.288MHz
0 1 14MHz
1 X 14.318MHz
CD-AUDIO INTERFACE
Elitegroup Computer Systems
AUDIO CODEC
Size B
Document Number A535-1-4-01
Rev 2.3
Date: Tuesday, May 25, 2004
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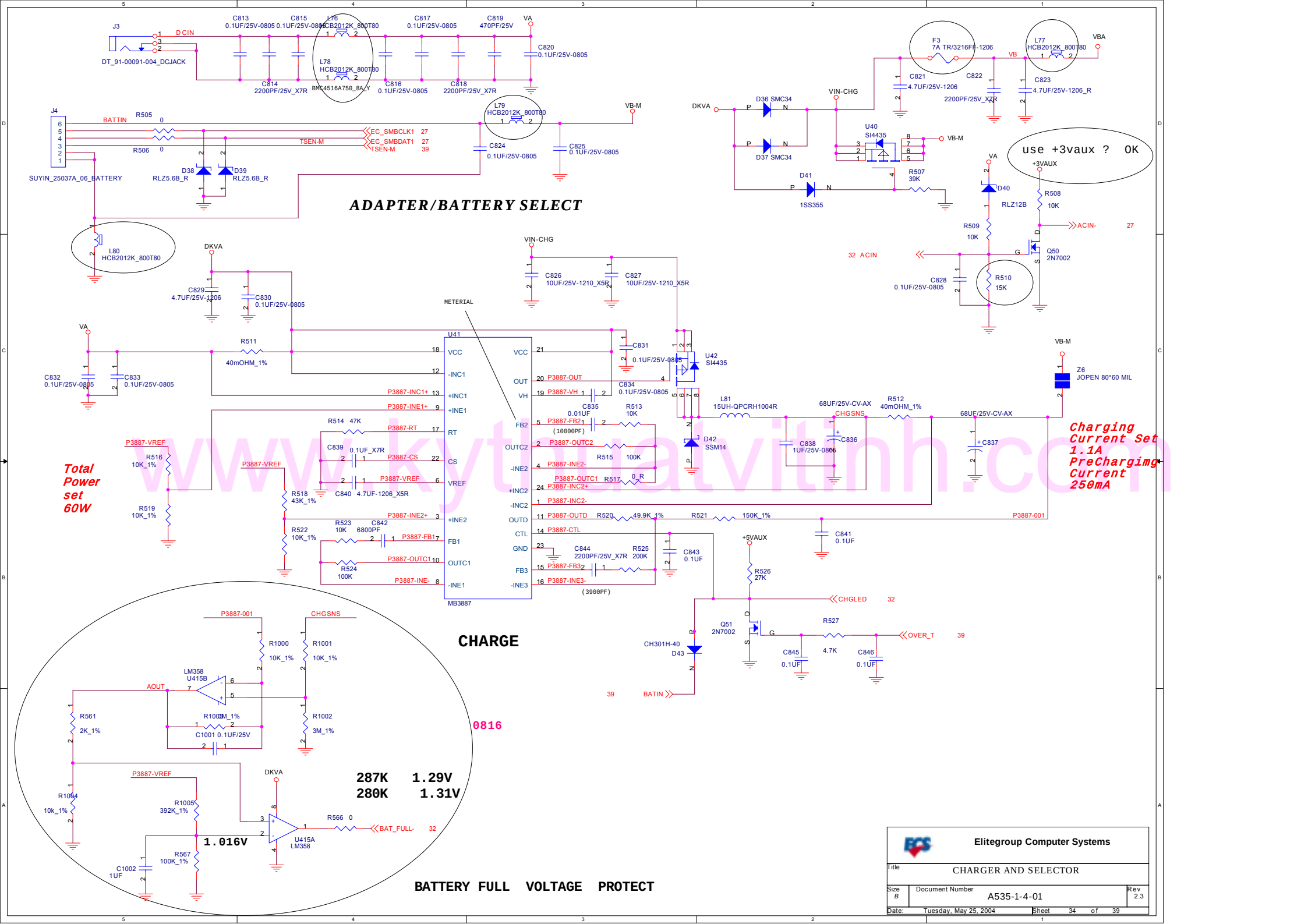


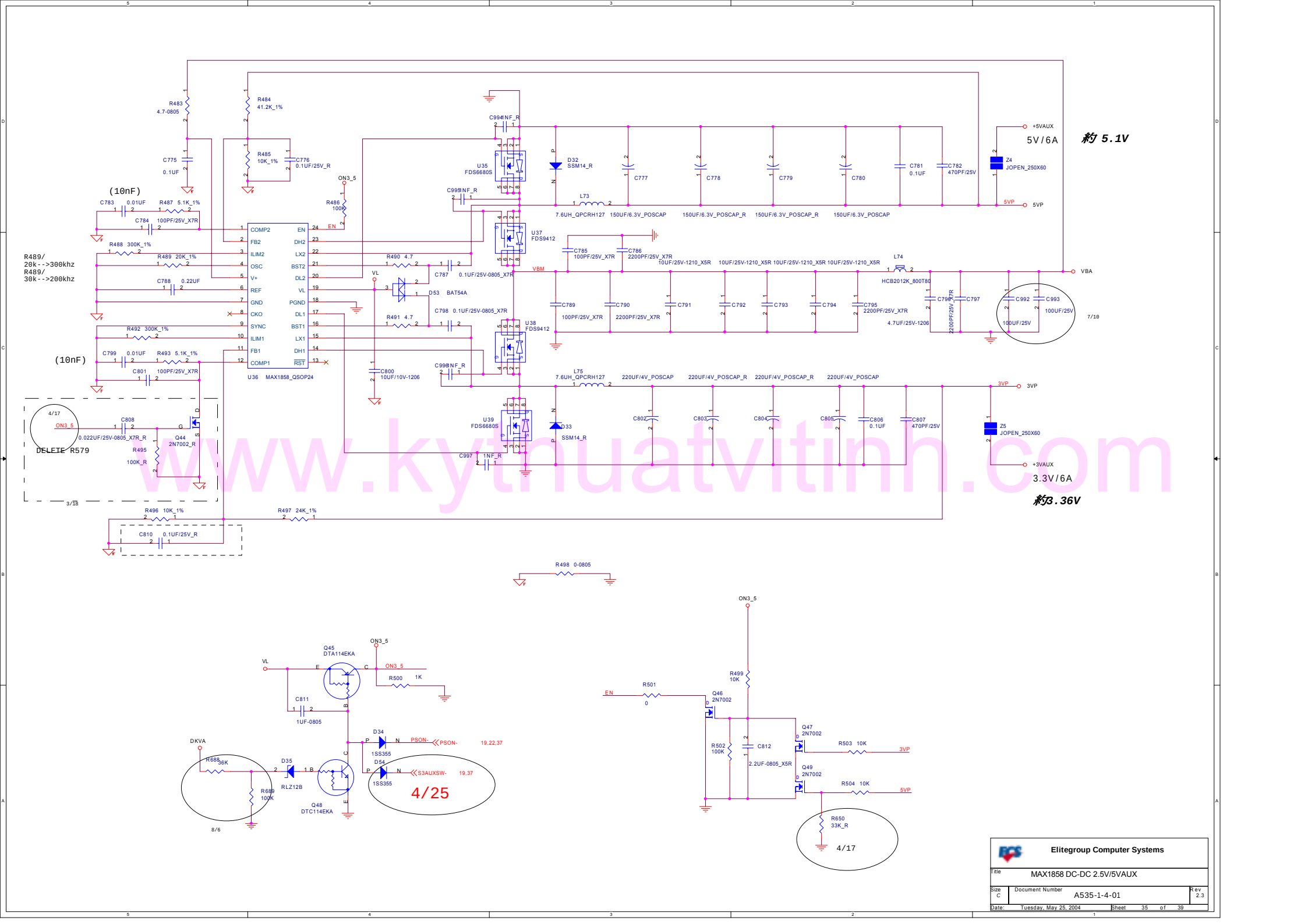
7/1

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ALL THESE CLOSE TO CONNECTOR

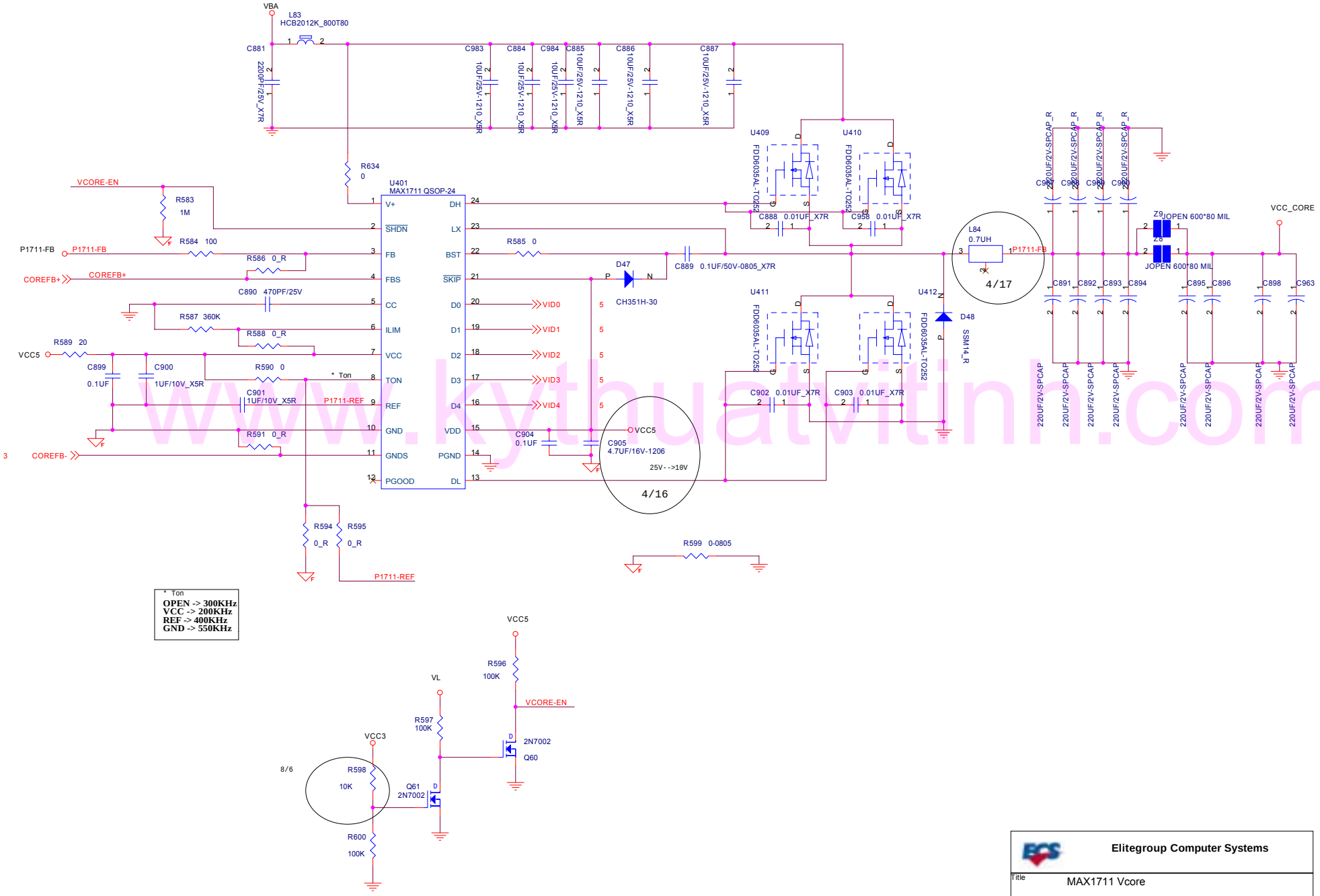
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ADAPTER/BATTERY SELECT
CHARGE
BATTERY FULL VOLTAGE PROTECT
use +3vaux ? OK
Charging Current Set 1.1A
PreChargimg Current 250mA
Total Power set 60W
0816
287K 1.29V
280K 1.31V
1.016V
MB3887
Elitegroup Computer Systems
CHARGER AND SELECTOR
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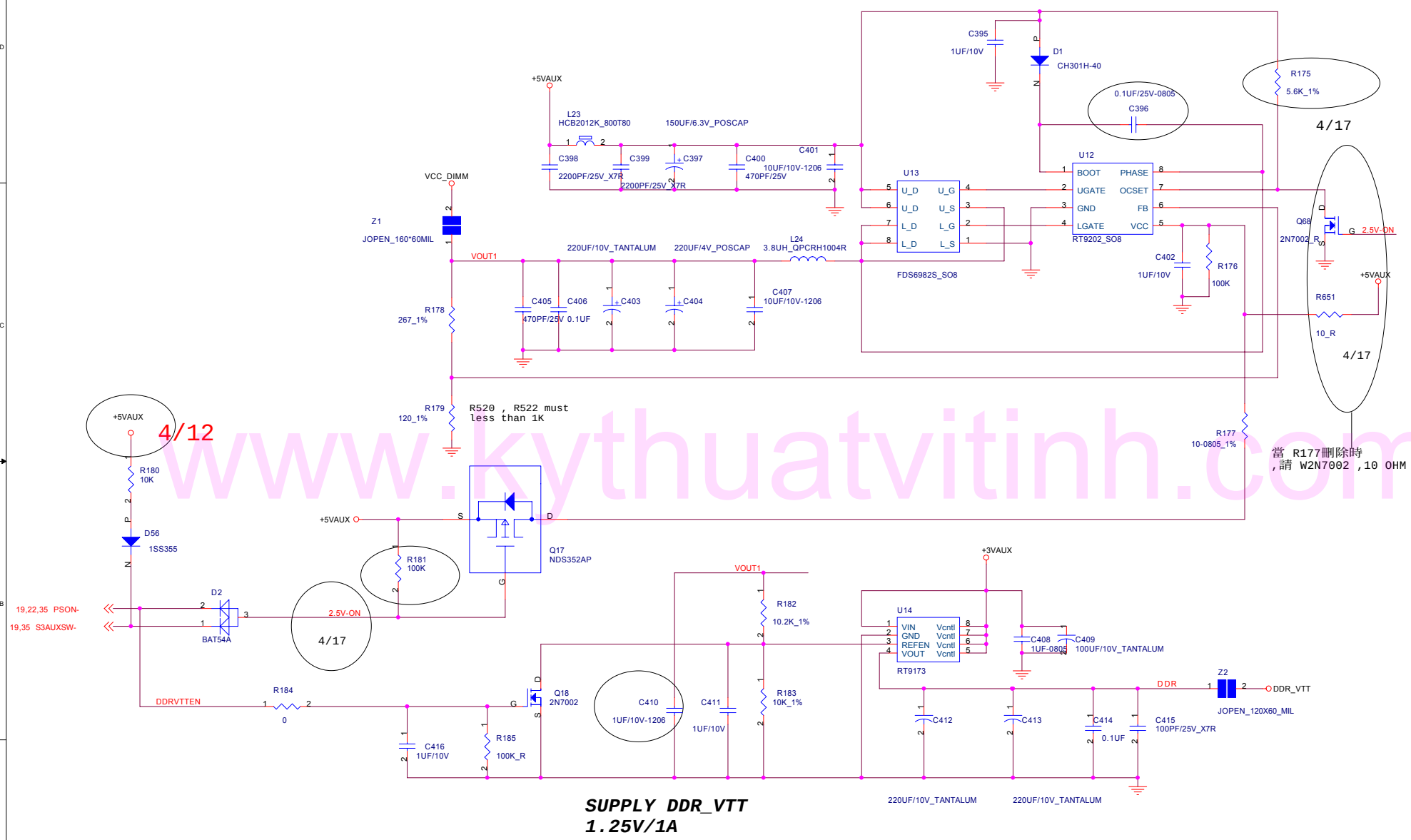
Elitegroup Computer Systems	
Title	MAX1858 DC-DC 2.5V/5VAUX
Size C	Document Number A535-1-4-01 Rev 2.3
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Elitegroup Computer Systems	
Title	MAX1711 Vcore
Size: Custom	Document Number: A535-1-4-01
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VCC2.5V SUPPLY 5A FOR VCC_DIMM

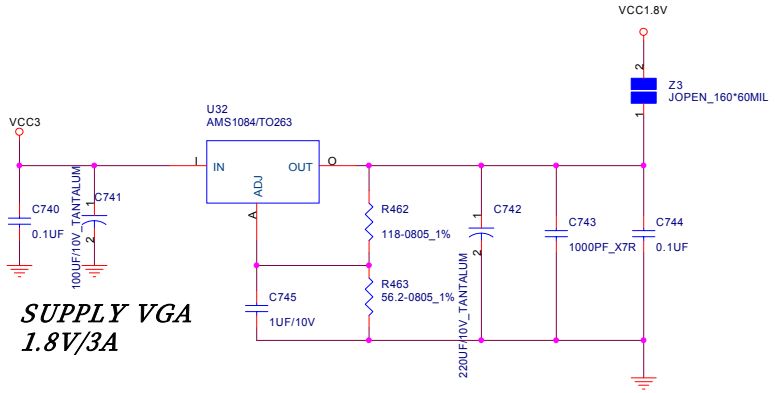


SUPPLY DDR_VTT
1.25V/1A

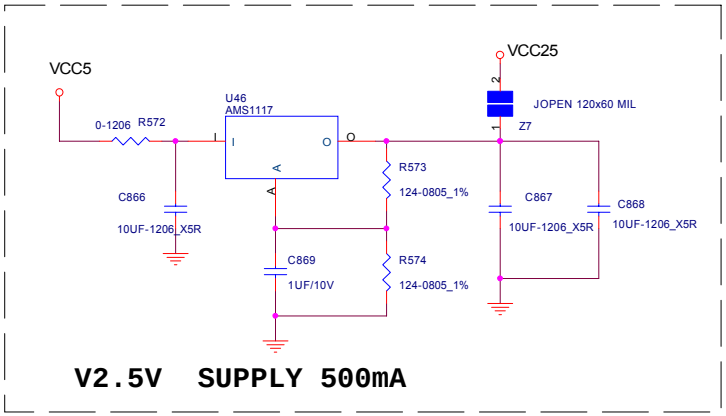
3 8.3K .5 7K
4 5.9K 6 3K
7 2.2K .5 1.97K
8 1.71K .5 1.49K
9 1.30 .5 1.14
10 1.0

Elitegroup Computer Systems			
Title: DDR POWER (2.5V/1.25V)			
Size: Custom	Document Number: A535-1-4-01		Rev: 2.3
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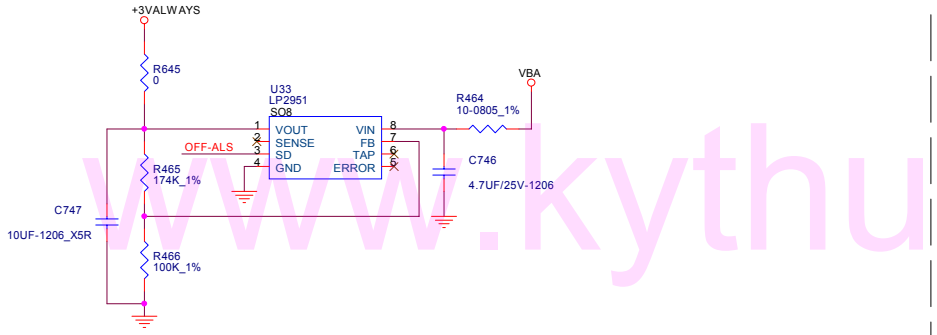
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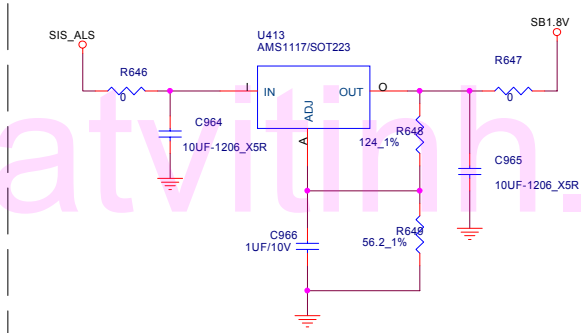
SUPPLY VGA
1.8V/3A



V2.5V SUPPLY 500mA



+3VALWAYS SUPPLY 20mA



+1.8VALWAYS SUPPLY 20mA for SIS CHIP

未 *PLACEMENT*
CLOSE CHIPSET

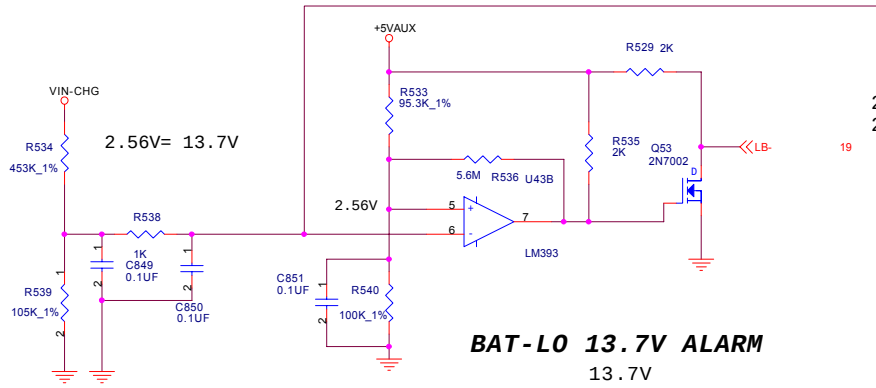
未 *PLACEMENT*
CLOSE CHIPSET

OFF-ALS <<OFF-ALS 39

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Elitegroup Computer Systems		
Title: VTT_1.8V		
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107->95.3 ECN OK

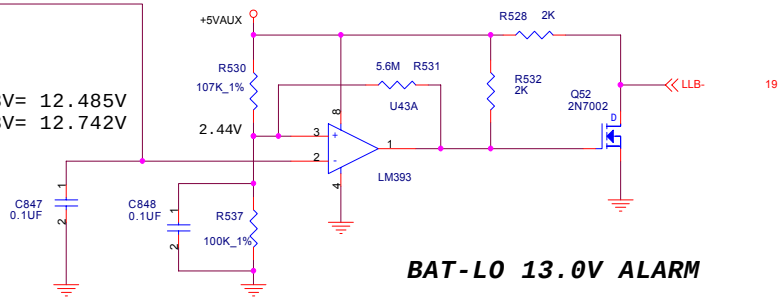


BAT-LO 13.7V ALARM

13.7V

115->107 ECN OK

2.30358V= 12.485V
2.35088V= 12.742V

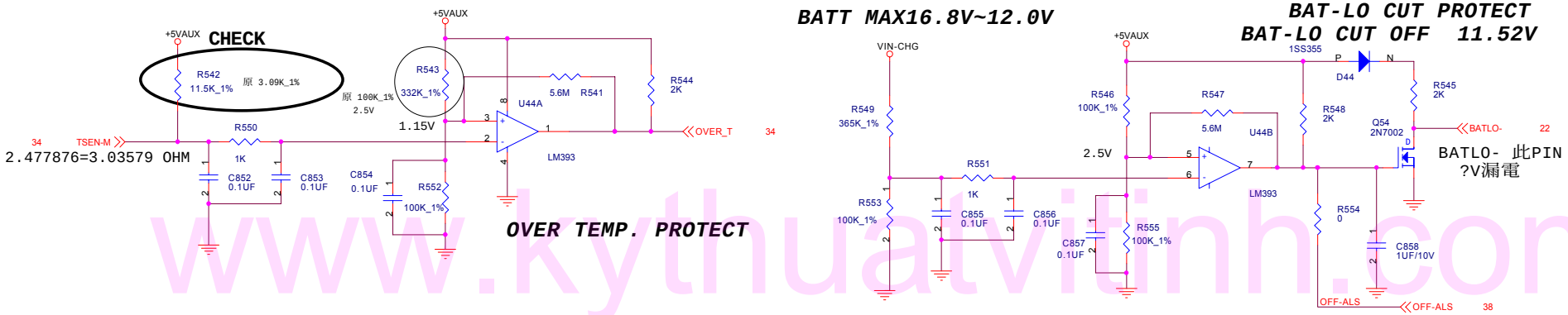


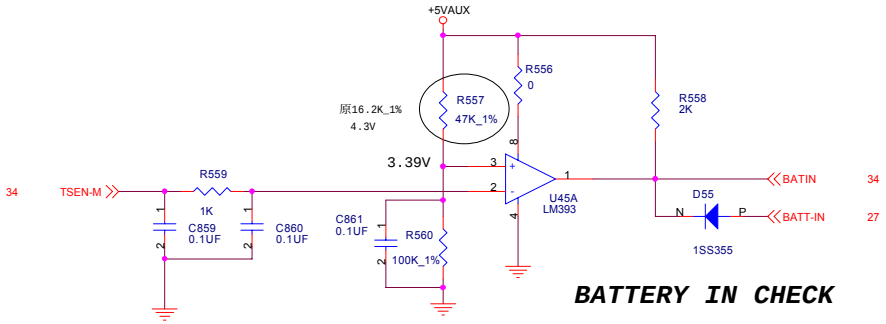
BAT-LO 13.0V ALARM

13.0V

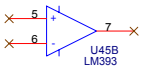
BATT MAX16.8V~12.0V

BAT-LO CUT PROTECT
BAT-LO CUT OFF 11.52V





BATTERY IN CHECK



T	MAX	TYP	MIN
0C-->	27.844K	27.303K	26.974K
5C -->	22.442K	22.075K	21.727K
25C-->	10.1k	10.0k	9.9k
55C-->	3.6k	3.54k	3.463k
60C-->	3.083k	3.0215k	2.9536k

Elitegroup Computer Systems

Title: BAT. LOW & OVER T.& LDO PWR

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