LLW-1/LGG-1 Schematics

Sandy Bridge

Cougar Point

2010-11-08

REV : SB

DY:None Installed
UMA:UMA platform installed only
PX:Discrete(both Robson and Whistler) SKU installed
RBS:Robson SKU installed only
WTL:Whistler SKU installed only
SAMSUNG:Use SAMSUNG VRAM
Hynix:Use Hynix VRAM
VRAM_1G:Use 1G VRAM
VRAM_2G:Use 2G VRAM

<Core Design>

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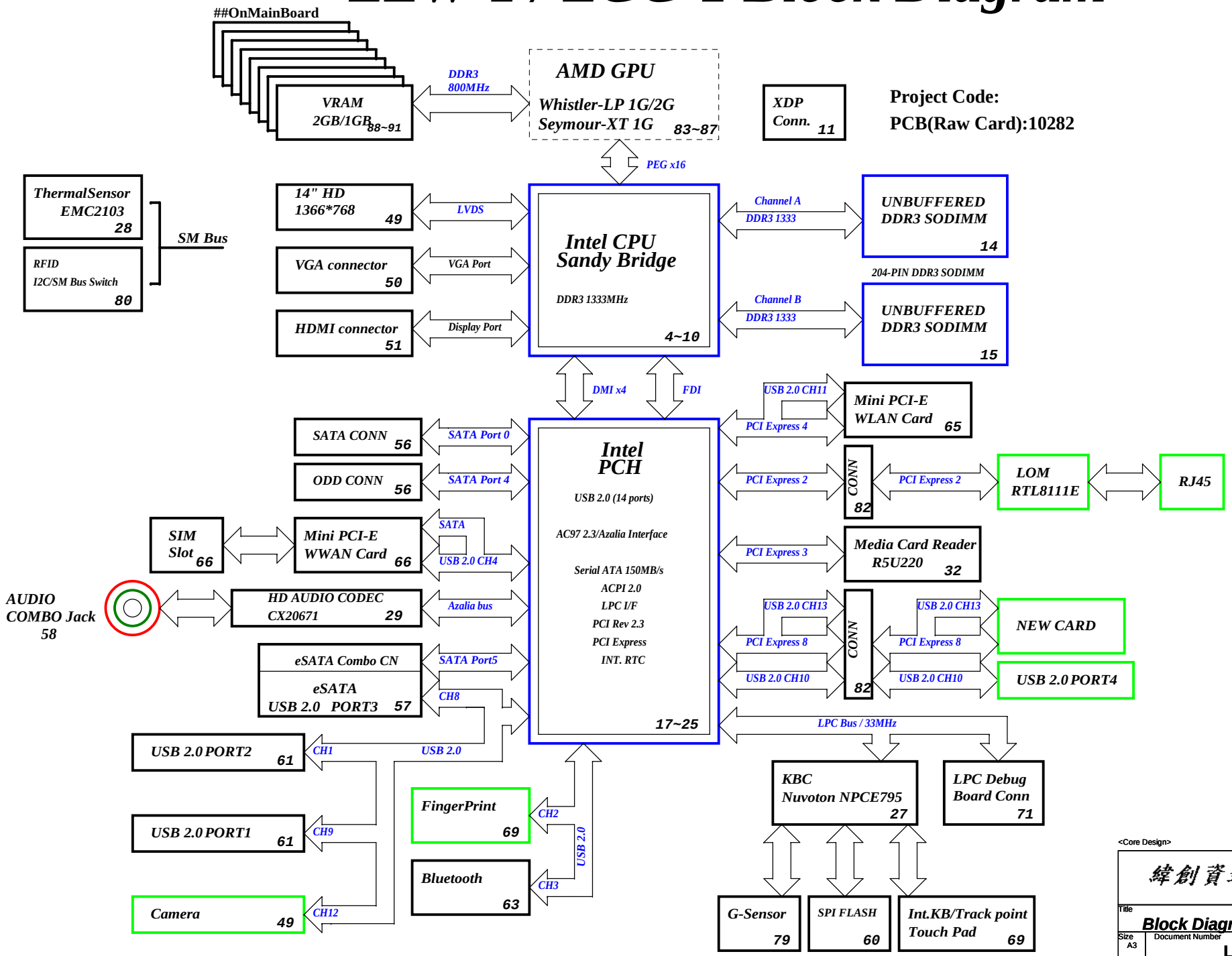
Title: Cover Page

Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 1 of 94

LLW-1 / LGG-1 Block Diagram



PCB Layer Stackup

L1: TOP	L5: VCC
L2: GND	L6: Signal
L3: Signal	L7: GND
L4: Signal	L8: BOTTOM

Battery Charger/Selector BQ24745 40

INPUTS	OUTPUTS
DCBATOUT	BT+

System DC/DC BD95280 41

PWR_3D3V_DCBATOUT	3D3V_S5
PWR_5V_DCBATOUT	5V_S5

CPU DC/DC NCP6131 42~44

DCBATOUT	VCC_CORE
DCBATOUT_VCC_GFXCORE	VCC_GFXCORE

1D05V_VTT TPS51218 45

PWR_1D05V_DCBATOUT	1D05V_VTT

1D5V_S3 TPS51218 46

PWR_1D5V_DCBATOUT	1D5V_S3

0D75V RT9026 46

1D5V_S3	DDR_VREF_S3 0D75V_S0

1D8V_S0 RT8015 47

3D3V_S5	1D8V_S0

VCCSA RT8208B 48

PWR_VCCSA_DCBATOUT	0D85V_S0

GFX CORE RT8208B 92

PWR_DCBATOUT_VGA_CORE	VGA_CORE

1V_VGA RT9025 93

1D5V_S3	1V_VGA_S0

1D8V_VGA RT9025 93

3D3V_S5	1D8V_VGA_S0

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Title: Block Diagram

Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 2 of 94

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	X
1	USB2
2	FINGERPRINT
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	ESATA1
9	USB1
10	USB Ext. port 4
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	RESERVED
LANE2	LAN
LANE3	CARD READER
LANE4	MiniCard WLAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	RESERVED
LANE8	NEW CARD

SATA Table

SATA	
Pair	Device
0	HDD
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses		HURON RIVER ORB		
Device	Ref Des	Address	Hex	Bus
EC SMBus 1				
Battery				KBC_SDA1/KBC_SCL1
Capacity Board				KBC_SDA1/KBC_SCL1
EC SMBus 2				
PCH				KBC_SDA2/KBC_SCL2
MXM				KBC_SDA2/KBC_SCL2
LCD				KBC_SDA2/KBC_SCL2
Thermal Sensor				KBC_SDA2/KBC_SCL2
PCH SMBus				
CK505 Clock Generator				
SO-DIMMA (SPD)				PCH_SMBDATA/PCH_SMBCLK
SO-DIMMB (SPD)				PCH_SMBDATA/PCH_SMBCLK
Digital Pot				PCH_SMBDATA/PCH_SMBCLK
				PCH_SMBDATA/PCH_SMBCLK

<Core Design>

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Title: Table of Content

Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 3 of 94

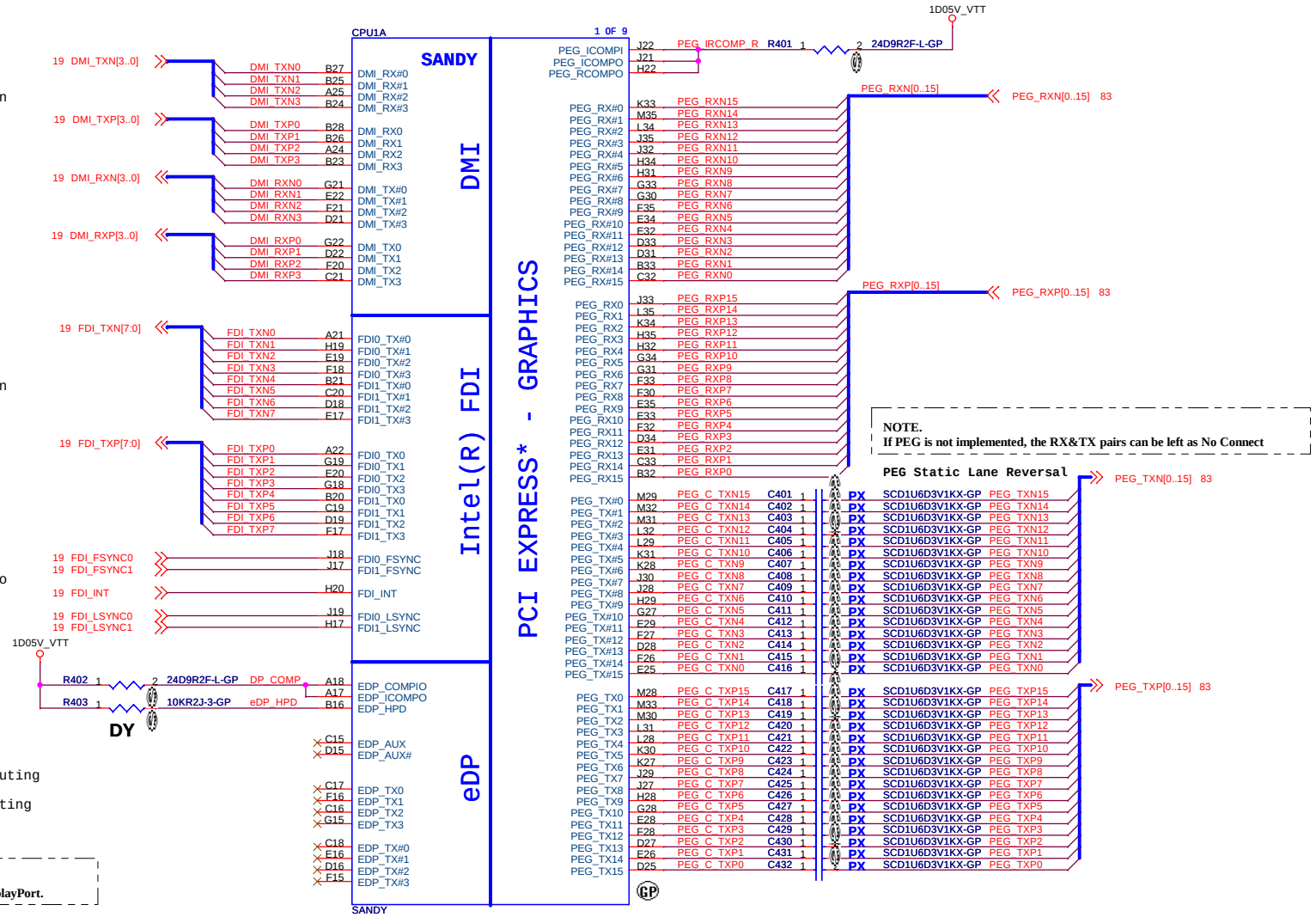
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.



NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Table 4.1- Central Processing Unit slot multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
FOXCONN	PZ98827-364B-41F	N/A	62.10055.421
TYCO	2-2013620-3	N/A	62.10040.771

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Title: CPU (PCIE/DMI/FDI)
Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB
Date: Tuesday, November 09, 2010 | Sheet 4 of 94

SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

RN502 CLK_DP_P_R CLK_DP_N_R SRN1KJ-11-GP-U DY

Connect EC to PROCHOT# through inverting OD buffer.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

CPU1B 2 OF 9 SANDY

MISC: SNB_IVB# SKTOCC#
THERMAL: CATERR# PECI PROCHOT# THERMTRIP#
PWR MANAGEMENT: PM_SYNC UNCOREPWRGOOD SM_DRAMPWROK RESET#
CLOCKS: BCLK BCLK# DPLL_REF_SSCLK DPLL_REF_SSCLK#
DDR3 MISC: SM_DRAMRST# SM_RCOMP0 SM_RCOMP1 SM_RCOMP2
JTAG & BPM: PRDY# PREQ# TCK TMS TRST# TDI TDO DBR# BPM#0 BPM#1 BPM#2 BPM#3 BPM#4 BPM#5 BPM#6 BPM#7

1D05V_VTT R501 62R2J-GP H_PROCHOT# C502 SC47P50V2JN-3GP
R506 H_CPUPWRGD_R 10KR2J-3-GP
R504 0R2J-2-GP R505 0R2J-2-GP DY
R513 56R2F-1-GP
R508 140R2F-GP R507 25D5R2F-GP R510 200R2F-L-GP R503 4K99R2F-L-GP
RN501 XDP_TDI XDP_TMS XDP_TDO XDP_TCLK SRN51J-1-GP
R511 51R2J-2-GP
R516 1KR2J-1-GP
3D3V_S0
R502 1KR2J-1-GP
R509 75R2F-2-GP
R512 43R2J-GP
Q501 2N7002K-2-GP 84.2N702.J31 2nd = 84.2N702.031
Q502 2N7002K-2-GP 84.2N702.J31 2nd = 84.2N702.031
TP501 TP502 TP503 TP504 TP505 TP506 TP507 TP508 TP509 TP510 TP511 TP512 TP513 TP514 TP515

Table 5.1- N-Channel MOSFET multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
PANJIT	2N7002K	N/A	84.2N702.J31
DIODES	2N7002K	N/A	84.2N702.031
NXP	2N7002BK	N/A	84.07002.I31

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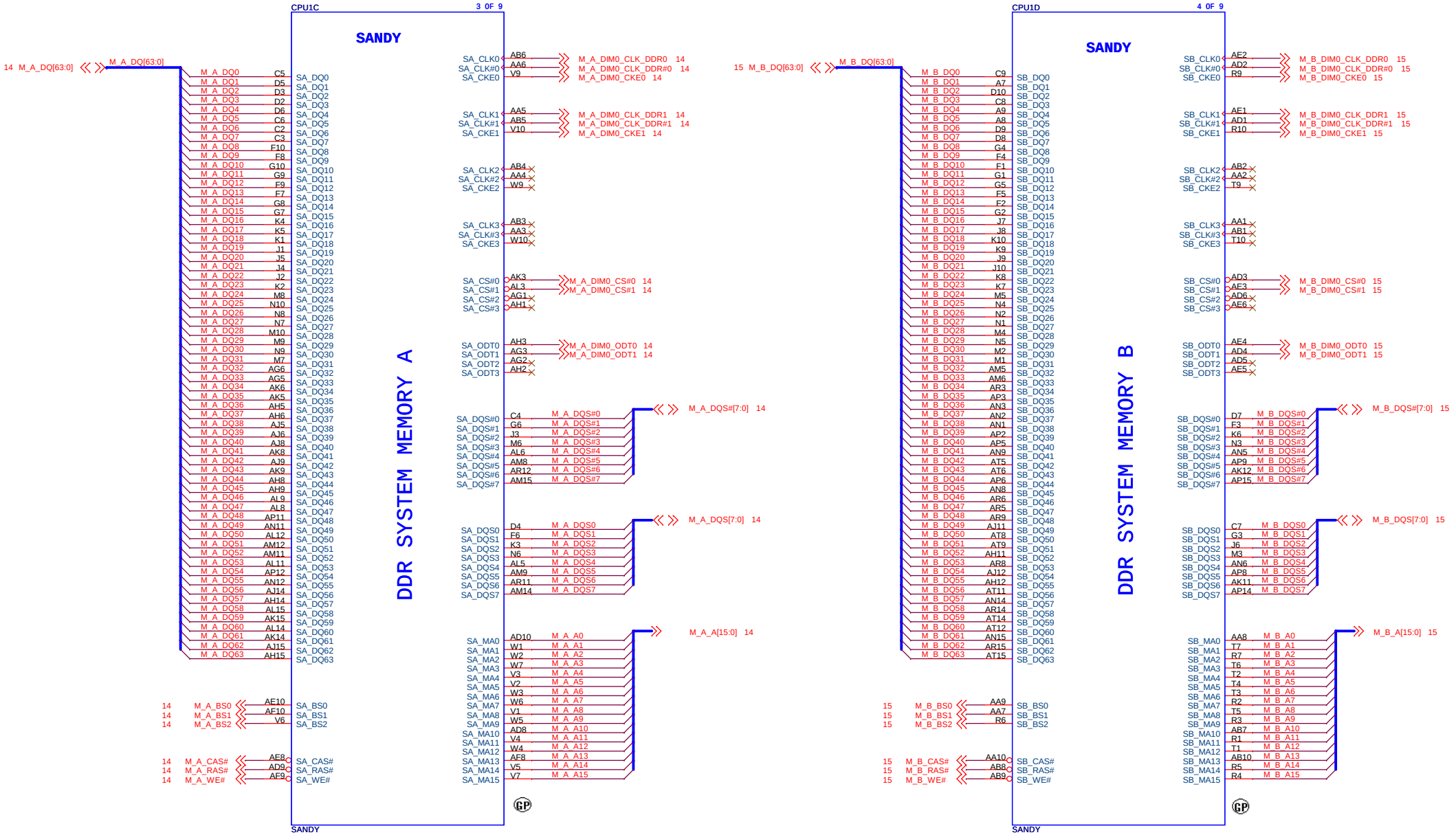
Title: CPU (Thermal/CLK/PM)
Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB
Date: Tuesday, November 09, 2010 | Sheet 5 of 94

SSID = CPU



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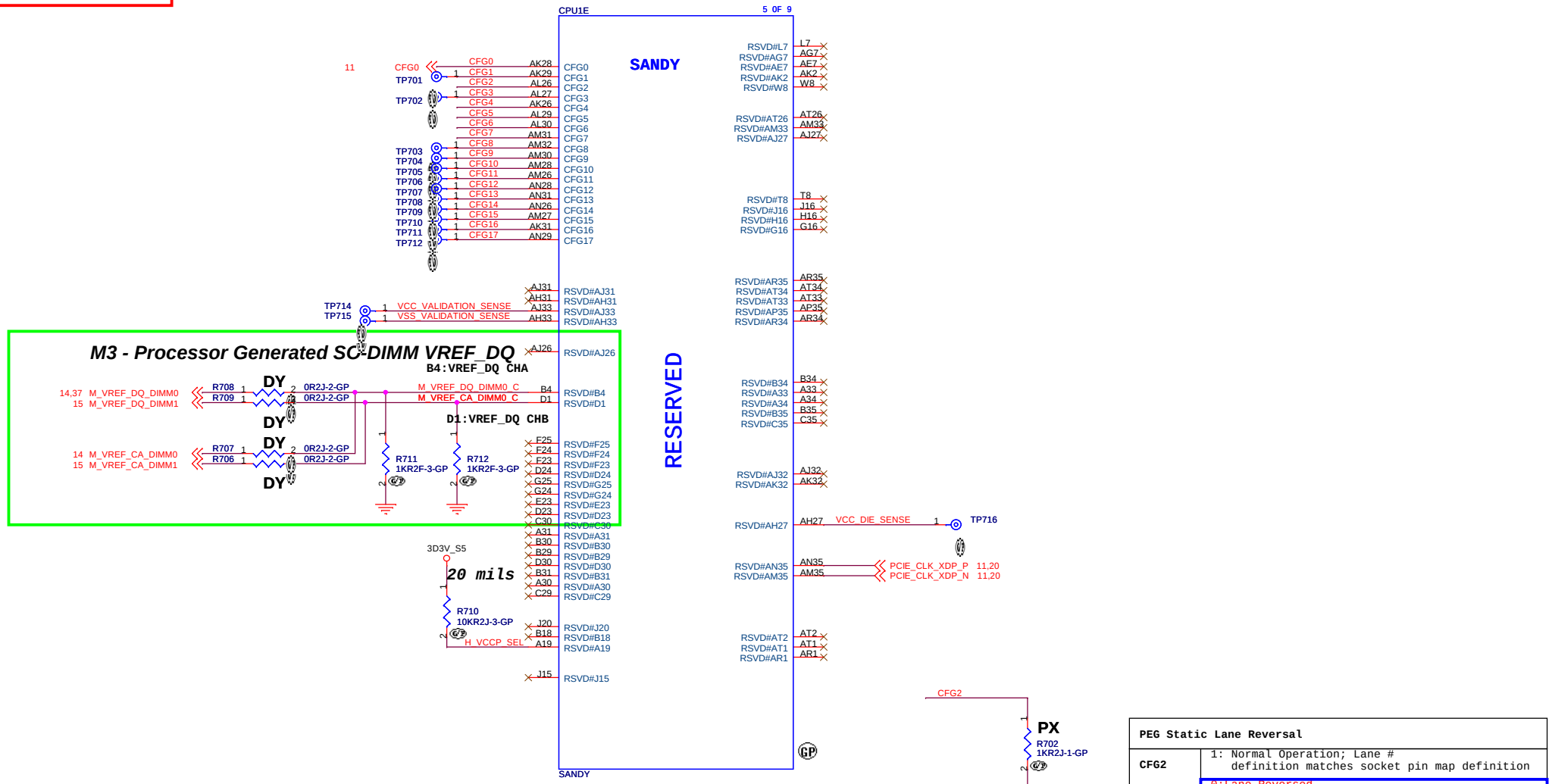
Title: **CPU (DDR)**

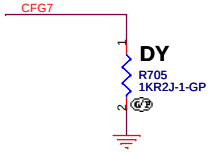
Size: A3 | Document Number: **LLW-1 / LGG-1** | Rev: **SB**

Date: Tuesday, November 09, 2010 | Sheet 6 of 94

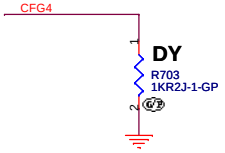
SSID = CPU



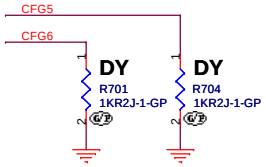
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

<Core Design>

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Title: **CPU (RESERVED)**

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 7 of 94

SSID = CPU

POWER

PROCESSOR CORE POWER

53A

VCC_CORE

SC10U6D3V3MX-GP: C801, C802, C803, C804, C811

SC10U6D3V3MX-GP: C815, C817, C818, C819, C820

SC10U6D3V5KX-1GP: C816, C821, C822, C823, C824, C825, C826, C827

SC10U6D3V5KX-1GP: C837, C836, C835, C834, C833, C832, C831, C828

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

CPU1F — SANDY — 6 OF 9

VCC_CORE

VCC: AG35, AG34, AG33, AG32, AG31, AG30, AG29, AG28, AG27, AG26, AF35, AF34, AF33, AF32, AF31, AF30, AF29, AF28, AF27, AF26, AD35, AD34, AD33, AD32, AD31, AD30, AD29, AD28, AD27, AD26, AC35, AC34, AC33, AC32, AC31, AC30, AC29, AC28, AC27, AC26, AA35, AA34, AA33, AA32, AA31, AA30, AA29, AA28, AA27, AA26, Y35, Y34, Y33, Y32, Y31, Y30, Y29, Y28, Y27, Y26, V35, V34, V33, V32, V31, V30, V29, V28, V27, V26, U35, U34, U33, U32, U31, U30, U29, U28, U27, U26, R35, R34, R33, R32, R31, R30, R29, R28, R27, R26, P35, P34, P33, P32, P31, P30, P29, P28, P27, P26

PEG AND DDR

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

VCCIO: AH13, AH10, AG10, AC10, Y10, U10, P10, L10, J14, J13, J12, J11, H14, H12, H11, G14, G13, G12, F14, F13, F12, F11, F14, F12

SC10U6D3V5KX-1GP: C805, C806, C807, C808, C809, C810, C838, C839, C840, C841

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

VCCIO: E11, D14, D13, D12, D11, C14, C13, C12, C11, B14, B12, A14, A13, A12, A11, J23

SC10U6D3V5KX-1GP: C812, C813, C814, C829, C830, C842, C843, C844, C845

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT

H_CPU_SVIDDAT — R804 — 130R2F-1-GP

S-HS_20100610 V1.0

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT# — R803 — 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK — H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT — H_CPU_SVIDDAT 42

SENSE LINES

R801, R802 need to close to CPU

VCC_CORE

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 — VCCSENSE 42
VSS_SENSE AJ34 — VSSSENSE 42

VCCIO_SENSE B10 — VCCIO_SENSE 45
VSSIO_SENSE A10 — VSSIO_SENSE 45

R802 100R2F-L1-GP-U

SANDY

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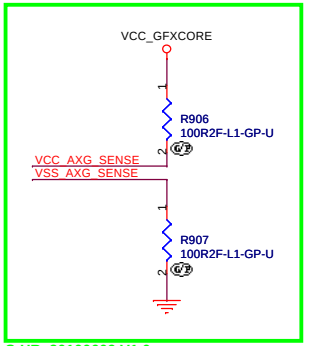
Title: CPU (VCC_CORE)
Size: Custom | Document Number: LLW-1 / LGG-1 | Rev: SB
Date: Tuesday, November 09, 2010 | Sheet 8 of 94

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU



POWER

CPU1G — 7 OF 9 — SANDY

VCC_GFXCORE

PROCESSOR VAXG: 24A

VAXG: AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

C901 C902 C903 C904 C905 C906 C907 C908 C918 C919 C920 C921 — SC10U6D3V5KX-1GP

SENSE LINES

VAXG_SENSE — AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE — AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF — AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_S0

PROCESSOR VDDQ: 10A

VDDQ: AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

C916 C915 C917 — SC10U6D3V5KX-1GP

TC903 ST330U2VDM-4-GP 79.33719.20L

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0

R902 10R2J-2-GP — **R902 need be close to pin H23.**

MISC

VCCSA_SENSE — H23 — VCCSA_SENSE — VCCSA_SENSE 48

FC_C22 — C22 — H_FC_C22 — H_FC_C22 48
VCCSA_VID1 — C24 — VCCSA_SEL — VCCSA_SEL 48

RN901 SRN1KJ-7-GP

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL: B6 A6 A2

C925 C923 C922 C924 — SC10U6D3V5KX-1GP / SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

SANDY

<Core Design>

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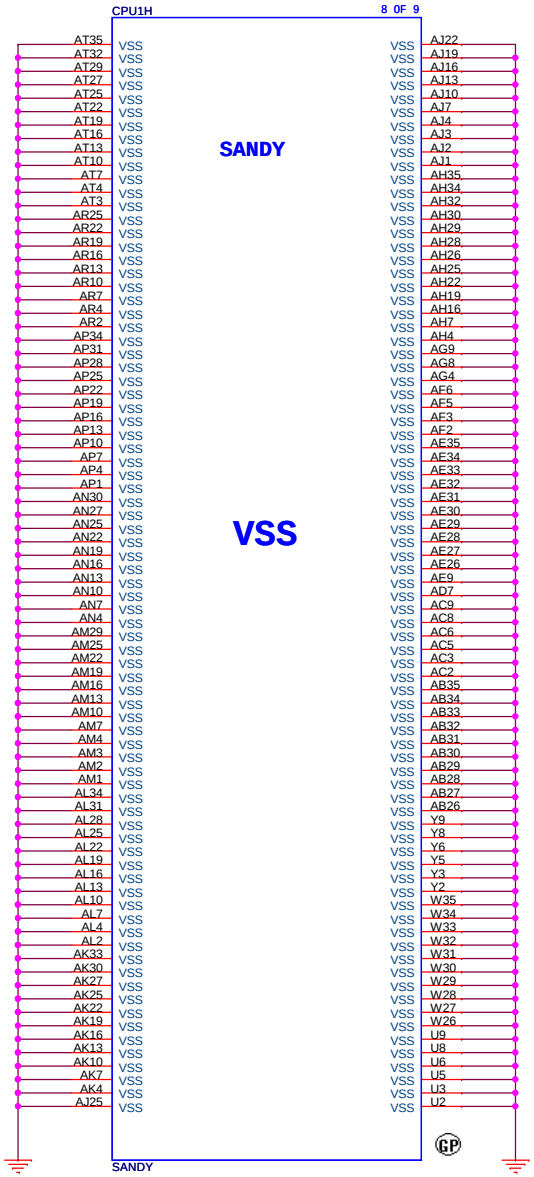
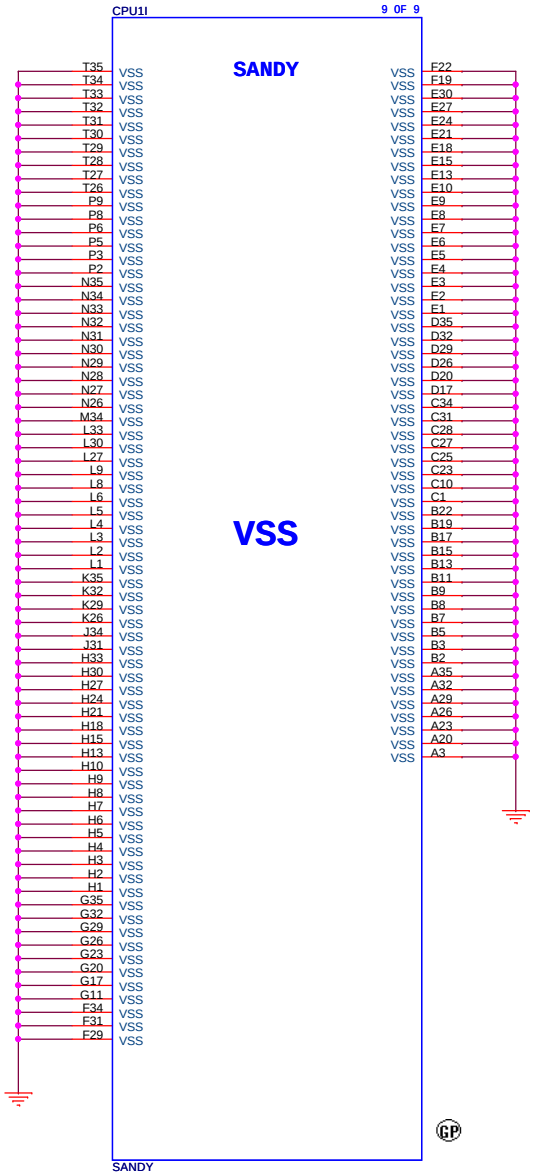
Title: **CPU (VCC_GFXCORE)**

Size: A3 | Document Number: **LLW-1 / LGG-1** | Rev: **SB**

Date: Tuesday, November 09, 2010 | Sheet 9 of 94

SSID = CPU





<Core Design>

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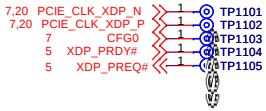
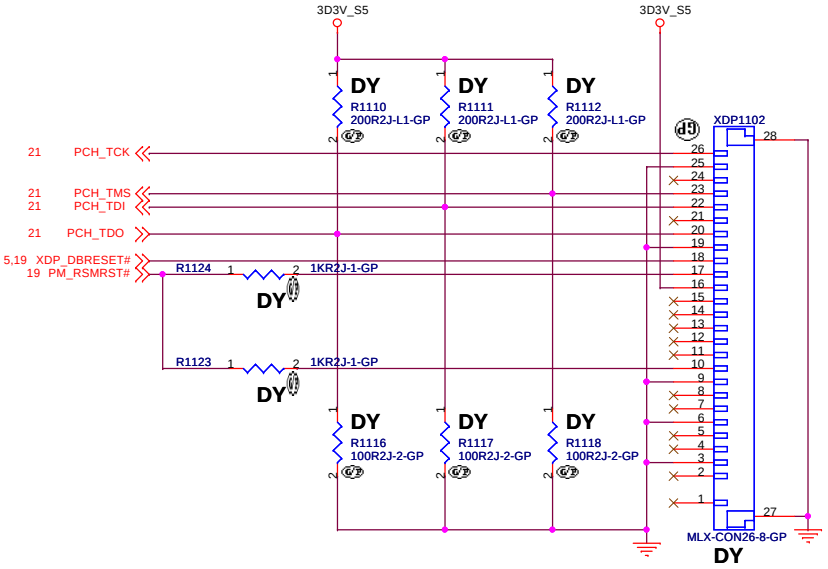
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 10 of 94





DEBUG Interface for Processor.

CPU XDP SFF 26pin IF
Pin 1 OBSFN_A0 (PREQ#, I/O)
Pin 2 OBSFN_A1 (PRDY#, I/O)
Pin 3 GND
Pin 4 OBSDATA_A0 (Open, I/O)
Pin 5 OBSDATA_A1 (Open, I/O)
Pin 6 GND
Pin 7 OBSDATA_A2 (Open, I/O)
Pin 8 OBSDATA_A3 (Open, I/O)
Pin 9 GND
Pin 10 HOOK0 (PWRGD, In)
Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
Pin 12 HOOK2 (CFG0, Out)
Pin 13 HOOK3 (vr_READYSYS_PWROK,Out)
Pin 14 HOOK4 (BCLK, In)
Pin 15 HOOK5 (BCLK#, In)
Pin 16 VCCOBS_AB (VCCP Voltage of CPU, In)
Pin 17 HOOK6 (RESET#, Out)
Pin 18 HOOK7 (DBR#, Out)
Pin 19 GND
Pin 20 TDO, In
Pin 21 TRST#, Out
Pin 22 TDI, Out
Pin 23 TMS, Out
Pin 24 TCK1 (Open)
Pin 25 GND
Pin 26 TCK0 ,Out

TABLE

PCH PIN	REF DES	PCH ES1 JTAG		PCH ES2 JTAG		PRODUCTION	
		Enable	Disable	Enable	Disable	Enable	Disable
TDO	R1110	DY	DY	200 Ohms	DY	DY	DY
	R1116	DY	DY	100 Ohms	DY	DY	DY
	R2	DY	DY	DY	DY	51 Ohms	DY
TMS	R1112	200 Ohms	DY	200 Ohms	DY	DY	DY
	R1118	100 Ohms	DY	100 Ohms	DY	DY	DY
	R91	DY	DY	DY	DY	51 Ohms	DY
TDI	R1111	200 Ohms	20K Ohms	200 Ohms	DY	DY	DY
	R1117	100 Ohms	10K Ohms	100 Ohms	DY	DY	DY
	R90	DY	DY	DY	DY	51 Ohms	DY
TCK	R541	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms
TRST#	R953	20K Ohms	DY	DY	DY	DY	DY
	R535	10K Ohms	DY	DY	DY	DY	DY
	R103	DY	DY	DY	DY	DY	DY

LOGIC

DEBUG Interface for PCH.

PCH XDP SFF 26pin IF
Pin 1 OBSFN_A0 (Open), I/O)
Pin 2 OBSFN_A1 (Open, I/O)
Pin 3 GND
Pin 4 OBSDATA_A0 (Open, I/O)
Pin 5 OBSDATA_A1 (Open, I/O)
Pin 6 GND
Pin 7 OBSDATA_A2 (Open, I/O)
Pin 8 OBSDATA_A3 (Open, I/O)
Pin 9 GND
Pin 10 HOOK0 (RSMRST#, In)
Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
Pin 12 HOOK2 (Open)
Pin 13 HOOK3 (Open)
Pin 14 HOOK4 (Open)
Pin 15 HOOK5 (Open)
Pin 16 VCCOBS_AB (3.3VSUS, In)
Pin 17 HOOK6 (RSMRST#, Out)
Pin 18 HOOK7 (DBR#, Out)
Pin 19 GND
Pin 20 TDO (JTAG, In)
Pin 21 TRST# (Open)
Pin 22 TDI (JTAG, Out)
Pin 23 TMS (JTAG, Out)
Pin 24 TCK1 (Open)
Pin 25 GND
Pin 26 TCK0 (JTAG, Out)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP CONN
Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB
Date: Tuesday, November 09, 2010 | Sheet 11 of 94

BLANK

<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
A4	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 12 of 94

BLANK

<Core Design>

緯創資通

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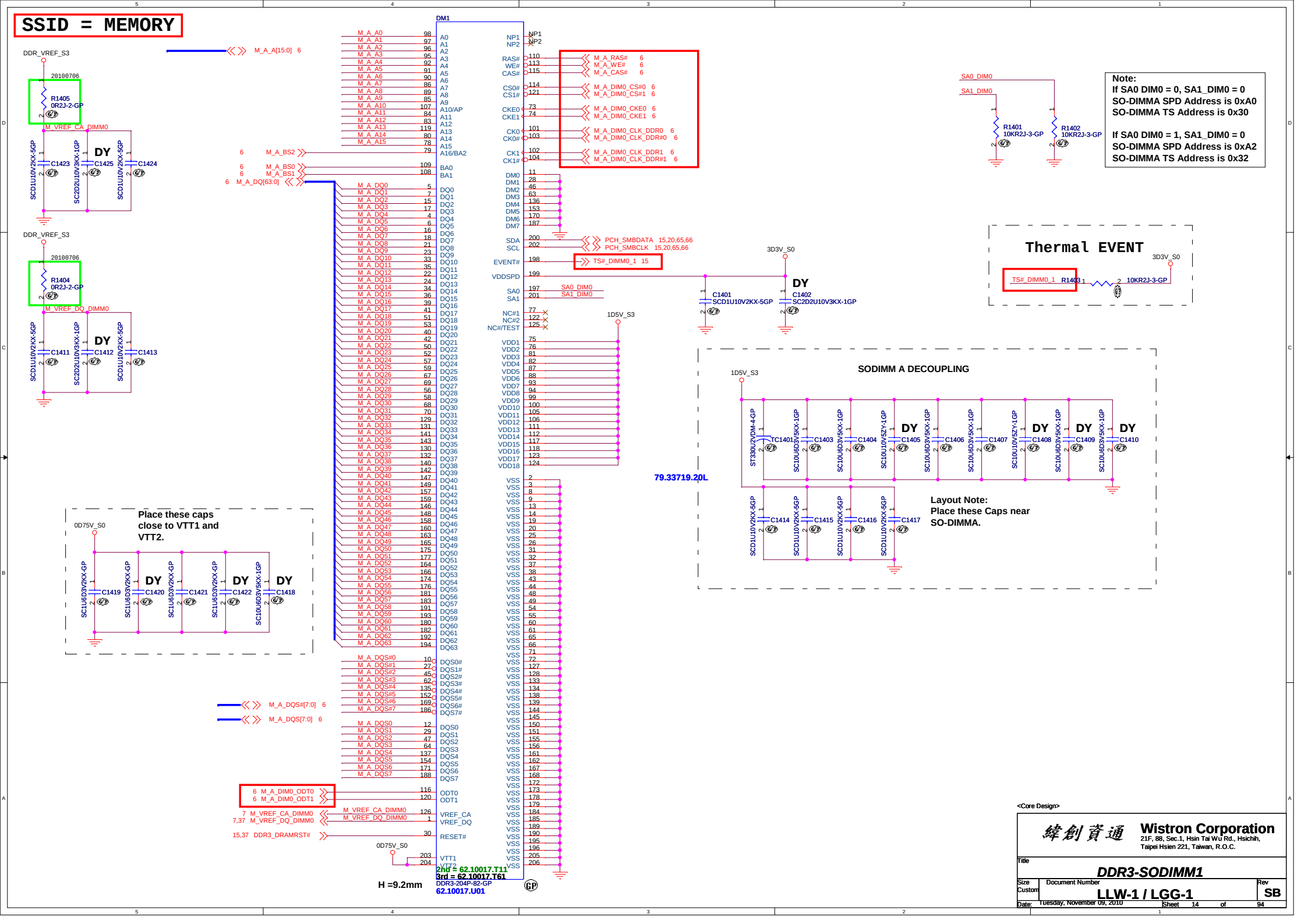
Title

CLOCK GEN

Size	Document Number	Rev
A4	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 13 of 94

SSID = MEMORY



<Core Design>

Wistron Corporation
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Title: DDR3-SODIMM1

Size: Custom | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 14 of 94

SSID = MEMORY

DM2

M_B_A[15:0] 6

M_B_BS2 6

M_B_BS0 6

M_B_BS1 6

M_B_DQ[63:0] 6

M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6

M_B_DIM0_CS#0 6
M_B_DIM0_CS#1 6

M_B_DIM0_CKE0 6
M_B_DIM0_CKE1 6

M_B_DIM0_CLK_DDR0 6
M_B_DIM0_CLK_DDR#0 6

M_B_DIM0_CLK_DDR1 6
M_B_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14,20,65,66
PCH_SMBCLK 14,20,65,66

TS#_DIMM0_1 14

SA0_DIM1
SA1_DIM1

M_B_DQS#[7:0] 6

M_B_DQS[7:0] 6

6 M_B_DIM0_ODT0
6 M_B_DIM0_ODT1

7 M_VREF_CA_DIMM1
7 M_VREF_DQ_DIMM1

14,37 DDR3_DRAMRST#

DDR_VREF_S3

R1504 0R2J-2-GP

M_VREF_CA_DIMM1

C1523 SCD1U10V2KX-5GP
C1524 SC2D2U10V3KX-1GP DY
C1522 SCD1U10V2KX-5GP

DDR_VREF_S3

R1503 0R2J-2-GP

M_VREF_DQ_DIMM1

C1515 SCD1U10V2KX-5GP
C1516 SC2D2U10V3KX-1GP DY
C1517 SCD1U10V2KX-5GP

0D75V_S0

Place these caps close to VTT1 and VTT2.

C1518 SC1U6D3V2KX-GP
C1519 SC1U6D3V2KX-GP
C1520 SC1U6D3V2KX-GP DY
C1521 SC1U6D3V2KX-GP

0D75V_S0

H = 5.2mm

2nd = 62.10017.T01
3rd = 62.10017.T51
DDR3-204P-83-GP
62.10017.T91

3D3V_S0

R1501 10KR2J-3-GP
R1502 10KR2J-3-GP

SA1_DIM1
SA0_DIM1

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

3D3V_S0

C1501 SCD1U10V2KX-5GP
C1502 SC2D2U10V3KX-1GP DY

1D5V_S3

SODIMM B DECOUPLING

C1503 SC10U10V5ZY-1GP DY
C1504 SC10U10V5ZY-1GP DY
C1505 SC10U6D3V5KX-1GP
C1506 SC10U6D3V5KX-1GP
C1507 SC10U6D3V5KX-1GP
C1508 SC10U10V5ZY-1GP DY
C1509 SC10U6D3V5KX-1GP
C1510 SC10U6D3V5KX-1GP DY

C1511 SCD1U10V2KX-5GP
C1512 SCD1U10V2KX-5GP
C1513 SCD1U10V2KX-5GP
C1514 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMB.

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 15 of 94

(Blanking)

<Core Design>

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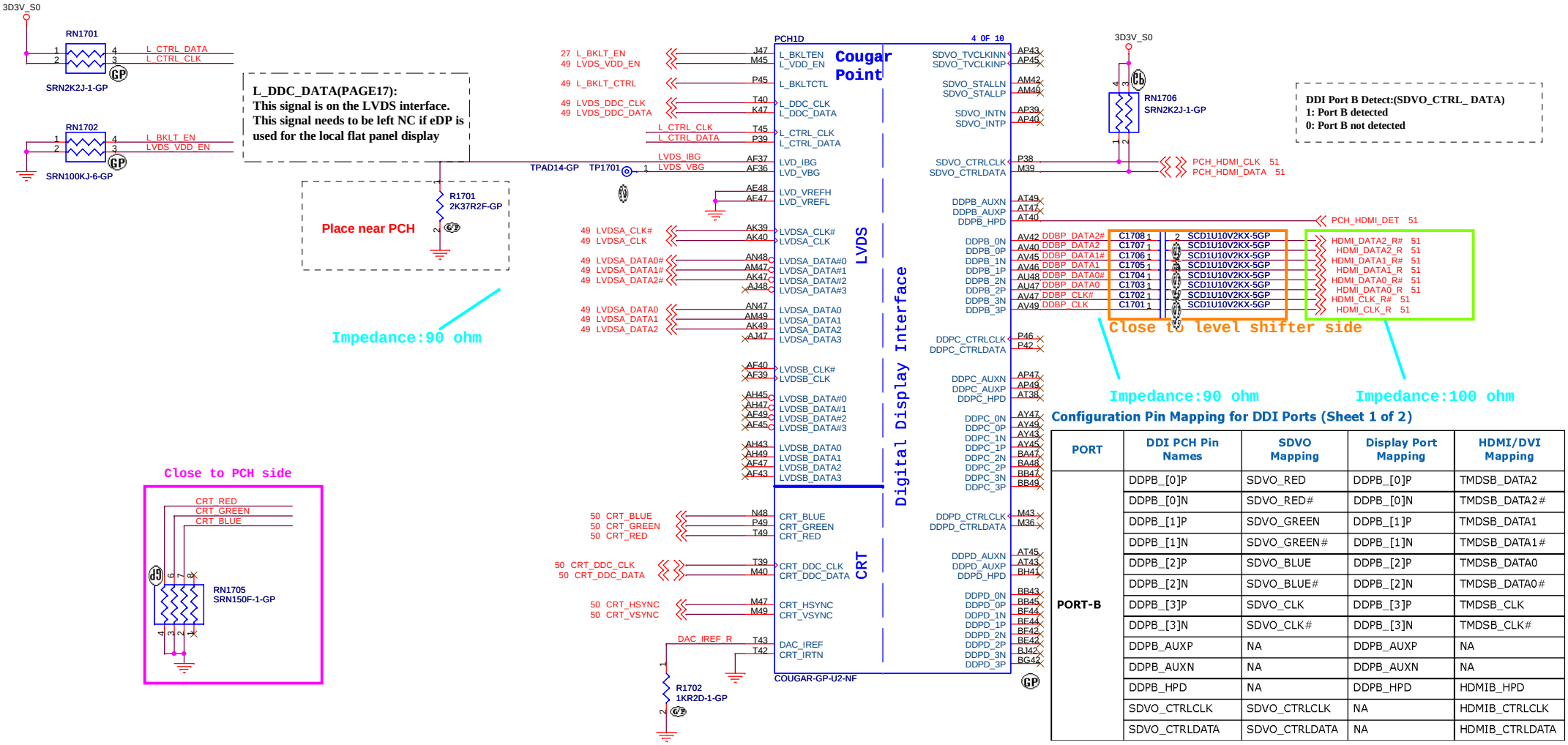
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	**LLW-1 / LGG-1**	**SB**

Date: Tuesday, November 09, 2010 Sheet 16 of 94



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

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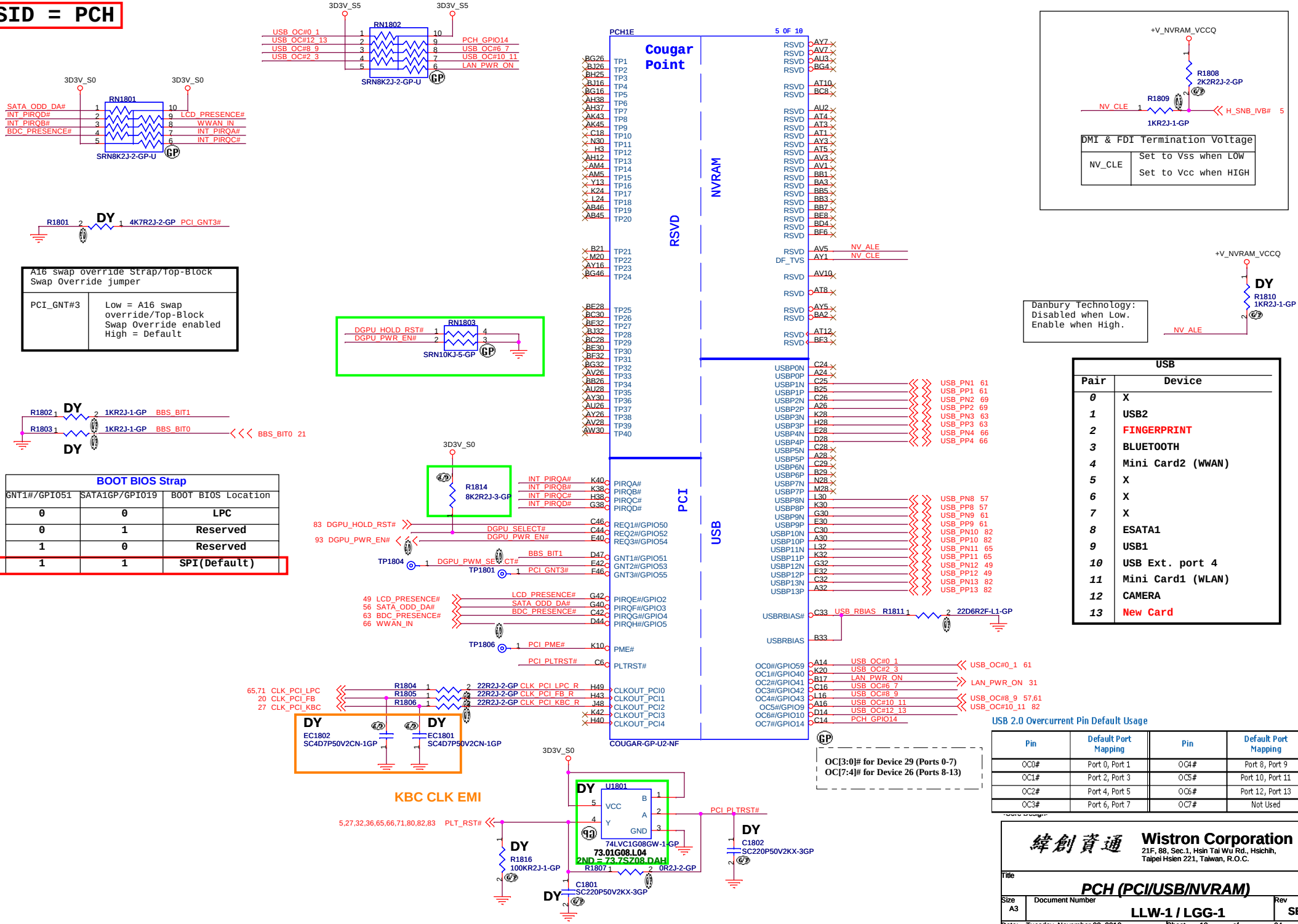
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB

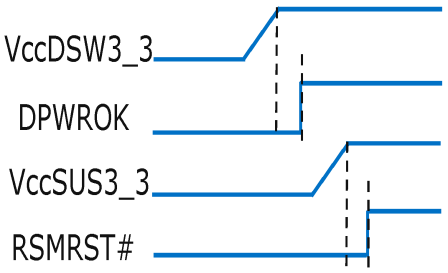
Date: Tuesday, November 09, 2010 | Sheet 17 of 94

SSID = PCH

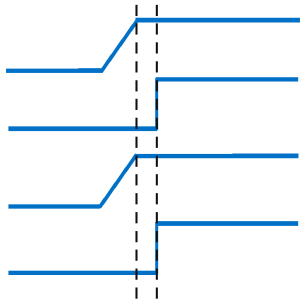

RN1802
SRN8K2J-2-GP-U
RN1801
SRN8K2J-2-GP-U
R1801 DY 4K7R2J-2-GP PCI_GNT3#
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT3# Low = A16 swap override/Top-Block Swap Override enabled High = Default
RN1803
SRN10KJ-5-GP
R1802 DY 1KR2J-1-GP BBS_BIT1
R1803 DY 1KR2J-1-GP BBS_BIT0
BOOT BIOS Strap
GNT1#/GPIO51 SATA1GP/GPIO19 BOOT BIOS Location
0 0 LPC
0 1 Reserved
1 0 Reserved
1 1 SPI(Default)
R1814 8K2R2J-3-GP
TP1804
TP1801
TP1806
EC1802 DY SC4D7P50V2CN-1GP
EC1801 DY SC4D7P50V2CN-1GP
KBC CLK EMI
U1801 74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
R1816 DY 100KR2J-1-GP
R1807 0R2J-2-GP
C1801 DY SC220P50V2KX-3GP
C1802 DY SC220P50V2KX-3GP
PCH1E
Cougar Point
RSVD
NVRAM
PCI
USB
COUGAR-GP-U2-NF
5 OF 10
OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)
+V_NVRAM_VCCQ
R1808 2K2R2J-2-GP
R1809 1KR2J-1-GP
NV_CLE
H_SNB_IVB# 5
DMI & FDI Termination Voltage
NV_CLE Set to Vss when LOW
Set to Vcc when HIGH
R1810 DY 1KR2J-1-GP
NV_ALE
Danbury Technology:
Disabled when Low.
Enable when High.
USB
Pair Device
0 X
1 USB2
2 FINGERPRINT
3 BLUETOOTH
4 Mini Card2 (WWAN)
5 X
6 X
7 X
8 ESATA1
9 USB1
10 USB Ext. port 4
11 Mini Card1 (WLAN)
12 CAMERA
13 New Card
USB 2.0 Overcurrent Pin Default Usage
Pin Default Port Mapping Pin Default Port Mapping
OC0# Port 0, Port 1 OC4# Port 8, Port 9
OC1# Port 2, Port 3 OC5# Port 10, Port 11
OC2# Port 4, Port 5 OC6# Port 12, Port 13
OC3# Port 6, Port 7 OC7# Not Used
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title PCH (PCI/USB/NVRAM)
Size A3 Document Number LLW-1 / LGG-1 Rev SB
Date: Tuesday, November 09, 2010 Sheet 18 of 94

SSID = PCH

Deep S4/S5 Supported



Deep S4/S5 **Not** Supported



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

4 DMI_RXN[3..0]
4 DMI_RXP[3..0]
4 DMI_TXN[3..0]
4 DMI_TXP[3..0]

FDI_TXN[7:0] 4
FDI_TXP[7:0] 4

PCH1C — 3 OF 10 — Cougar Point

DMI: DMI0RXN BC24, DMI1RXN BE20, DMI2RXN BG18, DMI3RXN BG20; DMI0RXP BE24, DMI1RXP BC20, DMI2RXP BJ18, DMI3RXP BJ20; DMI0TXN AW24, DMI1TXN AW20, DMI2TXN BB18, DMI3TXN AV18; DMI0TXP AY24, DMI1TXP AY20, DMI2TXP AY18, DMI3TXP AU18; DMI_ZCOMP BJ24, DMI_IRCOMP BG25, DMI2RBIAS BH21

FDI: FDI_RXN0 BJ14, FDI_RXN1 AY14, FDI_RXN2 BE14, FDI_RXN3 BH13, FDI_RXN4 BC12, FDI_RXN5 BJ12, FDI_RXN6 BG10, FDI_RXN7 BG9; FDI_RXP0 BG14, FDI_RXP1 BB14, FDI_RXP2 BF14, FDI_RXP3 BG13, FDI_RXP4 BE12, FDI_RXP5 BG12, FDI_RXP6 BJ10, FDI_RXP7 BH9; FDI_INT AW16, FDI_FSYNC0 AV12, FDI_FSYNC1 BC10, FDI_LSYNC0 AV14, FDI_LSYNC1 BB10

System Power Management: DSWVRMEN A18 DSWODVREN; DPWROK E22 PCH_DPWROK; WAKE# B9 PCIE_WAKE#; CLKRUN#/GPIO32 N3 PM_CLKRUN#; SUS_STAT#/GPIO61 G8 PM_SUS_STAT#; SUSCLK/GPIO62 N14 SUS_CLK; SLP_S5#/GPIO63 D10 PM_SLP_S5#; SLP_S4# H4 SLP_S4#_R; SLP_S3# F4 SLP_S3#_R; SLP_A# G10 PM_SLP_A#; SLP_SUS# G16 PM_SLP_SUS#; PMSYNCH AP14 H_PM_SYNC; SLP_LAN#/GPIO29 K14 PM_SLP_LAN#

SUSACK# C12 SUS_PWR_ACK; SYS_RESET# K3; SYS_PWROK P12; PWROK L22; APWROK L10 MEPWROK; DRAMPWROK B13; RSMRST# C21 PM_RSMRST#; SUSWARN#/SUSPWRDNACK/GPIO30 K16 SUS_PWR_ACK; PWRBTN# E20; ACPRESENT/GPIO31 H20 AC_PRESENT; BATLOW#/GPIO72 E10 BATLOW#; RI# A10 PM_RI#

COUGAR-GP-U2-NF

SYS_PWROK — DY R1926 10KR2J-3-GP — R1904 100KR2J-1-GP — PWROK

1D05V_VTT — R1901 49D9R2F-GP DMI_COMP_R — R1902 750R2F-GP RBIAS_CPY

3D3V_S0

SUS_PWR_ACK — R1903 DY 0R2J-2-GP — SUSACK# C12

5,11 XDP_DBRESET# — R1925 DY 0R2J-2-GP — SYS_RESET# K3

R1905 10KR2J-3-GP

36 SYS_PWROK — R1923 DY 0R2J-2-GP — PWROK L22

27,36 S0_PWR_GOOD — R1924 0R2J-2-GP
42,48 D85V_PWRGD — R1927 0R2J-2-GP

R1906 0R2J-2-GP — MEPWROK L10

36,37,45,46,47 RUNPWROK — R1907 DY 0R2J-2-GP

5,37 PM_DRAM_PWRGD — B13

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

11 PM_RSMRST# — PM_RSMRST# C21

27 SUS_PWR_ACK — SUS_PWR_ACK K16

27 PM_PWRBTN# — E20

27 AC_PRESENT — AC_PRESENT H20

20 BATLOW# — E10

20 PM_RI# — A10

RTC_AUX_S5 — R1911 DY 10KR2J-3-GP — R1910 0R2J-2-GP — PM_RSMRST#

PCH_DPWROK — PCIE_WAKE# 65,82

PM_CLKRUN# 27

TP1901 TPAD14-GP

R1913 0R2J-2-GP — PCH_SUSCLK_KBC 27

TP1902 TPAD14-GP

R1914 0R2J-2-GP — PM_SLP_S4# 27,46,82

R1915 0R2J-2-GP — PM_SLP_S3# 27,36,37,47,82

TP1903TPAD14-GP

TP1904TPAD14-GP

H_PM_SYNC 5

TP1905TPAD14-GP

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5 — R1917 330KR2J-L1-GP — DSWODVREN — R1918 DY 330KR2J-L1-GP

3D3V_S0 — PM_CLKRUN# R1919 8K2R2J-3-GP

3D3V_S5 — RN1901 SRN10KJ-6-GP — AC_PRESENT, SUS_PWR_ACK — PEG_B_CLK_RQ# 20

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

R1921 10KR2J-3-GP PCIE_WAKE#
DY R1922 10KR2J-3-GP PM_PWRBTN#
R1920 10KR2J-3-GP PM_SLP_LAN#

Need Check!!

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

R1908 10KR2J-3-GP PM_RSMRST#

3D3V_AUX_S5 — R1909 100KR2J-1-GP — R1916 10KR2J-3-GP — 3V_5V_POK_# — Q1901 2N7002KDW-GP — PM_RSMRST# R1912 1KR2J-1-GP — RSMRST#_KBC 27 — 3V_5V_POK 41

84.2N702.A3F
2nd = 84.DM601.03F

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DMI/FDI/PM)**

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 19 of 94

SSID = PCH

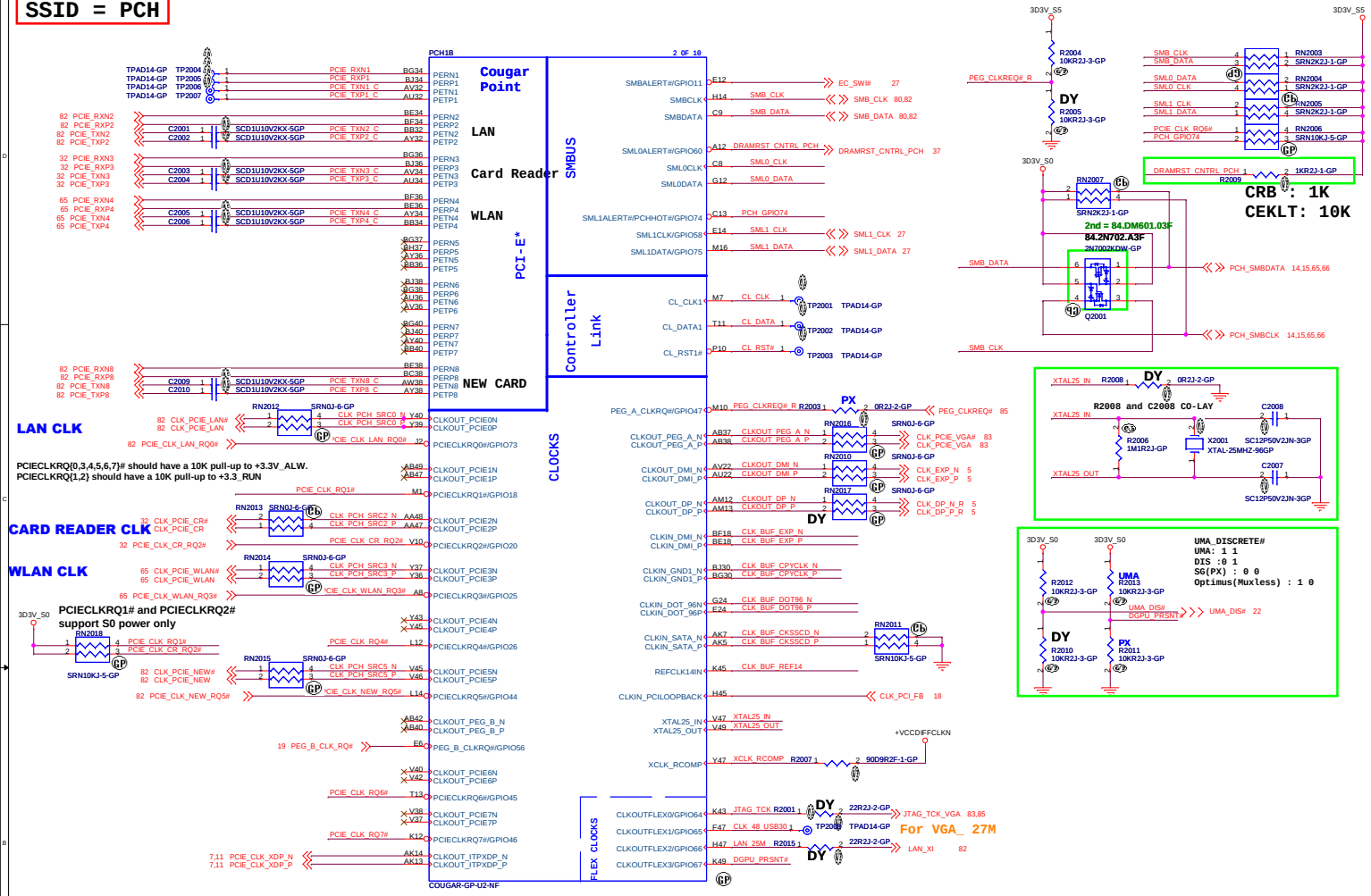


Table 20.1- Dual N-Channel MOSFET multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
PANJIT	2N7002KDW	N/A	84.2N702.A3F
DIODES	DMN601DWK-7	N/A	84.DM601.03F
NXP	2N7002BKS	N/A	84.2N702.E3F

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size: A2 | Document Number: **LLW-1 / LGG-1** | Rev: **SB**

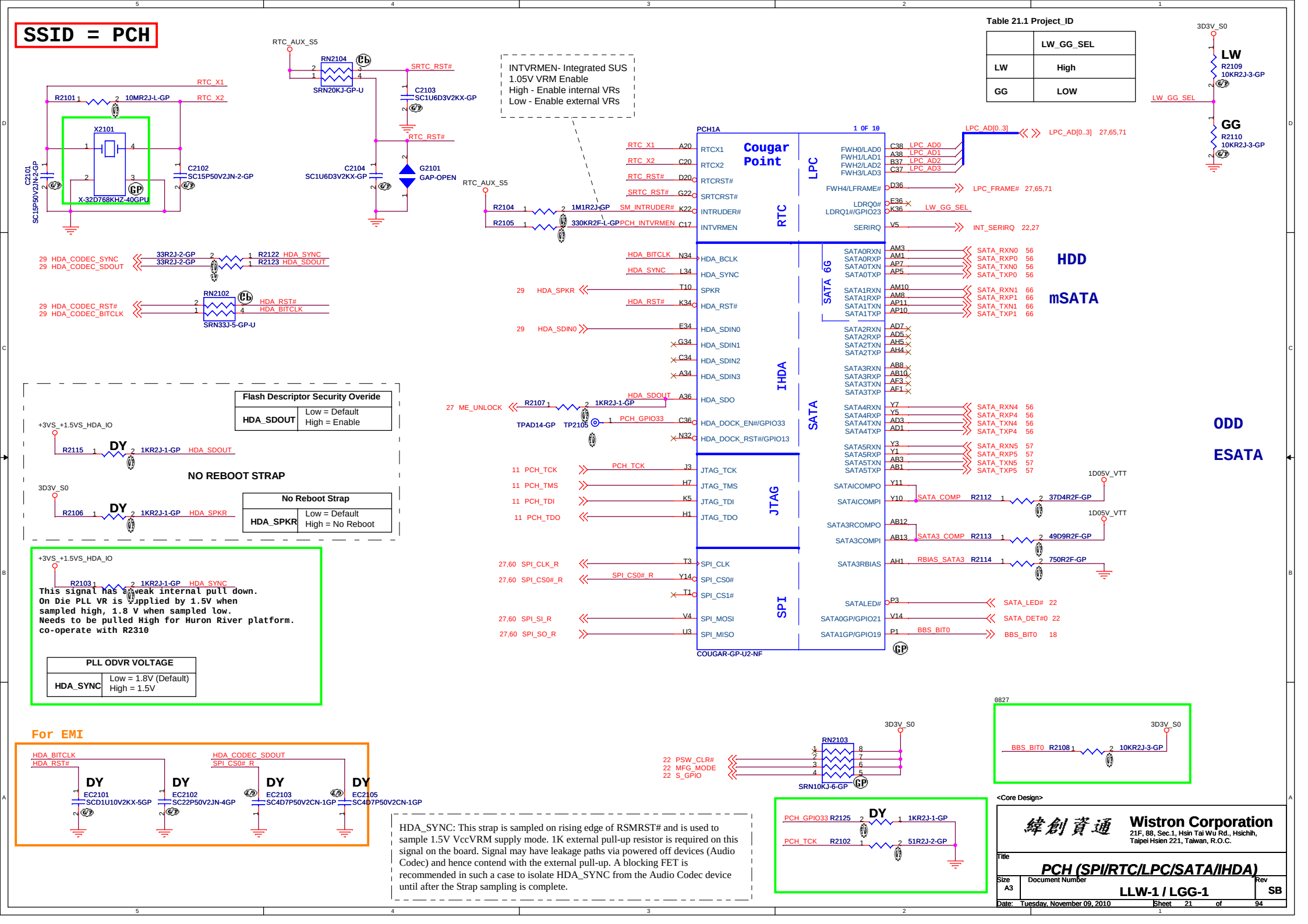
Date: Tuesday, November 09, 2010 | Sheet 20 of 94

SSID = PCH

Table 21.1 Project_ID

	LW_GG_SEL
LW	High
GG	LOW

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 21 of 94

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

GPIO27 has a weak[20K] internal pull up. To enable on-die PLL Voltage regurator, should not place external pull down.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

20100723 V1.62

<Core Design>

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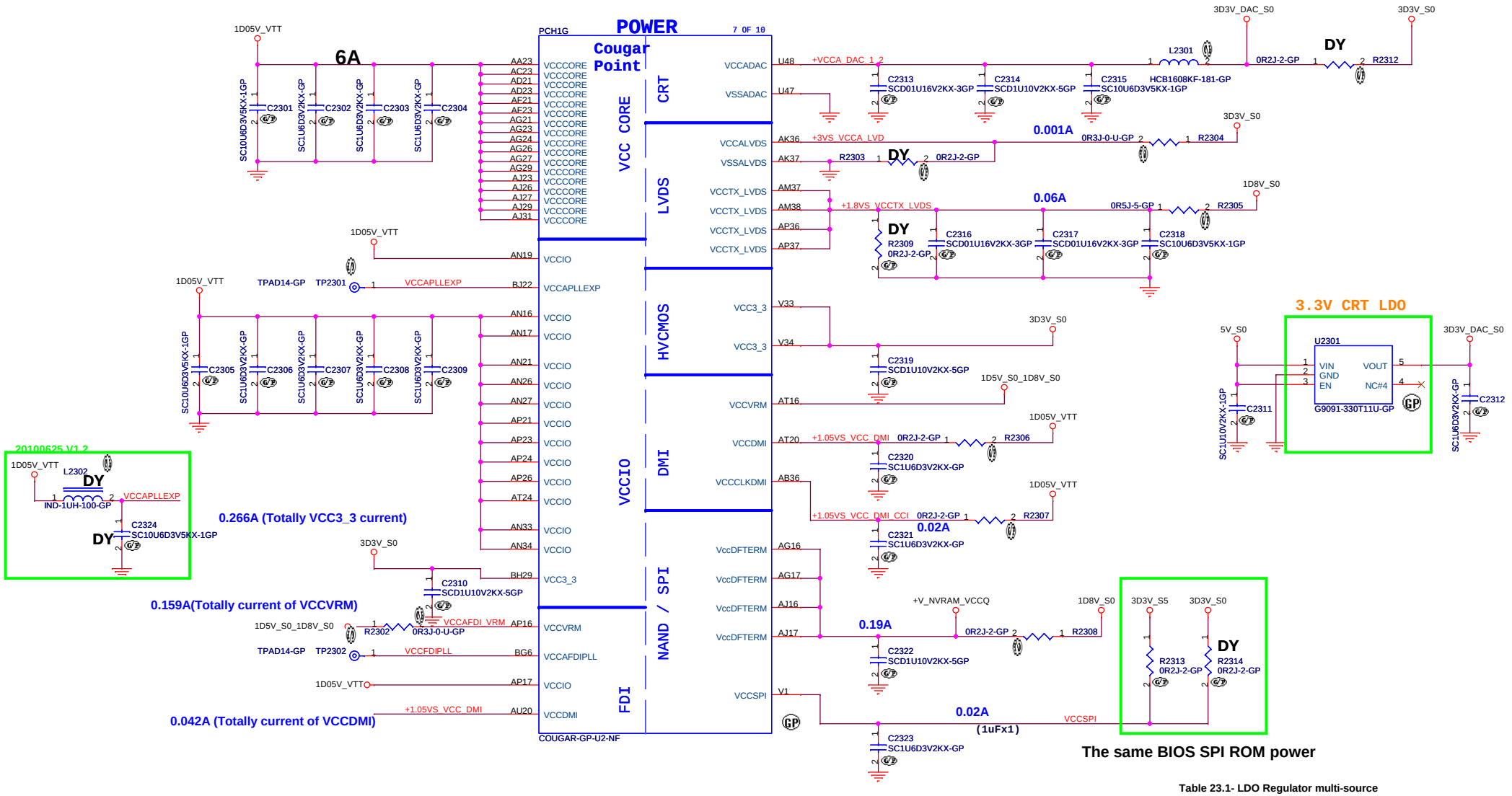
Title: **PCH (GPIO/CPU)**

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 22 of 94

SSID = PCH



VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop
co-operate with R2103

Table 23.1- LDO Regulator multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
GMT	G9091-330T11U	N/A	74.09091.J3F
RICHTEK	RT9198-33GBR	N/A	74.09198.Q7F

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 23 of 94

SSID = PCH

POWER

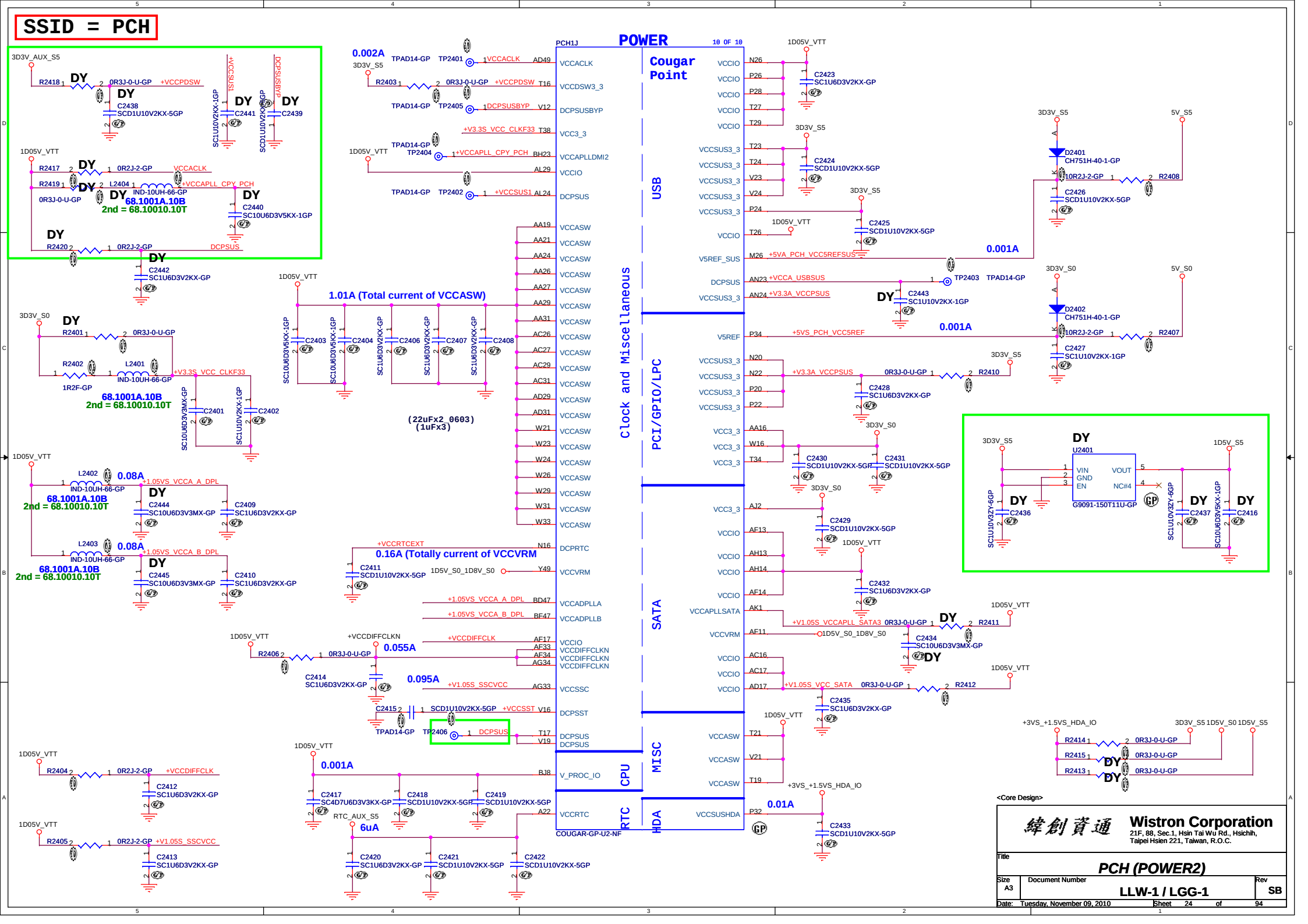
Cougar Point

PCH1J

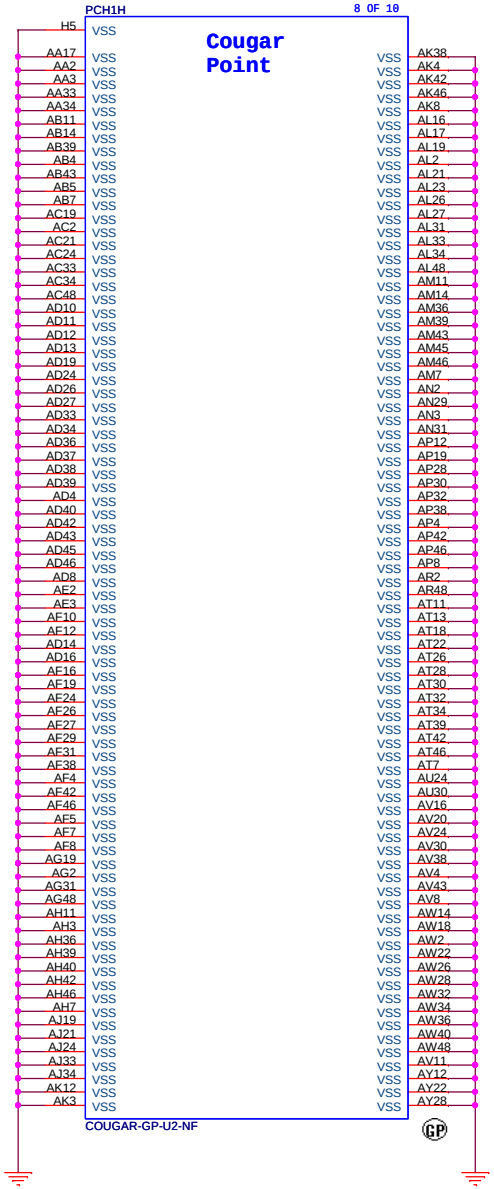
COUGAR-GP-U2-NF

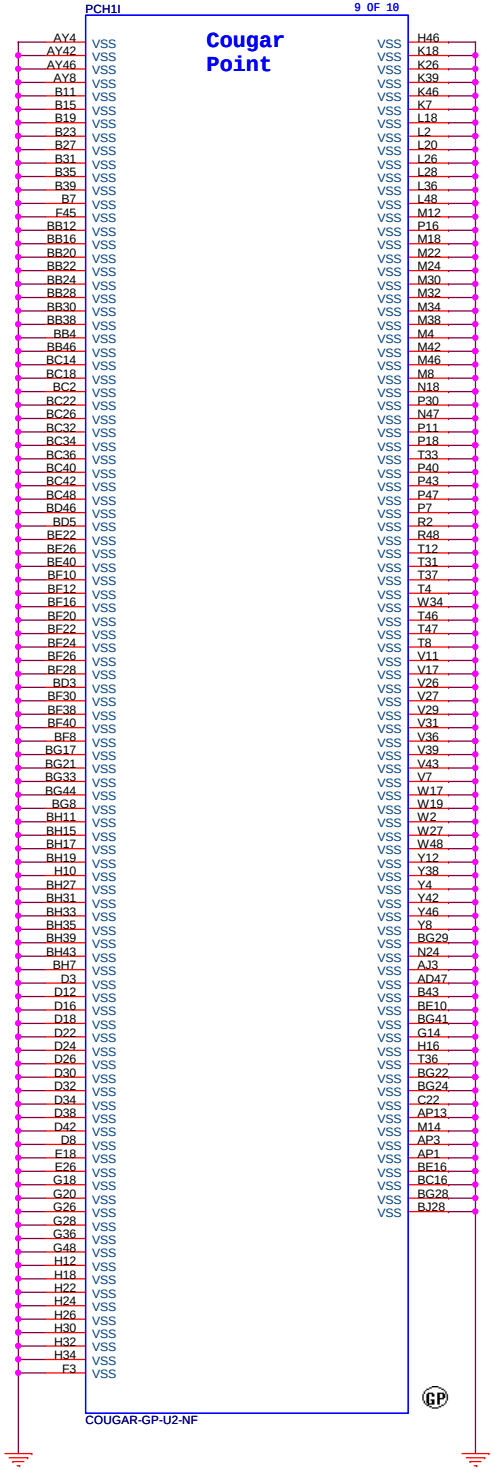
10 OF 10

USB | Clock and Miscellaneous | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA



SSID = PCH





<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 25 of 94

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

Size	Document Number	Rev
A4	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 26 of 94

SSID = KBC

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.48 V
-1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

BOM Ctrl

G Sensor ID:
High: ST
Low:ADI

NOTE:
PWM Signal :
1. If unused, select altrnative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

<------ TP
<------ BATTERY / CHARGER
<------ PCH / eDP

R2701 and C2716
Need very close to EC

NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 6500mils,. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE:
C2712 must place close to VCORF pin.

NOTE:
Please place R2711 close to AGND pin.

Prevent BIOS data loss solution

84.T3906.A11
2nd = 84.03906.F11

EC_GPIO47 High Active

84.2N702.J31
2nd = 84.2N702.031

EC GPIO standard PH/PL

84.2N702.A3F
2nd = 84.DM601.03F

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

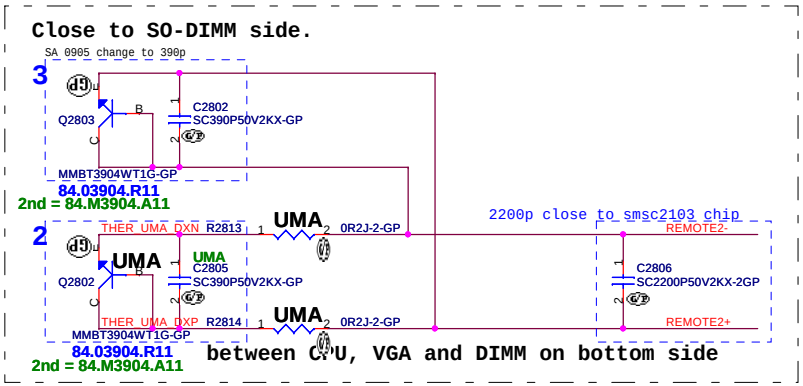
Title: KBC Nuvoton NPCE795

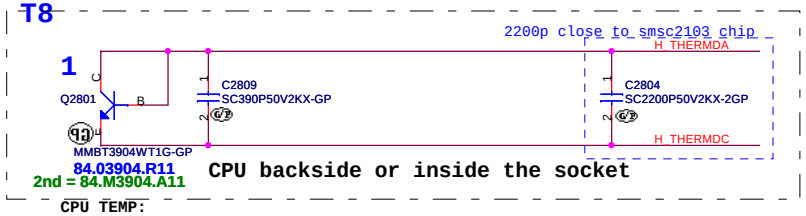
Size: A2 | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 27 of 94

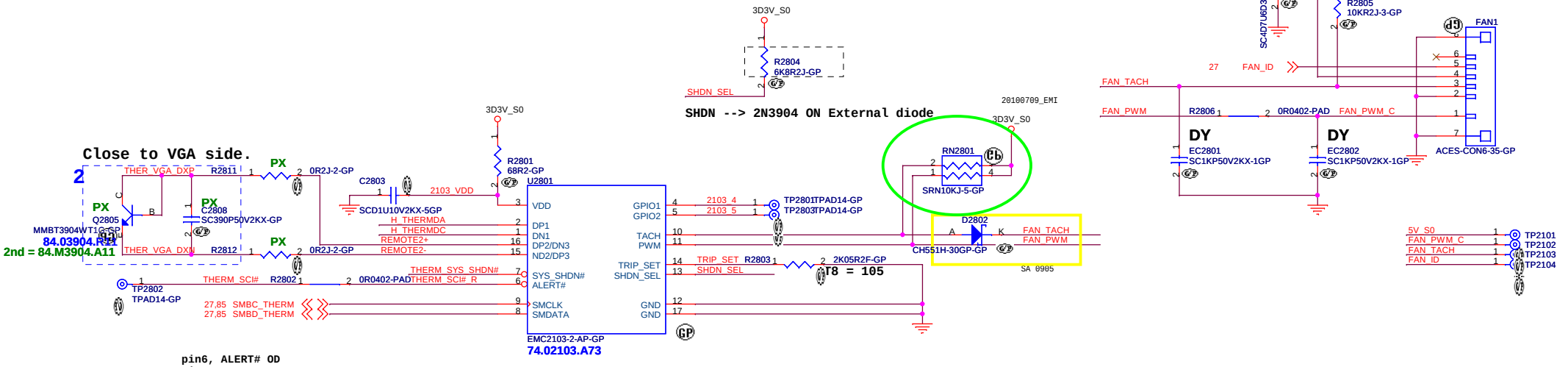
SSID = Thermal

Thermal sensor





CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.



pin6, ALERT# OD
pin7, SYS_SHDN# OD

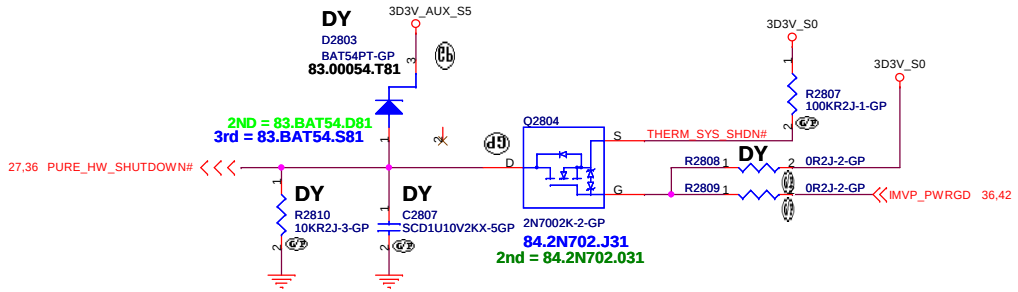


Table 28.1- General Purpose Transistors multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***THERMAL SENSOR SMSC EMC2103***

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 28 of 94

AUDIO CODEC

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

Port Configuration

Port A: Headphone jack
Port B:
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Internal stereo digital mic

JACK DETECT RESISTORS

Close to Pin36

SENSE PIN A

For EMI issue.

Should be used at least 20 MIL width copper line for "AUD_SPK_L+","AUD_SPK_L-", "AUD_SPK_R+", "AUD_SPK_R-

Place R2913/R2914 under CODEC, and place R2921/R2922 near CODEC

Place EMI components close to audio codec.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC

Size: A2 | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 29 of 94

<Core Design>

緯創資通 **Wistron Corporation**

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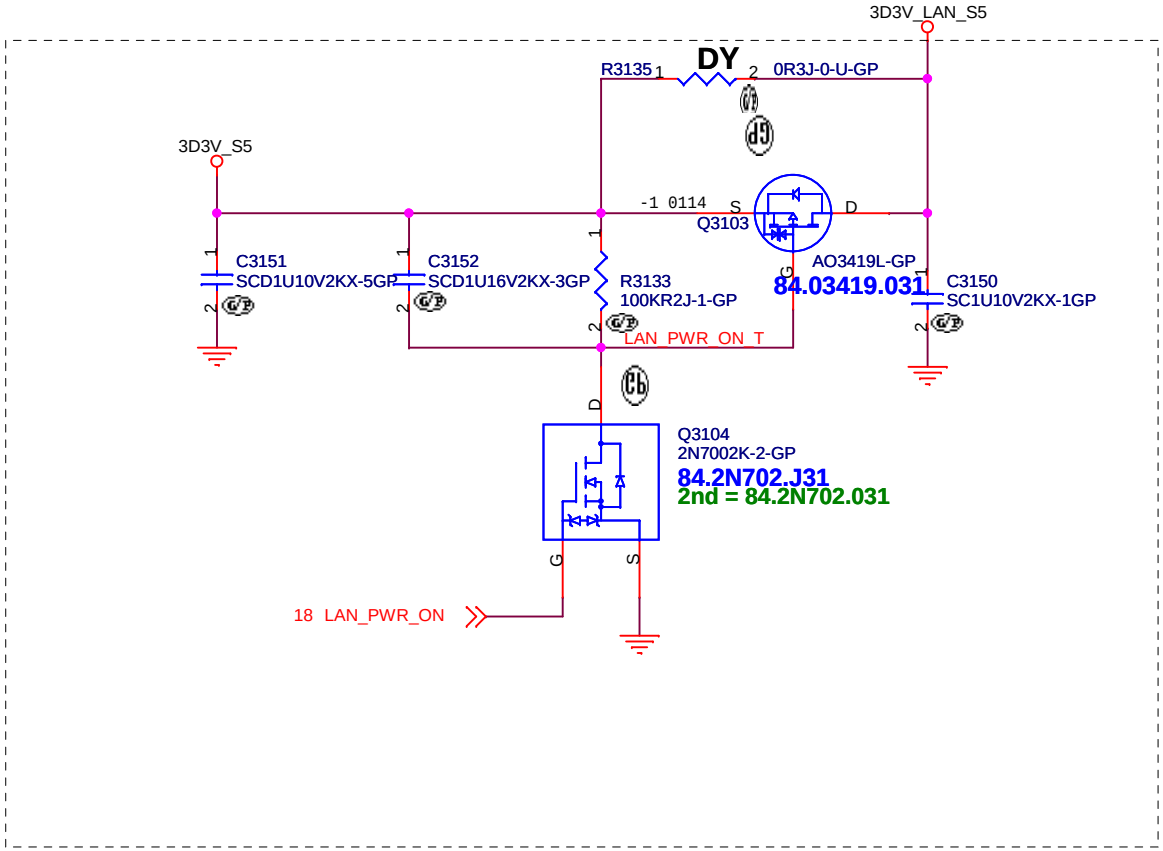
Title

AMP

Size	Document Number	Rev
A3	**LLW-1 / LGG-1**	**SB**

Date: Tuesday, November 09, 2010 Sheet 30 of 94



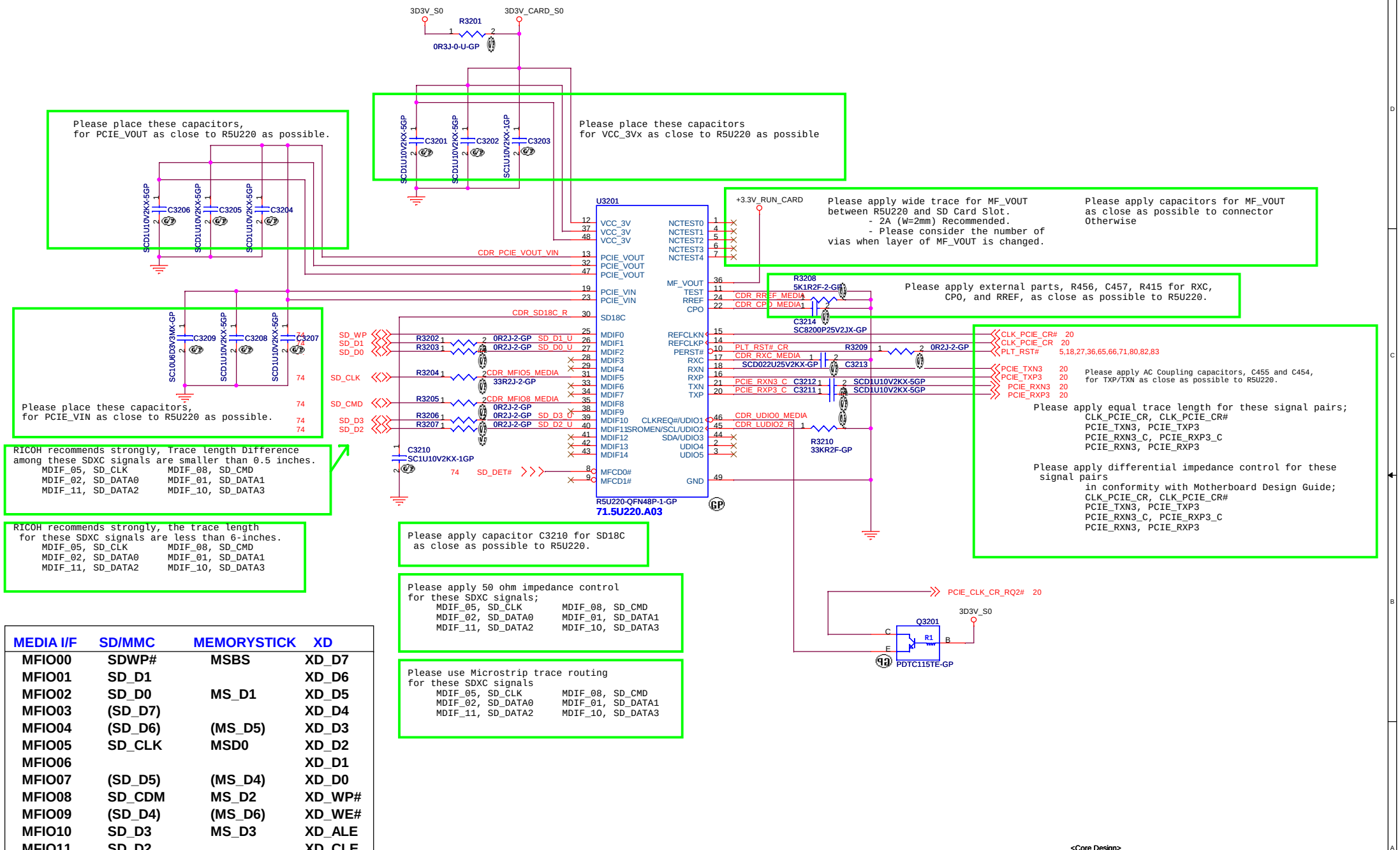
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN PWR SW***

Size	Document Number	Rev
A4	**LLW-1 / LGG-1**	**SB**

Date: Tuesday, November 09, 2010 Sheet 31 of 94



MEDIA I/F	SD/MMC	MEMORYSTICK	XD
MFIO00	SDWP#	MSBS	XD_D7
MFIO01	SD_D1		XD_D6
MFIO02	SD_D0	MS_D1	XD_D5
MFIO03	(SD_D7)		XD_D4
MFIO04	(SD_D6)	(MS_D5)	XD_D3
MFIO05	SD_CLK	MSD0	XD_D2
MFIO06			XD_D1
MFIO07	(SD_D5)	(MS_D4)	XD_D0
MFIO08	SD_CDM	MS_D2	XD_WP#
MFIO09	(SD_D4)	(MS_D6)	XD_WE#
MFIO10	SD_D3	MS_D3	XD_ALE
MFIO11	SD_D2		XD_CLE
MFIO12			XD_CE#
MFIO13		(MS_D7)	XD_RE#
MFIO14		MS_CLK	XD_R/B
MFCD0#	SDDC#		XDCD0#
MFCD1#		MSINS#	XDCD1#

<Core Design>

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Title: R5U220 (CARD READER)

Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 32 of 94

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	***1394***	
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 33 of 94	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Smart Card Reader***

Size	Document Number	Rev
A4	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 34 of 94

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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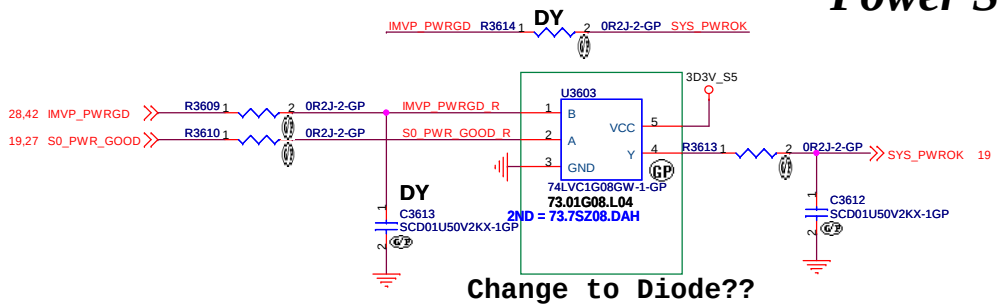
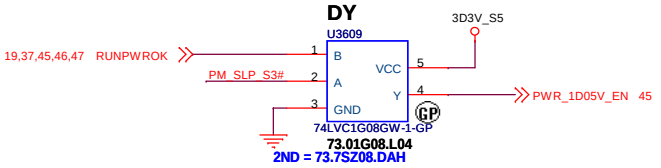
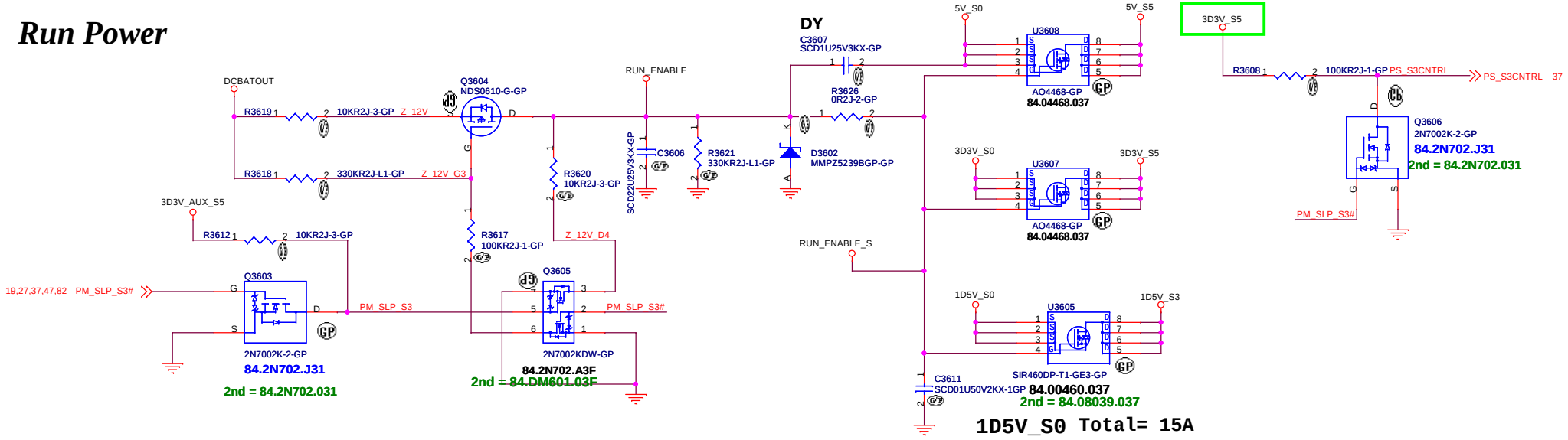
Title	***USB3.0***	
Size: A4	Document Number: **LLW-1 / LGG-1**	Rev: **SB**
Date: Tuesday, November 09, 2010	Sheet 35 of 94	

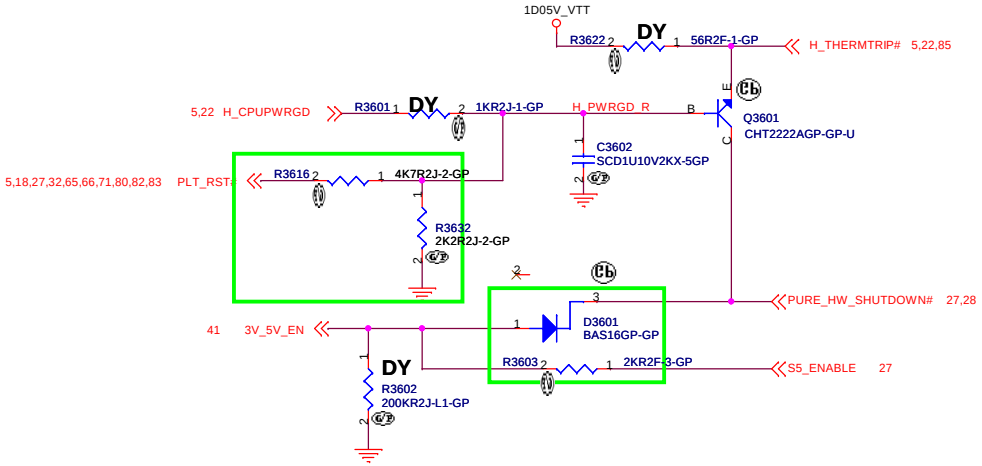
Power Sequence

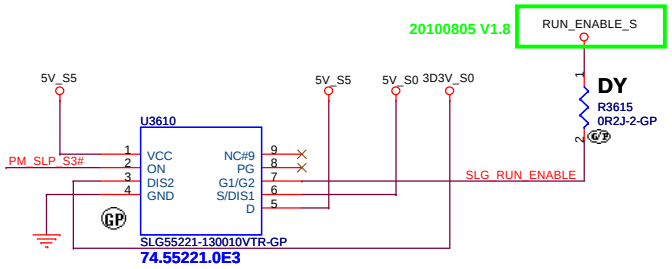




Run Power







<Core Design>

緯創資通 Wistron Corporation
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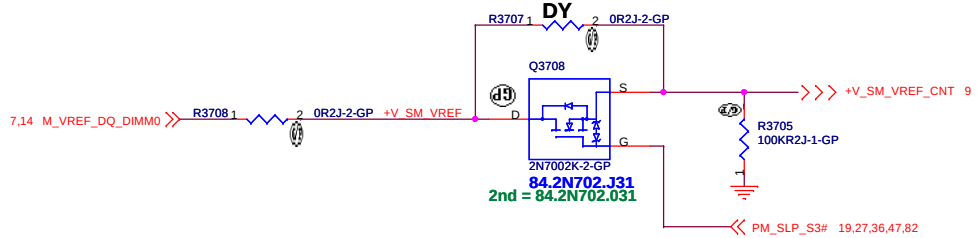
Title: **POWER SEQUENCE**

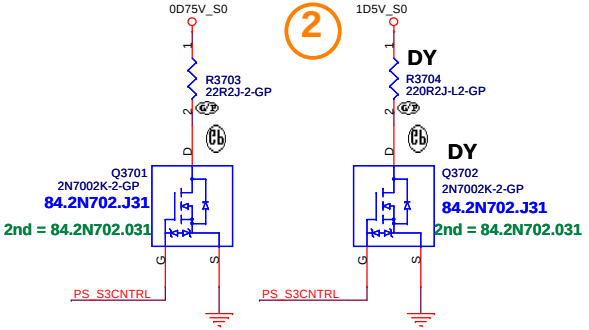
Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

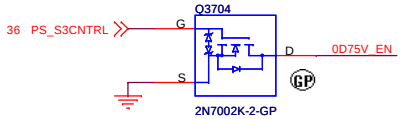
Date: Tuesday, November 09, 2010 Sheet 36 of 94

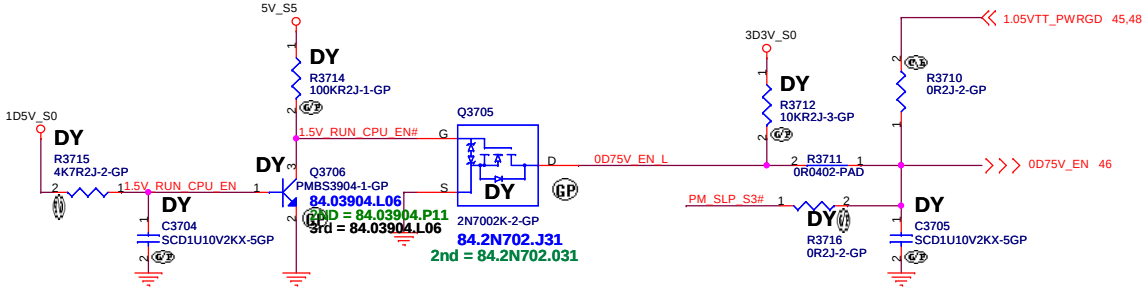
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



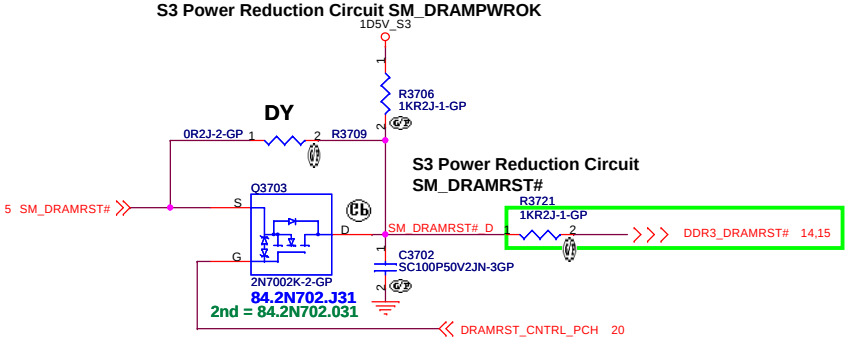
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



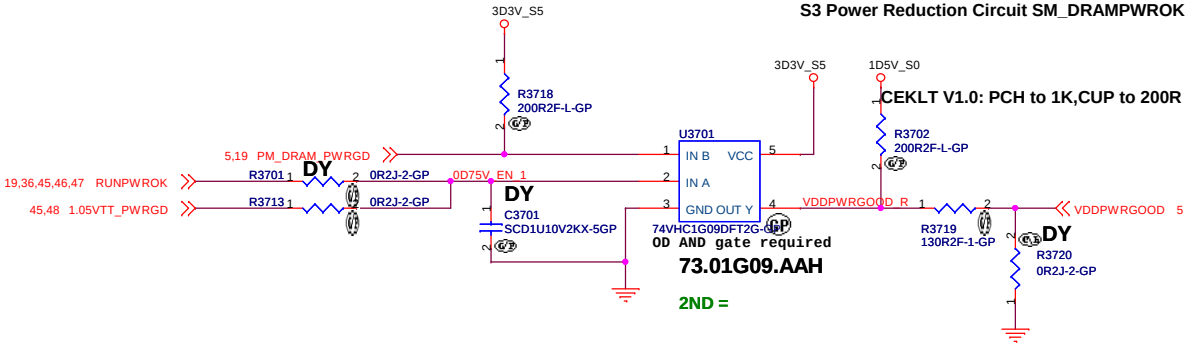




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

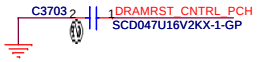


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time
over VDDQ * 0.55± 200mV and the edge must be monotonic



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER OCP / S3 reduction

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 37 of 94

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***DCIN_JACK***

Size	Document Number	Rev
	LLW-1 / LGG-1	**SB**

Date: Tuesday, November 09, 2010 Sheet 38 of 94

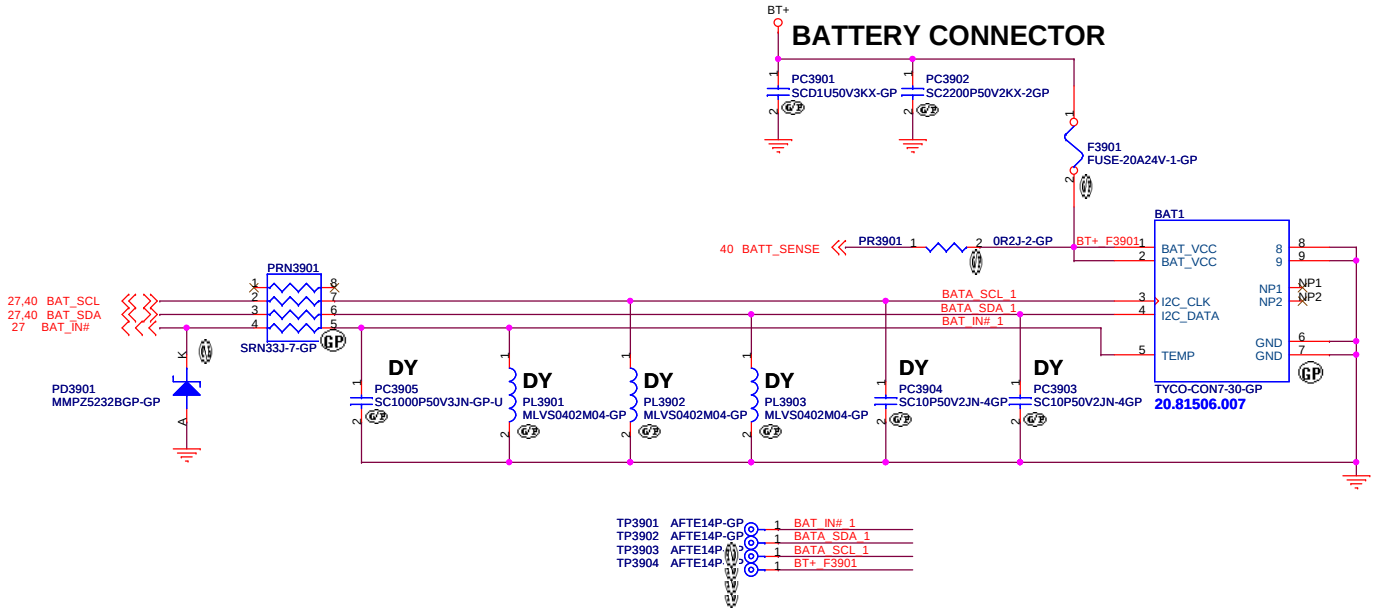


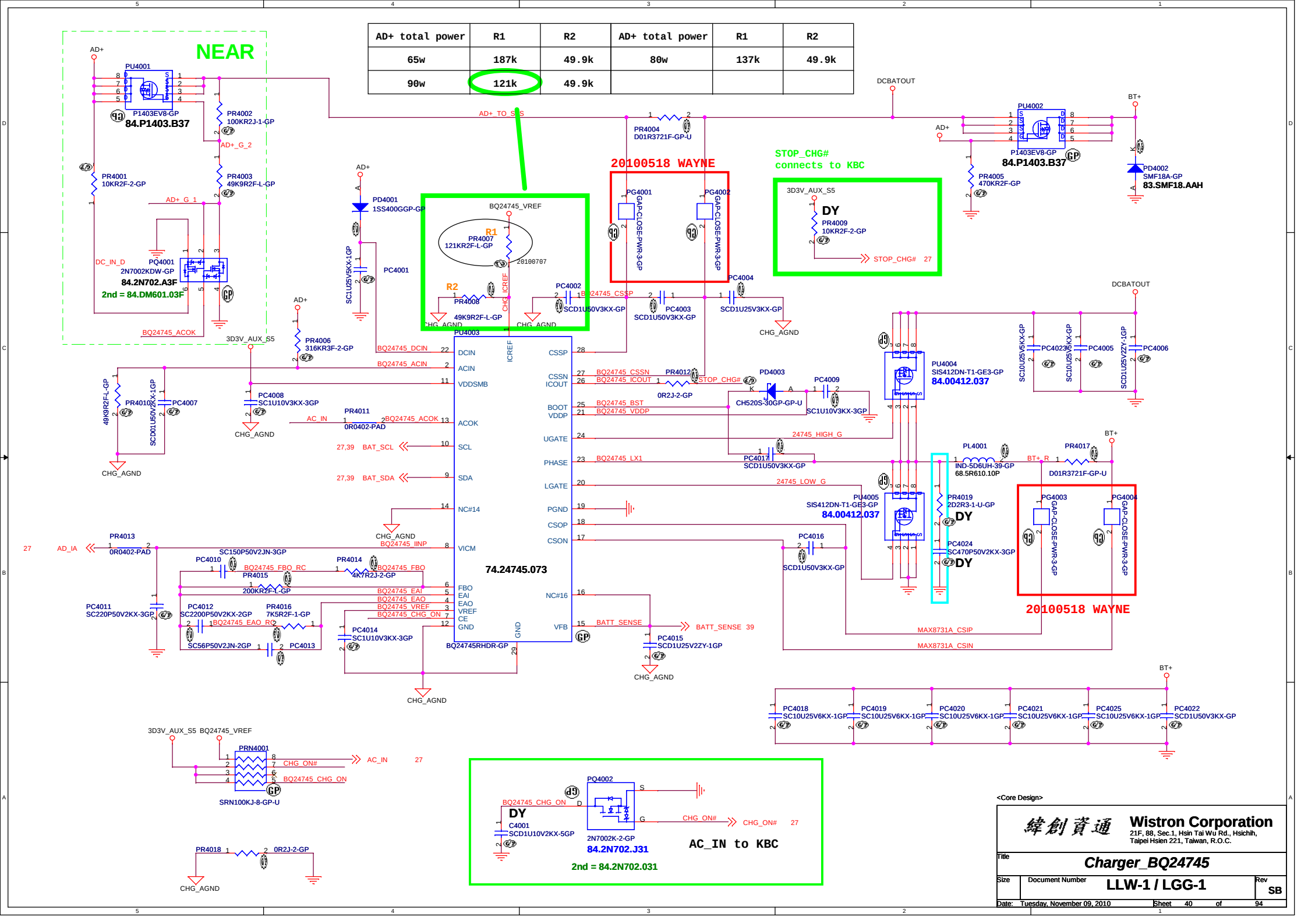
Table 39.1- Surface Mount Zener ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	MMPZ5232BGP	N/A	83.5R603.R3F
DIODES	MMSZ5232BS-7-F	N/A	83.5R603.K3F
PANJIT	MMSZ5232BS	N/A	83.5R603.Q3F

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	BATT_CONN	
Size	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 39 of 94	


NEAR
AD+ total power | R1 | R2 | AD+ total power | R1 | R2
65w | 187k | 49.9k | 80w | 137k | 49.9k
90w | 121k | 49.9k
20100518 WAYNE
STOP_CHG# connects to KBC
74.24745.073
BQ24745RHDR-GP
AC_IN to KBC
Wistron Corporation
Charger_BQ24745
LLW-1 / LGG-1

SSID = PWR.Plane.Regulator_5v3p3v

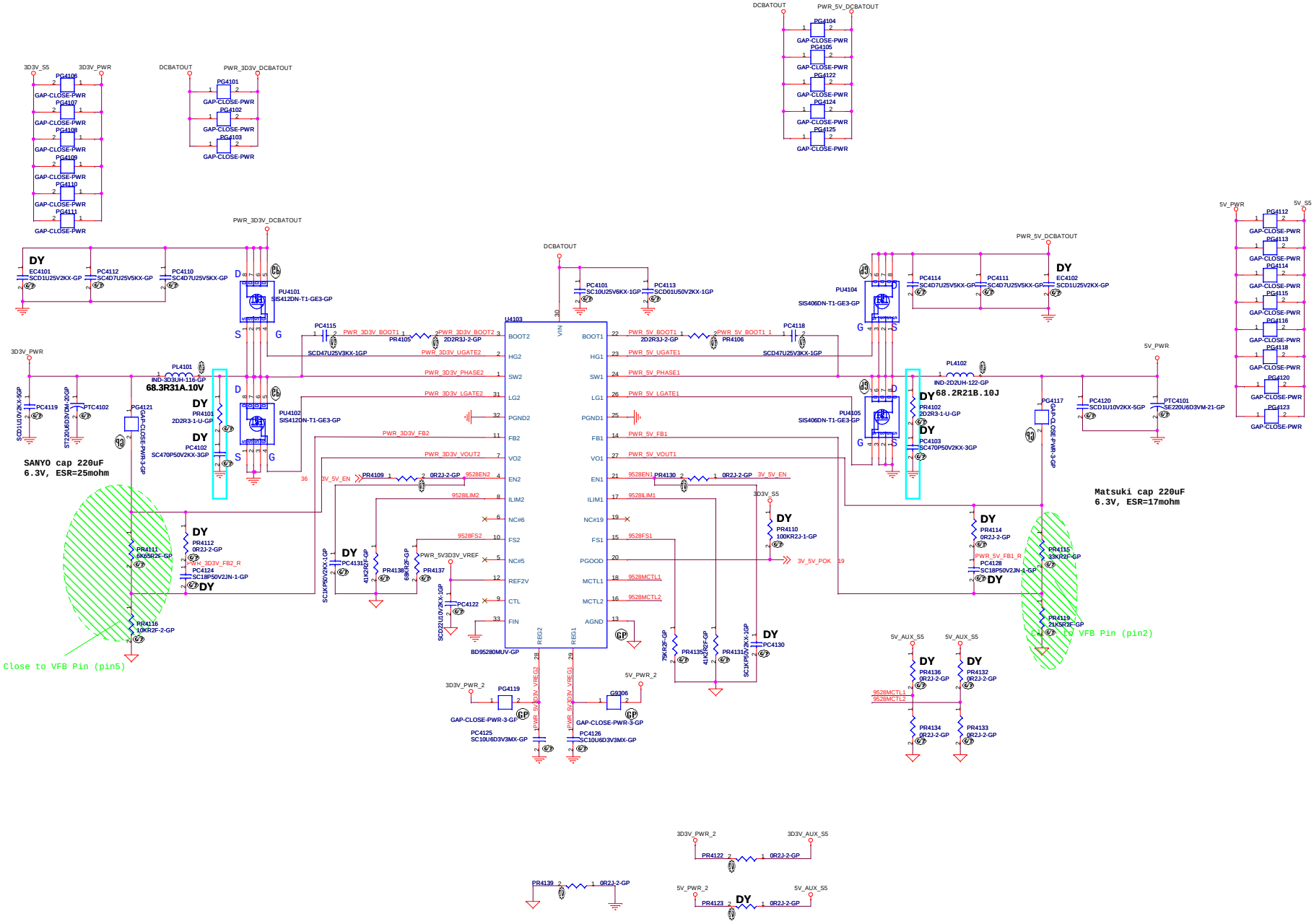


Table 41.1 - POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
SANYO	6TPE220MAP	N/A	77.22271.27L
NEC-TOKIN	V0J227M(25)12RE	N/A	77.C2271.00L

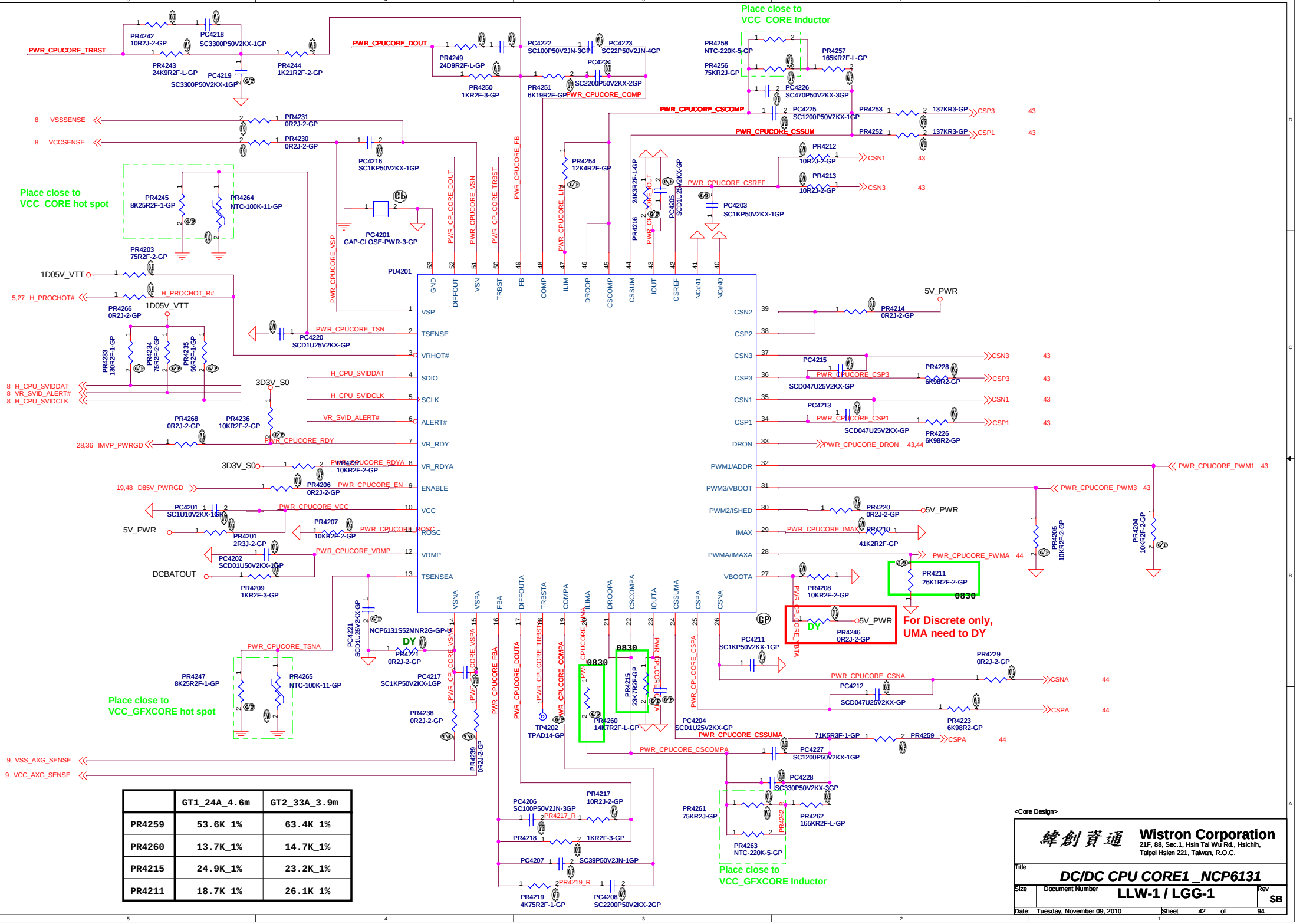
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 3D3V5V

Size | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 41 of 94



	GT1_24A_4.6m	GT2_33A_3.9m
PR4259	53.6K_1%	63.4K_1%
PR4260	13.7K_1%	14.7K_1%
PR4215	24.9K_1%	23.2K_1%
PR4211	18.7K_1%	26.1K_1%

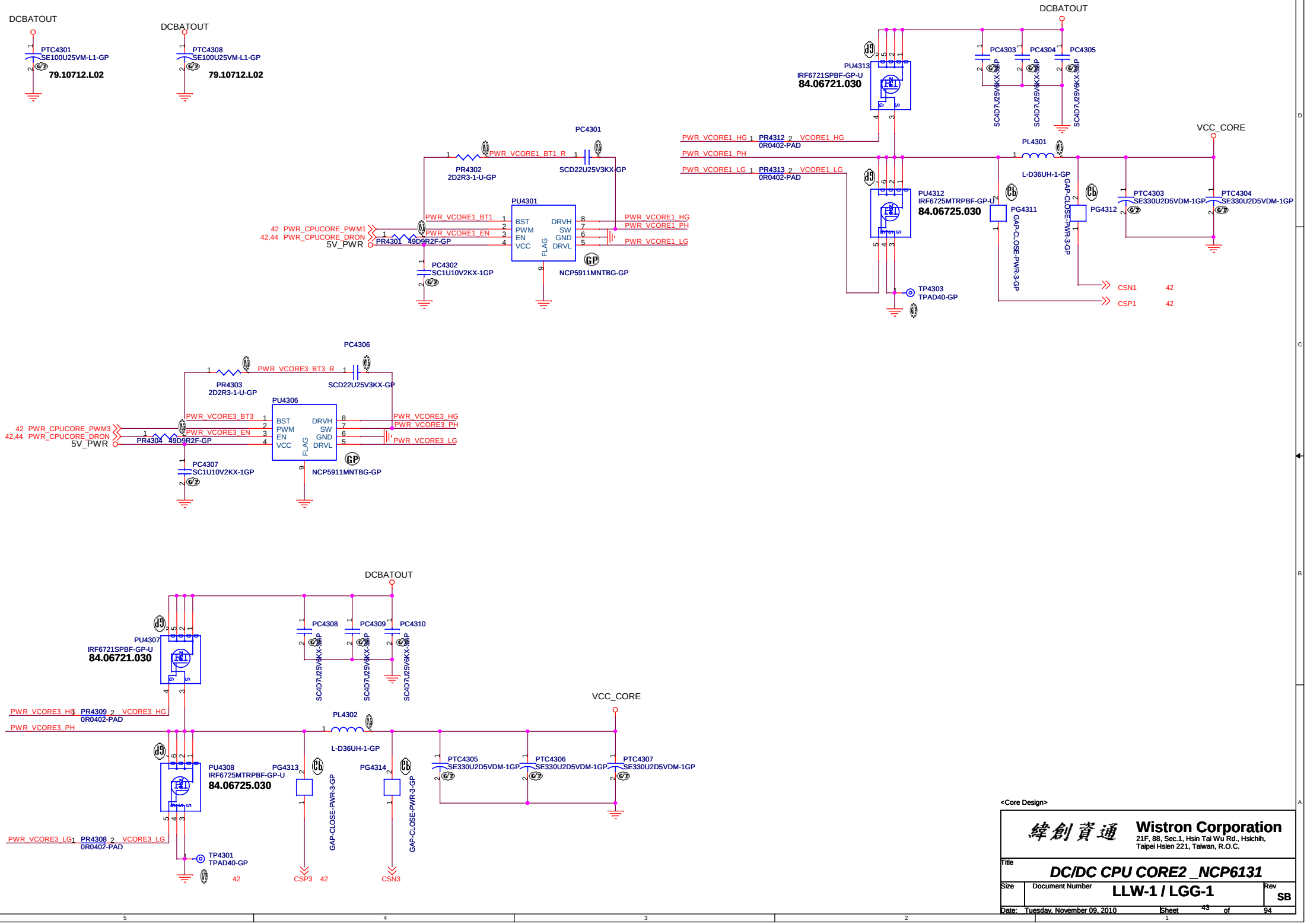
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC CPU CORE1 _NCP6131

Size: | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 42 of 94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SE100U25VM-L1-GP
79.10712.L02
DCBATOUT
PTC4308
SE100U25VM-L1-GP
79.10712.L02
PC4301
PWR_VCORE1_BT1_R
PR4302
2D2R3-1-U-GP
SCD22U25V3KX-GP
PU4301
42 PWR_CPUCORE_PWM1
42,44 PWR_CPUCORE_DRON
5V_PWR
PR4301 49D9R2F-GP
PWR_VCORE1_BT1
PWR_VCORE1_EN
BST
PWM
EN
VCC
FLAG
DRVH
SW
GND
DRVL
PWR_VCORE1_HG
PWR_VCORE1_PH
PWR_VCORE1_LG
PC4302
SC1U10V2KX-1GP
NCP5911MNTBG-GP
DCBATOUT
PU4313
IRF6721SPBF-GP-U
84.06721.030
PC4303
PC4304
PC4305
SC4D7U25V6KX-3GP
PWR_VCORE1_HG
PR4312
0R0402-PAD
VCORE1_HG
PWR_VCORE1_PH
PWR_VCORE1_LG
PR4313
0R0402-PAD
VCORE1_LG
PL4301
L-D36UH-1-GP
VCC_CORE
PU4312
IRF6725MTRPBF-GP-U
84.06725.030
PG4311
PG4312
GAP-CLOSE-PWR-3-GP
PTC4303
PTC4304
SE330U2D5VDM-1GP
TP4303
TPAD40-GP
CSN1
CSP1
42
PC4306
PWR_VCORE3_BT3_R
PR4303
2D2R3-1-U-GP
SCD22U25V3KX-GP
PU4306
42 PWR_CPUCORE_PWM3
42,44 PWR_CPUCORE_DRON
5V_PWR
PR4304 49D9R2F-GP
PWR_VCORE3_BT3
PWR_VCORE3_EN
PWR_VCORE3_HG
PWR_VCORE3_PH
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PTC4306
PTC4307
SE330U2D5VDM-1GP
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VCORE3_LG
TP4301
TPAD40-GP
42
CSP3
CSN3
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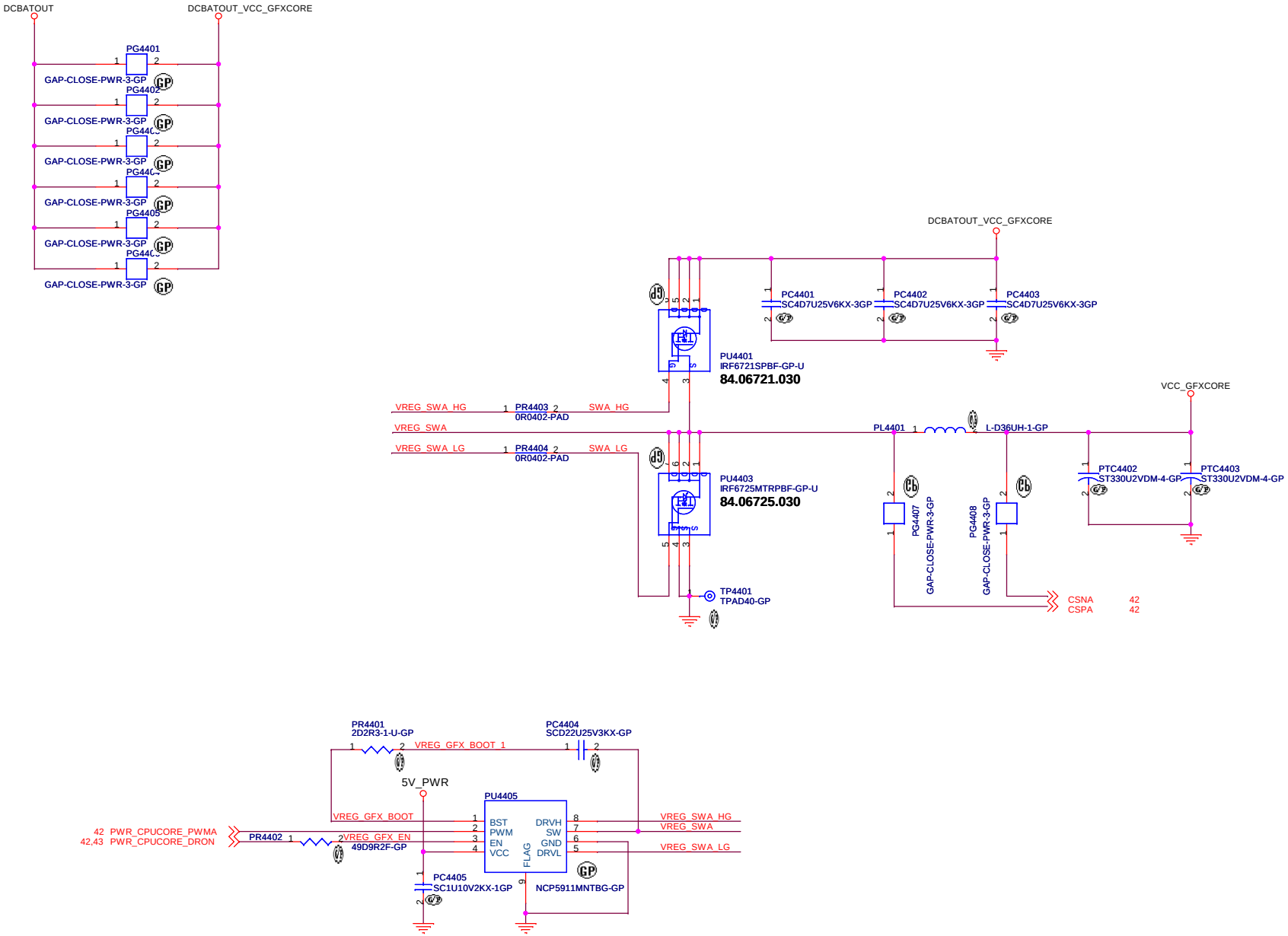
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC/DC CPU CORE2 _NCP6131
Size
Document Number
LLW-1 / LGG-1
Rev
SB
Date: Tuesday, November 09, 2010
Sheet 43 of 94



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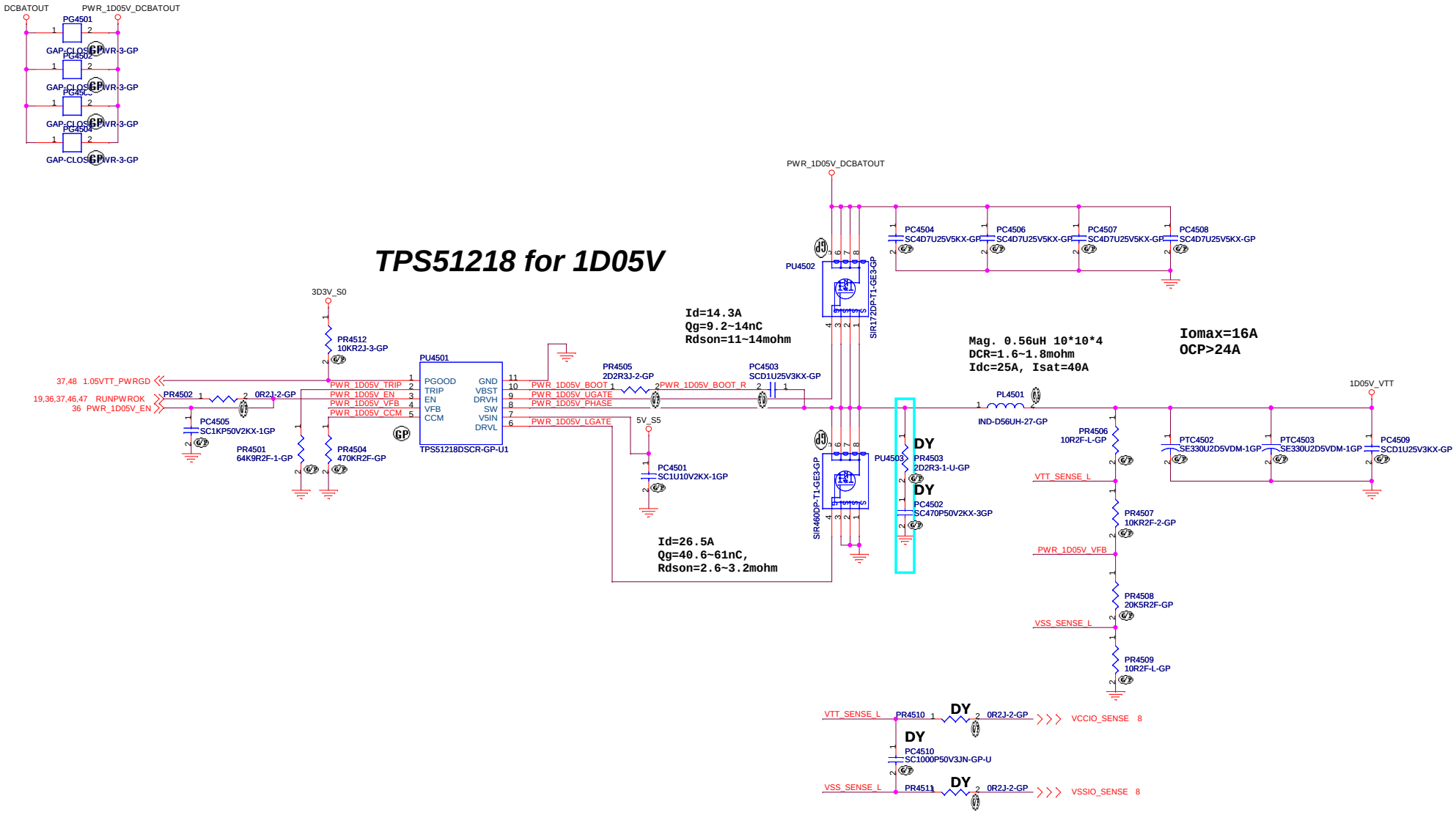
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC CPU CORE3 _NCP6131

Size | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 44 of 94



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Wistron Corporation
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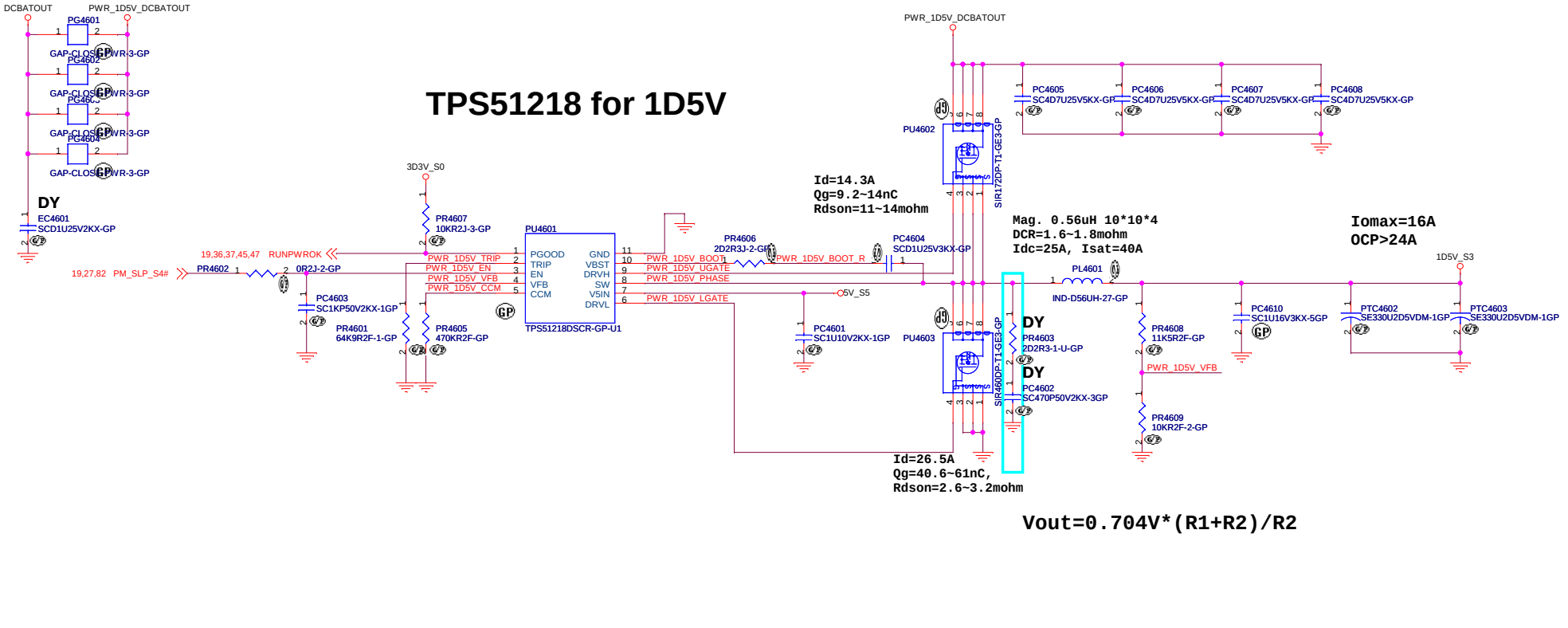
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51218_1D05V	
Size	Document Number: LLW-1 / LGG-1	Rev: SB
Date: Tuesday, November 09, 2010	Sheet 45 of 94	



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緯創資通 Wistron Corporation
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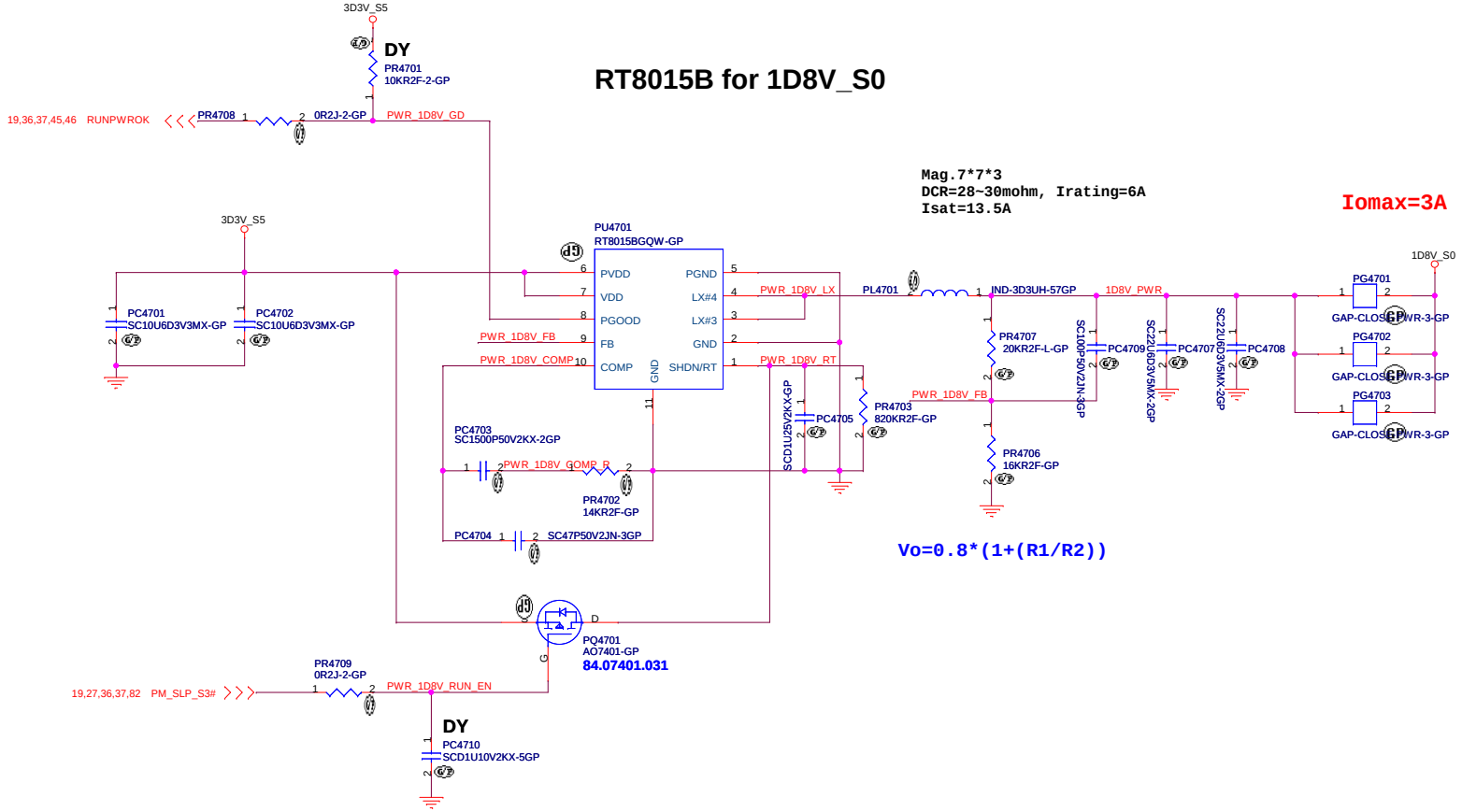
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51128_1D5V & RT9026_0D75V

Size | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 46 of 94

RT8015B for 1D8V_S0



Vo=0.8*(1+(R1/R2))

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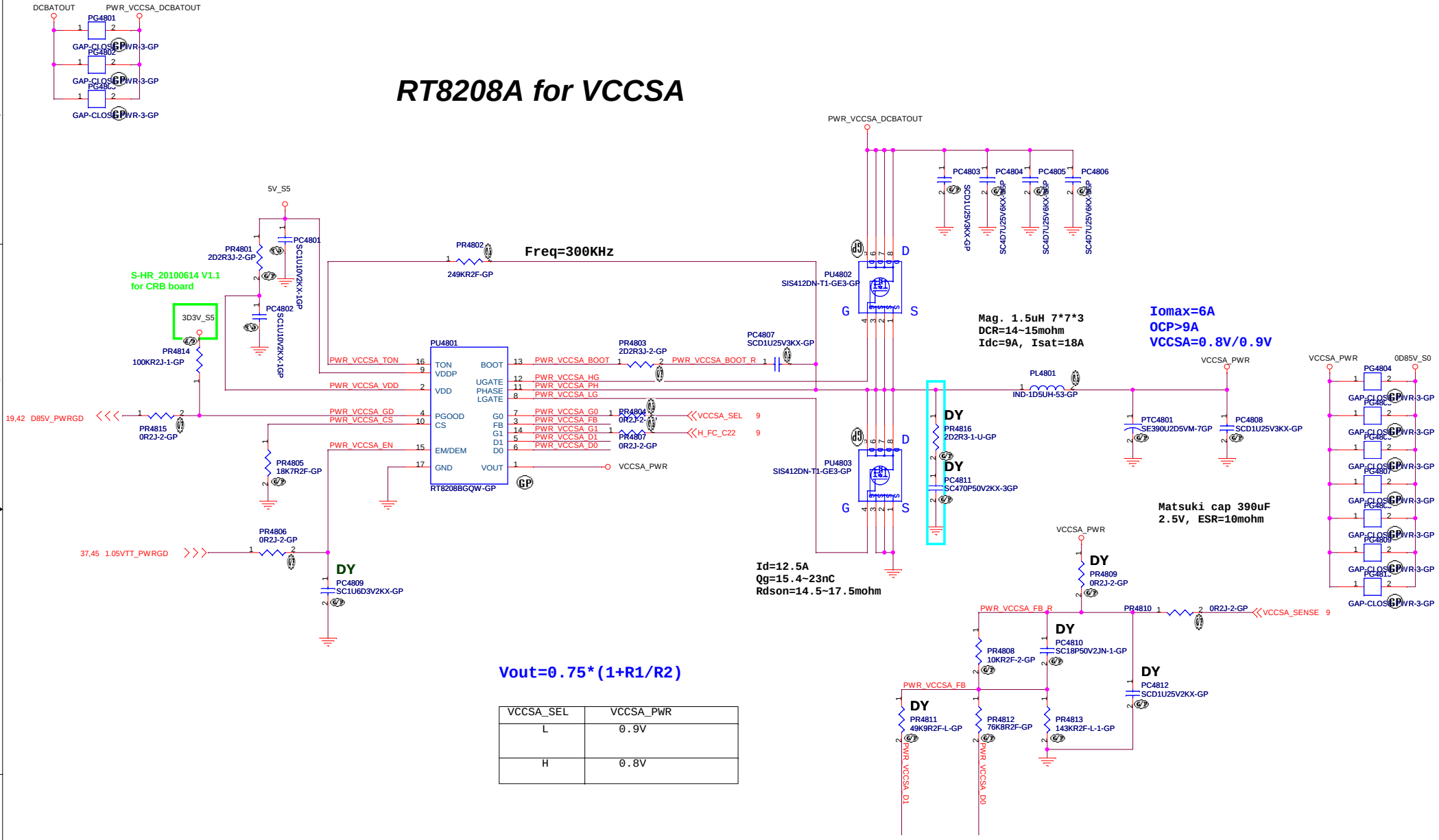
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWM_1D8V_RT8015B	
Size	Document Number: LLW-1 / LGG-1	Rev: SB
Date: Tuesday, November 09, 2010	Sheet 47 of 94	

RT8208A for VCCSA



VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

<Core Design>

緯創資通 Wistron Corporation
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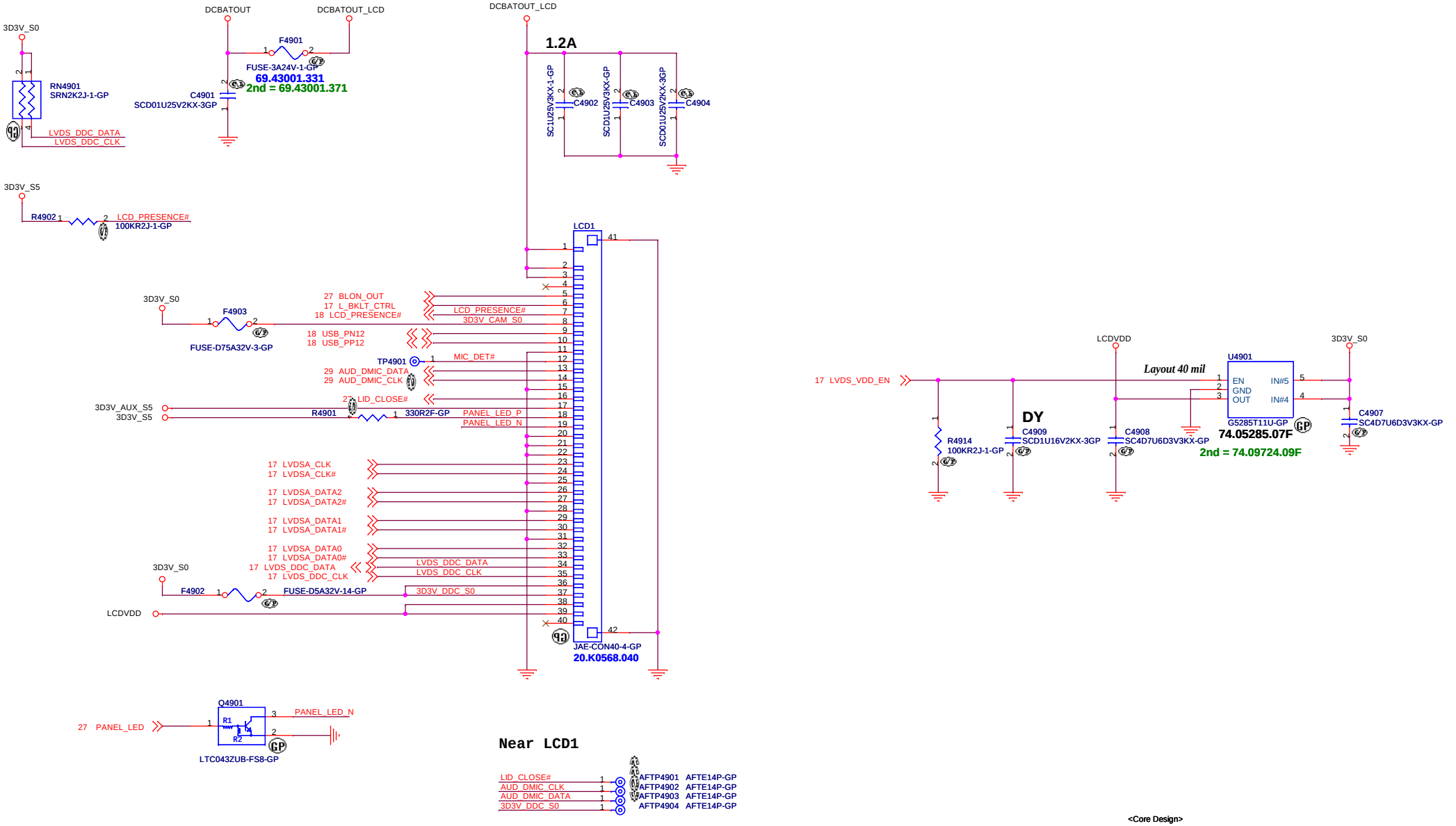
Title	RT8208B_VCCSA	
Size	Document Number: LLW-1 / LGG-1	Rev: SB
Date: Tuesday, November 09, 2010	Sheet 48 of 94	

LCD / Inverter Connector



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Wistron Corporation
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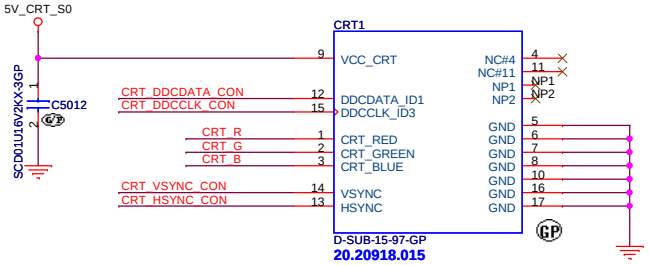
Taipei Hsien 221, Taiwan, R.O.C.

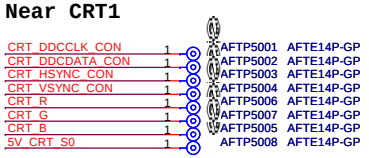
Title: LCD CONNECTOR

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 49 of 94

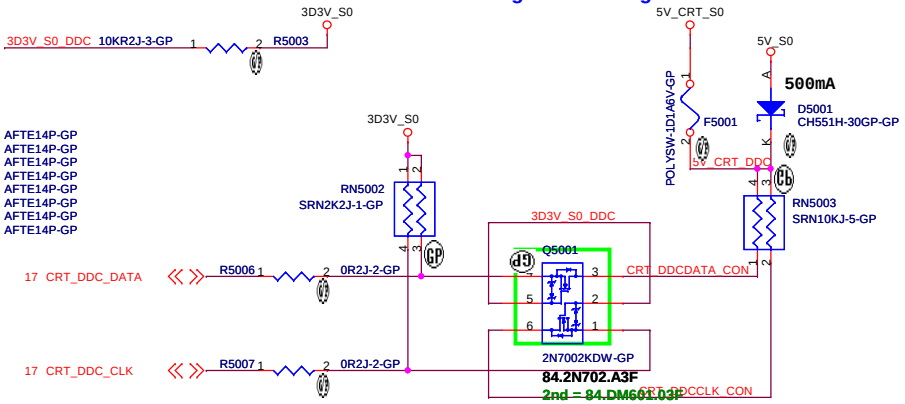
CRT CONNECTOR



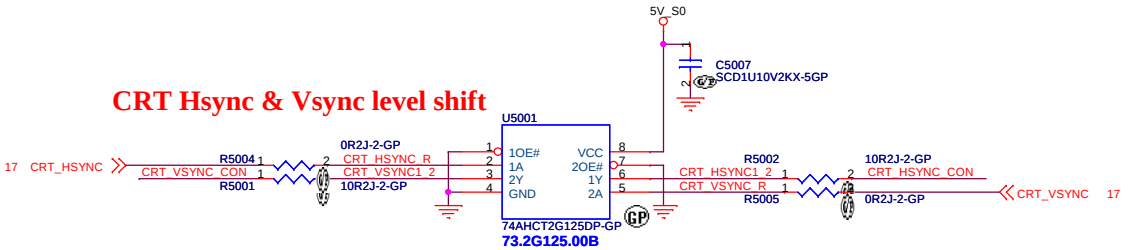


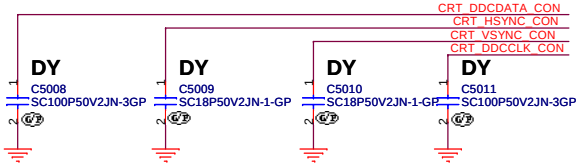
CRT DDCDATA & DDCCLK level shift

Pull High 5V Design on CRT Board

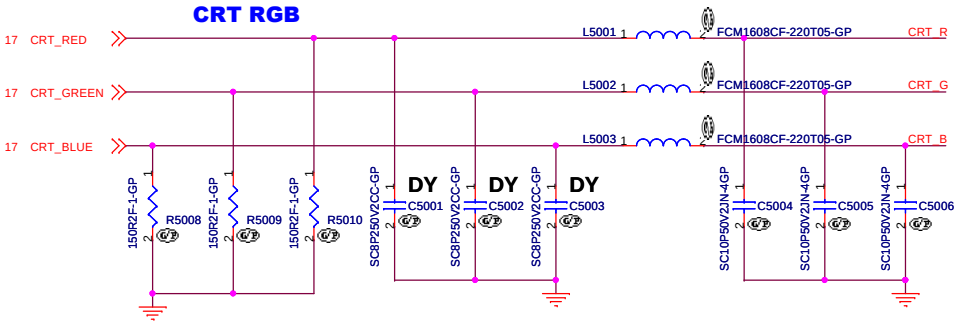


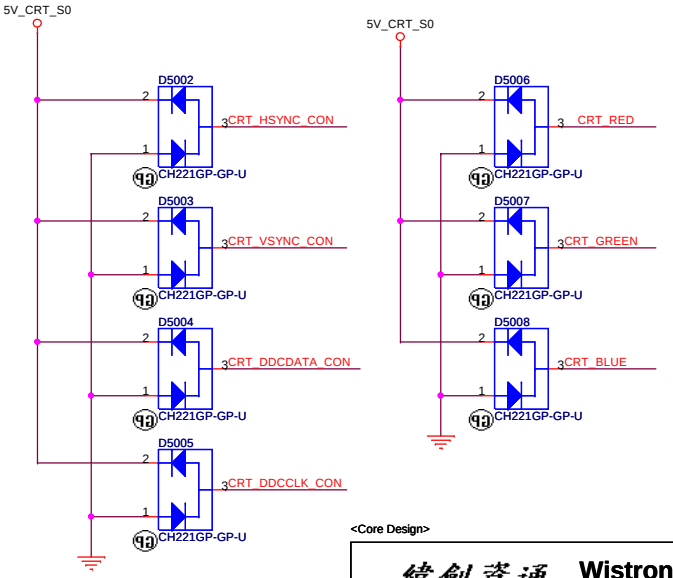
CRT Hsync & Vsync level shift





CRT RGB





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緯創資通 Wistron Corporation
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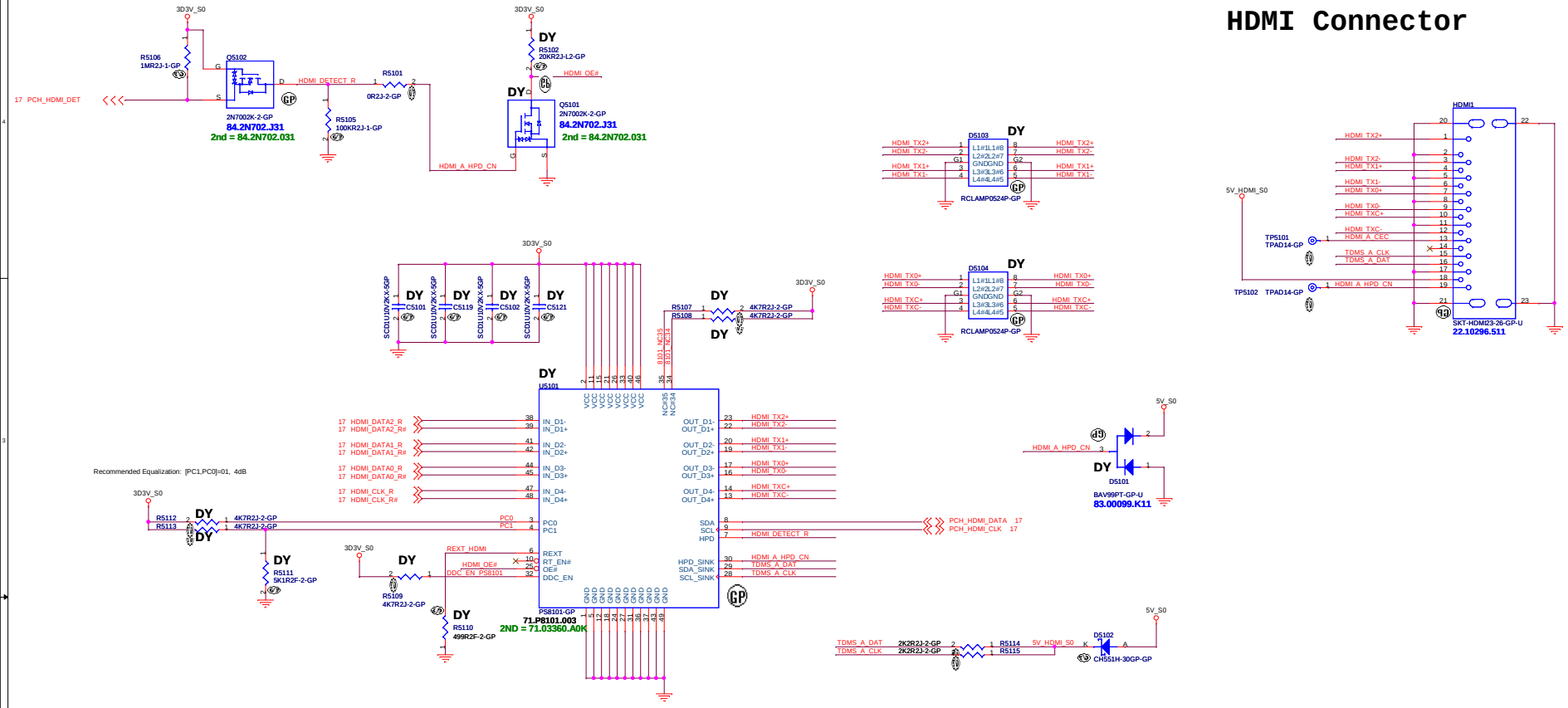
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

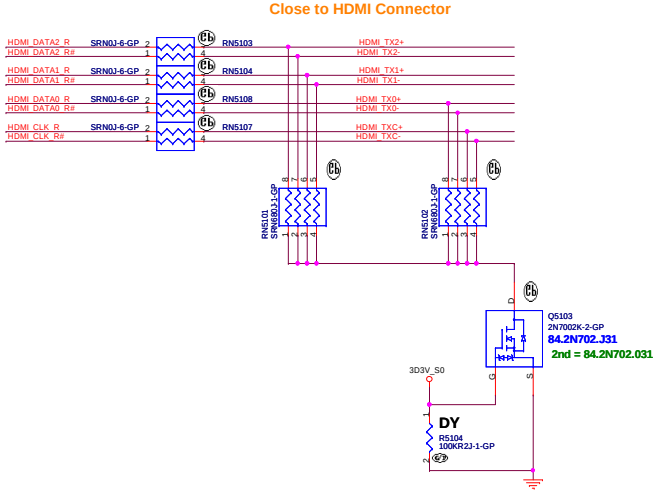
Date: Tuesday, November 09, 2010 Sheet 50 of 94

HDMI Connector

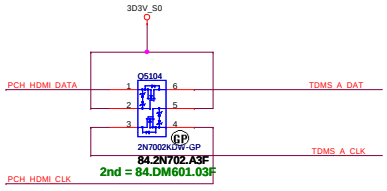


HDMI Passive Level Shifter

Close to HDMI Connector



HDMI DDC Passive Level Shifter



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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI

Size	Document Number	Rev
A2	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 51 of 94

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DISPLAY PORT CONNECTOR***	
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 52 of 94	

5 4 3 2 1

D

C

B

A

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Title	***BLANK***	
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 53 of 94	

5 4 3 2 1

D

C

B

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緯創資通

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLANK***	
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 54 of 94	

<Core Design>

緯創資通

Wistron Corporation
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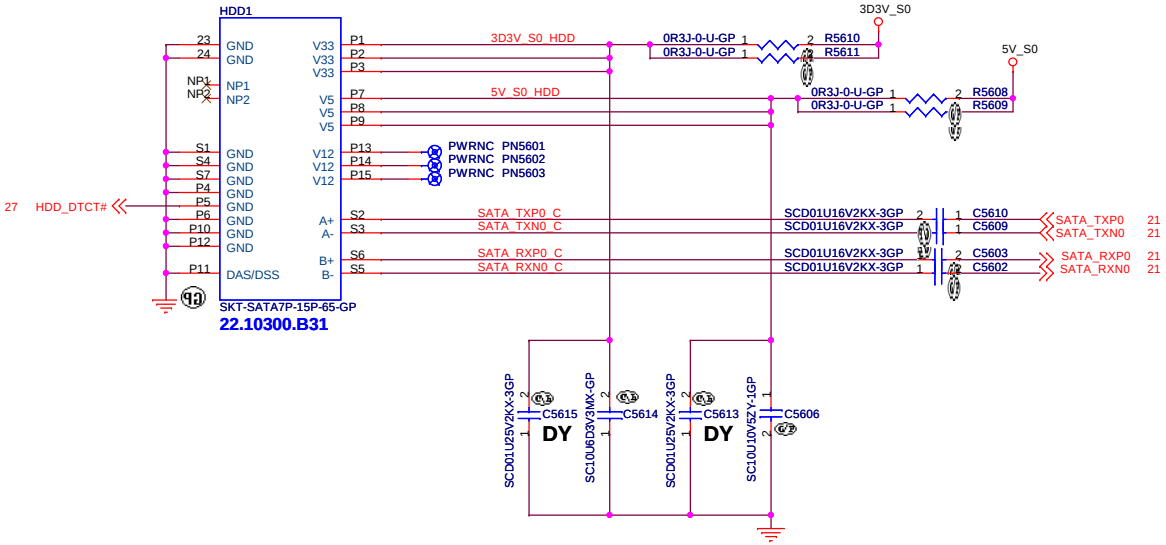
Title

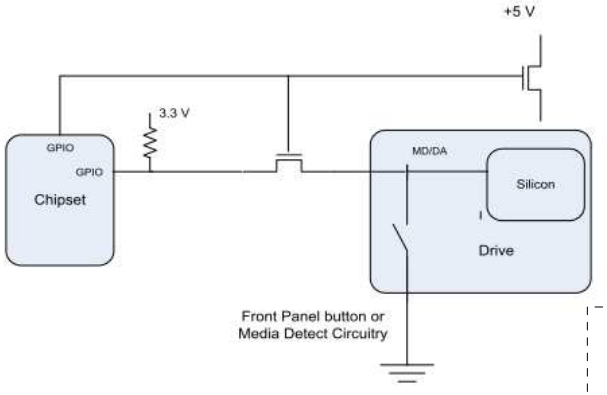
FAN CONTROL

Size	Document Number	Rev
A4	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 55 of 94

HDD Connector

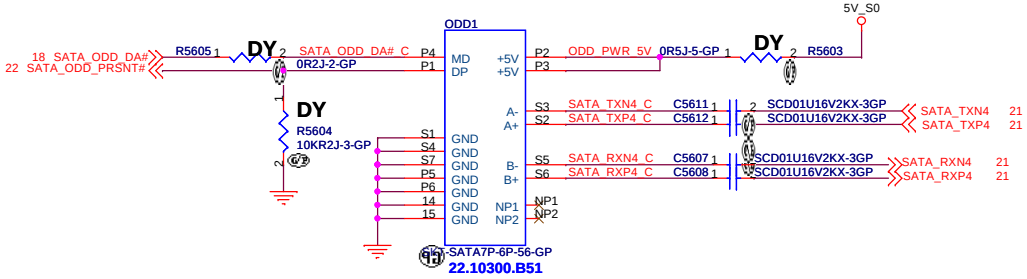




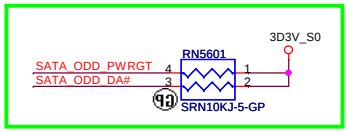
ODD Connector

SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

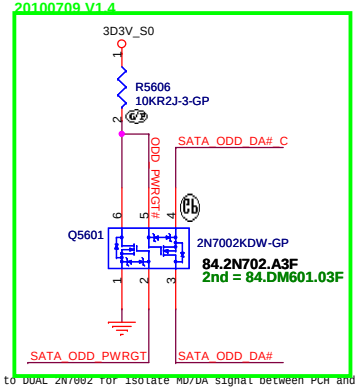


When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



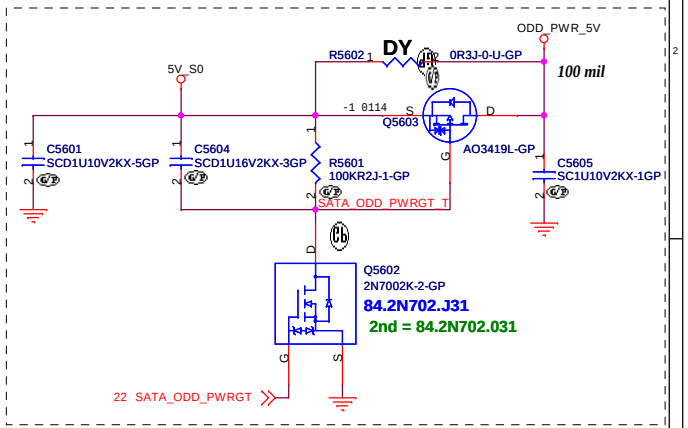
SUPPORT ZERO SATA ODD

20100709 V1.4



0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SATA Zero Power ODD



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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SATA HDD	
Size A3	Document Number LLW-1 / LGG-1	Rev SB
Date: Tuesday, November 09, 2010	Sheet 56 of 94	

ESATA Connector

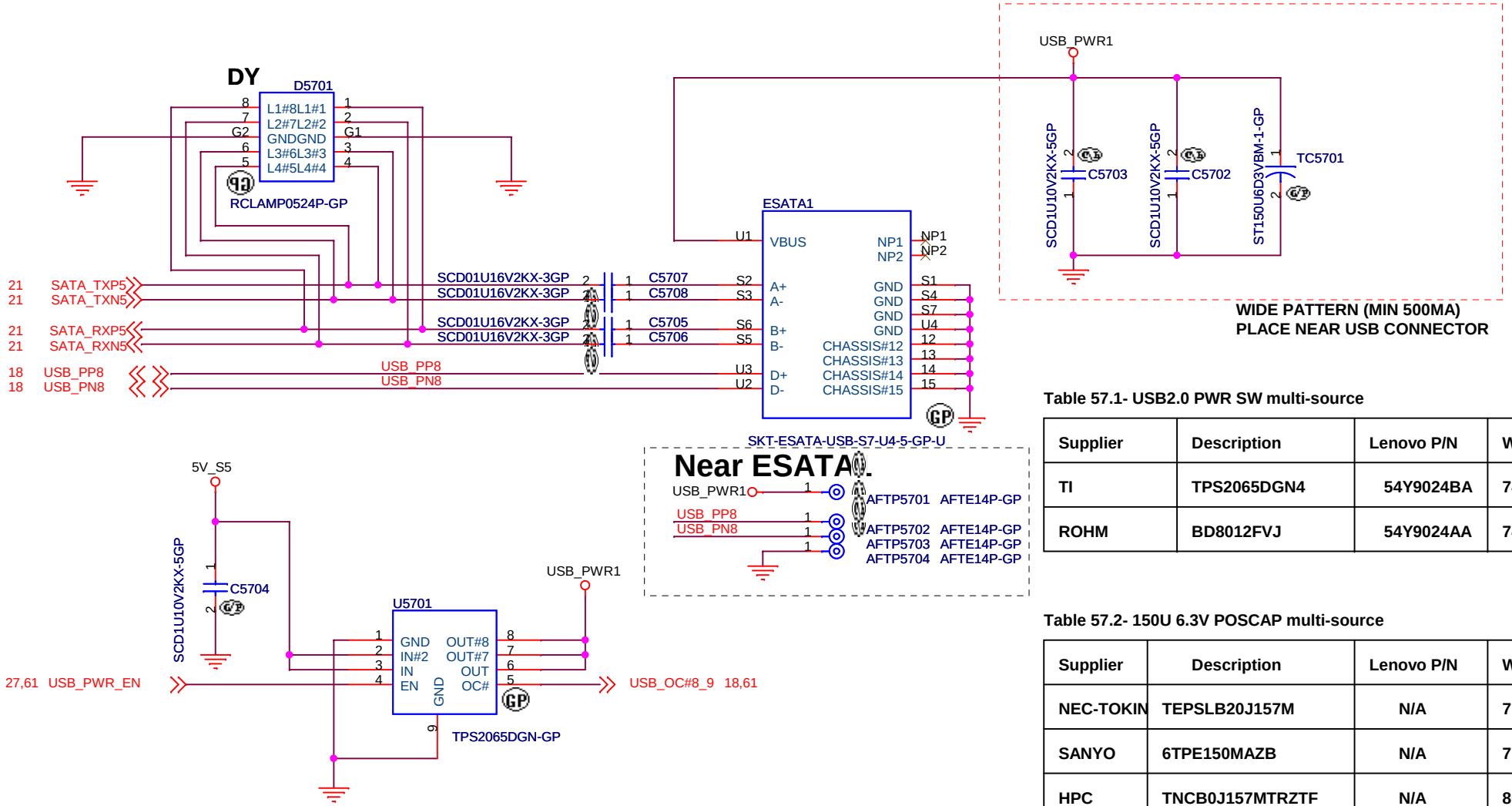

Table 57.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2065DGN4	54Y9024BA	74.02065.079
ROHM	BD8012FVJ	54Y9024AA	74.08012.07G

Table 57.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L

<Core Design>

緯創資通 **Wistron Corporation**
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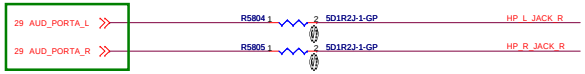
Taipei Hsien 221, Taiwan, R.O.C.

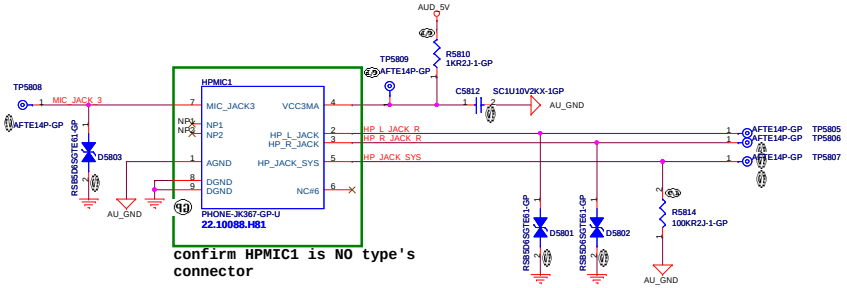
Title: ***ESATA CONNECTOR***

Size	Document Number	Rev
A4	LLW-1 / LGG-1	SB

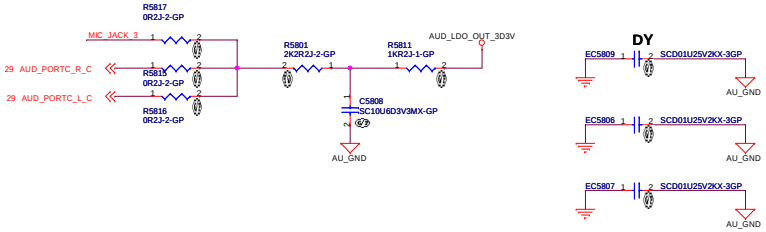
Date: Tuesday, November 09, 2010 Sheet 57 of 94

NEAR HEADPHONE CONN



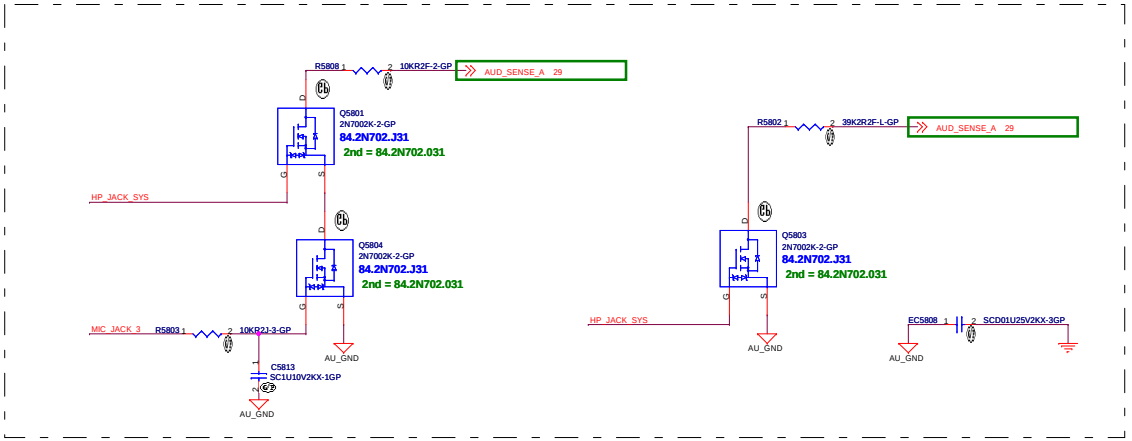


confirm HPMIC1 is NO type's connector



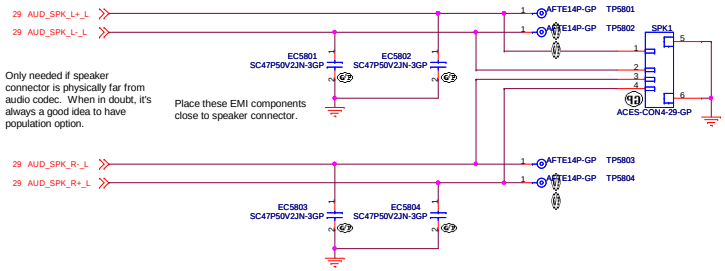
DY

JACK SENSE



INTERNAL STEREO SPEAKERS

Port G



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size: A2 | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 58 of 94

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH

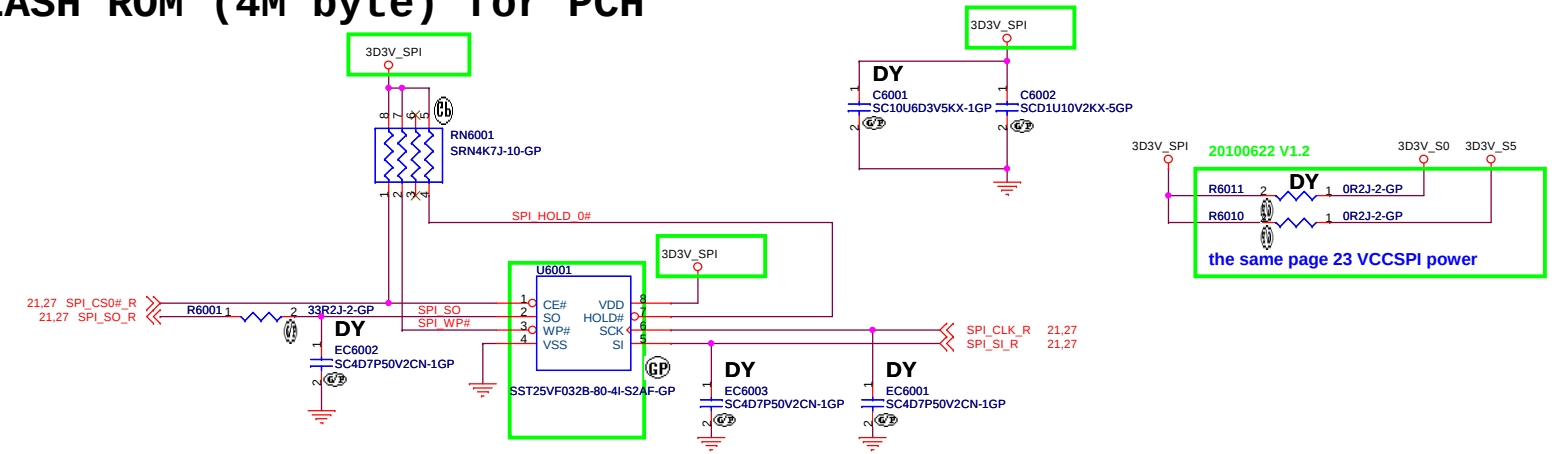


Table 60.1- SPI Serial Flash Memory multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
SST	SST25VF032B-80-4I-S2A	N/A	72.25032.D01
MXIC	MX25L3206EM2I-12G	N/A	72.25320.C01
WINBOND	W25Q32BVSSIG	N/A	72.25Q32.A01
NUMONYX	M25PX32-VMW6F	N/A	72.25P32.C01

SSID = RBATT

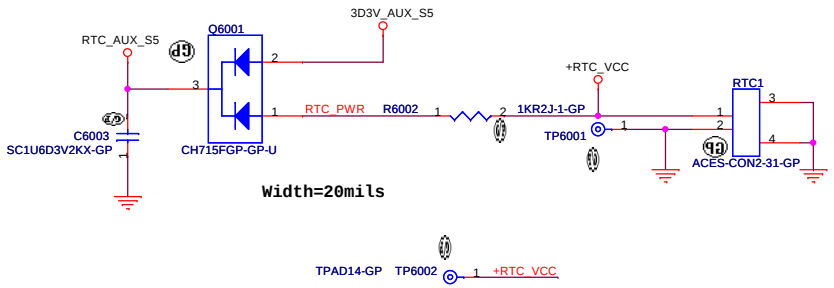


Table 60.2 - Schottky Barrier Diode multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	CH715FGP	N/A	83.R0304.D81
CHENMKO	BAS40CWGP	N/A	83.00040.R81
PANJIT	BAS40CW	N/A	83.00040.E81

<Core Design>

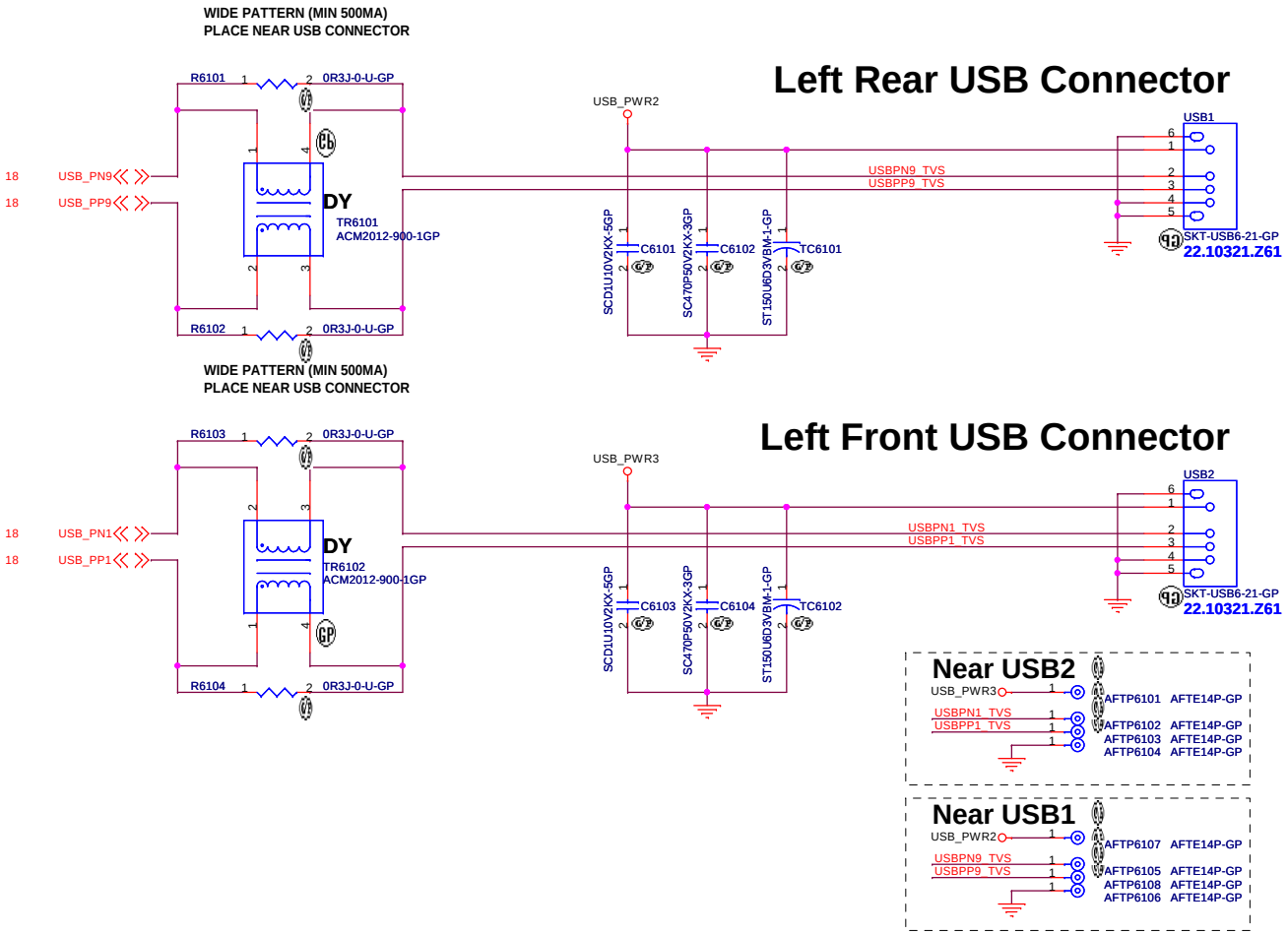
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash/RTC***

Size: A3 | Document Number: **LLW-1 / LGG-1** | Rev: **SB**

Date: Tuesday, November 09, 2010 | Sheet 60 of 94

USB Connector



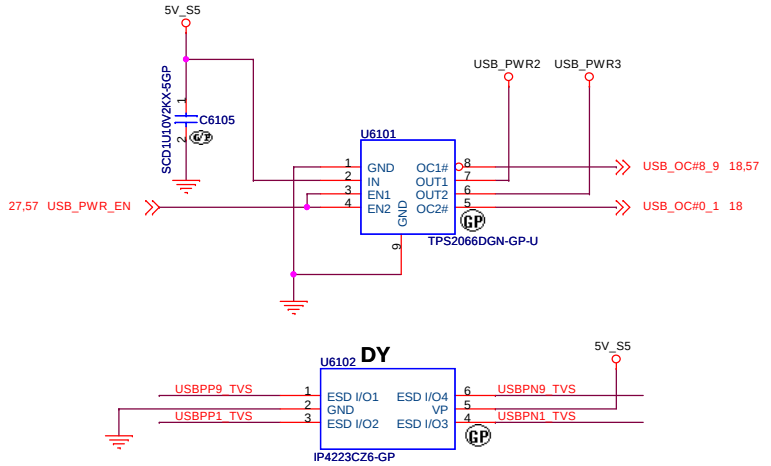


Table 61.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2066DGN	41R0511AA	74.02066.A71
TI	TPS2066DGN-1	N/A	74.02066.B71

Table 61.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L

<Core Design>

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Title: ***USB Connector***

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 61 of 94

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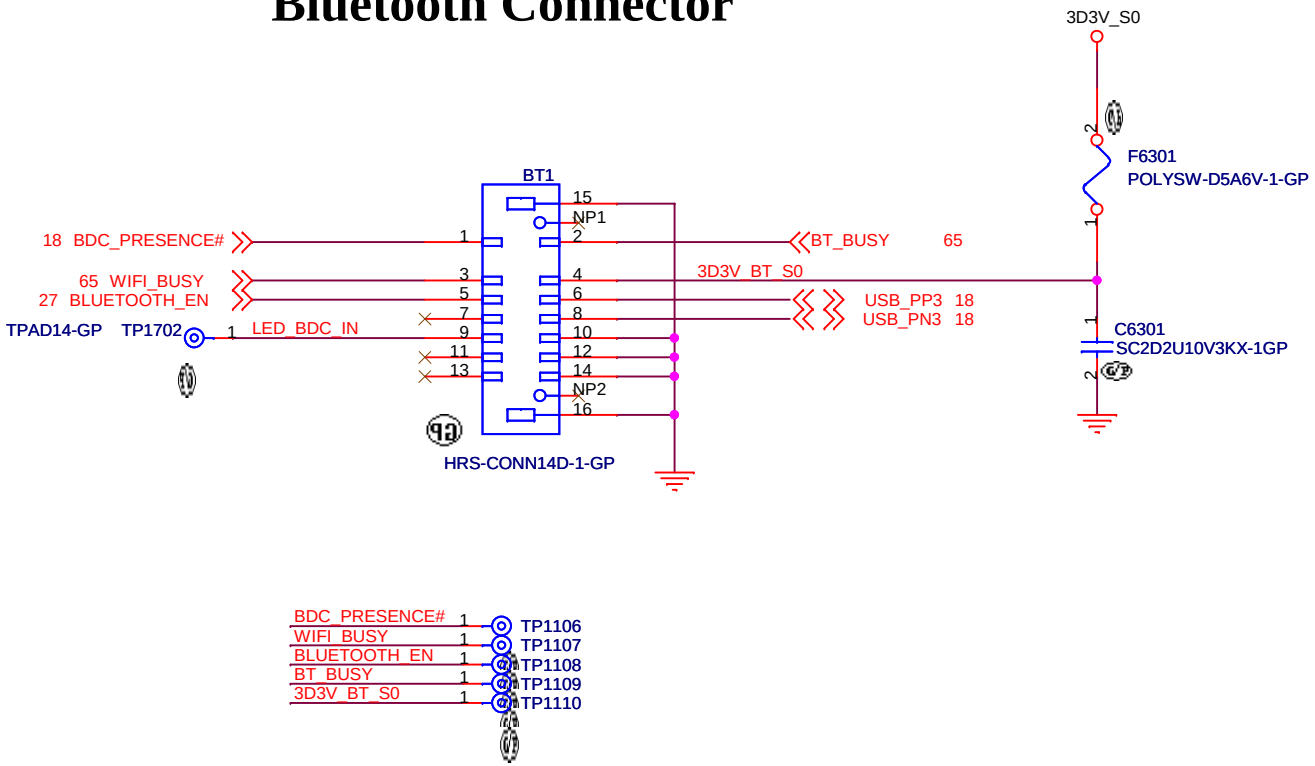
<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLANK***	
Size: A4	Document Number: **LLW-1 / LGG-1**	Rev: **SB**
Date: Tuesday, November 09, 2010	Sheet 62 of 94	

Bluetooth Connector



<Core Design>

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Title: ***Bluetooth***

Size	Document Number	Rev
A4	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 63 of 94

5 4 3 2 1

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<Core Design>

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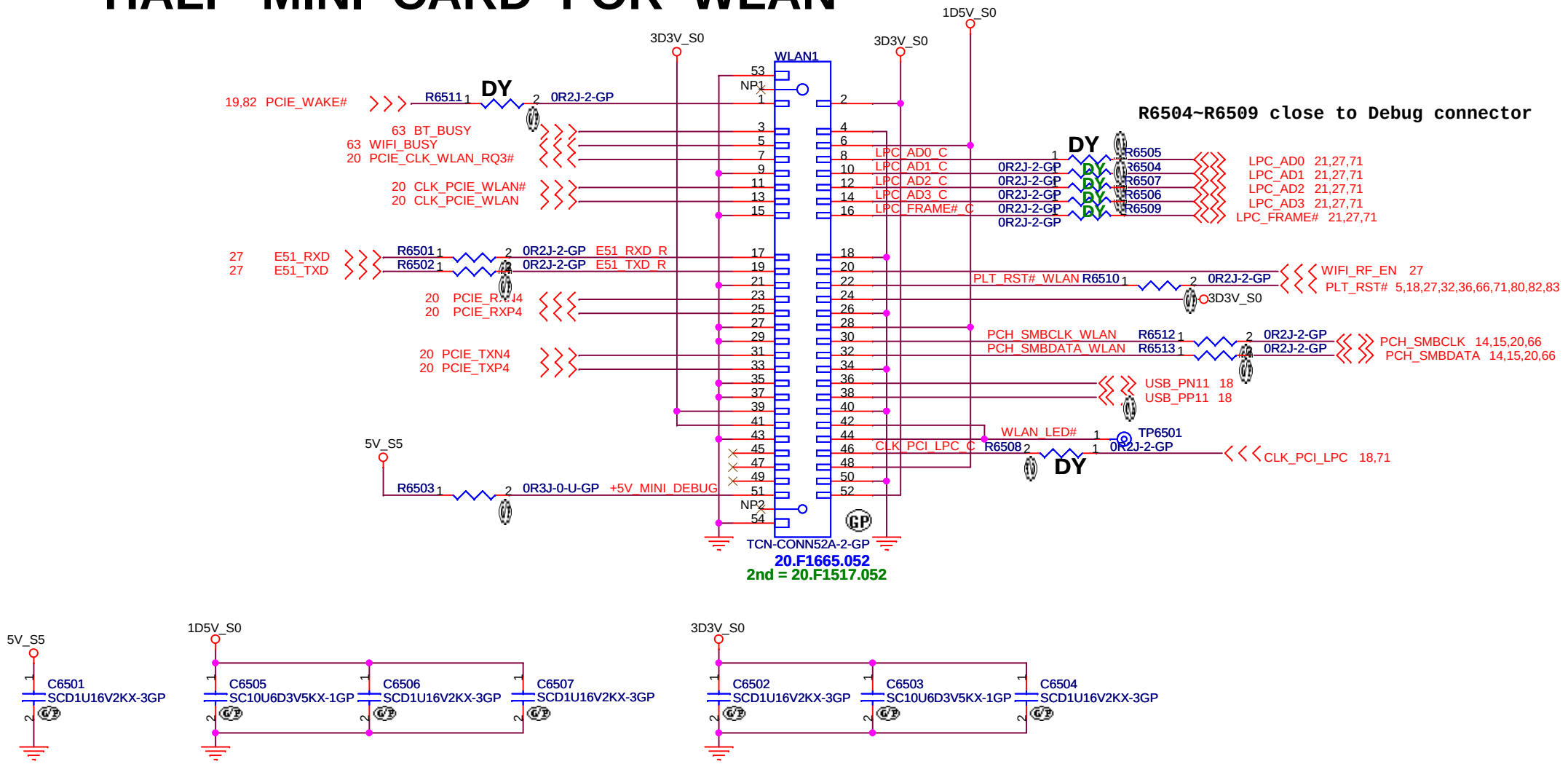
Title: ***FingerPrint***

Size	Document Number	Rev
A4	**LLW-1 / LGG-1**	**SB**

Date: Tuesday, November 09, 2010 Sheet 64 of 94

HALF MINI CARD FOR WLAN



<Core Design>

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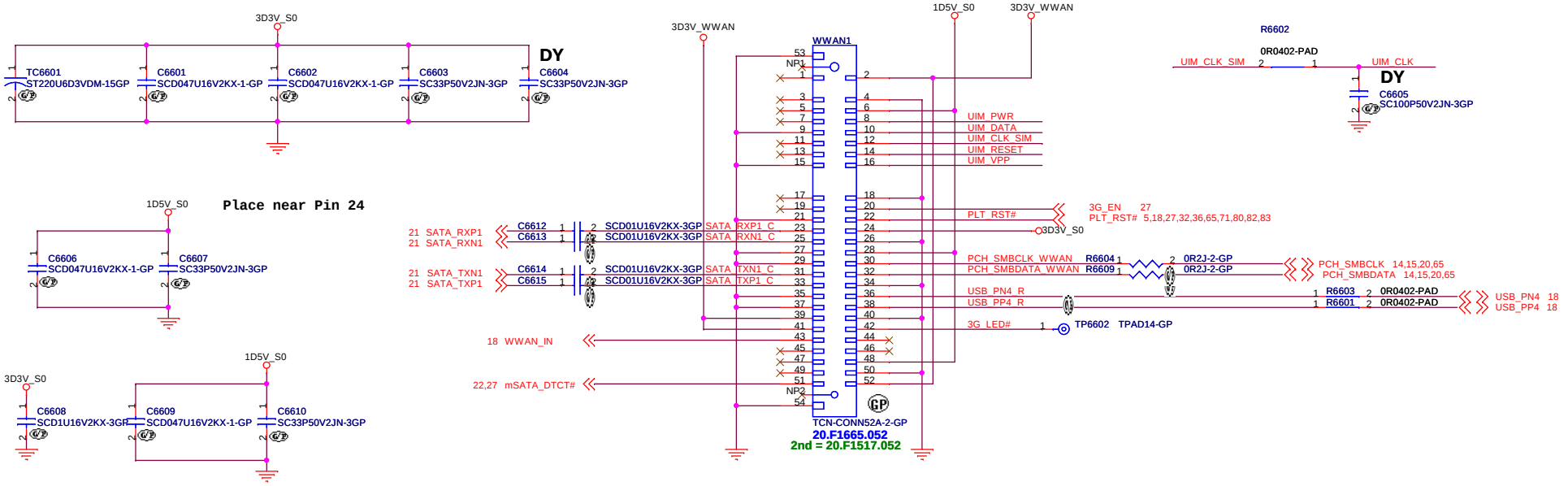
Title: ***MINI CARD SLOT 1***

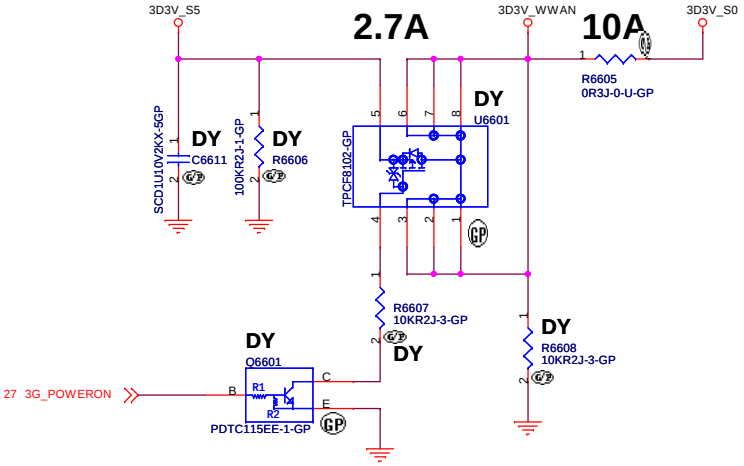
Size	Document Number	Rev
A4	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 65 of 94

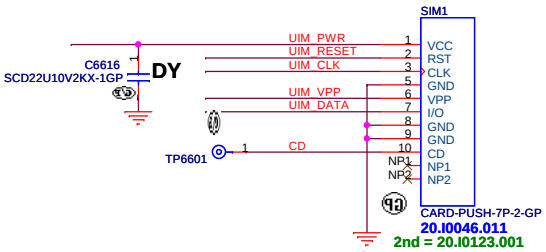
Mini Card Connector(WWAN)

Place near MINI Card CONN





SIM Connector



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Title: ***MINI CARD SLOT 2***

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 66 of 94

5 4 3 2 1

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Title	***BLANK***	
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 67 of 94	

5 4 3 2 1

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Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 68 of 94	

Touch Pad Connector

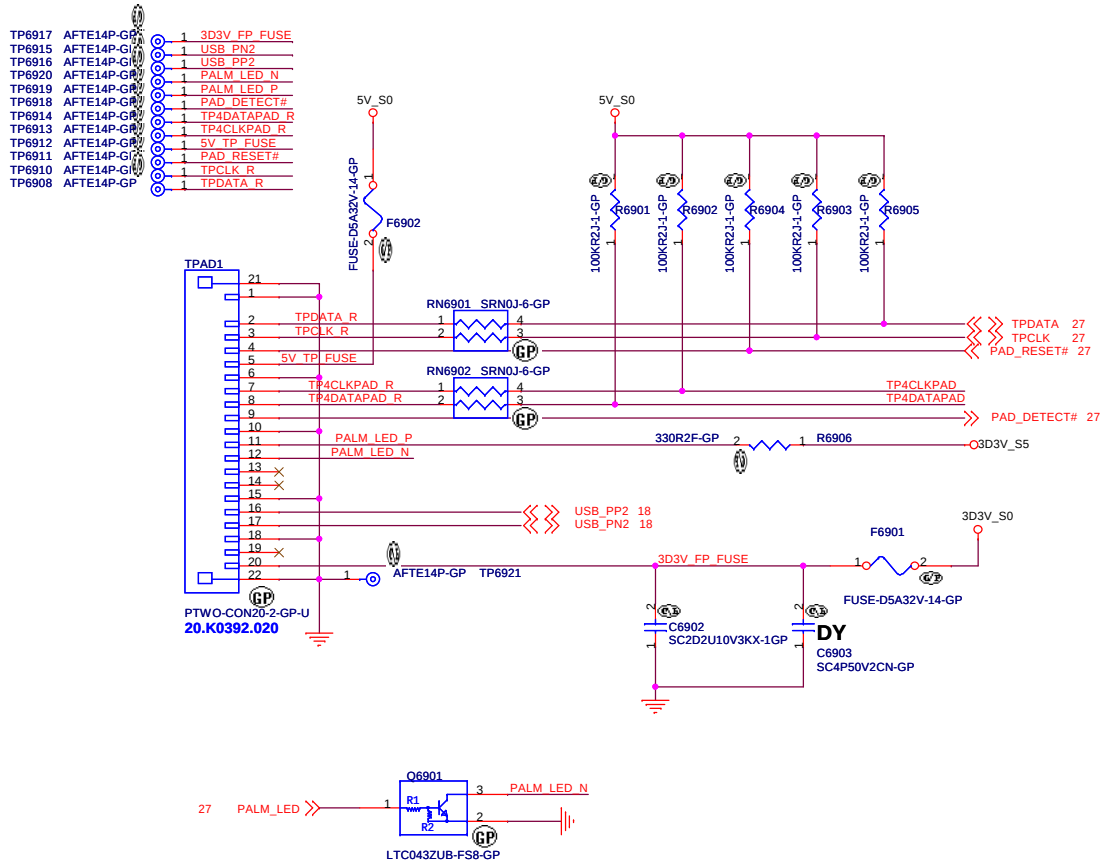
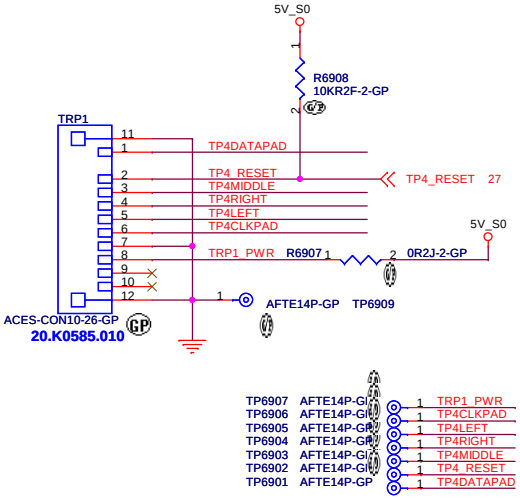


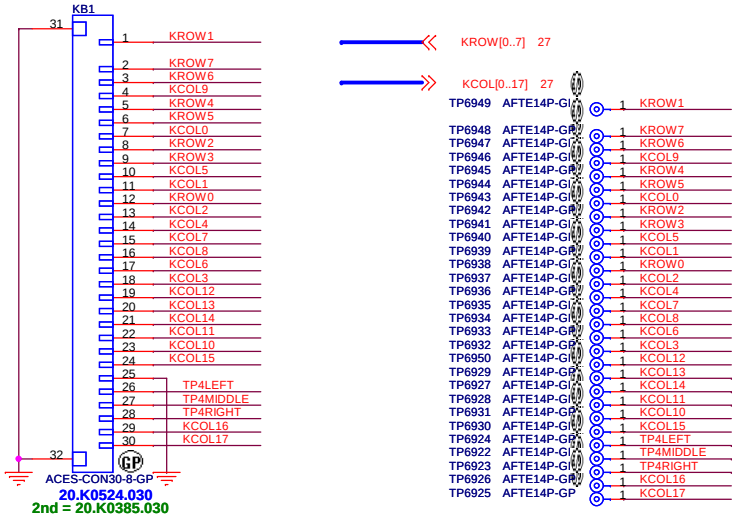
Table 69.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC143ZU	N/A	84.00143.E1K
ON	DTA114EET1G	N/A	84.DT114.B11
ROHM	LTC043ZUB	N/A	84.00043.011
Panasonic	DRC5143Z0L	N/A	84.05143.011

Track Point Connector



KeyBoard Connector



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Title: **TOUCH PAD CONNECTOR**

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 69 of 94

5 4 3 2 1

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緯創資通 **Wistron Corporation**
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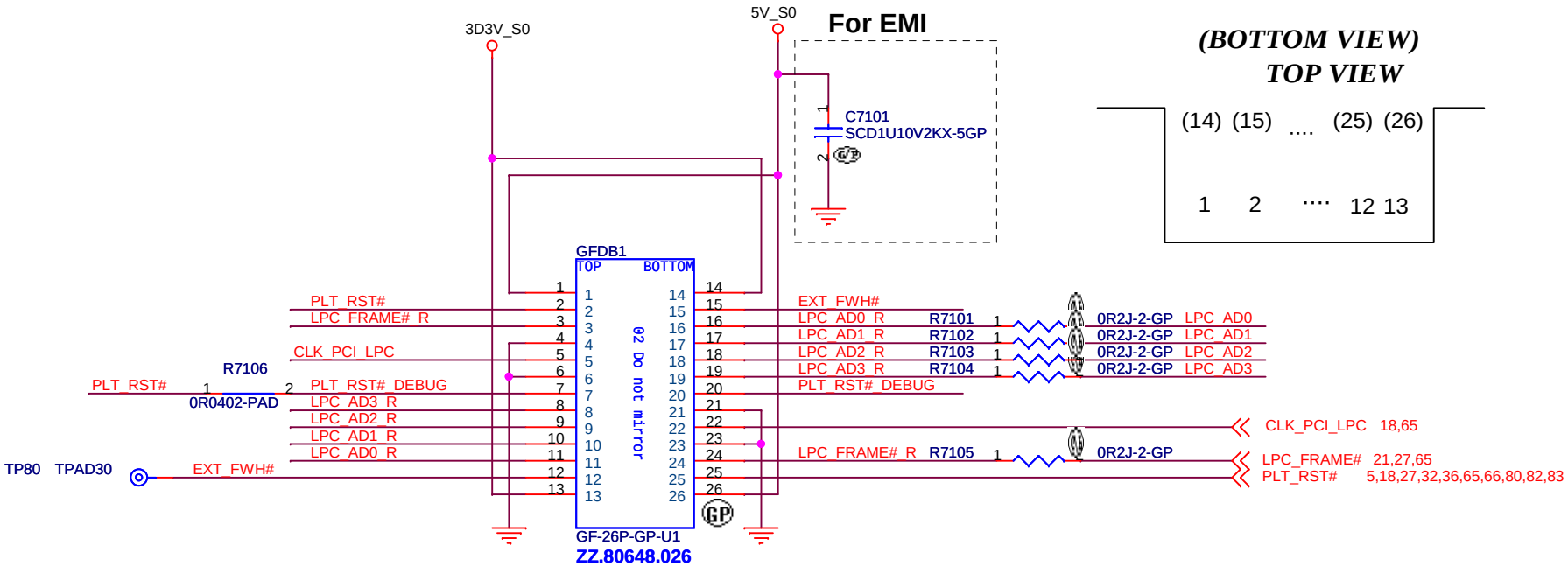
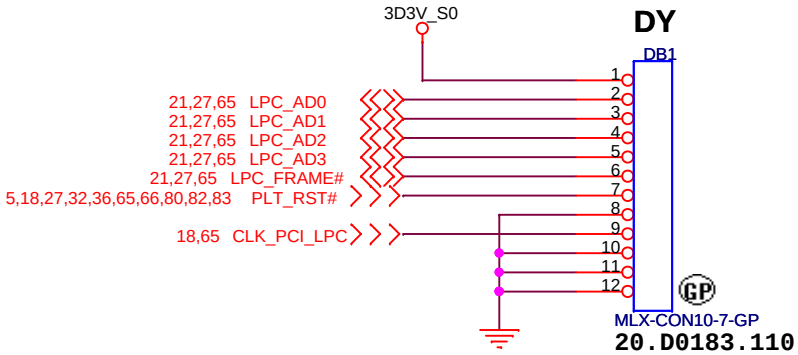
Title	***BLANK***	
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 70 of 94	

Golden Finger for Debug Board





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Title	DEBUG CONN	
Size A4	Document Number LLW-1 / LGG-1	Rev SB
Date: Tuesday, November 09, 2010	Sheet 71 of 94	

5 4 3 2 1

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Title	***BLANK***	
Size: A4	Document Number: **LLW-1 / LGG-1**	Rev: **SB**
Date: Tuesday, November 09, 2010	Sheet 72 of 94	

5 4 3 2 1

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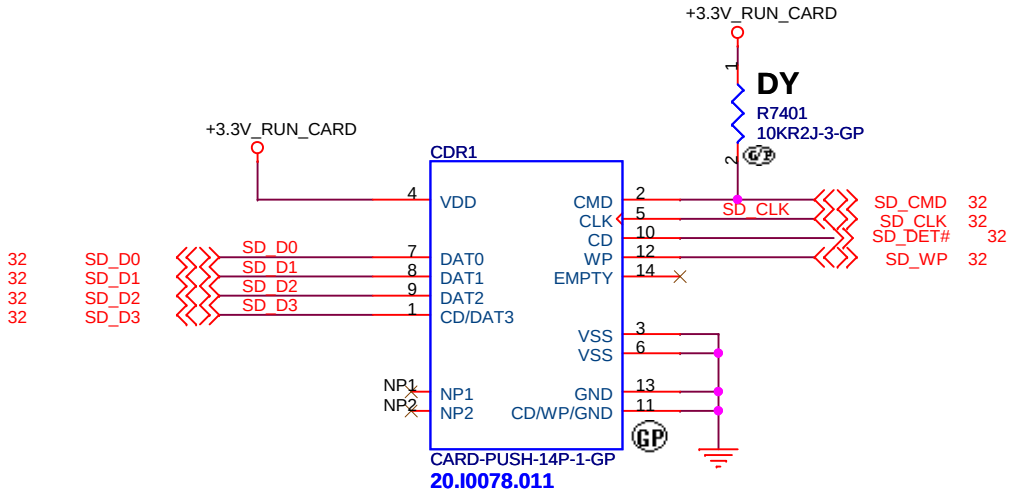
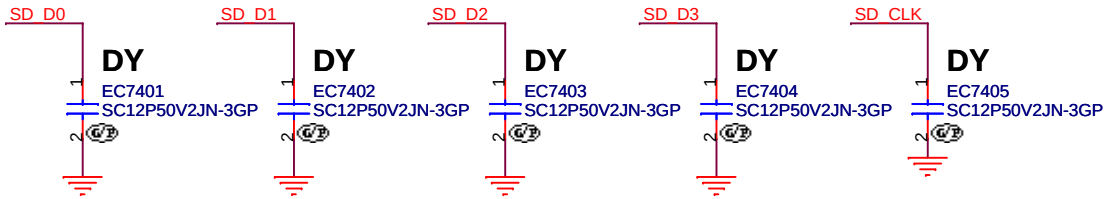
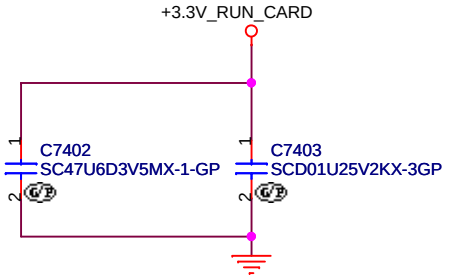
Title	***BLANK***	
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 73 of 94	

Please apply Shield GND for SD_CLK signal between
R5U220 and SD Card Slot to decrease external noise.

Card Reader Connector







+3.3V_RUN_CARD trace = 40mil

C7402 lose CDR1

<Core Design>

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Title	*CARD Reader CONN*	
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 74 of 94	

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

緯創資通 Wistron Corporation
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Title: *New Card*

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 75 of 94

5 4 3 2 1

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Title	***BLANK***	
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 76 of 94	

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Title: *TPM*		
Size: Custom	Document Number: LLW-1 / LGG-1	Rev: SB
Date: Tuesday, November 09, 2010	Sheet 77 of 94	

5 4 3 2 1

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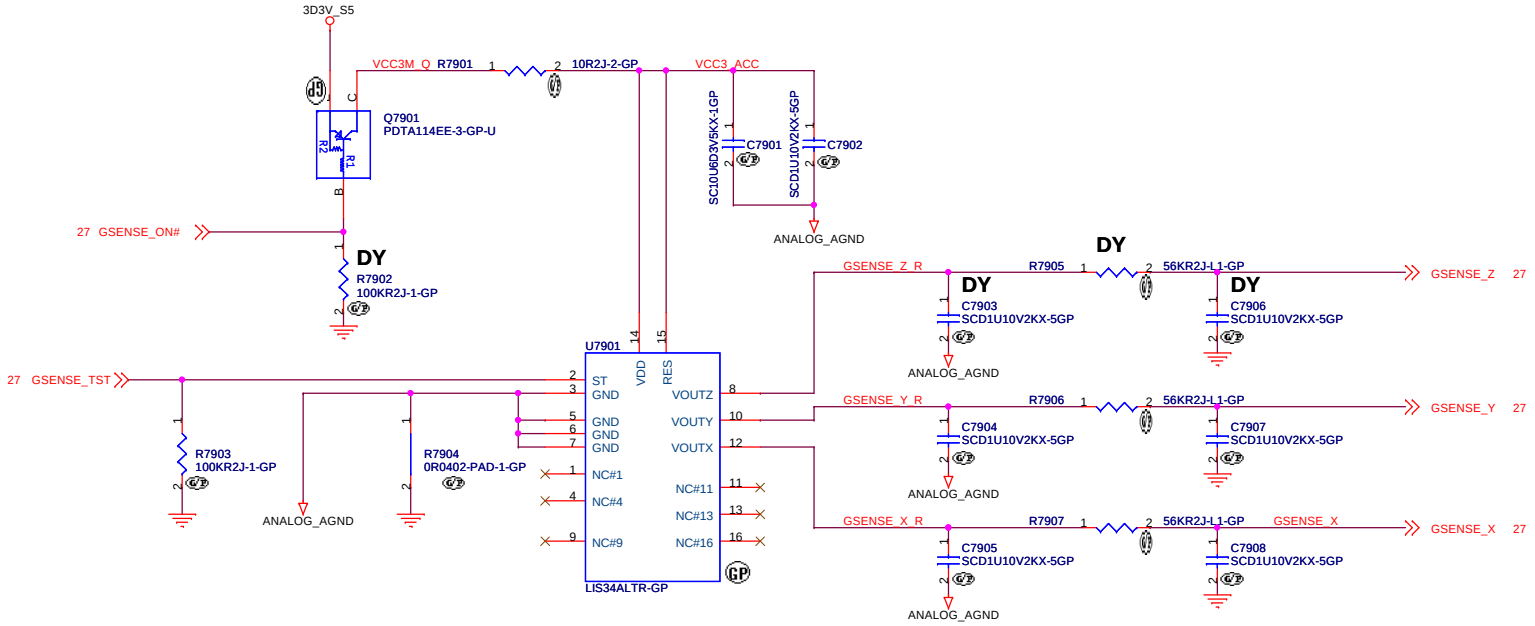
Size A4	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 78 of 94	

G-Sensor



	LIS34AL KXTC8-2850	No Accel
R7902	NO_ASM	ASM
R7903	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C7904, C7905, Q7901, R7901, R7902, C7901, C7902, R7903, R508 close to U7901.

(2) Avoid routing under DCDC switching area.

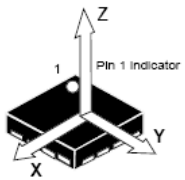


Table 79.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTA114EE	N/A	84.00114.H1K
ON	DTA114EET1G	N/A	84.DT114.B11
ROHM	LTA014EEB	N/A	84.00014.01H
Panasonic	DRA9114E0L	N/A	84.09114.A11

Table 79.2- Accelerometer multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ST	LIS34ALTR-GP	41R0828AA	74.00034.0BZ
ROHM-KIONIX	KXTC8-2850-GP	N/A	74.KXTC8.0BZ

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Title: ***G-Sensor***

Size: Custom | Document Number: **LLW-1 / LGG-1** | Rev: **SB**

Date: Tuesday, November 09, 2010 | Sheet 79 of 94

RFID

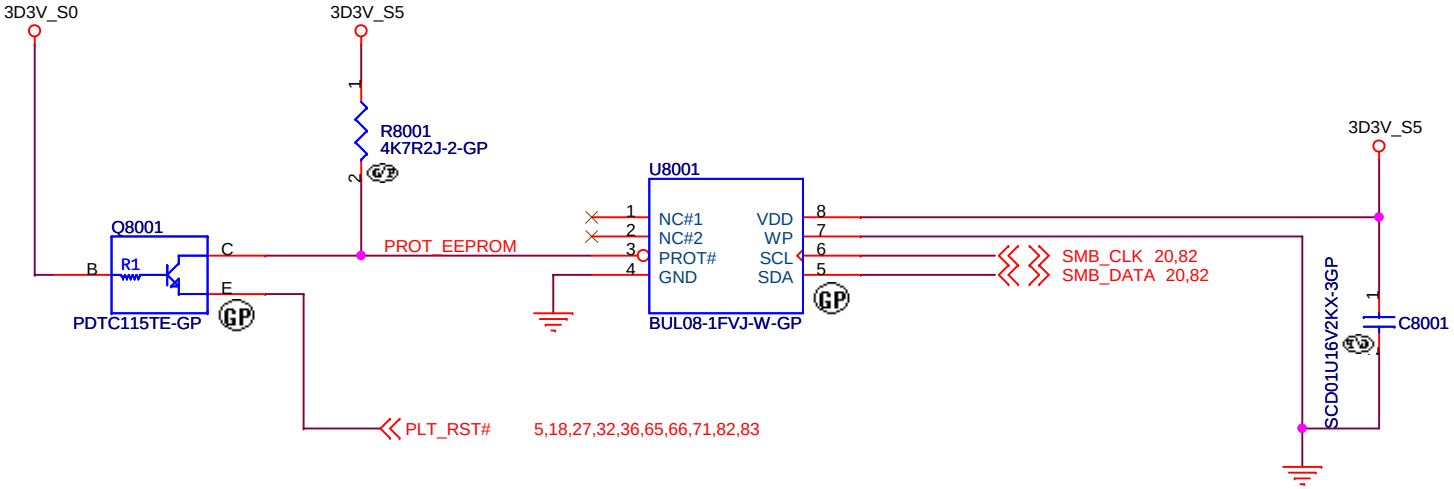

Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015EEB	N/A	84.00015.01H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-W	54Y9016AA	72.BUL08.00Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

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Title	RFID	
Size A4	Document Number LLW-1 / LGG-1	Rev SB
Date: Tuesday, November 09, 2010	Sheet 80 of 94	

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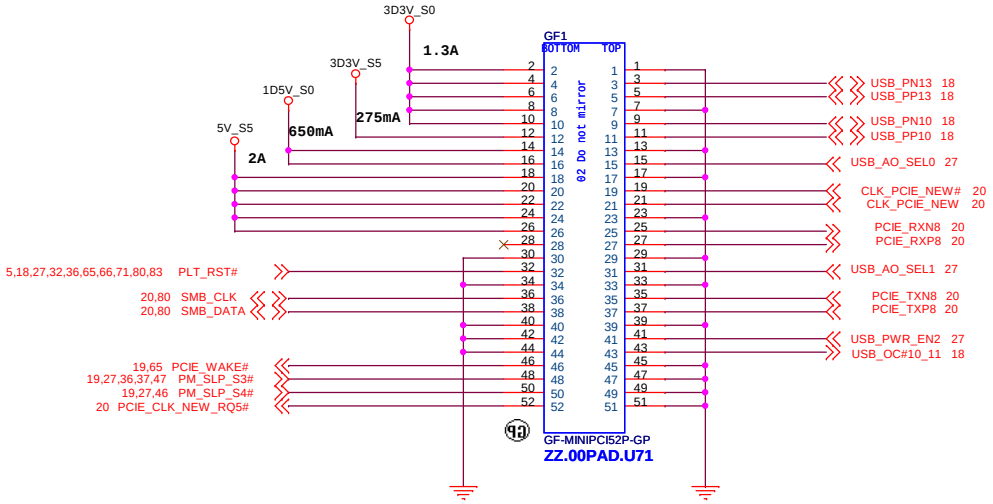
Title: ***Reserved***

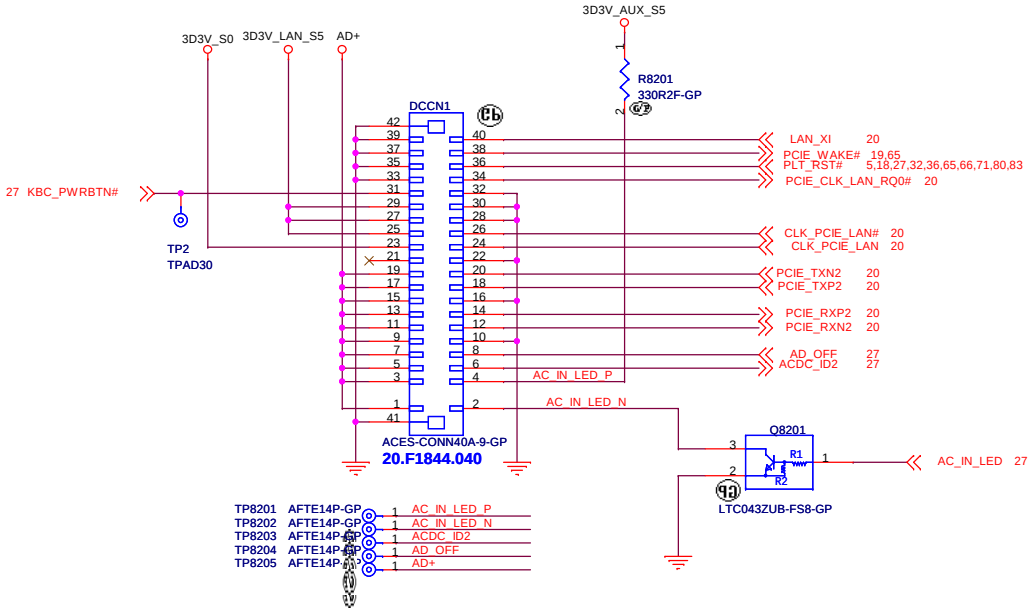
Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 81 of 94

TO EXP BOARD CONN



TO DC BOARD CONN



<Core Design>

緯創資通 Wistron Corporation
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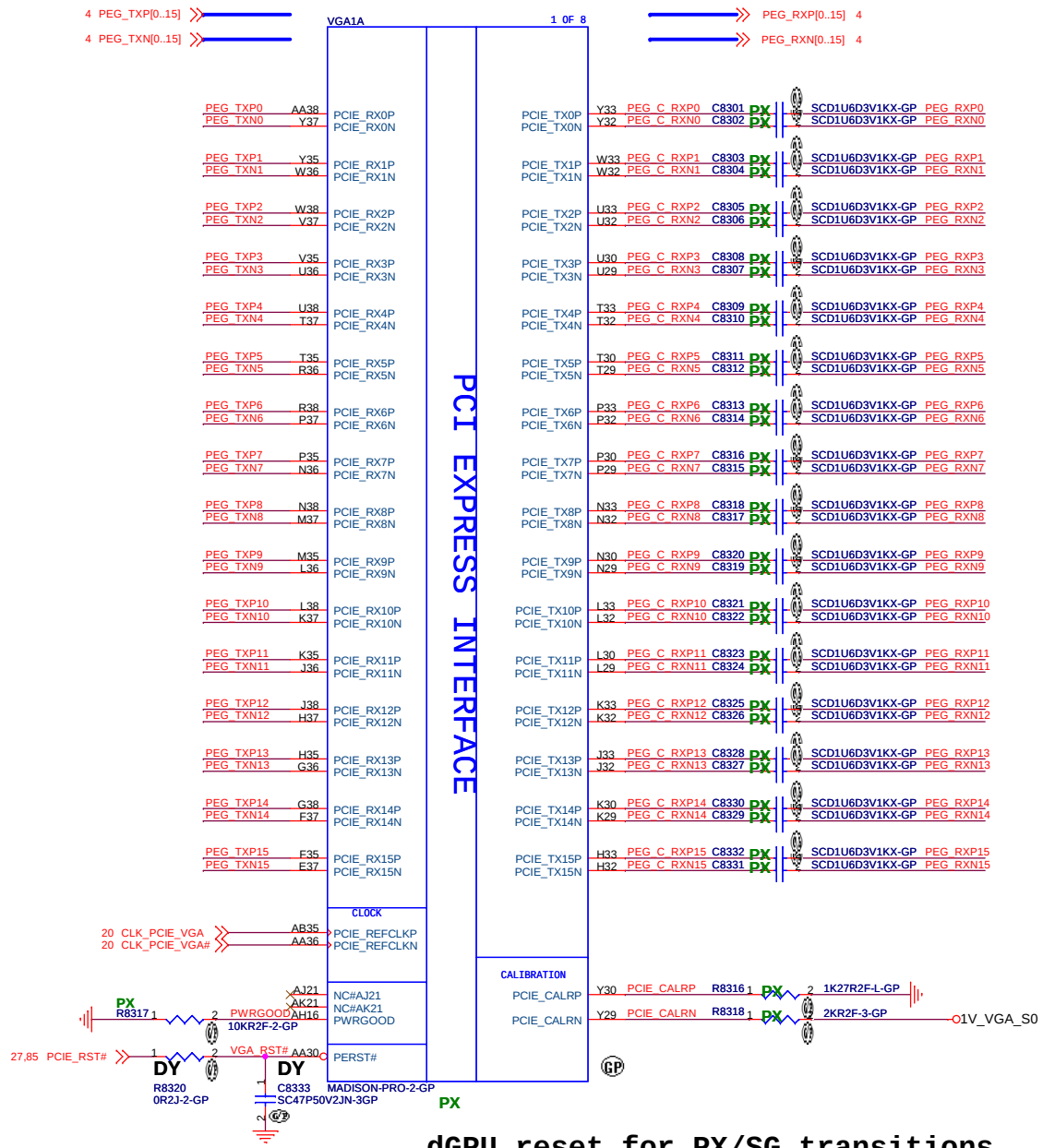
Title: *IO Board Connector*

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 82 of 94



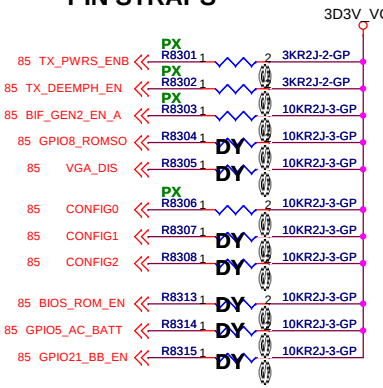
CONFIGURATION STRAPS

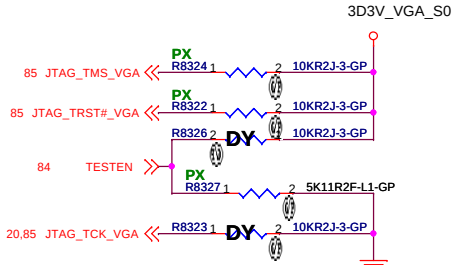
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



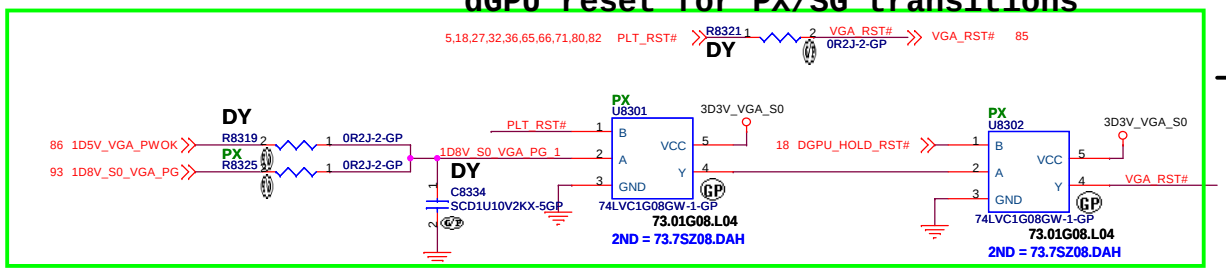


TESTEN Vancouver need to 5.1K ohm
Mannhatton need to 1K ohm

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

dGPU reset for PX/SG transitions



	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACO	H

<Core Design>

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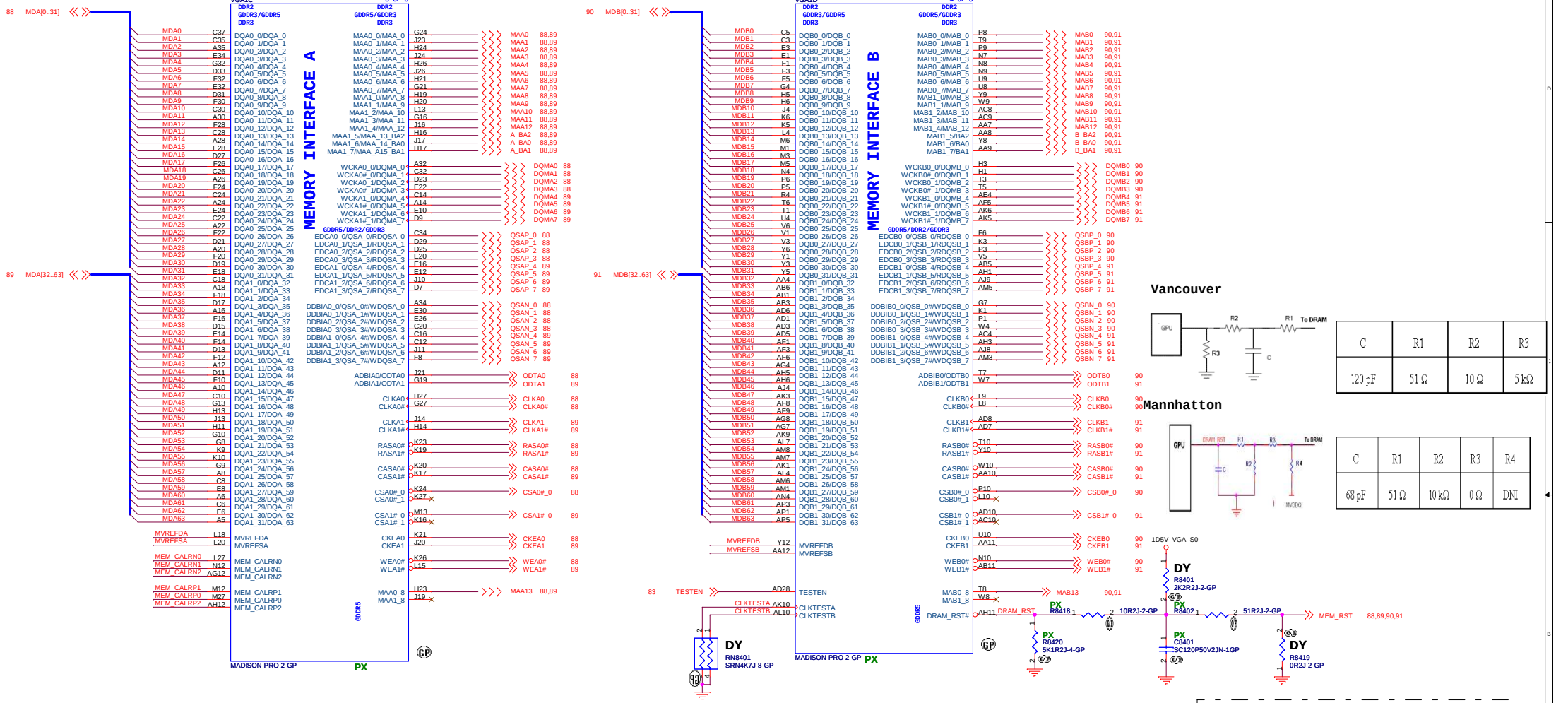
Title: **GPU_PCIE/STRAPPING(1/5)**

Size: A3 | Document Number: **LLW-1 / LGG-1** | Rev: **SB**

Date: Tuesday, November 09, 2010 | Sheet 83 of 94



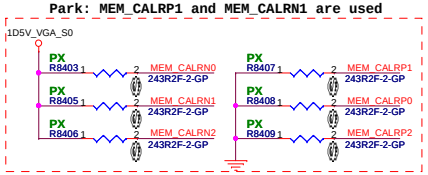
Vancouver

C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

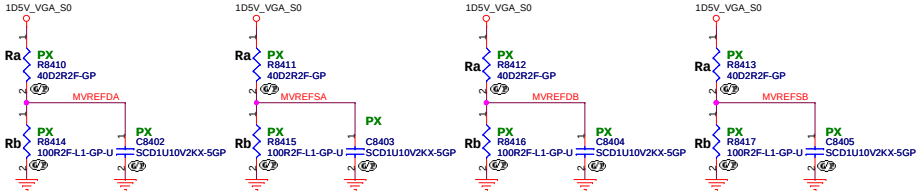
Mannhatton

C	R1	R2	R3	R4
68 pF	51 Ω	10 kΩ	0 Ω	DNI

Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

DDR3/GDDR3 Memory Stuff Option(M92/M96)

	GDDR3	DDR3
MVDDQ	1.8V/1.5V	1.5V
Ra	40.2R	100R
Rb	100R	100R

** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU Memory(2/5)**

Size: Custom | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 84 of 94

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios request

DVPDATA [3:0]
0111 2Gbit Hynix-H5TQ2G63BFR-12C (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
1111 2Gbit Samsung-K4W2G1646C-HC12 (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
0011 1Gbit Hynix-H5TQ1G63BFR-12C (800MHz) (Whistler-LP 1G)
1011 1Gbit Samsung-K4W1G1646E-HC12 (800MHz) (Whistler-LP 1G)

LVDS Interface

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

DDC1/DDC2/DDC6 have 5V-tolerant

Voltage Swing:1.8V

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

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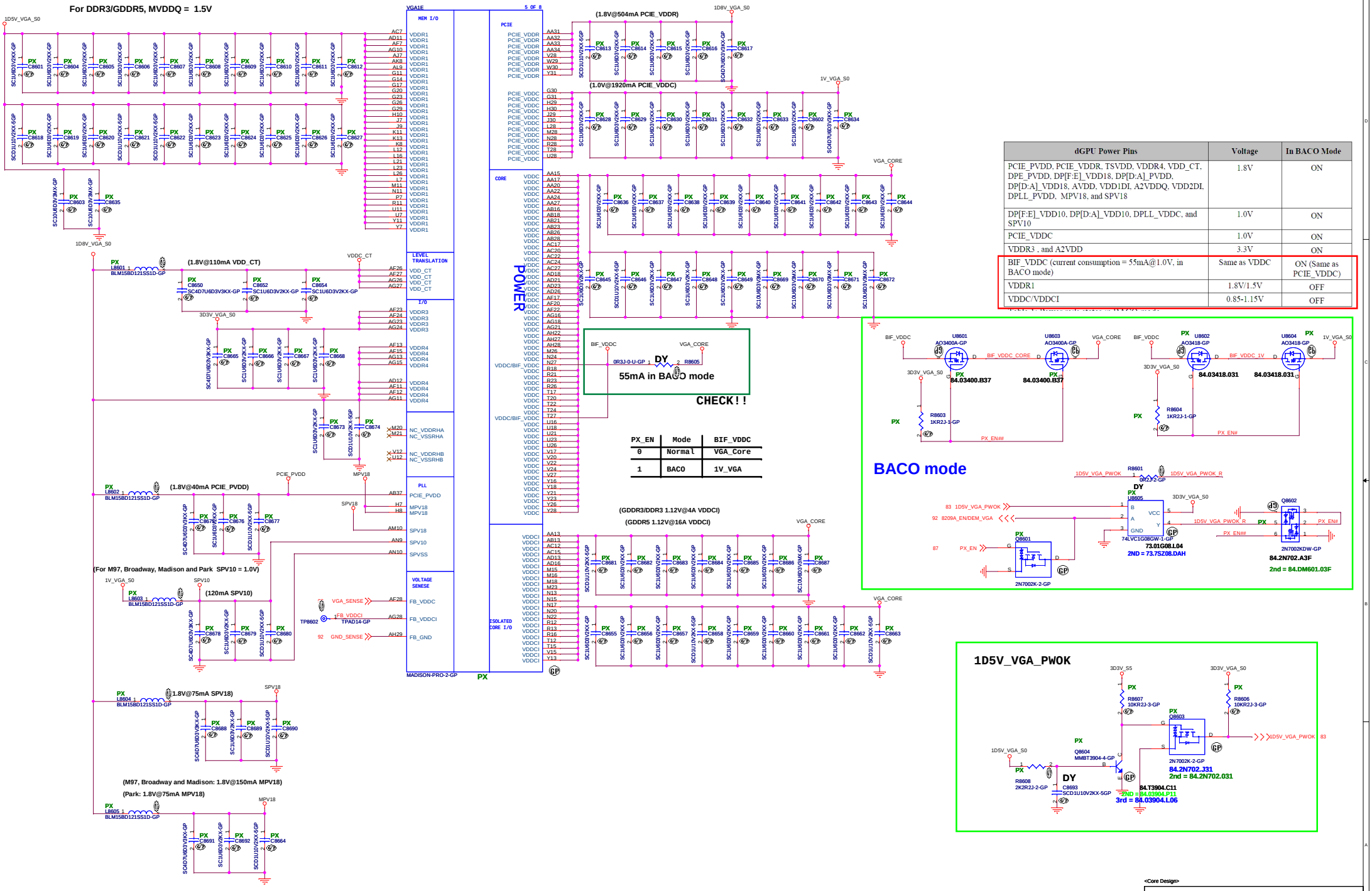
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)
Size: A2 | Document Number: LLW-1 / LGG-1 | Rev: SB
Date: Tuesday, November 09, 2010 | Sheet 85 of 94


For DDR3/GDDR5, MVDDQ = 1.5V
POWER
(1.8V@504mA PCIE_VDDR)
(1.0V@1920mA PCIE_VDDC)
(1.8V@110mA VDD_CT)
(1.8V@40mA PCIE_PVDD)
(120mA SPV10)
(For M97, Broadway, Madison and Park SPV10 = 1.0V)
(1.8V@75mA SPV18)
(M97, Broadway and Madison: 1.8V@150mA MPV18)
(Park: 1.8V@75mA MPV18)
(GDDR3/DDR3 1.12V@4A VDDCI)
(GDDR5 1.12V@16A VDDCI)
DY
55mA in BACO mode
CHECK!!
PX_EN | Mode | BIF_VDDC
0 | Normal | VGA_Core
1 | BACO | 1V_VGA
BACO mode
1D5V_VGA_PWOK
dGPU Power Pins | Voltage | In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18 | 1.8V | ON
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10 | 1.0V | ON
PCIE_VDDC | 1.0V | ON
VDDR3 , and A2VDD | 3.3V | ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode) | Same as VDDC | ON (Same as PCIE_VDDC)
VDDR1 | 1.8V/1.5V | OFF
VDDC/VDDCI | 0.85-1.15V | OFF
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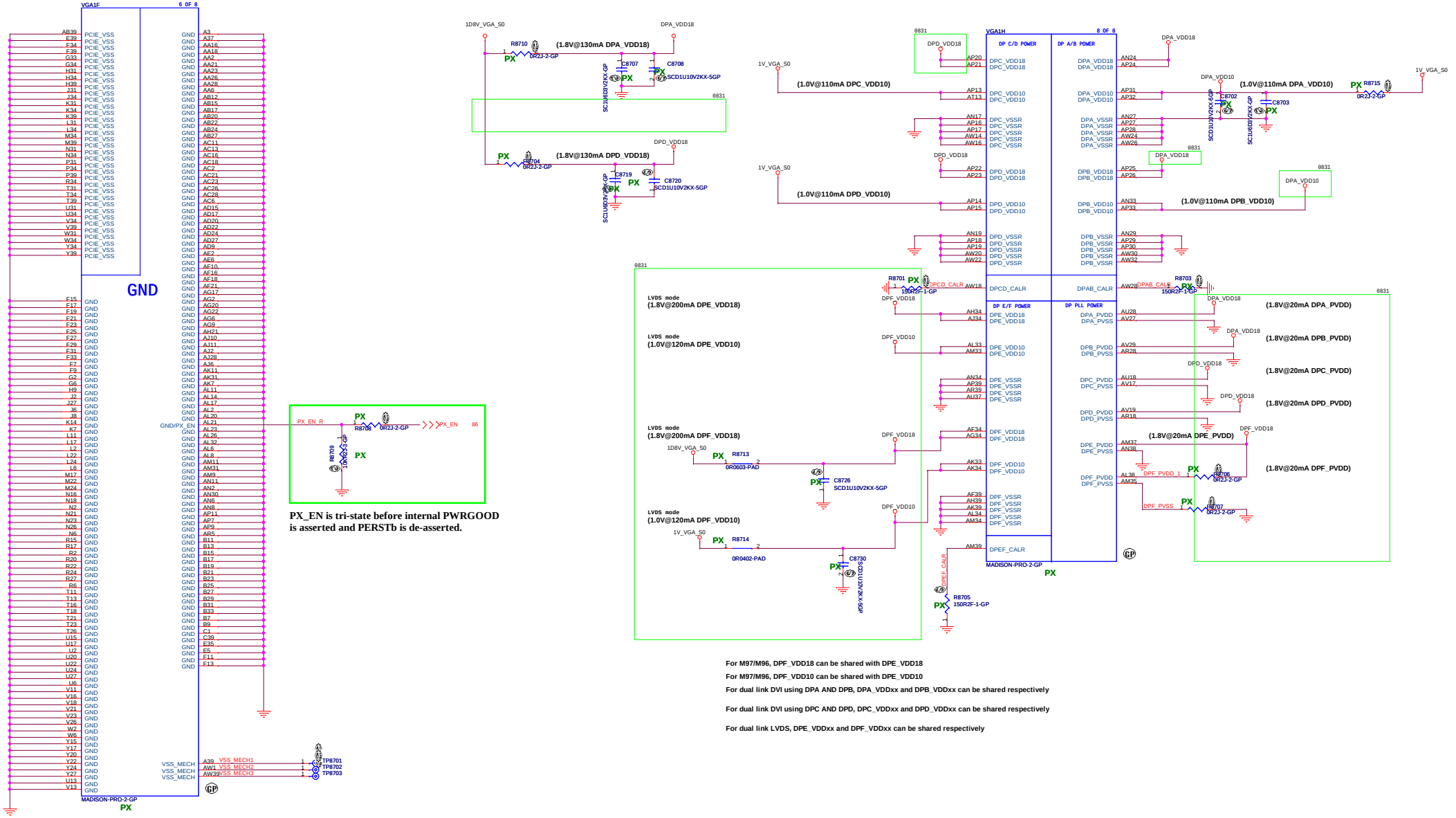
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
GPU_POWER(4/5)
LLW-1 / LGG-1
SB
Tuesday, November 09, 2010
Sheet 86 of 94



<Core Design>

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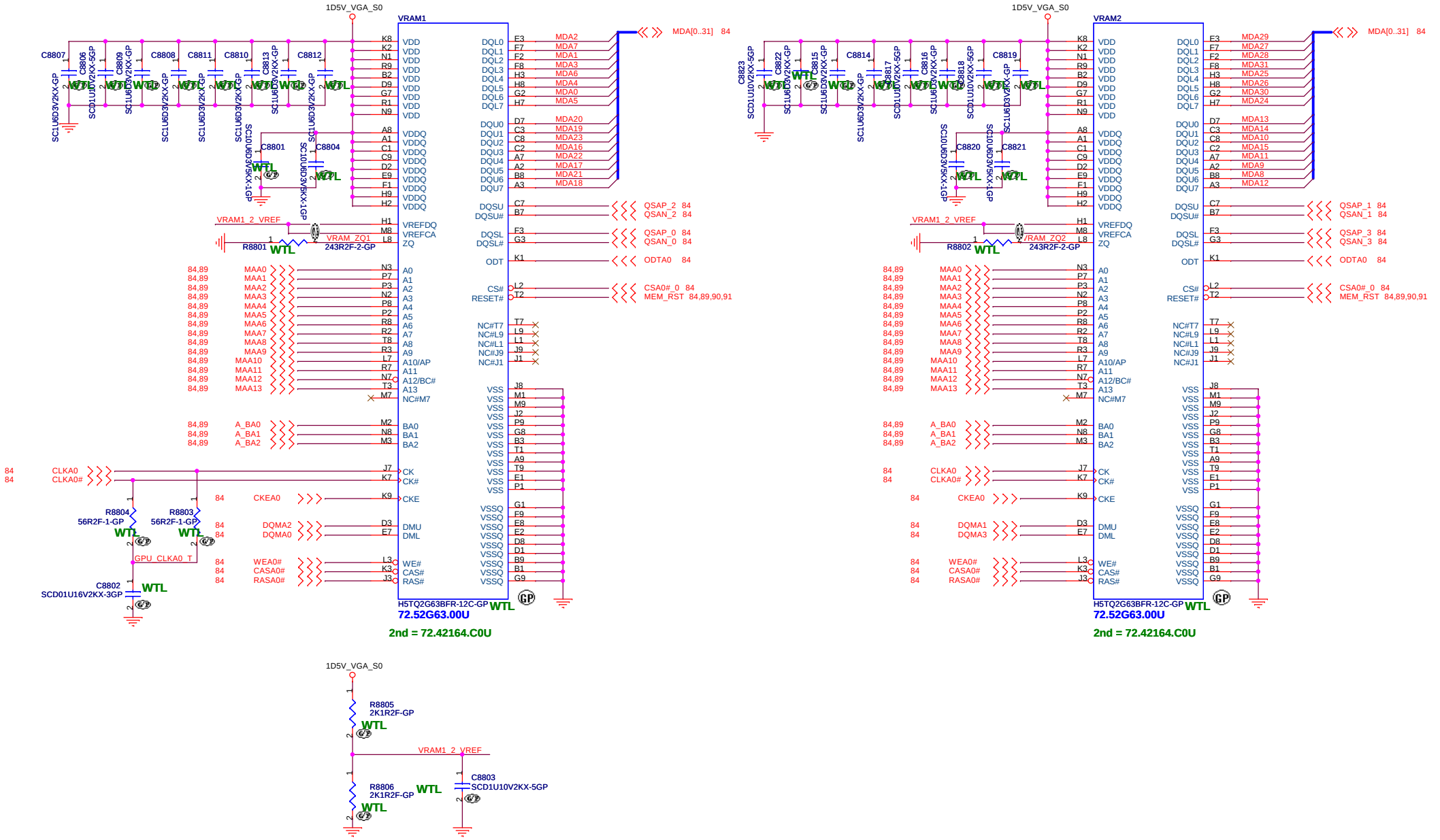
Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A2	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 87 of 94



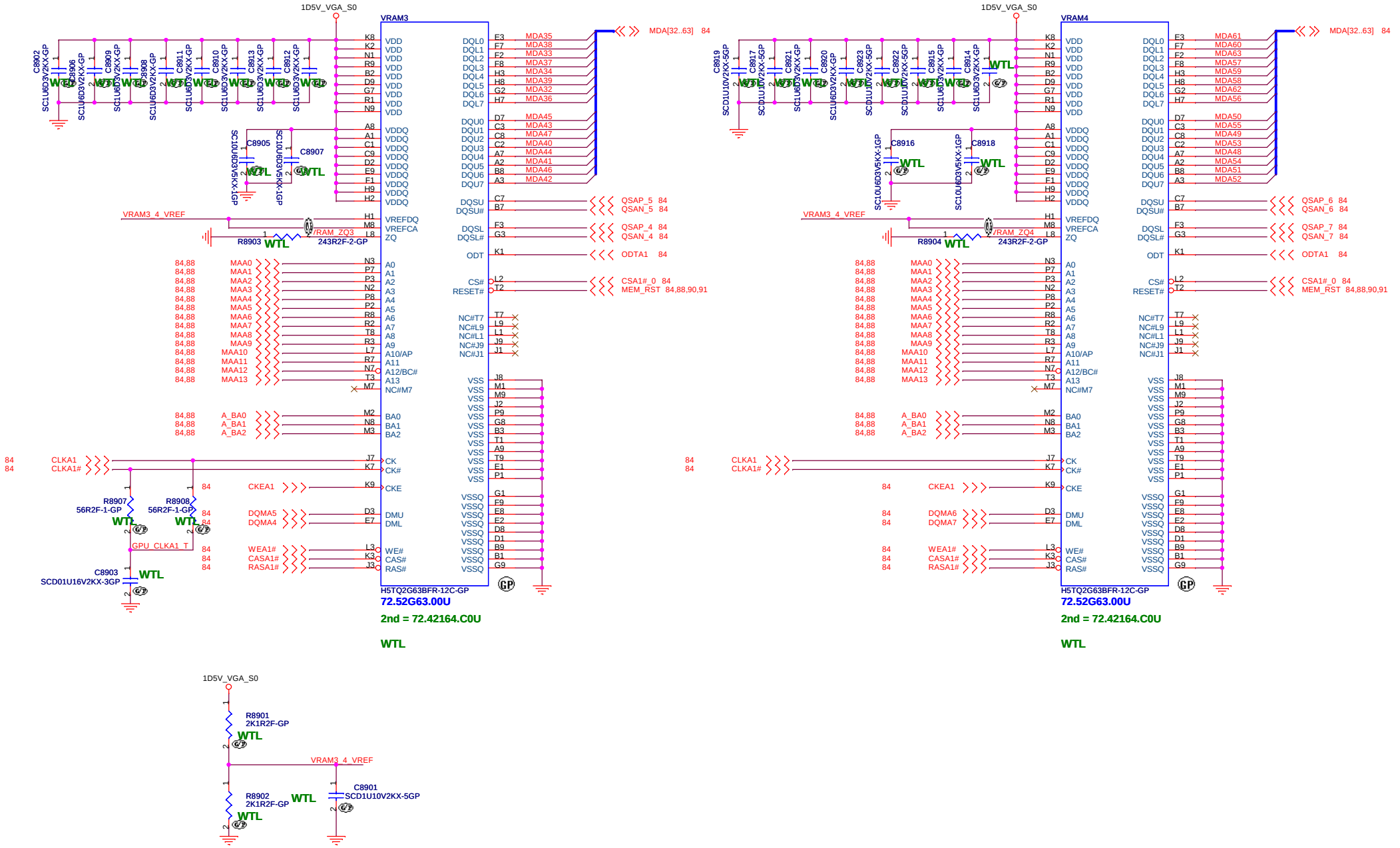
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM1,2 (1/4)**

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 88 of 94



<Core Design>

Wistron Corporation
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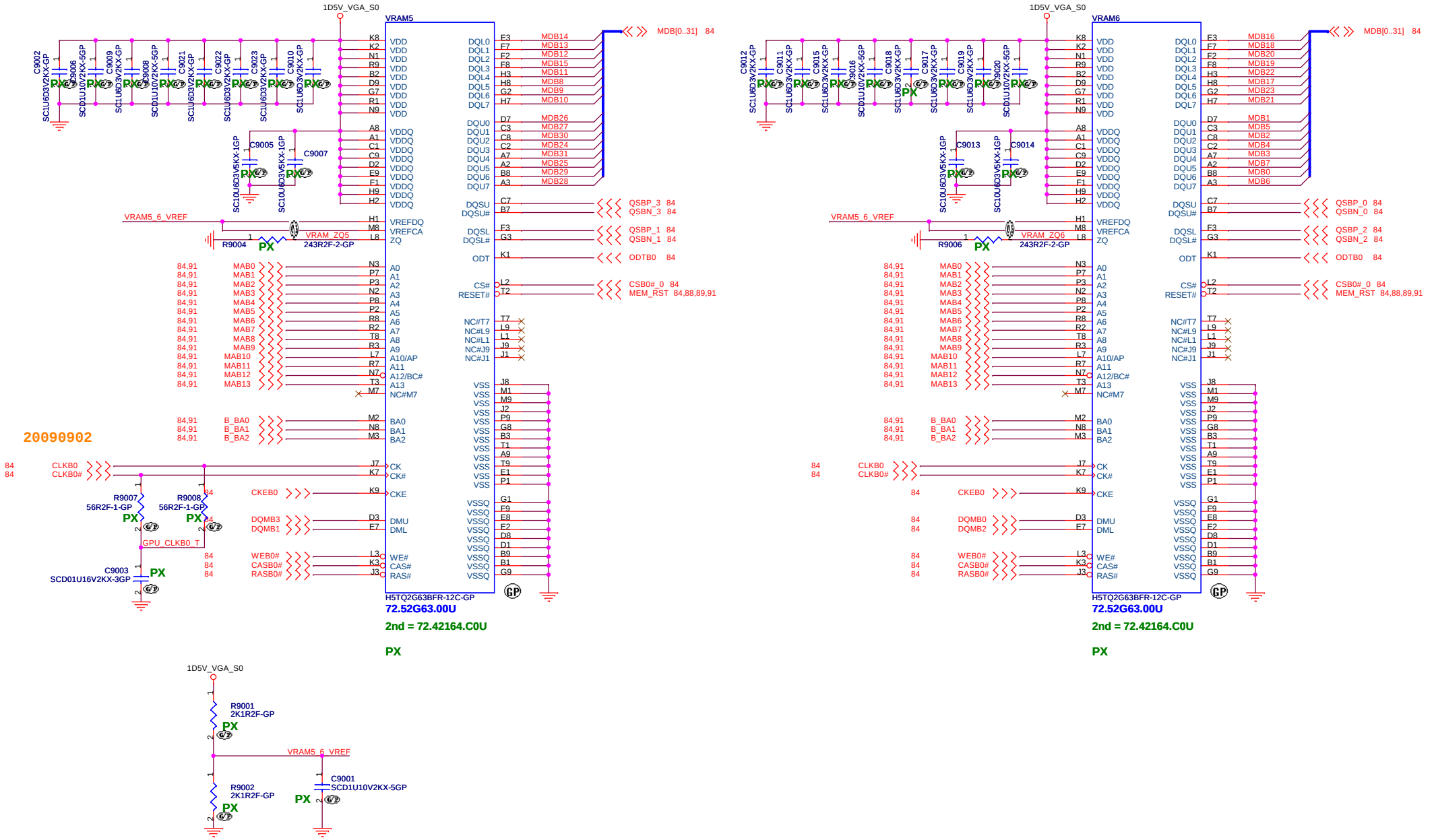
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM3,4 (2/4)**

Size	Document Number	Rev
A3	LLW-1 / LGG-1	SB

Date: Tuesday, November 09, 2010 Sheet 89 of 94



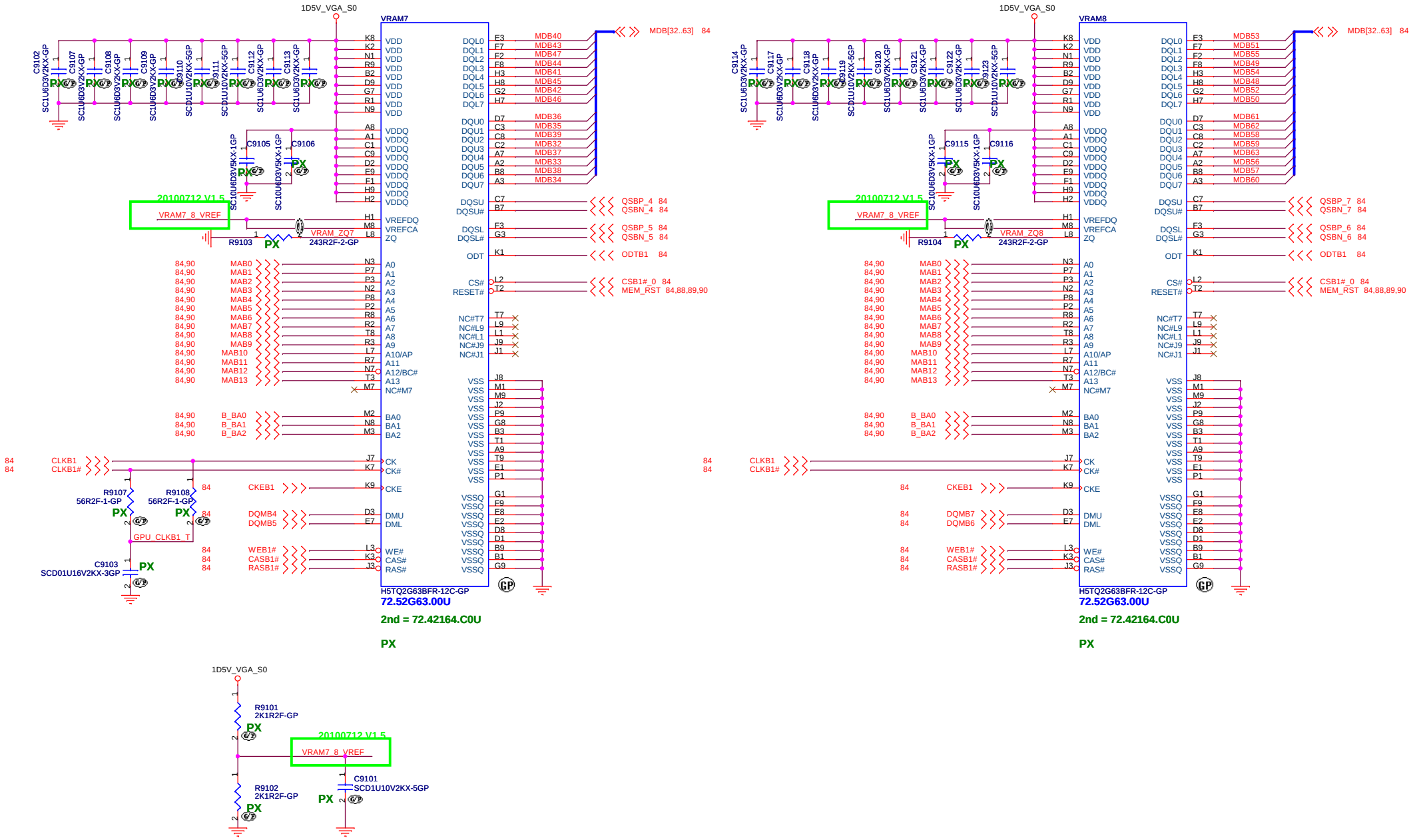
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB

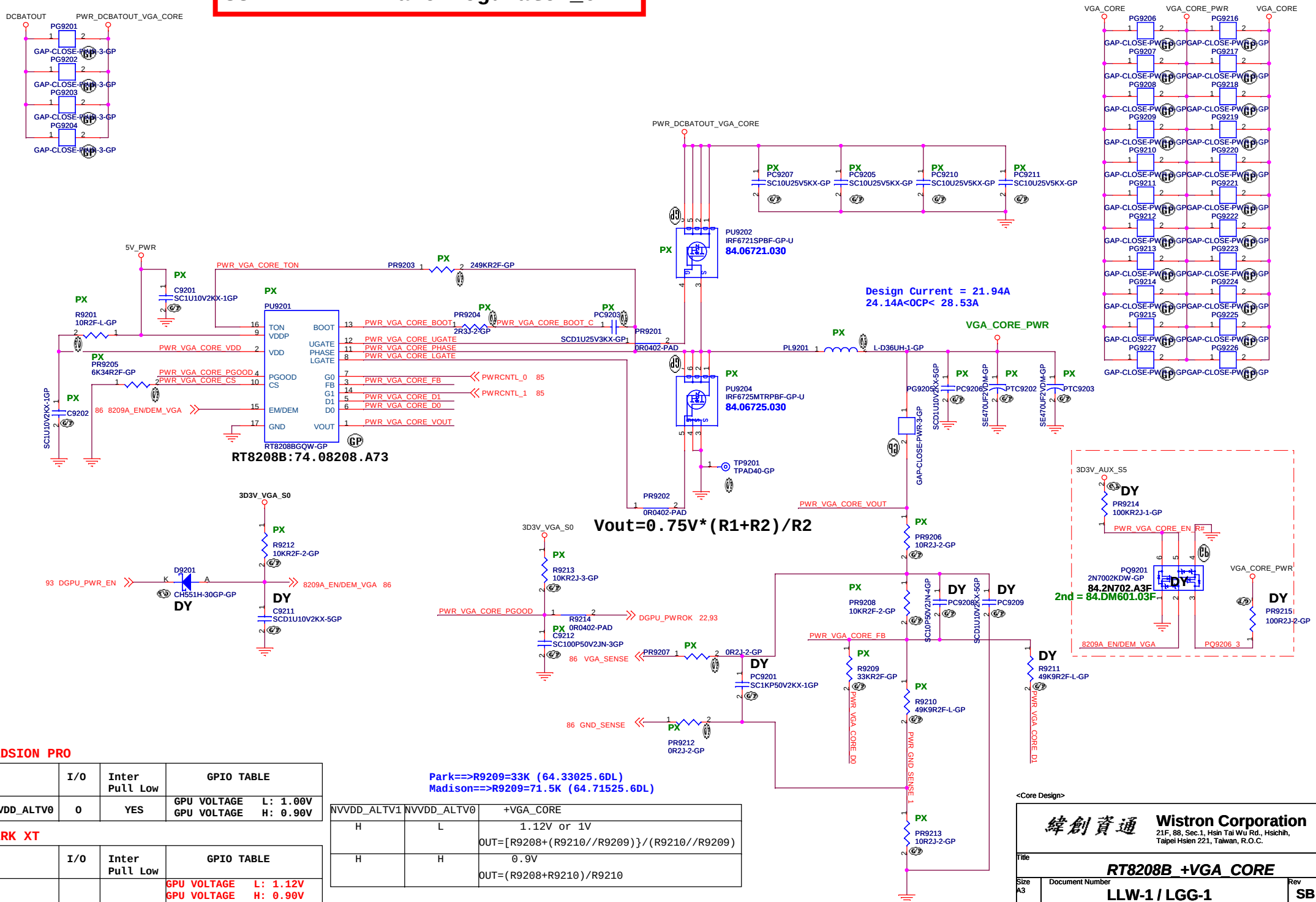
Date: Tuesday, November 09, 2010 | Sheet 90 of 94



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU-VRAM7,8 (4/4)***	
Size A3	Document Number **LLW-1 / LGG-1**	Rev **SB**
Date: Tuesday, November 09, 2010	Sheet 91 of 94	

SSID = PWR.Plane.Regulator_GFX



MADSION PRO

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

	I/O	Inter Pull Low	GPIO TABLE
			GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

Park==>R9209=33K (64.33025.6DL)
Madison==>R9209=71.5K (64.71525.6DL)

NVVDD_ALTV1	NVVDD_ALTV0	+VGA_CORE
H	L	1.12V or 1V OUT=[R9208+(R9210//R9209)}/(R9210//R9209)
H	H	0.9V OUT=(R9208+R9210)/R9210

<Core Design>

緯創資通 Wistron Corporation
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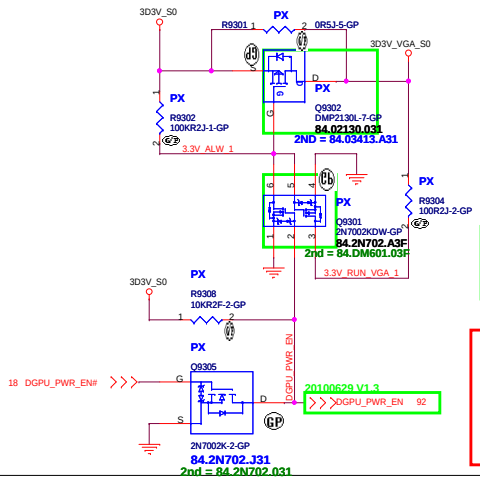
Taipei Hsien 221, Taiwan, R.O.C.

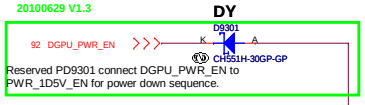
Title: RT8208B_+VGA_CORE

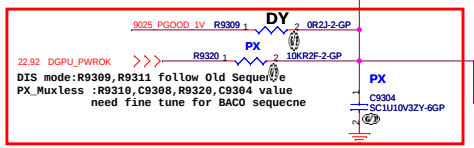
Size: A3 | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 92 of 94

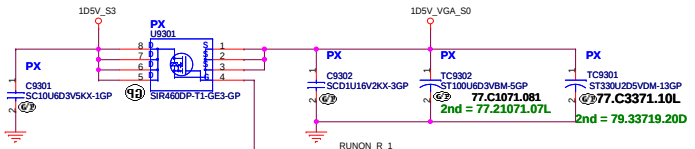
+3VS to 3.3V_DELAY Transfer

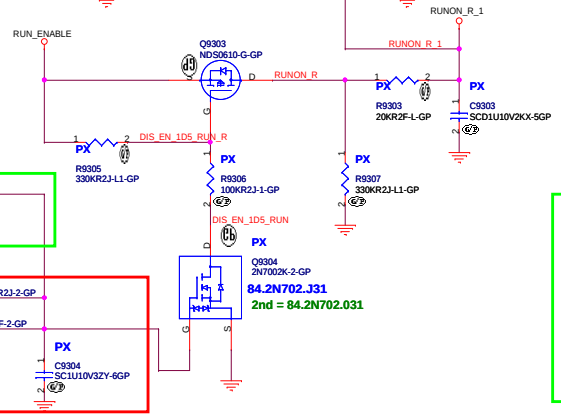


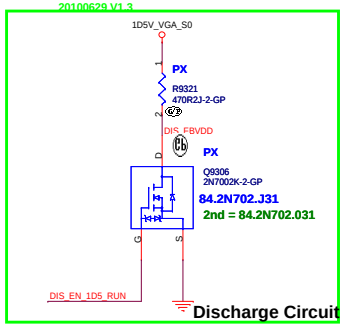


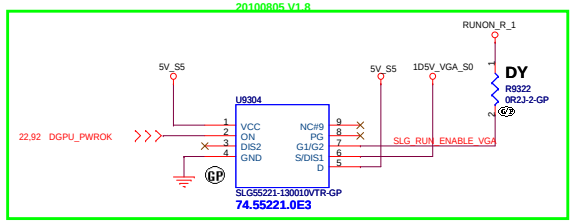


1D5V_VGA_S0

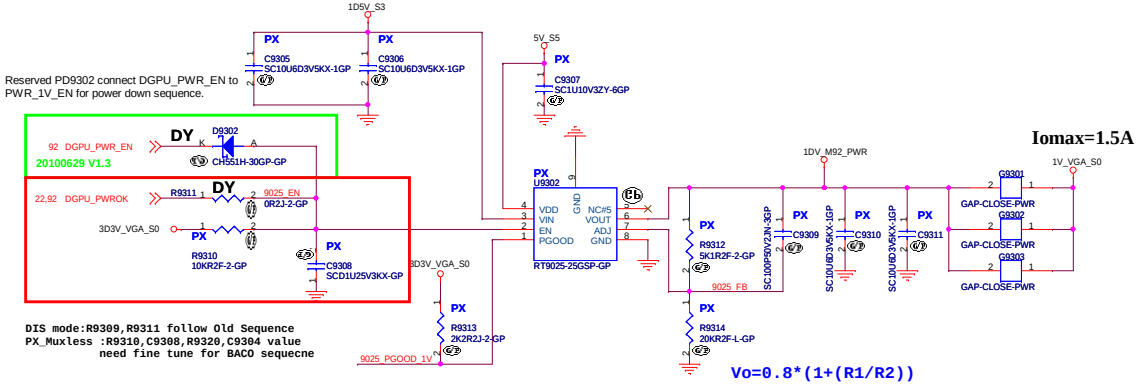


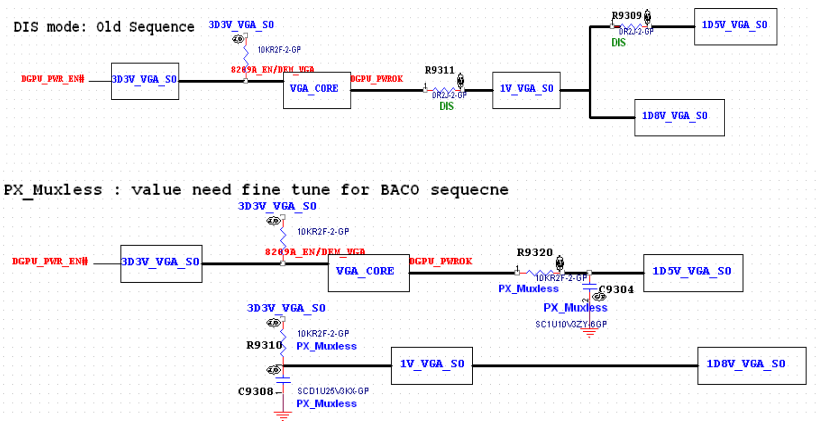






RT9025 for 1V_VGA





RT9025 for 1D8V_VGA

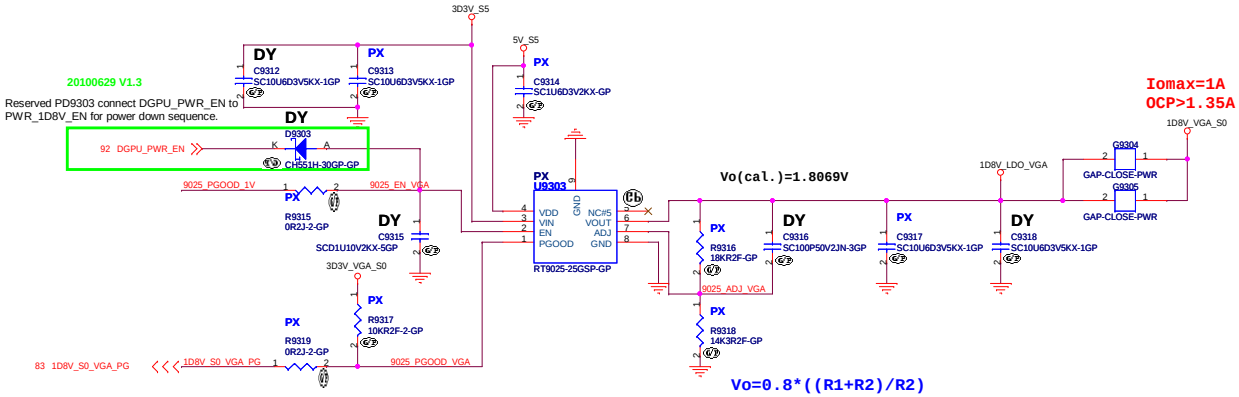


Table 93.1- Adjustable LDO Regulator multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
GMT	G9661-25ADJF11U	N/A	74.09661.07D
RICHTEK	RT9025-25GSP	N/A	74.09025.A3D

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size: C | Document Number: LLW-1 / LGG-1 | Rev: SB

Date: Tuesday, November 09, 2010 | Sheet 93 of 94

CPU

H1 HOLET157B276R134-GP — ZZ.SCREW.091
H2 HOLET157B276R134-GP — ZZ.SCREW.091
H3 HOLET157B276R134-GP — ZZ.SCREW.091
H4 HOLET157B276R134-GP — ZZ.SCREW.091

VGA

H5 HOLET157B276R134-GP — ZZ.SCREW.091
H6 HOLET157B276R134-GP — ZZ.SCREW.091

H8 HOLE237R95-GP — ZZ.00PAD.921
H9 HT85X105B85R26-S-GP — ZZ.SCREW.191
H10 HT85X105B85R26-S-GP — ZZ.SCREW.191
H11 HOLE237R95-GP — ZZ.00PAD.921
H12 HOLE237R95-GP — ZZ.00PAD.921
H13 HT6BE75R24-U-45-GP — ZZ.00PAD.971

H14 HOLE237R95-GP — ZZ.00PAD.921
H15 STF217R113H119-GP — 34.4C408.001
H16 STF256R117H221-GP — 34.4B804.001
H17 STF256R117H221-GP — 34.4B804.001
H18 HOLE315R95-GP — ZZ.00PAD.911
H19 HOLE315R95-GP — ZZ.00PAD.911
H20 HOLE315R95-GP — ZZ.00PAD.911

H21 HOLE197R67X146 — KN1.PAD.01
H22 HOLE197R67X146 — KN1.PAD.01
H23 GNDPADSR197 — ZZ.NDPAD.XXX
H24 GNDPADSR197 — ZZ.NDPAD.XXX
H25 GNDPADSR197 — ZZ.NDPAD.XXX
H26 GNDPADSR197 — ZZ.NDPAD.XXX

LGG Use

H27 HT85X105B85R26-S-GP — ZZ.SCREW.191
H28 HT6BE75R24-U-45-GP — ZZ.00PAD.971
H30 HOLE315R95-GP — ZZ.00PAD.911
H31 HOLE237R95-GP — ZZ.00PAD.921

EMI CAP

DCBATOUT: EC9701 SCD1U25V2ZY-1GP, EC9702 SCD1U25V2ZY-1GP, EC9703 SCD1U25V2ZY-1GP

3D3V_S0: EC9708 SCD1U25V2ZY-1GP, EC9709 SCD1U25V2ZY-1GP, EC9710 SCD1U25V2ZY-1GP

1D05V_VTT: EC9712 SCD1U25V2ZY-1GP, EC9721 SCD1U25V2ZY-1GP, EC9722 SCD1U25V2ZY-1GP

1D8V_S0: EC9717 SCD1U25V2ZY-1GP, EC9718 SCD1U25V2ZY-1GP

3D3V_S5: EC9704 SCD1U25V2ZY-1GP, EC9705 SCD1U25V2ZY-1GP, EC9706 SCD1U25V2ZY-1GP, EC9707 SCD1U25V2ZY-1GP

1D5V_VGA_S0: EC9711 SCD1U25V2ZY-1GP, EC9719 SCD1U25V2ZY-1GP, EC9720 SCD1U25V2ZY-1GP

1D5V_S0: EC9713 SCD1U25V2ZY-1GP, EC9714 SCD1U25V2ZY-1GP, EC9723 SCD1U25V2ZY-1GP, EC9724 SCD1U25V2ZY-1GP, EC9725 SCD1U25V2ZY-1GP, EC9726 SCD1U25V2ZY-1GP, EC9727 SCD1U25V2ZY-1GP, EC9728 SCD1U25V2ZY-1GP

5V_S5: EC9715 SCD1U25V2ZY-1GP, EC9716 SCD1U25V2ZY-1GP, EC9729 SCD1U25V2ZY-1GP, EC9730 SCD1U25V2ZY-1GP, EC9731 SCD1U25V2ZY-1GP, EC9732 SCD1U25V2ZY-1GP, EC9733 SCD1U25V2ZY-1GP

5V_S0: EC9734 SCD1U25V2ZY-1GP, EC9735 SCD1U25V2ZY-1GP, EC9736 SCD1U25V2ZY-1GP, EC9737 SCD1U25V2ZY-1GP, EC9738 SCD1U25V2ZY-1GP, EC9739 SCD1U25V2ZY-1GP, EC9740 SCD1U25V2ZY-1GP, EC9741 SCD1U25V2ZY-1GP, EC9742 SCD1U25V2ZY-1GP, EC9743 SCD1U25V2ZY-1GP, EC9744 SCD1U25V2ZY-1GP, EC9745 SCD1U25V2ZY-1GP

1D5V_S3: EC9746 SCD1U25V2ZY-1GP, EC9747 SCD1U25V2ZY-1GP, EC9748 SCD1U25V2ZY-1GP, EC9749 SCD1U25V2ZY-1GP, EC9750 SCD1U25V2ZY-1GP, EC9751 SCD1U25V2ZY-1GP

<Core Design>

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Title: UNUSED PARTS/EMI Capacitors
Size: A2 | Document Number: LLW-1 / LGG-1 | Rev: SB
Date: Tuesday, November 09, 2010 | Sheet 94 of 94