Leopard2 Block Diagram

Project code: 91.4C701.001
PCB P/N : 48.4C701.011
REVISION : 05202 -1

CLK GEN 3
ICS954206

4,5 Mobile CPU
Dothan

Host BUS
400/533MHz

6,7,8,9,10 Alviso

DMI I/F
100MHz

21,22,23,24 ICH6-M

DDRII*2 11,12

DDR-SDRAM 16,17
HY5DS573222F-28

13,14,15 VGA
ATI M26P

PEG

LVDS → LCD 19

SVIDEO/COMP → TVOUT 18

RGB CRT → CRT

DAUGHTER BOARD

BLUE THUMB

USB 2.0 → USB x 2
USB x 2 35

P EIDE → HDD 26

S EIDE → DVD/ CD-RW 26

PCI EXPRESS/ USB2.0 → EXPRESSCARD 26

LPC Bus

1394 Conn 31

PCMCIA 1 SLOT 29

Power Switch 28
TPS2220A

SD/MS 6 in 1 Card Slost 29

27,28 PCI 7411
CARDBUS
1394
SD/MS/MMC/SM

Mini-PCI 34
802.11a/b/g

RJ45 CONN 31

10/100 RTL8100C 30,31

PCI BUS

RJ11 CONN 31

MODEM 35
MDC Card

AC97-LINK

MIC IN 18

AC'97 CODEC 31
AD1981B

LINE OUT

OP AMP 33
G1420B

DAUGHTER BOARD

Docking 18

KBC 36
NS97551

LPC Debug Conn 38

Power Switch 26
TPS2231

Comsumer IR 35

Touch Pad 37

Int. KB 37

Thermal & Fan 25
G768D

FlashRom 38
4Mb
(512kB)

SYSTEM DC/DC TPS5130 42	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 5V_S3 3V_AUX

SYSTEM DC/DC MAX8743 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_VGA_S0

MAXIM CHARGER MAX8725 40	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC MAX1907 41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4
L7: GND
L8: Signal 5

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: Leopard2 | Rev: -1
Date: Monday, July 11, 2005 | Sheet 1 of 47

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D8V= 2.8 Voltage power up on system work(S0 state)
1D8V_S3= 1.8 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF= 0.9 Voltage power up on system work(S0 state)
1D2V_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
VRAM_VDDQ= 1.8 Voltage power up on system work(S0 state) for VRAM
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power

PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0#/GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1#/GNT1#
LAN	AD23	P_INTE#	REQ2#/GNT2#
Blue Thumb	AD24		

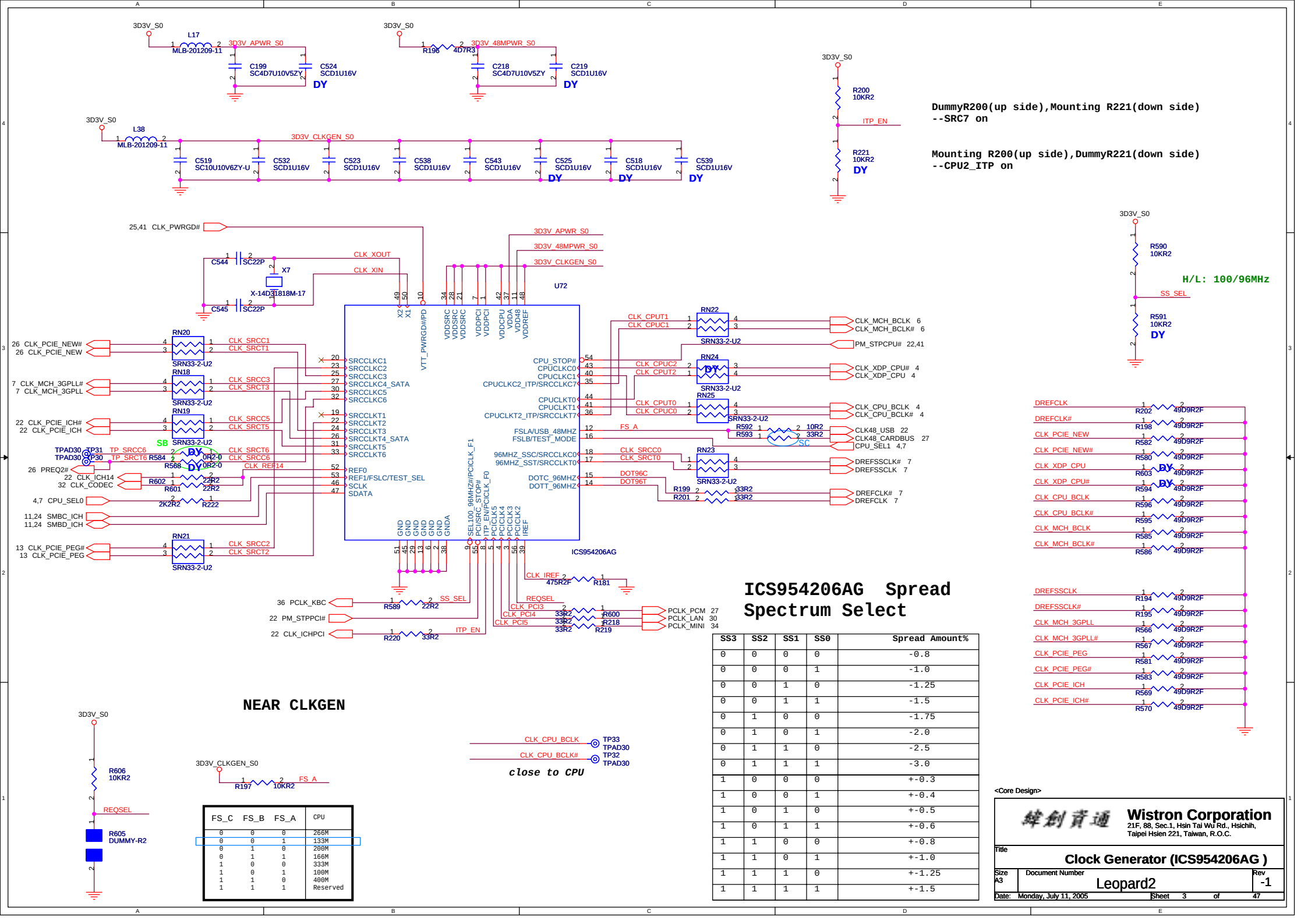
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ITP*

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Wednesday, July 06, 2005 | Sheet 2 of 47



ICS954206AG Spread Spectrum Select

SS3	SS2	SS1	SS0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+-0.3
1	0	0	1	+-0.4
1	0	1	0	+-0.5
1	0	1	1	+-0.6
1	1	0	0	+-0.8
1	1	0	1	+-1.0
1	1	1	0	+-1.25
1	1	1	1	+-1.5

FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

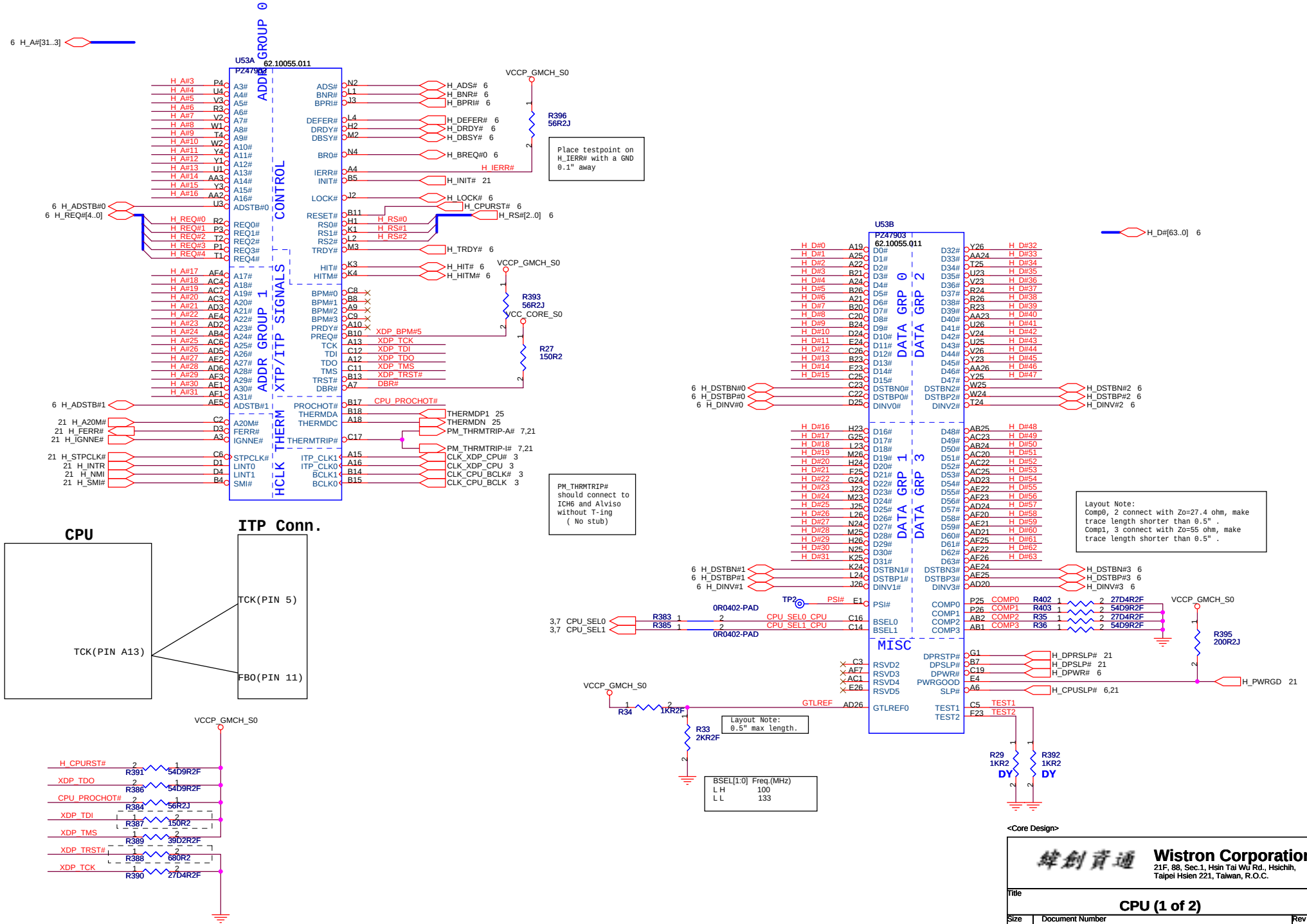
<Core Design>

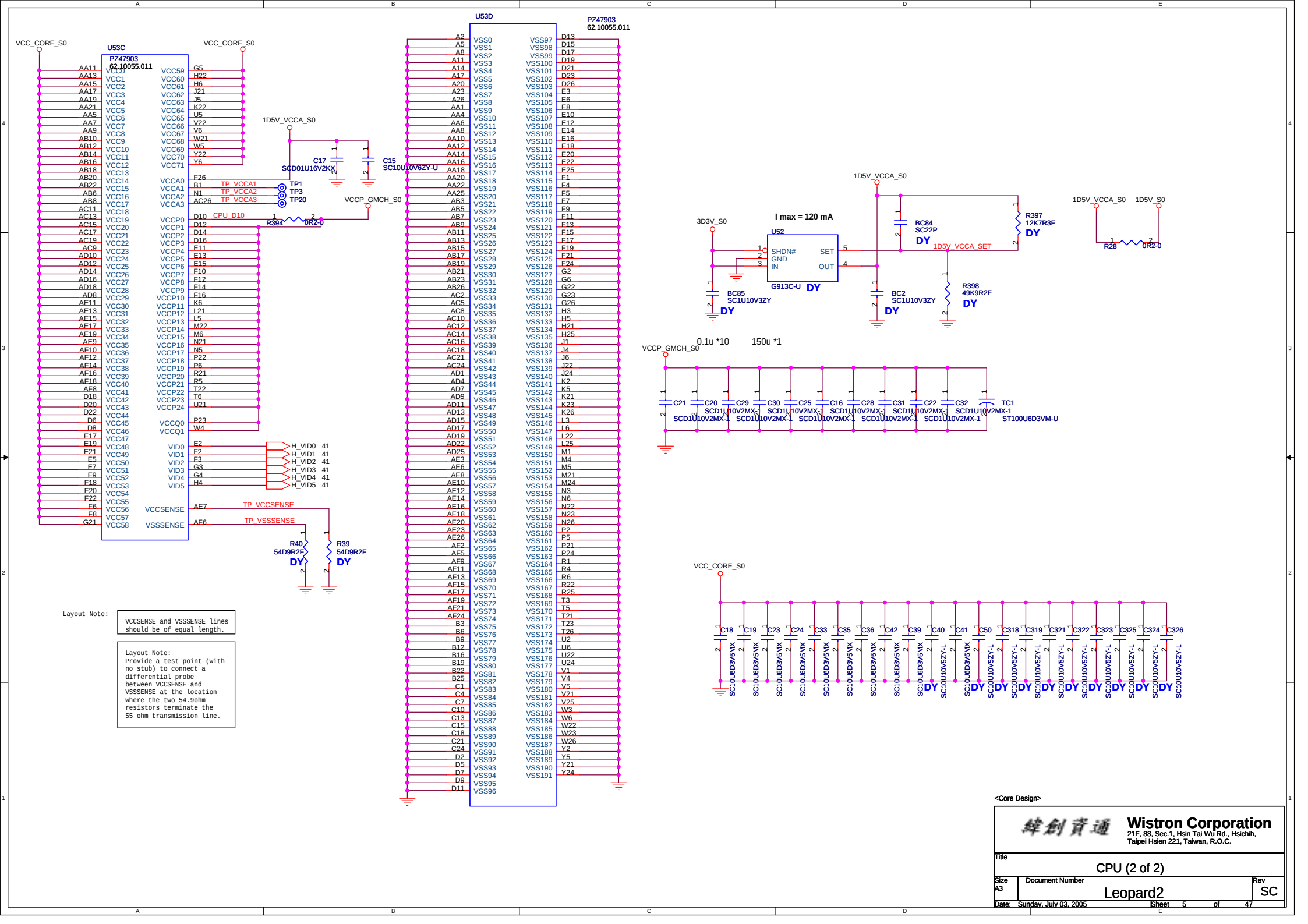
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

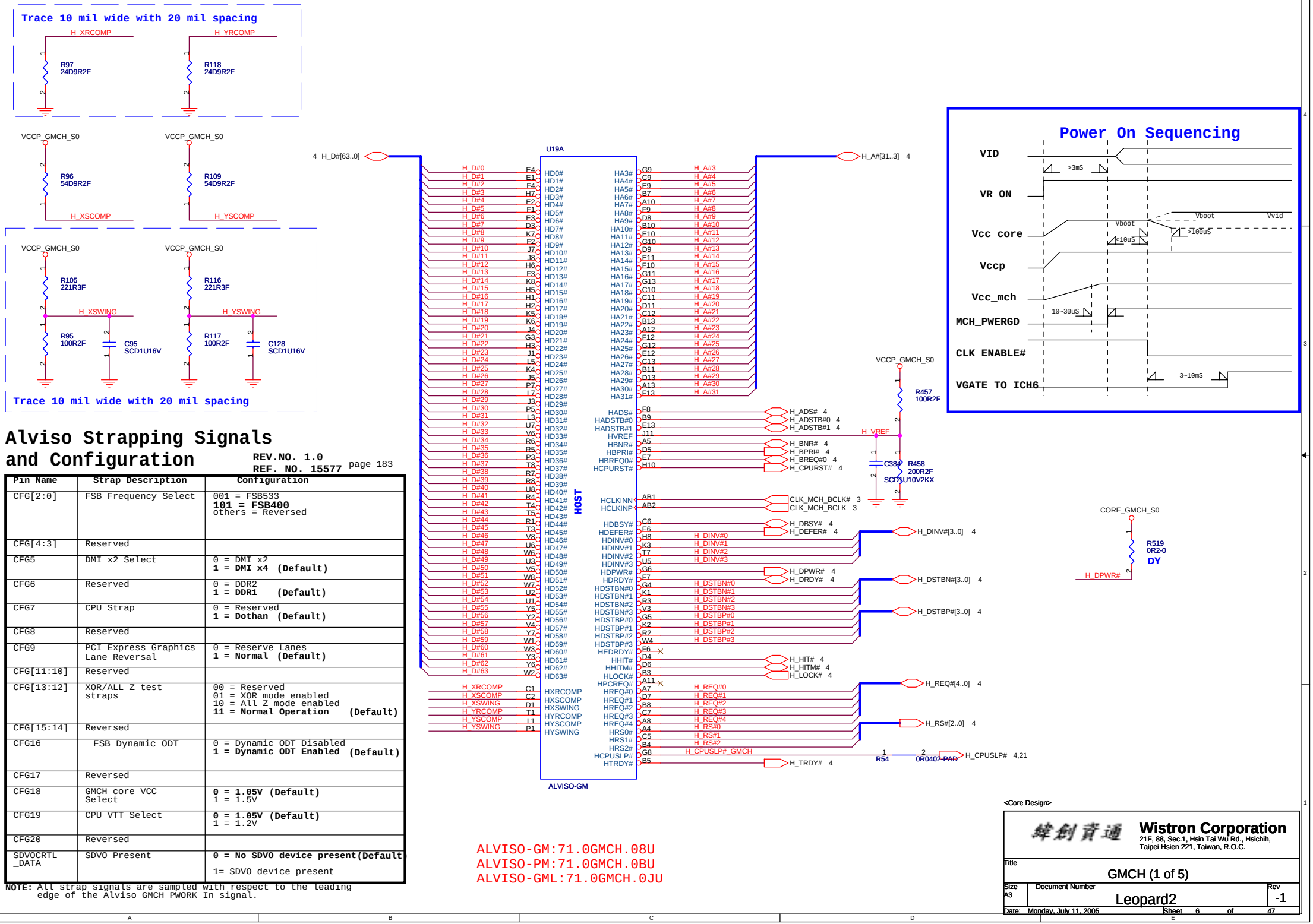
Title: Clock Generator (ICS954206AG)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Monday, July 11, 2005 | Sheet 3 of 47


U53A
62.10055.011
PZ47902
ADDR GROUP 0
ADDR GROUP 1
XTP/ITP SIGNALS
CONTROL
HCLK THERM
6 H_A#[31..3]
6 H_ADSTB#0
6 H_REQ#[4..0]
6 H_ADSTB#1
21 H_A20M#
21 H_FERR#
21 H_IGNNE#
21 H_STPCLK#
21 H_INTR
21 H_NMI
21 H_SMI#
VCCP_GMCH_S0
R396 56R2J
R393 56R2J
R27 150R2
VCC_CORE_S0
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)
CPU
ITP Conn.
TCK(PIN A13)
TCK(PIN 5)
FBO(PIN 11)
R391 54D9R2F
R386 54D9R2F
R384 56R2J
R387 150R2
R389 39D2R2F
R388 680R2
R390 27D4R2F
All place within 2" to CPU
U53B
PZ47903
62.10055.011
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
6 H_DSTBN#0
6 H_DSTBP#0
6 H_DINV#0
6 H_DSTBN#1
6 H_DSTBP#1
6 H_DINV#1
H_DSTBN#2 6
H_DSTBP#2 6
H_DINV#2 6
H_DSTBN#3 6
H_DSTBP#3 6
H_DINV#3 6
H_D#[63..0] 6
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
TP2
R383 0R0402-PAD
R385 0R0402-PAD
3,7 CPU_SEL0
3,7 CPU_SEL1
R402 27D4R2F
R403 54D9R2F
R35 27D4R2F
R36 54D9R2F
R395 200R2J
H_DPRSLP# 21
H_DPSLP# 21
H_DPWR# 6
H_PWRGD 21
H_CPUSLP# 6,21
R34 1KR2F
R33 2KR2F
Layout Note: 0.5" max length.
R29 1KR2 DY
R392 1KR2 DY
BSEL[1:0] Freq.(MHz)
L H 100
L L 133
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (1 of 2)
Size A3
Document Number
Leopard2
Rev -1
Date: Monday, July 11, 2005
Sheet 4 of 47


U53C
PZ47903
62.10055.011
U53D
PZ47903
62.10055.011
VCC_CORE_S0
1D5V_VCCA_S0
VCCP_GMCH_S0
C17
SCD01U16V2KX
C15
SC10U10V6ZY-U
TP1
TP3
TP20
TP_VCCA1
TP_VCCA2
TP_VCCA3
CPU_D10
R394
0R2-0
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
TP_VCCSENSE
TP_VSSSENSE
R40
54D9R2F
R39
54D9R2F
DY
I max = 120 mA
3D3V_S0
U52
SHDN#
GND
IN
SET
OUT
G913C-U
BC85
SC1U10V3ZY
BC84
SC22P
BC2
SC1U10V3ZY
1D5V_VCCA_SET
R397
12K7R3F
R398
49K9R2F
1D5V_S0
R28
0R2-0
0.1u *10
150u *1
C21
C20
C29
C30
C25
C16
C28
C31
C22
C32
TC1
SCD1U10V2MX-1
ST100U6D3VM-U
C18
C19
C23
C24
C33
C35
C36
C42
C39
C40
C41
C50
C318
C319
C321
C322
C323
C325
C324
C326
SC10U6D3V5MX
SC10U10V5ZY-L
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2 of 2)
Size
A3
Document Number
Leopard2
Rev
SC
Date: Sunday, July 03, 2005
Sheet 5 of 47



Alviso Strapping Signals and Configuration

REV.NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 **101 = FSB400** others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	Reserved	0 = DDR2 **1 = DDR1 (Default)**
CFG7	CPU Strap	0 = Reserved **1 = Dothan (Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes **1 = Normal (Default)**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation (Default)**
CFG[15:14]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Reversed	
CFG18	GMCH core VCC Select	**0 = 1.05V (Default)** 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V (Default)** 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present(Default)** 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

ALVISO-GM:71.0GMCH.08U
ALVISO-PM:71.0GMCH.0BU
ALVISO-GML:71.0GMCH.0JU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (1 of 5)
Size: A3
Document Number: Leopard2
Rev: -1
Date: Monday, July 11, 2005
Sheet 6 of 47

Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die

U19B

DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
ALVISO-GM

Intel suggest NC Due to votusly DVO

U19G

MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
ALVISO-GM

Note: CRT_RED, CRT_GREEN, CRT_BLUE, are ground referenced.

Intel design guide suggest Ref no.:14511 page 210

Place 150 Ohm termination resistors close to GMCH

Note: Intel design guide suggest(page 203) If the LVDS interface is not implementd, all signals associated with the interface can be left as no connects.

Layout Note: Route as short as possible

DDR_VREF_S3

C154 SCD1U10V2MX-1

2D5V_S0

FOR DDR2

1D8V_S3

VCCP_GMCH_S0

Ref ALVISO EDS-1 Page 115

For Dothan-B

DY DY

CFG(2..1) FREQ.(MHz)
10 400
00 533
11 Reserved

CFG2=0(R419):133MHZ
CFG2=1(R420):100MHZ

When Low 2.2K Ohm

When High 1K Ohm

<Core Design>

Strapping

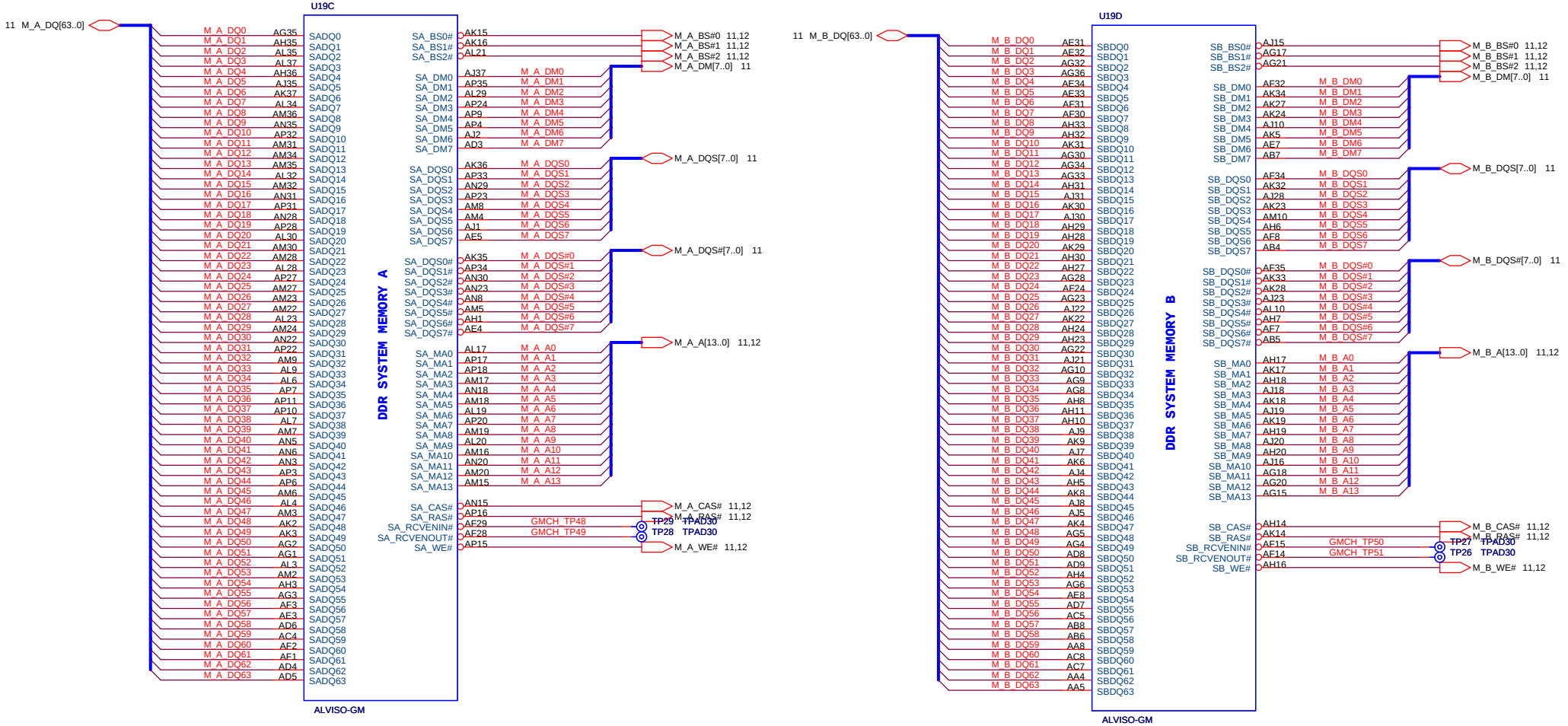
CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (2 of 5)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Thursday, July 07, 2005 | Sheet 7 of 47



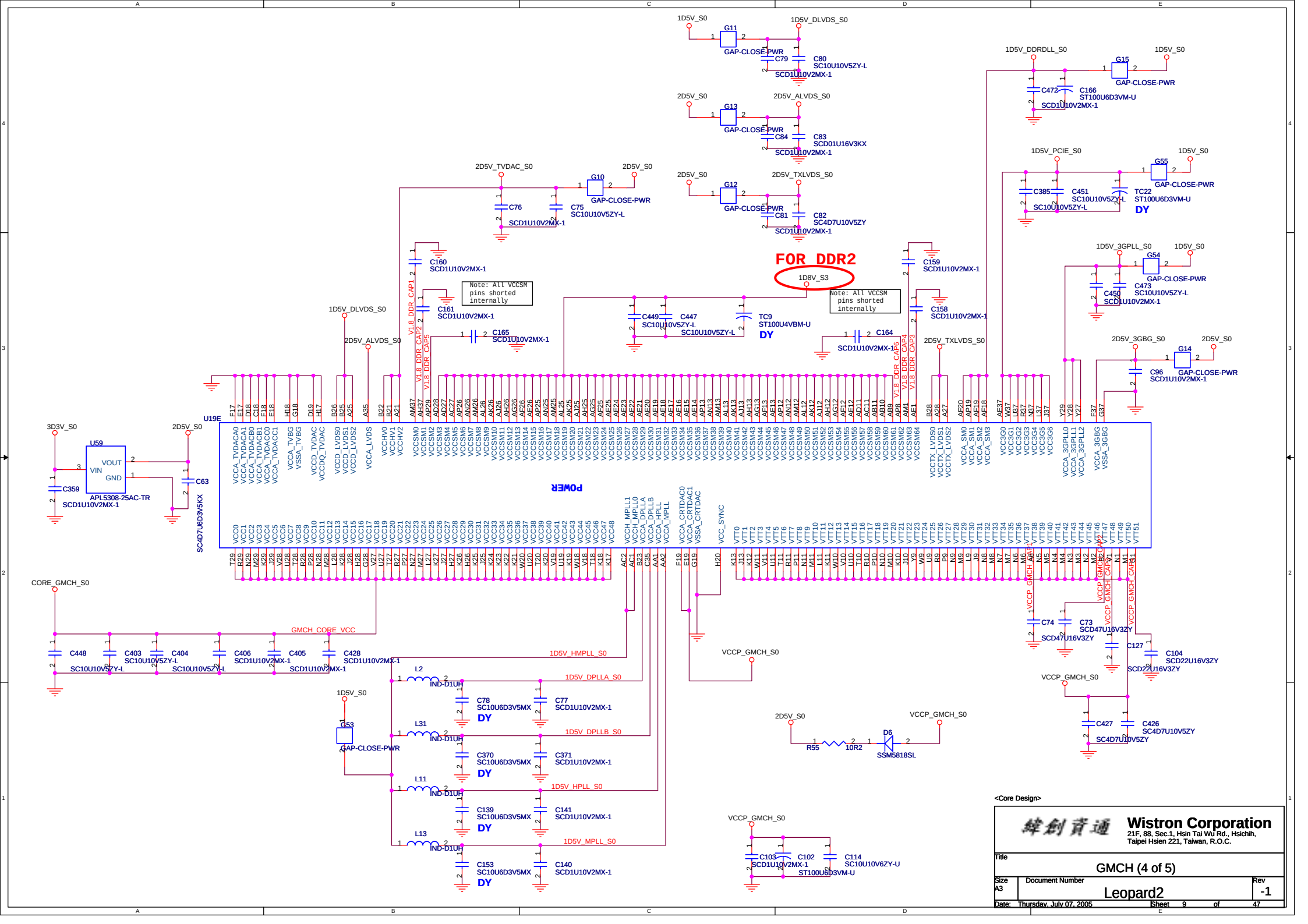
<Core Design>

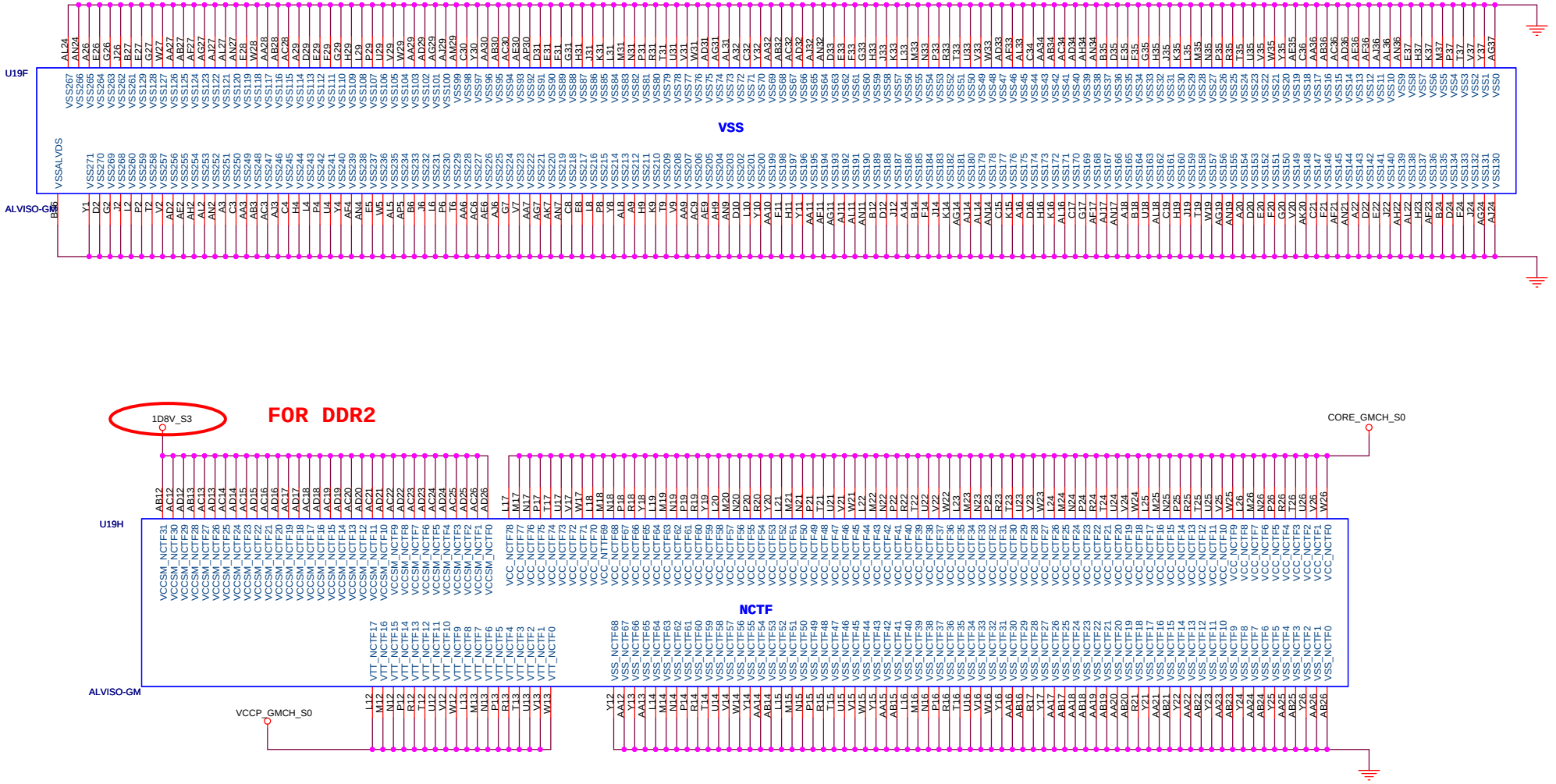
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (3 of 5)

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 8 of 47


FOR DDR2
1D8V_S3
POWER
U19E
Note: All VCCSM pins shorted internally
Note: All VCCSM pins shorted internally
DY
DY
DY
DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (4 of 5)
Size A3
Document Number
Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 9 of 47



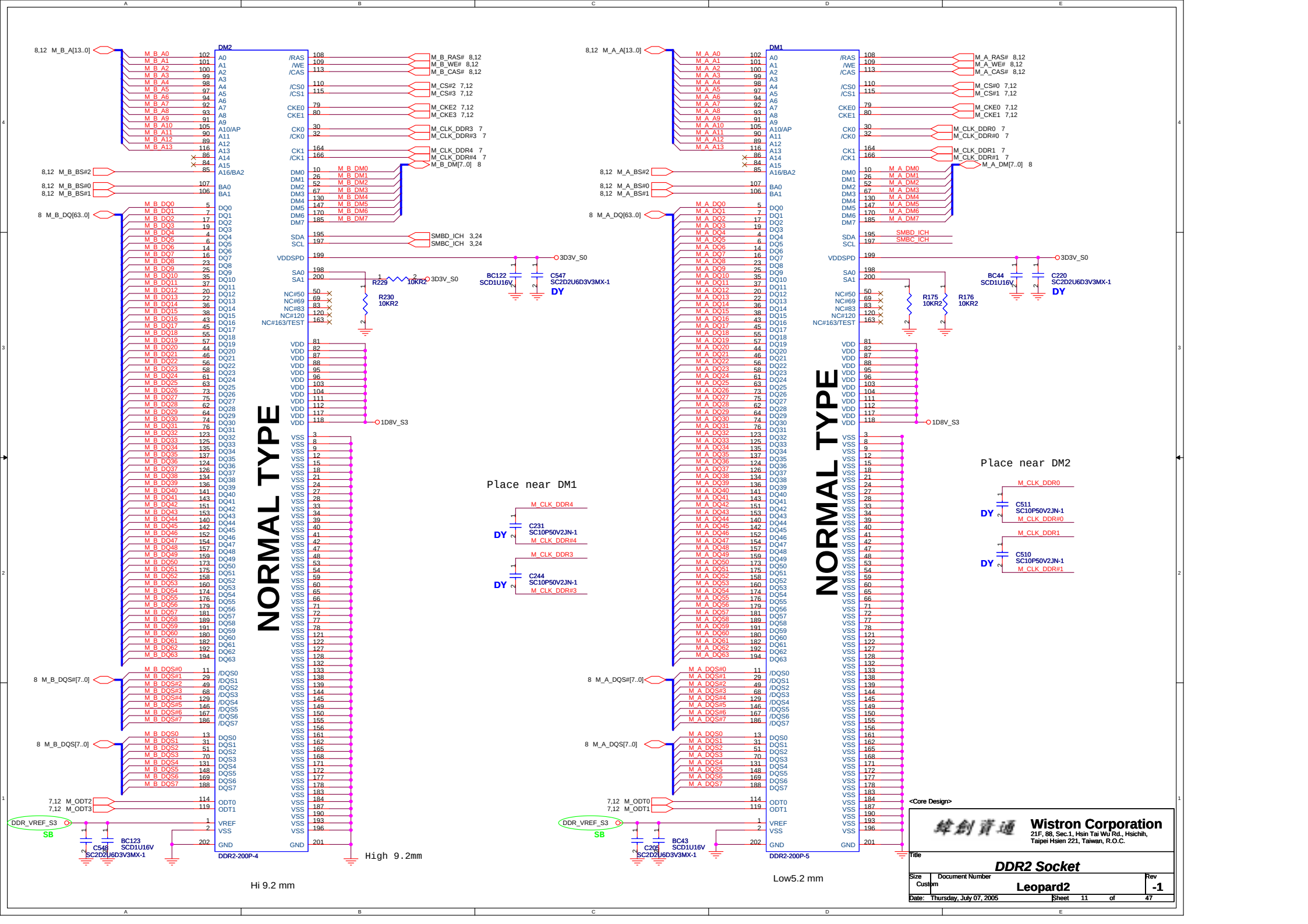
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (5 of 5)

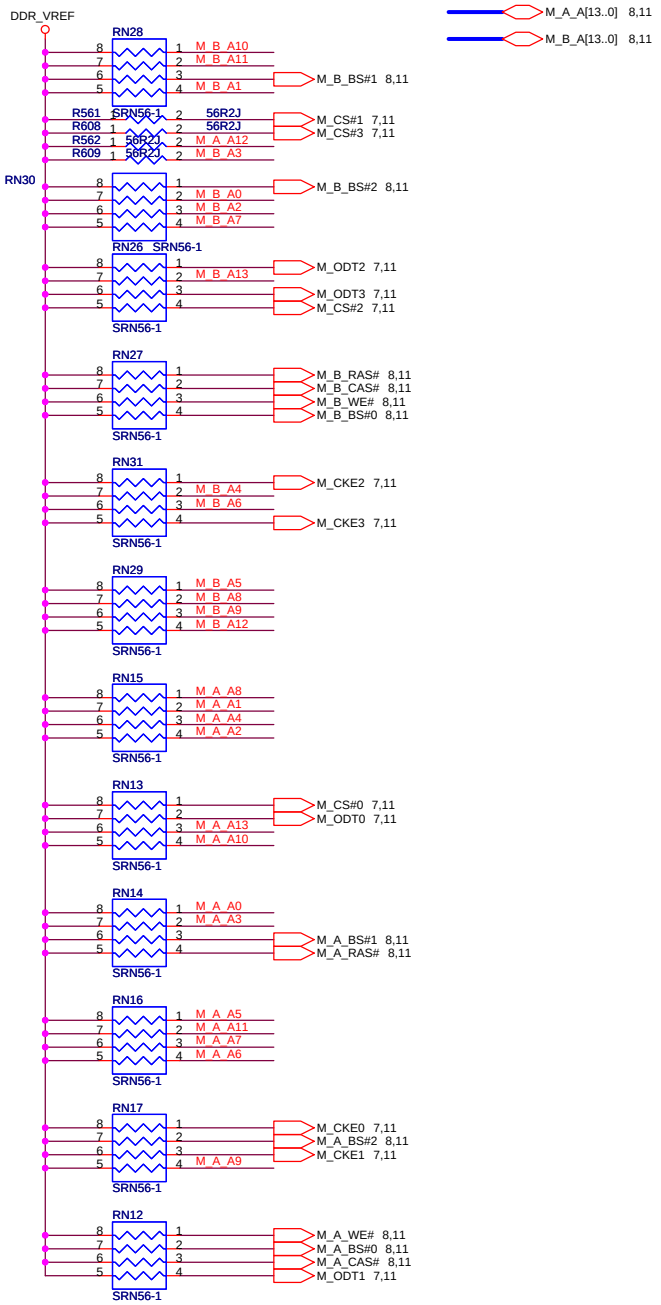
Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 10 of 47


DM2
NORMAL TYPE
DDR2-200P-4
Hi 9.2 mm
High 9.2mm
DM1
NORMAL TYPE
DDR2-200P-5
Low5.2 mm
Place near DM1
Place near DM2
R229 10KR2
R230 10KR2
R175 10KR2
R176 10KR2
BC122 SCD1U16V
C547 SC2D2U6D3V3MX-1 DY
BC44 SCD1U16V
C220 SC2D2U6D3V3MX-1 DY
C231 SC10P50V2JN-1 DY
C244 SC10P50V2JN-1 DY
C511 SC10P50V2JN-1 DY
C510 SC10P50V2JN-1 DY
C548 SCD1U16V SC2D2U6D3V3MX-1
BC123 SCD1U16V
C205 SC2D2U6D3V3MX-1
BC43 SCD1U16V
DDR_VREF_S3
SB
3D3V_S0
1D8V_S3
SMBD_ICH 3,24
SMBC_ICH 3,24
M_CLK_DDR4
M_CLK_DDR#4
M_CLK_DDR3
M_CLK_DDR#3
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size Custom
Document Number Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 11 of 47

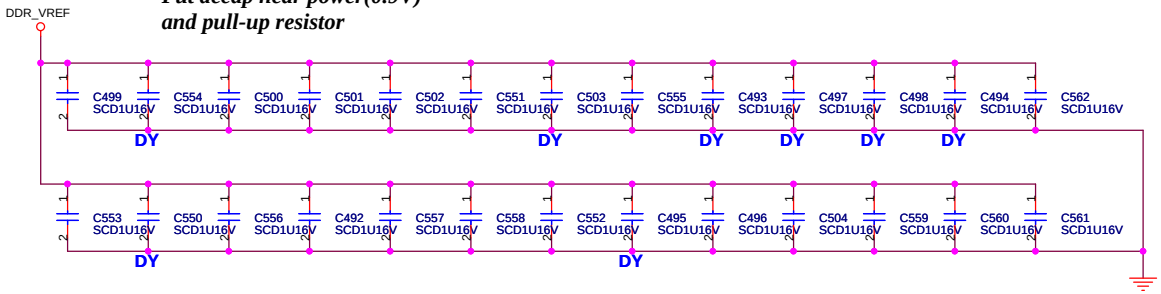
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

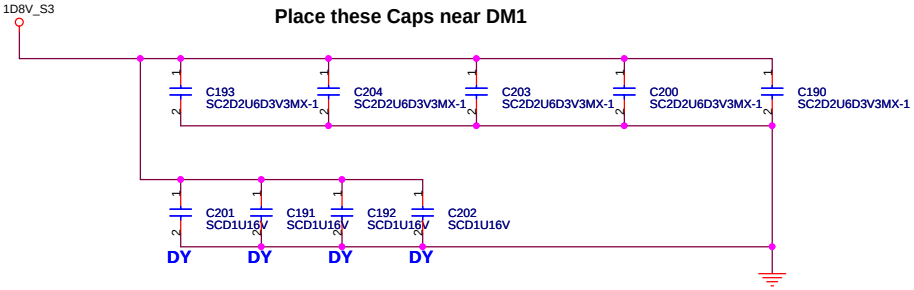


Decoupling Capacitor

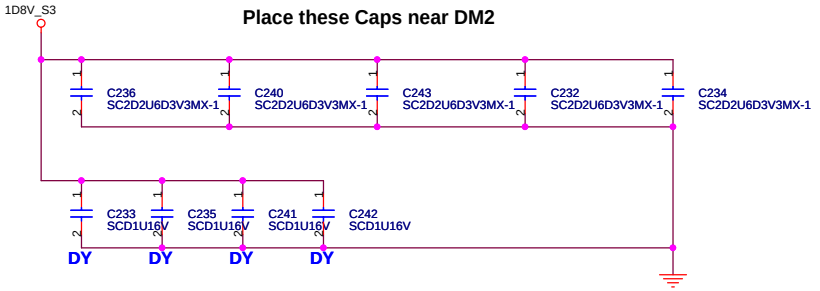
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



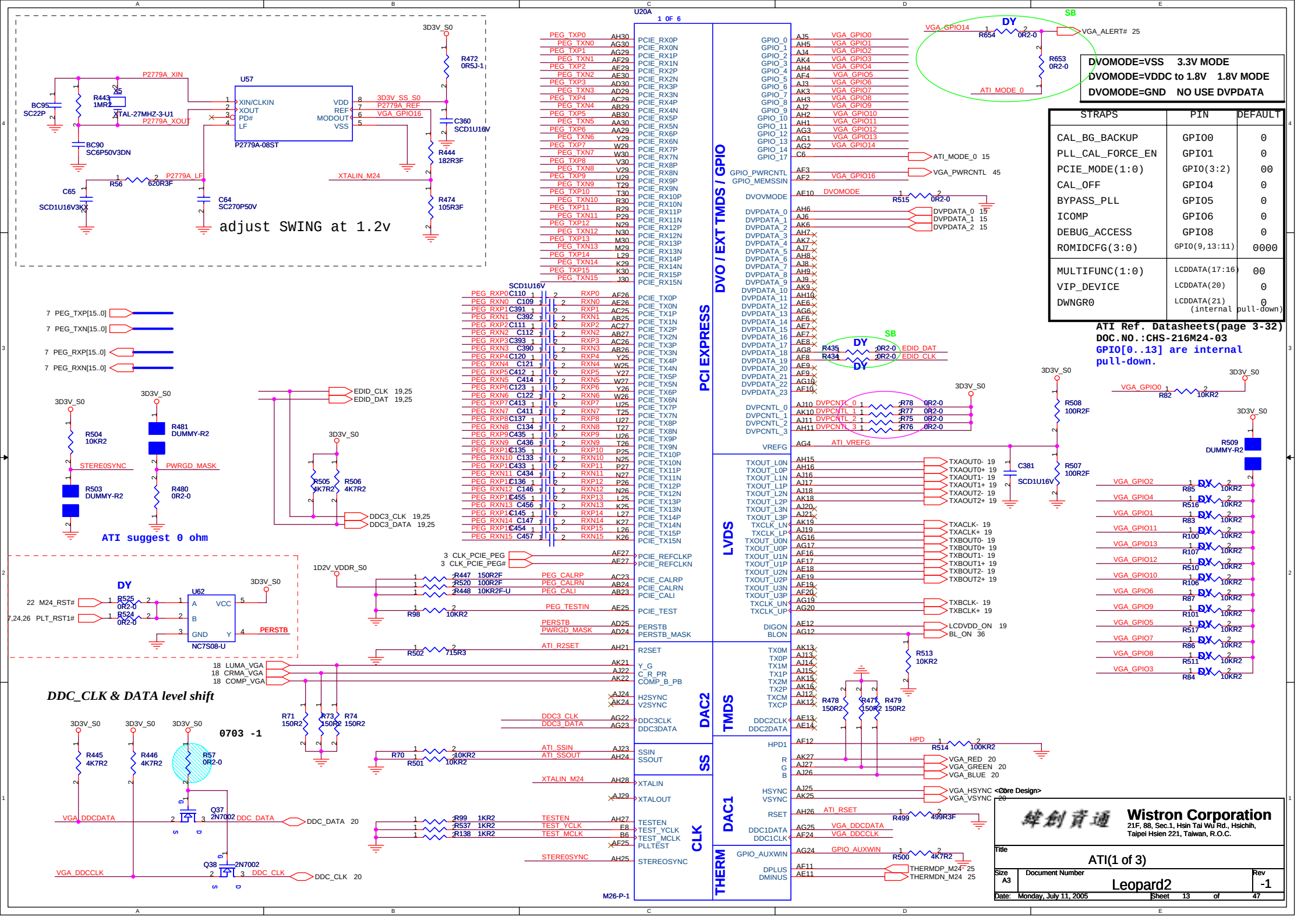
<Core Design>

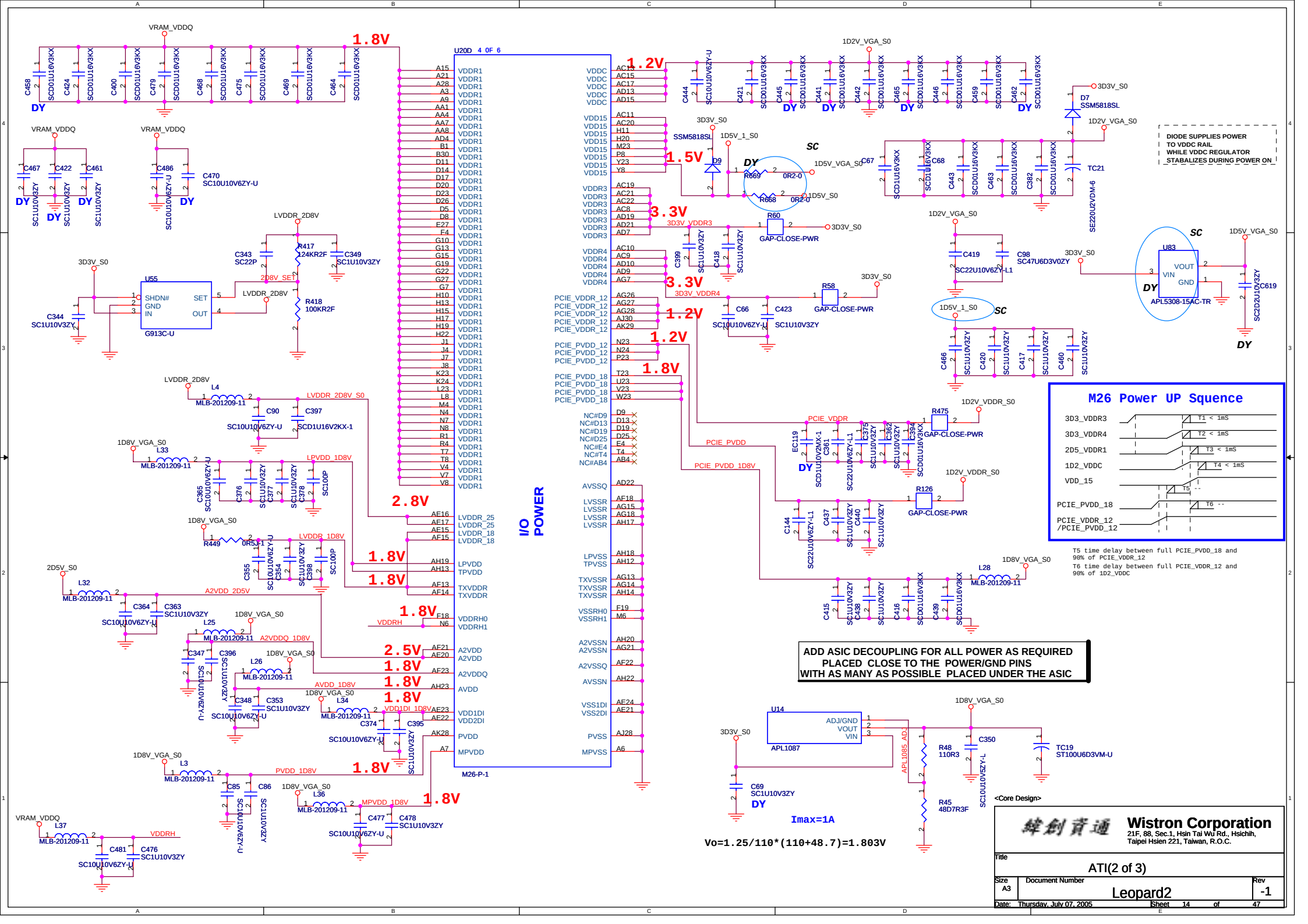
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

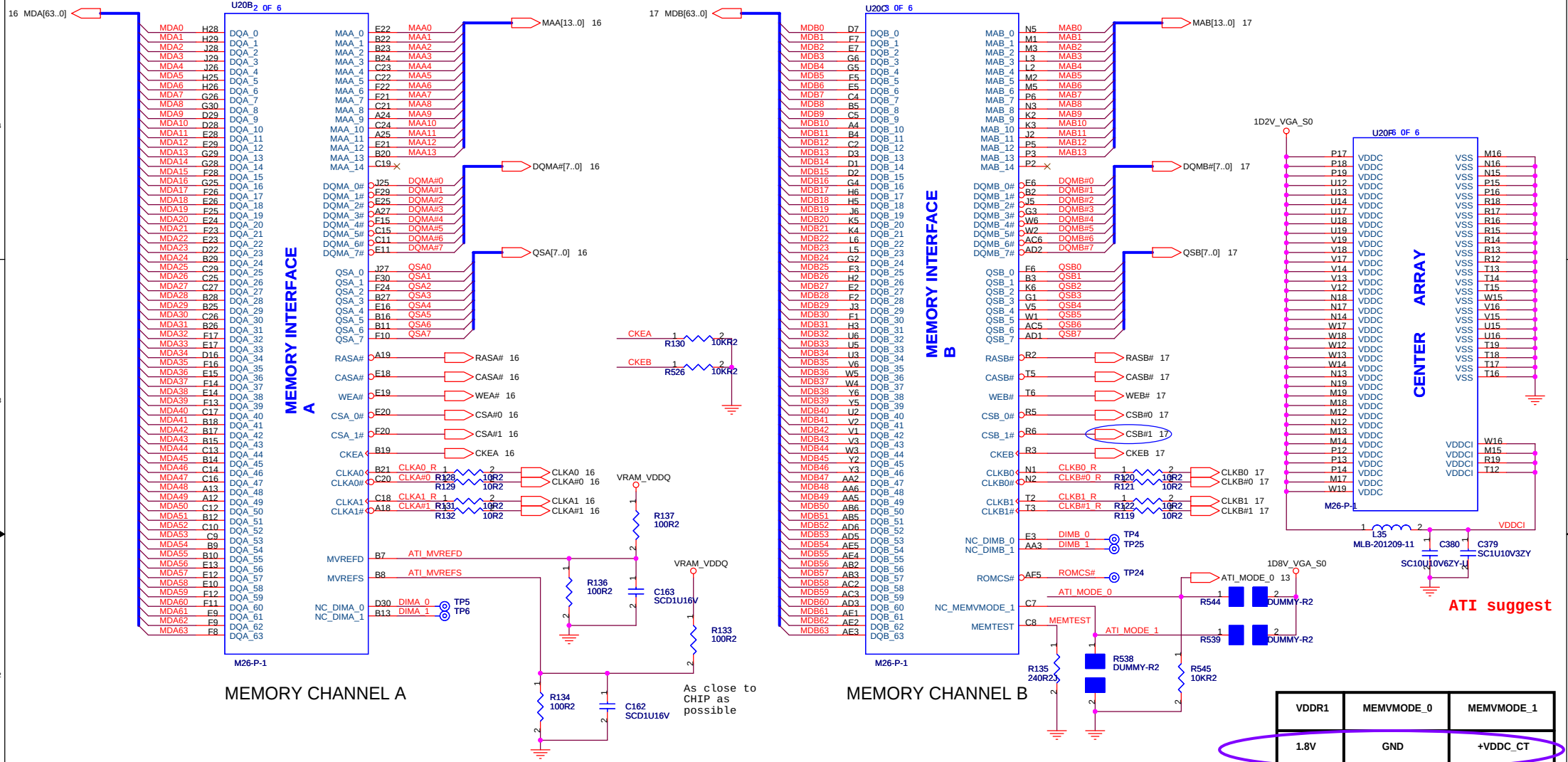
Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 12 of 47


U20A
1 OF 6
PCI EXPRESS
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_TEST
PERSTB
PERSTB_MASK
DVO / EXT TMDS / GPIO
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_17
GPIO_PWRCNTL
GPIO_MEMSSIN
DVOVMODE
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_3
VREFG
LVDS
TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
TXCLK_LN
TXCLK_LP
TXOUT_U0N
TXOUT_U0P
TXOUT_U1N
TXOUT_U1P
TXOUT_U2N
TXOUT_U2P
TXOUT_U3N
TXOUT_U3P
TXCLK_UN
TXCLK_UP
DIGON
BLON
DAC2
R2SET
Y_G
C_R_PR
COMP_B_PB
H2SYNC
V2SYNC
DDC3CLK
DDC3DATA
TMDS
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCM
TXCP
DDC2CLK
DDC2DATA
SS
SSIN
SSOUT
DAC1
HPD1
R
G
B
HSYNC
VSYNC
RSET
DDC1DATA
DDC1CLK
CLK
XTALIN
XTALOUT
TESTEN
TEST_YCLK
TEST_MCLK
PLLTEST
STEREOSYNC
THERM
GPIO_AUXWIN
DPLUS
DMINUS
M26-P-1
DVOMODE=VSS 3.3V MODE
DVOMODE=VDDC to 1.8V 1.8V MODE
DVOMODE=GND NO USE DVPDATA
STRAPS | PIN | DEFAULT
CAL_BG_BACKUP | GPIO0 | 0
PLL_CAL_FORCE_EN | GPIO1 | 0
PCIE_MODE(1:0) | GPIO(3:2) | 00
CAL_OFF | GPIO4 | 0
BYPASS_PLL | GPIO5 | 0
ICOMP | GPIO6 | 0
DEBUG_ACCESS | GPIO8 | 0
ROMIDCFG(3:0) | GPIO(9,13:11) | 0000
MULTIFUNC(1:0) | LCDDATA(17:16) | 00
VIP_DEVICE | LCDDATA(20) | 0
DWNGR0 | LCDDATA(21) (internal pull-down) | 0
ATI Ref. Datasheets(page 3-32)
DOC.NO.:CHS-216M24-03
GPIO[0..13] are internal pull-down.
adjust SWING at 1.2v
ATI suggest 0 ohm
DDC_CLK & DATA level shift
0703 -1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI(1 of 3)
Size A3
Document Number
Leopard2
Rev -1
Date: Monday, July 11, 2005
Sheet 13 of 47


U20D 4 0F 6
M26-P1
I/O POWER
1.8V
1.2V
1.5V
3.3V
2.8V
2.5V
1D2V_VGA_S0
1D5V_1_S0
3D3V_S0
1D8V_VGA_S0
2D5V_S0
LVDDR_2D8V
VRAM_VDDQ
DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON
M26 Power UP Squence
3D3_VDDR3
3D3_VDDR4
2D5_VDDR1
1D2_VDDC
VDD_15
PCIE_PVDD_18
PCIE_VDDR_12 /PCIE_PVDD_12
T1 < 1mS
T2 < 1mS
T3 < 1mS
T4 < 1mS
T5 --
T6 --
T5 time delay between full PCIE_PVDD_18 and 90% of PCIE_VDDR_12
T6 time delay between full PCIE_VDDR_12 and 90% of 1D2_VDDC
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
Imax=1A
Vo=1.25/110*(110+48.7)=1.803V
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI(2 of 3)
Size A3
Document Number
Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 14 of 47



VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

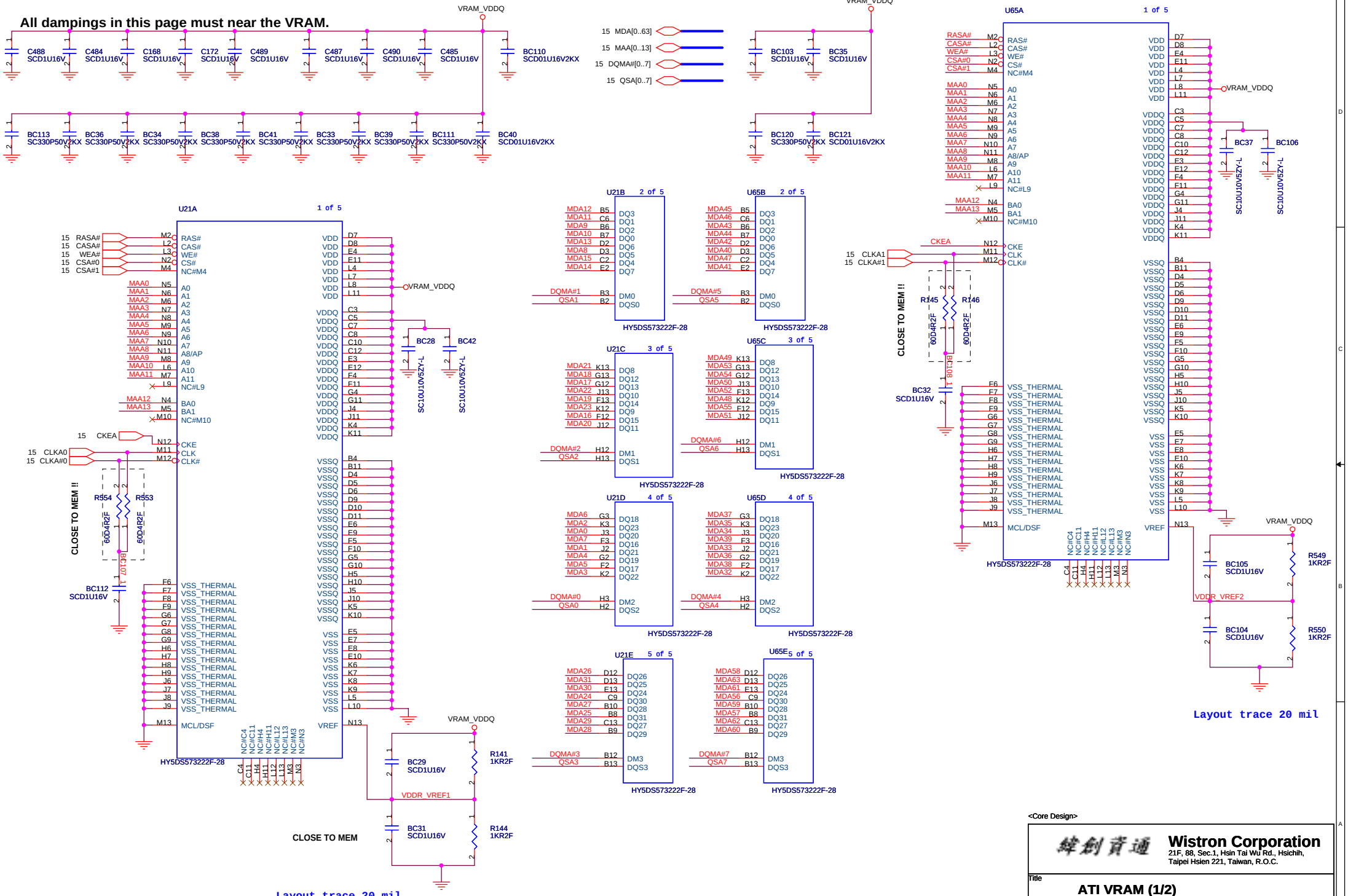
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI(3 of 3)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Thursday, July 07, 2005 | Sheet 15 of 47

All dampings in this page must near the VRAM.



<Core Design>

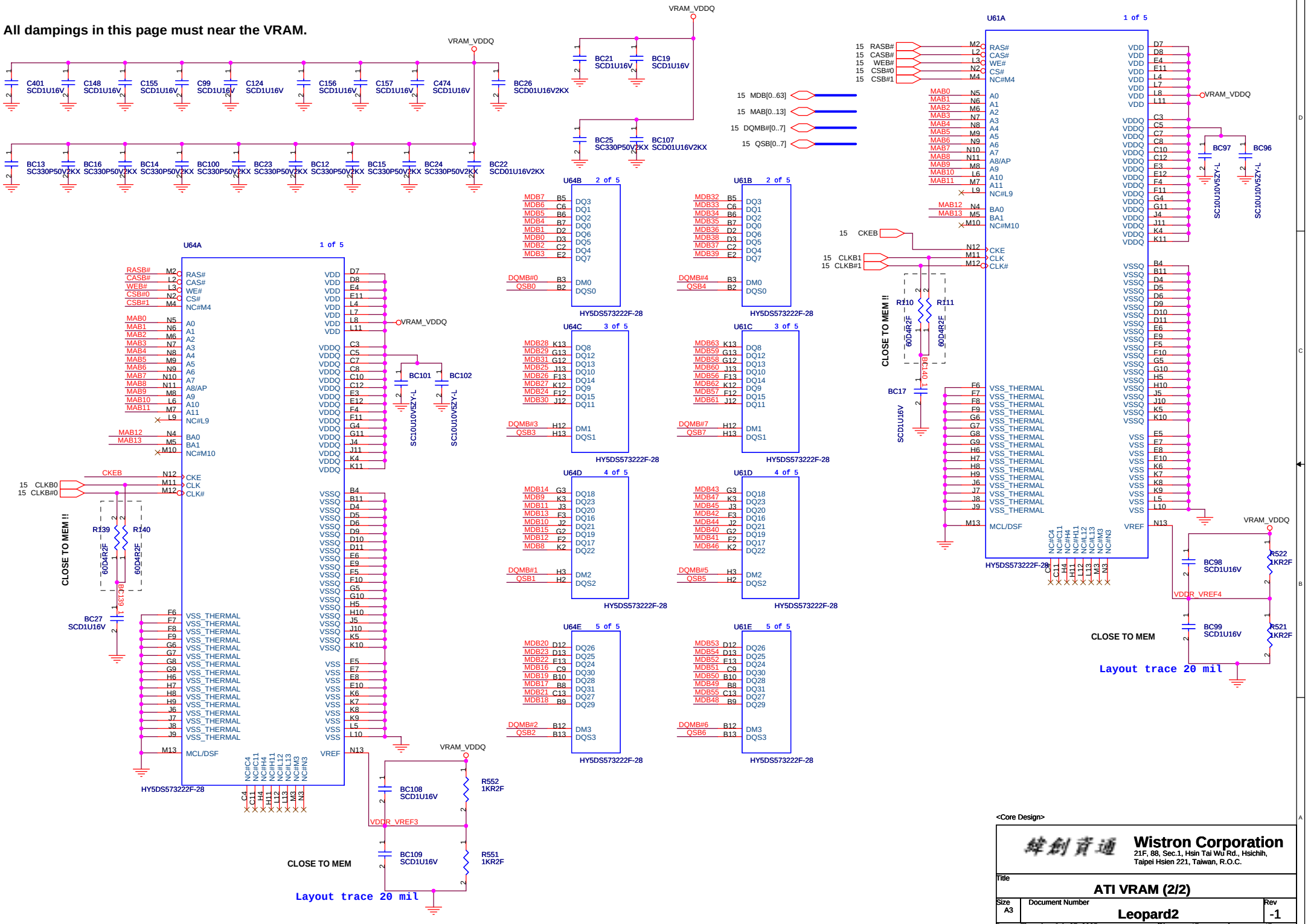
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI VRAM (1/2)

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 16 of 47

All dampings in this page must near the VRAM.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI VRAM (2/2)**

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 17 of 47

Digital Signal CONN

CN5 — JST-CON20

USB_P_CON0
USB_N_CON0
USB_P_CON1
USB_N_CON1
CRMA_CN5
LUMA_CN5
DDC_DATA_CON 20
DDC_CLK_CON 20
JVGA_HS 20
JVGA_VS 20
CRT_R 20
CRT_G 20
CRT_B 20
5V_S3
5V_S0

LUMA_CN5 — L8 BLM11B750S — LUMA
CRMA_CN5 — L12 BLM11B750S — CRMA
BC18 SC3P50V2CN
BC20 SC3P50V2CN
C138 SC3P50V2CN
C149 SC3P50V2CN
R122 150R2F
R123 150R2F
DY

VOL_UP_DK# — D5 BAV99LT1 — DY
VOL_DWN_DK# — D30 BAV99LT1 — DY

Close to Docking CN

LINE-OUT

Docking Connector

CN12 — FOX-CONN58D-U3

PR_PRESENT#
RJ45-4 31
RJ45-5 31
RJ45-1 31
RJ45-2 31
RJ45-7 31
RJ45-8 31
RJ45-3 31
RJ45-6 31
JACK_DETECT# 33
MIC_PR
AUD_AGND
33 DK_SPKR_R+
33 DK_SPKR_L+
36 VOL_UP_DK#
SPDIF
5V_Dock_S0
R51 0R2-0
5V_S0
MUTE_LED 19,36
1394_TPA1P_PR 31
1394_TPA1N_PR 31
1394_TPB1P_PR 31
1394_TPB1N_PR 31
USB_N_CON6
USB_P_CON6
TPAD30
TP21
IR_OUT
R455 0R2-0
COMP_PR
LUMA_PR
CRMA_PR
36 VOL_DWN_DK#
CIR_PR
5V_DOCK
DOCK_PRESENT
DCBATOUT
AD+
R94 1KR2
MH1
MH2

JACK_DETECT# — EC14 SCD1U16V
MUTE_LED — EC19 SCD1U16V
AUD_AGND — EC104 SCD1U16V
MIC_PR — EC106 SC1000P16V2KX
DK_SPKR_R+ — EC105 SC1000P16V2KX
DK_SPKR_L+ — EC110 SC1000P16V2KX
COMP_PR — EC109 SC1000P16V2KX
VOL_UP_DK# — EC111 SC1000P16V2KX
VOL_DWN_DK# — EC118 SC1000P16V2KX
DOCK_PRESENT — EC30 SC1000P16V2KX
PR_PRESENT# — EC103 SC1000P16V2KX
BT_LED — EC28 SC1000P16V2KX
BT_LED 19,31

Analog Signal CONN

CN6 — MOLEX-CON10-1

MIC_PR
EXT_MIC_1 32
EXT_MIC_2 32
HP_OUT_R 32
HP_OUT_L 32
EARPHONE 33
LID_SW 19
AUD_AGND
3D3V_S0
R548 47KR2 63.47334.1D1
EARPHONE

MIC-IN

22 USB_PN7 — USB_N_CON6
22 USB_PP7 — USB_P_CON6
22 USB_PN1 — USB_N_CON0
22 USB_PP1 — USB_P_CON0
USB_N_CON1 — USB_PN3 22
USB_P_CON1 — USB_PP3 22

3D3V_S3
D31 BAV99LT1
LID_SW

31 BC0EX1 — R624 DUMMY-R2 — ICH_PME# 22,30,34
31 BC0EX2 — R310 DUMMY-R2 — PCI_AD24 22,27,30,34

Please close to ICH6

HP suggest

5V_S0
R408 10KR2
PR_INSERT# — PR_INSERT# 36
DOCK_PRESENT — R103 47R2 — Q31 S2N3904-U3
R104 2K2R2
PR_PRESENT#

5V_S3 — C471 SCD1U16V
AD+ — C101 SCD1U25V3KX
5V_S0 — C617 SCD1U16V
DCBATOUT — C94 SCD1U25V3KX
5V_S0 — C425 SCD1U16V

32 SPDIF_OUT — SPDIF_OUT — L19 BLM18PG600SN1 — SPDIF
C315 SC470P25V2KN
C62 SC470P25V2KN
EC131 SCD1U16V — DY
AUD_AGND

INPUT	FUNCTION
LOW	B0
HIGH	B1

Place near the GMCH

5V_S0
U16 — NC7SB3157P6X-U
LUMA_PR — L30 IND-1D2UH — LUMA_PR_1
C357 SC47P50V2JN
C358 SC47P50V2JN
R456 150R2F
LUMA — PR_INSERT# — LUMA_VGA 13
U15 — NC7SB3157P6X-U
CRMA_PR — L29 IND-1D2UH — CRMA_PR_1
C356 SC47P50V2JN
C369 SC47P50V2JN
CRMA — PR_INSERT# — CRMA_VGA 13
COMP_PR — L27 IND-1D2UH
C351 SC47P50V2JN
C352 SC47P50V2JN
R491 150R2F
R436 150R2F
R72 0R2-0 — COMP_VGA 13

Place near the DOCK
<Core Design>

5V_S3 — F1 FUSE-2A6V — 5V_DOCK
100 mil
C368 SC4D7U10V5ZY
C367 SCD1U16V
TC6 ST47U6D3V-U1 — DY

20 CIR — R361 0R2-0
CIR_PR — R512 0R2-0
CIR_KBC 36

CIR,CIR_PR,CIR_KBC are connect togather. default setting 12/12

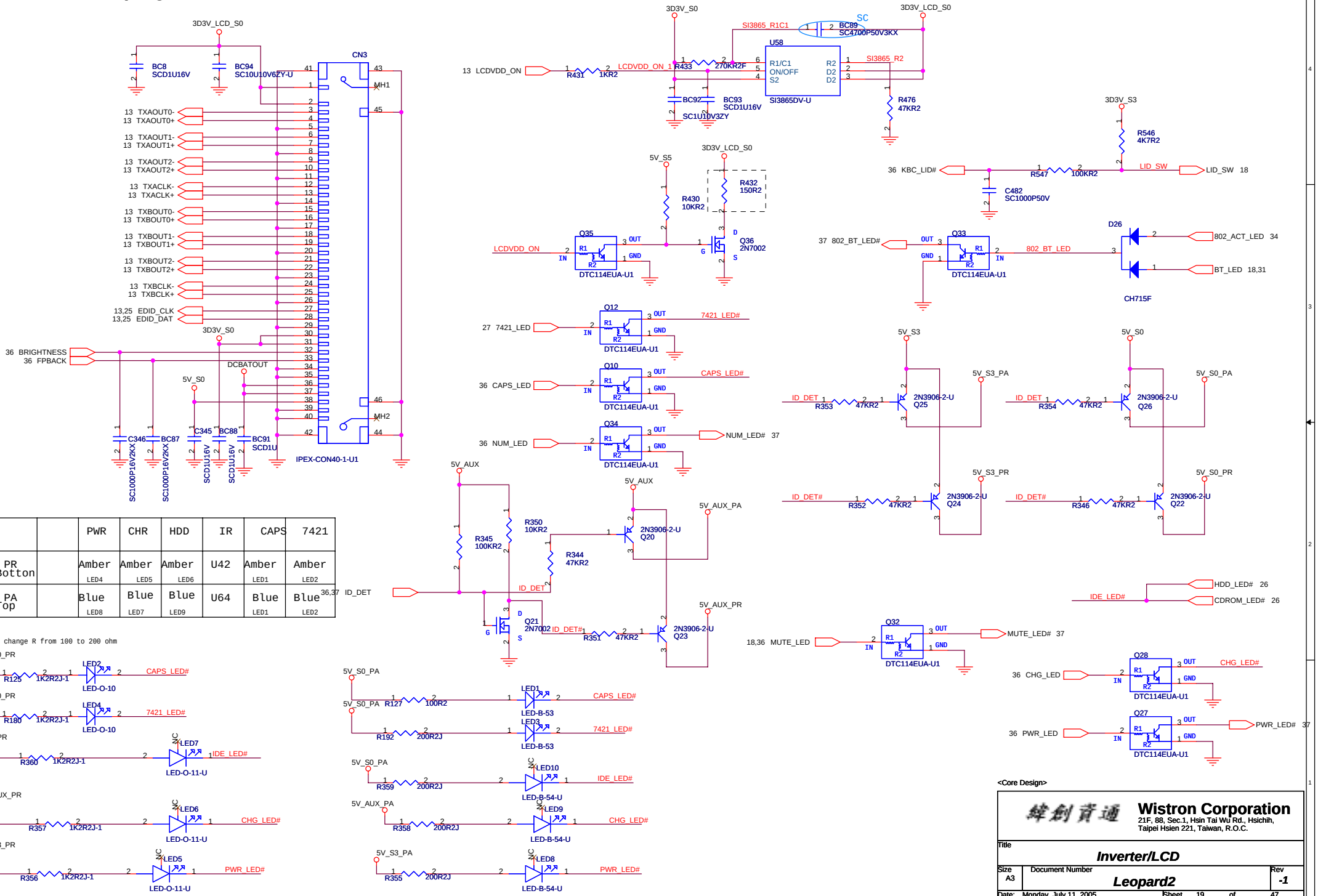
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Board to board conn/ Docking**

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 18 of 47

INVERTER/LCD



		PWR	CHR	HDD	IR	CAPS	7421
PR Botton		Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top		Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2

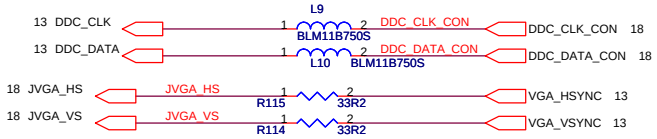
change R from 100 to 200 ohm

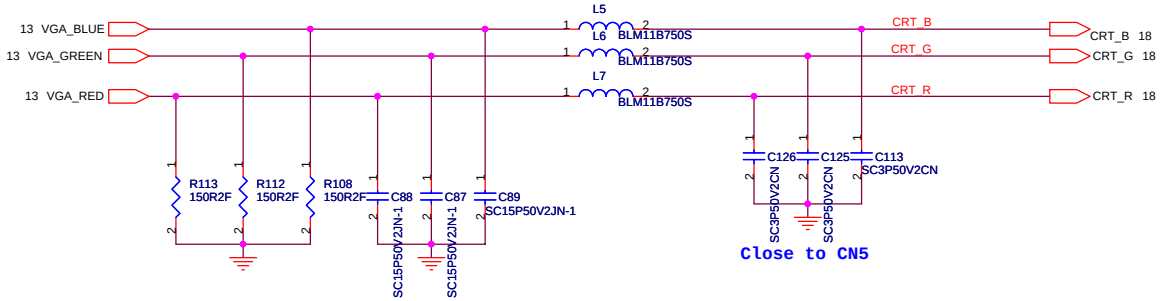
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Inverter/LCD*	
Size A3	Document Number *Leopard2*	Rev *-1*
Date: Monday, July 11, 2005	Sheet 19 of 47	

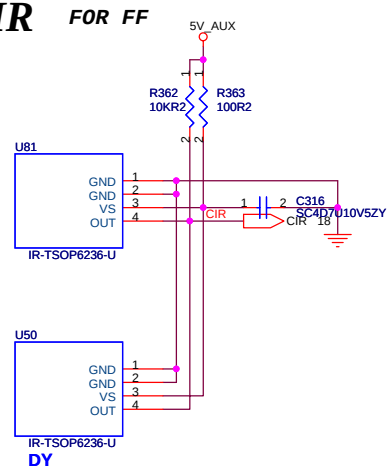
CRT





010804 Modified on Astro ID request

CIR *FOR FF*



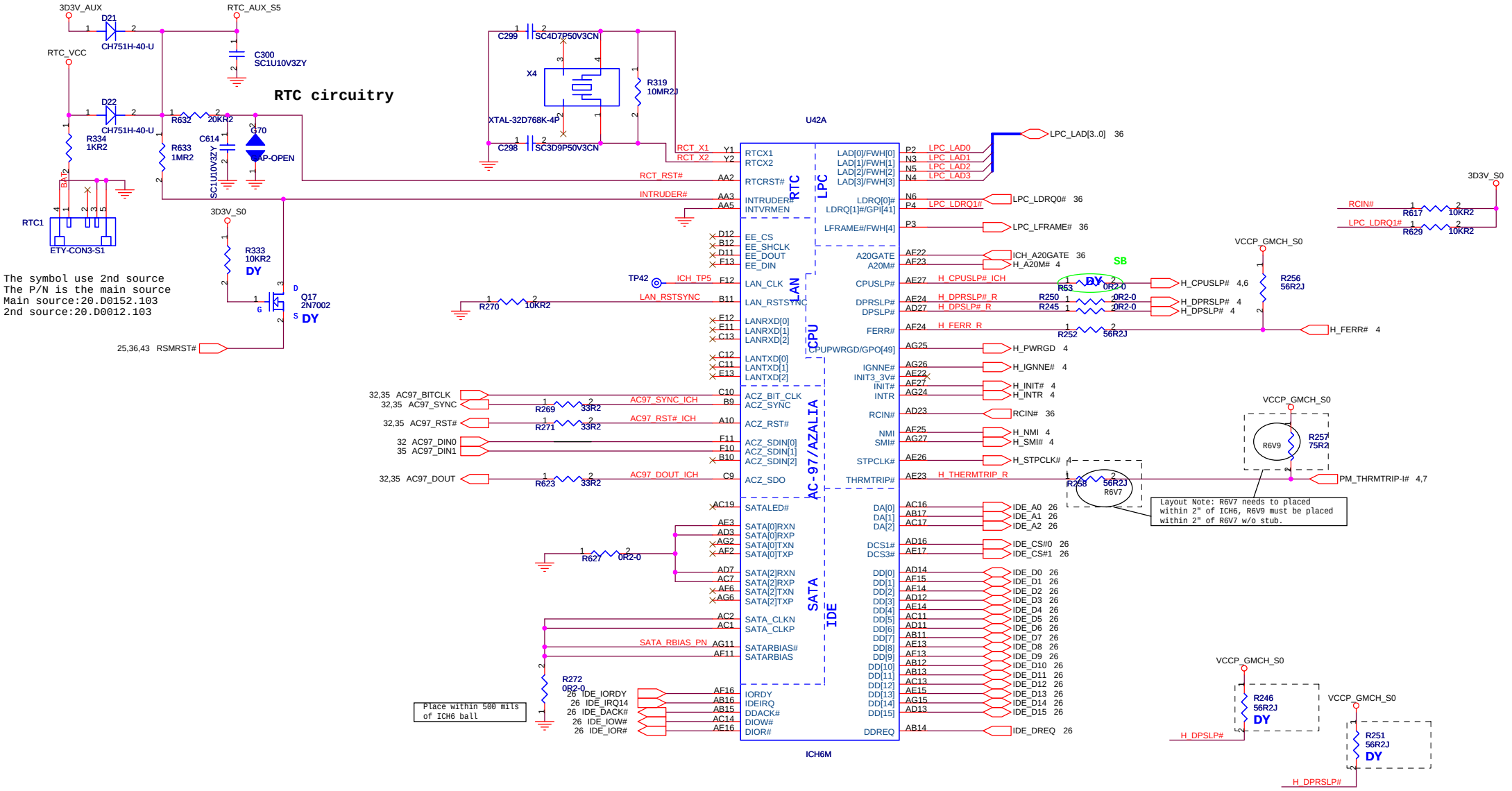
<Core Design>

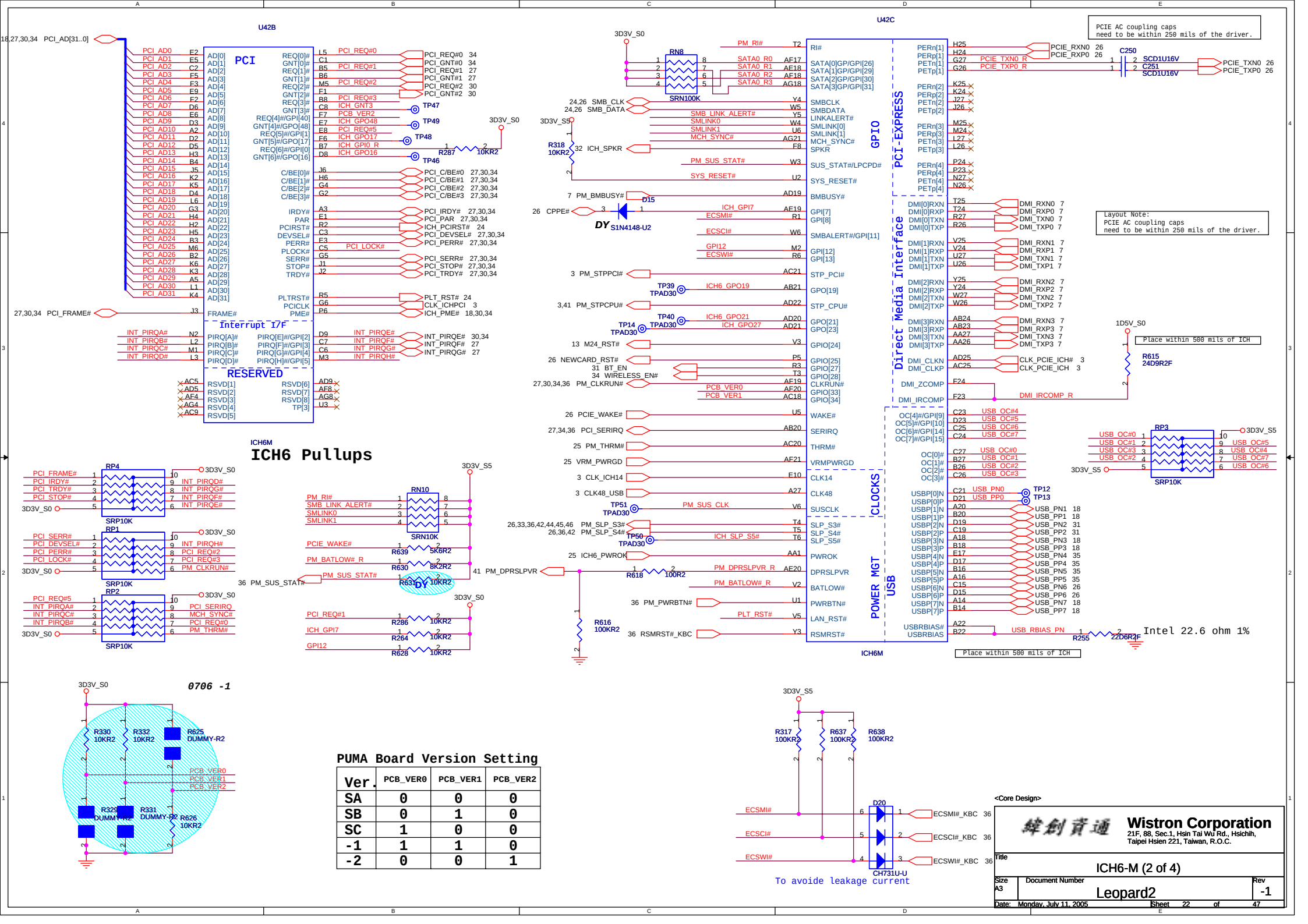
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

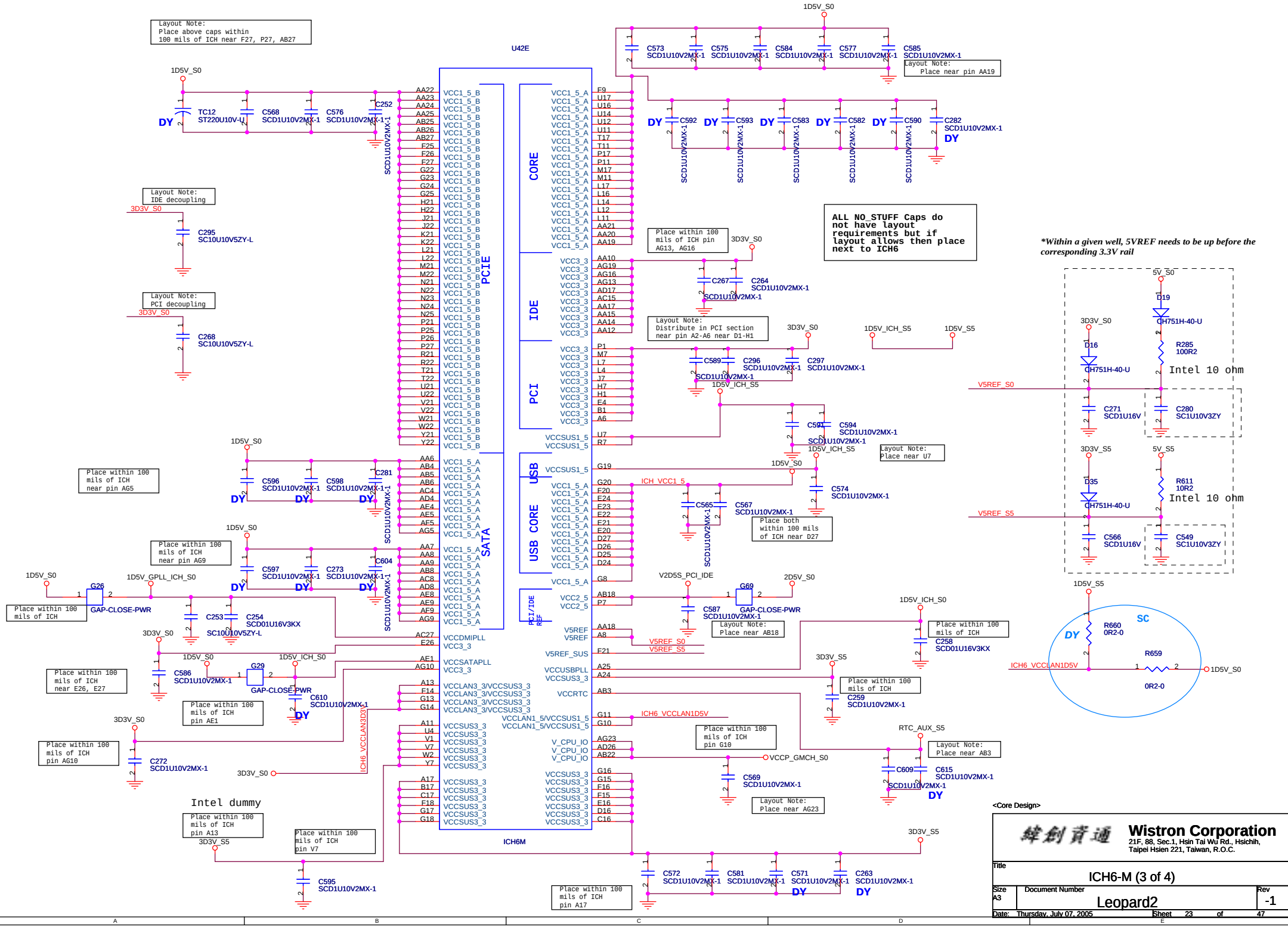
Title: CRT/ CIR

Size: A3 | Document Number: Leopard2 | Rev: -1

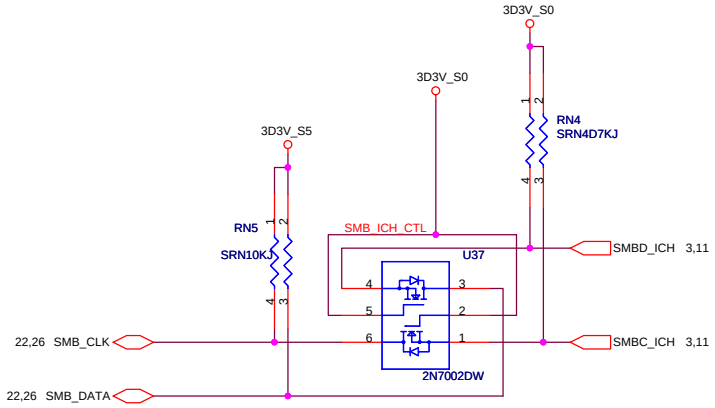
Date: Thursday, July 07, 2005 | Sheet 20 of 47

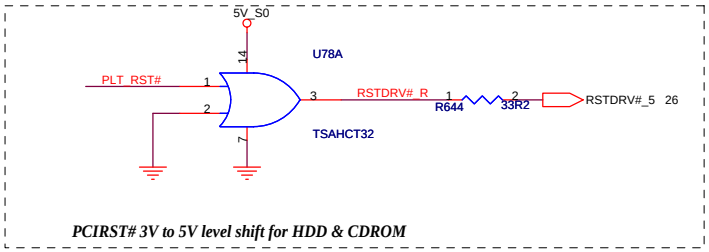

RTC circuitry
The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103
U42A
ICH6M
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
Place within 500 mils of ICH6 ball
Layout Note: R6V7 needs to placed within 2" of ICH6, R6V9 must be placed within 2" of R6V7 w/o stub.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (1 of 4)
Size A3
Document Number
Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 21 of 47


U42B
PCI
Interrupt I/F
RESERVED
U42C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
POWER MGT
USB
ICH6M
ICH6 Pullups
PCIE AC coupling caps need to be within 250 mils of the driver.
Layout Note: PCIE AC coupling caps need to be within 250 mils of the driver.
Place within 500 mils of ICH
Intel 22.6 ohm 1%
0706 -1
PUMA Board Version Setting
Ver. | PCB_VER0 | PCB_VER1 | PCB_VER2
SA | 0 | 0 | 0
SB | 0 | 1 | 0
SC | 1 | 0 | 0
-1 | 1 | 1 | 0
-2 | 0 | 0 | 1
To avoide leakage current
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: ICH6-M (2 of 4)
Size: A3
Document Number: Leopard2
Rev: -1
Date: Monday, July 11, 2005
Sheet 22 of 47

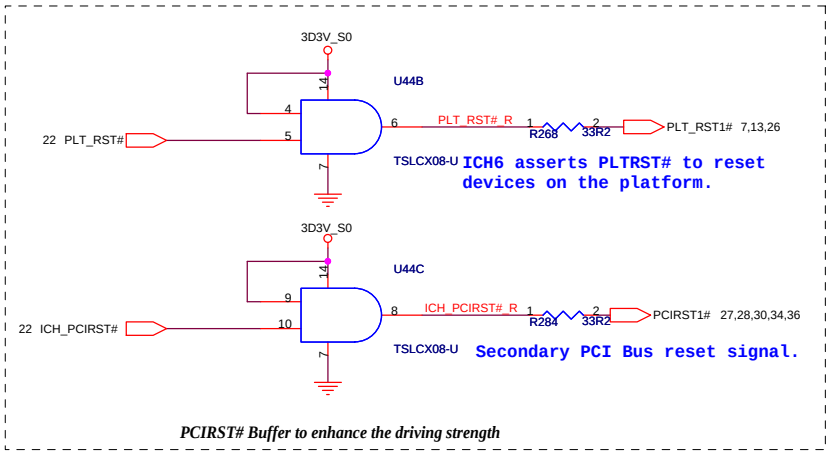

U42E
ICH6M
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
PCI/IDE REF
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin A17
Place within 100 mils of ICH pin AG13, AG16
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Layout Note: Place near pin AA19
Layout Note: Place near U7
Layout Note: Place near AB18
Layout Note: Place near AG23
Layout Note: Place near AB3
Place both within 100 mils of ICH near D27
Place within 100 mils of ICH pin G10
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Intel dummy
Intel 10 ohm
Intel 10 ohm
SC
1D5V_S0
3D3V_S0
5V_S0
1D5V_S5
3D3V_S5
5V_S5
1D5V_ICH_S5
1D5V_ICH_S0
2D5V_S0
RTC_AUX_S5
V5REF_S0
V5REF_S5
ICH_VCC1_5
ICH6_VCCLAN1D5V
VCCP_GMCH_S0
V2D5S_PCI_IDE
1D5V_GPLL_ICH_S0
ICH6_VCCLAN3D3V
GAP-CLOSE-PWR
DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (3 of 4)
Size A3
Document Number
Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 23 of 47

SMBUS(ICH6 ---> SODIMM,CLKGEN)

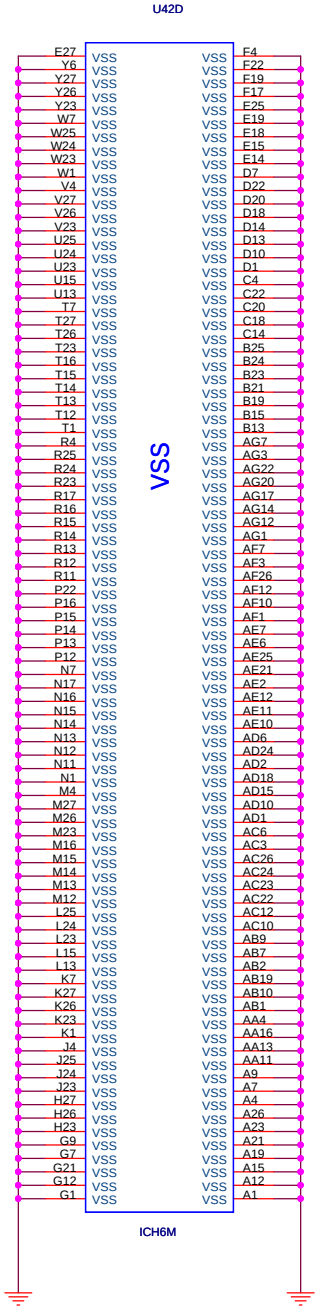




PCIRST# 3V to 5V level shift for HDD & CDROM



PCIRST# Buffer to enhance the driving strength



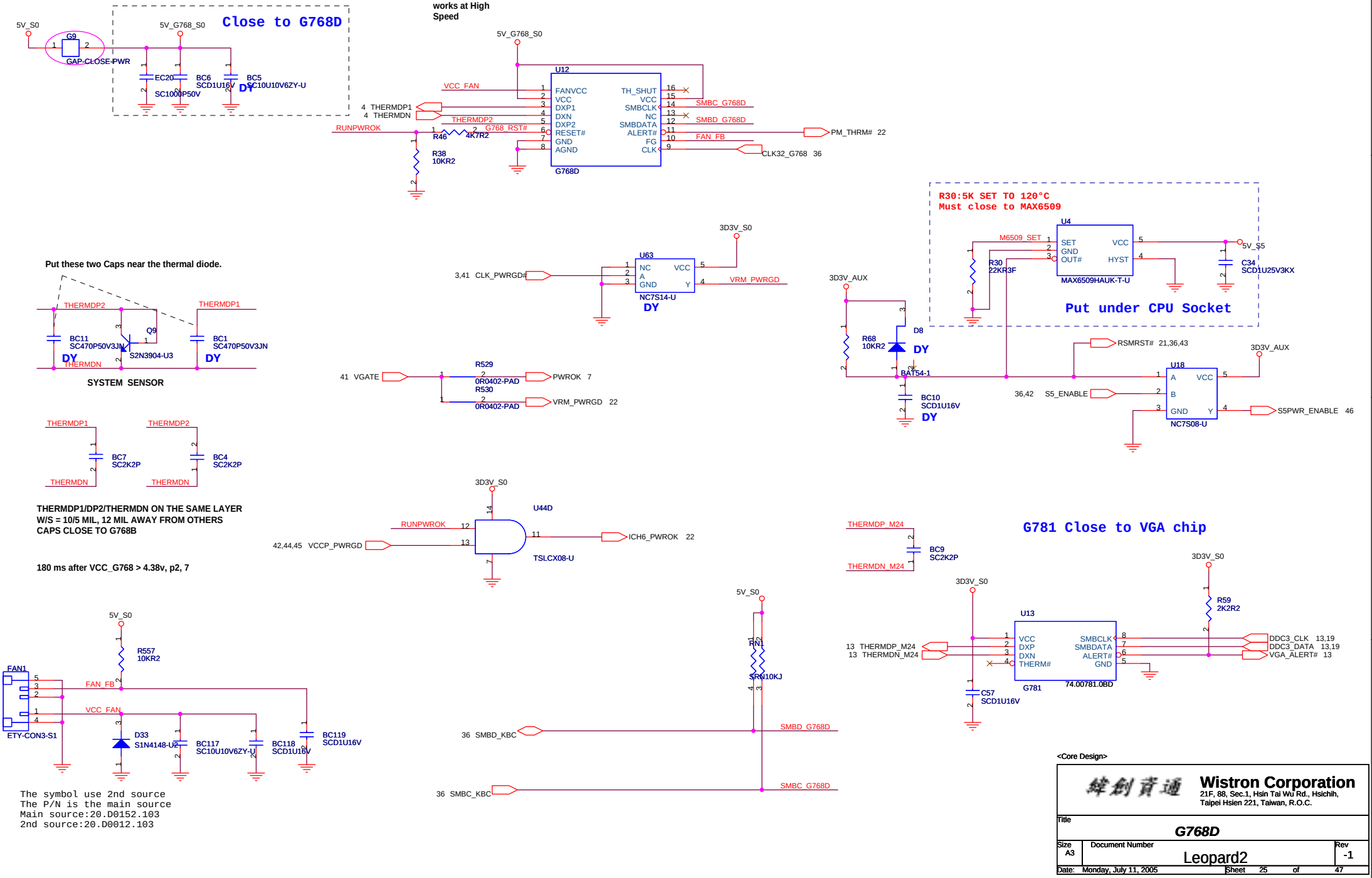
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH6-M (4 of 4)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Thursday, July 07, 2005 | Sheet 24 of 47



<Core Design>

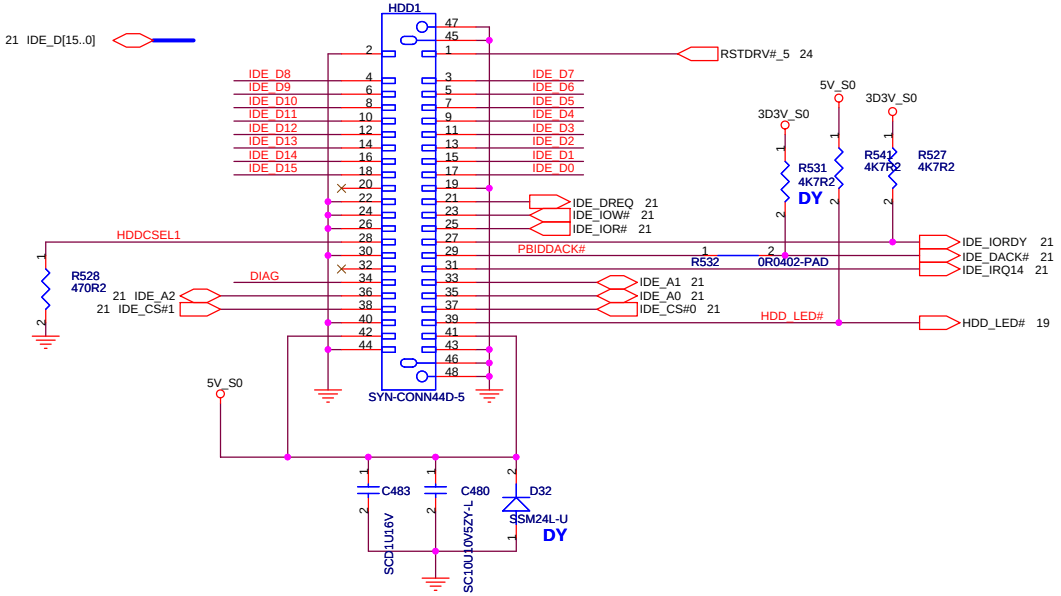
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G768D

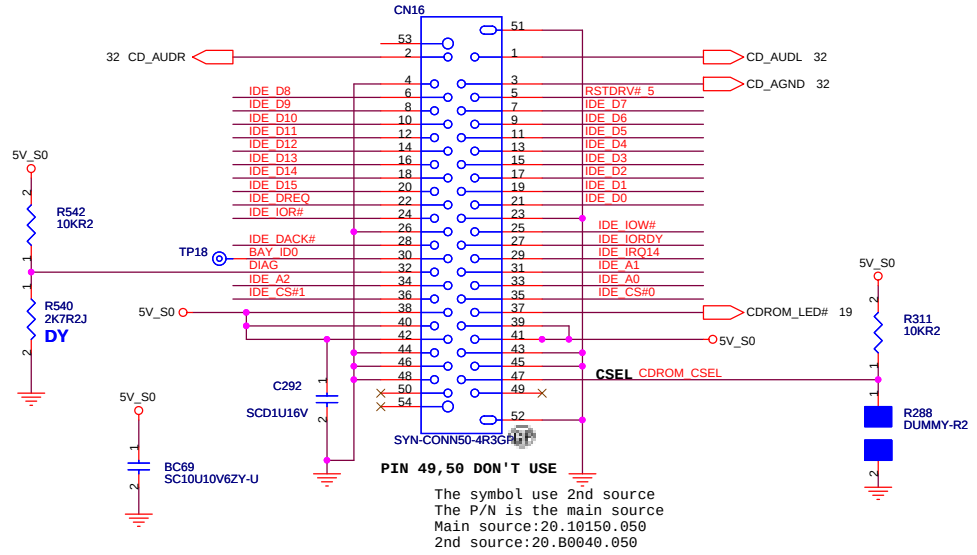
Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 25 of 47

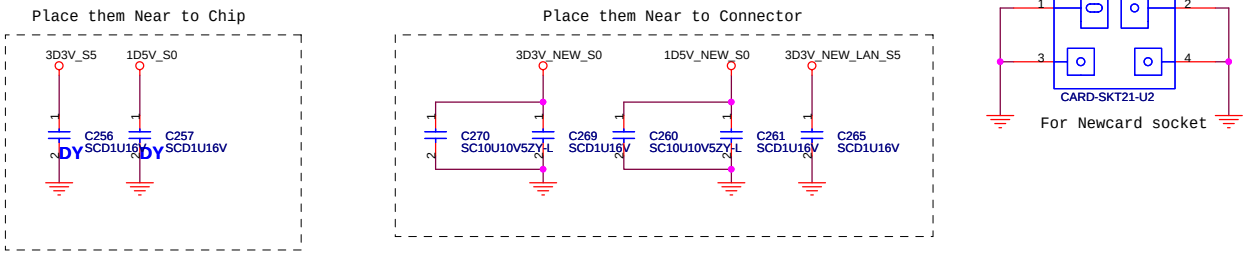
HDD Connector

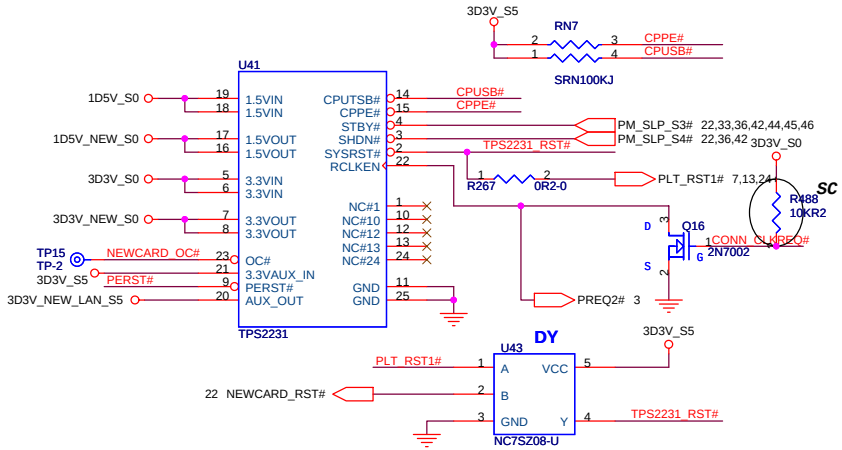


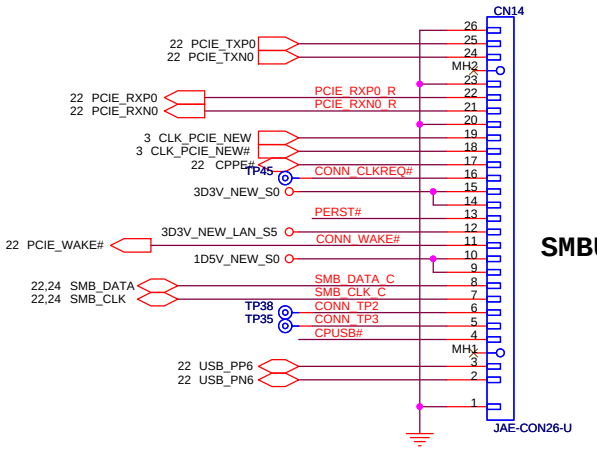
CDROM



NEWCARD Connector







SMBUS(ICH6--NEWCARD,LAN)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD / CDROM/NEWCARD***

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 26 of 47

INTA# CARBUS 1
INTB# NONE
INTC# 1394
INTD# CARD READER

1 of 4

U47A

PCI7411-1

CARD BUS

1394

SD/SDIO

UNUSED TERMINALS

Bypass/Decupoling Capacitors
Should be places as close to
PCI7421 as possible

* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible

SD
MS/MS_pro

MS/MS_pro
XD
SM

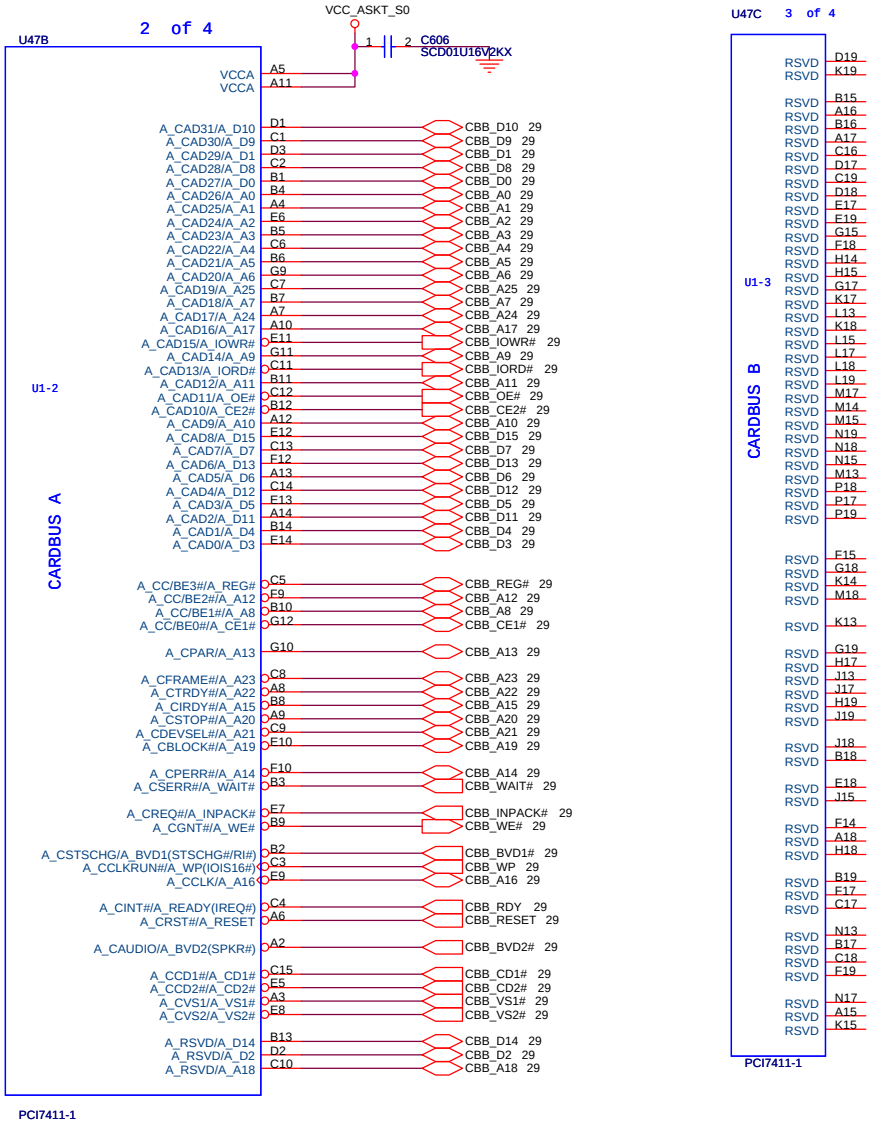
<Core Design>

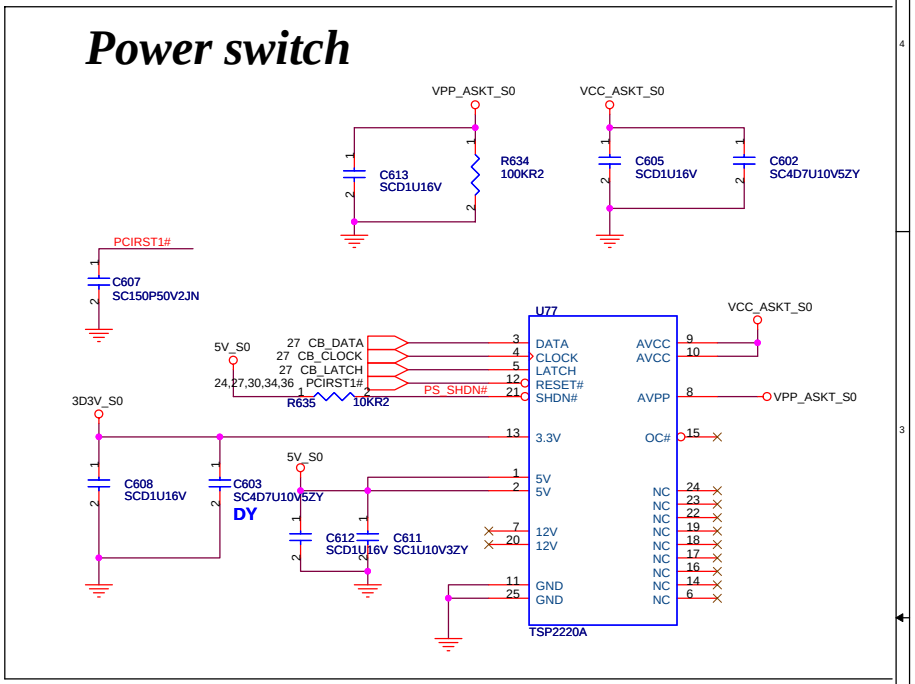
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

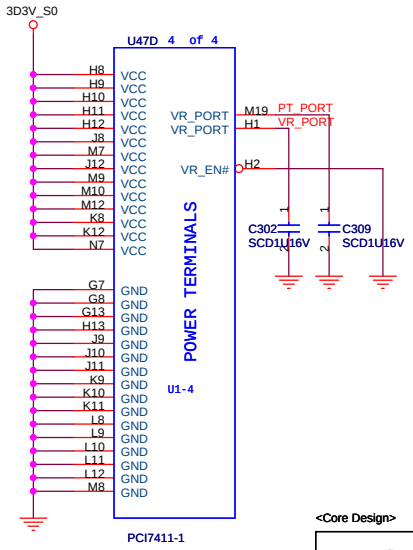
Title: TI SNC1Q21 (1 of 2)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Monday, July 11, 2005 | Sheet 27 of 47







<Core Design>

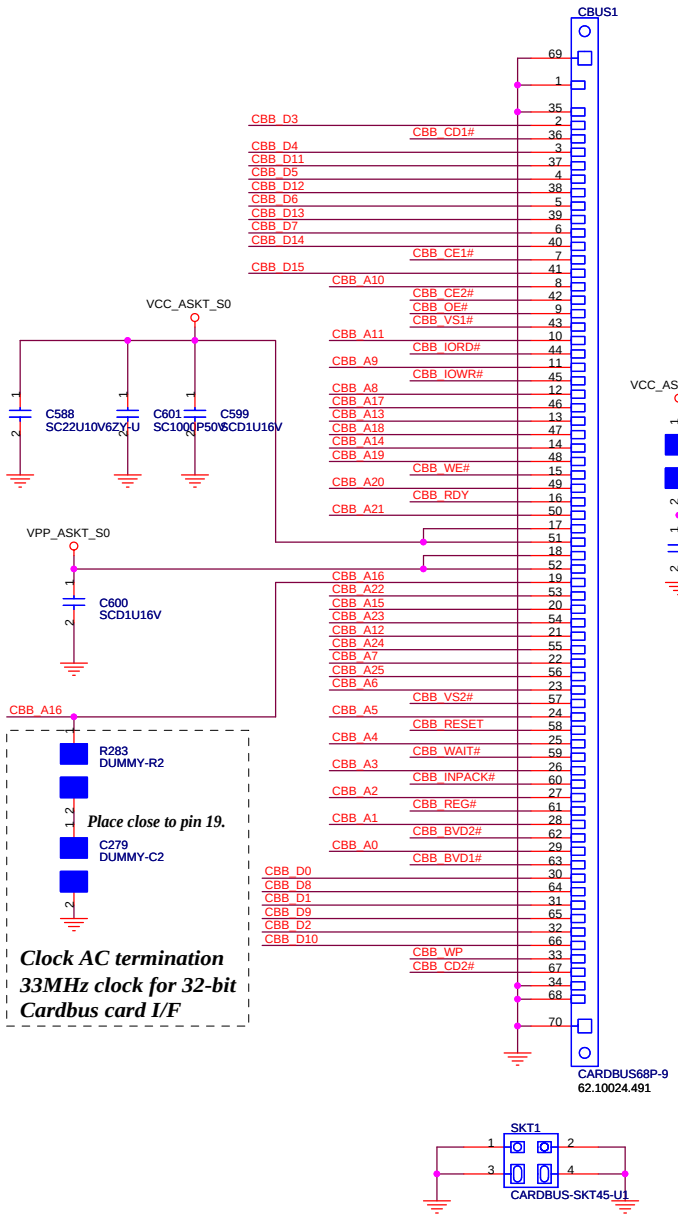
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI PCI7411 GHK (2 of 2)

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Monday, July 11, 2005 | Sheet 28 of 47

PCMCIA Socket



Cardbus I/F

CBB_D[0..15] 28
CBB_A[0..25] 28
CBB_IORD# 28
CBB_IOWR# 28
CBB_OE# 28
CBB_WE# 28
CBB_REG# 28
CBB_RDY 28
CBB_WP 28
CBB_RESET 28
CBB_WAIT# 28
CBB_INPACK# 28
CBB_CE1# 28
CBB_CE2# 28
CBB_BVD1# 28
CBB_BVD2# 28
CBB_CD1# 28
CBB_CD2# 28
CBB_VS1# 28
CBB_VS2# 28

VCC_ASKT_S0
R301 DUMMY-R2
47K
CBB_RESET
C290 SCD01U16V3KX

3D3V_CR_S0
R577 2K2R2 — SM_RE#
R216 2K2R2 — MS_BS
R558 2K2R2 DY — SM_ALE
R560 2K2R2 DY — SM_CLE
R579 2K2R2 — SM_R/B#
R578 4K7R2 — SD_WP

SKT1
CARDBUS-SKT45-U1

6 in 1 Connector

3D3V_CR_S0
C509 SCD01U16V2KX
C537 SCD01U16V2KX
C517 SCD01U16V2KX
C531 SCD01U16V2KX

SKT2
SKT-MEMO-9-U1
XD-VCC
S.M-VCC
MS-VCC
SD-VCC
SD-DAT0
SD-DAT1
SD-DAT2
SD-DAT3
MS-DATA0
MS-DATA1
MS-DATA2
MS-DATA3
S.M/XD-D1
S.M/XD-D2
S.M/XD-D3
S.M/XD-D4
S.M/XD-D5
S.M/XD-D6
S.M/XD-D7
S.M-LVD
S.M-CD#
S.M-D0
SM-CD-COM
SM-CD-SW
SM-WP-SW
MS-BS
MS-INS
MS-SCLK
RSV#4
XD-CD
SD-CD-COM
SD-CD-SW
SD-WP-SW
SD-CLK
SD-CMD
S.M#/XD-CLE
S.M#/XD-ALE
S.M#/XD-WE
S.M#/XD-CE
S.M#/XD-RE
S.M#/XD-R/B
S.M/XD-WP-IN
GND

MS_SDIO
MS_D1
MS_D2
MS_D3
SM_D4
SM_D5
SM_D6
SM_D7
SM_CD#
MS_CLK
MS_CLK_R
MS_BS
SD_CD#
SD_WP
SM_CLE
SM_ALE
SM_RE#
SM_R/B#
MS_CLK_R0
MS_BS_1
MC_PWR_CTRL

R214 33R2
R212 33R2
R213 33R2
R193 33R2
R604 33R2
R599 33R2
R588 330R2
R215 22R2
R559 0R2-0 DY

U34
AAT46101GV-1
OUT
GND
SET
IN
ON#
R228 4K7R2
C230 SCD1U16V
R239 15KR2
C239 SC1U10V3ZY

3D3V_S0
U75
NC7SZ66P5X DY
A
B
GND
VCC
SE
MS_CLK
MS_CLK_R
SD_CD#

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA SLOT/ CARDBUS SKT
Size: A3
Document Number: Leopard2
Rev: -1
Date: Thursday, July 07, 2005
Sheet 29 of 47

Close to RTL8100C Pin121,Pin122

LAN_X1
LAN_X2
R166 DUMMY-R2
X6 XTAL-25MHZ-43
C186 SC12P50V2JN
C185 SC12P50V2JN

Close to LAN chip

TX+ TX- RX- RX+
R156 49D9R2F
R155 49D9R2F
R153 49D9R2F
R154 49D9R2F
C171 SCD1U16V
C169 SCD1U16V

3D3V_LAN_S5
R174 3K6R3
U27 M93C46-W-3
EECS_3 EESK EEDI EEDO
C225 SCD1U16V

PCI_C/BE#[0..3] 22,27,34
PCI_AD[0..31] 18,22,27,34

AVDD25 VDD25
R152 0R3-U
C176 SCD1U16V

R157 5K6R3F
TP7 TP8 TP9

U24 RTL8100CL-U

1	TX+	31 TX+	
2	TX-	31 TX-	
3	AVDD33	AVDD33	
4	GND		
5	RX+	31 RX+	
6	RX-	31 RX-	
7	AVDD33	AVDD33	
8	CTRL25	CTRL25	
9	NC		
10	NC		
11	NC		
12	AVDD25	AVDD25	
13	NC		
14	NC		
15	NC		
16	NC		
17	GND		
18	NC		
19	NC		
20	AVDD33	AVDD33	
21	GND		
22	NC		
23	ISOLATEB	ISOLATE	
24	NC		
25	INTAB	22,34 INT_PIRQE#	
26	VDD33	3D3V_LAN_S5	
27	PCIRSTB	24,27,28,34,36 PCIRST1#	
28	PCICLK	3 PCLK_LAN	
29	GNTB	22 PCI_GNT#2	
30	REQB	22 PCI_REQ#2	
31	PMEB	18,22,34 ICH_PME#	
32	VDD25	VDD25	
33	PCIAD31	PCI_AD31	
34	PCIAD30	PCI_AD30	
35	GND		
36	PCIAD29	PCI_AD29	
37	PCIAD28	PCI_AD28	
38	GND		
39	PCIAD27	PCI_AD27	
40	PCIAD26	PCI_AD26	
41	PCIAD25	PCI_AD25	
42	PCIAD24	PCI_AD24	
43	CBEB3	PCI_C/BE#3	
44	IDSEL	LAN_IDSEL	
45	NC		
46	PCIAD23	PCI_AD23	
47	NC		
48	PCIAD22	PCI_AD22	
49	PCIAD21	PCI_AD21	
50	GND		
51	PCIAD20	PCI_AD20	
52	VDD25	VDD25	
53	PCIAD19	PCI_AD19	
54	VDD33		
55	PCIAD18	PCI_AD18	
56	PCIAD17	PCI_AD17	
57	PCIAD16	PCI_AD16	
58	CBEB2	PCI_C/BE#2	
59	FRAMEB	PCI_FRAME# 22,27,34	
60	NC		
61	IRDYB	PCI_IRDY# 22,27,34	
62	NC		
63			
64			
65	CLKRUNB	PM_CLKRUN# 22,27,34,36	
66	GND		
67	TRDYB	PCI_TRDY# 22,27,34	
68	DEVSELB	PCI_DEVSEL# 22,27,34	
69	STOPB	PCI_STOP# 22,27,34	
70	PERRB	PCI_PERR# 22,27,34	
71	VDD33		
72	NC		
73	NC		
74	NC		
75	SERRB	PCI_SERR# 22,27,34	
76	PAR	PCI_PAR 22,27,34	
77	CBEB1	PCI_C/BE#1	
78	VDD25	VDD25	
79	PCIAD15	PCI_AD15	
80	GND		
81	GND		
82	PCIAD14	PCI_AD14	
83	PCIAD13	PCI_AD13	
84	VDD33		
85	PCIAD12	PCI_AD12	
86	PCIAD11	PCI_AD11	
87	PCIAD10	PCI_AD10	
88	NC		
89	PCIAD9	PCI_AD9	
90	PCIAD8	PCI_AD8	
91	GND		
92	CBEB0	PCI_C/BE#0	
93	PCIAD7	PCI_AD7	
94	VDD33		
95	PCIAD6	PCI_AD6	
96	PCIAD5	PCI_AD5	
97	PCIAD4	PCI_AD4	
98	PCIAD3	PCI_AD3	
99	VDD25	VDD25	
100	GND		
101	PCIAD2	PCI_AD2	
102	GND		
103	PCIAD1		
104	PCIAD0		
105	LANWAKE		
106	EECS		
107	VDD33		
108	EEDO		
109	EEDI		
110	EESK		
111	LED2		
112	LED1		
113	LED0		
114	NC		
115	NC		
116	NC		
117	GND		
118	NC		
119	NC		
120	NC		
121	XTAL1		
122	XTAL2		
123	GND		
124	GND		
125			
126			
127	RSET		
128	GND		

LAN_X2 LAN_X1 LAN_LED0 LAN_LED1 LAN_LED2 EESK EEDI EEDO EECS_3 PCI_AD0 PCI_AD1

3D3V_LAN_S5
R151 0R2-0 CTRL25
LAN_PWR_CTRL
CHP69 Q11
G19 GAP-CLOSE-PWR
C167 SC22U10V6ZY-U
C189 C213 C215 C184 C216 C198 C174 SCD1U16V
C173 C188 C214 C217 SCD1U16V

L14 BLM11A601S
C178 C170 C177 C175 SCD1U16V
DY

3D3V_S0
R150 1KR2
R149 15KR2
ISOLATE

R165 100R2
PCI_AD23

3D3V_S5 3D3V_LAN_S5
G23 GAP-CLOSE-PWR

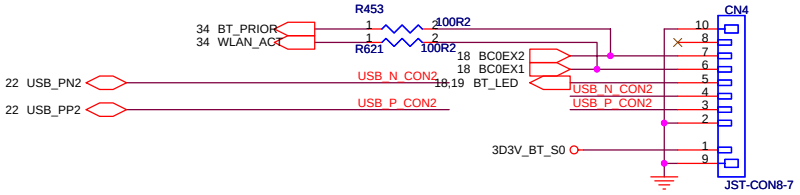
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8100C
Size: A3
Document Number: Leopard2
Rev: -1
Date: Thursday, July 07, 2005
Sheet 30 of 47

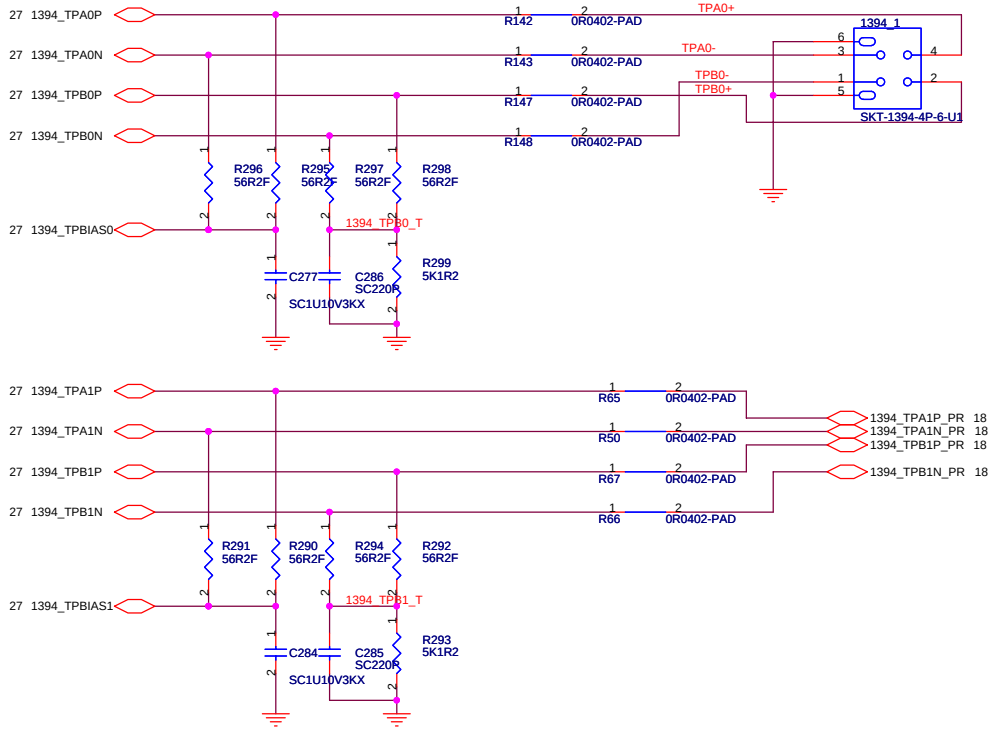
Blue thumb

Place on bottom side
From NEW!
1004-1



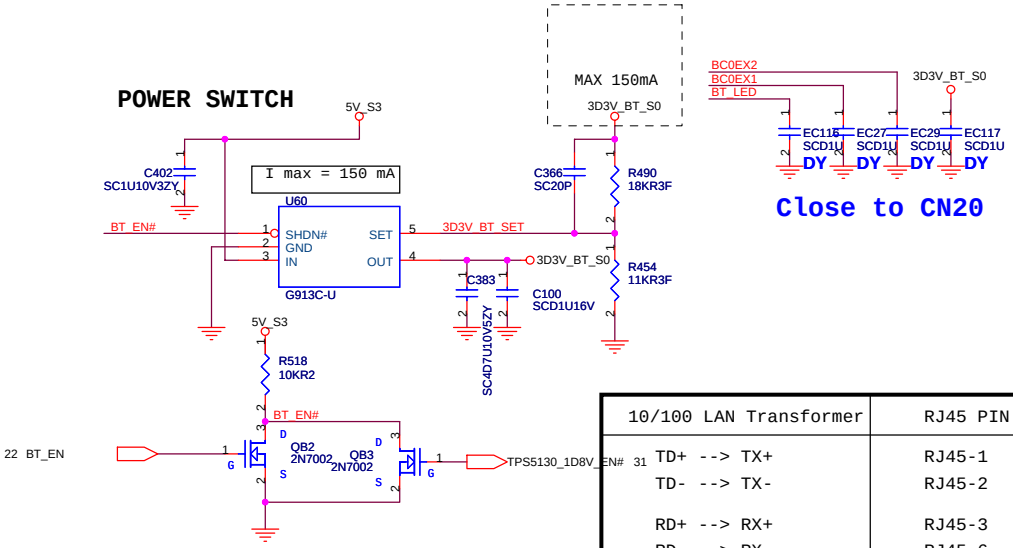
BC0EX2 connect to PCI_AD22 on main board.
BC0EX1 connect to ICH_PME# on main board.

1394 Connector



These components near to chip side.

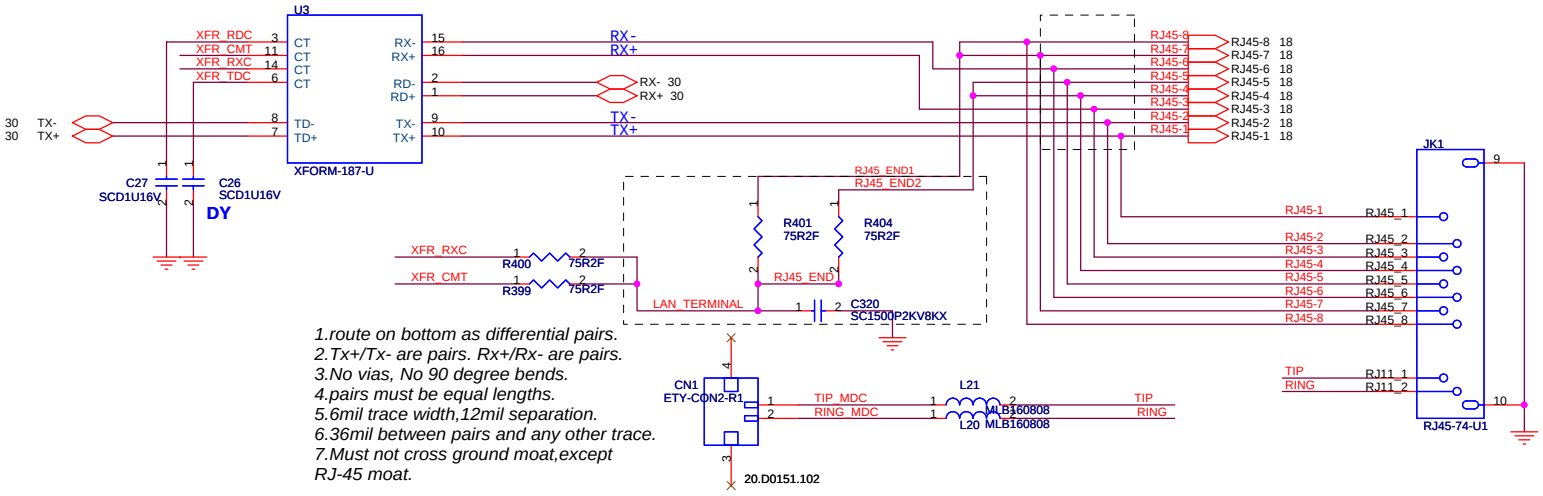
POWER SWITCH



Close to CN20

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

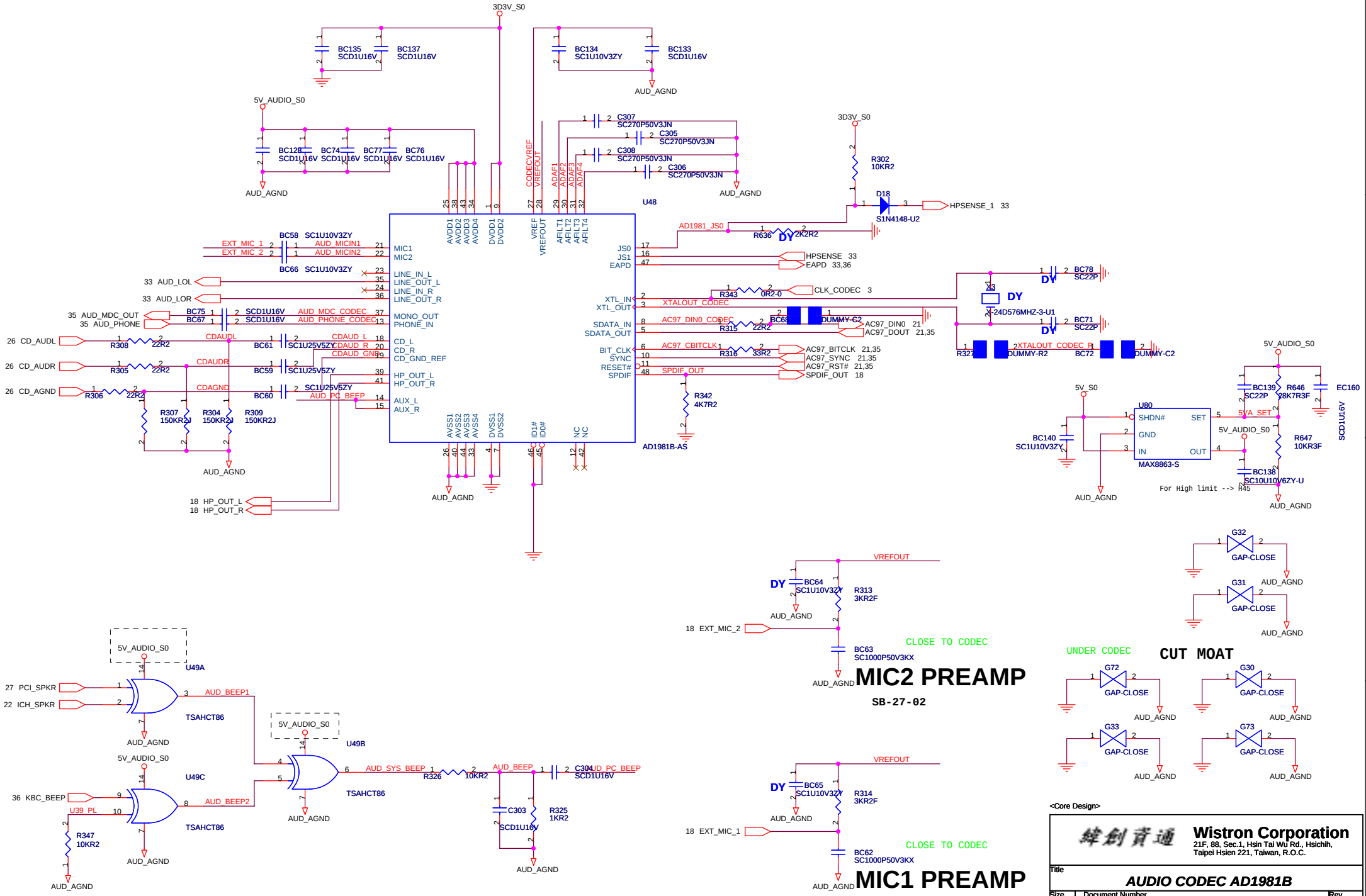
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN / 1394 Connector***

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 31 of 47

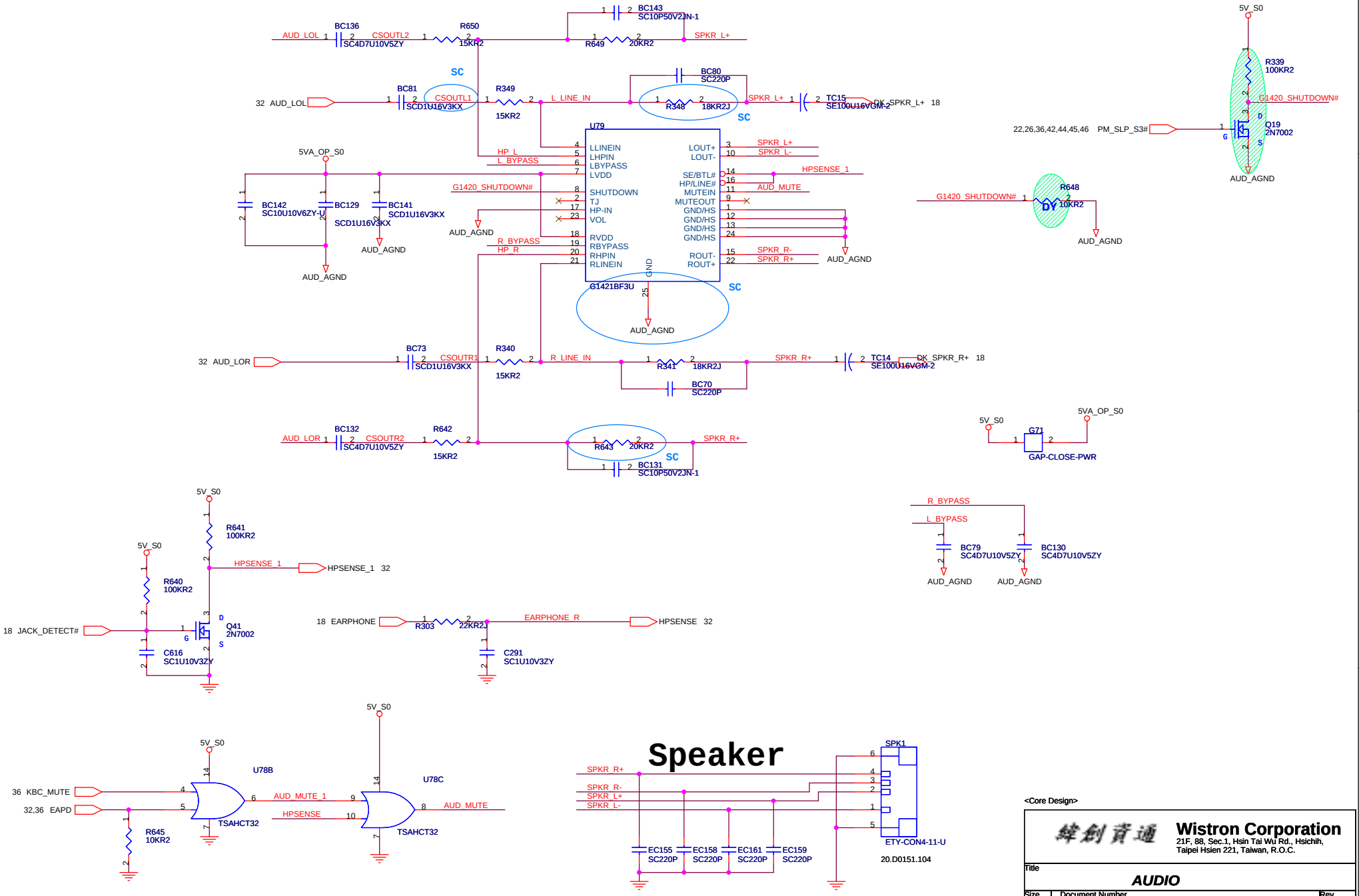


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC AD1981B

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 32 of 47



<Core Design>

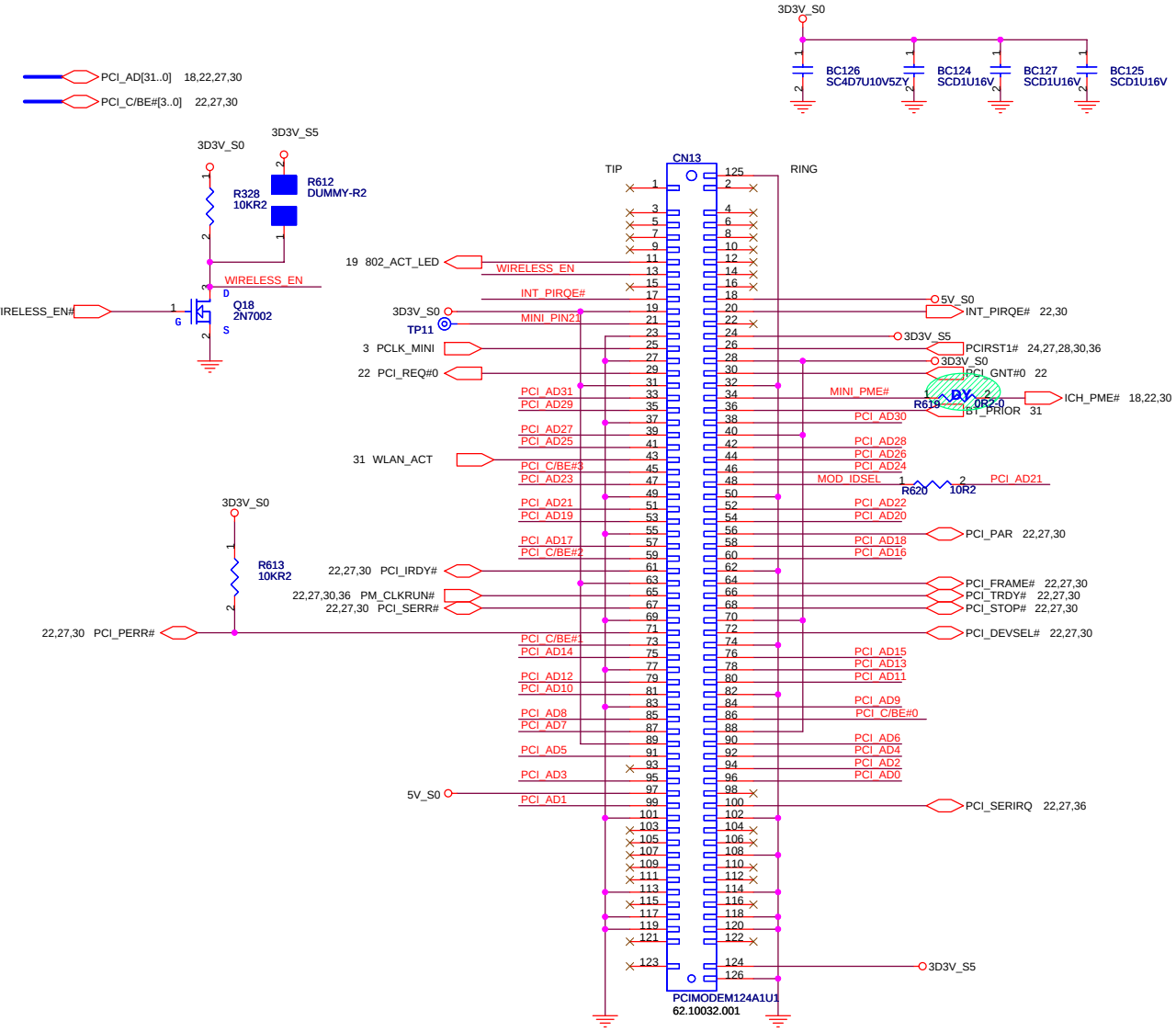
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 33 of 47

MINI-PCI



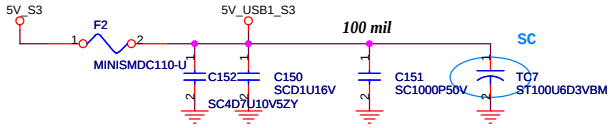
The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

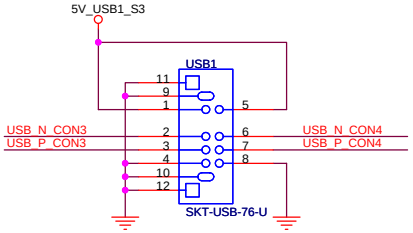
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

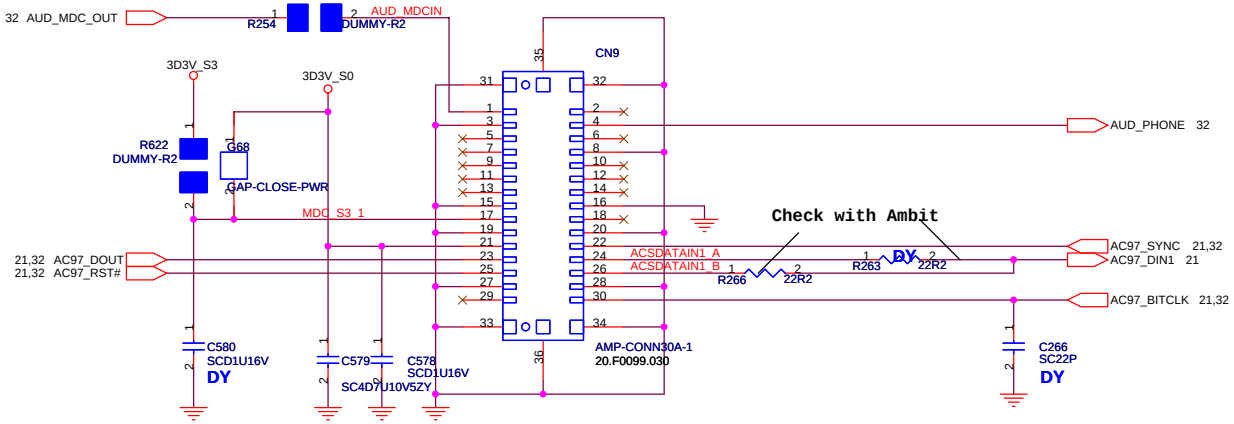
Title	MINI-PCI	
Size A3	Document Number Leopard2	Rev -1
Date: Thursday, July 07, 2005	Sheet 34 of 47	

USB POWER





MDC Connector



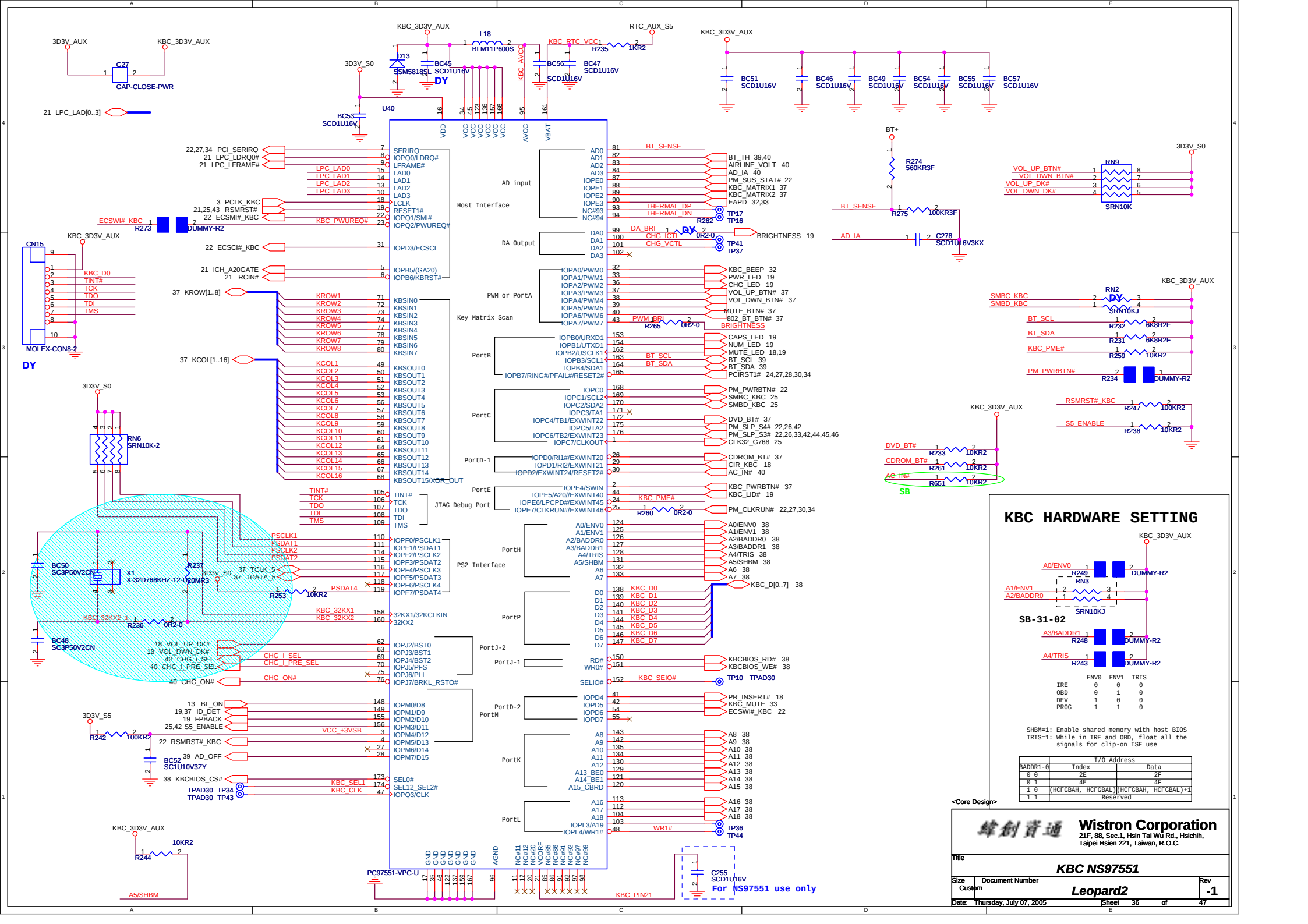
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

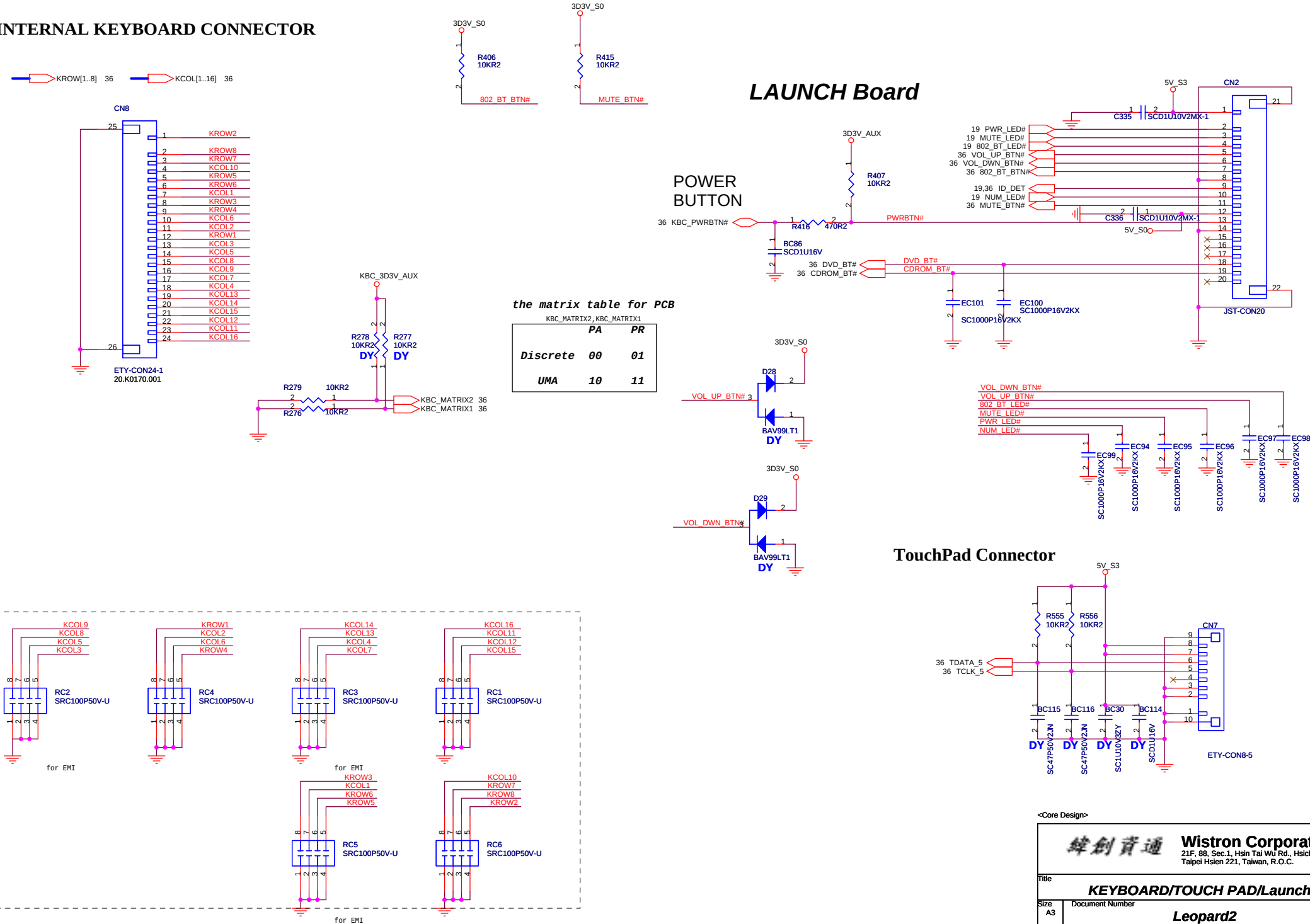
Title: ***USB / MDC CONN.***

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 35 of 47


KBC HARDWARE SETTING
SB-31-02
ENV0 ENV1 TRIS
IRE 0 0 0
OBD 0 1 0
DEV 1 0 0
PROG 1 1 0
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use
I/O Address
BADDR1-0 Index Data
0 0 2E 2F
0 1 4E 4F
1 0 (HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1
1 1 Reserved
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC NS97551
Size Custom
Document Number Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 36 of 47
U40
Host Interface
AD input
DA Output
PWM or PortA
Key Matrix Scan
PortB
PortC
PortD-1
PortE
JTAG Debug Port
PS2 Interface
PortH
PortP
PortJ-2
PortJ-1
PortD-2
PortM
PortK
PortL
PC97551-VPC-U
For NS97551 use only
DY
SB

INTERNAL KEYBOARD CONNECTOR



LAUNCH Board

TouchPad Connector

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCH PAD/Launch key

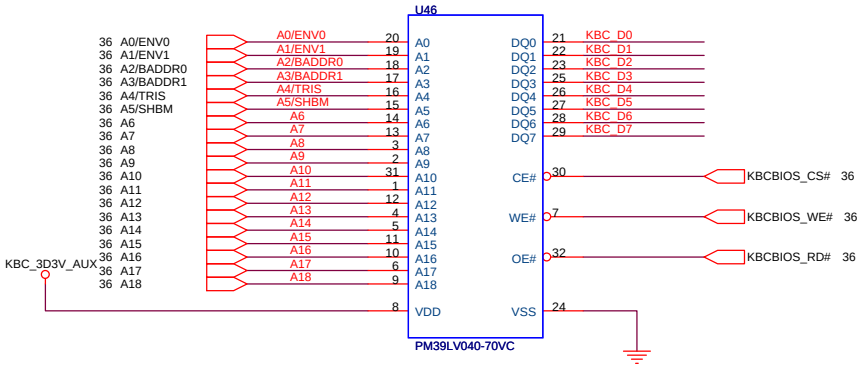
Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Thursday, July 07, 2005 | Sheet 37 of 47

KBC_D[0..7] 36

FLASH ROM

512KB Flash

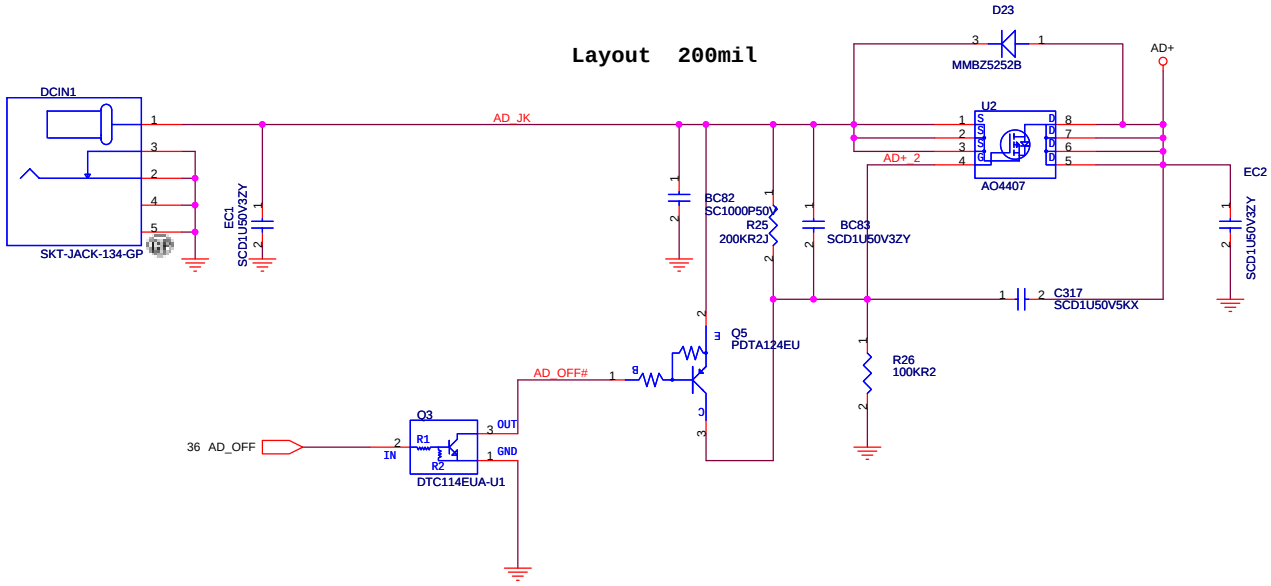


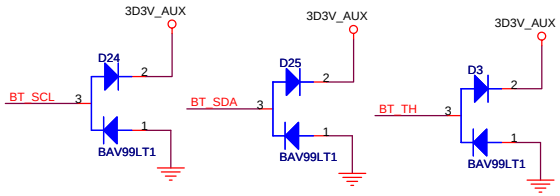
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

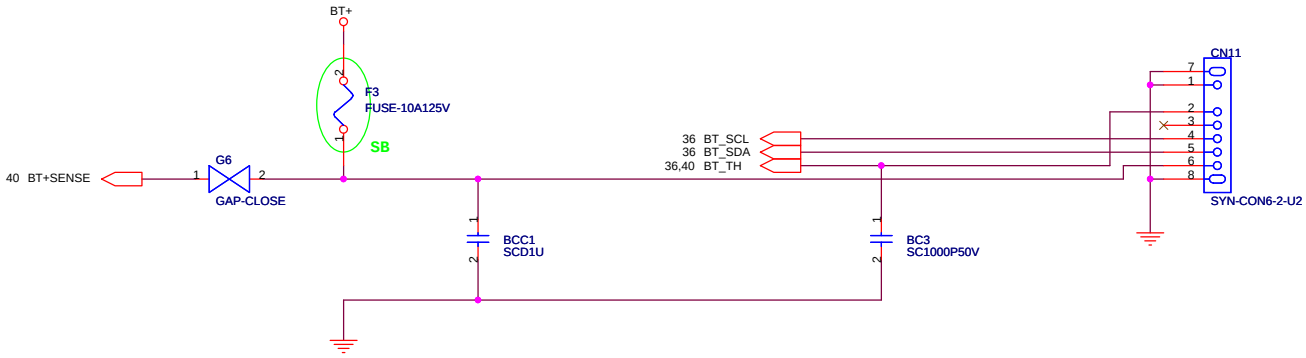
Title	BIOS/GF	
Size A3	Document Number Leopard2	Rev -1
Date: Thursday, July 07, 2005	Sheet 38 of 47	

Adaptor in to generate DCBATOUT





BATTERY CONNECTOR



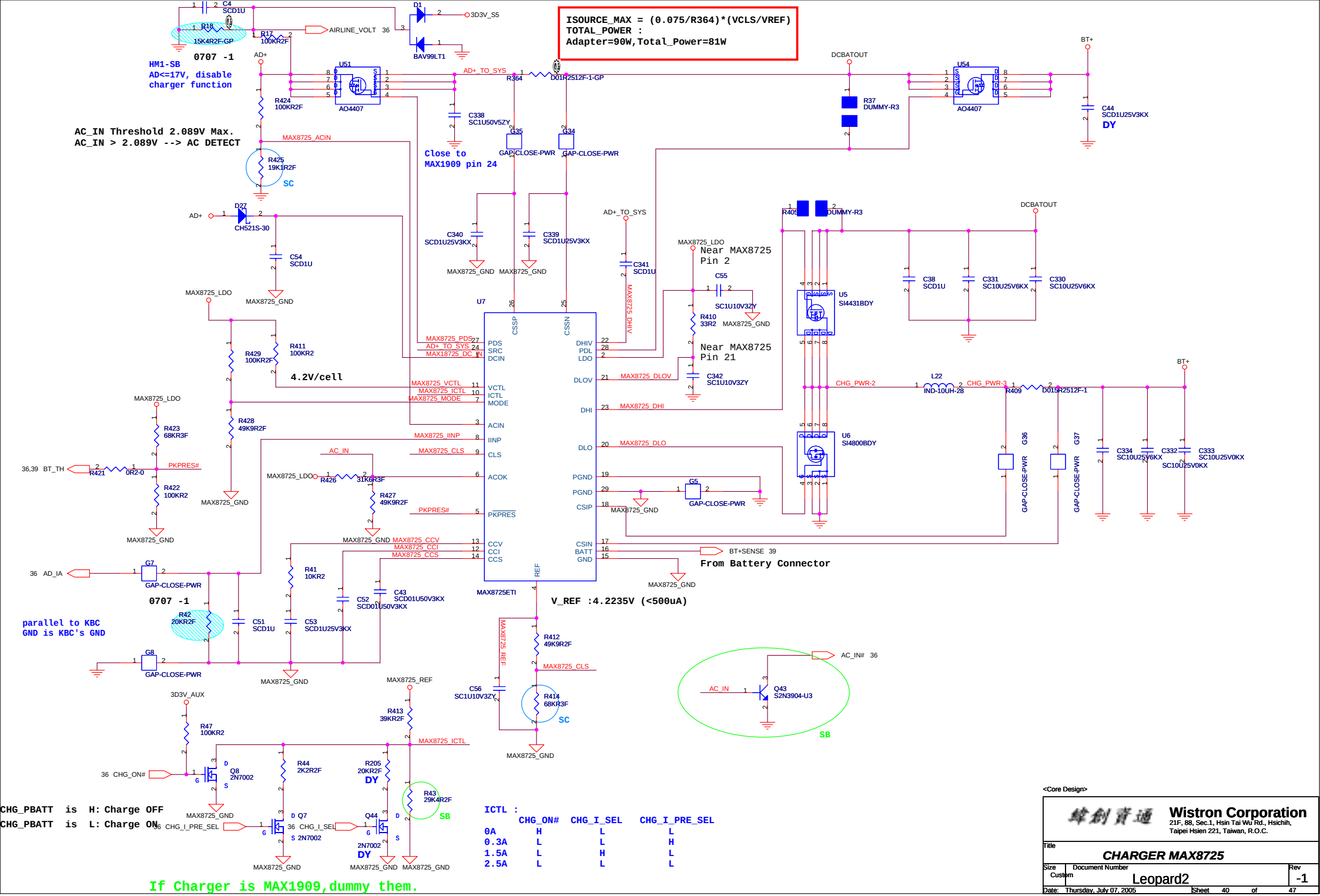
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

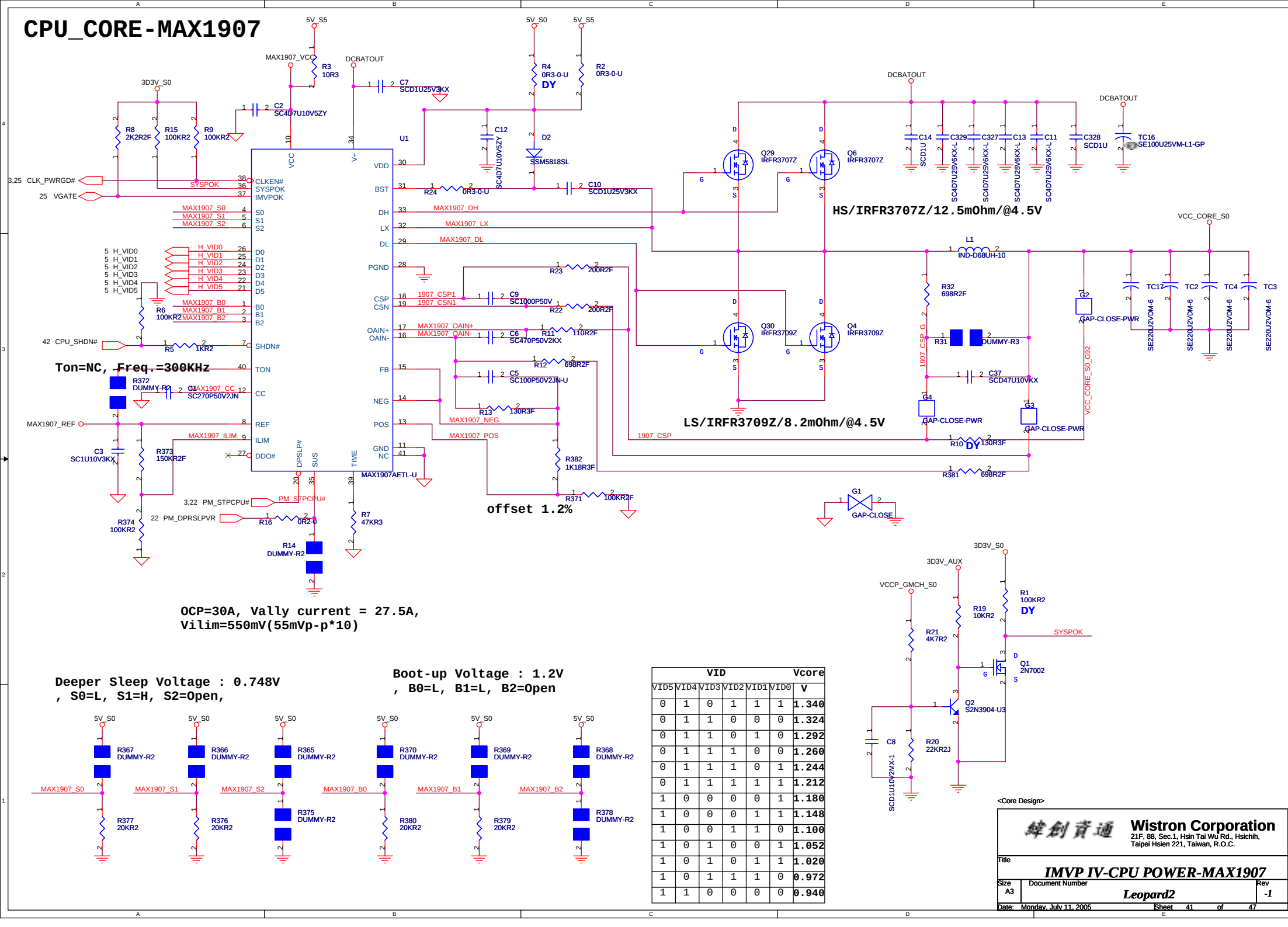
Title: *Adaptor/ Bettery conn.*

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 39 of 47


ISOURCE_MAX = (0.075/R364)*(VCLS/VREF)
TOTAL_POWER :
Adapter=90W,Total_Power=81W
HM1-SB
AD<=17V, disable charger function
0707 -1
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
Close to MAX1909 pin 24
Near MAX8725 Pin 2
Near MAX8725 Pin 21
4.2V/cell
From Battery Connector
V_REF :4.2235V (<500uA)
parallel to KBC
GND is KBC's GND
MAX8725ETI
U7
AO4407
SI4431BDY
SI4800BDY
IND-10UH-28
S2N3904-U3
CH521S-30
BAV99LT1
DUMMY-R3
GAP-CLOSE-PWR
2N7002
DY
SC
SB
CHG_PBATT is H: Charge OFF
CHG_PBATT is L: Charge ON
If Charger is MAX1909,dummy them.
ICTL :
CHG_ON# CHG_I_SEL CHG_I_PRE_SEL
0A H L L
0.3A L L H
1.5A L H L
2.5A L L L
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER MAX8725
Size Custom
Document Number Leopard2
Rev -1
Date: Thursday, July 07, 2005
Sheet 40 of 47

CPU_CORE-MAX1907



VID						Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IMVP IV-CPU POWER-MAX1907

Size: A3 | Document Number: Leopard2 | Rev: -1

Date: Monday, July 11, 2005 | Sheet 41 of 47

TI TPS5130 for 1D8V, 3D3V, 5V

(1D8V=>CH1 , 3D3V=>CH2 , 5V =>CH3)

For 3.3V
SETTING=3.349V

For 5V
SETTING=5.0915V

For 1.8V
SETTING=1.82V

Vo=(R1*0.85)/R2+0.85

close to IC

0703 -1

T(soft)=1.736ms

1D8V_OCP
SC
DCBATOUT
OCP
8.2A=>R186=13K
close to IC

3D3V_OCP
SC
DCBATOUT
OCP
5.82A=>R182=10K
close to IC

5V_OCP
SC
DCBATOUT
OCP
8.88A=>R207=15K
close to IC

TPS5130

TPS5130PT-U

2N7002DW
84.27002.03F

DTC115EE-U

CH521S-30

BAW56-1

BAT54-1
83.00054.L03

TSLCX08-U

GAP-CLOSE-PWR

GAP-CLOSE
ZZ.CON2C.XX1

SC4D7U10V5ZY
78.47593.411

SCD1U25V2ZY-U

SC4700P50V2KX
78.47224.2F1

SC47P50V2JN
78.47034.1F1

SCD1U16V2KX-2

SC1000P50V2KX

SC4700P50V2KX

SCD01U16V2KX

SC1000P25V

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

HW Thermal Throttling

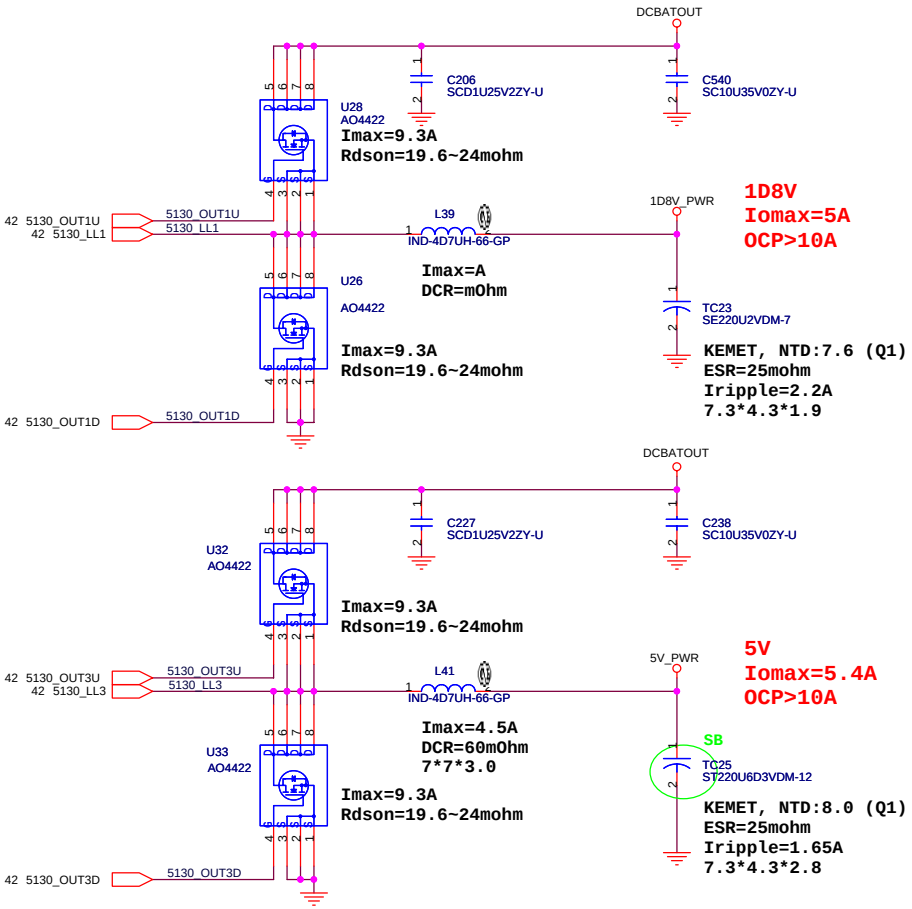
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

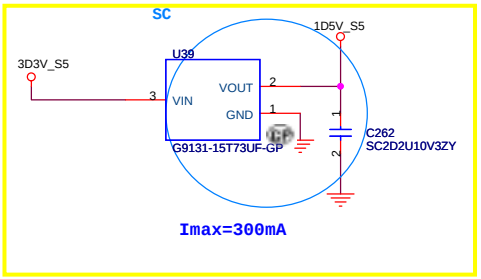
Title		
TPS5130 (3D3V/5V/1D8V)		
Size: A3	Document Number: Leopard2	Rev: -1
Date: Thursday, July 07, 2005	Sheet 42 of 47	

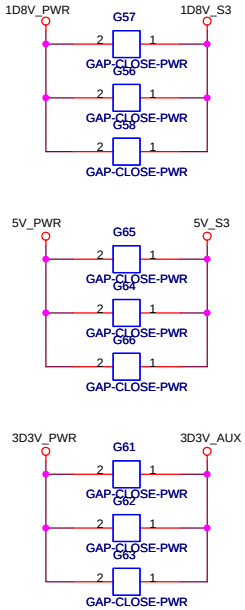
TI TPS5130 for 1D2V, 5V, 3D3V

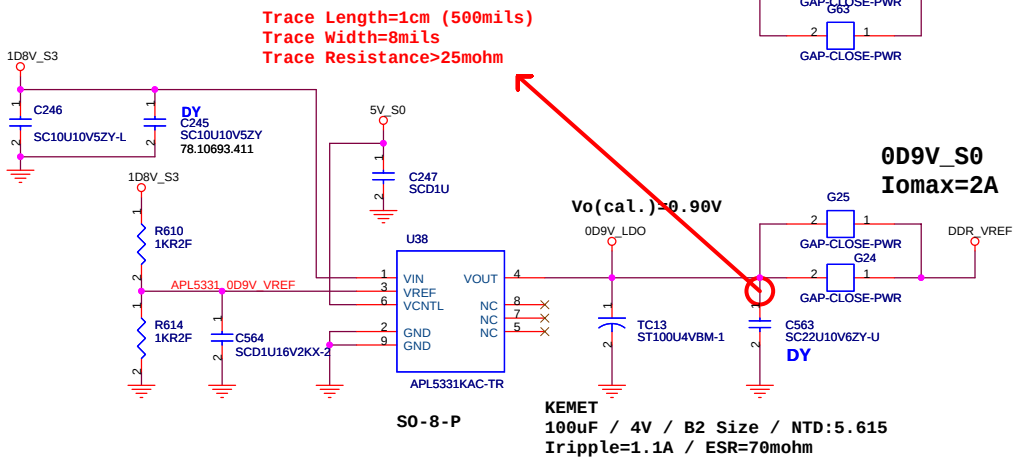
(1D2V=>CH1 , 5V=>CH2 , 3D3V =>CH3)



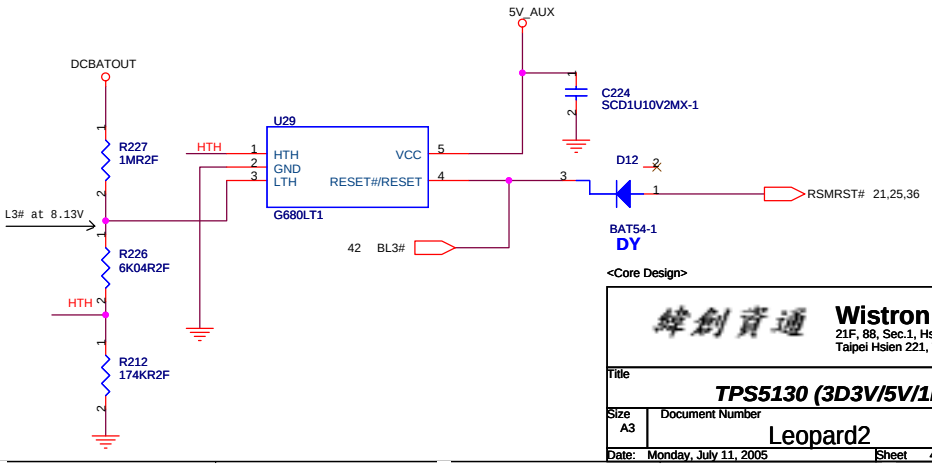
1.5V_S5 (For ICH6)







L3# circuit



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

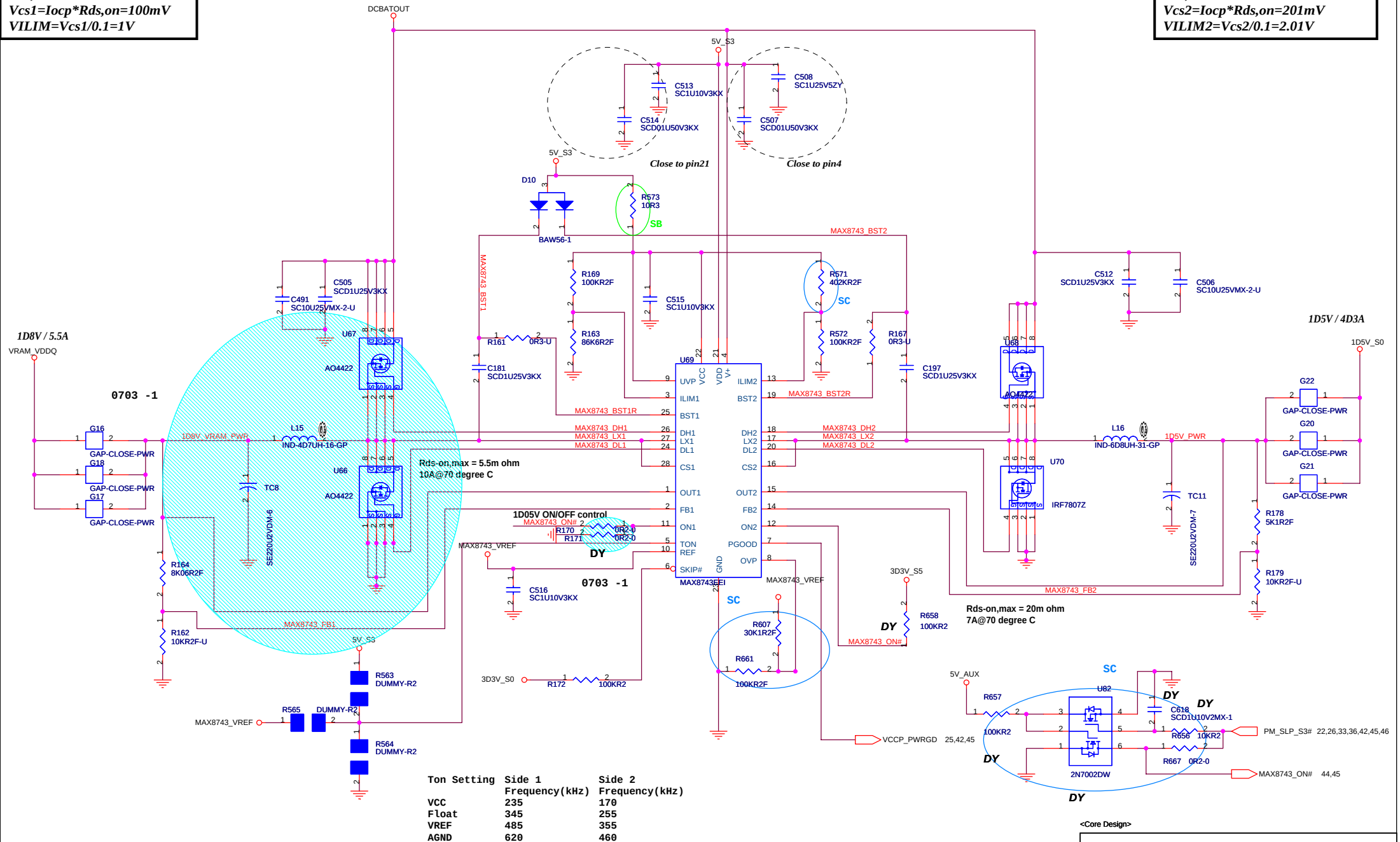
Title: *TPS5130 (3D3V/5V/1D8V/0D9V)*

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 43 of 47

*Iocp=7.8 * 1.7 = 13.3A*
*Rds,on=5.5*1.375=7.563m ohm*
*Vcs1=Iocp*Rds,on=100mV*
VILIM=Vcs1/0.1=1V

*Iocp=4.3 * 1.7 = 7.3A*
*Rds,on=20*1.375=27.5m ohm*
*Vcs2=Iocp*Rds,on=201mV*
VILIM2=Vcs2/0.1=2.01V



Ton Setting	Side 1 Frequency(kHz)	Side 2 Frequency(kHz)
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

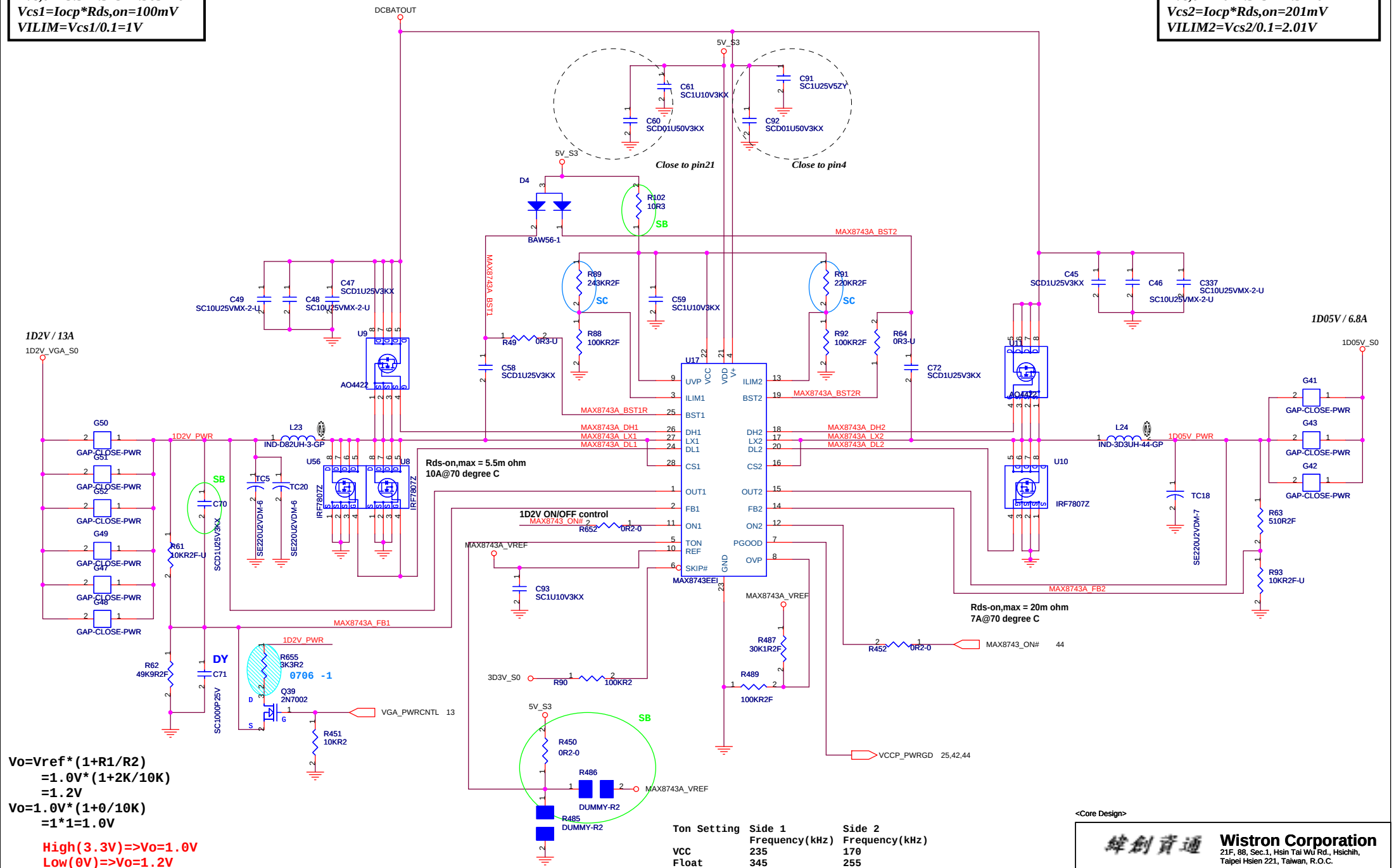
Title: *MAX8743 (1D8V_S0/1D5V_S0)*

Size	Document Number	Rev
A3	Leopard2	-1

Date: Monday, July 11, 2005 Sheet 44 of 47

*Iocp=7.8 * 1.7 = 13.3A*
*Rds,on=5.5*1.375=7.563m ohm*
*Vcs1=Iocp*Rds,on=100mV*
VILIM=Vcs1/0.1=1V

*Iocp=4.3 * 1.7 = 7.3A*
*Rds,on=20*1.375=27.5m ohm*
*Vcs2=Iocp*Rds,on=201mV*
VILIM2=Vcs2/0.1=2.01V




```
Vo=Vref*(1+R1/R2)
    =1.0V*(1+2K/10K)
    =1.2V
Vo=1.0V*(1+0/10K)
    =1*1=1.0V
```

High(3.3V)=>Vo=1.0V
Low(0V)=>Vo=1.2V

M24/M26 POWER PLAY (VGA_PWRCNTL)
high (3.3V) = set lower core voltage (VDDC = 1.0V)
low (0V) = set higher core voltage (VDDC = 1.2V)

Ton Setting	Side 1 Frequency(kHz)	Side 2 Frequency(kHz)
VCC	235	170
Float	345	255
VREF	485	355
AGND	620	460

<Core Design>

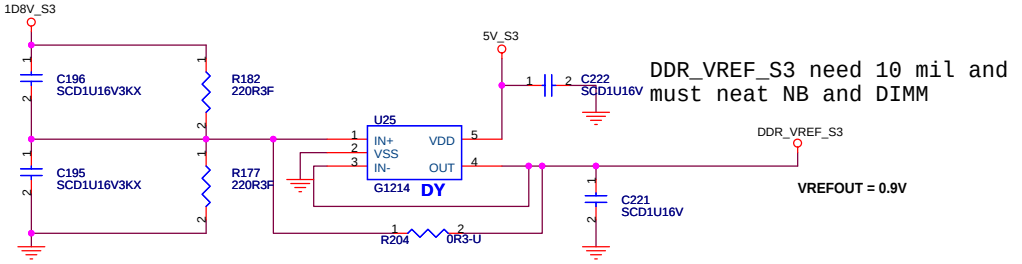
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *MAX8743 (1D2V_VGA_S0/1D05V)*

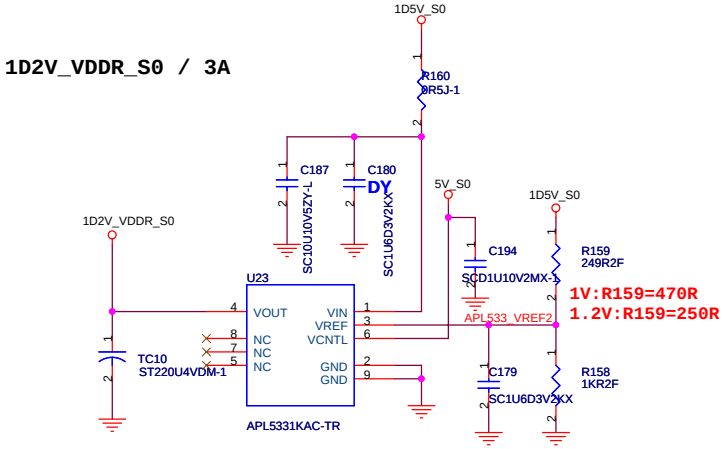
Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 45 of 47

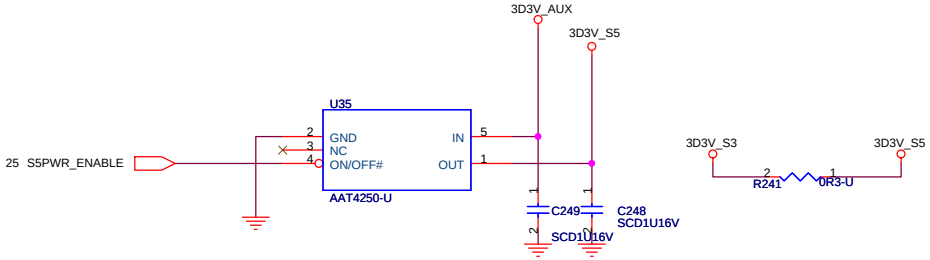
FOR GMCH Power



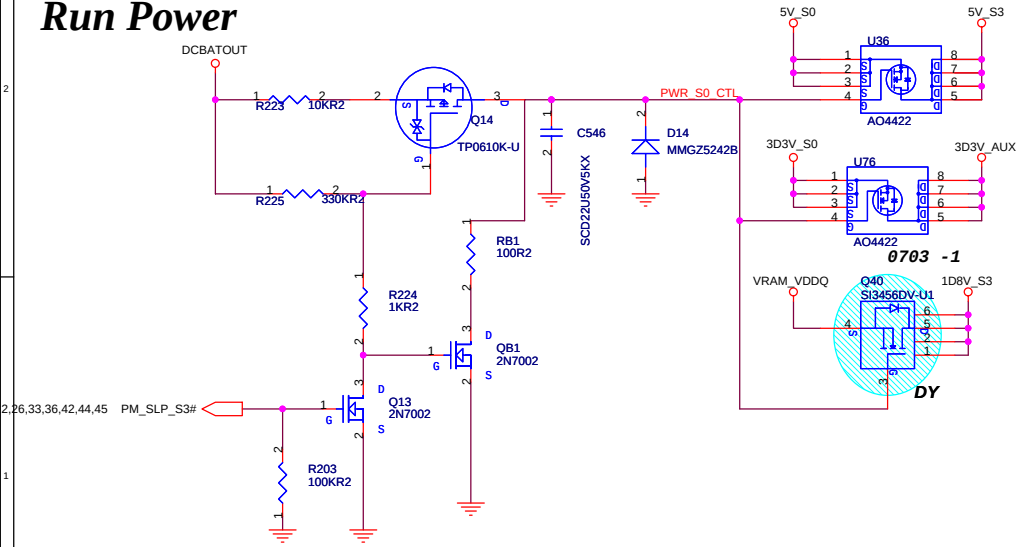
FOR DDR2 Power

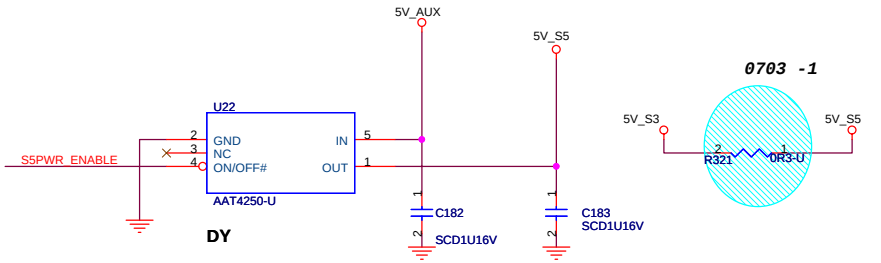


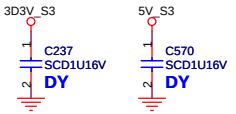
Suspend Power



Run Power



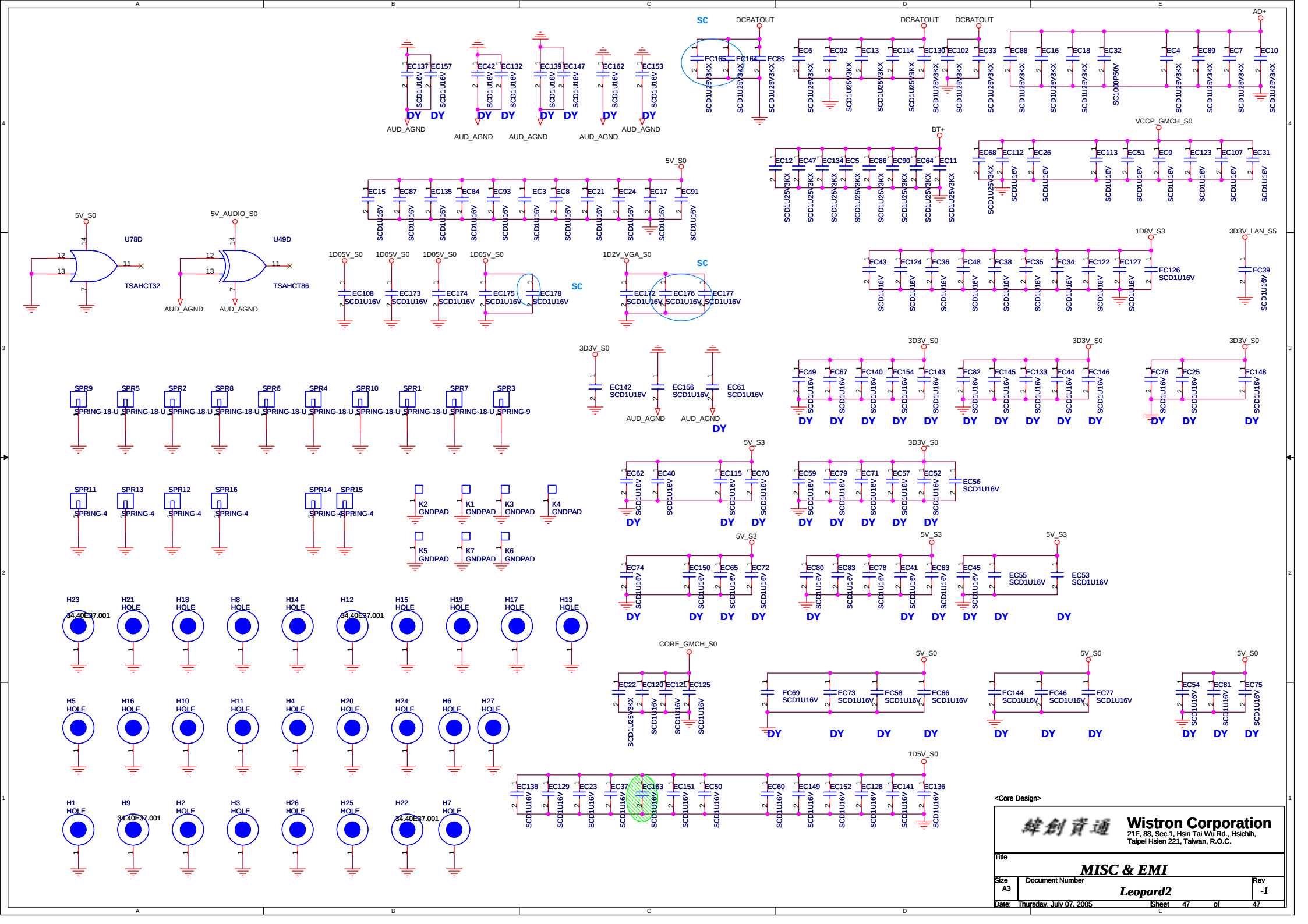




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWRPLANE&RESETLOGIC	
Size A3	Document Number Leopard2	Rev -1
Date: Thursday, July 07, 2005	Sheet 46 of 47	



<core_design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MISC & EMI**

Size	Document Number	Rev
A3	Leopard2	-1

Date: Thursday, July 07, 2005 Sheet 47 of 47
</core_design>