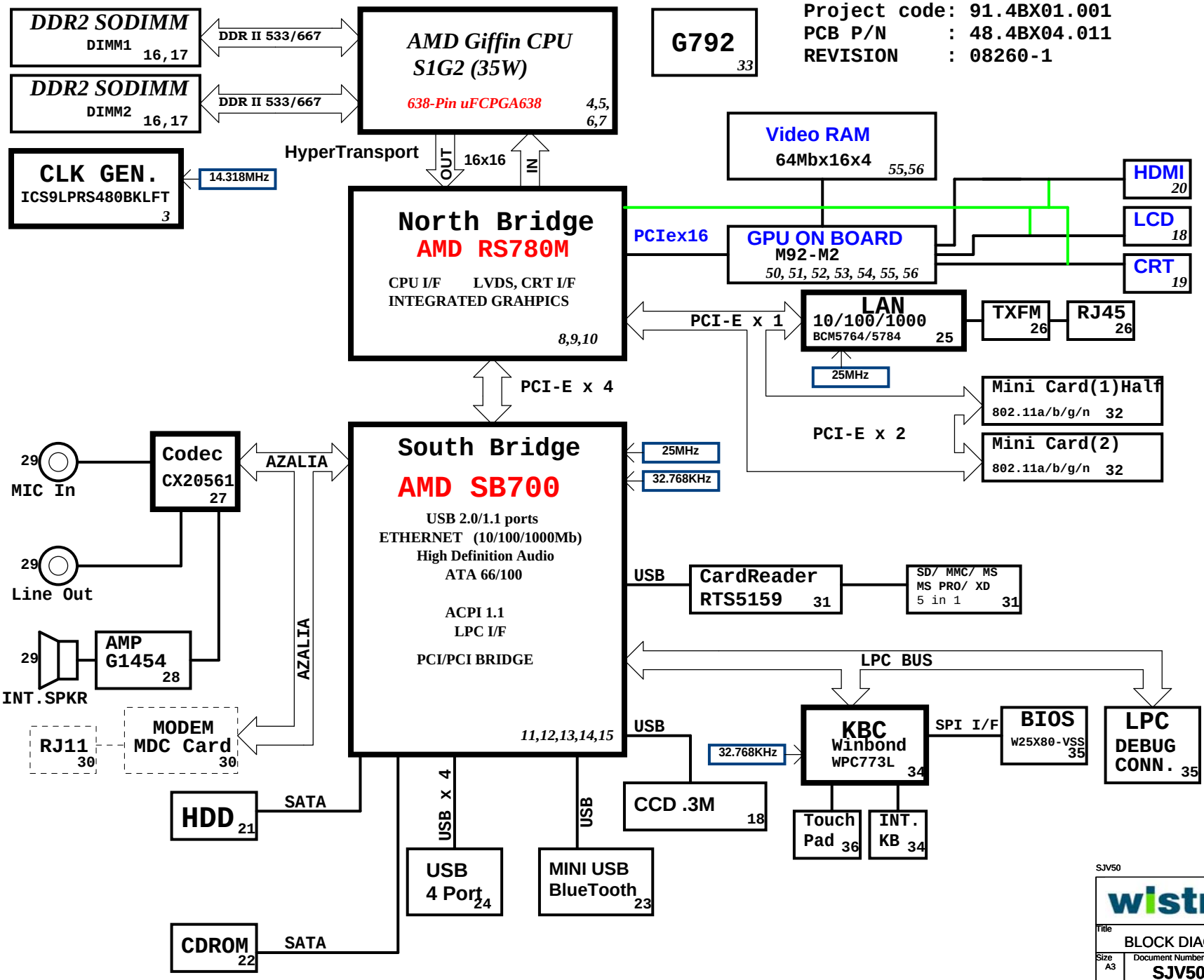
SJV50-PU Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D1V_S0 1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SJV50

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

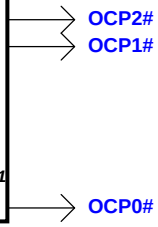
Size: A3 | Document Number: SJV50-PU | Rev: -1

Date: Wednesday, February 25, 2009 | Sheet 1 of 59

PCIE

PCIE0	LAN
PCIE1	MINICARD1
PCIE2	MINICARD2
PCIE3	

USB	
Pair	Device
11	CardReader
10	CCD
9	Mini Card2
8	USB4
7	USB1
6	USB2
5	BlueTooth
4	NC
3	NC
2	NC
1	Mini Card1
0	USB3



SJV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB&PCIE ROUTING

Size: A3 | Document Number: SJV50-PU | Rev: -1

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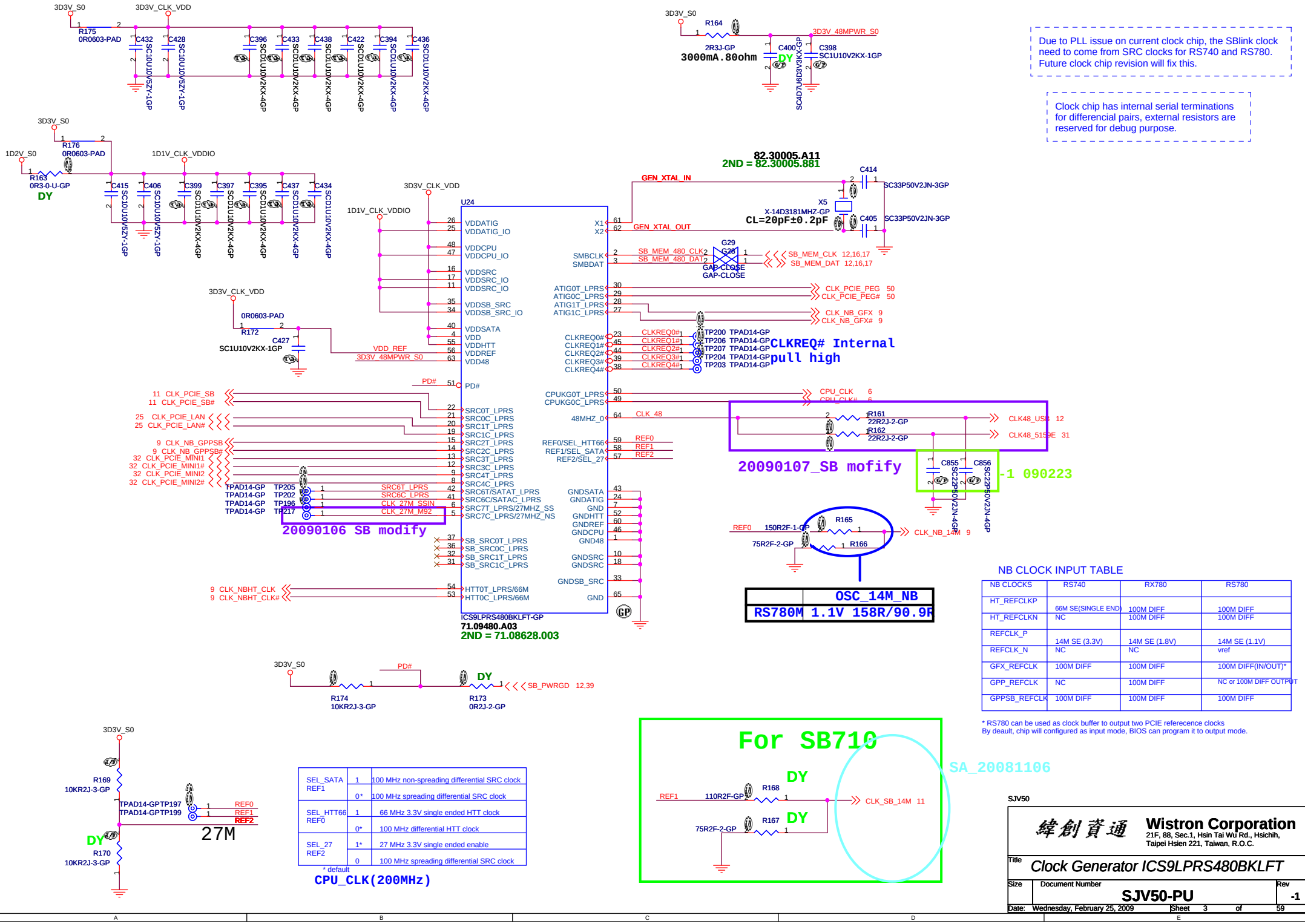
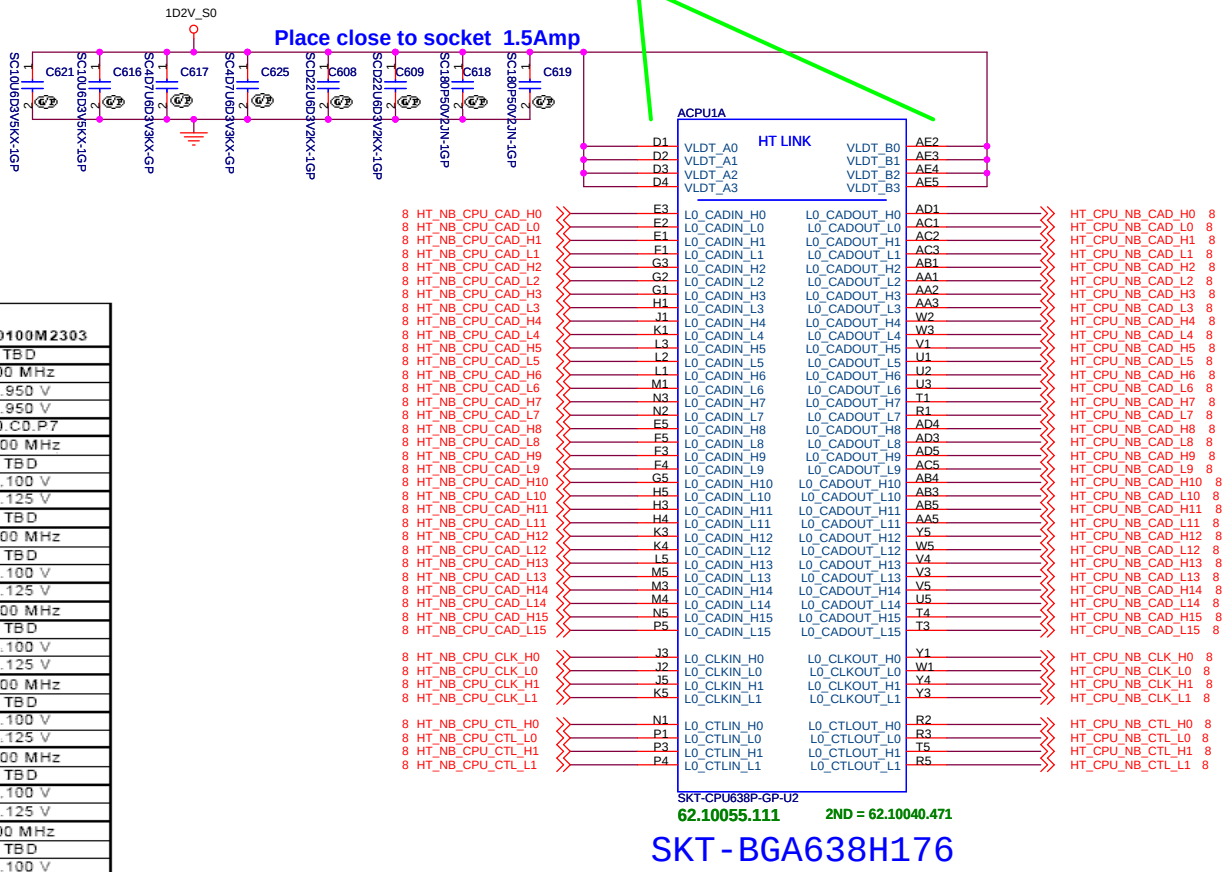

3D3V_S0
3D3V_CLK_VDD
R175 0R0603-PAD
C432 SC10U10V5ZY-1GP
C428 SC10U10V5ZY-1GP
C396 SCD1U10V2KX-4GP
C433 SCD1U10V2KX-4GP
C438 SCD1U10V2KX-4GP
C422 SCD1U10V2KX-4GP
C394 SCD1U10V2KX-4GP
C436 SCD1U10V2KX-4GP
3D3V_S0
R164
2R3J-GP
3000mA.80ohm
3D3V_48MPWR_S0
C400 DY
C398 SC1U10V2KX-1GP
SC4D7U6D3V3KX-GP
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
3D3V_S0
1D2V_S0
R176 0R0603-PAD
R163 0R3-0-U-GP
DY
1D1V_CLK_VDDIO
C415 SC10U10V5ZY-1GP
C406 SC10U10V5ZY-1GP
C399 SCD1U10V2KX-4GP
C397 SCD1U10V2KX-4GP
C395 SCD1U10V2KX-4GP
C437 SCD1U10V2KX-4GP
C434 SCD1U10V2KX-4GP
82.30005.A11
2ND = 82.30005.881
3D3V_CLK_VDD
1D1V_CLK_VDDIO
U24
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
GEN_XTAL_IN
GEN_XTAL_OUT
X5
X-14D3181MHZ-GP
CL=20pF±0.2pF
C414 SC33P50V2JN-3GP
C405 SC33P50V2JN-3GP
SMBCLK
SMBDAT
SB_MEM_480_CLK
SB_MEM_480_DAT
G29 GAP-CLOSE
G28 GAP-CLOSE
SB_MEM_CLK 12,16,17
SB_MEM_DAT 12,16,17
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLK_PCIE_PEG 50
CLK_PCIE_PEG# 50
CLK_NB_GFX 9
CLK_NB_GFX# 9
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TP200 TPAD14-GP
TP206 TPAD14-GP
TP207 TPAD14-GP
TP204 TPAD14-GP
TP203 TPAD14-GP
CLKREQ# Internal pull high
3D3V_CLK_VDD
0R0603-PAD
R172
C427 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
PD#
CPUKG0T_LPRS
CPUKG0C_LPRS
CPU_CLK 6
CPU_CLK# 6
48MHZ_0
CLK_48
R161 22R2J-2-GP
R162 22R2J-2-GP
CLK48_USB 12
CLK48_515DE 31
20090107_SB mofify
C855 SC22P50V2JN-4GP
C856 SC22P50V2JN-4GP
-1 090223
11 CLK_PCIE_SB
11 CLK_PCIE_SB#
25 CLK_PCIE_LAN
25 CLK_PCIE_LAN#
9 CLK_NB_GPPSB
9 CLK_NB_GPPSB#
32 CLK_PCIE_MINI1
32 CLK_PCIE_MINI1#
32 CLK_PCIE_MINI2
32 CLK_PCIE_MINI2#
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
TPAD14-GP TP205
TPAD14-GP TP202
TPAD14-GP TP196
TPAD14-GP TP217
SRC6T_LPRS
SRC6C_LPRS
CLK_27M_SSIN
CLK_27M_M92
20090106 SB modify
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
REF0
REF1
REF2
R165
R166
150R2F-1-GP
75R2F-2-GP
CLK_NB_14M 9
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSRC
GNDSB_SRC
GND
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
HTT0T_LPRS/66M
HTT0C_LPRS/66M
ICS9LPRS480BKLFT-GP
71.09480.A03
2ND = 71.08628.003
OSC_14M_NB
RS780M 1.1V 158R/90.9R
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
3D3V_S0
PD#
DY
R174 10KR2J-3-GP
R173 0R2J-2-GP
SB_PWRGD 12,39
3D3V_S0
R169 10KR2J-3-GP
TPAD14-GPTP197
TPAD14-GPTP199
REF0
REF1
REF2
27M
DY
R170 10KR2J-3-GP
SEL_SATA REF1
1 100 MHz non-spreading differential SRC clock
0* 100 MHz spreading differential SRC clock
SEL_HTT66 REF0
1 66 MHz 3.3V single ended HTT clock
0* 100 MHz differential HTT clock
SEL_27 REF2
1* 27 MHz 3.3V single ended enable
0 100 MHz spreading differential SRC clock
* default
CPU_CLK(200MHz)
For SB710
DY
REF1
110R2F-GP
R168
CLK_SB_14M 11
DY
75R2F-2-GP
R167
SA_20081106
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator ICS9LPRS480BKLFT
Size
Document Number
SJV50-PU
Rev
-1
Date: Wednesday, February 25, 2009
Sheet 3 of 59

Placement note:
10ux1,4.7ux1,0.22ux1,180px1 for each group



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

SJV50

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***CPU (1 of 4)***

Size | Document Number: **SJV50-PU** | Rev: -1

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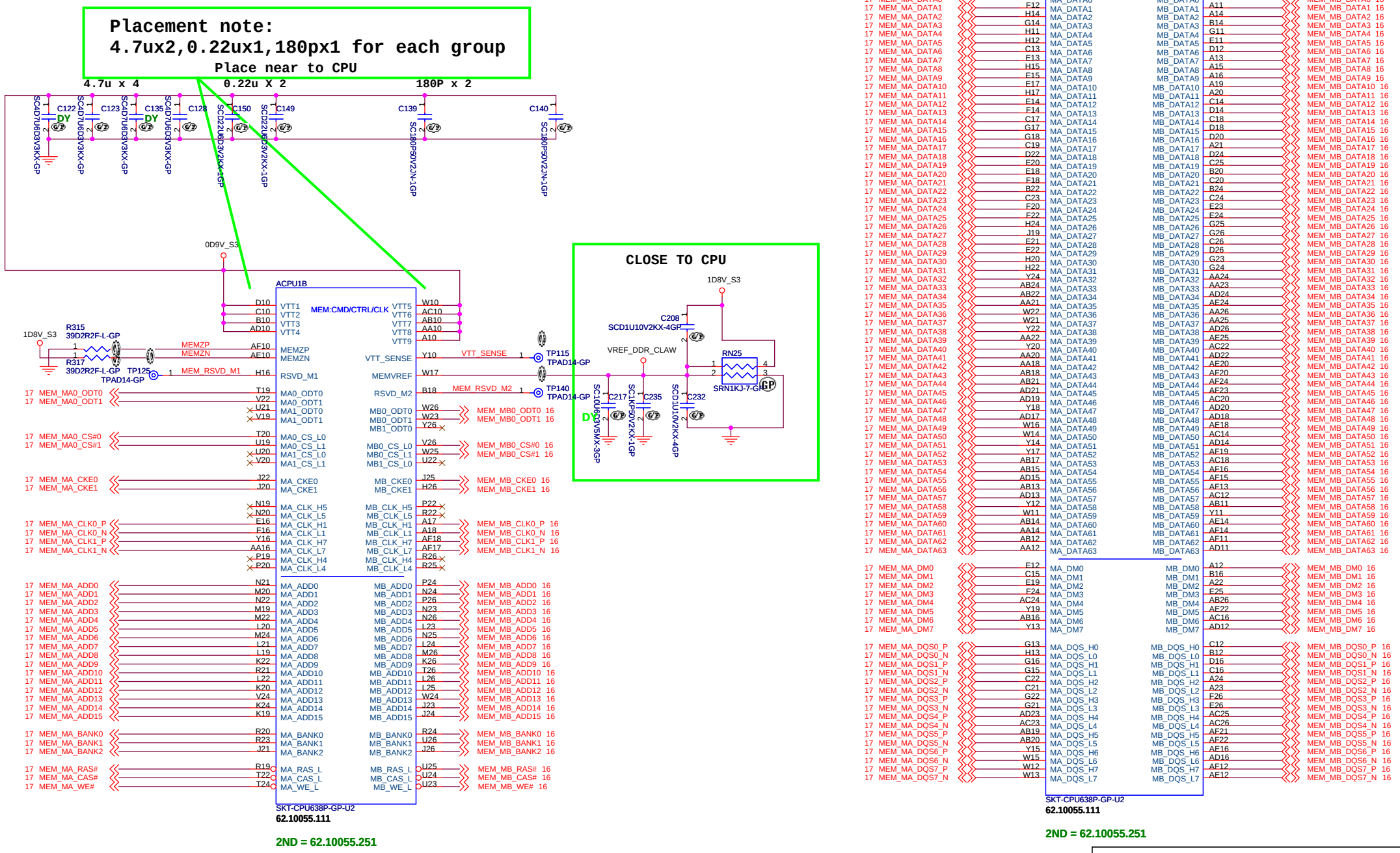

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (2 of 4)

Size | Document Number: SJV50-PU | Rev: -1

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The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

SA_20081127

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

-1 090213

20081126

SA_20081030

CPU exceeds to 125℃

SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10040.471

84.T3904.C11
2ND = 84.03904.L06

HDT Connectors

HDT1 DY
SMC-CONN26A-FP

SJV50

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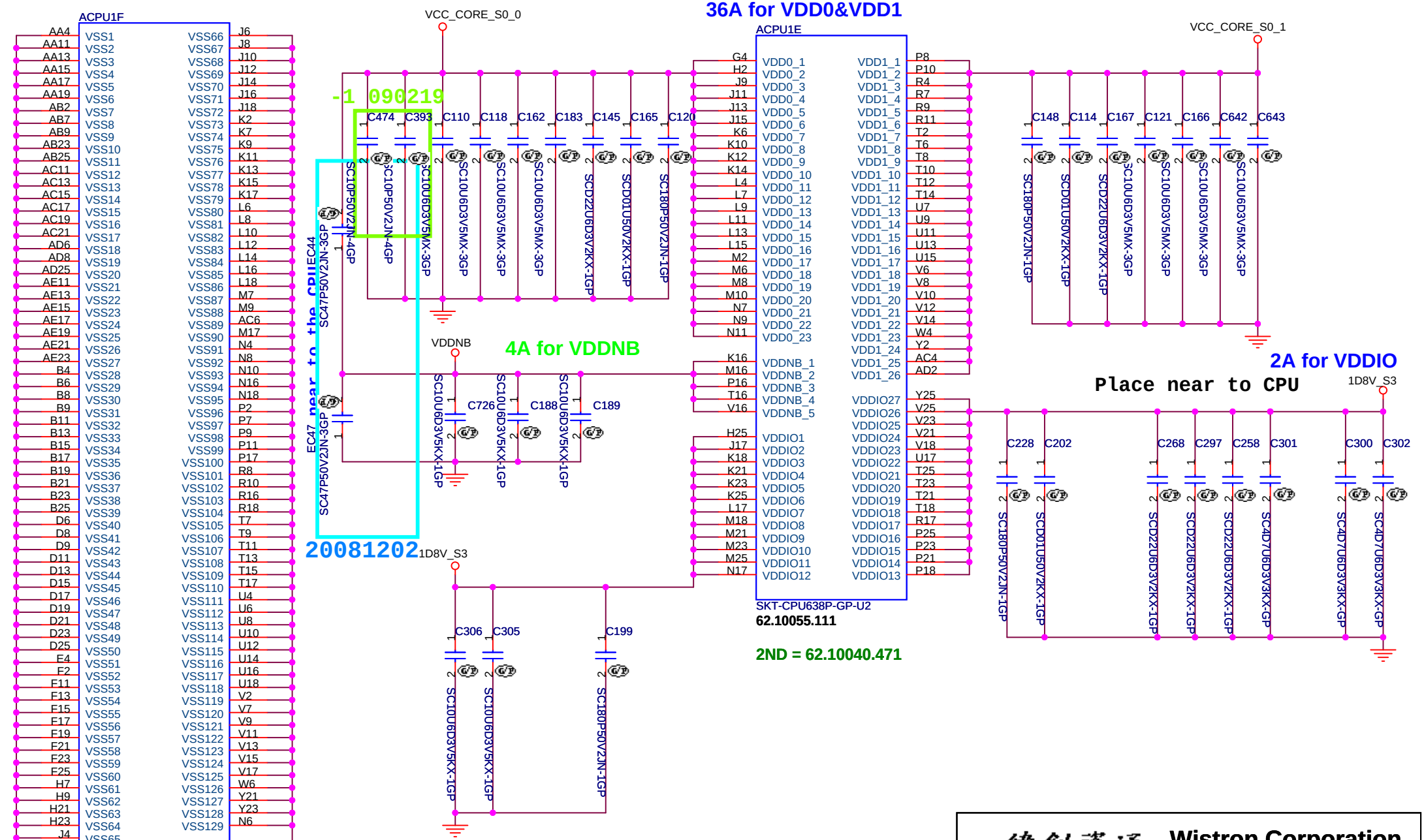
Title: CPU (3 of 4)
Size: Document Number: SJV50-PU Rev: -1
Date: Wednesday, February 25, 2009 Sheet 6 of 59


ACPU1F
SKT-CPU638P-GP-U2
62.10055.111
VCC_CORE_S0_0
-1 090219
C474 C393 C110 C118 C162 C183 C145 C165 C120
SC10P50V2JN-4GP
SC10U6D3V5MX-3GP
SC22U6D3V2KX-1GP
SC01U50V2KX-1GP
SC180P50V2JN-1GP
EC44 SC47P50V2JN-3GP
EC47 SC47P50V2JN-3GP
near to the CPU
20081202
VDDNB
4A for VDDNB
C726 C188 C189
SC10U6D3V5KX-1GP
1D8V_S3
C306 C305 C199
SC10U6D3V5KX-1GP
SC180P50V2JN-1GP
36A for VDD0&VDD1
ACPU1E
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10040.471
VCC_CORE_S0_1
C148 C114 C167 C121 C166 C642 C643
2A for VDDIO
Place near to CPU
1D8V_S3
C228 C202 C268 C297 C258 C301 C300 C302
SC4D7U6D3V3KX-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (4 of 4)
Size
Document Number
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Date: Wednesday, February 25, 2009
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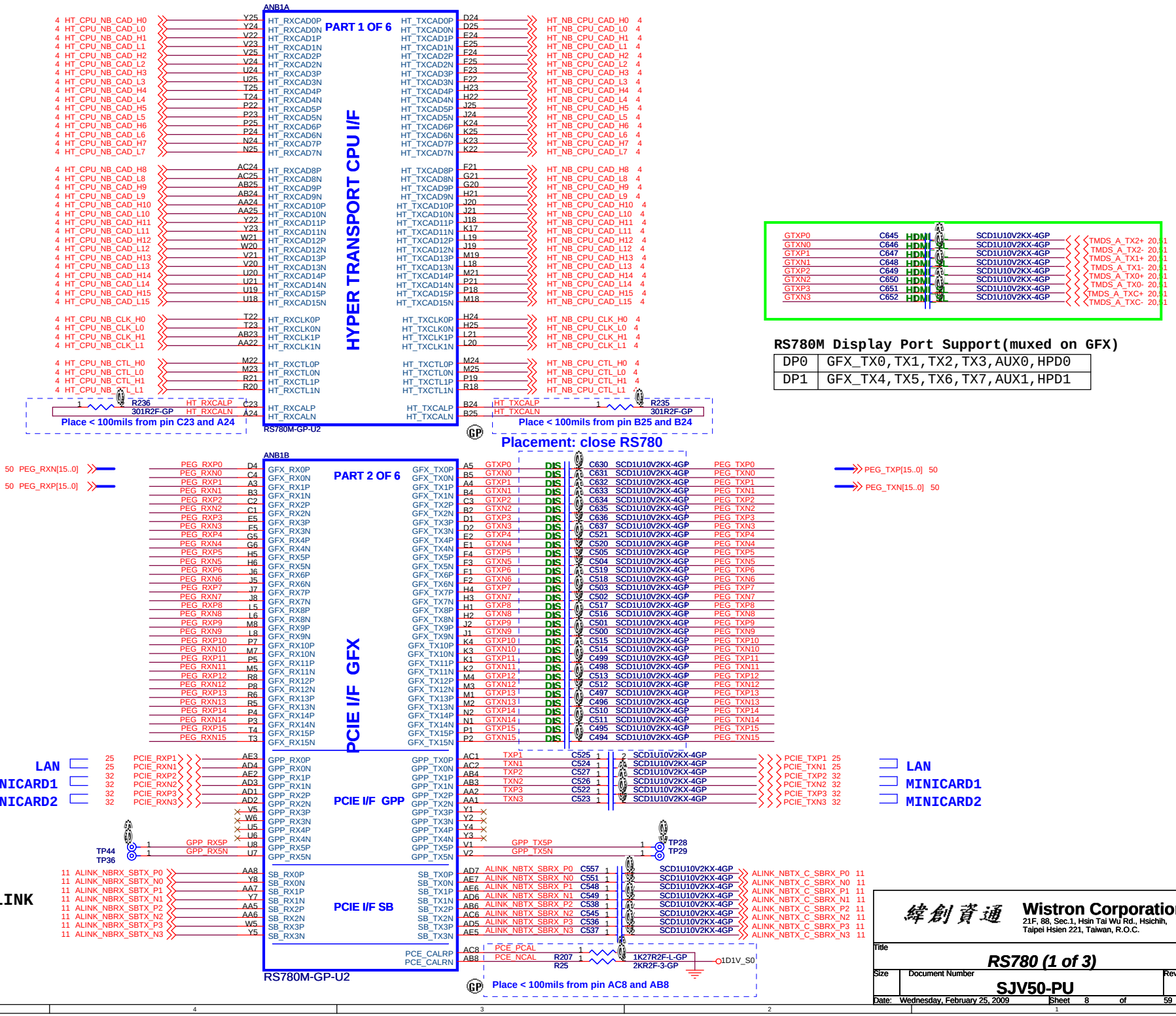
ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS780
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Place < 100mils from pin AC8 and AB8
LAN
MINICARD1
MINICARD2
A-LINK
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RS780 (1 of 3)
Size
Document Number
SJV50-PU
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-1
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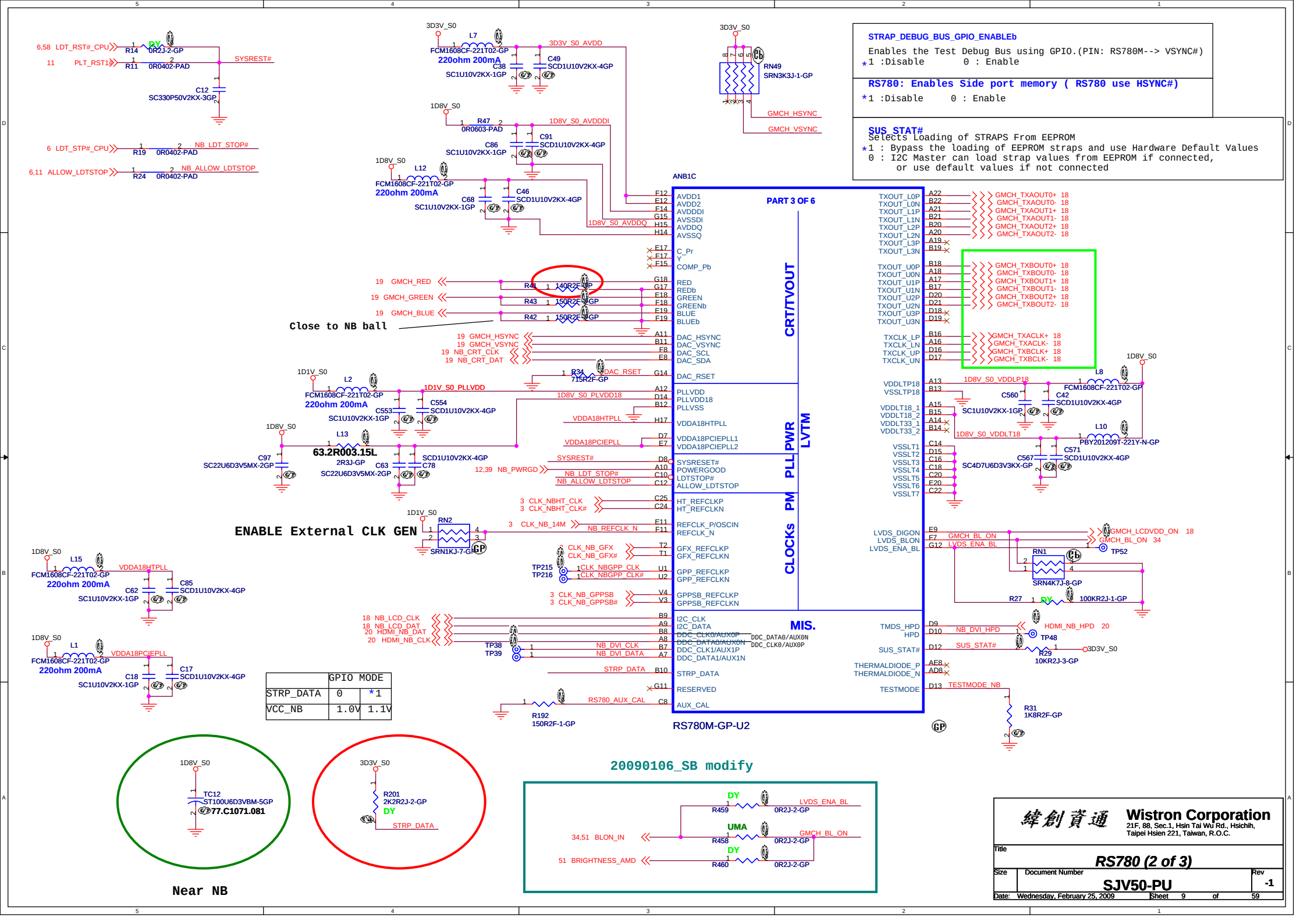
STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
ANB1C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
PLL PWR
LVTM
CLOCKs PM
MIS.
Close to NB ball
ENABLE External CLK GEN
Near NB
20090106_SB modify
GPIO MODE
STRP_DATA 0 *1
VCC_NB 1.0V 1.1V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RS780 (2 of 3)
SJV50-PU
Rev -1
Date: Wednesday, February 25, 2009
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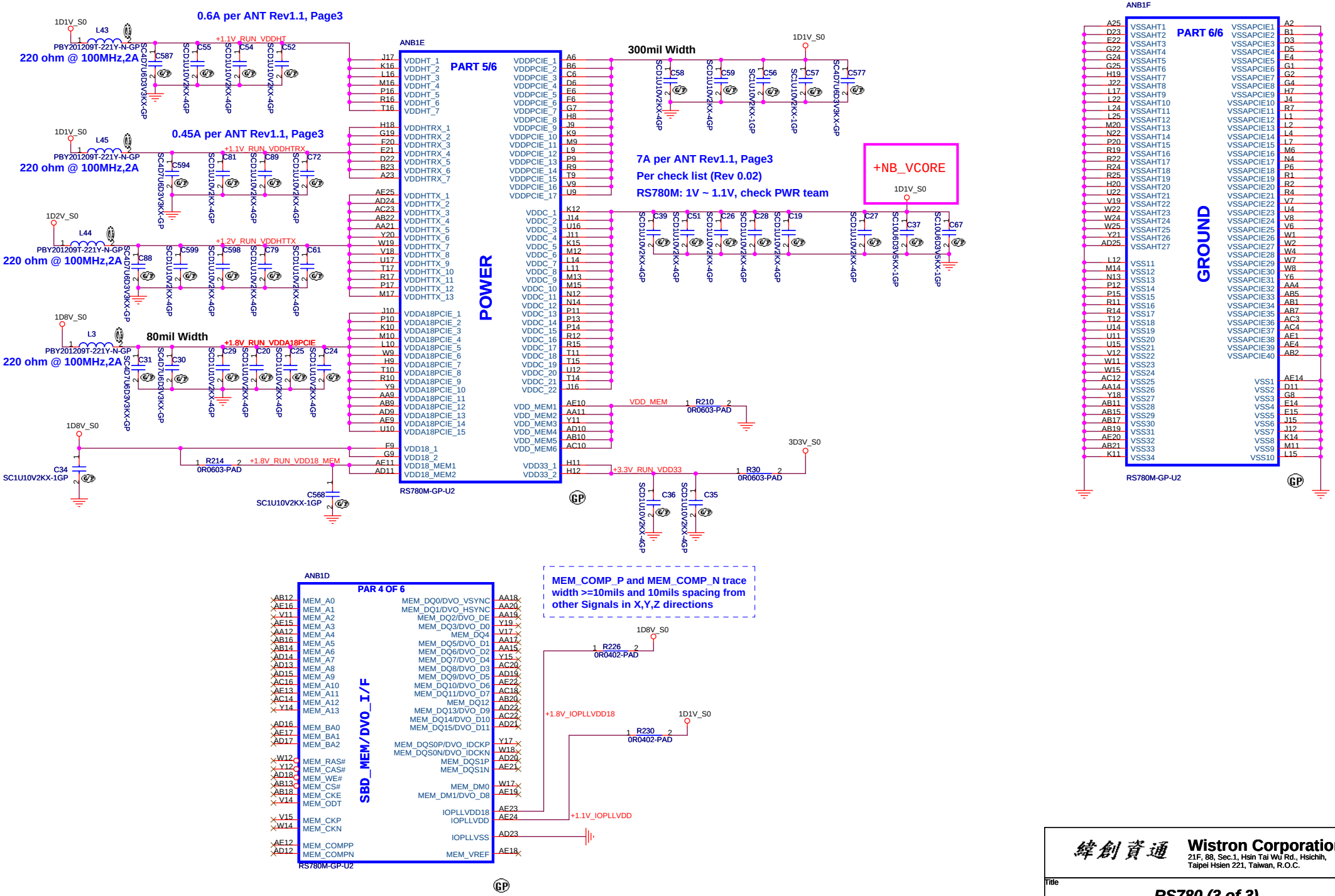
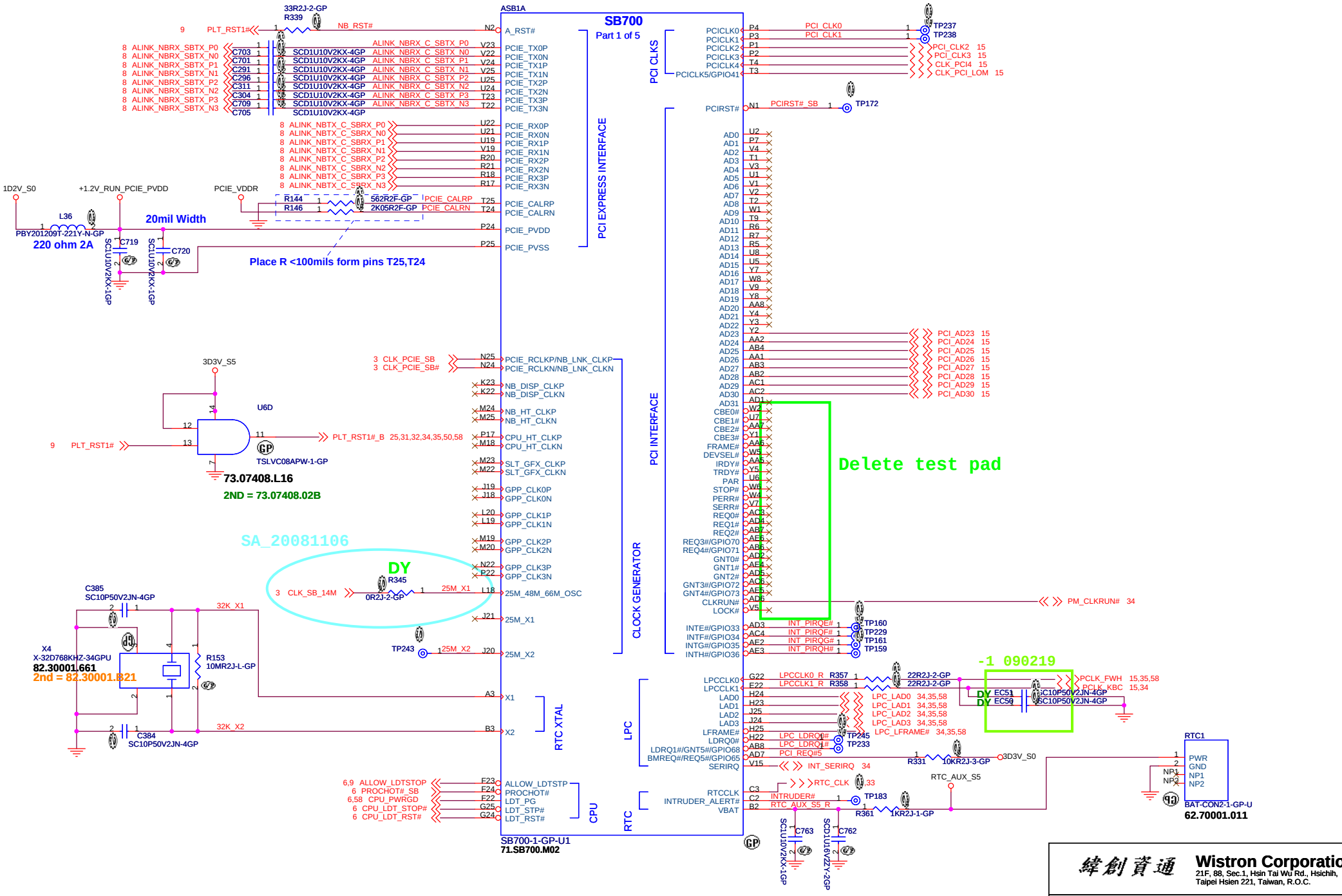

0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
ANB1E
PART 5/6
POWER
RS780M-GP-U2
ANB1F
PART 6/6
GROUND
RS780M-GP-U2
ANB1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
RS780M-GP-U2
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RS780 (3 of 3)
SJV50-PU
Rev -1
Date: Wednesday, February 25, 2009
Sheet 10 of 59



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***SB700 (1 of 5)***		
Size	Document Number **SJV50-PU**		Rev -1
Date: Wednesday, February 25, 2009	Sheet 11 of 59		

20090114 SB

SB700

Part 4 of 5

ASB1D

SB700-1-GP-U1

71.SB700.M02

USB

Pair	Device
11	CardReader
10	CCD
9	Mini Card2
8	USB4
7	USB3
6	USB2
5	BlueTooth
4	NC
3	NC
2	NC
1	Mini Card1
0	USB1

OCP2#

OCP1#

OCP0#

Close to SB700

TO STRAPS

Strap Pin / define to use LPC or SPI ROM

Place these close SB700

Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.

SJV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB700 (2 of 5)

Size | Document Number: SJV50-PU | Rev: -1

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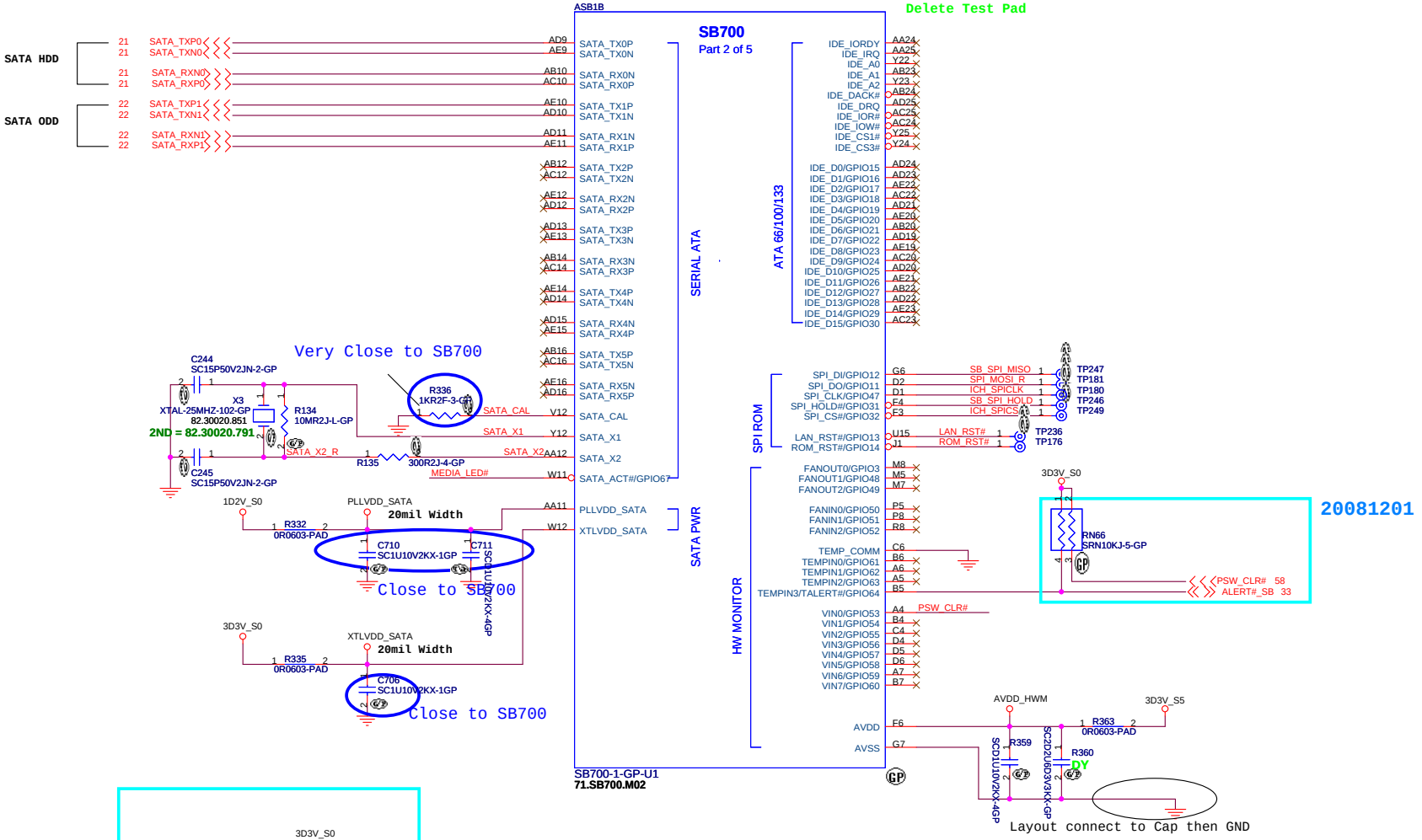

SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***SB700 (3 of 5)***
Size	Document Number: **SJV50-PU** Rev: -1
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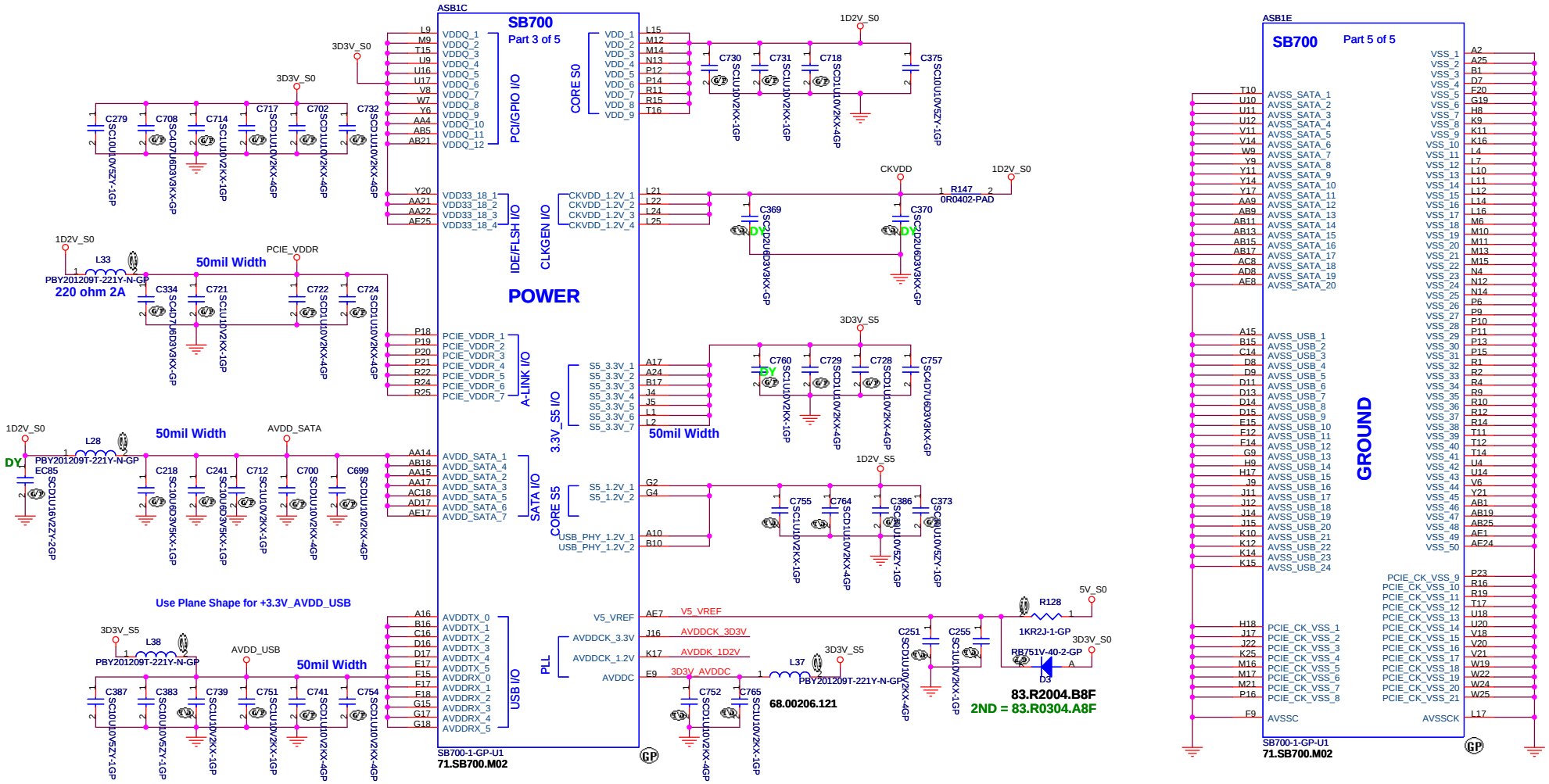


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB700 (4 of 5)

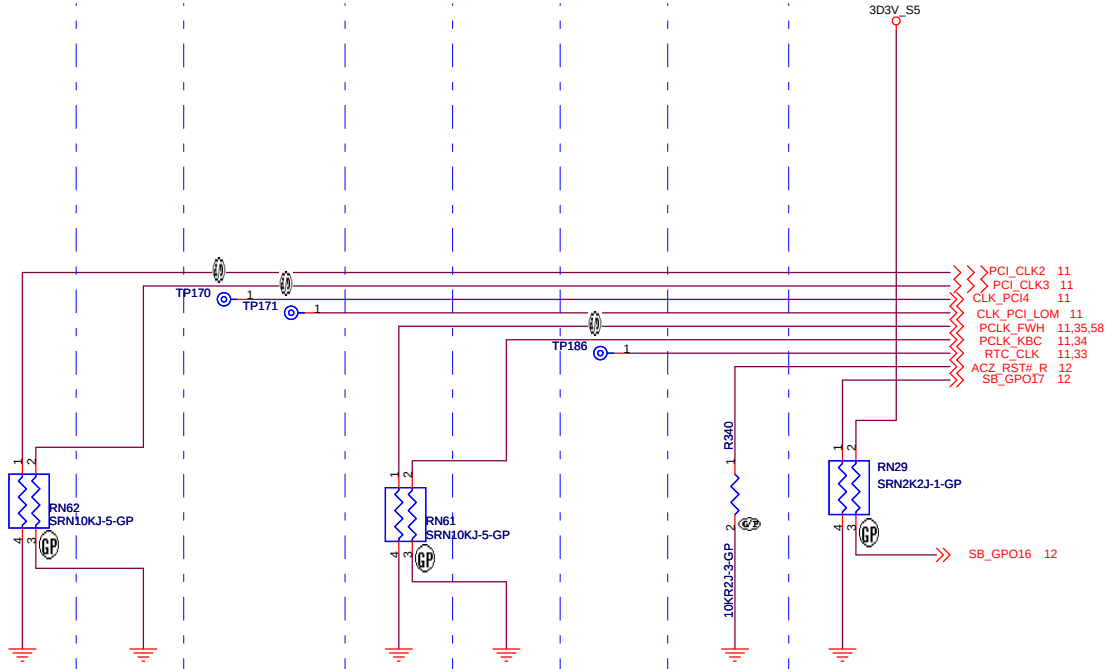
Size	Document Number	Rev
	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 14 of 59

Delete DY Parts

REQUIRED STRAPS

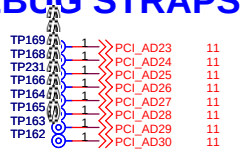
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

緯創資通 Wistron Corporation
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Title: *SB700 (5 of 5)*

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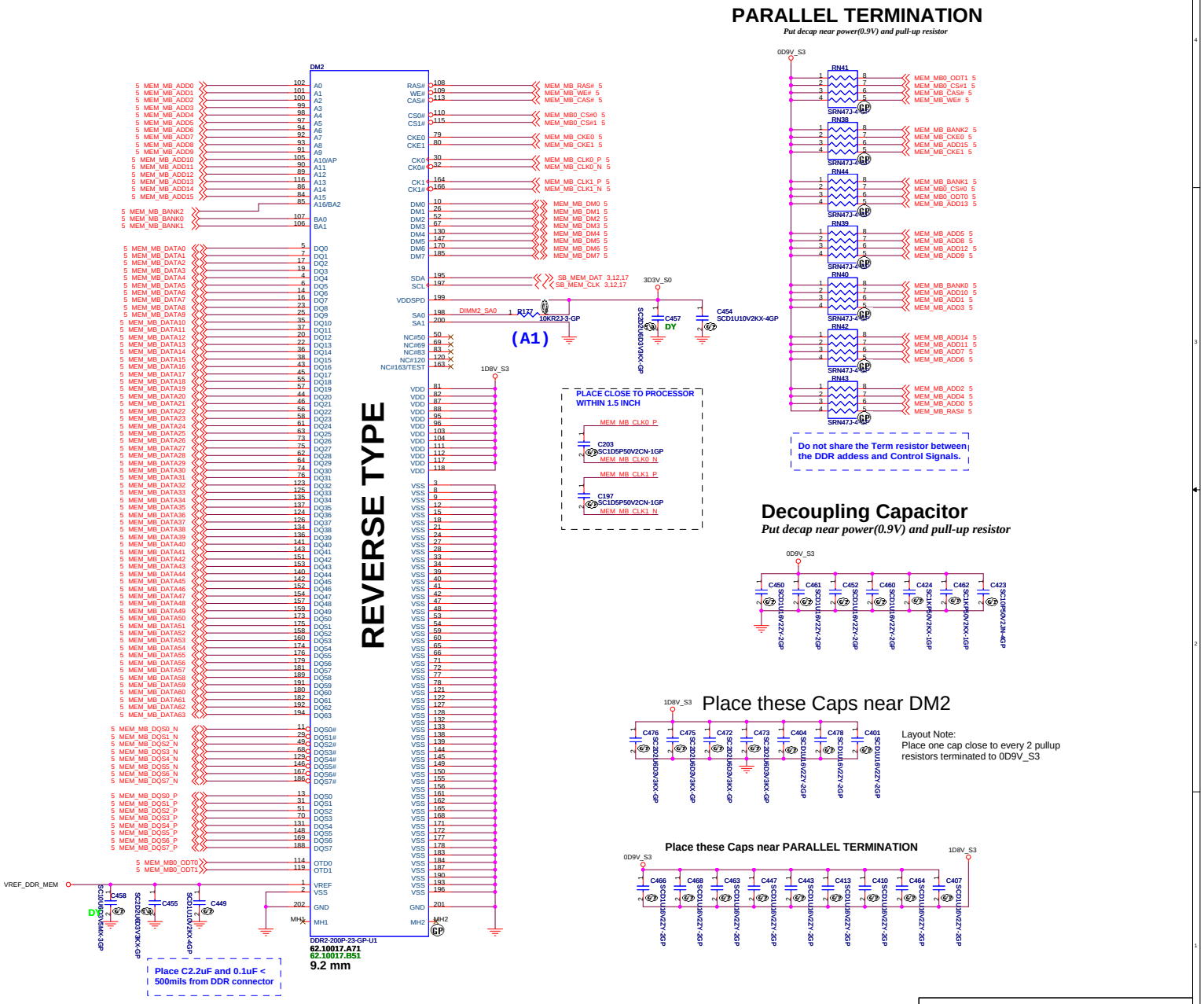
Date: Wednesday, February 25, 2009 | Sheet 15 of 59

DDR2 SOCKET_2 (9.2mm)



PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

Place these Caps near DM2

Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION

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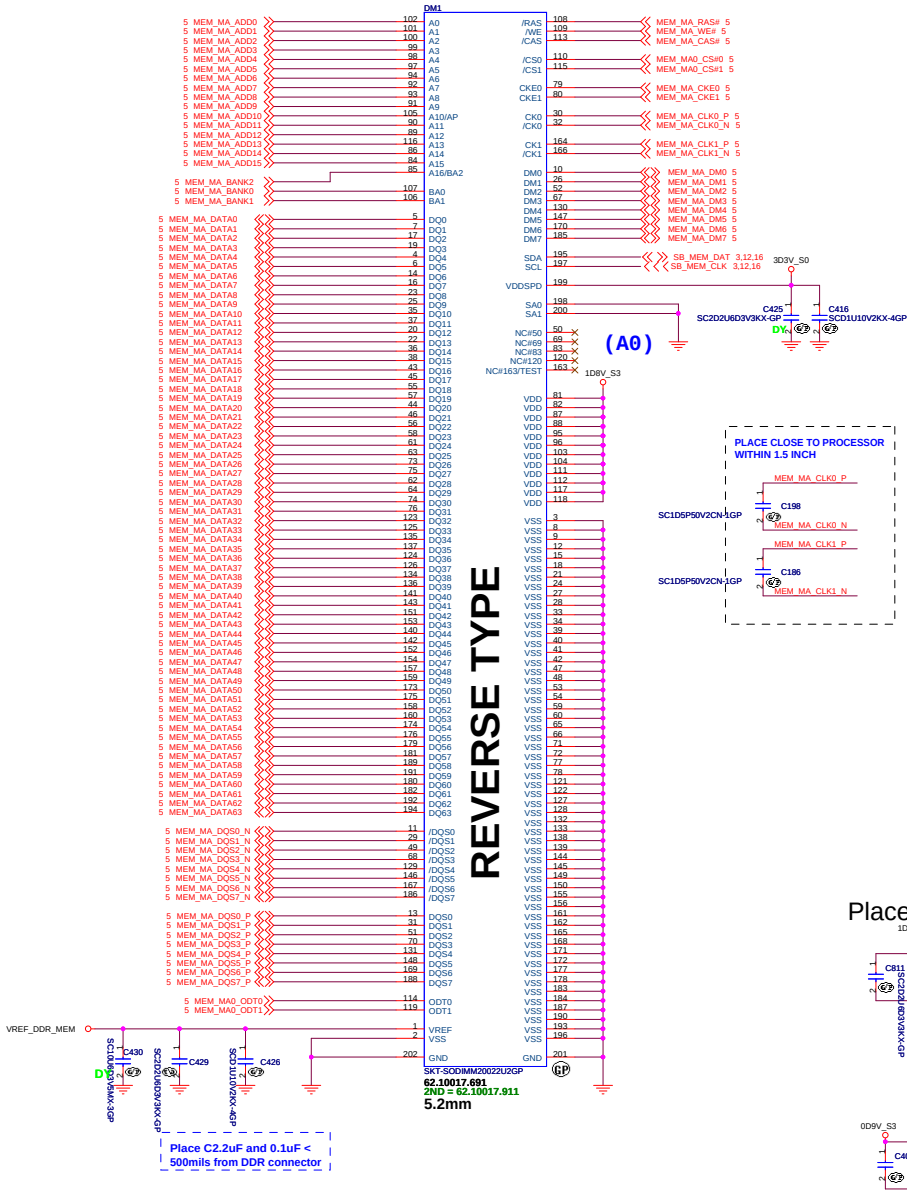
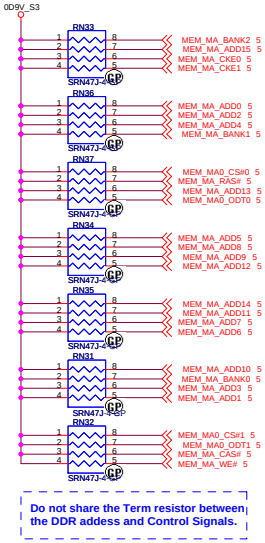
Title: DDR2 Socket_2		
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 16 of 59	

DDR2 SOCKET_1 (5.2mm)



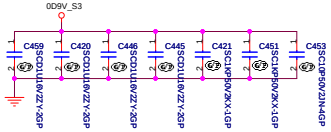
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

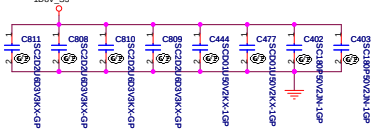


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

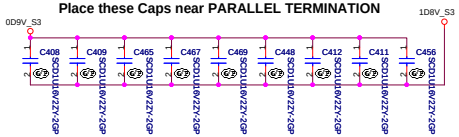


Place these Caps near DM2

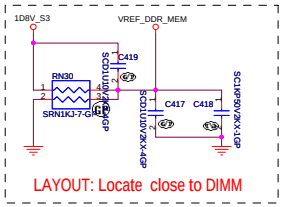


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION

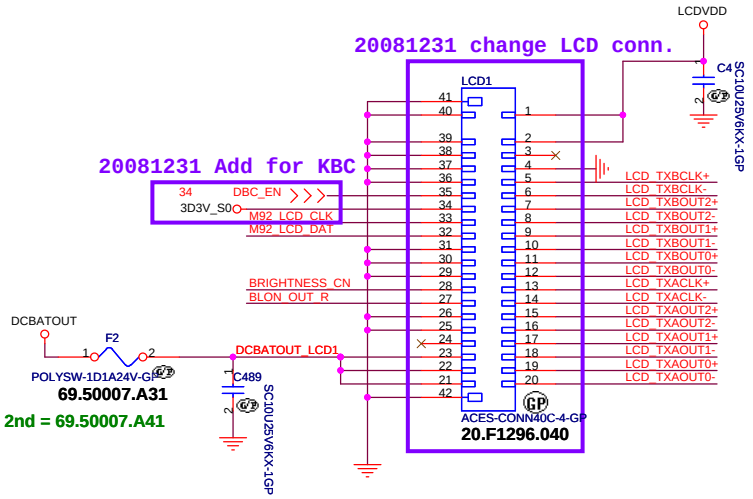


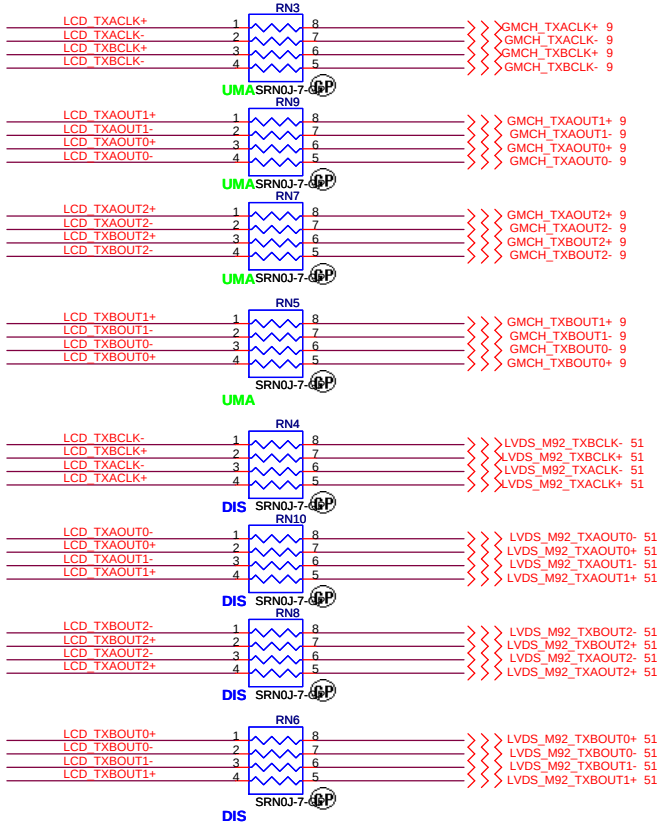
DDR_VREF

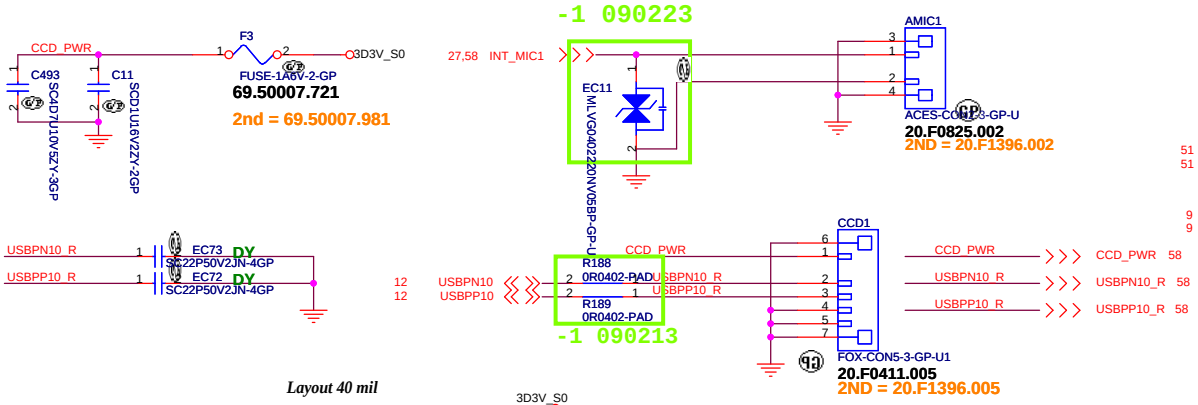


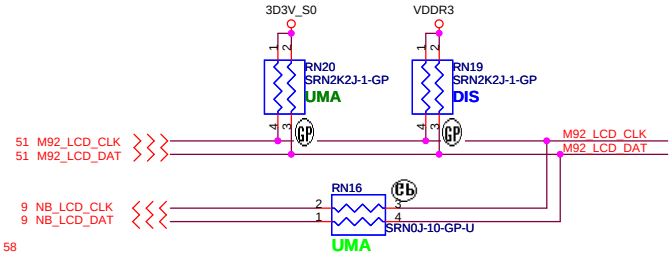
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR2 Socket_1		
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 17 of 59	

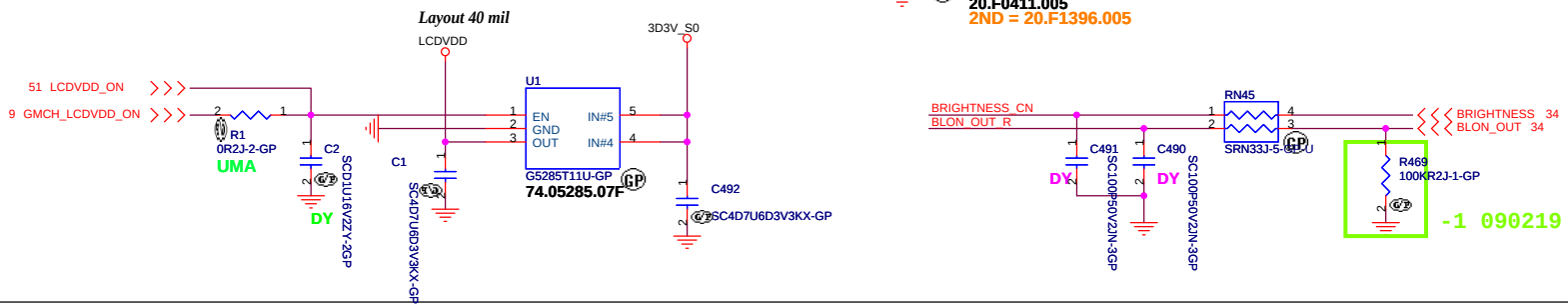
LCD/CCD CONN











SJV50

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Title: LED & LCD CONN / CCD

Size	Document Number	Rev
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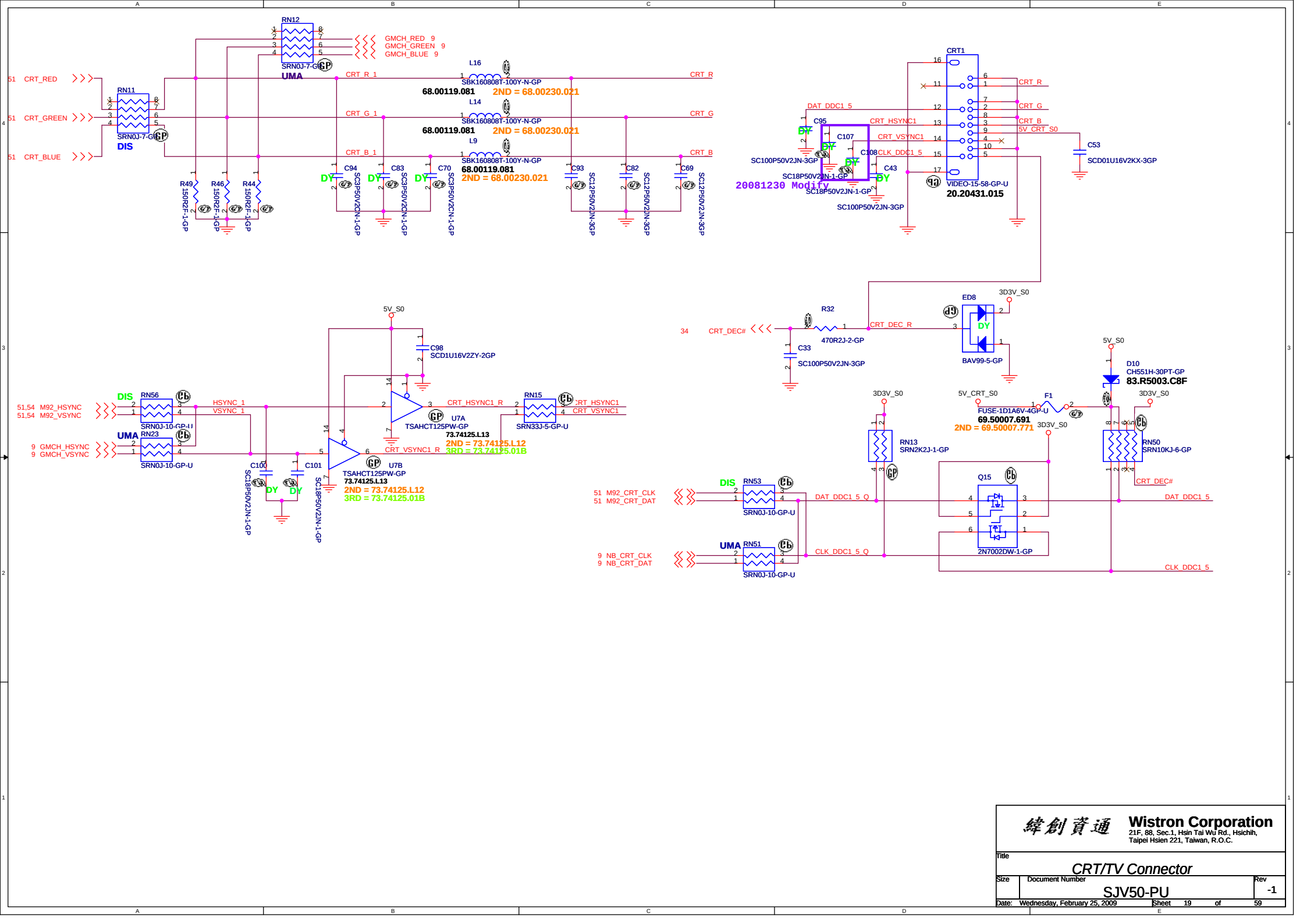

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	*CRT/TV Connector*	
Size	Document Number: SJV50-PU	Rev: -1
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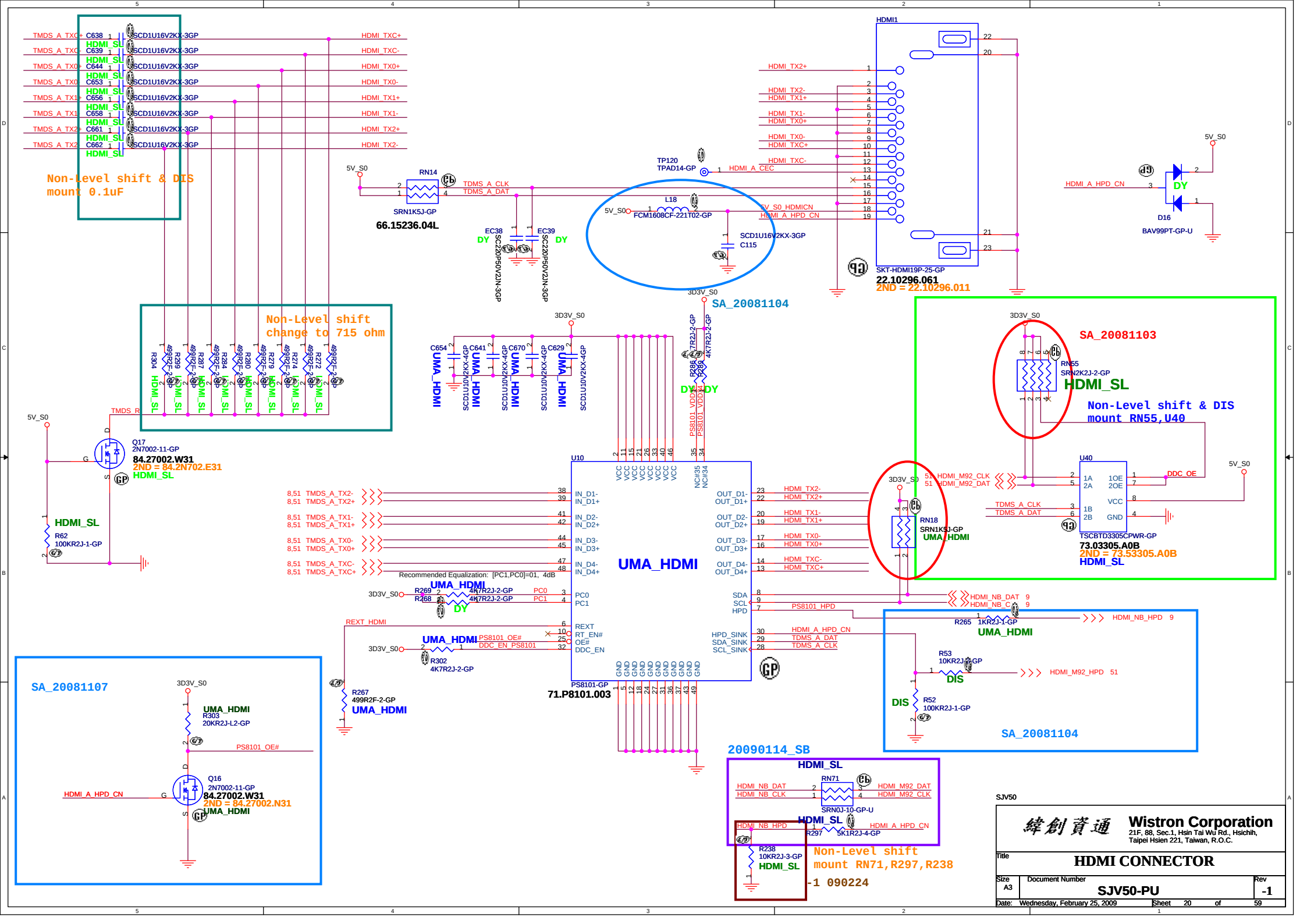
Non-Level shift & DIS mount 0.1uF
Non-Level shift change to 715 ohm
SA_20081104
SA_20081103
Non-Level shift & DIS mount RN55,U40
SA_20081107
20090114_SB
Non-Level shift mount RN71,R297,R238
HDMI CONNECTOR
Wistron Corporation
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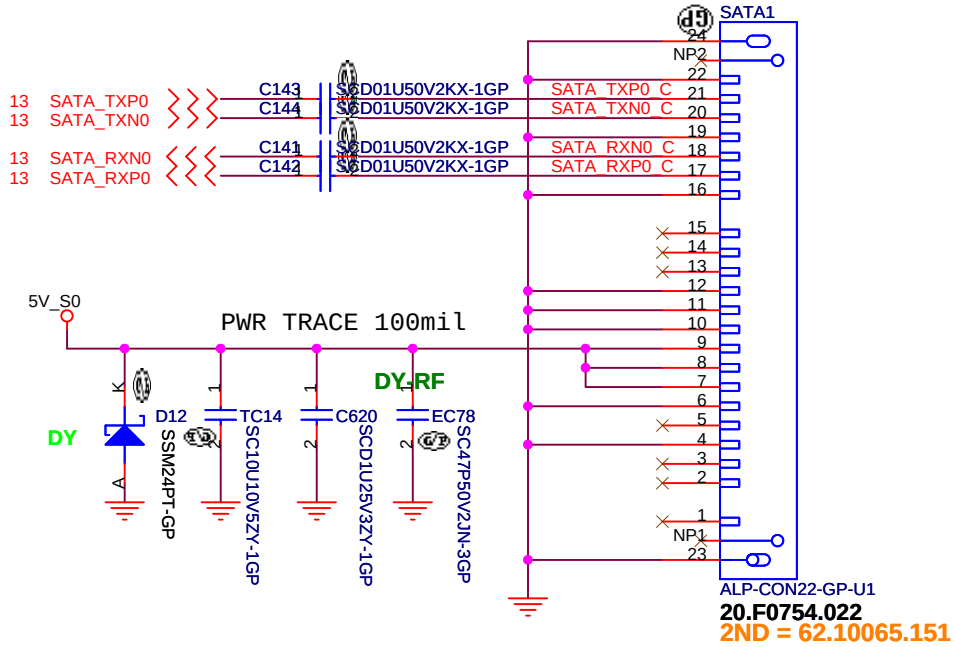
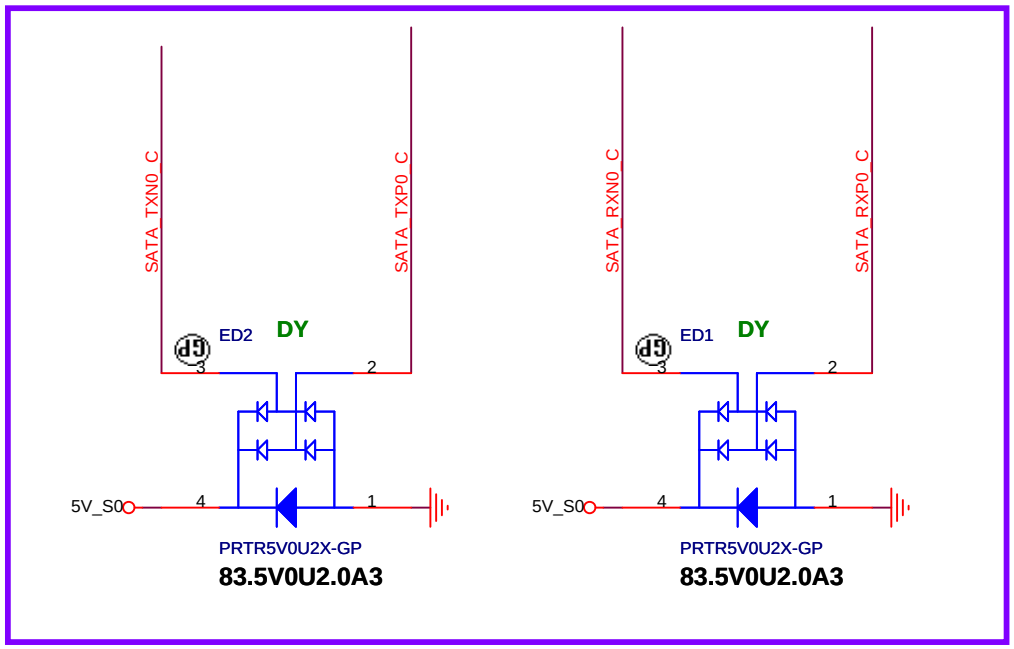
SATA HDD Connector





SA_20081112

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Title	***HDD***	
Size	Document Number **SJV50-PU**	Rev -1
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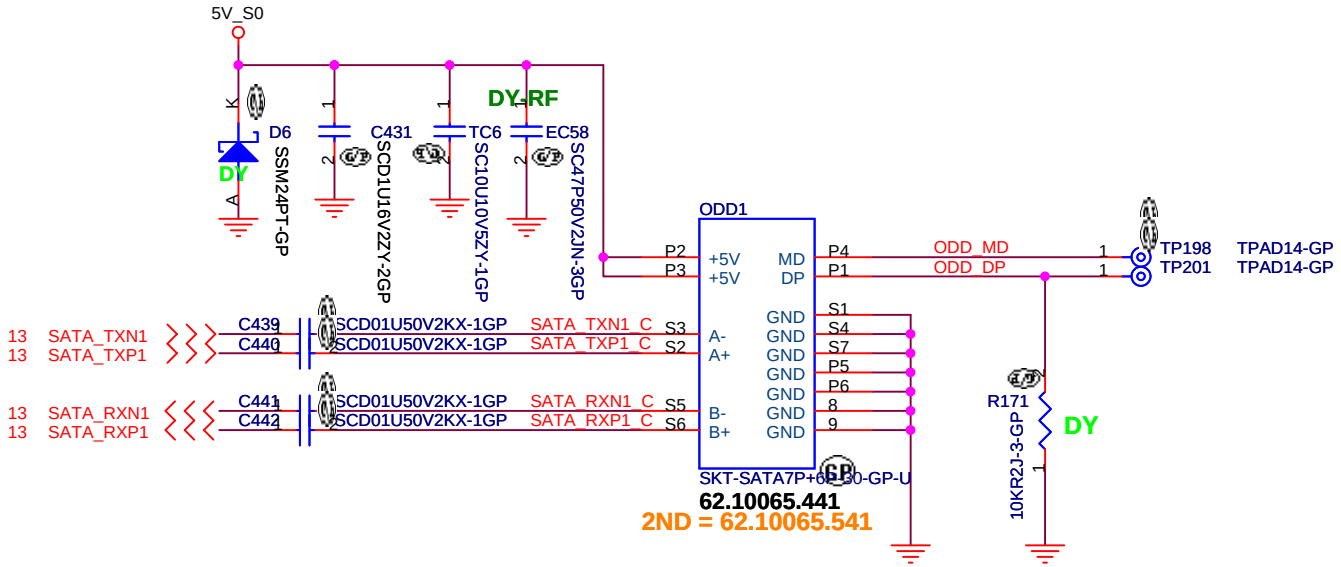
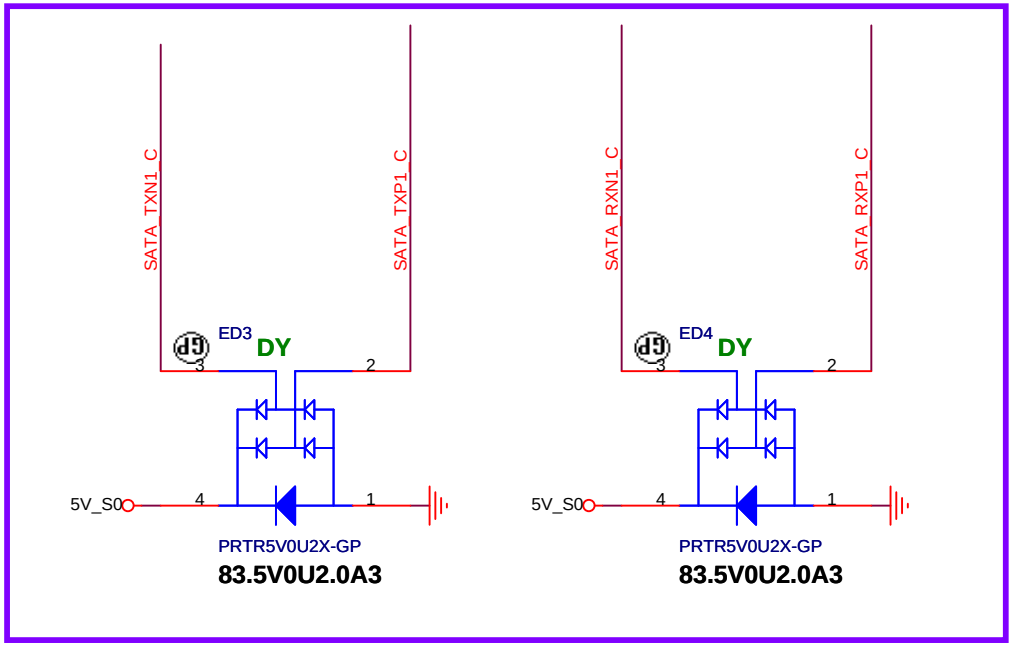
SATA ODD Connector





SA_20081112

SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ODD

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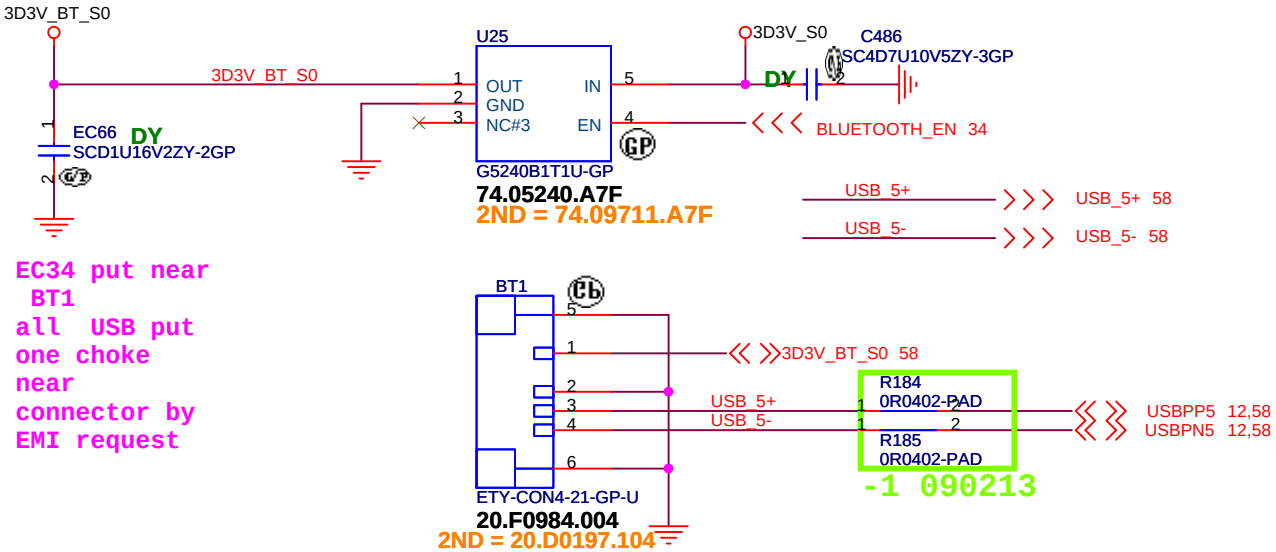
BLUETOOTH MODULE



SJV50

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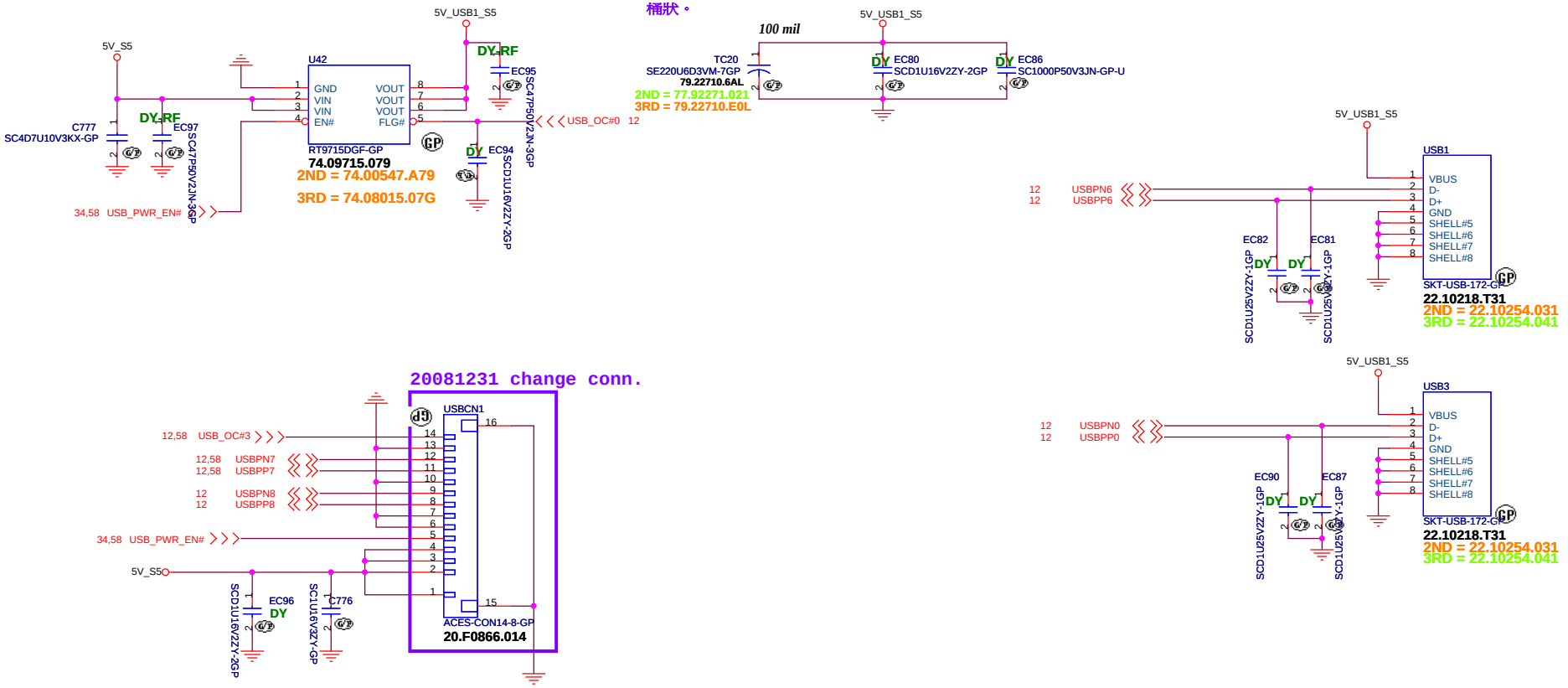
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BLUETOOTH***	
Size	Document Number **SJV50-PU**	Rev -1
Date: Wednesday, February 25, 2009	Sheet 23 of 59	



PD UMA

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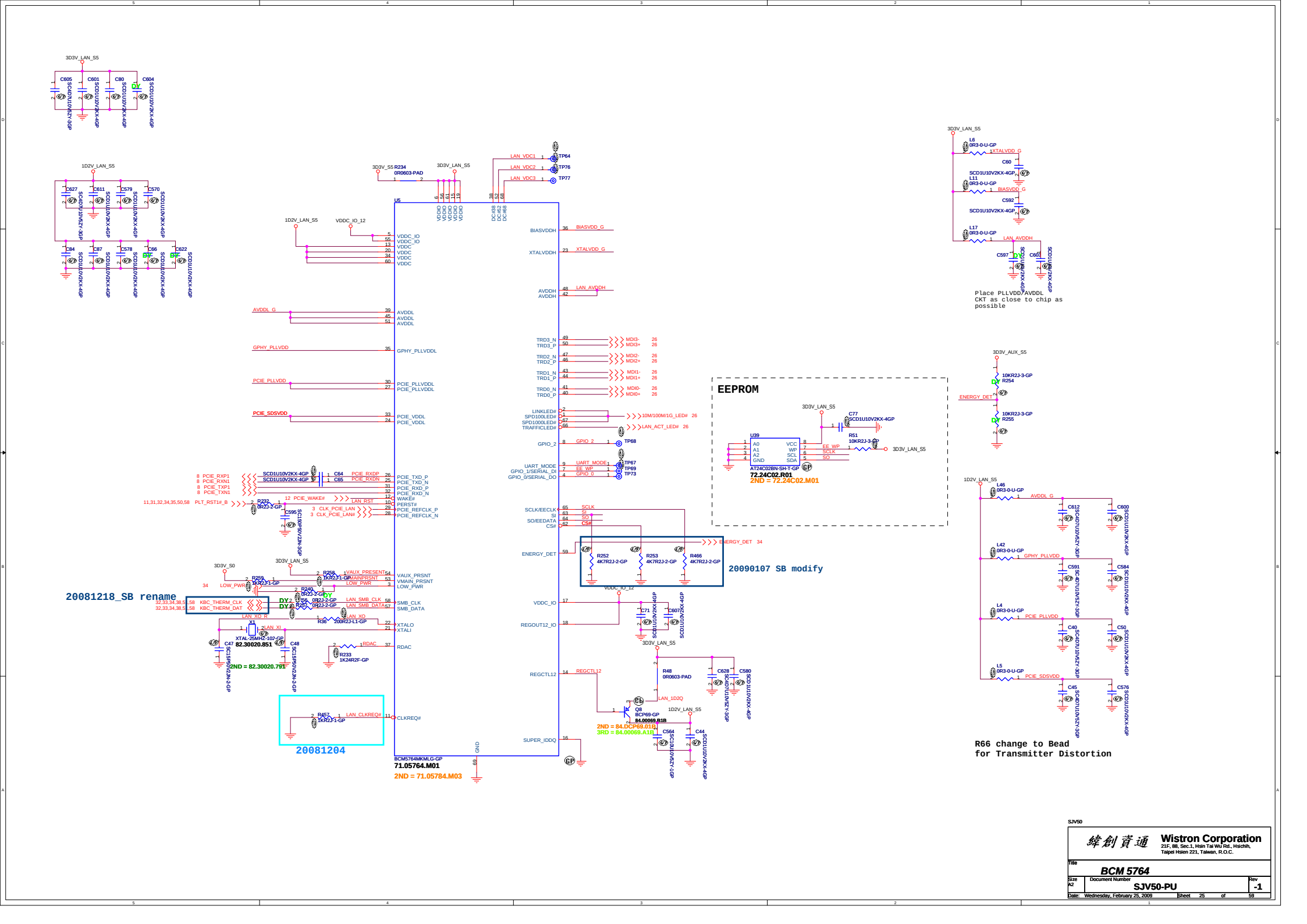
Title: *USB Connector*		
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 24 of 59	


3D3V_LAN_S5
1D2V_LAN_S5
3D3V_S5
3D3V_AUX_S5
3D3V_S0
U5
BCM5764MKMLG-GP
71.05764.M01
2ND = 71.05784.M03
EEPROM
U39
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
20081218_SB rename
20090107 SB modify
20081204
Place PLLVDD/AVDDL CKT as close to chip as possible
R66 change to Bead for Transmitter Distortion
2ND = 82.30020.781
2ND = 84.DCP69.01G
3RD = 84.00069.A1G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
BCM 5764
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Wednesday, February 25, 2009
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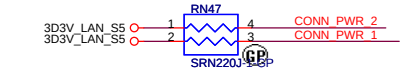
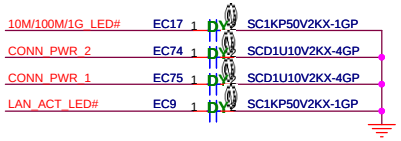
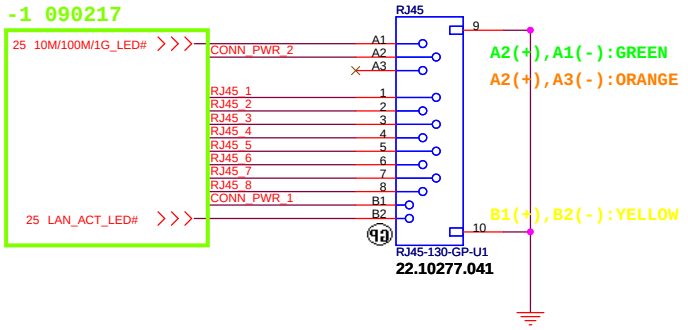
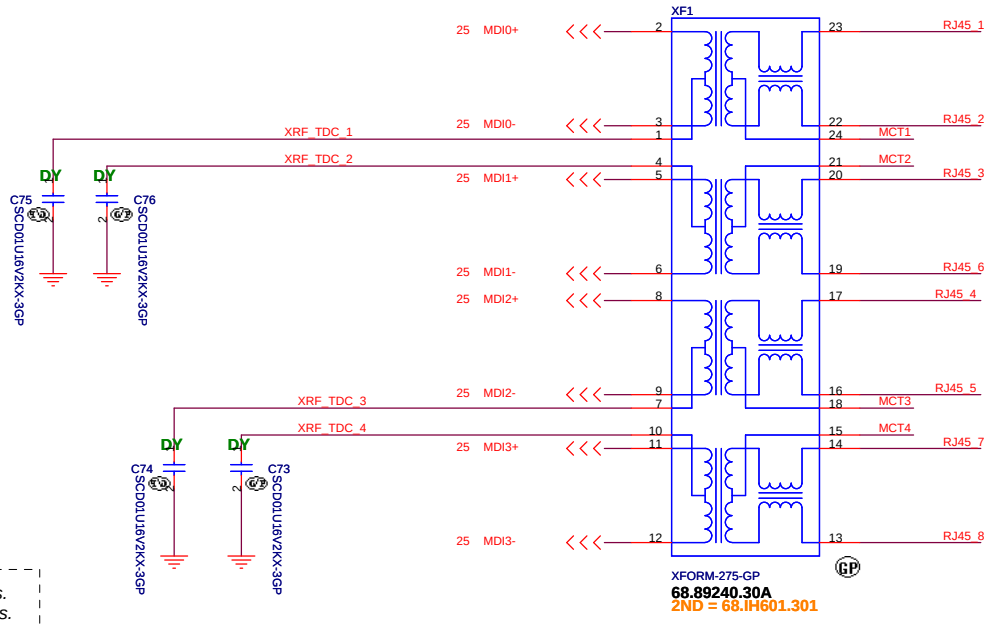
LAN Connector



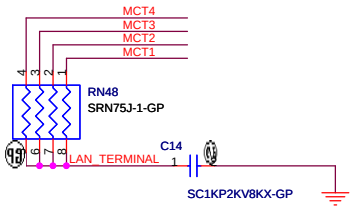




GIGA Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector

Size	Document Number	Rev
A3	SJV50-PU	-1

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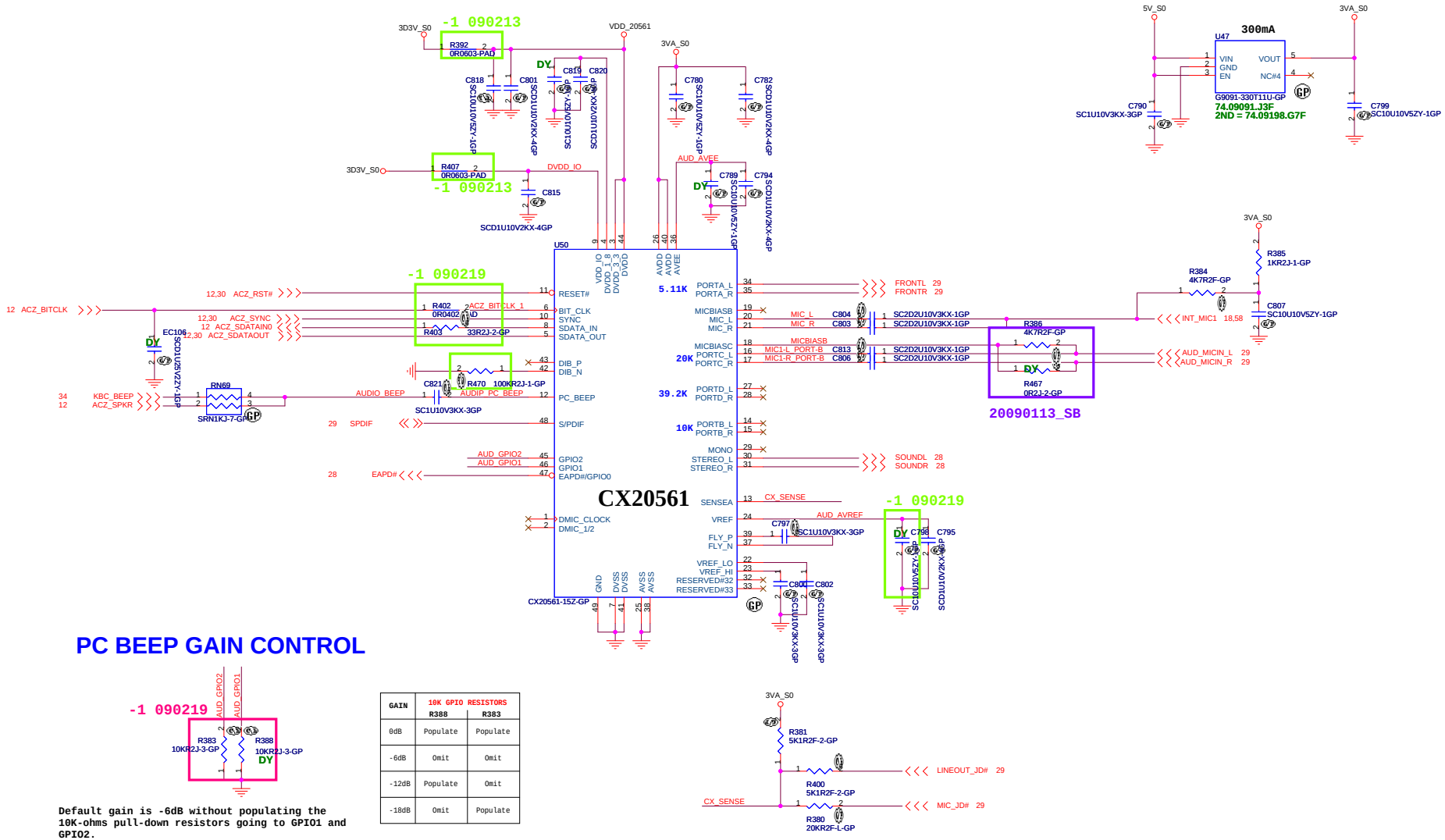

SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: AZALIA CODEC - CX20561

Size	Document Number	Rev
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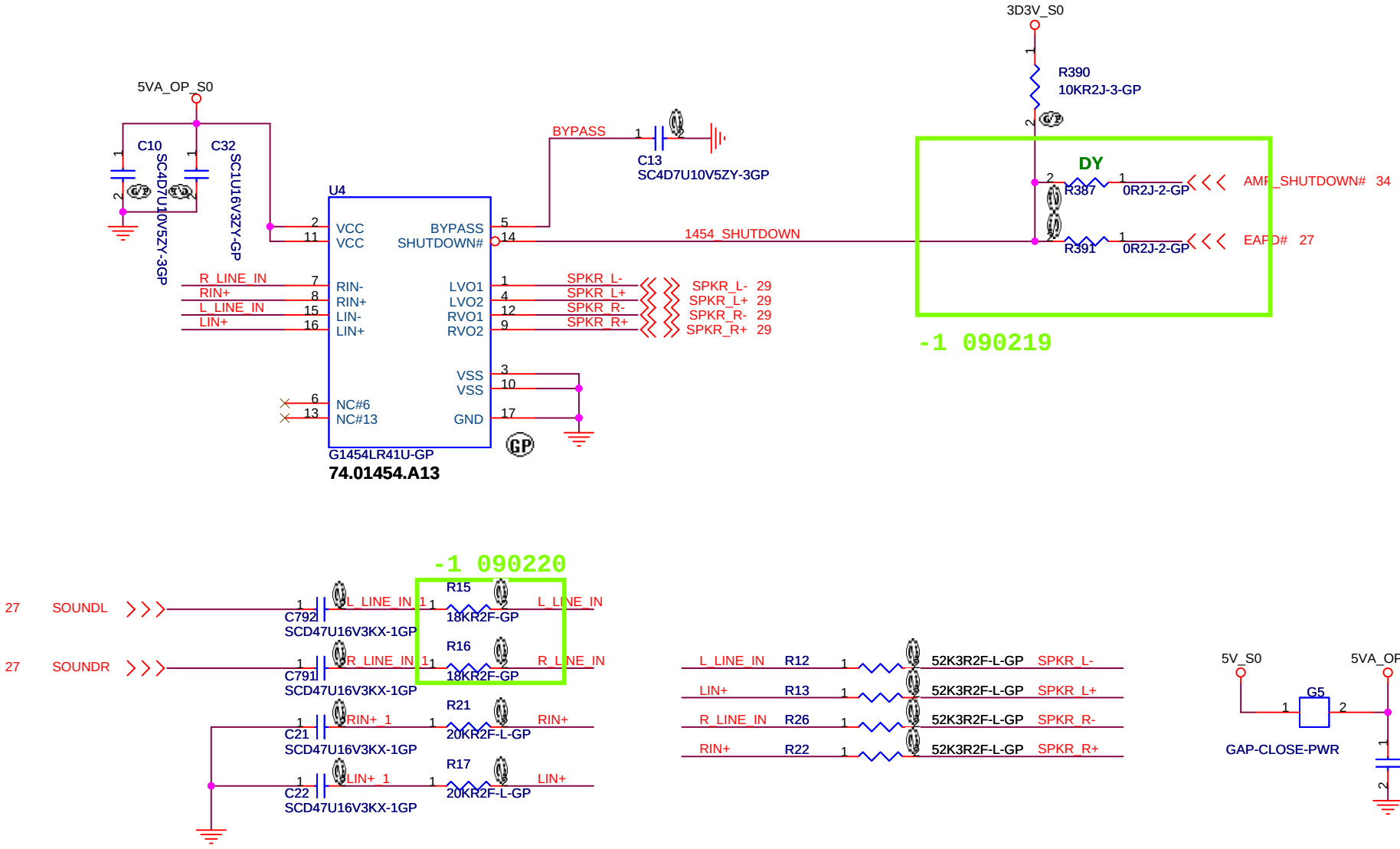
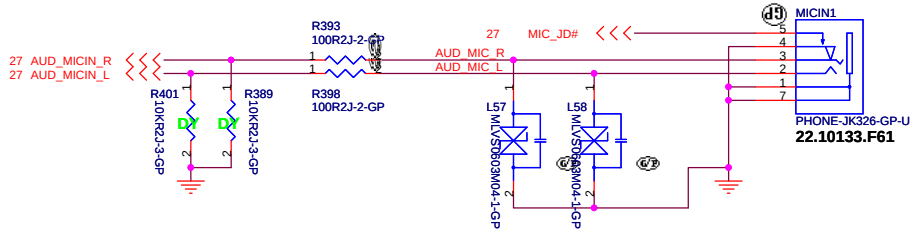
AUDIO OP AMPLIFIER



PD UMA

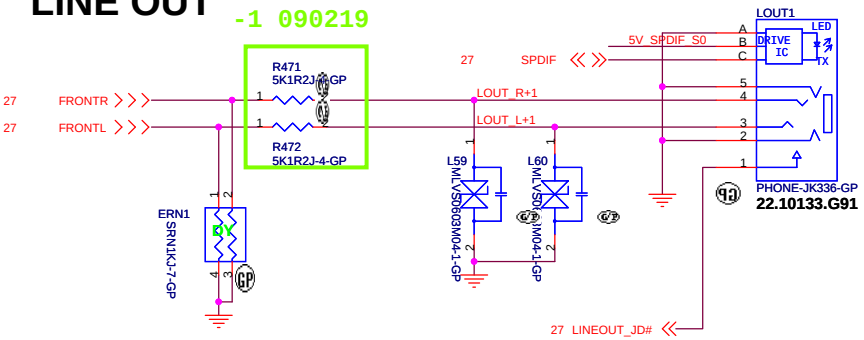
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO AMP (G1454)		
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 28 of 59	

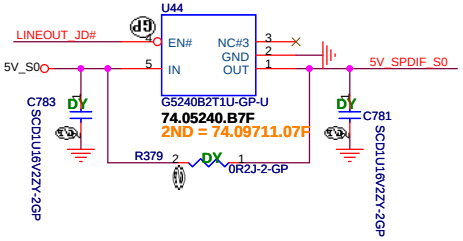
MIC IN



LINE OUT

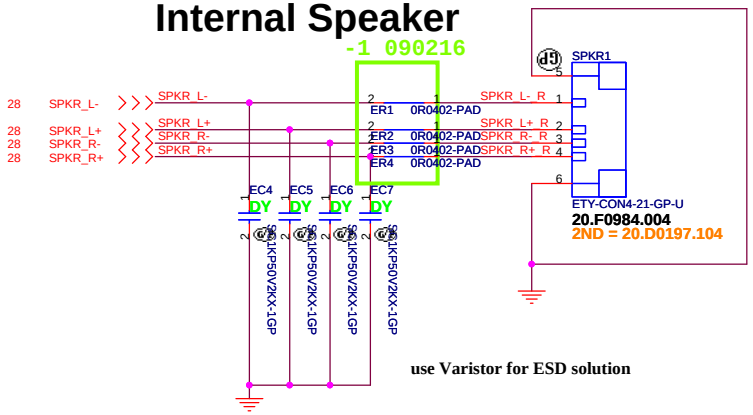
-1 090219





Internal Speaker

-1 090216



use Varistor for ESD solution

SPKR_L-_R 58
SPKR_L+_R 58
SPKR_R-_R 58
SPKR_R+_R 58

SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

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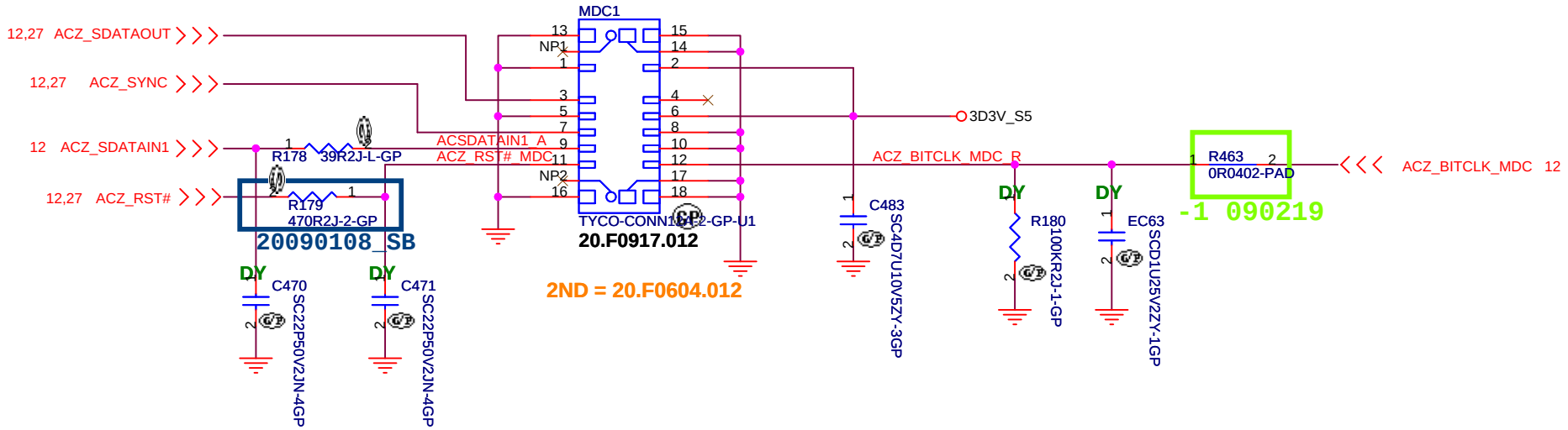
MDC 1.5 CONN



SJV50

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB Connector*

Size	Document Number	Rev
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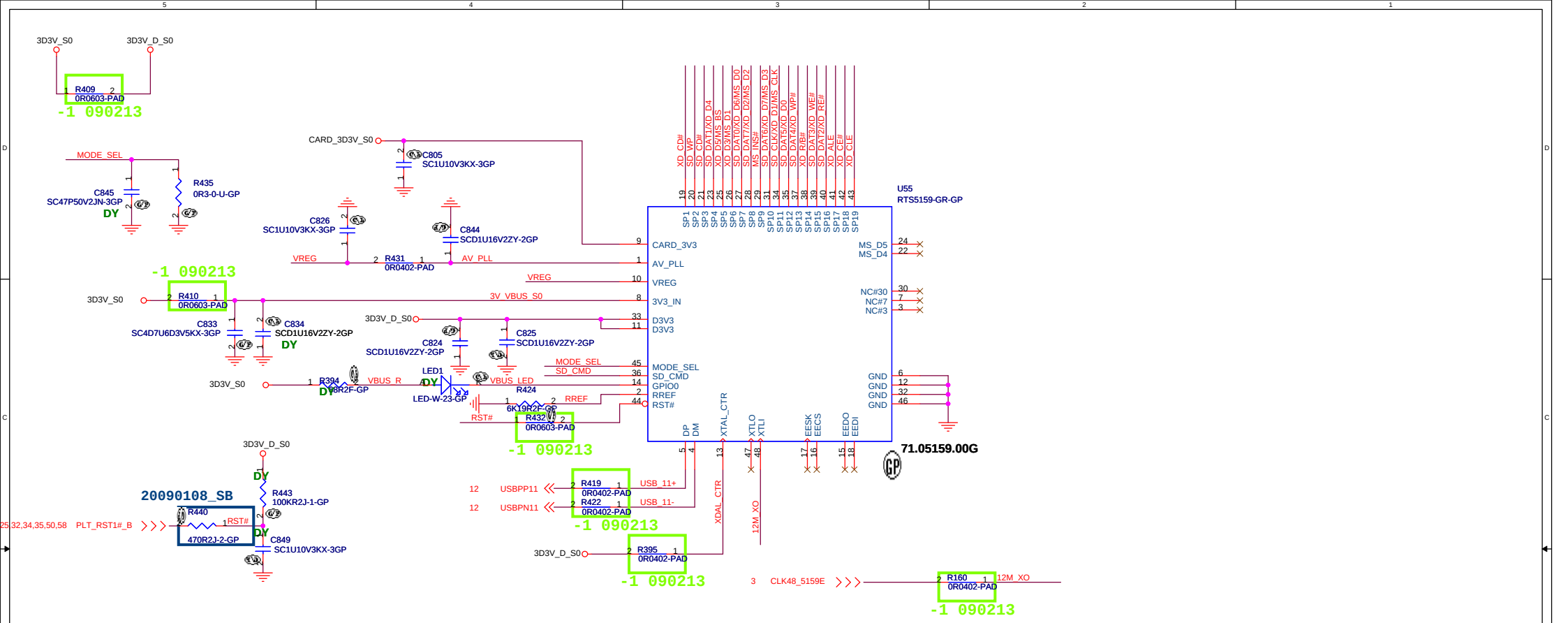

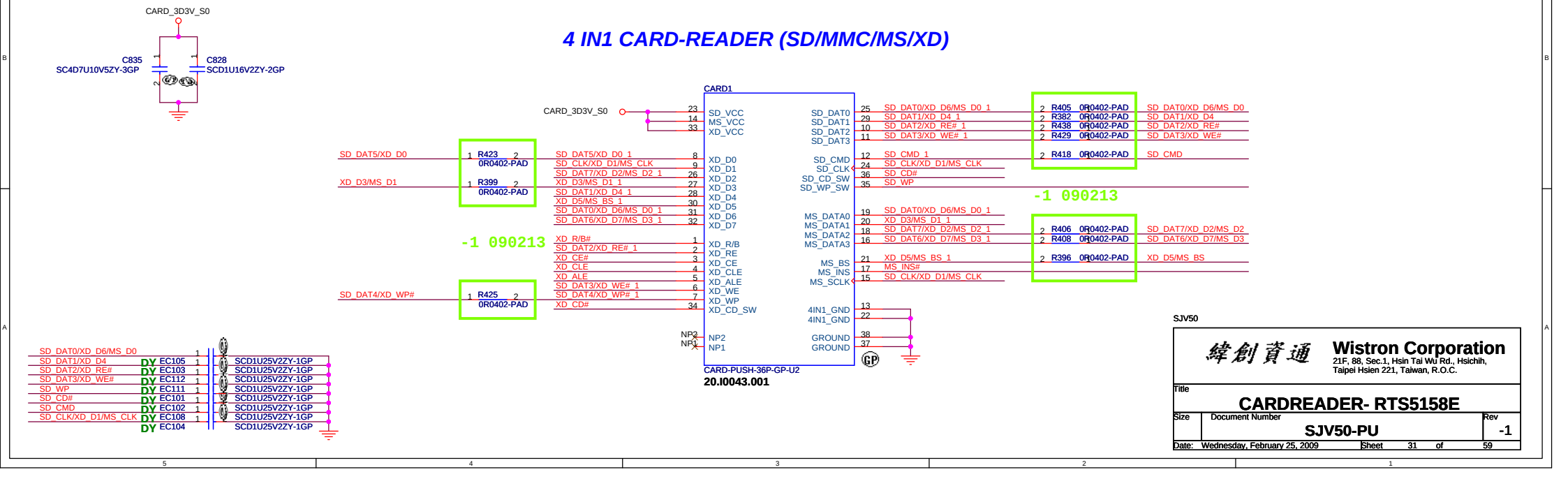

SJV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARDREADER- RTS5158E**

Size	Document Number	Rev
	SJV50-PU	-1

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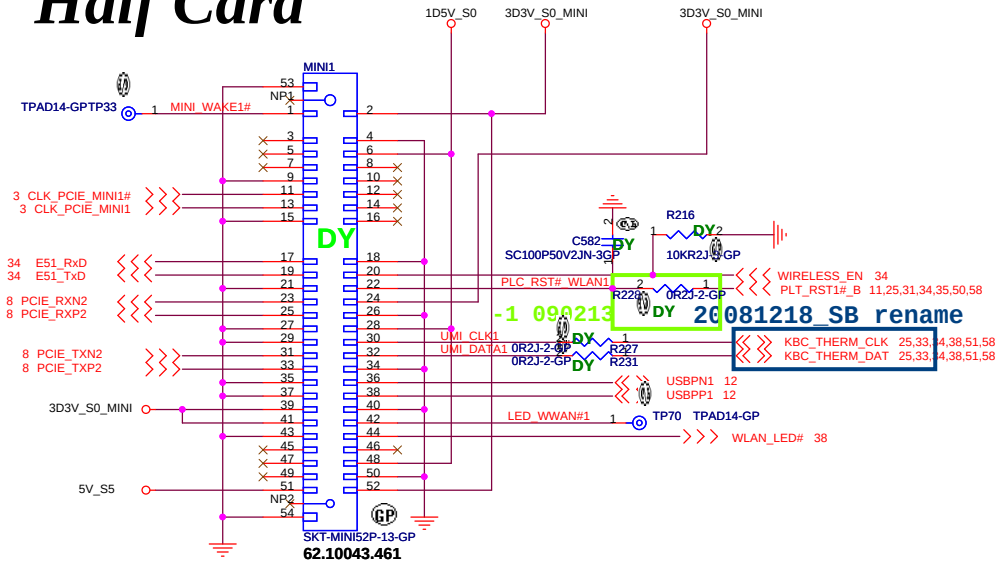
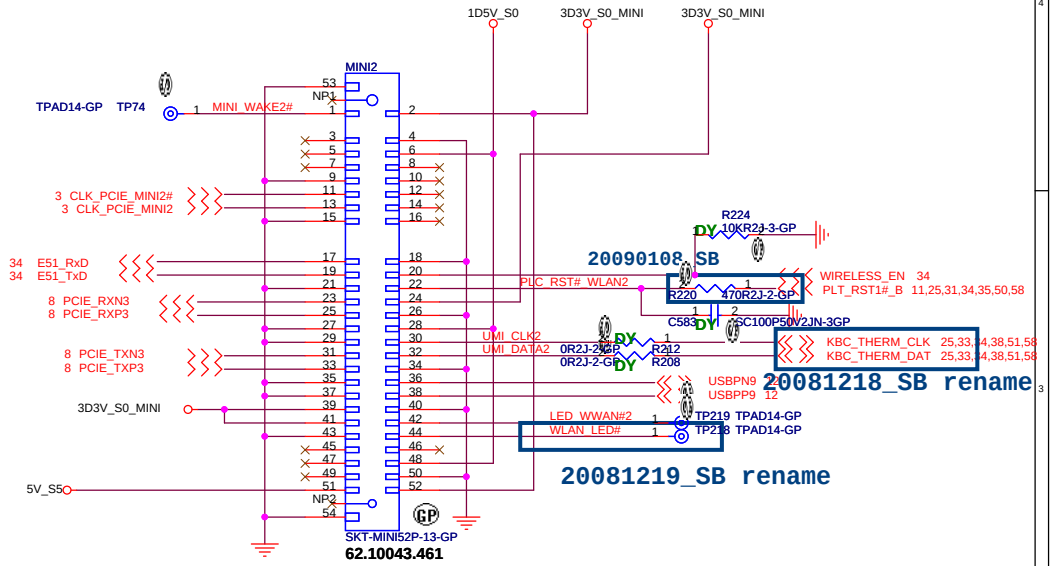
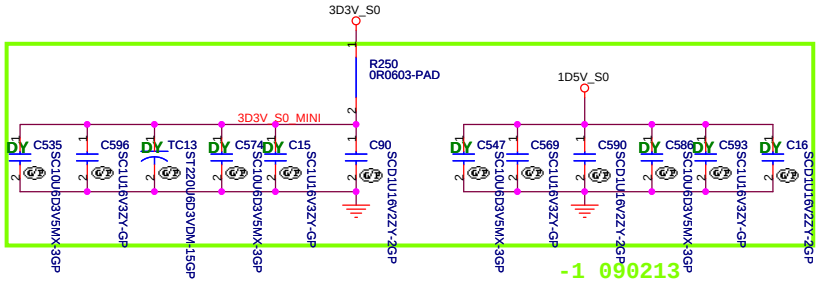
Mini Card Connector

Half Card

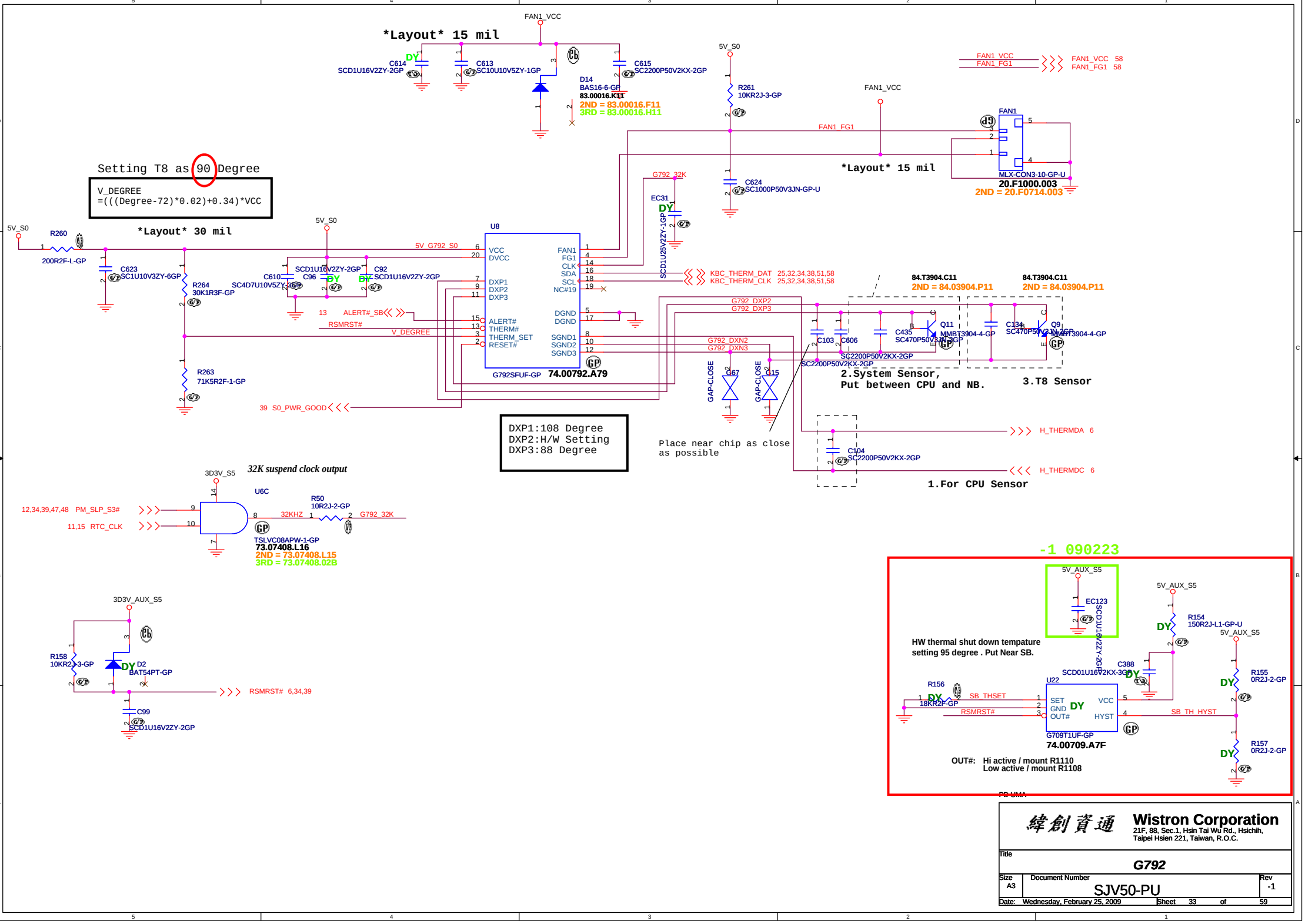


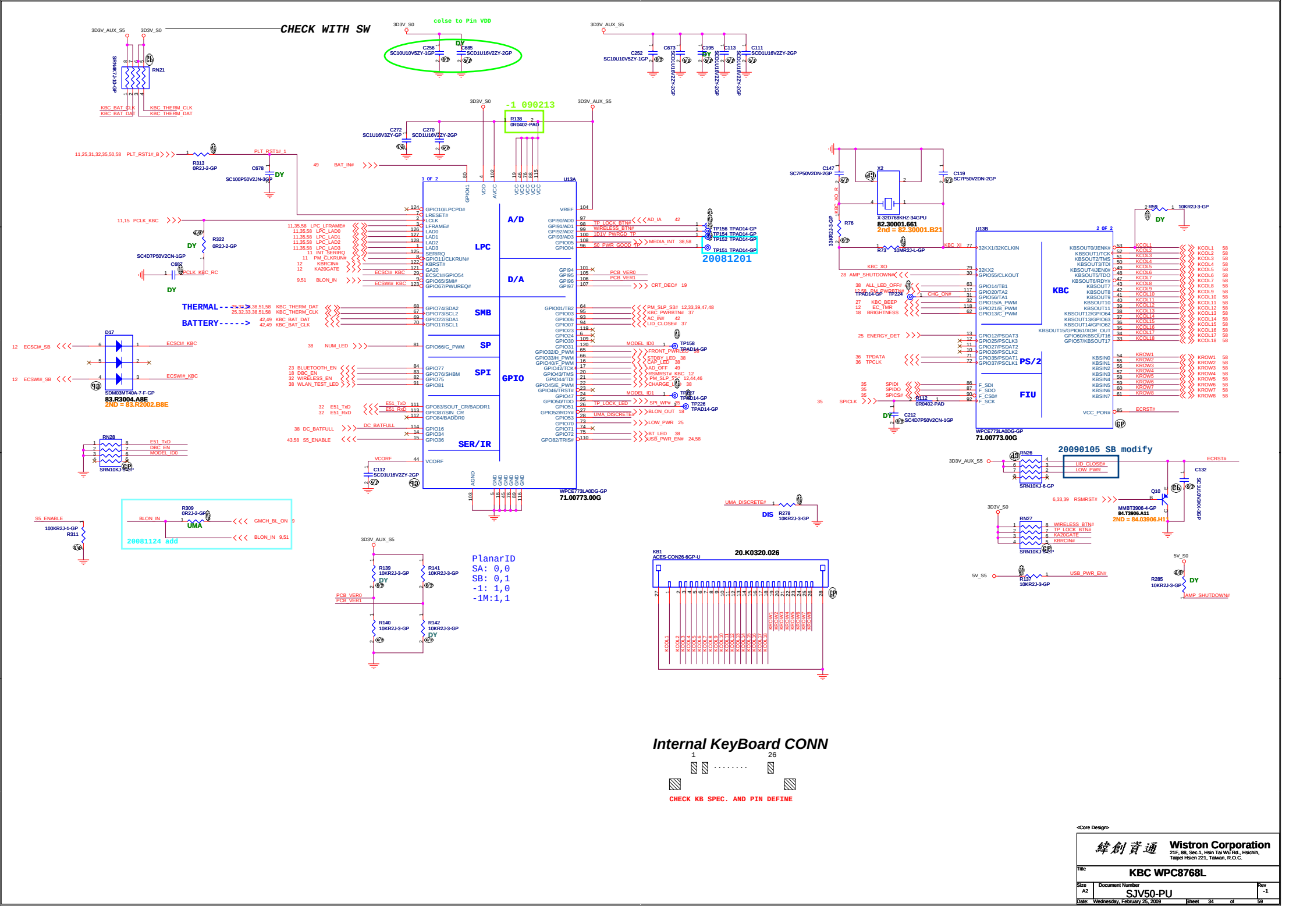




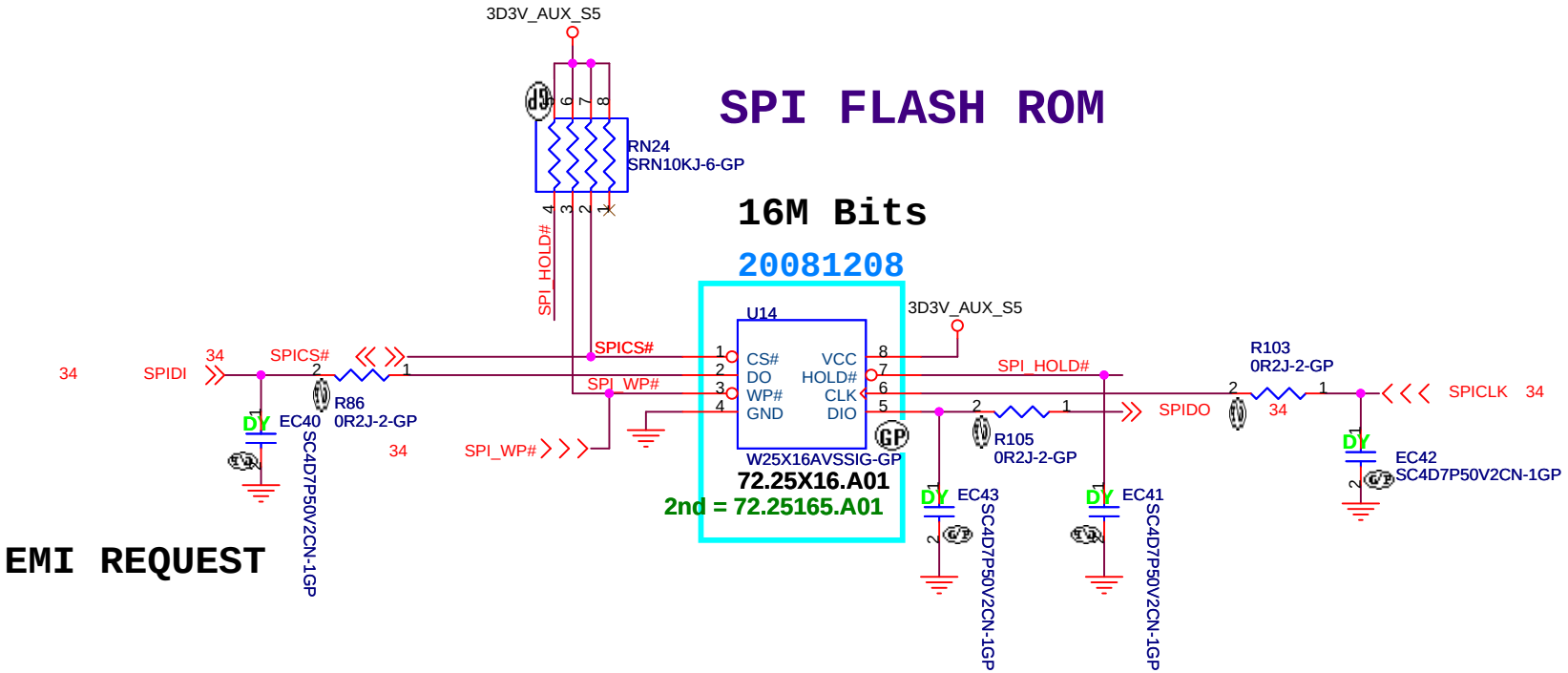
SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 32 of 59	


Layout 15 mil
FAN1_VCC
C614 SCD1U16V2ZY-2GP
C613 SC10U10V5ZY-1GP
C615 SC2200P50V2KX-2GP
D14 BAS16-6-GP
83.00016.K11
2ND = 83.00016.F11
3RD = 83.00016.H11
5V_S0
R261 10KR2J-3-GP
FAN1_VCC 58
FAN1_FG1 58
FAN1_FG1
FAN1
MLX-CON3-10-GP-U
20.F1000.003
2ND = 20.F0714.003
Layout 15 mil
C624 SC1000P50V3JN-GP-U
Setting T8 as 90 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
Layout 30 mil
5V_S0
R260 200R2F-L-GP
C623 SC1U10V3ZY-6GP
R264 30K1R3F-GP
R263 71K5R2F-1-GP
C610 SCD1U16V2ZY-2GP
C96 SC4D7U10V5ZY-1GP
C92 SCD1U16V2ZY-2GP
5V_G792_S0
U8
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
74.00792.A79
G792_32K
EC31 SCD1U25V2ZY-1GP
KBC_THERM_DAT 25,32,34,38,51,58
KBC_THERM_CLK 25,32,34,38,51,58
13 ALERT#_SB
RSMRST#
V_DEGREE
39 S0_PWR_GOOD
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
GAP-CLOSE
G67
GAP-CLOSE
C15
84.T3904.C11
2ND = 84.03904.P11
Q11 MMBT3904-4-GP
C435 SC470P50V3JN-2GP
84.T3904.C11
2ND = 84.03904.P11
C134 SC470P50V3JN-2GP
Q9 MMBT3904-4-GP
C103 C606 SC2200P50V2KX-2GP
2.System Sensor,
Put between CPU and NB.
3.T8 Sensor
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
H_THERMDA 6
C104 SC2200P50V2KX-2GP
H_THERMDC 6
1.For CPU Sensor
3D3V_S5
32K suspend clock output
U6C
R50 10R2J-2-GP
12,34,39,47,48 PM_SLP_S3#
11,15 RTC_CLK
32KHZ
G792_32K
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
3D3V_AUX_S5
R158 10KR2J-3-GP
D2 BAT54PT-GP
RSMRST# 6,34,39
C99 SCD1U16V2ZY-2GP
-1 090223
5V_AUX_S5
EC123 SCD01U16V2KX-3GP
HW thermal shut down tempature setting 95 degree . Put Near SB.
R156 18KR2F-GP
SB_THSET
RSMRST#
U22
SET
GND
OUT#
VCC
HYST
G709T1UF-GP
74.00709.A7F
SB_TH_HYST
R154 150R2J-L1-GP-U
C388 SCD01U16V2KX-3GP
R155 0R2J-2-GP
R157 0R2J-2-GP
OUT#: Hi active / mount R1110
Low active / mount R1108
PB UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size A3
Document Number
SJV50-PU
Rev -1
Date: Wednesday, February 25, 2009
Sheet 33 of 59


CHECK WITH SW
colse to Pin VDD
-1 090213
20081201
THERMAL-------->
BATTERY------->
83.R3004.A8E
2ND = 83.R2002.B8E
82.30001.661
2nd = 82.30001.B21
71.00773.00G
20090105 SB modify
20081124 add
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M:1,1
20.K0320.026
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
Wistron Corporation
KBC WPC8768L
SJV50-PU

SPI FLASH ROM



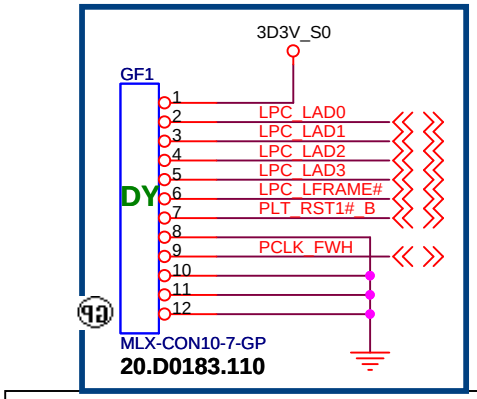
16M Bits

20081208

EMI REQUEST

Connector FOR DEBUG BOARD

20081219



LPC_LAD0 11,34,58
LPC_LAD1 11,34,58
LPC_LAD2 11,34,58
LPC_LAD3 11,34,58
LPC_LFRAME# 11,34,58
PLT_RST1#_B 11,25,31,32,34,50,58

PCLK_FWH 11,15,58

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size: A4	Document Number: SJV50-PU	Rev: -1
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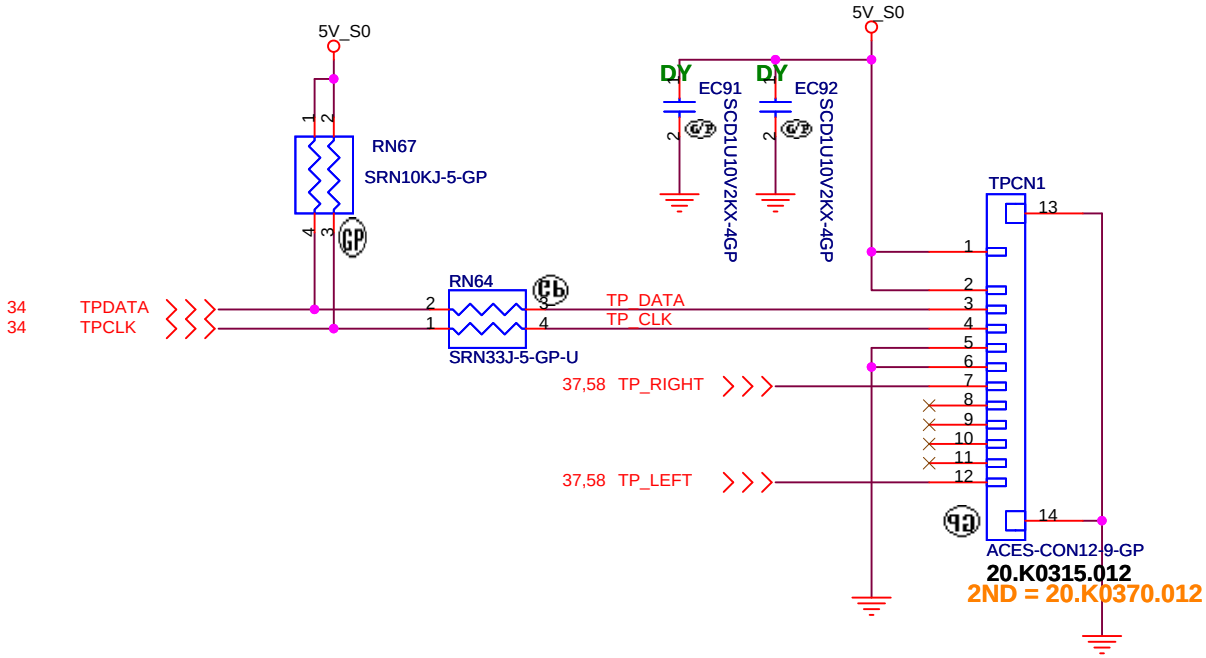
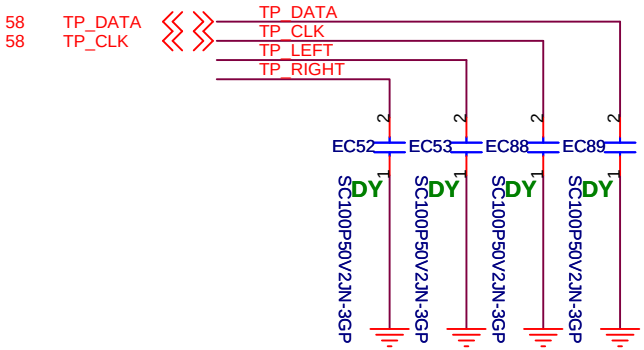
TOUCH PAD





1 12

T/P

SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **TouchPad**

Size	Document Number	Rev
	SJV50-PU	-1

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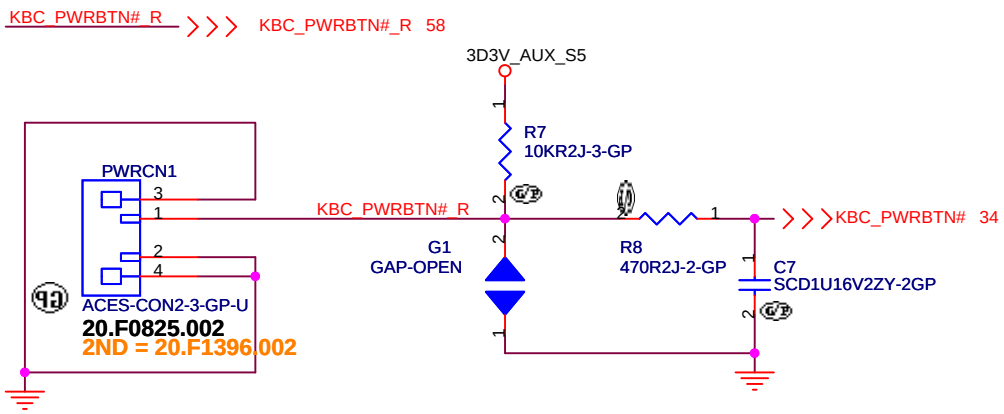
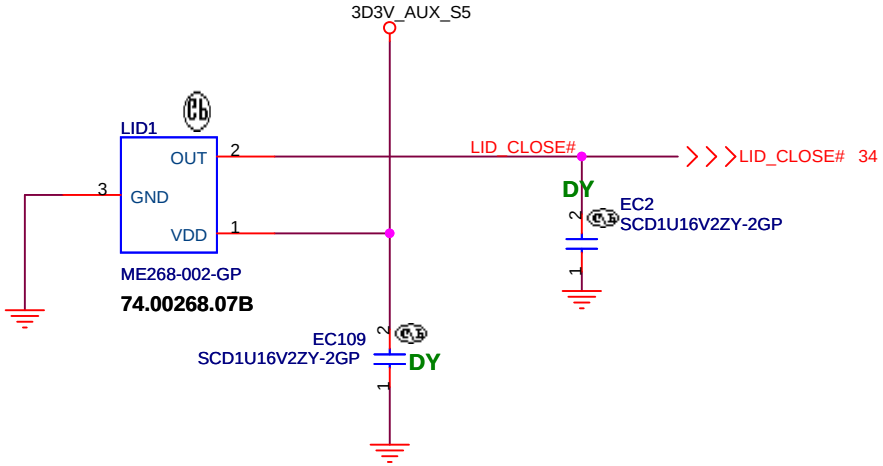
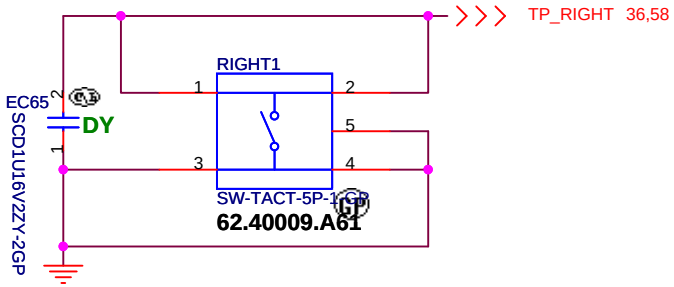
Power Button Board



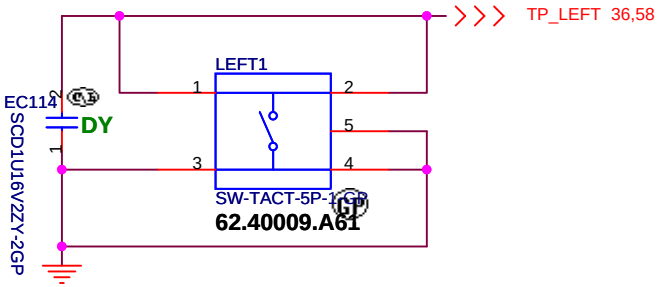
Cover Up Switch



RIGHT



LEFT



SJV50

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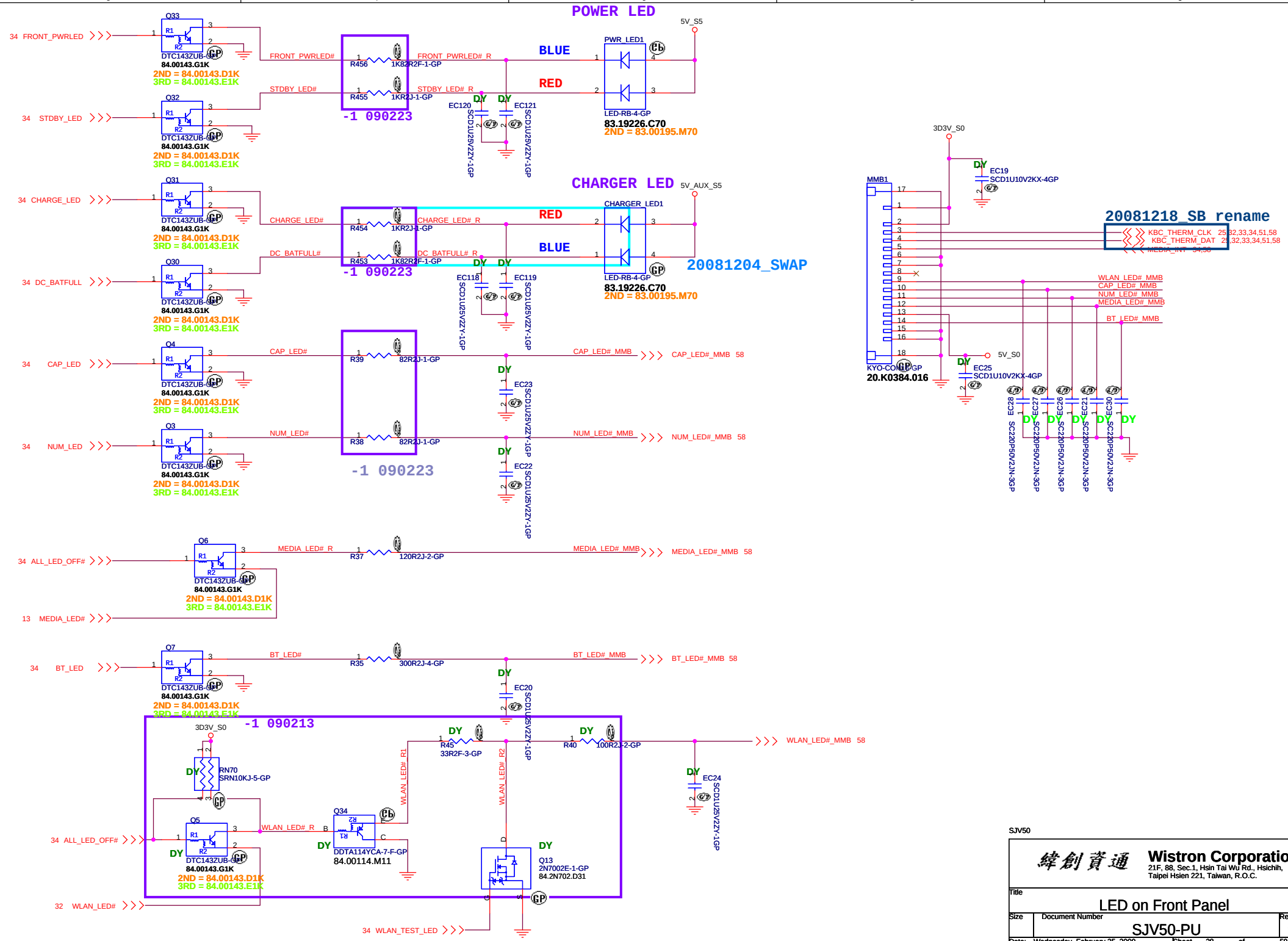
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Switchs*		
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 37 of 59	



SJV50

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Title: LED on Front Panel

Size	Document Number	Rev
	SJV50-PU	-1

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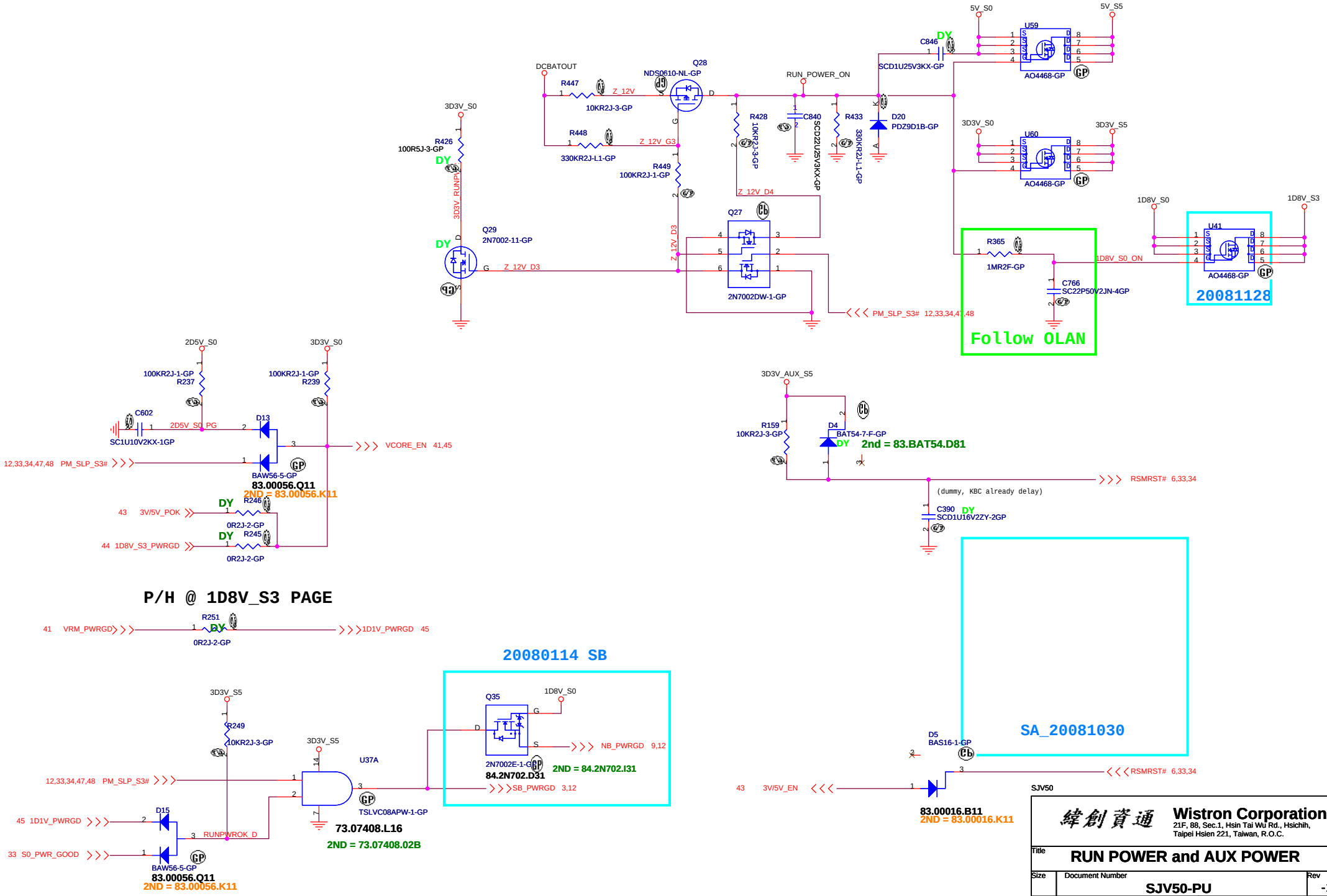
Run Power



SJV50

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Title	RUN POWER and AUX POWER	
Size	Document Number	Rev
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CPU_CORE
ISL6264

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51125
3D3V/5V

DCBATOUT_51120

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

1D5V_S0

3D3V_S0 → INPUT / OUT → 1D5V_S0

G957

1D2V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

G9091

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

G9091

0D9V_S3

5V_S5 → INPUT / OUT → 0D9V_S3

RT9026

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Output Signal
(O)

AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD+

Charger_MAX8731

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

AD+

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

Input Power
DCIN (I)

TI TPS51124
1.8V / 1.2V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
DCBATOUT
5V_S5
VCC(I)
VCC(I)

Output Power
VCC(O)
VCC(O)

1.8V_S3
1.2V_S0

SJV50

緯創資通 Wistron Corporation
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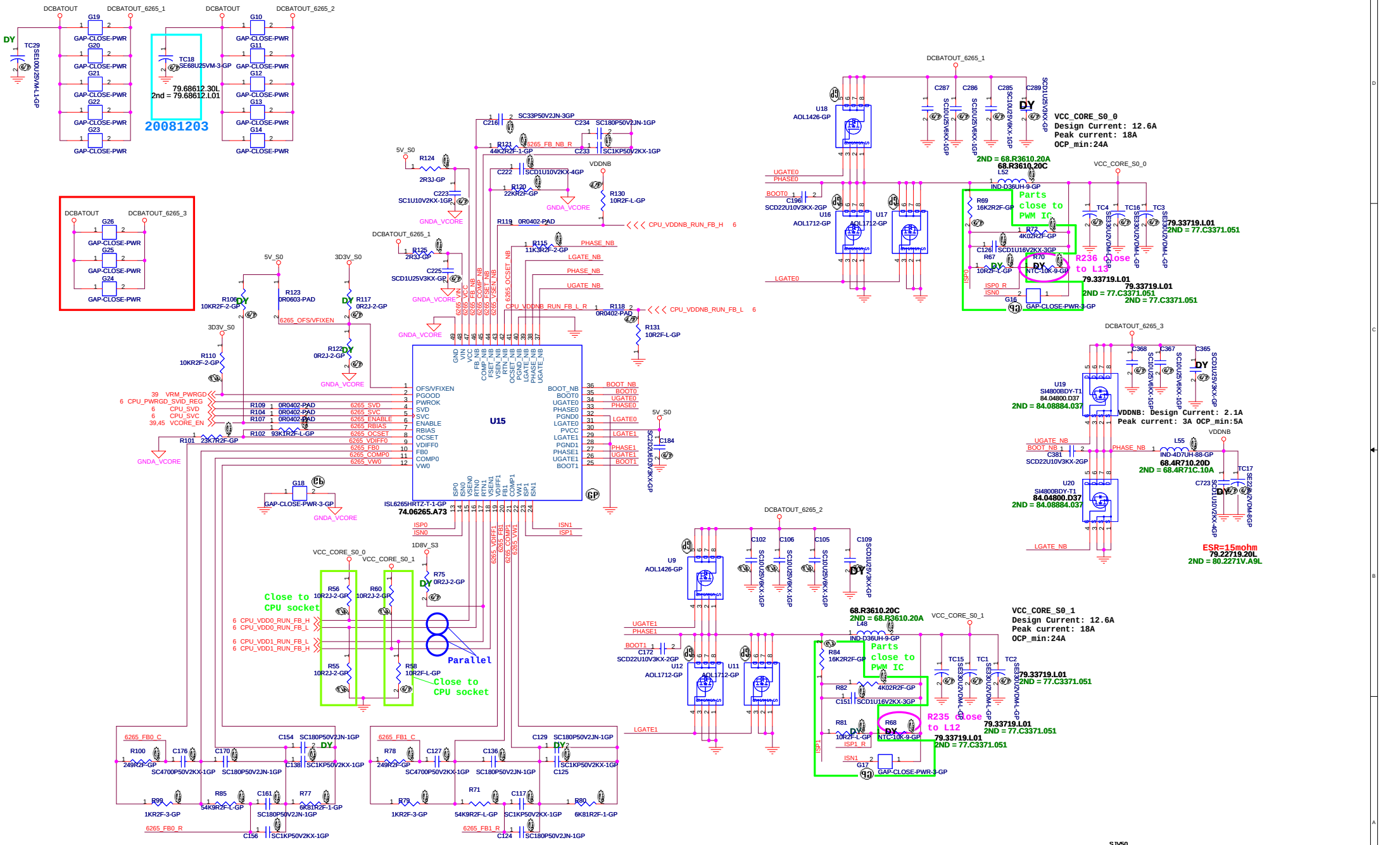
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 40 of 59



SJV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore (ISL6265HR)

Size	Document Number	Rev
Custom	SJV50-PU	-1

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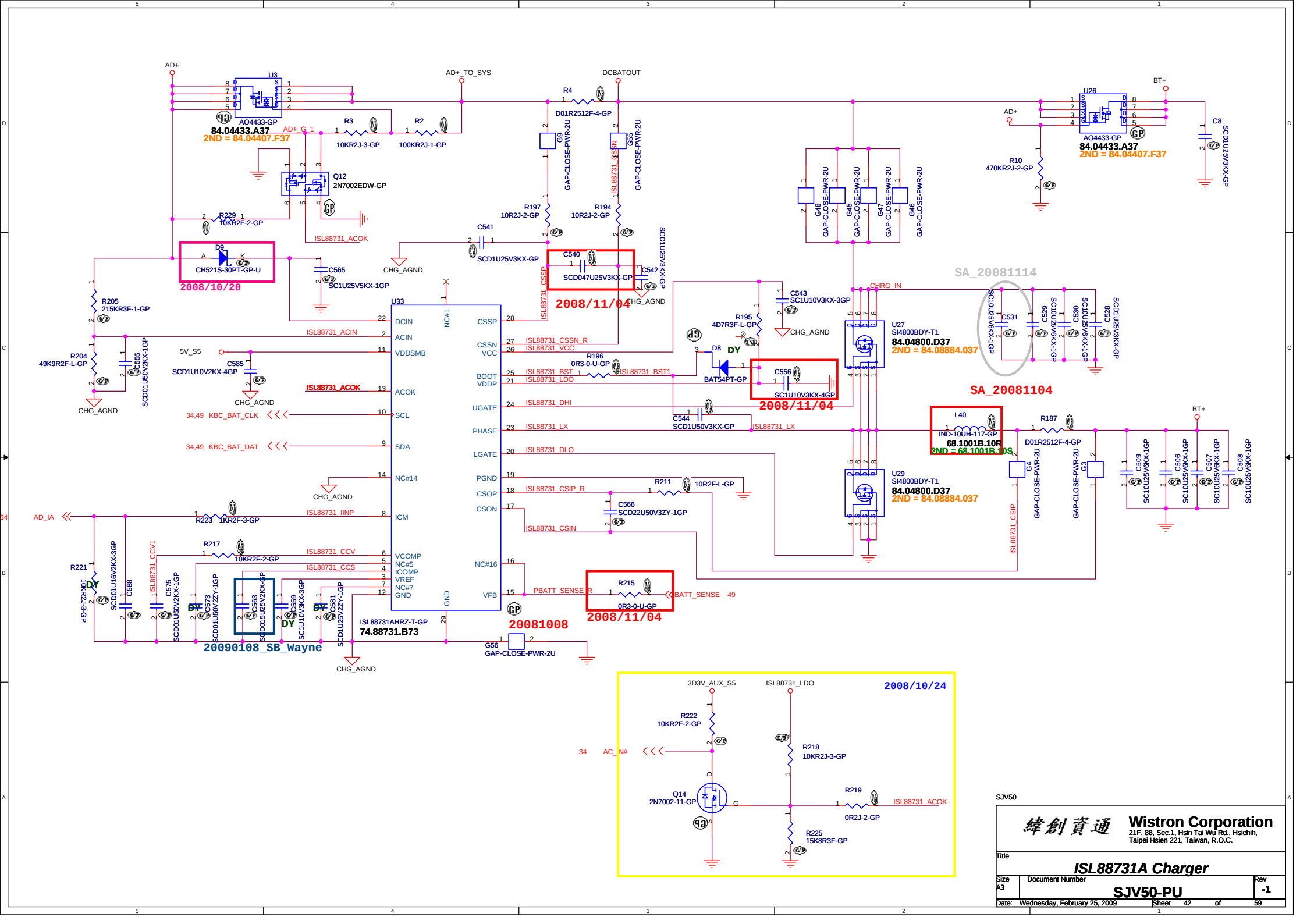
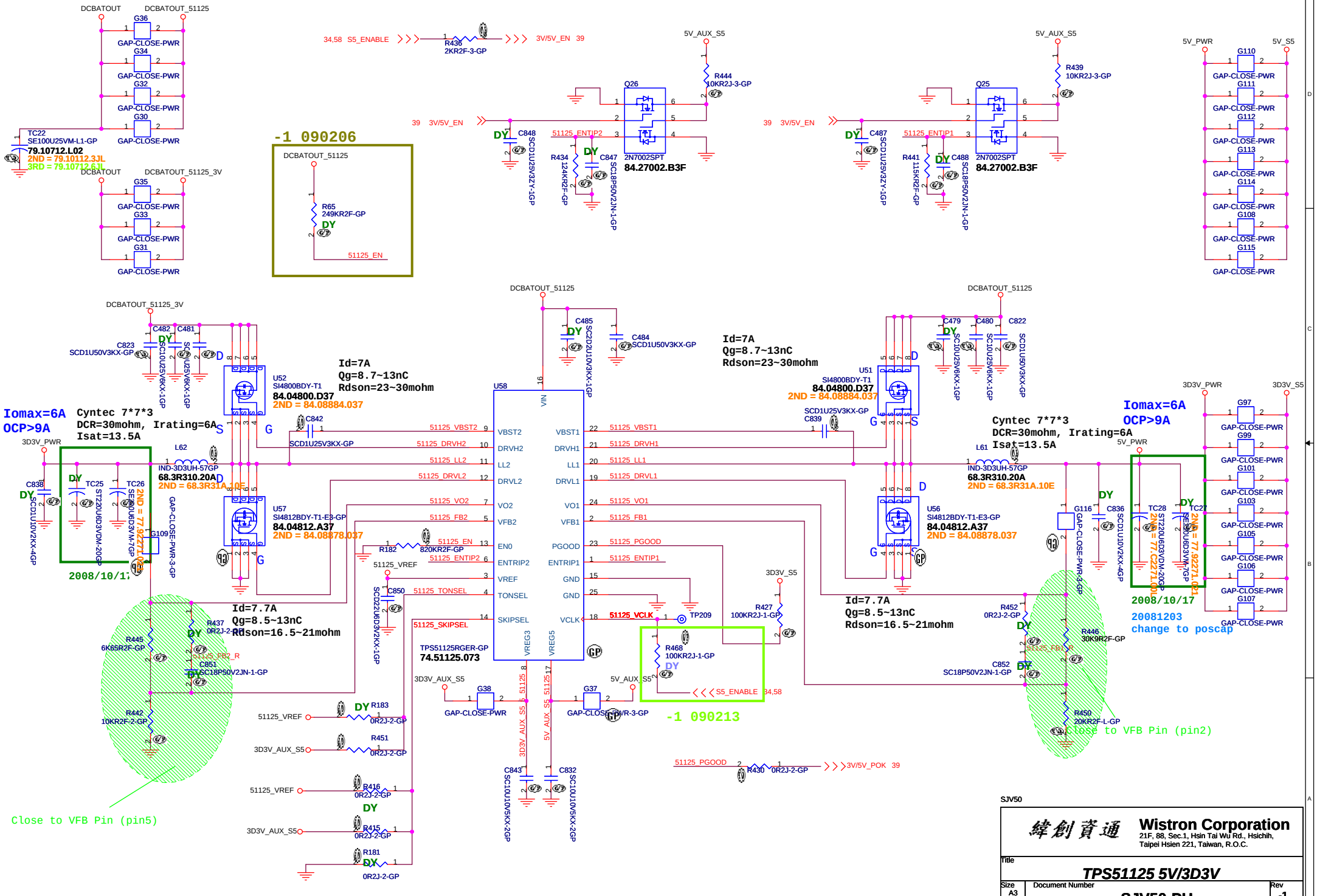
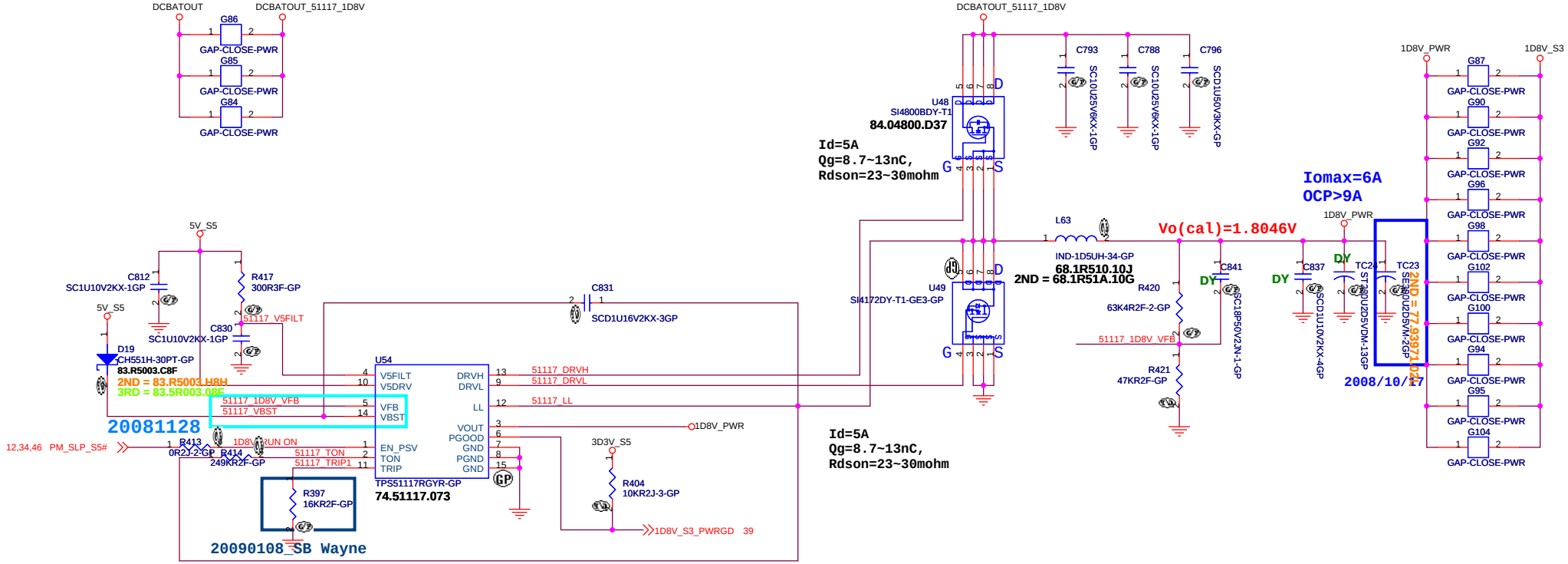

AD+
U3
AO4433-GP
84.04433.A37
2ND = 84.04407.F37
AD+_TO_SYS
DCBATOUT
R4
D01R2512F-4-GP
R3
10KR2J-3-GP
R2
100KR2J-1-GP
Q12
2N7002EDW-GP
R229
10KR2F-2-GP
ISL88731_ACOK
D9
CH521S-30PT-GP-U
2008/10/20
C565
SC1U25V5KX-1GP
CHG_AGND
C541
SCD1U25V3KX-GP
R197
10R2J-2-GP
R194
10R2J-2-GP
C540
SCD047U25V3KX-GP
C542
2008/11/04
ISL88731_CSSP
ISL88731_GSFN
GAP-CLOSE-PWR-2U
G9
G55
G48
G45
G47
G46
U26
R10
470KR2J-2-GP
C8
SCD1U25V3KX-GP
SA_20081114
SA_20081104
R205
215KR3F-1-GP
R204
49K9R2F-L-GP
C555
SCD01U50V2KX-1GP
C585
SCD1U10V2KX-4GP
5V_S5
U33
ISL88731AHRZ-T-GP
74.88731.B73
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731_ACIN
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
PBATT_SENSE_R
34,49 KBC_BAT_CLK
34,49 KBC_BAT_DAT
R196
0R3-0-U-GP
R195
4D7R3F-L-GP
D8
BAT54PT-GP
C556
SC1U10V3KX-4GP
2008/11/04
C543
SC1U10V3KX-3GP
CHRG_IN
U27
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
U29
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
C544
SCD1U50V3KX-GP
L40
IND-10UH-117-GP
68.1001B.10R
2ND = 68.1001B.10S
R187
D01R2512F-4-GP
BT+
C509
C506
C507
C508
SC10U25V6KX-1GP
C531
C529
C530
C528
SC10U25V6KX-1GP
SC10U25V6KX-4GP
SC10U25V6KX-1GP
AD_IA
R223
1KR2F-3-GP
R217
10KR2F-2-GP
R221
10KR2F-2-GP
R211
10R2F-L-GP
C566
SCD22U50V3ZY-1GP
R215
0R3-0-U-GP
PBATT_SENSE
49
2008/11/04
20081008
G56
GAP-CLOSE-PWR-2U
20090108_SB_Wayne
C588
C575
C573
C563
C559
C581
SCD01U16V2KX-3GP
SCD01U50V2KX-1GP
SCD01U50V2ZY-1GP
SCD01U50V2KX-4GP
SC1U10V3KX-3GP
SCD1U25V2ZY-1GP
DY
3D3V_AUX_S5
ISL88731_LDO
2008/10/24
R222
10KR2F-2-GP
R218
10KR2J-3-GP
Q14
2N7002-11-GP
R219
0R2J-2-GP
R225
15K8R3F-GP
AC_IN#
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
SJV50-PU
Rev
-1
Date: Wednesday, February 25, 2009
Sheet 42 of 59


DCBATOUT
DCBATOUT_51125
G36
GAP-CLOSE-PWR
G34
GAP-CLOSE-PWR
G32
GAP-CLOSE-PWR
G30
GAP-CLOSE-PWR
TC22
SE100U25VM-L1-GP
79.10712.L02
2ND = 79.10112.3JL
3RD = 79.10712.6JL
DCBATOUT_51125_3V
G35
GAP-CLOSE-PWR
G33
GAP-CLOSE-PWR
G31
GAP-CLOSE-PWR
-1 090206
DCBATOUT_51125
R65
249KR2F-GP
DY
51125_EN
34,58 S5_ENABLE
R436
2KR2F-GP
3V/5V_EN 39
5V_AUX_S5
R444
10KR2J-3-GP
Q26
39 3V/5V_EN
C848
SCD1U25V3ZY-1GP
51125_ENTIP2
R434
124KR2F-GP
C847
SC18P50V2JN-1-GP
2N7002SPT
84.27002.B3F
R439
10KR2J-3-GP
Q25
C487
51125_ENTIP1
R441
115KR2F-GP
C488
5V_PWR
5V_S5
G110
G111
G112
G113
G114
G108
G115
C485
SC2D2U10V3KX-1GP
C484
SCD1U50V3KX-GP
U58
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
GND
PGOOD
ENTRIP1
VCLK
VREG3
VREG5
TPS51125RGER-GP
74.51125.073
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_PGOOD
51125_ENTIP1
51125_VCLK
DCBATOUT_51125_3V
C482
C481
C823
SCD1U50V3KX-GP
SC1U25V6KX-1GP
U52
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
C842
SCD1U25V3KX-GP
U57
SI4812BDY-T1-E3-GP
84.04812.A37
2ND = 84.08878.037
R182
820KR2F-GP
51125_VREF
C850
SCD22U6D3V2KX-1GP
R437
0R2J-2-GP
R445
6K65R2F-GP
51125_FB2_R
C851
SC18P50V2JN-1-GP
R442
10KR2F-2-GP
Iomax=6A
OCP>9A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
3D3V_PWR
C838
SCD1U10V2KX-4GP
TC25
ST220U6D3VDM-20GP
TC26
SE330U6D3VM-7GP
G109
GAP-CLOSE-PWR-3-GP
L62
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
2008/10/17
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
R183
0R2J-2-GP
R451
0R2J-2-GP
R416
0R2J-2-GP
R415
0R2J-2-GP
R181
0R2J-2-GP
3D3V_AUX_S5
5V_AUX_S5
G38
GAP-CLOSE-PWR
G37
GAP-CLOSE-PWR-3-GP
C843
C832
SC10U10V5KX-2GP
R468
100KR2J-1-GP
TP209
R427
100KR2J-1-GP
-1 090213
51125_PGOOD
R430
0R2J-2-GP
3V/5V_POK 39
U51
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
C839
SCD1U25V3KX-GP
C479
C480
C822
SC10U25V6KX-1GP
SCD1U50V3KX-GP
U56
SI4812BDY-T1-E3-GP
84.04812.A37
2ND = 84.08878.037
L61
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Iomax=6A
OCP>9A
2008/10/17
20081203
change to poscap
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
G116
C836
SCD1U10V2KX-4GP
TC28
ST220U6D3VDM-20GP
TC27
SE330U6D3VM-7GP
G97
G99
G101
G103
G105
G106
G107
R452
0R2J-2-GP
R446
30K9R2F-GP
C852
SC18P50V2JN-1-GP
R450
20KR2F-L-GP
Close to VFB Pin (pin2)
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51125 5V/3D3V
Size
A3
Document Number
SJV50-PU
Rev
-1
Date: Wednesday, February 25, 2009
Sheet 43 of 59



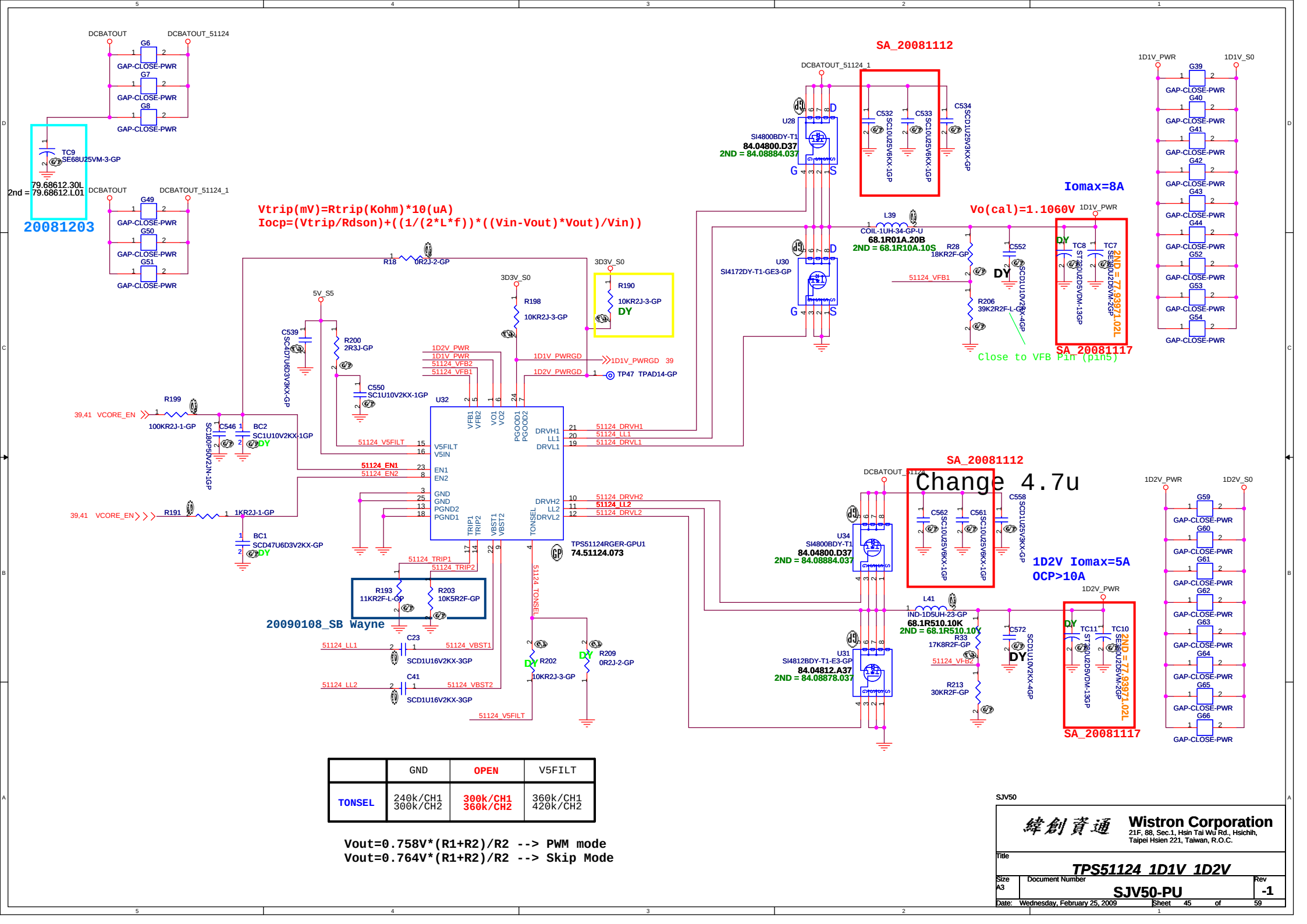
SJV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V/1D2V

Size	Document Number	Rev
A3	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 44 of 59



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

SJV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

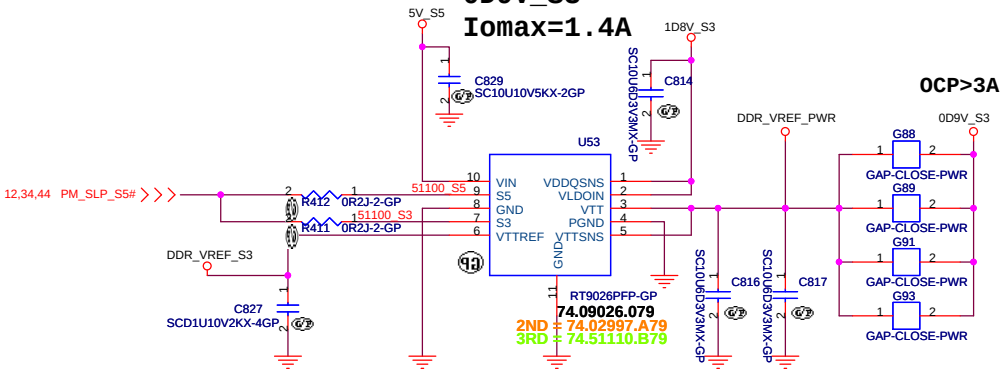
Title: TPS51124 1D1V 1D2V

Size: A3 | Document Number: SJV50-PU | Rev: -1

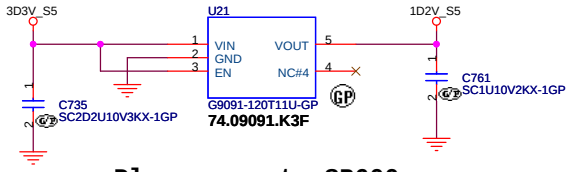
Date: Wednesday, February 25, 2009 | Sheet 45 of 59

0D9V_S3
Iomax=1.4A

OCP>3A



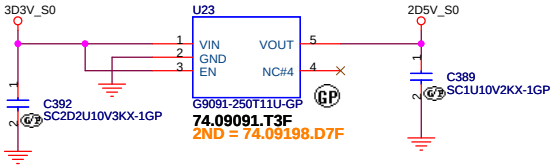
1D2V_S5
Iomax=0.2A



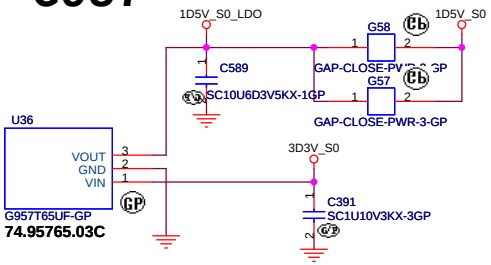
Place near to SB600

2D5V_S0
Iomax=200mA

OCP>430mA



G957
1D5V_S0
Iomax=1A

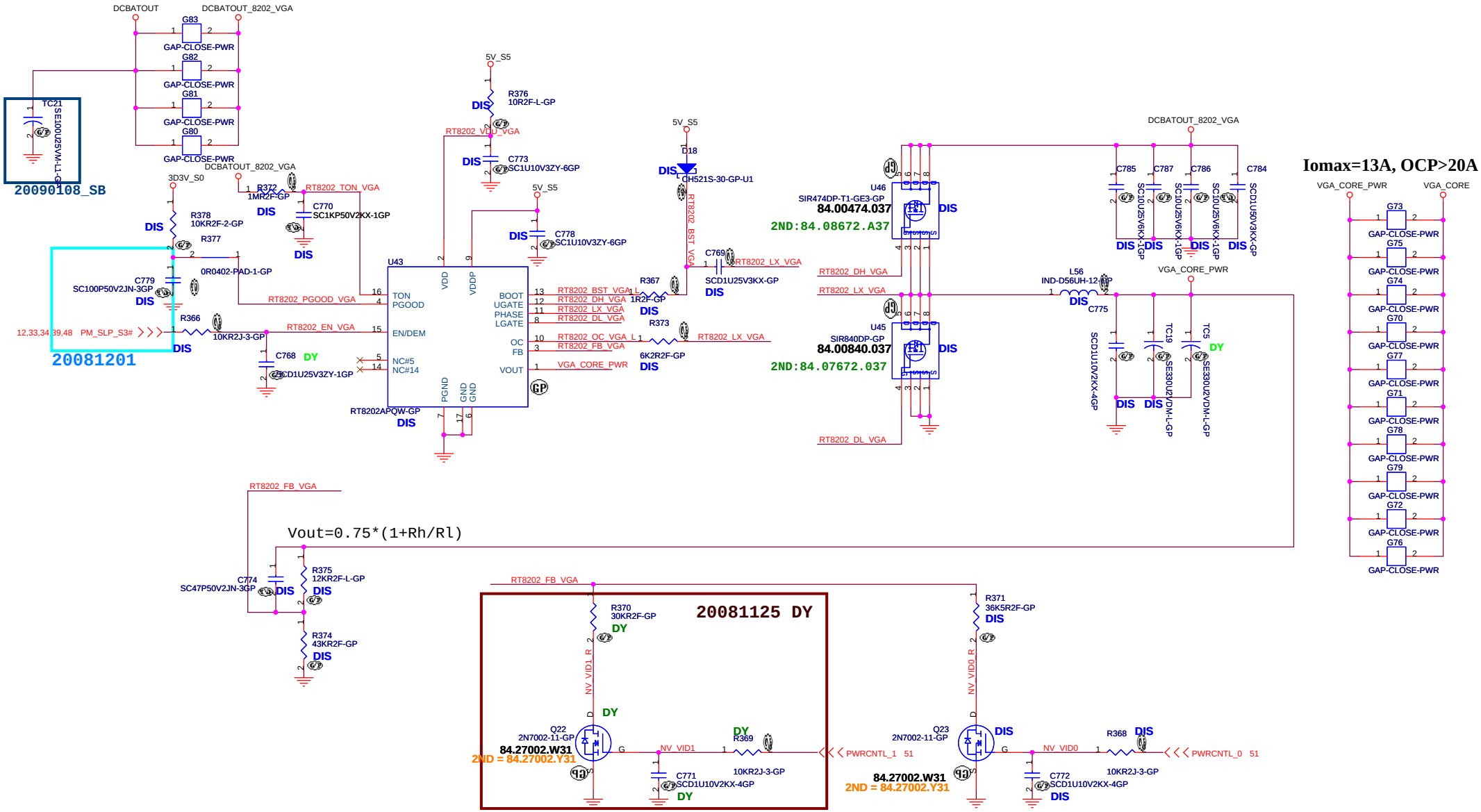


For MINI Card power SW

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

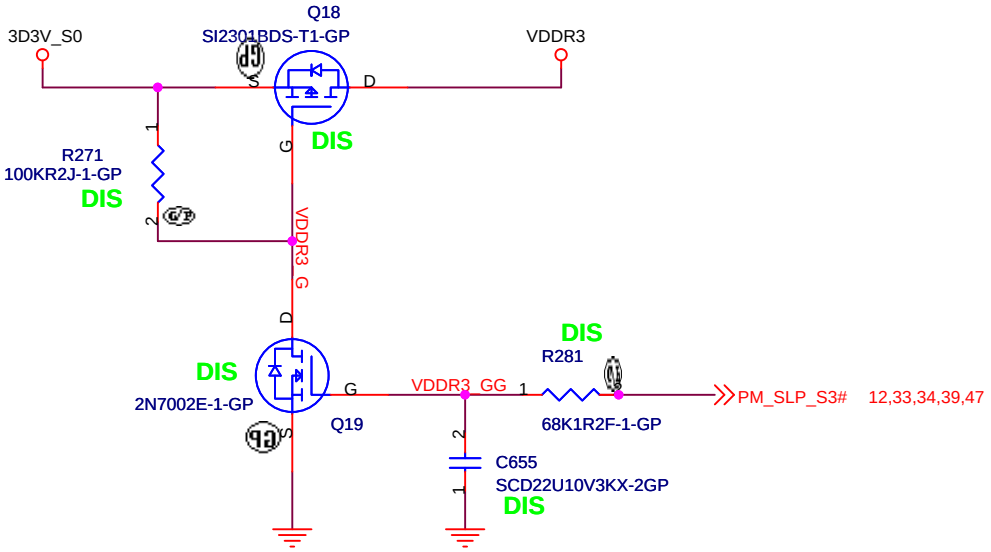
Title	2D5V/1D5V0D9V	
Size: A3	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 46 of 59	



SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8202A_VGA CORE	
Size	Document Number SJV50-PU	Rev -1
Date: Wednesday, February 25, 2009	Sheet 47 of 59	

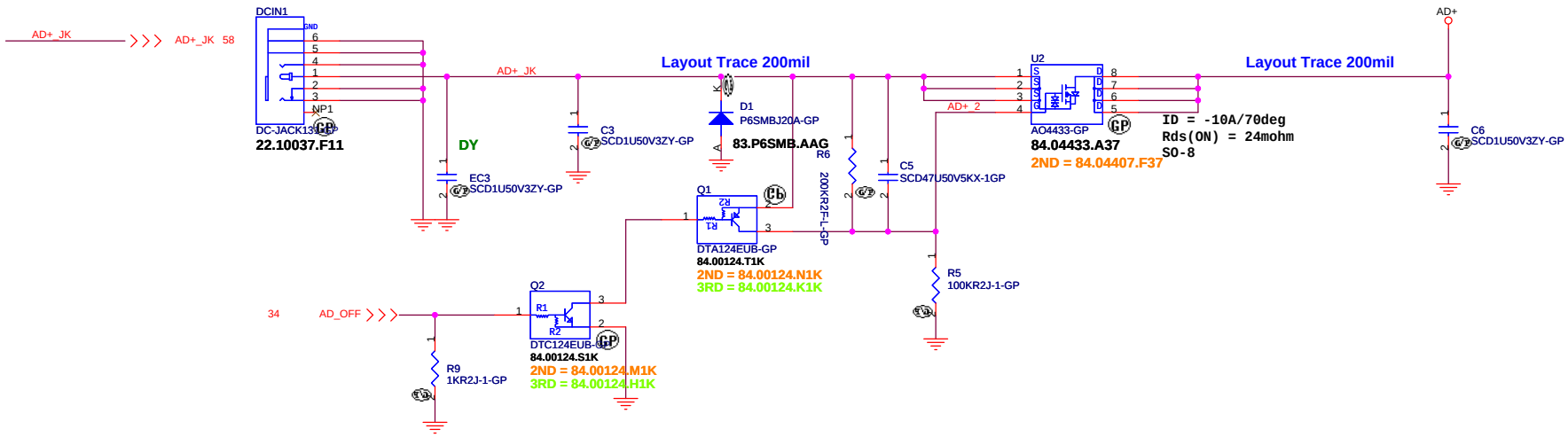


SJV50

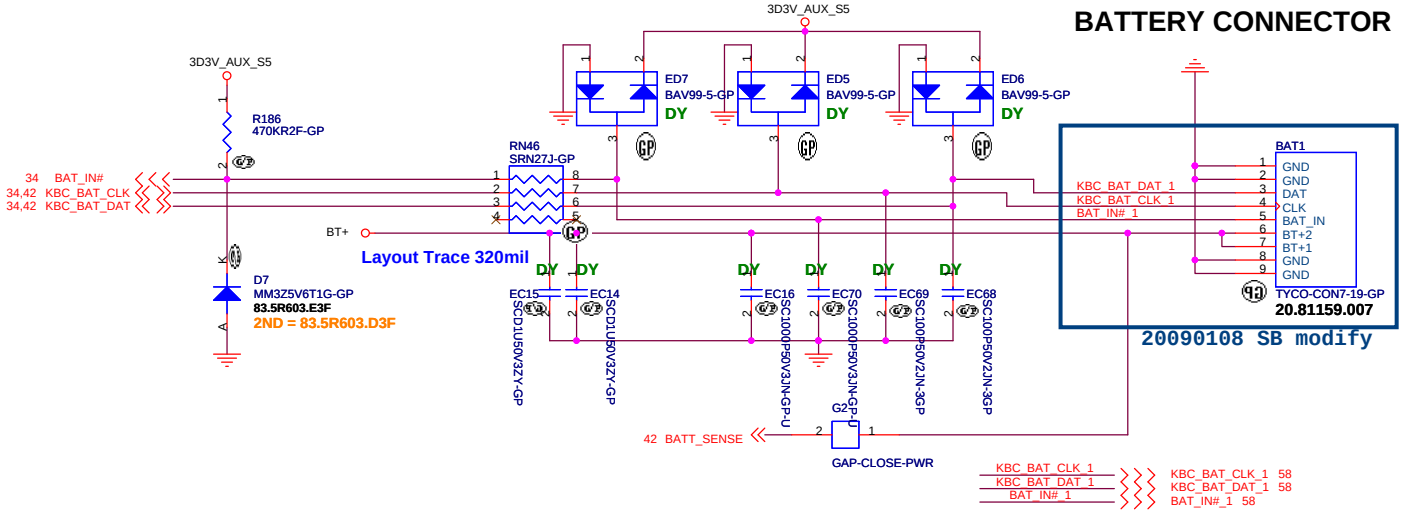
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VDDR3***	
Size A4	Document Number **SJV50-PU**	Rev **-1**
Date: Wednesday, February 25, 2009	Sheet 48 of 59	

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



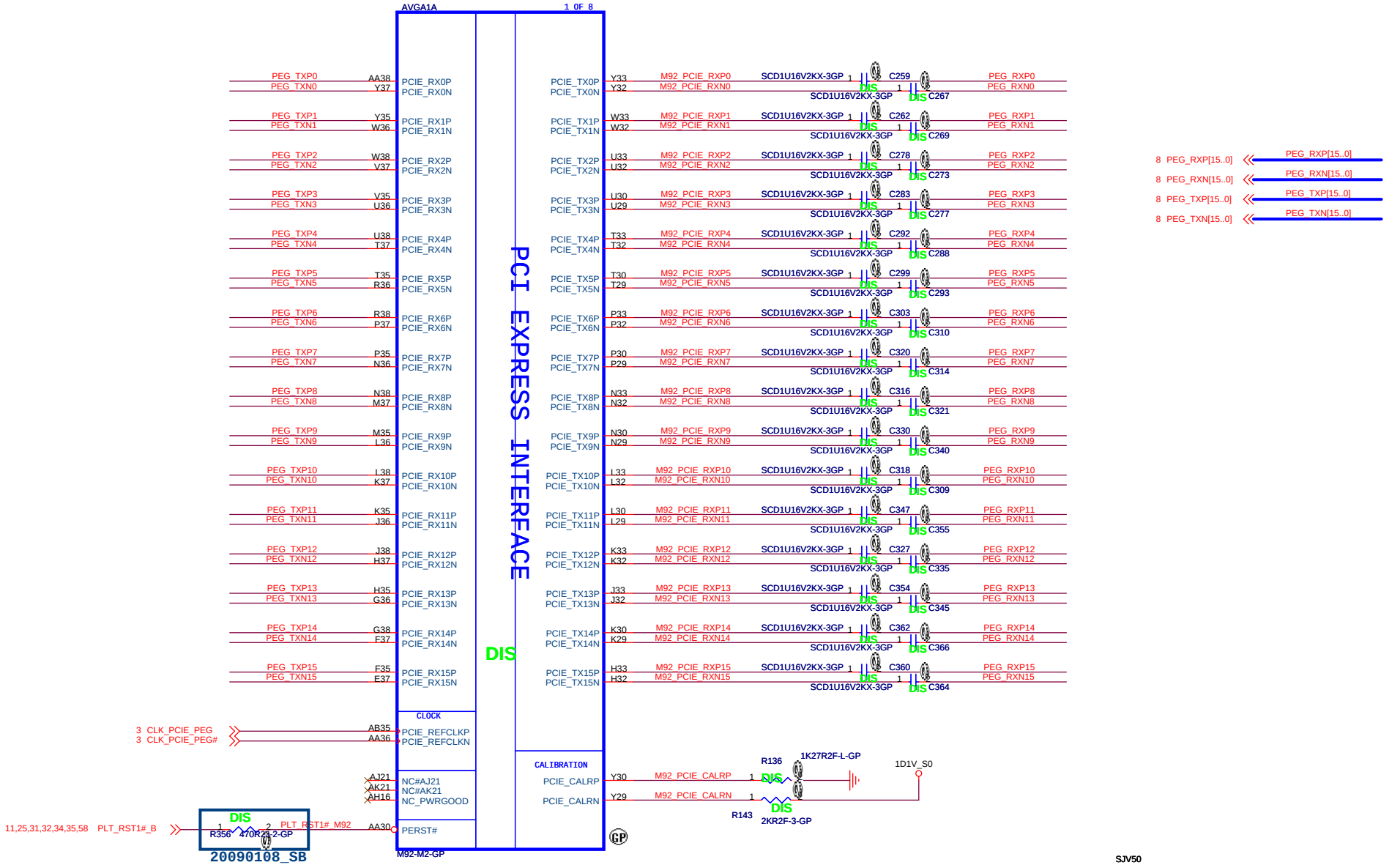
SJV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

Size	Document Number	Rev
A3	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 49 of 59



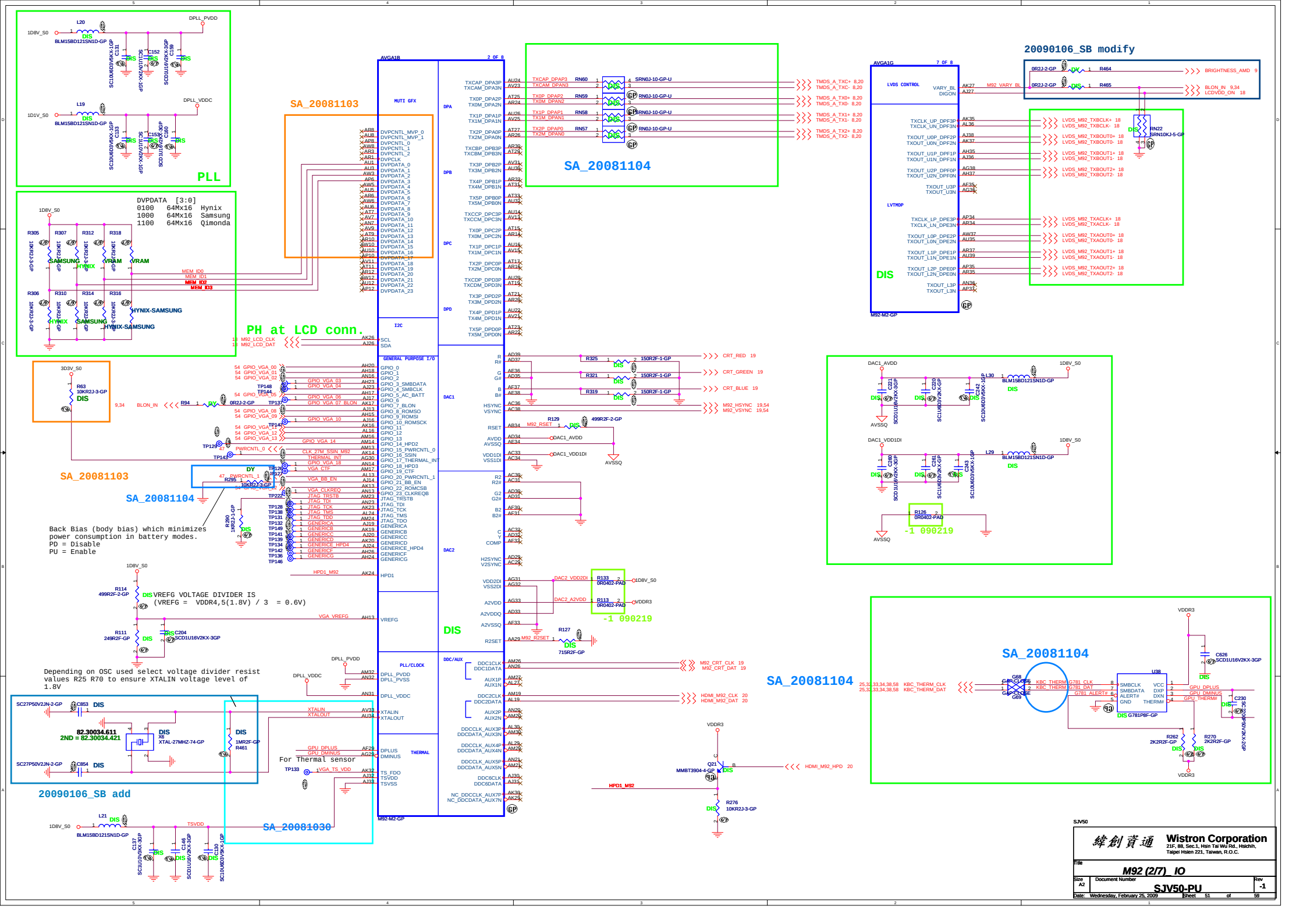
SJV50

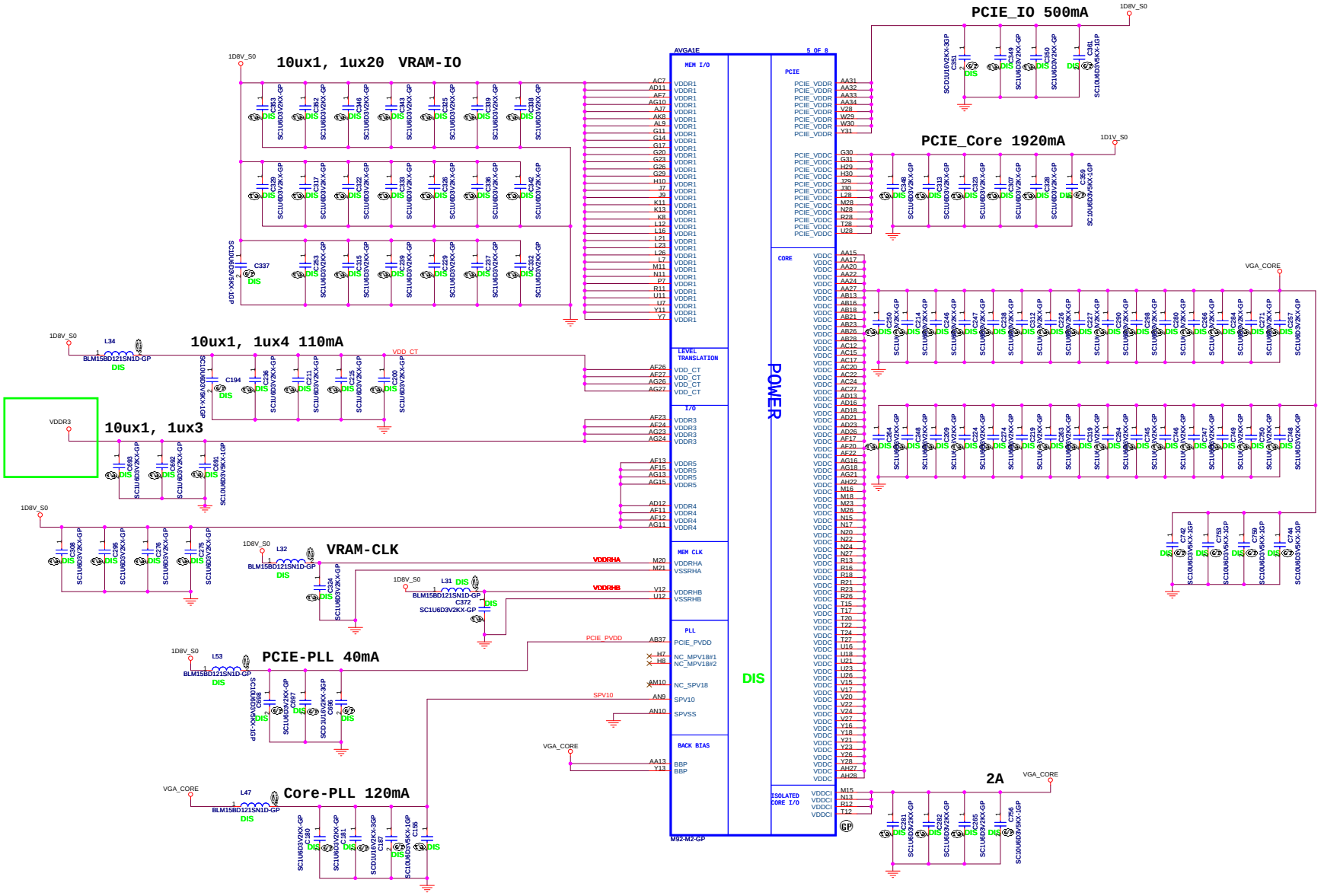
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***M92 (1/7) PCIE***

Size	Document Number	Rev
A3	**SJV50-PU**	-1

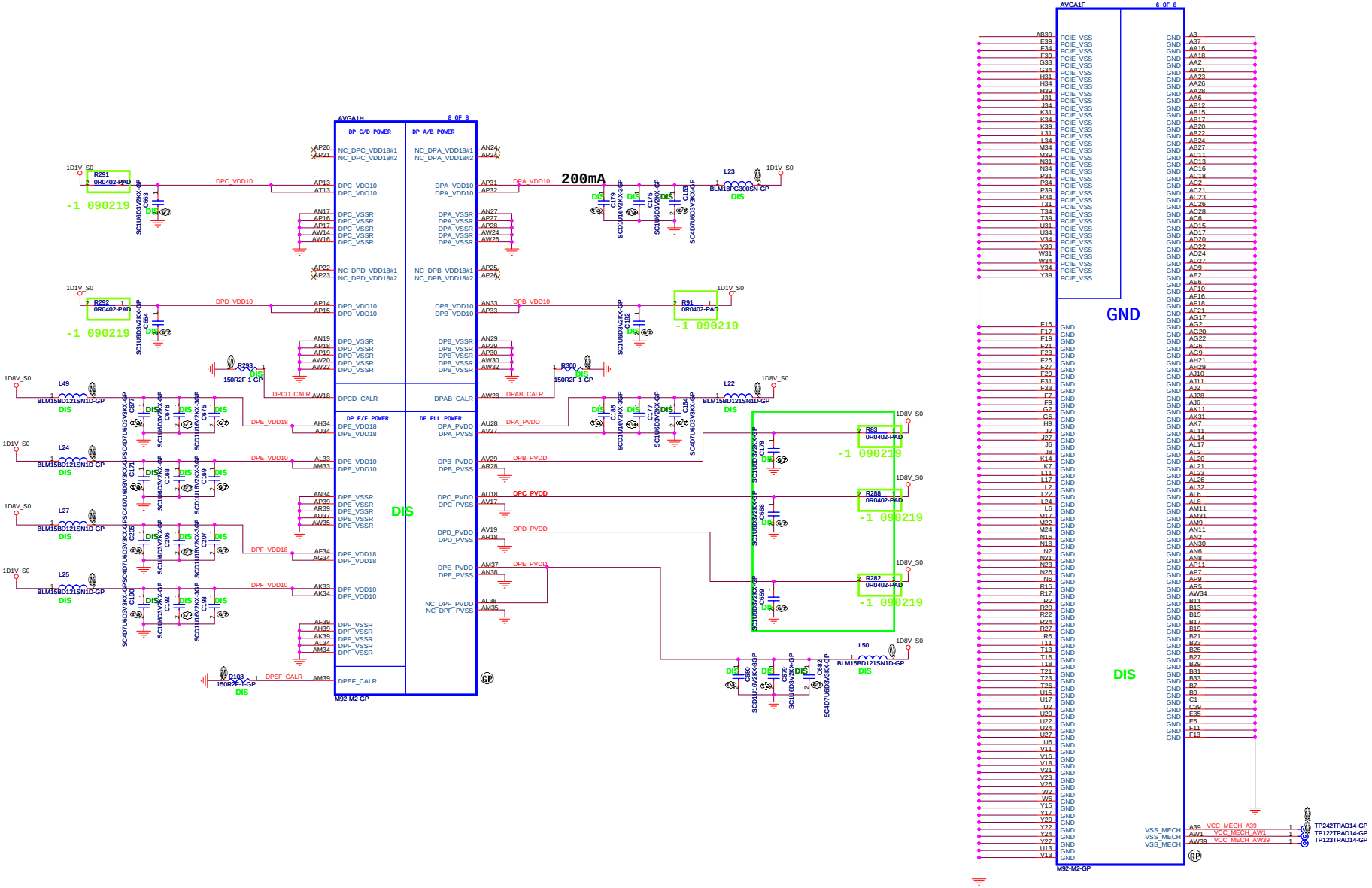
Date: Wednesday, February 25, 2009 Sheet 50 of 59


PLL
SA_20081103
SA_20081104
SA_20081030
20090106_SB modify
20090106_SB add
PH at LCD conn.
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
1100 64Mx16 Qimonda
Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable
VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V
For Thermal sensor
-1 090219
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
M92 (2/7)_IO
SJV50-PU
Date: Wednesday, February 25, 2009



SJV50

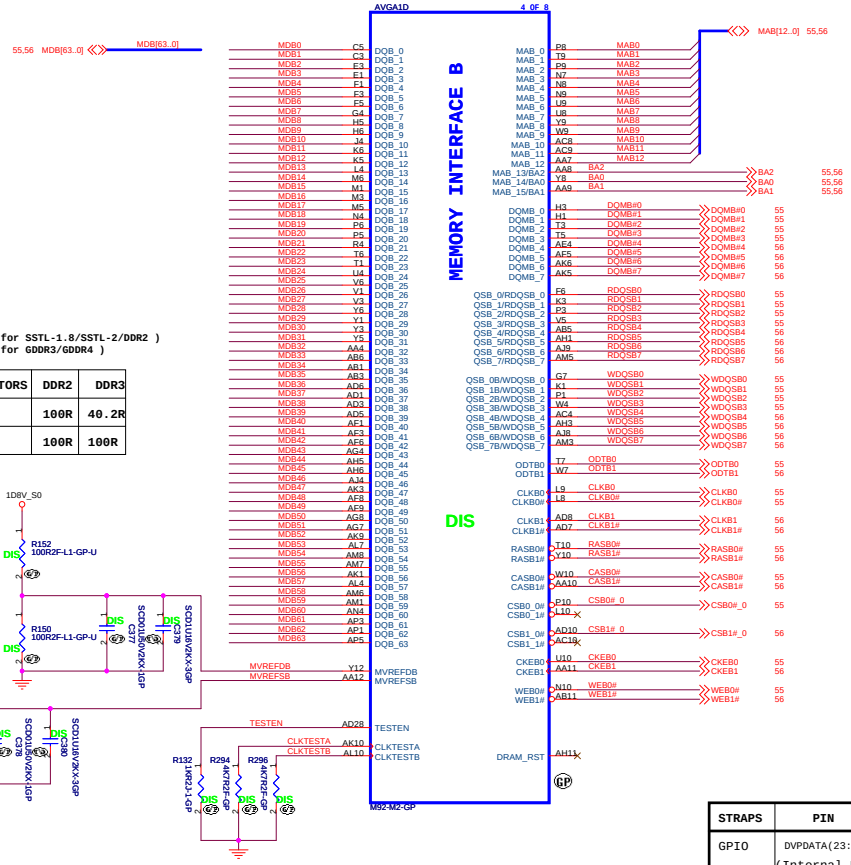
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 (3/7) Power		
Size: A2	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 52 of 59	



SJV50

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	M92 (4/7) DP POWER_GND	
Size: A2	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 53 of 59	

M92-M2 uses memory group B only

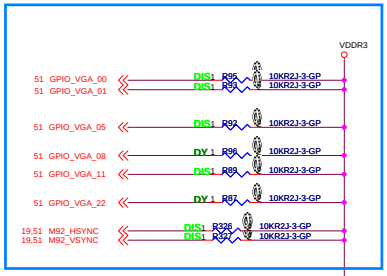


(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

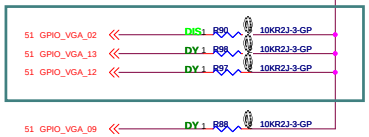
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

SA_20081104



SA_20081105



HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

SJV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 (5/7) Memory Straps

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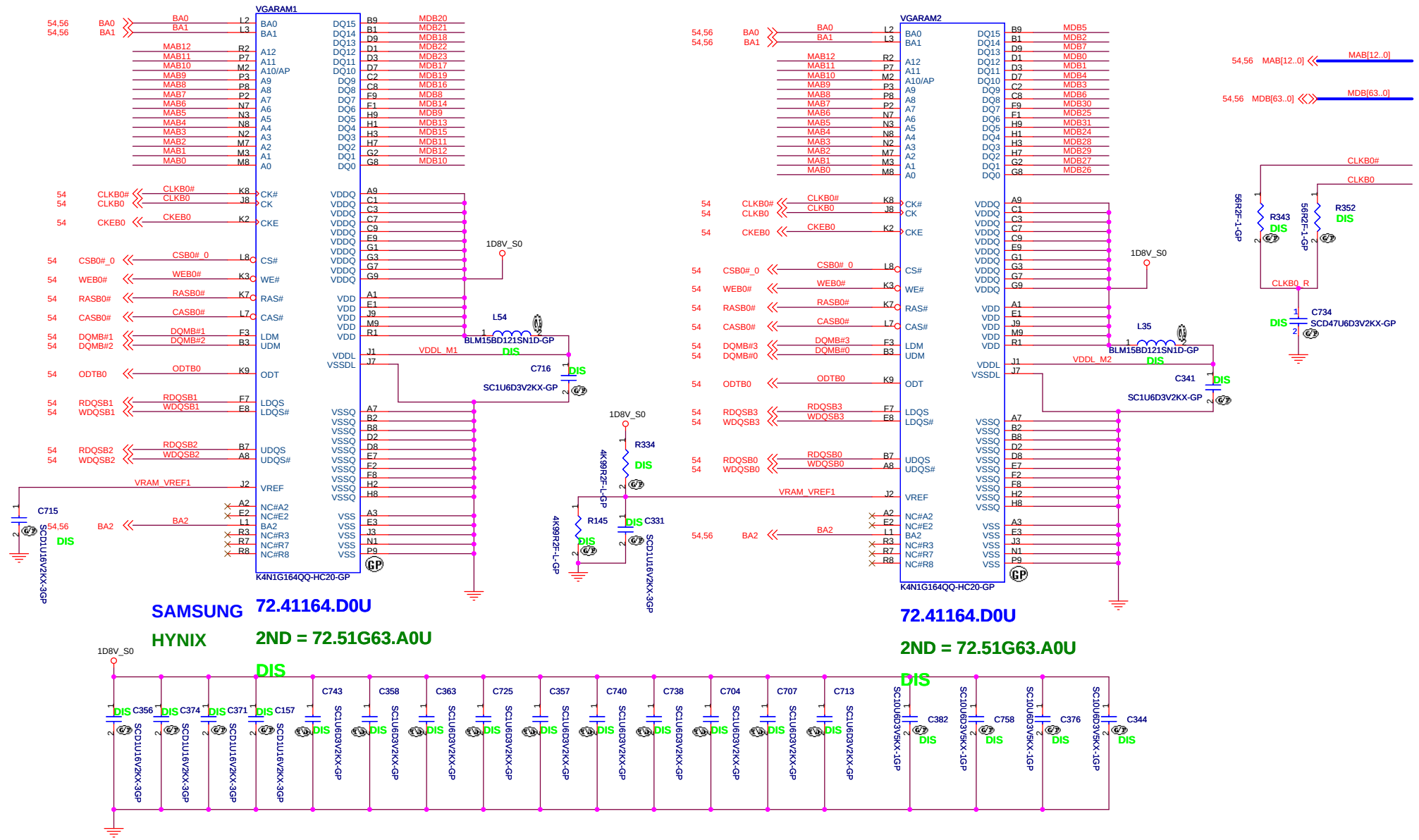

SJV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *M92 (6/7) VRAM B0*

Size	Document Number	Rev
A3	SJV50-PU	-1

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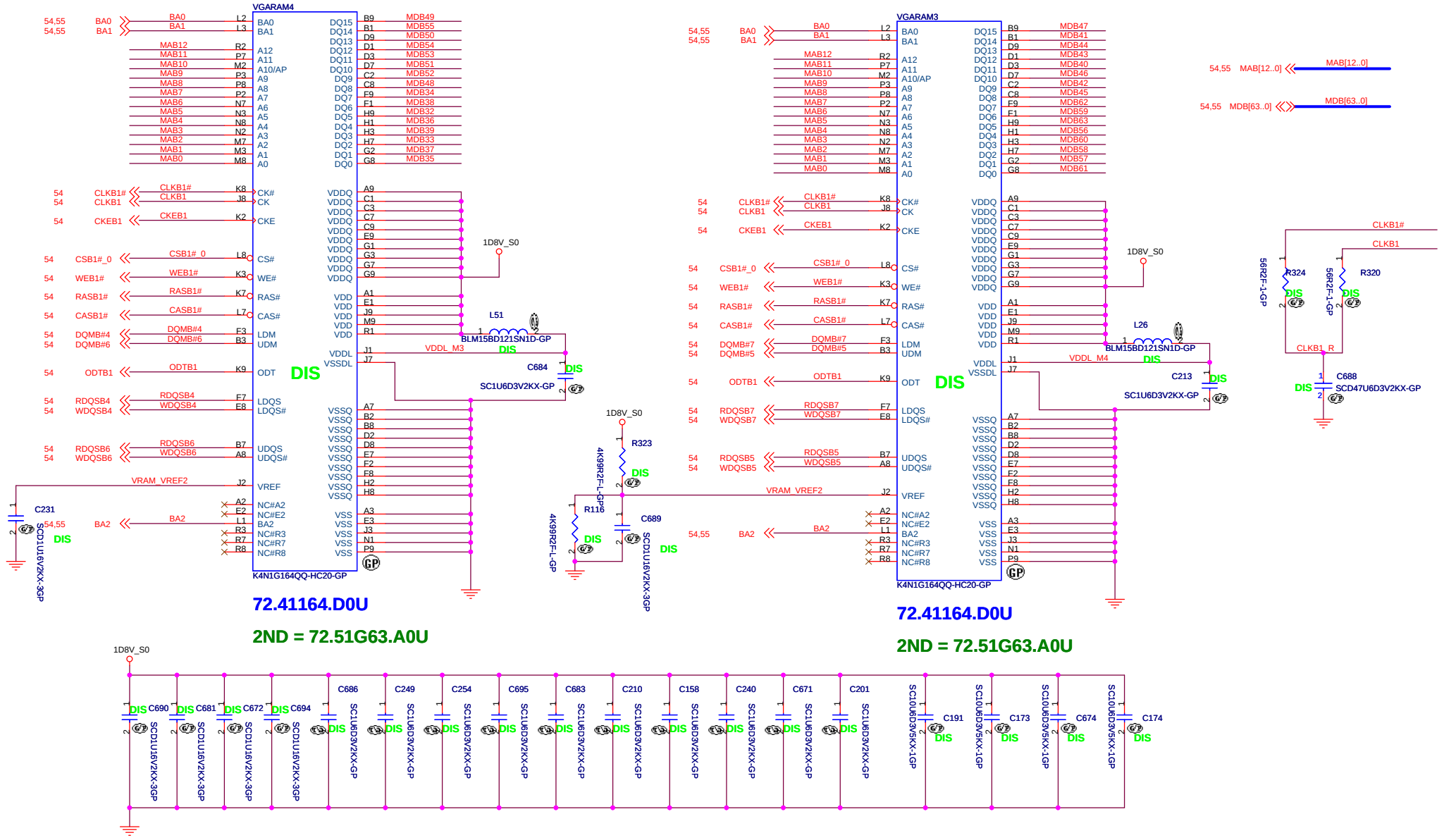
VGARAM4
K4N1G164QQ-HC20-GP
DIS
1D8V_S0
L51
BLM15BD121SN1D-GP
VDDL_M3
C684
SC1U6D3V2KX-GP
R323
4K99R2F-L-GP
R116
C689
SCD1U16V2KX-3GP
VRAM_VREF2
C231
72.41164.D0U
2ND = 72.51G63.A0U
VGARAM3
L26
VDDL_M4
C213
MAB[12..0]
MDB[63..0]
R324
R320
56R2F-1-GP
CLKB1_R
C688
SCD47U6D3V2KX-GP
C690
C681
C672
C694
C686
C249
C254
C695
C683
C210
C158
C240
C671
C201
C191
C173
C674
C174
SC1U6D3V5KX-1GP
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M92 (7/7) VRAM B1
Size A3
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Date: Wednesday, February 25, 2009
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SA

SB

-1

5V_S0

U7C
TSAHCT125PW-GP
73.74125.L13
2ND = 73.74125.L12
3RD = 73.74125.01B

5V_S0

U7D
TSAHCT125PW-GP
73.74125.L13
2ND = 73.74125.L12
3RD = 73.74125.01B

GND1 HOLE355X355R111-S1-GP
GND2 HOLE355X355R111-S1-GP
GND3 HOLE355X355R111-S1-GP
GND4 HOLE355X355R111-S1-GP
GND5
GND6 HOLE355X355R111-S1-GP
GND7 HOLE355X355R111-S1-GP
GND8 HOLE355X355R111-S1-GP
GND9 HOLE355X355R111-S1-GP
GND10

-1_0205

-1_0217

H7 HOLE236R142 34.42Y01.031 Type-M

H8 HOLE236R142 34.42Y01.031 Type-M

H15 HOLE276R110 34.4B804.001 DY

H20 HOLE276R110 34.4B804.001 DY

H11 HOLE276R142 34.42Y01.031 Type-I

H12 HOLE276R142 34.42Y01.031 Type-I

H13 HOLE276R142 34.42Y01.031 Type-I

H14 HOLE276R142 34.42Y01.031 Type-I

H16 HOLE276R142 34.42Y01.031 Type-I

H17 HOLE276R142 34.42Y01.031 Type-I

SPR1 SPRING-71-GP 34.4H551.001

SPR2 SPRING-71-GP DY 34.4H551.001

SPR3 SPRING-71-GP DY 34.4H551.001

20081203

20081202

DCBATOUT

-1 090223_EMI

-1 090223_EMI

1D1V_S0

5V_S5

5V_S0

3D3V_S0

SJV50

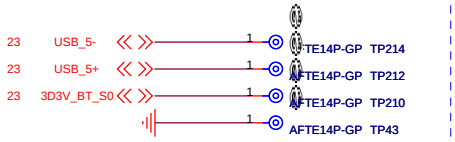
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

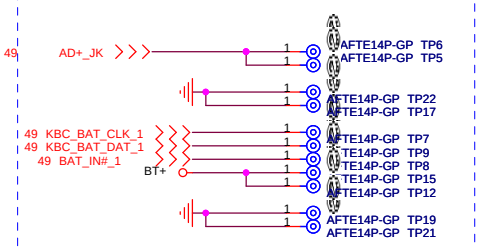
Size | Document Number: SJV50-PU | Rev: -1

Date: Wednesday, February 25, 2009 | Sheet 57 of 59

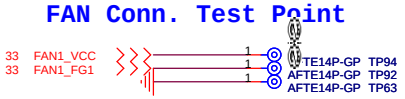
BT Conn. Test Point



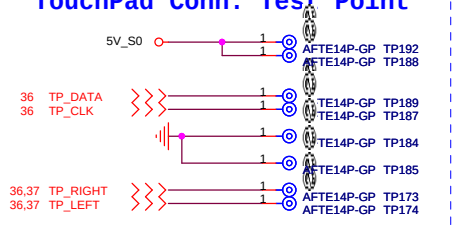
AD+, BAT Conn. Test Point



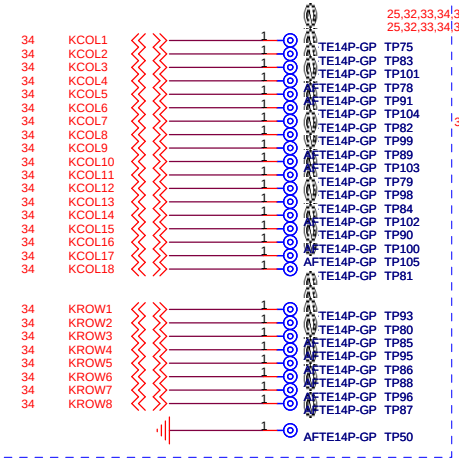
FAN Conn. Test Point



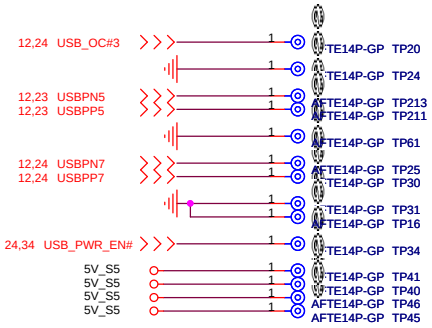
TouchPad Conn. Test Point



KB Conn. Test Point

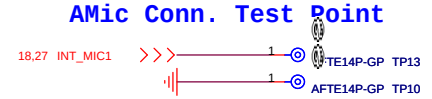


USBCN1 Conn. Test Point

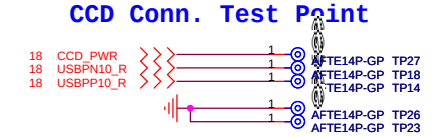


PowerButton Conn. Test Point

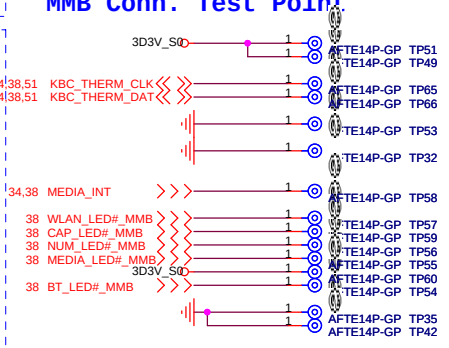
AMic Conn. Test Point



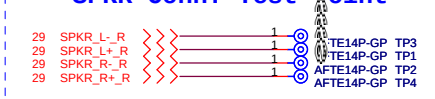
CCD Conn. Test Point



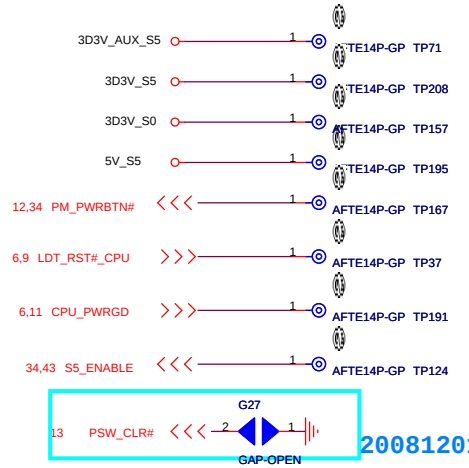
MMB Conn. Test Point



SPKR Conn. Test Point



Check test point



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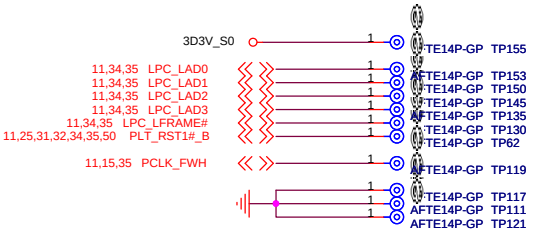
Test Point放在Dimm Door打開可量測處



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