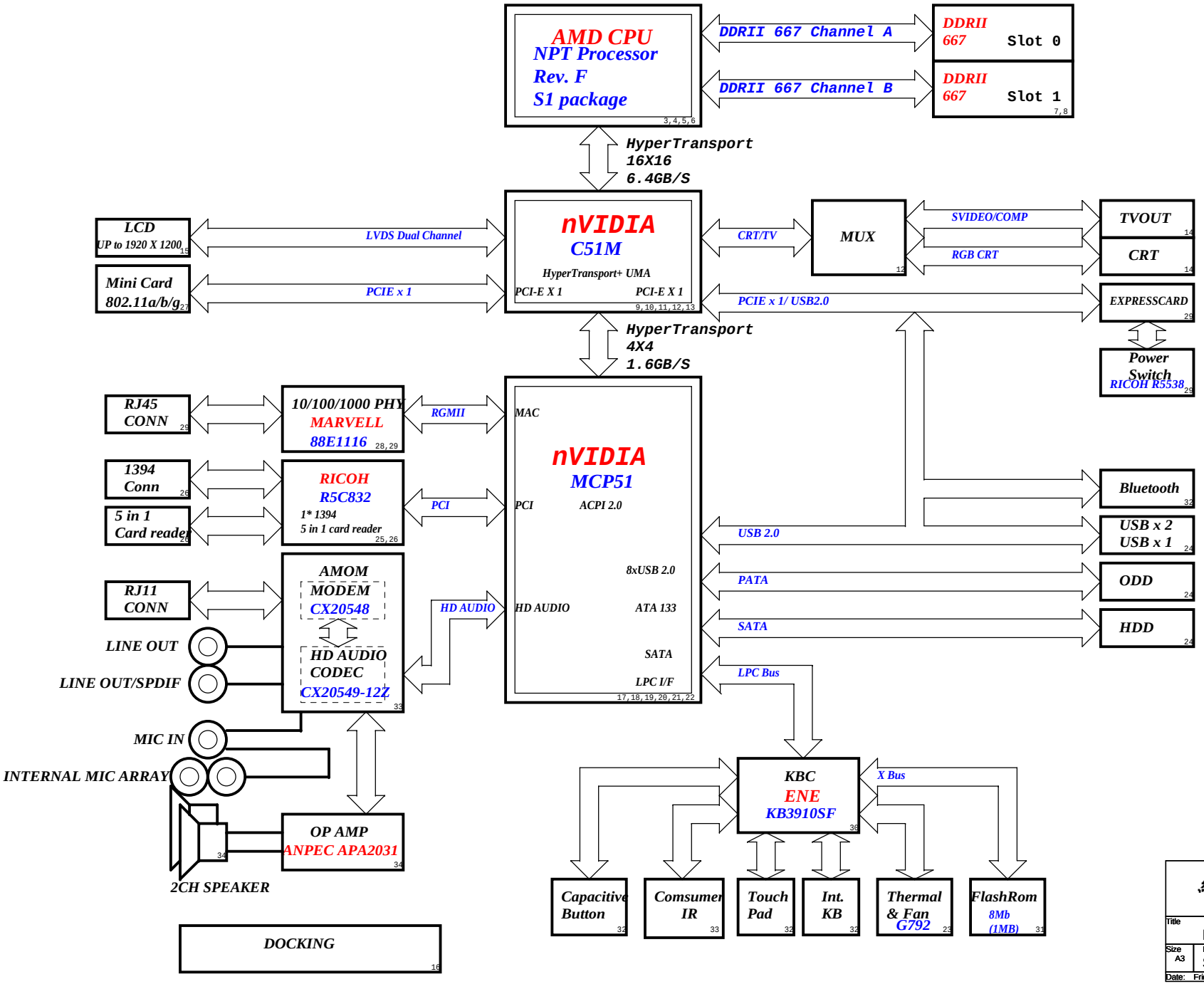
Shiba Block Diagram(FF+)

Project Code: 91.4F701.001
Project Name: Shiba
PCB Number: 05234



SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

PCB LAYER

L1:SIGNAL 1
L2:GND
L3:SIGNAL 2
L4:SIGNAL 3
L5:VCC
L6:SIGNAL 4

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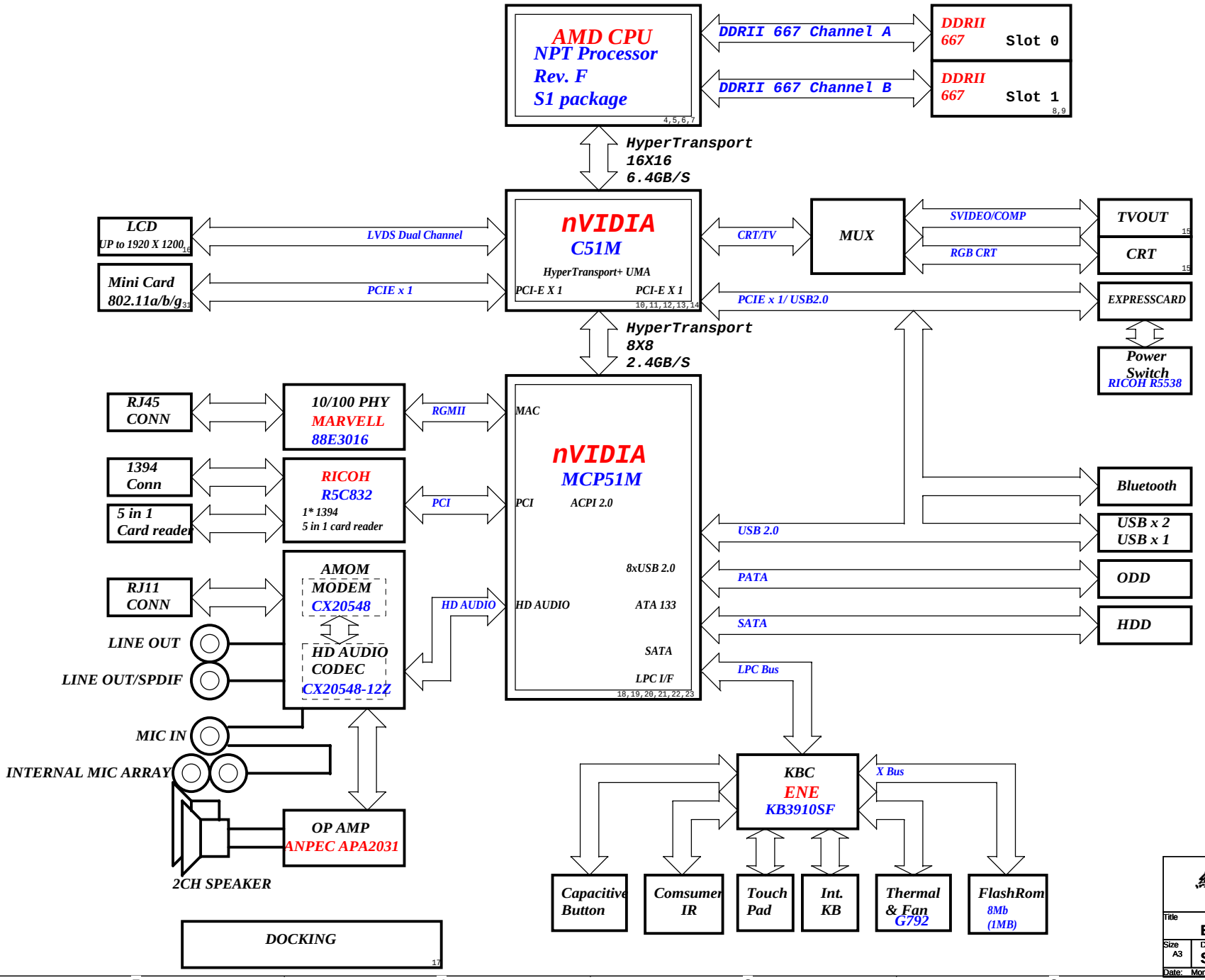
Title: Block Diagram(FF+)
Size: A3 | Document Number: SHIBA | Rev: SA
Date: Friday, November 11, 2005 | Sheet 1 of 44

Shiba Block Diagram(DF)



SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

PCB LAYER
L1:SIGNAL 1
L2:GND
L3:SIGNAL 2
L4:SIGNAL 3
L5:VCC
L6:SIGNAL 4

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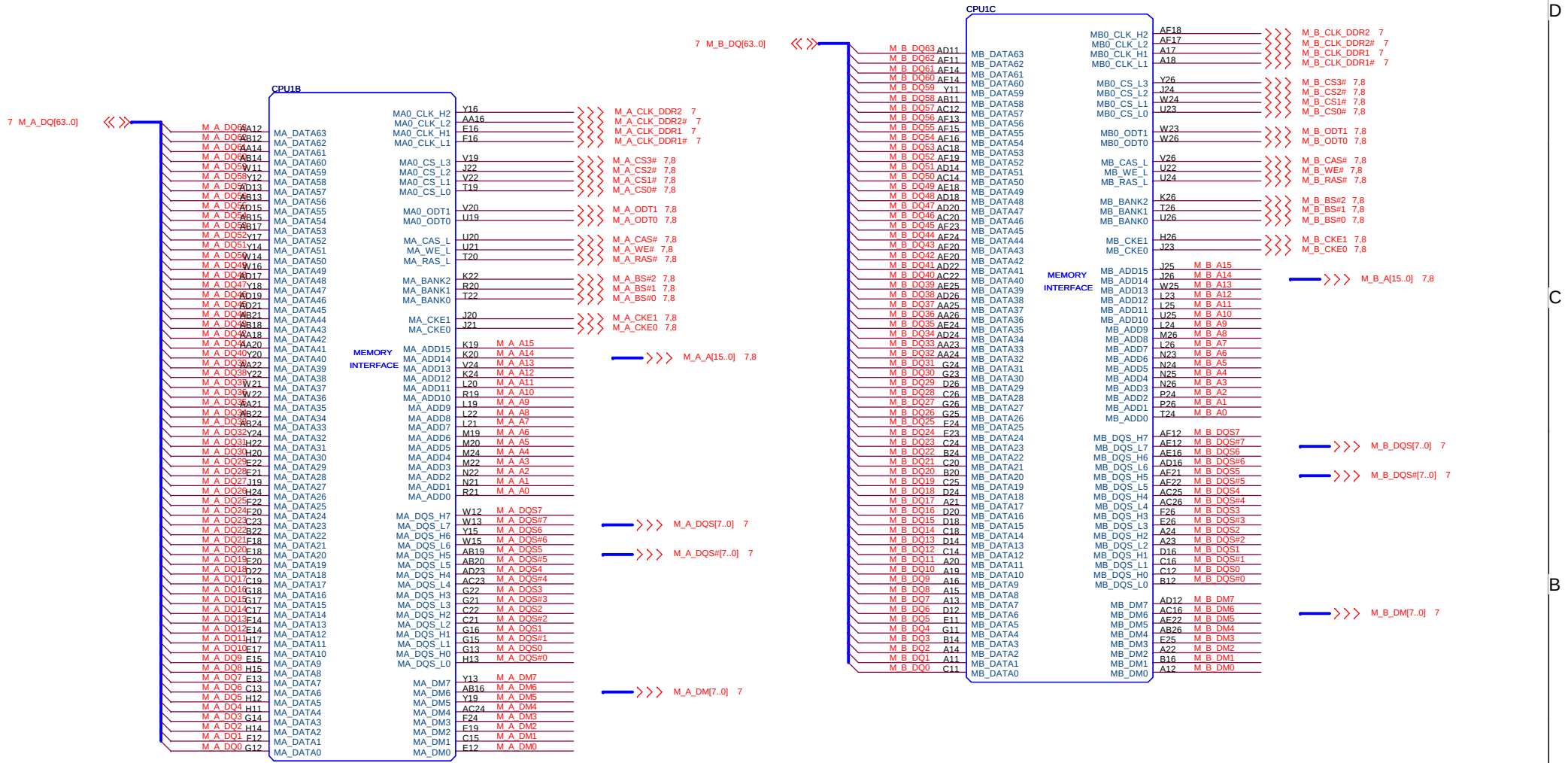
Title: Block Diagram(FF+)

Size: A3 | Document Number: SHIBA | Rev: SA

Date: Monday, October 31, 2005 | Sheet 2 of 44


CPU1A
HYPERTRANSPORT
1D2V_HT_S0
R469
51R2J-2-GP
R468
51R2J-2-GP
9 NB0HTTCLKOUT1
9 NB0HTTCLKOUTJ1
9 NB0HTTCLKOUT0
9 NB0HTTCLKOUTJ0
9 NB0HTTCTLOUT
9 NB0HTTCTLOUTJ
9 NB0CADOUT[15..0]
9 NB0CADOUTJ[15..0]
CPUHTTCLKOUT1 9
CPUHTTCLKOUTJ1 9
CPUHTTCLKOUT0 9
CPUHTTCLKOUTJ0 9
CPUHTTCTLOUT0 9
CPUHTTCTLOUTJ0 9
CPUCADOUT[15..0] 9
CPUCADOUTJ[15..0] 9


CPU1B
MEMORY INTERFACE
7 M_A_DQ[63..0]
M_A_DQ63 AB12
M_A_DQ62 AB14
M_A_DQ61 AA14
M_A_DQ60 AB14
M_A_DQ59 W11
M_A_DQ58 Y12
M_A_DQ57 AD13
M_A_DQ56 AB13
M_A_DQ55 AD15
M_A_DQ54 AB15
M_A_DQ53 AB17
M_A_DQ52 Y17
M_A_DQ51 Y14
M_A_DQ50 W14
M_A_DQ49 W16
M_A_DQ48 AD17
M_A_DQ47 Y18
M_A_DQ46 AD19
M_A_DQ45 AD21
M_A_DQ44 AB21
M_A_DQ43 AB18
M_A_DQ42 AA18
M_A_DQ41 AA20
M_A_DQ40 Y20
M_A_DQ39 AA22
M_A_DQ38 Y22
M_A_DQ37 W21
M_A_DQ36 W22
M_A_DQ35 AA21
M_A_DQ34 AB22
M_A_DQ33 AB24
M_A_DQ32 Y24
M_A_DQ31 H22
M_A_DQ30 H20
M_A_DQ29 E22
M_A_DQ28 E21
M_A_DQ27 J19
M_A_DQ26 H24
M_A_DQ25 E22
M_A_DQ24 E20
M_A_DQ23 C23
M_A_DQ22 B22
M_A_DQ21 F18
M_A_DQ20 E18
M_A_DQ19 E20
M_A_DQ18 D22
M_A_DQ17 C19
M_A_DQ16 G18
M_A_DQ15 G17
M_A_DQ14 C17
M_A_DQ13 F14
M_A_DQ12 E14
M_A_DQ11 H17
M_A_DQ10 E17
M_A_DQ9 E15
M_A_DQ8 H15
M_A_DQ7 E13
M_A_DQ6 C13
M_A_DQ5 H12
M_A_DQ4 H11
M_A_DQ3 G14
M_A_DQ2 H14
M_A_DQ1 F12
M_A_DQ0 G12
MA_DATA63 MA_DATA62 MA_DATA61 MA_DATA60 MA_DATA59 MA_DATA58 MA_DATA57 MA_DATA56 MA_DATA55 MA_DATA54 MA_DATA53 MA_DATA52 MA_DATA51 MA_DATA50 MA_DATA49 MA_DATA48 MA_DATA47 MA_DATA46 MA_DATA45 MA_DATA44 MA_DATA43 MA_DATA42 MA_DATA41 MA_DATA40 MA_DATA39 MA_DATA38 MA_DATA37 MA_DATA36 MA_DATA35 MA_DATA34 MA_DATA33 MA_DATA32 MA_DATA31 MA_DATA30 MA_DATA29 MA_DATA28 MA_DATA27 MA_DATA26 MA_DATA25 MA_DATA24 MA_DATA23 MA_DATA22 MA_DATA21 MA_DATA20 MA_DATA19 MA_DATA18 MA_DATA17 MA_DATA16 MA_DATA15 MA_DATA14 MA_DATA13 MA_DATA12 MA_DATA11 MA_DATA10 MA_DATA9 MA_DATA8 MA_DATA7 MA_DATA6 MA_DATA5 MA_DATA4 MA_DATA3 MA_DATA2 MA_DATA1 MA_DATA0
MA0_CLK_H2 MA0_CLK_L2 MA0_CLK_H1 MA0_CLK_L1
Y16 AA16 F16 F16
M_A_CLK_DDR2 7
M_A_CLK_DDR2# 7
M_A_CLK_DDR1 7
M_A_CLK_DDR1# 7
MA0_CS_L3 MA0_CS_L2 MA0_CS_L1 MA0_CS_L0
V19 J22 V22 T19
M_A_CS3# 7,8
M_A_CS2# 7,8
M_A_CS1# 7,8
M_A_CS0# 7,8
MA0_ODT1 MA0_ODT0
V20 U19
M_A_ODT1 7,8
M_A_ODT0 7,8
MA_CAS_L MA_WE_L MA_RAS_L
U20 U21 T20
M_A_CAS# 7,8
M_A_WE# 7,8
M_A_RAS# 7,8
MA_BANK2 MA_BANK1 MA_BANK0
K22 R20 T22
M_A_BS#2 7,8
M_A_BS#1 7,8
M_A_BS#0 7,8
MA_CKE1 MA_CKE0
J20 J21
M_A_CKE1 7,8
M_A_CKE0 7,8
MA_ADD15 MA_ADD14 MA_ADD13 MA_ADD12 MA_ADD11 MA_ADD10 MA_ADD9 MA_ADD8 MA_ADD7 MA_ADD6 MA_ADD5 MA_ADD4 MA_ADD3 MA_ADD2 MA_ADD1 MA_ADD0
K19 K20 V24 K24 L20 R19 L19 L22 L21 M19 M20 M24 M22 N22 N21 R21
M_A_A15 M_A_A14 M_A_A13 M_A_A12 M_A_A11 M_A_A10 M_A_A9 M_A_A8 M_A_A7 M_A_A6 M_A_A5 M_A_A4 M_A_A3 M_A_A2 M_A_A1 M_A_A0
M_A_A[15..0] 7,8
MA_DQS_H7 MA_DQS_L7 MA_DQS_H6 MA_DQS_L6 MA_DQS_H5 MA_DQS_L5 MA_DQS_H4 MA_DQS_L4 MA_DQS_H3 MA_DQS_L3 MA_DQS_H2 MA_DQS_L2 MA_DQS_H1 MA_DQS_L1 MA_DQS_H0 MA_DQS_L0
W12 W13 Y15 W15 AB19 AB20 AD23 AC23 G22 G21 C22 C21 G16 G15 G13 H13
M_A_DQS7 M_A_DQS#7 M_A_DQS6 M_A_DQS#6 M_A_DQS5 M_A_DQS#5 M_A_DQS4 M_A_DQS#4 M_A_DQS3 M_A_DQS#3 M_A_DQS2 M_A_DQS#2 M_A_DQS1 M_A_DQS#1 M_A_DQS0 M_A_DQS#0
M_A_DQS[7..0] 7
M_A_DQS#[7..0] 7
MA_DM7 MA_DM6 MA_DM5 MA_DM4 MA_DM3 MA_DM2 MA_DM1 MA_DM0
Y13 AB16 Y19 AC24 F24 F19 C15 F12
M_A_DM7 M_A_DM6 M_A_DM5 M_A_DM4 M_A_DM3 M_A_DM2 M_A_DM1 M_A_DM0
M_A_DM[7..0] 7
CPU1C
MEMORY INTERFACE
7 M_B_DQ[63..0]
M_B_DQ63 AD11
M_B_DQ62 AF11
M_B_DQ61 AE14
M_B_DQ60 AE14
M_B_DQ59 Y11
M_B_DQ58 AB11
M_B_DQ57 AC12
M_B_DQ56 AE13
M_B_DQ55 AE15
M_B_DQ54 AF16
M_B_DQ53 AC18
M_B_DQ52 AF19
M_B_DQ51 AD14
M_B_DQ50 AC14
M_B_DQ49 AE18
M_B_DQ48 AD18
M_B_DQ47 AD20
M_B_DQ46 AC20
M_B_DQ45 AF23
M_B_DQ44 AF24
M_B_DQ43 AF20
M_B_DQ42 AE20
M_B_DQ41 AD22
M_B_DQ40 AC22
M_B_DQ39 AE25
M_B_DQ38 AD26
M_B_DQ37 AA25
M_B_DQ36 AA26
M_B_DQ35 AE24
M_B_DQ34 AD24
M_B_DQ33 AA23
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M_B_DQ31 G24
M_B_DQ30 G23
M_B_DQ29 D26
M_B_DQ28 C26
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M_B_DQ25 E24
M_B_DQ24 E23
M_B_DQ23 C24
M_B_DQ22 B24
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M_B_DQ20 B20
M_B_DQ19 C25
M_B_DQ18 D24
M_B_DQ17 A21
M_B_DQ16 D20
M_B_DQ15 D18
M_B_DQ14 C18
M_B_DQ13 D14
M_B_DQ12 C14
M_B_DQ11 A20
M_B_DQ10 A19
M_B_DQ9 A16
M_B_DQ8 A15
M_B_DQ7 A13
M_B_DQ6 D12
M_B_DQ5 E11
M_B_DQ4 G11
M_B_DQ3 B14
M_B_DQ2 A14
M_B_DQ1 A11
M_B_DQ0 C11
MB_DATA63 MB_DATA62 MB_DATA61 MB_DATA60 MB_DATA59 MB_DATA58 MB_DATA57 MB_DATA56 MB_DATA55 MB_DATA54 MB_DATA53 MB_DATA52 MB_DATA51 MB_DATA50 MB_DATA49 MB_DATA48 MB_DATA47 MB_DATA46 MB_DATA45 MB_DATA44 MB_DATA43 MB_DATA42 MB_DATA41 MB_DATA40 MB_DATA39 MB_DATA38 MB_DATA37 MB_DATA36 MB_DATA35 MB_DATA34 MB_DATA33 MB_DATA32 MB_DATA31 MB_DATA30 MB_DATA29 MB_DATA28 MB_DATA27 MB_DATA26 MB_DATA25 MB_DATA24 MB_DATA23 MB_DATA22 MB_DATA21 MB_DATA20 MB_DATA19 MB_DATA18 MB_DATA17 MB_DATA16 MB_DATA15 MB_DATA14 MB_DATA13 MB_DATA12 MB_DATA11 MB_DATA10 MB_DATA9 MB_DATA8 MB_DATA7 MB_DATA6 MB_DATA5 MB_DATA4 MB_DATA3 MB_DATA2 MB_DATA1 MB_DATA0
MB0_CLK_H2 MB0_CLK_L2 MB0_CLK_H1 MB0_CLK_L1
AF18 AF17 A17 A18
M_B_CLK_DDR2 7
M_B_CLK_DDR2# 7
M_B_CLK_DDR1 7
M_B_CLK_DDR1# 7
MB0_CS_L3 MB0_CS_L2 MB0_CS_L1 MB0_CS_L0
Y26 J24 W24 U23
M_B_CS3# 7,8
M_B_CS2# 7,8
M_B_CS1# 7,8
M_B_CS0# 7,8
MB0_ODT1 MB0_ODT0
W23 W26
M_B_ODT1 7,8
M_B_ODT0 7,8
MB_CAS_L MB_WE_L MB_RAS_L
V26 U22 U24
M_B_CAS# 7,8
M_B_WE# 7,8
M_B_RAS# 7,8
MB_BANK2 MB_BANK1 MB_BANK0
K26 T26 U26
M_B_BS#2 7,8
M_B_BS#1 7,8
M_B_BS#0 7,8
MB_CKE1 MB_CKE0
H26 J23
M_B_CKE1 7,8
M_B_CKE0 7,8
MB_ADD15 MB_ADD14 MB_ADD13 MB_ADD12 MB_ADD11 MB_ADD10 MB_ADD9 MB_ADD8 MB_ADD7 MB_ADD6 MB_ADD5 MB_ADD4 MB_ADD3 MB_ADD2 MB_ADD1 MB_ADD0
J25 J26 W25 L23 L25 U25 L24 M26 L26 N23 N24 N25 N26 P24 P26 T24
M_B_A15 M_B_A14 M_B_A13 M_B_A12 M_B_A11 M_B_A10 M_B_A9 M_B_A8 M_B_A7 M_B_A6 M_B_A5 M_B_A4 M_B_A3 M_B_A2 M_B_A1 M_B_A0
M_B_A[15..0] 7,8
MB_DQS_H7 MB_DQS_L7 MB_DQS_H6 MB_DQS_L6 MB_DQS_H5 MB_DQS_L5 MB_DQS_H4 MB_DQS_L4 MB_DQS_H3 MB_DQS_L3 MB_DQS_H2 MB_DQS_L2 MB_DQS_H1 MB_DQS_L1 MB_DQS_H0 MB_DQS_L0
AE12 AE12 AE16 AD16 AF21 AF22 AC25 AC26 F26 E26 A24 A23 D16 C16 C12 B12
M_B_DQS7 M_B_DQS#7 M_B_DQS6 M_B_DQS#6 M_B_DQS5 M_B_DQS#5 M_B_DQS4 M_B_DQS#4 M_B_DQS3 M_B_DQS#3 M_B_DQS2 M_B_DQS#2 M_B_DQS1 M_B_DQS#1 M_B_DQS0 M_B_DQS#0
M_B_DQS[7..0] 7
M_B_DQS#[7..0] 7
MB_DM7 MB_DM6 MB_DM5 MB_DM4 MB_DM3 MB_DM2 MB_DM1 MB_DM0
AD12 AC16 AE22 AB26 E25 A22 B16 A12
M_B_DM7 M_B_DM6 M_B_DM5 M_B_DM4 M_B_DM3 M_B_DM2 M_B_DM1 M_B_DM0
M_B_DM[7..0] 7
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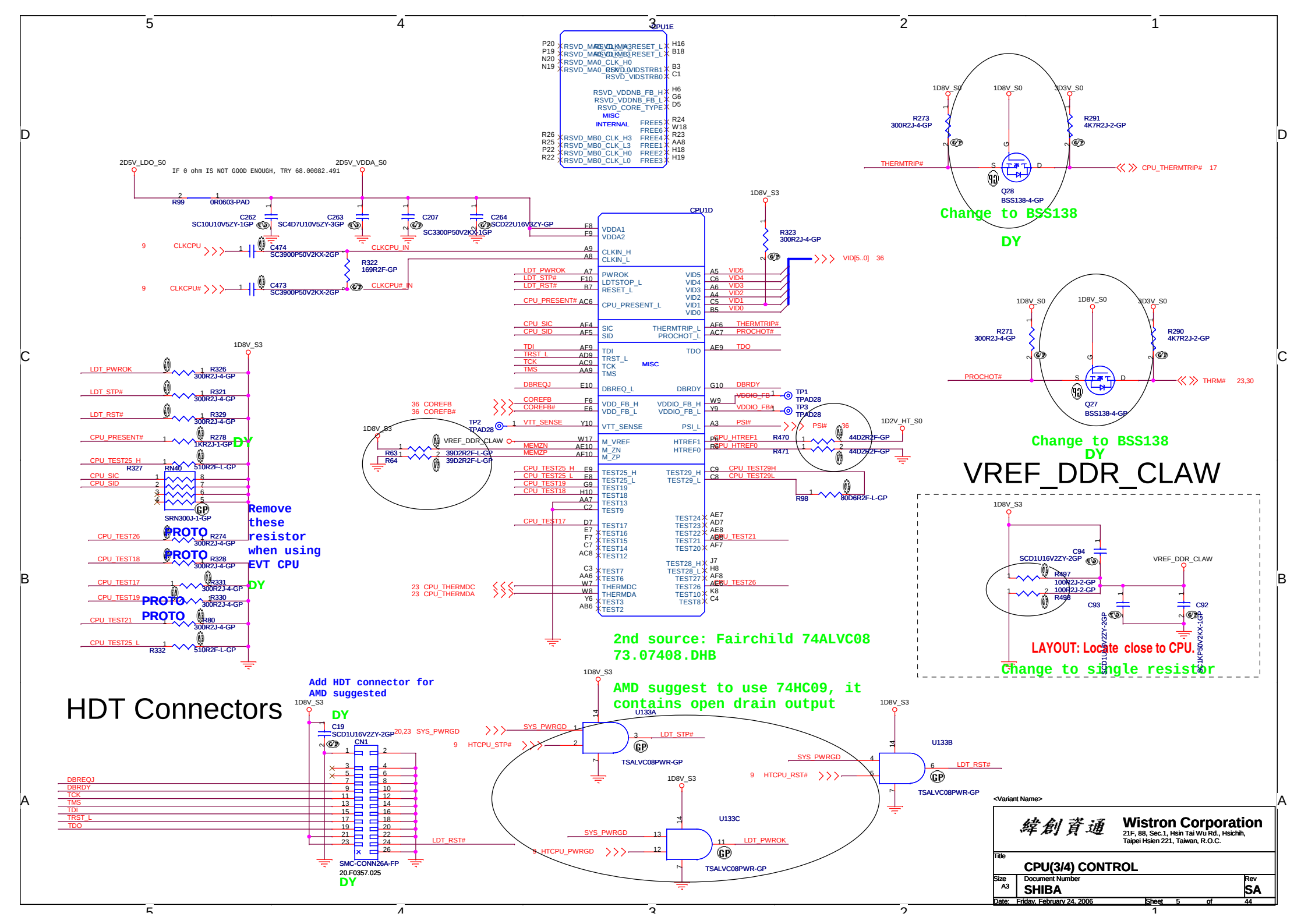
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(2/4) DDR II
Size A3
Document Number
SHIBA
Rev
SC
Date: Friday, February 24, 2006
Sheet 4 of 44


CPU1E
CPU1D
Change to BSS138
DY
VREF_DDR_CLAW
Change to BSS138
DY
Remove these resistor when using EVT CPU
DY
PROTO
2nd source: Fairchild 74ALVC08 73.07408.DHB
AMD suggest to use 74HC09, it contains open drain output
Add HDT connector for AMD suggested
HDT Connectors
LAYOUT: Locate close to CPU.
Change to single resistor
Wistron Corporation
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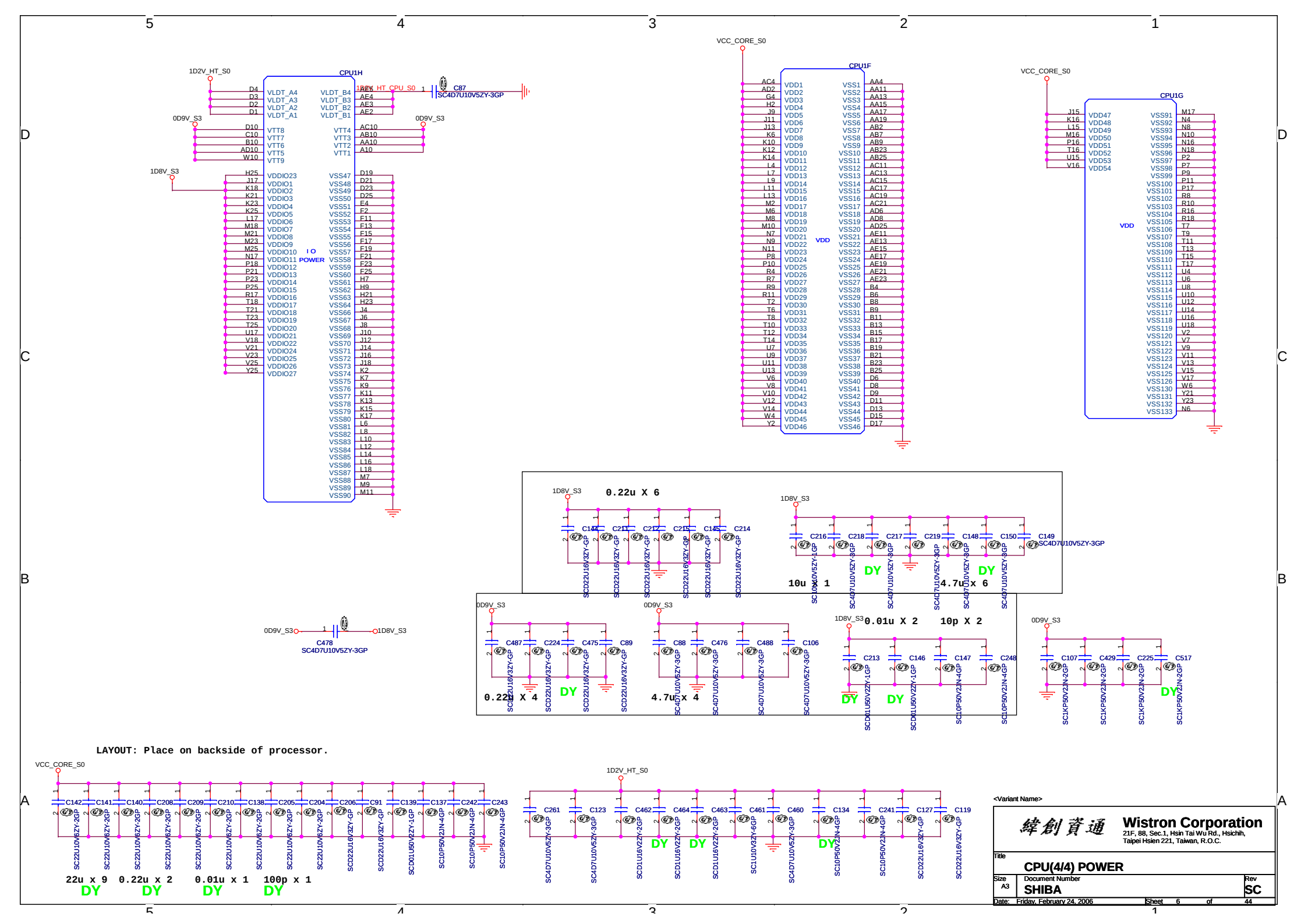
CPU(3/4) CONTROL
SHIBA
Friday, February 24, 2006


CPU1H
CPU1F
CPU1G
VCC_CORE_S0
1D2V_HT_S0
0D9V_S3
1D8V_S3
C87
SC4D7U10V5ZY-3GP
C478
SC4D7U10V5ZY-3GP
0.22u X 6
10u X 1
4.7u X 6
0.01u X 2
10p X 2
0.22u X 4
4.7u X 4
LAYOUT: Place on backside of processor.
22u x 9
0.22u x 2
0.01u x 1
100p x 1
DY
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
CPU(4/4) POWER
Size
A3
Document Number
SHIBA
Rev
SC
Date: Friday, February 24, 2006
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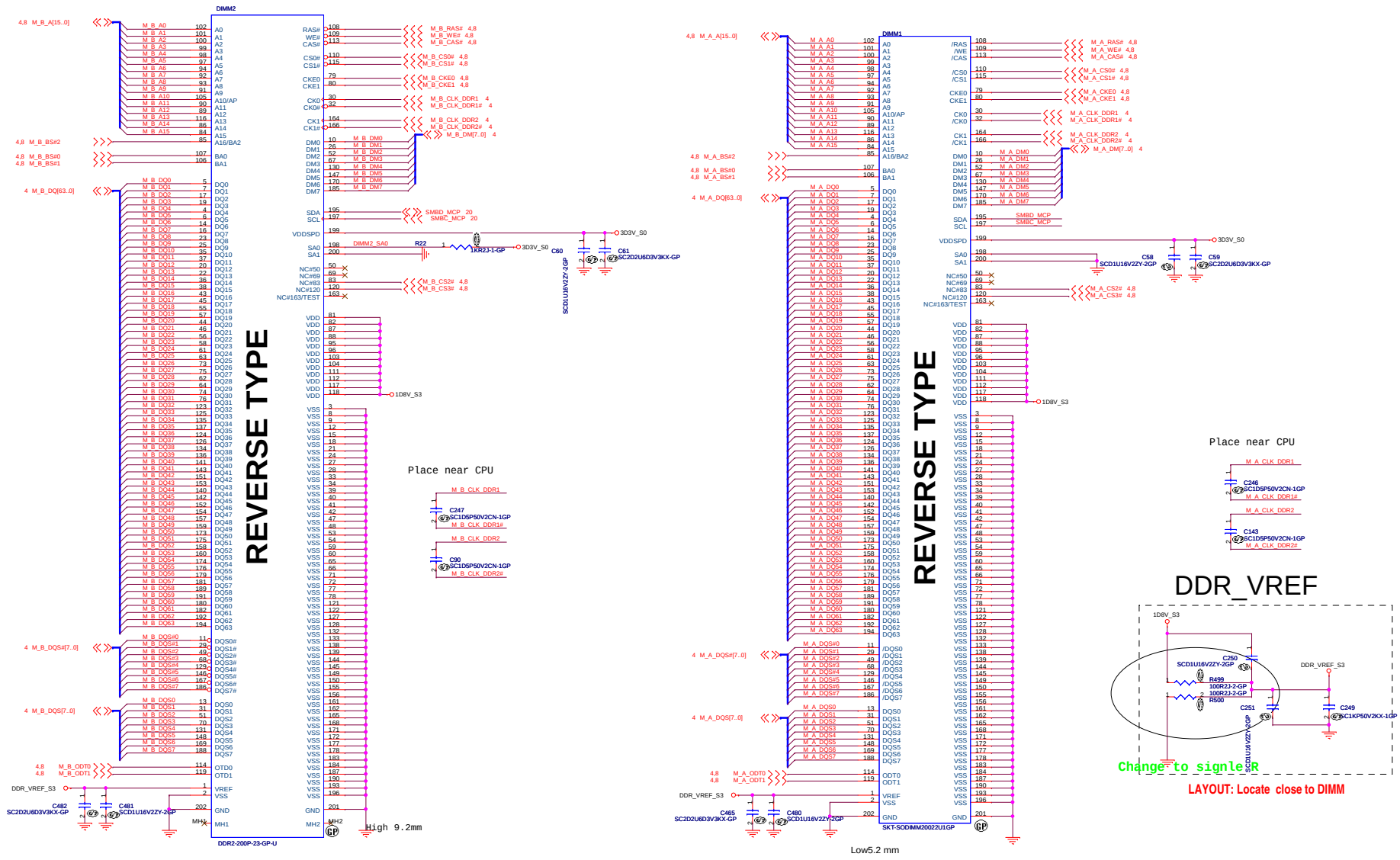

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2-SOCKET**

Size	Document Number	Rev
A2	SHIBA	SA

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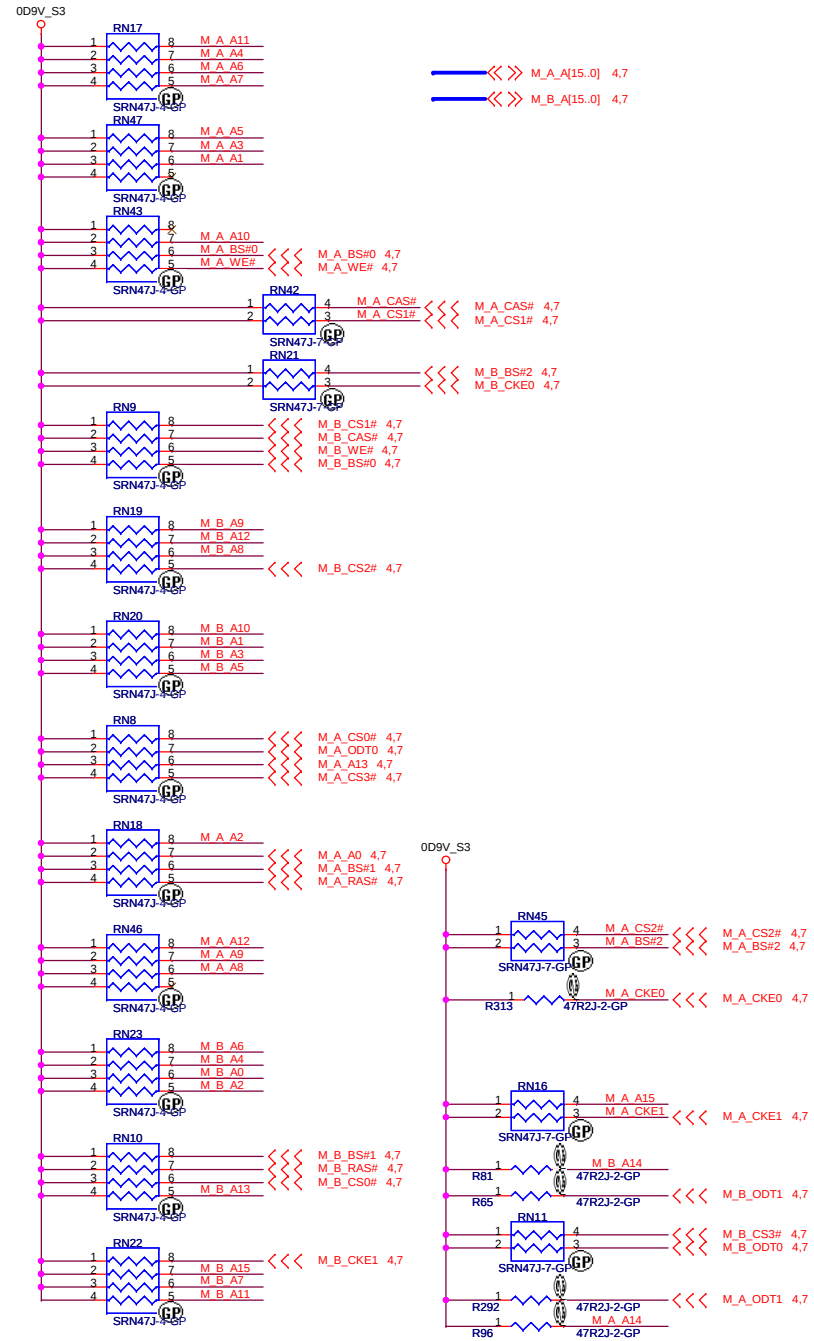
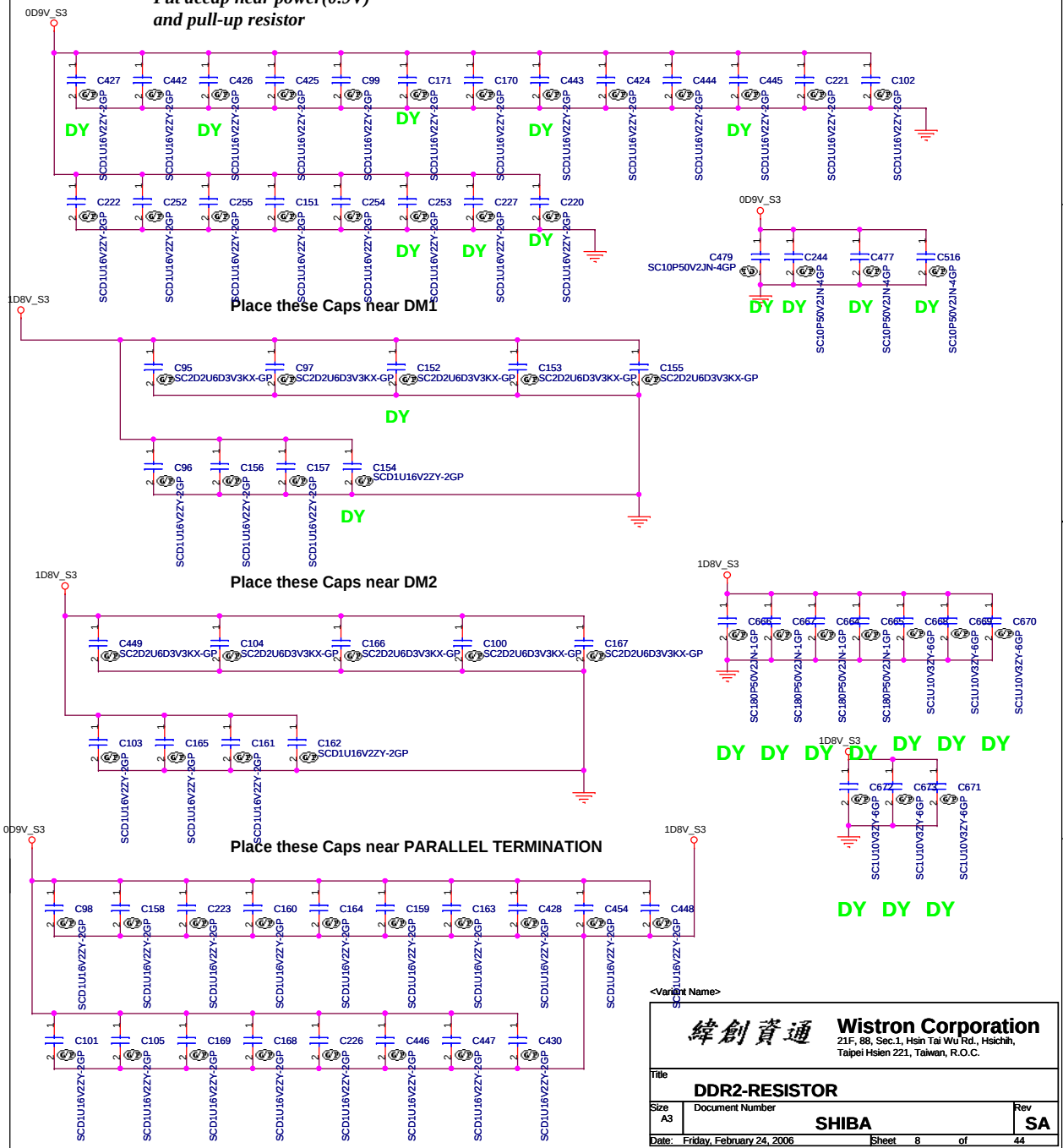
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

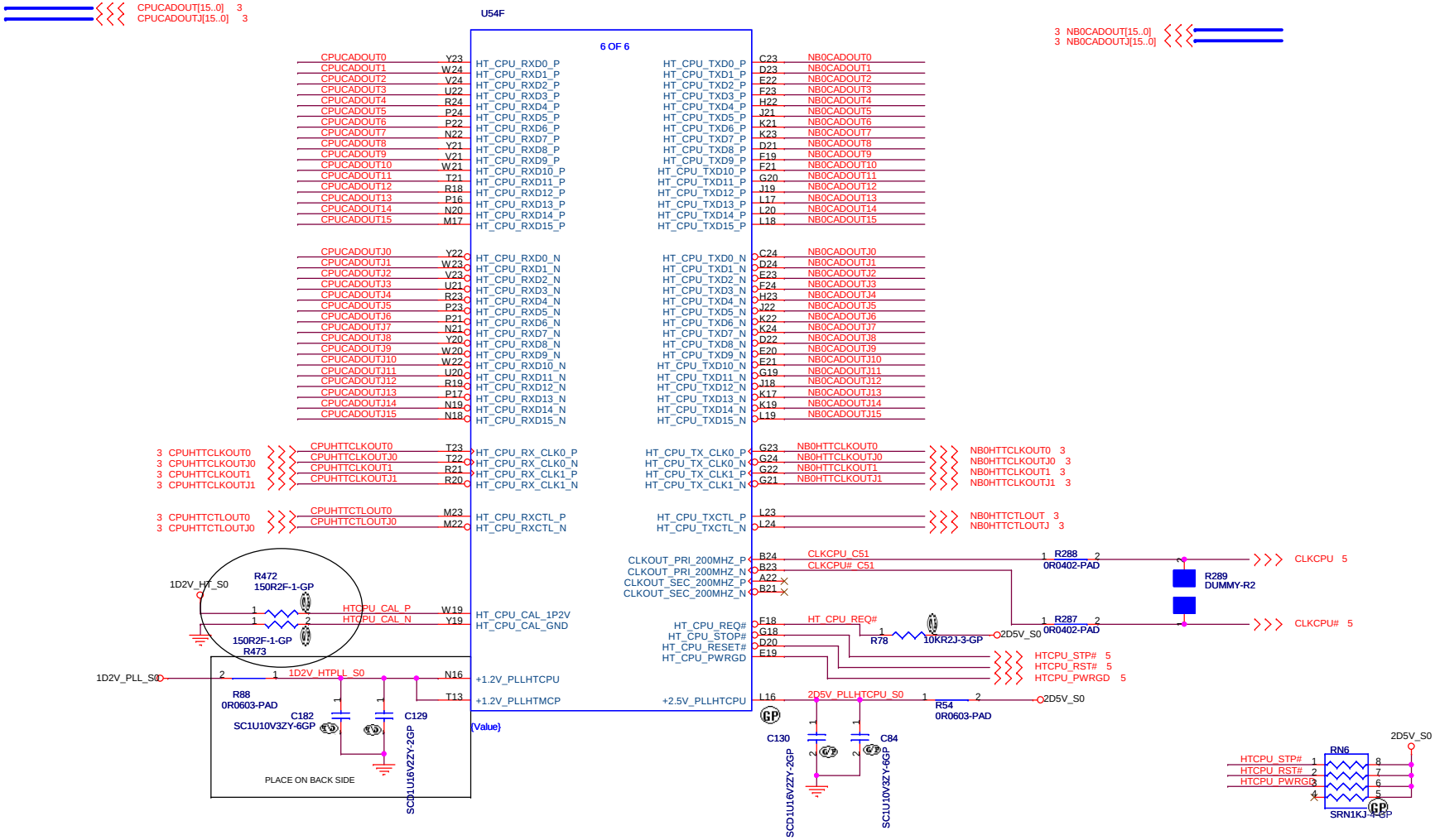
Put decap near power(0.9V) and pull-up resistor



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR2-RESISTOR	
Size A3	Document Number SHIBA	Rev SA
Date: Friday, February 24, 2006	Sheet 8 of 44	



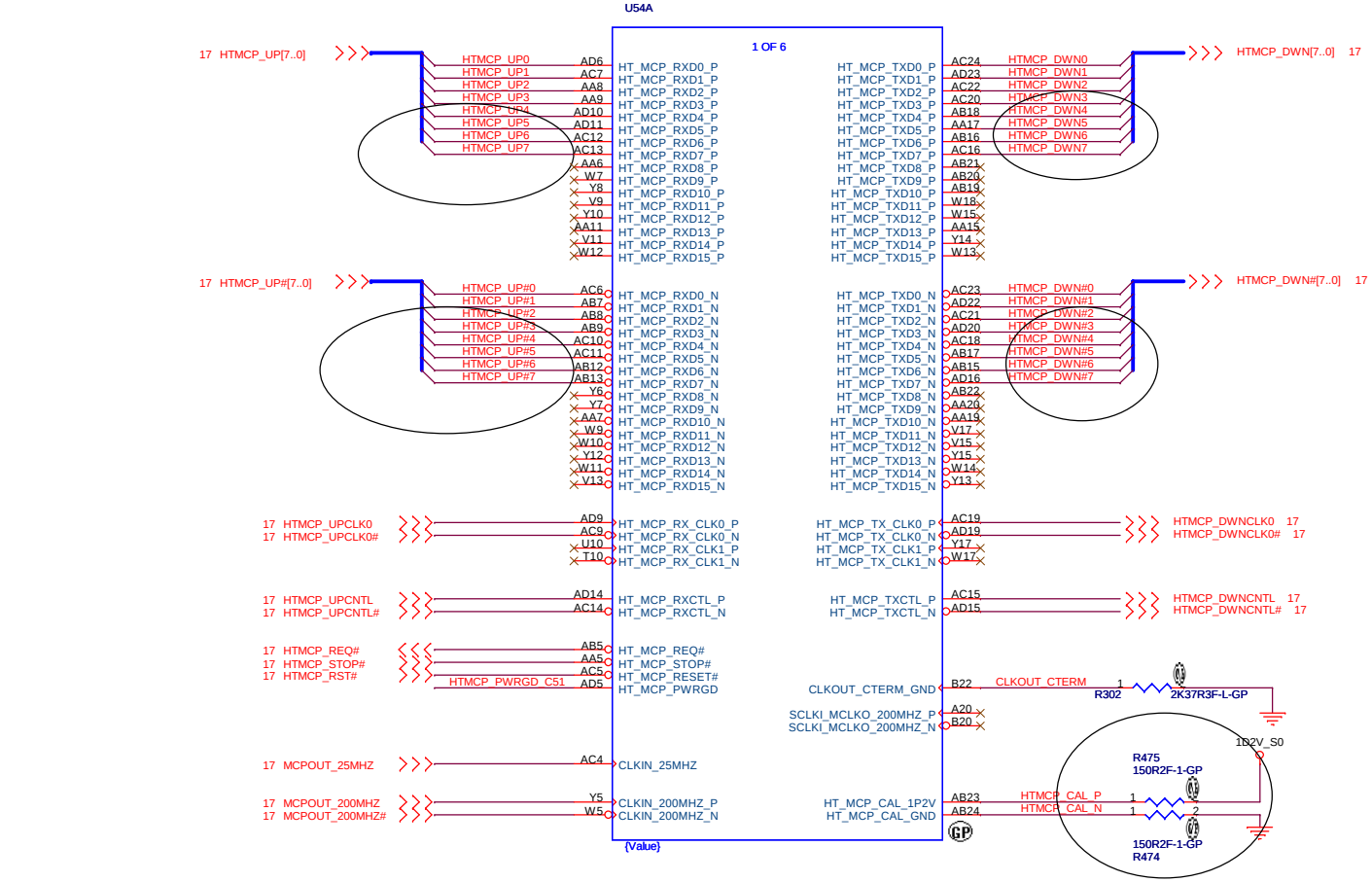
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: C51M(1/5) HT CPU

Size: A3 | Document Number: SHIBA | Rev: SC

Date: Friday, February 24, 2006 | Sheet 9 of 44



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **C51M(2/5)HT MCP**

Size	Document Number	Rev
A3	SHIBA	SC

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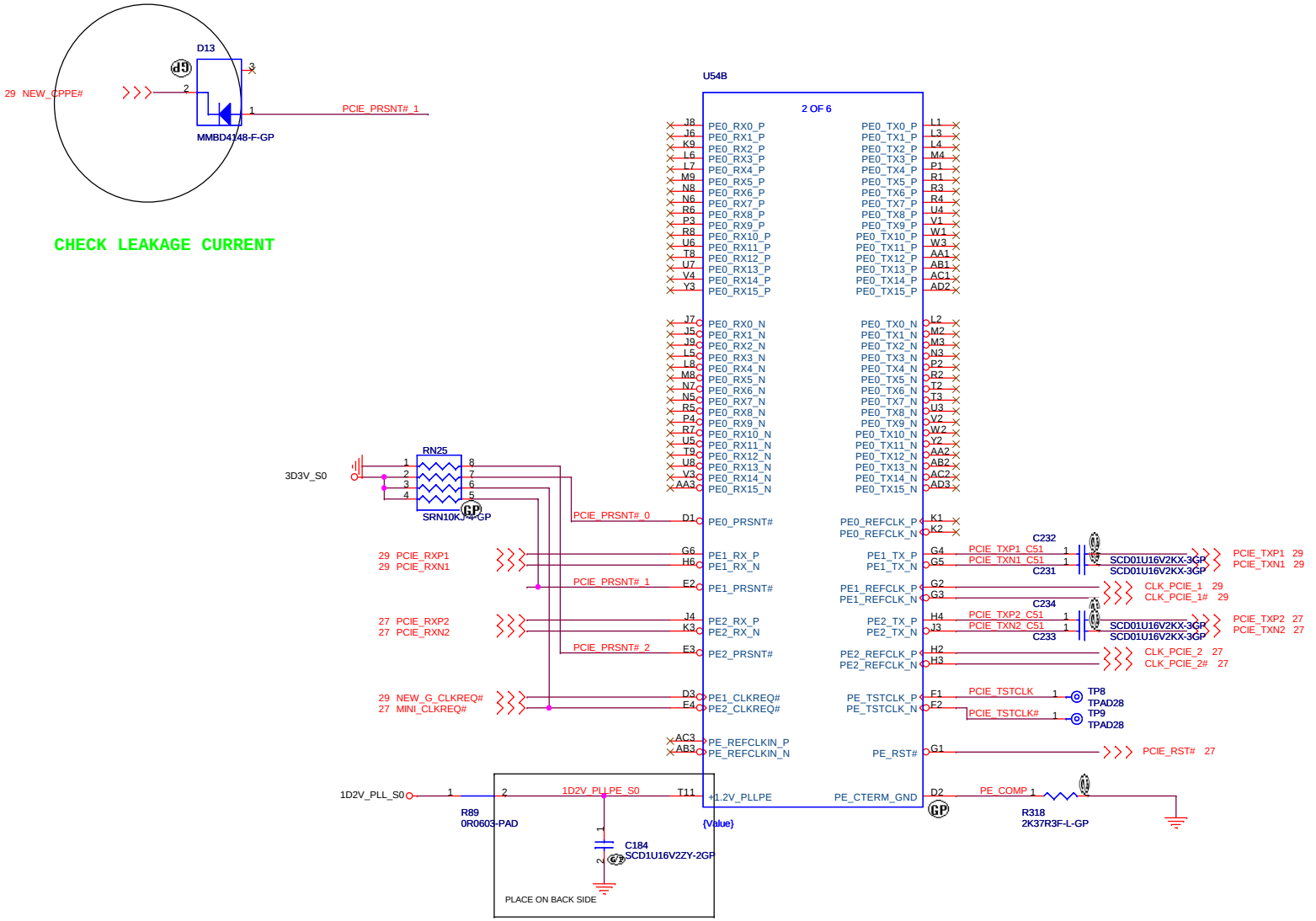

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **C51M(3/5)PCIE**

Size	Document Number	Rev
A3	SHIBA	SA

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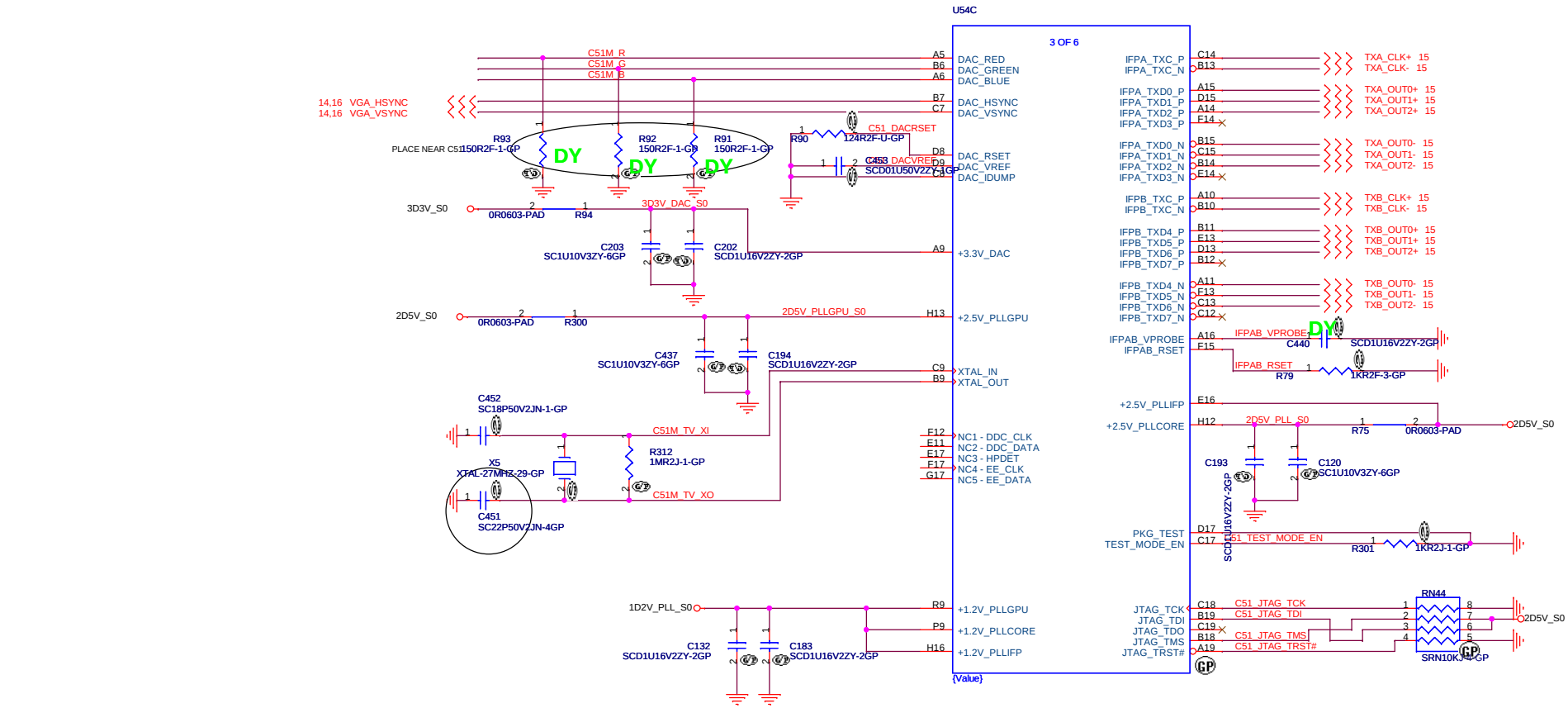


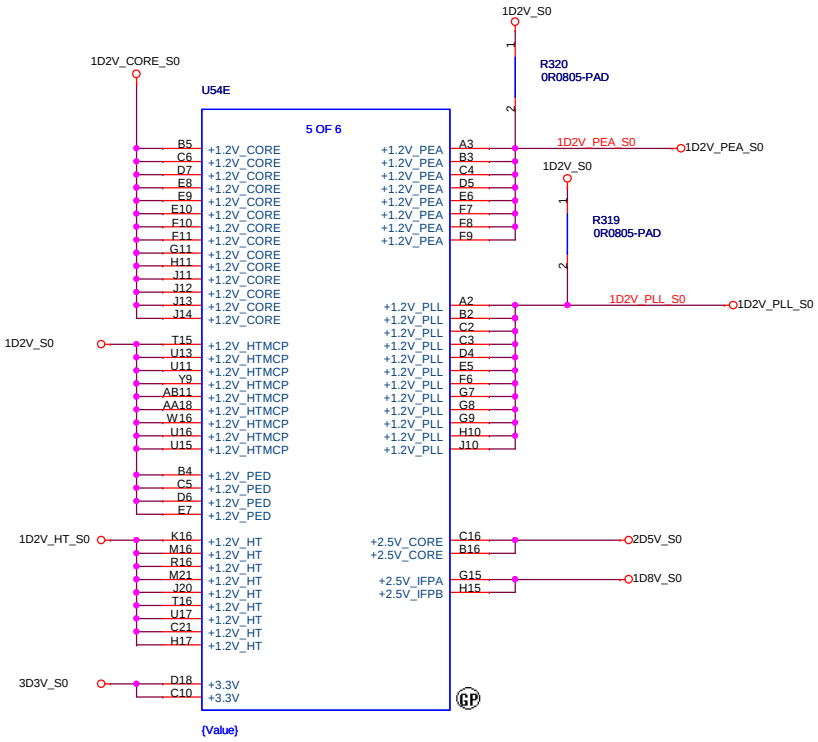
<Variant Name>

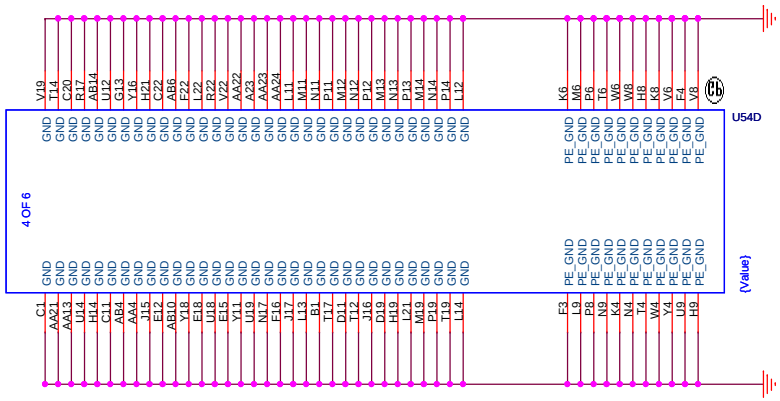
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **C51M(4/5)CRT/LVDS**

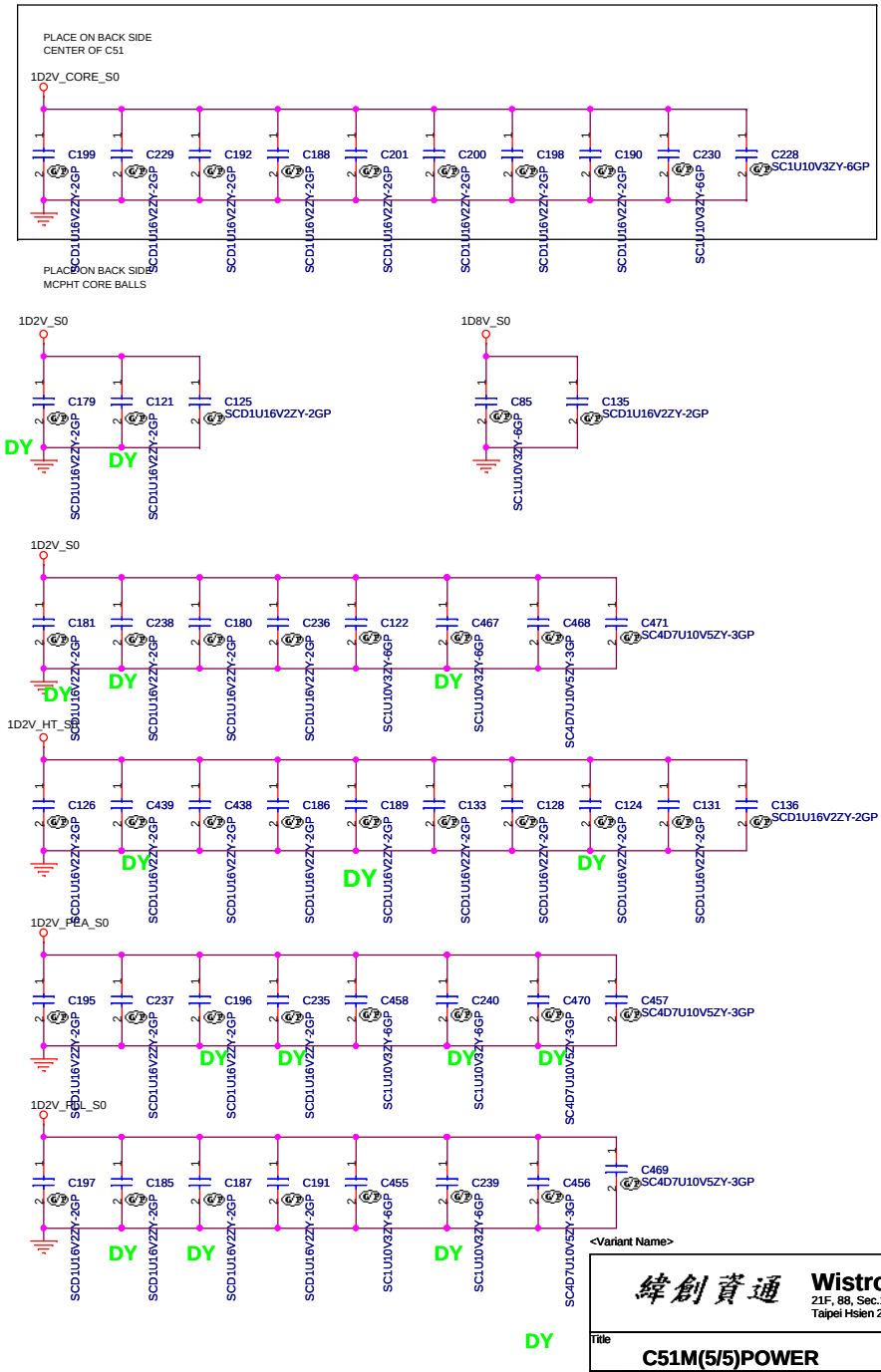
Size	Document Number	Rev
A3	SHIBA	SA

Date: Wednesday, March 15, 2006 Sheet 12 of 44





C51 DECOUPLING



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: C51M(5/5)POWER

Size: A3 | Document Number: SHIBA | Rev: SA

Date: Saturday, February 18, 2006 | Sheet 13 of 44

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

12 VGA_RED — L4 IND-68NH-1-GP — CRT_R — CRT_R 16
12 VGA_GREEN — L5 IND-68NH-1-GP — CRT_G — CRT_G 16
12 VGA_BLUE — L6 IND-68NH-1-GP — CRT_B — CRT_B 16

C22 SC10P50V2JN-4GP DY
C23 SC10P50V2JN-4GP DY
C25 SC10P50V2JN-4GP DY
C20 SC2P50V2CN-GP DY
C21 SC2P50V2CN-GP DY
C24 SC2P50V2CN-GP DY

E51_TXD

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

5V_CRT_S0 — F1 FUSE-1D1A6V-9GP — 5V_CRT_S0_D — D7 CH751H-40PT-1GP — 5V_S0
C16 SCD01U16V2KX-3GP DY

CRT1 VIDEO-15-57-GP-U
CRT_R, CRT_G, CRT_B
E51_RXD
DDC_DATA_CON
JVGA_HS
JVGA_VS
DDC_CLK_CON

RN1 SRN2K7J-3-GP

C13 SC33P50V2JN-3GP DY
C17 SC33P50V2JN-3GP DY
C15 SC22P50V2JN-4GP DY
C14 SC22P50V2JN-4GP DY

5V_CRT_S0
D5 BAV99TP-1-GP — DDC_DATA_CON
D6 BAV99TP-1-GP — DDC_CLK_CON

Hsync & Vsync level shift

5V_S0
C67 SCD1U16V2ZY-2GP
PR_INSERT 16
12,16 VGA_HSYNC — HSYNC_5 — U12B TSAHCT125PW-GP
12,16 VGA_VSYNC — VSYNC_5 — U12A TSAHCT125PW-GP
RN3 SRN33J-5-GP-U — JVGA_HS_L, JVGA_VS_L

5V_CRT_S0
JVGA_HS, CRT_R, JVGA_VS
U1 PACDN009MR-GP-U — CRT_G, CRT_R, CRT_B
DY

3D3V_S0
RN2 SRN2K7J-3-GP
20 DDC_VGA_5V_DAT — DDC_DATA_CON 16
16 DDC_CLK_CON — DDC_VGA_5V_CLK 20
U4 2N7002DW-7F-GP
C36 SCD1U16V2ZY-2GP DY
C37 SCD1U16V2ZY-2GP DY

5V @ ext. CRT side

TV OUT CONN

Layout Note:
Place this 2 resistors close to the TV-out connector

JVGA_HS_L — L7 0R0402-PAD — JVGA_HS
JVGA_VS_L — L8 0R0402-PAD — JVGA_VS

Thr org part is 68.2703N.10B

12 VGA_TV_CRMA — C8 SC8P250V2CC-GP — L1 IND-D56UH-16-GP — TV_CRMA 16
C11 SC82P50V2JN-3GP
C6 SC82P50V2JN-3GP

12 VGA_TV_COMP — C7 SC8P250V2CC-GP — L2 IND-D56UH-16-GP — TV_COMP 16
C10 SC82P50V2JN-3GP
C4 SC82P50V2JN-3GP

12 VGA_TV_LUMA — C9 SC8P250V2CC-GP — L3 IND-D56UH-16-GP — TV_LUMA 16
C12 SC82P50V2JN-3GP
C5 SC82P50V2JN-3GP

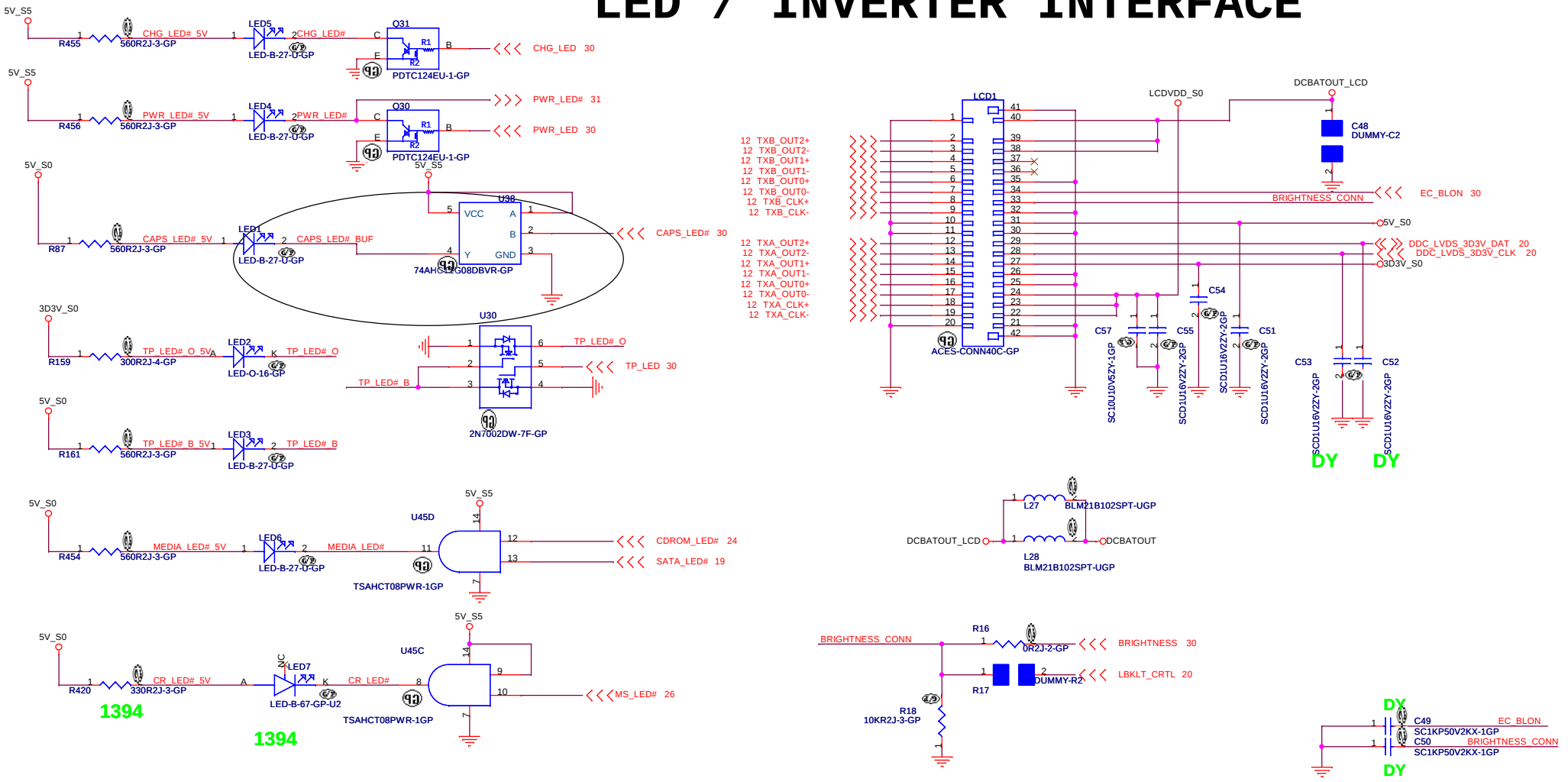
TV1 MINDIN7-16-GP
TV_LUMA, TV_CRMA, TV_COMP
LUMA, CRMA, COMP, NC#2, NC#5, GND

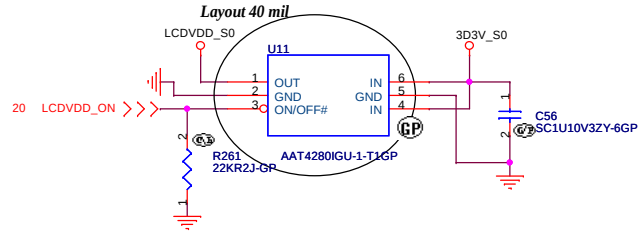
3D3V_S0
TV_COMP — D3 BAV99TP-1-GP — C1 SCD1U16V2ZY-2GP DY
TV_LUMA — D1 BAV99TP-1-GP — C2 SCD1U16V2ZY-2GP DY
TV_CRMA — D2 BAV99TP-1-GP — C3 SCD1U16V2ZY-2GP DY

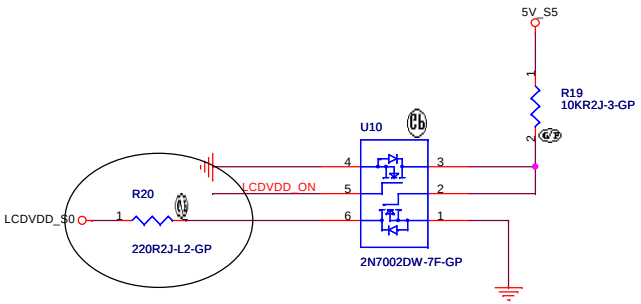
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT/TV CONNECTOR		
Size A3	Document Number SHIBA		Rev SA
Date: Thursday, February 23, 2006		Sheet 14 of 44	

LED / INVERTER INTERFACE

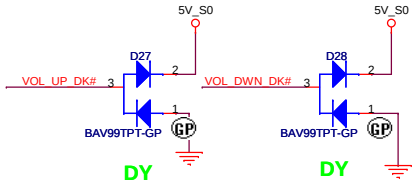




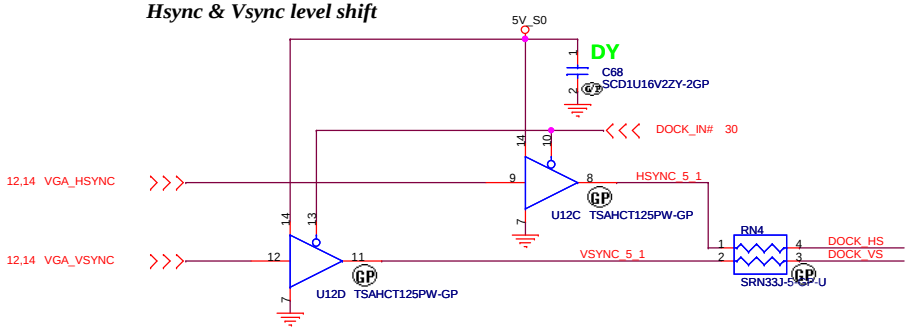


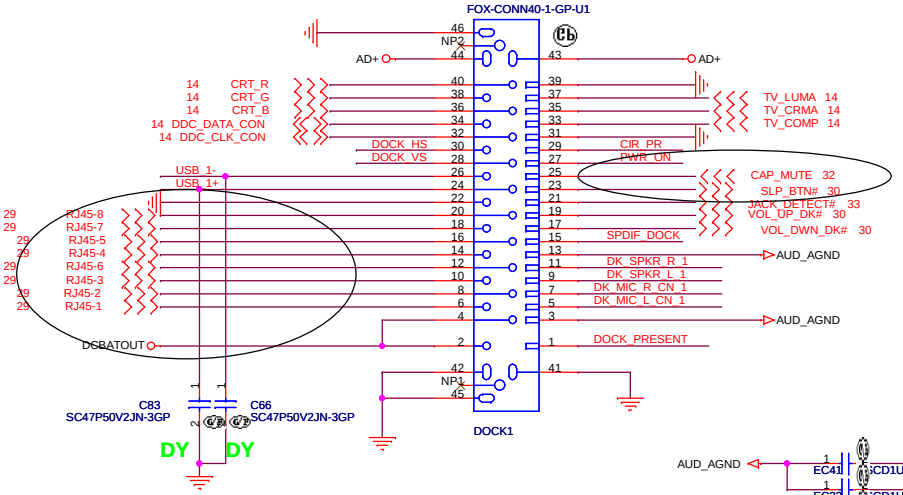
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD/Inverter Connector		
Size: Custom	Document Number: SHIBA	Rev: SA
Date: Friday, February 24, 2006	Sheet 15 of 44	

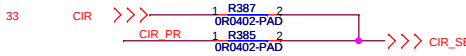
Docking Connector

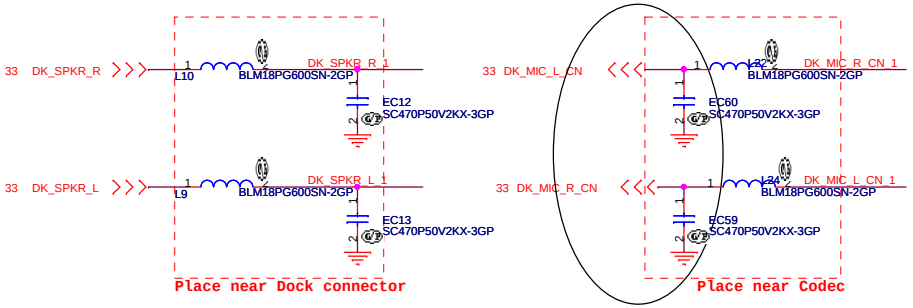


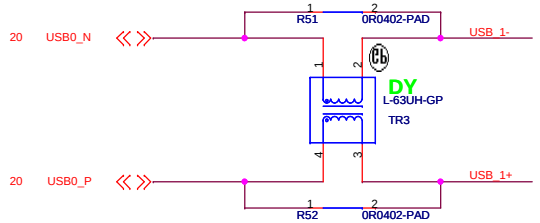
Hsync & Vsync level shift

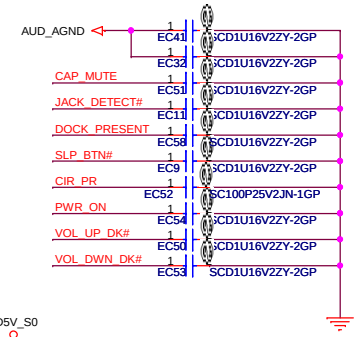


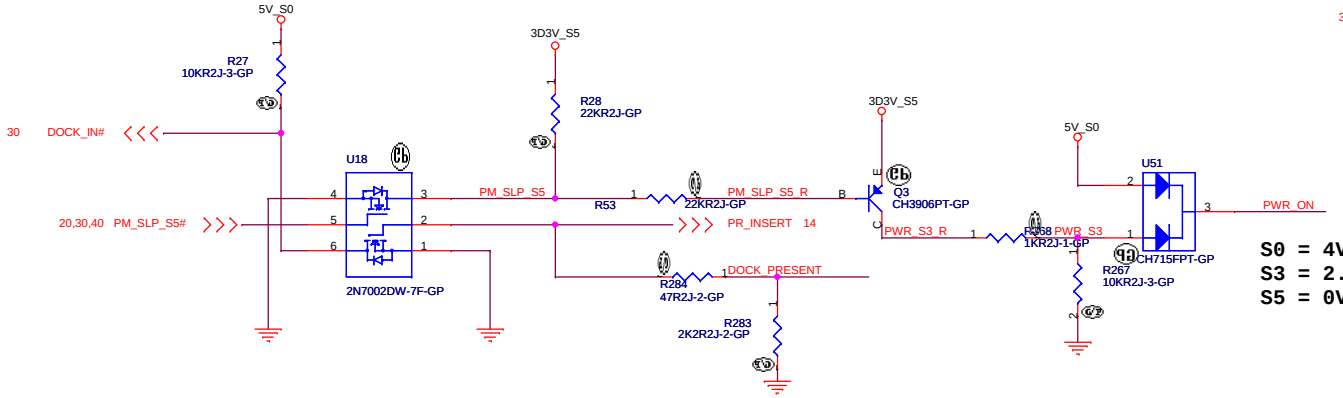




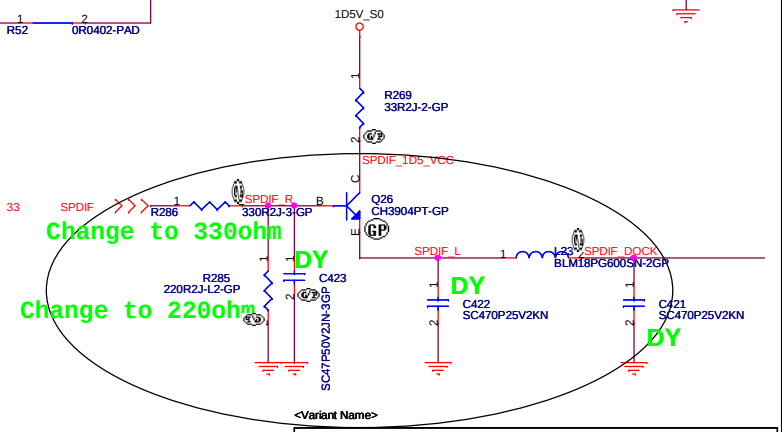








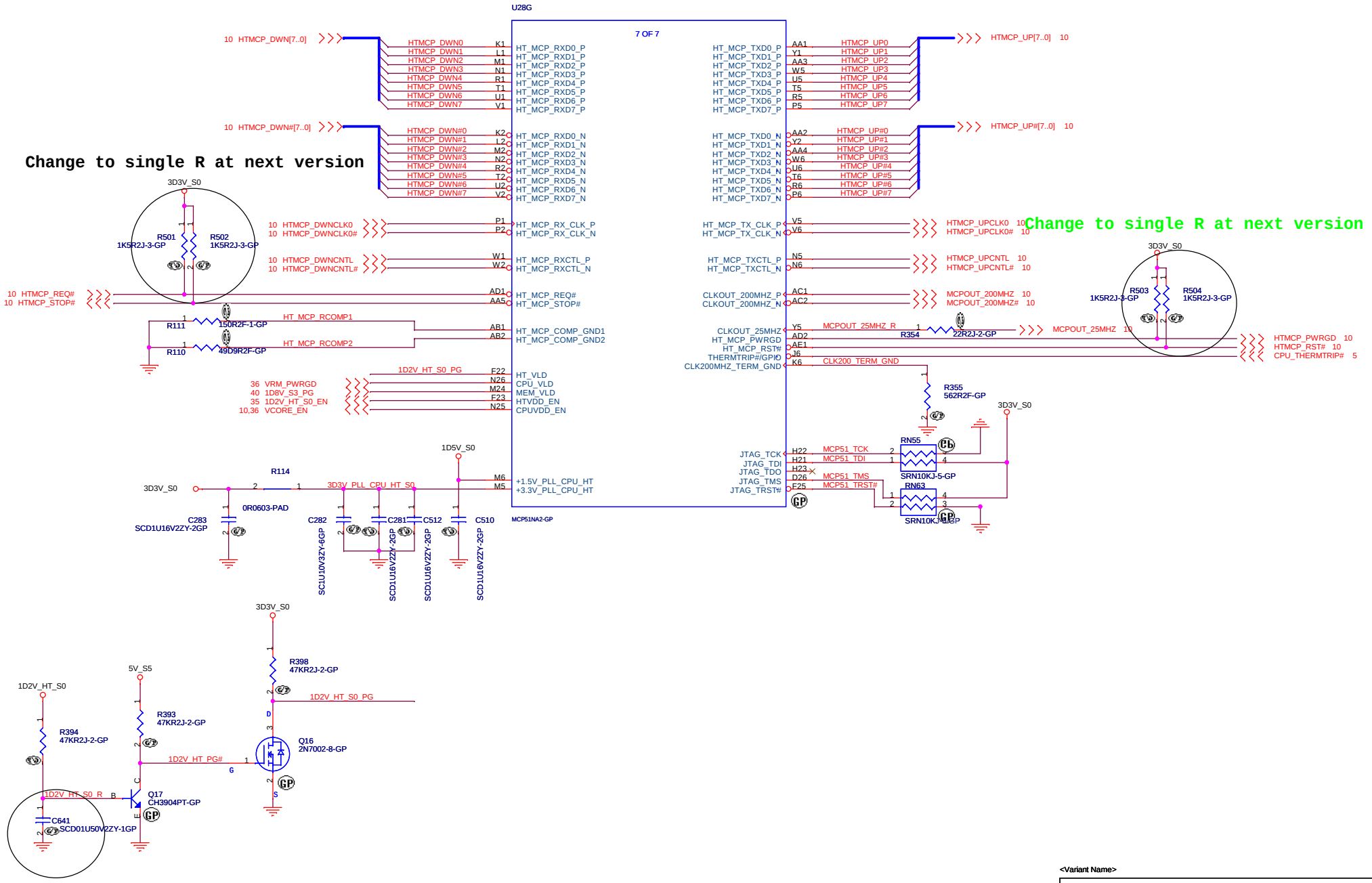
S0 = 4V
S3 = 2.5V
S5 = 0V



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Board to board conn/ Docking	
Size A3	Document Number SHIBA	Rev SA
Date: Monday, February 27, 2006	Sheet 16 of 44	



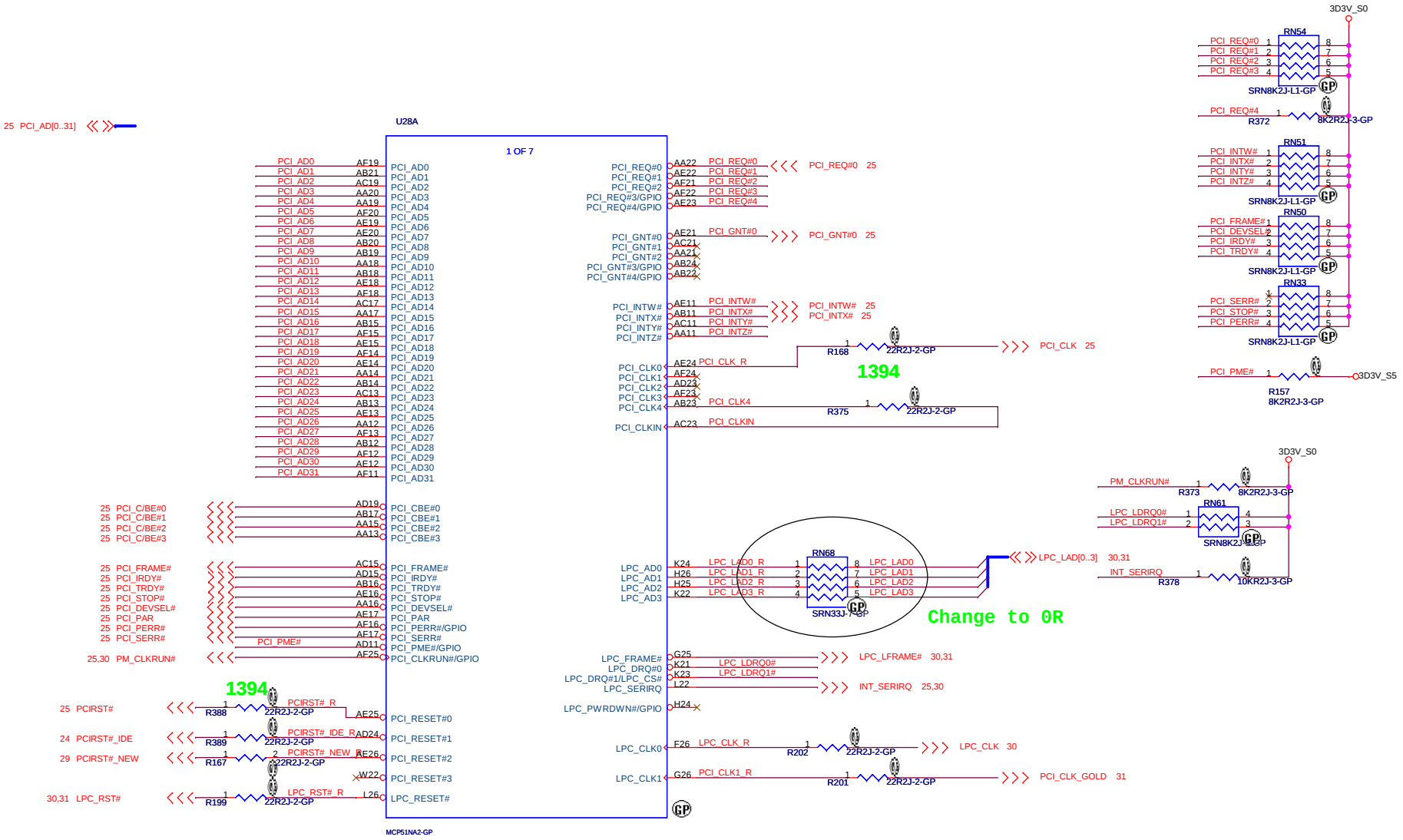
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(1/6)HT**

Size	Document Number	Rev
A3	SHIBA	SA

Date: Monday, February 20, 2006 Sheet 17 of 44



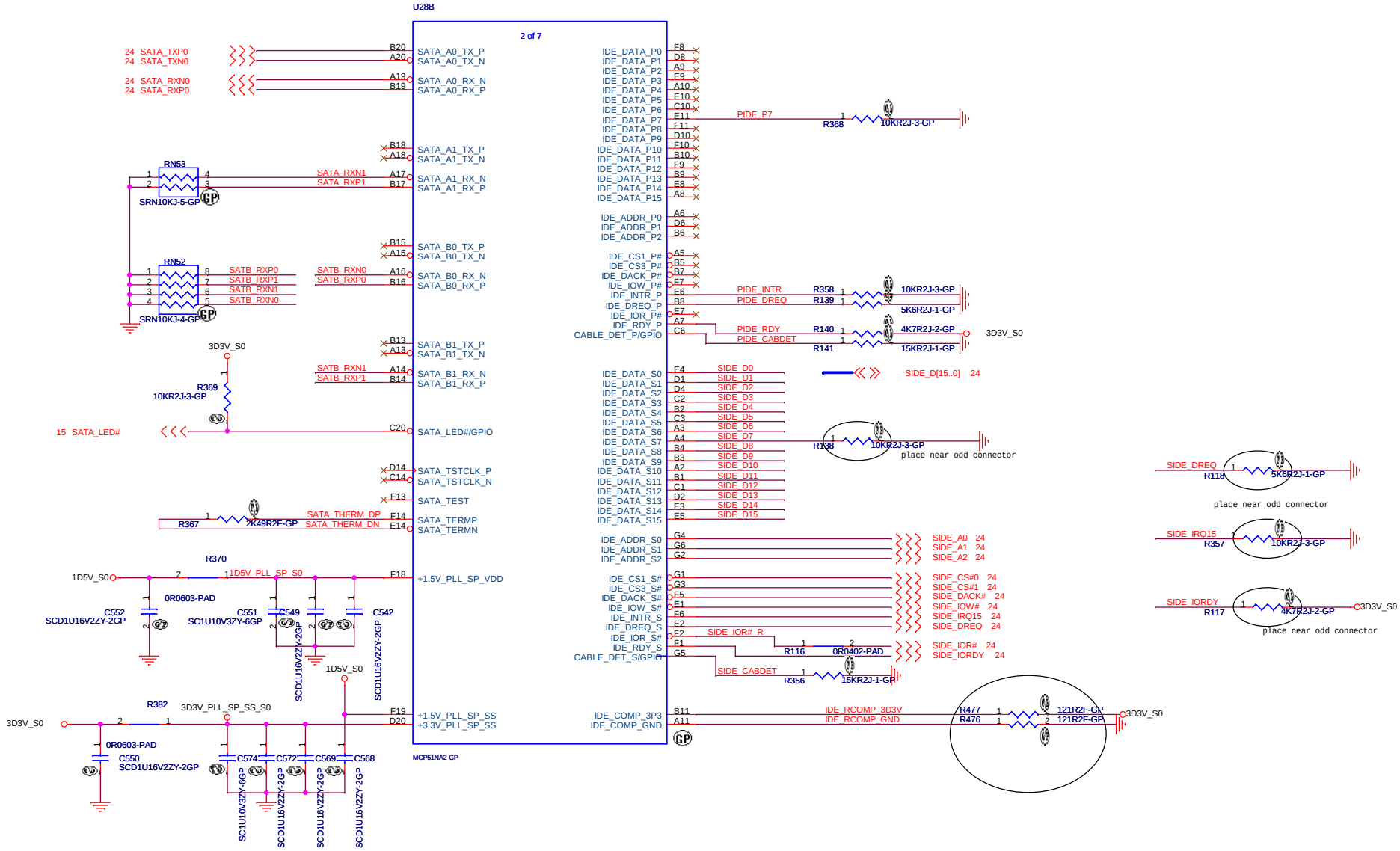
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP51(2/6)PCI

Size	Document Number	Rev
A3	SHIBA	SA

Date: Monday, February 20, 2006 Sheet 18 of 44



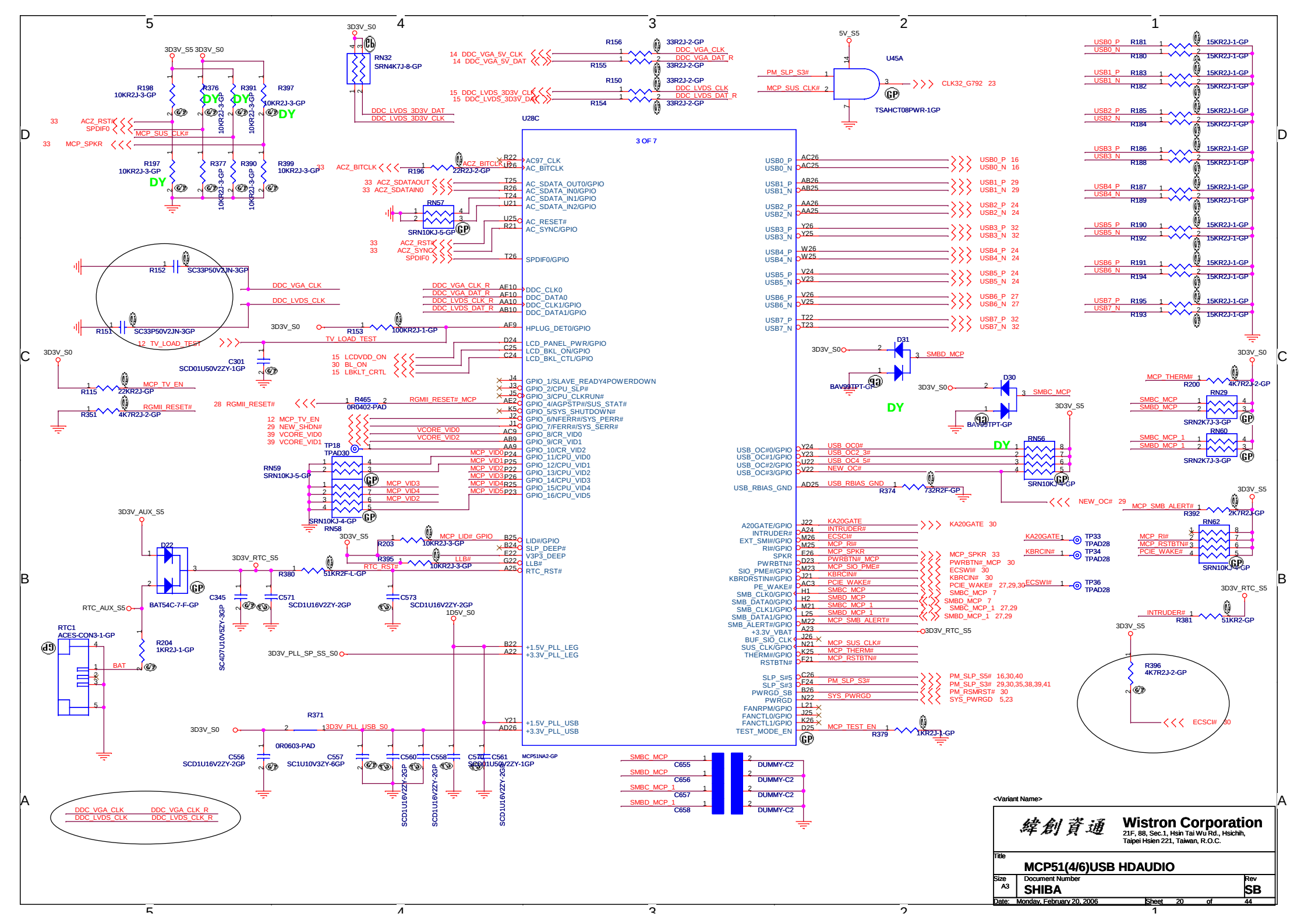
<Variant Name>

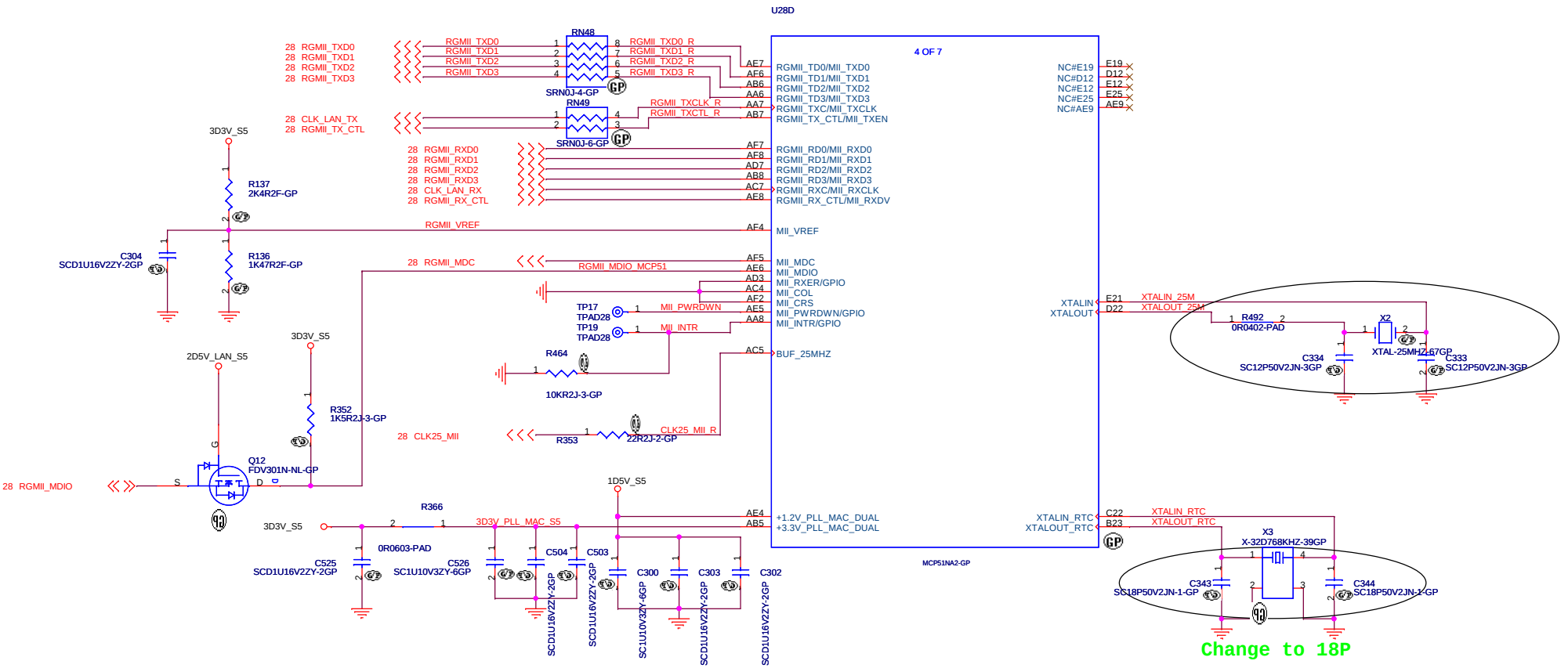
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(3/6)SATA/PATA**

Size	Document Number	Rev
A3	SHIBA	SA

Date: Monday, February 20, 2006 Sheet 19 of 44


U28C
3 OF 7
MCP51NA2-GP
U45A
TSAHCT08PWR-1GP
RN32 SRN4K7J-8-GP
RN57 SRN10KJ-5-GP
RN59 SRN10KJ-5-GP
RN58 SRN10KJ-4-GP
RN56 SRN10KJ-4-GP
RN29 SRN2K7J-3-GP
RN60 SRN2K7J-3-GP
RN62 SRN10KJ-4-GP
RTC1 ACES-CON3-1-GP
D22 BAT54C-7-F-GP
D31 BAV99TPT-GP
D30 BAV99TPT-GP
TP18 TPAD30
TP33 TPAD28
TP34 TPAD28
TP36 TPAD28
R152 SC33P50V2JN-3GP
R151 SC33P50V2JN-3GP
R153 100KR2J-1-GP
R196 22R2J-2-GP
R156 33R2J-2-GP
R155 33R2J-2-GP
R150 33R2J-2-GP
R154 33R2J-2-GP
R465 0R0402-PAD
R371 0R0603-PAD
R380 51KR2F-L-GP
R374 732R2F-GP
R379 1KR2J-1-GP
R396 4K7R2J-2-GP
R200 4K7R2J-2-GP
R392 2K7R2J-GP
R381 51KR2-GP
C301 SCD01U50V2ZY-1GP
C345 SC4D7U10V5ZY-3GP
C571 SCD1U16V2ZY-2GP
C573 SCD1U16V2ZY-2GP
C556 SCD01U16V2ZY-2GP
C557 SC1U10V3ZY-6GP
C560 SCD1U16V2ZY-2GP
C558 SCD1U16V2ZY-2GP
C570 SCD1U16V2ZY-2GP
C561 SCD01U50V2ZY-1GP
C655 DUMMY-C2
C656 DUMMY-C2
C657 DUMMY-C2
C658 DUMMY-C2
3D3V_S0
3D3V_S5
3D3V_AUX_S5
3D3V_RTC_S5
3D3V_PLL_SP_SS_S0
3D3V_PLL_USB_S0
1D5V_S0
5V_S5
DDC_VGA_CLK
DDC_LVDS_CLK
DDC_VGA_CLK_R
DDC_LVDS_CLK_R
MCP_SUS_CLK#
MCP_SPKR
ACZ_RST#
SPDIF0
ACZ_BITCLK
ACZ_SDATAOUT
ACZ_SDATAIN0
ACZ_SYNC
TV_LOAD_TEST
MCP_TV_EN
RGMII_RESET#
RGMII_RESET#_MCP
NEW_SHDN#
VCORE_VID0
VCORE_VID1
VCORE_VID2
MCP_VID0
MCP_VID1
MCP_VID2
MCP_VID3
MCP_VID4
MCP_VID5
MCP_LID#_GPIO
LLB#
RTC_RST#
RTC_AUX_S5
BAT
LCDVDD_ON
BL_ON
LBKLT_CRTL
SMBC_MCP
SMBD_MCP
SMBC_MCP_1
SMBD_MCP_1
MCP_SMB_ALERT#
KA20GATE
INTRUDER#
ECSCI#
MCP_RI#
MCP_SPKR
PWRBTN#_MCP
MCP_SIO_PME#
KBRCIN#
PCIE_WAKE#
MCP_SUS_CLK#
MCP_THERM#
MCP_RSTBTN#
PM_SLP_S3#
SYS_PWRGD
MCP_TEST_EN
NEW_OC#
USB_OC0#
USB_OC2_3#
USB_OC4_5#
USB_RBIAS_GND
ECSWI#
CLK32_G792
DDC_VGA_5V_CLK
DDC_VGA_5V_DAT
DDC_LVDS_3D3V_CLK
DDC_LVDS_3D3V_DAT
DDC_VGA_CLK
DDC_VGA_DAT_R
DDC_LVDS_CLK
DDC_LVDS_DAT_R
PM_SLP_S3#
PM_SLP_S5#
PM_RSMRST#
SYS_PWRGD
AC97_CLK
AC_BITCLK
AC_SDATA_OUT0/GPIO
AC_SDATA_IN0/GPIO
AC_SDATA_IN1/GPIO
AC_SDATA_IN2/GPIO
AC_RESET#
AC_SYNC/GPIO
SPDIF0/GPIO
DDC_CLK0
DDC_DATA0
DDC_CLK1/GPIO
DDC_DATA1/GPIO
HPLUG_DET0/GPIO
LCD_PANEL_PWR/GPIO
LCD_BKL_ON/GPIO
LCD_BKL_CTL/GPIO
GPIO_1/SLAVE_READY4POWERDOWN
GPIO_2/CPU_SLP#
GPIO_3/CPU_CLKRUN#
GPIO_4/AGPSTP#/SUS_STAT#
GPIO_5/SYS_SHUTDOWN#
GPIO_6/NFERR#/SYS_PERR#
GPIO_7/FERR#/SYS_SERR#
GPIO_8/CR_VID0
GPIO_9/CR_VID1
GPIO_10/CR_VID2
GPIO_11/CPU_VID0
GPIO_12/CPU_VID1
GPIO_13/CPU_VID2
GPIO_14/CPU_VID3
GPIO_15/CPU_VID4
GPIO_16/CPU_VID5
LID#/GPIO
SLP_DEEP#
V3P3_DEEP
LLB#
RTC_RST#
+1.5V_PLL_LEG
+3.3V_PLL_LEG
+1.5V_PLL_USB
+3.3V_PLL_USB
USB0_P
USB0_N
USB1_P
USB1_N
USB2_P
USB2_N
USB3_P
USB3_N
USB4_P
USB4_N
USB5_P
USB5_N
USB6_P
USB6_N
USB7_P
USB7_N
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MCP51(4/6)USB HDAUDIO
Size A3
Document Number SHIBA
Rev SB
Date: Monday, February 20, 2006
Sheet 20 of 44



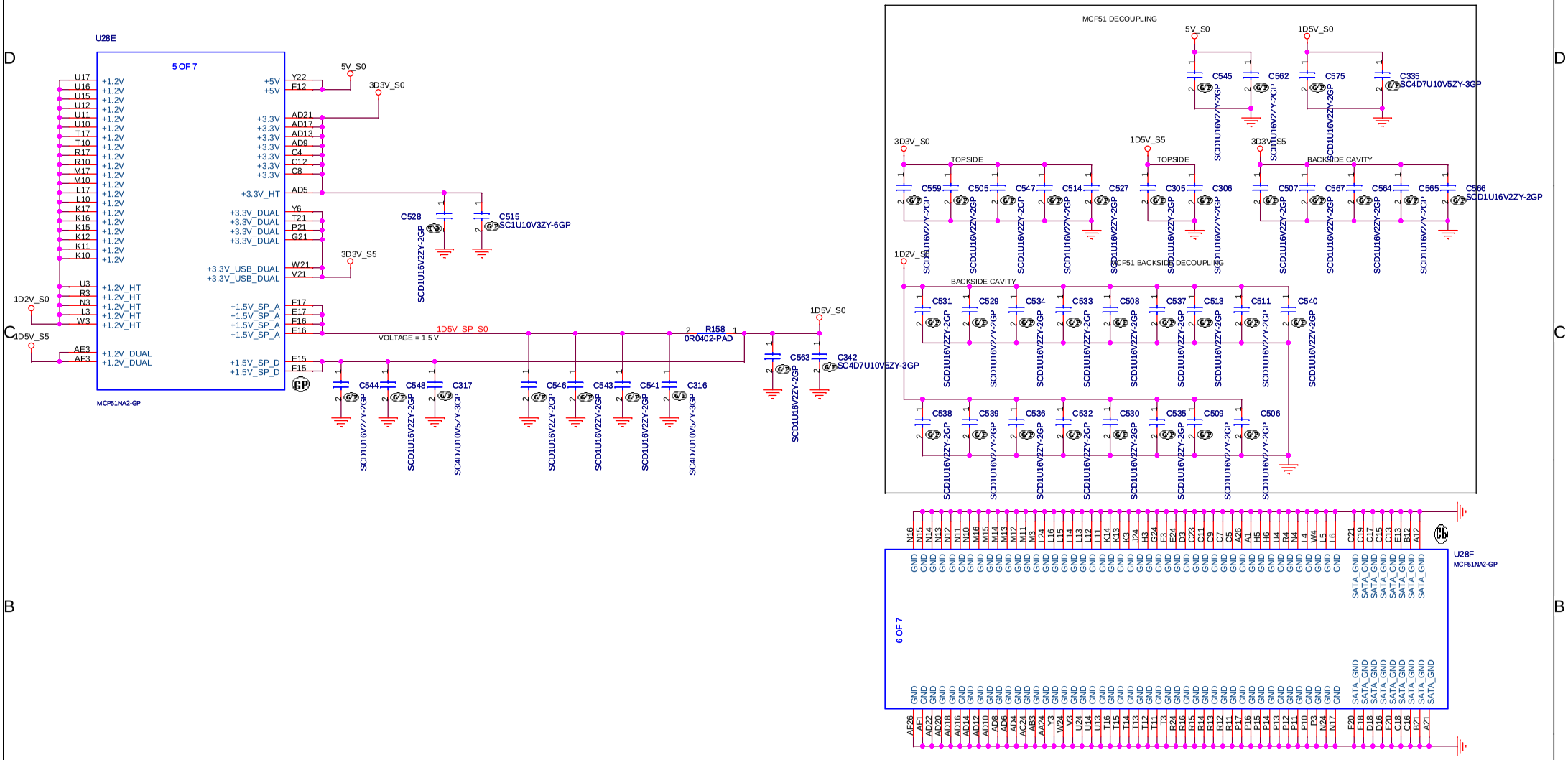
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(5/6)RGMII**

Size	Document Number	Rev
A3	SHIBA	SB

Date: Monday, February 20, 2006 Sheet 21 of 44



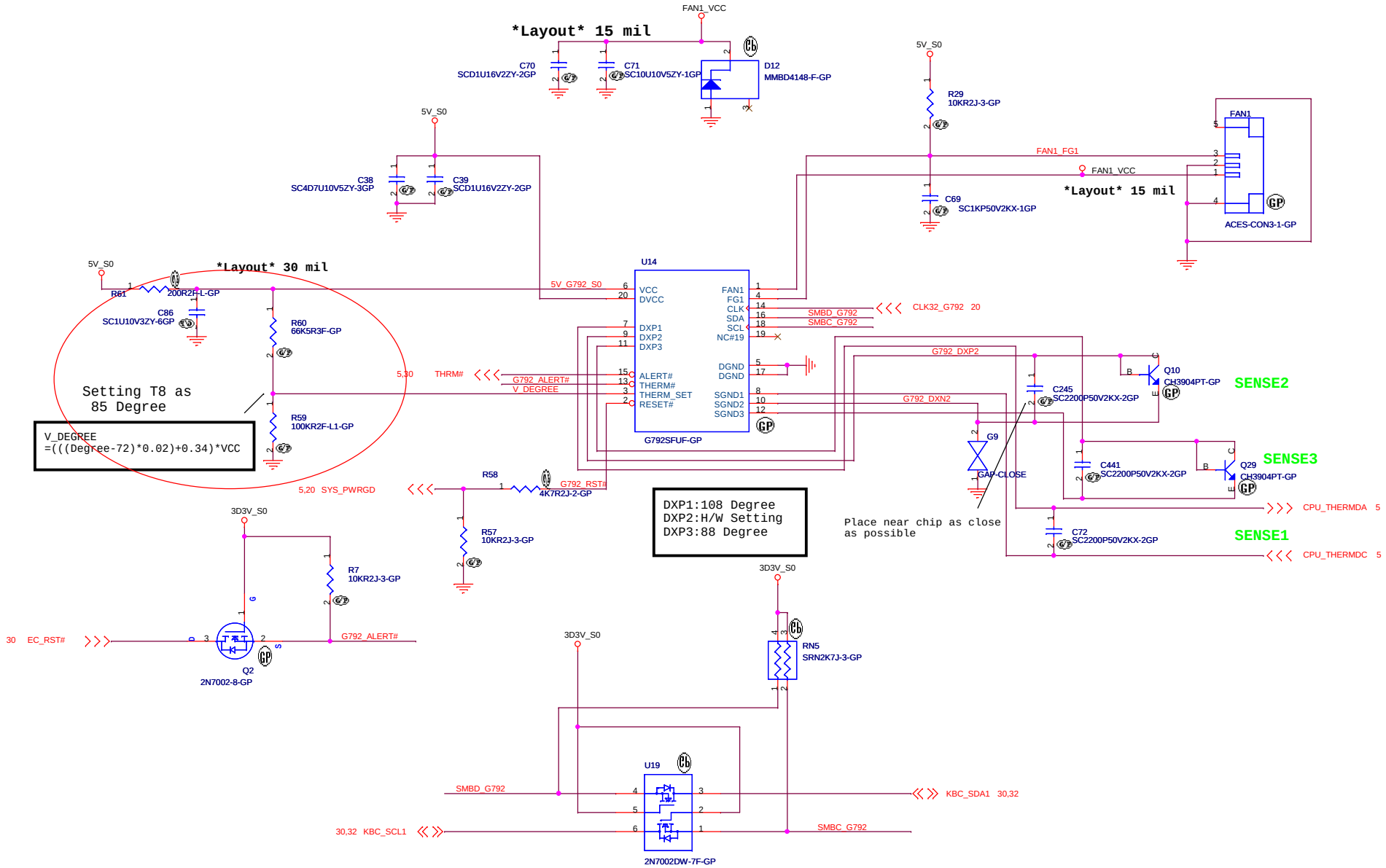
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP51(6/6)POWER

Size	Document Number	Rev
A3	SHIBA	SB

Date: Monday, February 20, 2006 Sheet 22 of 44



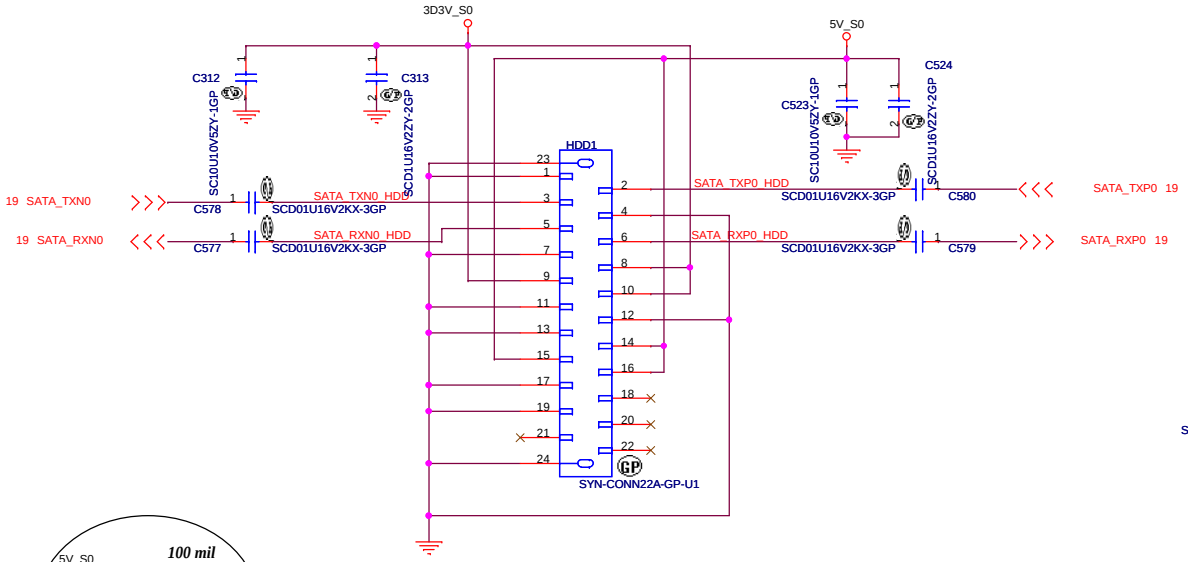
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal/Fan Controllor**

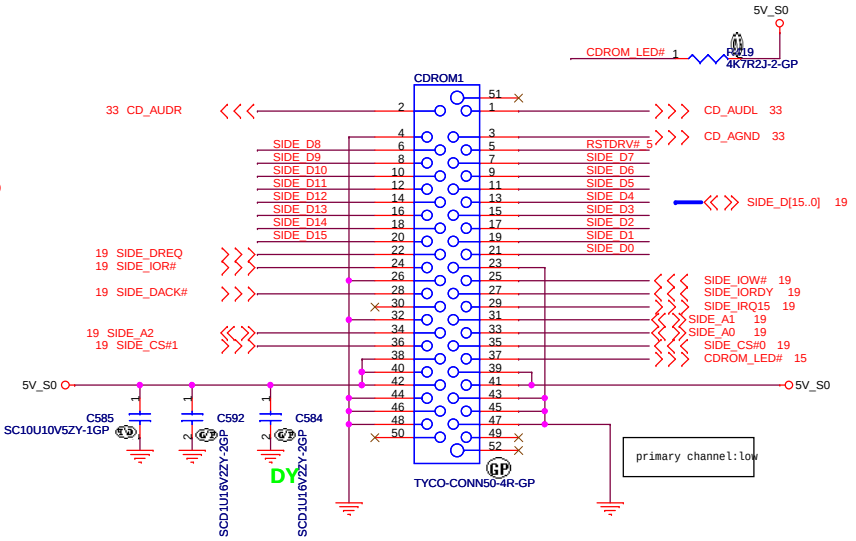
Size	Document Number	Rev
Custom	SHIBA	SA

Date: Monday, February 20, 2006 Sheet 23 of 44

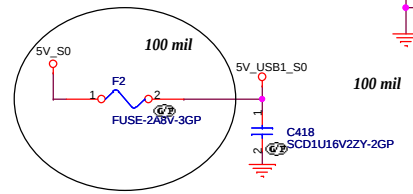
SATA HD Connector

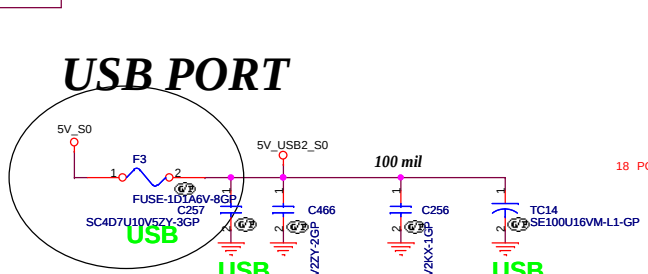


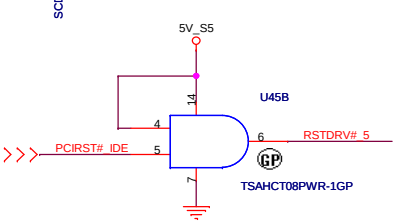
CD-ROM CONNECTOR

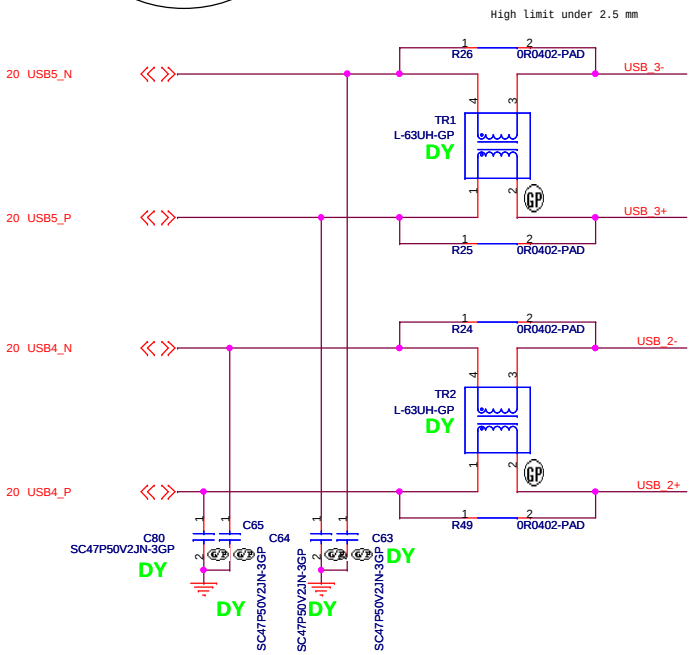


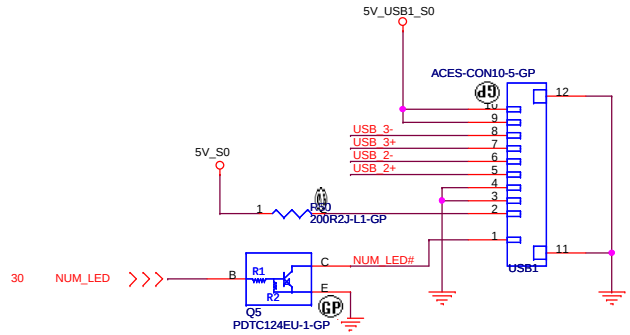
USB PORT

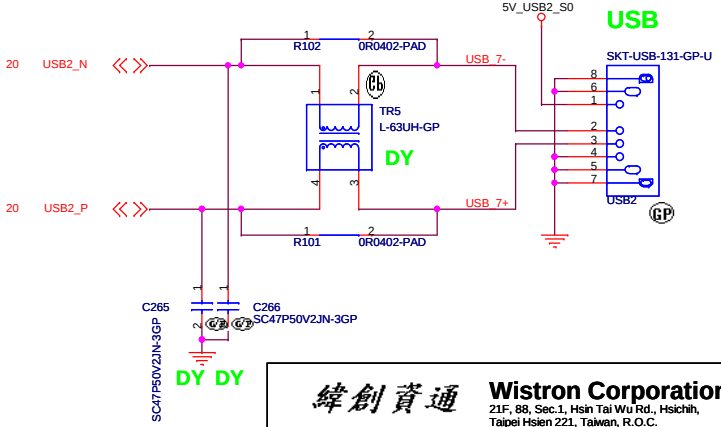




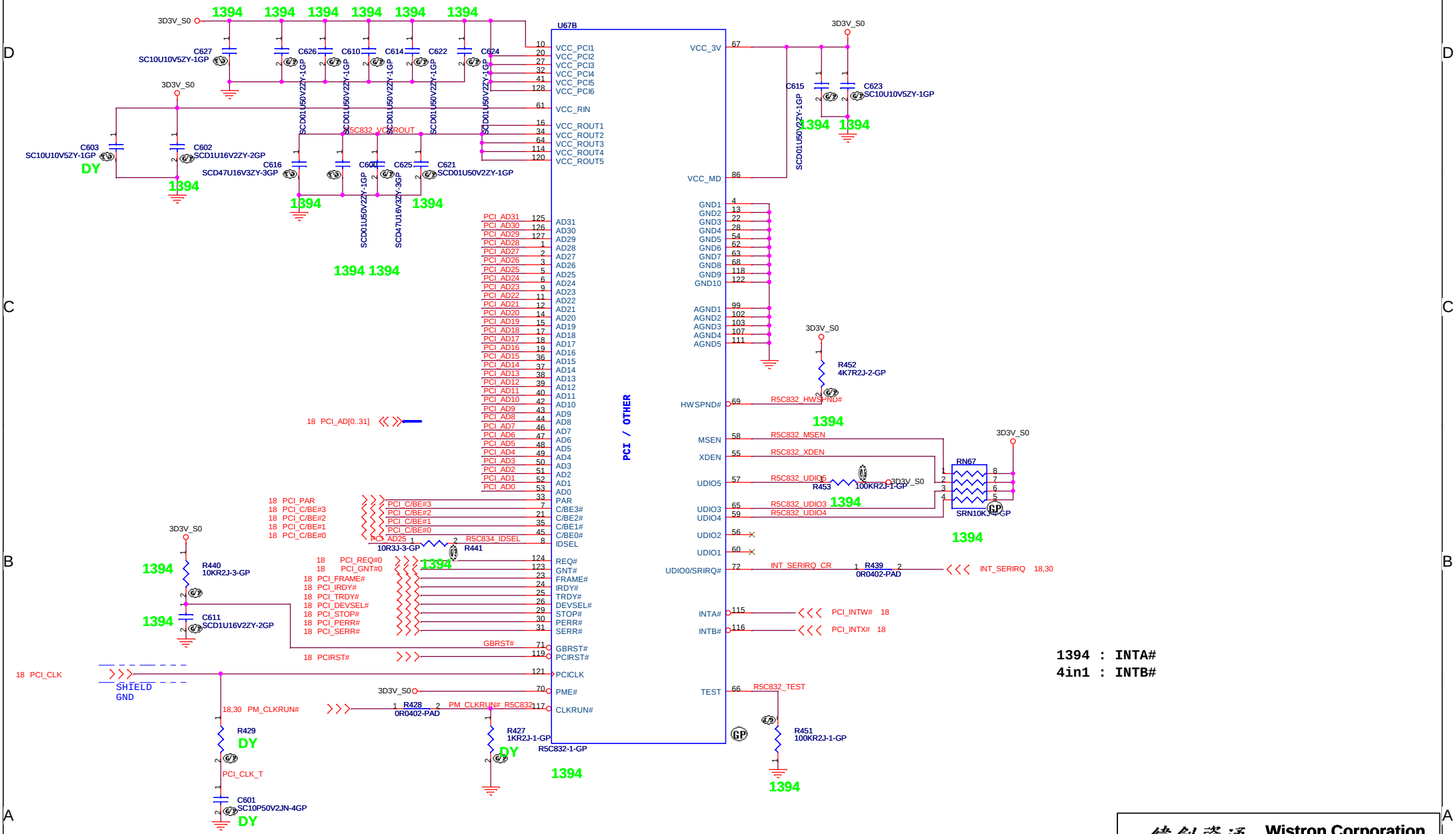


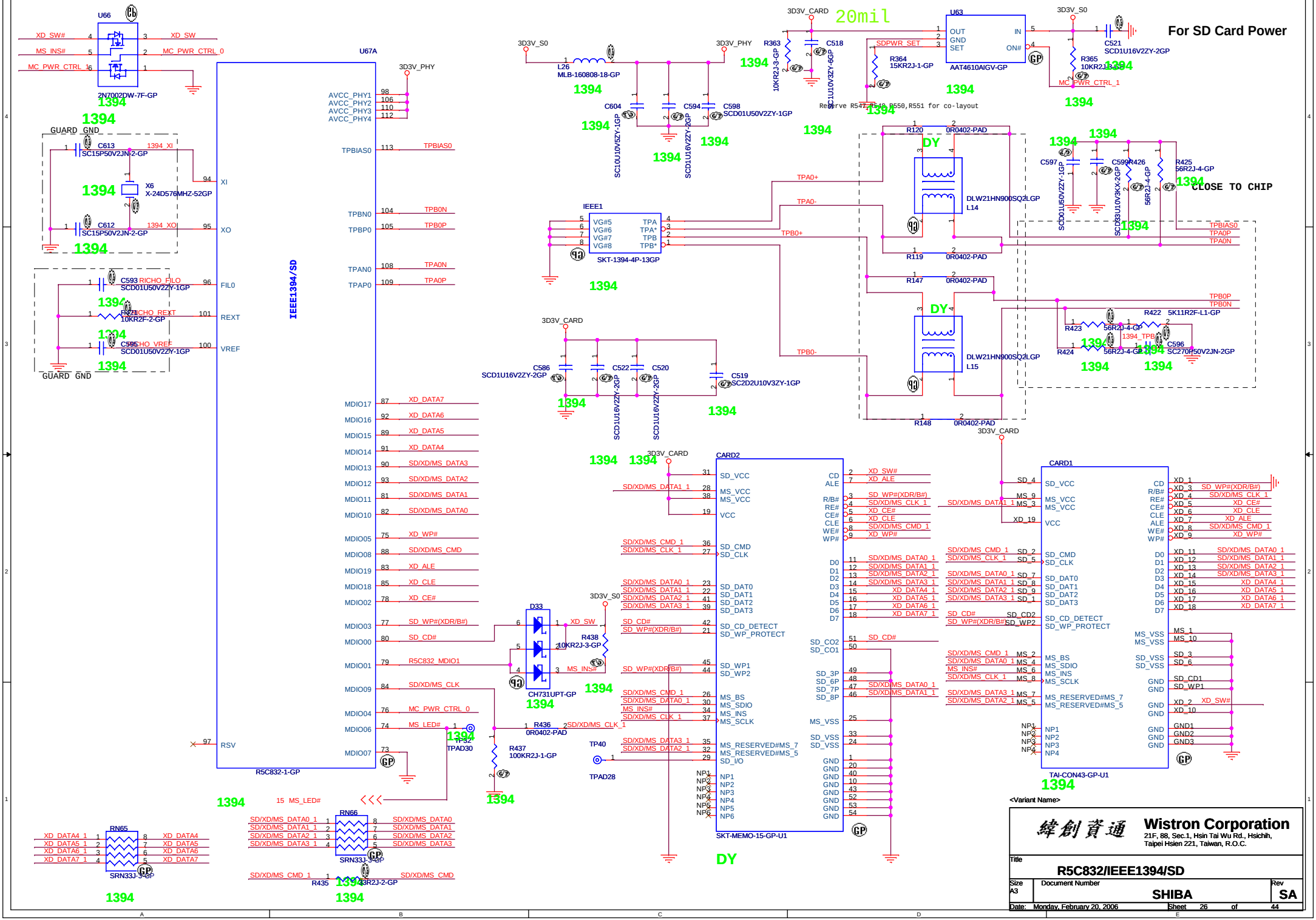






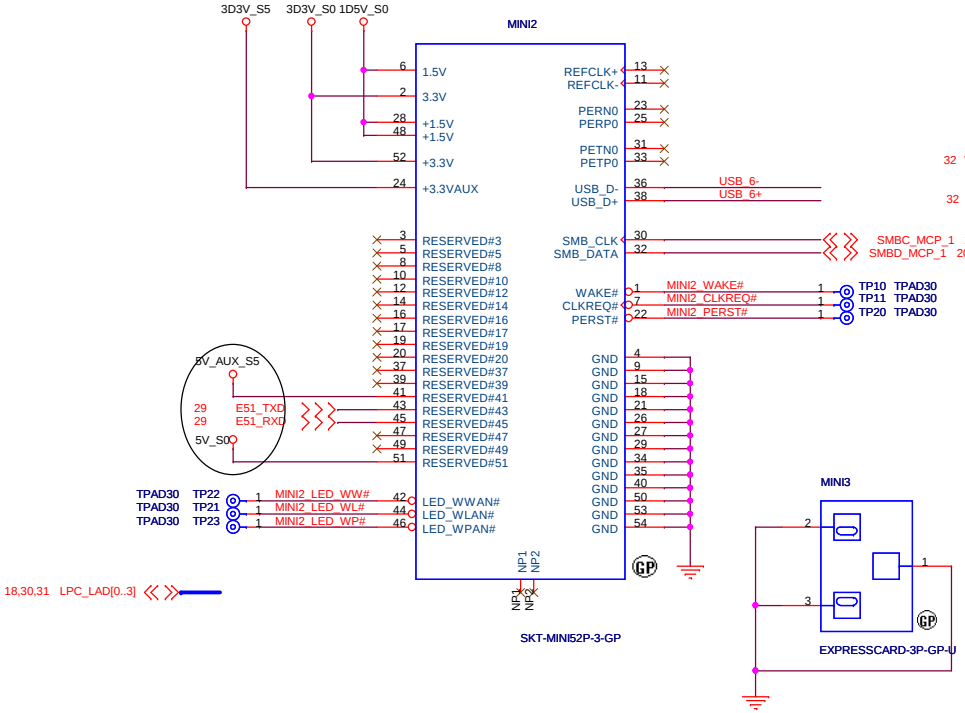
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HD/CDROM		
Size: A3	Document Number: SHIBA	Rev: SA
Date: Saturday, March 04, 2006	Sheet 24 of 44	

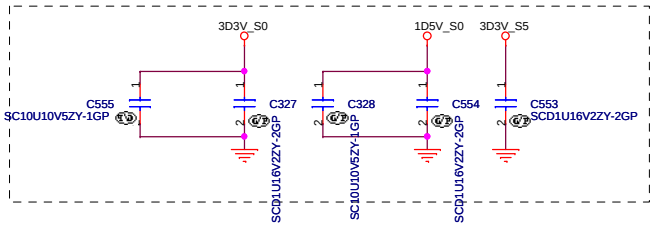

U67B
PCI / OTHER
1394 : INTA#
4in1 : INTB#
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/PCI
Size A3
Document Number
SHIBA
Rev
SA
Date: Monday, February 20, 2006
Sheet 25 of 44


For SD Card Power
CLOSE TO CHIP
20mil
U66
2N7002DW-7F-GP
U67A
IEEE1394/SD
R5C832-1-GP
U63
AAT4610AIGV-GP
IEEE1
SKT-1394-4P-13GP
DLW21HN900SQ2LGP
L14
L15
CARD2
SKT-MEMO-15-GP-U1
CARD1
TAI-CON43-GP-U1
CH731UPT-GP
SRN33J-3-GP
SRN33J-2-GP
Reserve R547,R548,R550,R551 for co-layout
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/IEEE1394/SD
Size A3
Document Number
SHIBA
Rev SA
Date: Monday, February 20, 2006
Sheet 26 of 44

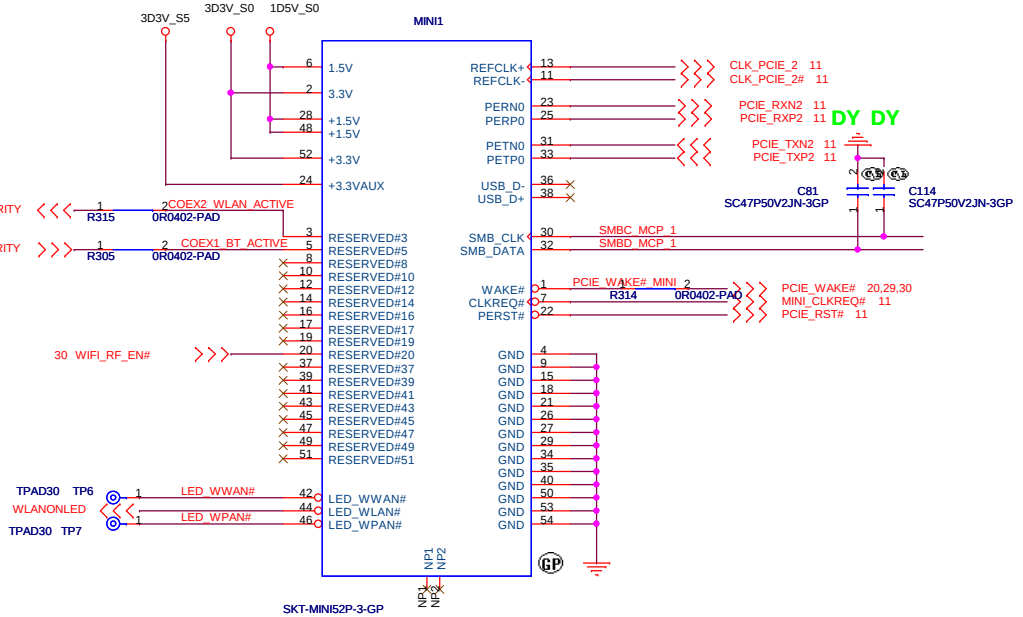
Mini Card Connector

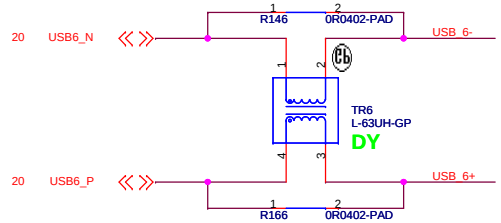
Mini Card Connector 1

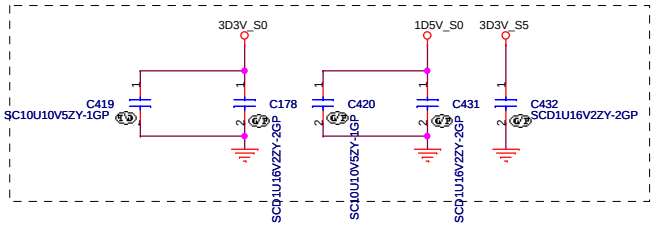




Mini Card Connector 2







緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD CONN .		
Size: A3	Document Number: SHIBA	Rev: SA
Date: Thursday, February 23, 2006	Sheet 27 of 44	

Hardware Configuration: See config _0:4

1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities

E1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

Put L10 for E3016 application since pin 28 NOB for E1116

RN31 SRN0J-6-GP
RGMII_RXD0_R
RGMII_RX_CTL_R
RGMII_RXD0 21
RGMII_RX_CTL 21

RN30 SRN0J-4-GP
RGMII_RXD3_R
RGMII_RXD2_R
RGMII_RX_CLK_R
RGMII_RXD1_R
RGMII_RXD3 21
RGMII_RXD2 21
CLK_LAN_RX 21
RGMII_RXD1 21

2D5V_LAN_S5
R135 1KR2J-1-GP
PHY_VREF
R109 1KR2J-1-GP

21 RGMII_TXD0
21 RGMII_TXD1
21 RGMII_TXD2
21 RGMII_TXD3
21 CLK_LAN_TX
21 RGMII_TX_CTL
LED1000
RGMII_RXD3_R
RGMII_RXD2_R
RGMII_RXD1_R
RGMII_RXD0_R
RGMII_RX_CLK_R
RGMII_RX_CTL_R

2D5V_LAN_S5
R130 0R3-0-U-GP
10/100
R129 0R0603-PAD
GIGA
R128 4K7R2J-2-GP
LAN_CTRL_18
R104 0R3-0-U-GP
Q11 BCP69T1-1-GP
C289 SCD1U16V2ZY-2GP
C288 SC4D7U10V5ZY-3GP
C291 SCD1U16V2ZY-2GP
C290 SC4D7U10V5ZY-3GP
1D8V_LAN_S5

2D5V_S5
G18 GAP-CLOSE-PWR
2D5V_LAN_S5

U23 88E1116-GP
1D2V_LAN_S5
1D8V_LAN_S5
2D5V_LAN_S5
CONFIG_1
CONFIG_2
CONFIG_3
CONFIG_4
DVDD5
LED_0
VDDO7
LED_1
LED_2
RESETn
TRSTn
DIS_REG12
DVDD13
AVDDR14
AVDDR15
AVDDX
MDC
DVDD47
VDDO46
MDIO
TDO
TDI
TCK
TMS
DVDD40
XTAL_2
XTAL_1
AVDDC37
HSDAC_P
HSDAC_N
AVDDC34
RSET
EPAD
RGMII_MDC 21
RGMII_MDIO 21
LAN_TDO
LAN_TDI
LAN_TCK
LAN_TMS
LAN_X2
LAN_X1
LAN_RSET
CLK25_MII 21
TP16 TPAD30
TP14 TPAD30
TP15 TPAD30
TP13 TPAD30
TP41 TPAD28
R134 10KR2J-3-GP
R149 0R0402-PAD
R133 2KR2F-3-GP
R108 4K7R2J-2-GP
TP4 TPAD30
20 RGMII_RESET#
LAN_TRST#
LED100
LED10
VSS

3016: 71.88316.A03
1116: 71.88116.A03
3016:2K 1%
1116: 4K99 1%
3016:4K7 5%
1116: NC
10/100

LAN_CTRL_18
R107 4K7R2J-2-GP
MDI0+ 29
MDI0- 29
MDI1+ 29
MDI1- 29
MDI2+ 29
MDI2- 29
MDI3+ 29
MDI3- 29

1D8V_LAN_S5
C293 C497 C499 C294 C498
SCD1U16V2ZY-2GP

1D8V_LAN_S5
C273 C272
2D5V_LAN_S5
C502 C295 C275
SCD1U16V2ZY-2GP

1D2V_LAN_S5
C274 C276 C299 C298
2D5V_LAN_S5
C500 C501 C277 C271
SCD1U16V2ZY-2GP

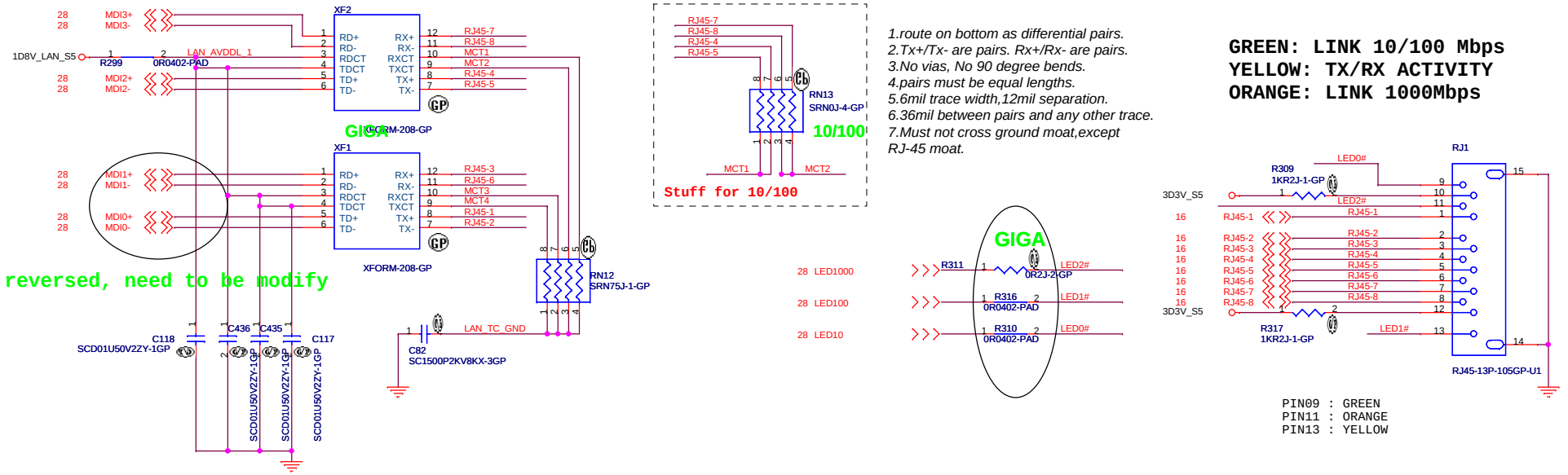
Bypass cap can share. User check it by layout consideration.
GIGA GIGA GIGA GIGA

CLOSE TO LAN CHIP
MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-
R347 49D9R2F-GP
R348 R350 R349 R131 R132 R105 R106
49D9R2F-GP
MDI0X MDI1X MDI2X MDI3X
C495 C496 C292 C270
SCD01U50V2ZY-1GP
GIGA

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN MARVELL 88E1116
Size: A3
Document Number: SHIBA
Rev: SA
Date: Friday, February 24, 2006
Sheet 28 of 44

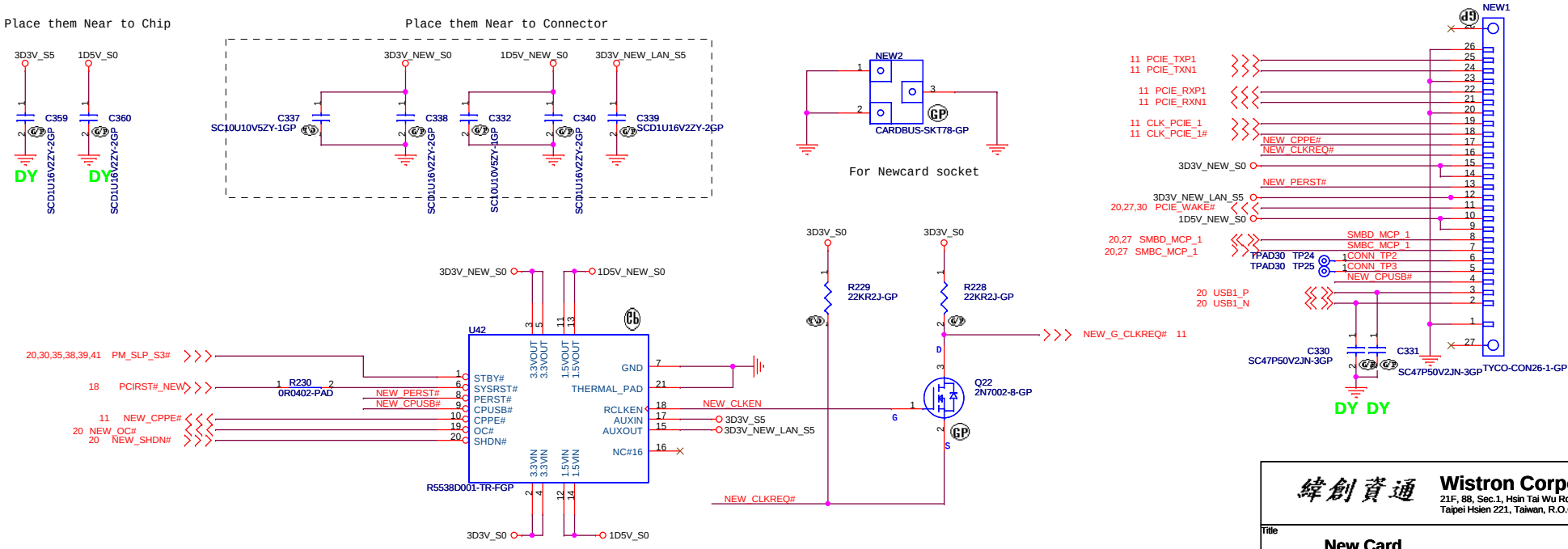


1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

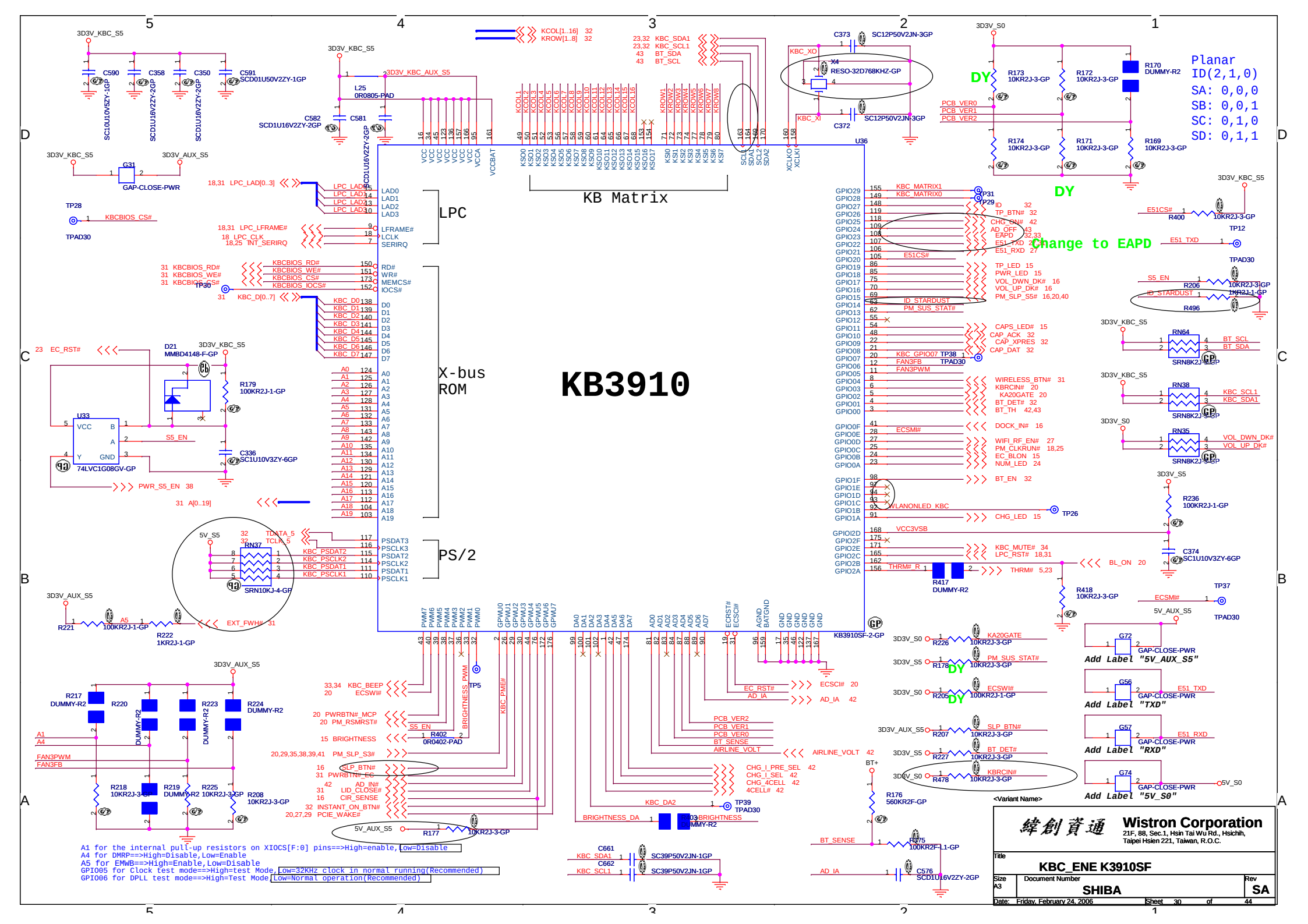
GREEN: LINK 10/100 Mbps
YELLOW: TX/RX ACTIVITY
ORANGE: LINK 1000Mbps

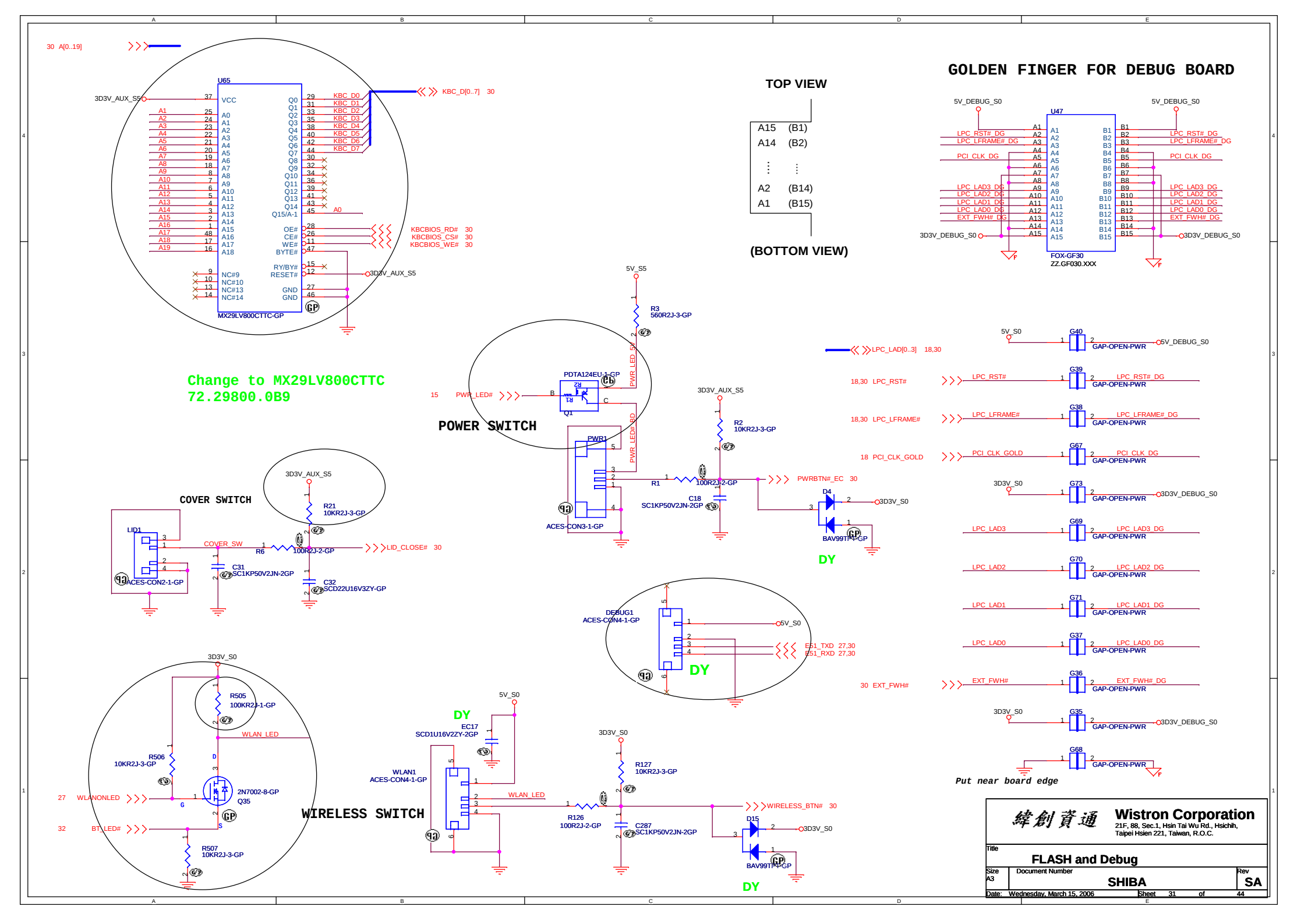
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW

NEWCARD Connector



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **New Card**		
Size: A3	Document Number: **SHIBA**	Rev: **SA**
Date: Monday, February 20, 2006	Sheet 29 of 44	


KB3910
KB3910SF-2-GP
LPC
X-bus ROM
PS/2
KB Matrix
U36
Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
DY
Change to EAPD
Add Label "5V_AUX_S5"
Add Label "TXD"
Add Label "RXD"
Add Label "5V_S0"
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode, Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode, Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
SHIBA
Size A3
Rev SA
Date: Friday, February 24, 2006
Sheet 30 of 44


30 A[0..19]
U65
3D3V_AUX_S5
VCC
MX29LV800CTTC-GP
KBC_D[0..7] 30
KBC_D0
KBC_D1
KBC_D2
KBC_D3
KBC_D4
KBC_D5
KBC_D6
KBC_D7
KBCBIOS_RD# 30
KBCBIOS_CS# 30
KBCBIOS_WE# 30
3D3V_AUX_S5
Change to MX29LV800CTTC
72.29800.0B9
TOP VIEW
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)
(BOTTOM VIEW)
GOLDEN FINGER FOR DEBUG BOARD
U47
FOX-GF30
ZZ.GF030.XXX
5V_DEBUG_S0
3D3V_DEBUG_S0
LPC_RST# DG
LPC_LFRAME# DG
PCI_CLK_DG
LPC_LAD3 DG
LPC_LAD2 DG
LPC_LAD1 DG
LPC_LAD0 DG
EXT_FWH# DG
POWER SWITCH
5V_S5
R3
560R2J-3-GP
PDTA124EU-1-GP
Q1
15 PWR_LED#
PWR_LED_5V
PWR_LED#_3D
PWR1
ACES-CON3-1-GP
3D3V_AUX_S5
R2
10KR2J-3-GP
R1
100R2J-2-GP
C18
SC1KP50V2JN-2GP
PWRBTN#_EC 30
D4
BAV99TP-1-GP
3D3V_S0
DY
LPC_LAD[0..3] 18,30
18,30 LPC_RST#
18,30 LPC_LFRAME#
18 PCI_CLK_GOLD
30 EXT_FWH#
G40
G39
G38
G67
G73
G69
G70
G71
G37
G36
G35
G68
GAP-OPEN-PWR
Put near board edge
COVER SWITCH
3D3V_AUX_S5
R21
10KR2J-3-GP
LID1
ACES-CON2-1-GP
COVER_SW
R6
100R2J-2-GP
LID_CLOSE# 30
C31
SC1KP50V2JN-2GP
C32
SCD22U16V3ZY-GP
DEBUG1
ACES-CON4-1-GP
5V_S0
E51_TXD 27,30
E51_RXD 27,30
DY
WIRELESS SWITCH
3D3V_S0
R505
100KR2J-1-GP
WLAN_LED
R506
10KR2J-3-GP
2N7002-8-GP
Q35
27 WLANONLED
32 BT_LED#
R507
10KR2J-3-GP
5V_S0
DY
EC17
SCD1U16V2ZY-2GP
WLAN1
ACES-CON4-1-GP
WLAN_LED
R127
10KR2J-3-GP
R126
100R2J-2-GP
C287
SC1KP50V2JN-2GP
WIRELESS_BTN# 30
D15
BAV99TP-1-GP
3D3V_S0
DY
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
FLASH and Debug
Size
A3
Document Number
SHIBA
Rev
SA
Date: Wednesday, March 15, 2006
Sheet 31 of 44

CAMERA

Blue thumb

Internal KeyBoard Connector

30 KROW[1..8]

30 KCOL[1..16]

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

CAPACITY BUTTON

TOUCH-PAD SWITCH

PLACE NEAR CAP1

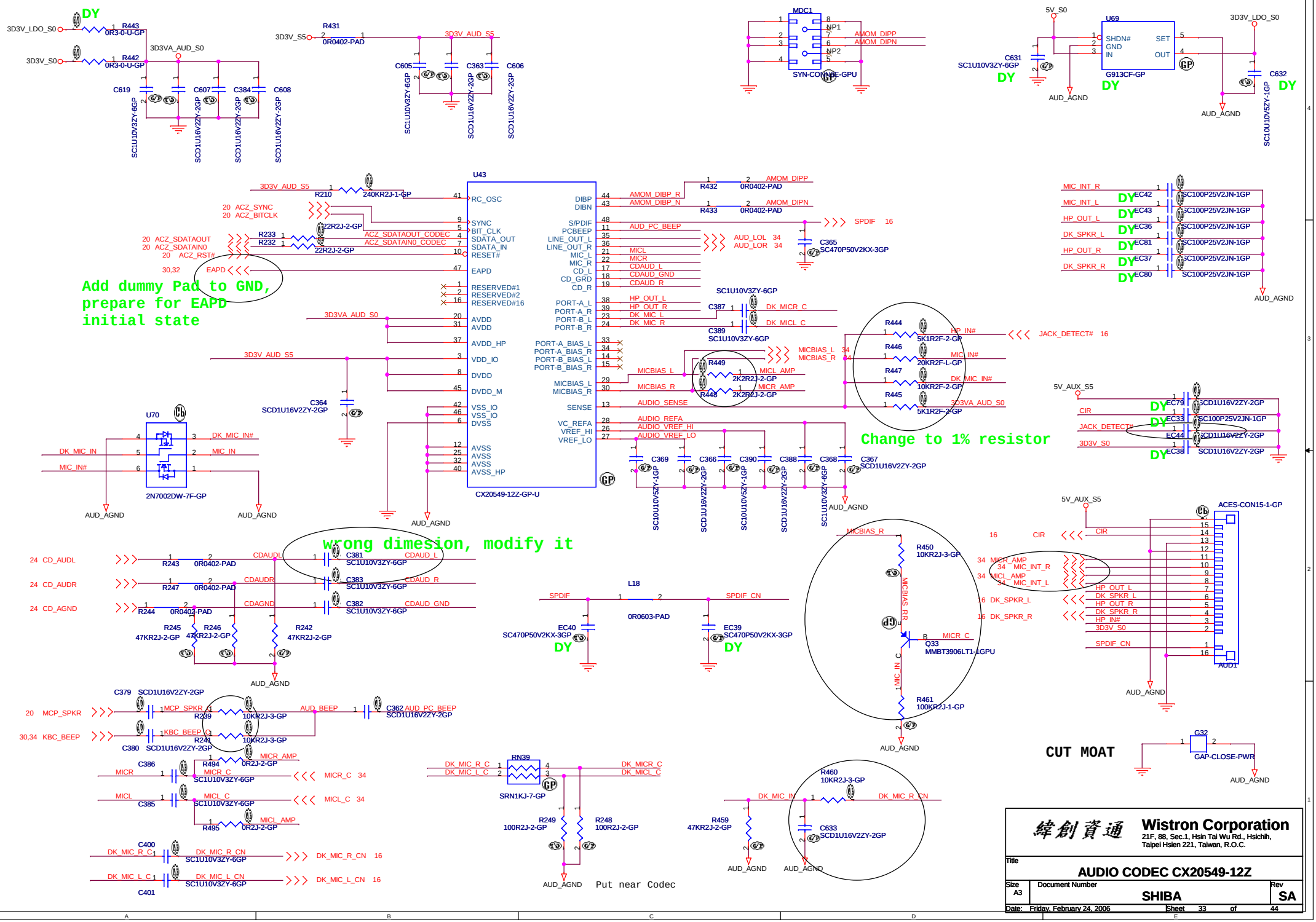
for EMI

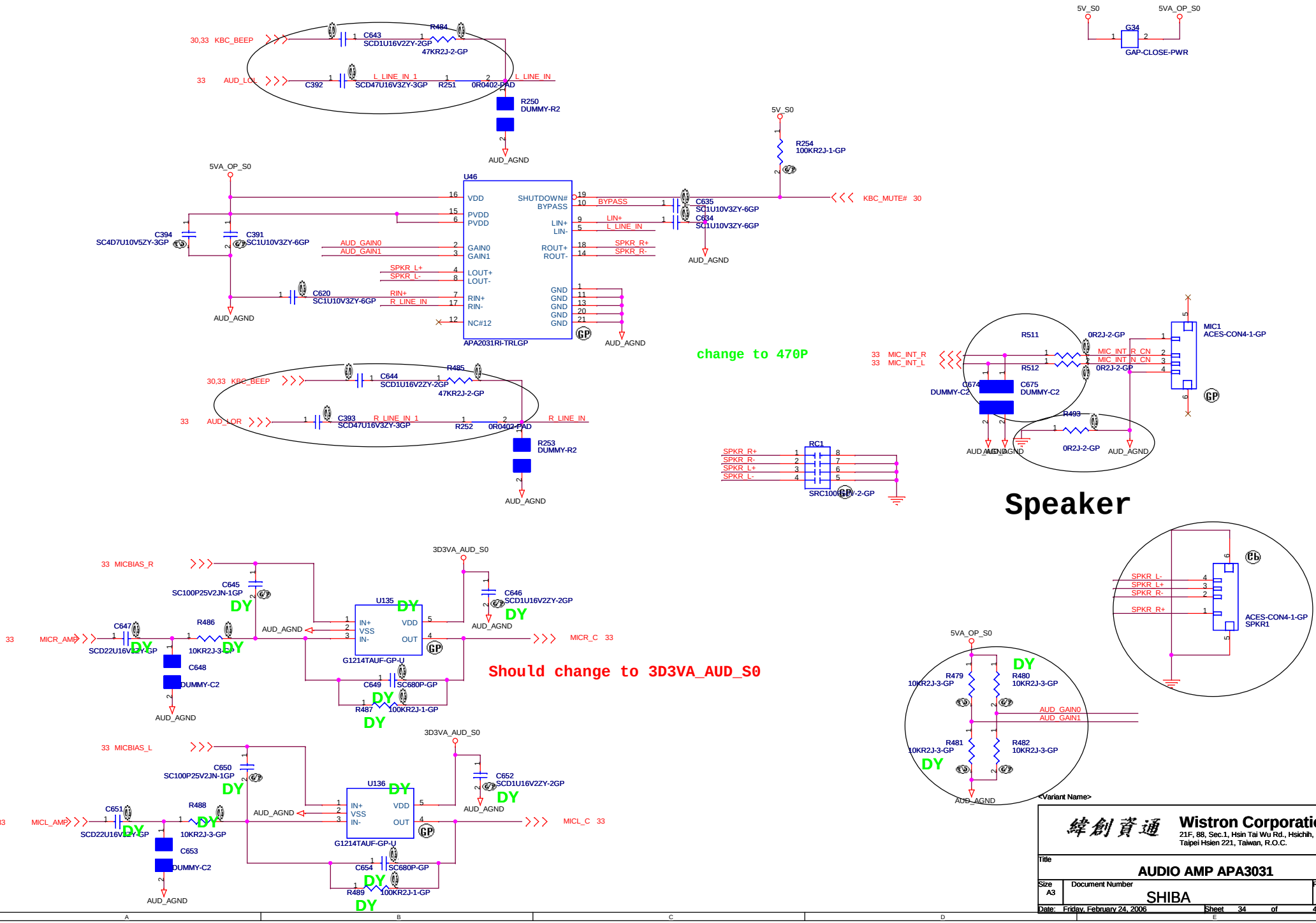
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard-CONN

Size: A3 | Document Number: SHIBA | Rev: SA

Date: Sunday, February 26, 2006 | Sheet 32 of 44


Add dummy Pad to GND, prepare for EAPD initial state
wrong dimension, modify it
Change to 1% resistor
CUT MOAT
Put near Codec
U43
CX20549-12Z-GP-U
U70
2N7002DW-7F-GP
MDC1
SYN-CONNF-GPU
U69
G913CF-GP
ACES-CON15-1-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX20549-12Z
Size A3
Document Number
SHIBA
Rev SA
Date: Friday, February 24, 2006
Sheet 33 of 44



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP APA3031

Size	Document Number	Rev
A3	SHIBA	SA

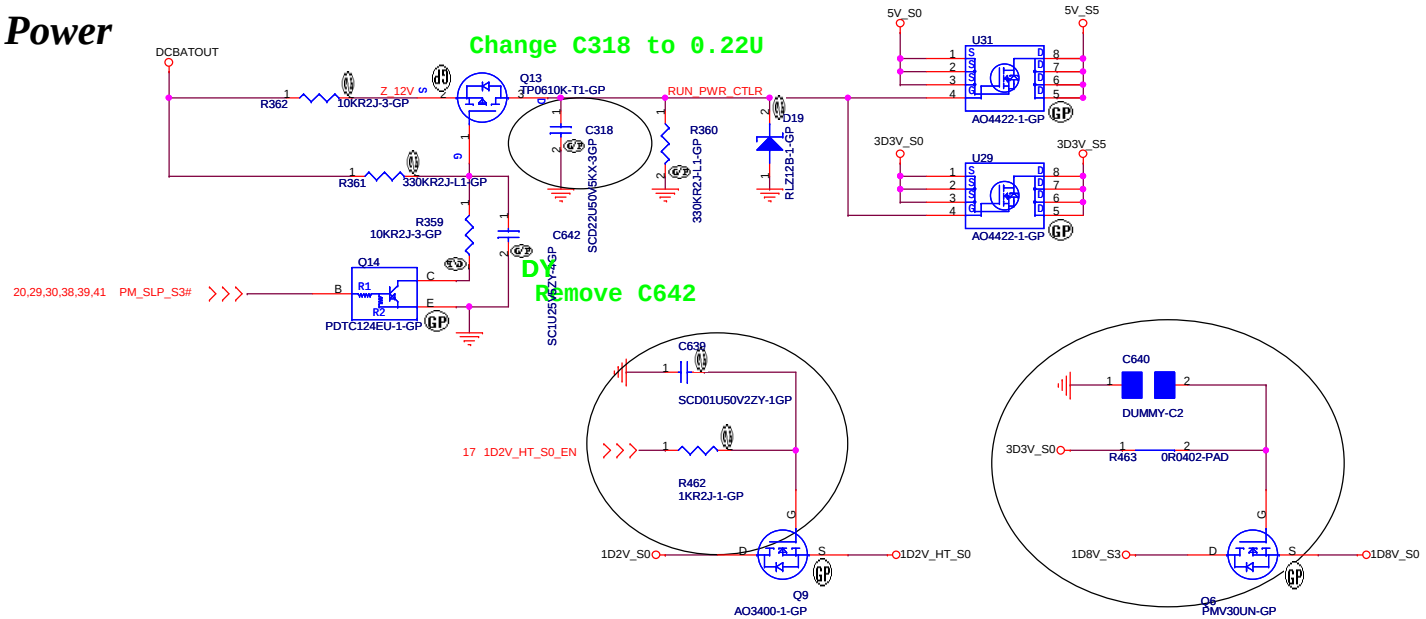
Date: Friday, February 24, 2006 Sheet 34 of 44

<Variant Name>

Suspend Power

Remove Dummy PAD

Run Power



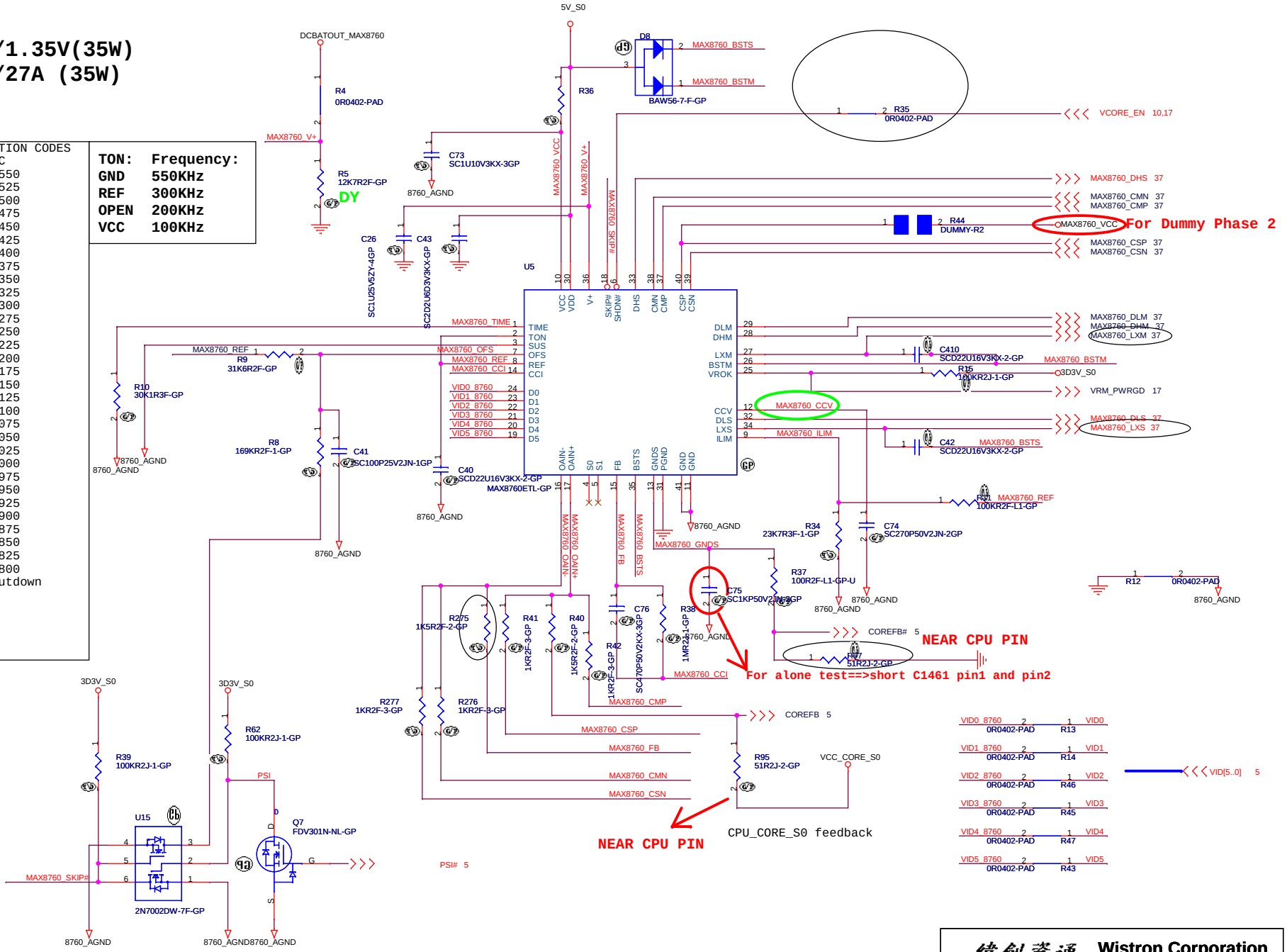
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PWRPLANE&RESETLOGIC		
Size: A3	Document Number: SHIBA	Rev: SA
Date: Monday, February 20, 2006	Sheet 35 of 44	

CPU_VCORE
VID=1.20V(25W)/1.35V(35W)
Iomax=21A(25W)/27A (35W)
OCP=40A~45A

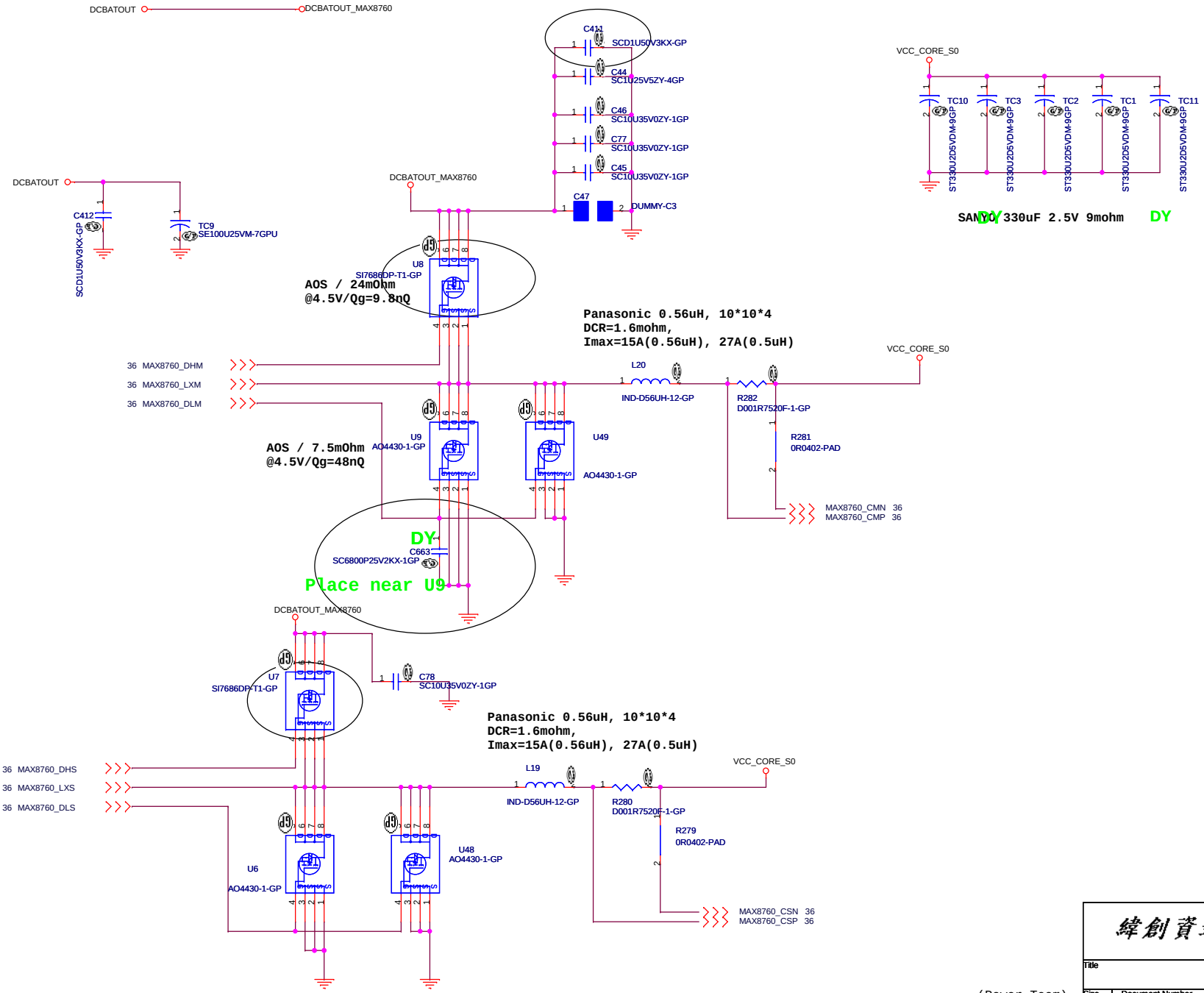
TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON:	Frequency:
GND	550KHz
REF	300KHz
OPEN	200KHz
VCC	100KHz

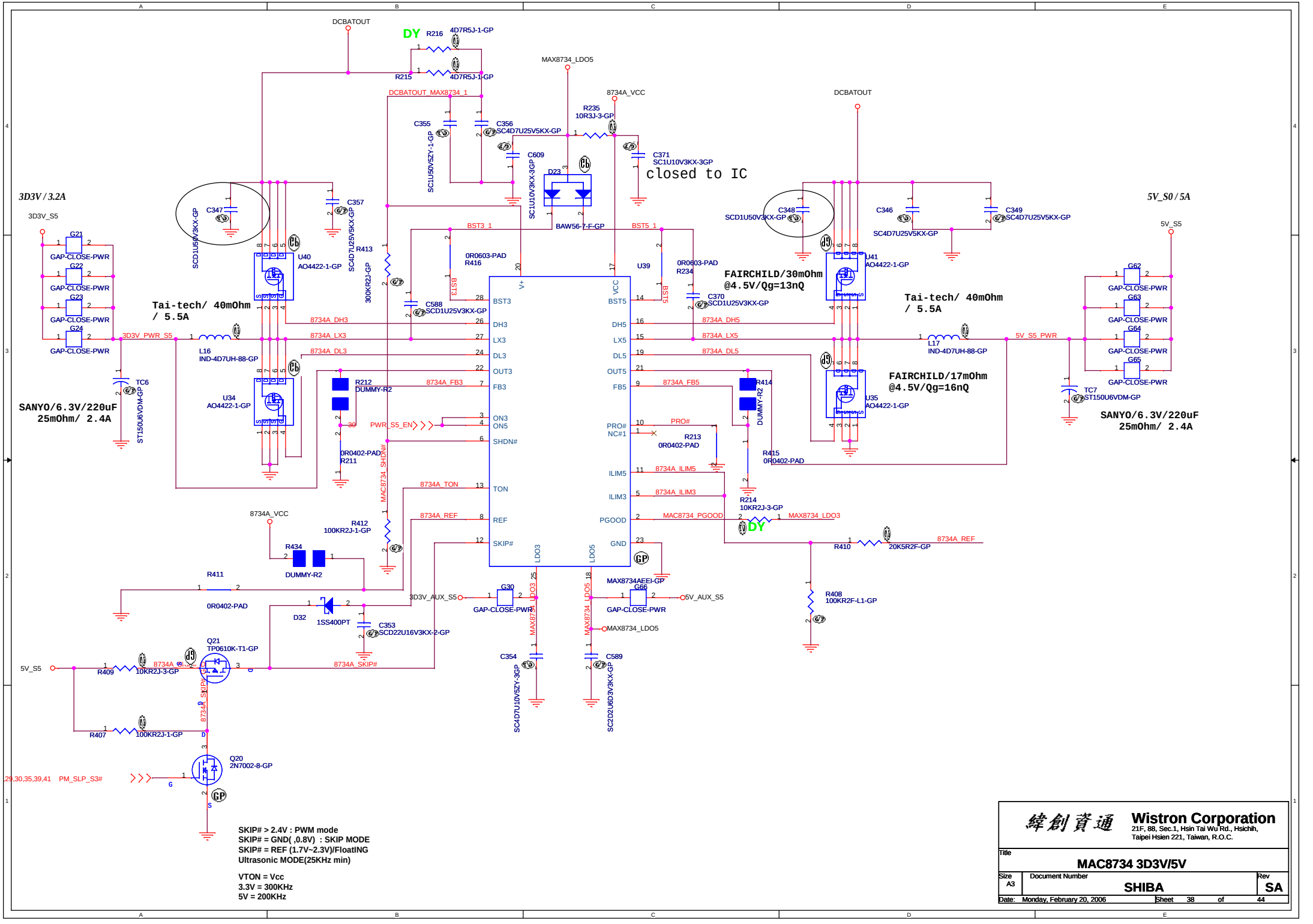


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU CORE MAX8760(1/2)	
Size: A3	Document Number: SHIBA	Rev: SA
Date: Wednesday, February 22, 2006	Sheet 36 of 44	



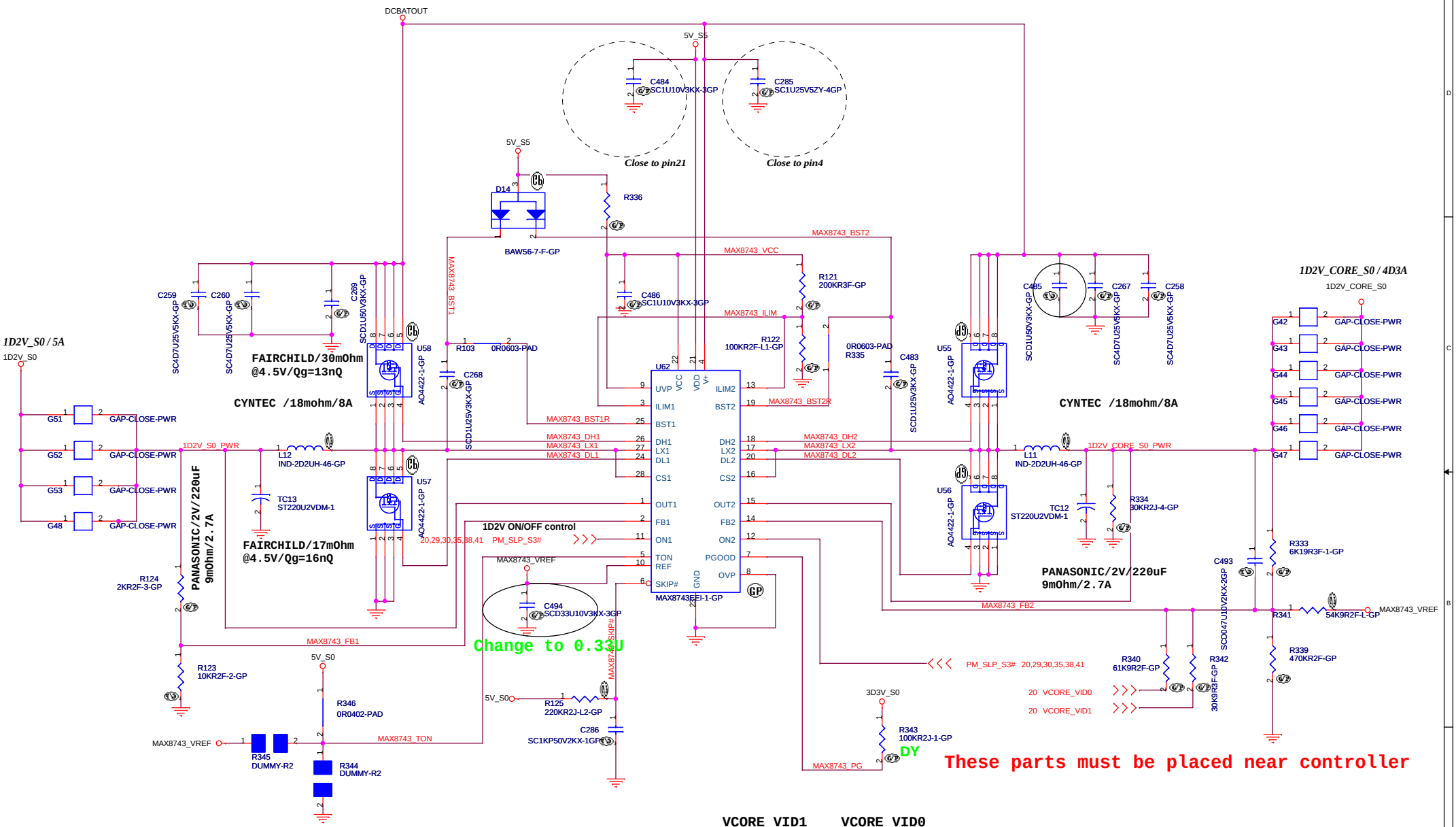
(Power Team)

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU CORE MAX8760(2/2)		
Size: A3	Document Number: SHIBA	Rev: SA
Date: Wednesday, February 22, 2006	Sheet 37 of 44	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MAC8734 3D3V/5V	
Size A3	Document Number SHIBA	Rev SA
Date: Monday, February 20, 2006	Sheet 38 of 44	

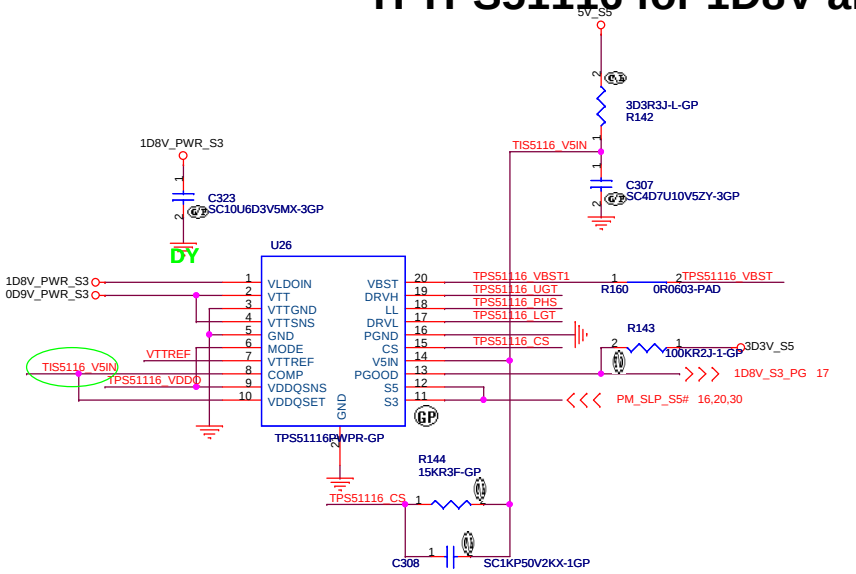


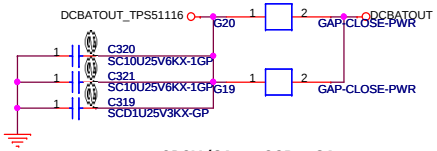
VCORE_VID1	VCORE_VID0	
L	L	1.2V
L	Z	1.1V
Z	L	1.0V
Z	Z	Reserved

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

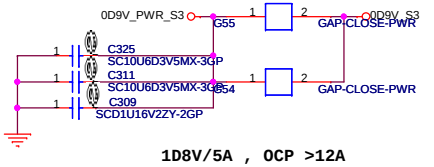
Title	MAX8743 1D2V/1D2V_CORE	
Size A3	Document Number SHIBA	Rev SA
Date: Monday, February 20, 2006	Sheet 39 of 44	

TI TPS51116 for 1D8V and 0D9V

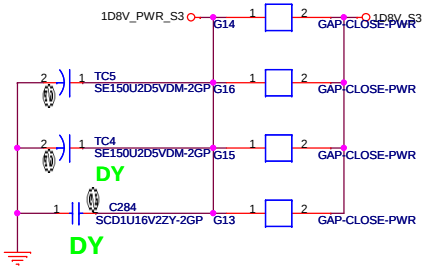


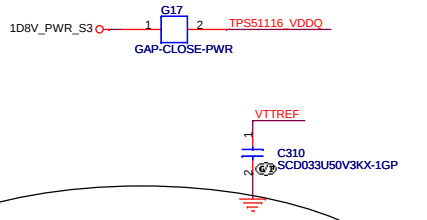


0D9V/2A , OCP >3A

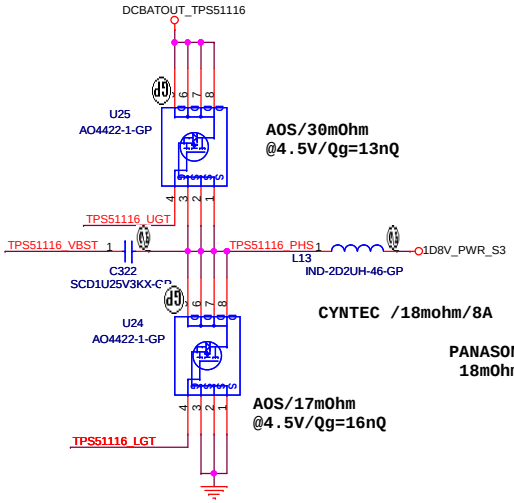


1D8V/5A , OCP >12A





State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



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	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**TPS51116 1D8V/0D9V**
Size A3	Document Number: **SHIBA**
Rev	**SA**
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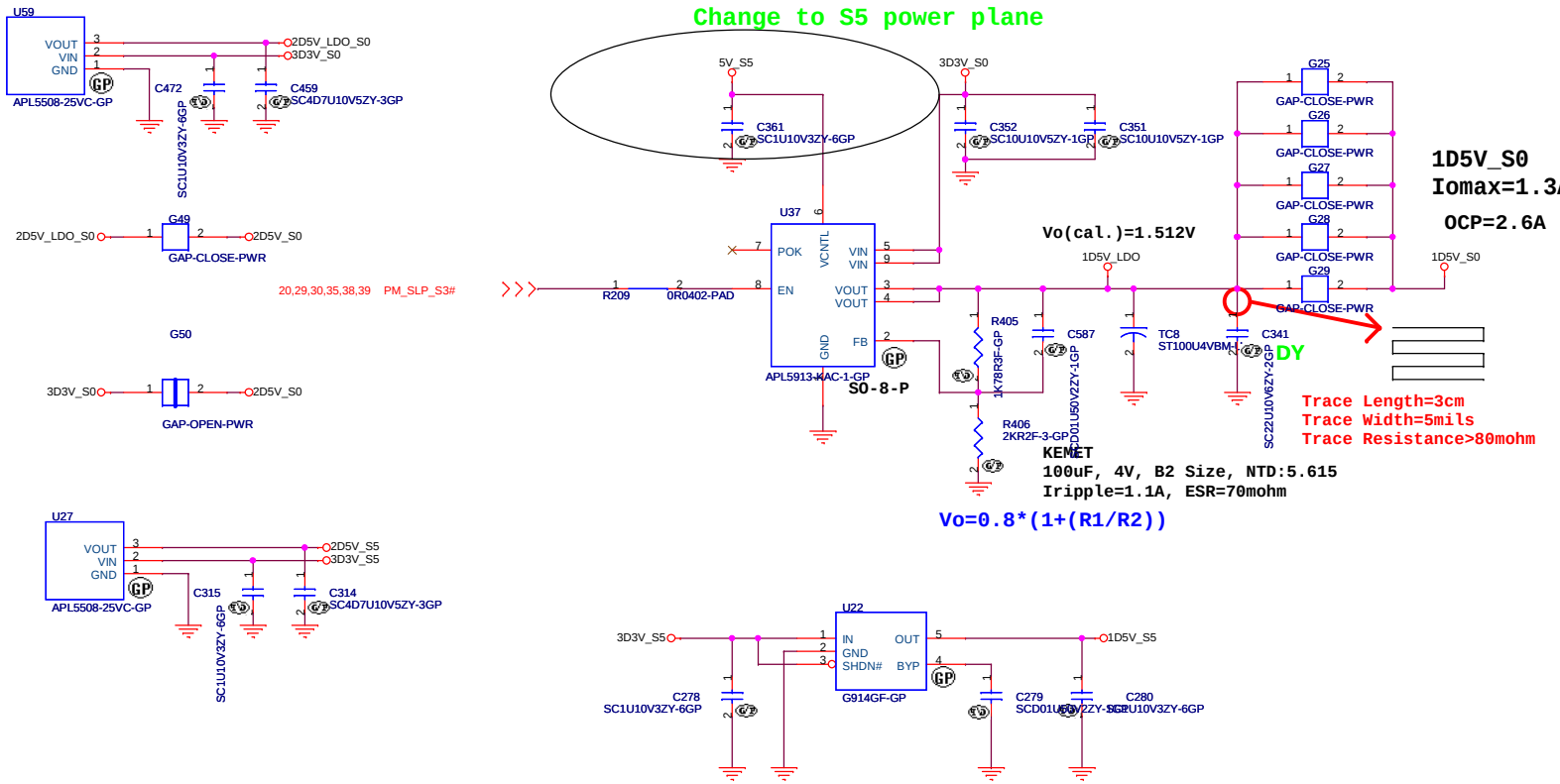

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Title: *1D5V/2D5V/3D3V/5V_AUX*		
Size: A3	Document Number: SHIBA	Rev: SA
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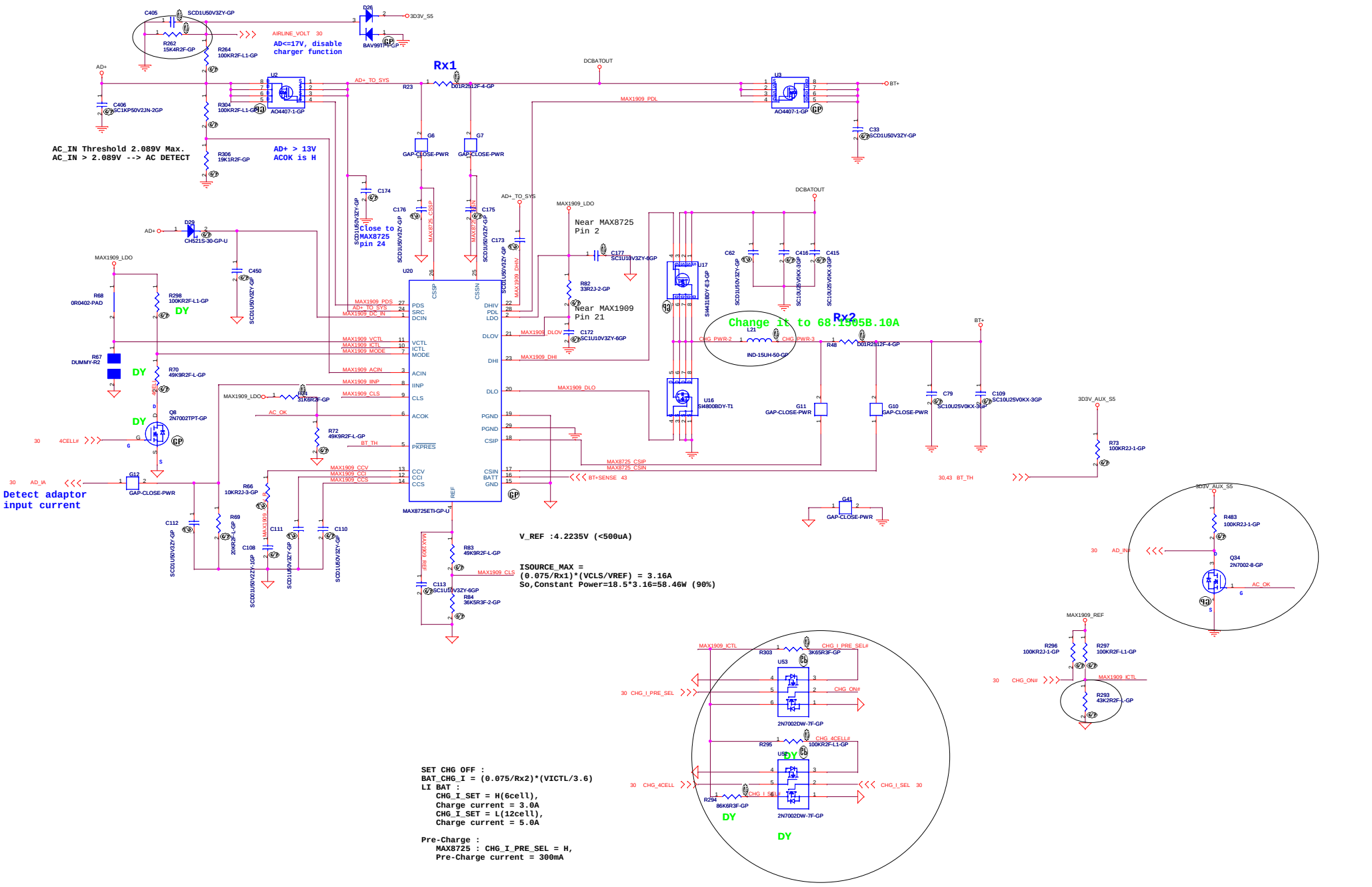

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Title	CHARGER MAX8725	
Size A2	Document Number SHIBA	Rev SA
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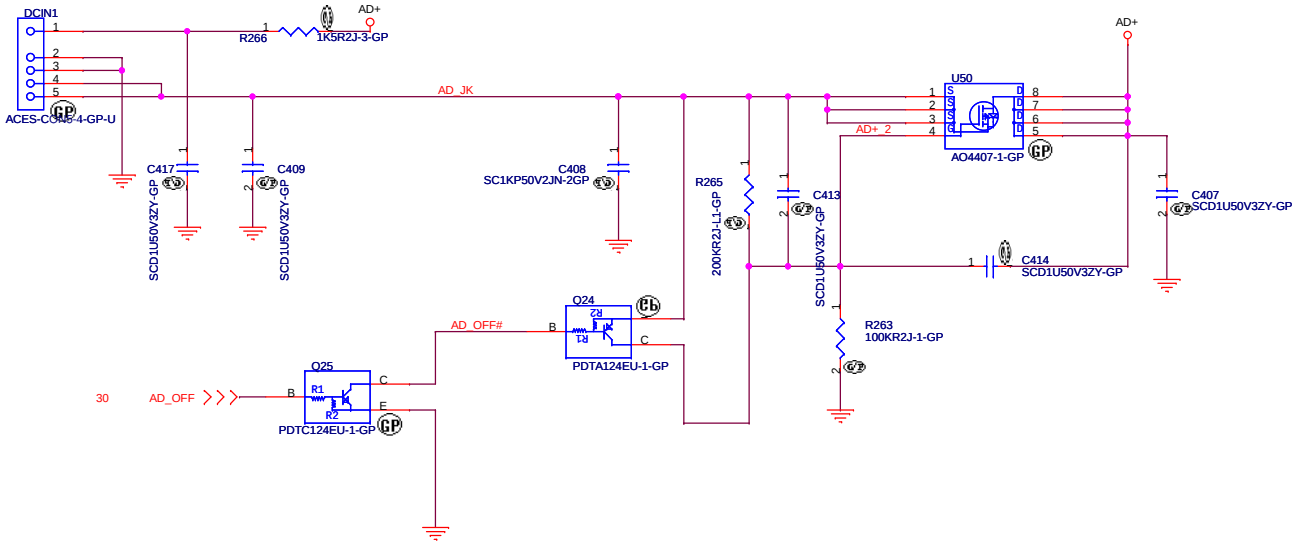
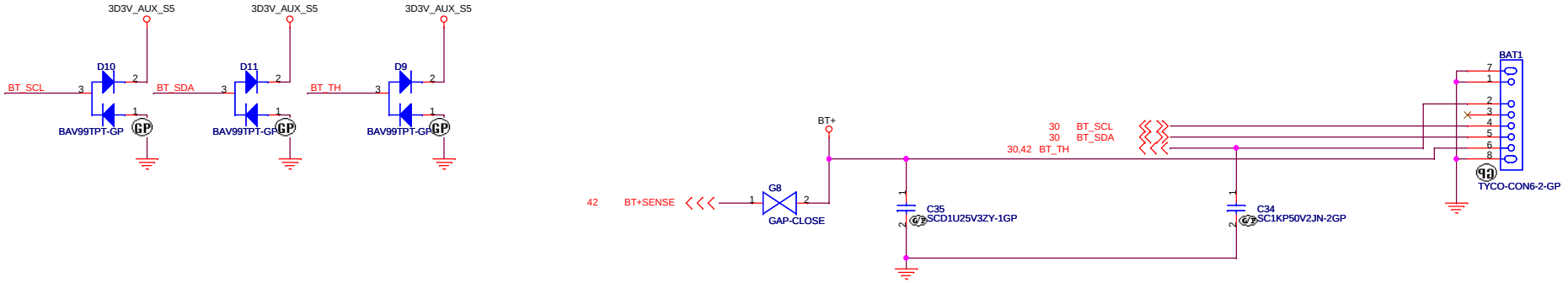
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title: AD/BATT CONN		
Size: A3	Document Number: SHIBA	Rev: SA
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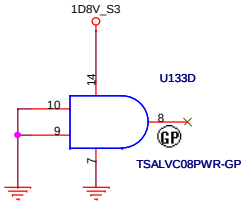
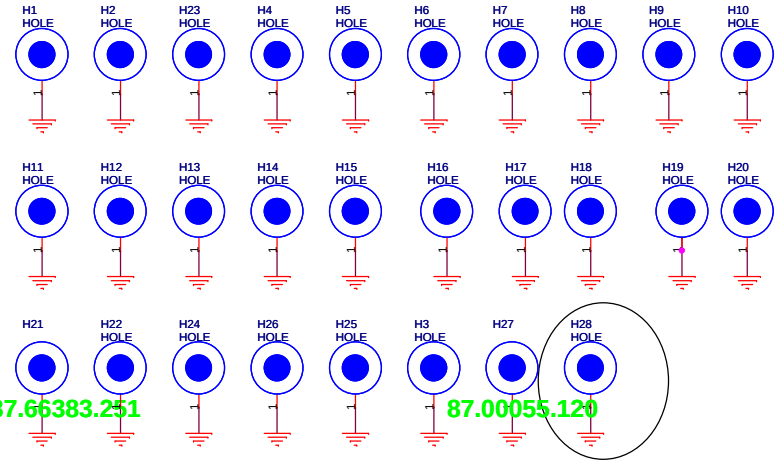
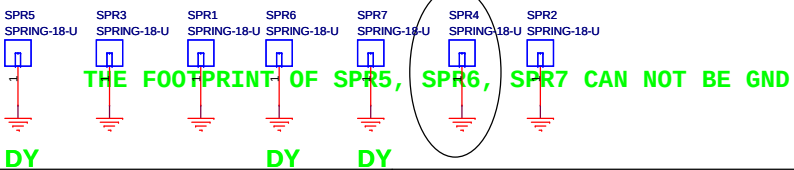
	FF	DF
CAMERA	○	X
LAN	10/100	10/100
1394/5 IN 1	○	X
EXTRA USB	○	X
MIC	○	X
CR LED	○	X



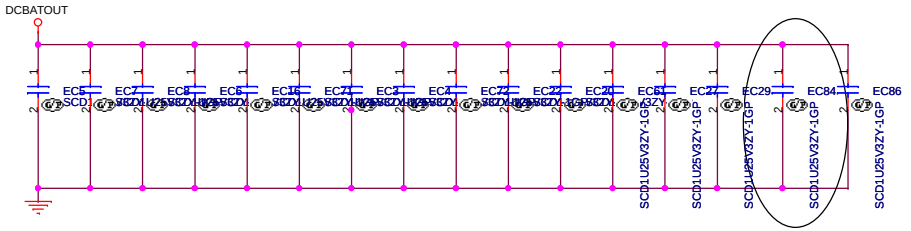


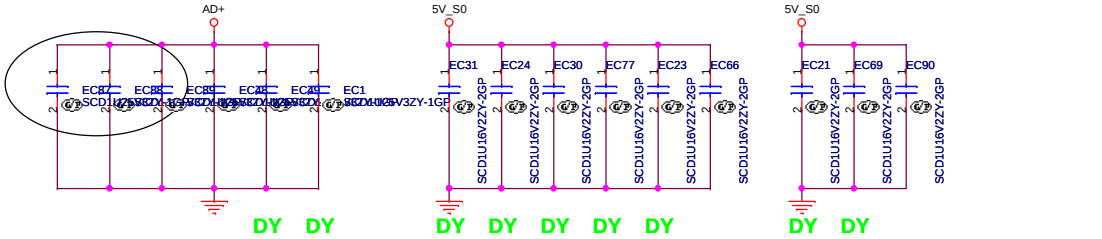
87.66383.251 87.00055.120



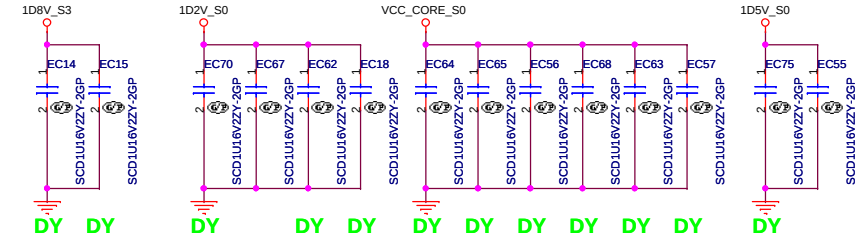
THE FOOTPRINT OF SPR5, SPR6, SPR7 CAN NOT BE GND

DY DY DY

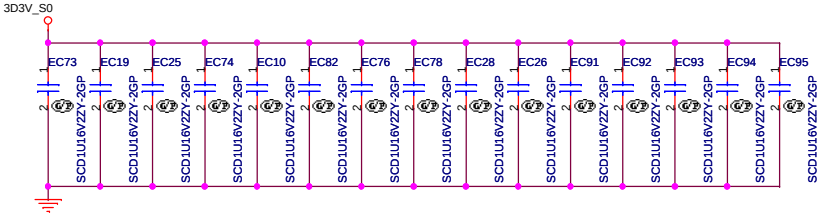




DY DY DY DY DY DY DY DY DY



DY DY DY DY DY DY DY DY DY DY DY



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Title: MISC		
Size: A3	Document Number: SHIBA	Rev: SA
Date: Saturday, March 04, 2006	Sheet 44 of 44	