

Siberia Block Diagram

Project code: 91.4Q601.001
PCB P/N : 48.4Q613.0SC
REVISION : 06248-SC

Thermal Sensor
EMC4001 20

Clock Generator
CY28547LFXC 4

Intel Mobile CPU
Merom 4M
FSB:667/ 800 Mhz
5, 6

HOST BUS FSB 667/800MHz

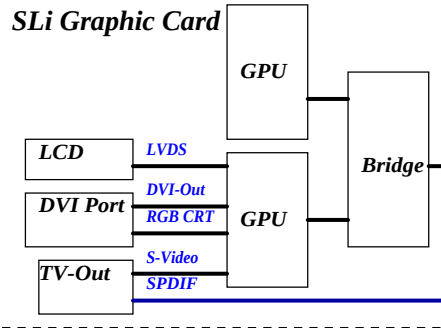
Crestline-PM

AGTL+ CPU I/F
DDR Memory I/F
EXTERNAL GRAHPICS
7, 8, 9, 10, 11, 12

200-PIN DDR2 SODIMM

UNBUFFERED
DDR2 SODIMM
Socket 13

UNBUFFERED
DDR2 SODIMM
Socket 14



SPDIF

PCI-e x16

SATA HDD 21

SATA HDD 21

ODD Bay 21

INT. Speaker 5W x 2 25

Speaker AMP. MAX9714 25

SPDIF

INT. Digital Array MIC 24

Azalia CODEC STAC 9228 24

Headphone AMP. MAX4411 x 2 26

Audio Jack Board

7 in1 CONN 7 in1

1394 CONN 1394

USB CONN.x1 23

IO Board

BIOS SPI FLASH 16Mb 36

EC SMSC MEC5025 33

Touch Pad CONN. 35

Touch Pad

KBC SMSC ECE1077

Int. KB Numpad

Touch Pad Module

CIR Board

Camera Module 35

Bulletproof 2.1 36

W to B CONN. 32

W to B CONN. 32

USB CONN.x2

Sniffer Board

Gaming LCD Module

Power Switch 31

Express Card Slot 54mm 30

Mini-Card WPAN/Robson 31

Mini-Card 802.11a/g/n 30

PPU Card CONN. 29

BCM5754M Giga LAN 27

RJ45 CONN 28

SIM CONN 31

USB CONN.x1 23

W to B CONN. 32

W to B CONN. 32

USB CONN.x2

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W to B CONN. 32

USB CONN.x2

Sniffer Board

CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15

IO_VOUT[2,1,0]

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Lane Reserved
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	Reserved
LL(00)	Reserved
LW(01)	XOR Mode Enabled
HL(10)	ALL Z Mode Enabled
HH(11)	Normal Operation

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	BT/UWB/Robson
LANE4	Express Card
LANE5	PPU card
LANE6	Giba Bit LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/MediaCard	AD17	C D	1	1

USB TABLE

ICH

USB0	Ext Lift Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPI020	Reserved. Rising Edge of PWROK.	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCl1_5 VRM Enable/disable. Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCl1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCl1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCl1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
XCR_RSVD[3]	AZ_DOUT	ICH	Description
0	0	0	RSVD
0	1	1	Enter XOR Chain
1	0	0	Normal Operation(default)
1	1	1	Set PCIE port cofig bit1

A16 swap override strap			
PCI_GNT#3	low = A16 swap override enable	high = default	
800T BIOS Strap			
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location	
0	1	SPI	
1	0	PCI	
1	1	LPC	(default)

Integrated VccSus1_05,VccSus1_5,VccCl1_5			
SM_INTVRMEN	High=Enable	Low=Disable	
Integrated VccLAN1_05VccCl1_05			
LAN100_SLP	High=Enable	Low=Disable	

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Default
	High=No Reboot

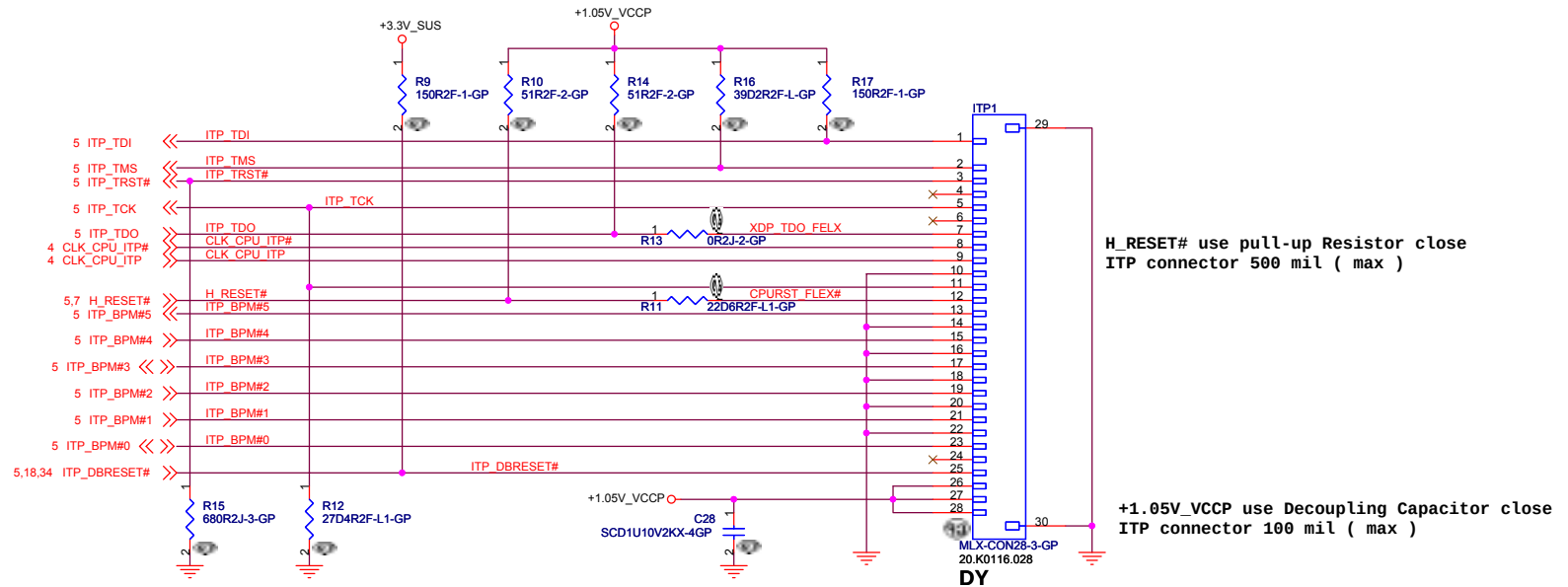
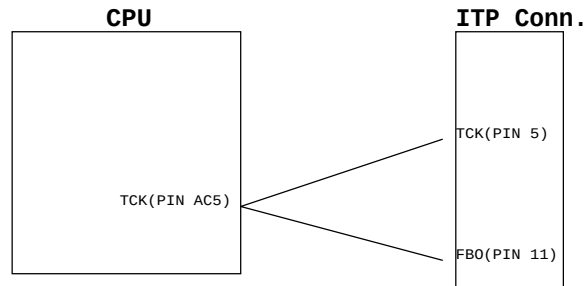
8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPI0[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPI023	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST0#	PULL-UP 13K



Title			Table of Content	
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ITP Debug Conn.

<Variant Name>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ITP Debug

Size
A3

Document Number

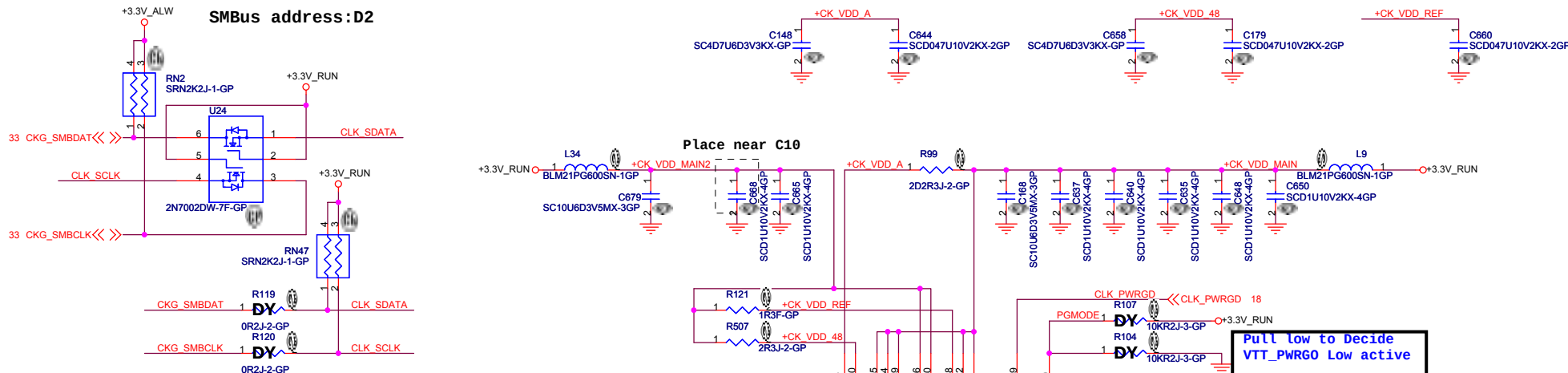
Siberia

Rev
SC

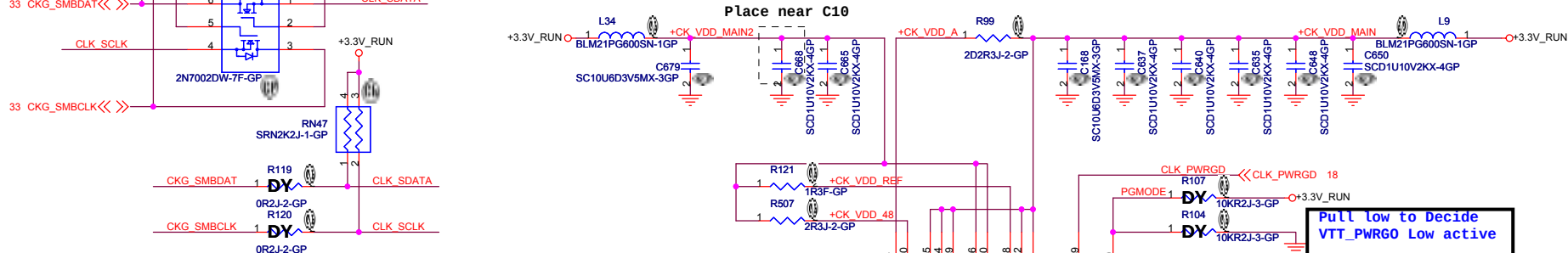
Date: Friday, May 25, 2007

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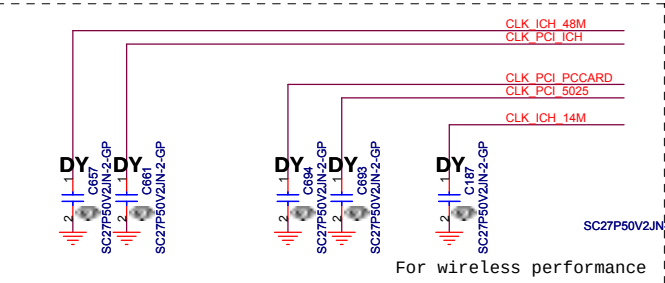
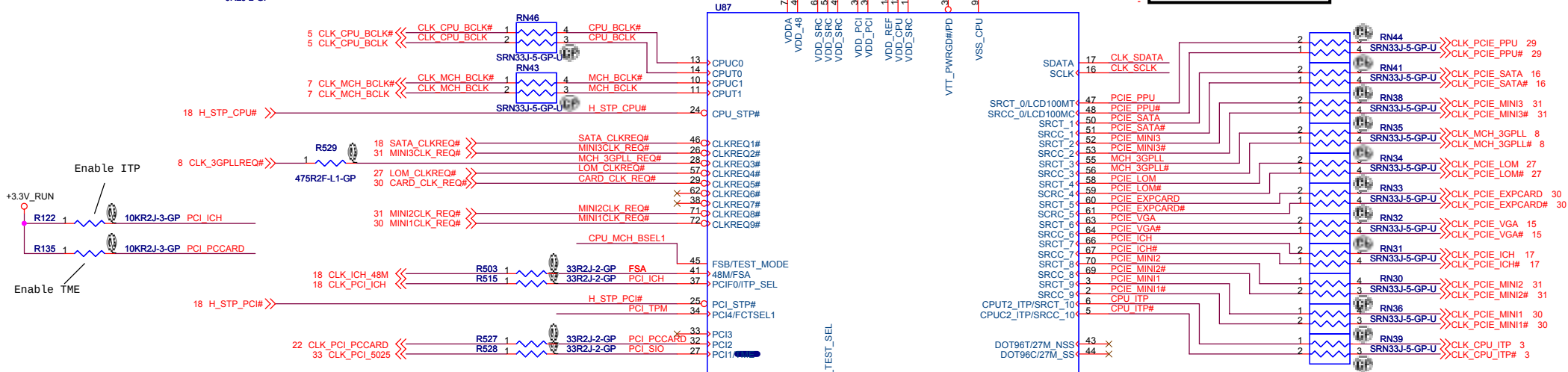
SMBus address:D2



Place near C10



Pull low to Decide VTT_PWRG0 Low active

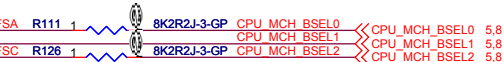


For wireless performance

CL=20pF±0.2pF
Freq. Tolerance:±30ppm

Clock Gen.
1st source: ICS ICS9LPR333CLKF (71.09333.A03)
2nd source: Cypress CY28547LFXC (71.28547.003)

Solder Thermal Pad to GND add min 4 vias

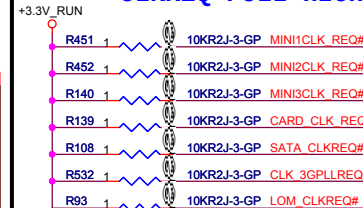


SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

PCI_TPM=FCTSEL1

PIN34	FCTSEL1	0	1
PIN43	DOT96T	27M_NonSpread	
PIN44	DOT96C	27M_Spread	
PIN47	LCD100/96T	SRCT_0	
PIN48	LCD100/96C	SRCC_0	

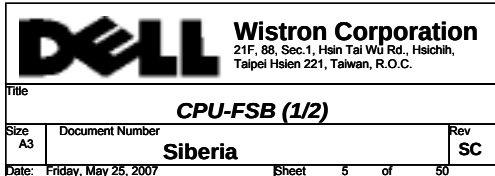
CLKREQ PULL HIGH

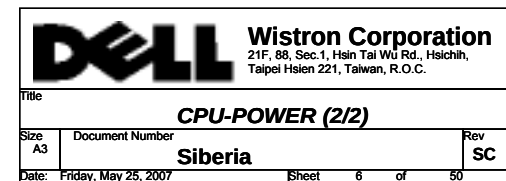


PIN9	PIN39
PGMODE	DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD# (DEFAULT)



Title		
CLK GEN CY28547		
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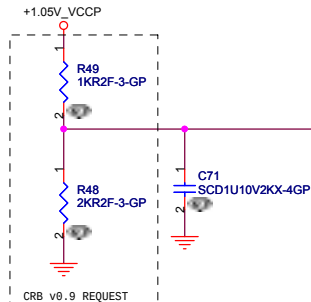


H_D#[63..0] << >> H_D#[63..0] 5
H_A#[35..3] << >> H_A#[35..3] 5
H_REQ#[4..0] << >> H_REQ#[4..0] 5
H_RS#[2..0] >>> H_RS#[2..0] 5

U84A 1 0F 18



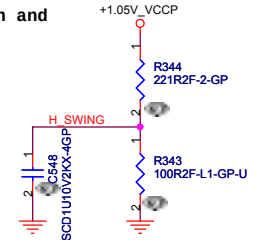
H_REF Decoupling Crestline
close Crestline 100 mil



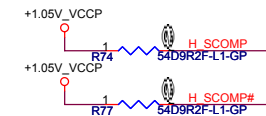
H_SWING routing Trace width and
Spacing use 10 / 20 mil

H_SWING Resistors and
Capacitors close
Caliistoga 500 mil (MAX)

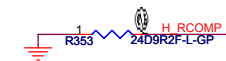
From Schematic Design
Checklit v.1201
221 1% pull high 100
1% pull low



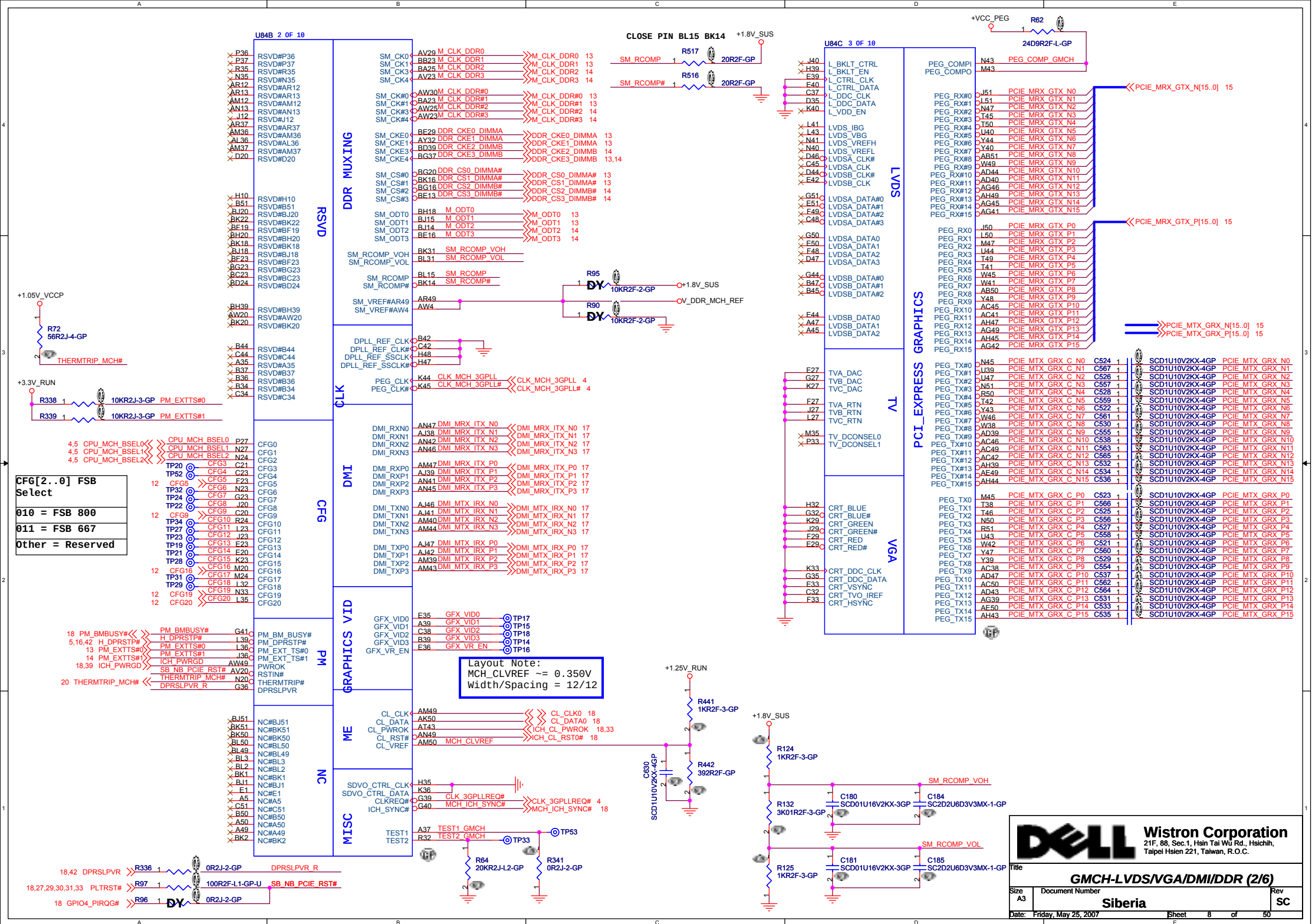
H_SCOMP and H_SCOMP# Resistors
and Capacitors close Caliistoga
500 mil (MAX)
Zo=55ohms



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.



DDR A D[63..0] << >> DDR_A_D[63..0] 13
DDR A BS[2..0] >> DDR_A_BS[2..0] 13,14
DDR A DM[7..0] >> DDR_A_DM[7..0] 13
DDR A DQS[7..0] << >> DDR_A_DQS[7..0] 13
DDR A DQS#[7..0] << >> DDR_A_DQS#[7..0] 13
DDR A MA[14..0] >> DDR_A_MA[14..0] 13,14

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DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS#
DDR A D5	AR45	SA_DQ5			
DDR A D6	AT42	SA_DQ6	SA_DM0	AT45	DDR A DM0
DDR A D7	AW47	SA_DQ7	SA_DM1	BD44	DDR A DM1
DDR A D8	BB45	SA_DQ8	SA_DM2	BD42	DDR A DM2
DDR A D9	BF48	SA_DQ9	SA_DM3	AW38	DDR A DM3
DDR A D10	BG47	SA_DQ10	SA_DM4	AW13	DDR A DM4
DDR A D11	BJ45	SA_DQ11	SA_DM5	BG8	DDR A DM5
DDR A D12	BB47	SA_DQ12	SA_DM6	AY5	DDR A DM6
DDR A D13	BG50	SA_DQ13	SA_DM7	AN6	DDR A DM7
DDR A D14	BH49	SA_DQ14			
DDR A D15	BE45	SA_DQ15	SA_DQS0	AT46	DDR A DQS0
DDR A D16	AW43	SA_DQ16	SA_DQS1	BE48	DDR A DQS1
DDR A D17	BE44	SA_DQ17	SA_DQS2	BB43	DDR A DQS2
DDR A D18	BG42	SA_DQ18	SA_DQS3	BC37	DDR A DQS3
DDR A D19	BE40	SA_DQ19	SA_DQS4	BB16	DDR A DQS4
DDR A D20	BF44	SA_DQ20	SA_DQS5	BH6	DDR A DQS5
DDR A D21	BH45	SA_DQ21	SA_DQS6	BB2	DDR A DQS6
DDR A D22	BG40	SA_DQ22	SA_DQS7	AP3	DDR A DQS7
DDR A D23	BF40	SA_DQ23	SA_DQS#0	AT47	DDR A DQS#0
DDR A D24	AR40	SA_DQ24	SA_DQS#1	BD47	DDR A DQS#1
DDR A D25	AW40	SA_DQ25	SA_DQS#2	BC41	DDR A DQS#2
DDR A D26	AT38	SA_DQ26	SA_DQS#3	BG47	DDR A DQS#3
DDR A D27	AW36	SA_DQ27	SA_DQS#4	BA16	DDR A DQS#4
DDR A D28	AW41	SA_DQ28	SA_DQS#5	BH7	DDR A DQS#5
DDR A D29	AY41	SA_DQ29	SA_DQS#6	BC1	DDR A DQS#6
DDR A D30	AV38	SA_DQ30	SA_DQS#7	AP2	DDR A DQS#7
DDR A D31	AT38	SA_DQ31			
DDR A D32	AV13	SA_DQ32	SA_MA0	BJ19	DDR A MA0
DDR A D33	AT13	SA_DQ33	SA_MA1	BD20	DDR A MA1
DDR A D34	AW11	SA_DQ34	SA_MA2	BK27	DDR A MA2
DDR A D35	AV11	SA_DQ35	SA_MA3	BH28	DDR A MA3
DDR A D36	AU15	SA_DQ36	SA_MA4	BL24	DDR A MA4
DDR A D37	AT11	SA_DQ37	SA_MA5	BK28	DDR A MA5
DDR A D38	BA13	SA_DQ38	SA_MA6	BJ27	DDR A MA6
DDR A D39	BA11	SA_DQ39	SA_MA7	BJ25	DDR A MA7
DDR A D40	BE10	SA_DQ40	SA_MA8	BL28	DDR A MA8
DDR A D41	BD10	SA_DQ41	SA_MA9	BA28	DDR A MA9
DDR A D42	BD8	SA_DQ42	SA_MA10	BC19	DDR A MA10
DDR A D43	AY9	SA_DQ43	SA_MA11	BE28	DDR A MA11
DDR A D44	BG10	SA_DQ44	SA_MA12	BG30	DDR A MA12
DDR A D45	AW9	SA_DQ45	SA_MA13	BJ16	DDR A MA13
DDR A D46	BD7	SA_DQ46	SA_MA14	BJ29	DDR A MA14
DDR A D47	BB9	SA_DQ47			
DDR A D48	BB5	SA_DQ48	SA_RAS#	BE18	DDR A RAS#
DDR A D49	AY7	SA_DQ49	SA_RCVEN#	AY20	M A RCVEN#
DDR A D50	AT5	SA_DQ50			
DDR A D51	AT7	SA_DQ51	SA_WE#	BA19	DDR A WE#
DDR A D52	AY2	SA_DQ52			
DDR A D53	BB7	SA_DQ53			
DDR A D54	AR5	SA_DQ54			
DDR A D55	AR8	SA_DQ55			
DDR A D56	AR9	SA_DQ56			
DDR A D57	AN3	SA_DQ57			
DDR A D58	AM8	SA_DQ58			
DDR A D59	AN10	SA_DQ59			
DDR A D60	AT9	SA_DQ60			
DDR A D61	AN9	SA_DQ61			
DDR A D62	AM9	SA_DQ62			
DDR A D63	AN11	SA_DQ63			

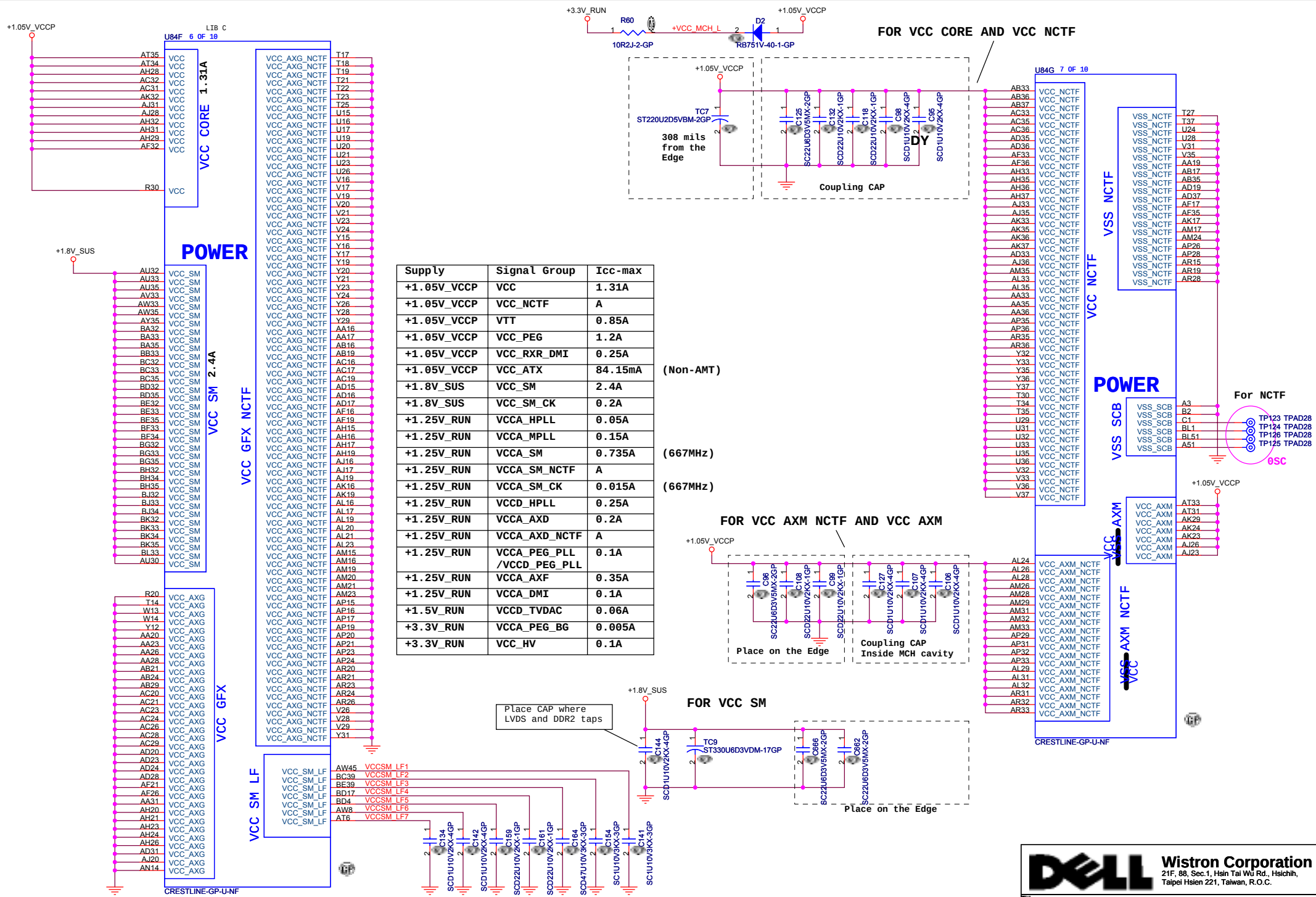
CRESTLINE-GP-U-NF

DDR B D[63..0] << >> DDR_B_D[63..0] 14
DDR B BS[2..0] >> DDR_B_BS[2..0] 14
DDR B DM[7..0] >> DDR_B_DM[7..0] 14
DDR B DQS[7..0] << >> DDR_B_DQS[7..0] 14
DDR B DQS#[7..0] << >> DDR_B_DQS#[7..0] 14
DDR B MA[14..0] >> DDR_B_MA[14..0] 13,14

U84E 5 OF 10

DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AW51	SB_DQ3			
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS#
DDR B D5	AN50	SB_DQ5			
DDR B D6	AV50	SB_DQ6	SB_DM0	AR50	DDR B DM0
DDR B D7	AV49	SB_DQ7	SB_DM1	BD49	DDR B DM1
DDR B D8	BA50	SB_DQ8	SB_DM2	BK45	DDR B DM2
DDR B D9	BB50	SB_DQ9	SB_DM3	BL39	DDR B DM3
DDR B D10	BA49	SB_DQ10	SB_DM4	BH12	DDR B DM4
DDR B D11	BE50	SB_DQ11	SB_DM5	BJ7	DDR B DM5
DDR B D12	BA51	SB_DQ12	SB_DM6	BF3	DDR B DM6
DDR B D13	AY49	SB_DQ13	SB_DM7	AW2	DDR B DM7
DDR B D14	BE50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR B DQS0
DDR B D16	BJ50	SB_DQ16	SB_DQS1	BD50	DDR B DQS1
DDR B D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR B DQS2
DDR B D18	BJ43	SB_DQ18	SB_DQS3	BK39	DDR B DQS3
DDR B D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR B DQS4
DDR B D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR B DQS5
DDR B D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR B DQS6
DDR B D22	BK43	SB_DQ22	SB_DQS7	AV2	DDR B DQS7
DDR B D23	BK42	SB_DQ23	SB_DQS#0	AU50	DDR B DQS#0
DDR B D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR B DQS#1
DDR B D25	BL41	SB_DQ25	SB_DQS#2	BL45	DDR B DQS#2
DDR B D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR B DQS#3
DDR B D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR B DQS#4
DDR B D28	BK41	SB_DQ28	SB_DQS#5	BK7	DDR B DQS#5
DDR B D29	BJ40	SB_DQ29	SB_DQS#6	BF2	DDR B DQS#6
DDR B D30	BL35	SB_DQ30	SB_DQS#7	AV3	DDR B DQS#7
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	SB_MA0	BC18	DDR B MA0
DDR B D33	BE11	SB_DQ33	SB_MA1	BG28	DDR B MA1
DDR B D34	BK11	SB_DQ34	SB_MA2	BG25	DDR B MA2
DDR B D35	BC11	SB_DQ35	SB_MA3	AW17	DDR B MA3
DDR B D36	BC13	SB_DQ36	SB_MA4	BF25	DDR B MA4
DDR B D37	BE12	SB_DQ37	SB_MA5	BE25	DDR B MA5
DDR B D38	BC12	SB_DQ38	SB_MA6	BA29	DDR B MA6
DDR B D39	BG12	SB_DQ39	SB_MA7	BC28	DDR B MA7
DDR B D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR B MA8
DDR B D41	BL9	SB_DQ41	SB_MA9	BD37	DDR B MA9
DDR B D42	BK5	SB_DQ42	SB_MA10	BG17	DDR B MA10
DDR B D43	BL5	SB_DQ43	SB_MA11	BE37	DDR B MA11
DDR B D44	BK9	SB_DQ44	SB_MA12	BA39	DDR B MA12
DDR B D45	BK10	SB_DQ45	SB_MA13	BG13	DDR B MA13
DDR B D46	BJ8	SB_DQ46	SB_MA14	BE24	DDR B MA14
DDR B D47	BJ6	SB_DQ47			
DDR B D48	BF4	SB_DQ48	SB_RAS#	AV16	DDR B RAS#
DDR B D49	BH5	SB_DQ49	SB_RCVEN#	AY18	M B RCVEN#
DDR B D50	BG1	SB_DQ50			
DDR B D51	BC2	SB_DQ51	SB_WE#	BC17	DDR B WE#
DDR B D52	BK3	SB_DQ52			
DDR B D53	BE4	SB_DQ53			
DDR B D54	BD3	SB_DQ54			
DDR B D55	BJ2	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AR1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AU2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

CRESTLINE-GP-U-NF



Supply	Signal Group	Icc-max
+1.05V_VCCP	VCC	1.31A
+1.05V_VCCP	VCC_NCTF	A
+1.05V_VCCP	VTT	0.85A
+1.05V_VCCP	VCC_PEG	1.2A
+1.05V_VCCP	VCC_RXR_DMI	0.25A
+1.05V_VCCP	VCC_ATX	84.15mA
+1.8V_SUS	VCC_SM	2.4A
+1.8V_SUS	VCC_SM_CK	0.2A
+1.25V_RUN	VCCA_HPLL	0.05A
+1.25V_RUN	VCCA_MPLL	0.15A
+1.25V_RUN	VCCA_SM	0.735A
+1.25V_RUN	VCCA_SM_NCTF	A
+1.25V_RUN	VCCA_SM_CK	0.015A
+1.25V_RUN	VCCD_HPLL	0.25A
+1.25V_RUN	VCCA_AXD	0.2A
+1.25V_RUN	VCCA_AXD_NCTF	A
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A
+1.25V_RUN	VCCA_AXF	0.35A
+1.25V_RUN	VCCA_DMI	0.1A
+1.5V_RUN	VCCD_TVDAC	0.06A
+3.3V_RUN	VCCA_PEG_BG	0.005A
+3.3V_RUN	VCC_HV	0.1A

(Non-AMT)

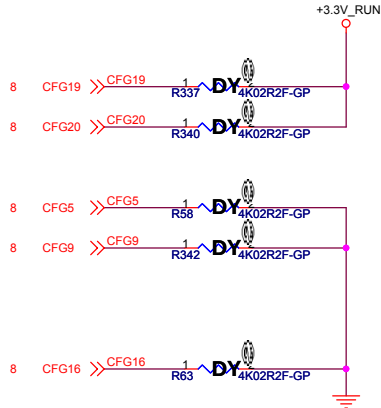
(667MHz)

(667MHz)

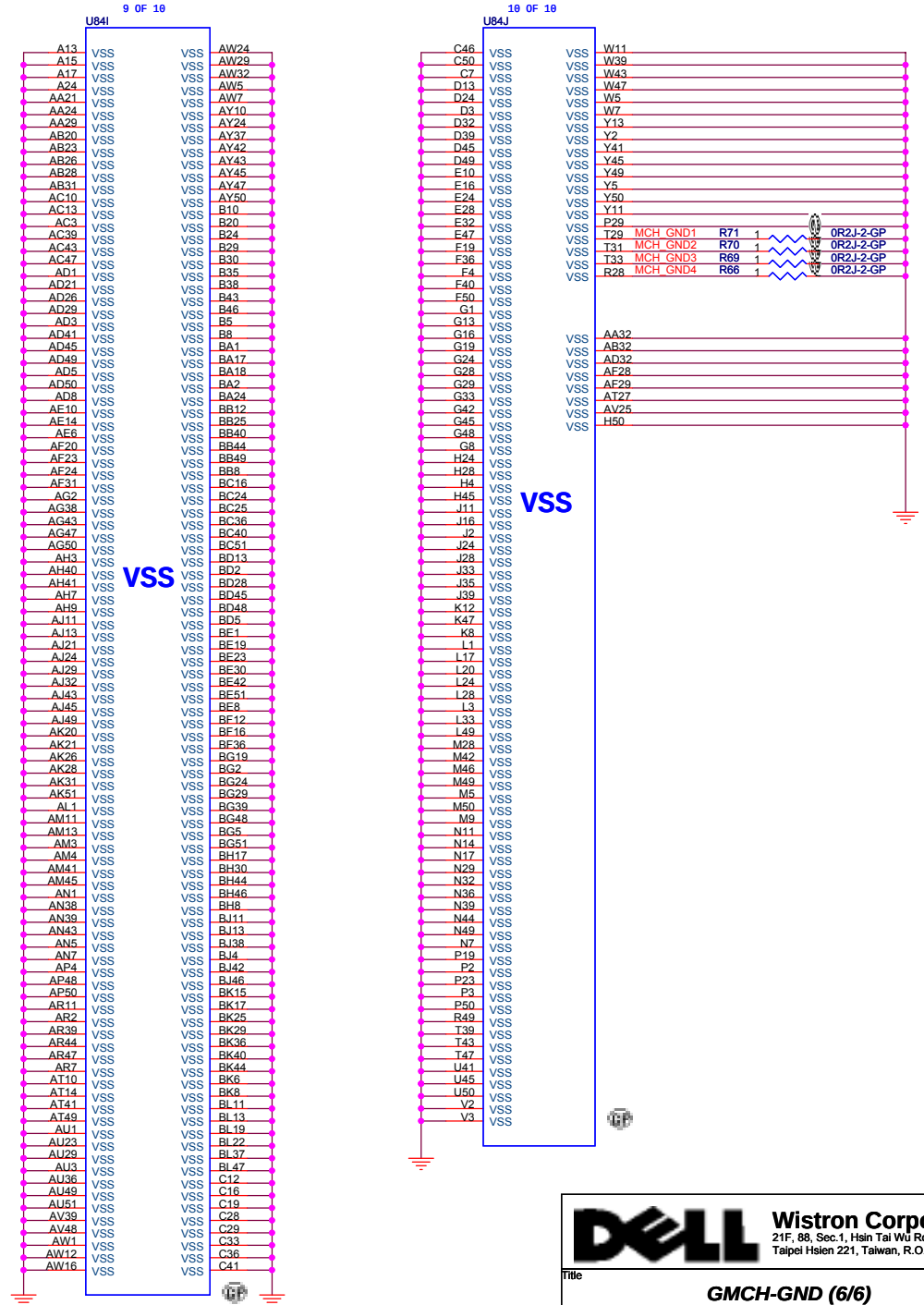


Title		
GMCH-POWER (4/6)		
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Layout Note:
Location of all MCH CFG strap resistors
need to be close to trace to minimize stub



CFG Strap	LOW 0	HIGH 1
CFG 5		
CFG 9	DMI X 2	DMI X 4
PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)
CFG 16		
FSB Dynamic ODT	Disabled	Enabled
CFG 18		
VCC select	1.05V	1.5V
CFG 19		
DMI Lane Reserved	Normal Operation	Reserved Lane
CFG 20		
Concurrent SDVO/PCIE	Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous
CFG 12 CFG 13	XOR/ALL -Z	
LL(00)	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HH(11)	Normal Operation	





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Title

GMCH-GND (6/6)

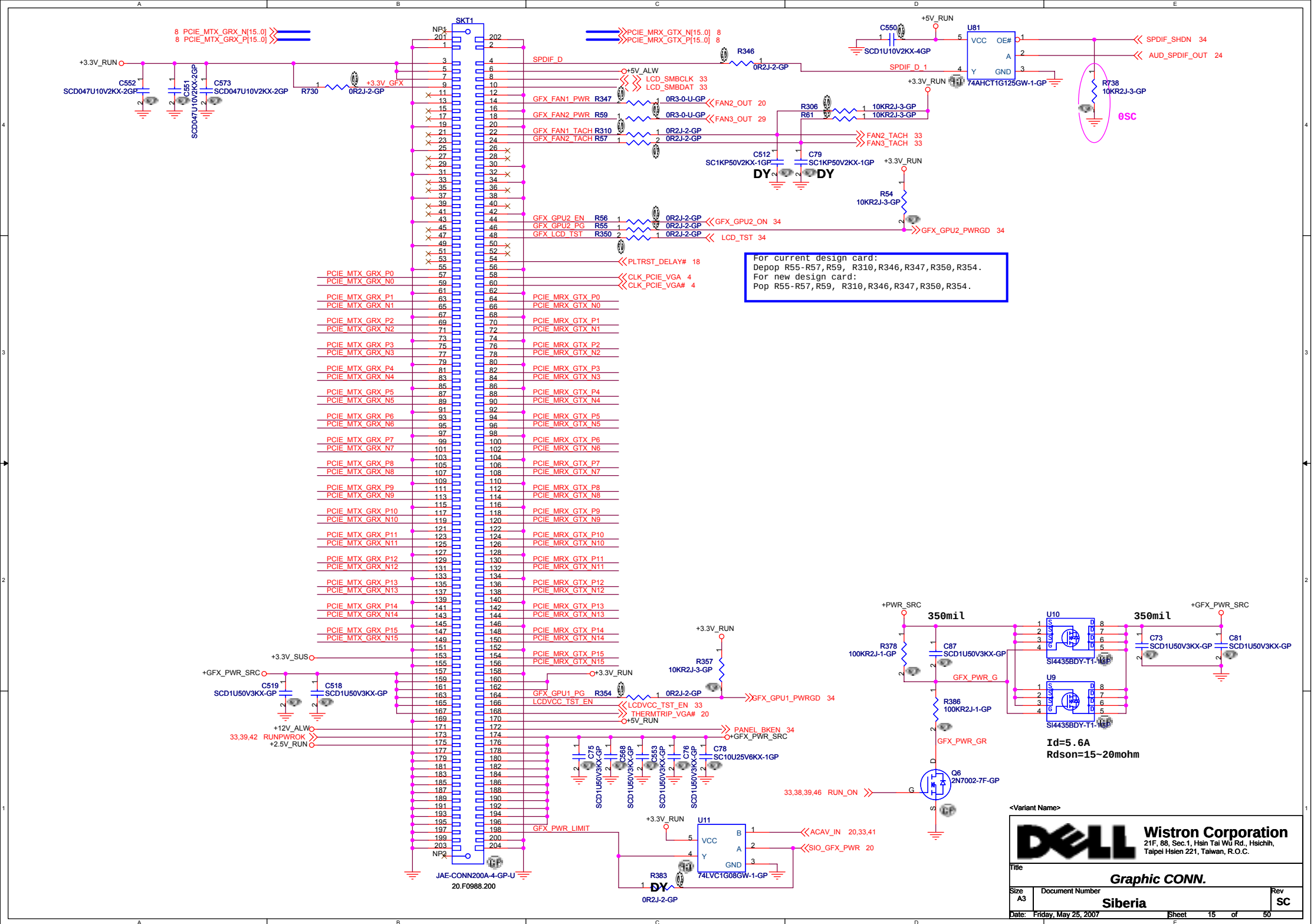
Size
A3

Document Number
Siberia

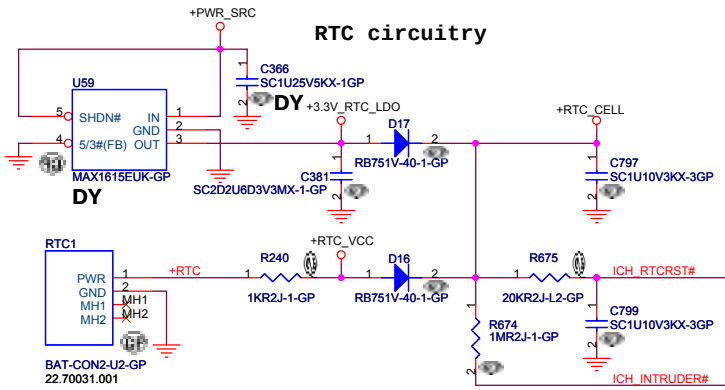
Rev
SC

Date: Friday, May 25, 2007

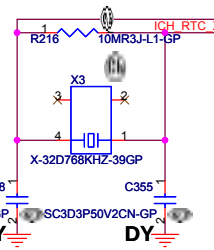
Sheet 12 of 50



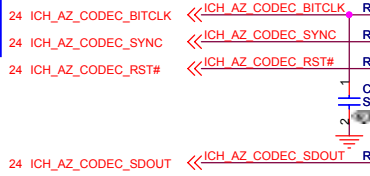
RTC circuitry



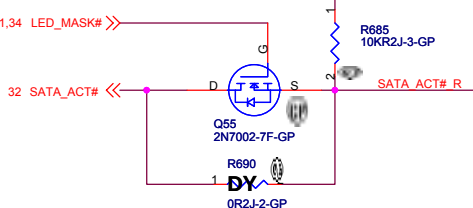
CL=6pF
Freq. Tolerance:±10ppm



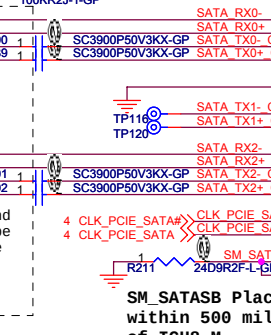
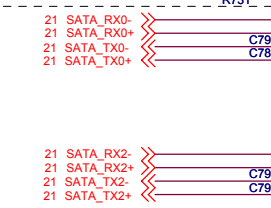
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source.



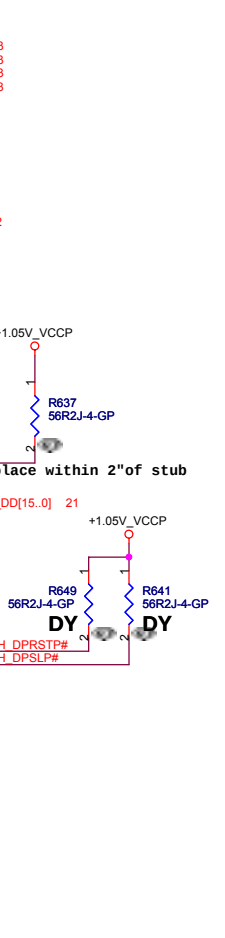
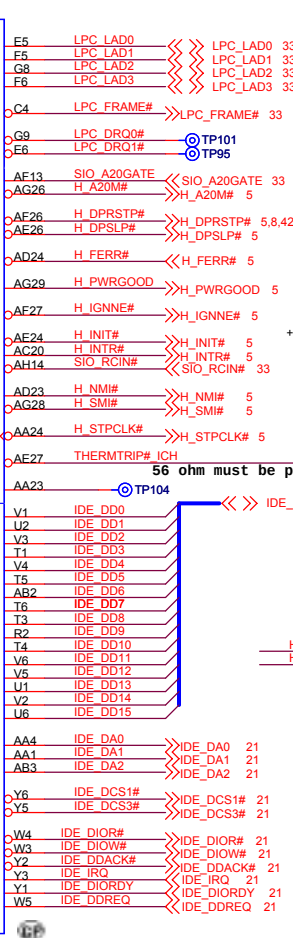
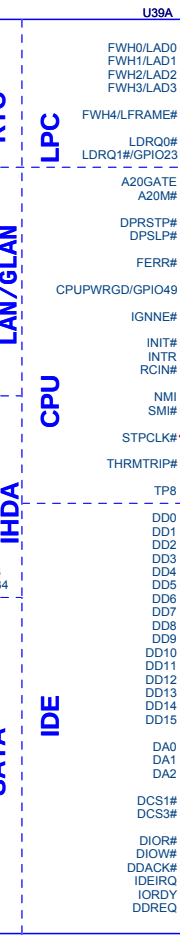
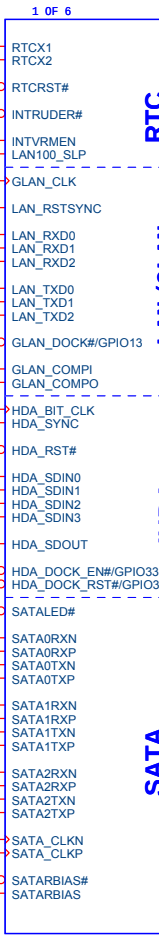
This circuit is only needed if the platform has the SNIFFER



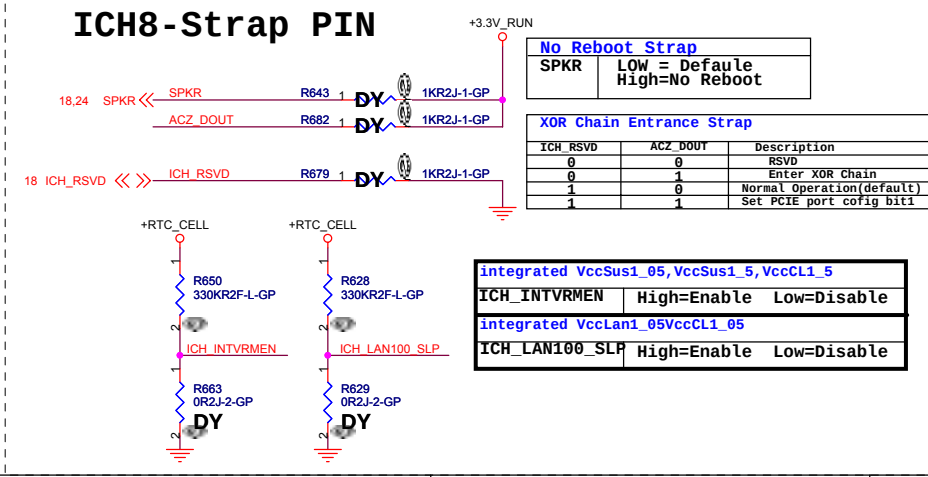
Distance between the ICH8-M and cap on the "P" signal should be identical distance between the ICH8-M and cap on the "N" signal for same pair.



SM_SATASB Place within 500 mil of ICH8-M



ICH8-Strap PIN



No Reboot Strap
SPKR LOW = Default High=No Reboot

XOR Chain Entrance Strap		
ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIe port config bit1

Integrated VccSus1_05,VccSus1_5,VccCl1_5		
ICH_INTVRMEN	High=Enable Low=Disable	
Integrated VccLan1_05VccCl1_05		
ICH_LAN100_SLP	High=Enable Low=Disable	

<Variant Name>

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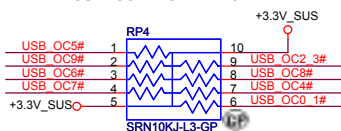
LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	MiniCard WPAN
LANE4	Express Card
LANE5	PPU Card
LANE6	Giba Bit LOM

The diagram illustrates the pin configuration for PCI-Express lanes 0 through 27. It is organized into four groups of seven lanes each, with each lane having a corresponding pin number and function. The functions are categorized into RX (Receive), TX (Transmit), and GLAN (Gigabit LAN) TX/RX.

Lane	Pin	Function
31	P27	PERN6
30	P26	PERP6
29	P25	PETN6
28	P24	PETP6
31	M27	PERN2
30	M26	PERP2
29	L29	PETN2
28	L28	PETP2
31	K27	PERN3
30	K26	PERP3
29	J29	PETN3
28	J28	PETP3
31	H27	PERN4
30	H26	PERP4
29	G29	PETN4
28	G28	PETP4
29	F27	PERN5
28	F26	PERP5
27	E29	PETN5
26	E28	PETP5
27	D27	PERN6/GLAN_RXN
26	D26	PERP6/GLAN_RXP
25	C29	PETN6/GLAN_TXN
24	C28	PETP6/GLAN_TXP

ICH8-Strap PIN

PCI_GNT#0 (R617)	SPI_CS#1 (R623)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R620)	low = A16 swap override enable high = default	



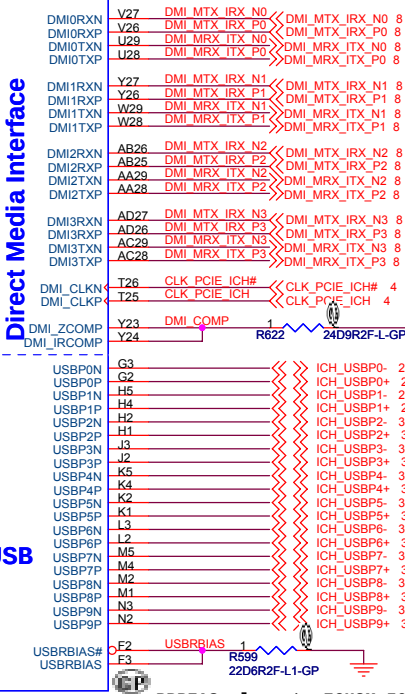
PCI-Express Media Interface

SPI

AN_RXN
AN_RXP
AN_TXN
AN_TXP

O40
O41
O42

USE

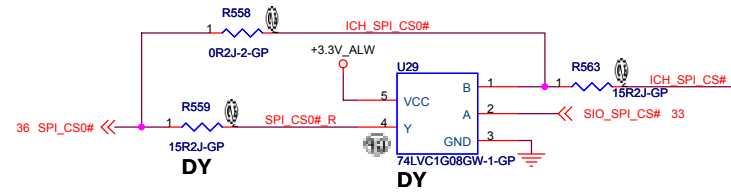


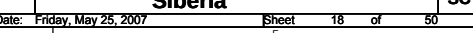
DMI_COMP R622 place
within 500 mil of ICH8M

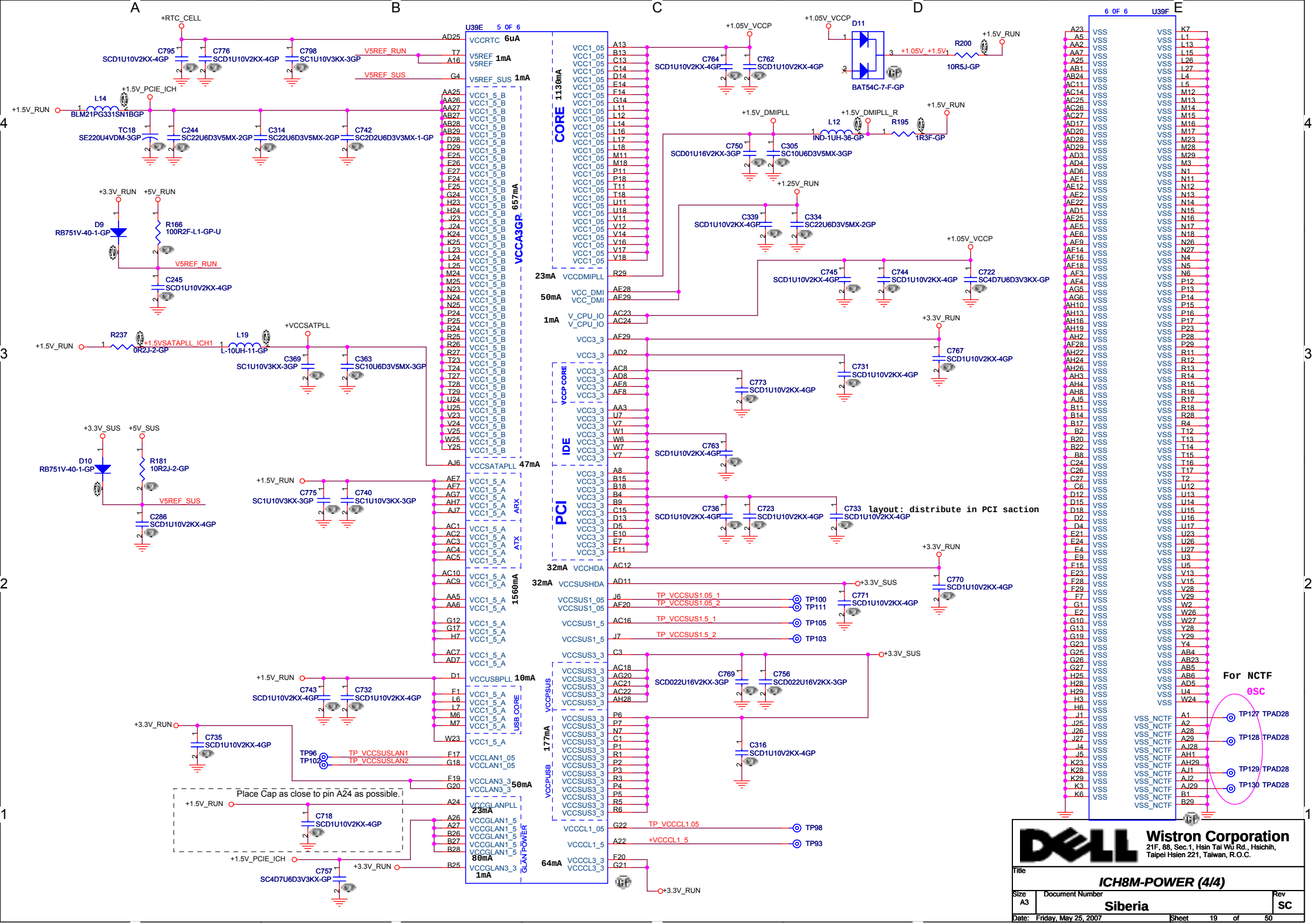
ICH

USB0	Ext Left Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

USBRBIAS close to ICH8M 500
mils and Trace impedance
should be 60 ohm +/- 15%

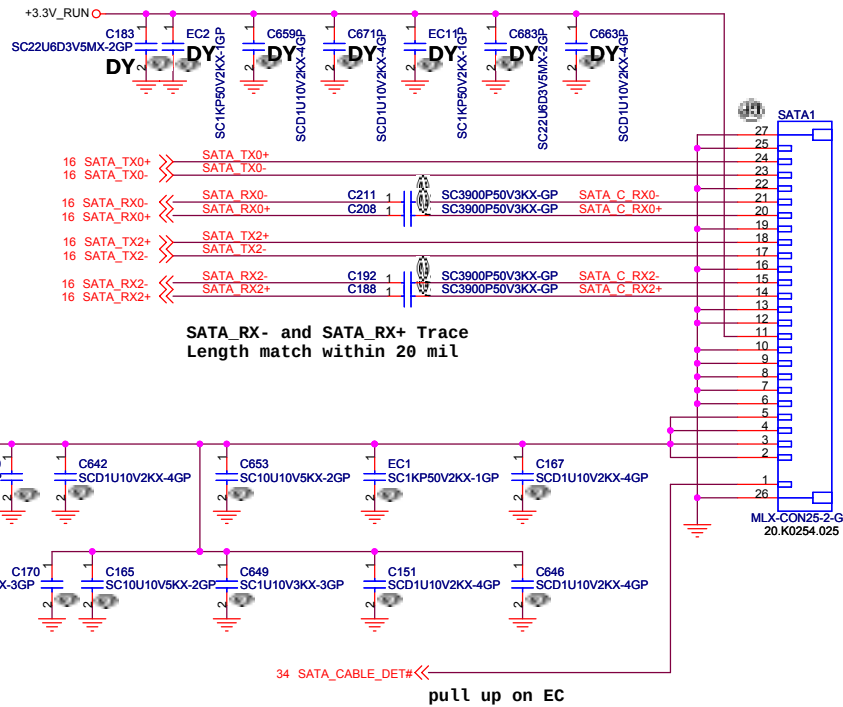
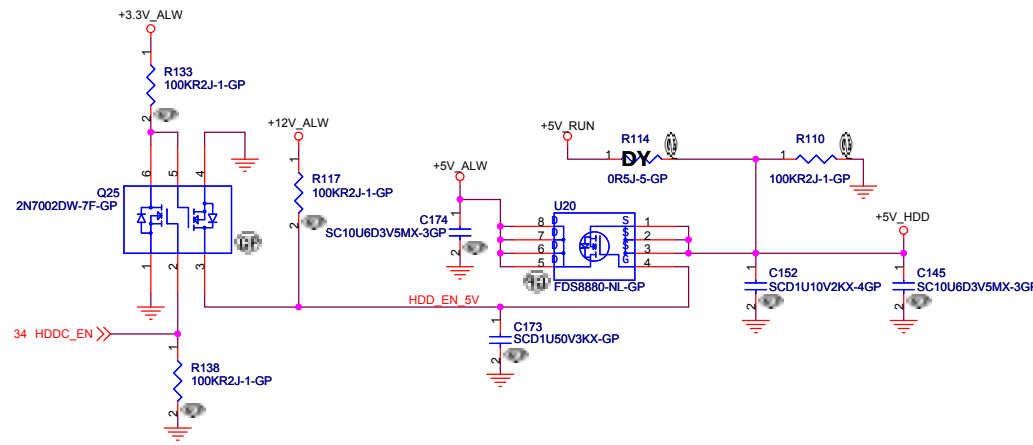




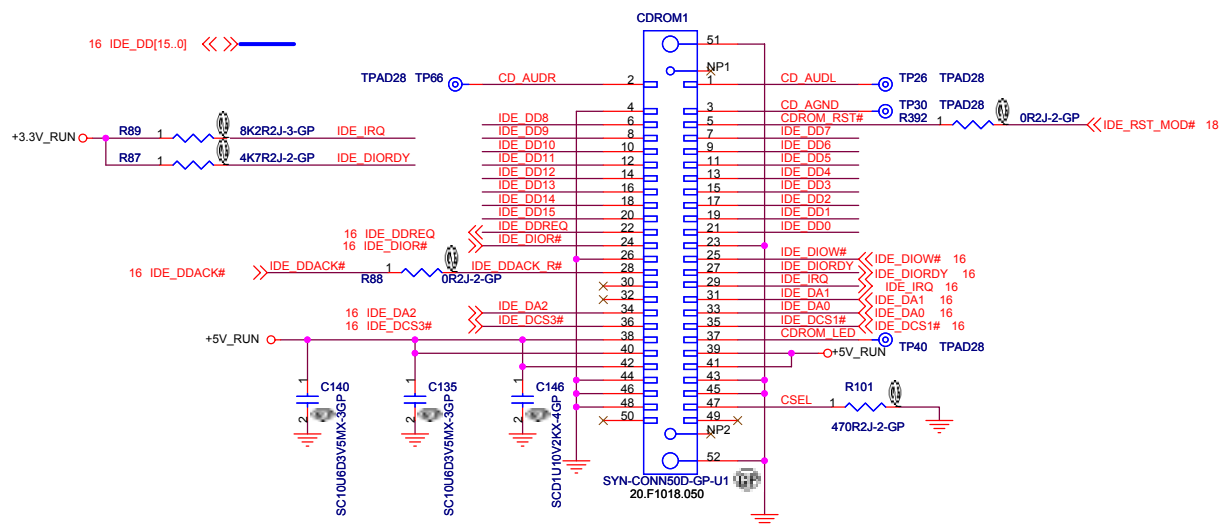


SSID = IDE & SATA

SATA HDD Connector



ODD Connector

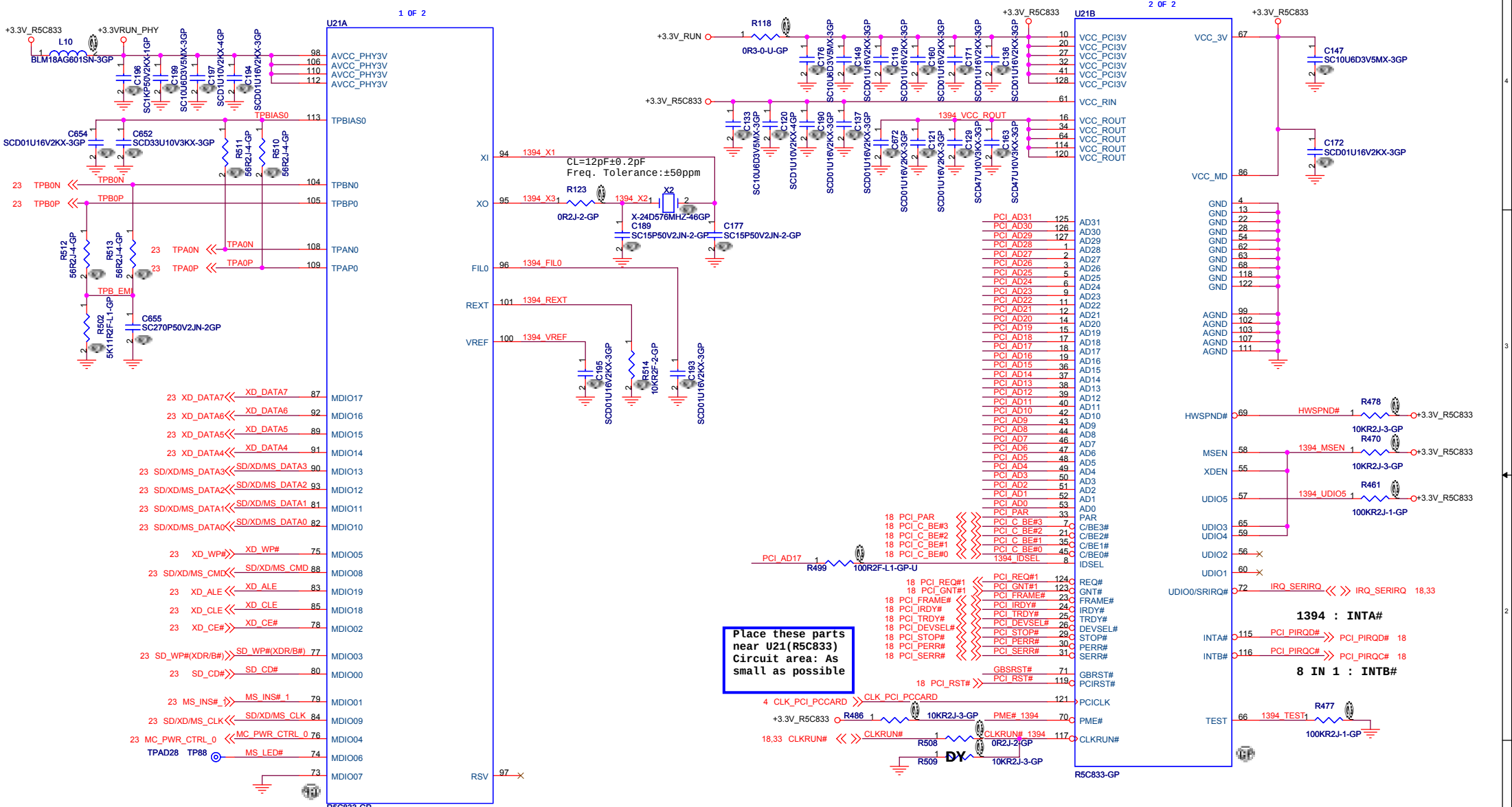


<Variant Name>

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Title: **HDD&ODD**

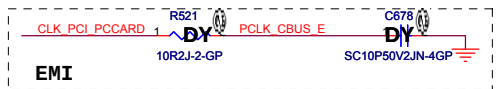
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We use the R5C832 in X00 for R5C833 not ready.

SSID = 1394

Place these parts near U21(R5C833)
Circuit area: As small as possible



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Title

1394 - R5C833

Size A3 Document Number

Siberia

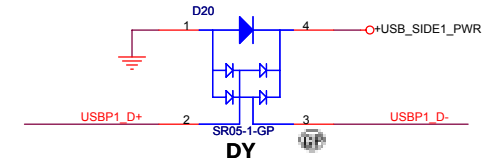
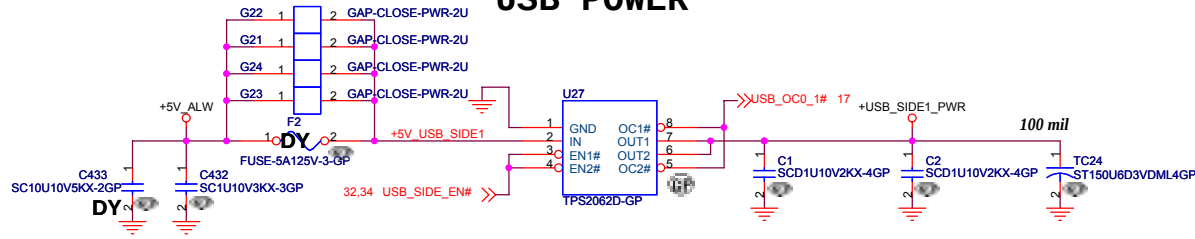
Date: Friday, May 25, 2007

Rev

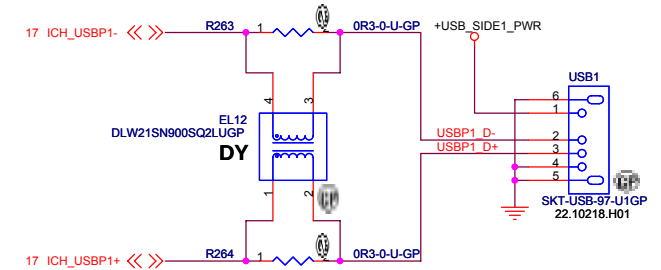
SC

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USB POWER

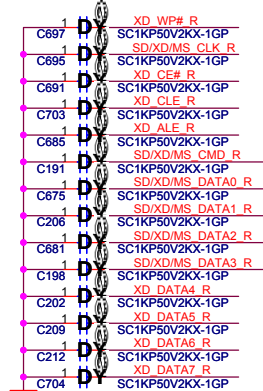
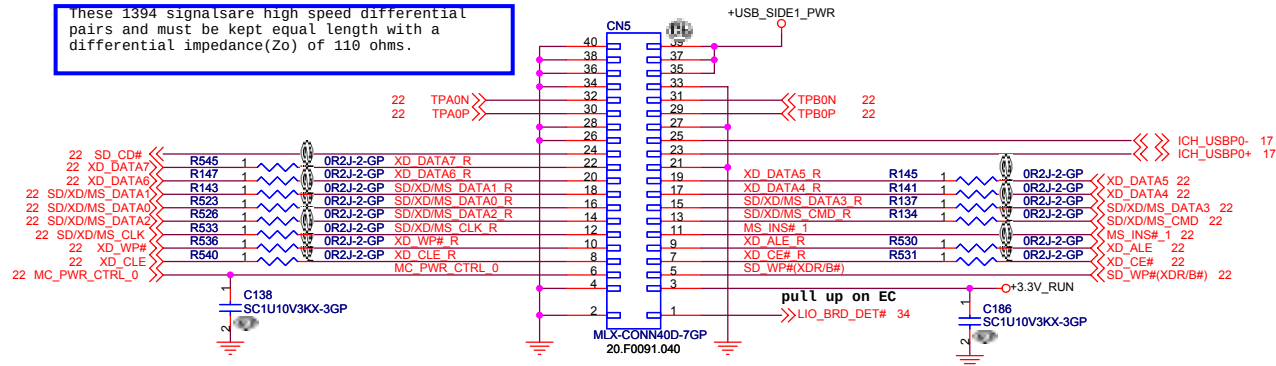


Place ESD diodes as close to the connector as possible.



I/O board conn. (1394/7 IN 1/USB)

These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Z_0) of 110 ohms.



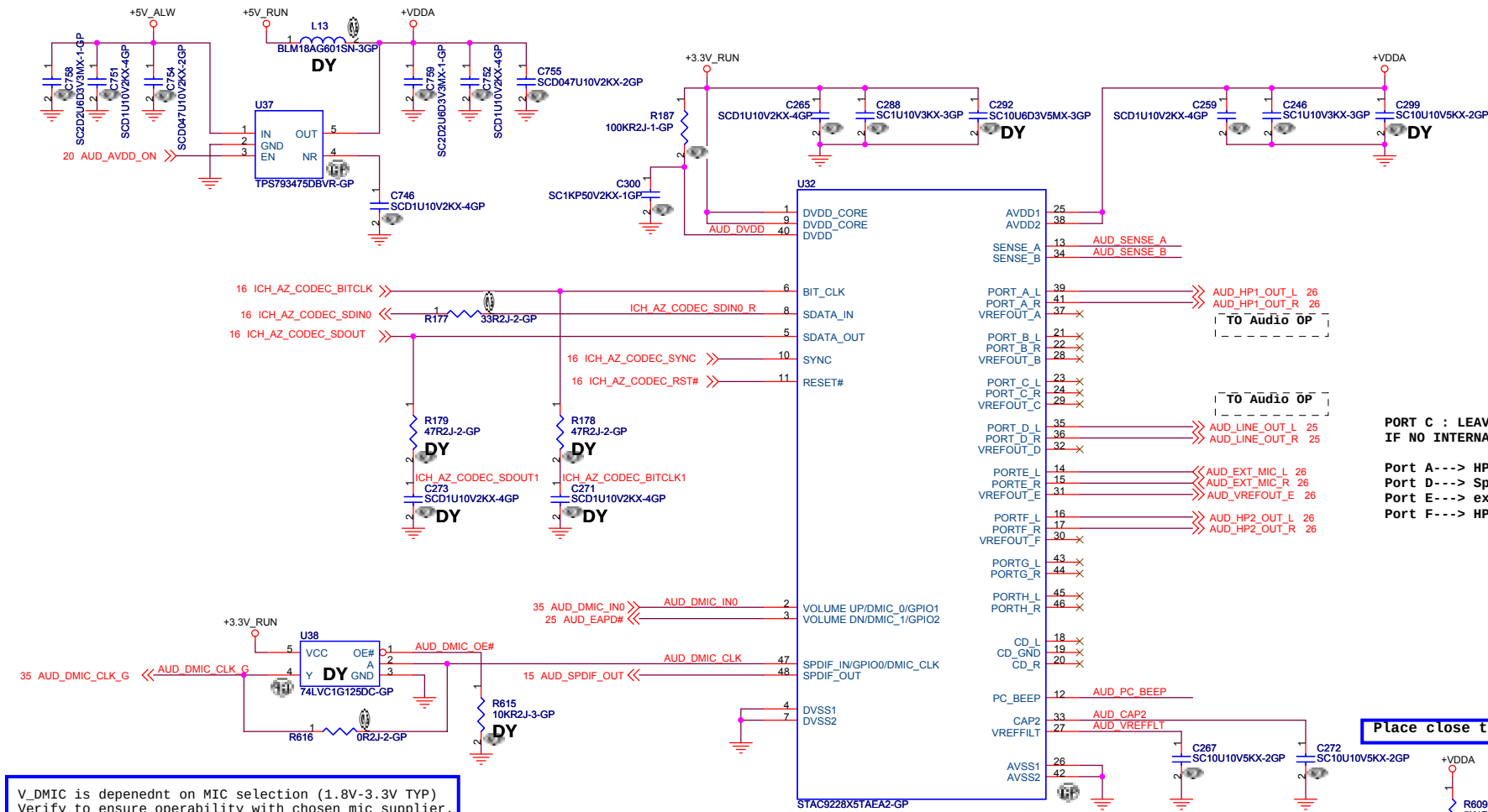
<Variant Name>

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Title
I/O board (1394/7 IN 1/USB) / USB CONN.

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V_DMIC is depenednt on MIC selection (1.8V-3.3V TYP). Verify to ensure operability with chosen mic supplier.
 Note1: If only 1 digital mic, use AUD_DMIC_IN0.
 Note2: If using 2 digital mics, also use AUD_DMIC_IN0. This input supports 2 digital mics.
 AUD_DMIC_IN1 is only used to support 4 digital mics.

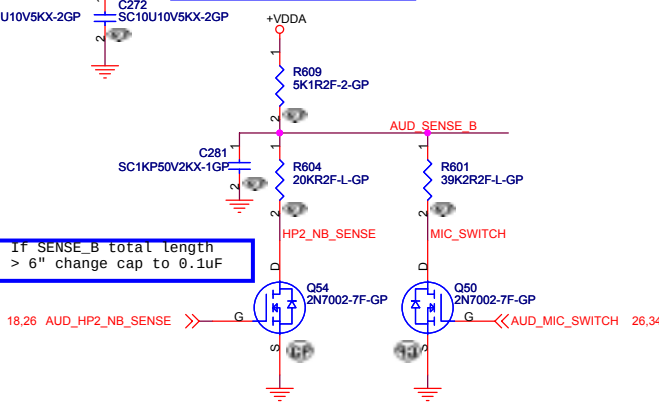
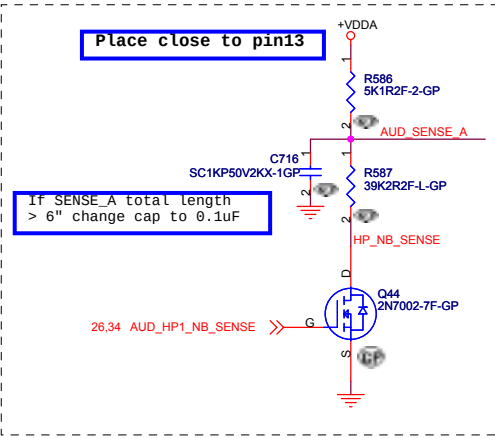
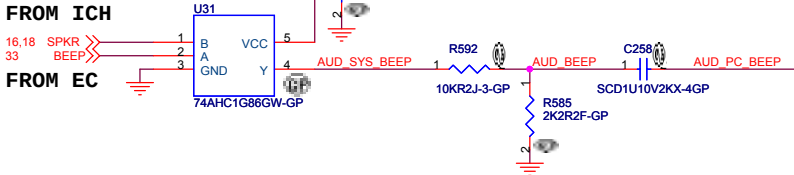
PORT C : LEAVE NC
 IF NO INTERNAL MICS.
 Port A---> HP1
 Port D---> Speaker
 Port E---> ext Mic
 Port F---> HP2

Place close to pin34

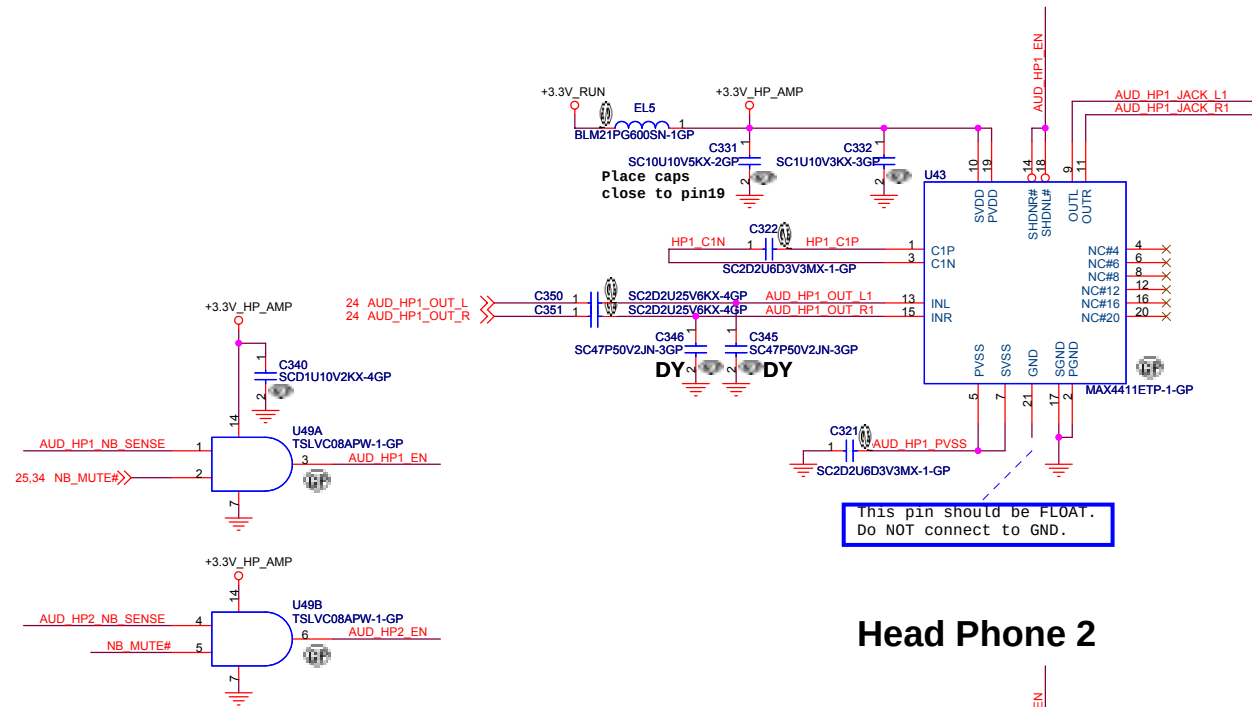
Place close to pin13

If SENSE_A total length > 6" change cap to 0.1uF

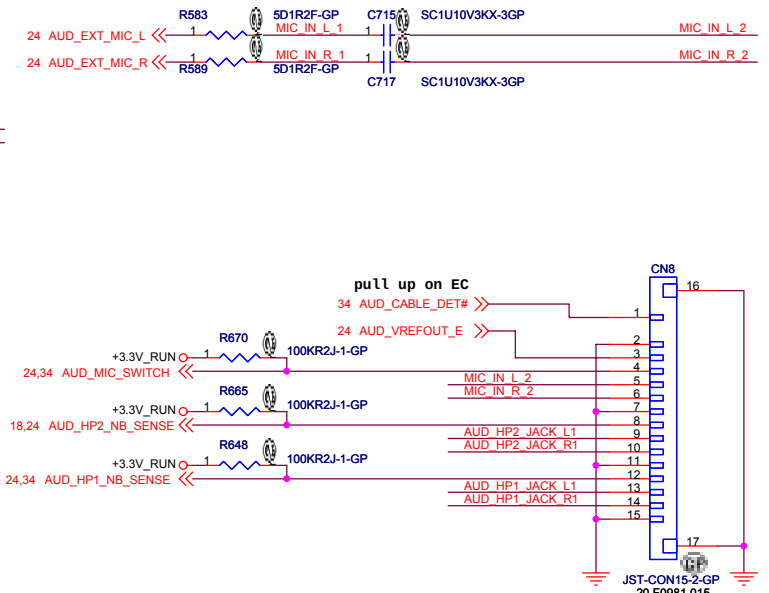
If SENSE_B total length > 6" change cap to 0.1uF



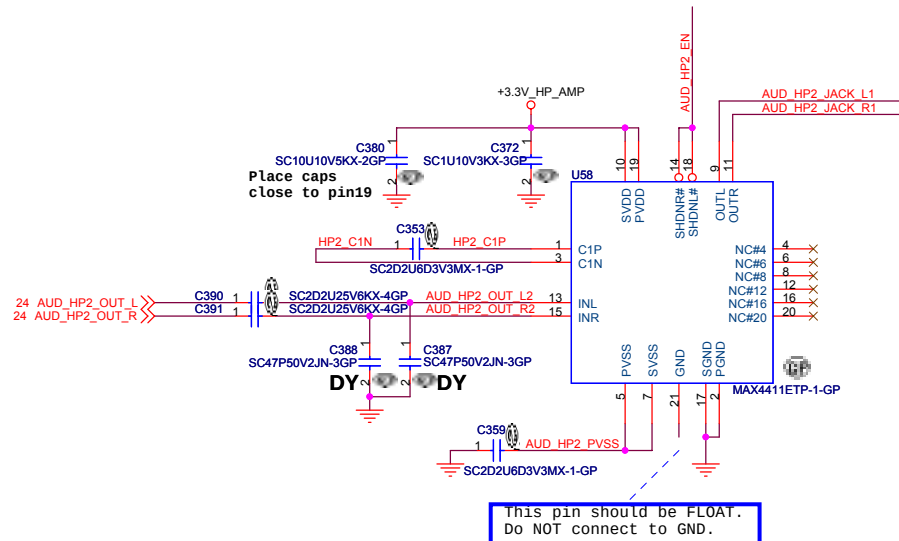
Head Phone 1



MIC



Head Phone 2



<Core Design>



Title			AUDIO (3/3)	
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Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Place filters close to the power pins - 47pF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Place one cap close to each of the pins, 38, 45 and 52.

Place resistor as close as possible to the ASIC. Pad is needed to measure 125MHz clock for debugging.

Important Layout Note for Dual footprint design:
AT4501 is available in standard package size, where as ST-Micro part is available in narrow package size. Ensure that pads are laid out for both footprints.
Recommendation: Pads for pins 1 (reference) through 4 can be standard and identically located for both packages. Pads for pins 5-8 need to be larger to accommodate both packages.

LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOM_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIO defined by the GPIO mapping.

Layout Note:
PNP Q3 and Q64 needs 0.5 inch by 0.5 inch thermal relief pad.

REGSEN12 and REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane. Use 8mils trace width for these signals

Place C447 as close to pin17 of LOM as possible.

Place C457 as close to pin13 of LOM as possible.

Place high-frequency decoupling cpas close to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Atto-Sense Mode	S0	S1	CS#	SCLK
ST M45PE10	1	0	0	0
Atmel AT45DB011B	1	1	0	0

VDDIOPower Decoupling

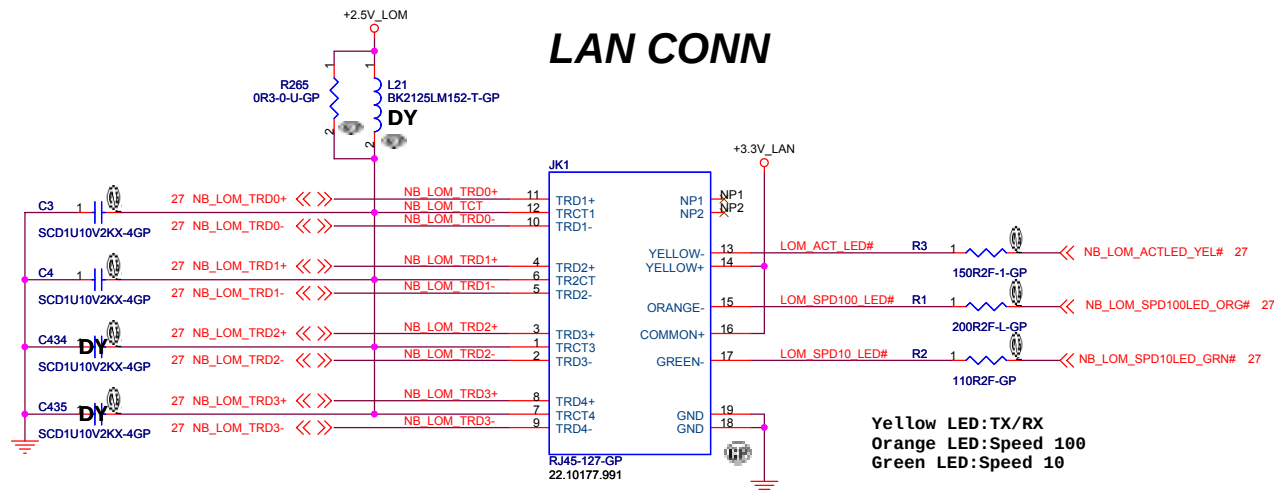
VDDP Power Decoupling

Core Power Decoupling



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Title		LAN BCM5754M	
Size	Document Number	Siberia	Rev
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1. Route as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. Pairs must be equal lengths.
5. 4mil trace width, 7mil separation.
6. 30mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

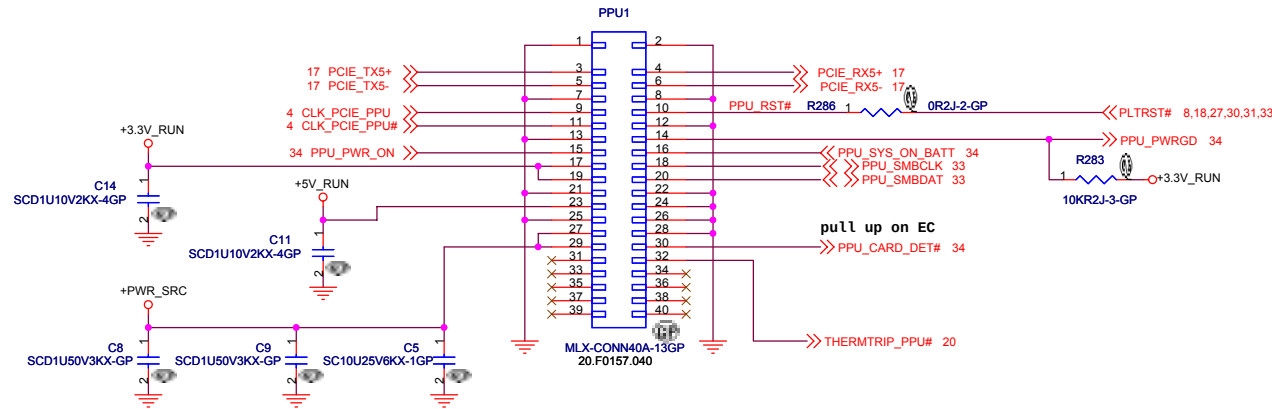
The blowout from the LAN magnetics to the RJ45 connector maintaining the distance between the two to be within 1 inch.

<Variant Name>

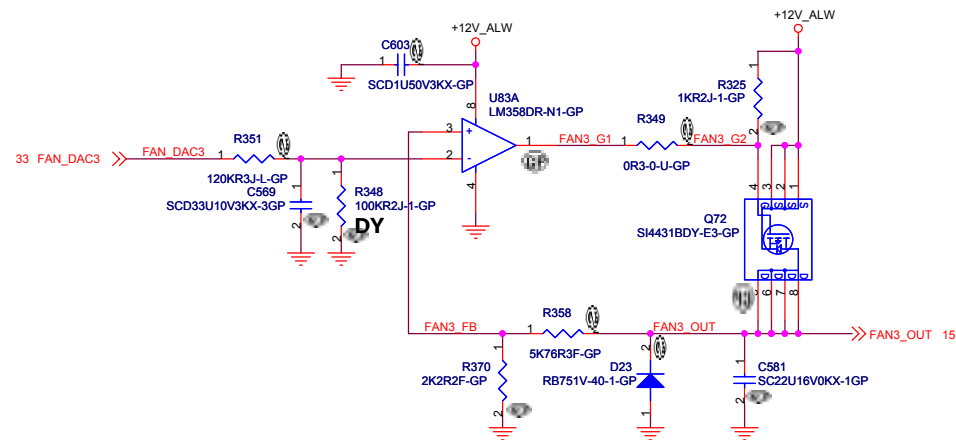


Title			LAN Connector	
Size	Document Number	Rev		
A3	Siberia	SC		
Date:	Friday, May 25, 2007	Sheet	28	of 50

PPU connector



2nd GPU FAN

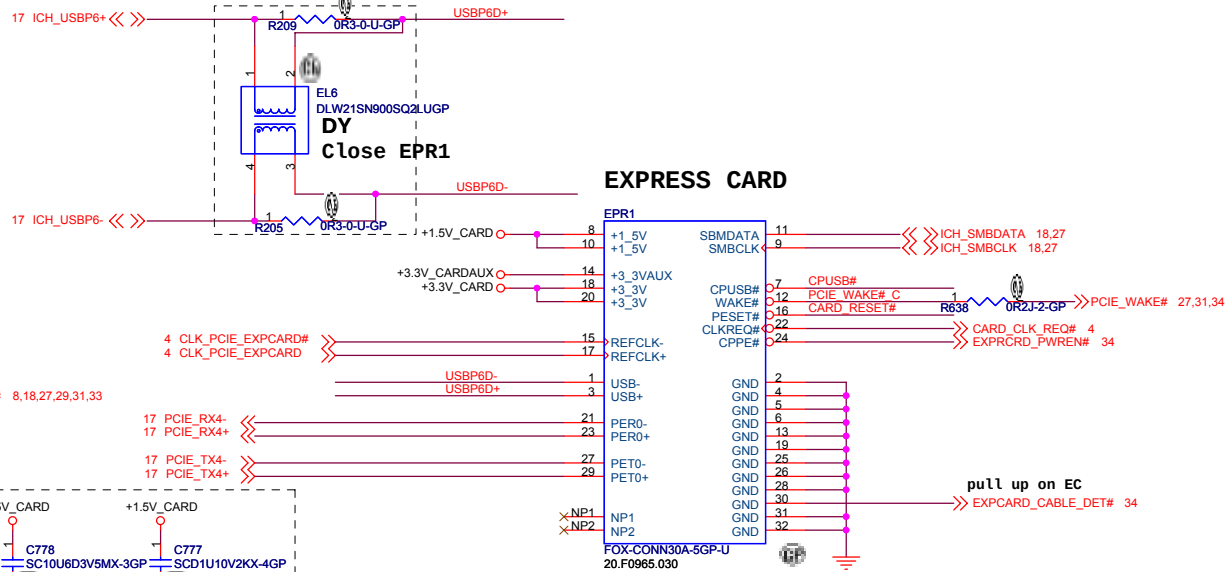
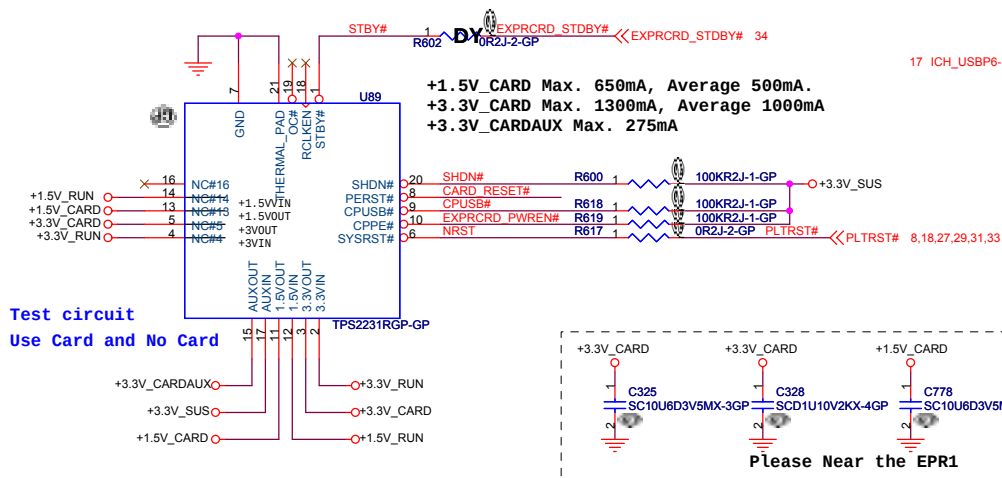
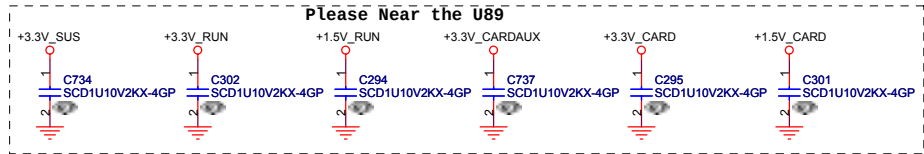


<Variant Name>



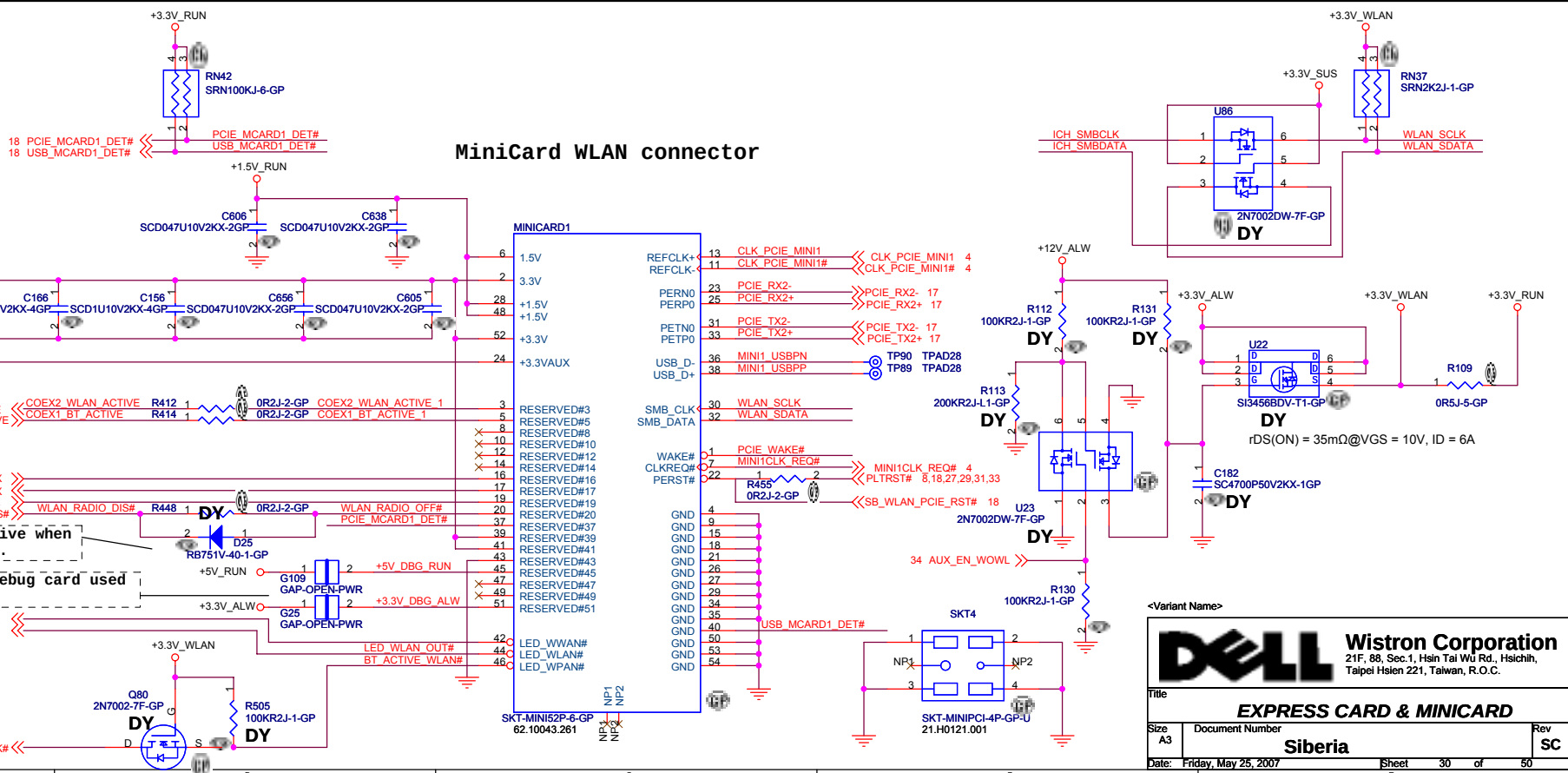
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Title		PPU CONN. / 2rd GPU FAN	
Size	Document Number	Rev	SC
A3	Siberia		
Date:	Friday, May 25, 2007	Sheet	29 of 50



DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



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EXPRESS CARD & MINICARD

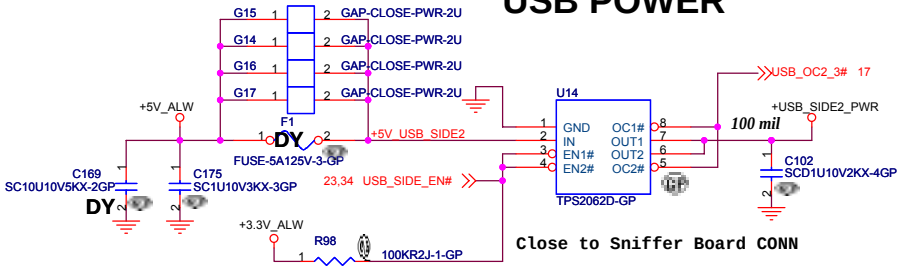
Siberia

Friday, May 25, 2007

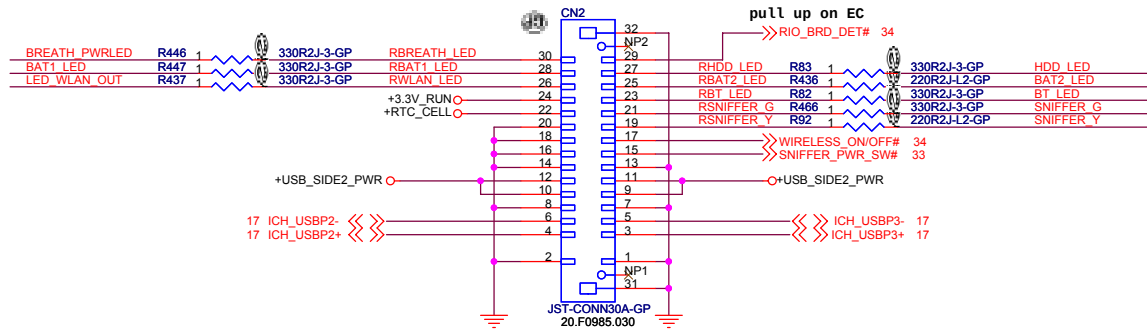
Sheet 30 of 50



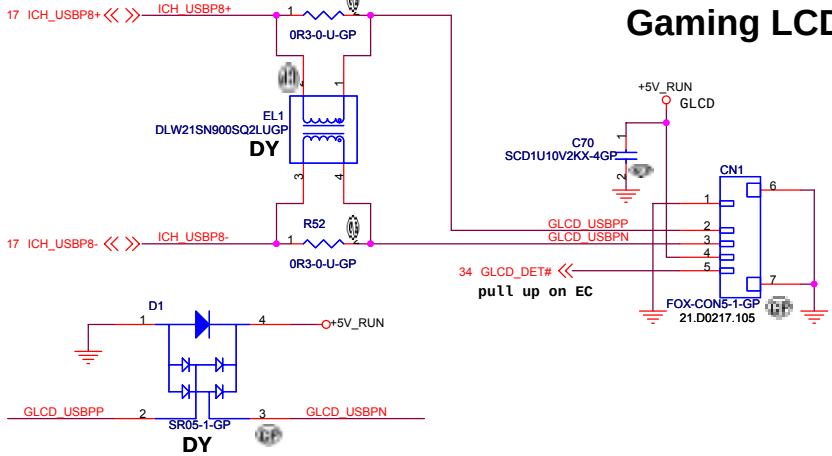
USB POWER



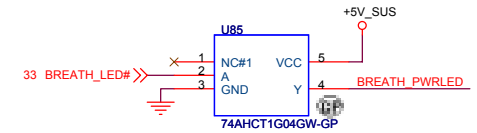
Sniffer board for USB, Indicator LEDs, Sniffer Switch conn.



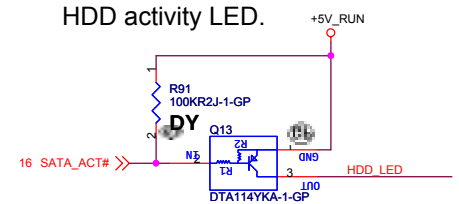
Gaming LCD



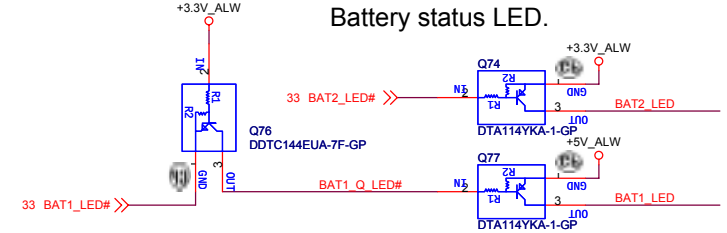
Power & Suspend LED.



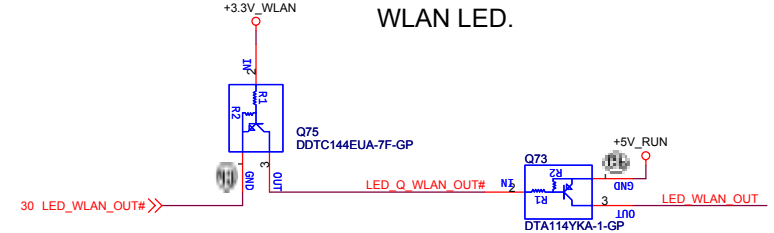
HDD activity LED.



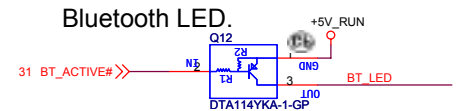
Battery status LED.



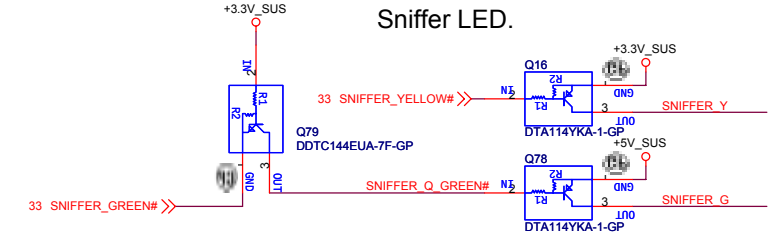
WLAN LED.



Bluetooth LED.



Sniffer LED.

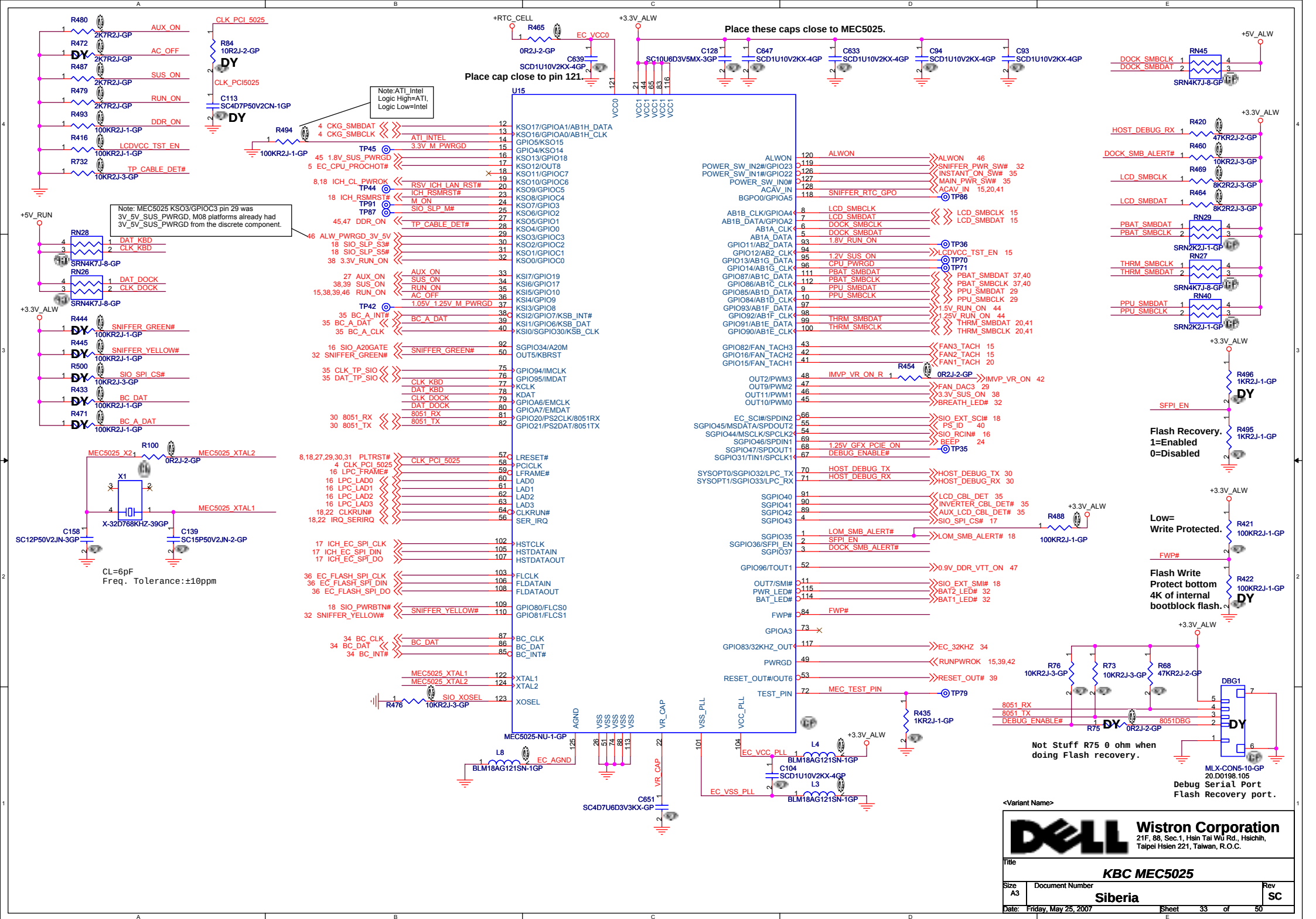


<Variant Name>

DELL

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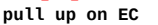
Title			
Sniffer board (USB/Status LEDs) / Gaming LCD			
Size A3	Document Number	Rev	
	Siberia	SC	
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+RTC_CELL
R544
10KR2J-3GP



KB BKLT LED





Sheet 36 of 50

LEFT SPKR LED

The diagram shows four parallel channels for driving Red, Green, and Blue LEDs. Each channel consists of a 5V_RUN input, a 10K resistor, an LED, a 2N7002-7F-GP MOSFET, and a BSS138-4-GP MOSFET.

- Red Channel:** 5V_RUN → R539 (10K) → LED L SPKR R# → Q29 (2N7002-7F-GP) → Q34 (BSS138-4-GP) → L_SPKRLED_R#
- Green Channel:** 5V_RUN → R548 (10K) → LED L SPKR G# → Q39 (2N7002-7F-GP) → Q40 (BSS138-4-GP) → L_SPKRLED_G#
- Blue Channel:** 5V_RUN → R562 (10K) → LED L SPKR B# → Q41 (2N7002-7F-GP) → Q45 (BSS138-4-GP) → L_SPKRLED_B#

RIGHT SPKR LED

KB BKLT LED

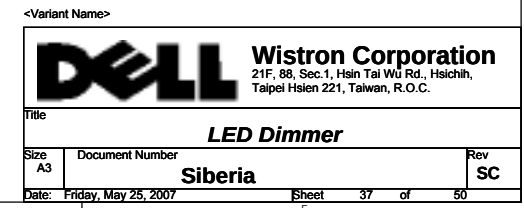
TP LED

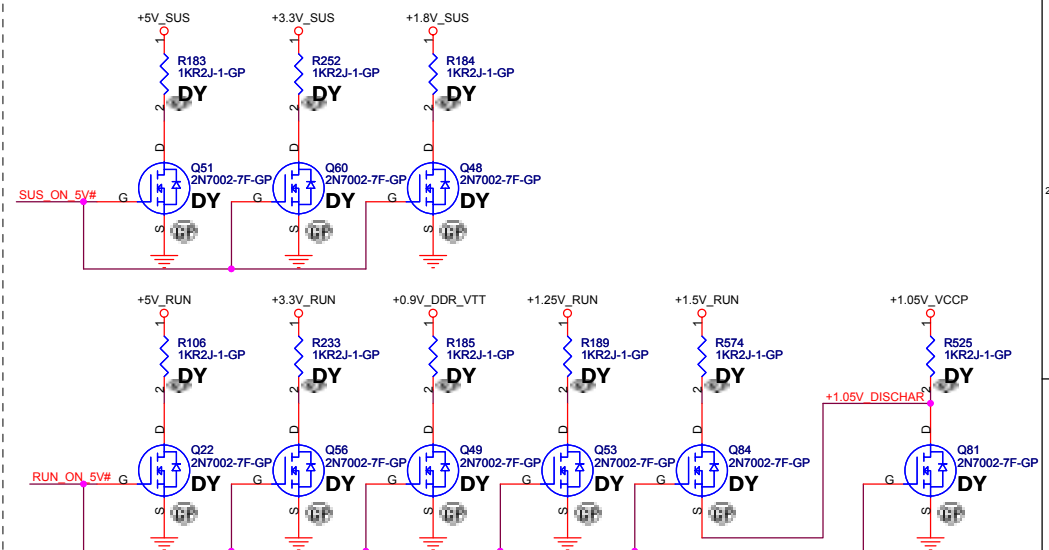
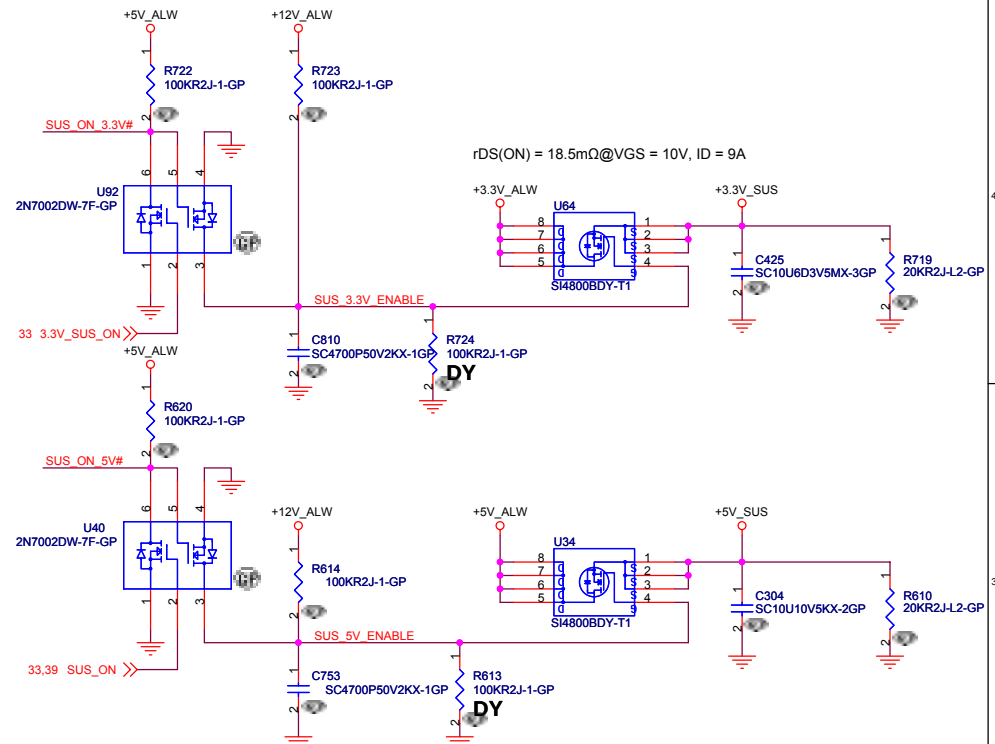
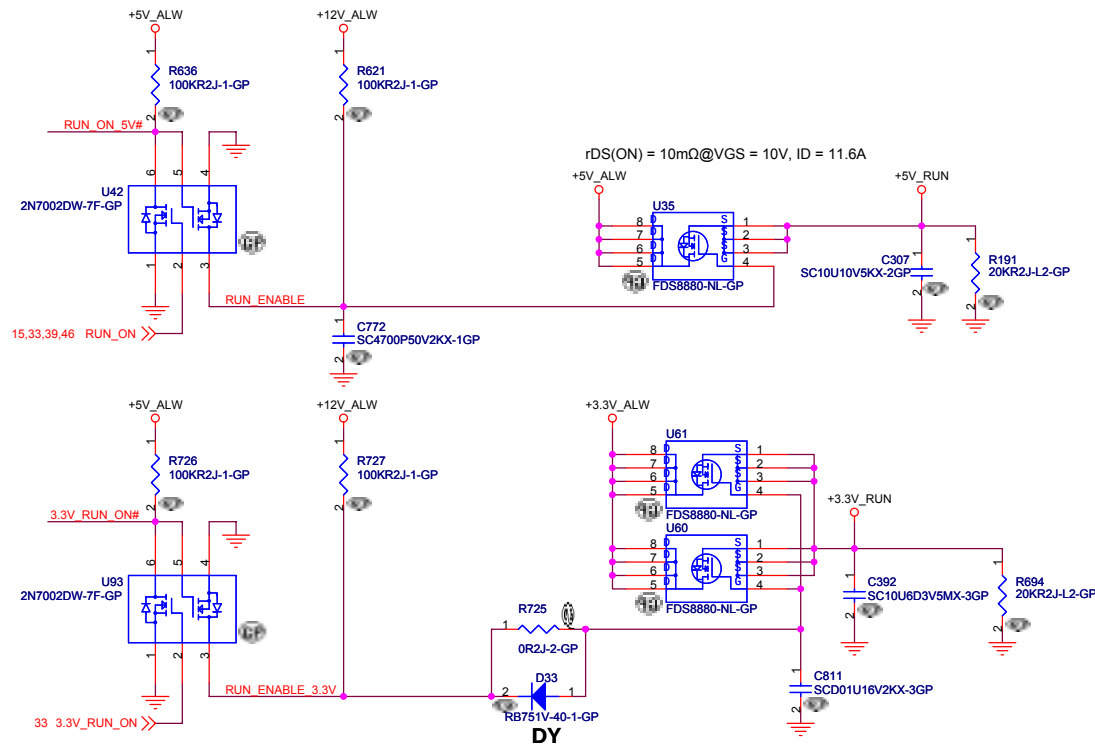
LEFT PANEL LED

The circuit for the LEFT PANEL LED is powered by a +5V_RUN input. The current flows through a 10KR2J-3-GP resistor (R501) to the LEDQ10 LED. The LED is connected to the drain of MOSFET Q19 (2N7002-7F-GP). The gate of Q19 is connected to the LEDQ10 signal line. The source of Q19 is connected to ground. The drain of Q19 is also connected to the L_PANEL_W# input, which is pulled up to +5V_RUN by a 0R5J-5-GP resistor (R491). The output of the LED is connected to the L_PANEL_LED output.

RIGHT PANEL LED

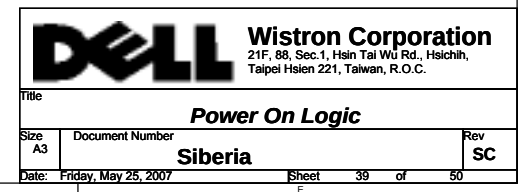
The circuit for the RIGHT PANEL LED is powered by a +5V_RUN input. The current flows through a 10KR2J-3-GP resistor (R504) to the LEDQ9 LED. The LED is connected to the drain of MOSFET Q23 (2N7002-7F-GP). The gate of Q23 is connected to the LEDQ9 signal line. The source of Q23 is connected to ground. The drain of Q23 is also connected to the R_PANEL_W# input, which is pulled up to +5V_RUN by a 0R5J-5-GP resistor (R490). The output of the LED is connected to the R_PANEL_LED output.

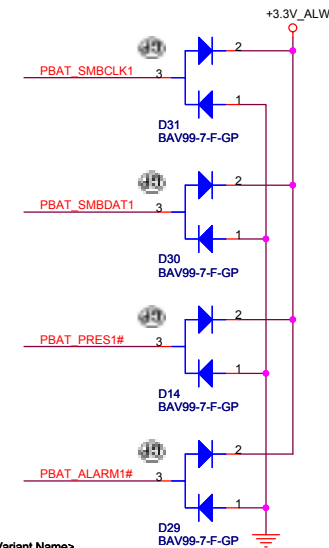
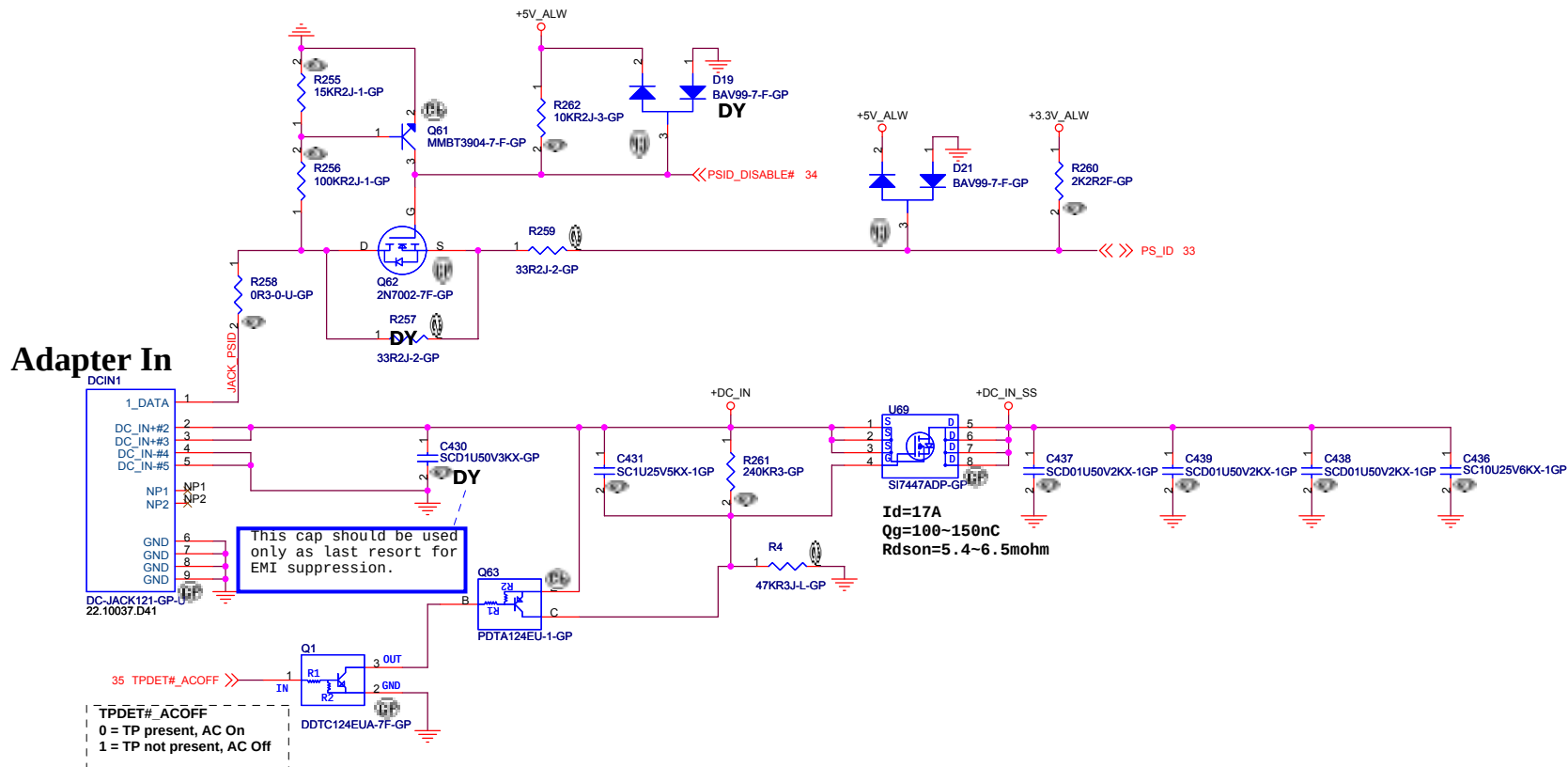


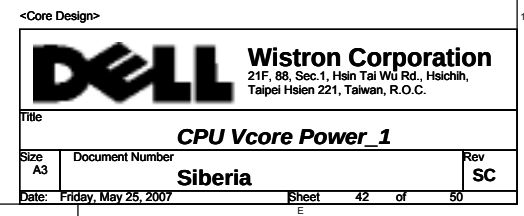


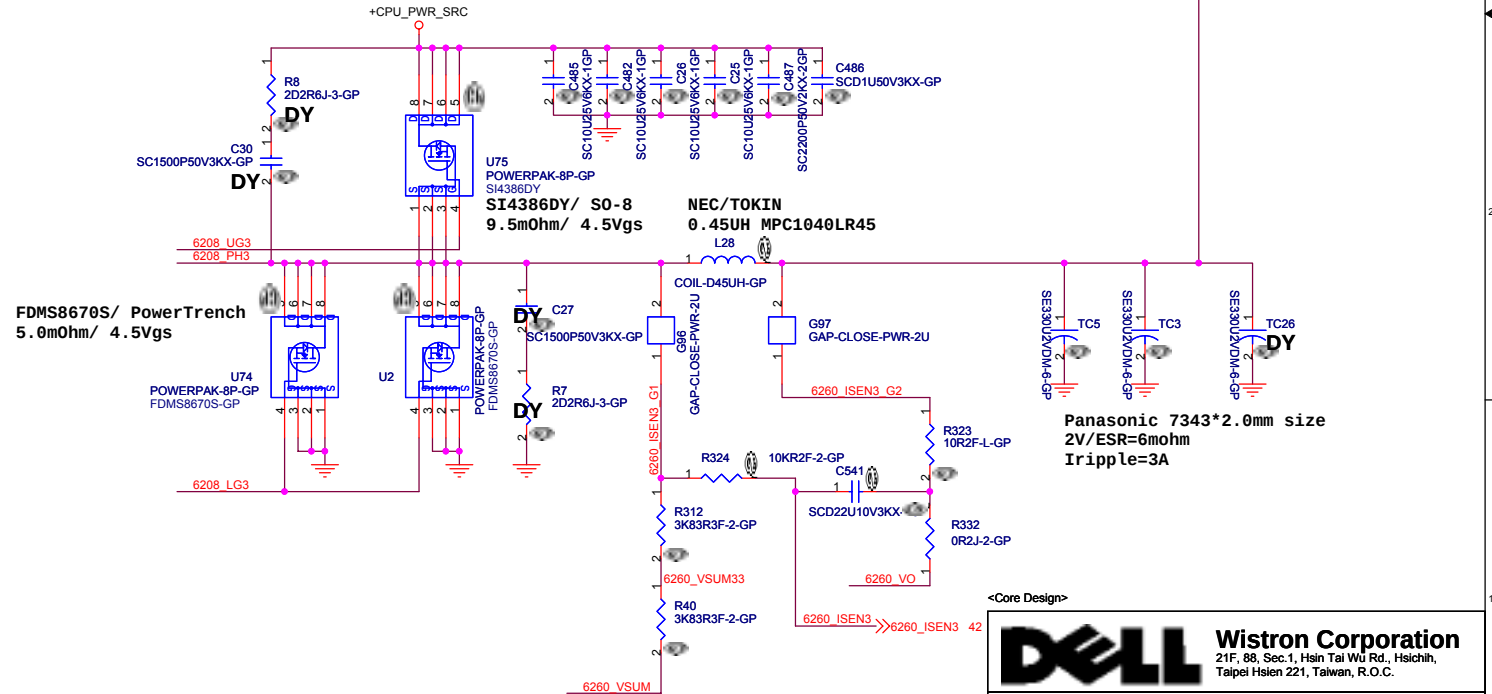
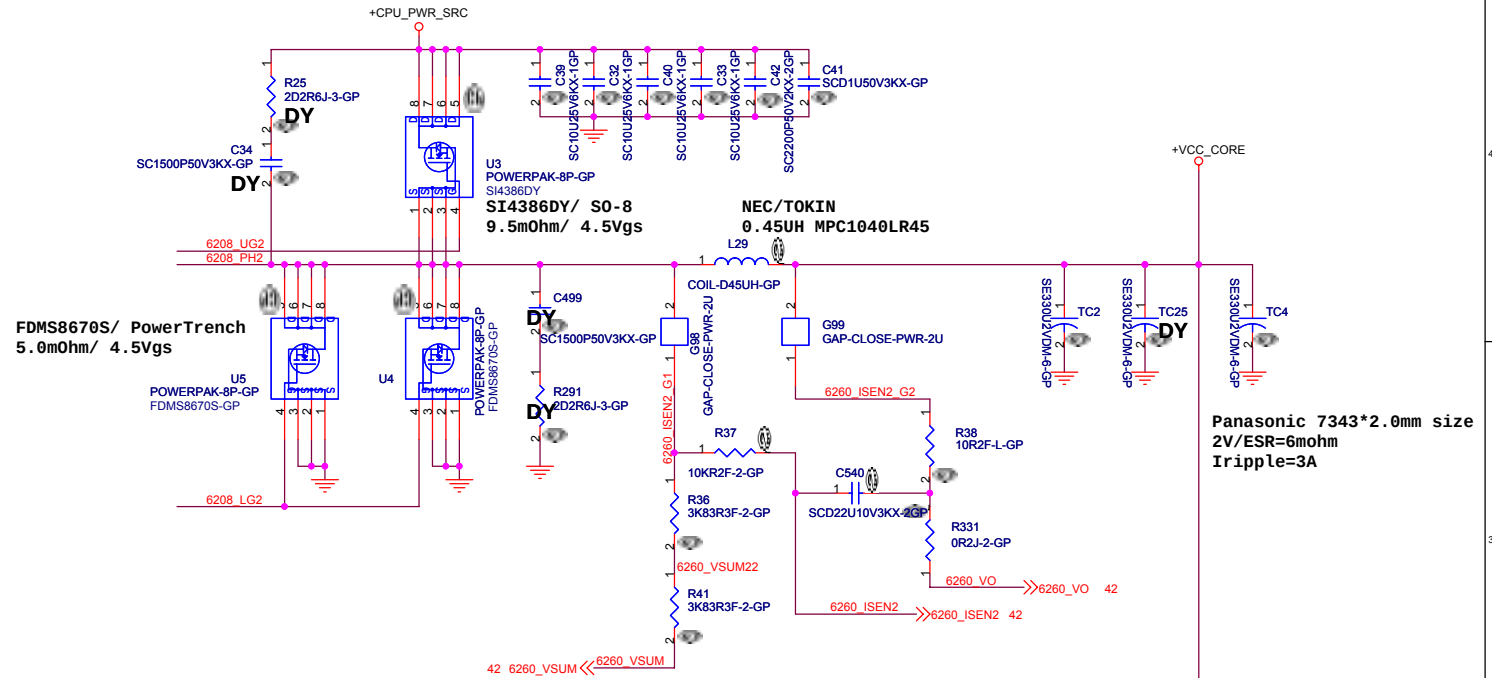
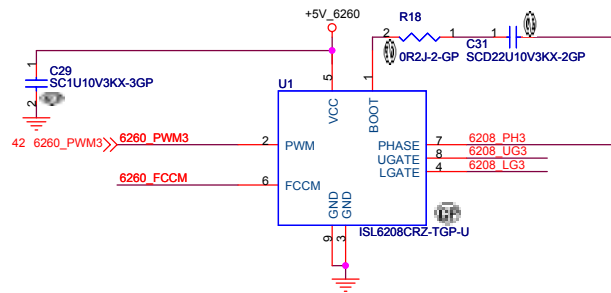
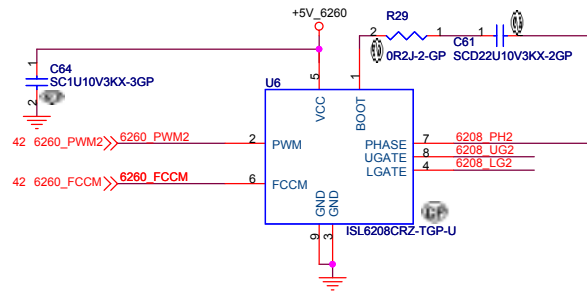
Reserve discharge path

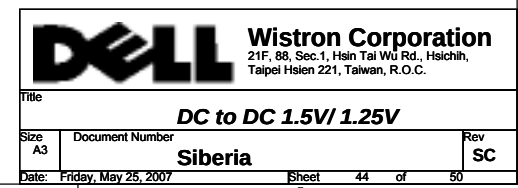
CRB 0.95:
 Insures that +1.05_VCCP and +1.5_RUN ramp
 down together by discharging +1.5V_RUN into
 +1.05V_VCCP

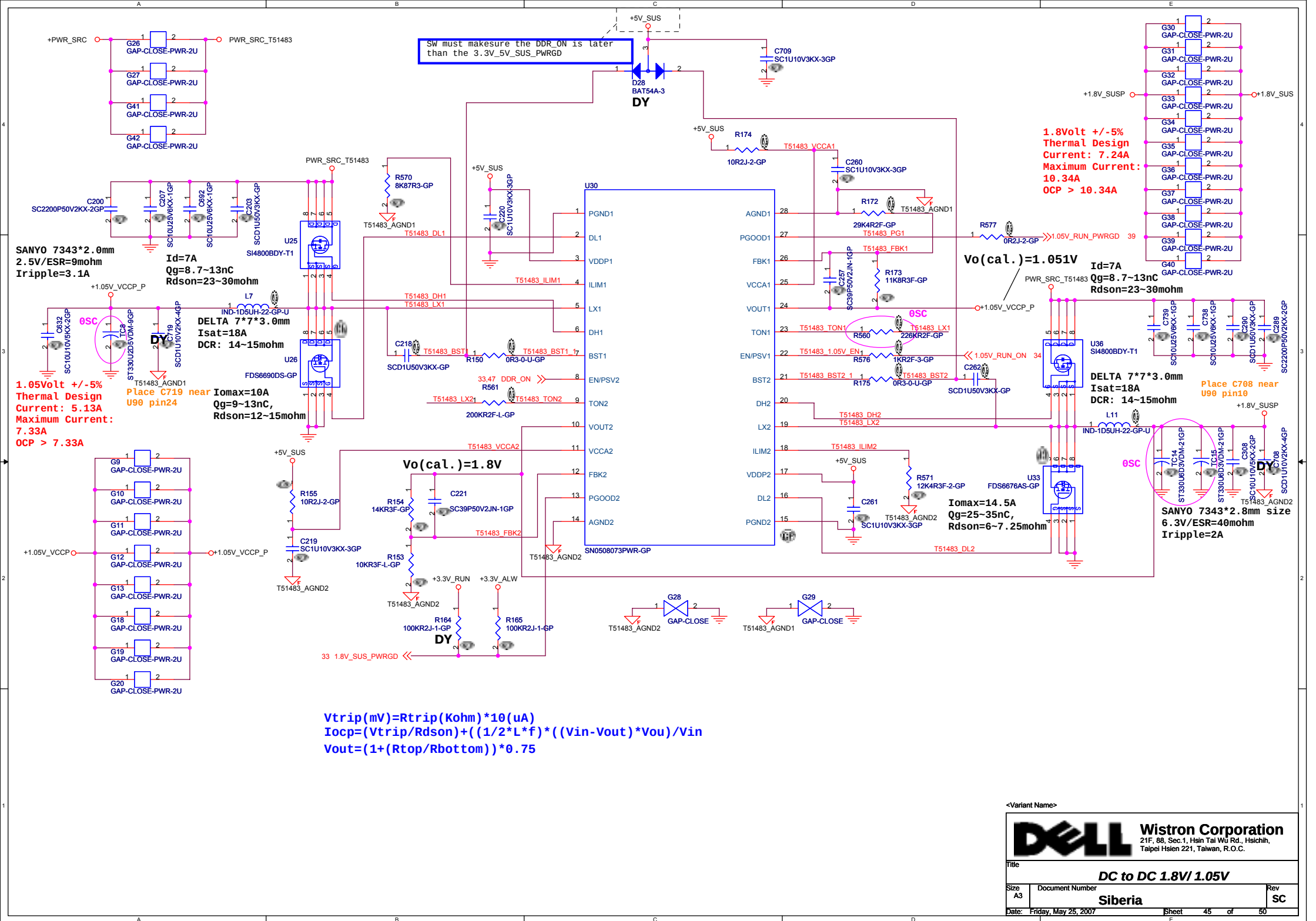


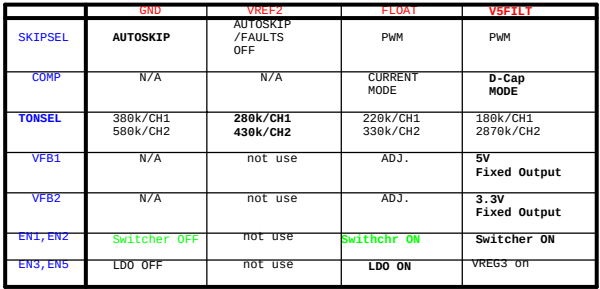




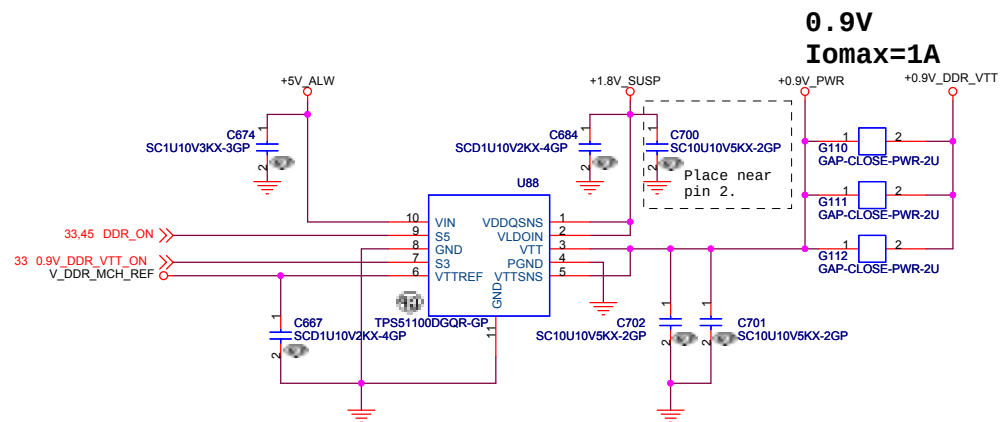
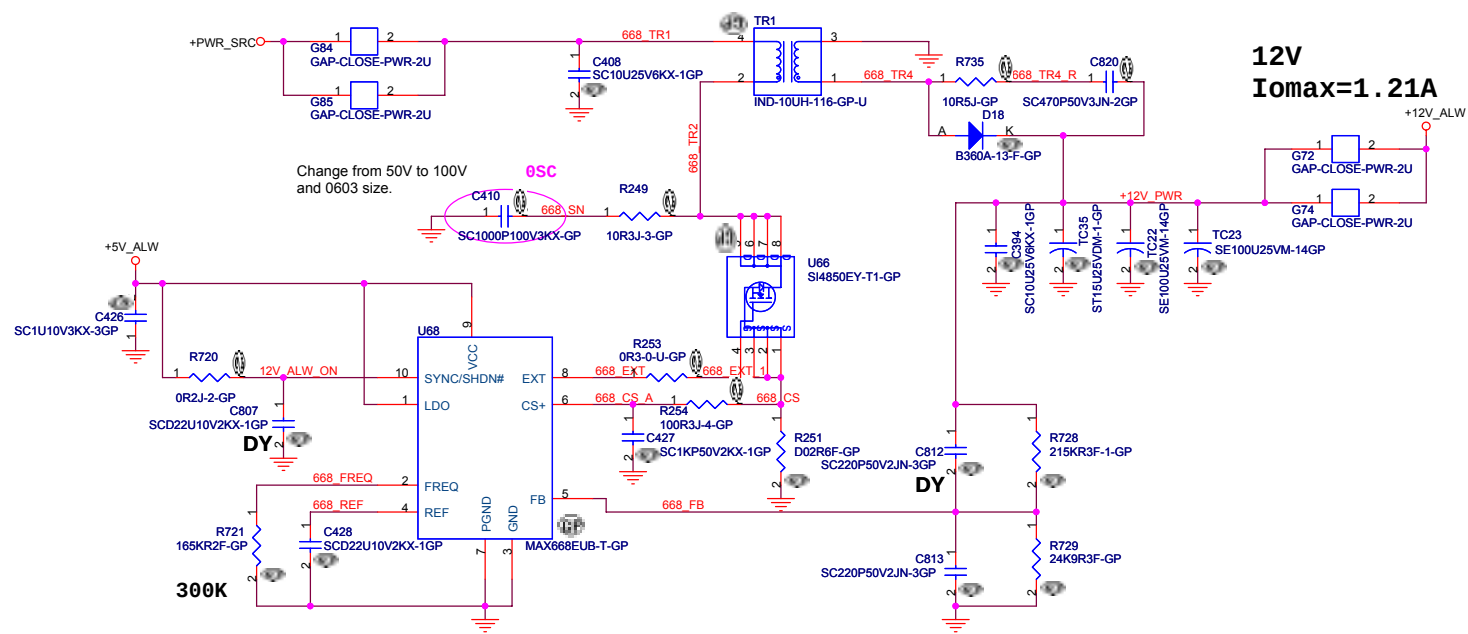








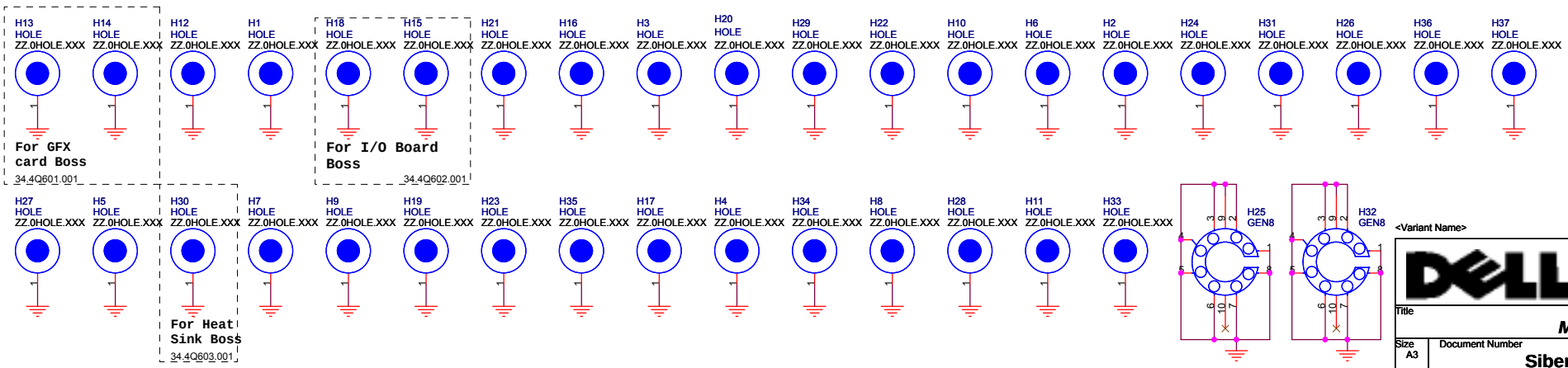
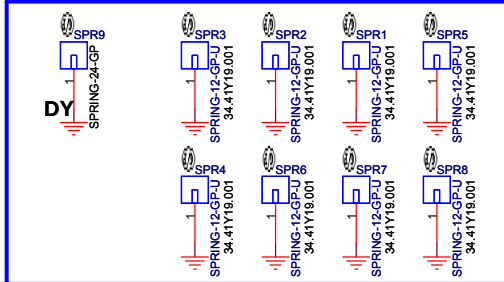
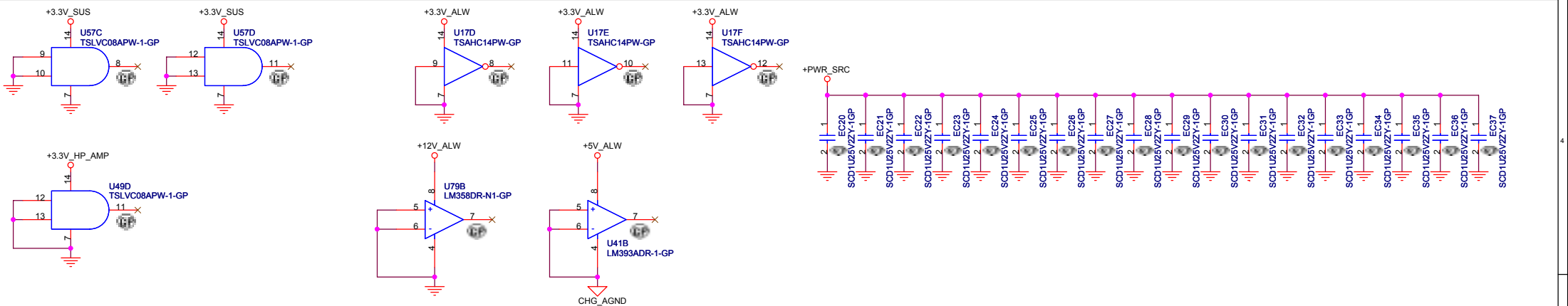
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<Core Design>



Title			DC to DC 12V / 0.9V	
Size	Document Number	Siberia		Rev
A3				SC
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<Variant Name>

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Title _____

Size A3 Document Number **Siberia** Rev **SC**

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ICH8 SMBus Block Diagram

ICH8-M
SMBCLK
SMBDATA

DIMM 1
SCL (Reverse Type)
SDA
SMBus Address : A0

DIMM 2
SCL (Reverse Type)
SDA
SMBus Address : A4

BCM5754M
SMB_CLK
SMB_DATA
SMBus Address : C8(Pebble)

Express Card
SMB_CLK
SMB_DATA

WWAN Minicard
SMB_CLK
SMB_DATA

3rd Minicard
SMB_CLK
SMB_DATA

WLAN Minicard
SMB_CLK
SMB_DATA

ICH8 SMBus Block Diagram

ICH8-M
SMBCLK
SMBDATA

DIMM 1
SCL (Reverse Type)
SDA
SMBus Address : A0

DIMM 2
SCL (Reverse Type)
SDA
SMBus Address : A4

BCM5754M
SMB_CLK
SMB_DATA
SMBus Address : C8(Pebble)

Express Card
SMB_CLK
SMB_DATA

WWAN Minicard
SMB_CLK
SMB_DATA

3rd Minicard
SMB_CLK
SMB_DATA

WLAN Minicard
SMB_CLK
SMB_DATA

SIO MEC5025
KS017/GPIOA1/AB1H_DATA
KS016/GPIOA0/AB1H_CLK

CLK GEN.
SDATA
SCLK
SMBus address:D2

LED dimmer
SDA
SCL
SMBus address:C0

Battery Conn.
CLK_SMB
DAT_SMB
SMBus address:16

Charger
SCL
SDA
SMBus address:12

Thermal
SMBCLK
SMBDATA
SMBus address:5E

GFX Conn. (Inverter)
SMBus address:58

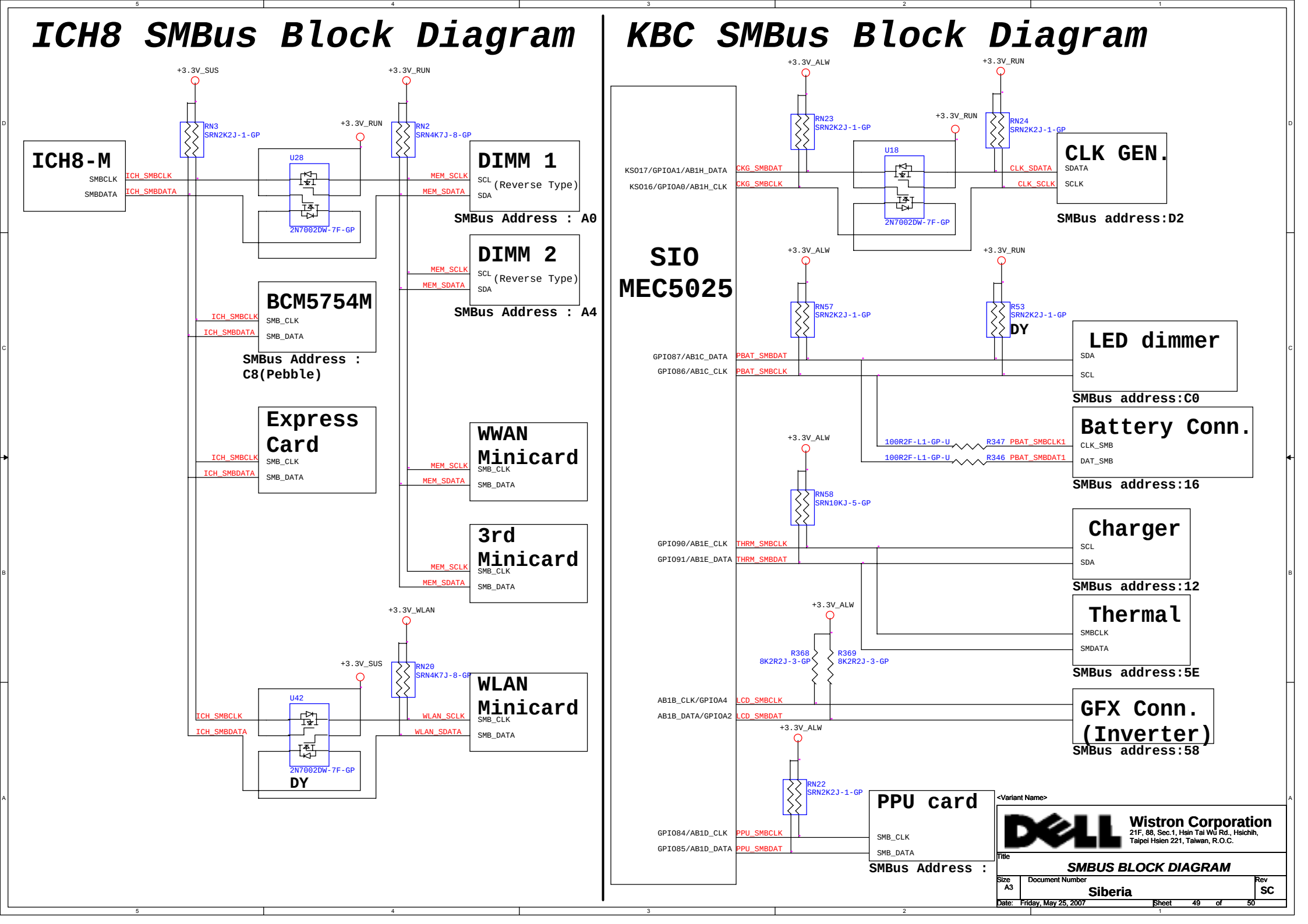
PPU card
SMB_CLK
SMB_DATA
SMBus Address :

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SMBUS BLOCK DIAGRAM

Size A3
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Rev SC



This diagram illustrates the SMBus Block Diagram for the ICH8 and KBC components, showing the connections between various hardware modules and the SMBus controller.

ICH8 SMBus Block Diagram

The ICH8-M controller is connected to the following modules:

- DIMM 1** (SCL (Reverse Type), SDA): SMBus Address : A0
- DIMM 2** (SCL (Reverse Type), SDA): SMBus Address : A4
- BCM5754M** (SMB_CLK, SMB_DATA): SMBus Address : C8 (Pebble)
- Express Card** (SMB_CLK, SMB_DATA): SMBus Address : C8 (Pebble)
- WWAN Minicard** (SMB_CLK, SMB_DATA): SMBus Address : C8 (Pebble)
- 3rd Minicard** (SMB_CLK, SMB_DATA): SMBus Address : C8 (Pebble)
- WLAN Minicard** (SMB_CLK, SMB_DATA): SMBus Address : C8 (Pebble)

KBC SMBus Block Diagram

The KBC (SIO MEC5025) is connected to the following modules:

- CLK GEN.** (SDATA, SCLK): SMBus address:D2
- LED dimmer** (SDA, SCL): SMBus address:C0
- Battery Conn.** (CLK_SMB, DAT_SMB): SMBus address:16
- Charger** (SCL, SDA): SMBus address:12
- Thermal** (SMBCLK, SMDATA): SMBus address:5E
- GFX Conn. (Inverter)** (SMB_CLK, SMB_DATA): SMBus address:58
- PPU card** (SMB_CLK, SMB_DATA): SMBus Address :

The diagram also shows the connections for the ICH8-M and KBC components, including the SMBus controller, various power supplies, and the system clock generator.

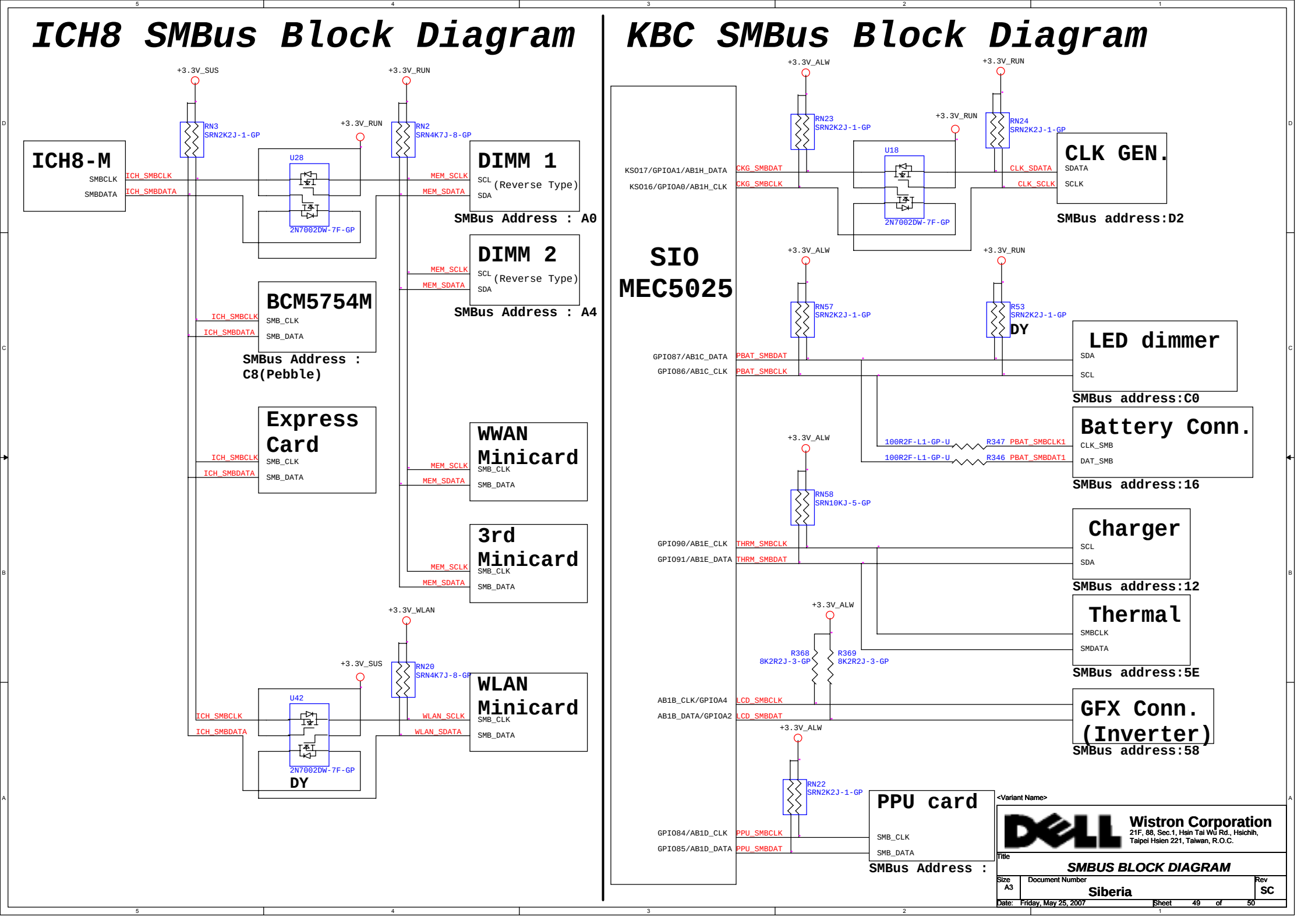
Legend:

- ICH8-M: SMBCLK, SMBDATA
- KBC: SMBCLK, SMBDATA
- ICH8-M: SMBCLK, SMBDATA
- KBC: SMBCLK, SMBDATA

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SMBUS BLOCK DIAGRAM

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DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/05/15	X01 to X02	1	41	Change C318 to 0.01U and change R202 to 17.8K and change R194 to 2.87K.	By power team suggestion.	Power
		2	44,45	Change TC14, TC15, TC19, TC34 to 330U.	By power team suggestion.	Power
		3	47	Change C410 to 1000P 100V 0603 size.	Change to 100V because derating is fail.	Power
		4	6,10,19	Add TP123~TP134.	For NCTF.	EE
		5	31	Change ESD1.	Vendor from Semtech to Philips inside DELL PSL.	EE
2007/05/21		6	15	Add 10K ohm resistor to GND at U81 pin1.	Dell's command for SPDIF.	EE
		7	25	Populate R712 and R708, non-populate R711 and R707.	Dell's command for AUDIO noise.	EE
		8	45	Change TC8 to 77.23371.13L.	By power team suggestion.	Power
		9	46	Change L15 to 68.4R71B.10K.	By power team suggestion.	Power
2007/05/22		10	45	Change R560 from 150K ohm to 226K ohm.	Slow down +1.05V_RUN frequency from 600KHz to 400KHz.	Power
		11	46	Non-populate R716.	Slow down +3.3V_ALW frequency from 580KHz to 330KHz, +5V_ALW frequency from 380KHz to 220KHz	Power
2007/05/23		12	25	Change C400, C413 from 0.033U to 0.047U 1206size.	Increase value of capacitor to promote audio performance.	EE
		13	27	Change R274 from 39K ohm to 0 ohm.	Change LOM supper IDDQ setting.	EE
		14	34	Non-populate R407 and R387, populate R388 and R406.	Change board ID from X01 to X02.	EE

<Core Design>



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Title			HISTORY from X00 to X01		
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