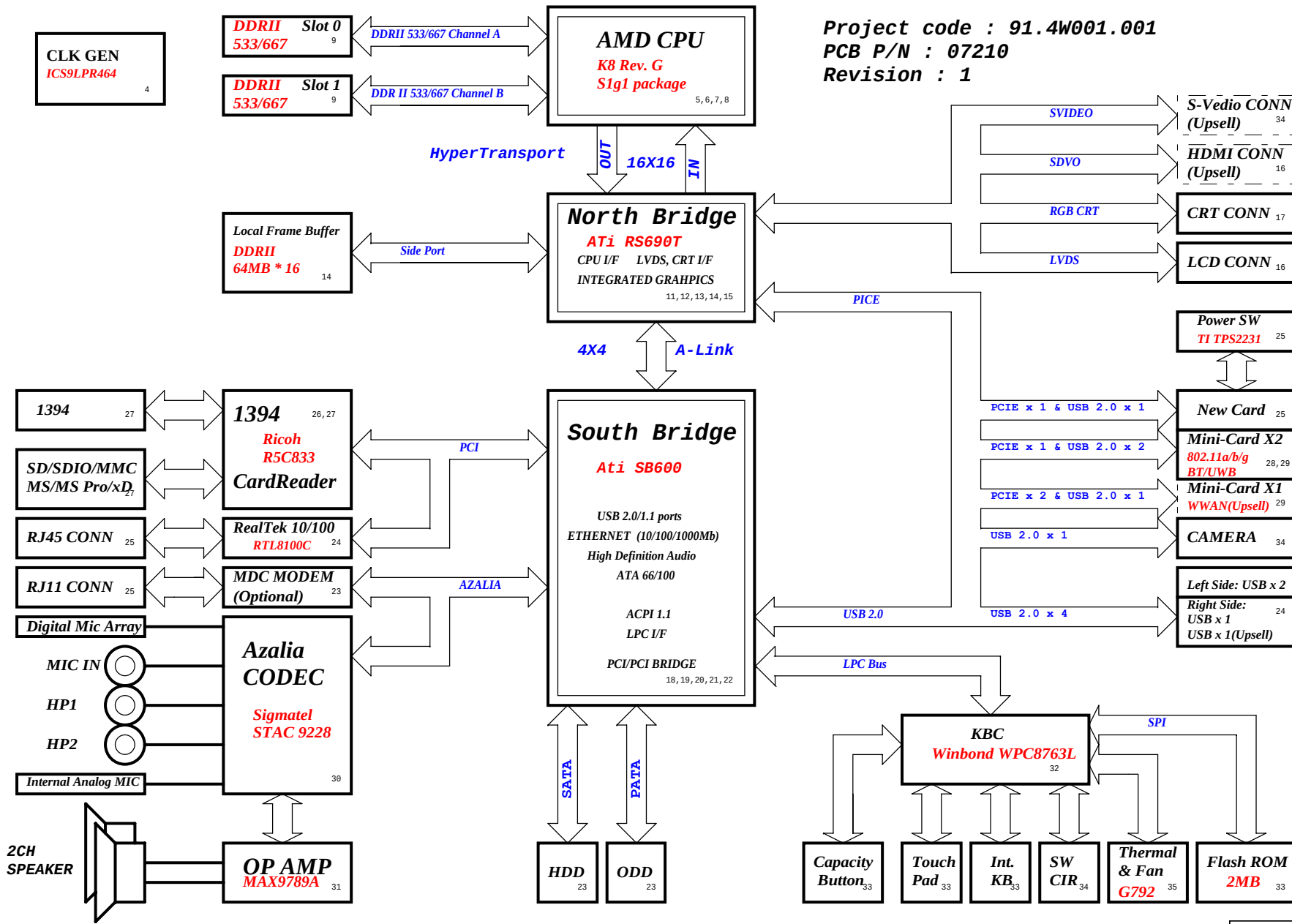


Spears AMD UMA Block Diagram



Project code : 91.4W001.001
PCB P/N : 07210
Revision : 1

CPU V_CORE	
ISL6264	39
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC	
TPS51117	40, 41
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3
	1D2V_S0

SYSTEM DC/DC	
TPS51120	38
INPUTS	OUTPUTS
DCBATOUT	5V_S5
	3D3V_S5

SYSTEM DC/DC	
LDO	42
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3
1D8V_S0	1D5V_S0

SYSTEM DC/DC	
LDO	42
INPUTS	OUTPUTS
3D3V_S5	1D2V_S5
3D3V_S0	2D5V_S0

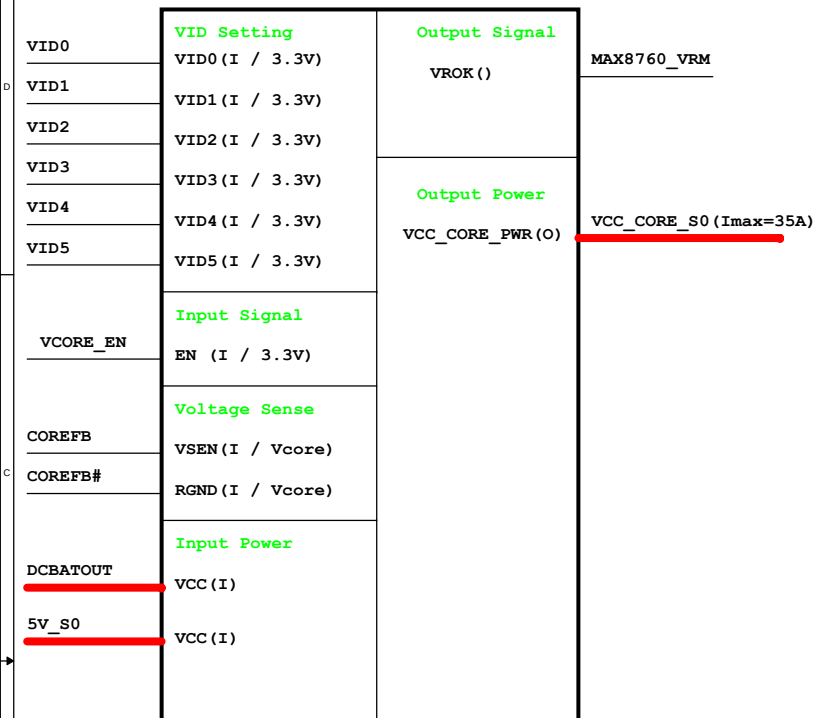
SYSTEM DC/DC	
TPS51120	38
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5
	3D3V_AUX_S5

MAXIM CHARGER	
MAX8731A	37
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

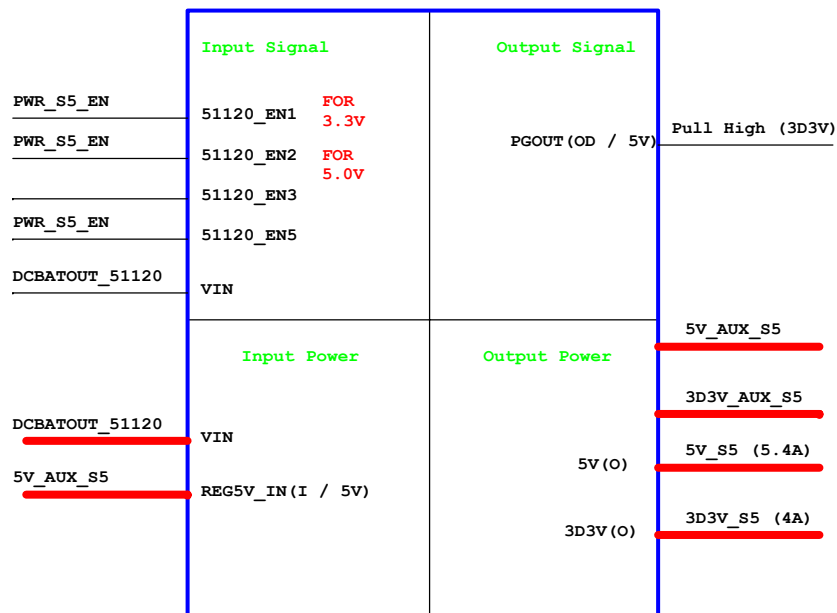
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

System Block Diagram		
Size	Document Number	Rev
A3	DS2-AMD	1
Date:	Monday, September 24, 2007	Sheet 1 of 44

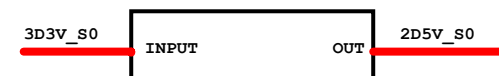
CPU_CORE
ISL6264CRZ



3D3V/5V
TI TPS51120

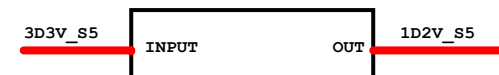


2D5V_S0



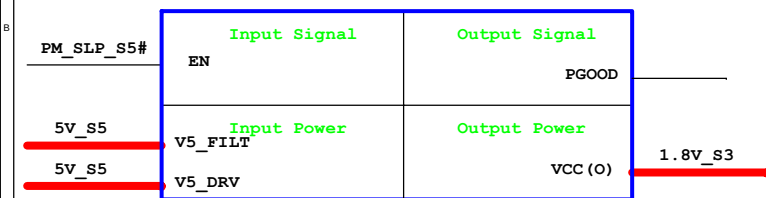
APL5913

1D8V_S5

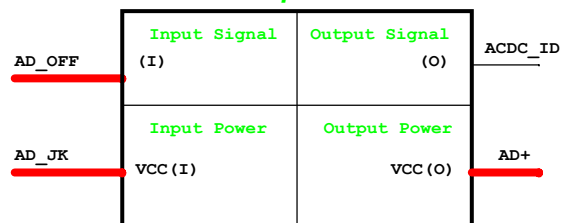


APL5332KAC-TRLGP

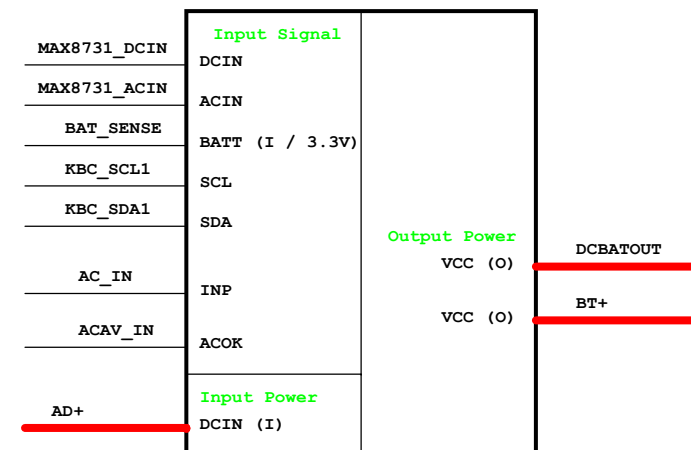
TI TPS51117
1.8V



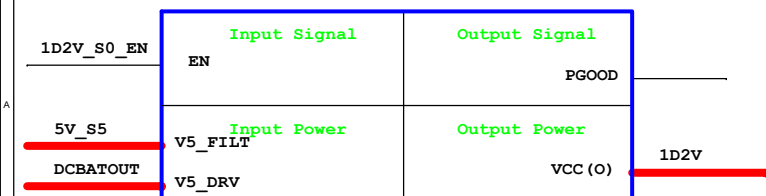
Adapter



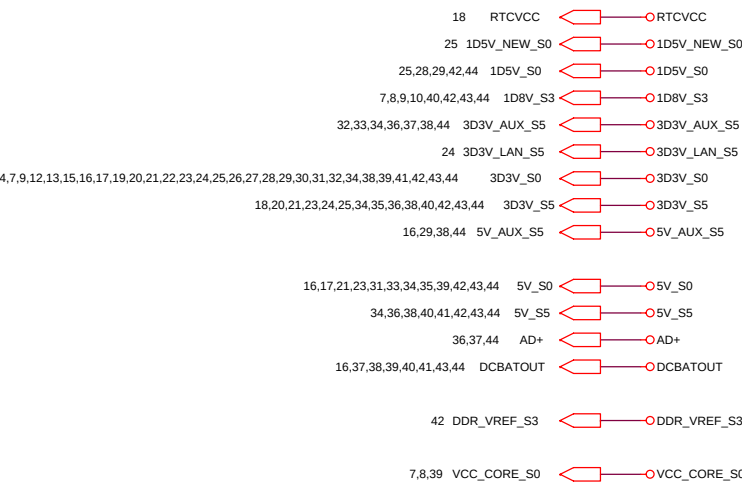
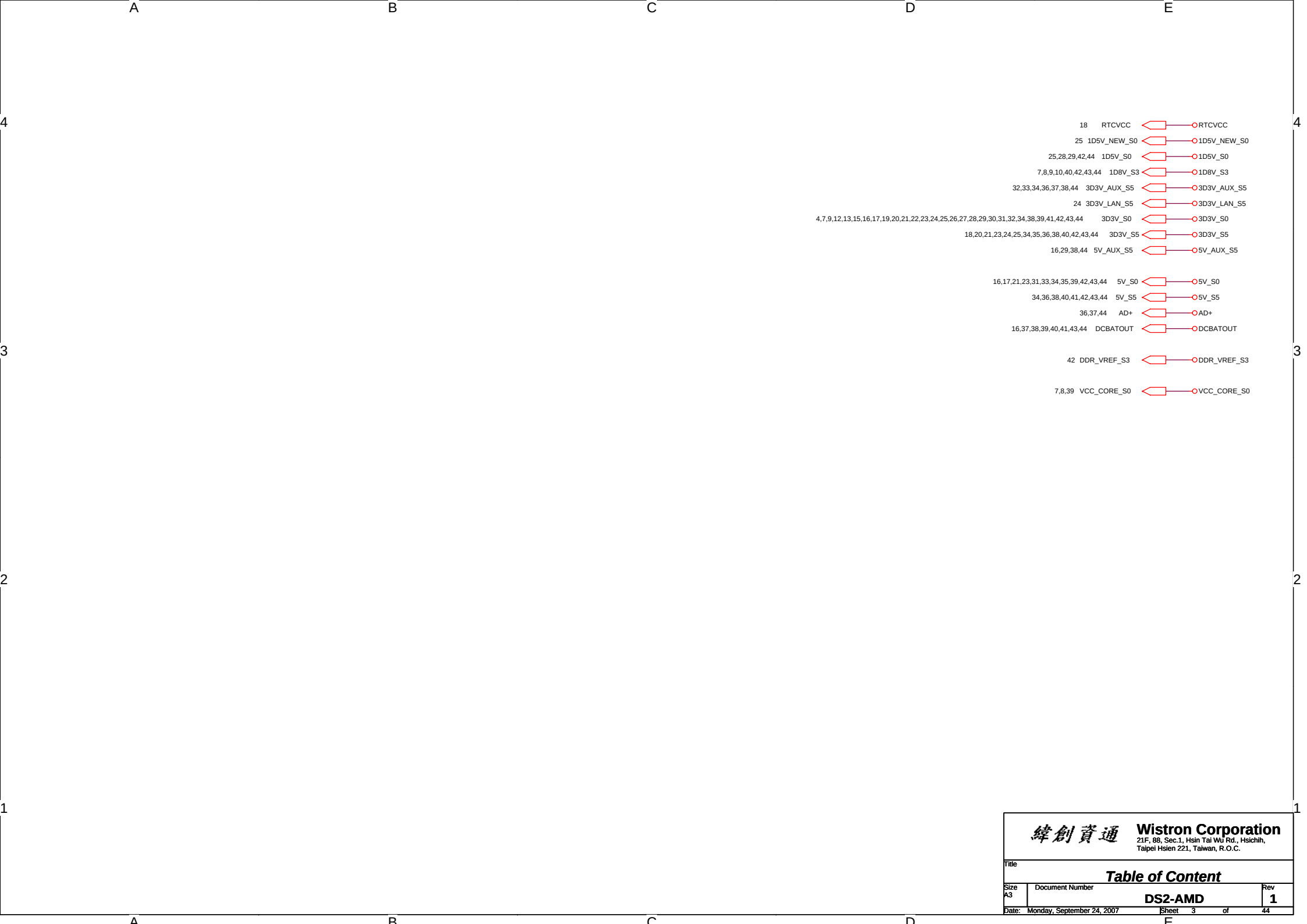
Charger_MAX8731AETI

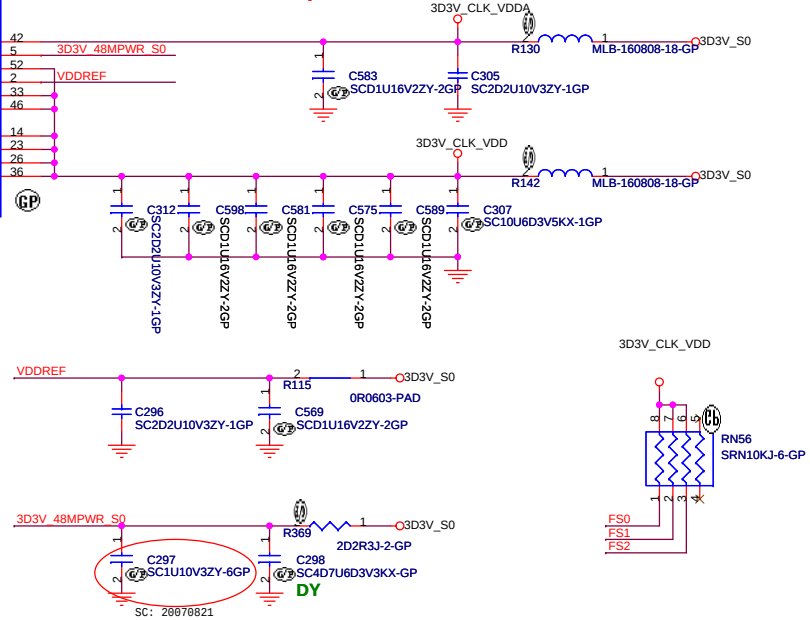


TI TPS51117
1.2V

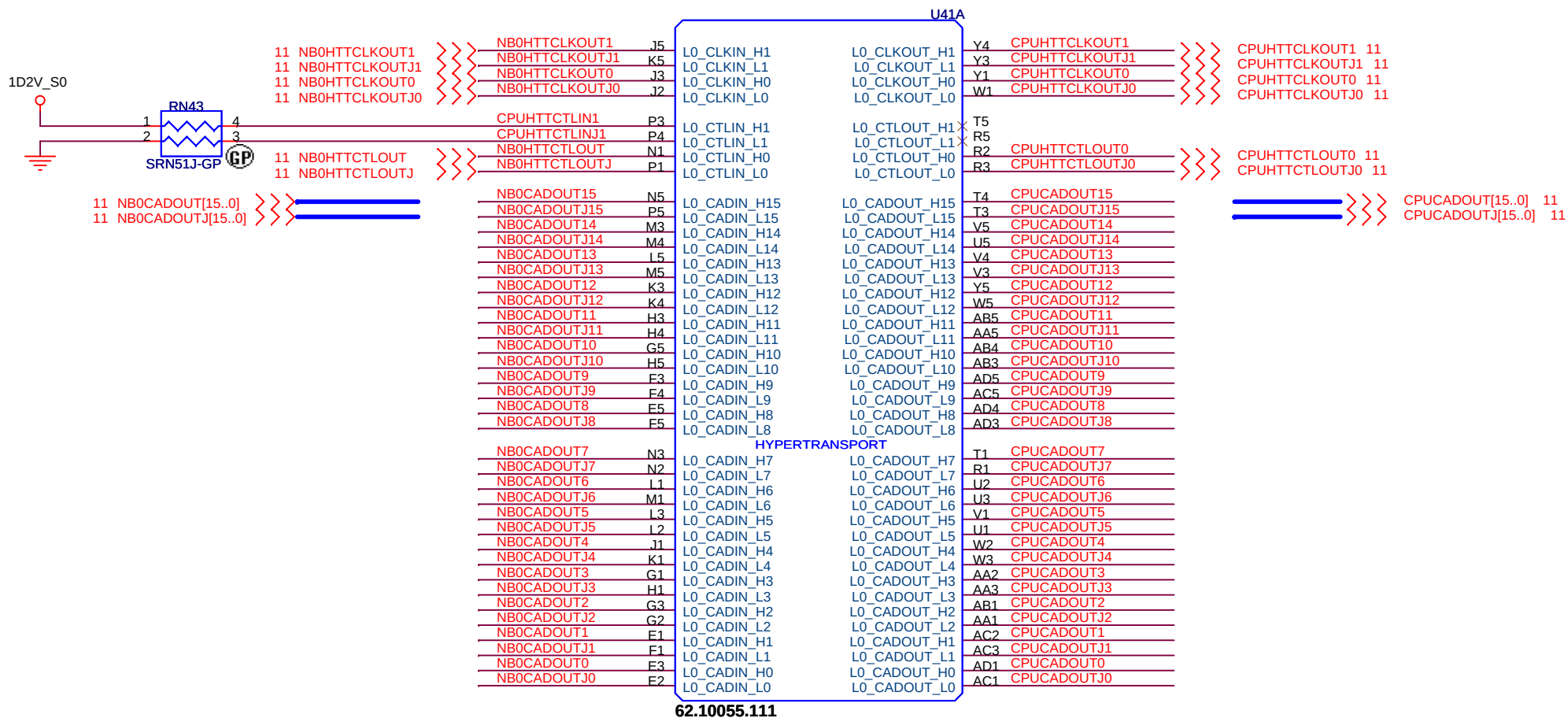


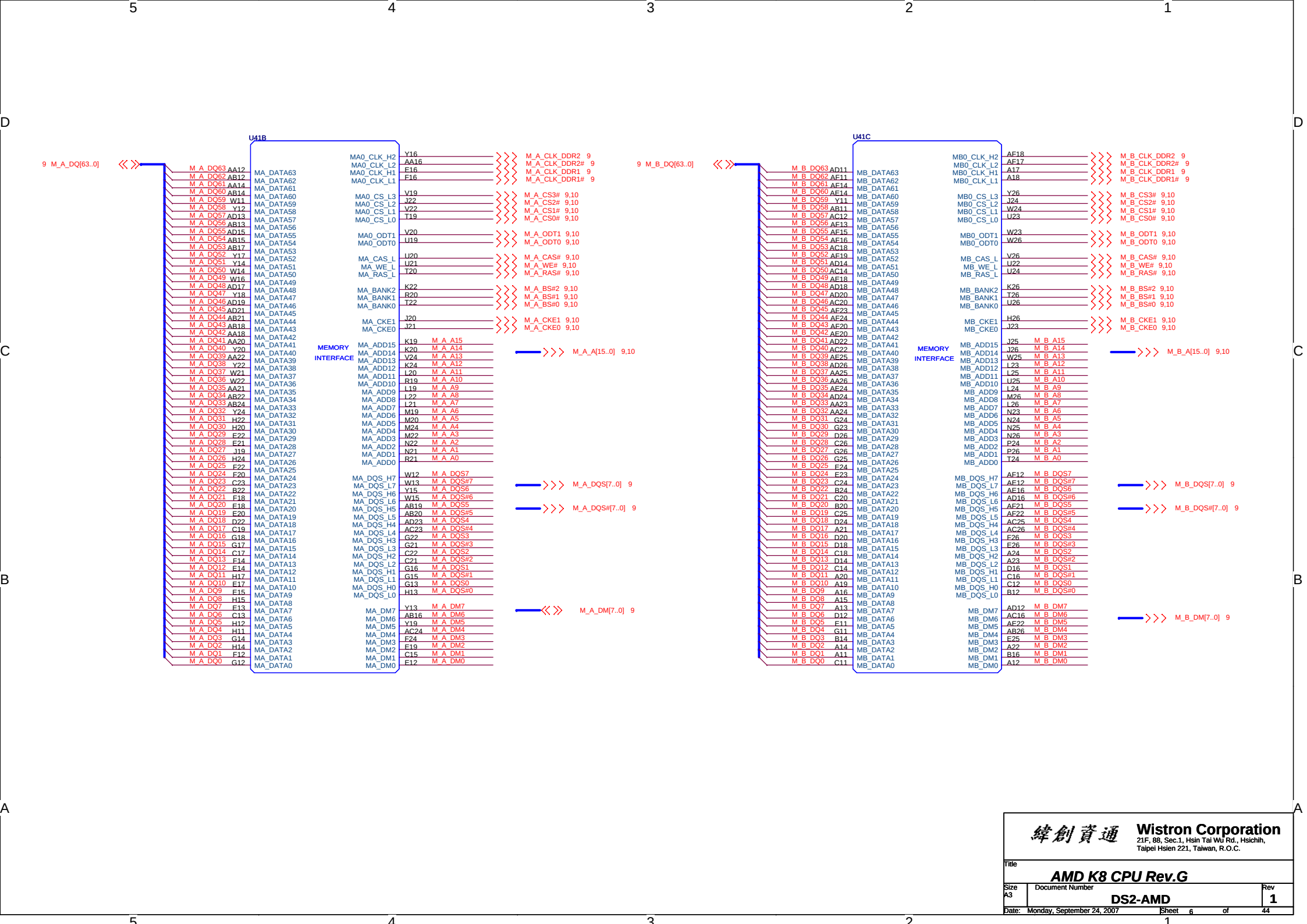
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Taipei Hsien 221, Taiwan, R.O.C.

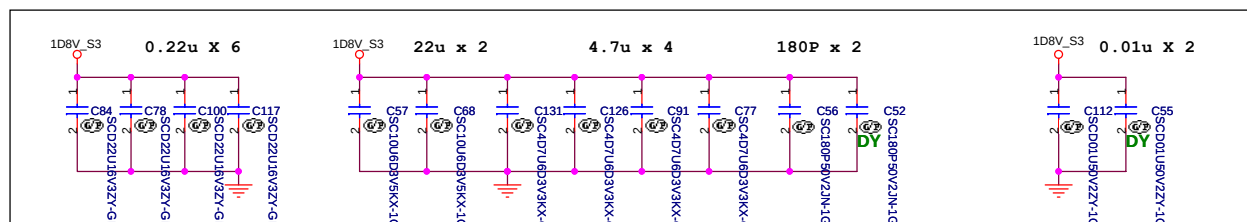
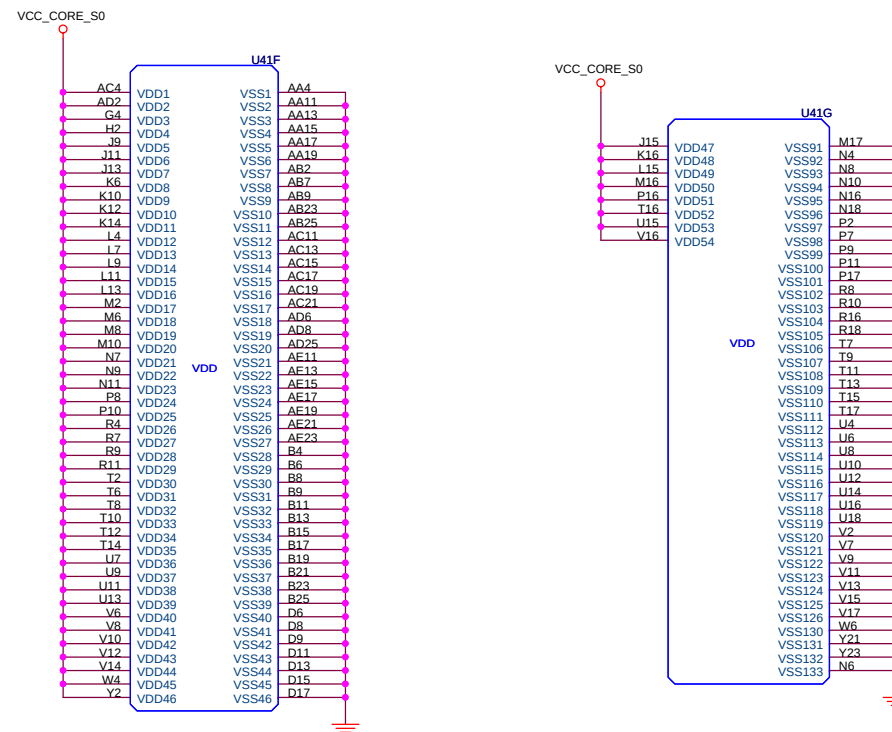
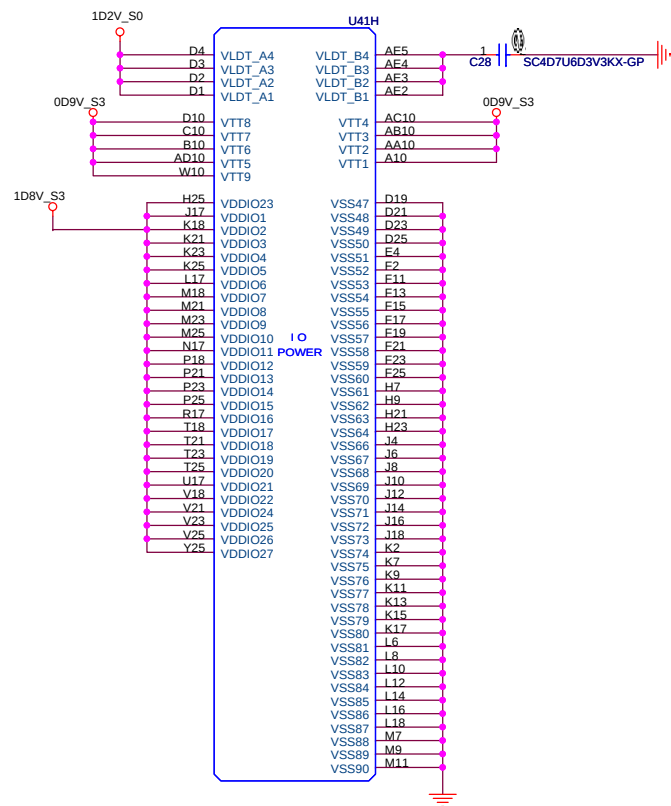




FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	USB	REF0 REF1 REF2
0	0	0	Hi-Z	100.00	Hi-Z	48.00	14.318
0	0	1	X/2	100.00	X/3	48.00	14.318
0	1	0	230.00	100.00	76.67	48.00	14.318
0	1	1	240.00	100.00	80.00	48.00	14.318
1	0	0	100.00	100.00	66.66	48.00	14.318
1	0	1	133.33	100.00	66.66	48.00	14.318
1	1	0	166.67	100.00	66.66	48.00	14.318
1	1	1	200.00	100.00	66.67	48.00	14.318

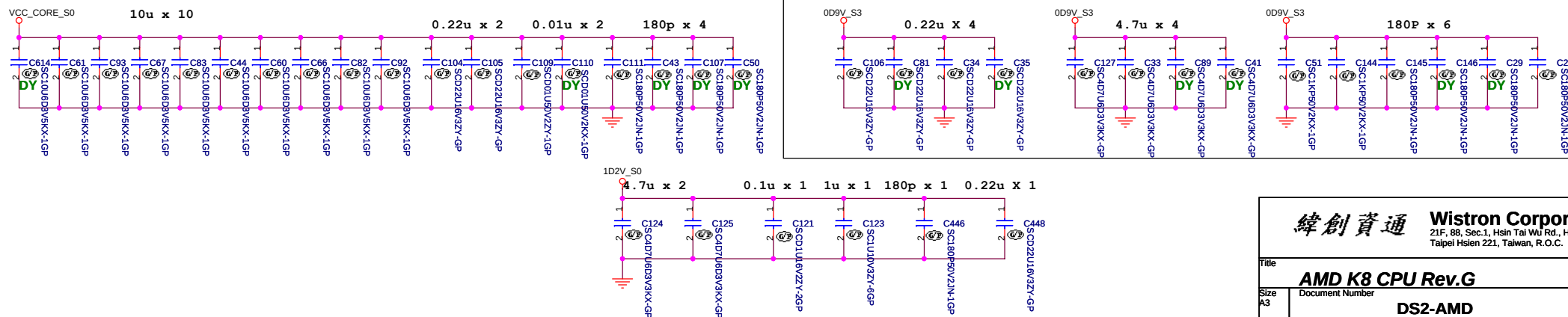


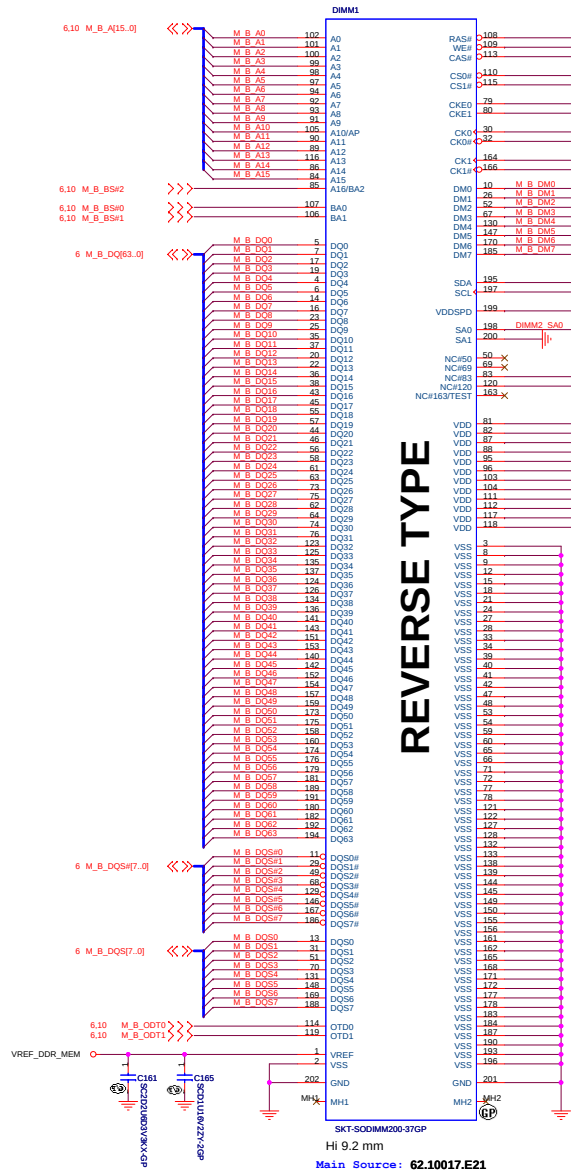




Place near to CPU

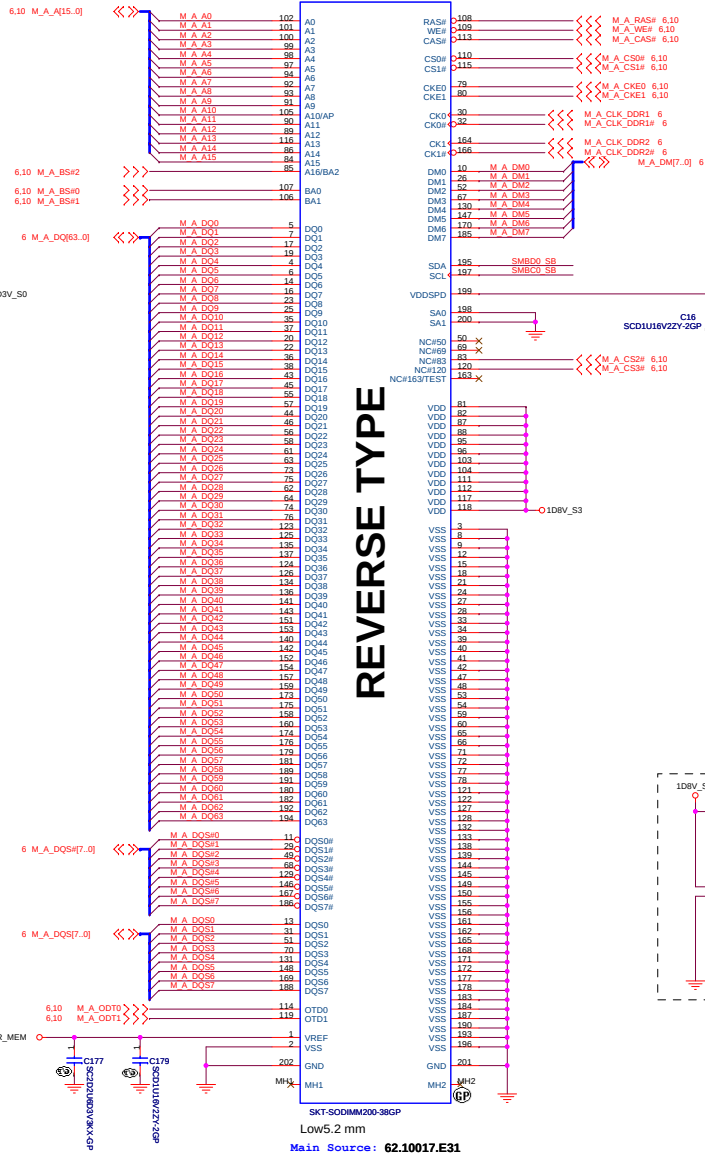
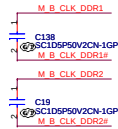
LAYOUT: Place on backside of processor.





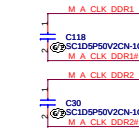
REVERSE TYPE

Place near CPU

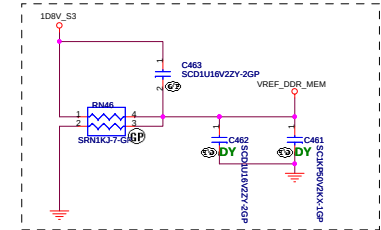


REVERSE TYPE

Place near CPU

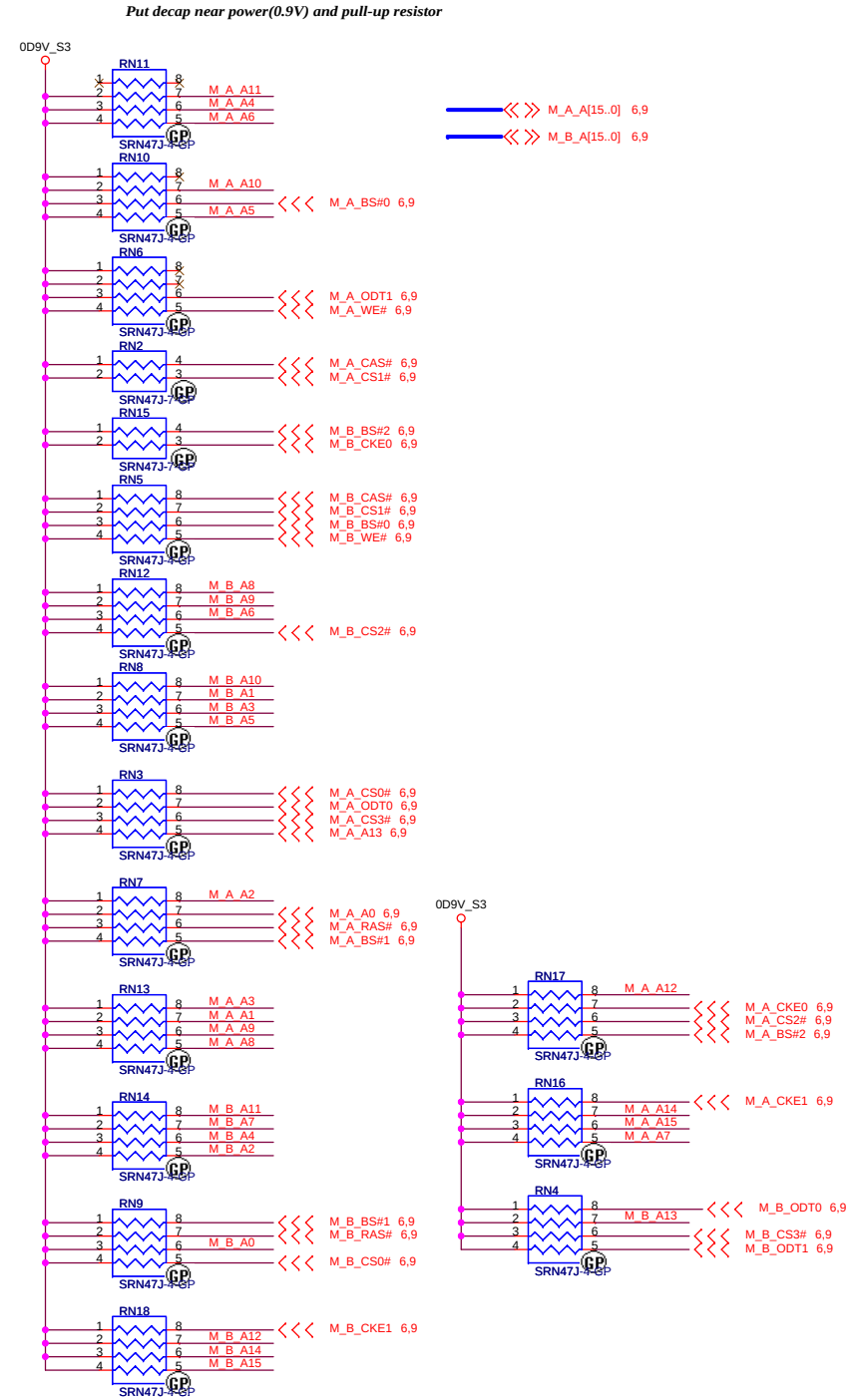


DDR_VREF

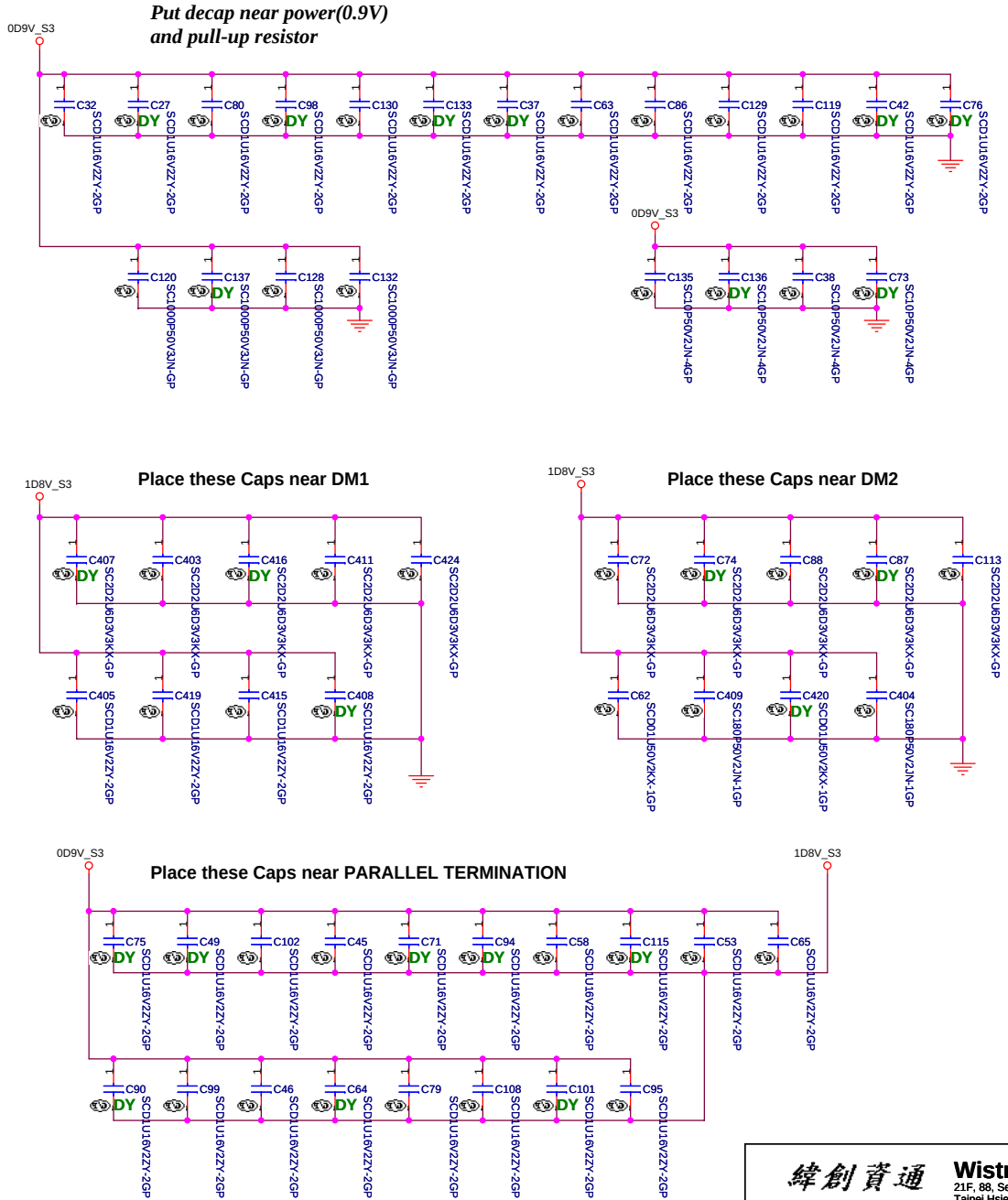


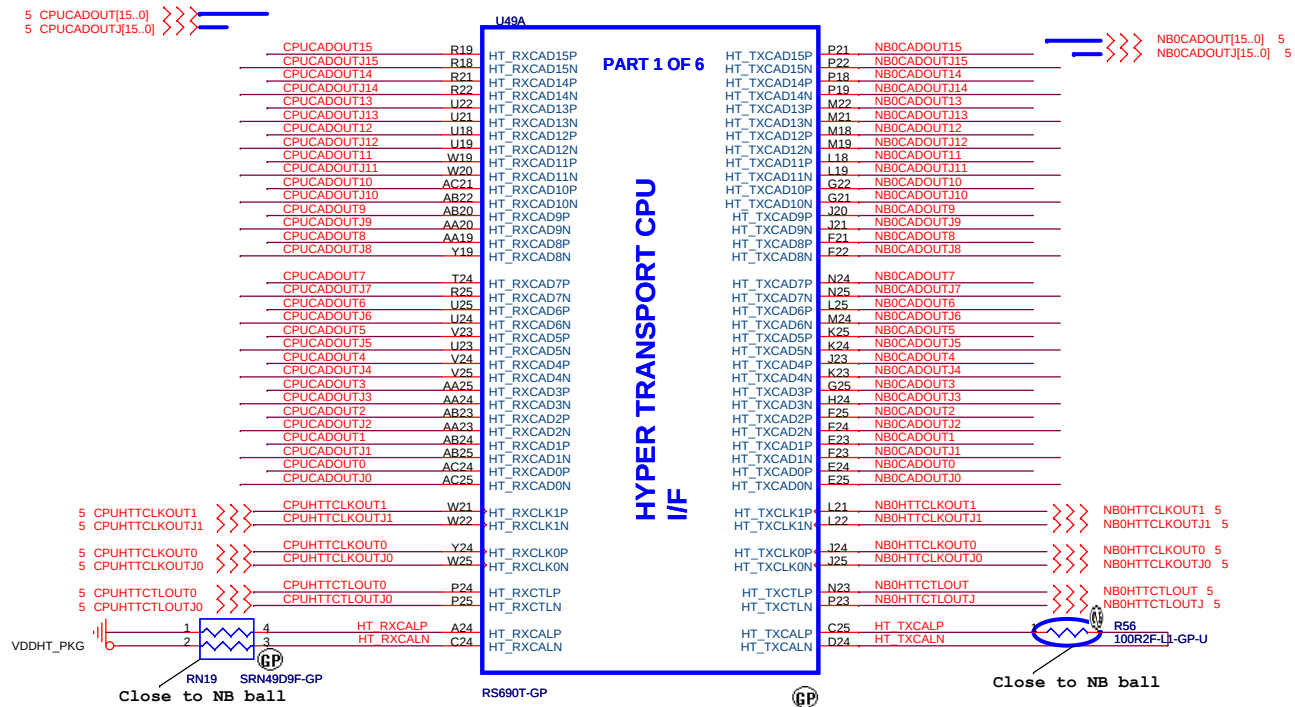
LAYOUT: Locate close to DIMM

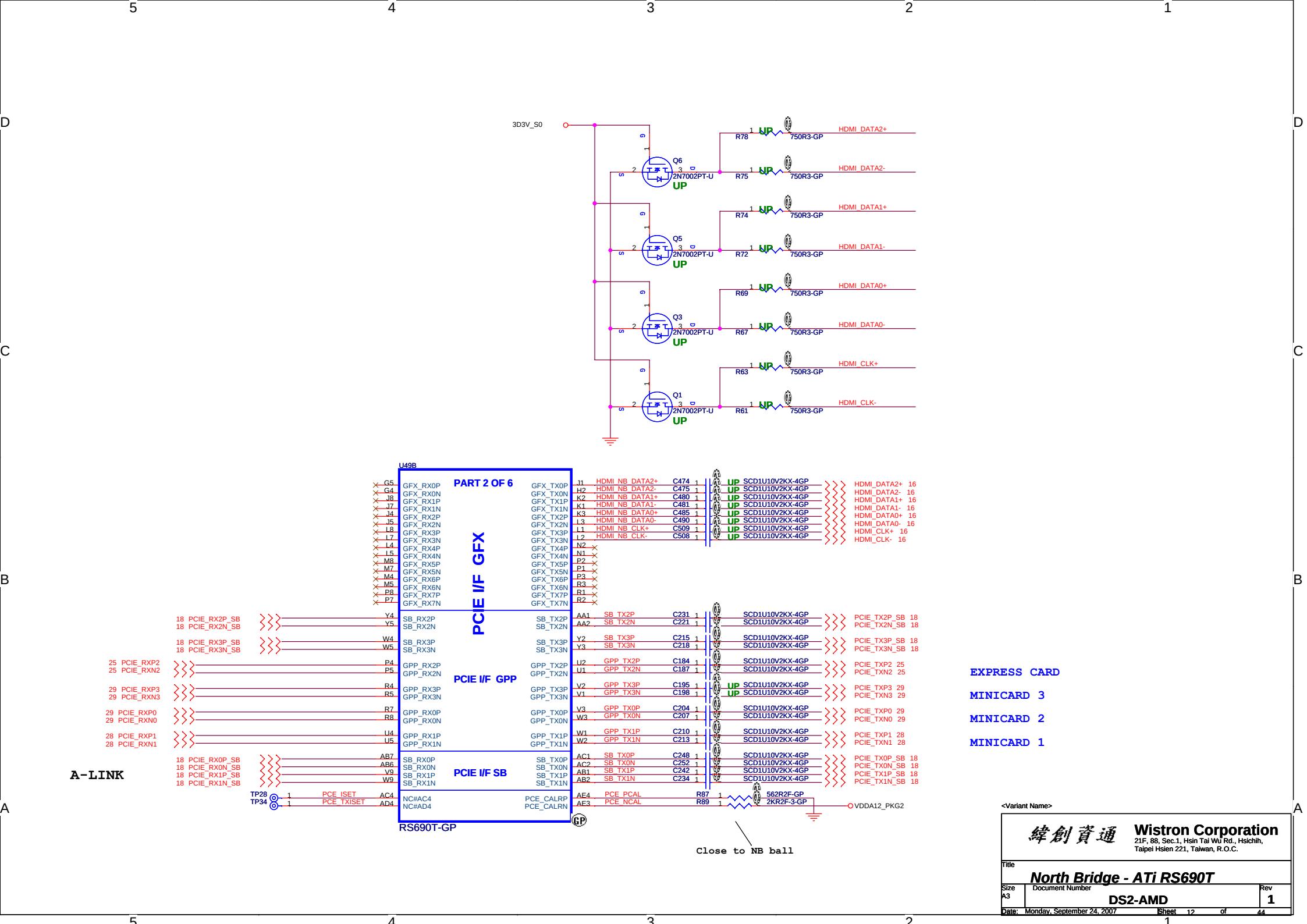
PARALLEL TERMINATION

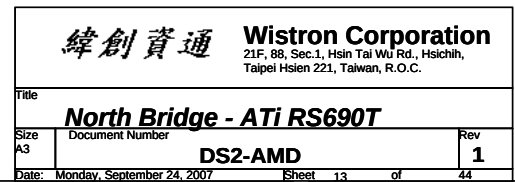


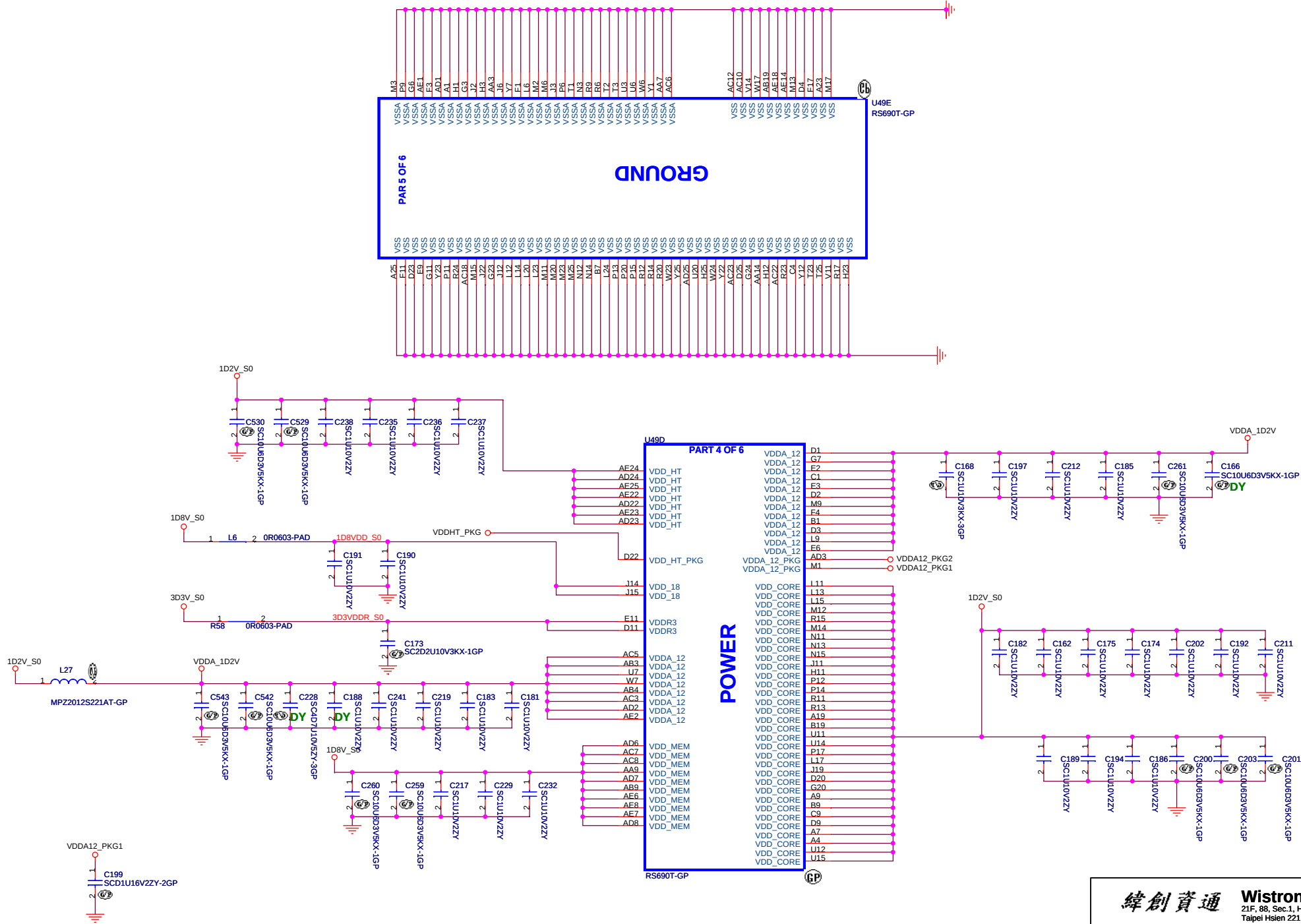
Decoupling Capacitor



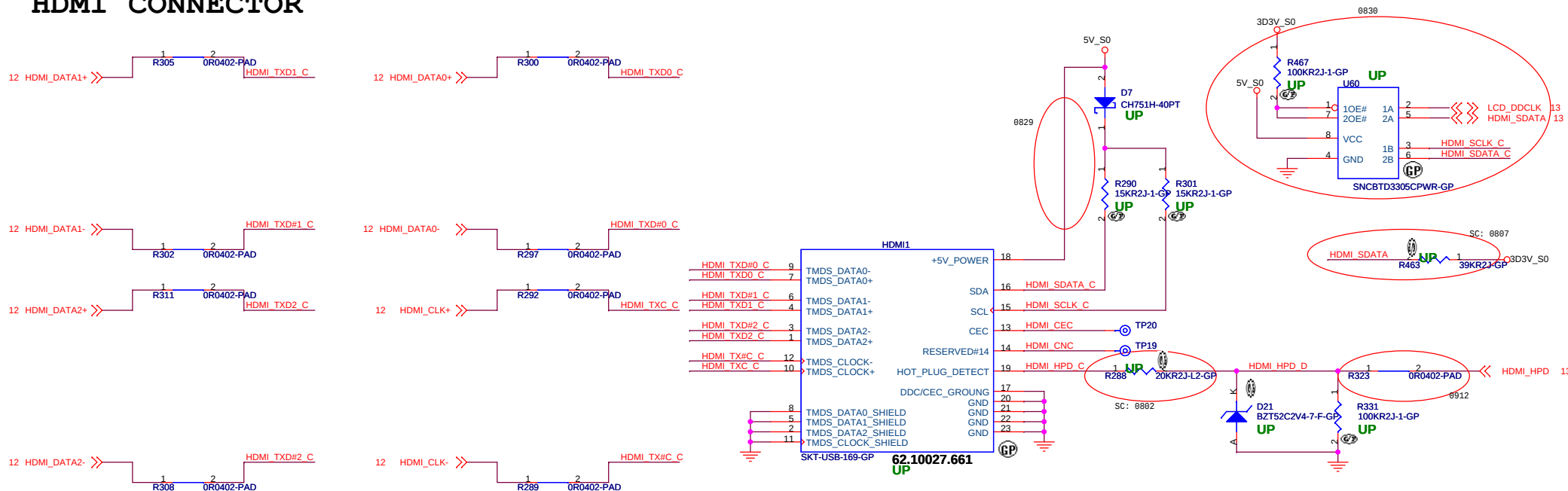




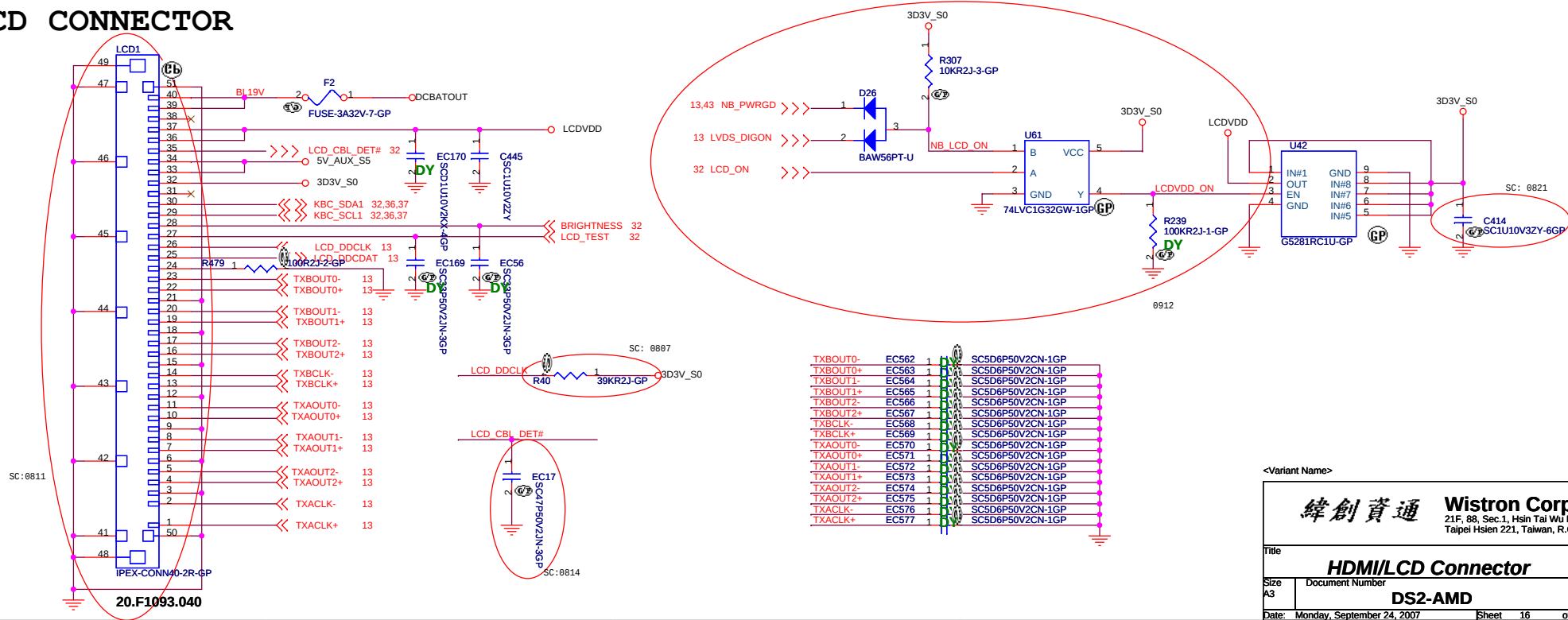




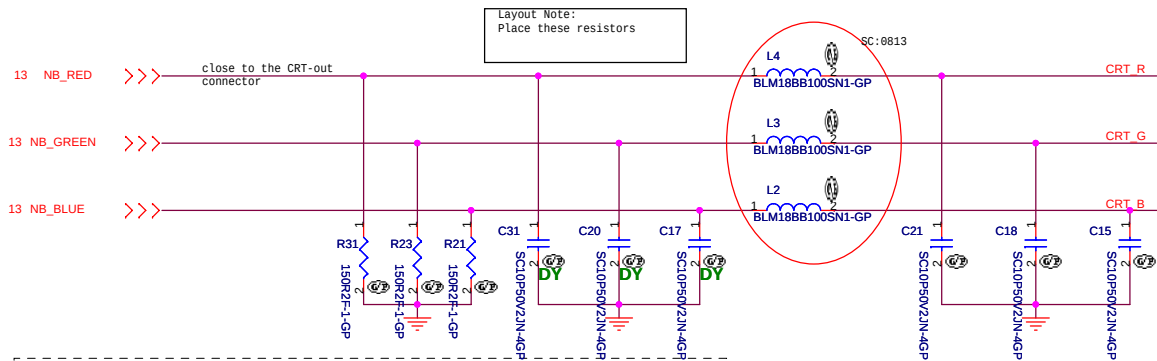
HDMI CONNECTOR



LCD CONNECTOR

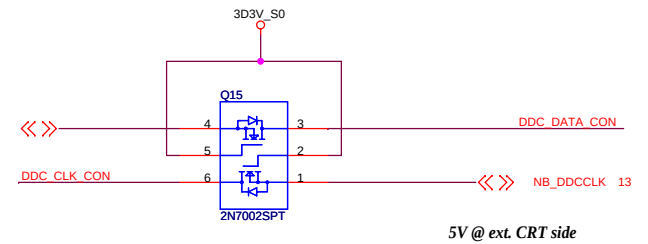
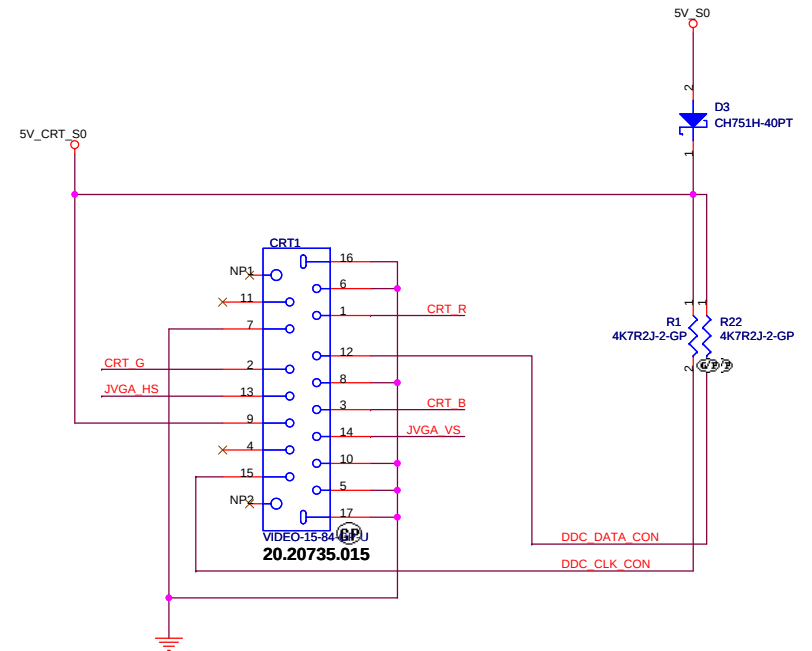
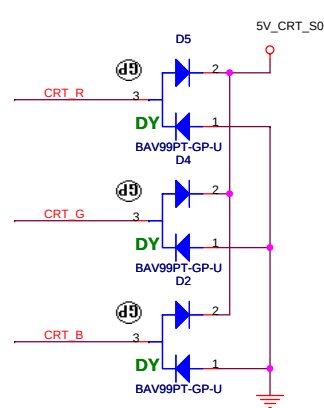
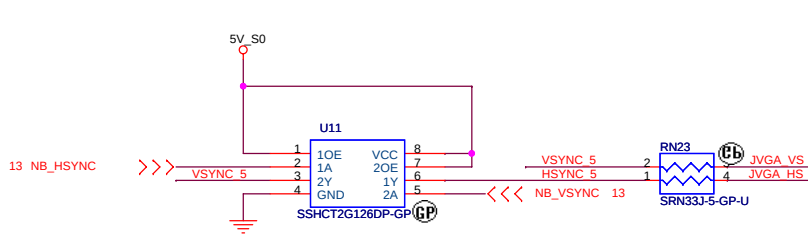


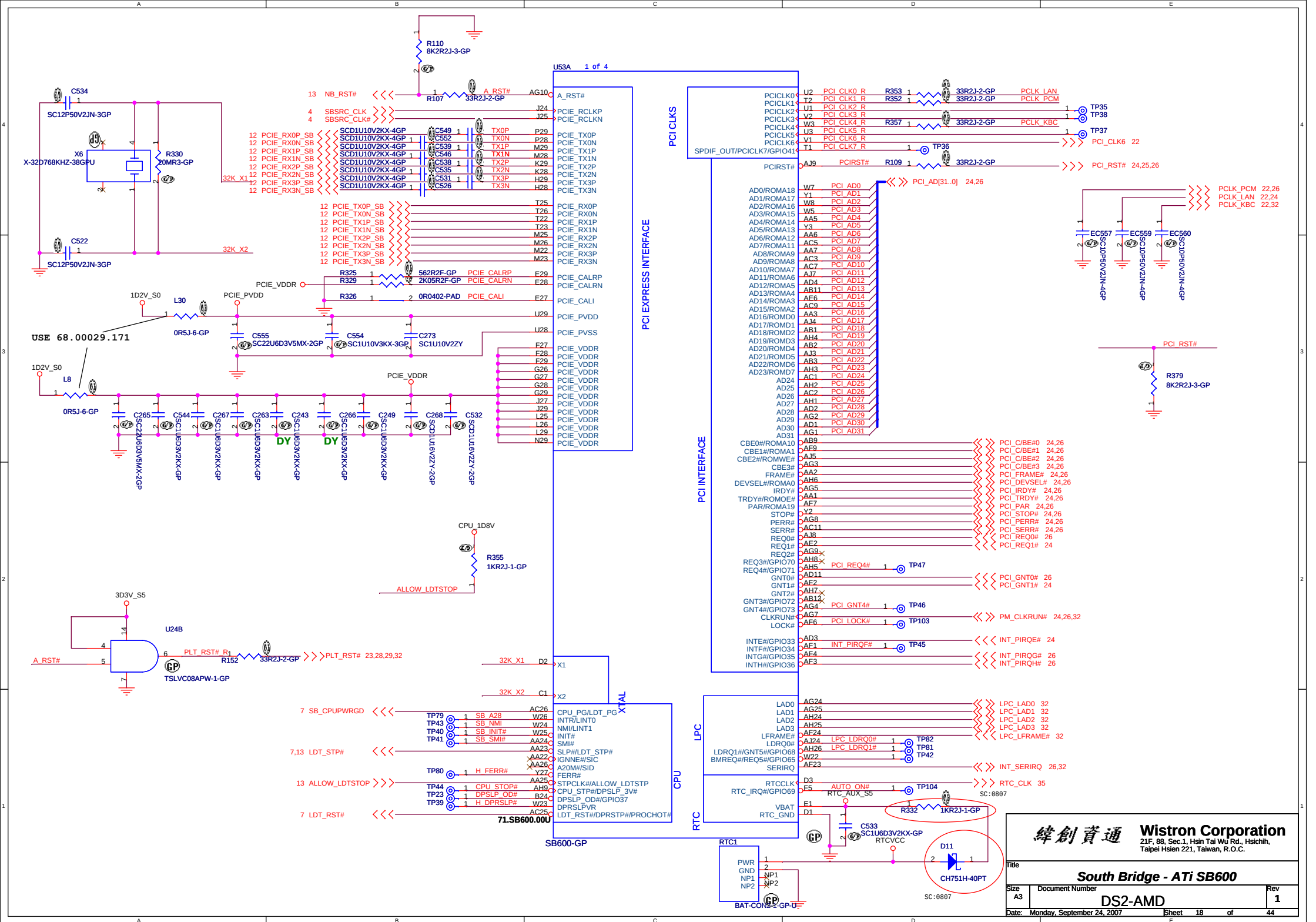
CRT I/F & CONNECTOR

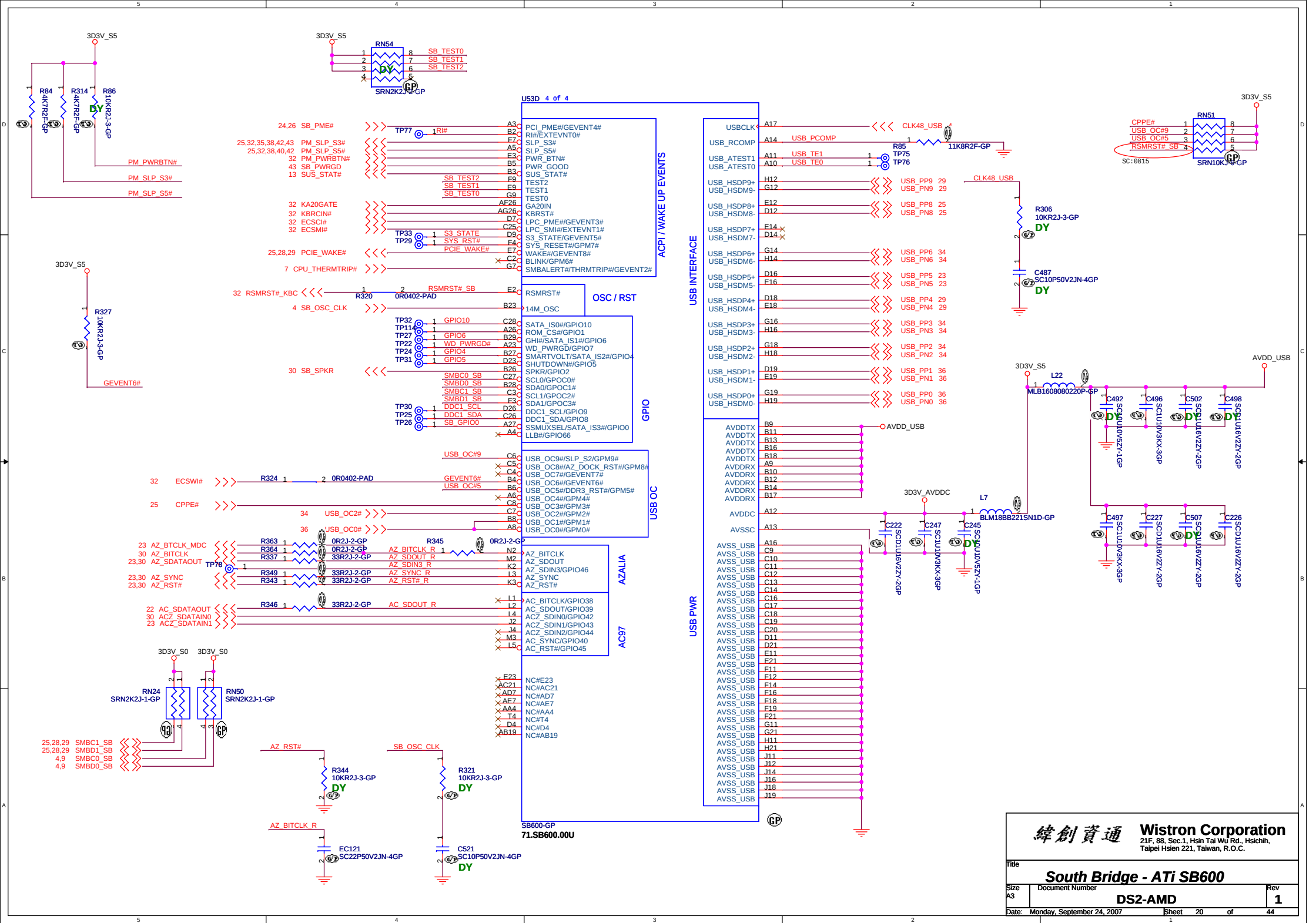


Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

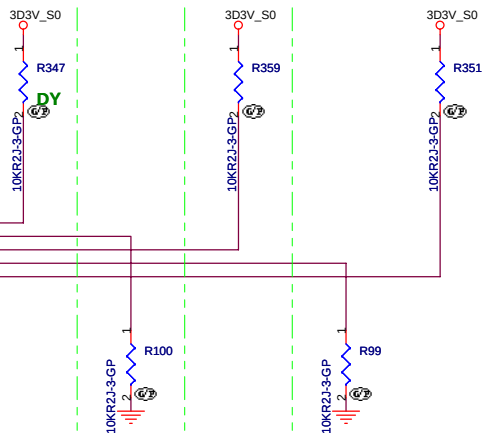






PCI_CLK4
PCI_CLK6
PCI_CLK0
PCI_CLK1

20 AC_SDATAOUT
18,32 PCLK_KBC
18 PCI_CLK6
18,24 PCLK_LAN
18,26 PCLK_PCM



REQUIRED SYSTEM STRAPS

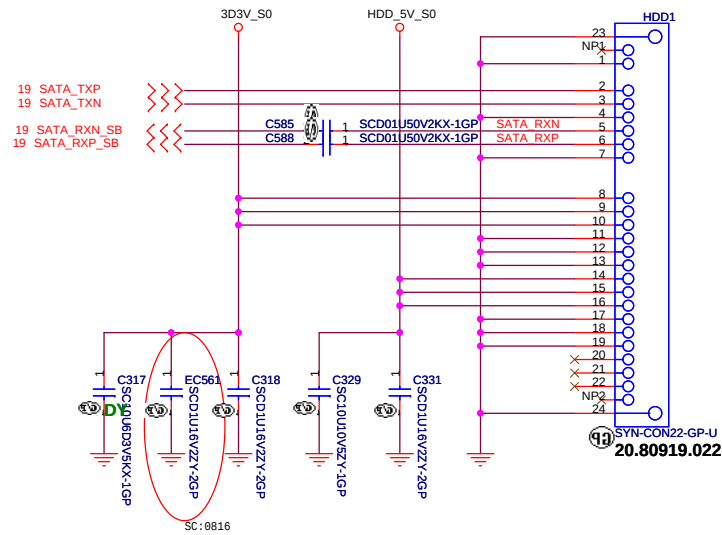
SB600					
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

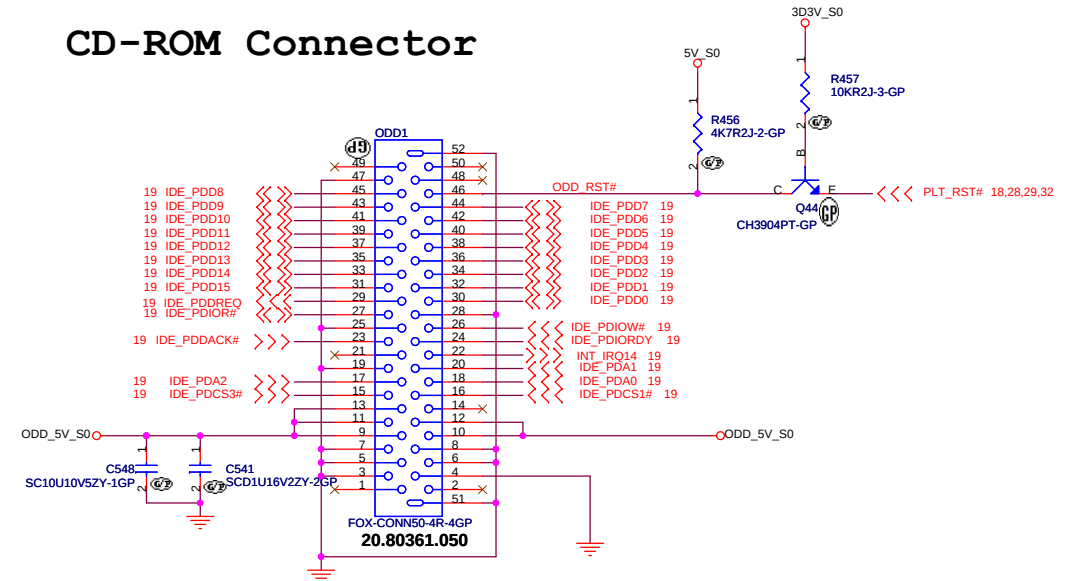
DEBUG STRAPS

	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

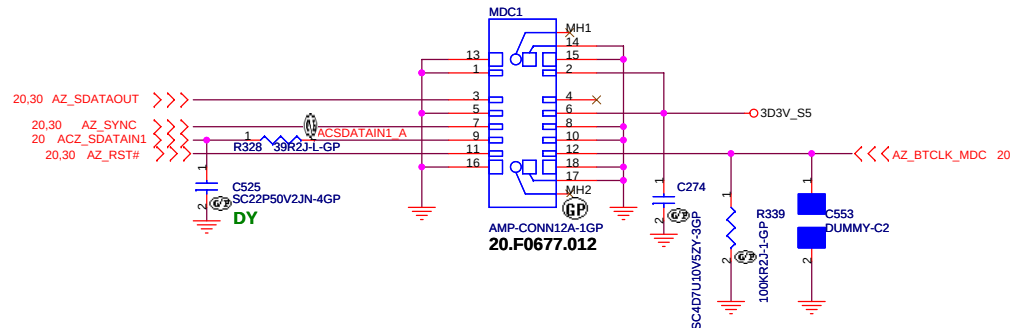
SATA HD Connector



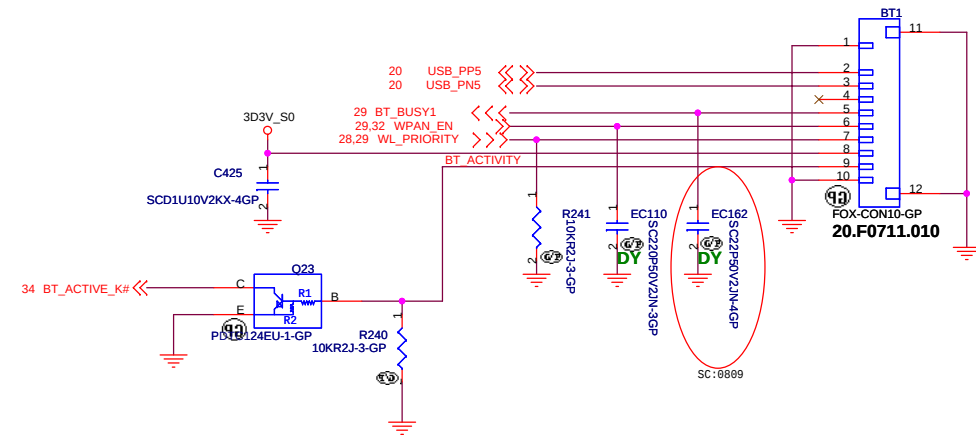
CD-ROM Connector



MDC 1.5 Connector

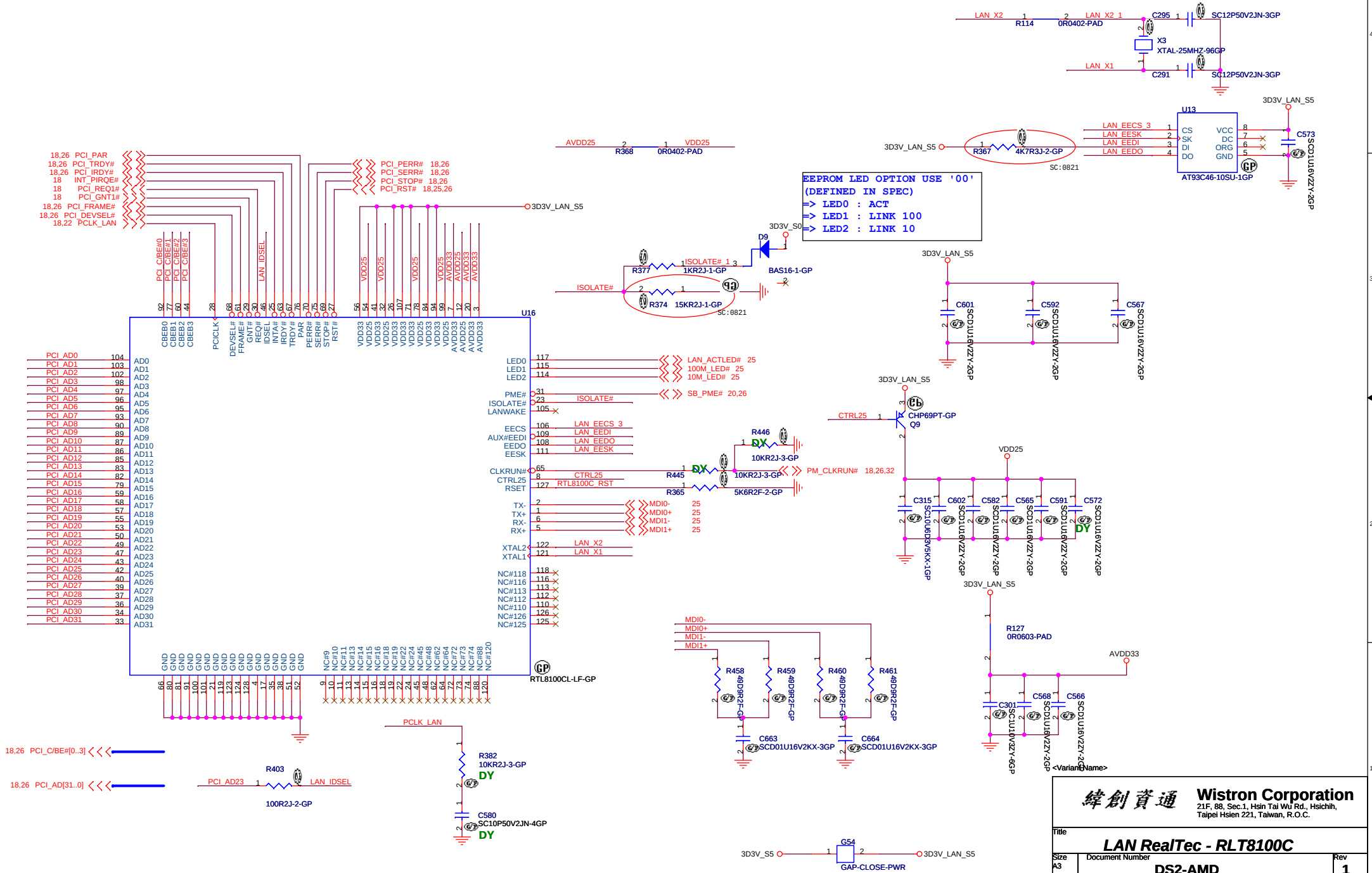


BT Module Connector

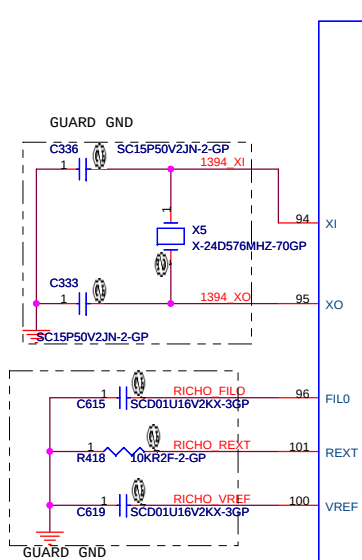


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Taipei Hsien 221, Taiwan, R.O.C.

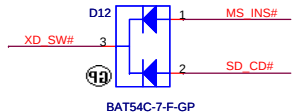
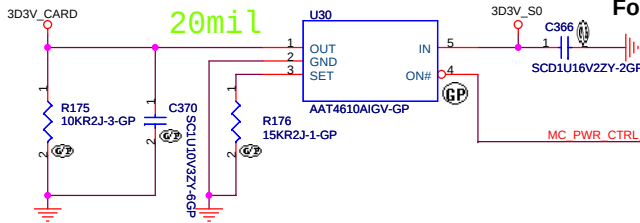
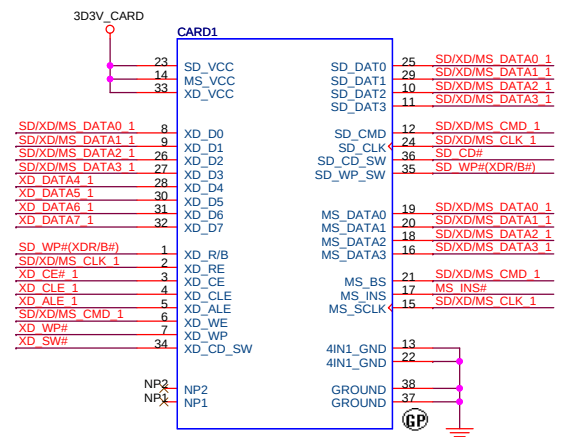
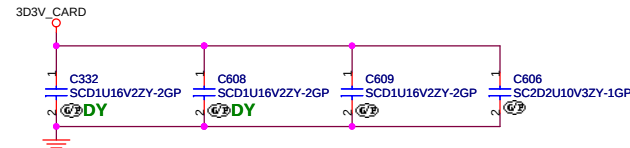
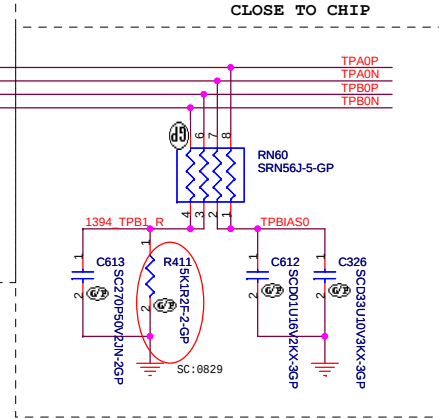
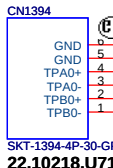
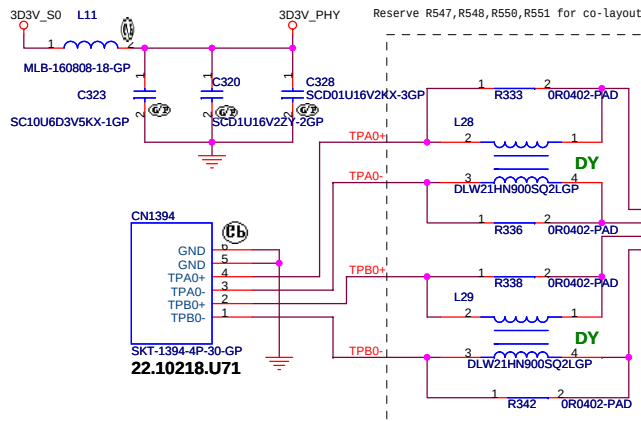
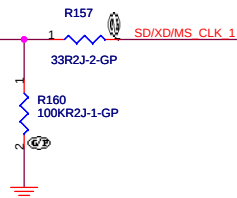
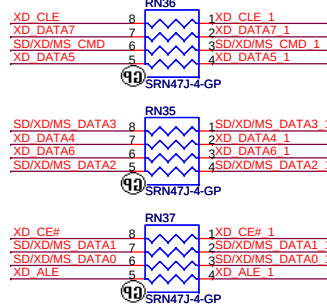
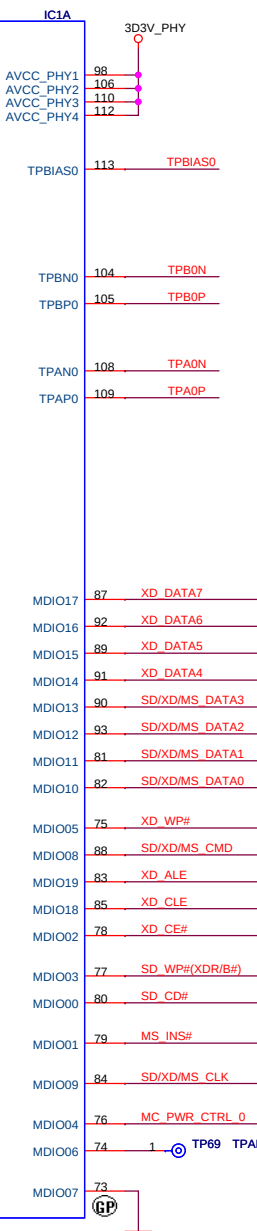
Title HD/CDROM/MDC/BT		
Size A3	Document Number DS2-AMD	Rev 1
Date: Monday, September 24, 2007	Sheet 23	of 44



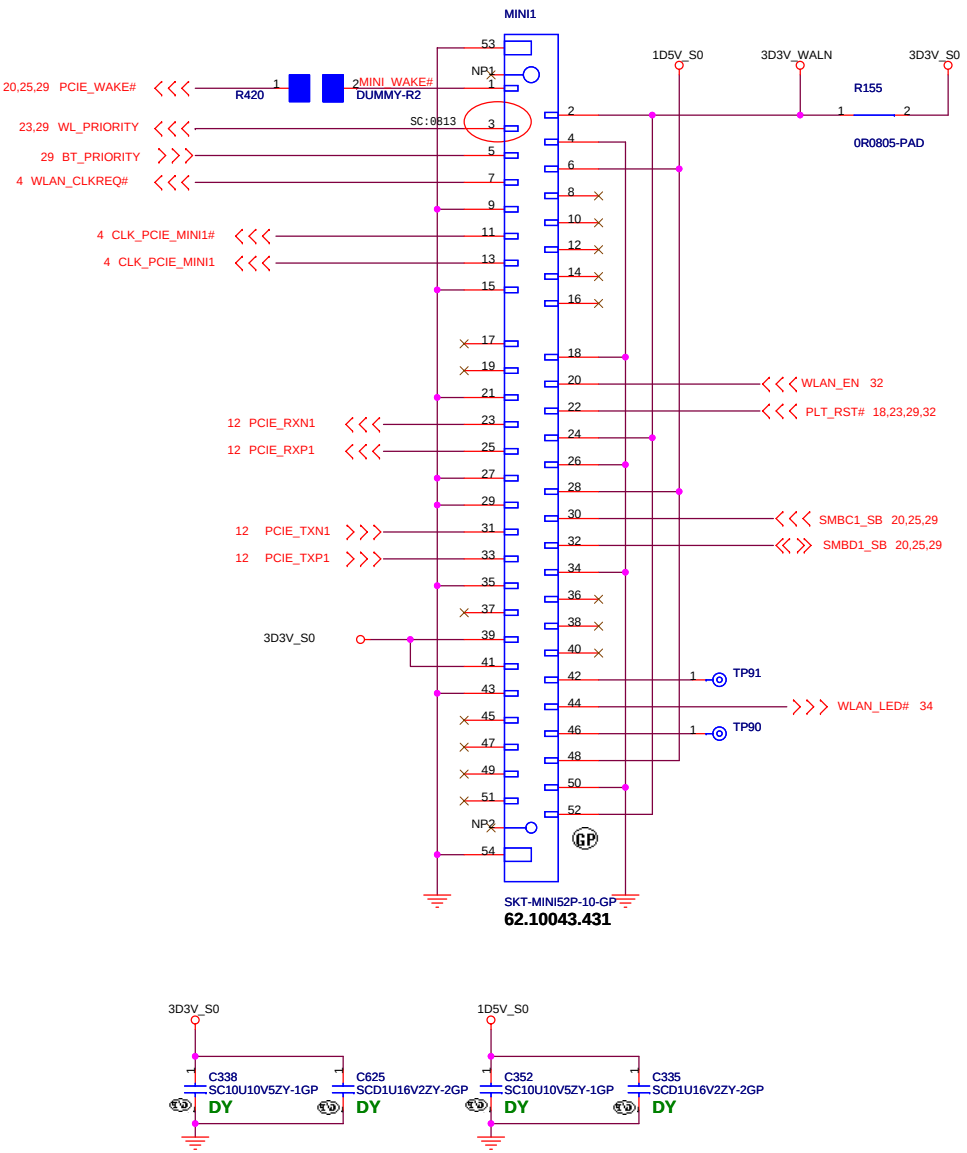
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Taipei Hsien 221, Taiwan, R.O.C.



IEEE1394/SD

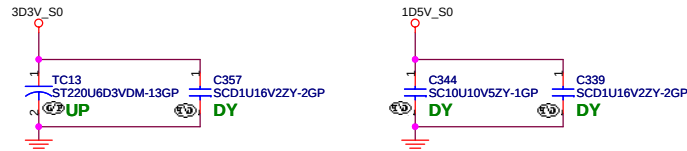
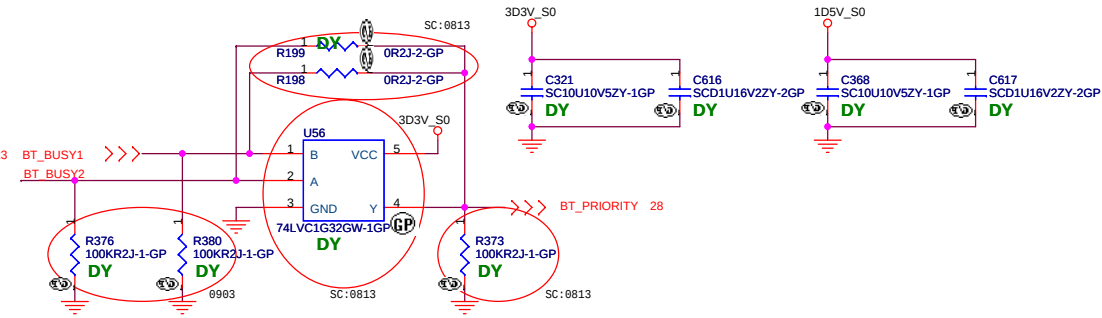
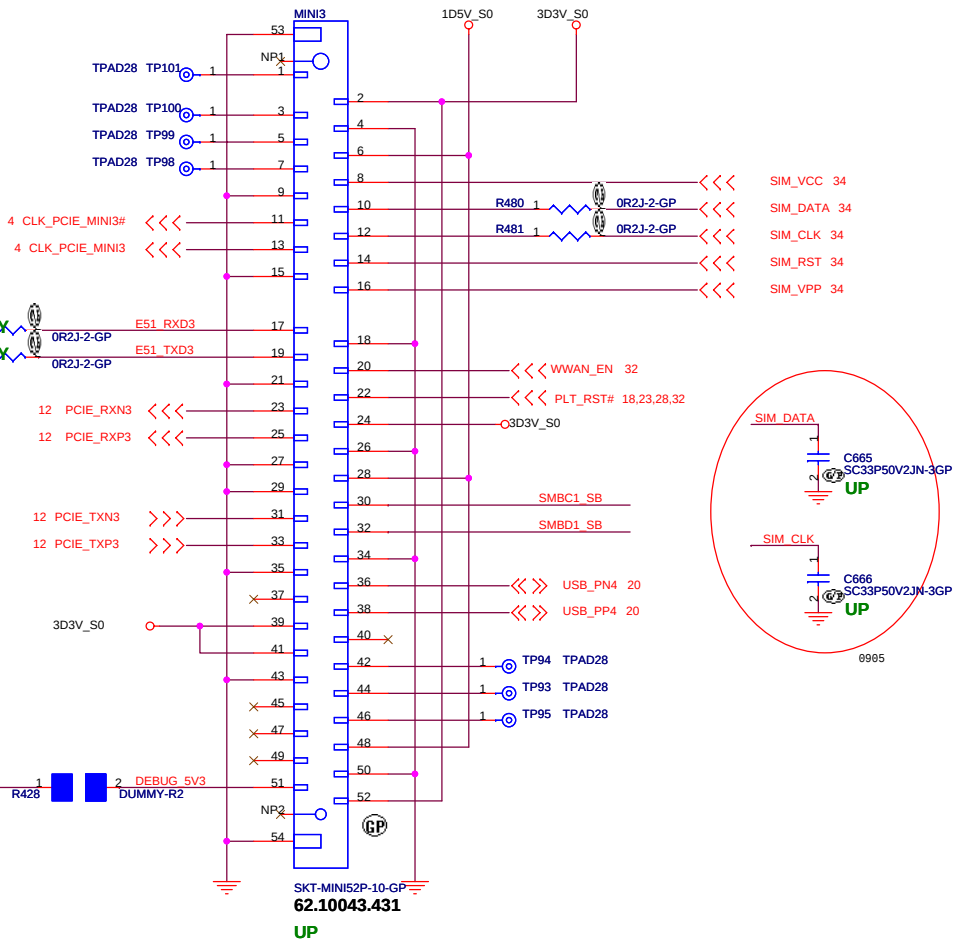
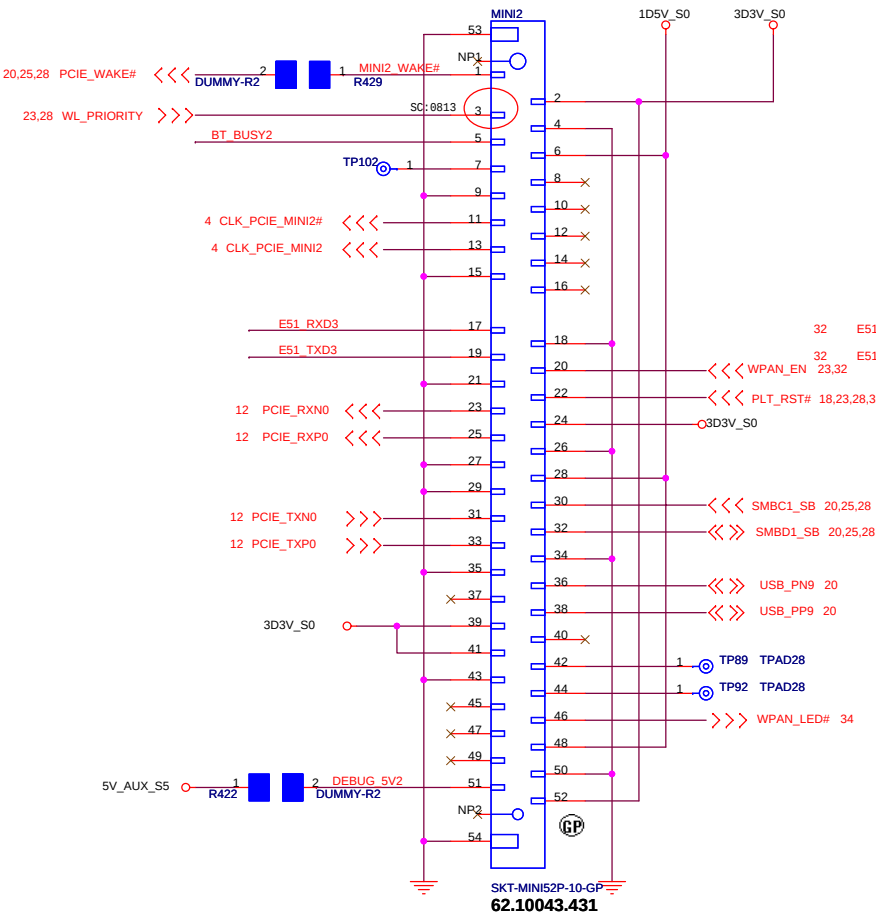


Mini Card Connector 1(802.11a/b/g)



Mini Card Connector 2(UWB)

Mini Card Connector 3(WWAN)



WPC8763L STRAP PIN

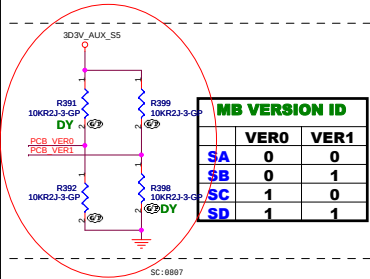
JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES	GPIO Port	GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

TRIS#(Pin 110) TRI-STATE
Forces the device to float all its output and I/O pins,if an external 10 KΩ pull-down resistor is conected.

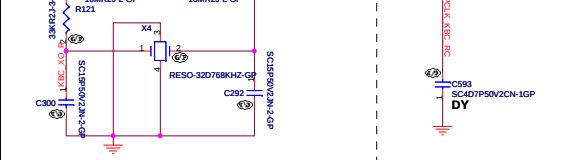
BADDR1-0 (PIN 111, 112) I/O Base Address.
10KΩ external pull-down resistor on BADDR1: Core defined

SHBM PIPN83 Shared Host BIOS Memory.
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.

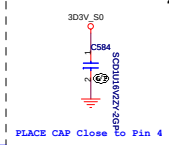
B



A

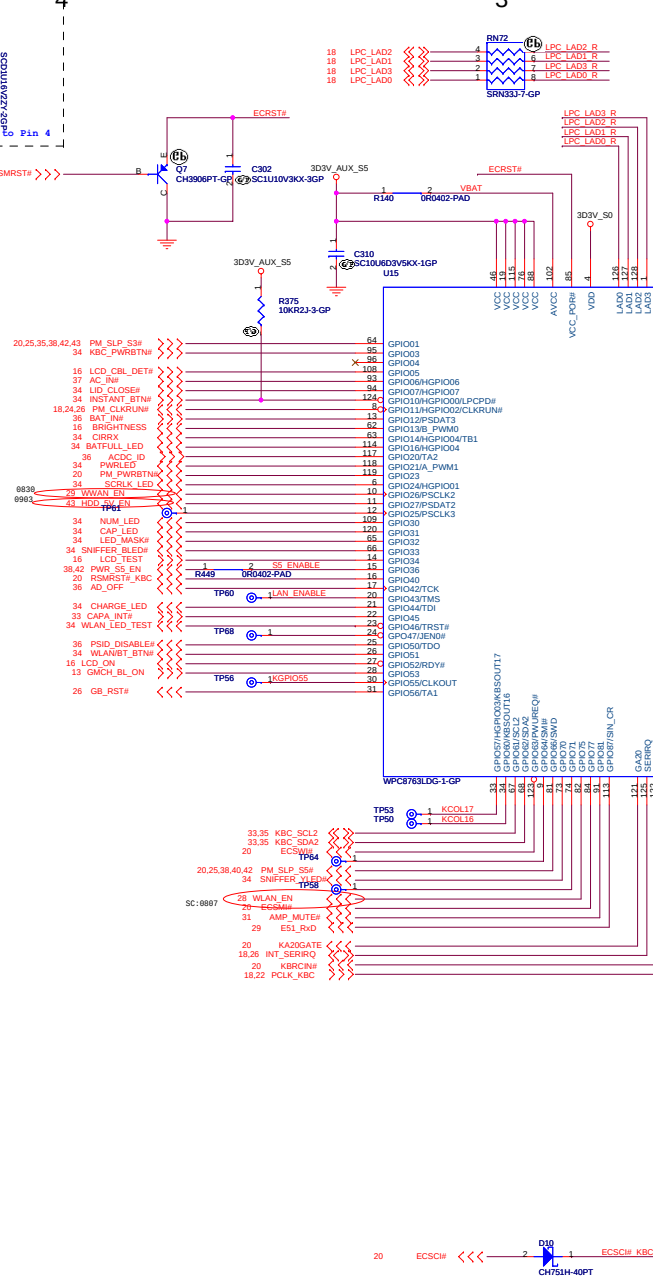


4

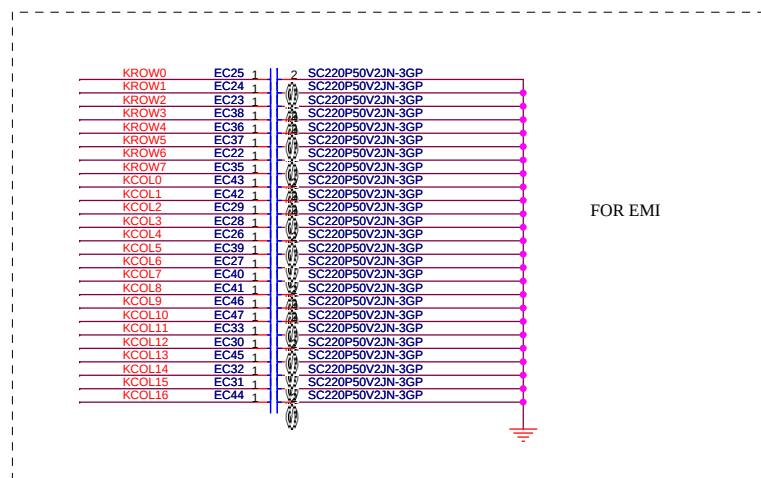
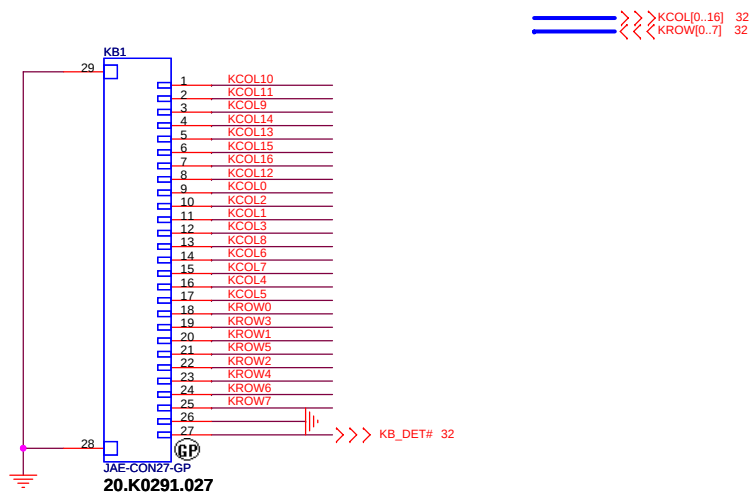


4

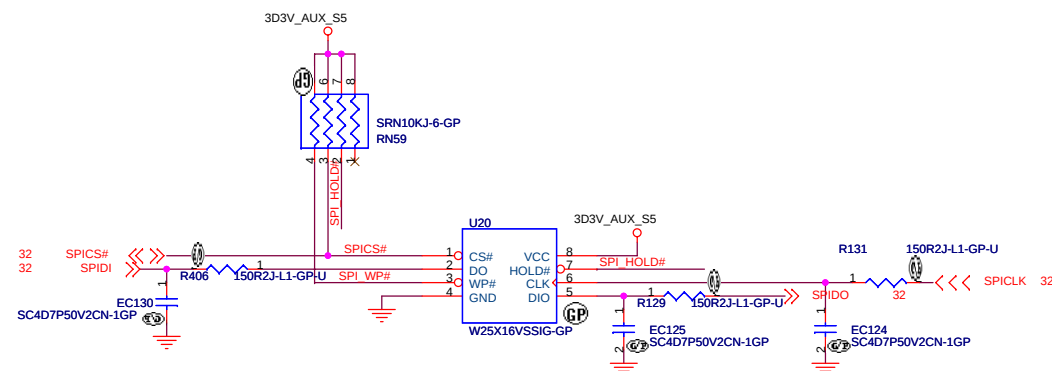
3



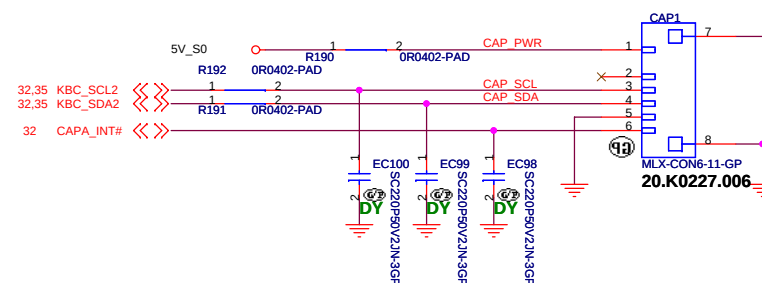
Internal KeyBoard Connector



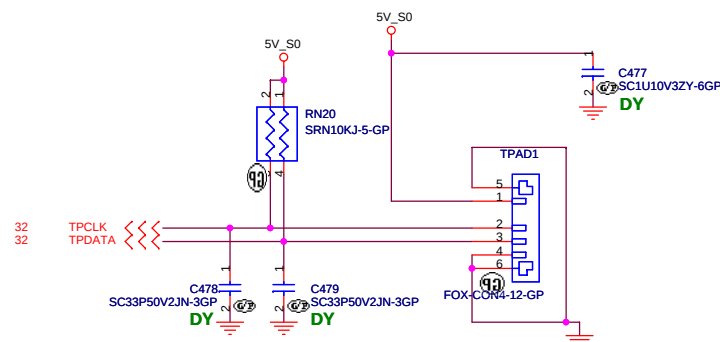
SPI ROM



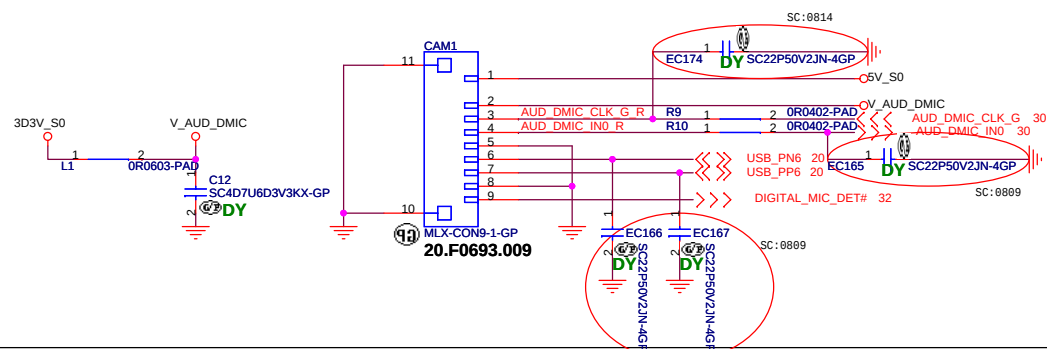
CAPACITY BUTTON



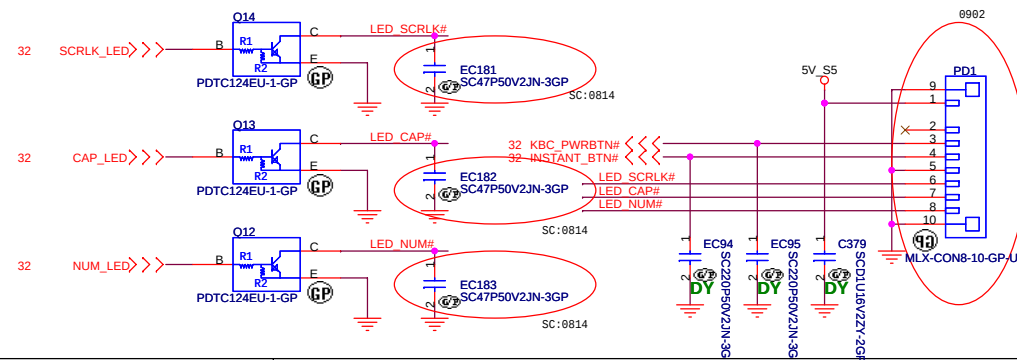
TouchPad Connector



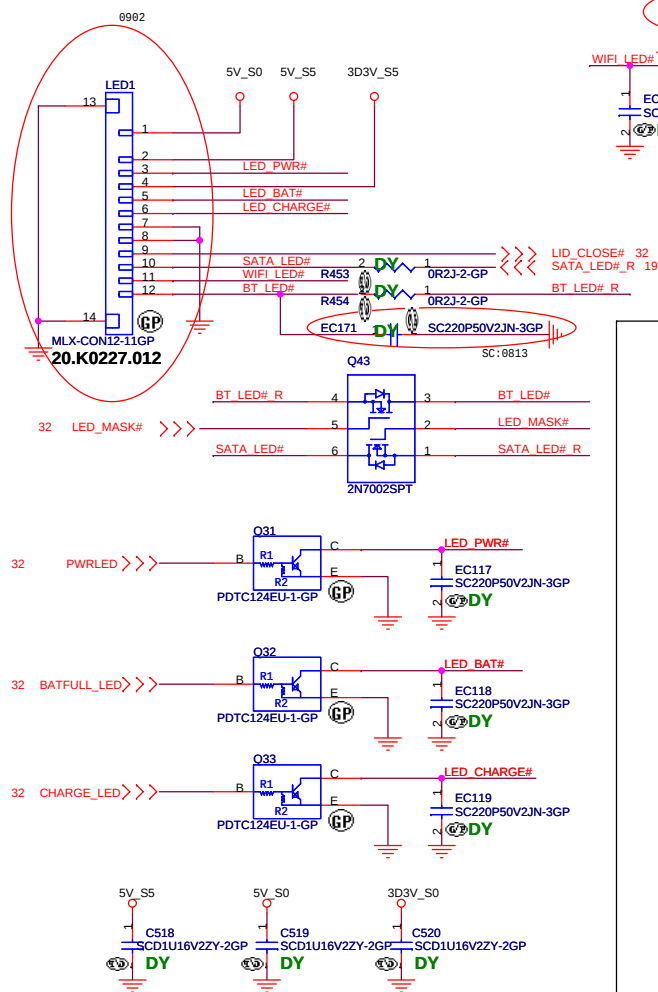
CAMERA/D.MIC Connector



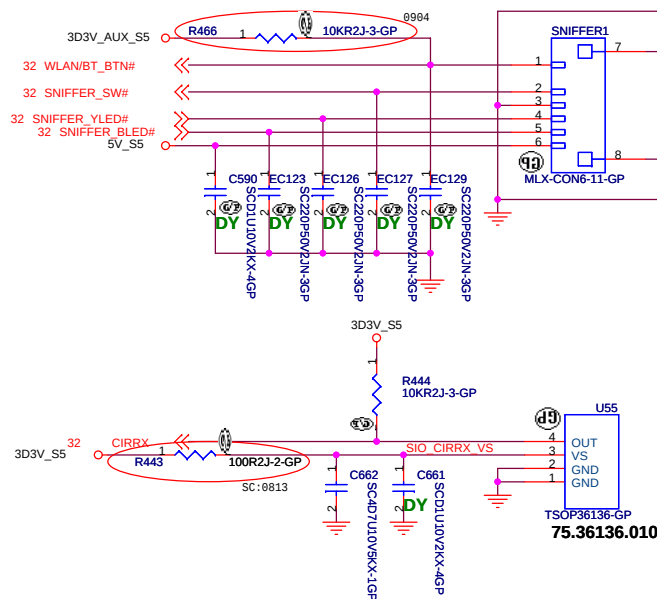
Power Dash Board Connector



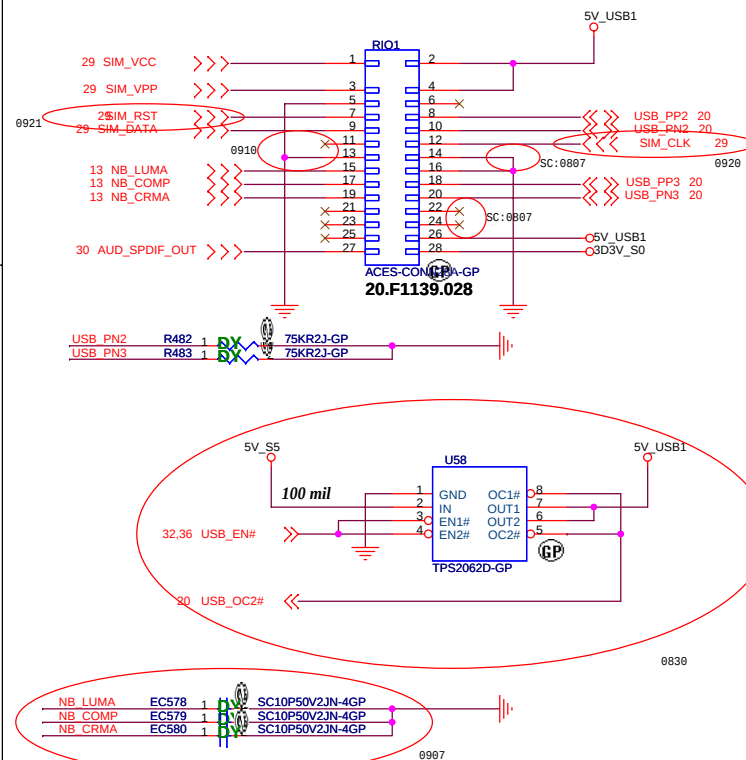
LED Board Connector

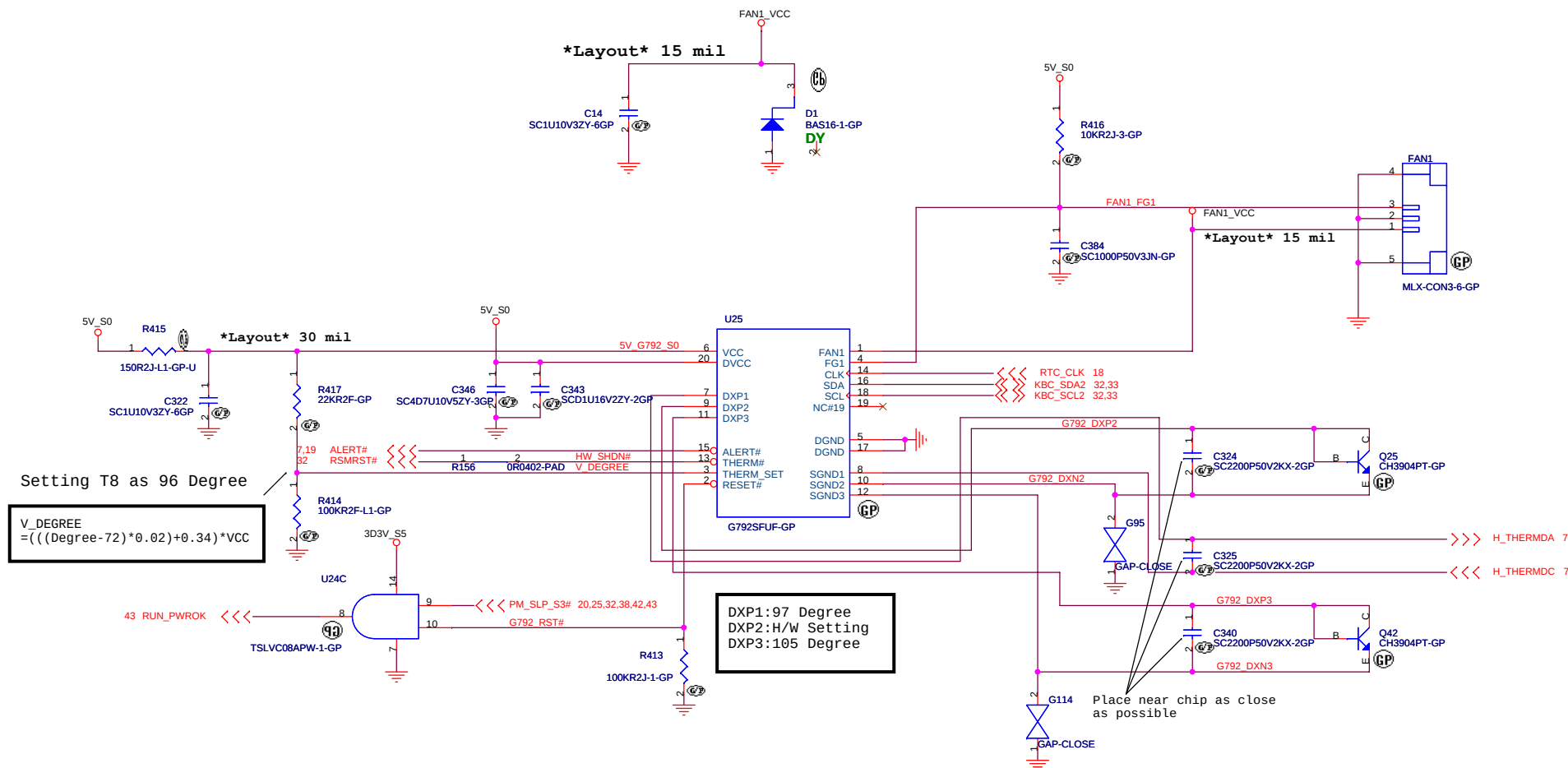


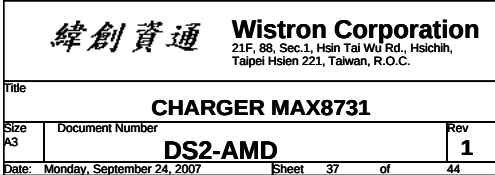
SNIFFER Board Connector

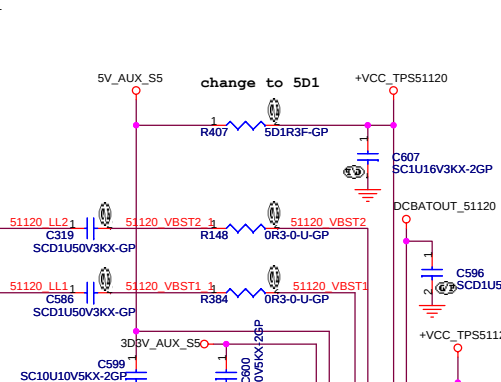
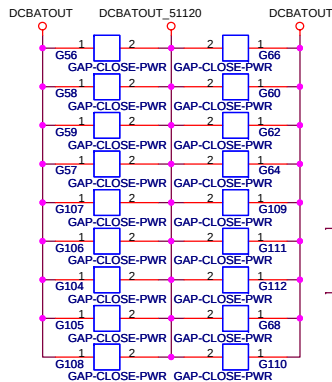


RIGHT I/O Board Connector



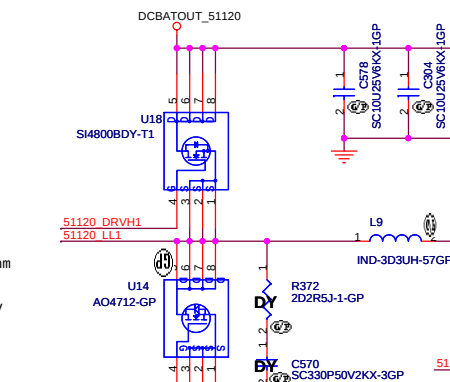




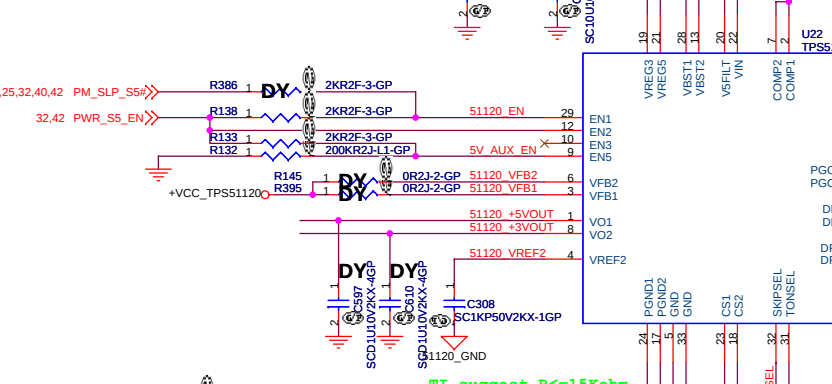
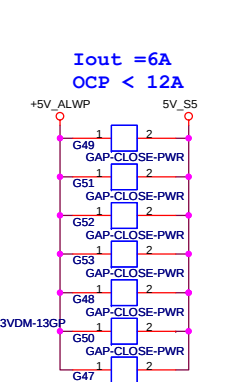


HS:
 $R_{ds(on)} = 23\text{m}\Omega \sim 30\text{m}\Omega$
 $Q_g = 8.7 \sim 13\text{nC}$
 $I_d = 6.5\text{A}$ @25degree C
 $V_{gs(th)} = 0.8\text{V}, 1.8\text{V}$
 $R_g = 0.5, 1.4, 2.2\text{ohm}$

LS:
 $R_{ds(on)} = 15\text{m}\Omega \sim 18\text{m}\Omega$
 $Q_g = 12\text{nC}$
 $I_d = 9.1\text{A}$
 $V_{gs(th)} = 1.5\text{V}, 1.8\text{V}, 2.4\text{V}$
 $R_g = 2.4 \sim 3.6\text{ohm}$

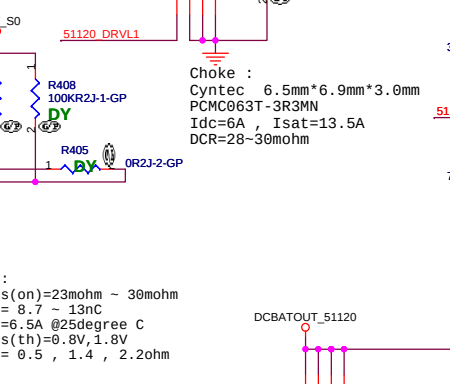


Choke :
 Cyntec 6.5mm*6.9mm*3.0mm
 PCMC063T-3R3MN
 $I_{dc} = 6\text{A}$, $I_{sat} = 13.5\text{A}$
 $DCR = 28 \sim 30\text{m}\Omega$

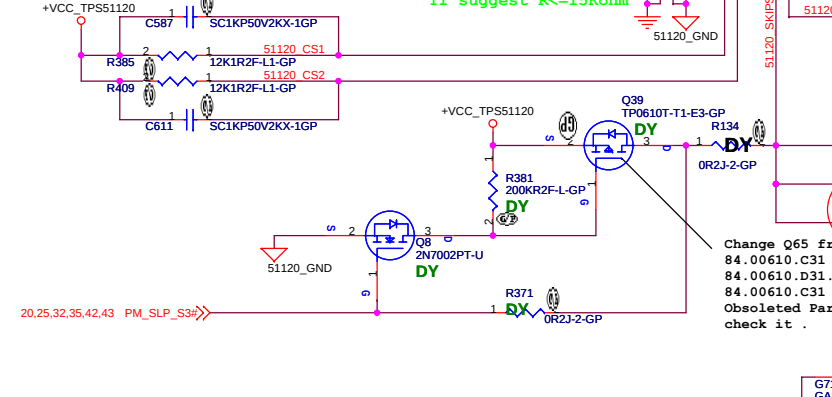
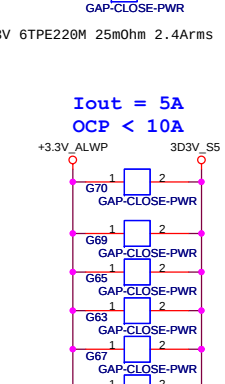


HS:
 $R_{ds(on)} = 23\text{m}\Omega \sim 30\text{m}\Omega$
 $Q_g = 8.7 \sim 13\text{nC}$
 $I_d = 6.5\text{A}$ @25degree C
 $V_{gs(th)} = 0.8\text{V}, 1.8\text{V}$
 $R_g = 0.5, 1.4, 2.2\text{ohm}$

LS:
 $R_{ds(on)} = 15\text{m}\Omega \sim 18\text{m}\Omega$
 $Q_g = 12\text{nC}$
 $I_d = 9.1\text{A}$
 $V_{gs(th)} = 1.5\text{V}, 1.8\text{V}, 2.4\text{V}$
 $R_g = 2.4 \sim 3.6\text{ohm}$

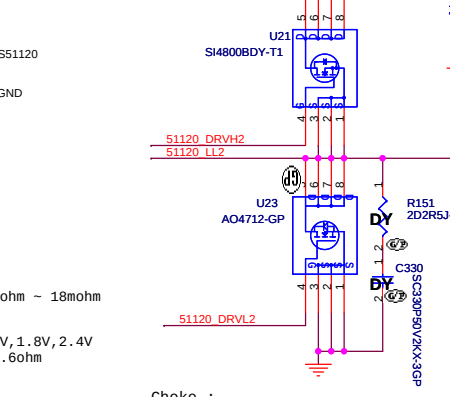


Choke :
 Cyntec 6.5mm*6.9mm*3.0mm
 PCMC063T-3R3MN
 $I_{dc} = 6\text{A}$, $I_{sat} = 13.5\text{A}$
 $DCR = 28 \sim 30\text{m}\Omega$

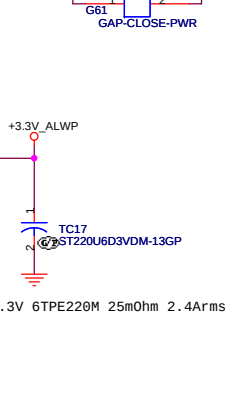


HS:
 $R_{ds(on)} = 23\text{m}\Omega \sim 30\text{m}\Omega$
 $Q_g = 8.7 \sim 13\text{nC}$
 $I_d = 6.5\text{A}$ @25degree C
 $V_{gs(th)} = 0.8\text{V}, 1.8\text{V}$
 $R_g = 0.5, 1.4, 2.2\text{ohm}$

LS:
 $R_{ds(on)} = 15\text{m}\Omega \sim 18\text{m}\Omega$
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Choke :
 Cyntec 6.5mm*6.9mm*3.0mm
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 $DCR = 28 \sim 30\text{m}\Omega$

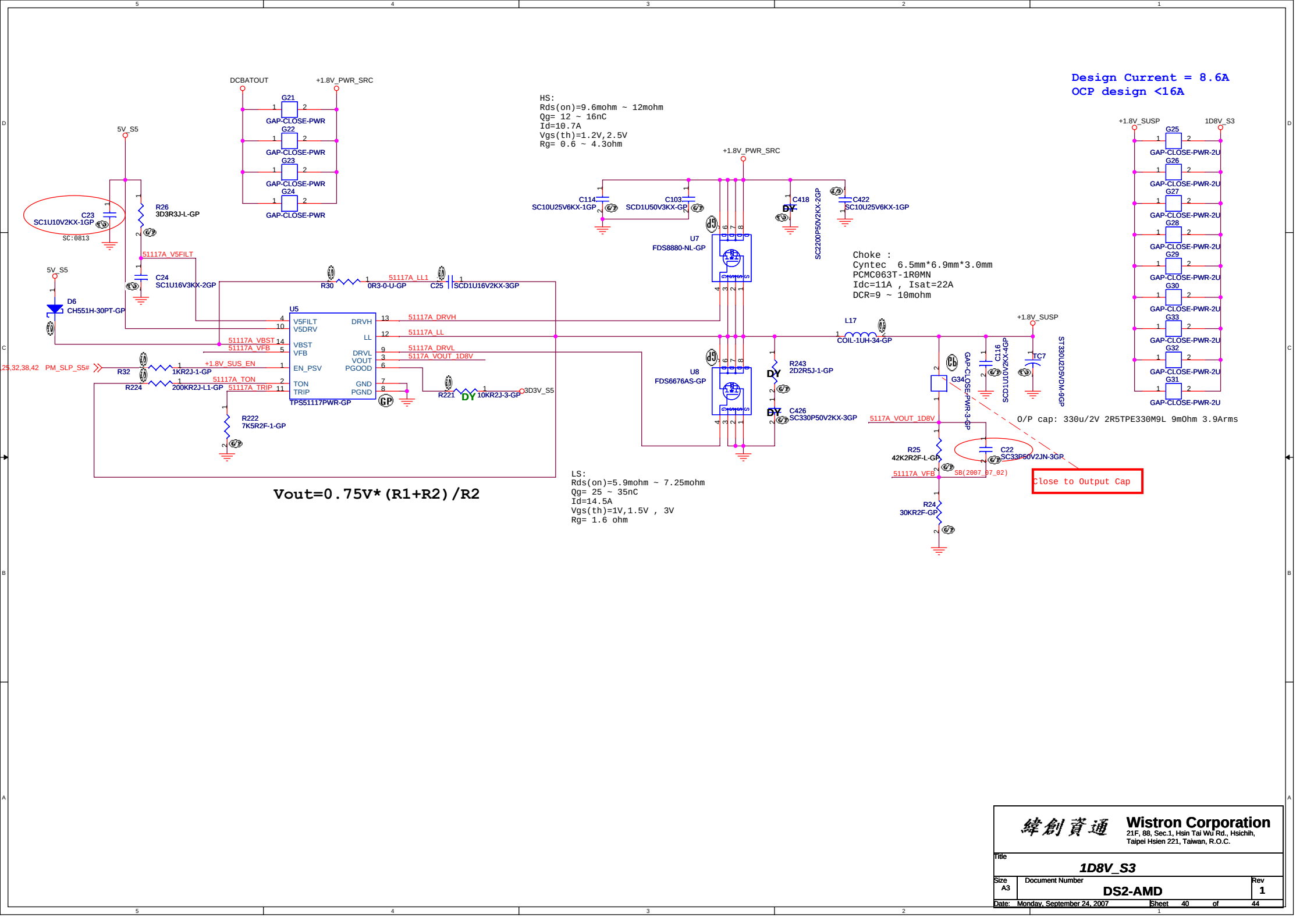


$$V_{out} = 1V * (R1 + R2) / R2$$

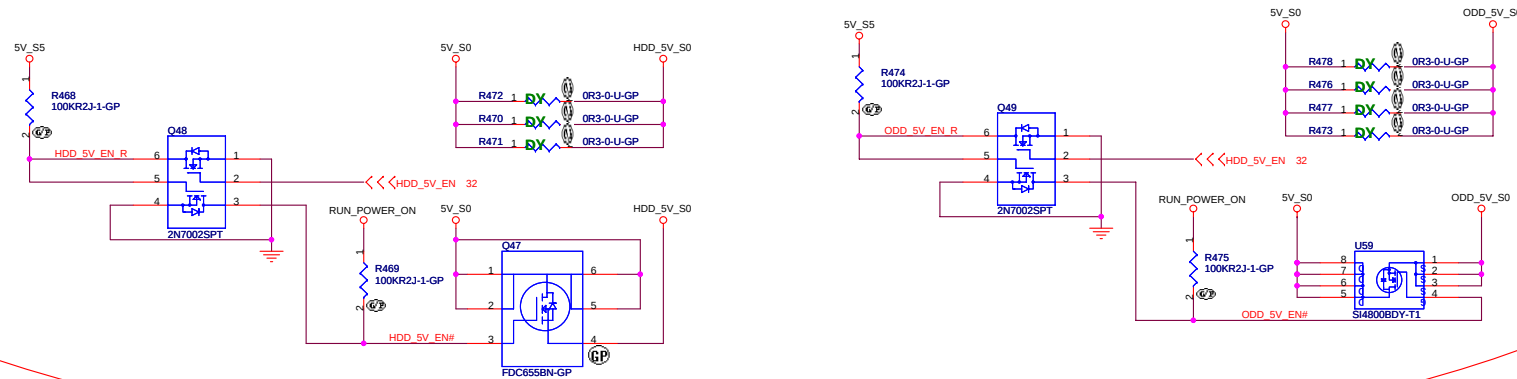
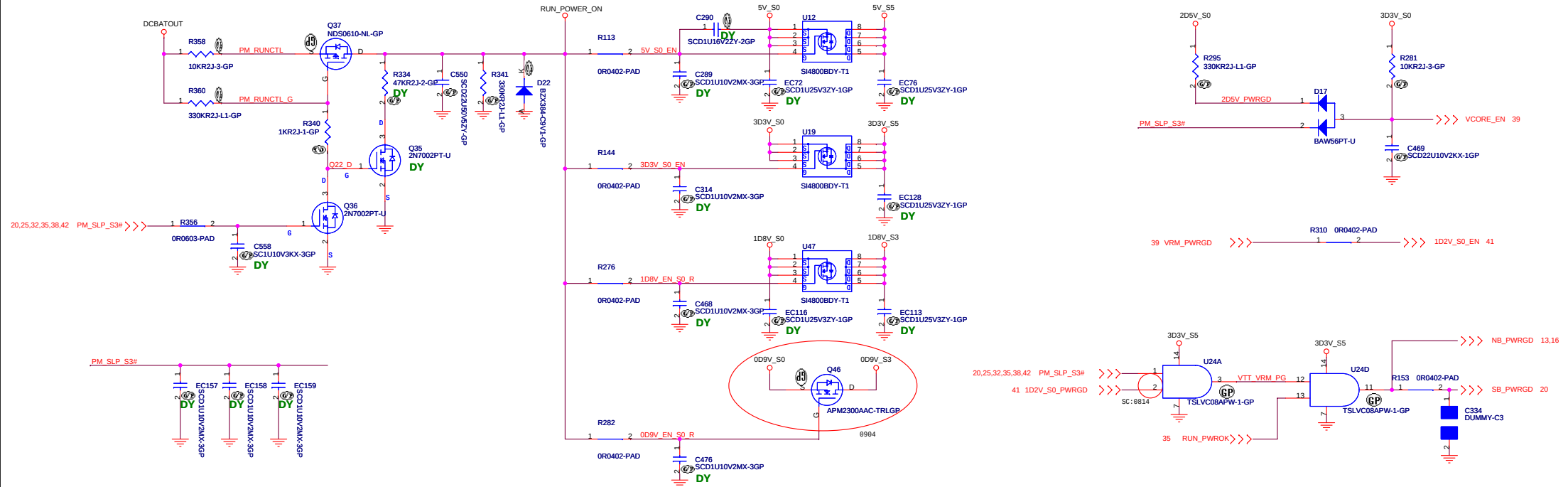
	GPIO	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1	280k/CH1	220k/CH1	180k/CH1
VFB1	580k/CH2	430k/CH2	330k/CH2	2870k/CH2
VFB2	N/A	not use	5V	Fixed Output
VFB2	N/A	not use	Adj.	3.3V
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

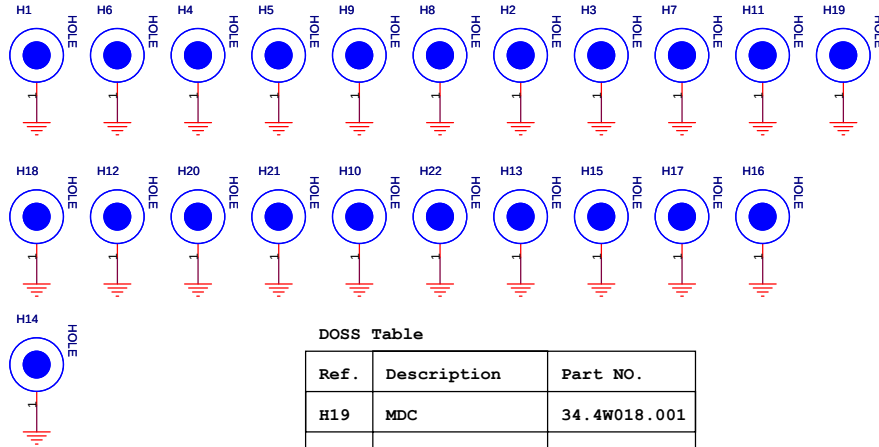
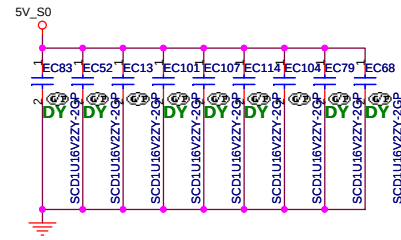
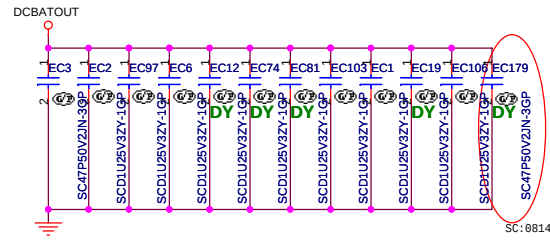
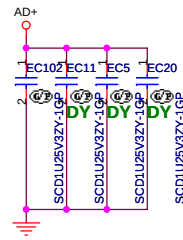
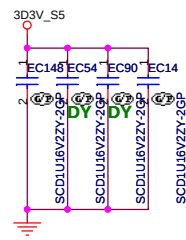
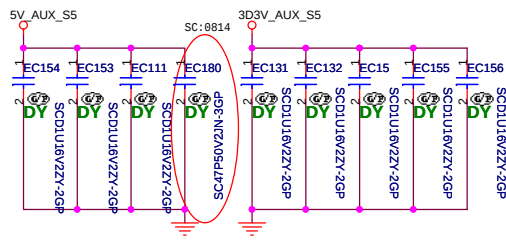
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi,
 Taipei Hsien 221, Taiwan, R.O.C.

Title	3V/5V TPS51120		
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Run Power





DOSS Table

Ref.	Description	Part NO.
H19	MDC	34.4W018.001
H20	Mini Card	34.4W005.001
H21	Mini Card	34.4W005.001
H22	Mini Card	34.4W005.001
H18	Heat sink	34.4A908.001
H15	New Card	34.4W004.001

