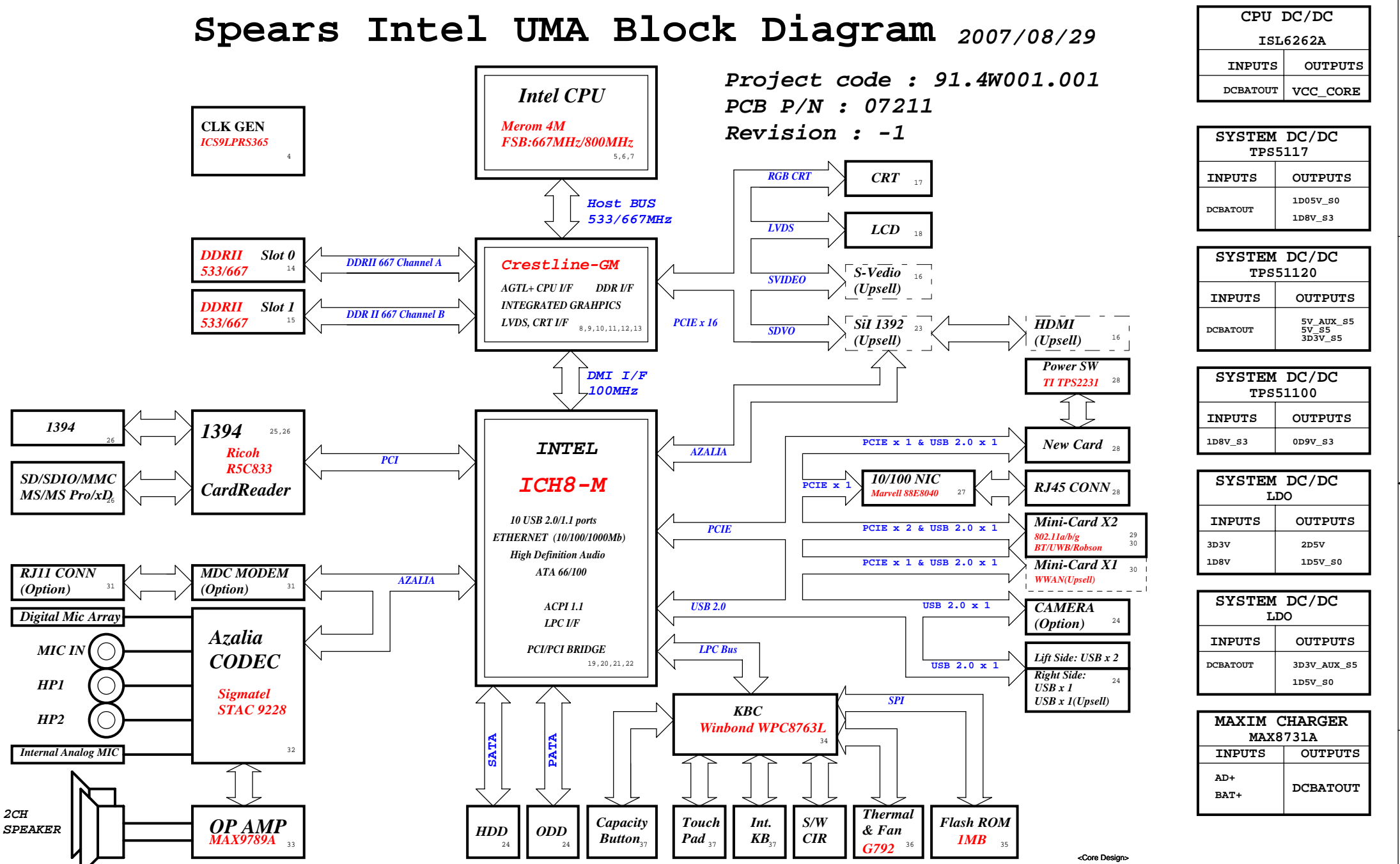


# Spears Intel UMA Block Diagram 2007/08/29

Project code : 91.4W001.001  
PCB P/N : 07211  
Revision : -1



CPU DC/DC ISL6262A	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS5117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51100	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3

SYSTEM DC/DC LDO	
INPUTS	OUTPUTS
3D3V 1D8V	2D5V 1D5V_S0

SYSTEM DC/DC LDO	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 1D5V_S0

MAXIM CHARGER MAX8731A	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size A3 Document Number

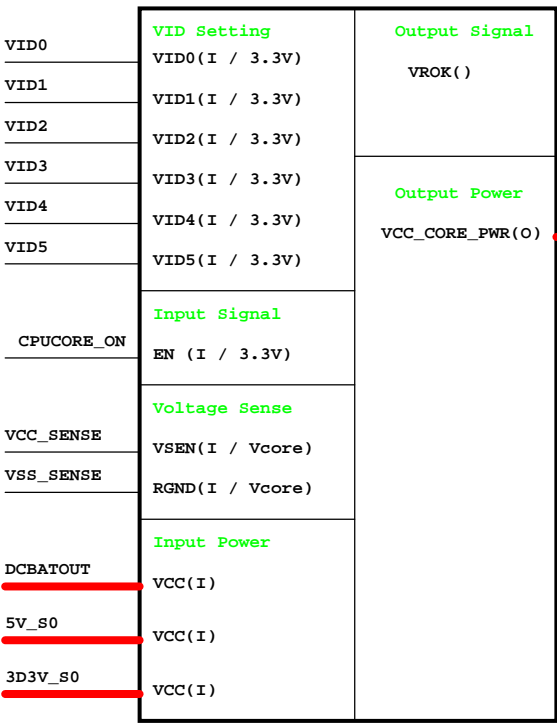
Date: Wednesday, September 12, 2007 Sheet 1 of 47

DS2 System Block Diagram

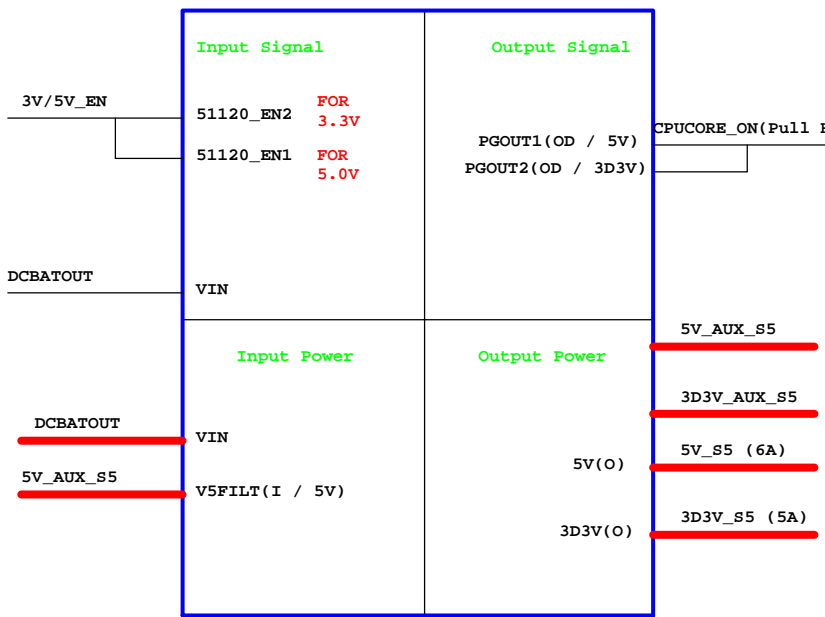
Spears-Intel

Rev -1

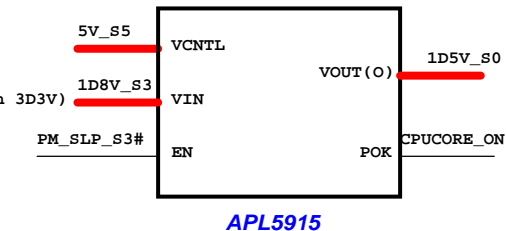
**CPU\_CORE**  
**ISL6262A**



**TI TPS51120**  
**3D3V/5V**



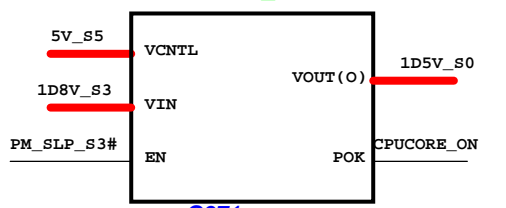
**1D5V\_S0**



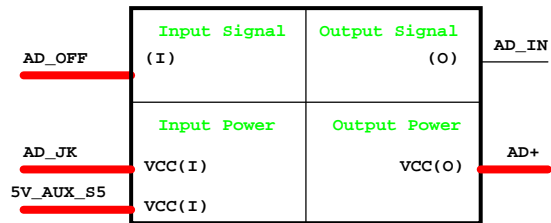
**2D5V\_S0**



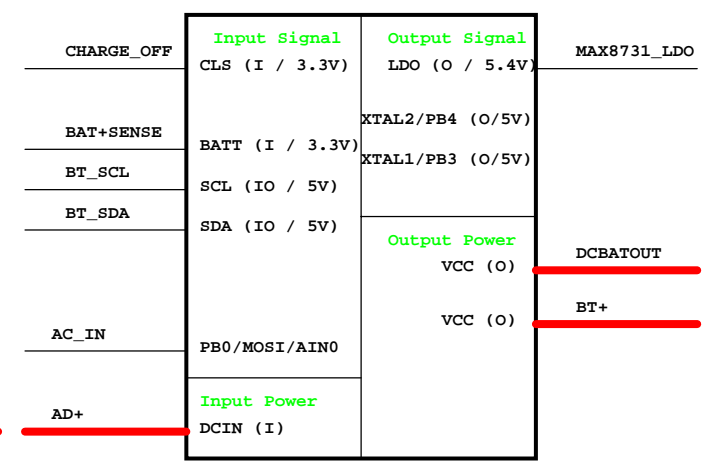
**G9131**  
**1D25V\_S0**



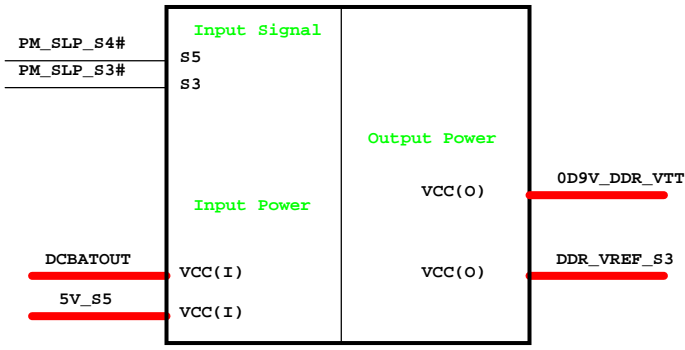
**Adapter**



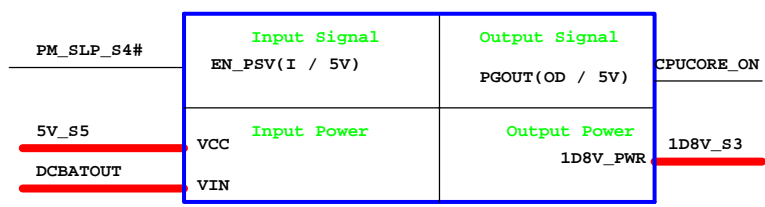
**Charger\_MAX8731A**



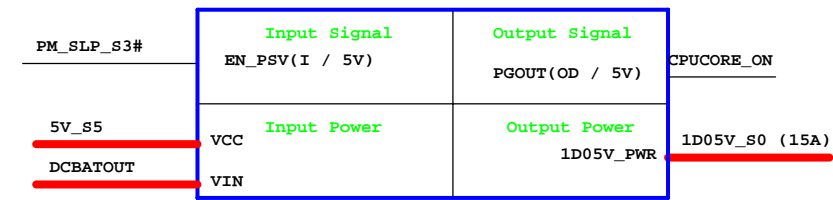
**TI TPS51100**  
**0.9V/DDR\_VREF\_S3**



**TPS51117\_1D8V\_S3**



**TPS51117\_1D05V**



<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size: A3 Document Number: **DS2-Intel** Rev: **-1**

Date: Wednesday, September 12, 2007 Sheet 2 of 47

# INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIe Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIe LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVPtp3	AZ DOUT ICH	Description	RSVD
0	0	Enter XOR Chain	
1	1	Normal Operation(default)	
1	1	Set PCIe port cofig bit1	

A16 swap override strap	
PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	DCT
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5	
SM_INTVRMEN	High=Enable Low=Disable
Integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

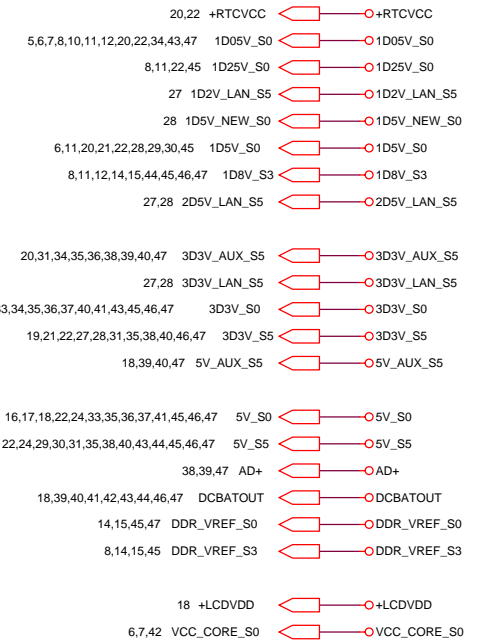
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

# INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

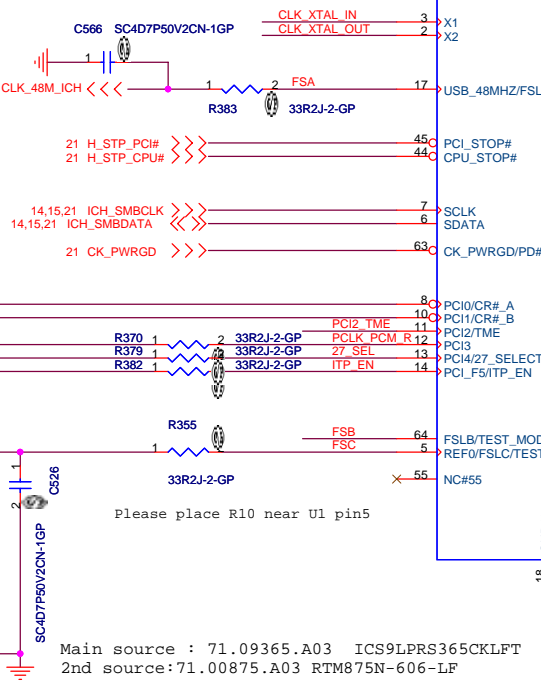
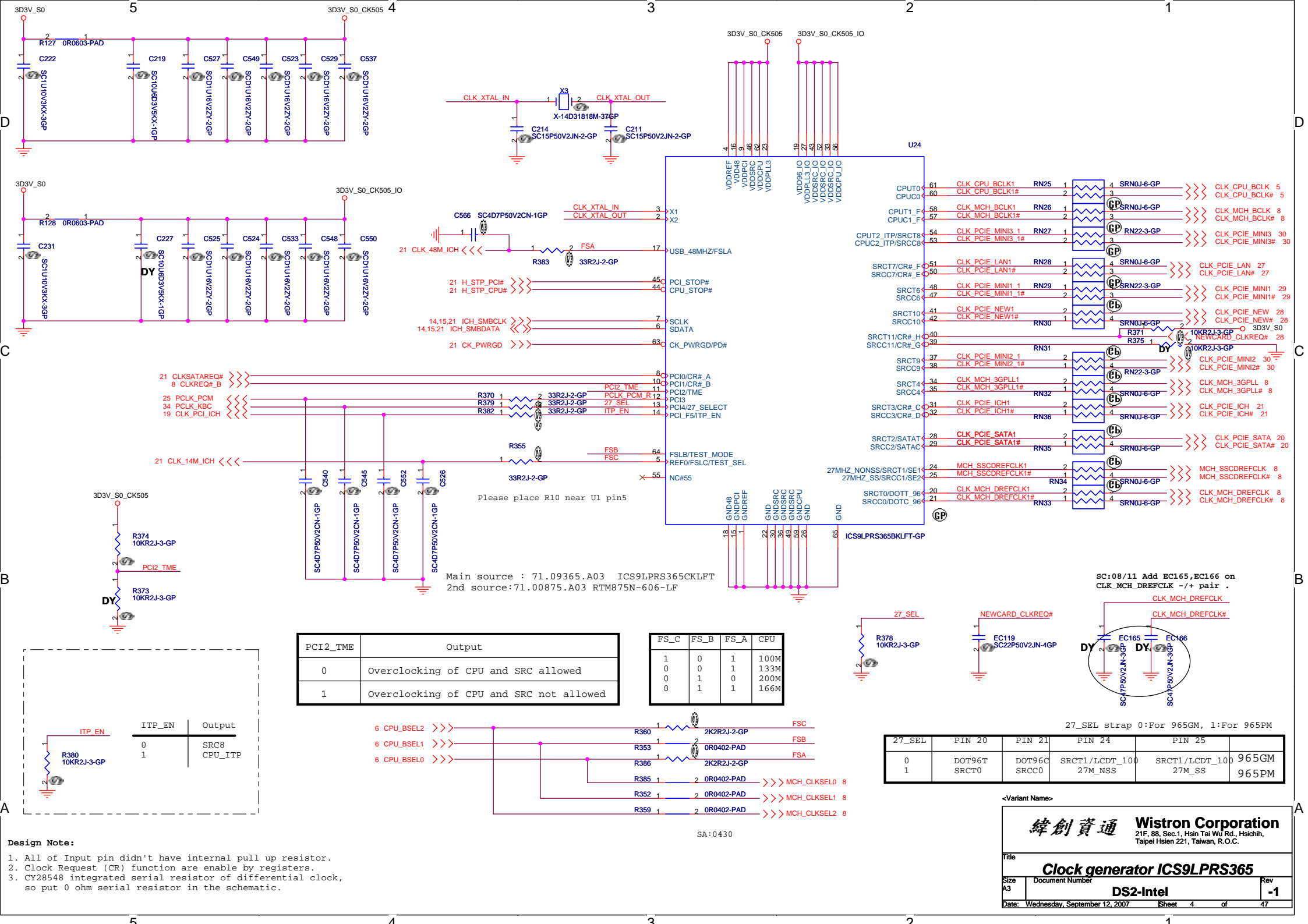


# INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 8 Low Power PCI Express	Normal	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled
CFG 19 DMI Lane Reserved	Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIe	Only PCIe or SDVO is operation	PCIe and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13	Reserved	
LL(00)	Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HH(11)	Normal Operation	

<Core Design>

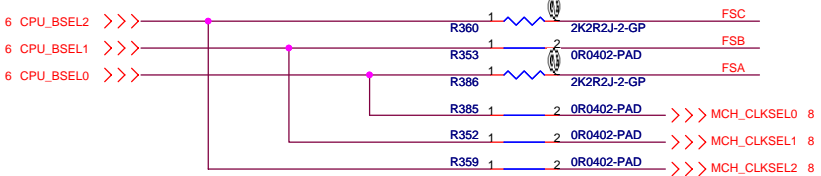
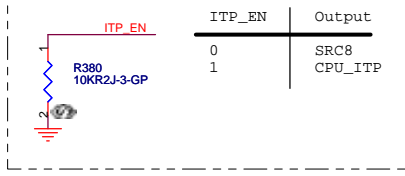
<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
<b>Table of Content</b>		
Size A3	Document Number	Rev
	<b>DS2-Intel</b>	<b>-1</b>
Date: Wednesday, September 12, 2007		
	Sheet 3	of 47



Main source : 71.09365.A03 ICS9LPRS365CKLFT  
 2nd source:71.00875.A03 RTM875N-606-LF

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M



27\_SEL strap 0:For 965GM, 1:For 965PM

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25	
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100	965GM
1		SRCC0	27M_NSS	27M_SS	965PM

Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

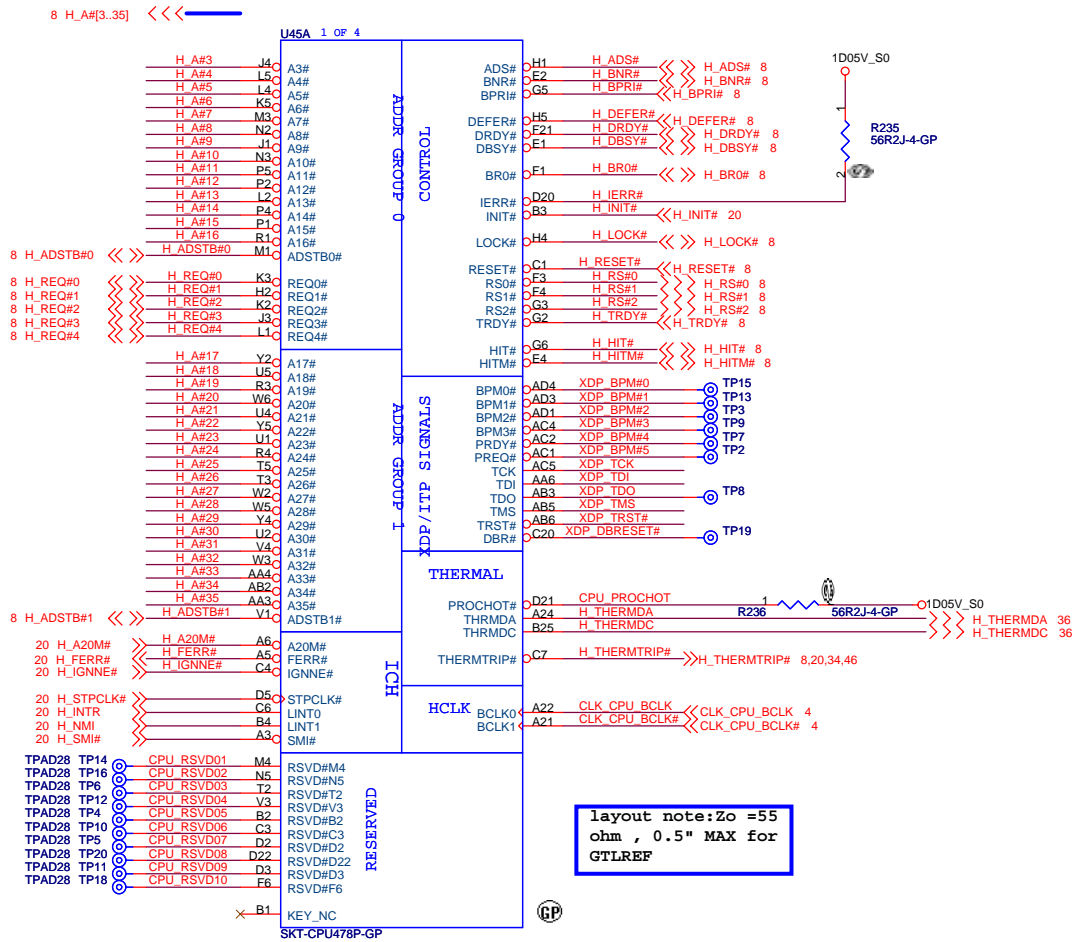
**Clock generator ICS9LPRS365**

SA:0430

Document Number: **DS2-Intel**  
 Rev: **-1**

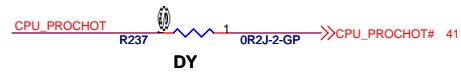
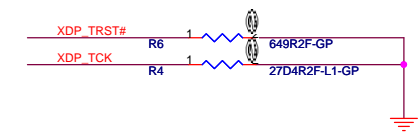
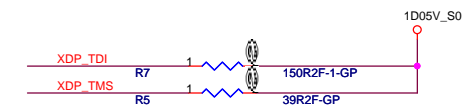
Date: Wednesday, September 12, 2007 Sheet 4 of 47

- Design Note:**
- All of Input pin didn't have internal pull up resistor.
  - Clock Request (CR) function are enable by registers.
  - CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.



H\_THERMDA, H\_THERMDC routing together,  
Trace width / Spacing = 10 / 10 mil

layout note: Zo = 55  
ohm , 0.5" MAX for  
GTLREF



<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**Meron(1/3)-AGTL+/XDP**

Size A3 Document Number DS2-Intel Rev -1

Date: Wednesday, September 12, 2007 Sheet 5 of 47

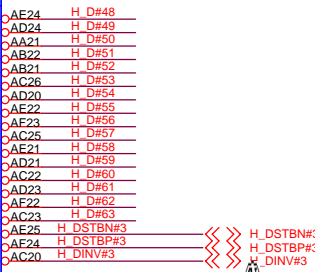
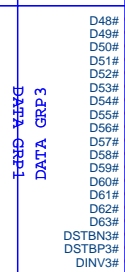
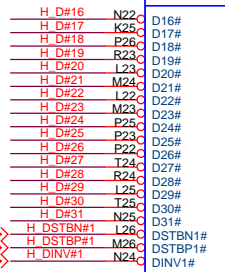
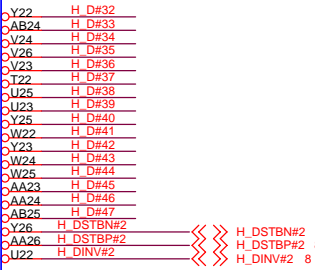
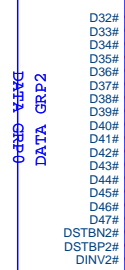
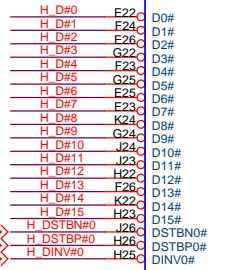
8 H\_D# [0..63] <<>>

8 H\_DSTBN#0 <<>>  
8 H\_DSTBP#0 <<>>  
8 H\_DINV#0 <<>>

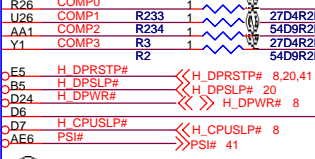
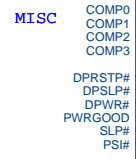
8 H\_DSTBN#1 <<>>  
8 H\_DSTBP#1 <<>>  
8 H\_DINV#1 <<>>

4 CPU\_BSEL0 <<>>  
4 CPU\_BSEL1 <<>>  
4 CPU\_BSEL2 <<>>

U45B 2 OF 4

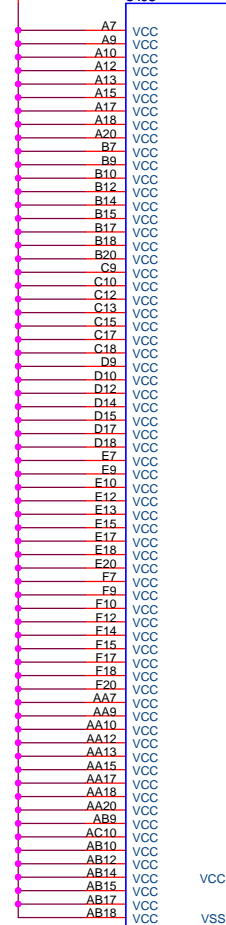


SKT-CPU478P-GP

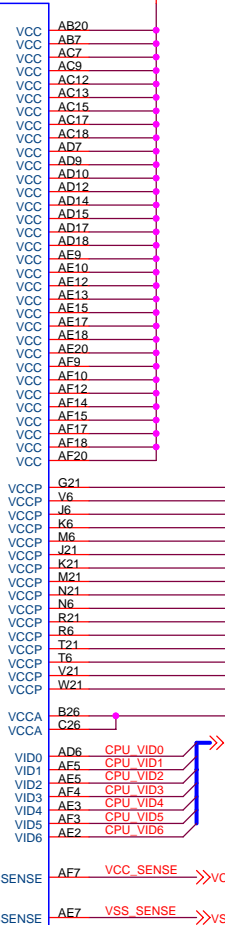


VCC\_CORE\_S0

U45C 3 OF 4



VCC\_CORE\_S0



1D05V\_S0

C20 SC10U6D3V5KX-1GP

1D5V\_S0

C394 SC10U6D3V5KX-3GP

C397 SC10U6D3V5KX-1GP

layout note:  
place C3 near  
PIN B26

Length match within  
25 mils . The trace  
width/space/other is  
20/7/25 .

SKT-CPU478P-GP

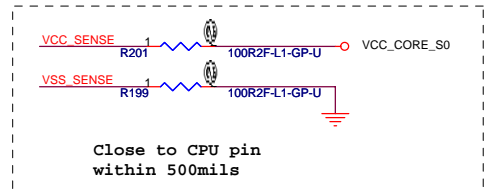
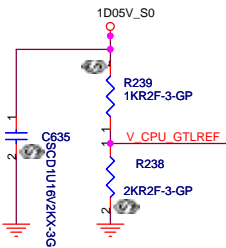
PLACE C25 close to the TEST4 PIN,  
make sure TEST3,TEST4,TEST5 trace  
routing is reference to GND and  
away other noisy signals

Resistor Placed  
within 0.5" of CPU  
pin. Trace should  
be at least 25 mils  
away from any other  
toggling signal .  
COMP[0,2] trace  
width is 18 mils.  
COMP[1,3] trace  
width is 4 mils .

Close to CPU  
pin AD26  
Z0=55 ohm  
with in  
500mils .

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Place C635 near  
R238 and R239



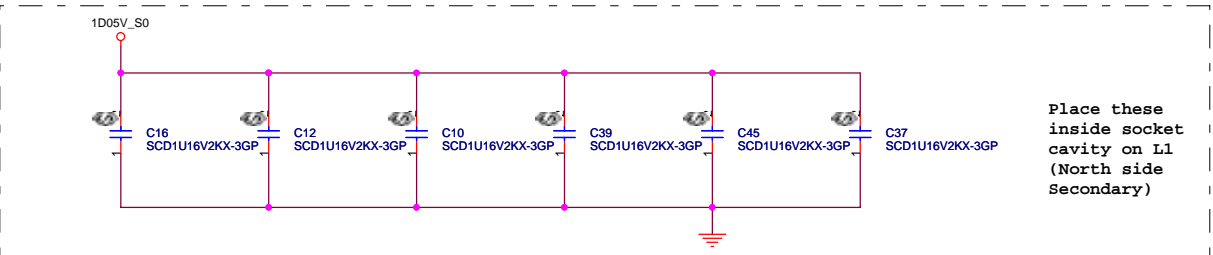
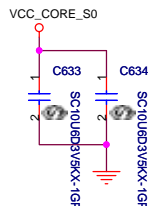
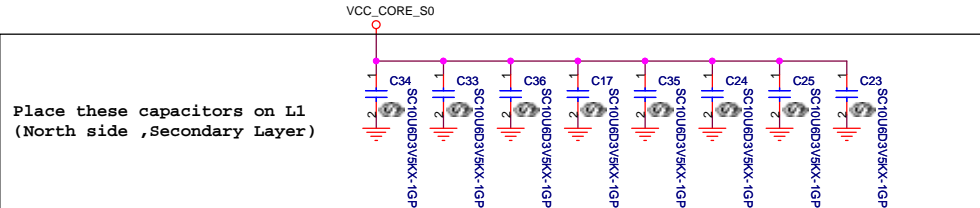
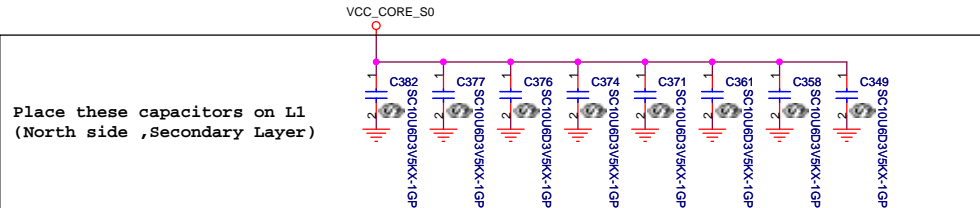
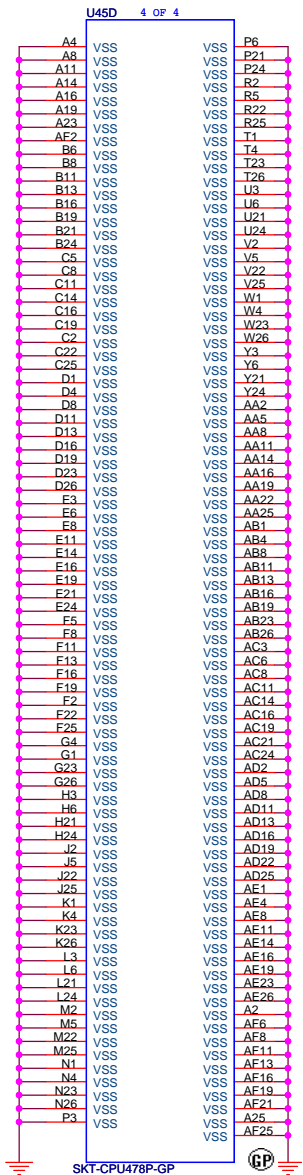
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

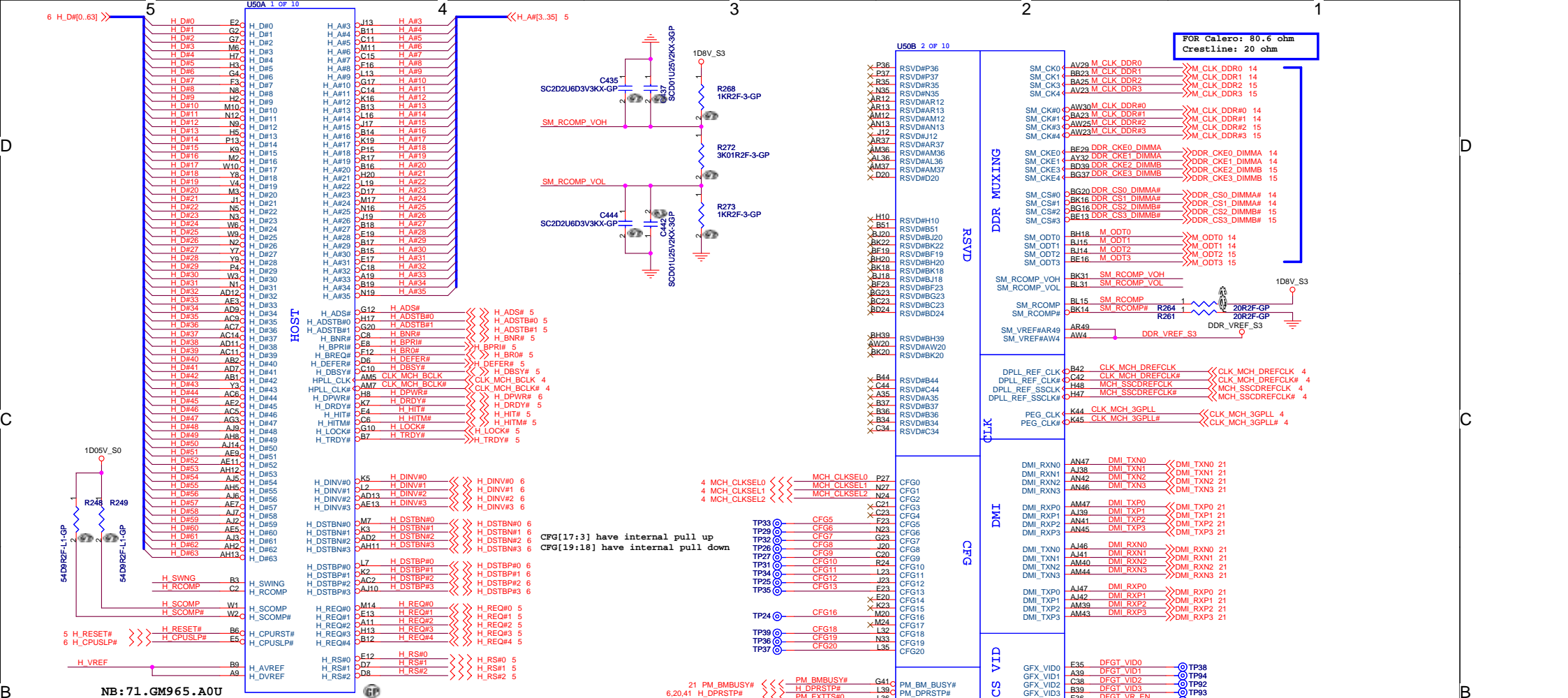
Title: **Meron(2/3)-AGTL+/PWR**

Size A3 Document Number **DS2-Intel** Rev **-1**

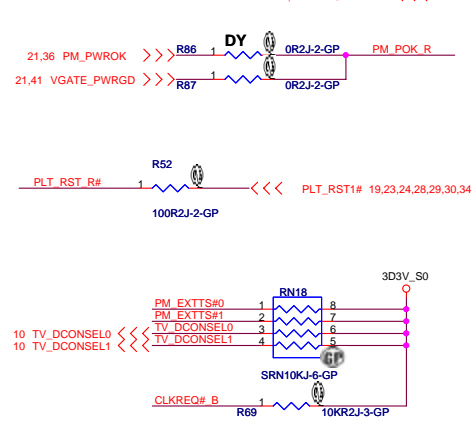
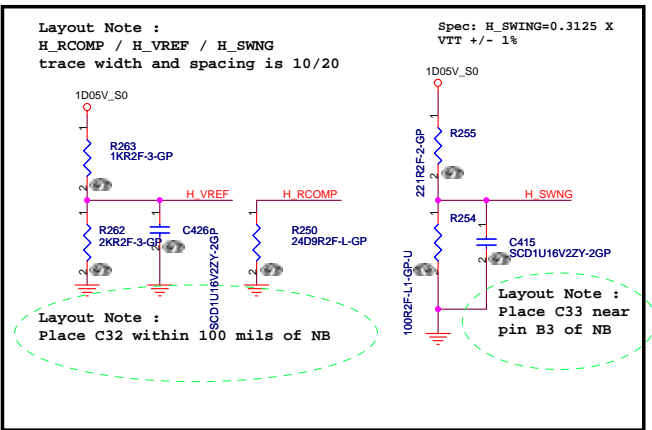
Date: Wednesday, September 12, 2007 Sheet 6 of 47







Layout note :  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



<Core Design>

**緯創資通** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRESTLINE(1/6)-AGTL+/DMI/DDR2**

Size: Custom Document Number: **DS2-Intel** Rev: **-1**

Date: Wednesday, September 12, 2007 Sheet: **g** of **47**



<< >> DDR\_A\_D[0..63] 14  
 << >> DDR\_A\_BS[0..2] 14  
 << >> DDR\_A\_DM[0..7] 14  
 << >> DDR\_A\_DQS[0..7] 14  
 << >> DDR\_A\_DQS#[0..7] 14  
 << >> DDR\_A\_MA[0..14] 14

<< >> DDR\_B\_D[0..63] 15  
 << >> DDR\_B\_BS[0..2] 15  
 << >> DDR\_B\_DM[0..7] 15  
 << >> DDR\_B\_DQS[0..7] 15  
 << >> DDR\_B\_DQS#[0..7] 15  
 << >> DDR\_B\_MA[0..14] 15

U50D 4 OF 10

DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS# >>> DDR_A_CAS# 14
DDR A D5	AR45	SA_DQ5			
DDR A D6	AT42	SA_DM0	AT45	DDR A DM0	
DDR A D7	AW47	SA_DM1	BD44	DDR A DM1	
DDR A D8	BB45	SA_DM2	BD42	DDR A DM2	
DDR A D9	BF48	SA_DM3	AW38	DDR A DM3	
DDR A D10	BG47	SA_DM4	AW13	DDR A DM4	
DDR A D11	BJ45	SA_DM5	BG8	DDR A DM5	
DDR A D12	BB47	SA_DM6	AY5	DDR A DM6	
DDR A D13	BG50	SA_DM7	AN6	DDR A DM7	
DDR A D14	BH49	SA_DQ14			
DDR A D15	BE45	SA_DQ15	AT46	DDR A DQS0	
DDR A D16	AW43	SA_DQ16	BE48	DDR A DQS1	
DDR A D17	BE44	SA_DQ17	BE43	DDR A DQS2	
DDR A D18	BG42	SA_DQ18	BC37	DDR A DQS3	
DDR A D19	BE40	SA_DQ19	BB16	DDR A DQS4	
DDR A D20	BF44	SA_DQ20	BH6	DDR A DQS5	
DDR A D21	BH45	SA_DQ21	BB2	DDR A DQS6	
DDR A D22	BG40	SA_DQ22	AP3	DDR A DQS7	
DDR A D23	BF40	SA_DQ23	AT47	DDR A DQS8	
DDR A D24	AR40	SA_DQ24	BD47	DDR A DQS9	
DDR A D25	AW40	SA_DQ25	BC41	DDR A DQS10	
DDR A D26	AT39	SA_DQ26	BA37	DDR A DQS11	
DDR A D27	AW36	SA_DQ27	BA16	DDR A DQS12	
DDR A D28	AW41	SA_DQ28	BH7	DDR A DQS13	
DDR A D29	AY41	SA_DQ29	BC1	DDR A DQS14	
DDR A D30	AY38	SA_DQ30	AF2	DDR A DQS15	
DDR A D31	AT38	SA_DQ31			
DDR A D32	AV13	SA_DQ32	BJ19	DDR A MA0	
DDR A D33	AT13	SA_DQ33	BD20	DDR A MA1	
DDR A D34	AW11	SA_DQ34	BK27	DDR A MA2	
DDR A D35	AV11	SA_DQ35	BH28	DDR A MA3	
DDR A D36	AU15	SA_DQ36	BL24	DDR A MA4	
DDR A D37	AT11	SA_DQ37	BK28	DDR A MA5	
DDR A D38	BA13	SA_DQ38	BJ27	DDR A MA6	
DDR A D39	BA11	SA_DQ39	BJ25	DDR A MA7	
DDR A D40	BE10	SA_DQ40	BL28	DDR A MA8	
DDR A D41	BD10	SA_DQ41	BA28	DDR A MA9	
DDR A D42	BD8	SA_DQ42	BC19	DDR A MA10	
DDR A D43	AY9	SA_DQ43	BE28	DDR A MA11	
DDR A D44	BG10	SA_DQ44	BG30	DDR A MA12	
DDR A D45	AW9	SA_DQ45	BJ16	DDR A MA13	
DDR A D46	BD7	SA_DQ46	BJ29	DDR A MA14	
DDR A D47	BB9	SA_DQ47			
DDR A D48	BB5	SA_DQ48	BE18	DDR A RAS# >>> DDR_A_RAS# 14	
DDR A D49	AY7	SA_DQ49	AY20	SA_RCVEN# TP30	
DDR A D50	AT5	SA_DQ50			
DDR A D51	AT7	SA_DQ51	BA19	DDR A WE# >>> DDR_A_WE# 14	
DDR A D52	AY6	SA_DQ52			
DDR A D53	BB7	SA_DQ53			
DDR A D54	AR5	SA_DQ54			
DDR A D55	AR8	SA_DQ55			
DDR A D56	AR9	SA_DQ56			
DDR A D57	AN3	SA_DQ57			
DDR A D58	AM8	SA_DQ58			
DDR A D59	AN10	SA_DQ59			
DDR A D60	AT9	SA_DQ60			
DDR A D61	AN9	SA_DQ61			
DDR A D62	AM9	SA_DQ62			
DDR A D63	AN11	SA_DQ63			

CRESTLINE-GP-U-NF  
NB: 71.GM965.A0U

U50E 5 OF 10

DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AW51	SB_DQ3			
DDR B D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR B CAS# >>> DDR_B_CAS# 15
DDR B D5	AN50	SB_DQ5			
DDR B D6	AV50	SB_DM0	AR50	DDR B DM0	
DDR B D7	AV49	SB_DM1	BD49	DDR B DM1	
DDR B D8	BA50	SB_DM2	BK45	DDR B DM2	
DDR B D9	BB50	SB_DM3	BL39	DDR B DM3	
DDR B D10	BA49	SB_DM4	BH12	DDR B DM4	
DDR B D11	BE50	SB_DM5	BH7	DDR B DM5	
DDR B D12	BA51	SB_DM6	BF3	DDR B DM6	
DDR B D13	AY49	SB_DM7	AW2	DDR B DM7	
DDR B D14	BF50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	AT50	DDR B DQS0	
DDR B D16	BJ50	SB_DQ16	BD50	DDR B DQS1	
DDR B D17	BJ44	SB_DQ17	BK46	DDR B DQS2	
DDR B D18	BJ43	SB_DQ18	BK39	DDR B DQS3	
DDR B D19	BL43	SB_DQ19	BJ12	DDR B DQS4	
DDR B D20	BK47	SB_DQ20	BL7	DDR B DQS5	
DDR B D21	BK49	SB_DQ21	BE2	DDR B DQS6	
DDR B D22	BK43	SB_DQ22	AV2	DDR B DQS7	
DDR B D23	BK42	SB_DQ23	AJ50	DDR B DQS8	
DDR B D24	BJ41	SB_DQ24	BC50	DDR B DQS9	
DDR B D25	BL41	SB_DQ25	BL45	DDR B DQS10	
DDR B D26	BJ37	SB_DQ26	BK38	DDR B DQS11	
DDR B D27	BJ36	SB_DQ27	BK12	DDR B DQS12	
DDR B D28	BK41	SB_DQ28	BK7	DDR B DQS13	
DDR B D29	BJ40	SB_DQ29	BE2	DDR B DQS14	
DDR B D30	BL35	SB_DQ30	AV3	DDR B DQS15	
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	BC18	DDR B MA0	
DDR B D33	BE11	SB_DQ33	BG28	DDR B MA1	
DDR B D34	BK11	SB_DQ34	BG25	DDR B MA2	
DDR B D35	BC11	SB_DQ35	AW17	DDR B MA3	
DDR B D36	BC13	SB_DQ36	BE25	DDR B MA4	
DDR B D37	BE12	SB_DQ37	BE25	DDR B MA5	
DDR B D38	BC12	SB_DQ38	BA29	DDR B MA6	
DDR B D39	BG12	SB_DQ39	BC28	DDR B MA7	
DDR B D40	BJ10	SB_DQ40	AY28	DDR B MA8	
DDR B D41	BL9	SB_DQ41	BD37	DDR B MA9	
DDR B D42	BK5	SB_DQ42	BG17	DDR B MA10	
DDR B D43	BL5	SB_DQ43	BE37	DDR B MA11	
DDR B D44	BK9	SB_DQ44	BA39	DDR B MA12	
DDR B D45	BK10	SB_DQ45	BG13	DDR B MA13	
DDR B D46	BJ8	SB_DQ46	BE24	DDR B MA14	
DDR B D47	BJ6	SB_DQ47			
DDR B D48	BF4	SB_DQ48	AV16	DDR B RAS# >>> DDR_B_RAS# 15	
DDR B D49	BH5	SB_DQ49	AY18	SB_RCVEN# TP28	
DDR B D50	BC1	SB_DQ50			
DDR B D51	BC2	SB_DQ51	BC17	DDR B WE# >>> DDR_B_WE# 15	
DDR B D52	BK3	SB_DQ52			
DDR B D53	BE4	SB_DQ53			
DDR B D54	BD3	SB_DQ54			
DDR B D55	BJ2	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AR1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AU2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

CRESTLINE-GP-U-NF  
NB: 71.GM965.A0U

<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>CRESTLINE(2/6)-DDR2 A/B CH</b>			
Size	Document Number	Rev	
A3		-1	
<b>DS2-Intel</b>			
Date:	Wednesday, September 12, 2007	Sheet	9 of 47

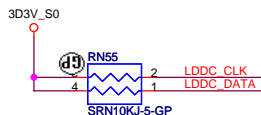
For Crestline : 2.4 Kohm  
For Calero : 1.5Kohm

D-1:0908 Chang R68 from  
64.24015.6DL to 64.33015.6DL

35 M\_COMP  
35 M\_LUMA  
35 M\_CRMA

17 M\_BLUE  
17 M\_GREEN  
17 M\_RED

17 GMCH\_DDCCLK  
17 GMCH\_DDCDATA  
17 GMCH\_VSYNC  
17 GMCH\_HSYNC



FOR Calero: 255 ohm  
Crestline: 1.3k ohm

CRESTLINE-GP-U/F  
NB: 71.GM965.A0U

1D05V\_S0

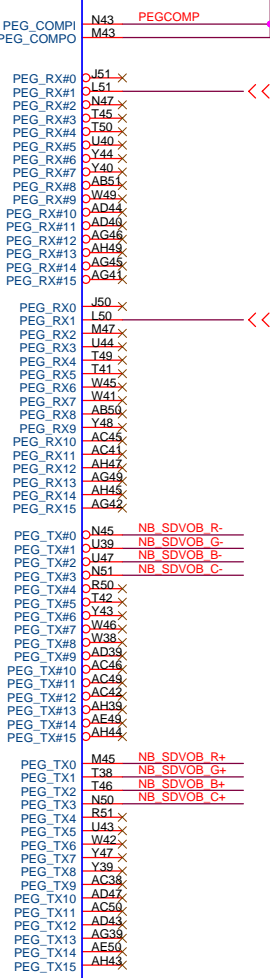
PEGCOMP trace  
width and spacing  
is 20/25 mils.

PCI\_EXPRESS GRAPHICS

LVDS

AL

VGA



### Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.



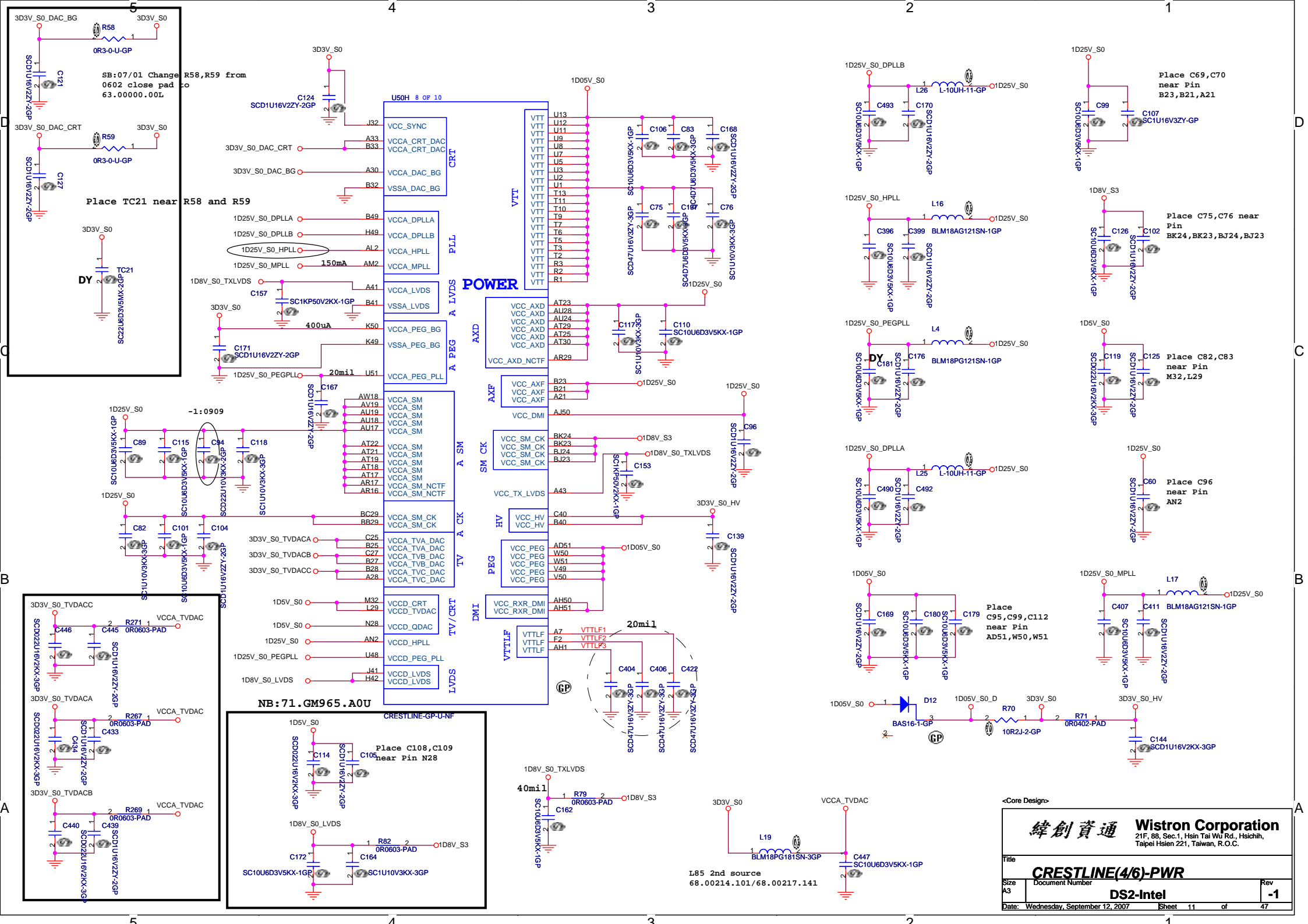
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRESTLINE(3/6)-VGA/LVDS/TV**

Size: A3 Document Number: **DS2-Intel** Rev: **-1**

Date: Wednesday, September 12, 2007 Sheet 10 of 47



SB:07/01 Change R58,R59 from 0602 to 0603 close pad to 63.00000.00L

Place TC21 near R58 and R59

150mA

400uA

-1:0909

NB: 71. GM965. A0U

CRESTLINE-GP-U-NF

<Core Design>

<b>緯創資通 Wistron Corporation</b>		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	<b>CRESTLINE(4/6)-PWR</b>	
Size	Document Number	Rev
A3		<b>-1</b>
Date:	Wednesday, September 12, 2007	Sheet 11 of 47

L85 2nd source 68.00214.101/68.00217.141

Place C82, C83 near Pin M32, L29

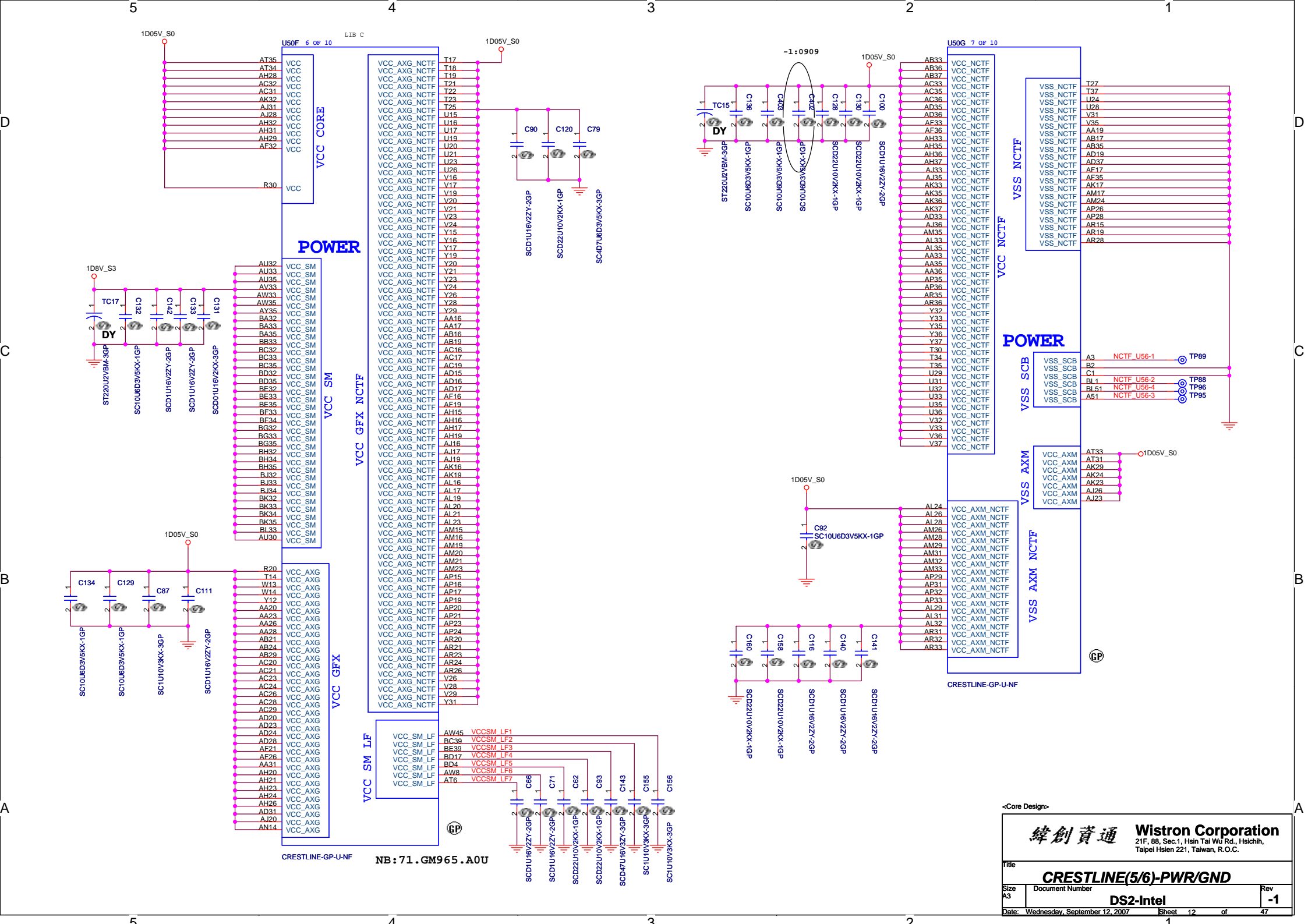
Place C95, C99, C112 near Pin AD51, W50, W51

Place C108, C109 near Pin N28

Place C60 near Pin AN2

Place C75, C76 near Pin BK24, BK23, BJ24, BJ23

Place C69, C70 near Pin B23, B21, A21



**POWER**

**POWER**

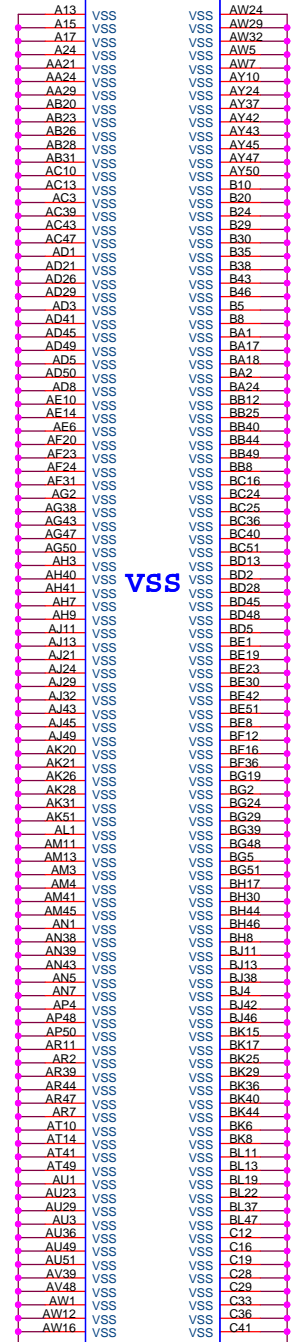
CRESTLINE-GP-U-NF NB: 71.GM965.A0U

<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

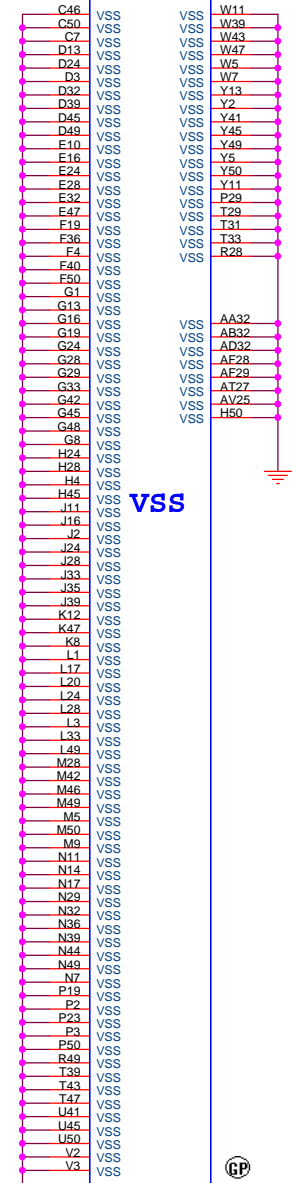
Title		
<b>CRESTLINE(5/6)-PWR/GND</b>		
Size	Document Number	Rev
A3	<b>DS2-Intel</b>	<b>-1</b>
Date: Wednesday, September 12, 2007		
Sheet 12 of 47		

U50I 9 OF 10



CRESTLINE-GP-U-NF  
NB: 71.GM965.A0U

U50J10 OF 10



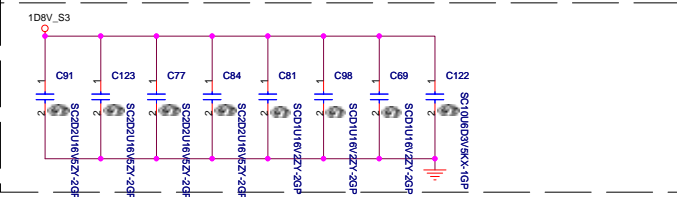
CRESTLINE-GP-U-NF  
NB: 71.GM965.A0U

<Core Design>

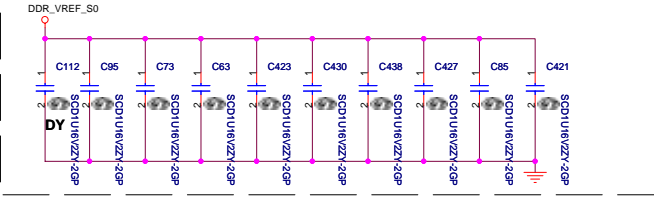
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CRESTLINE(6/6)-PWR/GND</b>			
Size A3 Document Number <b>DS2-Intel</b> Rev <b>-1</b>			
Date: Wednesday, September 12, 2007		Sheet 13 of 47	

- 9 DDR\_A\_DQS[0..7] <<>>
- 9 DDR\_A\_D[0..63] <<>>
- 9 DDR\_A\_DM[0..7] <<>>
- 9 DDR\_A\_DQS[0..7] <<>>
- 9 DDR\_A\_MA[0..14] <<>>
- 9 DDR\_A\_BS[0..2] <<>>

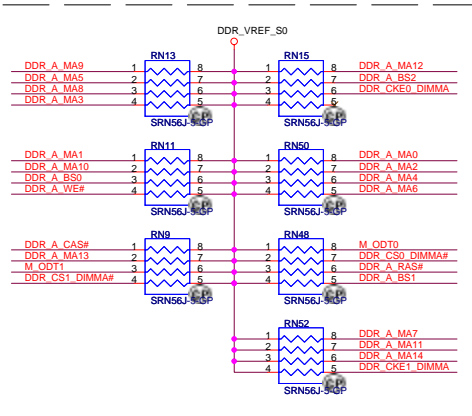
Layout Note:  
Place near DM1



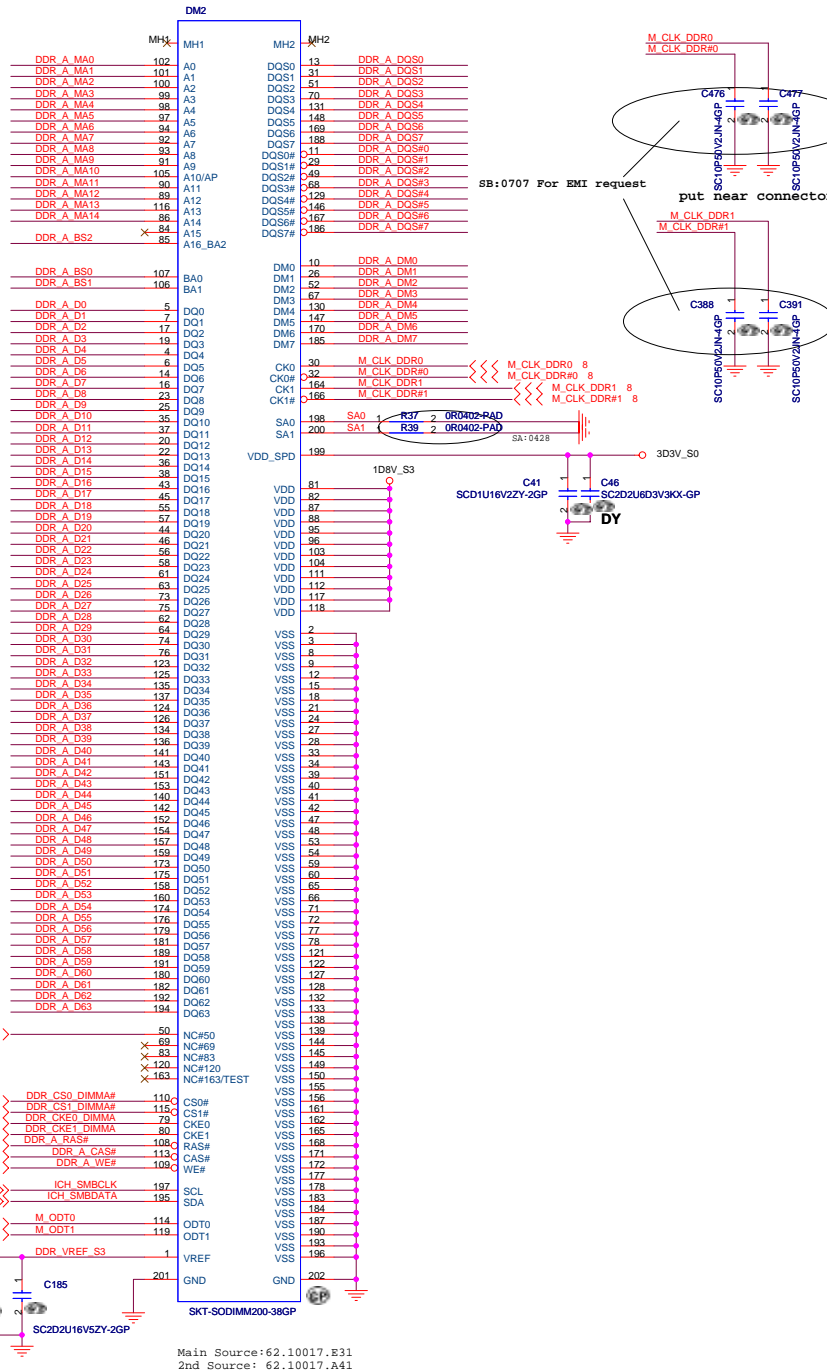
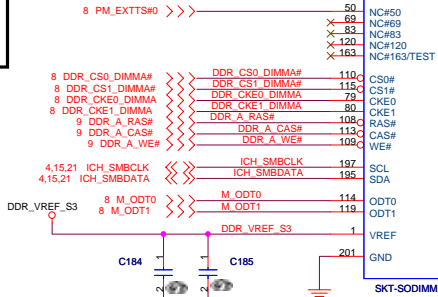
Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



change to 8P4R



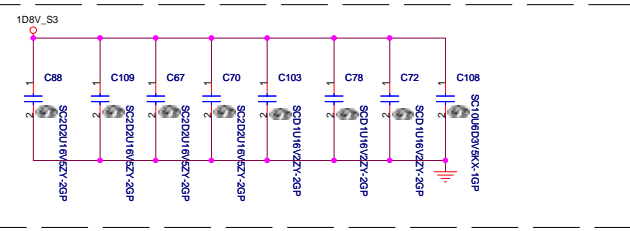
Layout Note:  
Place these resistors closely DM1, all trace length Max=1.5"



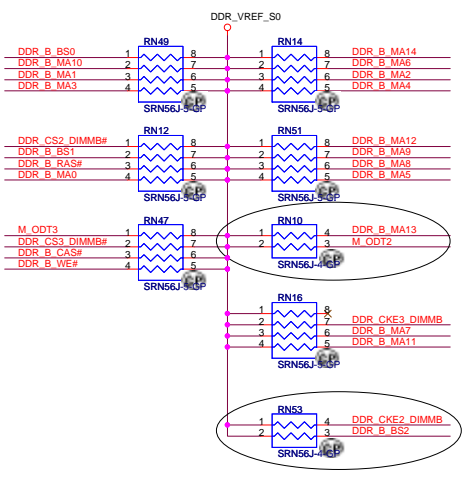
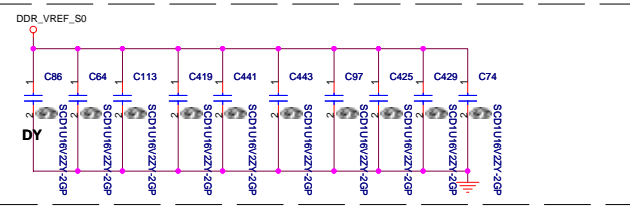


- 9 DDR\_B\_DQS#[0..7] <<<>>>
- 9 DDR\_B\_DQ[0..63] <<<>>>
- 9 DDR\_B\_DM[0..7] <<<>>>
- 9 DDR\_B\_DQS#[0..7] <<<>>>
- 9 DDR\_B\_MA[0..14] <<<>>>
- 9 DDR\_B\_BS[0..2] <<<>>>

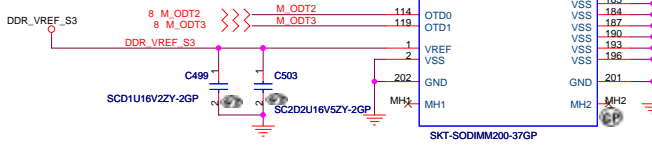
Layout Note:  
Place near DM2



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS

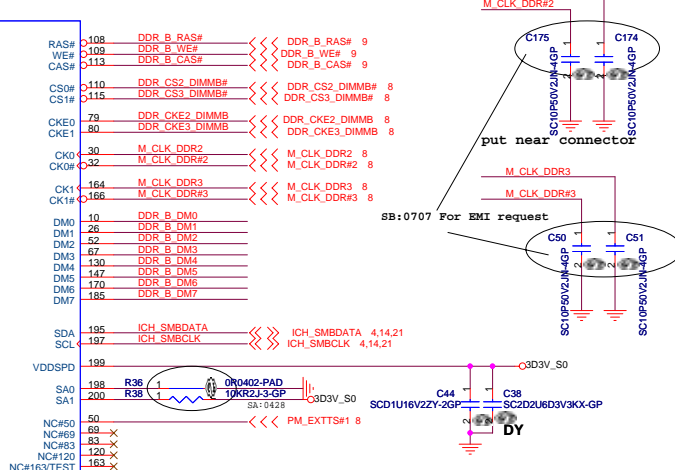


Layout Note:  
Place these resistors closely DM2, all trace length Max=1.5"



DDR_B_MA0	102	A0
DDR_B_MA1	101	A1
DDR_B_MA2	100	A2
DDR_B_MA3	99	A3
DDR_B_MA4	98	A4
DDR_B_MA5	97	A5
DDR_B_MA6	94	A6
DDR_B_MA7	92	A7
DDR_B_MA8	91	A8
DDR_B_MA9	91	A9
DDR_B_MA10	105	A10/AP
DDR_B_MA11	90	A11
DDR_B_MA12	90	A12
DDR_B_MA13	116	A13
DDR_B_MA14	86	A14
DDR_B_MA14	84	A14
DDR_B_MA14	85	A14
DDR_B_BS2	X	A16/BA2
DDR_B_BS0	107	BA0
DDR_B_BS1	106	BA1
DDR_B_D0	5	DO0
DDR_B_D1	7	DO1
DDR_B_D2	17	DO2
DDR_B_D3	15	DO3
DDR_B_D4	4	DO4
DDR_B_D5	6	DO5
DDR_B_D6	16	DO6
DDR_B_D7	16	DO7
DDR_B_D8	23	DO8
DDR_B_D9	25	DO9
DDR_B_D10	26	DO10
DDR_B_D11	37	DO11
DDR_B_D12	20	DO12
DDR_B_D13	22	DO13
DDR_B_D14	36	DO14
DDR_B_D15	38	DO15
DDR_B_D16	43	DO16
DDR_B_D17	45	DO17
DDR_B_D18	55	DO18
DDR_B_D19	57	DO19
DDR_B_D20	44	DO20
DDR_B_D21	46	DO21
DDR_B_D22	56	DO22
DDR_B_D23	58	DO23
DDR_B_D24	61	DO24
DDR_B_D25	63	DO25
DDR_B_D26	73	DO26
DDR_B_D27	75	DO27
DDR_B_D28	62	DO28
DDR_B_D29	64	DO29
DDR_B_D30	74	DO30
DDR_B_D31	76	DO31
DDR_B_D32	123	DO32
DDR_B_D33	125	DO33
DDR_B_D34	136	DO34
DDR_B_D35	137	DO35
DDR_B_D36	124	DO36
DDR_B_D37	126	DO37
DDR_B_D38	134	DO38
DDR_B_D39	138	DO39
DDR_B_D40	141	DO40
DDR_B_D41	143	DO41
DDR_B_D42	151	DO42
DDR_B_D43	153	DO43
DDR_B_D44	140	DO44
DDR_B_D45	142	DO45
DDR_B_D46	152	DO46
DDR_B_D47	154	DO47
DDR_B_D48	157	DO48
DDR_B_D49	159	DO49
DDR_B_D50	173	DO50
DDR_B_D51	175	DO51
DDR_B_D52	158	DO52
DDR_B_D53	160	DO53
DDR_B_D54	174	DO54
DDR_B_D55	176	DO55
DDR_B_D56	179	DO56
DDR_B_D57	181	DO57
DDR_B_D58	189	DO58
DDR_B_D59	191	DO59
DDR_B_D60	190	DO60
DDR_B_D61	182	DO61
DDR_B_D62	192	DO62
DDR_B_D63	194	DO63
DDR_B_DQS#0	11	DO64
DDR_B_DQS#1	29	DO65
DDR_B_DQS#2	49	DO66
DDR_B_DQS#3	68	DO67
DDR_B_DQS#4	120	DO68
DDR_B_DQS#5	146	DO69
DDR_B_DQS#6	167	DO70
DDR_B_DQS#7	186	DO71
DDR_B_DQS#0	13	DO72
DDR_B_DQS#1	31	DO73
DDR_B_DQS#2	51	DO74
DDR_B_DQS#3	70	DO75
DDR_B_DQS#4	131	DO76
DDR_B_DQS#5	148	DO77
DDR_B_DQS#6	169	DO78
DDR_B_DQS#7	188	DO79
DDR_B_DQS#0	114	DO80
DDR_B_DQS#1	119	DO81
M_ODT2	114	DO82
M_ODT3	119	DO83
VREF	2	DO84
VSS	202	DO85
GND	MH1	DO86
GND	MH2	DO87

Main Source: 62.10017.E21  
2nd Source: 62.10017.A51



put near connector

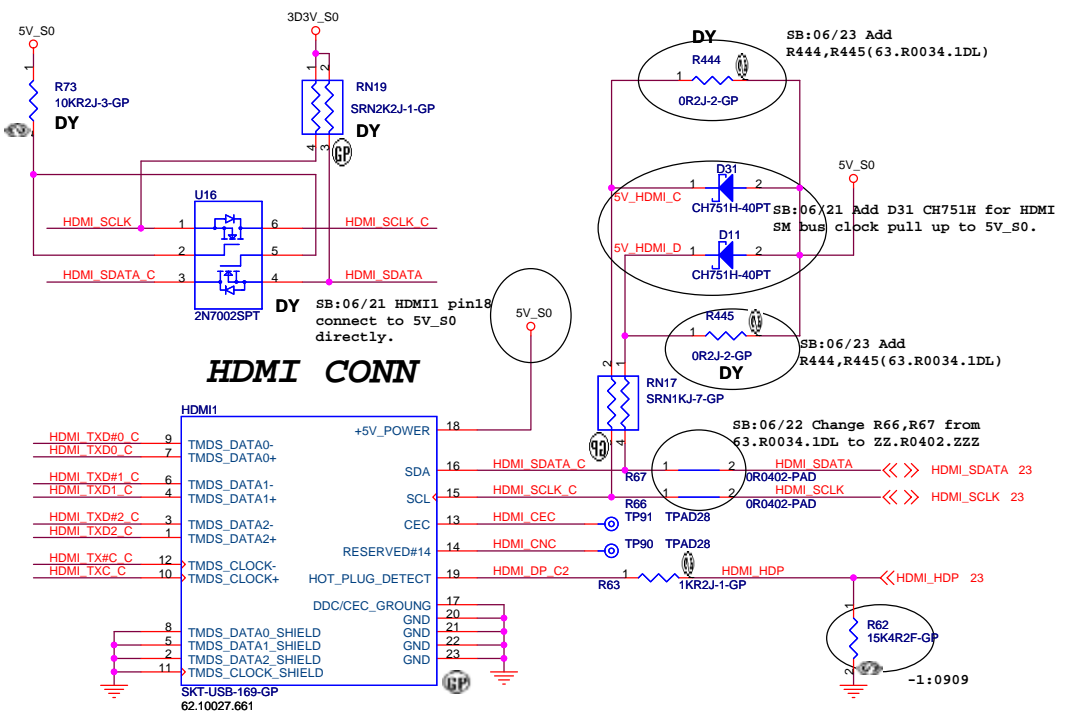
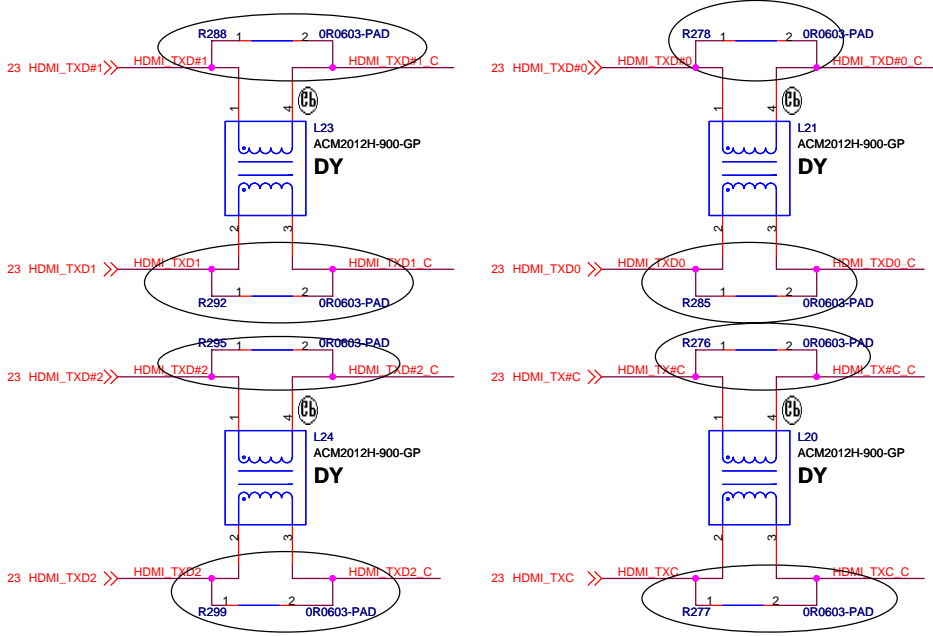
SB:0707 For EMI request

Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title: **DDR2-SODIMM SLOT2**

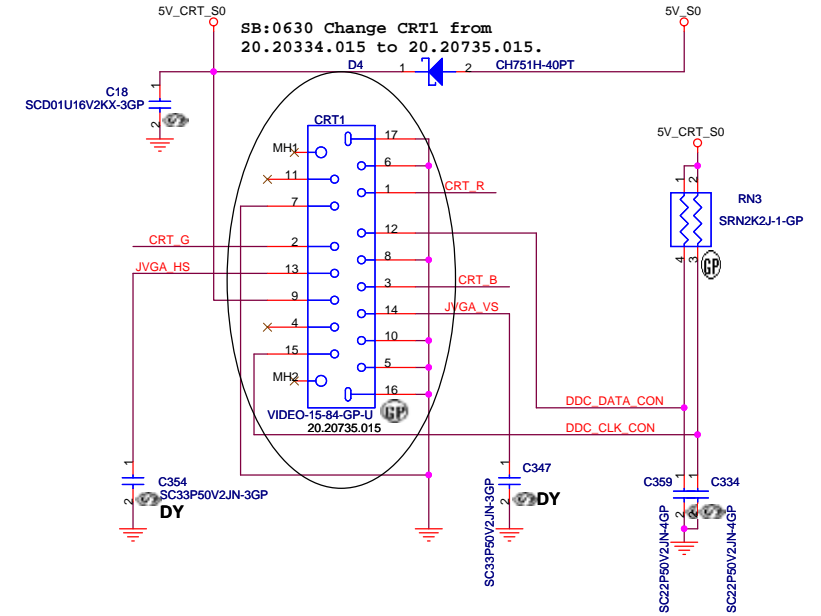
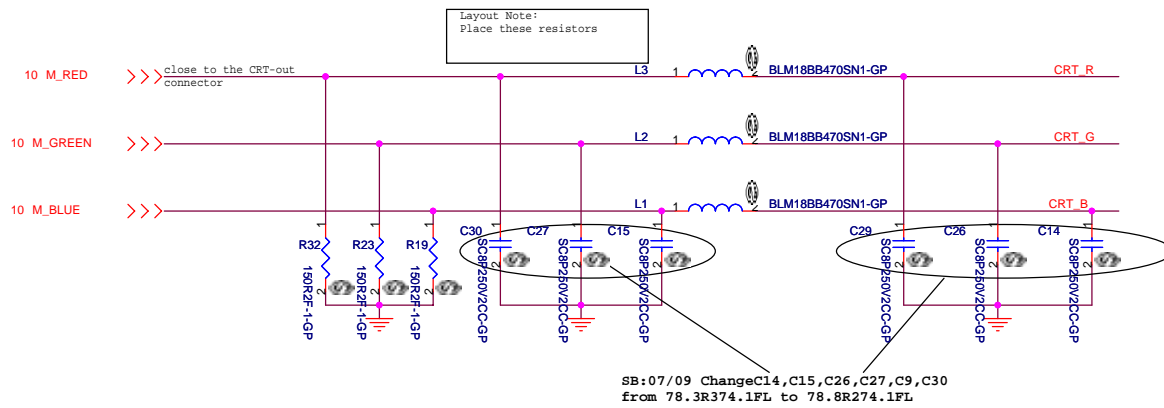
Size: Custom  
Document Number: **DS2-Intel**  
Date: Wednesday, September 12, 2007  
Sheet: 15 of 47  
Rev: **-1**

# HDMI I/F & CONNECTOR

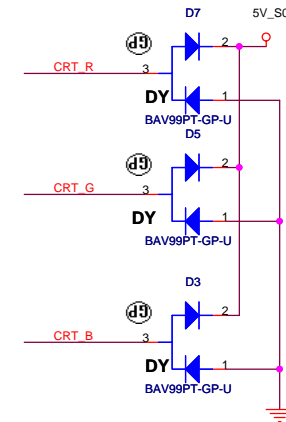
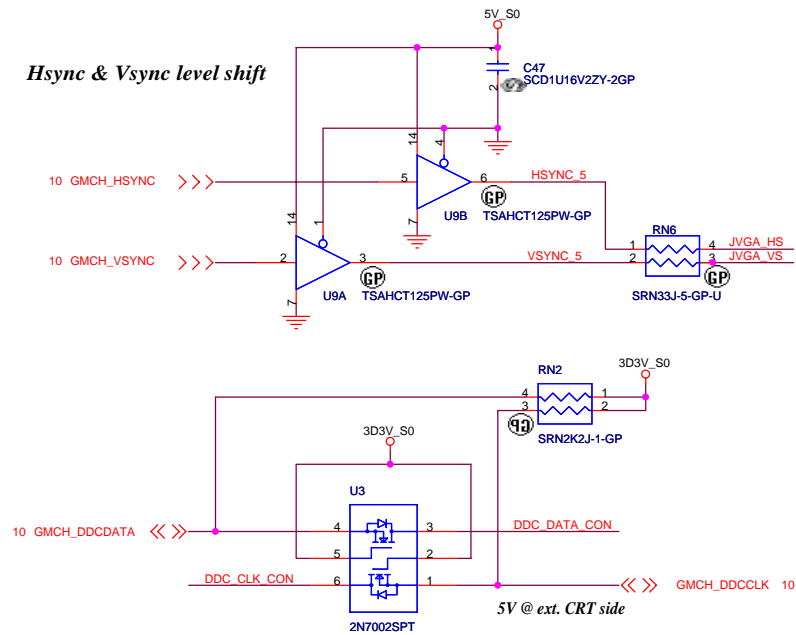


**TV OUT CONN (Optional) Move to Right I/O Board**

# CRT I/F & CONNECTOR



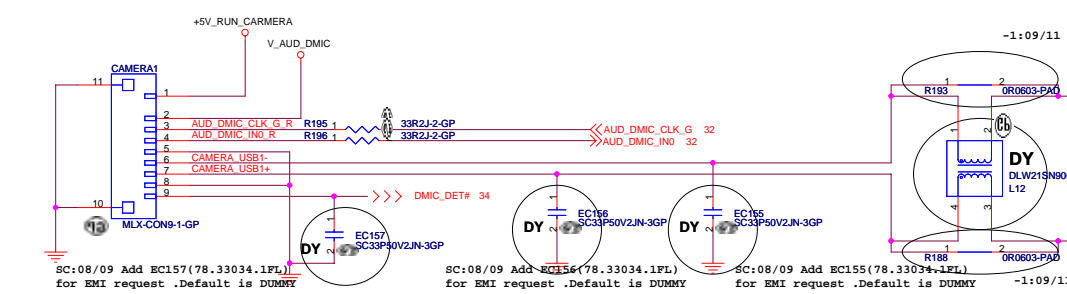
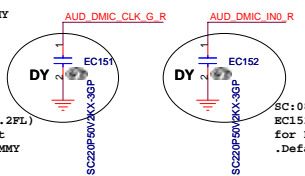
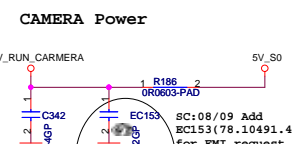
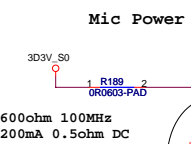
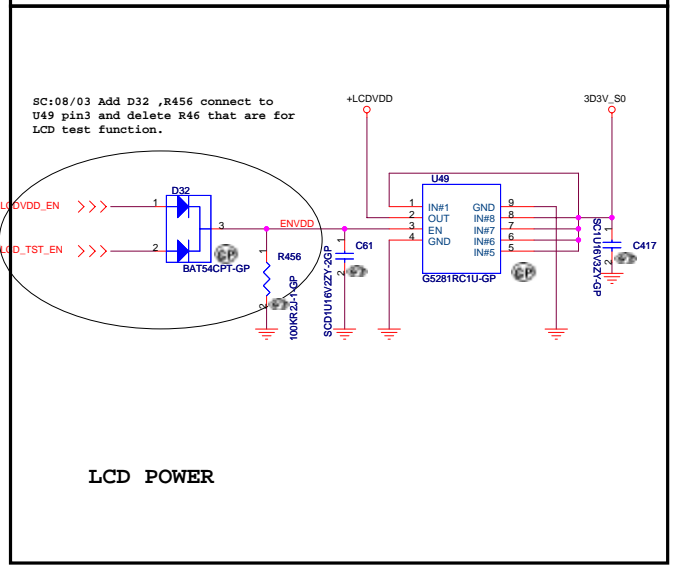
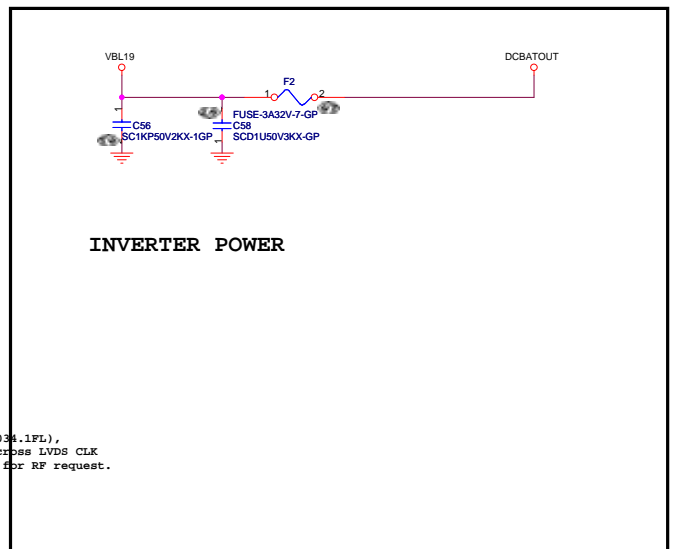
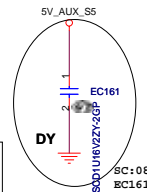
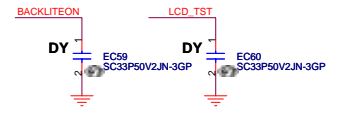
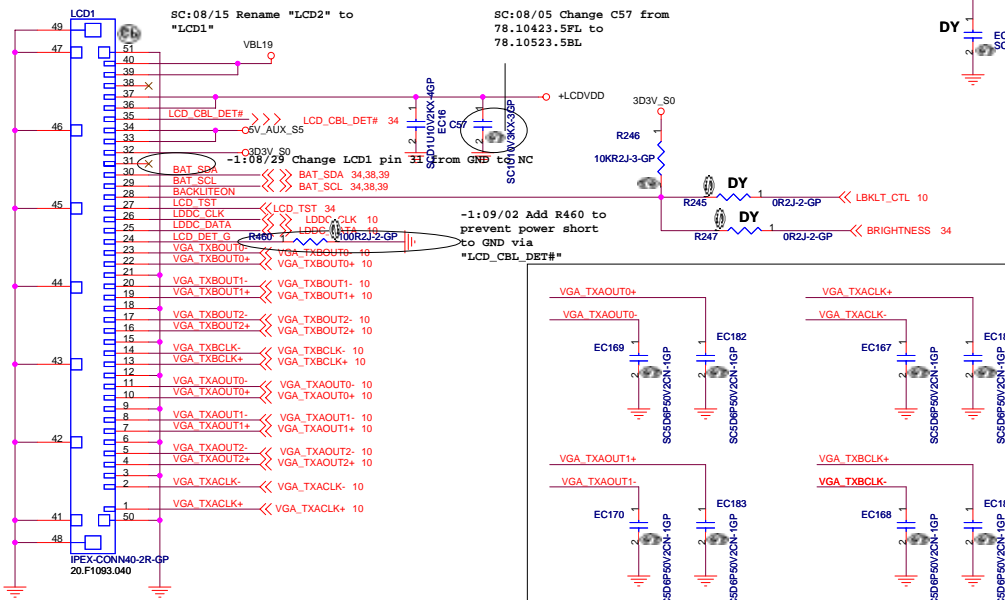
## Hsync & Vsync level shift

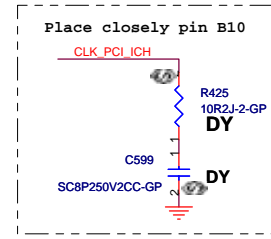
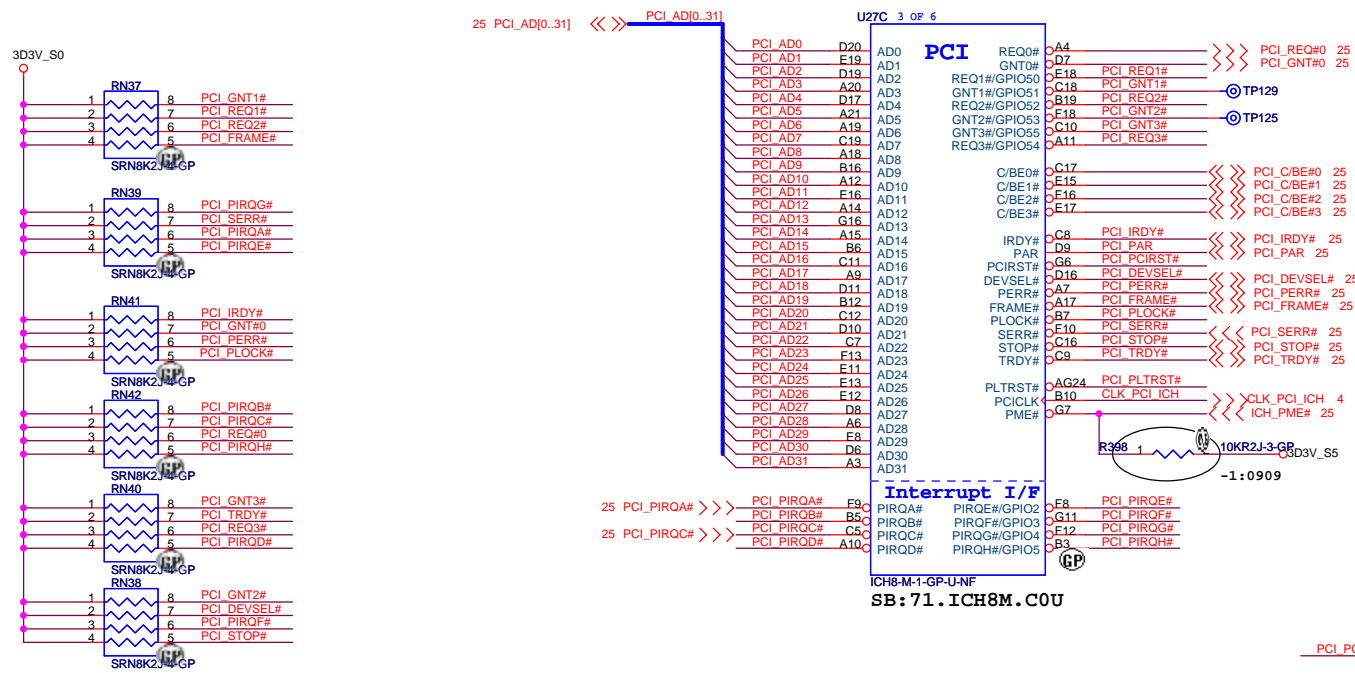


<Core Design>

<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b>CRT Connector</b>	
Size A3	Document Number
<b>DS2-Intel</b>	
Date: Wednesday, September 12, 2007	Sheet 17 of 47
Rev <b>-1</b>	

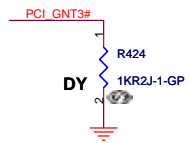
SC:08/09 Add LCD2 (20.F1093.04), please check LCD1 and LCD 2 layout overlap possibility.



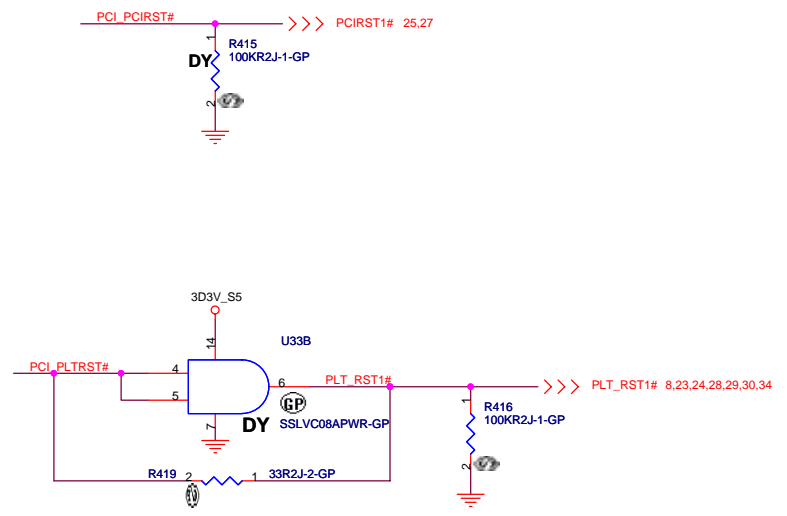


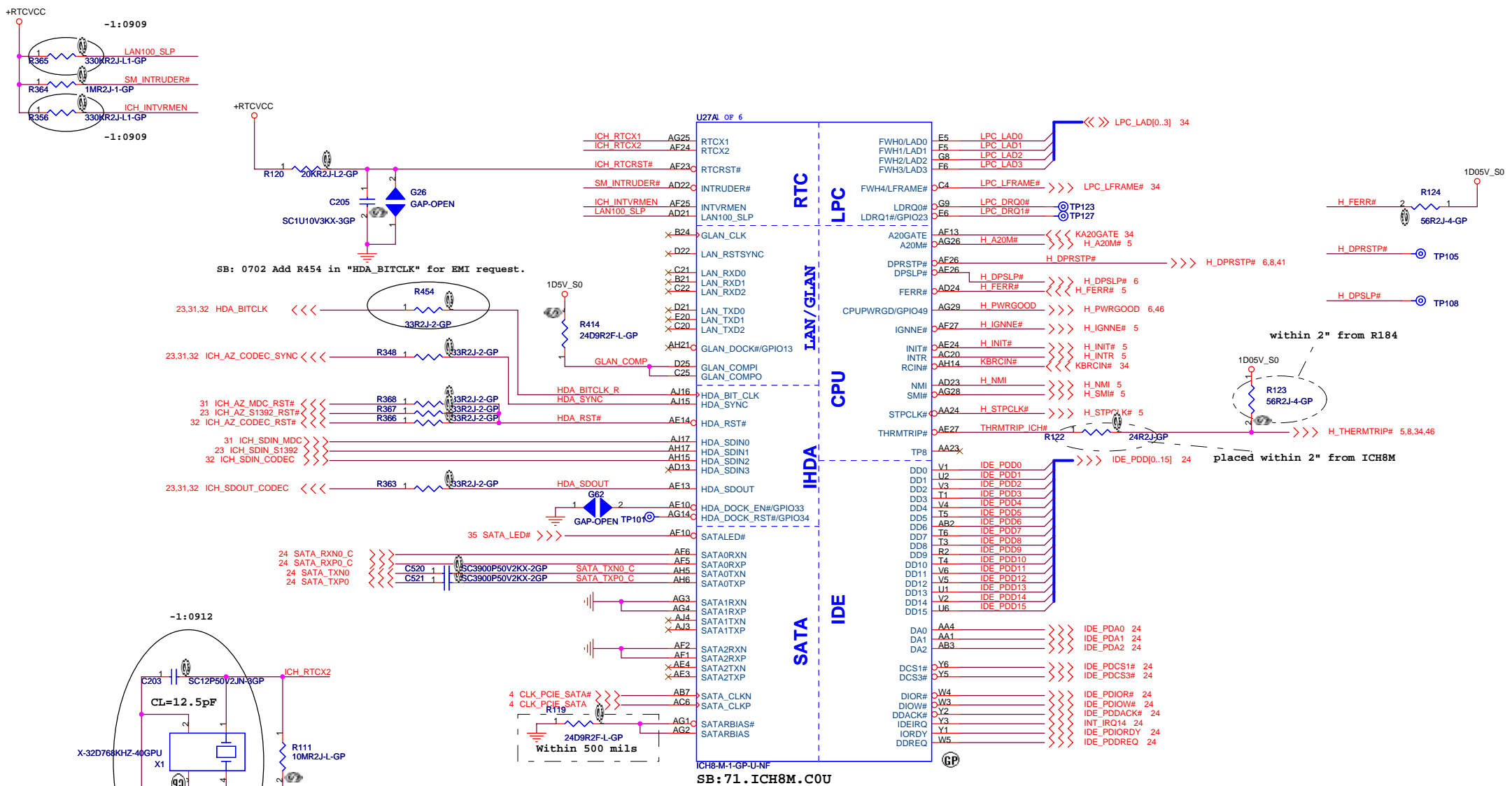
**Interrupt I/F**  
 ICH8-M-1-GP-U-NF  
 SB:71.ICH8M.CO0

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



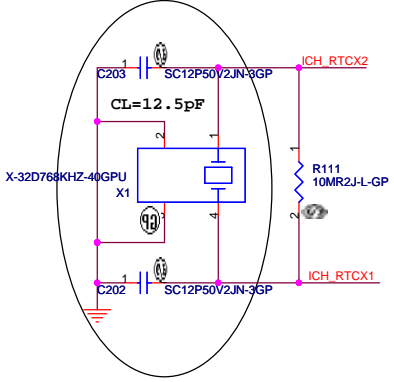
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



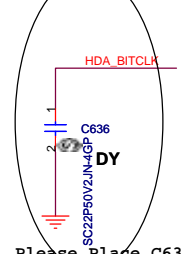


SB: 0702 Add R454 in "HDA\_BITCLK" for EMI request.

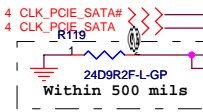
-1:0912



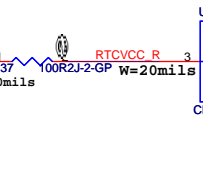
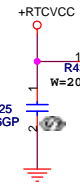
-1: 0904 change to DY



Please Place C636 near R454



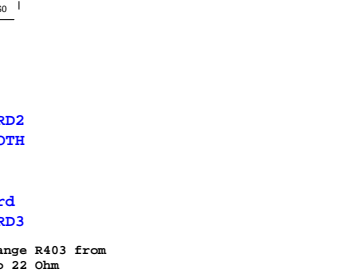
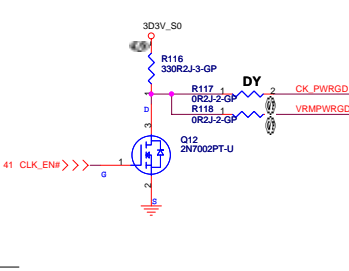
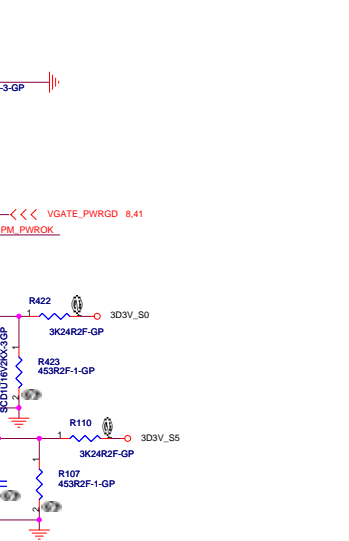
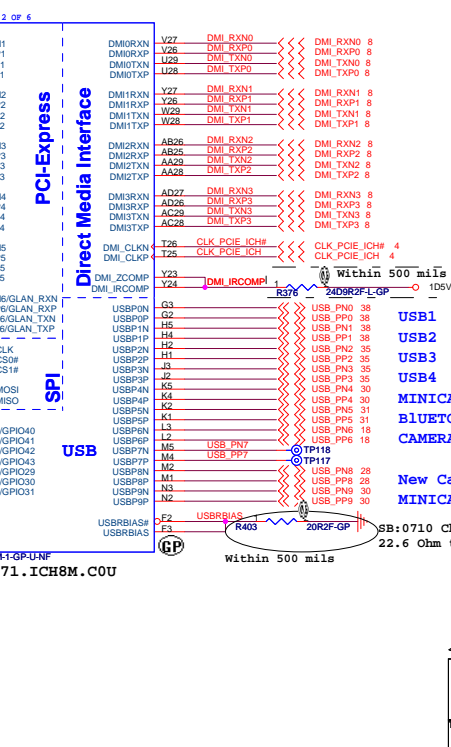
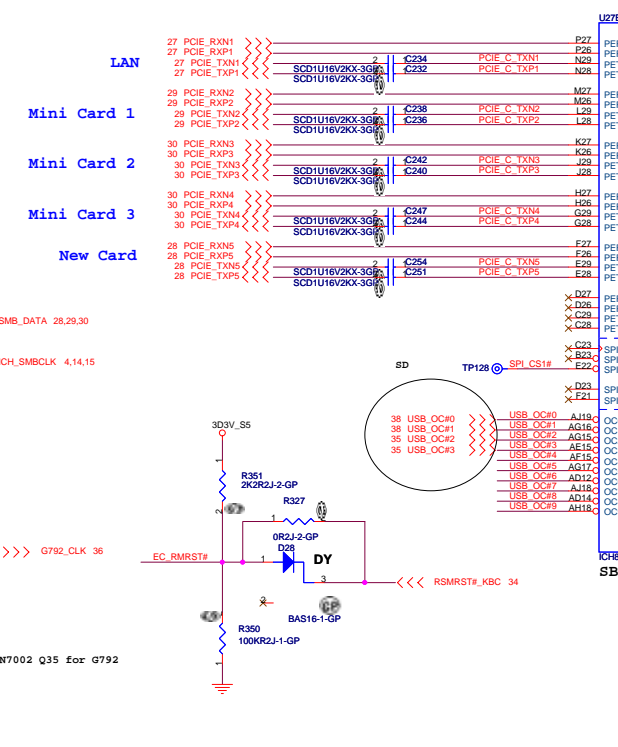
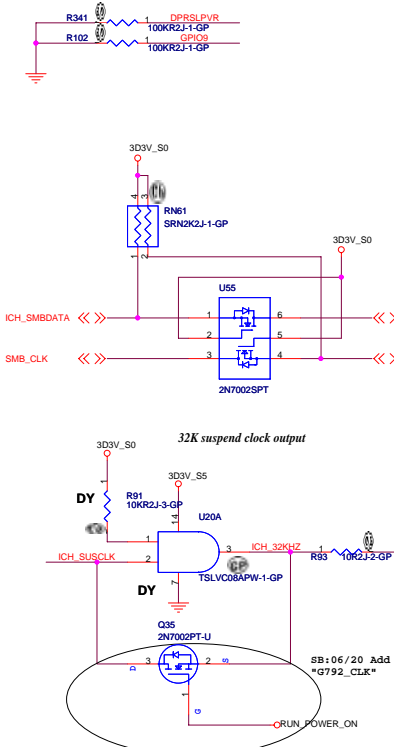
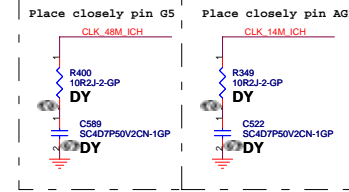
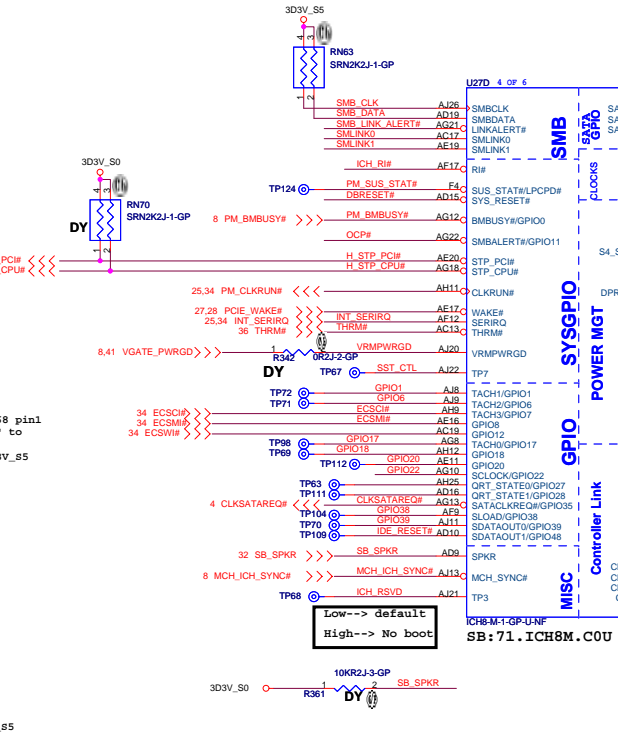
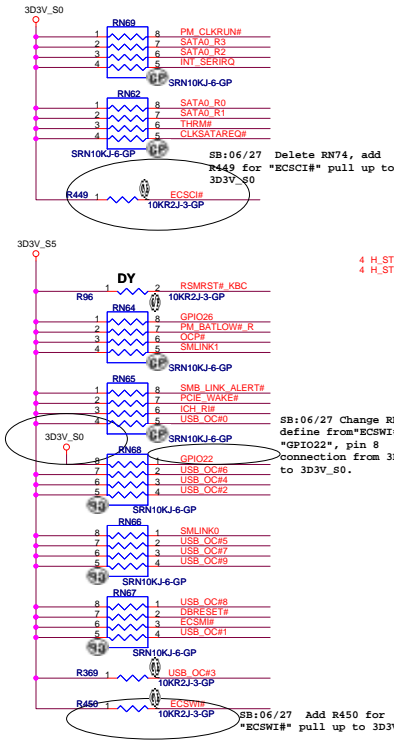
Within 500 mils

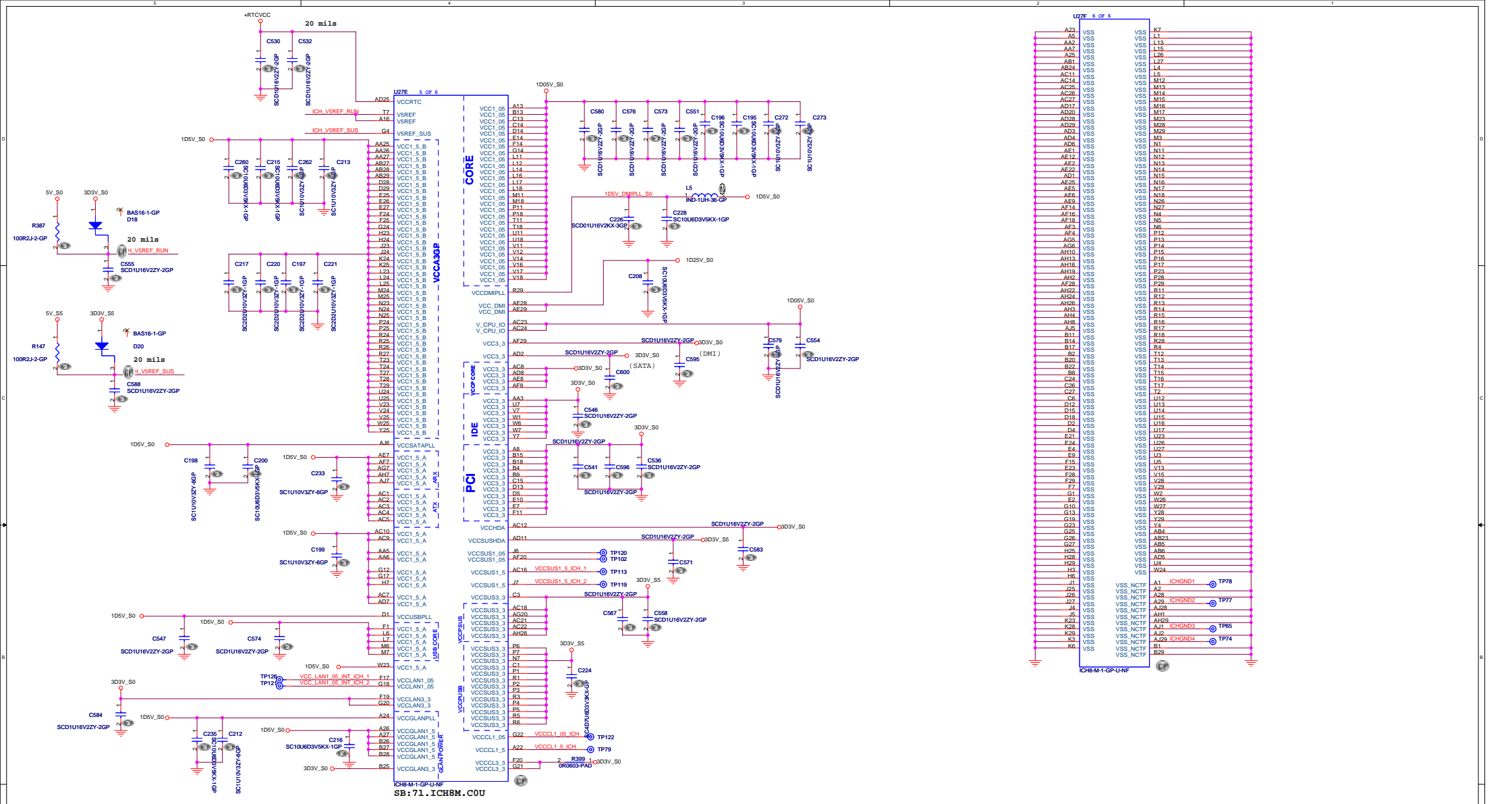


<Variant Name>

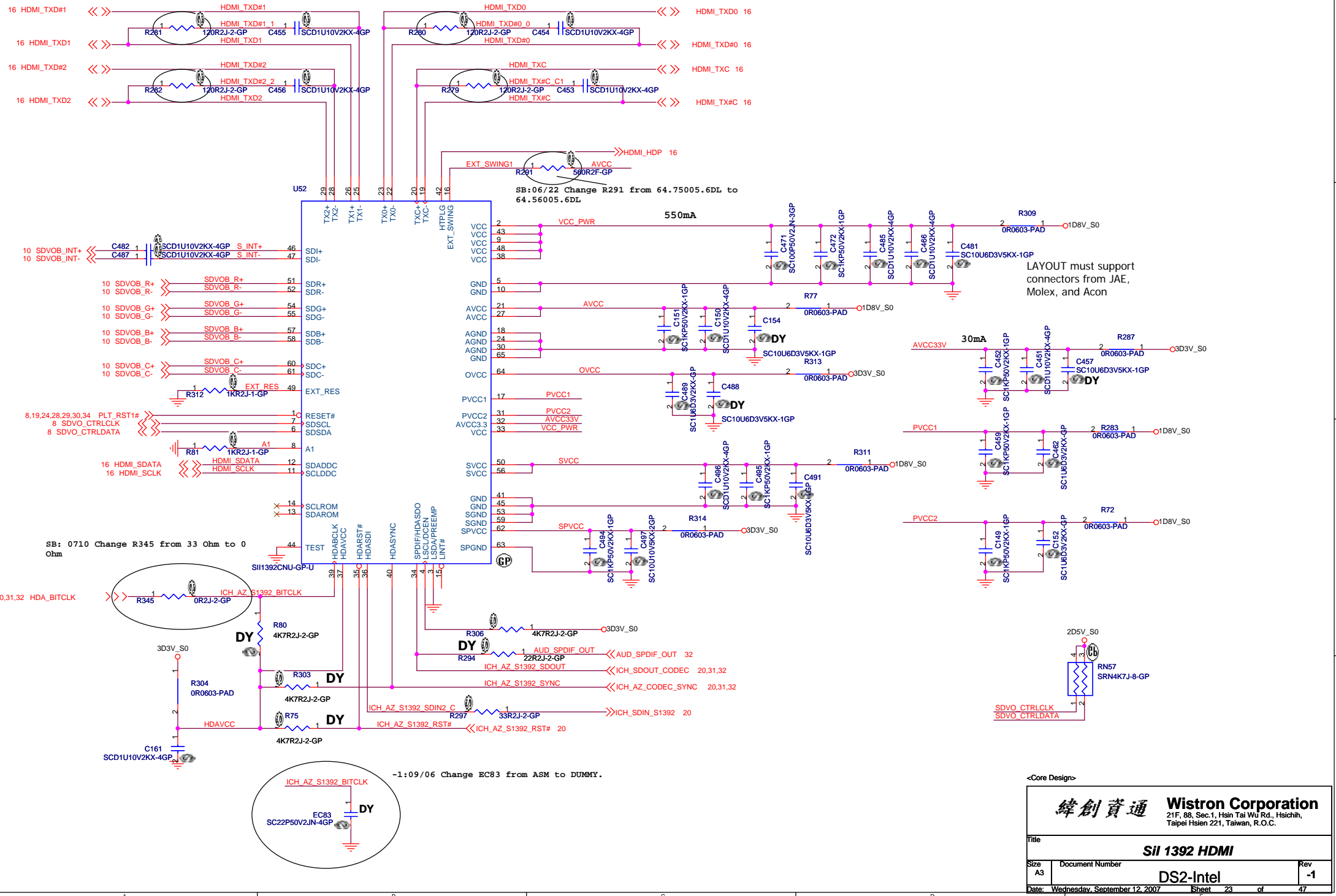
<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>ICH8(2/4) LAN,HD,IDE,LPC</b>	
Title	Rev
Size A3	Document Number
<b>DS2-Intel</b>	
Date: Wednesday, September 12, 2007	Sheet 20 of 47







SB:06/22 Change R279,R280,R281,R282 from 63.30134.1DL to 63.12134.1DL



LAYOUT must support connectors from JAE, Molex, and Acon

<Core Design>

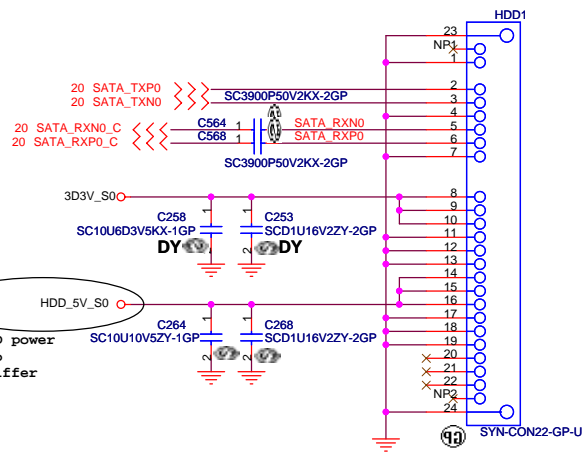
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Sii 1392 HDMI**

Size A3	Document Number	Rev -1
<b>DS2-Intel</b>		
Date: Wednesday, September 12, 2007		Sheet 23 of 47

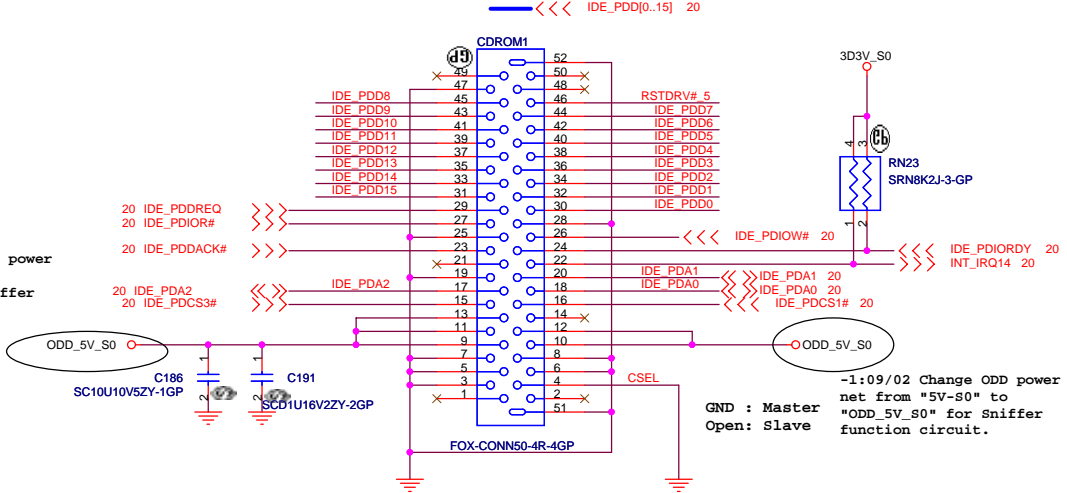
# SATA HD Connector

# CD-ROM Connector



-1:09/02 Change HDD power net from "5V-S0" to "ODD\_5V\_S0" for Sniffer function circuit.

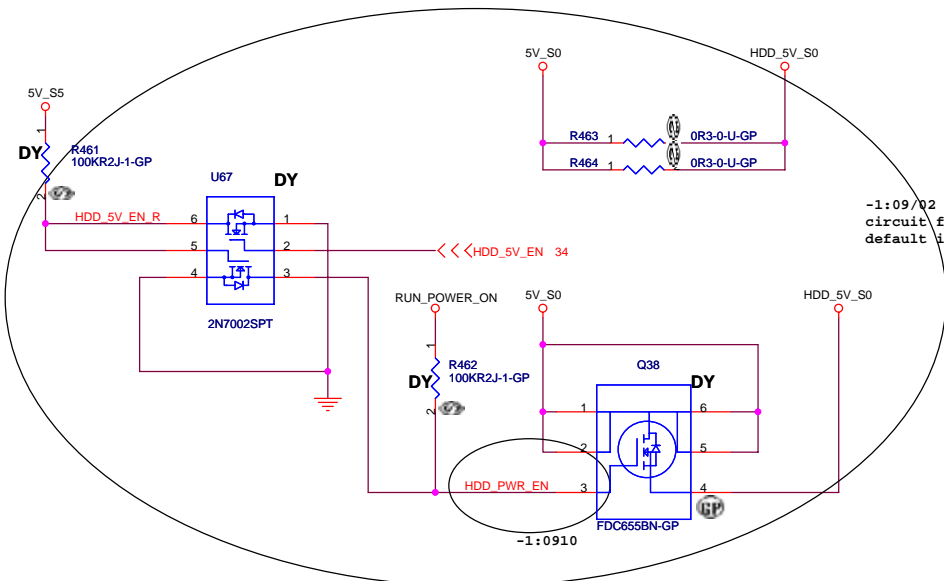
Main Source:20.80919.022



-1:09/02 Change ODD power net from "5V-S0" to "ODD\_5V\_S0" for Sniffer function circuit.

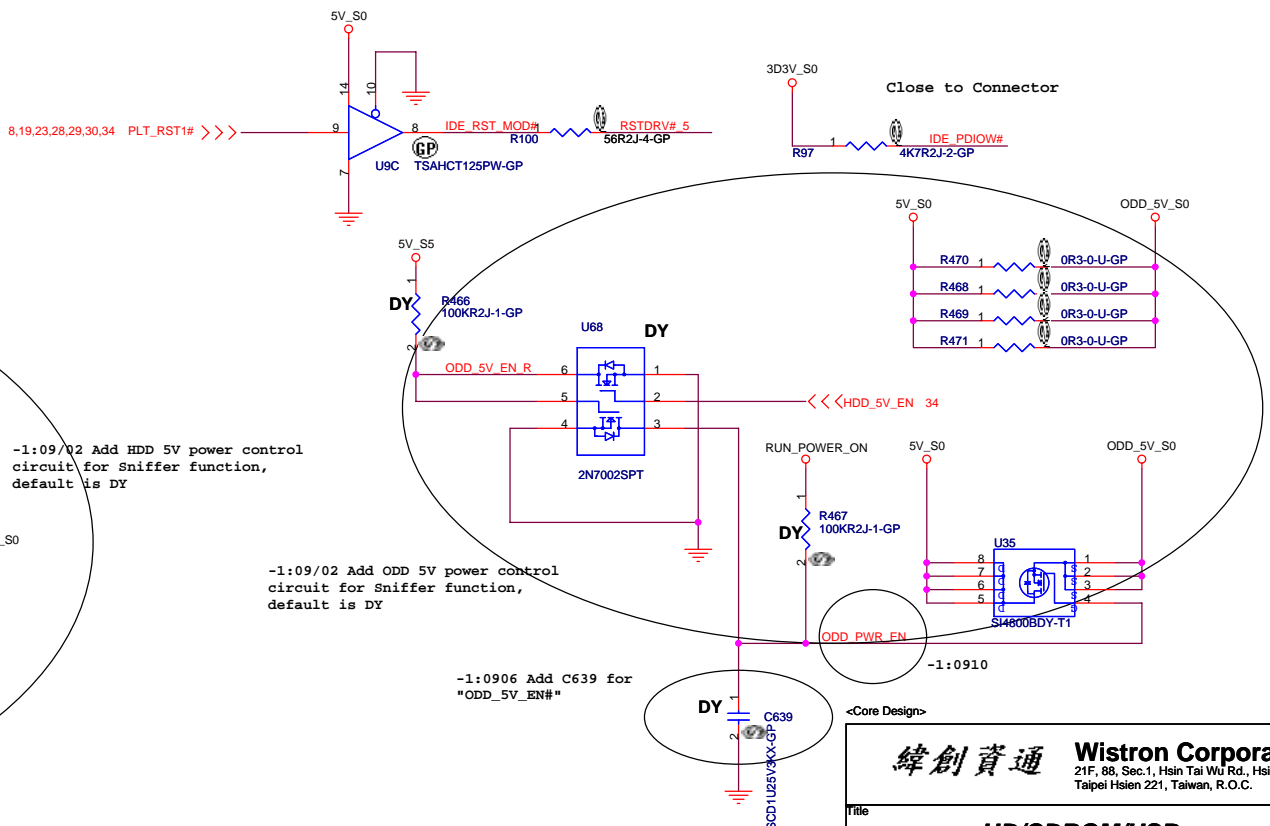
-1:09/02 Change ODD power net from "5V-S0" to "ODD\_5V\_S0" for Sniffer function circuit.

GND : Master  
Open: Slave



-1:09/02 Add HDD 5V power control circuit for Sniffer function, default is DY

-1:0910



-1:09/02 Add ODD 5V power control circuit for Sniffer function, default is DY

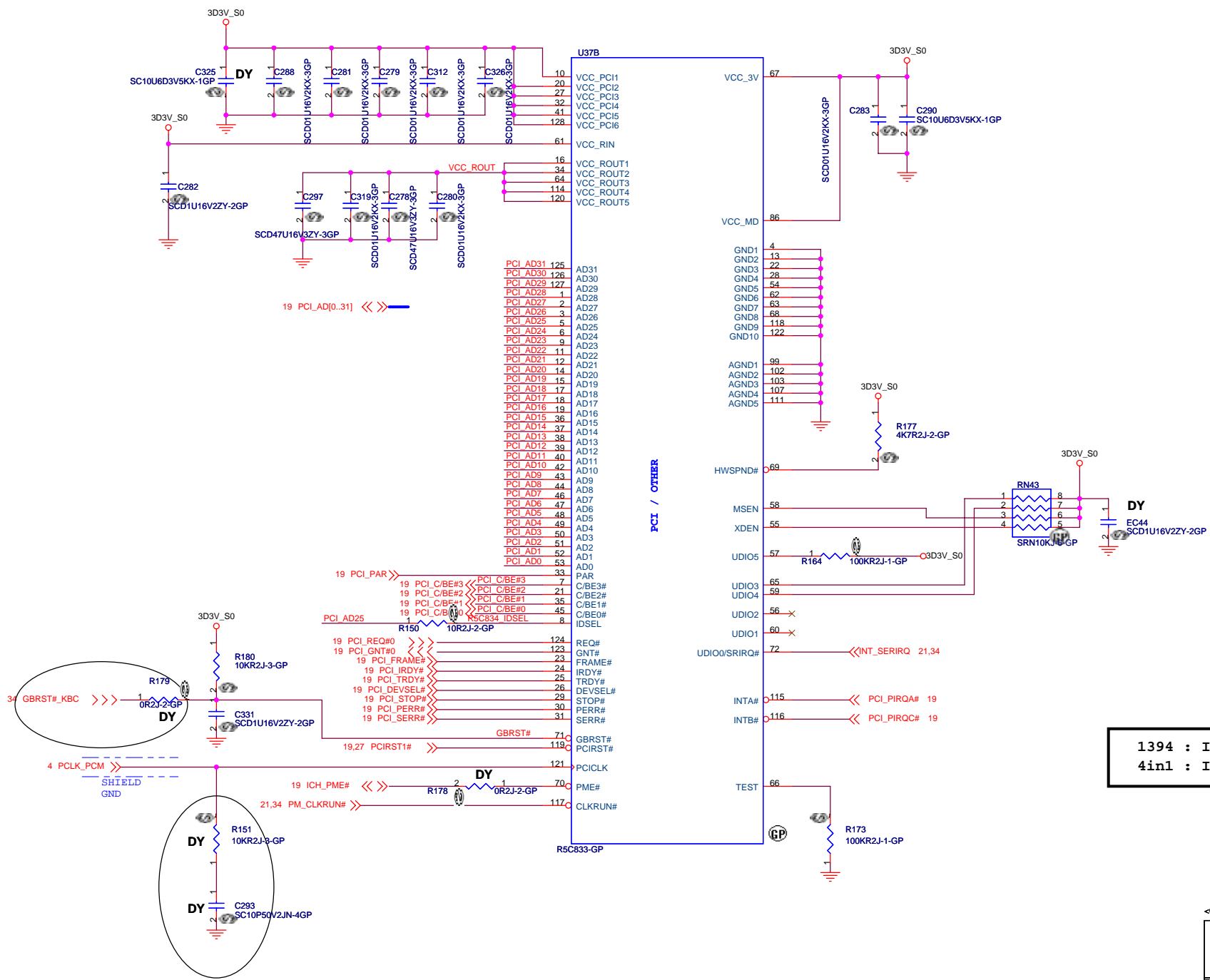
-1:0906 Add C639 for "ODD\_5V\_EN#"

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HD/CDROM/USB**

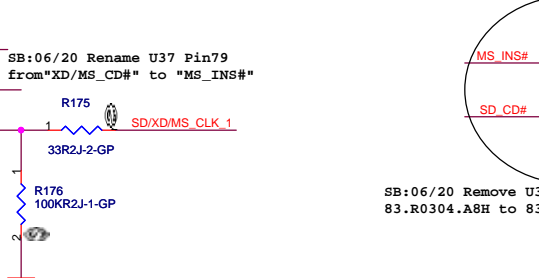
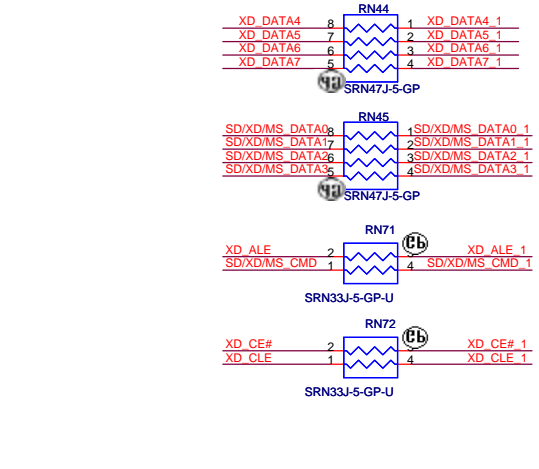
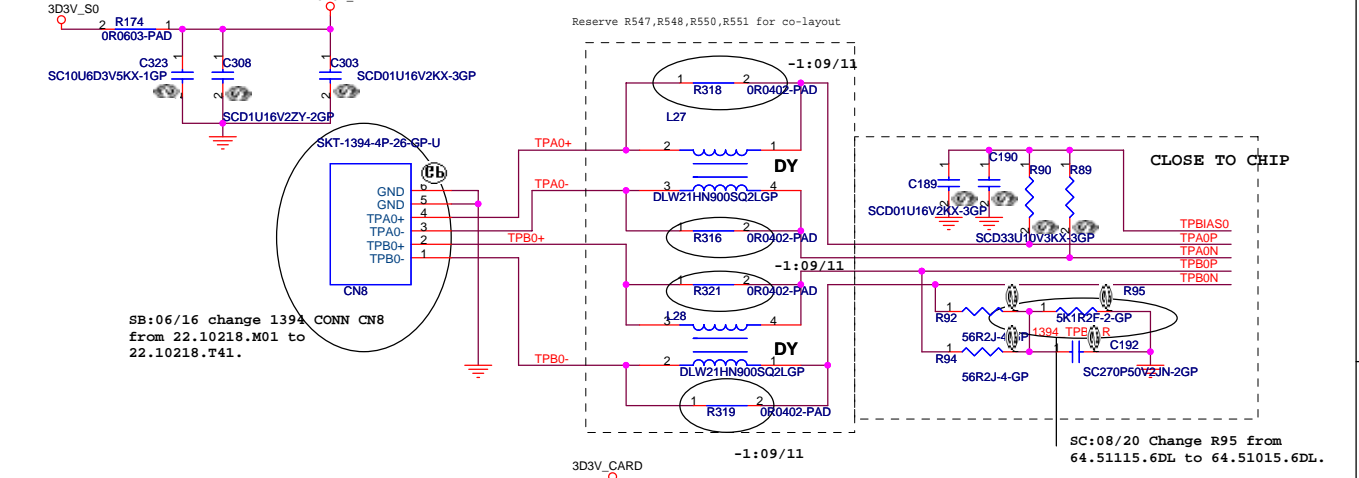
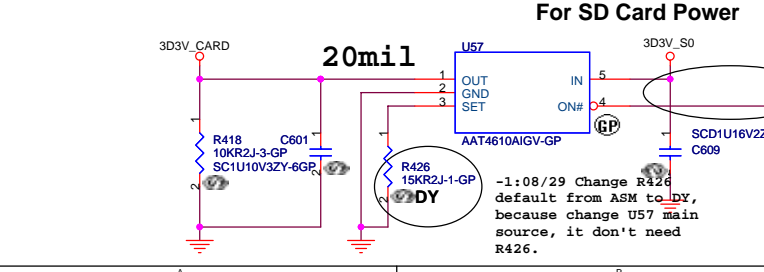
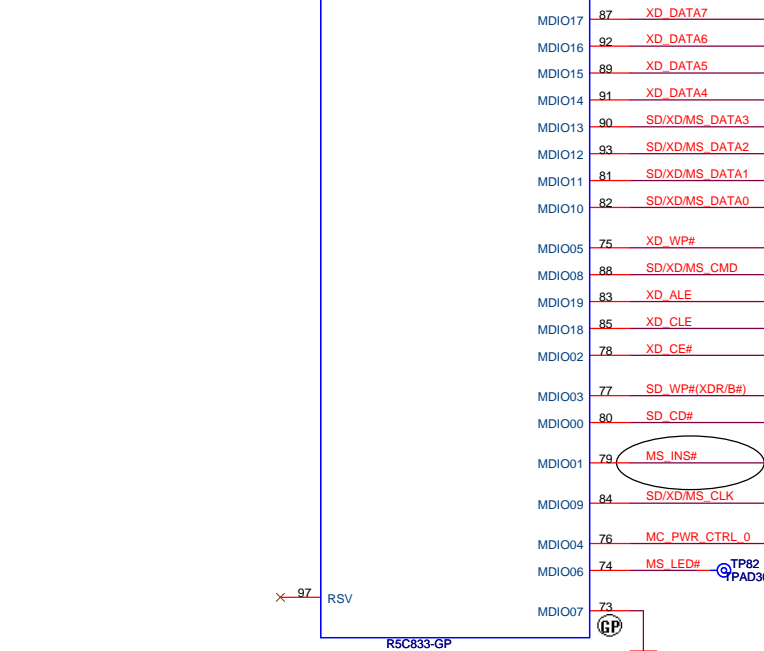
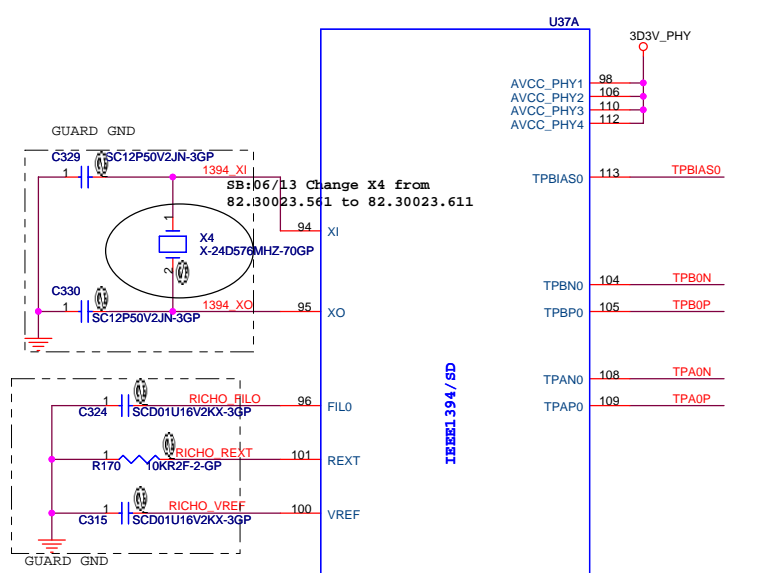
Size A3 Document Number **DS2-Intel** Rev **-1**

Date: Wednesday, September 12, 2007 Sheet 24 of 47



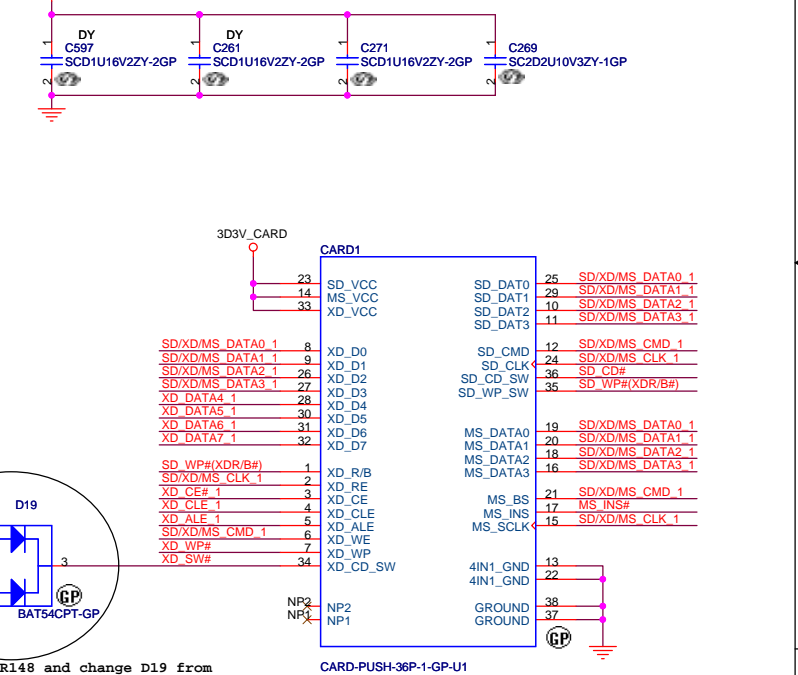
1394 : INTA#  
4in1 : INTB#

<Core Design>



SB:06/20 Remove R427 and change U57 pin4 connect to "MC\_PWR\_CTRL\_0"

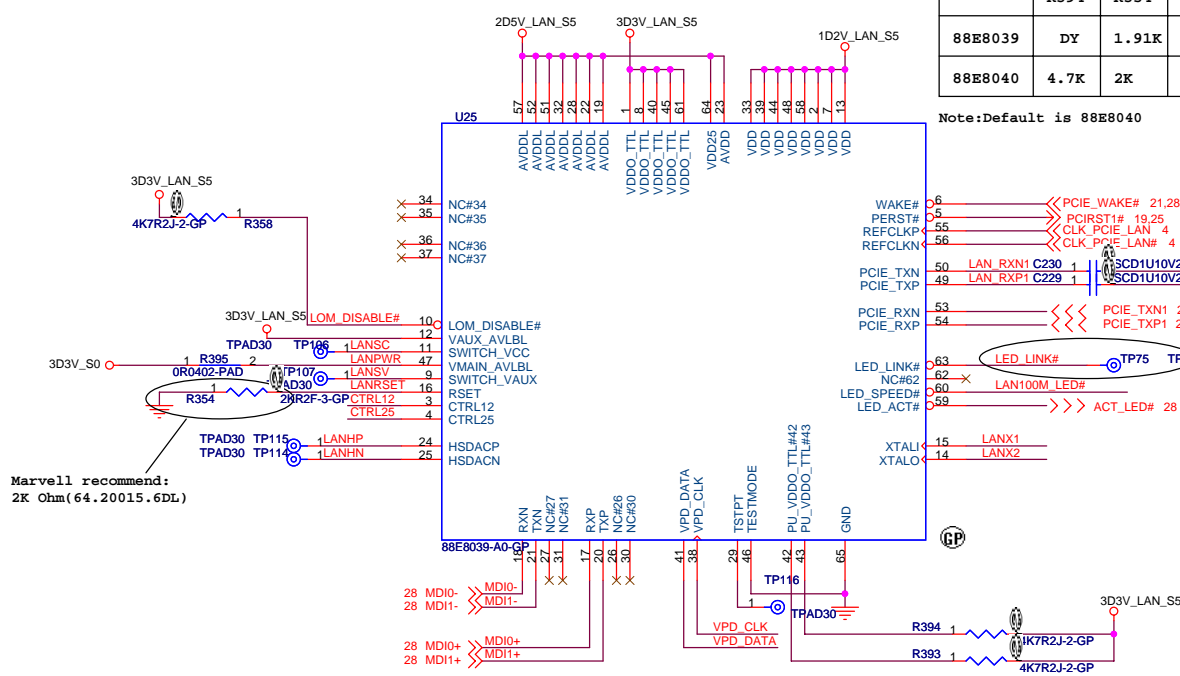
AAT4610AIGV	R426
RT9711DPBG	DY
G5240D2T1U	DY



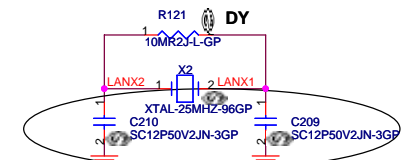


	R394	R354	R357	R362	R372	R377	C528	C544
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY

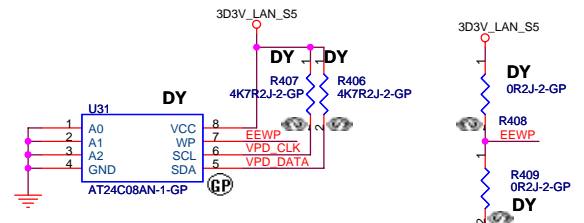
Note: Default is 88E8040



Marvell recommend:  
2K Ohm(64.20015.6DL)

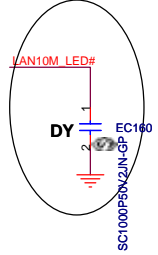


SB:06/13 Change C209,C210 from 27P to 12P

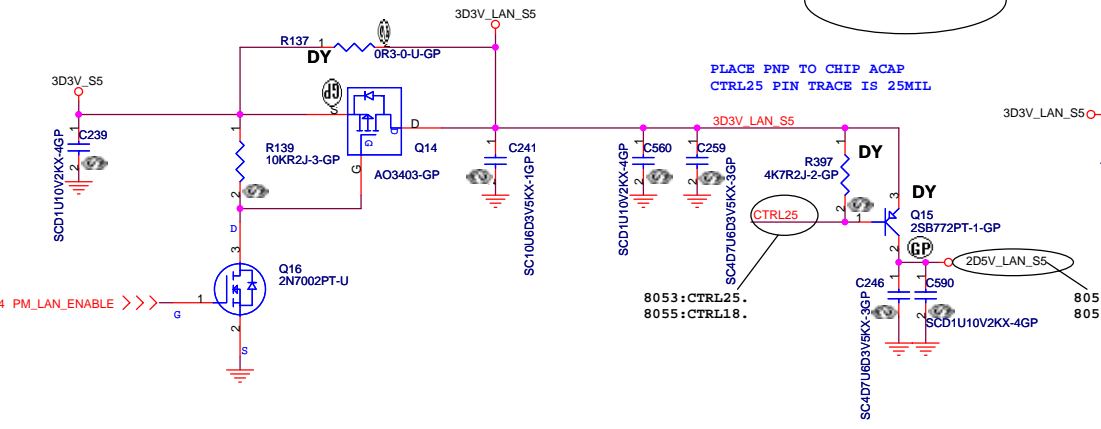
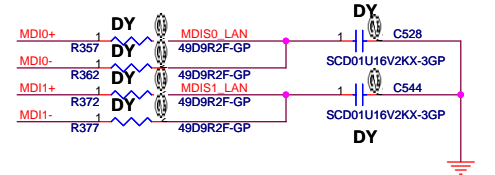


Pull up for AT24C08 another pull low

	R397	Q15	R417	Q17
88E8039	4K7	2SB772PT	4K7	2SB772PT
88E8040	DY	DY	DY	DY

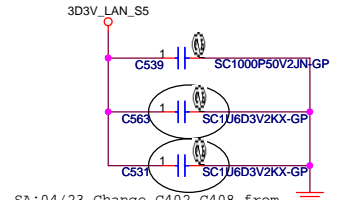


SC:08/09 Add  
EC160(78.10234.1FL) for EMI  
request .Default is DUMMY

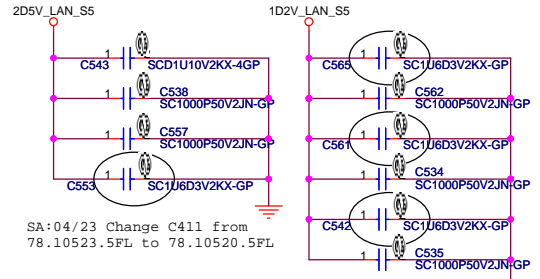


PLACE PNP TO CHIP ACAP  
CTRL25 PIN TRACE IS 25MIL

PLACE PNP TO CHIP ACAP  
CTRL12 PIN TRACE IS 25MIL



SA:04/23 Change C402,C408 from  
78.10523.5FL to 78.10520.5FL



SA:04/23 Change C411 from  
78.10523.5FL to 78.10520.5FL

<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

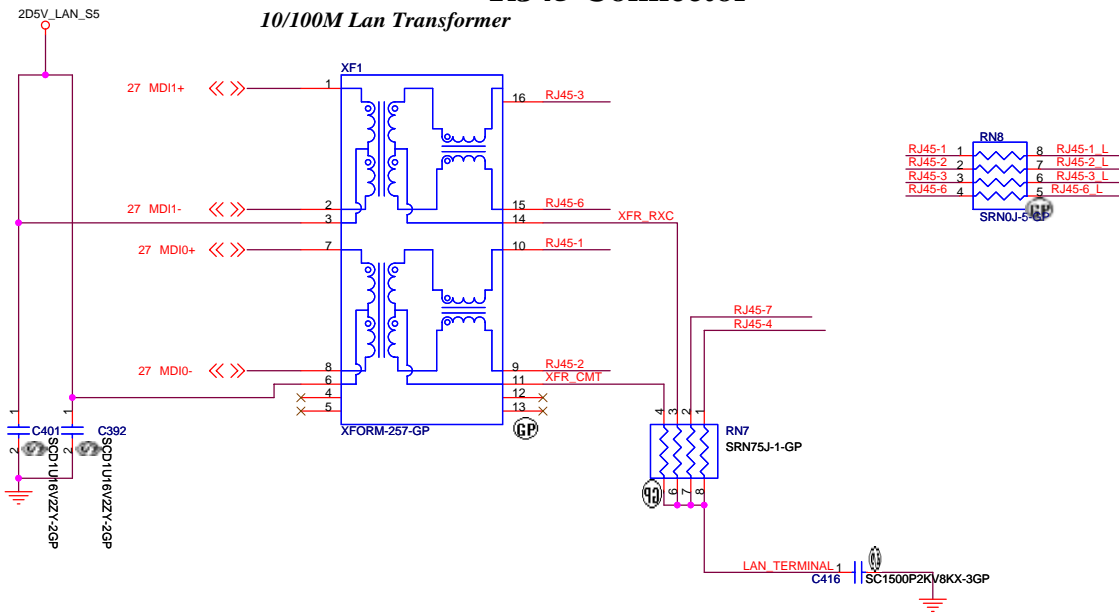
Title: **LAN MARVELL**

Size: A3 Document Number: **DS2-Intel** Rev: **-1**

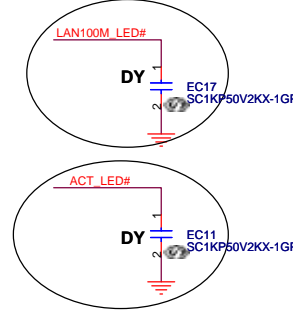
Date: Wednesday, September 12, 2007 Sheet 27 of 47

# RJ45 Connector

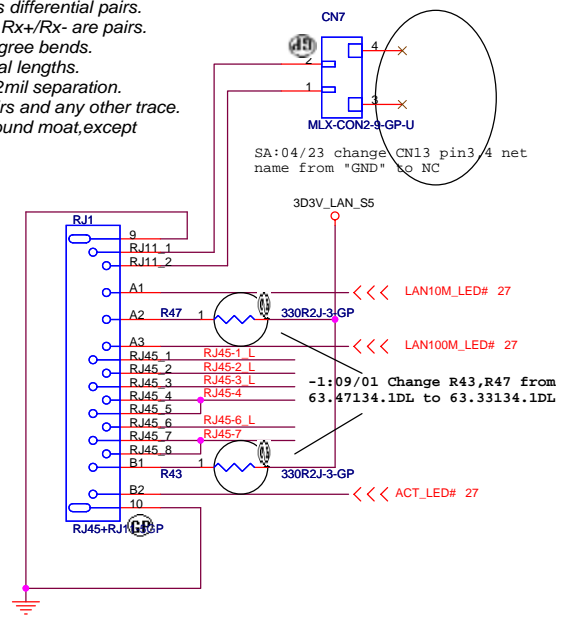
## 10/100M Lan Transformer



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 30mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

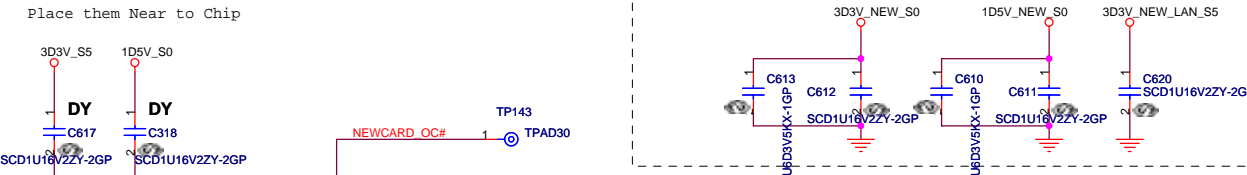


Green : Link up  
Blinking : TX/RX activity



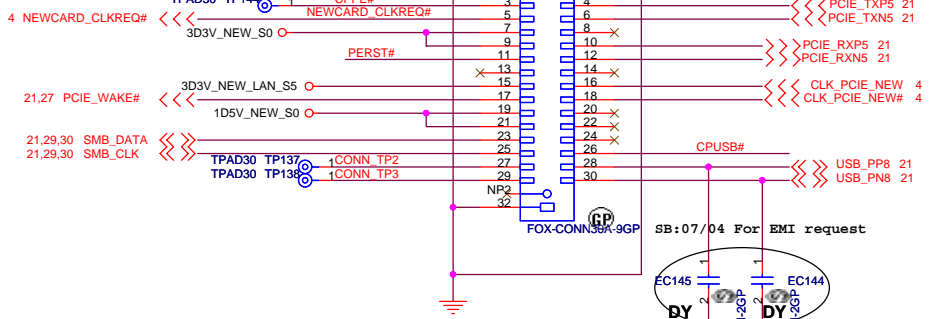
# NEWCARD Connector

Place them Near to Connector



Test circuit  
Use Card and No Card

+1.5V\_CARD Max. 650mA, Average 500mA.  
+3.3V\_CARD Max. 1300mA, Average 1000mA  
+3.3V\_CARDAUX Max. 275mA



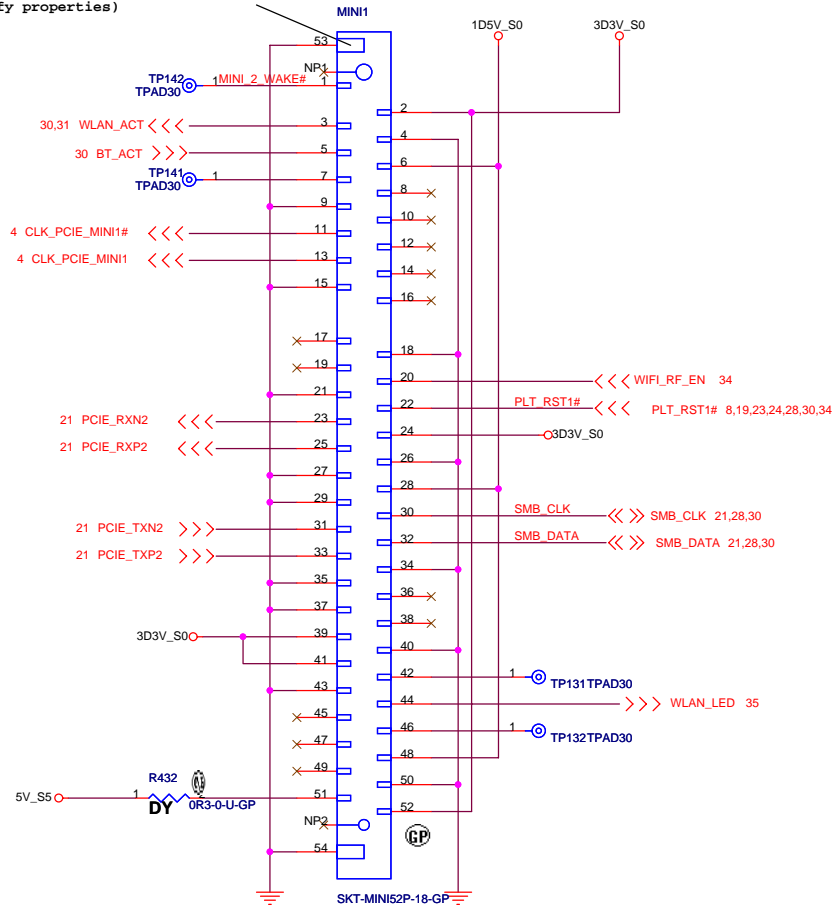
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

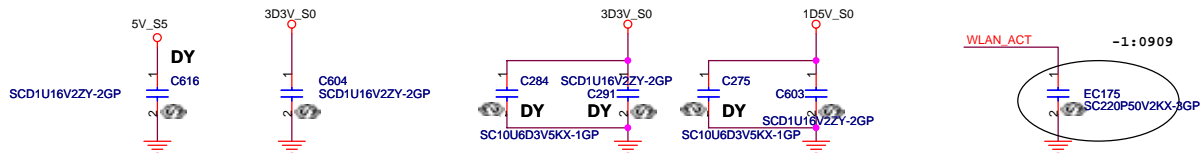
Title <b>LAN connector/NEW CARD/SIM</b>		
Size A3	Document Number <b>DS2-Intel</b>	Rev <b>-1</b>
Date: Wednesday, September 12, 2007	Sheet 26 of 47	

# Mini Card Connector 1(802.11a/b/g)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)



Main Source:62.10043.431  
2nd Source: 20.F0992.052



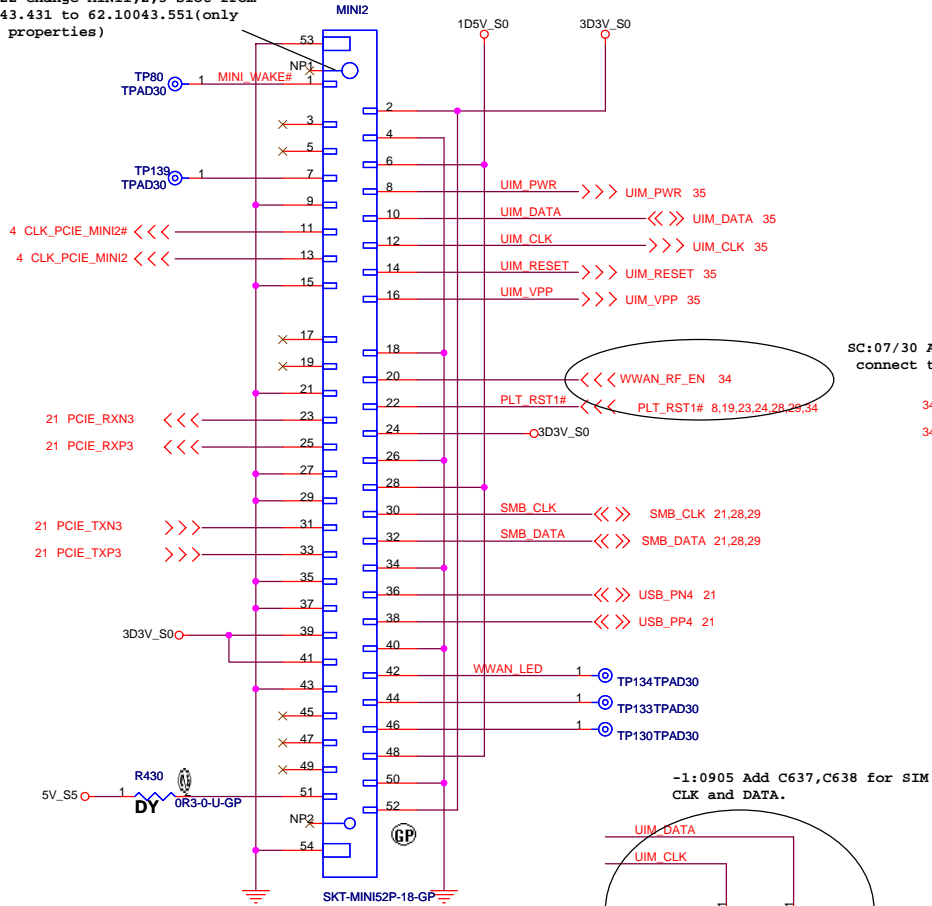
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MINI CARD CONN 1</b>			
Title	Document Number		Rev
Size A3	DS2-Intel		-1
Date: Wednesday, September 12, 2007	Sheet	29	of 47

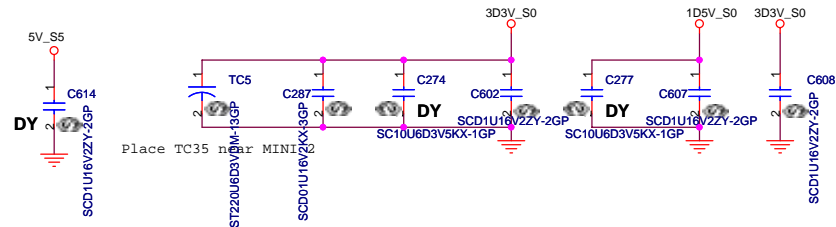
# Mini Card Connector

## Mini Card Connector 2(WWAN)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)

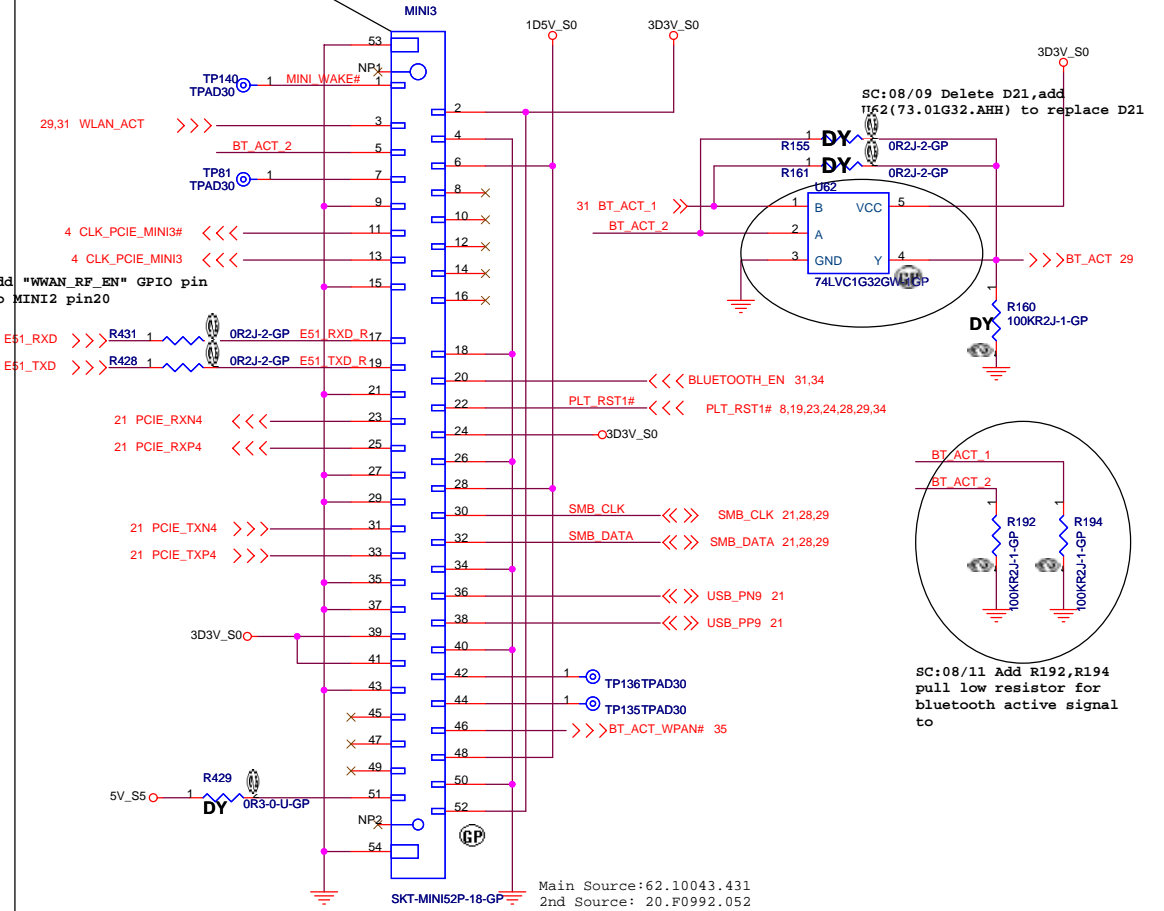


Main Source:62.10043.431  
2nd Source: 20.F0992.052

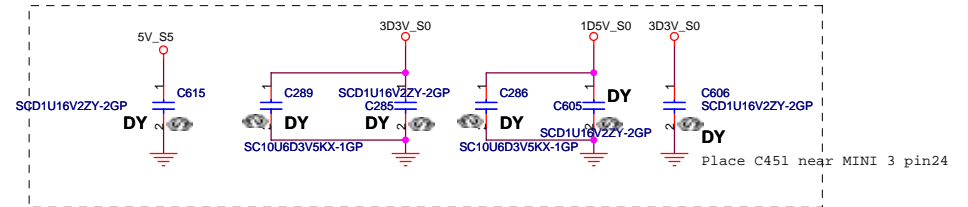


# Mini Card Connector 3(Robson)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)

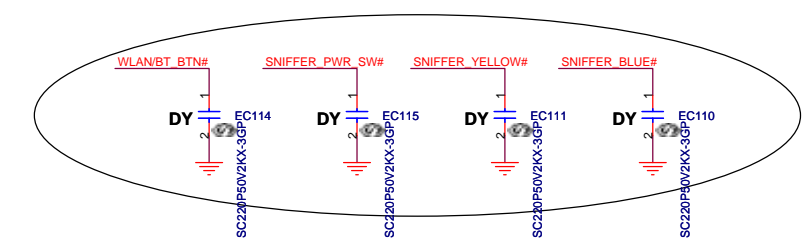
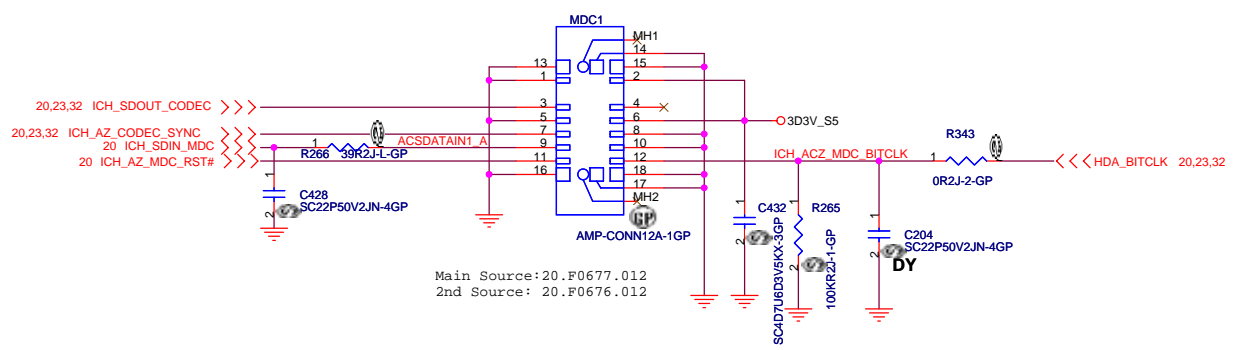
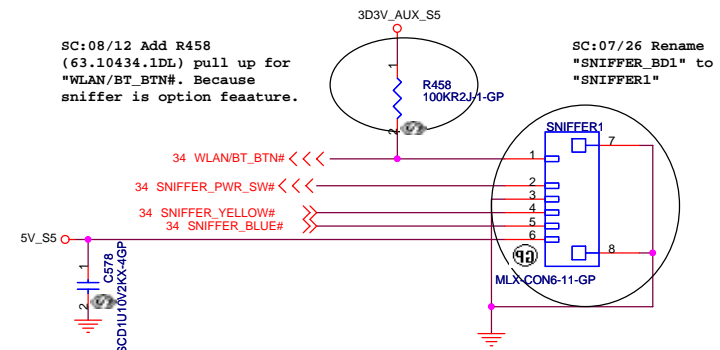
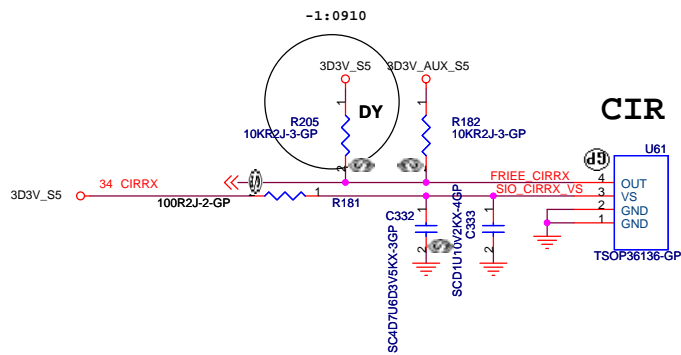


Main Source:62.10043.431  
2nd Source: 20.F0992.052

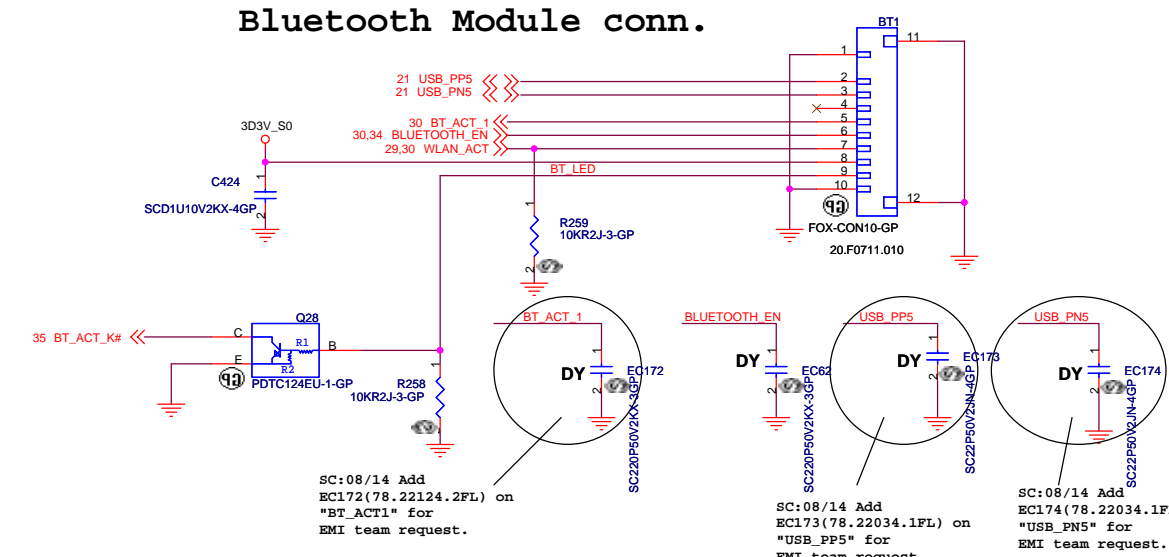


<Core Design>

<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MINI CARD CONN 2 &amp; 3</b>	
Title	
Size A3	Document Number
<b>DS2-Intel</b>	
Date: Wednesday, September 12, 2007	Sheet 30 of 47
Rev <b>-1</b>	



**Bluetooth Module conn.**

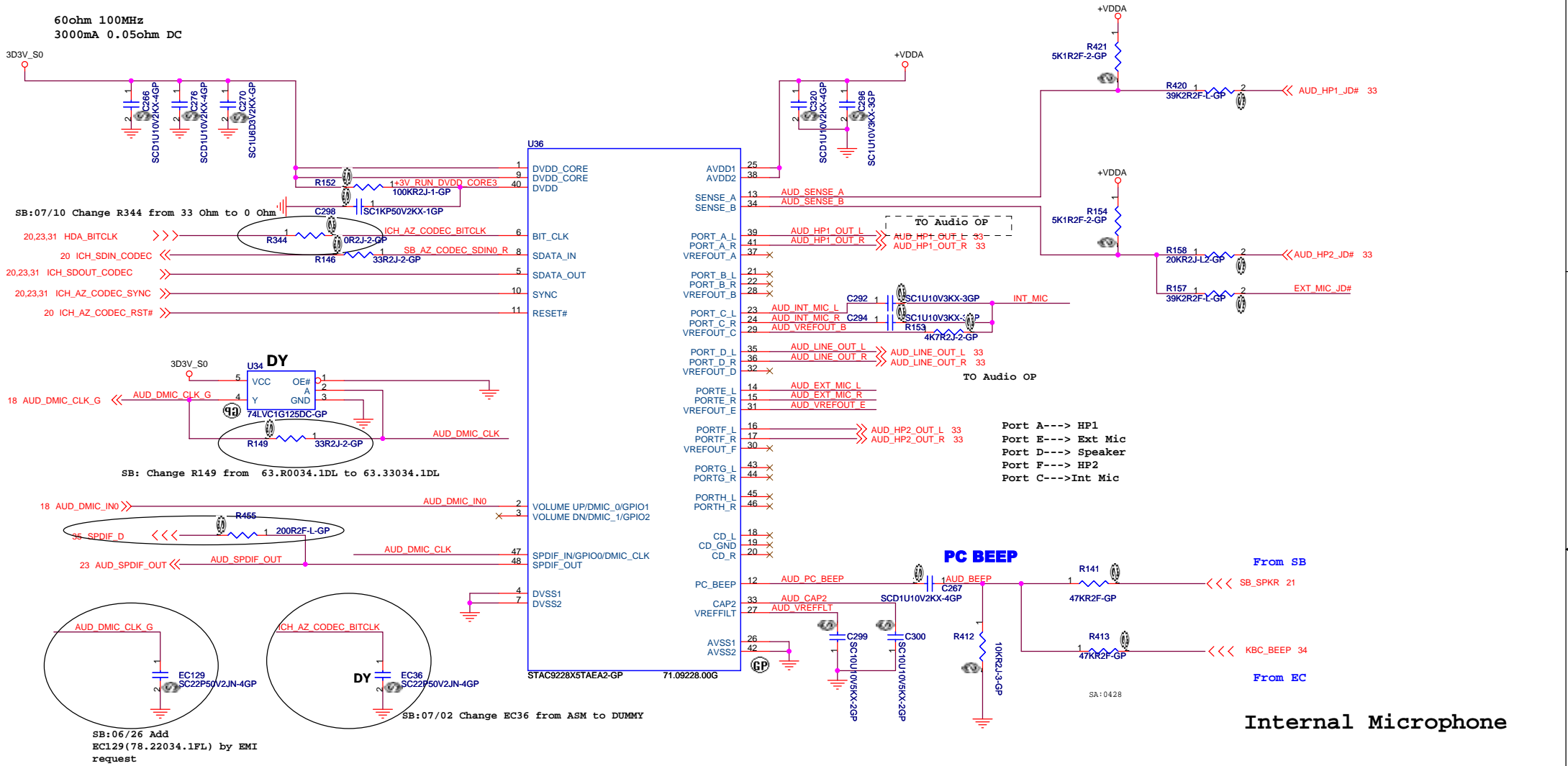


<Core Design>

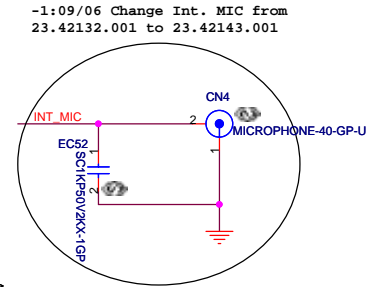
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MDC&RJ11 CONN**

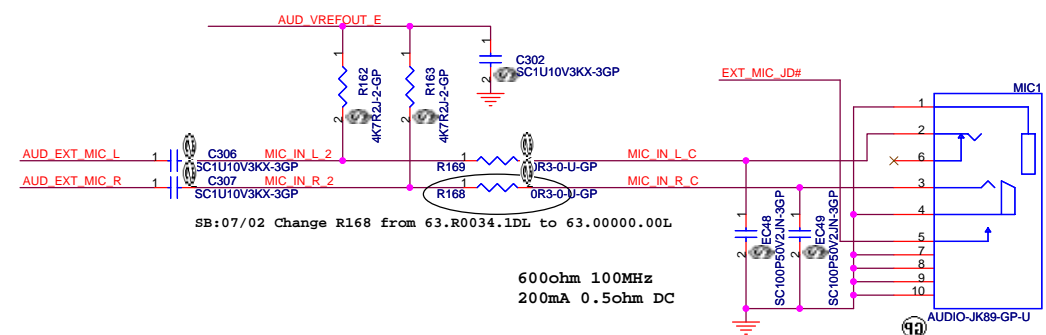
Size: A3  
 Document Number: **DS2-Intel**  
 Date: Wednesday, September 12, 2007  
 Sheet: 31 of 47  
 Rev: **-1**



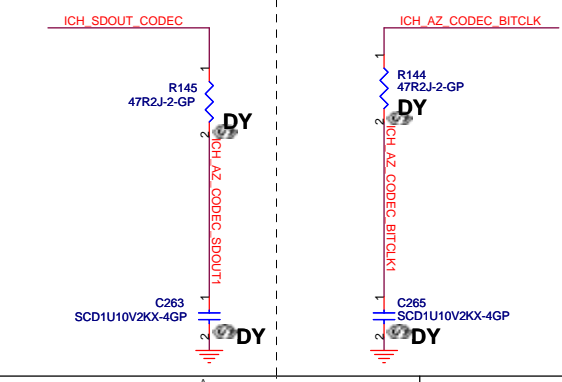
### Internal Microphone



### MIC IN



### Azalia I/F EMI



<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC STAC9228**

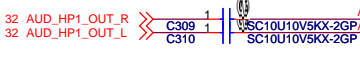
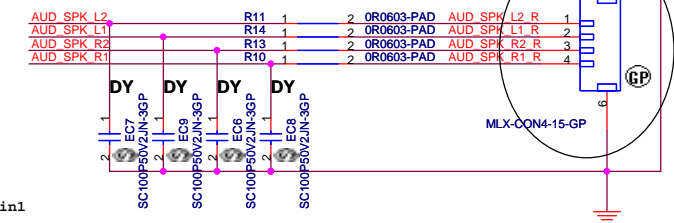
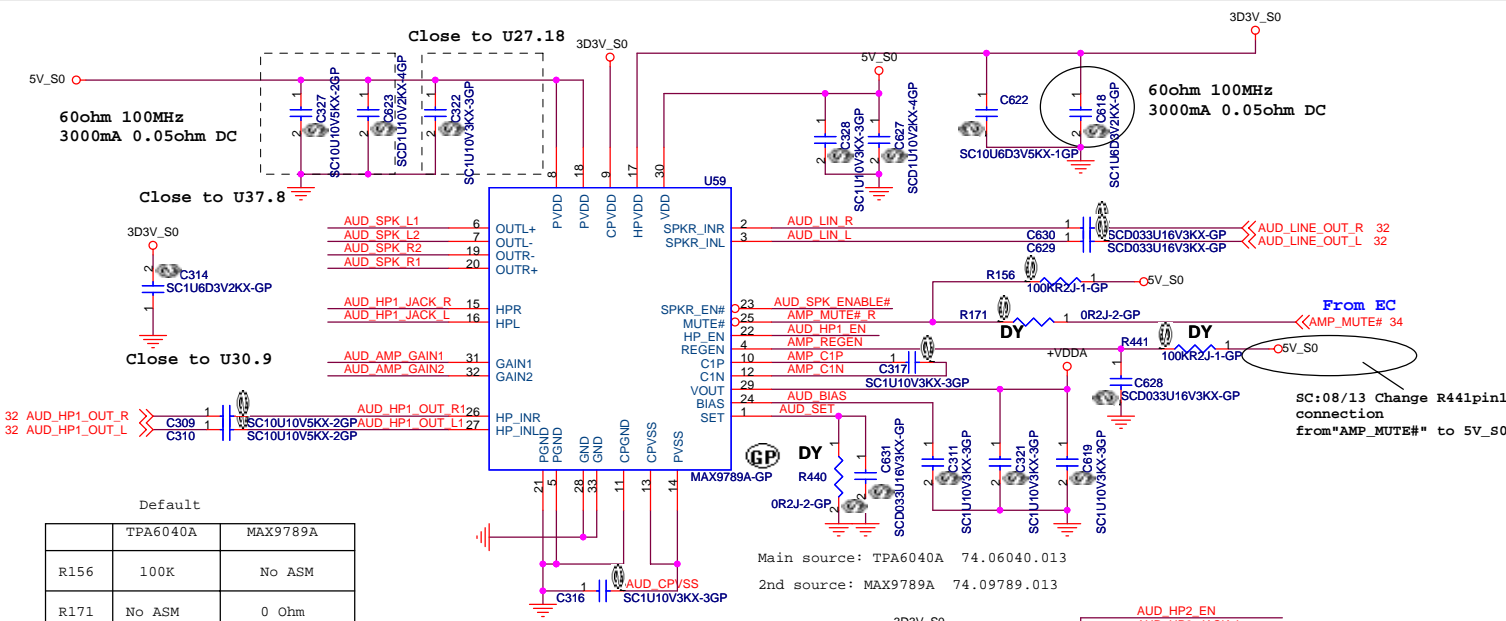
Size A3	Document Number	Rev -1
------------	-----------------	-----------

Date: Wednesday, September 12, 2007 Sheet 32 of 47



# Speaker

SC:08/11 Change SPK1 pin define that follow ME request

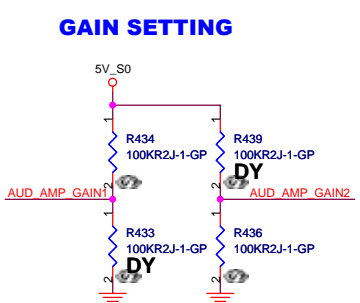
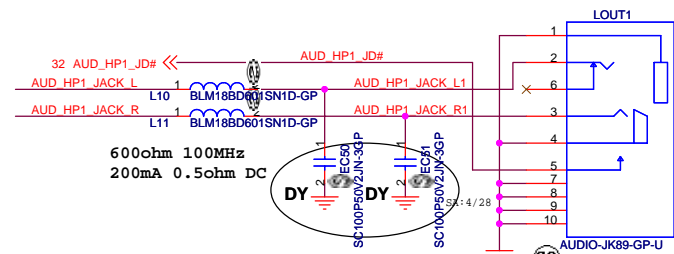


Default

	TPA6040A	MAX9789A
R156	100K	No ASM
R171	No ASM	0 Ohm
R440	No ASM	0 Ohm
R441	No ASM	100K
C631	0.33uF	No ASM
C628	0.33uF	No ASM

Main source: TPA6040A 74.06040.013  
2nd source: MAX9789A 74.09789.013

## LINE1 OUT

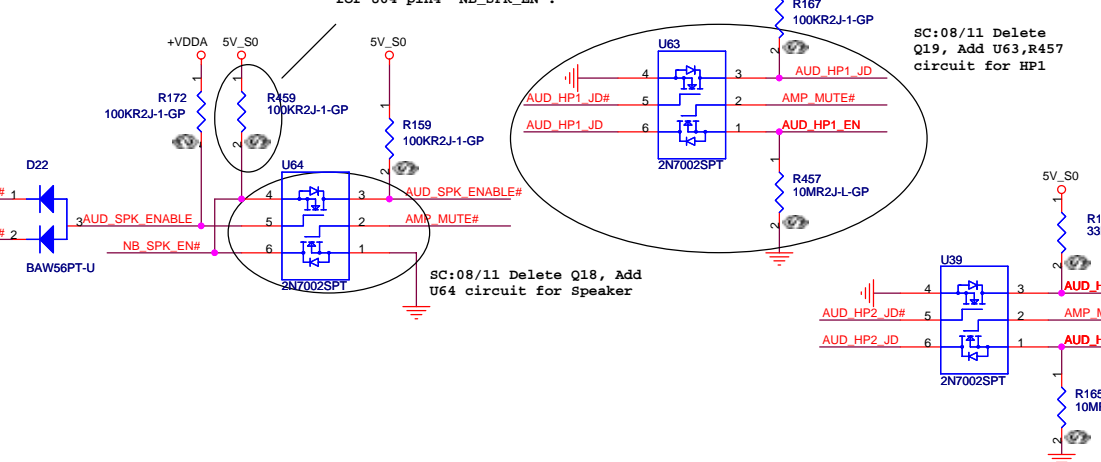


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Main source: TPA411MRTV 74.04411.AE3  
2nd source: MAX4411EPT+ 74.04411.A13

## Signal inverter for speaker shutdown

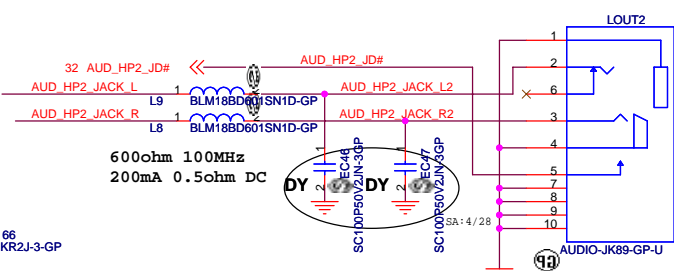
SC:08/12 Add R459 (63.10434.1DL) pull up for U64 pin4 "NB\_SPK\_EN".



SC:08/11 Delete Q19, Add U63, R457 circuit for HP1

SC:08/11 Delete Q18, Add U64 circuit for Speaker

## LINE2 OUT



<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **AUDIO AMP/SPEAKER**

Size: A3 Document Number: **DS2-Intel** Rev: **-1**

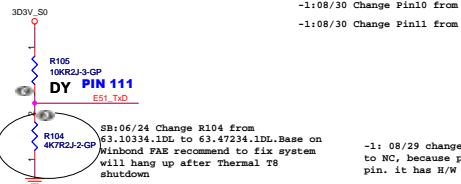
Date: Wednesday, September 12, 2007 Sheet: 33 of 47

### WPC8763L STRAP PIN

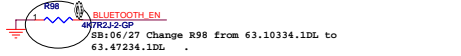
JENO (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES	GPIO Port	Keyboard Data	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

**TRIS#(Pin 110) TRI-STATE**  
**Forces the device to float all its output and I/O pins,if an external 10 KΩ pull-down resistor is connected.**

**BADDR1-0 (PIN 111, 112) I/O Base Address. 10KΩ external pull-down resistor on BADDR1: Core defined**



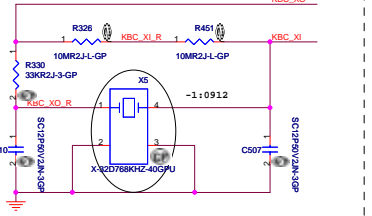
**SBHM PIPN83 Shared Host BIOS Memory. HIGH:NO SHARED(internal resistor) LOW:SHARED BIOS memory.**



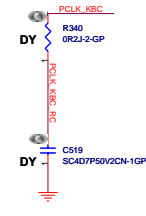
### MB VERSION ID

	VER0	VER1
SA	0	0
SB	0	1
SC	1	0
-1	1	1

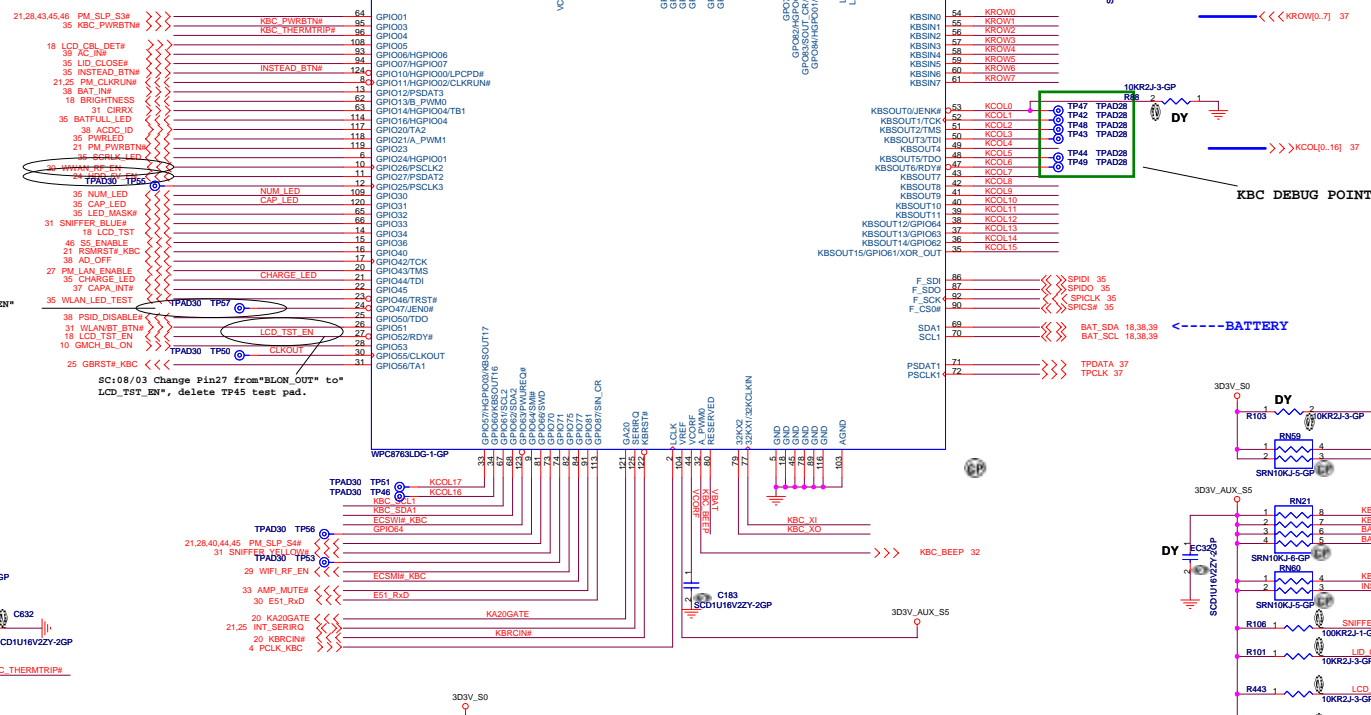
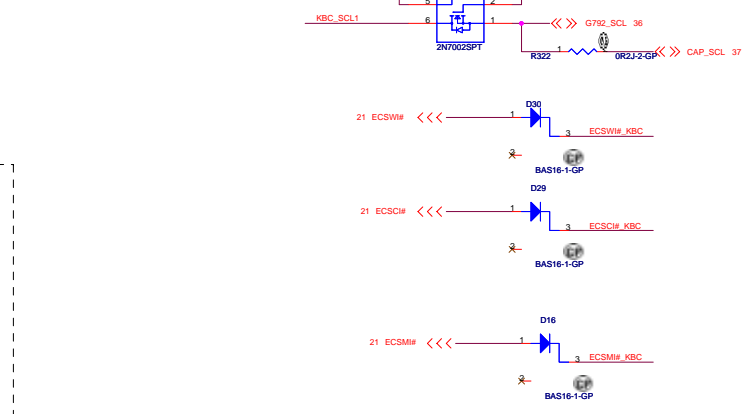
### WPC8763L XTAL



### KBC CLK EMI



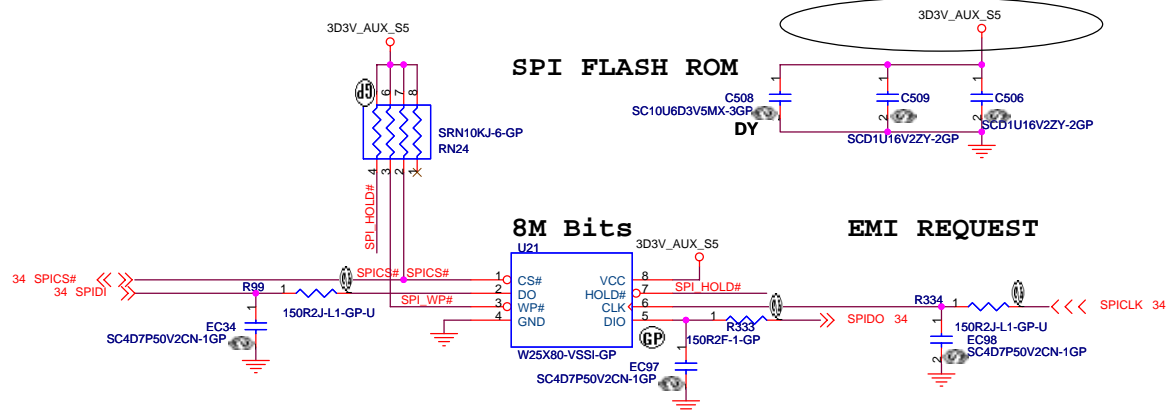
### FOR Thermal AND Capacity Button Module



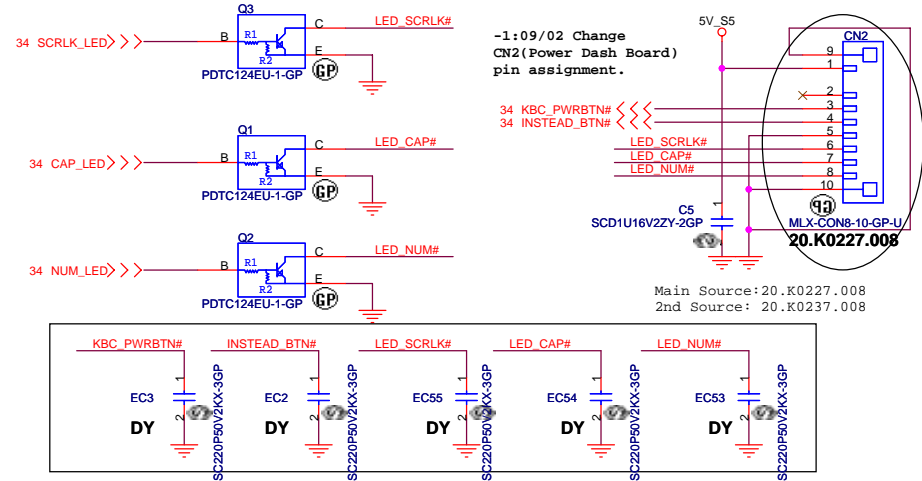
- ADIA:to Charger
- ACDC\_ID:from Adapter Conn
- KBC\_PWRBTN#:from power button
- BAT\_IN#:from Battery Conn
- DC\_BATFULL#:for Battery charge LED 1
- WLAN\_TEST#:for WES test WLAN LED
- AD\_OFF:enable AC adapter power source
- CHARGE\_LED#:for Battery charge LED 2
- WLAN/BT\_BTN#:from Wlan on/off button
- GMCH\_BL\_ON:Sense The Backlight On/Off Status from VGA Chip
- WIRELESS\_EN:Disable/Enable Wireless Module
- BLUETOOTH\_EN:Disable/Enable Bluetooth
- USB\_PWR\_EN#:to on/off USB power switch
- CCD\_ON:Webcam power on/off
- AC\_IN#:From Charge

# SPI

SA:04/22 change C532,C533,C534 connection power from "3D3V\_S0" to "3D3V\_AUX\_S5"

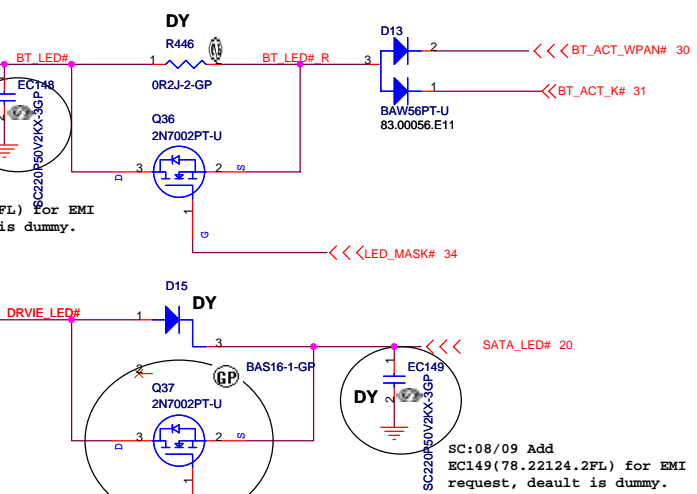
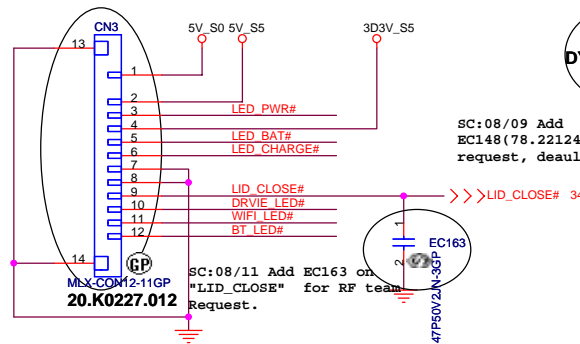


# Power Dash Board to Board CONN



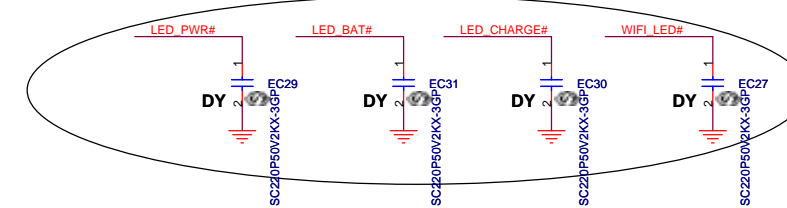
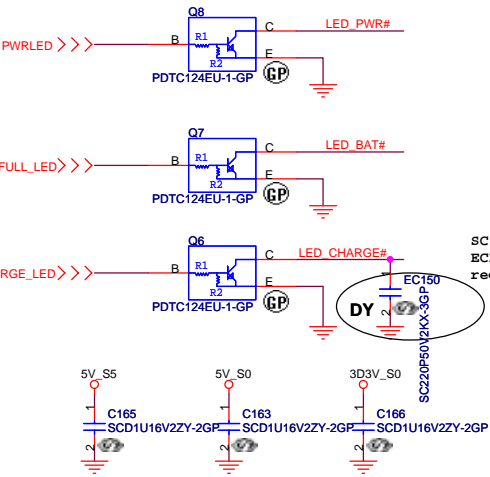
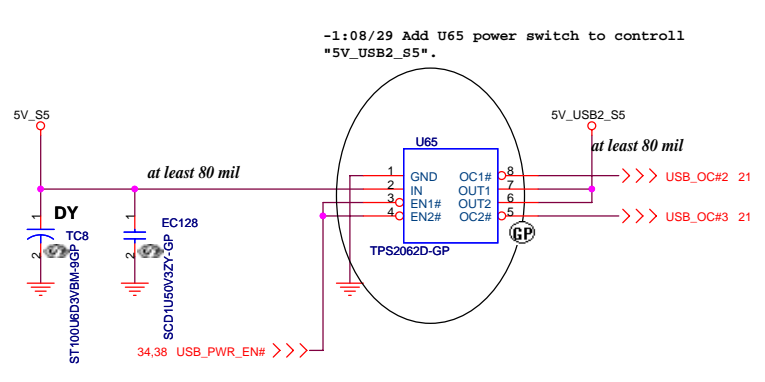
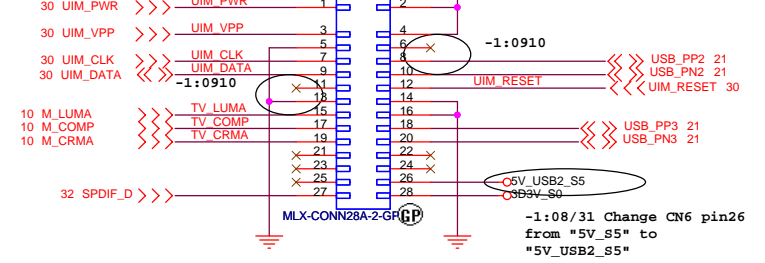
# LED Board to Board CONN

-1:09/02 Change CN3(LED Board) pin assignment.



# Right I/O Board to Board CONN

-1:08/29 Rename CN6 pin2, pin4 power net become "5V\_USB2\_S5".



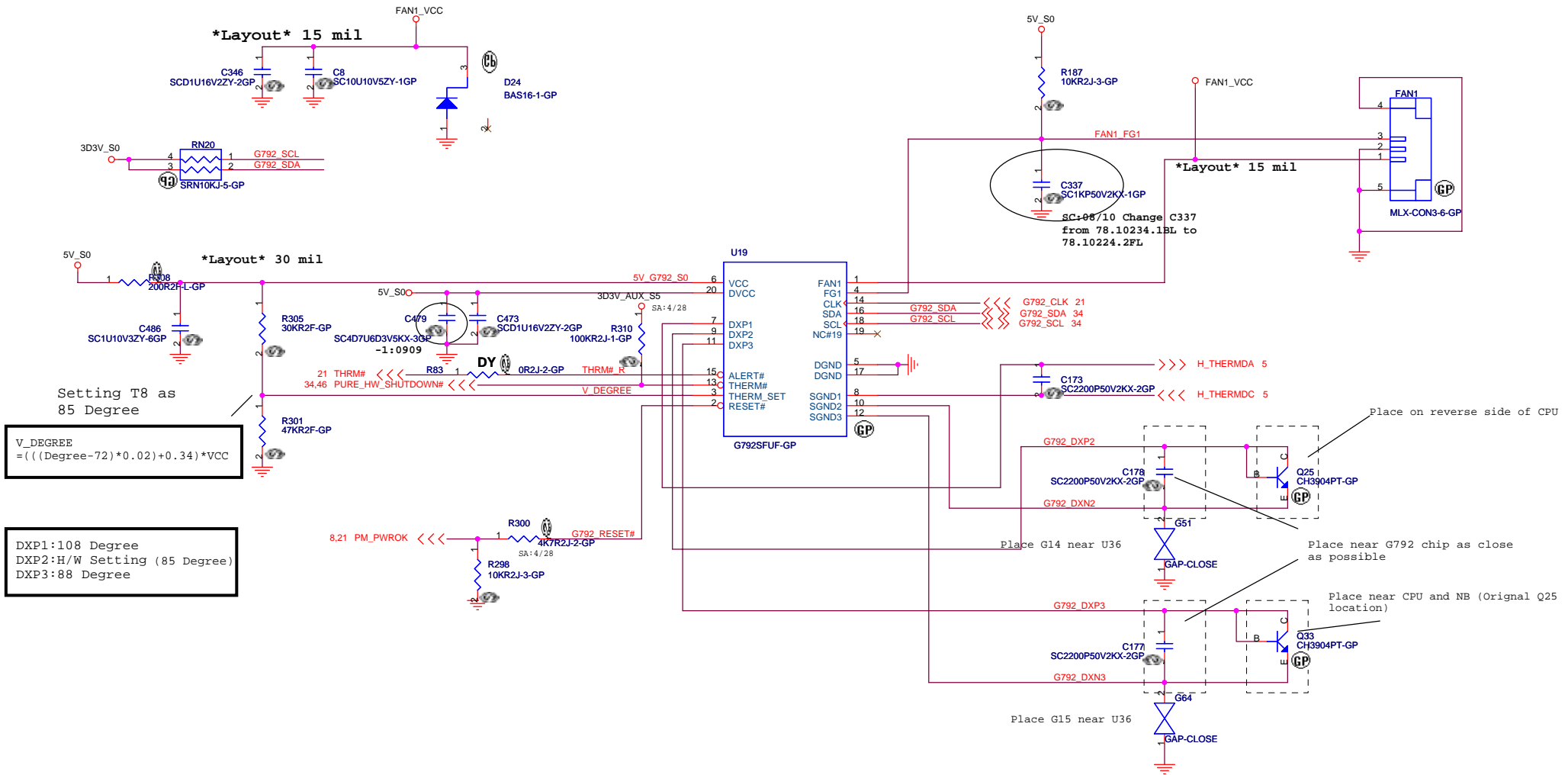
<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **FWH and Board to Board CONN**

Size: A3 Document Number: **DS2-Intel** Rev: **-1**

Date: Wednesday, September 12, 2007 Sheet 35 of 47



Setting T8 as 85 Degree

$$V\_DEGREE = (((Degree-72)*0.02)+0.34)*VCC$$

DXP1:108 Degree  
DXP2:H/W Setting (85 Degree)  
DXP3:88 Degree

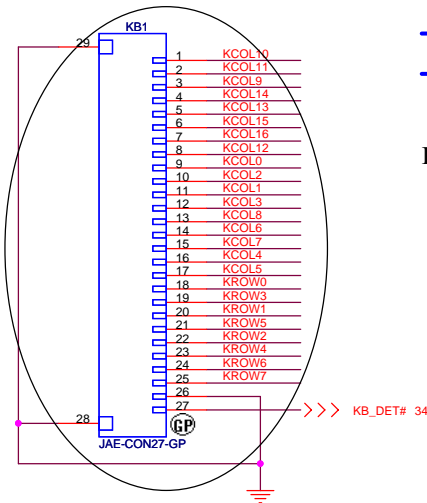
Place on reverse side of CPU

Place near G792 chip as close as possible

Place near CPU and NB (Original Q25 location)

Place G14 near U36

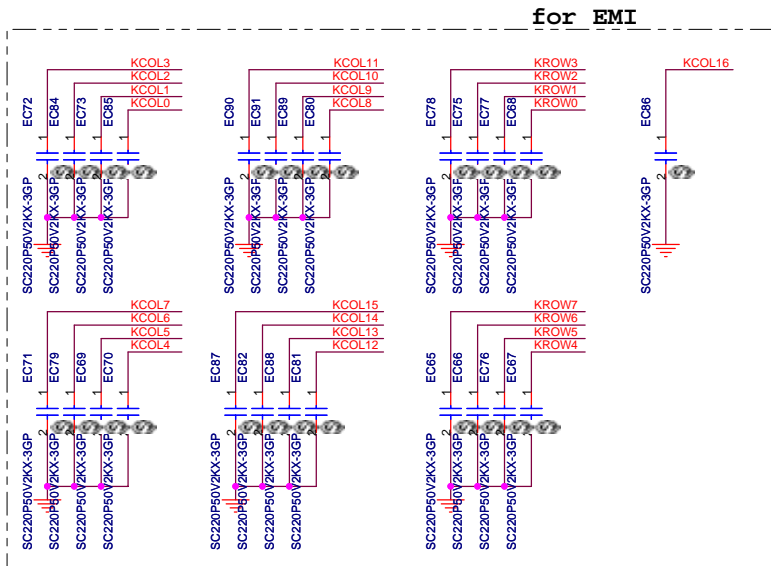
Place G15 near U36



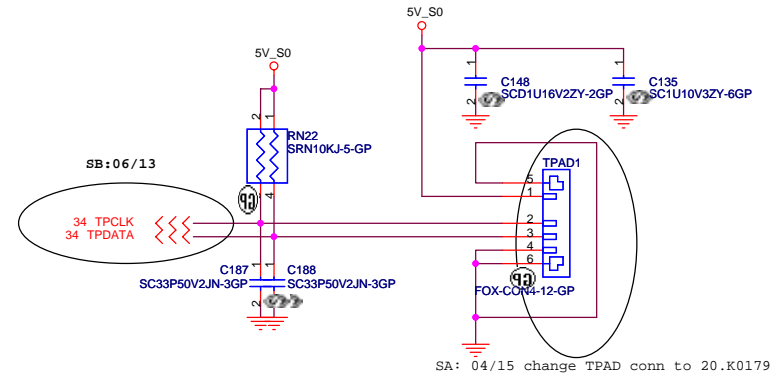
<<< KROW[0..7] 34

>>> KCOL[0..16] 34

Internal Keyboard Connector

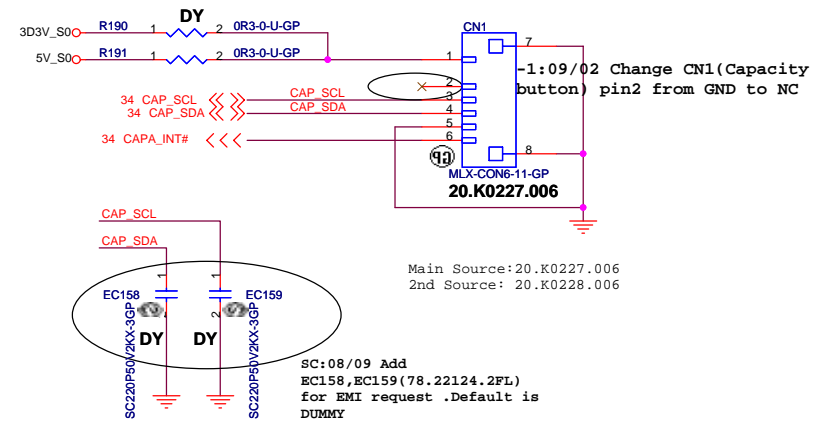


TouchPad Connector



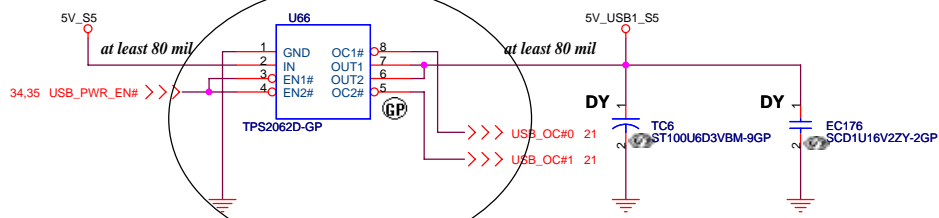
SA: 04/15 change TPAD conn to 20.K0179.004

CAPACITY BUTTON



<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>KeyBoard-CONN</b>			
Size A3	Document Number	Rev -1	
		<b>DS2-Intel</b>	
Date: Wednesday, September 12, 2007			
		Sheet 37	of 47



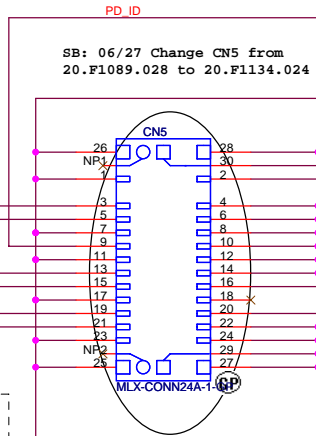
-1:08/30 Add U66 power switch to control USB power

### Left I/O Connector

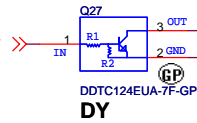
CONN 24PIN(AC-In+USB)

Reserved for EMI

Place near DCIN1

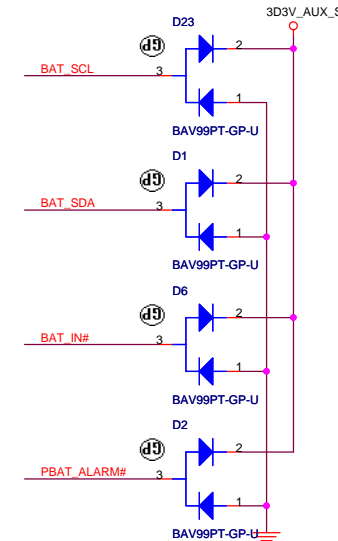
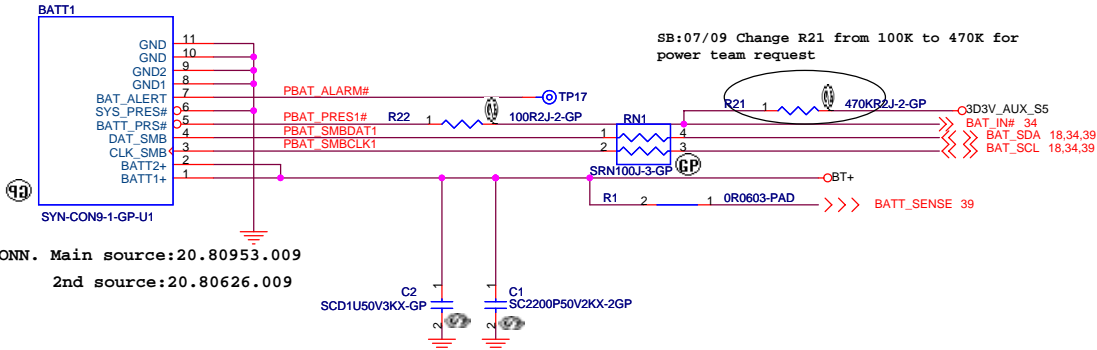


This cap should be used only as last resort for EMI suppression.



### Left I/O Board to Board CONN

### Batt Connector

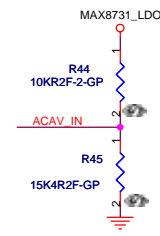


<Core Design>

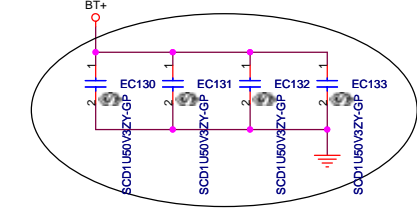
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size: A3	Document Number: <b>DS2-Intel</b>	Rev: -1
Date: Wednesday, September 12, 2007		
Sheet 38 of 47		

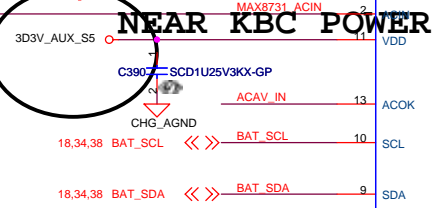
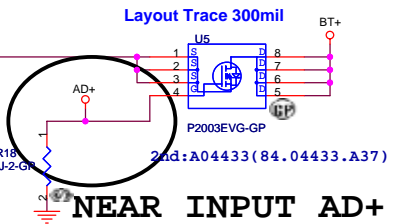
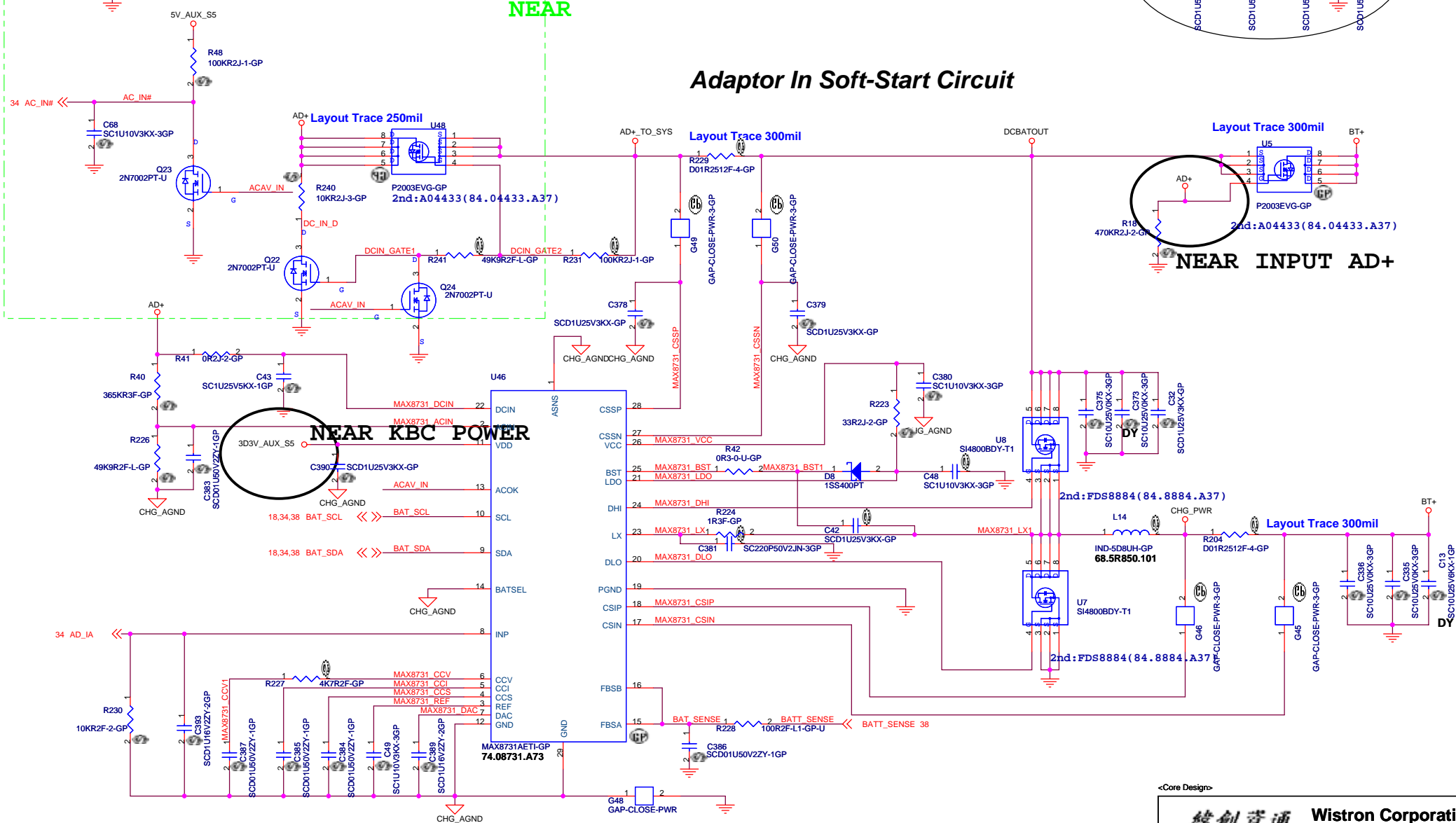


SB:06/29 Add  
 EC130, EC131, EC132, EC133 (78.10494.4BL)  
 for "BT+" by EMI request



**NEAR**

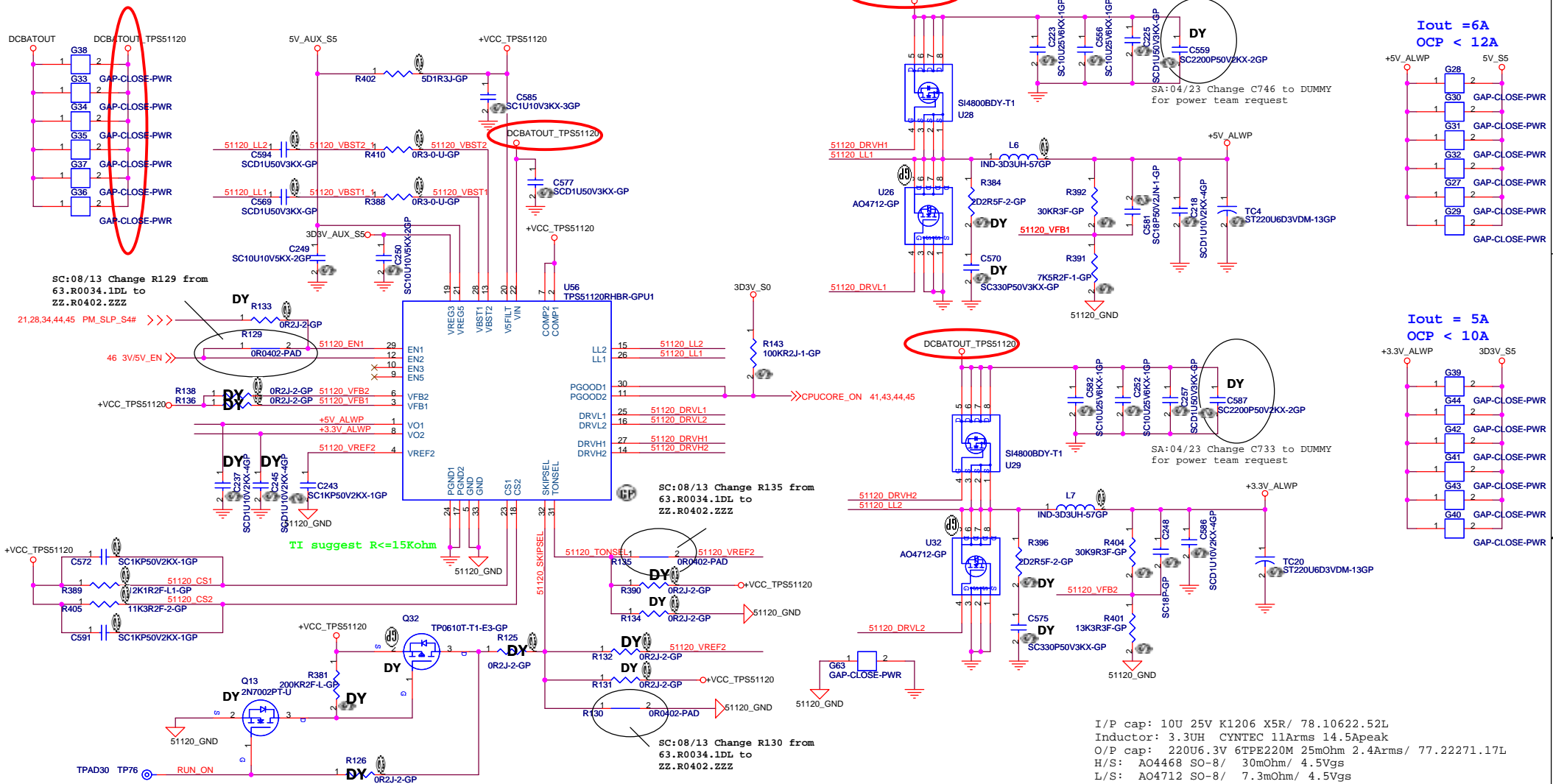
### Adaptor In Soft-Start Circuit



<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>CHARGER MAX8731</b>			
Size	Document Number	Rev	
Custom	<b>DS2-Intel</b>	<b>-1</b>	
Date: Wednesday, September 12, 2007		Sheet 39	of 47





Iout = 6A  
OCP < 12A

Iout = 5A  
OCP < 10A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: 3.3UH CYNTEC 11Arms 14.5Apeak  
 O/P cap: 220U6.3V 6TPE220M 25mOhm 2.4Arms/ 77.22271.17L  
 H/S: AO4468 SO-8/ 30mOhm/ 4.5Vgs  
 L/S: AO4712 SO-8/ 7.3mOhm/ 4.5Vgs

$$V_{out} = 1V * (R1 + R2) / R2$$

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

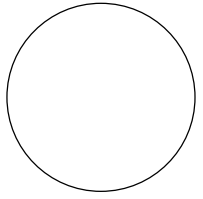
Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 3.3V & 5V**

Document Number: **DS2-Intel**

Date: Wednesday, September 12, 2007 Sheet 40 of 47

SB:06/17 Remove R205,C348,TP86 power monitor circuit.

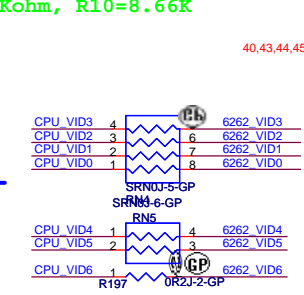


Place close to phase 1 choke

5 CPU\_PROCHOT#

470K /0402 size

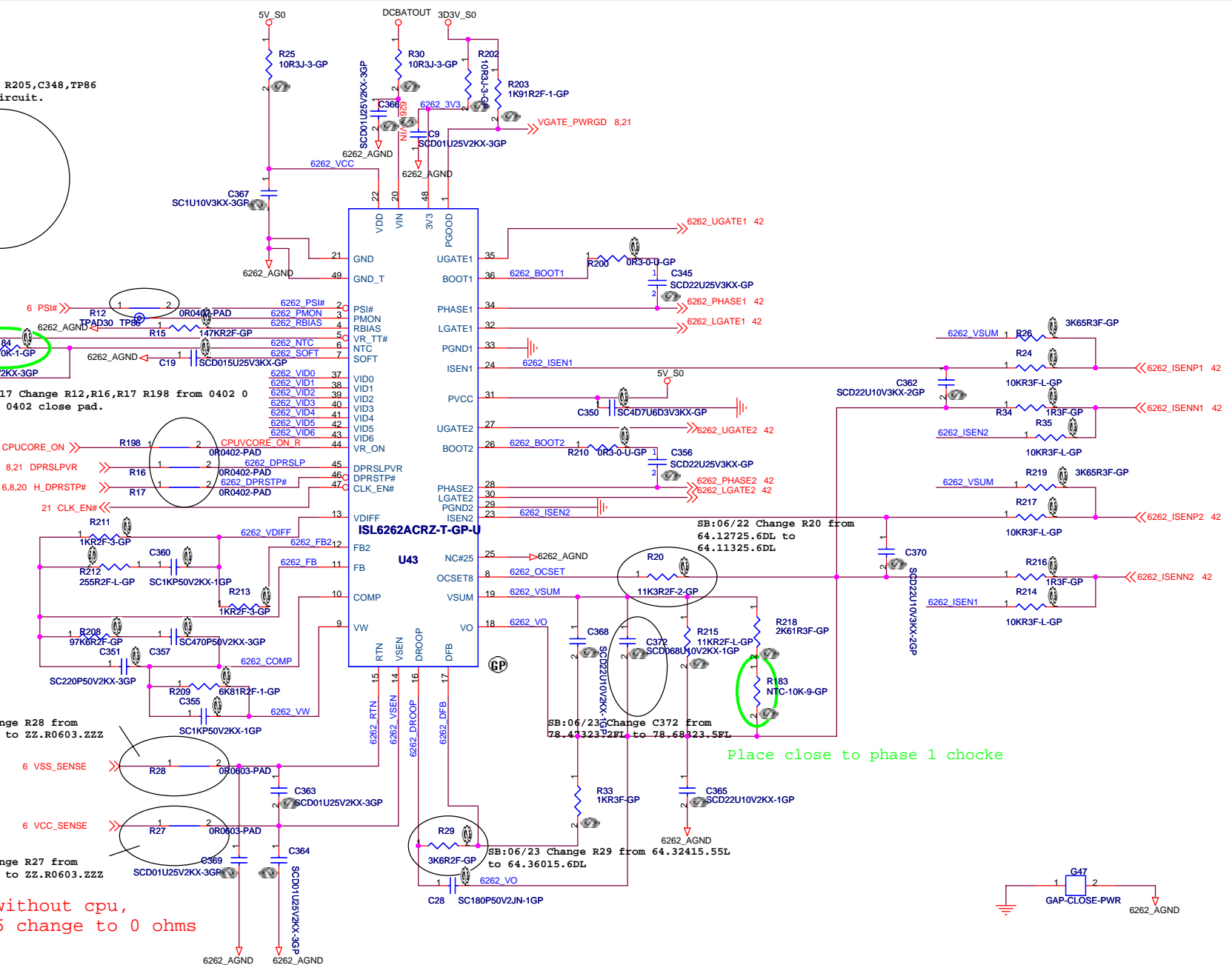
If NTC=330Kohm, R10=8.66K



SC:08/13 Change R28 from 63.00000.00L to ZZ.R0603.ZZZ

SC:08/13 Change R27 from 63.00000.00L to ZZ.R0603.ZZZ

When test without cpu, R483 & R486 change to 0 ohms



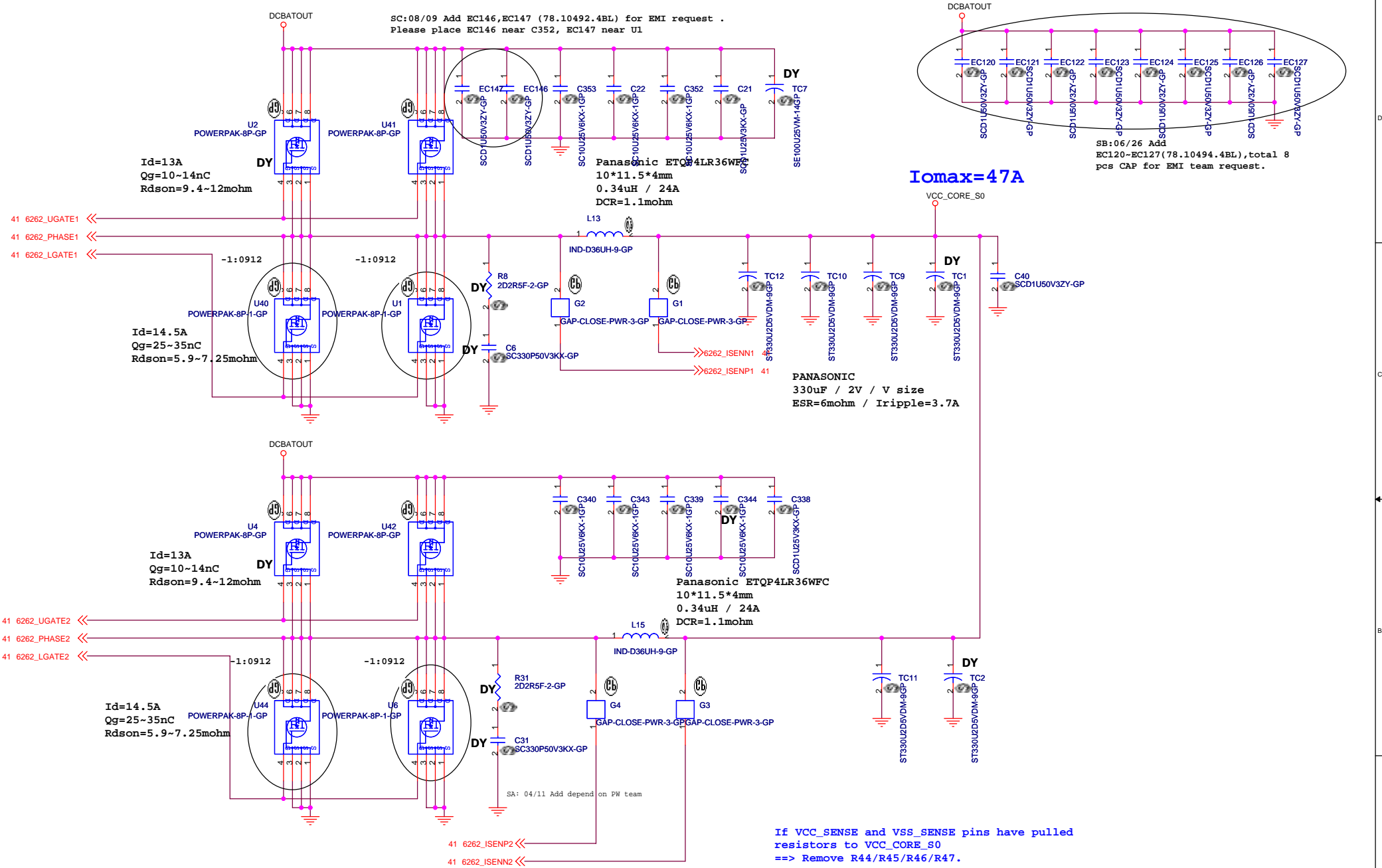
Place close to phase 1 choke

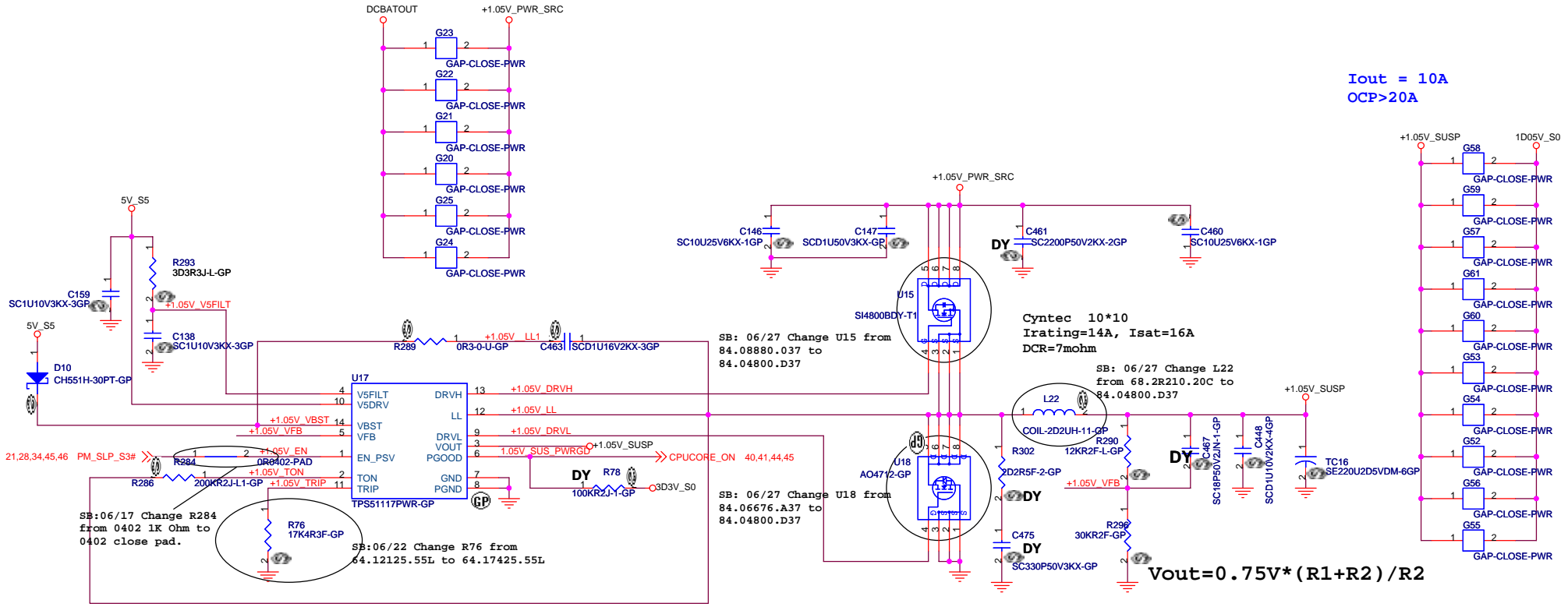
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC-DC VCCCPUCORE 1/2**

Size A3	Document Number	Rev -1
<b>DS2-Intel</b>		
Date: Wednesday, September 12, 2007	Sheet 41	of 47

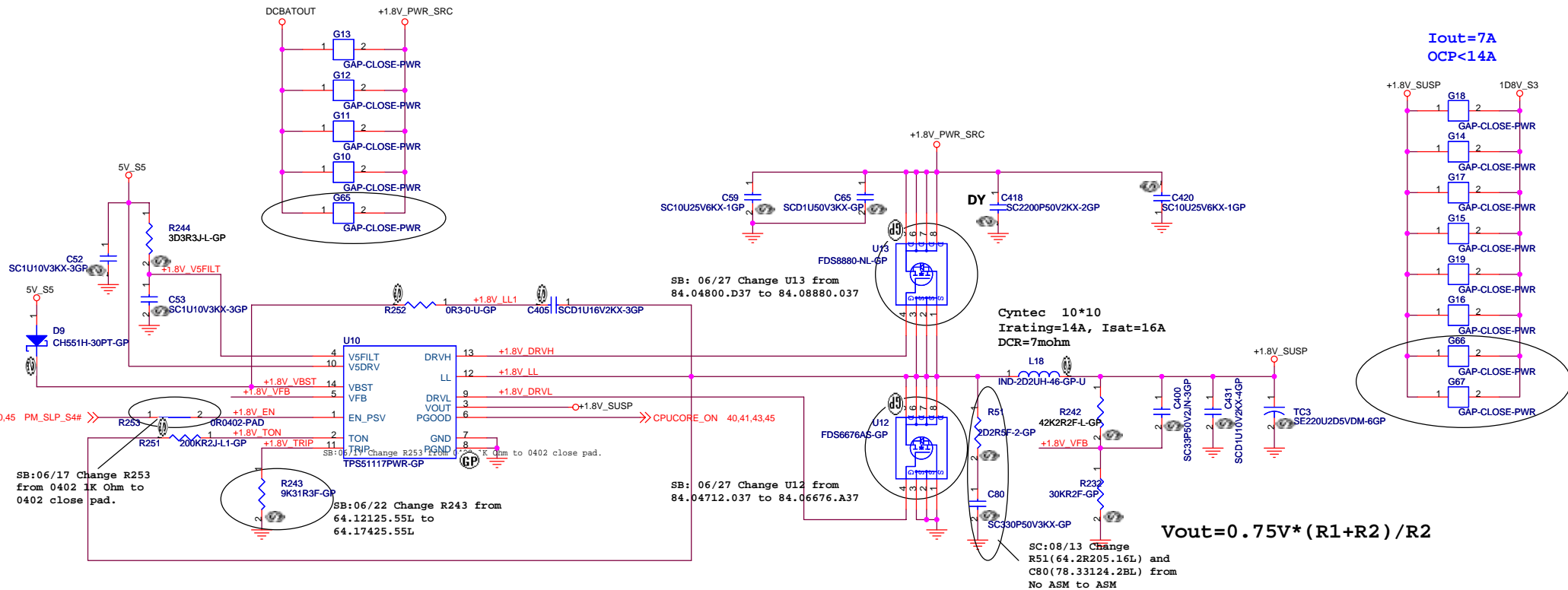




Iout = 10A  
OCP>20A

$$V_{out} = 0.75V * (R1 + R2) / R2$$

I/P cap: 10U 25V K1206 X5R / 78.10622.52L  
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I  
 O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms / 77.22271.161  
 H/S & L/S: FDS8884 SO-8 / 30mOhm / 4.5Vgs / 84.08884.037  
 L/S: FDS8896 SO-8 / 7.3mOhm / 4.5Vgs / 84.08896.037  
 Ton = 200Kohm --> 330KHz



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I  
 O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161  
 H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037  
 L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037  
 Ton = 200KOhm --> 330KHz

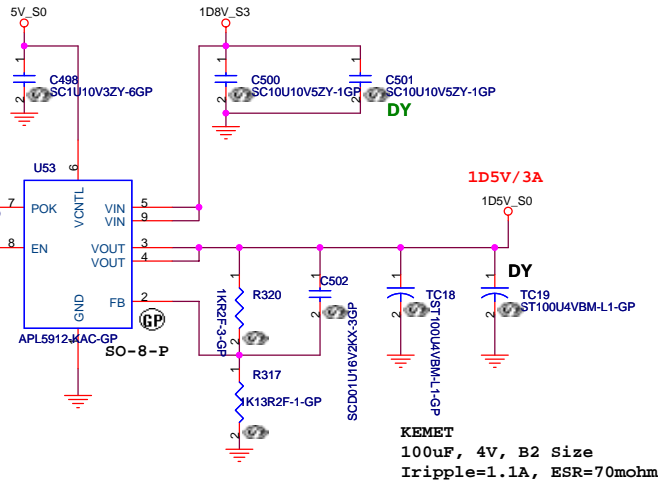
<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>DC/DC 1D8V</b>			
Size A3	Document Number		Rev -1
Date: Wednesday, September 12, 2007		Sheet 44 of 47	
<b>DS2-Intel</b>			

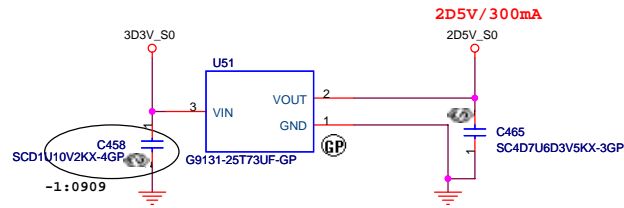
# 1D5V\_SB

SB:06/17 Change R315 from 0402 0 Ohm to 0402 close pad.

40,41,43,44 CPUCORE\_ON <<< R315 0R0402-PAD  
 21,28,34,43,46 PM\_SLP\_S3# >>>  
 $V_o = 0.8 * (1 + (R1/R2))$



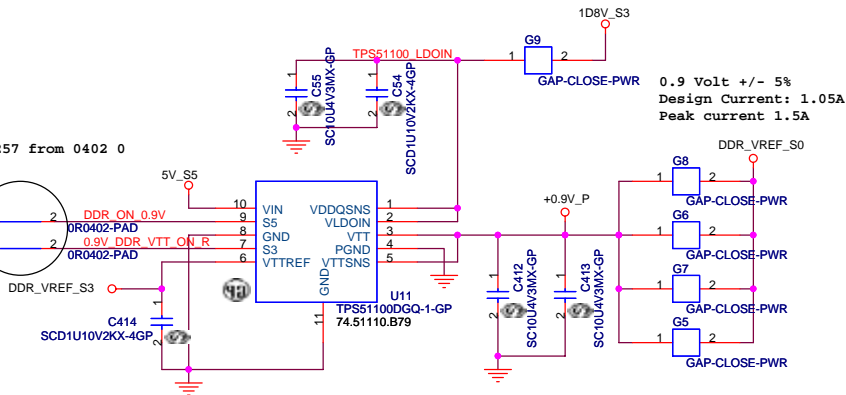
**KEMET**  
 100uF, 4V, B2 Size  
 Iripple=1.1A, ESR=70mohm



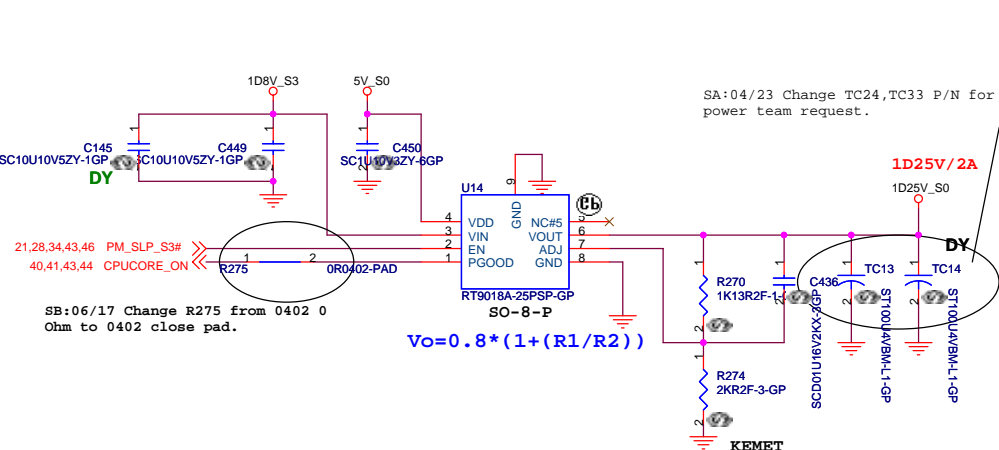
# SSID = PWR.Plane.Regulator\_0.9V

SB:06/17 Change R256,R257 from 0402 0 Ohm to 0402 close pad.

21,28,34,40,44 PM\_SLP\_S4# >>> R257 0R0402-PAD  
 21,28,34,43,46 PM\_SLP\_S3# >>> R256 0R0402-PAD



0.9 Volt +/- 5%  
 Design Current: 1.05A  
 Peak current 1.5A



SA:04/23 Change TC24,TC33 P/N for power team request.

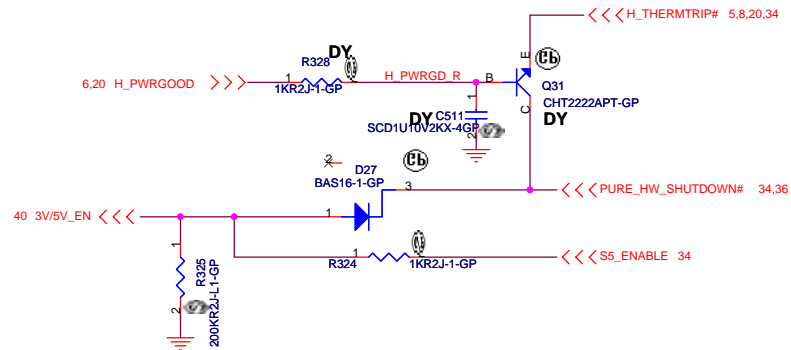
SB:06/17 Change R275 from 0402 0 Ohm to 0402 close pad.

$V_o = 0.8 * (1 + (R1/R2))$

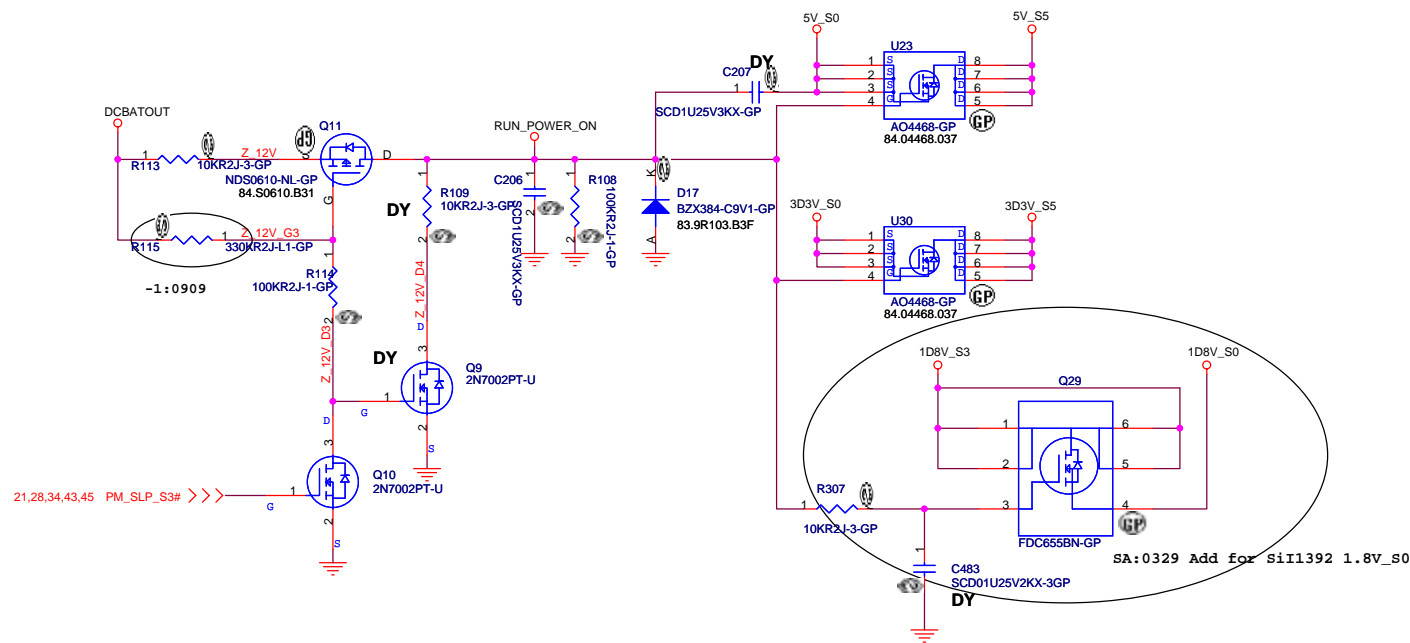
**KEMET**  
 100uF, 4V, B2 Size  
 Iripple=1.1A,  
 ESR=70mohm

Title		
<b>DC/DC 1D8V</b>		
Size	Document Number	Rev
A3	<b>DS2-Intel</b>	-1
Date: Wednesday, September 12, 2007 Sheet 45 of 47		

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.



# Run Power



<Core Design>

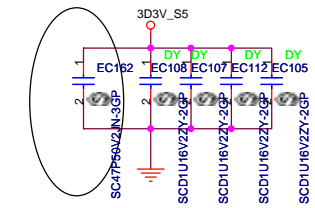
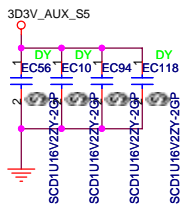
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWRPLANE&RESETLOGIC**

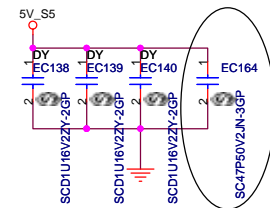
Size A3	Document Number	Rev
	<b>DS2-Intel</b>	<b>-1</b>

Date: Wednesday, September 12, 2007 Sheet 46 of 47

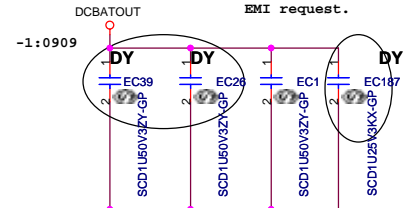
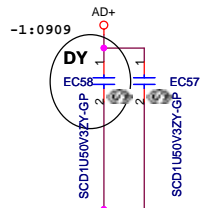




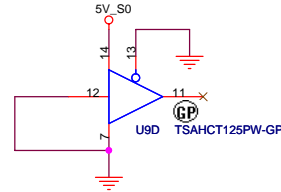
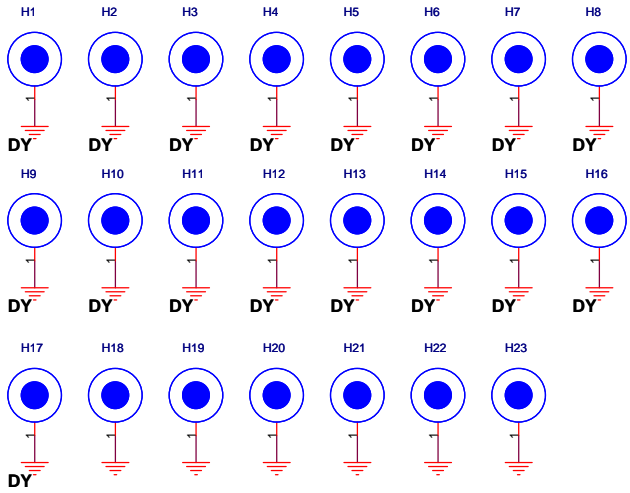
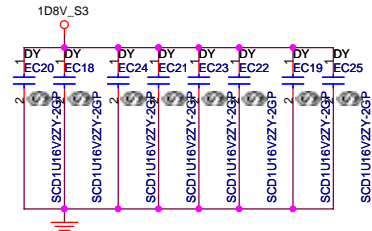
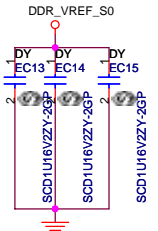
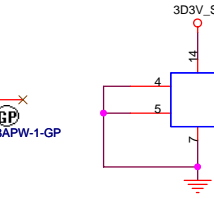
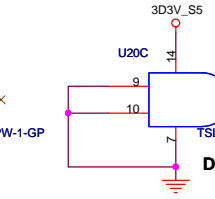
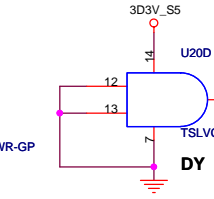
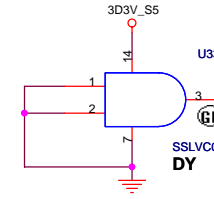
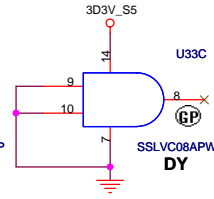
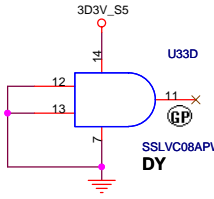
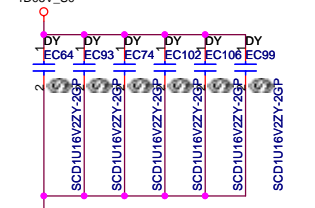
SC:08/11 Add EC162 on 3D3V\_S5 for RF team Request.



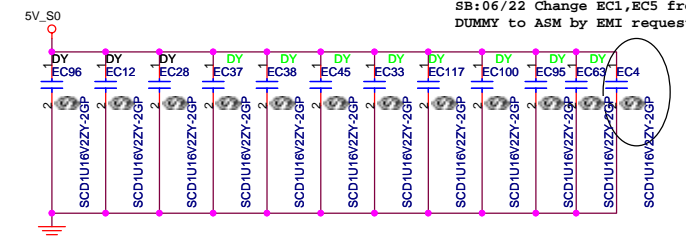
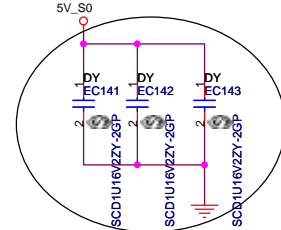
SC:08/11 Add EC164 on 5V\_S5 for RF team Request.



-1:0904 Add EC187(78.10422.2BL) for DCBATOUT decoupling, this is for EMI request.

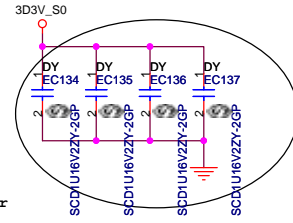


SB:06/29 Add EC141, EC142, EC143 (78.10491.4FL) for EMI request



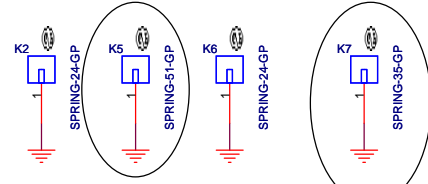
SB:06/22 Change EC1, EC5 from DUMMY to ASM by EMI request.

SB:06/29 Add EC134, EC135, EC136, EC137 (78.10491.4FL) for EMI request

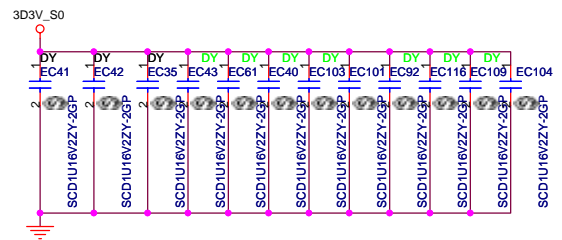


SC:08/09 Change K5 spring from 34.45T31.001 to 34.4B312.002 for ME request

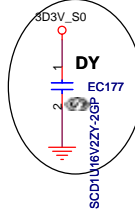
Place this spring near U40(bottom side)



SC:08/11 Change K7 from 34.39S07.001 to 34.41P18.001. This change is for EMI request



SC:08/15 Add EC177(78.10491.4FL) on 3D3V\_S0, this is for EMI request. Default is DY



<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: \_\_\_\_\_

Size: A3 Document Number: **MISC DS2-Intel** Rev: **-1**

Date: Wednesday, September 12, 2007 Sheet: 47 of 47