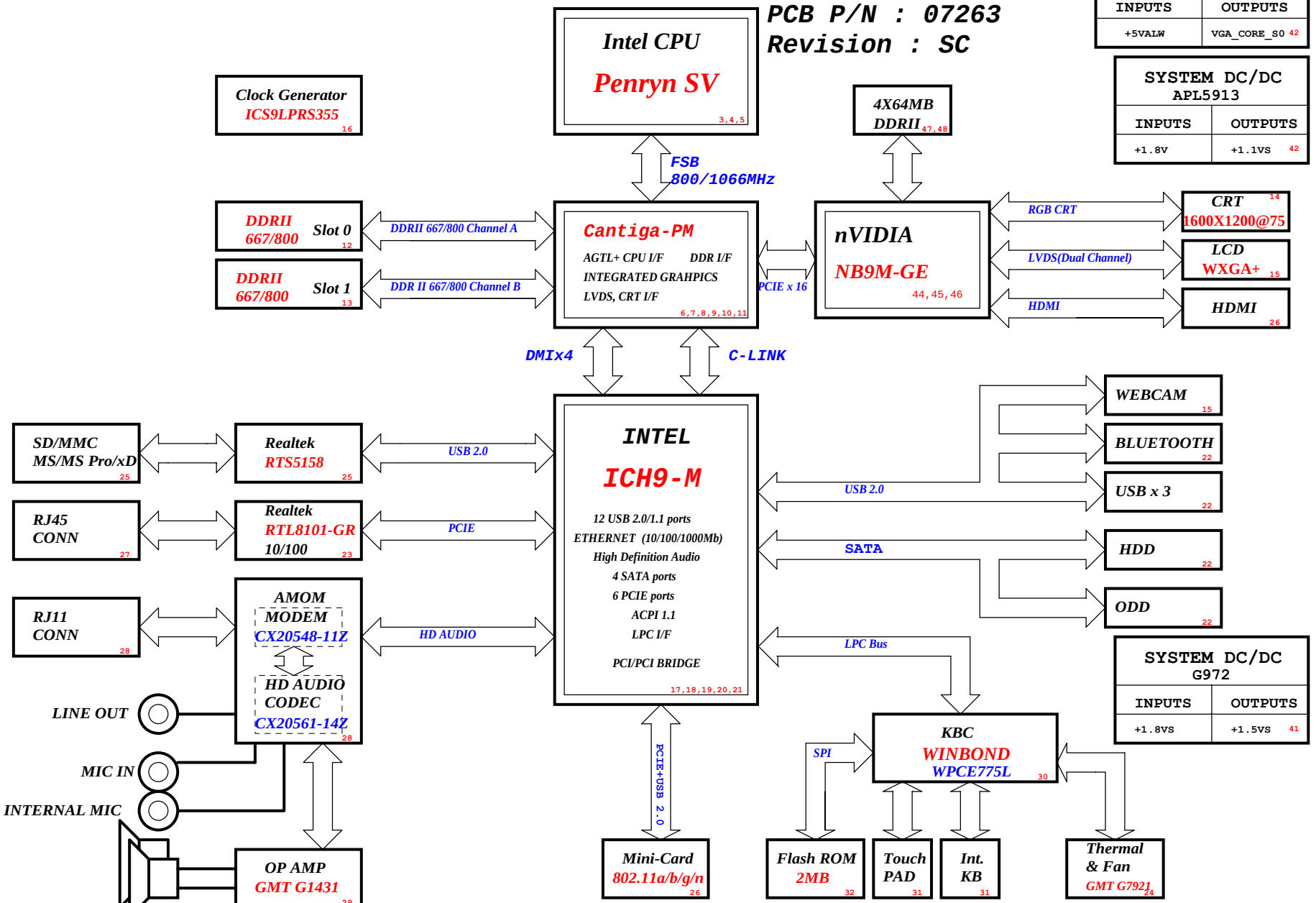
VITAS Block Diagram

Project code : 91.4I501.001
PCB P/N : 07263
Revision : SC



VGA DC/DC SC421A	
INPUTS	OUTPUTS
+5VALW	VGA_CORE_S0 42

SYSTEM DC/DC APL5913	
INPUTS	OUTPUTS
+1.8V	+1.1VS 42

SYSTEM DC/DC TPA51125	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 38

SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V 39

SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS
+5VALW	+1.05V 40

MAXIM CHARGER MAX8731	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 36

CPU DC/DC ISL6260CCRZ	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A 36,37

SYSTEM DC/DC G972	
INPUTS	OUTPUTS
+1.8VS	+1.5VS 41

PCB LAYER

L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4
L7:	GND
L8:	Signal 5

<Core Design>

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Title: **Block Diagram**

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

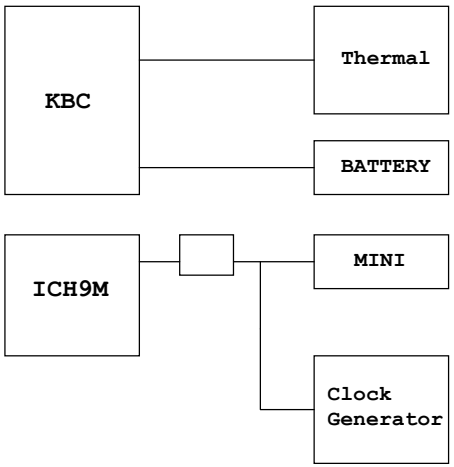
PCIE Routing page 19

LANE1	**LAN**
LANE2	**MiniCard WLAN**

USB Table page 19

USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus



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Title: ***Table of Content***

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Reserve for ITP, when install ITP connector, install R338.

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

Connect to V Core

4/23 Houston

PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)

ITP Connector

Reserve for ITP

<Core Design> Place R310 with in 200ps (~1") to CPU

62.10079.001

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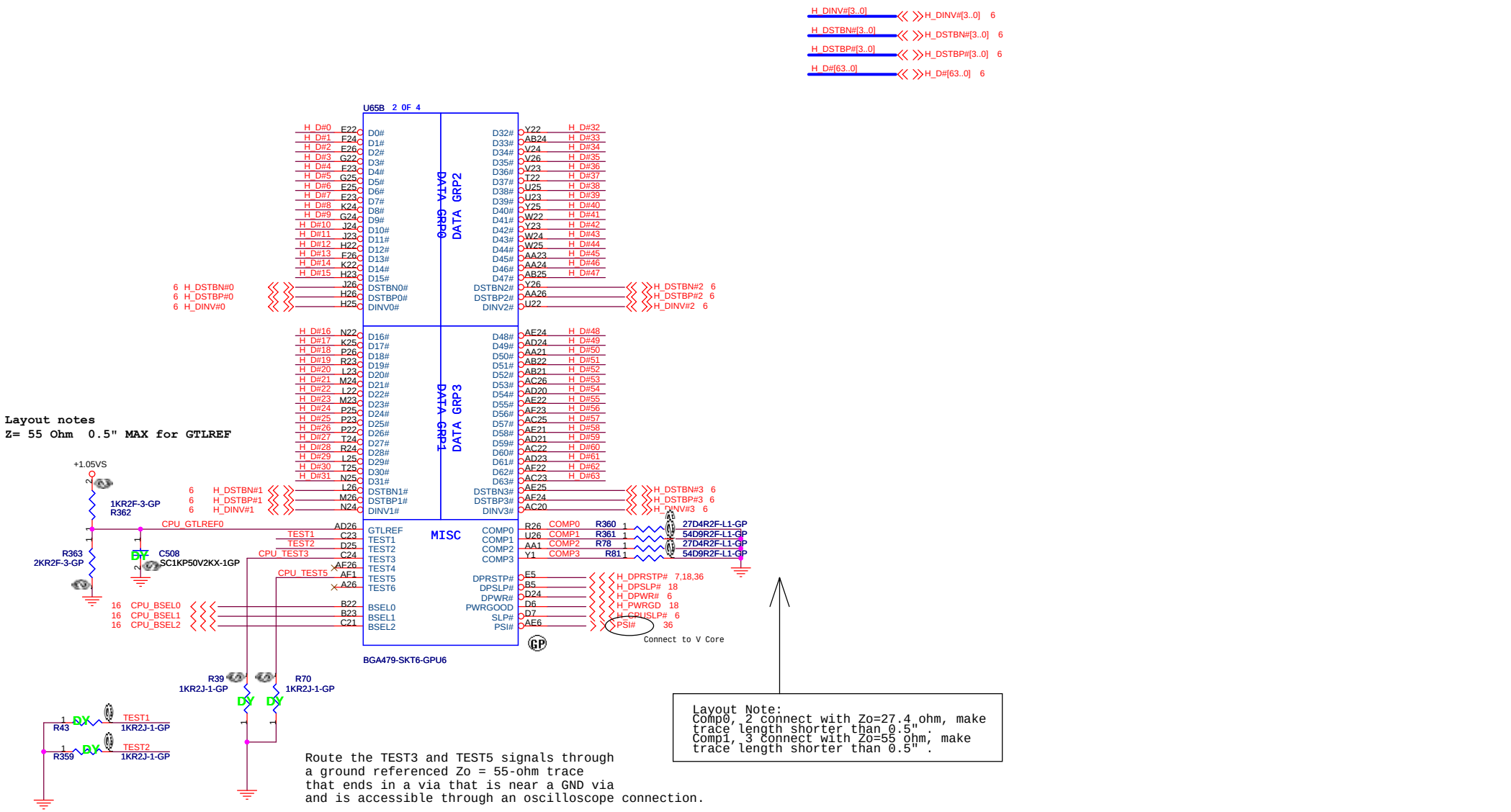
Title	CPU (1 of 2)
Size	Document Number: VITAS
Rev	SA
Date: Monday, May 05, 2008	Sheet 3 of 48



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Title		
CPU (3 of 2)		
Size	Document Number	Rev
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Please these inside socket cavity on L8(North side Secondary)

Please these inside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(North side Primary)

Please these outside socket cavity on L8(North side Secondary)

Please these outside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(South side Primary)

Please these inside socket cavity on L8(North side Secondary)

0128 DB

0429 PV

U65C 3 0F 4

BGA479-SKT6-GPU6

U65D 4 0F 4

BGA479-SKT6-GPU6

TC3 ST220U2D5VBM-LGP

SCD01U16V2KX-3GP

SC10U6D3V5MX-3GP

SC22U6D3V5MX-2GP

SCD1U10V2KX-4GP

R356 0R0603-PAD

R395 100R2F-L1-GP-U

R397 100R2F-L1-GP-U

layout note: "1D5V_VCCA_S0" as short as possible

Layout Note:
Place as close as possible to the CPU VCCA pin.

Connect to V Core

Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

H_VID[6..0] 36

VCC_SENSE 36

VSS_SENSE 36

NCTF PIN

TP67 TP166 TP71 TP165

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Title: CPU (3 of 3)

Size: | Document Number: VITAS | Rev: SA

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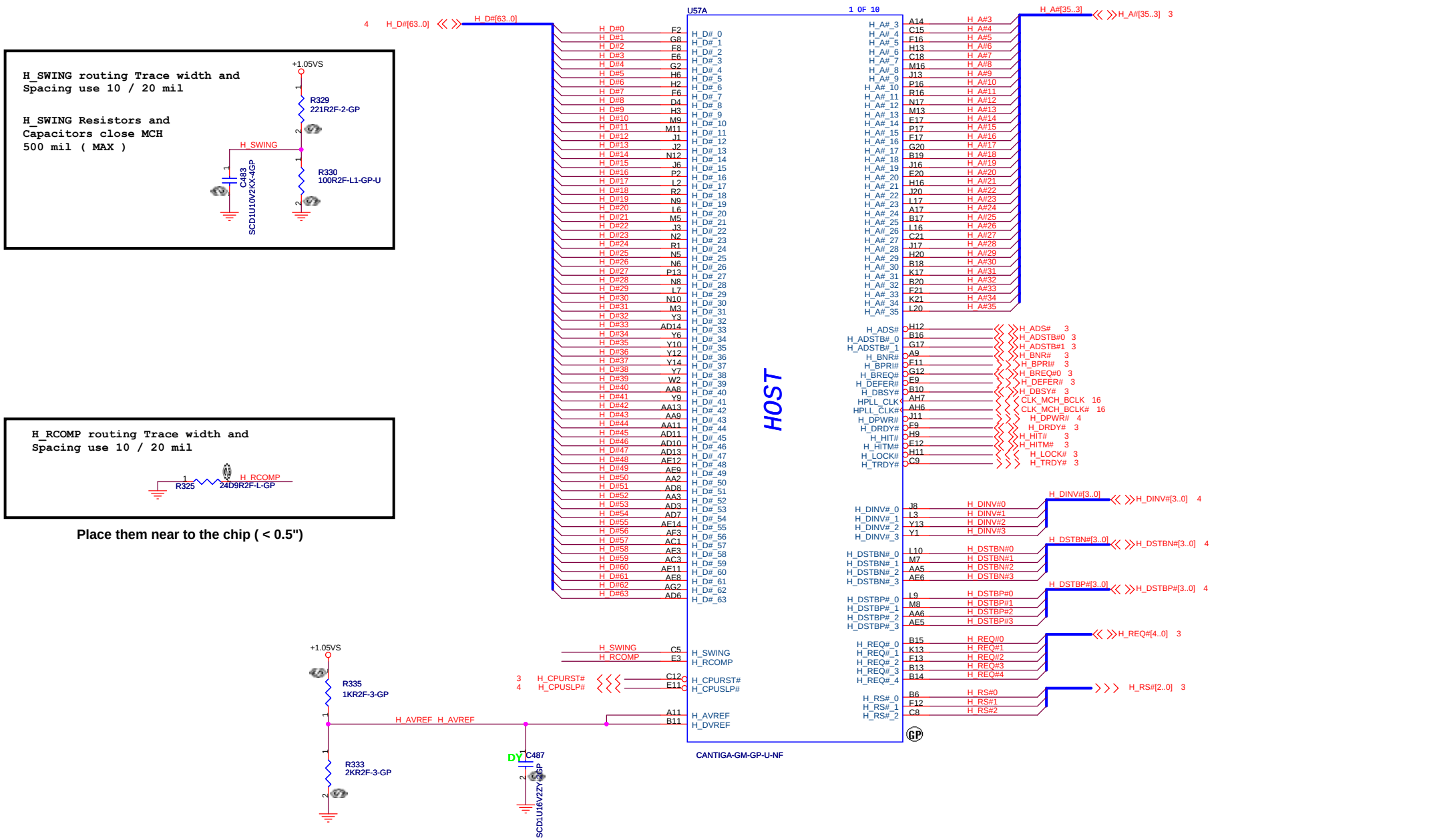

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Title: Cantiga (1 of 6)

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Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

U57B — 2 OF 10

RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA

CANTIGA-GM-GP-U-NF

U57C — 3 OF 10

PCI-EXPRESS GRAPHICS
SDVO
TV
VGA

CANTIGA-GM-GP-U-NF

FSB setting

DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

1011 DB

1015 DB

1107 DB

1113 DB

DDPC/SDVO for HDMI used

CL_VREF ~= 0.35V

Please Close GMCH

Please Close to U22

1218

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Title: Cantiga (2 of 6)

Size: Document Number: VITAS Rev: SA

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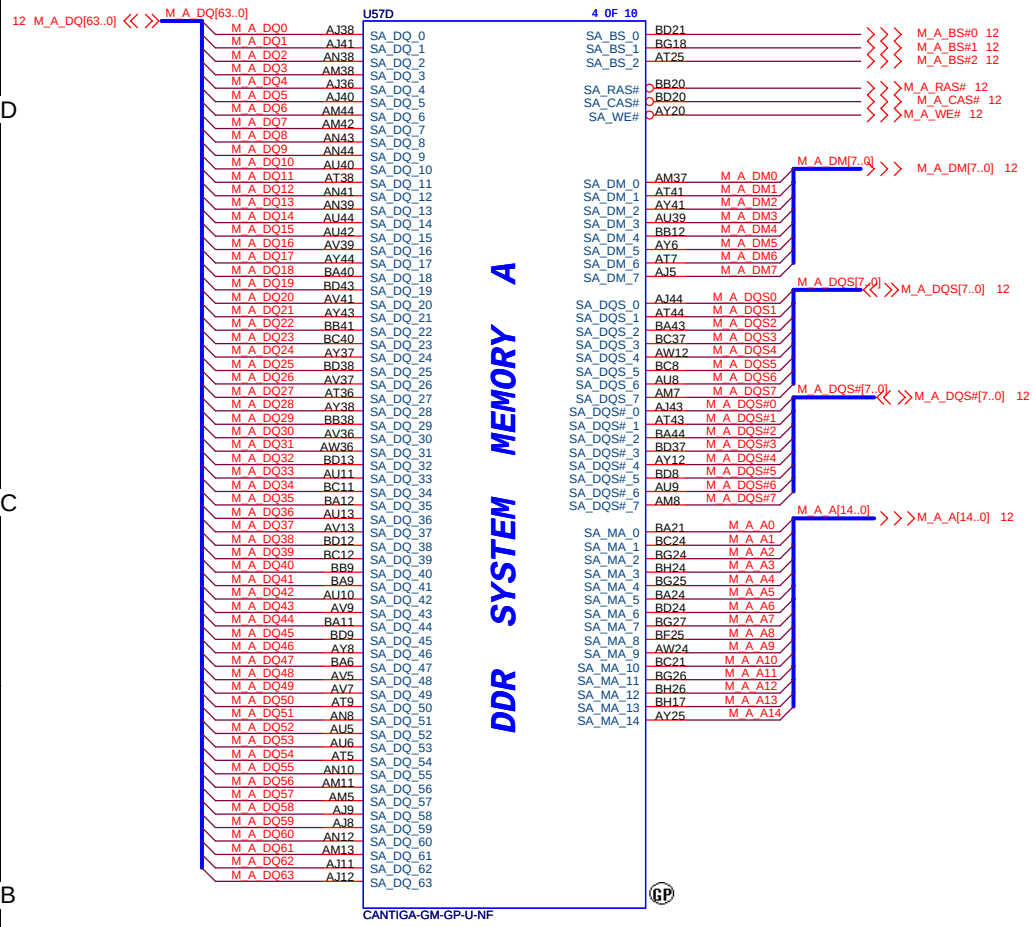

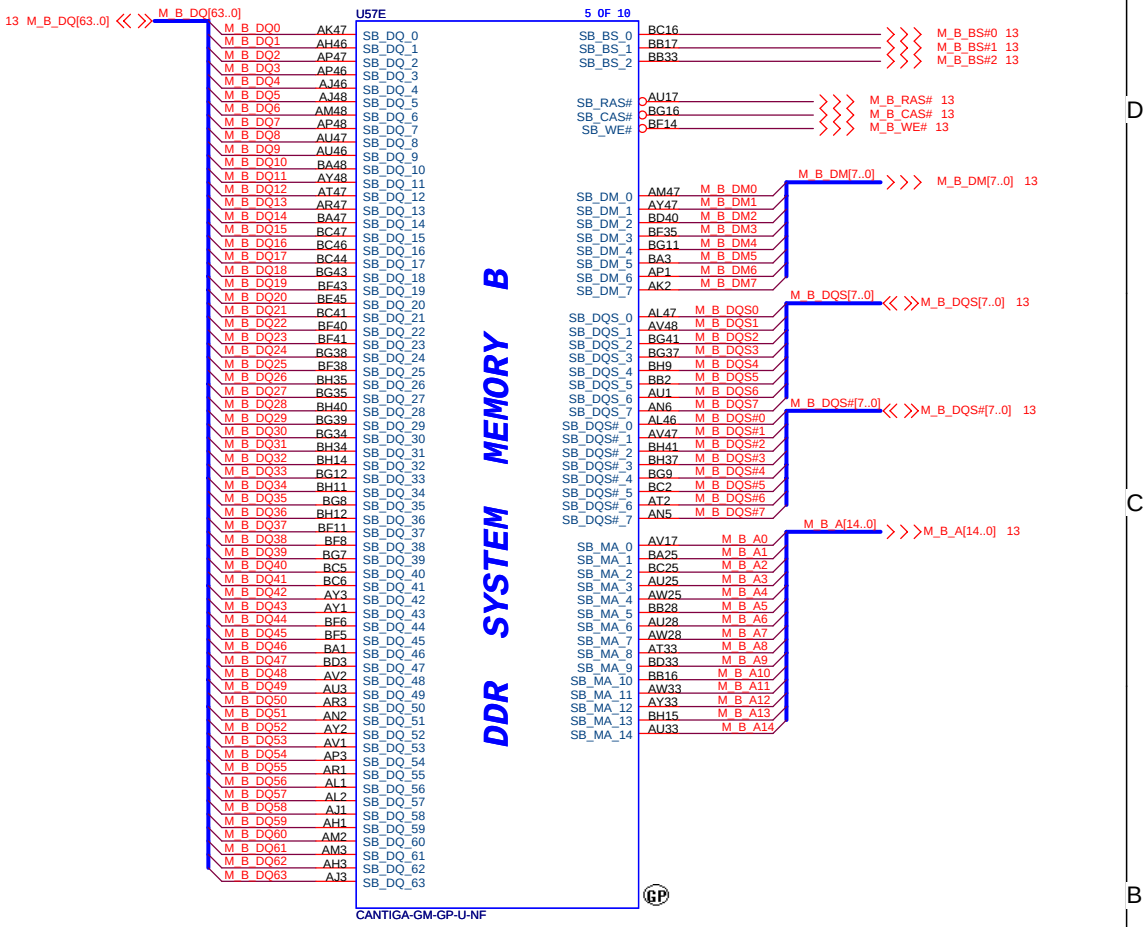

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Title: *Cantiga (3 of 6)*	
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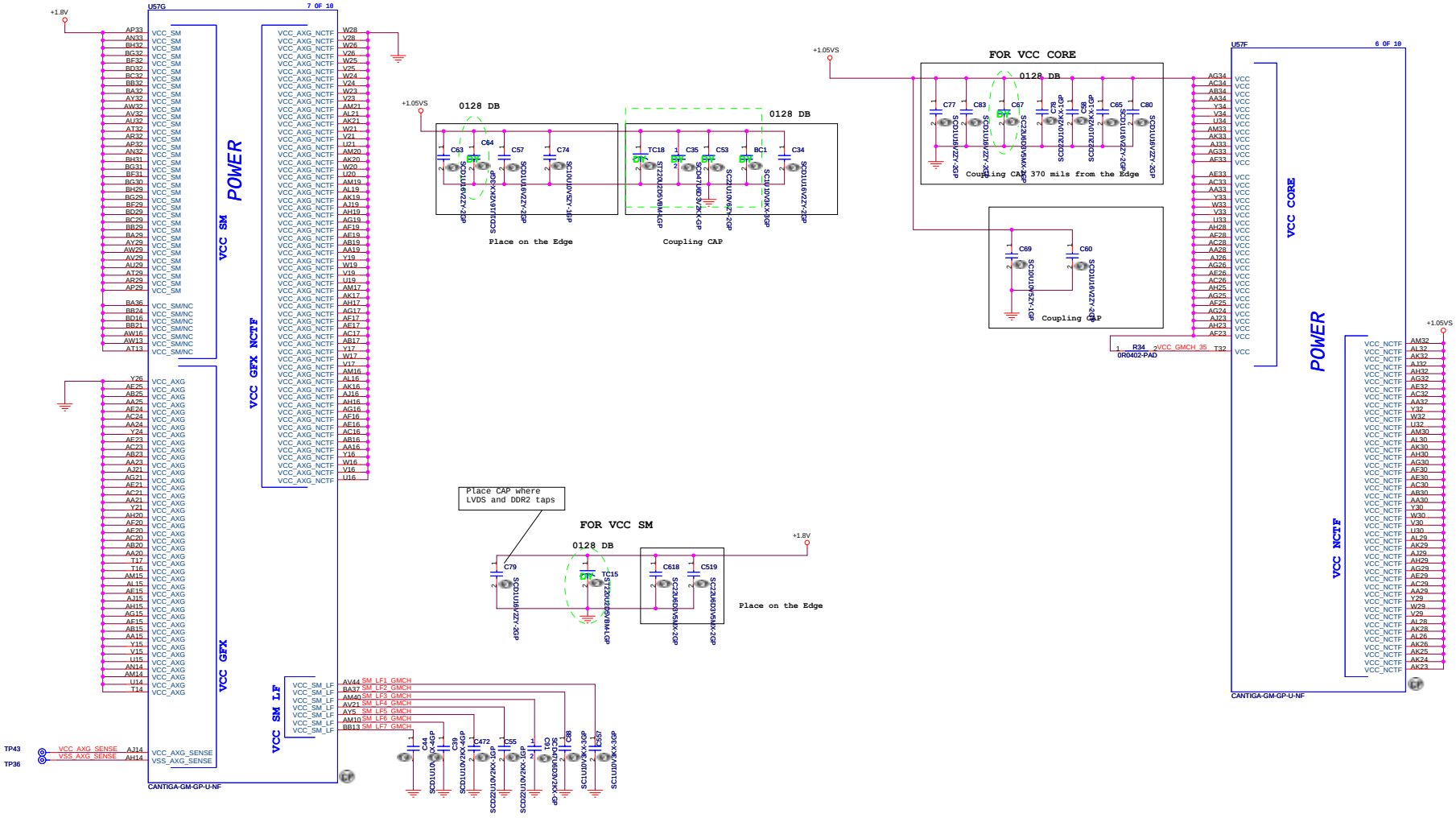

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Title	Cantiga (4 of 6)		
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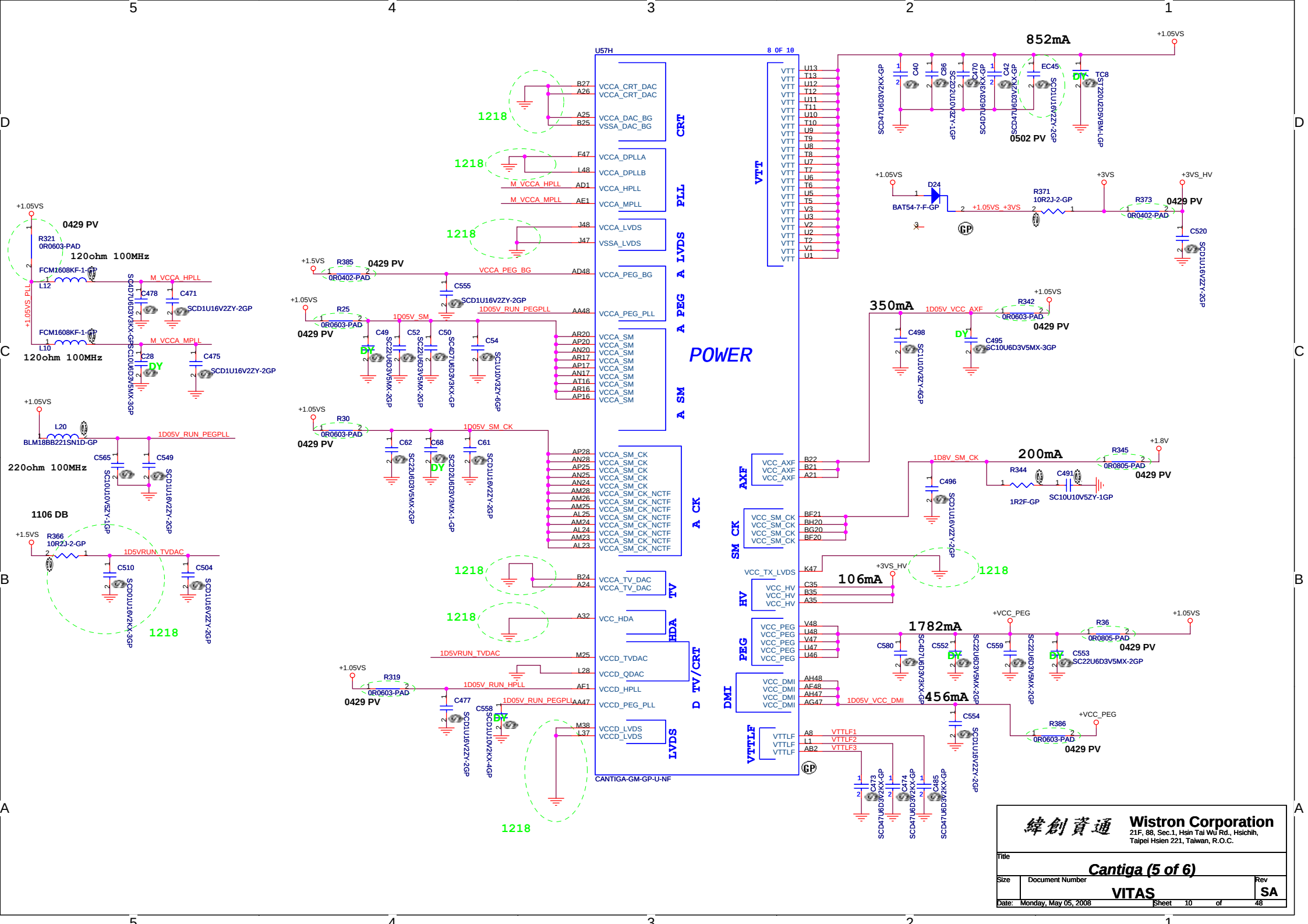
U57H
8 OF 10
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
PEG
HV
DMI
VTTLF
CANTIGA-GM-GP-U-NF
852mA
0502 PV
350mA
0429 PV
200mA
0429 PV
106mA
1782mA
456mA
0429 PV
1218
1106 DB
120ohm 100MHz
220ohm 100MHz
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Cantiga (5 of 6)
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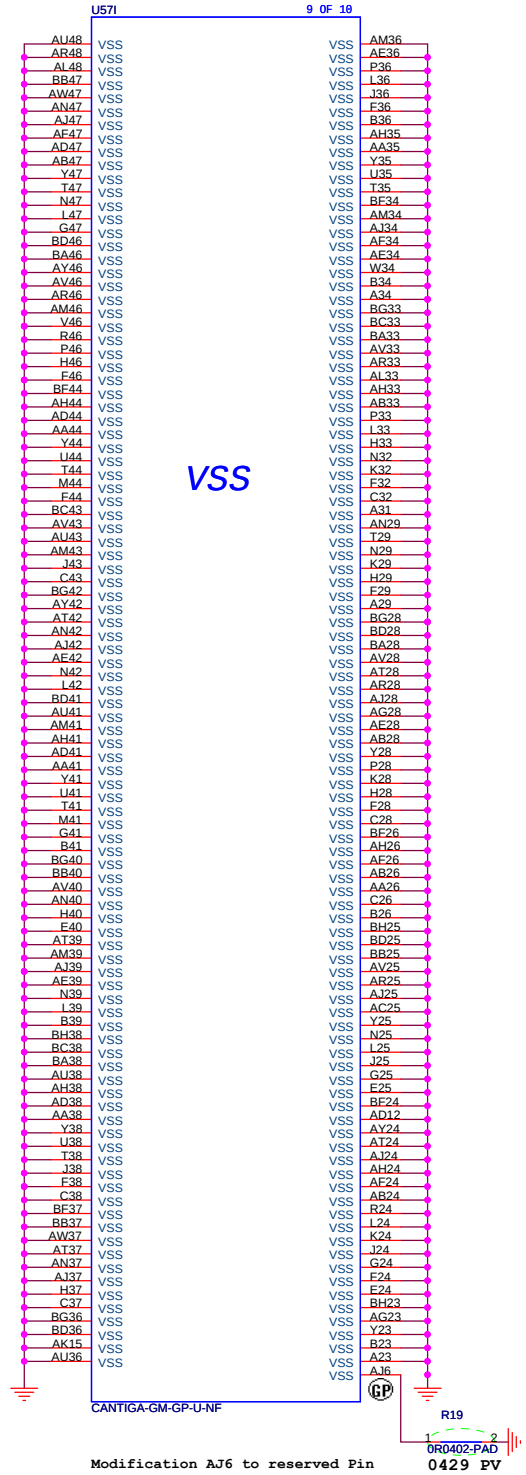

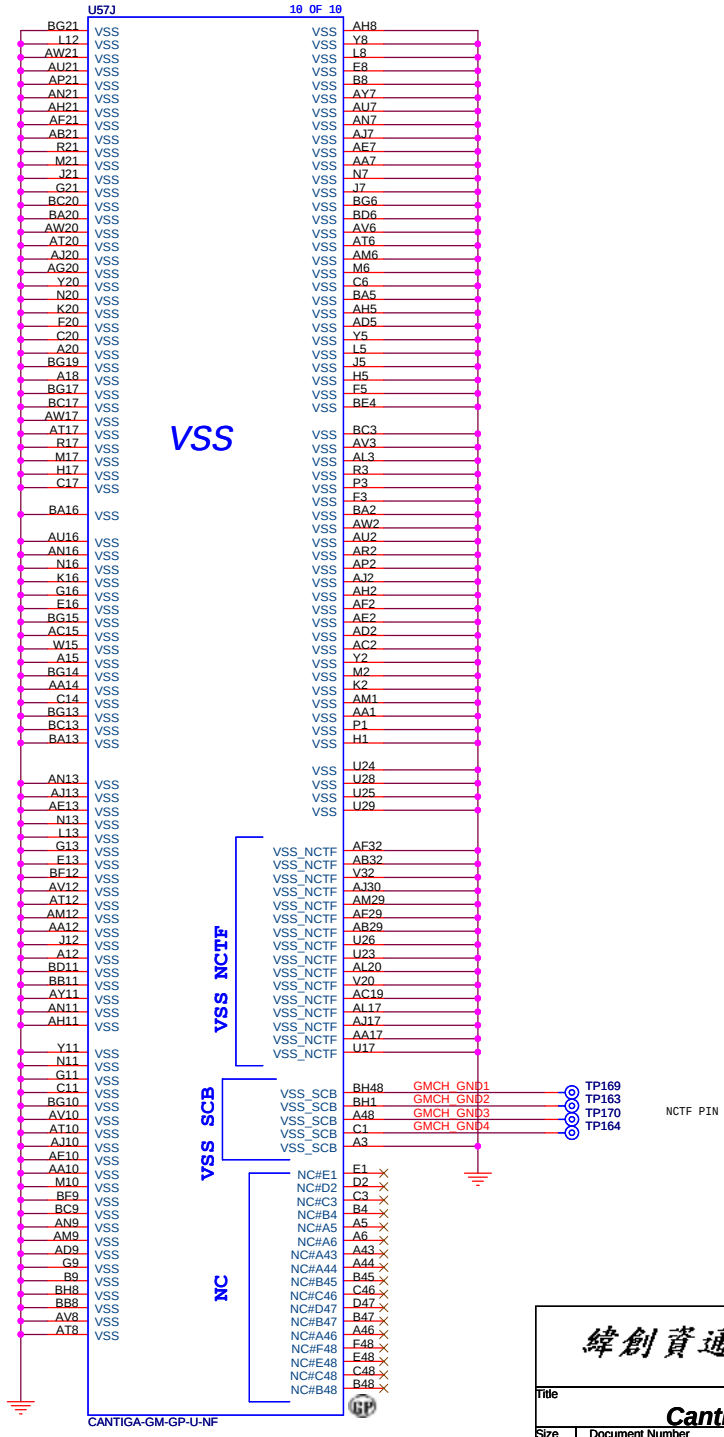

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Title: ***Cantiga (6 of 6)***

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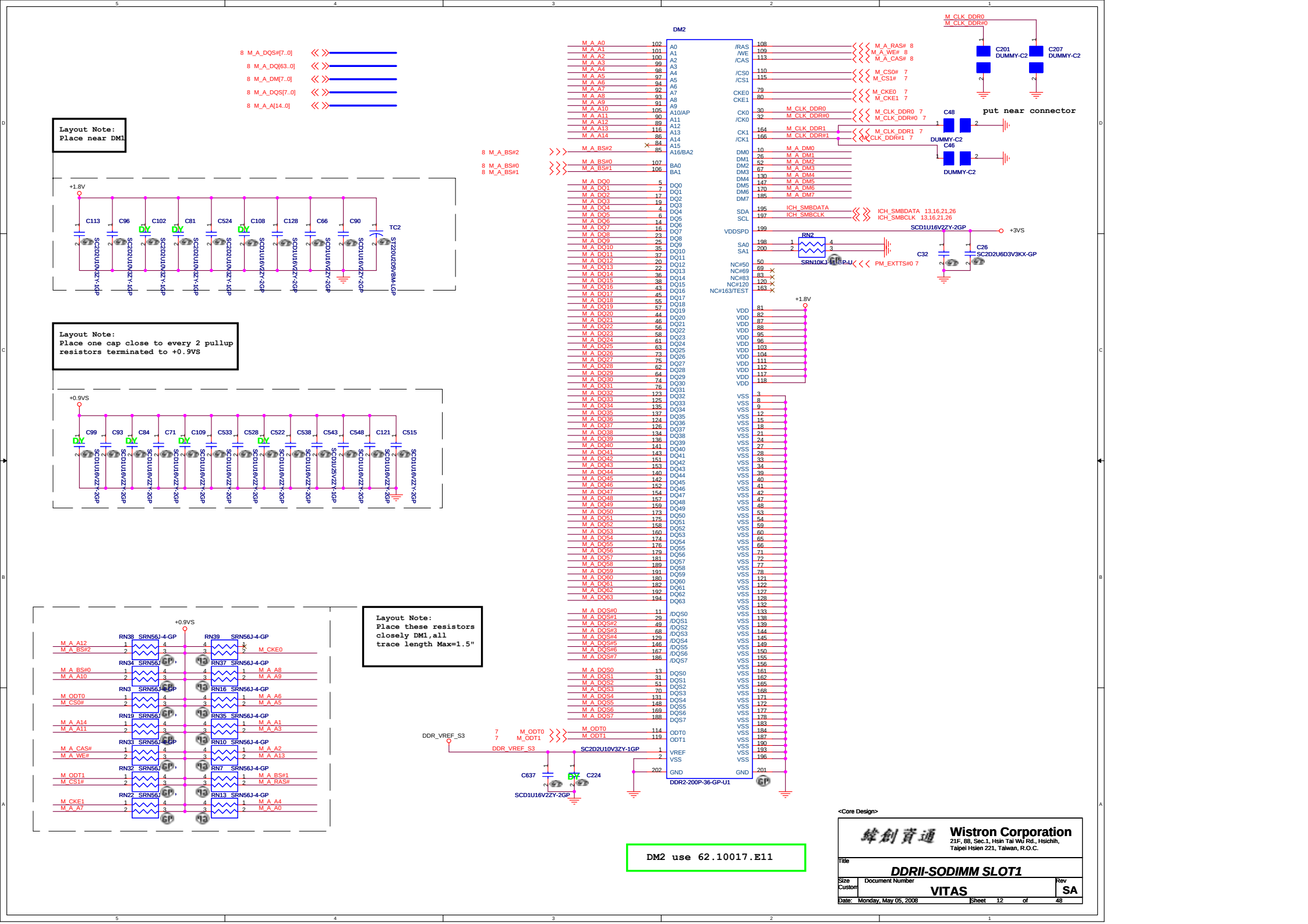
8 M_A_DQS#[7..0]
8 M_A_DQ[63..0]
8 M_A_DM[7..0]
8 M_A_DQS[7..0]
8 M_A_A[14..0]
Layout Note:
Place near DM1
+1.8V
C113 C96 C102 C81 C524 C108 C128 C66 C90 TC2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9VS
C99 C93 C84 C71 C109 C533 C528 C522 C538 C543 C548 C121 C515
+0.9VS
RN38 SRN56J-4-GP
RN39 SRN56J-4-GP
RN34 SRN56J-4-GP
RN37 SRN56J-4-GP
RN3 SRN56J-4-GP
RN16 SRN56J-4-GP
RN19 SRN56J-4-GP
RN35 SRN56J-4-GP
RN33 SRN56J-4-GP
RN10 SRN56J-4-GP
RN32 SRN56J-4-GP
RN7 SRN56J-4-GP
RN22 SRN56J-4-GP
RN13 SRN56J-4-GP
Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"
DM2
DDR2-200P-36-GP-U1
DDR_VREF_S3
SC2D2U10V3ZY-1GP
C637
C224
SCD1U16V2ZY-2GP
M_CLK_DDR0
M_CLK_DDR#0
C201 DUMMY-C2
C207 DUMMY-C2
C48 DUMMY-C2
C46 DUMMY-C2
put near connector
M_CLK_DDR1
M_CLK_DDR#1
RN2
SRN10K1-1-GP
PM_EXTTS#0 7
C32
C26 SC2D2U6D3V3KX-GP
SCD1U16V2ZY-2GP
+3VS
ICH_SMBDATA 13,16,21,26
ICH_SMBCLK 13,16,21,26
DM2 use 62.10017.E11
<Core Design>
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Size Custom
Document Number
VITAS
Rev SA
Date: Monday, May 05, 2008
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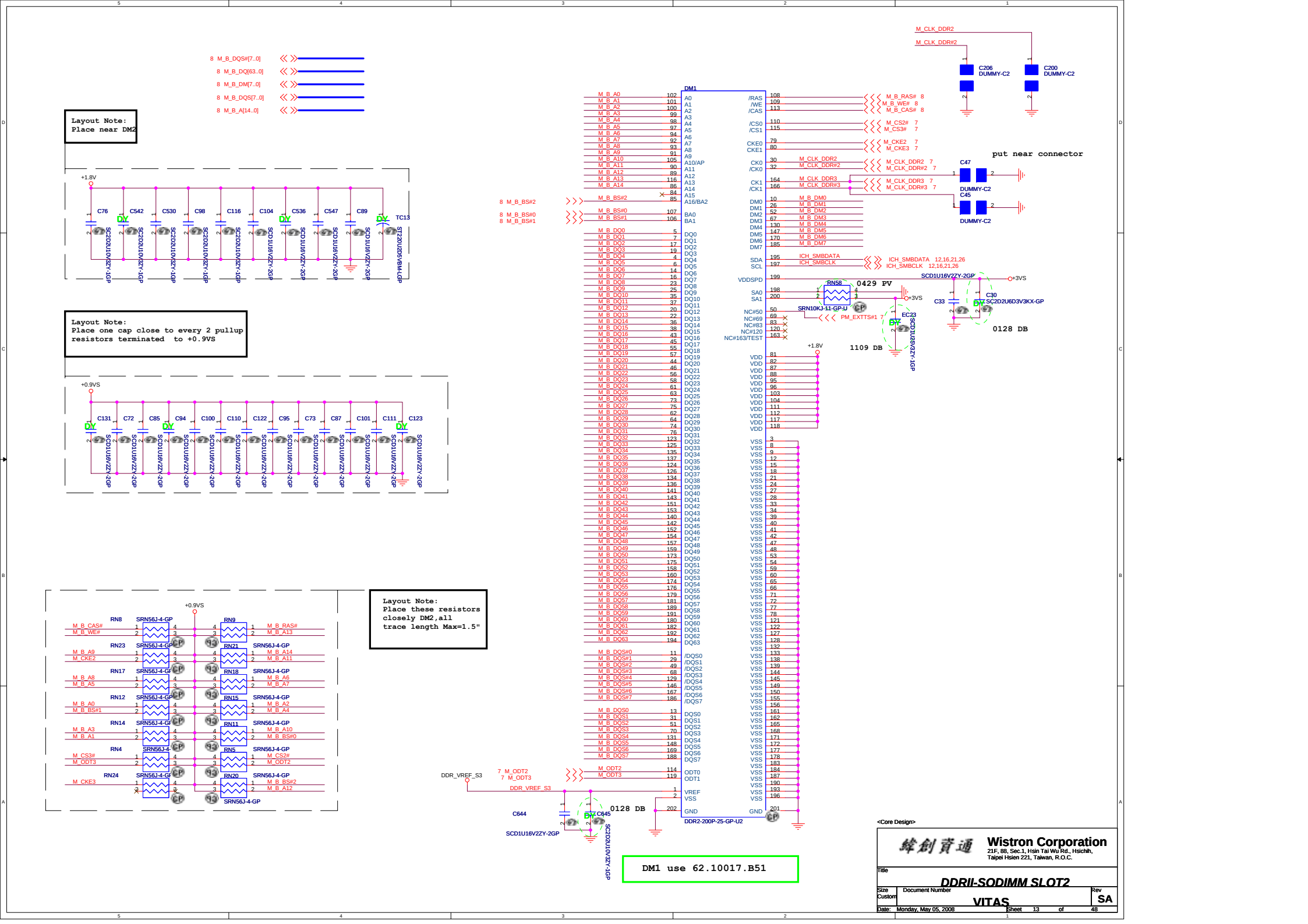
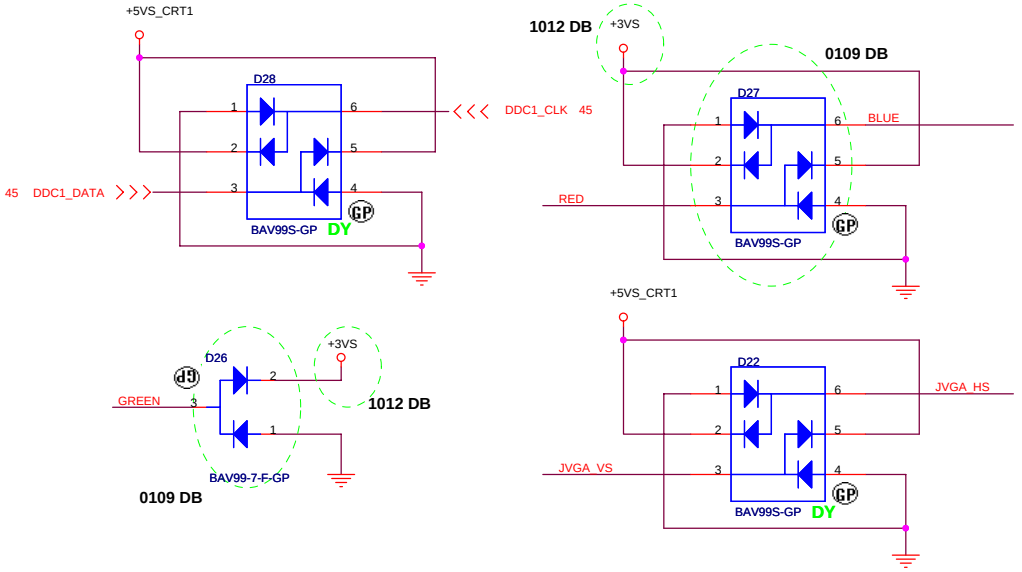
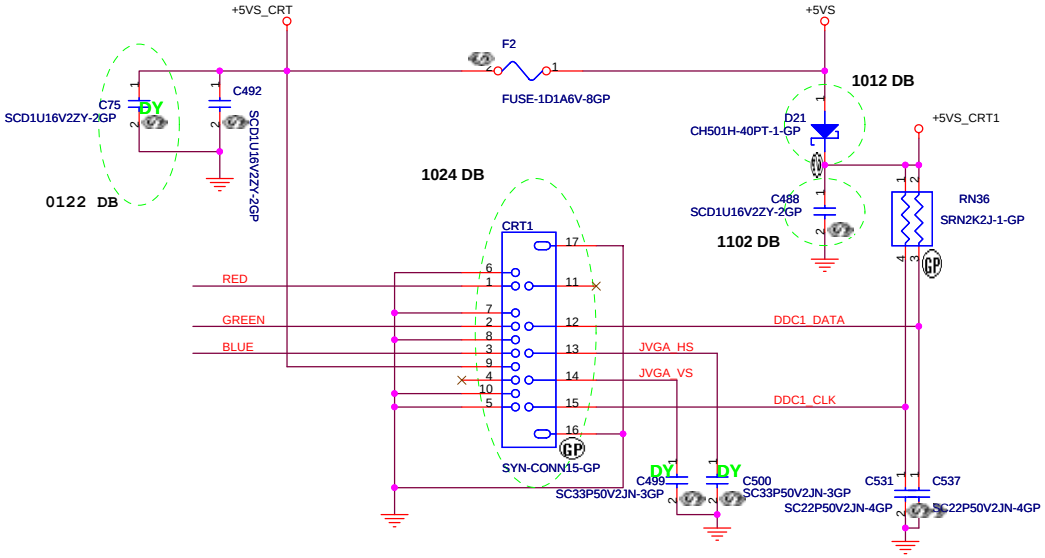
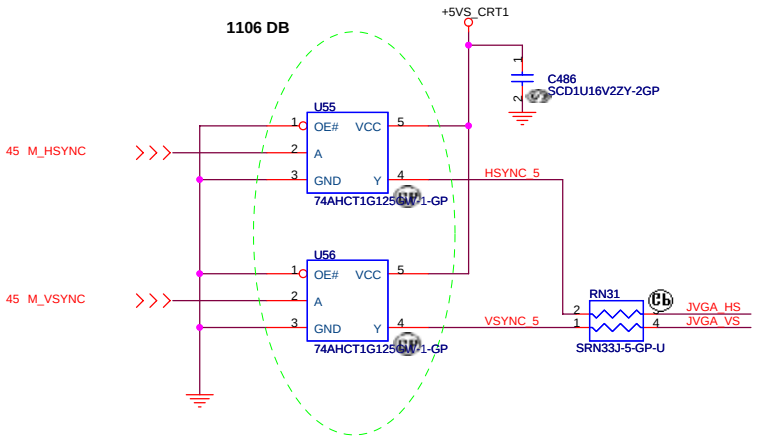

8 M_B_DQS#[7..0]
8 M_B_DQ[63..0]
8 M_B_DM[7..0]
8 M_B_DQS[7..0]
8 M_B_A[14..0]
Layout Note:
Place near DM2
+1.8V
C76 C542 C530 C98 C116 C104 C536 C547 C89 TC13
DY
SCD2DU0V2ZY-10GP
SCD1U16V2ZY-26P
ST220U2D5VBM4-GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9VS
C131 C72 C85 C94 C100 C110 C122 C95 C73 C87 C101 C111 C123
SCD1U16V2ZY-2GP
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
+0.9VS
RN8 SRN56J-4-GP
M_B_CAS#
M_B_WE#
M_B_RAS#
M_B_A13
RN23 M_B_A9 M_CKE2 M_B_A14 M_B_A11
RN17 M_B_A8 M_B_A5 M_B_A6 M_B_A7
RN12 M_B_A0 M_B_BS#1 M_B_A2 M_B_A4
RN14 M_B_A3 M_B_A1 M_B_A10 M_B_BS#0
RN4 M_CS3# M_ODT3 M_CS2# M_ODT2
RN24 M_CKE3 M_B_BS#2 M_B_A12
RN5 RN9 RN11 RN15 RN18 RN21 RN20
DM1
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14
M_B_BS#2
M_B_BS#0
M_B_BS#1
M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15 M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39 M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47 M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55 M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63
M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7
M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7
M_ODT2 M_ODT3
/RAS /WE /CAS
/CS0 /CS1
CKE0 CKE1
CK0 /CK0
CK1 /CK1
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
SDA SCL
VDDSPD
SA0 SA1
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
VDD VSS
VREF GND
DDR2-200P-25-GP-U2
M_B_RAS# 8
M_B_WE# 8
M_B_CAS# 8
M_CS2# 7
M_CS3# 7
M_CKE2 7
M_CKE3 7
M_CLK_DDR2 7
M_CLK_DDR#2 7
M_CLK_DDR3 7
M_CLK_DDR#3 7
ICH_SMBDATA 12,16,21,26
ICH_SMBCLK 12,16,21,26
PM_EXTTS#1 7
RN58 0429 PV
SRN10KJ-11-GP-U
EC23
1109 DB
C206 DUMMY-C2
C200 DUMMY-C2
C47
C45
DUMMY-C2
put near connector
SCD1U16V2ZY-2GP
C33
C30 SC2D2U6D3V3KX-GP
0128 DB
+3VS
+1.8V
DDR_VREF_S3
7 M_ODT2
7 M_ODT3
C644
C645
0128 DB
SCD1U16V2ZY-2GP
SC2D2U0V2ZY-1GP
DM1 use 62.10017.B51
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size Custom
Document Number
VITAS
Rev SA
Date: Monday, May 05, 2008
Sheet 13 of 48

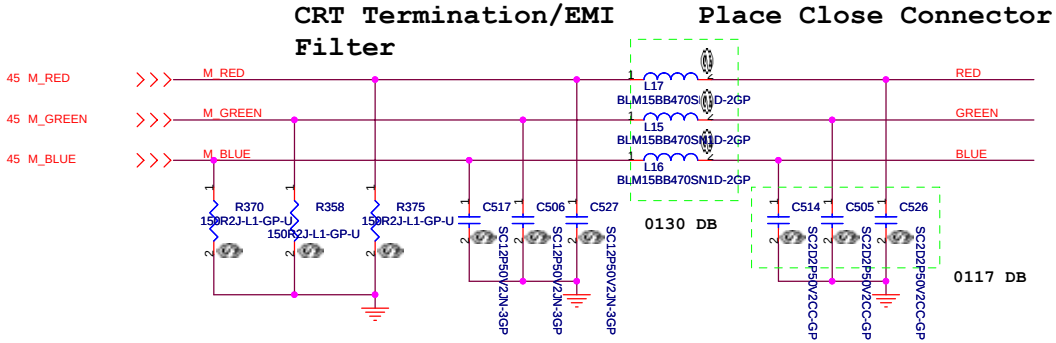
CRT I/F & CONNECTOR





Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





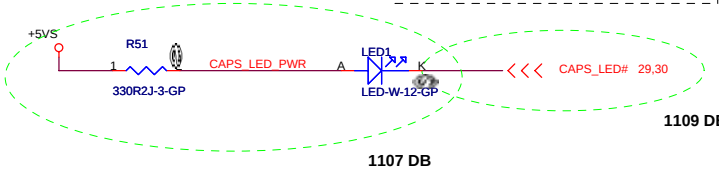
<Core Design>

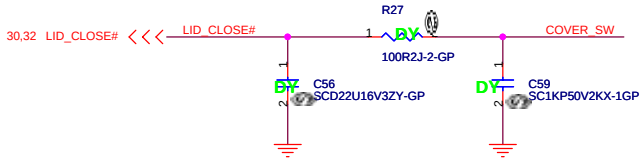
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

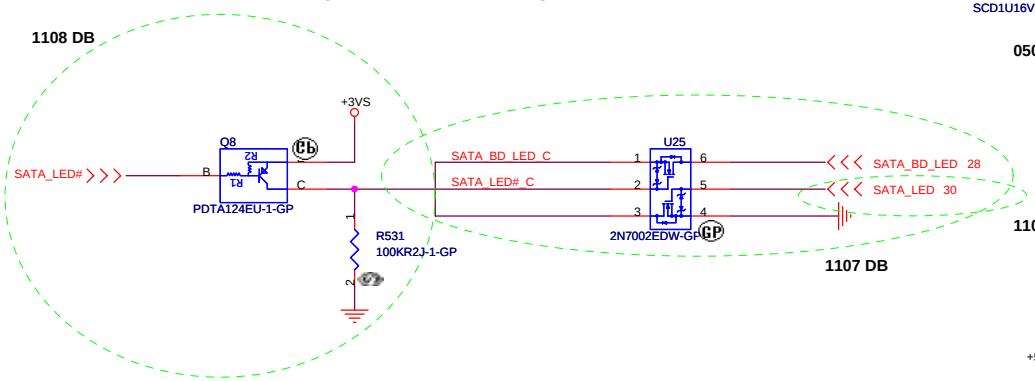
Title	CRT Connector	
Size A3	Document Number VITAS	Rev SA
Date: Monday, May 05, 2008	Sheet 14 of 48	

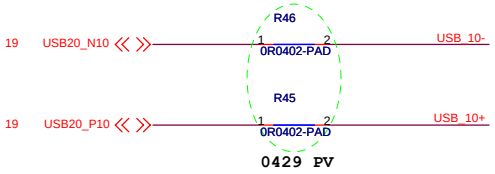
LCD / INVERTER INTERFACE / CAMERA

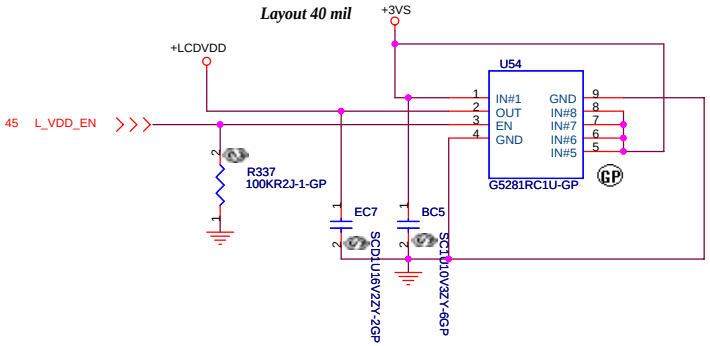
White LED:
Lite-On 83.00191.D70
Everlight 83.19217.F70

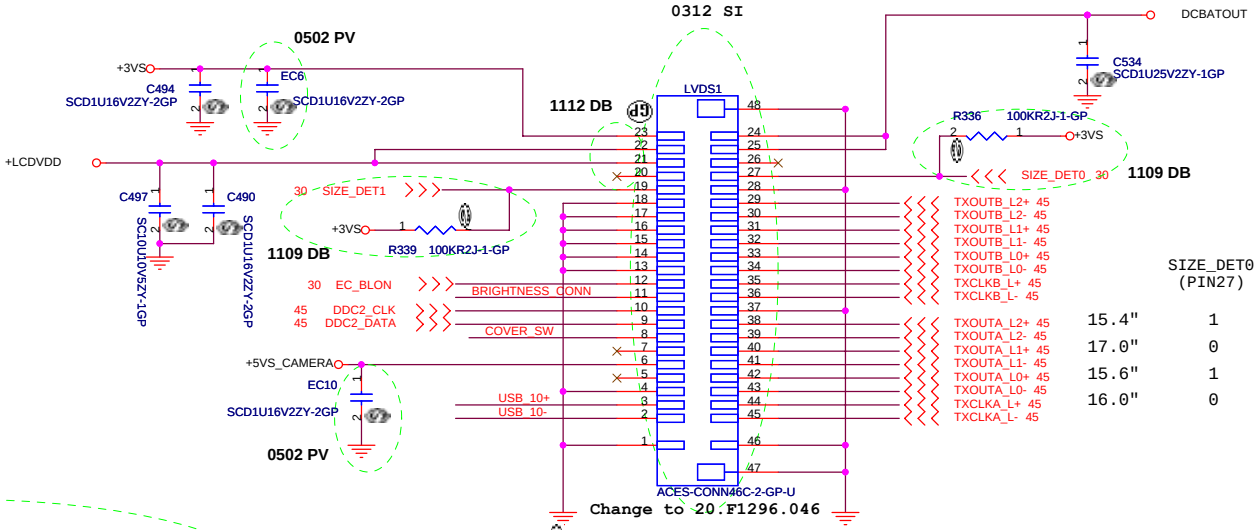




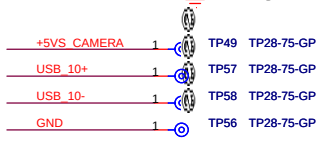


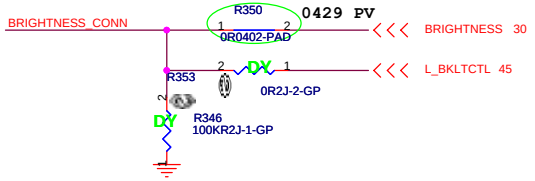


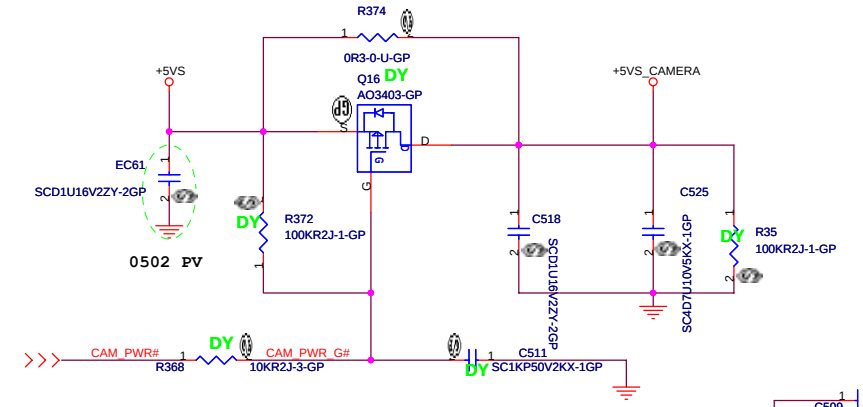


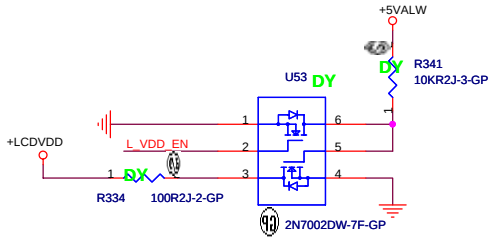


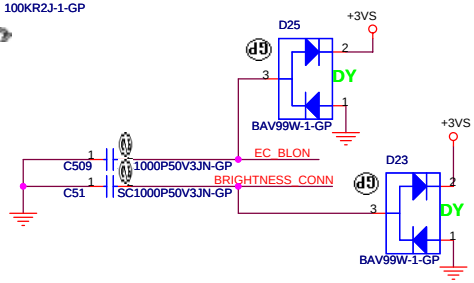
	SIZE_DET0 (PIN27)	SIZE_DET1 (PIN19)
15.4"	1	1
17.0"	0	1
15.6"	1	0
16.0"	0	0











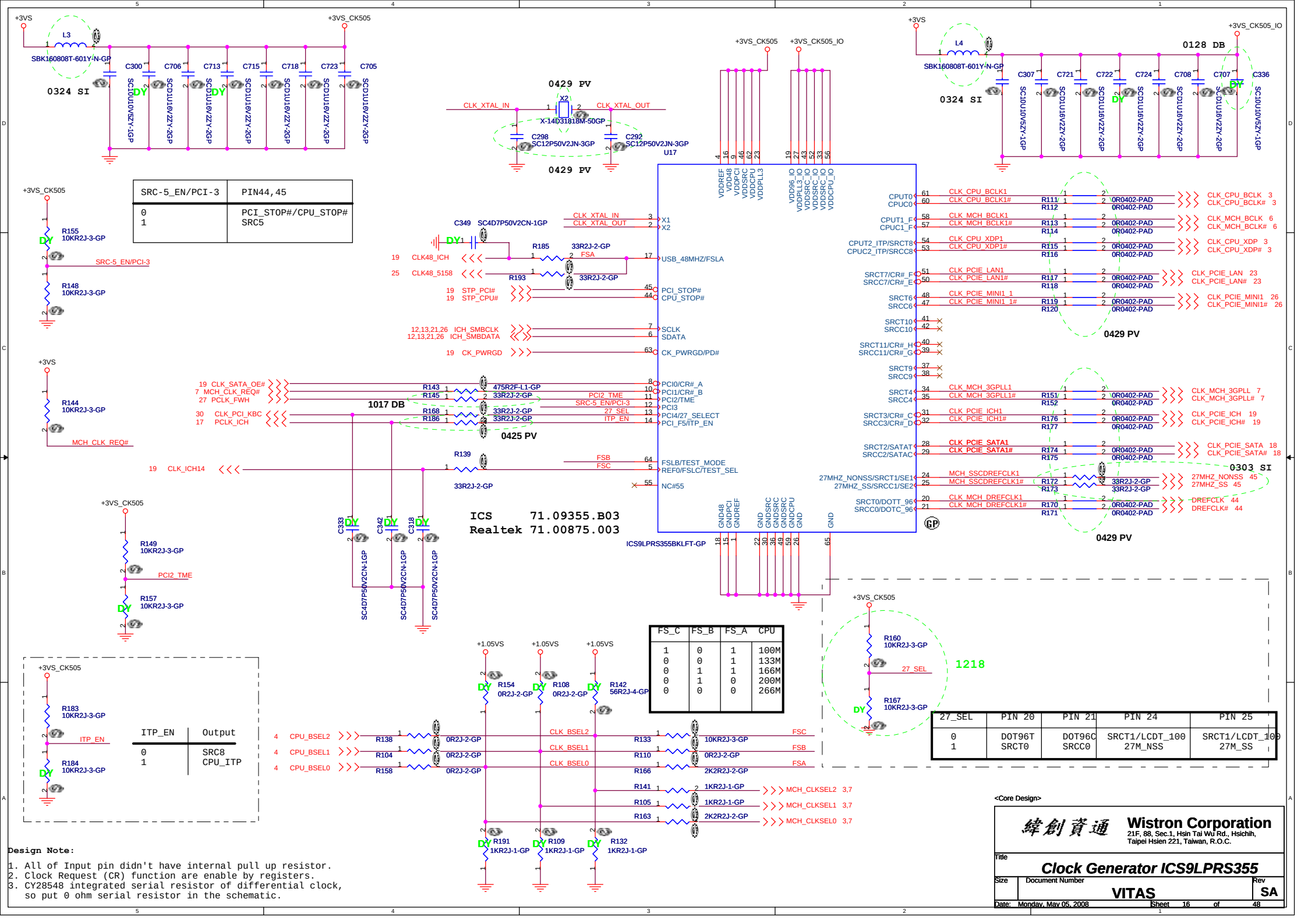
<Core Design>

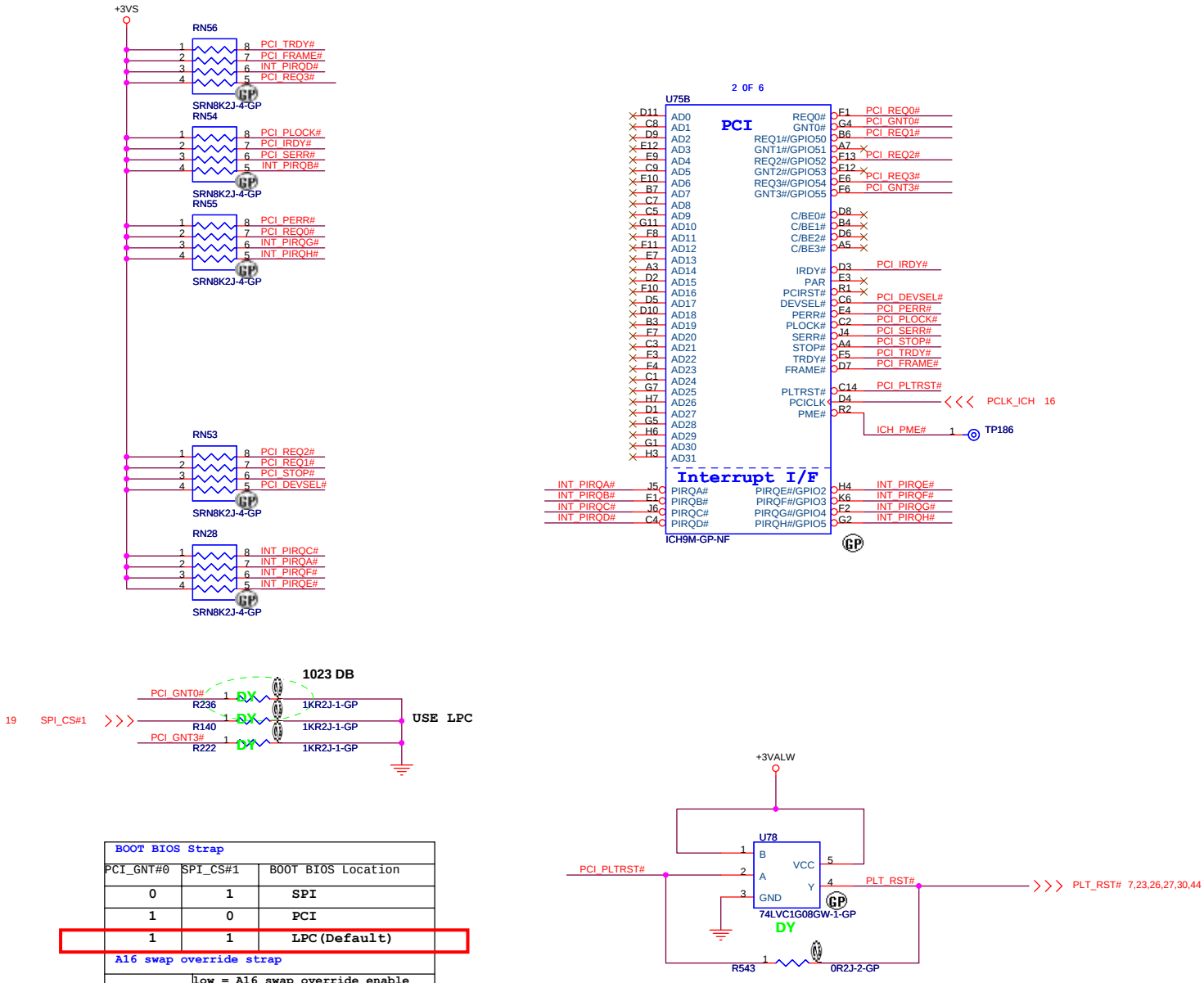
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector/CAM/LED

Size: A3 | Document Number: VITAS | Rev: SA

Date: Monday, May 05, 2008 | Sheet 15 of 48


+3VS
+3VS_CK505
+3VS_CK505_IO
L3
SBK160808T-601Y-N-GP
0324 SI
C300
C706
C713
C715
C718
C723
C705
SC10U10V5ZY-1GP
SC1U16V2ZY-2GP
DY
0429 PV
X2
X-14D31818M-50GP
CLK_XTAL_IN
CLK_XTAL_OUT
C298
SC12P50V2JN-3GP
C292
SC12P50V2JN-3GP
U17
L4
0128 DB
C307
C721
C722
C724
C708
C707
C336
SC10U10V5ZY-1GP
SRC-5_EN/PCI-3
PIN44,45
0
PCI_STOP#/CPU_STOP#
1
SRC5
R155
10KR2J-3-GP
R148
10KR2J-3-GP
C349
SC4D7P50V2CN-1GP
R185
33R2J-2-GP
R193
33R2J-2-GP
FSA
CLK48_ICH
CLK48_5158
STP_PCI#
STP_CPU#
PCI_STOP#
CPU_STOP#
SCLK
SDATA
ICH_SMBCLK
ICH_SMBDATA
CK_PWRGD
CK_PWRGD/PD#
USB_48MHZ/FSLA
R144
10KR2J-3-GP
MCH_CLK_REQ#
CLK_SATA_OE#
MCH_CLK_REQ#
PCLK_FWH
CLK_PCI_KBC
PCLK_ICH
R143
R145
R168
R186
475R2F-L1-GP
33R2J-2-GP
1017 DB
0425 PV
PCI2_TME
SRC-5_EN/PCI-3
27_SEL
ITP_EN
PCI0/CR#_A
PCI1/CR#_B
PCI2/TME
PCI3
PCI4/27_SELECT
PCI_F5/ITP_EN
CLK_ICH14
R139
33R2J-2-GP
FSB
FSC
FSLB/TEST_MODE
REF0/FSLC/TEST_SEL
NC#55
ICS 71.09355.B03
Realtek 71.00875.003
ICS9LPRS355BKLFT-GP
R149
10KR2J-3-GP
R157
10KR2J-3-GP
C333
C342
C318
SC4D7P50V2CN-1GP
CPUT0
CPUC0
CPUT1_F
CPUC1_F
CPUT2_ITP/SRCT8
CPUC2_ITP/SRCC8
SRCT7/CR#_F
SRCC7/CR#_E
SRCT6
SRCC6
SRCT10
SRCC10
SRCT11/CR#_H
SRCC11/CR#_G
SRCT9
SRCC9
SRCT4
SRCC4
SRCT3/CR#_C
SRCC3/CR#_D
SRCT2/SATAT
SRCC2/SATAC
SRCT0/DOTT_96
SRCC0/DOTC_96
27MHZ_NONSS/SRCT1/SE1
27MHZ_SS/SRCC1/SE2
CLK_CPU_BCLK1
CLK_CPU_BCLK1#
CLK_MCH_BCLK1
CLK_MCH_BCLK1#
CLK_CPU_XDP1
CLK_CPU_XDP1#
CLK_PCIE_LAN1
CLK_PCIE_LAN1#
CLK_PCIE_MINI1_1
CLK_PCIE_MINI1_1#
CLK_MCH_3GPLL1
CLK_MCH_3GPLL1#
CLK_PCIE_ICH1
CLK_PCIE_ICH1#
CLK_PCIE_SATA1
CLK_PCIE_SATA1#
MCH_SSCDREFCLK1
MCH_SSCDREFCLK1#
CLK_MCH_DREFCLK1
CLK_MCH_DREFCLK1#
R111
R112
R113
R114
R115
R116
R117
R118
R119
R120
R151
R152
R176
R177
R174
R175
R172
R173
R170
R171
0R0402-PAD
33R2J-2-GP
0429 PV
0303 SI
CLK_CPU_BCLK 3
CLK_CPU_BCLK# 3
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
CLK_CPU_XDP 3
CLK_CPU_XDP# 3
CLK_PCIE_LAN 23
CLK_PCIE_LAN# 23
CLK_PCIE_MINI1 26
CLK_PCIE_MINI1# 26
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
CLK_PCIE_ICH 19
CLK_PCIE_ICH# 19
CLK_PCIE_SATA 18
CLK_PCIE_SATA# 18
27MHZ_NONSS 45
27MHZ_SS 45
DREFCLK 44
DREFCLK# 44
R160
10KR2J-3-GP
27_SEL
R167
10KR2J-3-GP
1218
27_SEL
PIN 20
PIN 21
PIN 24
PIN 25
0
DOT96T
DOT96C
SRCT1/LCDT_100
SRCT1/LCDT_100
1
SRCT0
SRCC0
27M_NSS
27M_SS
R183
10KR2J-3-GP
R184
10KR2J-3-GP
ITP_EN
Output
0
SRC8
1
CPU_ITP
FS_C
FS_B
FS_A
CPU
1 0 1 100M
0 0 1 133M
0 1 1 166M
0 1 0 200M
0 0 0 266M
R154
0R2J-2-GP
R108
0R2J-2-GP
R142
56R2J-4-GP
CPU_BSEL2
CPU_BSEL1
CPU_BSEL0
R138
R104
R158
R133
R110
R166
10KR2J-3-GP
0R2J-2-GP
2K2R2J-2-GP
FSC
FSB
FSA
R141
R105
R163
1KR2J-1-GP
2K2R2J-2-GP
MCH_CLKSEL2 3,7
MCH_CLKSEL1 3,7
MCH_CLKSEL0 3,7
R191
R109
R132
1KR2J-1-GP
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator ICS9LPRS355
Size
Document Number
VITAS
Rev
SA
Date: Monday, May 05, 2008
Sheet 16 of 48



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

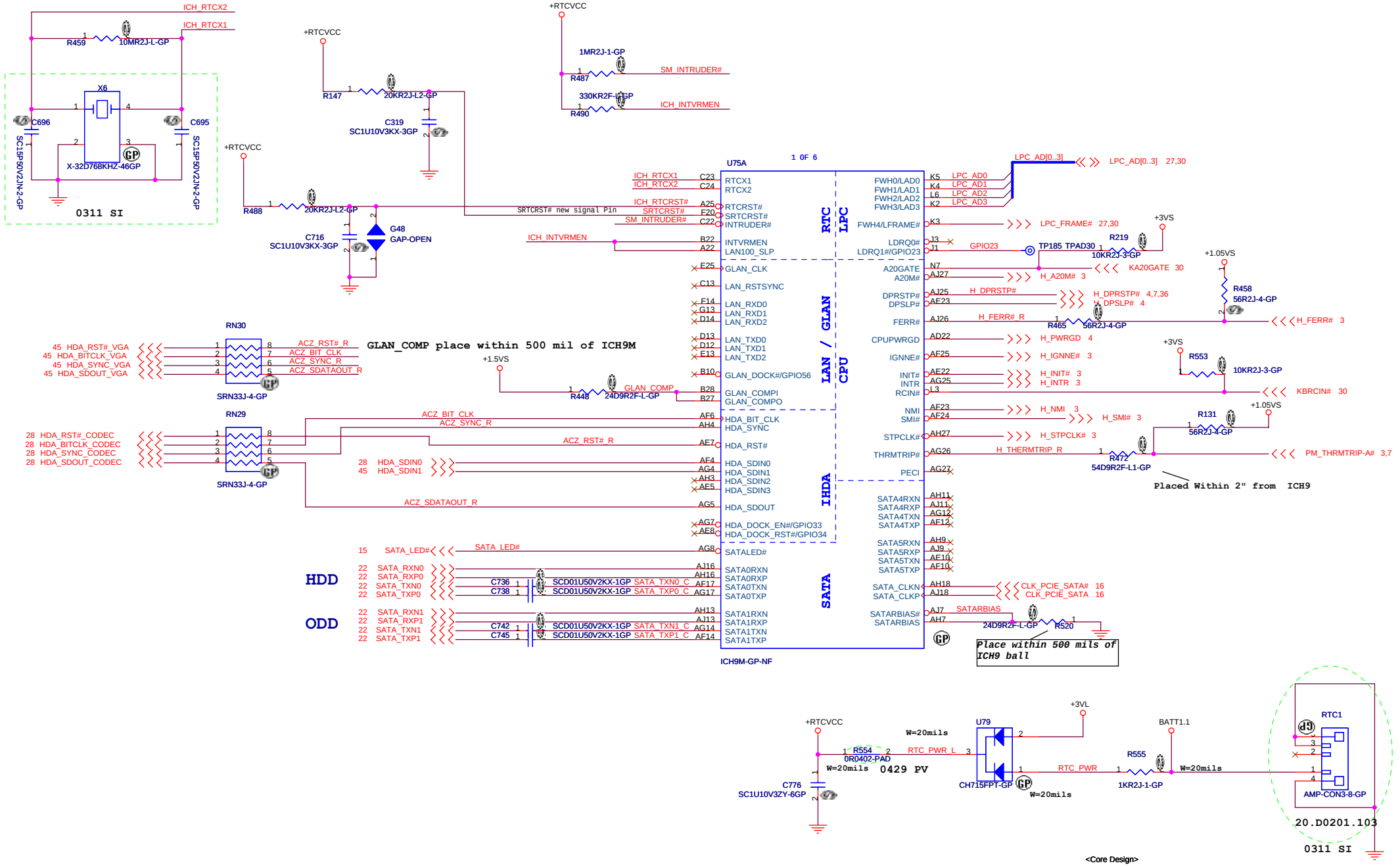
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 5)

Size | Document Number: VITAS | Rev: SA

Date: Monday, May 05, 2008 | Sheet 17 of 48



integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

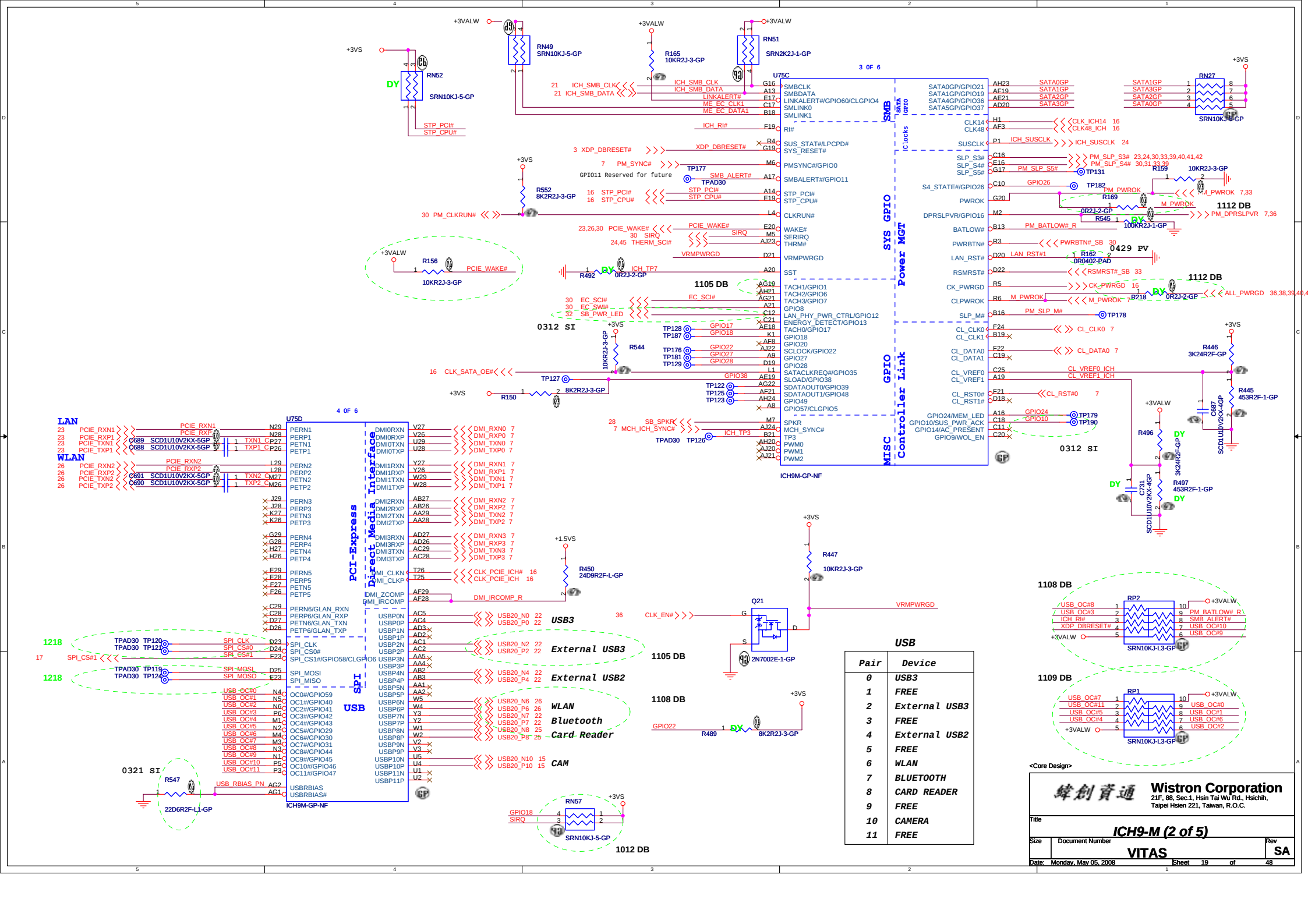
<Core Design>

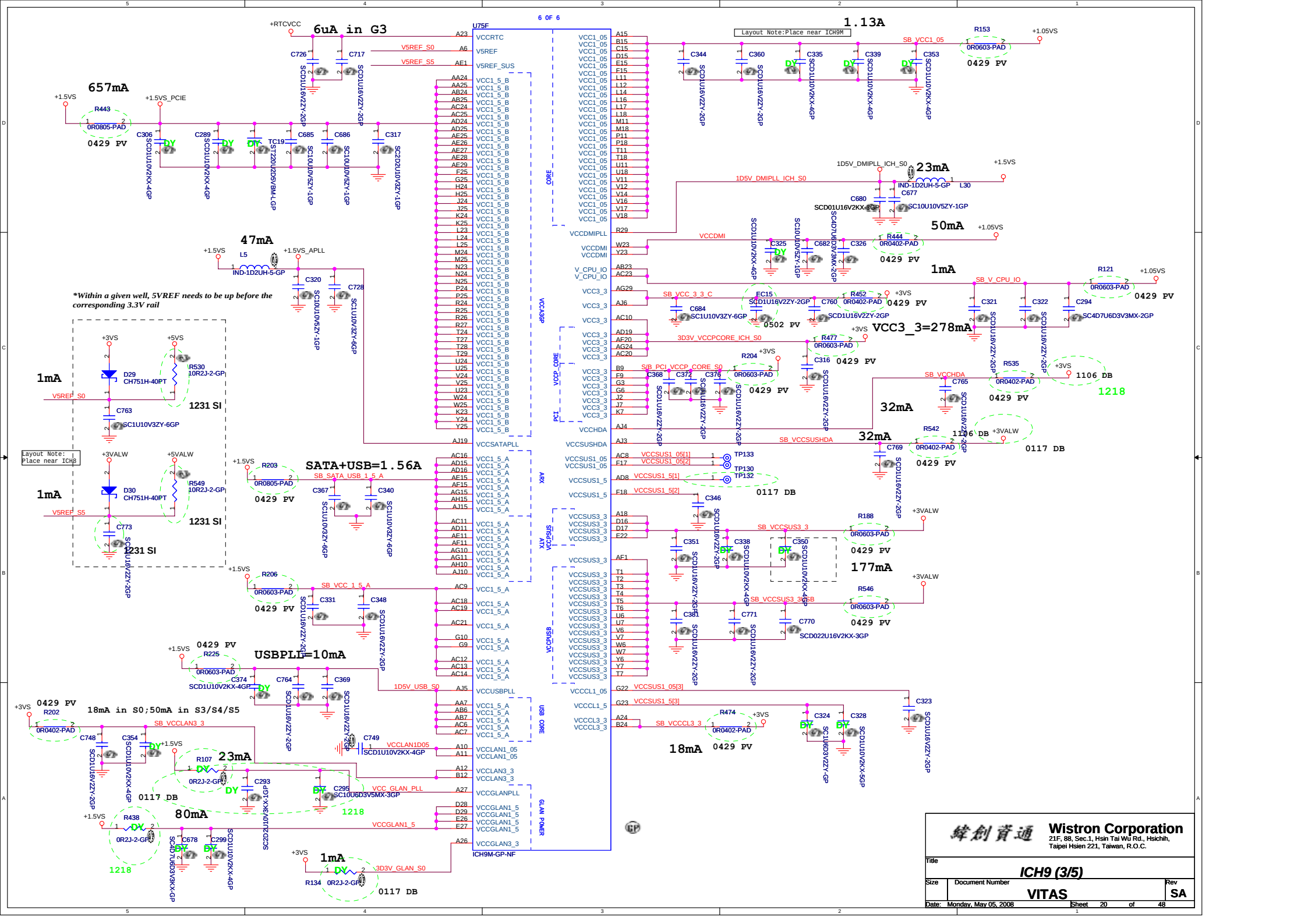
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

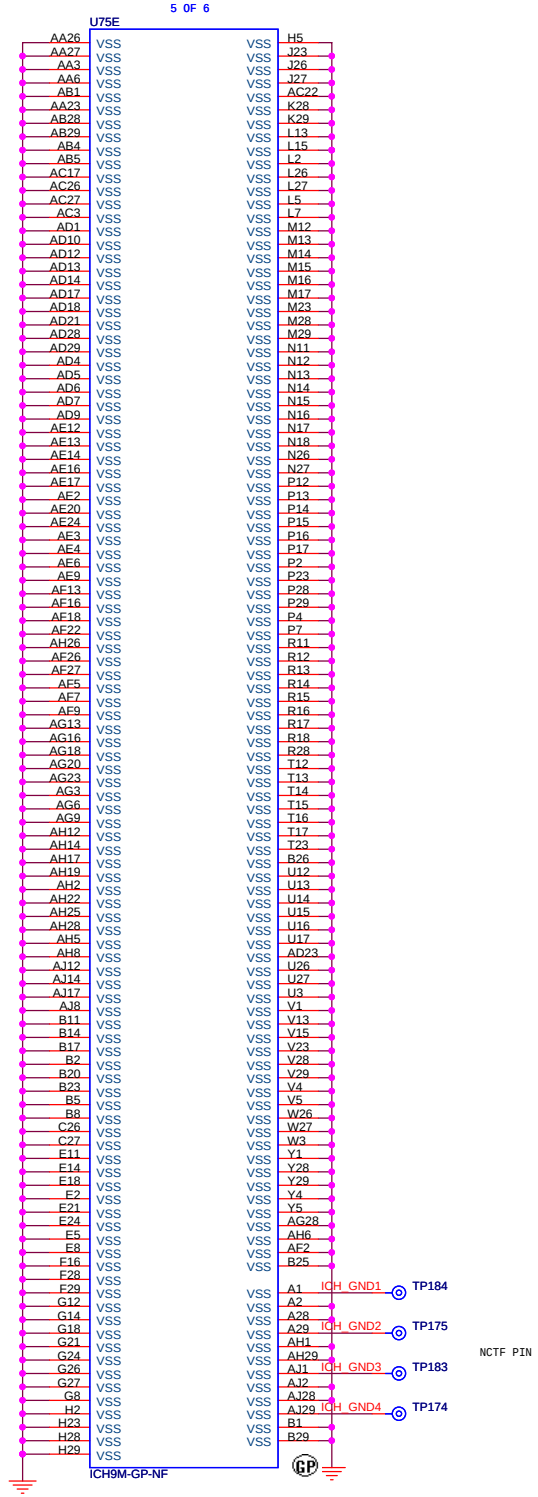
Title: ICH9-M (2 of 5)

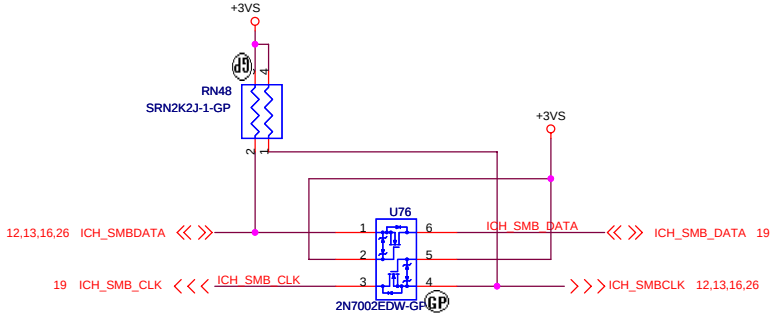
Size	Document Number	Rev
	VITAS	SA

Date: Monday, May 05, 2008 Sheet 18 of 48


U75C
ICH9M-GP-NF
3 OF 6
4 OF 6
U75D
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
PCI-Express
Direct Media Interface
USB
SPI
LAN
WLAN
USB
Pair Device
0 USB3
1 FREE
2 External USB3
3 FREE
4 External USB2
5 FREE
6 WLAN
7 BLUETOOTH
8 CARD READER
9 FREE
10 CAMERA
11 FREE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (2 of 5)
VITAS
SA
Monday, May 05, 2008
Sheet 19 of 48


6 OF 6
U75F
ICH9M-GP-NF
6uA in G3
+RTCVCC
657mA
+1.5VS
+1.5VS_PCIE
R443
0R0805-PAD
0429 PV
47mA
+1.5VS_APLL
L5
IND-1D2UH-5-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1mA
D29
CH751H-40PT
R530
10R2J-2-GP
1231 SI
D30
R549
Layout Note: Place near ICH8
SATA+USB=1.56A
R203
0R0805-PAD
USBPLL=10mA
R206
0R0603-PAD
R225
18mA in S0;50mA in S3/S4/S5
R202
0R0402-PAD
23mA
R107
0R2J-2-GP
0117 DB
80mA
R438
1218
R134
1.13A
Layout Note:Place near ICH9M
R153
0429 PV
1D5V_DMIPLL_ICH_S0
IND-1D2UH-5-GP
L30
50mA
R444
1mA
R121
VCC3_3=278mA
R204
R477
3D3V_VCCPCORE_ICH_S0
0502 PV
32mA
1106 DB
R542
R546
177mA
R188
R474
18mA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9 (3/5)
Size
Document Number
VITAS
Rev
SA
Date: Monday, May 05, 2008
Sheet 20 of 48

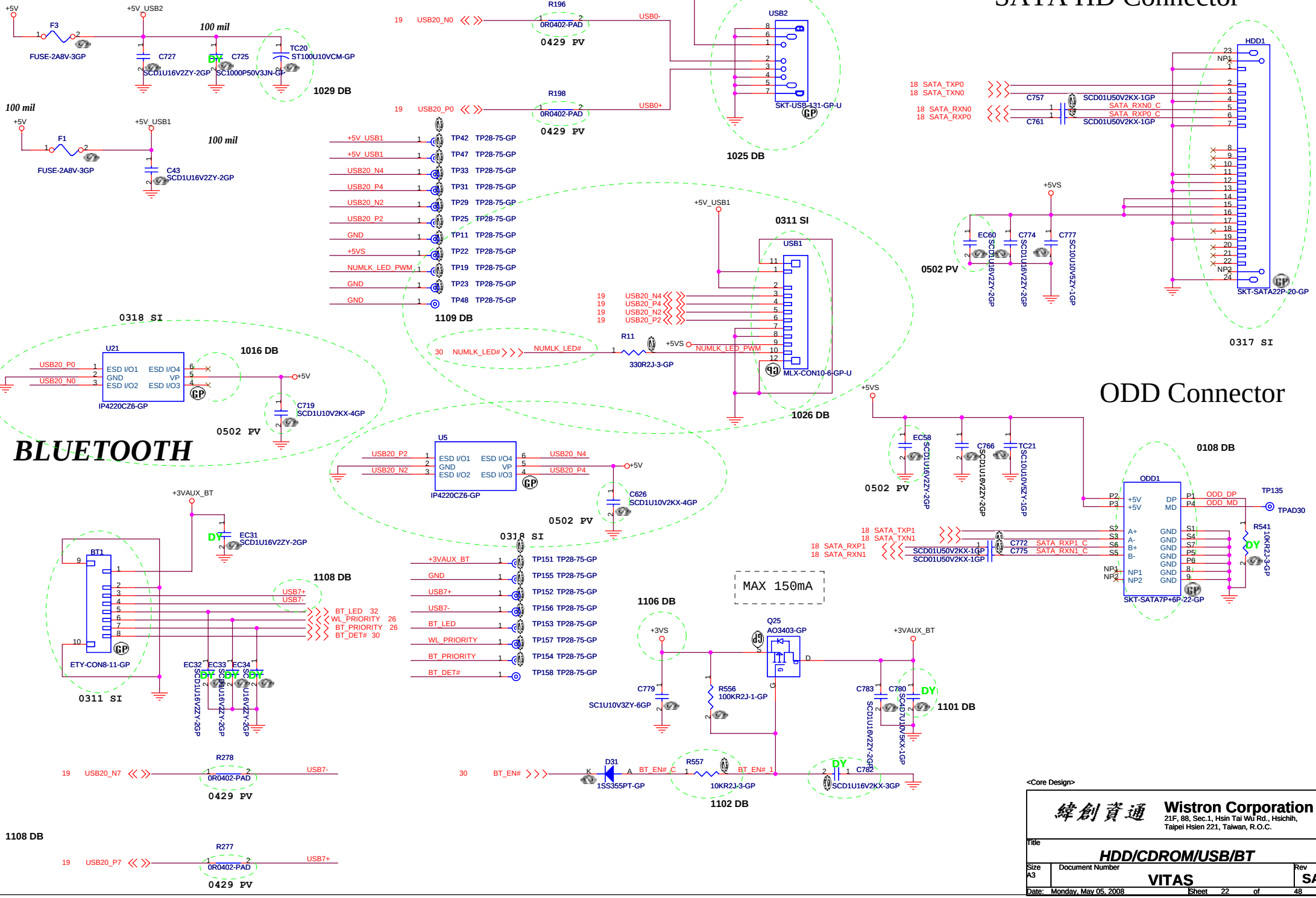


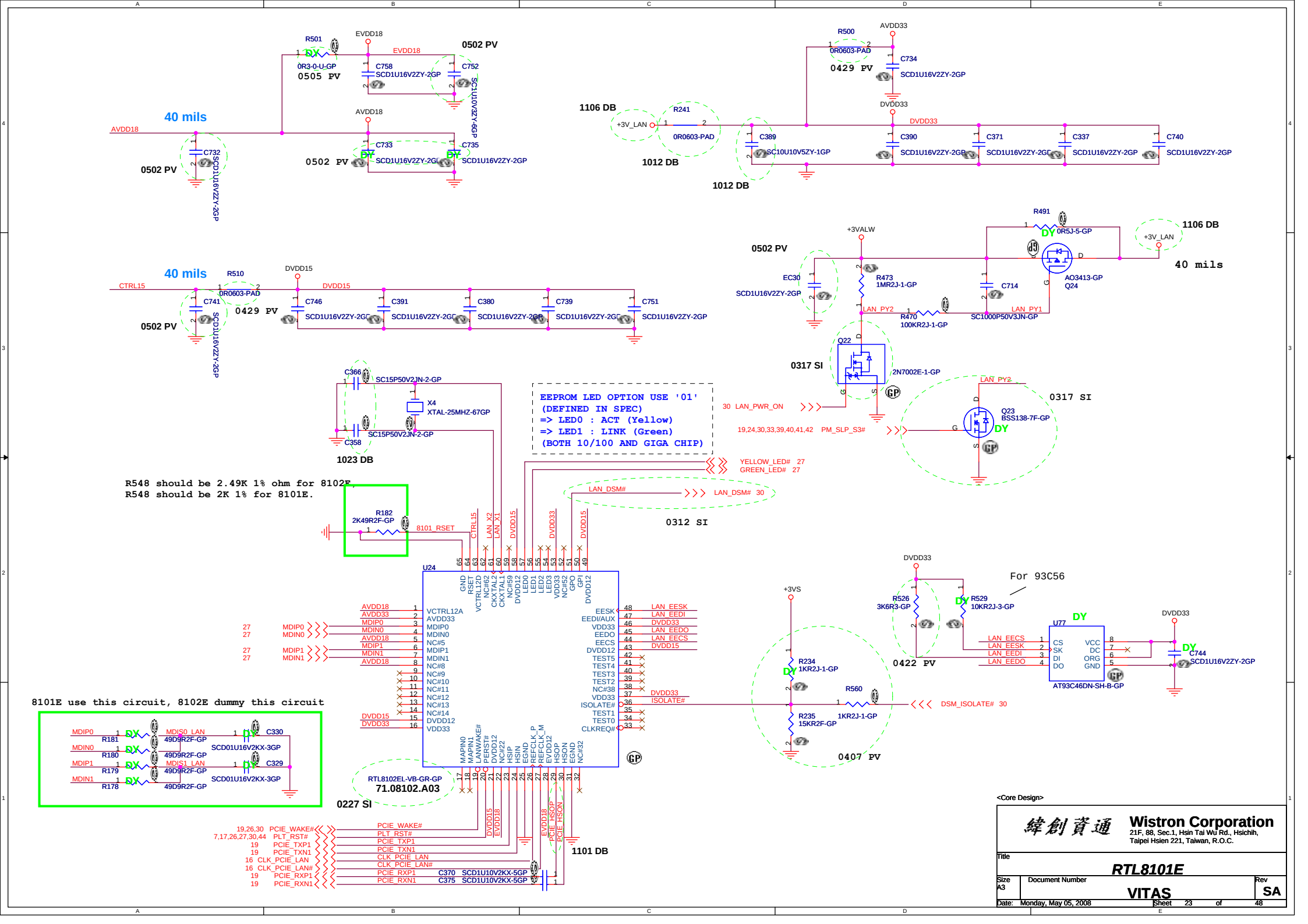


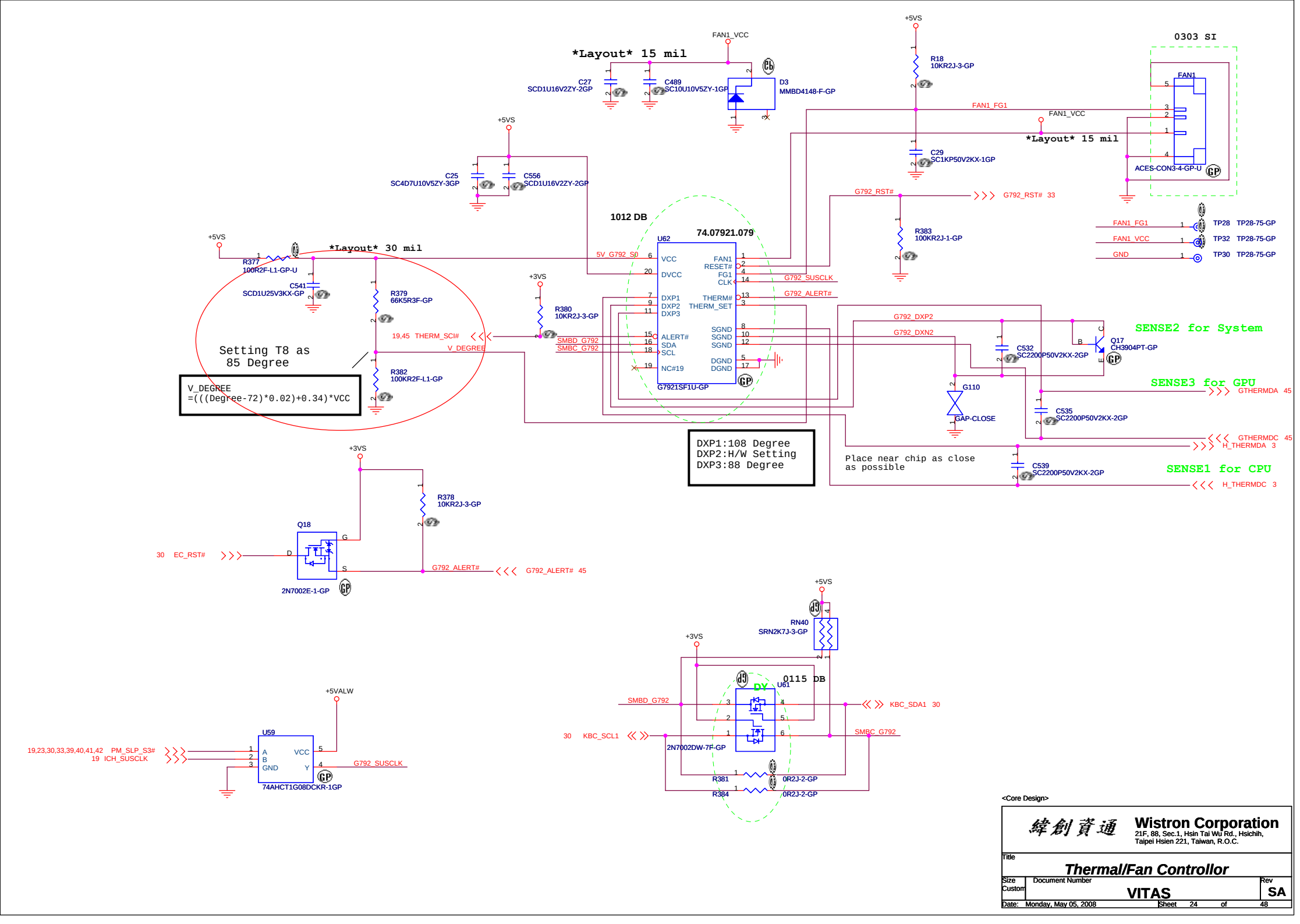
SMBUS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	*ICH9-M (4 of 4)*		
Size	Document Number: VITAS		Rev: SA
Date: Monday, May 05, 2008	Sheet 21 of 48		

USB PORT

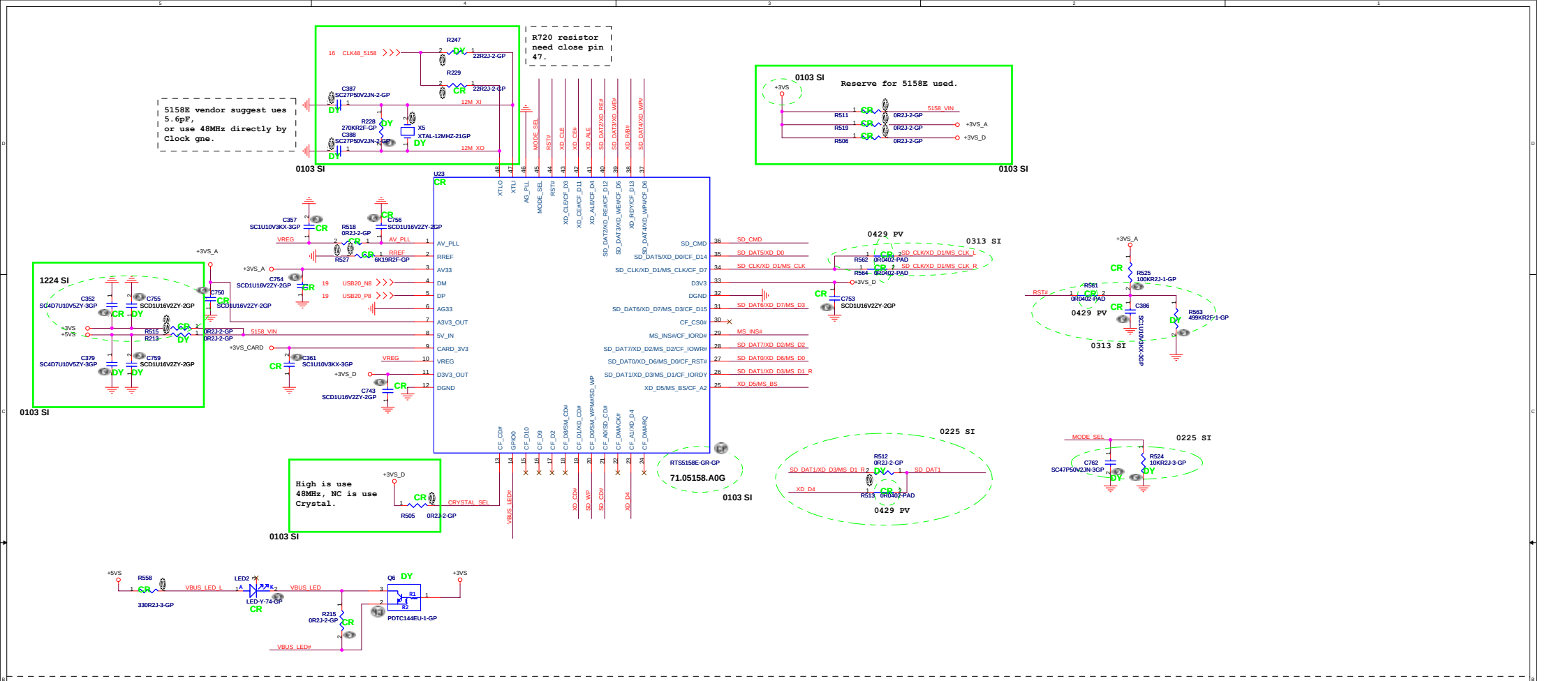



R501
EVDD18
0R3-0-U-GP
0505 PV
0502 PV
C758
SCD1U16V2ZY-2GP
C752
SC1U10V3ZY-6GP
40 mils
AVDD18
C732
SCD1U16V2ZY-2GP
C733
C735
R500
AVDD33
0R0603-PAD
0429 PV
C734
1106 DB
R241
+3V_LAN
1012 DB
DVDD33
C389
SC10U10V5ZY-1GP
C390
C371
C337
C740
R491
0R5J-5-GP
1106 DB
+3VALW
EC30
R473
1MR2J-1-GP
C714
AO3413-GP
Q24
LAN_PY2
LAN_PY1
R470
100KR2J-1-GP
SC1000P50V3JN-GP
Q22
2N7002E-1-GP
0317 SI
30 LAN_PWR_ON
19,24,30,33,39,40,41,42 PM_SLP_S3#
Q23
BSS138-7F-GP
R510
CTRL15
DVDD15
C741
C746
C391
C380
C739
C751
C366
SC15P50V2JN-2-GP
X4
XTAL-25MHZ-67GP
C358
1023 DB
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT (Yellow)
=> LED1 : LINK (Green)
(BOTH 10/100 AND GIGA CHIP)
YELLOW_LED# 27
GREEN_LED# 27
R548 should be 2.49K 1% ohm for 8102E.
R548 should be 2K 1% for 8101E.
R182
2K49R2F-GP
8101_RSET
LAN_DSM#
LAN_DSM# 30
0312 SI
U24
VCTRL12A
AVDD33
MDIP0
MDIN0
NC#5
MDIP1
MDIN1
NC#8
NC#9
NC#10
NC#11
NC#12
NC#13
NC#14
DVDD12
VDD33
EESK
EEDI/AUX
VDD33
EEDO
EECS
DVDD12
TEST5
TEST4
TEST3
TEST2
NC#38
VDD33
ISOLATE#
TEST1
TEST0
CLKREQ#
LAN_EESK
LAN_EEDI
DVDD33
LAN_EEDO
LAN_EECS
DVDD15
DVDD33
ISOLATE#
RTL8102EL-VB-GR-GP
71.08102.A03
0227 SI
8101E use this circuit, 8102E dummy this circuit
MDIP0
MDIN0
MDIP1
MDIN1
R181
R180
R179
R178
49D9R2F-GP
MDI0_LAN
MDI1_LAN
C330
C329
SCD01U16V2KX-3GP
+3VS
R234
1KR2J-1-GP
R235
15KR2F-GP
R560
1KR2J-1-GP
DSM_ISOLATE# 30
0407 PV
DVDD33
For 93C56
R526
3K6R3-GP
R529
10KR2J-3-GP
0422 PV
U77
CS
SK
DI
DO
VCC
DC
ORG
GND
AT93C46DN-SH-B-GP
C744
SCD1U16V2ZY-2GP
19,26,30 PCIE_WAKE#
7,17,26,27,30,44 PLT_RST#
19 PCIE_TXP1
19 PCIE_TXN1
16 CLK_PCIE_LAN
16 CLK_PCIE_LAN#
19 PCIE_RXP1
19 PCIE_RXN1
PCIE_WAKE#
PLT_RST#
PCIE_TXP1
PCIE_TXN1
CLK_PCIE_LAN
CLK_PCIE_LAN#
PCIE_RXP1
PCIE_RXN1
C370
C375
SCD1U10V2KX-5GP
1101 DB
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8101E
Size
A3
Document Number
VITAS
Rev
SA
Date: Monday, May 05, 2008
Sheet 23 of 48



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Thermal/Fan Controllor***
Size: Custom	Document Number: **VITAS**
Rev	**SA**
Date: Monday, May 05, 2008	Sheet 24 of 48



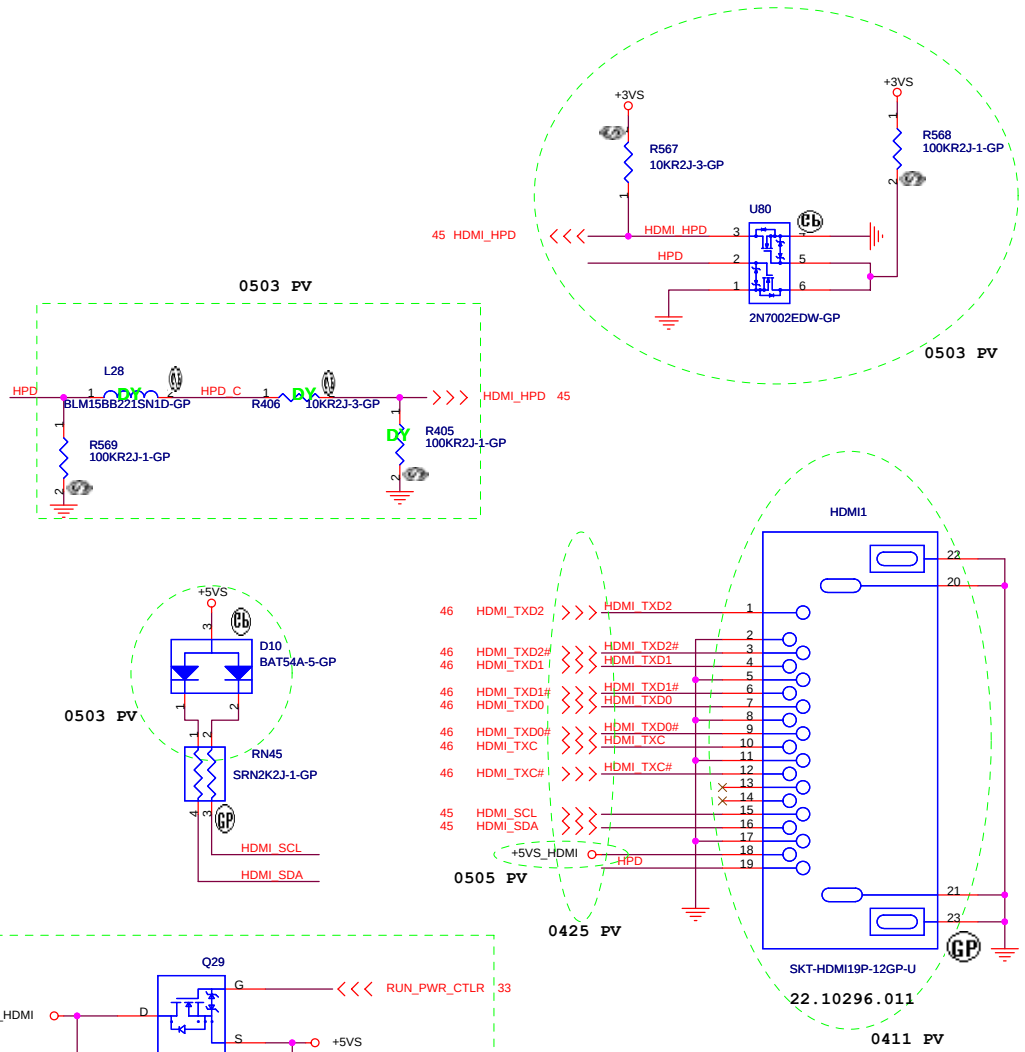
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Card Reader Controller - RTS5158**

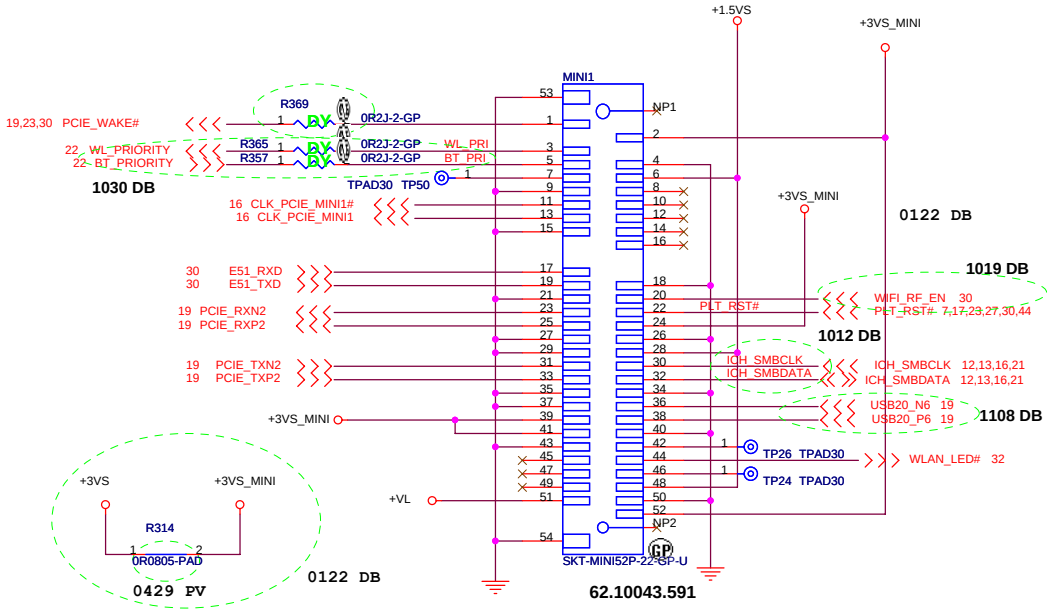
Size: | Document Number: **Warrior** | Rev: SC

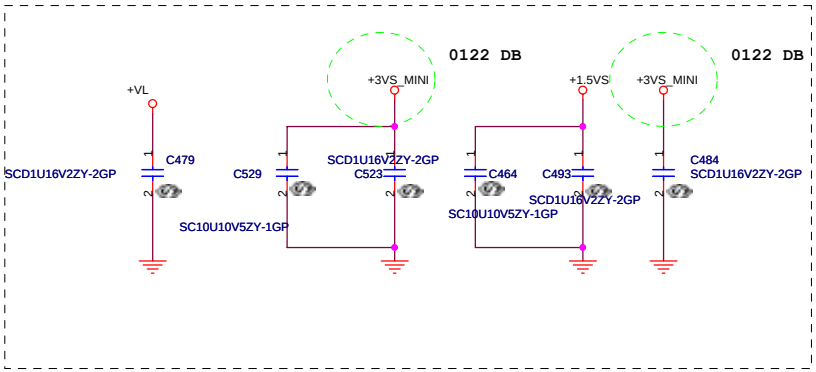
Date: Monday, May 05, 2008 | Sheet 25 of 42

HDMI Connector



Mini Card Connector1(802.11a/b/g)





<Core Design>

緯創資通 **Wistron Corporation**
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Title: **MINI CARD/HDMI CONN .**

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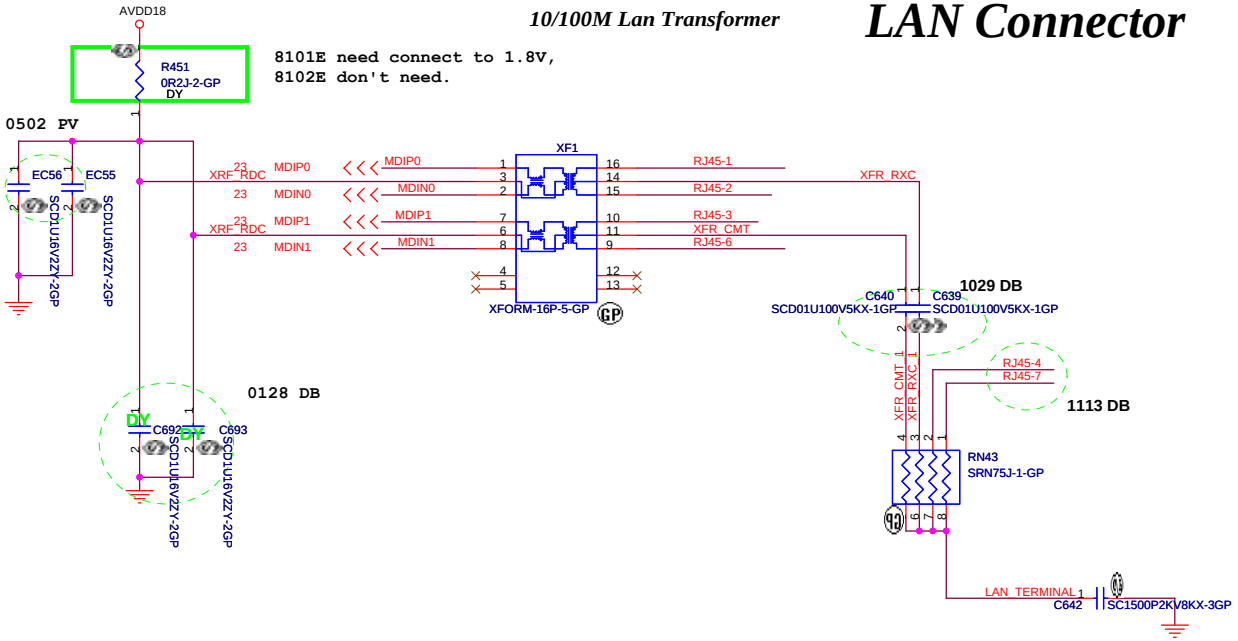
LAN Connector

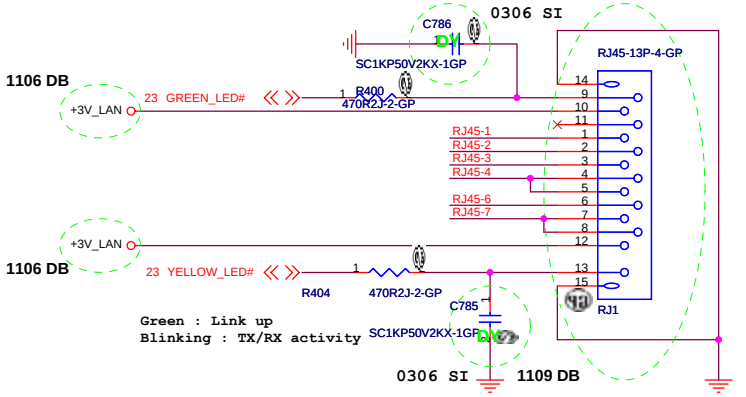
10/100M Lan Transformer

8101E need connect to 1.8V,
8102E don't need.



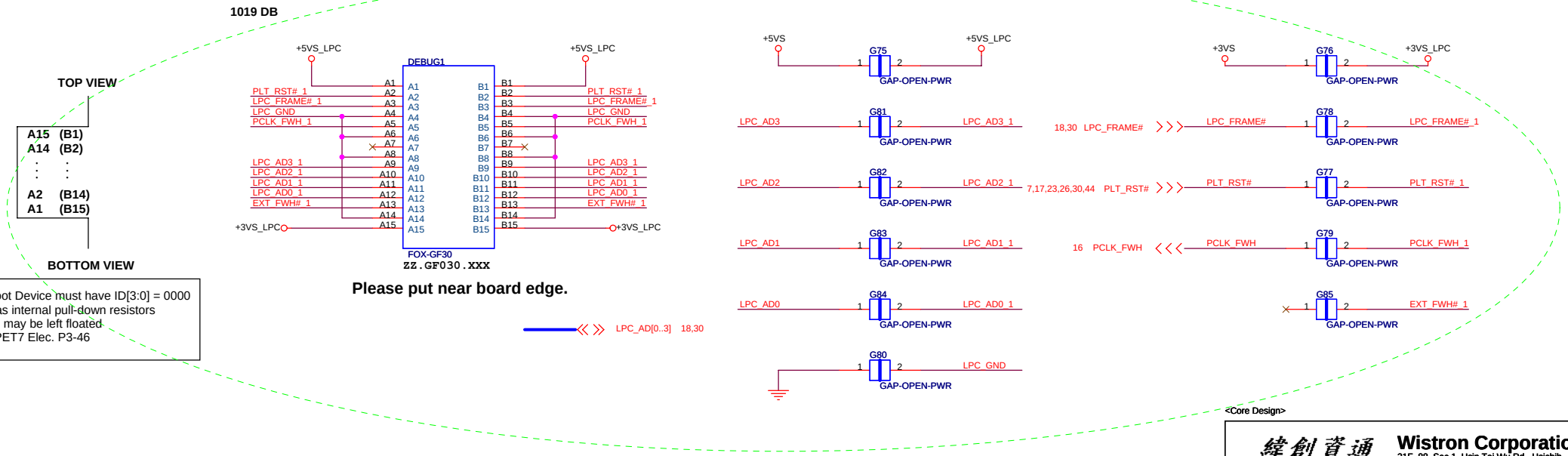
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Remark:
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.

Golden Finger for Debug Board



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

<Core Design>

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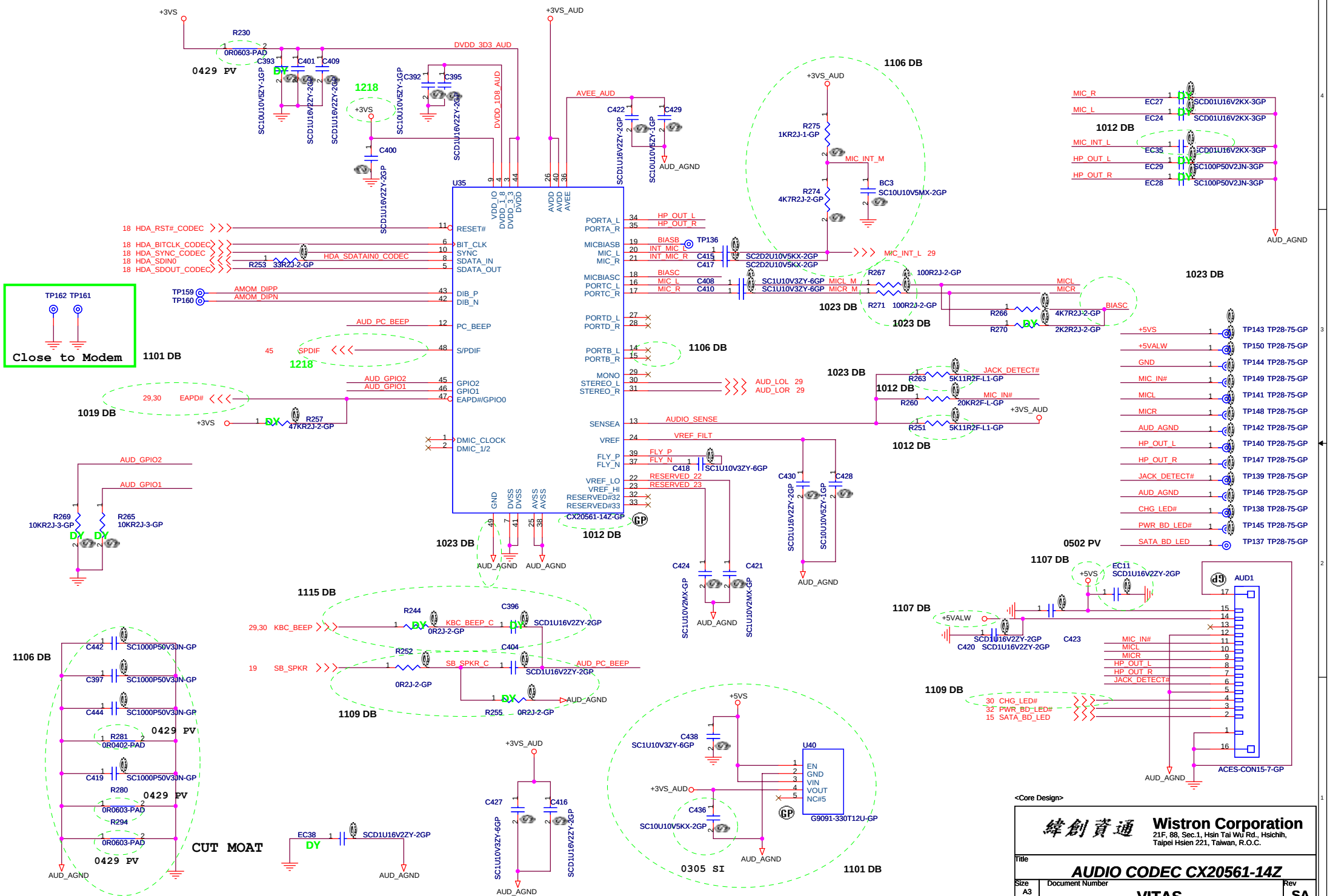
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN/Debug	
Size A3	Document Number VITAS	Rev SA
Date: Monday, May 05, 2008	Sheet 27 of 48	


U35
RESET#
BIT_CLK
SYNC
SDATA_IN
SDATA_OUT
DIB_P
DIB_N
PC_BEEP
S/PDIF
GPIO2
GPIO1
EAPD#/GPIO0
DMIC_CLOCK
DMIC_1/2
CX20561-14Z-GP
U40
G9091-330T12U-GP
Close to Modem
1101 DB
1106 DB
1115 DB
1109 DB
1019 DB
1012 DB
1023 DB
1107 DB
1012 DB
1012 DB
1012 DB
0502 PV
0429 PV
0305 SI
CUT MOAT
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC CX20561-14Z
VITAS
Size A3
Rev SA
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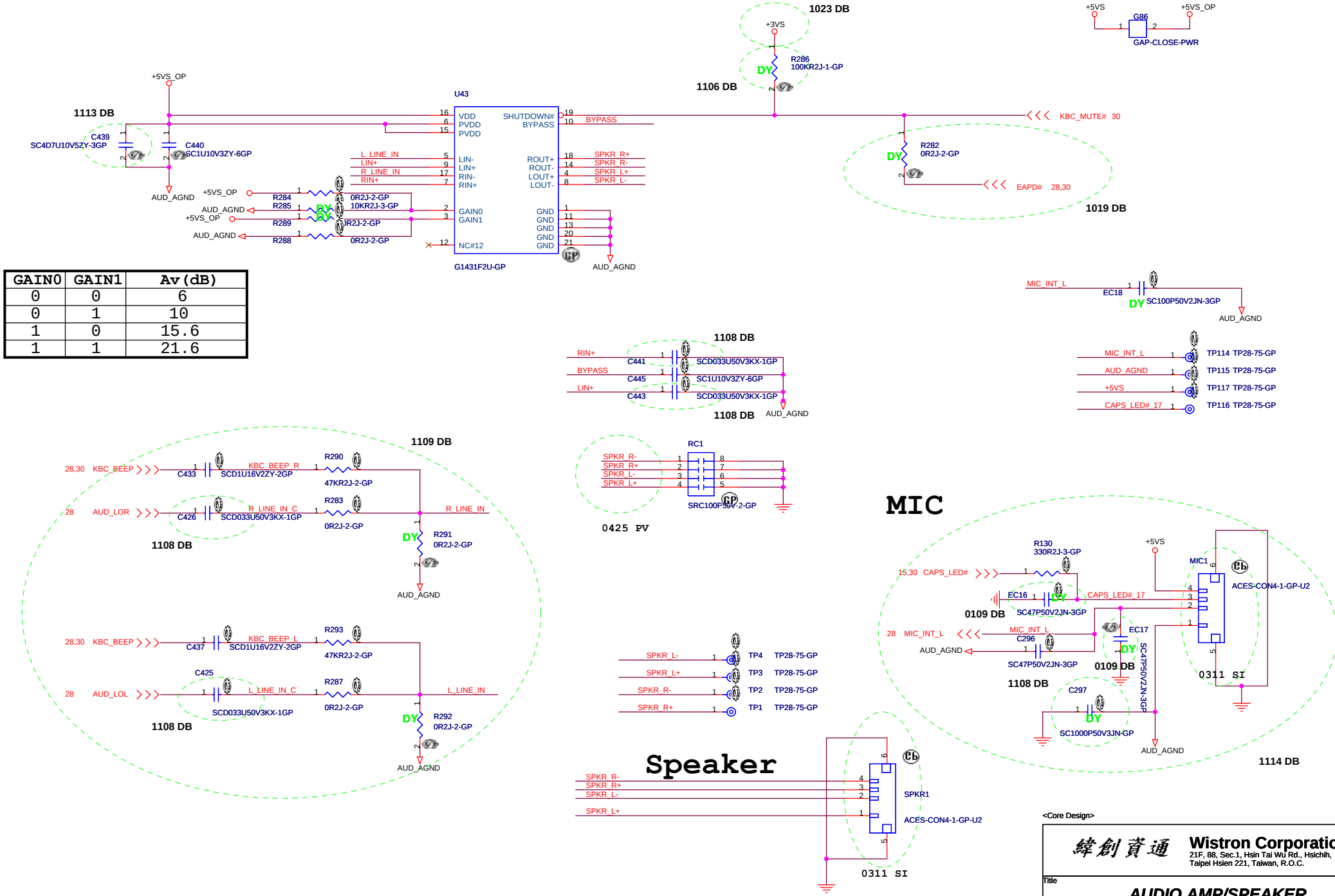

<Core Design>

緯創資通 **Wistron Corporation**
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Title: **AUDIO AMP/SPEAKER**

Size	Document Number	Rev
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CAP close to VCC-GND pin pair

CAP near ADC

TP near KB connector

2 GND connect at one point

U19A 1 OF 2

U19B 2 OF 2

WPCE773LA0DG-GP

82.30001.861 EPSON MC-306
32.768Khz 12.5pf 10ppm

Planar ID[2,1,0]
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 1,0,0
-2: 0,1,1
-3: 1,0,1

0425 PV

<Core Design>

Add Label "5V_S0"

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Title: KBC WPCE775L

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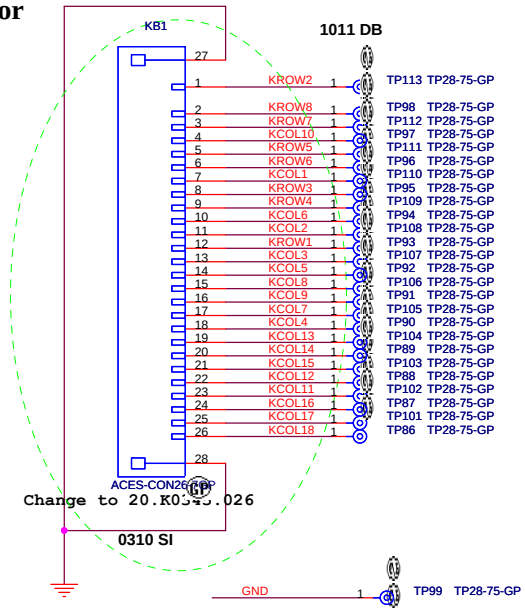
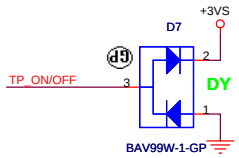
Internal KeyBoard Connector

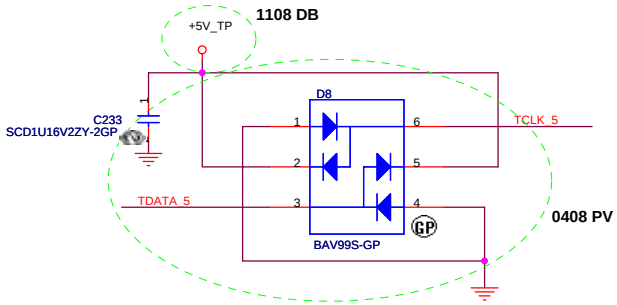
30 KROW[1..8]
30 KCOL[1..18]

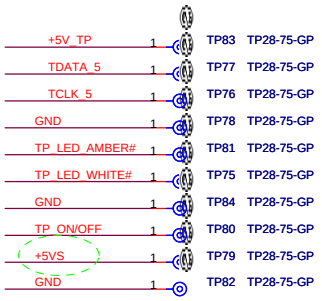
Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



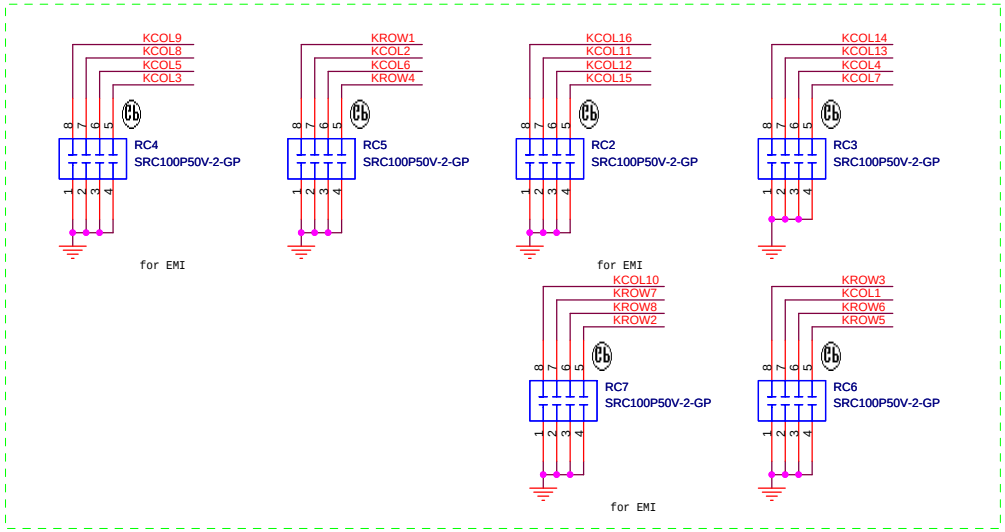






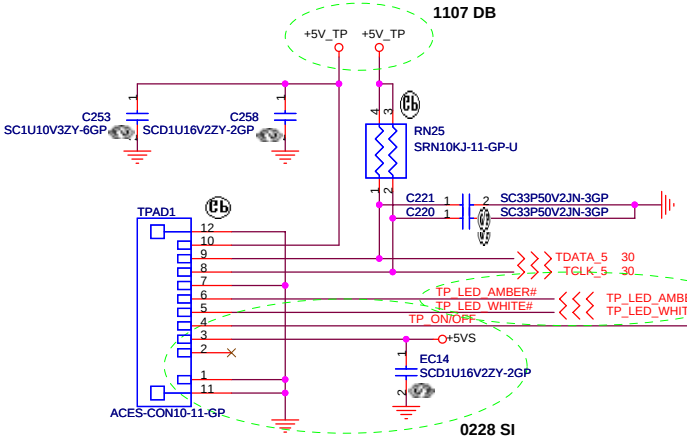
0228 SI

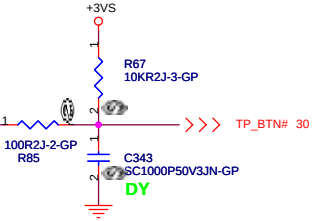
Please populate close TPAD1

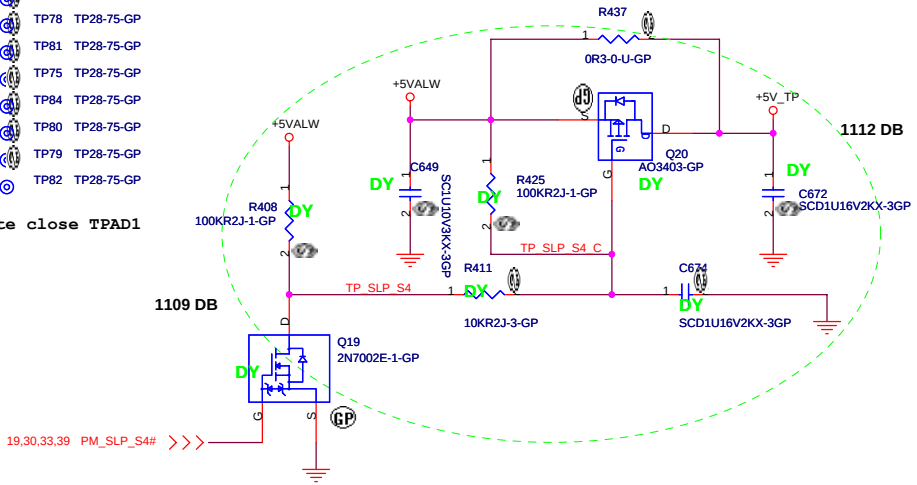


0408 PV

TouchPad Connector







<Core Design>

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Title: KeyBoard-CONN

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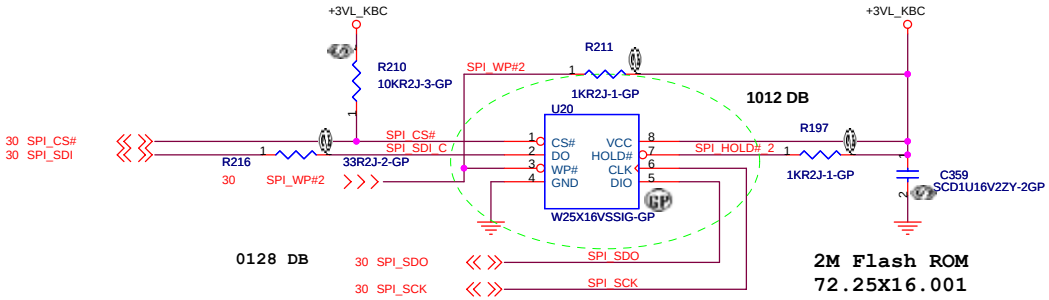

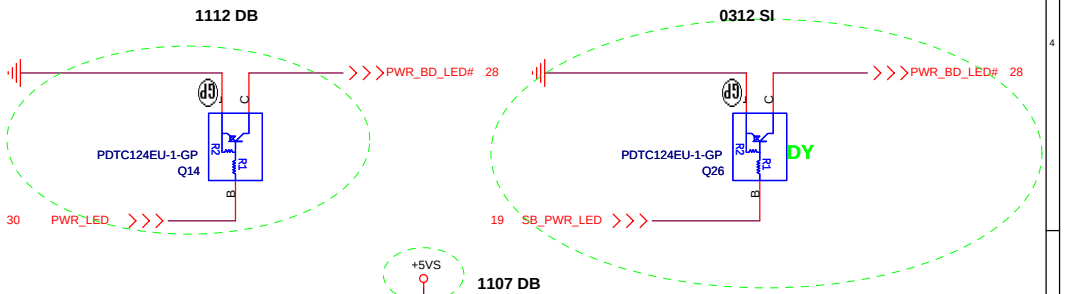

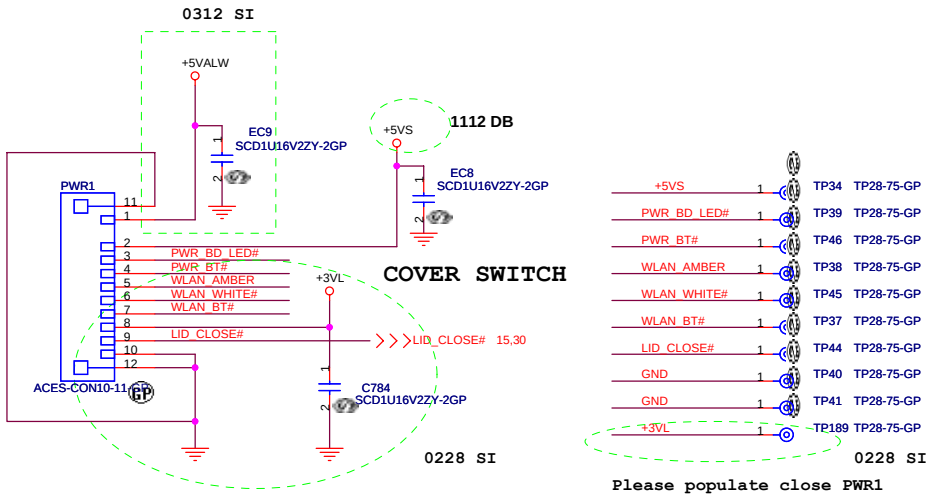

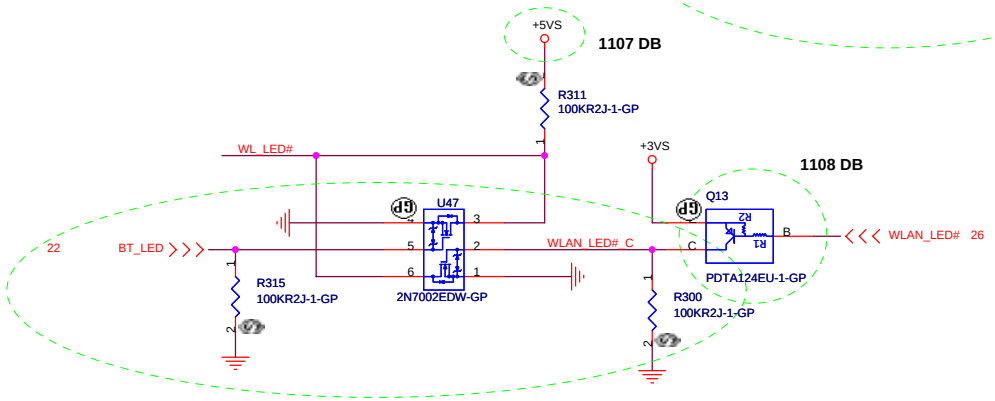

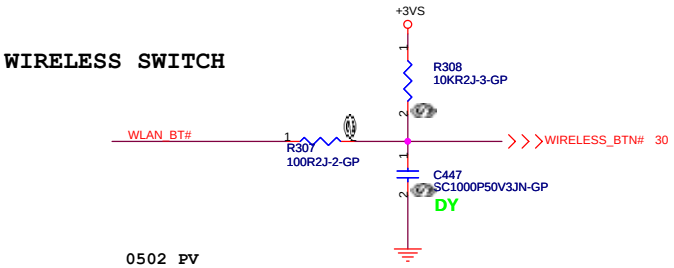

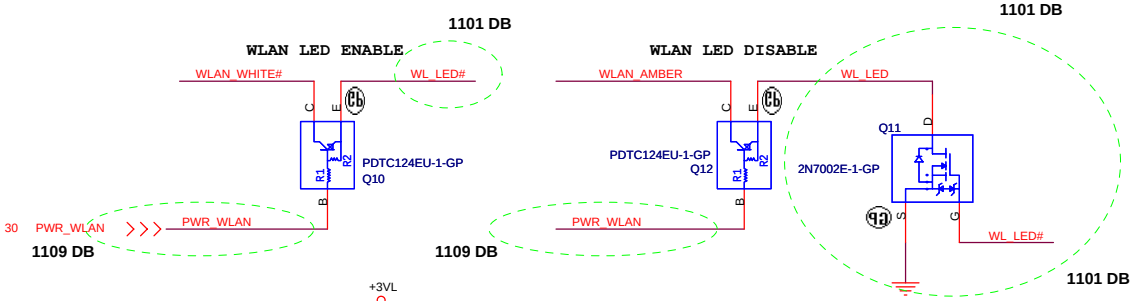

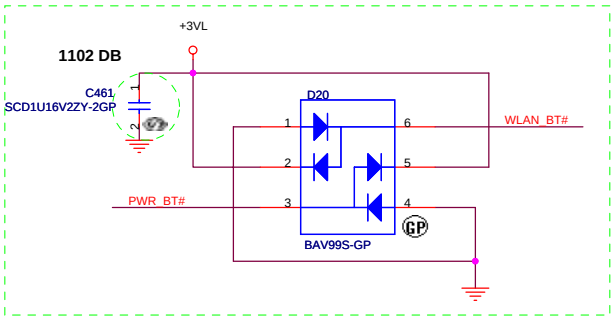

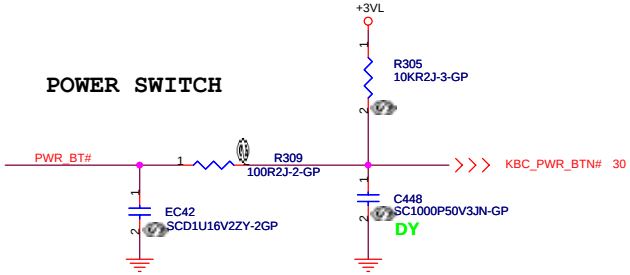

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Title: FWH and CONN.

Size: A3 | Document Number: VITAS | Rev: SA

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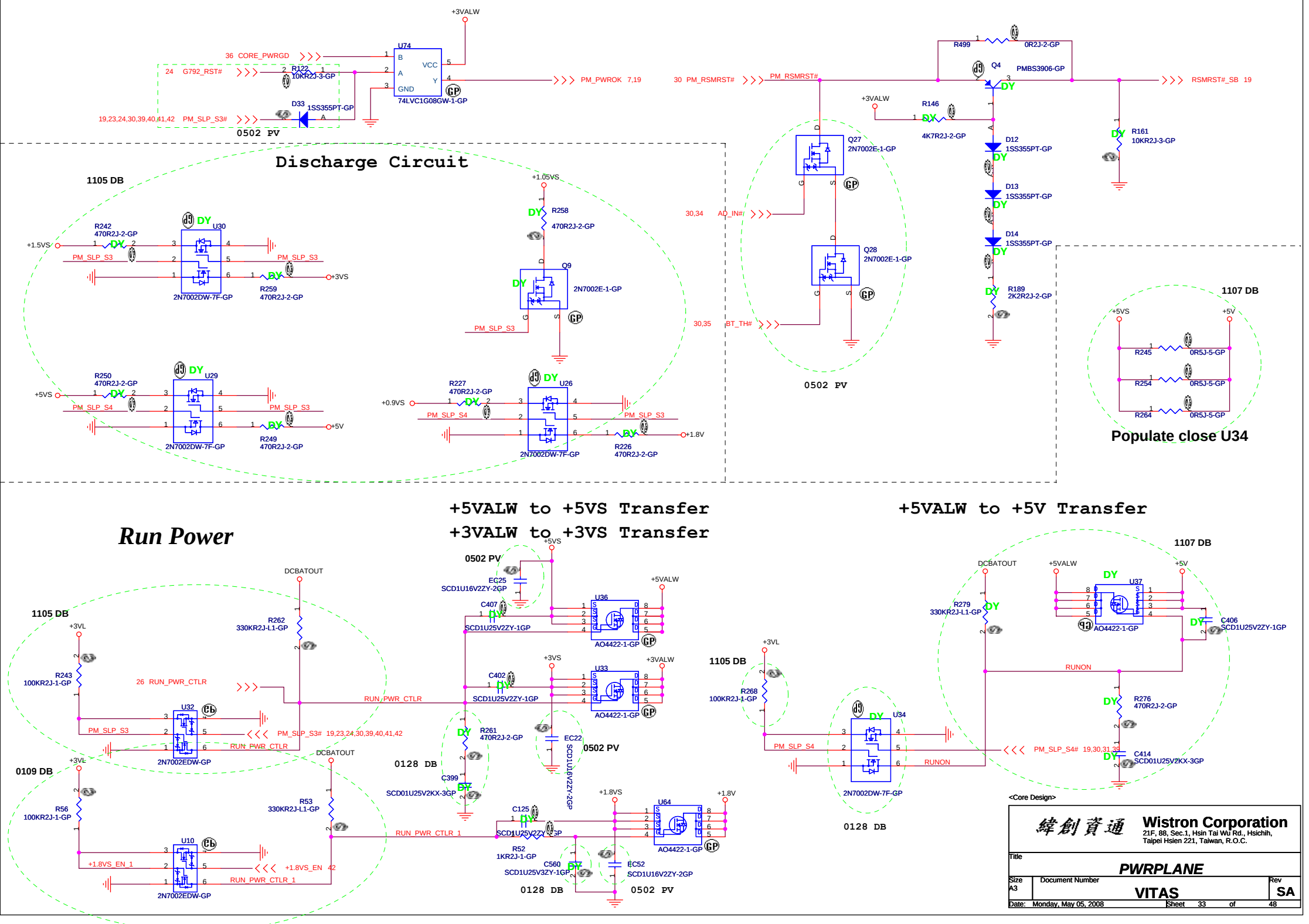
</core_design>


Discharge Circuit
1105 DB
0502 PV
1107 DB
Populate close U34
Run Power
+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+5VALW to +5V Transfer
0109 DB
0128 DB
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PWRPLANE
Size A3
Document Number
VITAS
Rev SA
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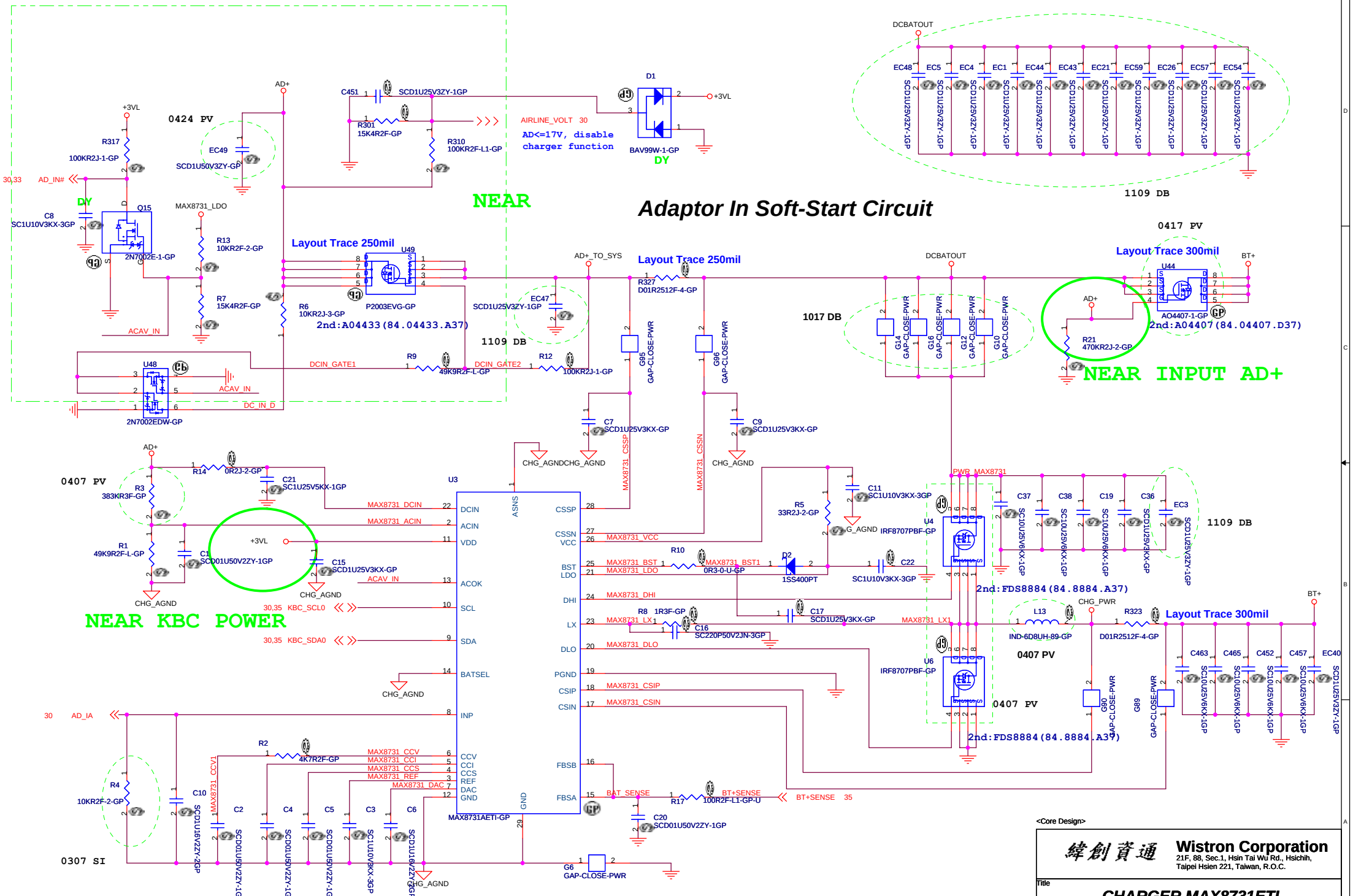
Adaptor In Soft-Start Circuit
NEAR
NEAR INPUT AD+
NEAR KBC POWER
0424 PV
0407 PV
0417 PV
0307 SI
1109 DB
1017 DB
Layout Trace 250mil
Layout Trace 300mil
2nd:A04433(84.04433.A37)
2nd:A04407(84.04407.D37)
2nd:FDS8884(84.8884.A37)
AD<=17V, disable charger function
MAX8731AETI-GP
Need Check MAXIM Sming Use MAX8731 or MAX8731A
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8731ETI
VITAS
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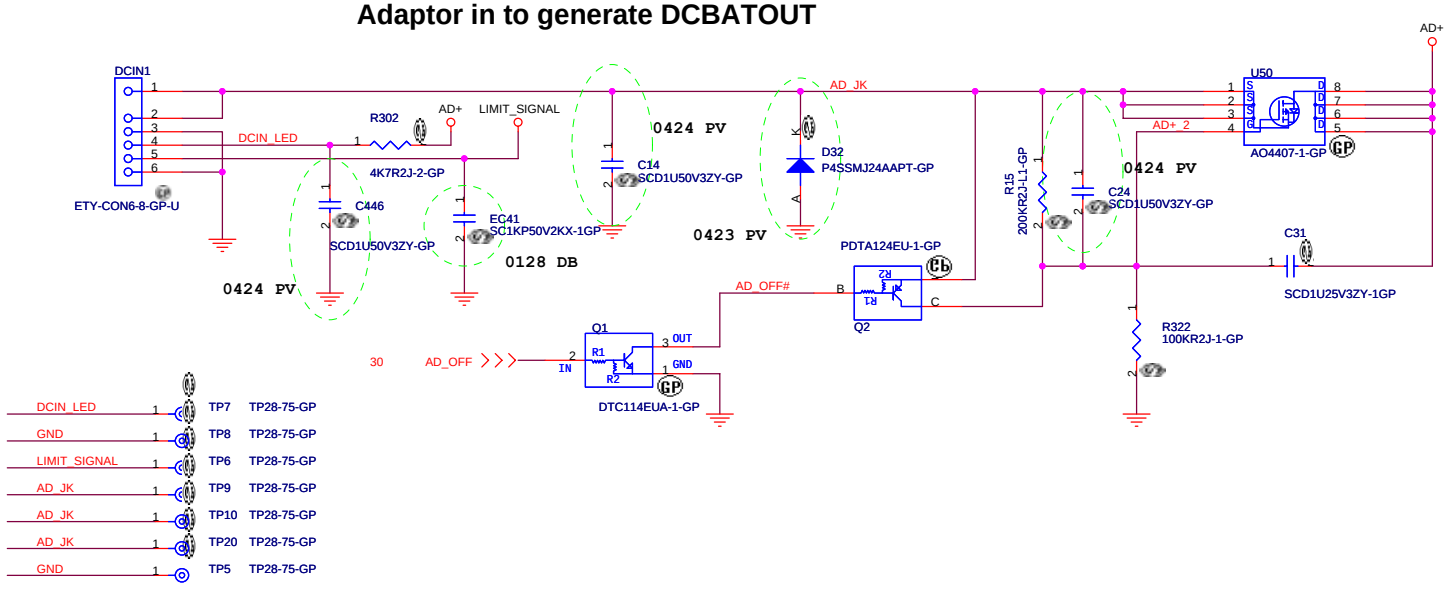
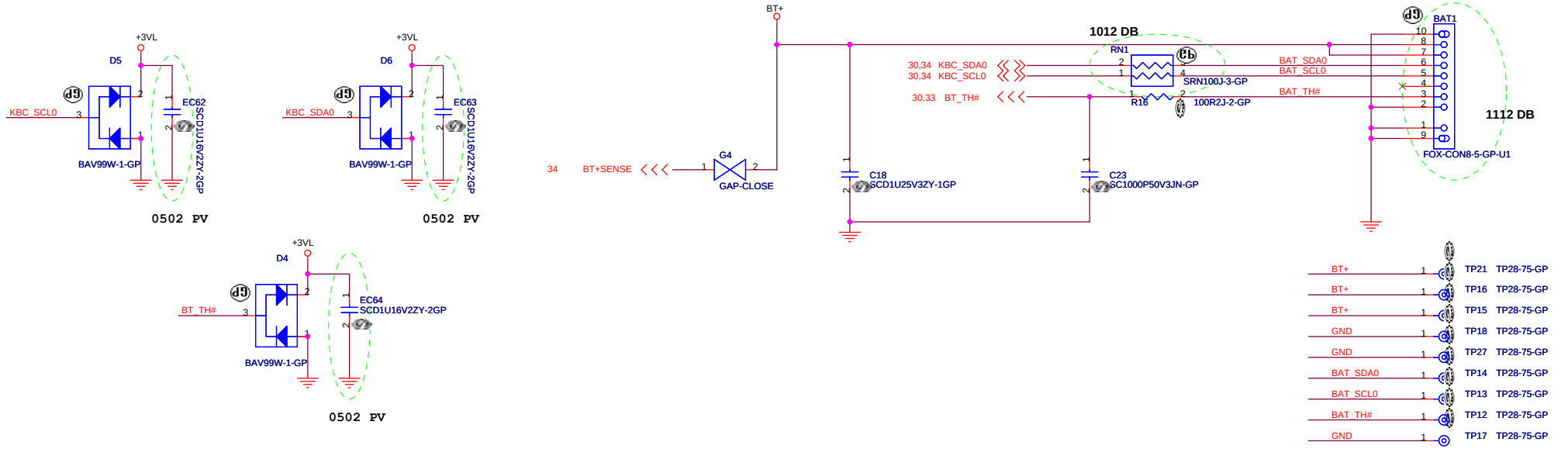
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AD/BATT CONN***

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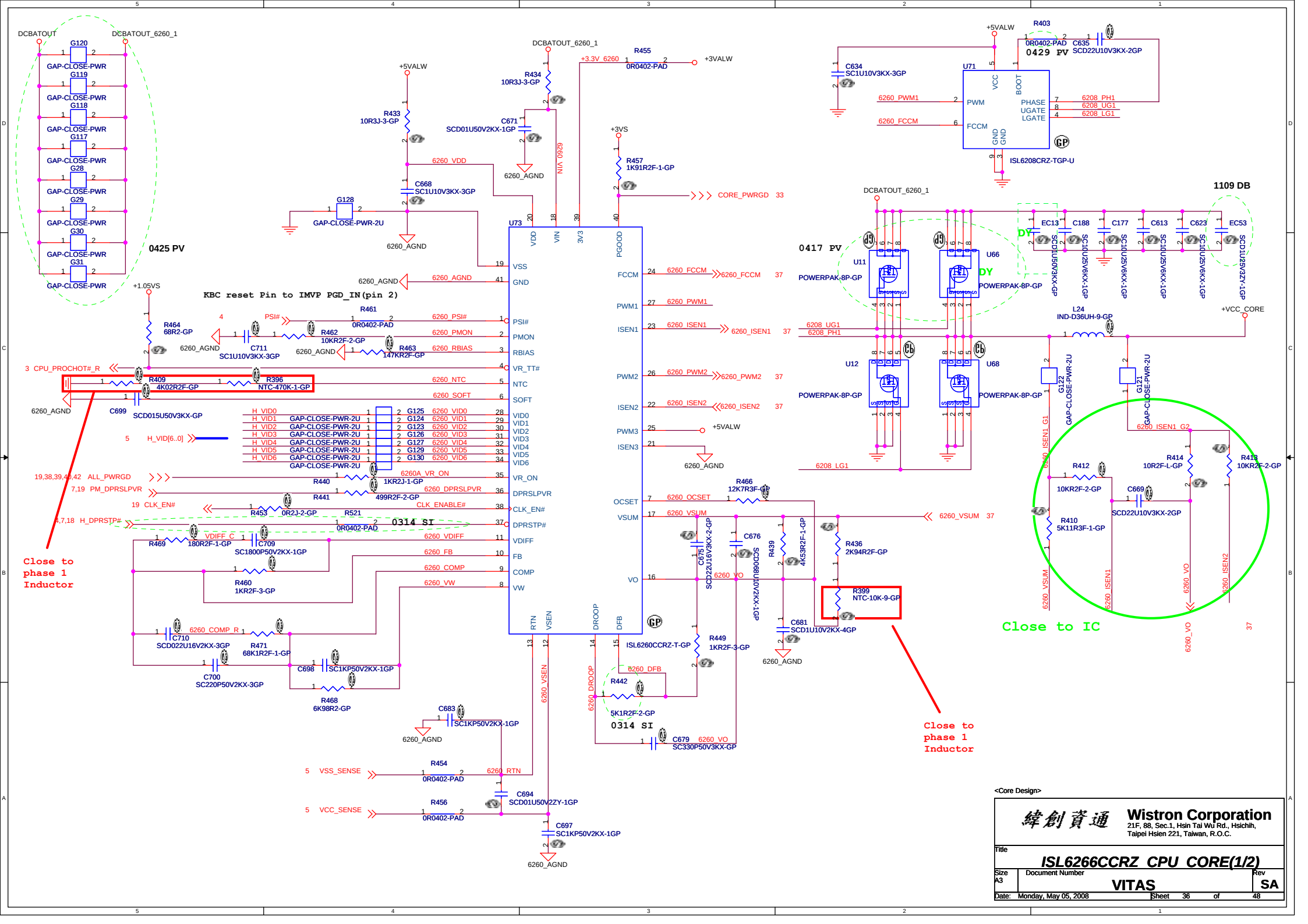
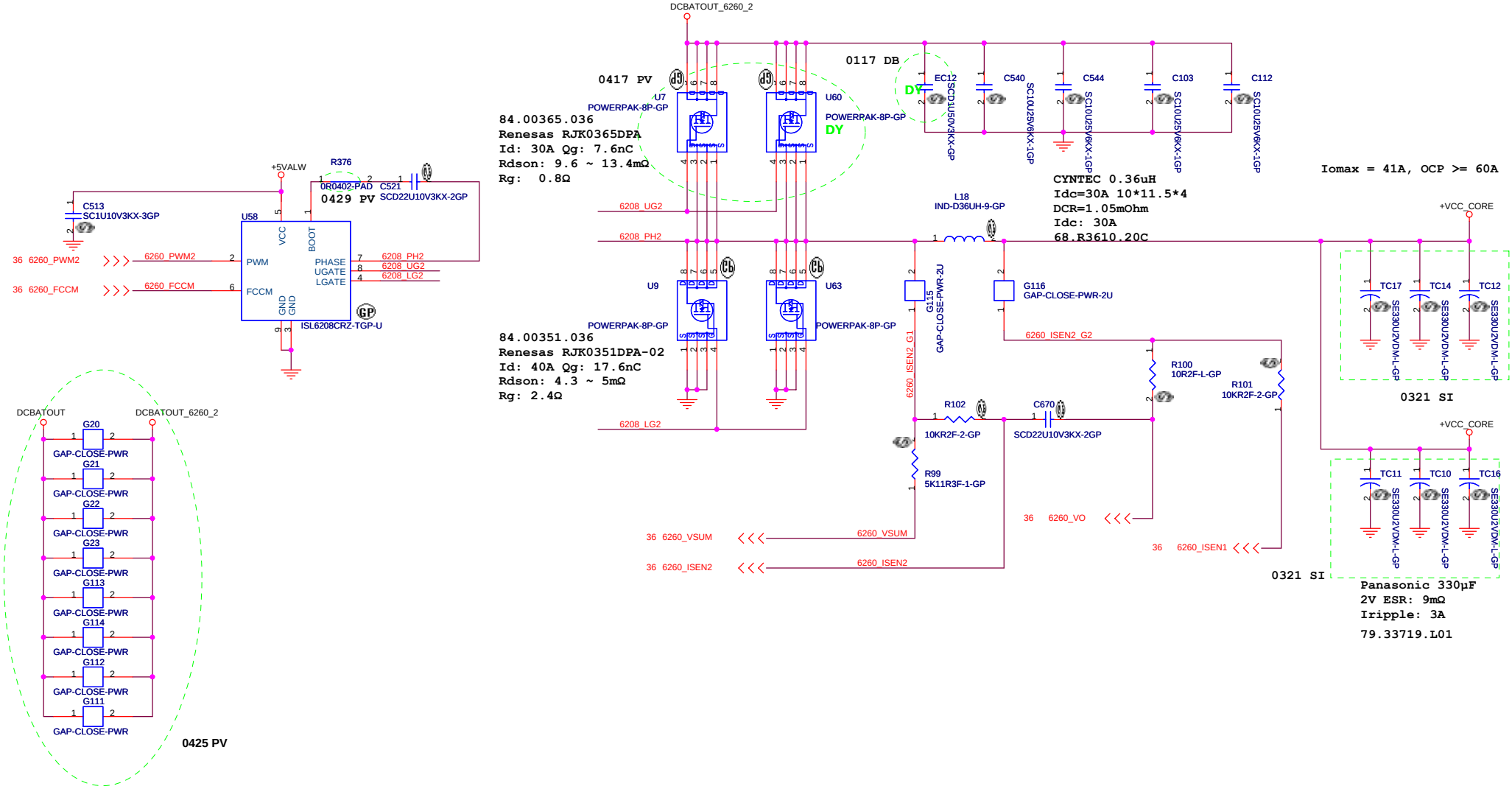
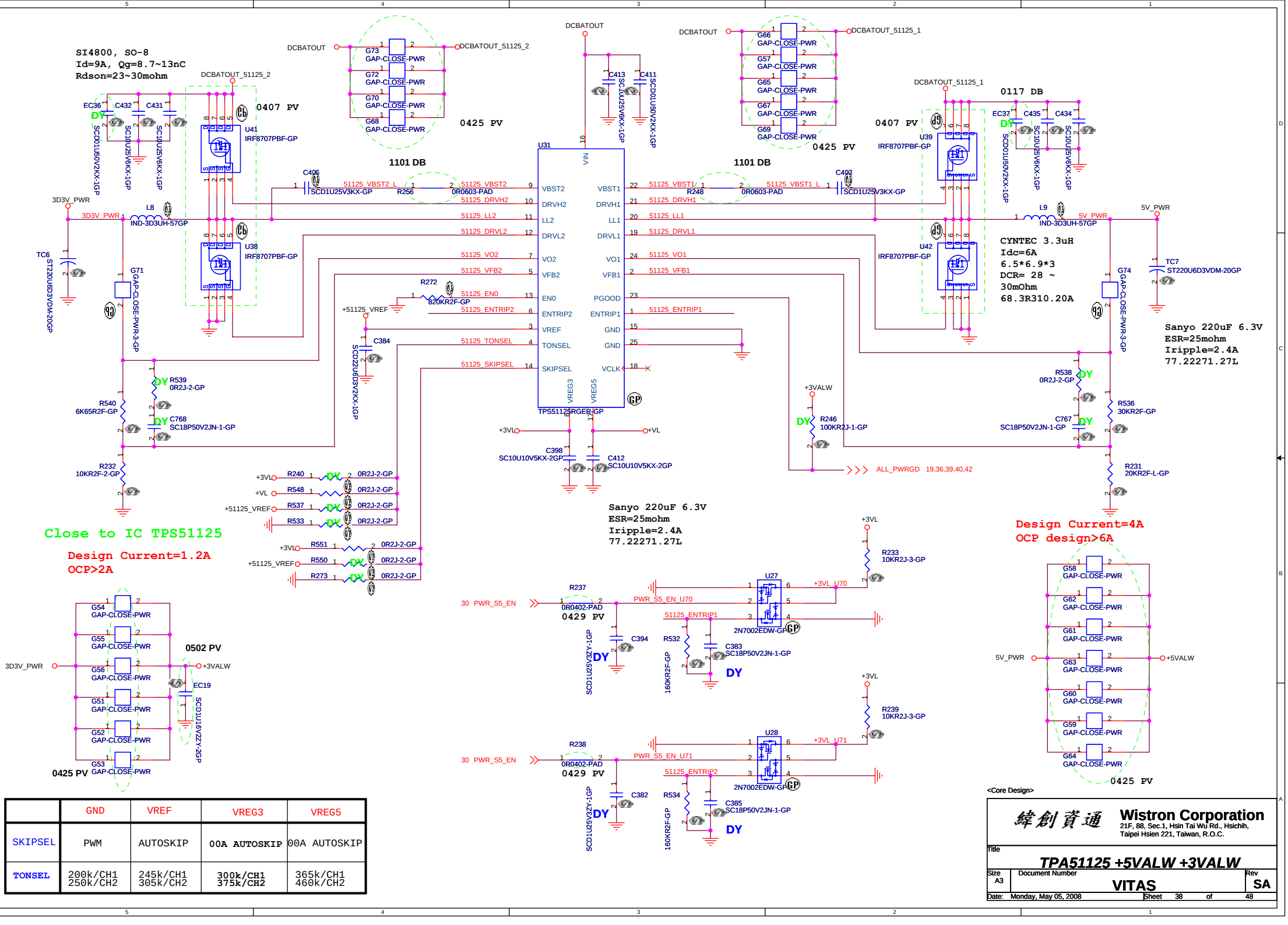

DCBATOUT
DCBATOUT_6260_1
G120
G119
G118
G117
G28
G29
G30
G31
GAP-CLOSE-PWR
0425 PV
+5VALW
+3.3V_6260
+3VALW
R455
0R0402-PAD
R434
10R3J-3-GP
R433
10R3J-3-GP
C671
SCD01U50V2KX-1GP
6260_AGND
6260_VDD
N/A 0929
+3VS
R457
1K91R2F-1-GP
CORE_PWRGD 33
C668
SC1U10V3KX-3GP
G128
GAP-CLOSE-PWR-2U
U73
VDD
VIN
3V3
PGOOD
VSS
GND
FCCM
PWM1
ISEN1
PWM2
ISEN2
PWM3
ISEN3
OCSET
VSUM
VO
RTN
VSEN
DROOP
DFB
ISL6260CCRZ-T-GP
+1.05VS
KBC reset Pin to IMVP PGD_IN(pin 2)
R461
0R0402-PAD
R464
68R2-GP
C711
SC1U10V3KX-3GP
R462
10KR2F-2-GP
R463
147KR2F-GP
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
VID0
VID1
VID2
VID3
VID4
VID5
VID6
3 CPU_PROCHOT#_R
R409
4K02R2F-GP
R396
NTC-470K-1-GP
C699
SCD015U50V3KX-GP
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
5 H_VID[6..0]
19,38,39,40,42 ALL_PWRGD
7,19 PM_DPRSLPVR
19 CLK_EN#
17,18 H_DPRSTP#
6260A_VR_ON
R440
1KR2J-1-GP
R441
499R2F-2-GP
R453
0R2J-2-GP
R521
0R0402-PAD
0314 SI
VR_ON
DPRSLPVR
CLK_EN#
DPRSTP#
VDIFF
FB
COMP
VW
R469
180R2F-1-GP
C709
SC1800P50V2KX-1GP
R460
1KR2F-3-GP
C710
SCD022U16V2KX-3GP
R471
68K1R2F-1-GP
C700
SC220P50V2KX-3GP
C698
SC1KP50V2KX-1GP
R468
6K98R2-GP
C683
SC1KP50V2KX-1GP
R454
0R0402-PAD
R456
0R0402-PAD
C694
SCD01U50V2ZY-1GP
C697
SC1KP50V2KX-1GP
5 VSS_SENSE
5 VCC_SENSE
R466
12K7R3F
C675
SCD22U16V3KX-2-GP
C676
SCD068U10V2KX-1GP
R439
4K53R2F-1-GP
R436
2K94R2F-GP
R399
NTC-10K-9-GP
C681
SCD1U10V2KX-4GP
R449
1KR2F-3-GP
R442
5K1R2F-2-GP
C679
SC330P50V3KX-GP
Close to phase 1 Inductor
Close to phase 1 Inductor
R403
0R0402-PAD
0429 PV
C635
SCD22U10V3KX-2GP
C634
SC1U10V3KX-3GP
U71
VCC
BOOT
PWM
PHASE
UGATE
LGATE
FCCM
GND
6260_PWM1
6260_FCCM
6208_PH1
6208_UG1
6208_LG1
ISL6208CRZ-TGP-U
1109 DB
0417 PV
U11
U66
U12
U68
POWERPAK-8P-GP
DY
EC13
C188
C177
C613
C623
EC53
SCD1U25V6KX-1GP
SCD1U25V2ZY-1GP
L24
IND-D36UH-9-GP
+VCC_CORE
6208_UG1
6208_PH1
6208_LG1
G122
G121
GAP-CLOSE-PWR-2U
6260_ISEN1_G1
6260_ISEN1_G2
R412
10KR2F-2-GP
R414
10R2F-L-GP
R413
10KR2F-2-GP
C669
SCD22U10V3KX-2GP
R410
5K11R3F-1-GP
6260_VSUM
6260_ISEN1
6260_VO
6260_ISEN2
Close to IC
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266CCRZ CPU CORE(1/2)
Size A3
Document Number
VITAS
Rev SA
Date: Monday, May 05, 2008
Sheet 36 of 48



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***ISL6260CCRZ CPU CORE(2/2)***
Size A3	Document Number: **VITAS**
Rev	**SA**
Date: Monday, May 05, 2008	Sheet 37 of 48



	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

Company	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TPA51125 +5VALW +3VALW
Size	A3
Document Number	VITAS
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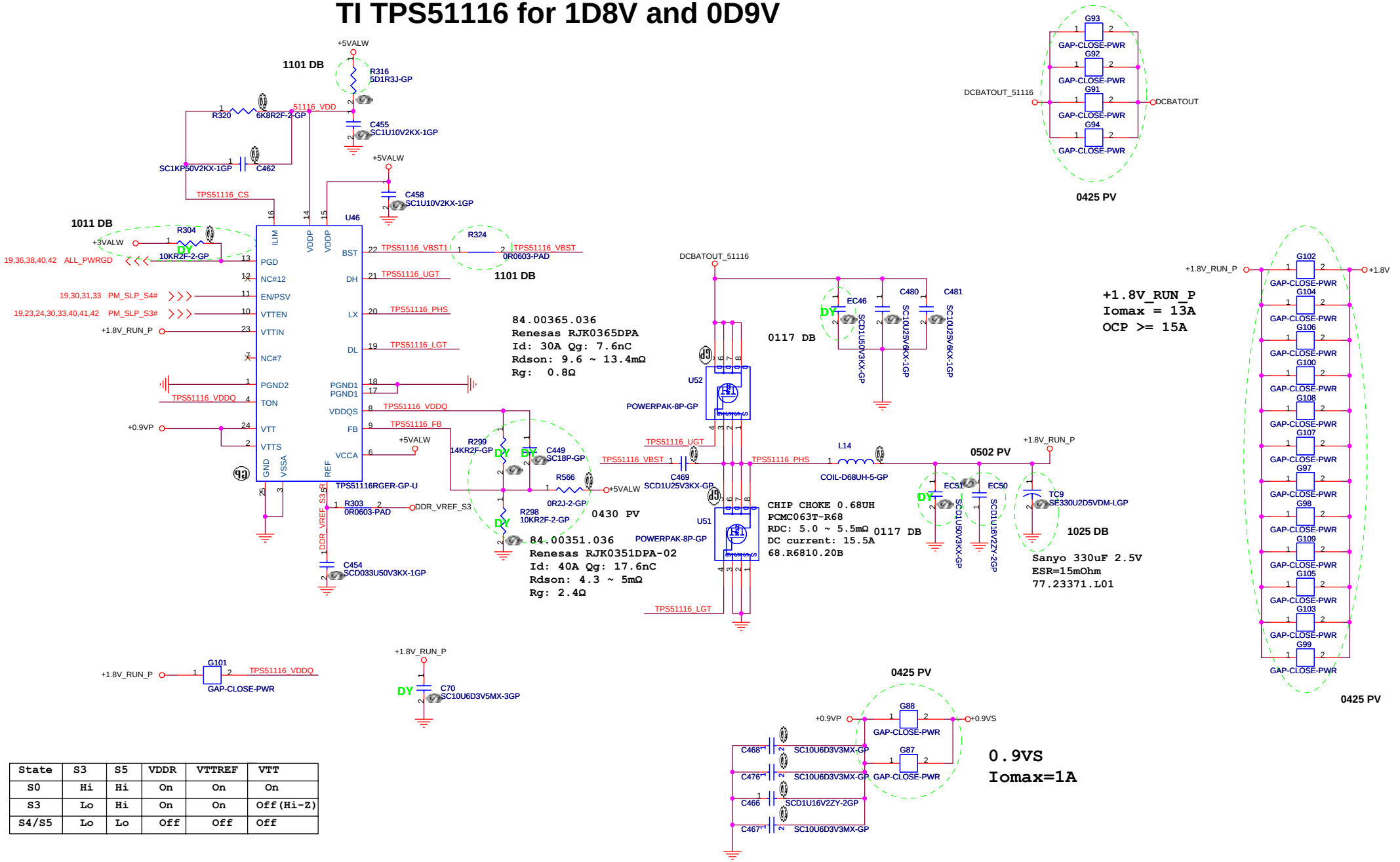
TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

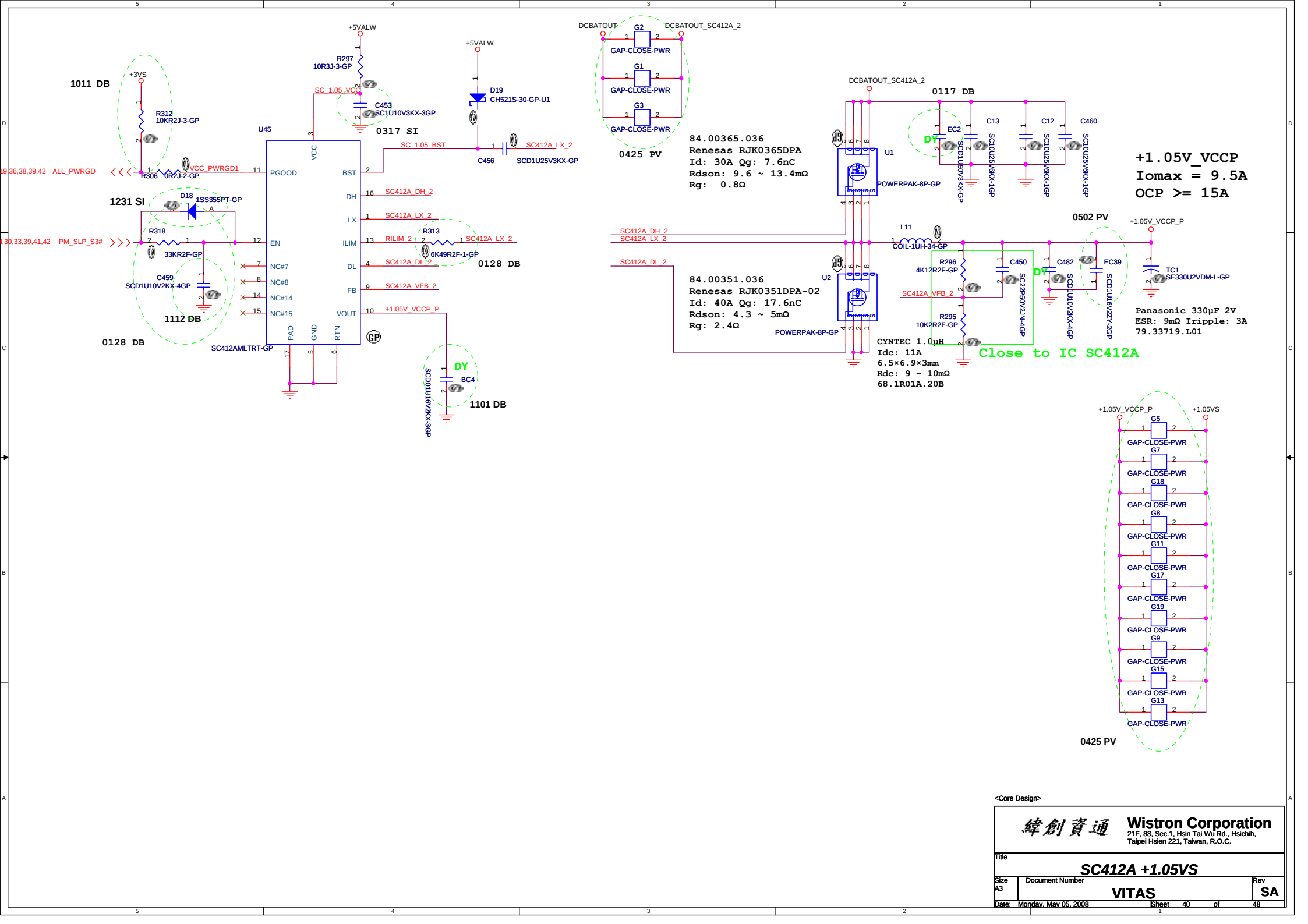
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: VITAS | Rev: SA

Date: Monday, May 05, 2008 | Sheet 39 of 48



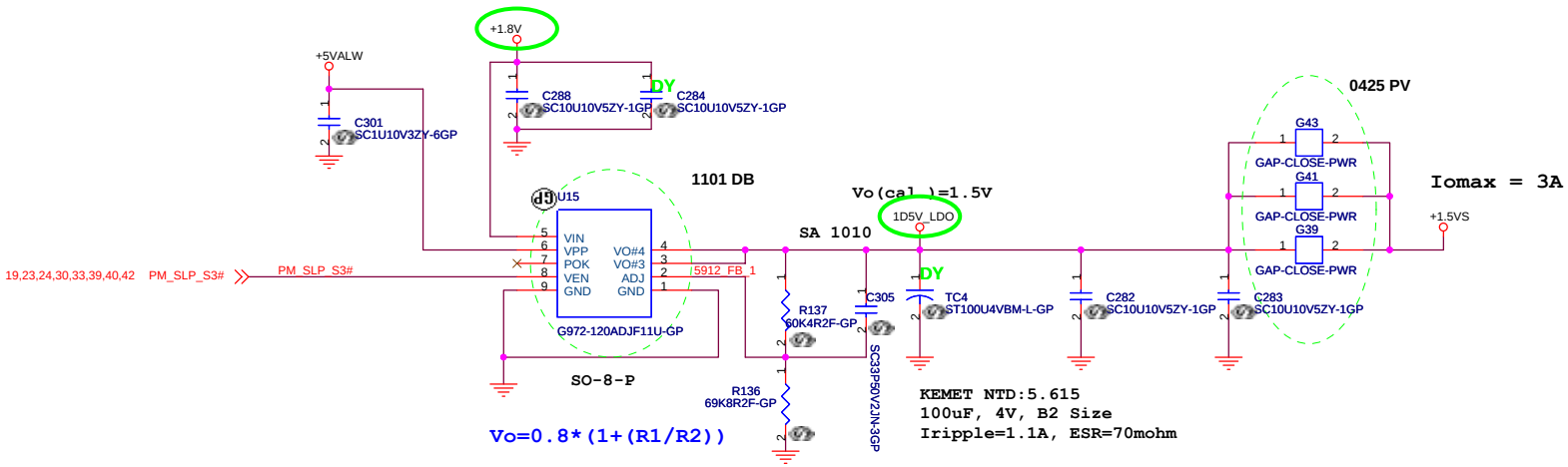
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SC412A +1.05VS***

Size	Document Number	Rev
A3	VITAS	SA

Date: Monday, May 05, 2008 Sheet 40 of 48



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GMT 1D5V LDO***

Size	Document Number	Rev
A3	VITAS	SA

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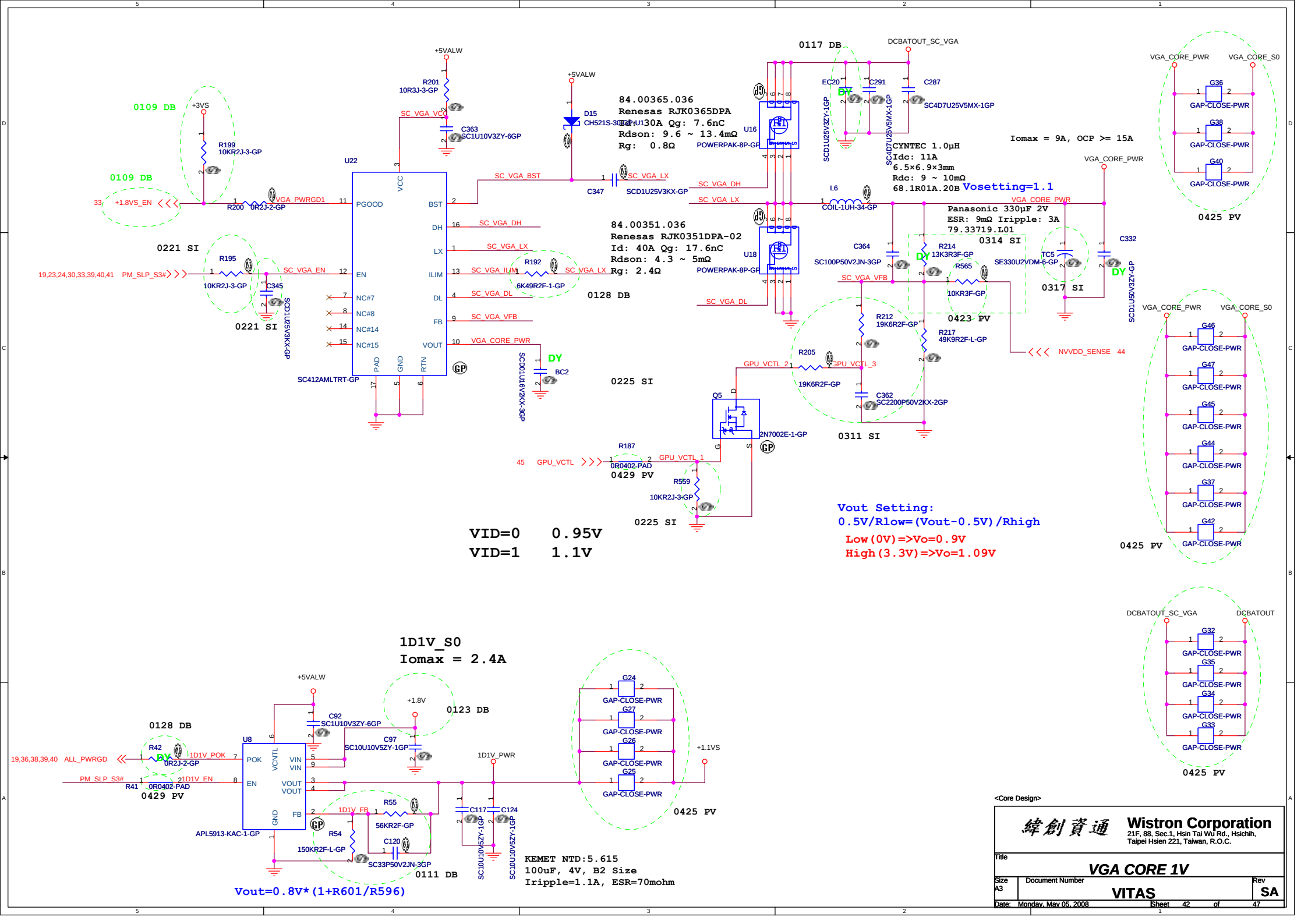
0109 DB
+3VS
R199
10KR2J-3-GP
0109 DB
33
+1.8VS_EN
R200 0R2J-2-GP
VGA_PWRGD1
+5VALW
R201
10R3J-3-GP
SC_VGA_VCC
C363
SC1U10V3ZY-6GP
U22
VCC
PGOOD
EN
NC#7
NC#8
NC#14
NC#15
PAD
GND
RTN
BST
DH
LX
ILIM
DL
FB
VOUT
SC412AMLTRT-GP
SC_VGA_BST
SC_VGA_DH
SC_VGA_LX
SC_VGA_ILIM
SC_VGA_DL
SC_VGA_VFB
VGA_CORE_PWR
0221 SI
R195
19,23,24,30,33,39,40,41
PM_SLP_S3#
10KR2J-3-GP
SC_VGA_EN
C345
SCD1U25V3KX-GP
0221 SI
R192
6K49R2F-1-GP
SC_VGA_LX
0128 DB
+5VALW
D15
CH521S-30-GP
C347
SCD1U25V3KX-GP
84.00365.036
Renesas RJK0365DPA
Id: 30A Qg: 7.6nC
Rdson: 9.6 ~ 13.4mΩ
Rg: 0.8Ω
U16
POWERPAK-8P-GP
84.00351.036
Renesas RJK0351DPA-02
Id: 40A Qg: 17.6nC
Rdson: 4.3 ~ 5mΩ
Rg: 2.4Ω
U18
POWERPAK-8P-GP
0117 DB
DCBATOUT_SC_VGA
EC20
DY
C291
C287
SC4D7U25V5MX-1GP
SCD1U25V3ZY-1GP
SC4D7U25V5MX-1GP
CYNTEC 1.0μH
Idc: 11A
6.5×6.9×3mm
Rdc: 9 ~ 10mΩ
68.1R01A.20B
Vosetting=1.1
Iomax = 9A, OCP >= 15A
L6
COIL-1UH-34-GP
VGA_CORE_PWR
Panasonic 330μF 2V
ESR: 9mΩ Iripple: 3A
79.33719.L01
0314 SI
C364
SC100P50V2JN-3GP
DY
R214
13K3R3F-GP
R565
10KR3F-GP
0423 PV
TC5
SE330U2VDM-6-GP
0317 SI
C332
DY
SCD1U50V3ZY-GP
NVVDD_SENSE 44
R212
19K6R2F-GP
R217
49K9R2F-L-GP
R205
19K6R2F-GP
GPU_VCTL_2
GPU_VCTL_3
C362
SC2200P50V2KX-2GP
0311 SI
0225 SI
Q5
2N7002E-1-GP
R187
0R0402-PAD
45
GPU_VCTL
GPU_VCTL_1
0429 PV
R559
10KR2J-3-GP
0225 SI
VID=0 0.95V
VID=1 1.1V
Vout Setting:
0.5V/Rlow=(Vout-0.5V)/Rhigh
Low(0V)=>Vo=0.9V
High(3.3V)=>Vo=1.09V
VGA_CORE_PWR
VGA_CORE_S0
G36
G38
G40
GAP-CLOSE-PWR
0425 PV
G46
G47
G45
G44
G37
G42
0425 PV
DCBATOUT_SC_VGA
DCBATOUT
G32
G35
G34
G33
0425 PV
1D1V_S0
Iomax = 2.4A
+5VALW
+1.8V
0123 DB
0128 DB
R42
19,36,38,39,40
ALL_PWRGD
DY
0R2J-2-GP
1D1V_POK
PM_SLP_S3#
R41
0R0402-PAD
0429 PV
1D1V_EN
U8
POK
EN
VCNTL
VIN
VOUT
GND
FB
APL5913-KAC-1-GP
C92
SC1U10V3ZY-6GP
C97
SC10U10V5ZY-1GP
1D1V_PWR
R55
56KR2F-GP
1D1V_FB
R54
150KR2F-L-GP
C120
SC33P50V2JN-3GP
0111 DB
C117
C124
SC10U10V5ZY-1GP
SC10U10V5ZY-1GP
G24
G27
G26
G25
GAP-CLOSE-PWR
+1.1VS
0425 PV
KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
Vout=0.8V*(1+R601/R596)
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA CORE 1V
Size
A3
Document Number
VITAS
Rev
SA
Date: Monday, May 05, 2008
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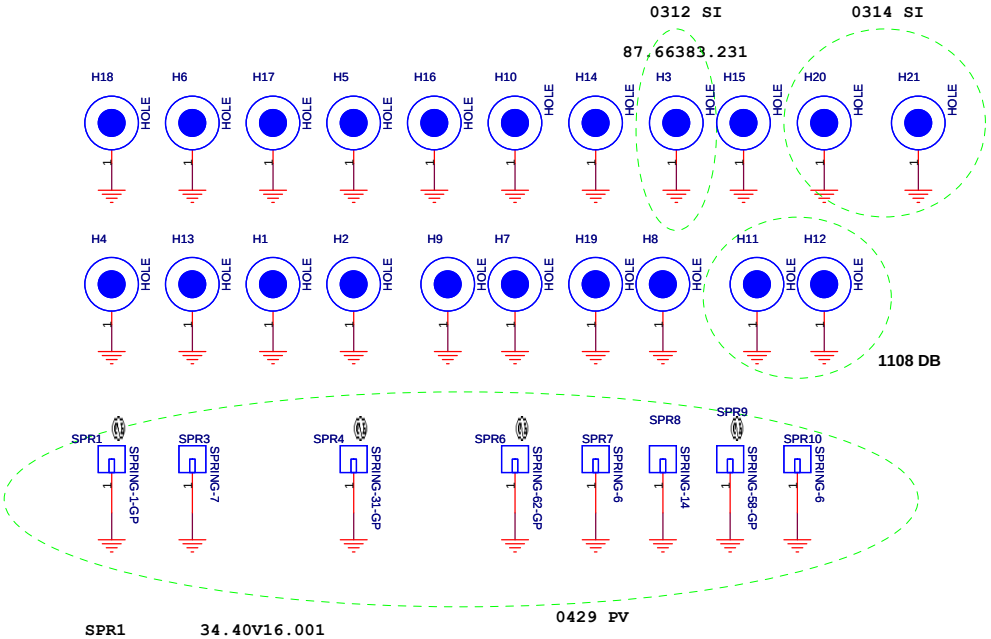


SPR1	34.40V16.001
SPR3	34.49U26.001
SPR4	34.49U24.001
SPR6	34.39S07.003
SPR7	34.13B01.001
SPR8	34.41V01.001
SPR9	34.4B312.002
SPR10	34.13B01.001

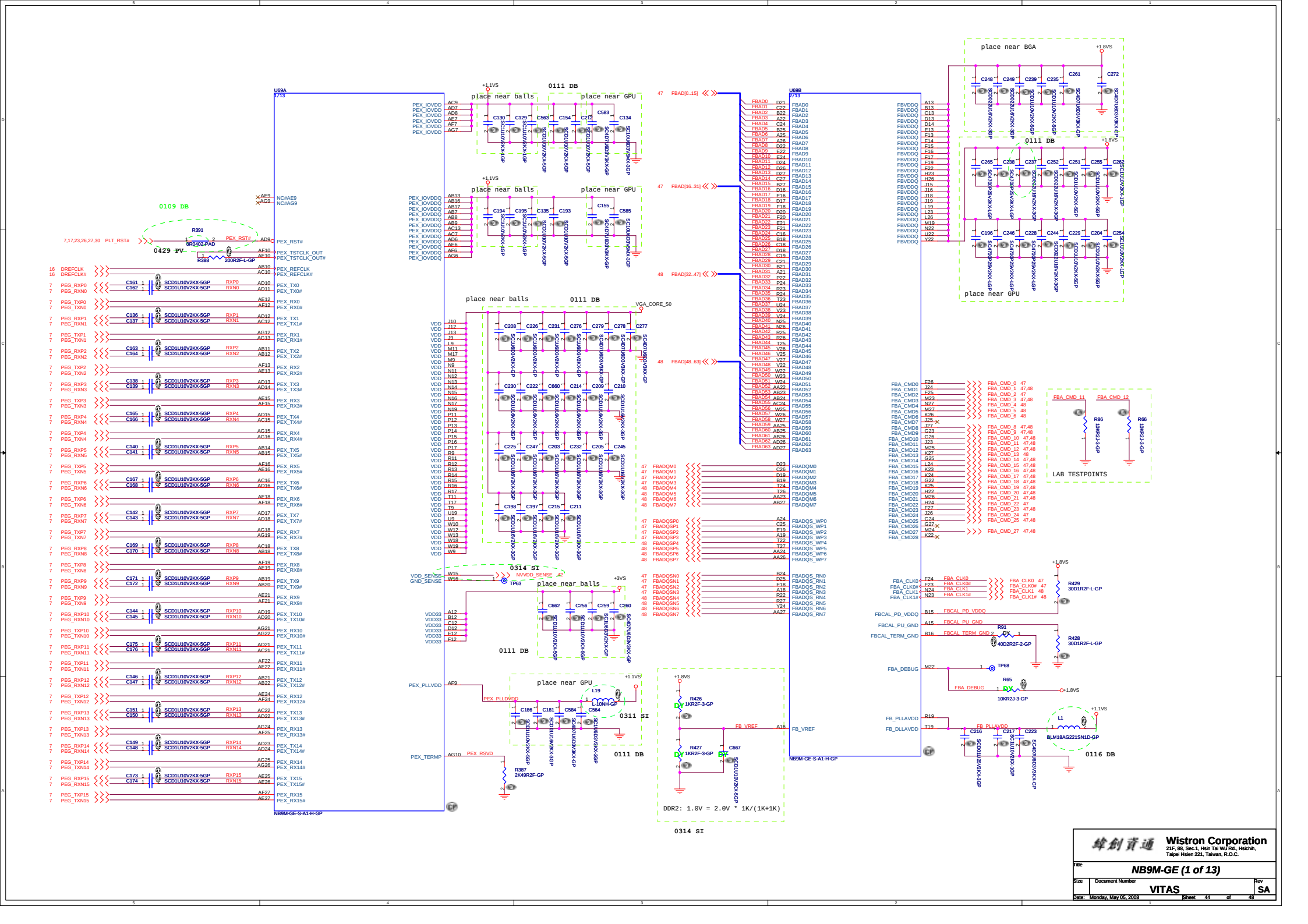
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

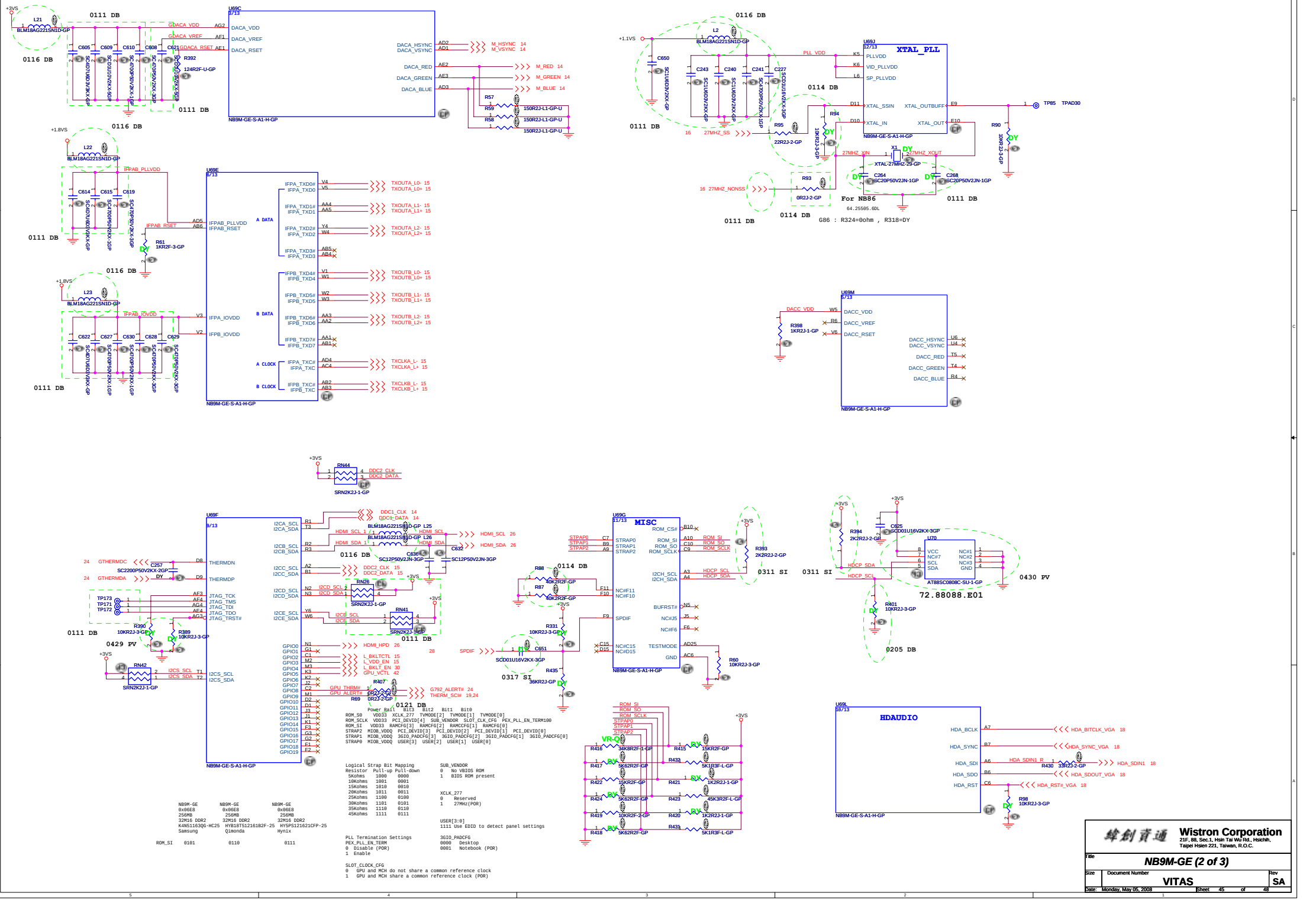
Title: ***MISC***

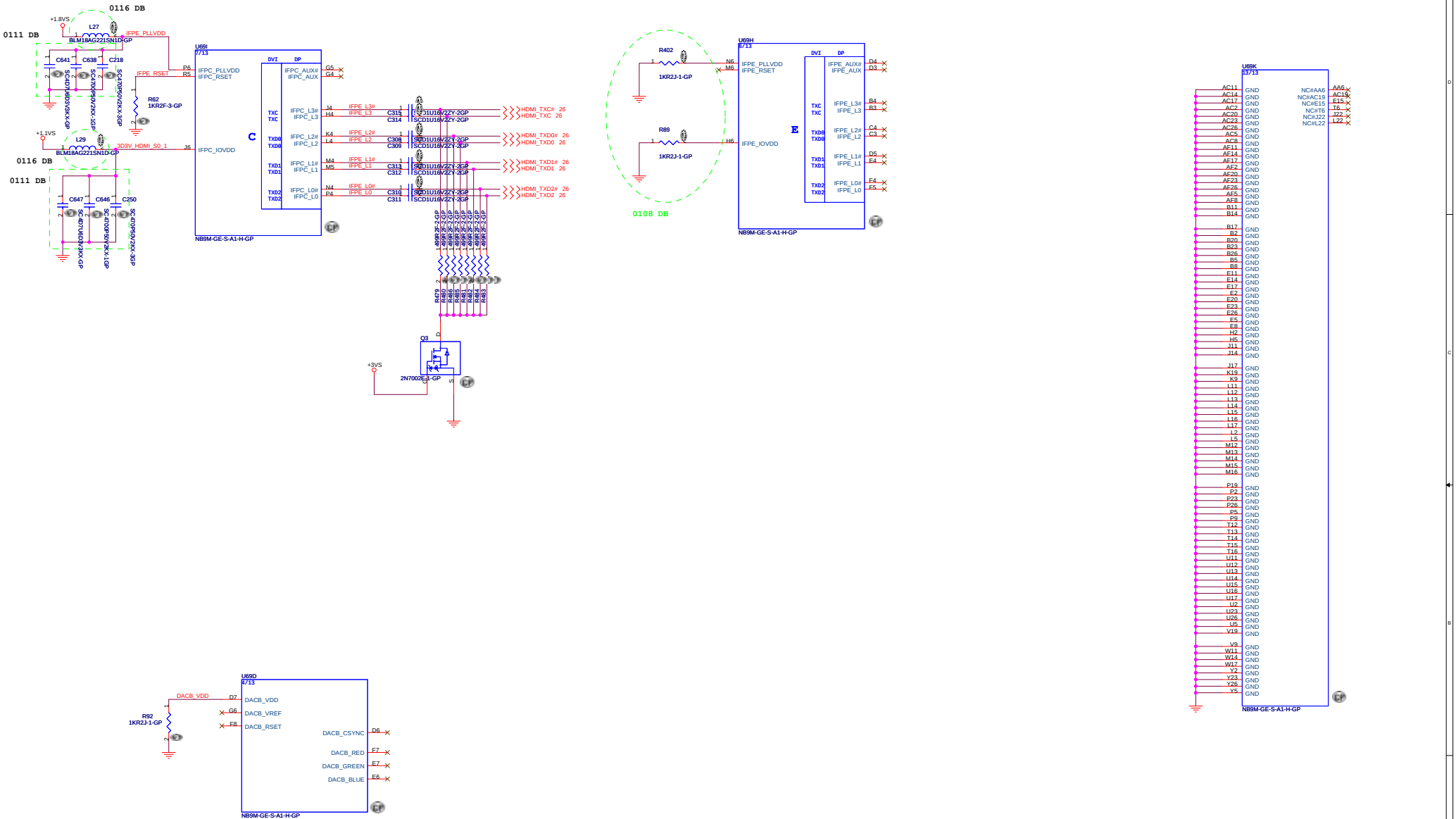
Size: A3 | Document Number: **VITAS** | Rev: **SA**

Date: Monday, May 05, 2008 | Sheet 43 of 48

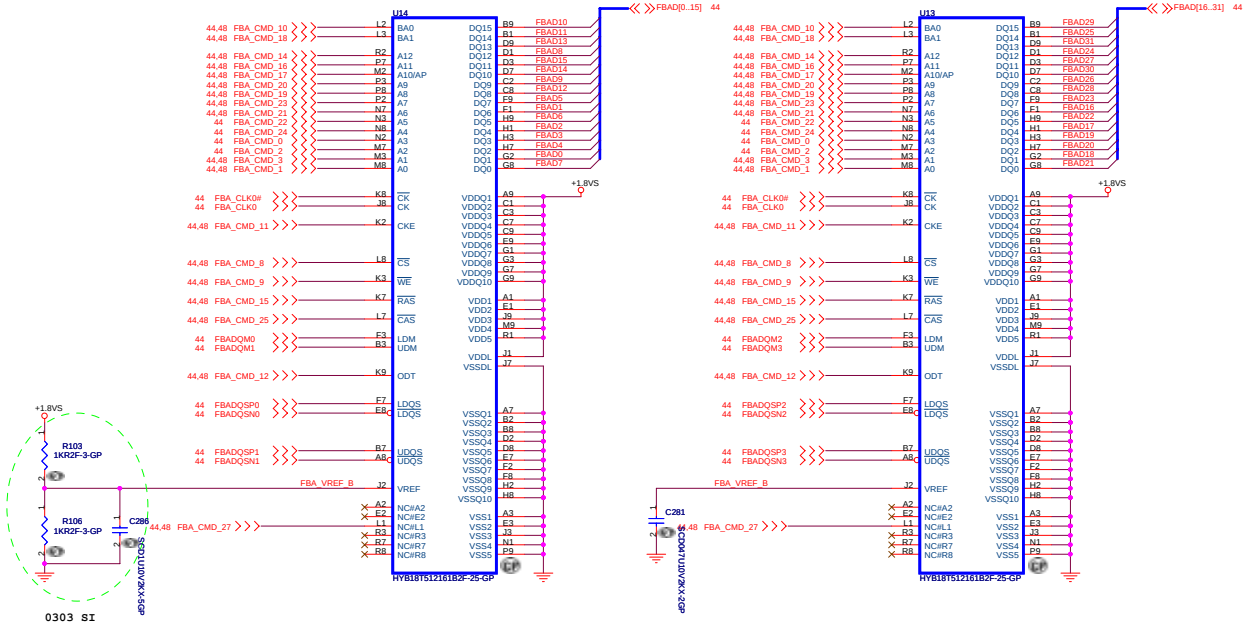


Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	NB9M-GE (1 of 13)
Size	Document Number: VITAS — Rev: SA
Date: Monday, May 05, 2008	Sheet 44 of 48

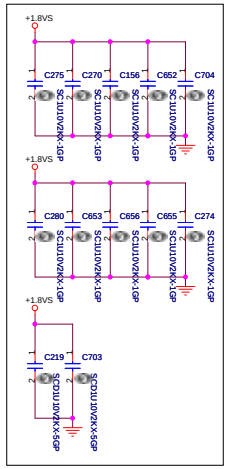

0111 DB
0116 DB
U69C
9/13
DACA_VDD
DACA_VREF
DACA_RSET
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
M_HSYNC 14
M_VSYNC 14
M_RED 14
M_GREEN 14
M_BLUE 14
NB9M-GE-S-A1-H-GP
0114 DB
U69J
12/13
XTAL_PLL
PLLVDD
VID_PLLVDD
SP_PLLVDD
XTAL_SSIN
XTAL_IN
XTAL_OUTBUFF
XTAL_OUT
TP85 TPAD30
27MHZ_SS
27MHZ_XIN
27MHZ_XOUT
XTAL-27MHZ-2S-GP
For NB86
64.25505.6DL
0111 DB
0114 DB
G86 : R324=0ohm , R318=DY
U69E
9/13
IFPAB_PLLVDD
IFPAB_RSET
IFPA_IOVDD
IFPB_IOVDD
A DATA
B DATA
A CLOCK
B CLOCK
TXOUTA_L0- 15
TXOUTA_L0+ 15
TXOUTA_L1- 15
TXOUTA_L1+ 15
TXOUTA_L2- 15
TXOUTA_L2+ 15
TXOUTB_L0- 15
TXOUTB_L0+ 15
TXOUTB_L1- 15
TXOUTB_L1+ 15
TXOUTB_L2- 15
TXOUTB_L2+ 15
TXCLKA_L- 15
TXCLKA_L+ 15
TXCLKB_L- 15
TXCLKB_L+ 15
U69M
6/13
DACC_VDD
DACC_VREF
DACC_RSET
DACC_HSYNC
DACC_VSYNC
DACC_RED
DACC_GREEN
DACC_BLUE
U69F
9/13
I2CA_SCL
I2CA_SDA
I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
I2CD_SCL
I2CD_SDA
I2CE_SCL
I2CE_SDA
I2CS_SCL
I2CS_SDA
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
THERMDN
THERMDP
GTHERMDC
GTHERMDA
DDC1_CLK 14
DDC1_DATA 14
HDMI_SCL 26
HDMI_SDA 26
DDC2_CLK 15
DDC2_DATA 15
HDMI_HPD 26
L_BKLTCTL 15
L_VDD_EN 15
L_BKLT_EN 30
GPU_VCTL 42
GPU_THRM#
GPU_ALERT#
G792_ALERT# 24
THERM_SCH# 19,24
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
NB9M-GE-S-A1-H-GP
0121 DB
Power Rail Bit3 Bit2 Bit1 Bit0
ROM_S0 VDD33 XCLK_277 TVMODE[2] TVMODE[1] TVMODE[0]
ROM_SCLK VDD33 PCI_DEVID[4] SUB_VENDOR SLOT_CLK_CFG PEX_PLL_EN_TERM100
ROM_SI VDD33 RAMCFG[3] RAMCFG[2] RAMCCFG[1] RAMCFG[0]
STRAP2 MIOB_VDDQ PCI_DEVID[3] PCI_DEVID[2] PCI_DEVID[1] PCI_DEVID[0]
STRAP1 MIOB_VDDQ 3GIO_PADCFG[3] 3GIO_PADCFG[2] 3GIO_PADCFG[1] 3GIO_PADCFG[0]
STRAP0 MIOB_VDDQ USER[3] USER[2] USER[1] USER[0]
Logical Strap Bit Mapping
Resistor Pull-up Pull-down
5Kohms 1000 0000
10Kohms 1001 0001
15Kohms 1010 0010
20Kohms 1011 0011
25Kohms 1100 0100
30Kohms 1101 0101
35Kohms 1110 0110
45Kohms 1111 0111
SUB_VENDOR
0 No VBIOS ROM
1 BIOS ROM present
XCLK_277
0 Reserved
1 27MHz(POR)
USER[3:0]
1111 Use EDID to detect panel settings
PLL Termination Settings
PEX_PLL_EN_TERM
0 Disable (POR)
1 Enable
3GIO_PADCFG
0000 Desktop
0001 Notebook (POR)
SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)
NB9M-GE 0x06E8 256MB 32M16 DDR2 K4N51163QG-HC25 Samsung
NB9M-GE 0x06E8 256MB 32M16 DDR2 HY18T512161B2F-25 Qimonda
NB9M-GE 0x06E8 256MB 32M16 DDR2 H Y5PS121621CFP-25 Hynix
ROM_SI 0101 0110 0111
0429 PV
0317 SI
0311 SI
0205 DB
0430 PV
72.88088.E01
U69G
11/13
MISC
ROM_CS#
ROM_SI
ROM_SO
ROM_SCLK
STRAP0
STRAP1
STRAP2
I2CH_SCL
I2CH_SDA
HDCP_SCL
HDCP_SDA
SPDIF
BUFRST#
NC#F11
NC#F10
NC#J5
NC#F6
NC#C15
NC#D15
TESTMODE
GND
NB9M-GE-S-A1-H-GP
U70
AT88SC0808C-SU-1-GP
U69L
10/13
HDAUDIO
HDA_BCLK
HDA_SYNC
HDA_SDI
HDA_SDO
HDA_RST
HDA_BITCLK_VGA 18
HDA_SYNC_VGA 18
HDA_SDIN1 18
HDA_SDOUT_VGA 18
HDA_RST#_VGA 18
NB9M-GE-S-A1-H-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB9M-GE (2 of 3)
Size
Document Number
VITAS
Rev
SA
Date: Monday, May 05, 2008
Sheet 45 of 48



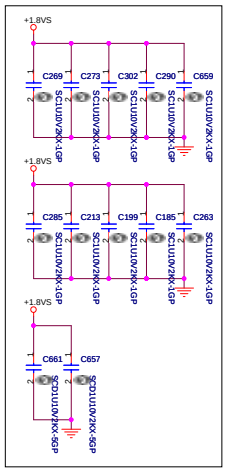
緯創資通	**Wistron Corporation**	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***NB9M-GE (3 of 3)***	
Size	Document Number: **VITAS**	Rev: **SA**
Date: Monday, May 05, 2008	Sheet 46 of 48	

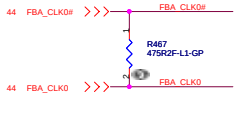


X - cap for CMD

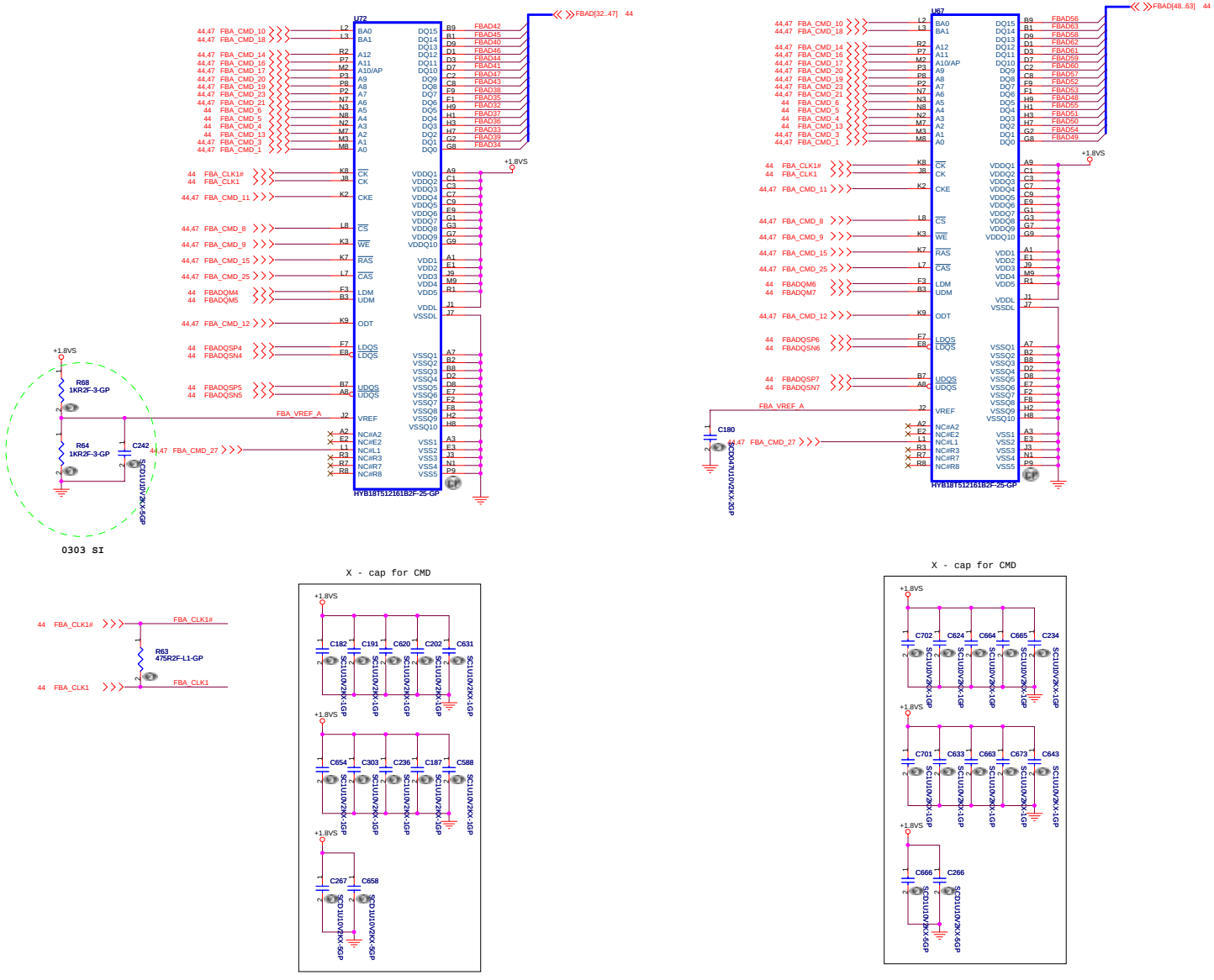


X - cap for CMD





蜂創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM1		
Size	Document Number: VITAS	Rev: SA
Date: Monday, May 05, 2008	Sheet 47 of 48	



X - cap for CMD

X - cap for CMD

蜂創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM2***	
Size	Document Number **VITAS**	Rev **SA**
Date: Monday, May 05, 2008	Sheet 48 of 48	