Volvi Block Diagram

Project code: 91.4U701.001
PCB P/N : 07200
REVISION : -1

CLK GEN.
ICS 9LPRS502
(RTM875T-605) 3
71.09502.00W

Mobile CPU
Yonah 478
Celeron M
62.10079.001 4, 5

G792 20

HOST BUS 400/533/667MHz@1.05V

DDR2 533/667 MHz 13,14
DDR2 533/667 MHz 13,14
533/667MHz
533/667MHz

Calistoga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CALIS.00U 6,7,8,9,10

TV Out 14
CRT 14
LCD 13
VGA Borad 26

X4 DMI 400MHz
C-Link0

ICH7M
4 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
2 SATA
1 PATA 66/100
8 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
71.ICH7M.00U
15,16,17,18

Line In
Codec ALC268 28
AZALIA
MIC In
14
31
INT.SPKR
OP AMP G1431Q 29
OP AMP G1412 29
Line Out (No-SPDIF)
RJ11
MODEM MDC Card 21

PCI BUS
OZ129 1394 CardReader 24
1394 CONN 25
Cardreader
MS/MS Pro/xD/ MMC/SD 5 in 1 25

Giga LAN 22 BCM5787MKMLG
TXFM 23
RJ45 23
PCIex1
Mini Card Kedron a/b/g/n 27

LPC BUS
New card 27
PCI Express
SATA
PATA
USB
MINI USB BlueTooth 22
KBC Winbond WPC8768L 30
SPI I/F
BIOS W25X80-VSS 32
LPC DEBUG CONN. 32

P2231NFC1 28
HDD 20
CDROM 20
MEDIA BD 31
Touch Pad 31
INT. KB 31
CIR 31
USB 4 Port 21
CAMERA 13

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC
MAX8744 36

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC
MAX8717 37

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D05V_S0

TPS51100 39

1D8V_S3	DDR_VREF

APL5312 39

3D3V_S0	2D5V_S0

APL5912 38

1D8V_S3	1D5V_S0

Intersil CHARGER
MAX8731 40

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
MAX8770 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

UMA

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: Volvi | Rev: -1
Date: Wednesday, April 18, 2007 | Sheet 1 of 43

ICH7M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH7M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

PCI Routing

page 16

	IDSEL	INT	REQ	GNT
OZ129	AD22	INT_PIRQG#	PCI_REQ#0	PCI_GNT#0

UMA

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Title: Reference

Size: A3 | Document Number: Volvi | Rev: -1

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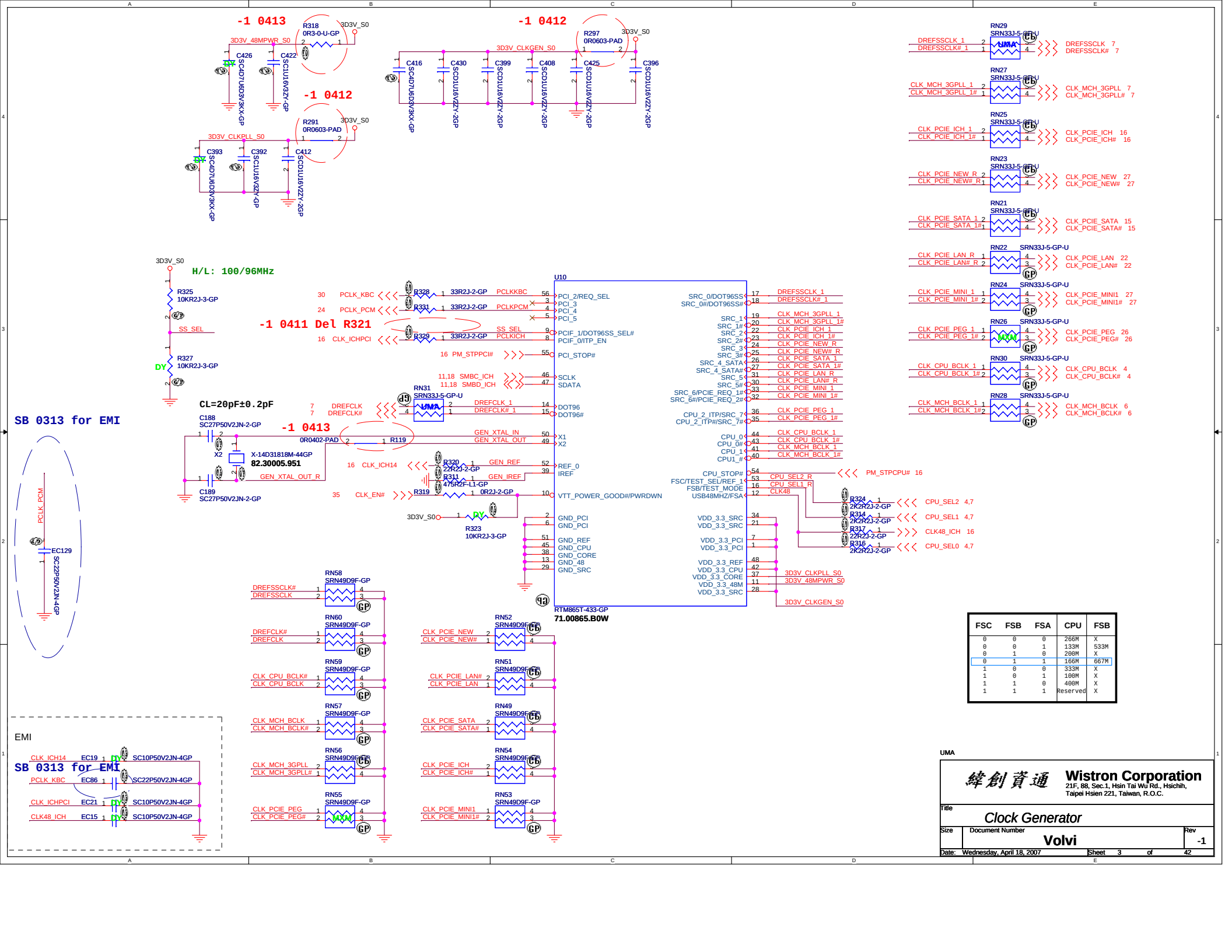
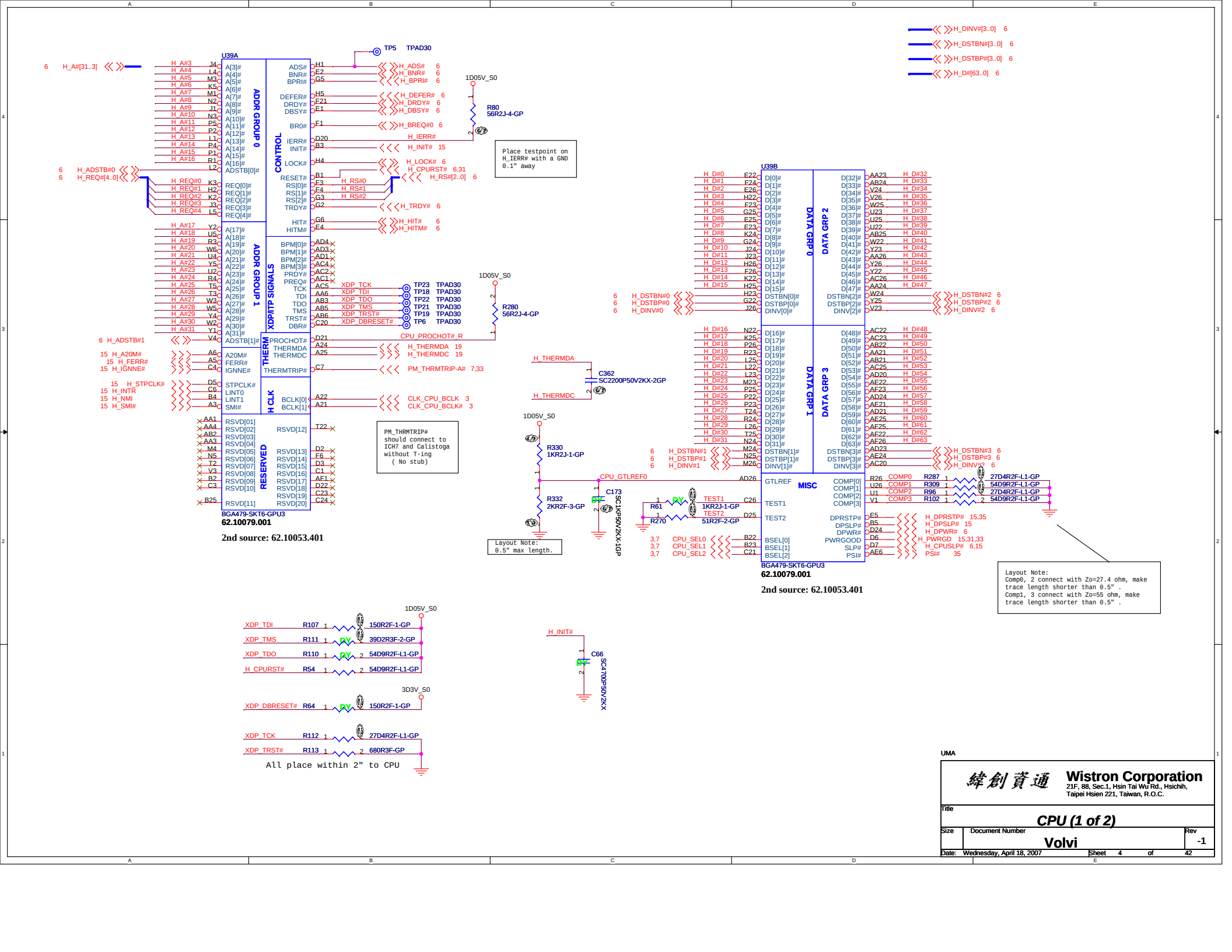


FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X


U39A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
BGA479-SKT6-GPU3
62.10079.001
2nd source: 62.10053.401
TP5 TPAD30
1D05V_S0
R80 56R2J-4-GP
Place testpoint on H_IERR# with a GND 0.1" away
R280 56R2J-4-GP
CPU_PROCHOT# R
PM_THRMTRIP# should connect to ICH7 and Calistoga without T-ing (No stub)
C362 SC2200P50V2KX-2GP
R330 1KR2J-1-GP
R332 2KR2F-3-GP
C173 SC1KP50V2KX-1GP
Layout Note: 0.5" max length.
U39B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
BGA479-SKT6-GPU3
62.10079.001
2nd source: 62.10053.401
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
3D3V_S0
All place within 2" to CPU
C66 SC470P50V2KX
UMA
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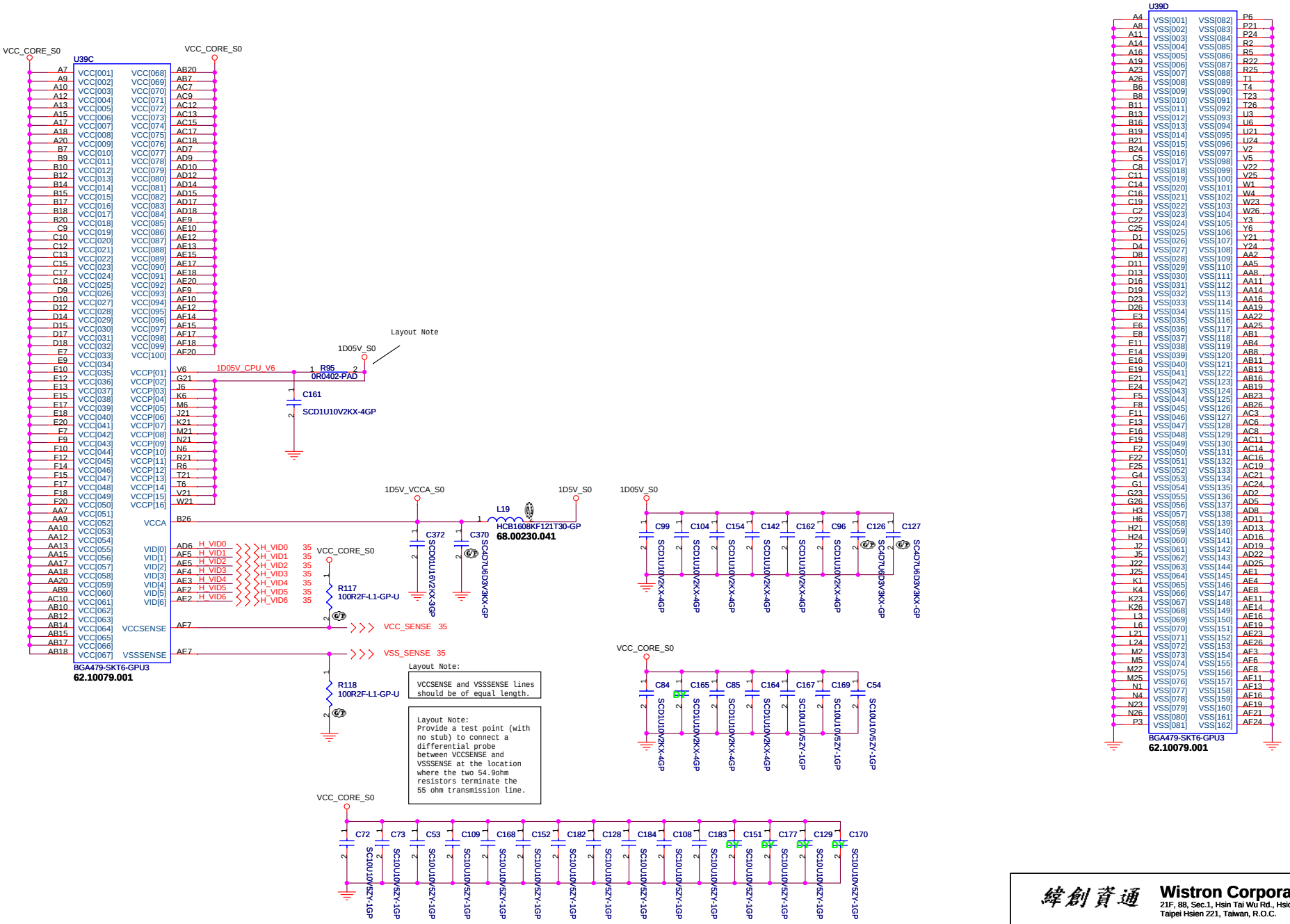
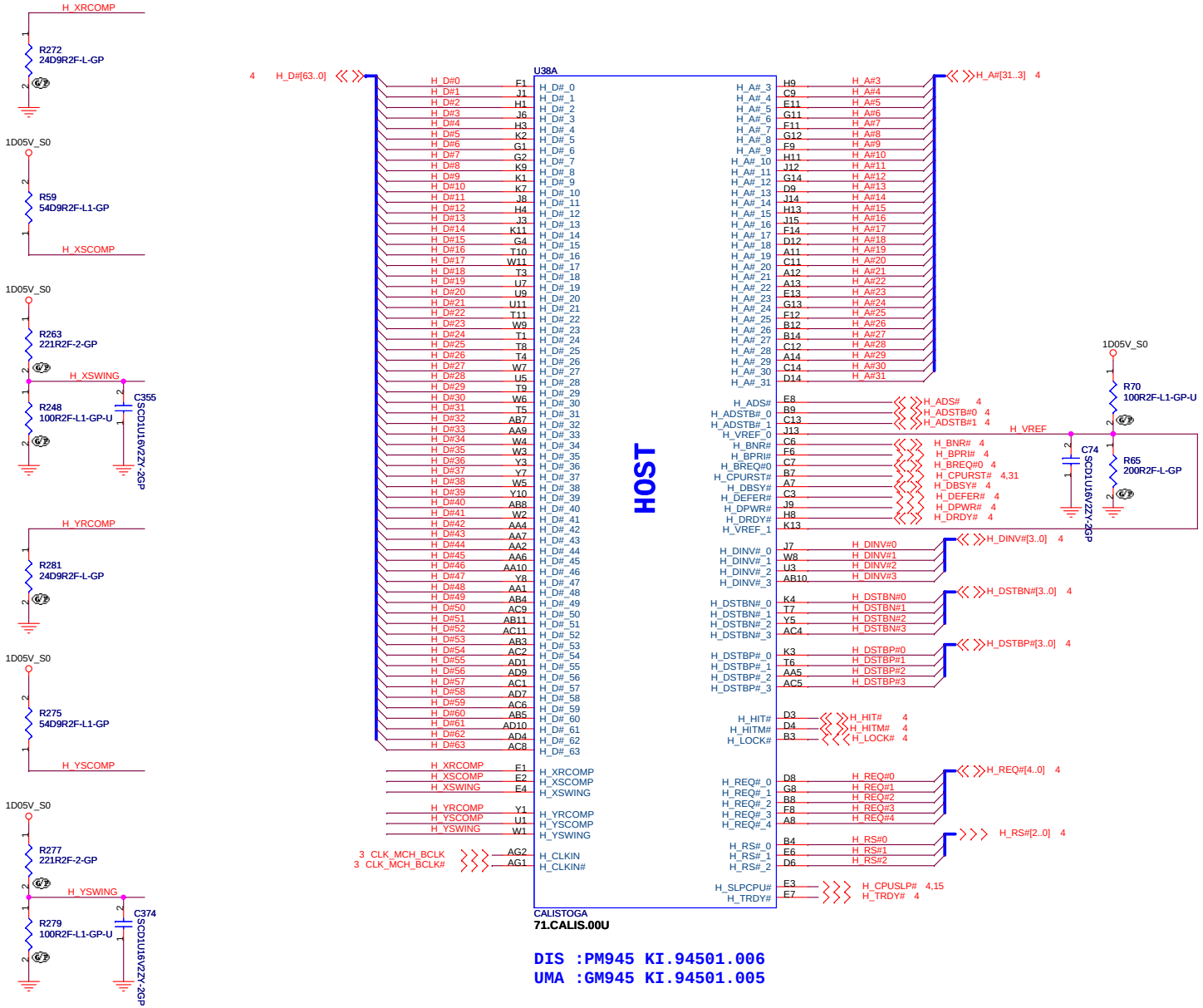
CPU (1 of 2)
Volvi
Rev -1
Date: Wednesday, April 18, 2007
Sheet 4 of 42



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***CPU (2 of 2)***		
Size	Document Number **Volvi**	Rev	-1
Date: Wednesday, April 18, 2007	Sheet 5 of 42		



Place them near to the chip (< 0.5")

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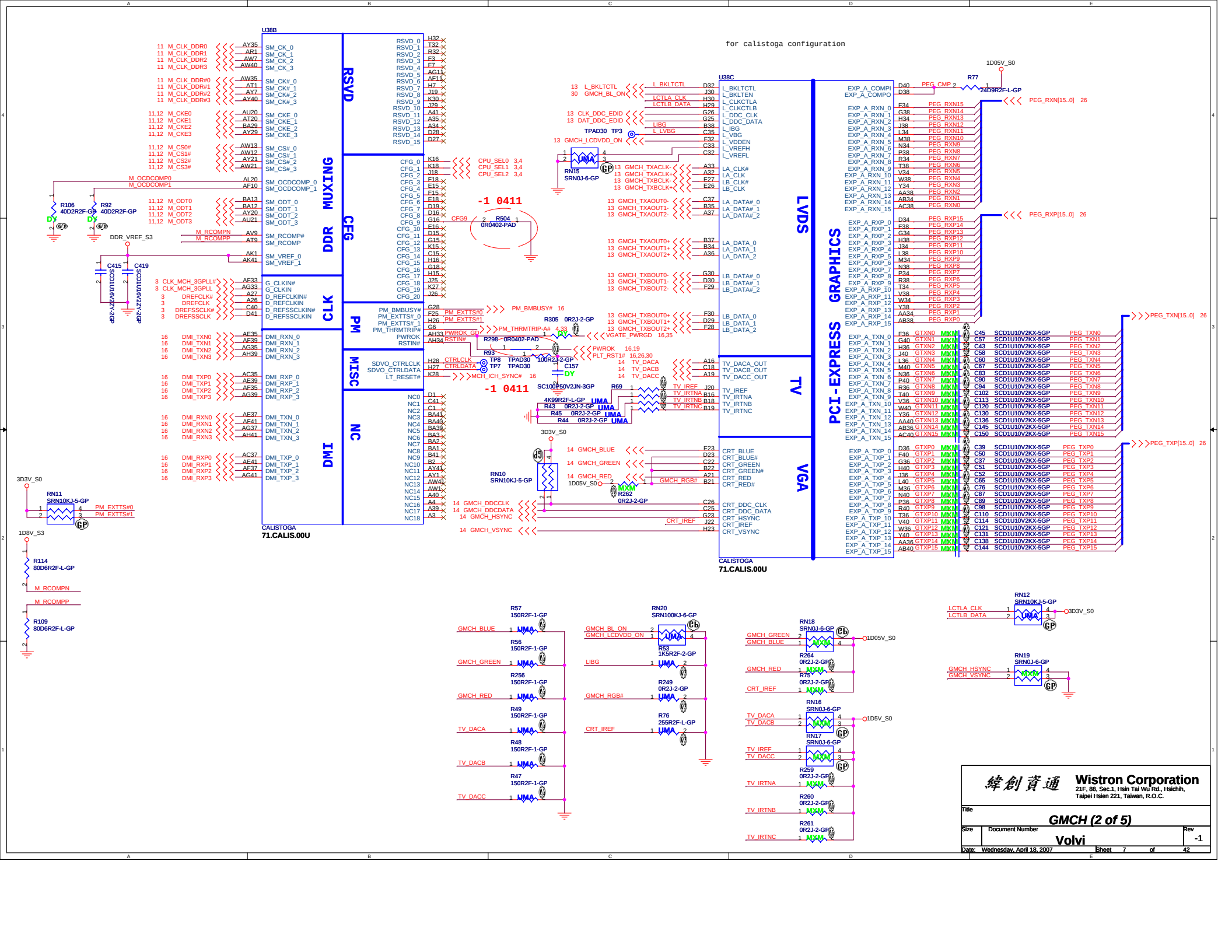
Title	***GMCH (1 of 5)***	
Size	Document Number **Volvi**	Rev -1
Date: Wednesday, April 18, 2007	Sheet 6 of 42	


for calistoga configuration
U38B
RSVD MUXING
DDR
CFG
CLK
PM
MISC
NC
DMI
CALISTOGA
71.CALIS.00U
U38C
LVDS
GRAPHICS
PCI-EXPRESS
TV
VGA
CALISTOGA
71.CALIS.00U
-1 0411
-1 0411
1D05V_S0
3D3V_S0
1D8V_S3
Wistron Corporation
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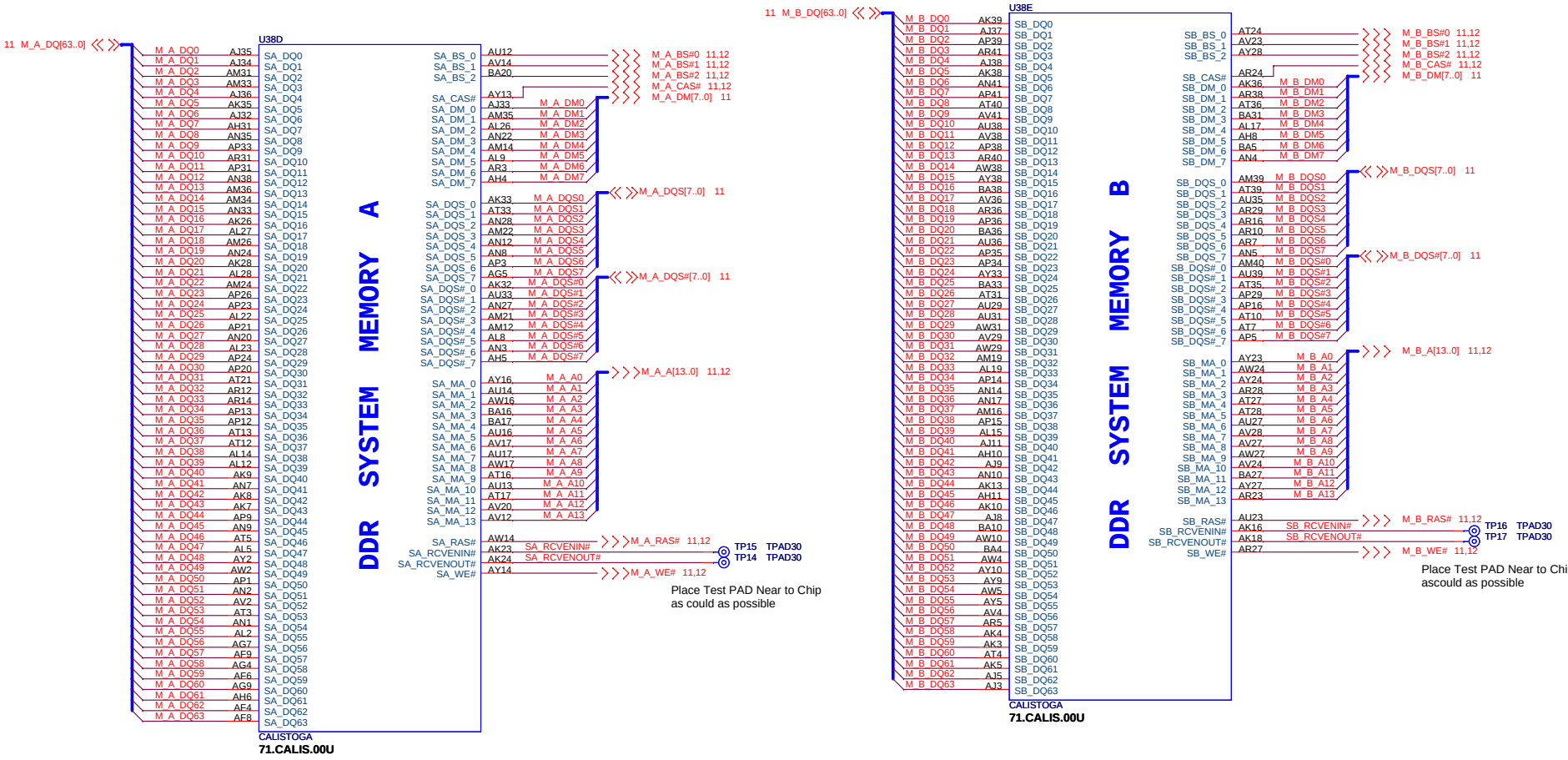
Title
GMCH (2 of 5)
Size
Document Number
Volvi
Rev
-1
Date: Wednesday, April 18, 2007
Sheet 7 of 42



緯創資通	**Wistron Corporation**	
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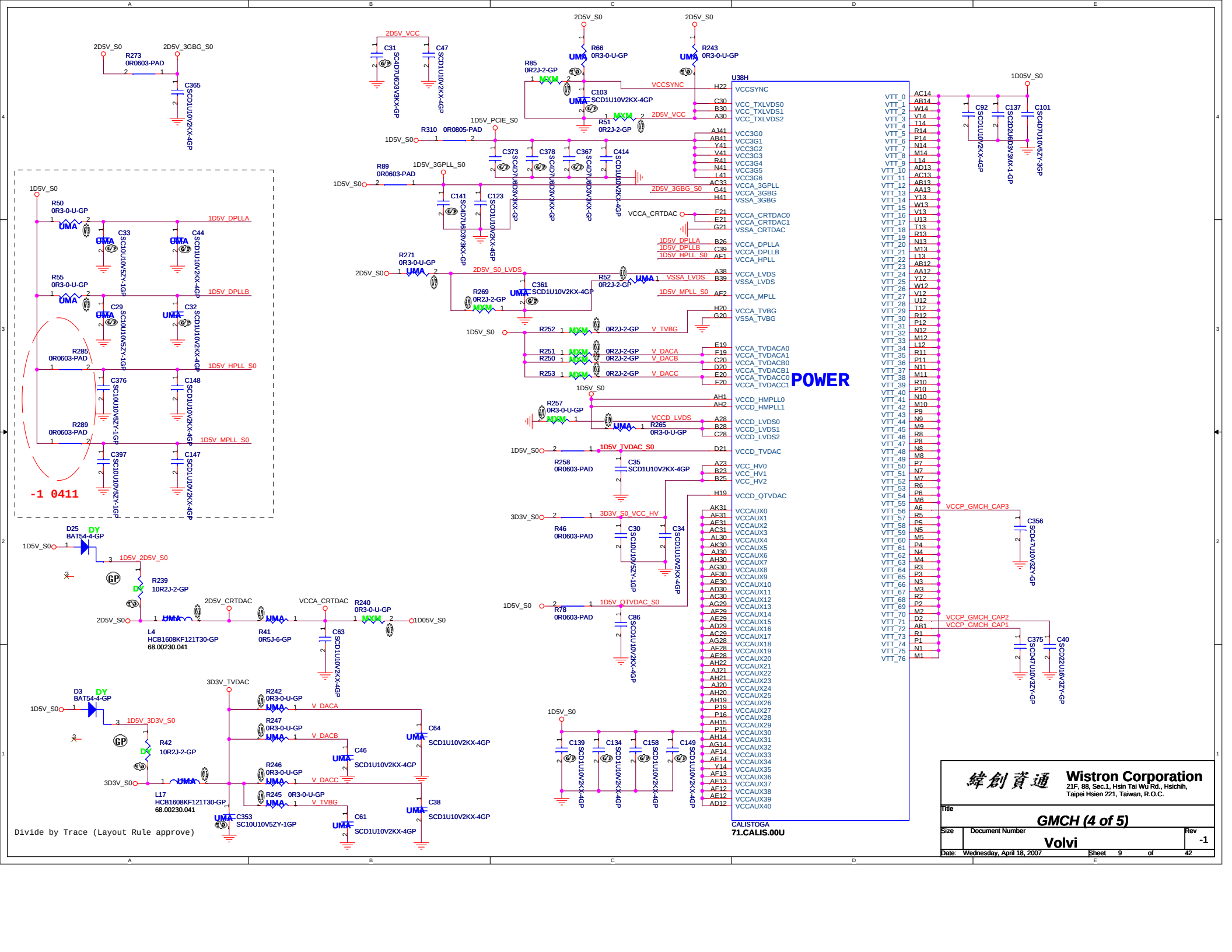
Title	***GMCH (3 of 5)***	
Size	Document Number: **Volvi**	Rev: -1
Date: Wednesday, April 18, 2007	Sheet 8 of 42	


POWER
U38H
CALISTOGA
71.CALIS.00U
-1 0411
Divide by Trace (Layout Rule approve)
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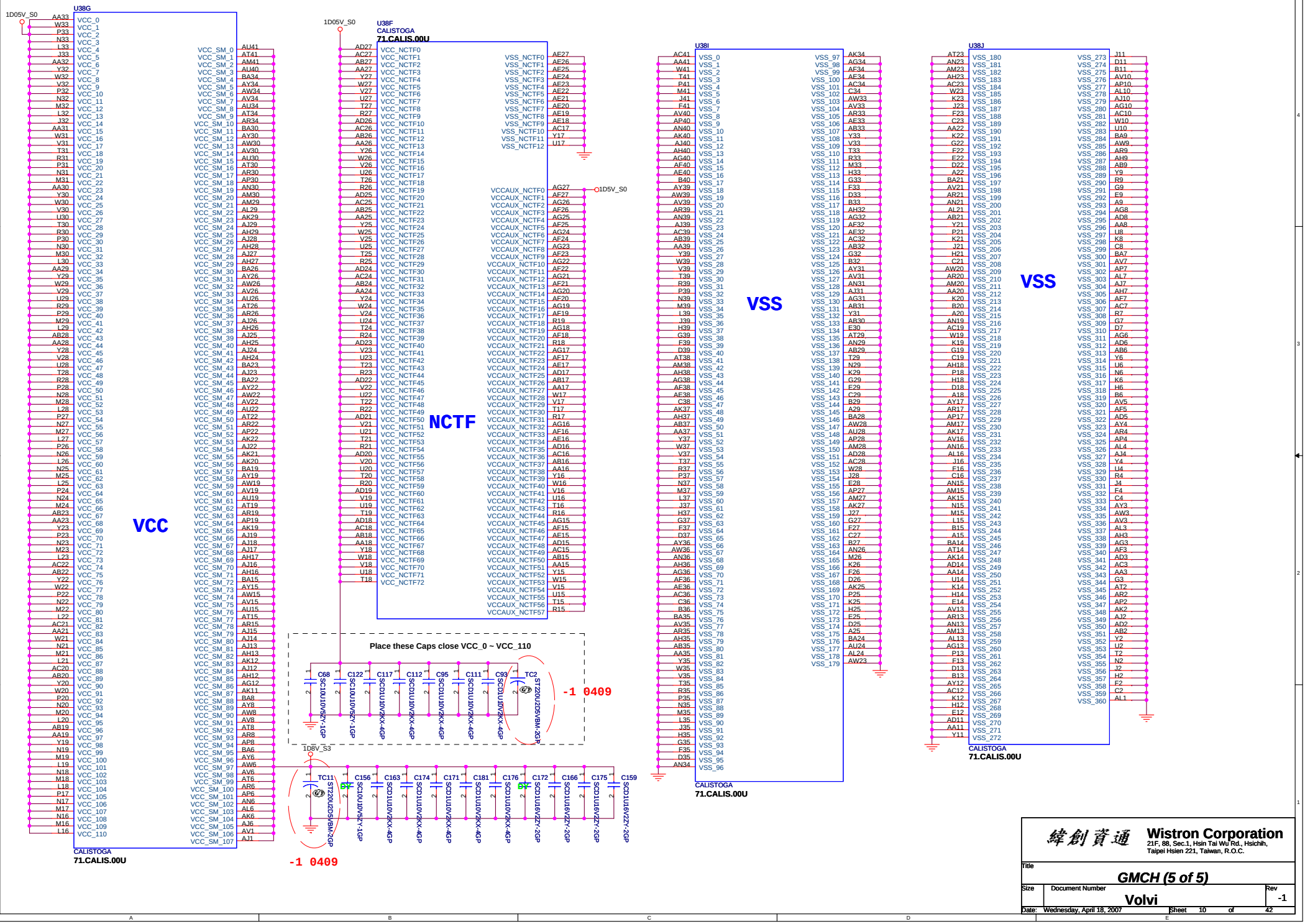
Title
GMCH (4 of 5)
Size
Document Number
Volvi
Rev
-1
Date: Wednesday, April 18, 2007
Sheet 9 of 42



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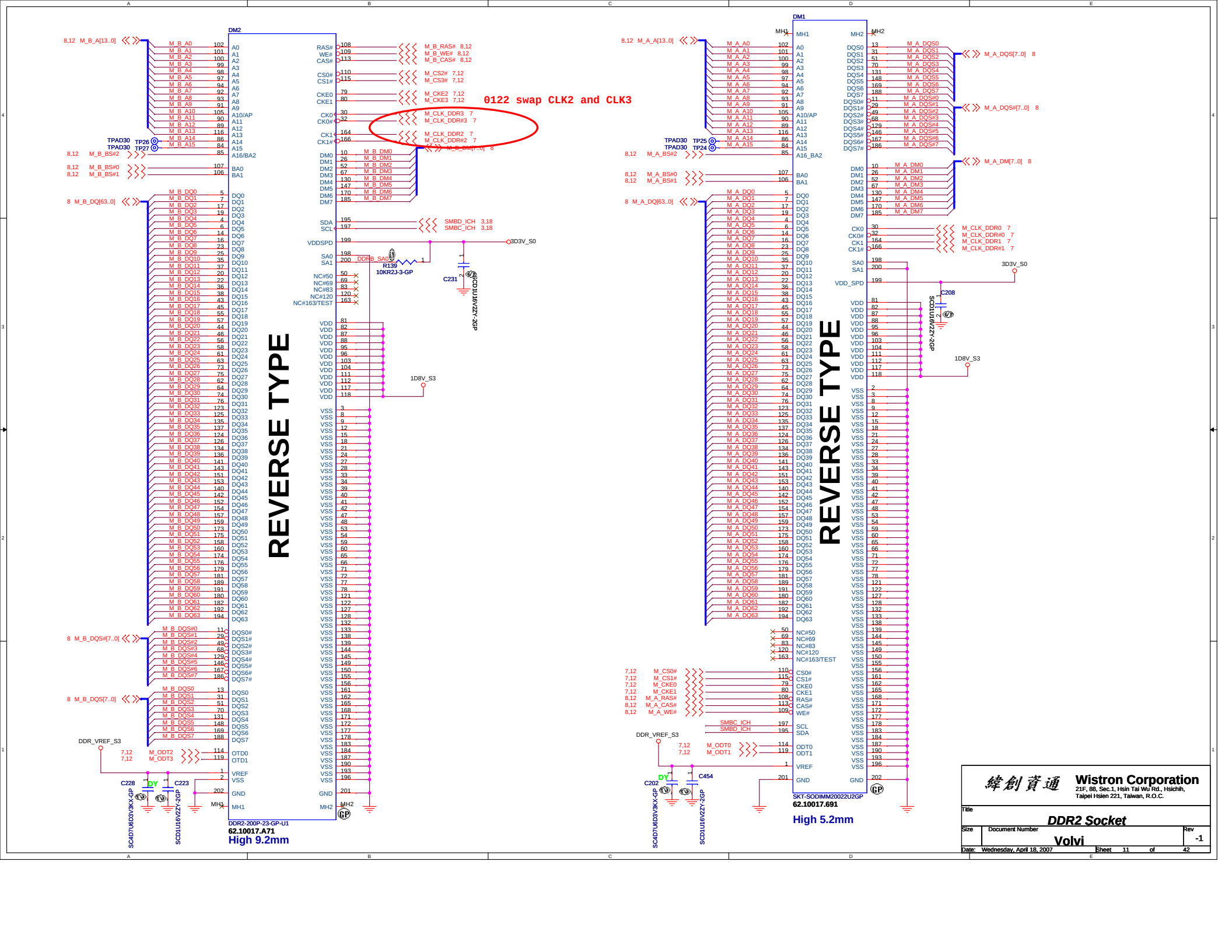
Title	GMCH (5 of 5)
Size	Document Number: Volvi
Rev	-1
Date:	Wednesday, April 18, 2007
Sheet	10 of 42



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR2 Socket	
Size	Document Number: Volvi
Rev: -1	
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PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN32 SRN56J-5-GP
- M_CKE0 7,11
- M_CKE1 7,11
- M_A_BS#2 8,11
- M_A_A12

RN40 SRN56J-5-GP
- M_B_A8
- M_B_A9
- M_B_A5

RN39 SRN56J-5-GP
- M_CKE2 7,11
- M_CKE3 7,11
- M_B_BS#2 8,11
- M_B_A12

RN41 SRN56J-5-GP
- M_B_A3
- M_B_A1
- M_B_A10
- M_B_WE# 8,11

RN45 SRN56J-5-GP
- M_B_A13
- M_ODT2 7,11
- M_ODT3 7,11
- M_B_RAS# 8,11

RN44 SRN56J-5-GP
- M_B_BS#1 8,11
- M_B_A2
- M_B_A0
- M_B_A4

RN43 SRN56J-5-GP
- M_B_A6
- M_B_A7
- M_B_A11

RN42 SRN56J-5-GP
- M_B_BS#0 8,11
- M_B_CAS# 8,11
- M_CS3# 7,11
- M_CS2# 7,11

RN38 SRN56J-5-GP
- M_A_A13
- M_ODT0 7,11
- M_CS0# 7,11
- M_A_RAS# 8,11

RN37 SRN56J-5-GP
- M_A_BS#1 8,11
- M_A_A0
- M_A_A2
- M_A_A4

RN35 SRN56J-5-GP
- M_A_CAS# 8,11
- M_CS1# 7,11
- M_ODT1 7,11

RN33 SRN56J-5-GP
- M_A_A9
- M_A_A8
- M_A_A5
- M_A_A3

RN36 SRN56J-5-GP
- M_A_A6
- M_A_A7
- M_A_A11

RN34 SRN56J-5-GP
- M_A_A1
- M_A_A10
- M_A_BS#0 8,11
- M_A_WE# 8,11

M_A_A[13..0] — M_A_A[13..0] 8,11

M_B_A[13..0] — M_B_A[13..0] 8,11

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C198 C240 C229 C206 C216 C221 C219 C207 C235 C218 C230 — SCD1U16V2ZY-2GP (DY)

C452 C217 C242 C210 C234 C211 C220 C199 C243 C241 C453 — SCD1U16V2ZY-2GP (DY)

Place these Caps near DM1

1D8V_S3

C447 C213 C448 C214 C446 — SC20U6D3V3MX-1GP

C197 C205 C209 C212 — SCD1U16V2ZY-2GP (DY)

Place these Caps near DM2

1D8V_S3

C226 C245 C227 C236 C246 — SC20U6D3V3MX-1GP

C238 C224 C239 C222 — SCD1U16V2ZY-2GP (DY)

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Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
	Volvi	-1

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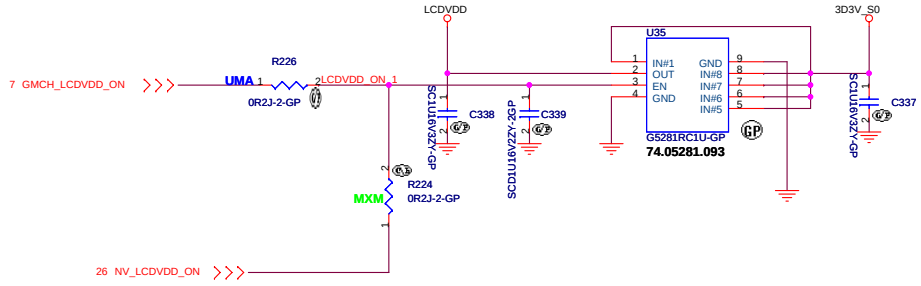
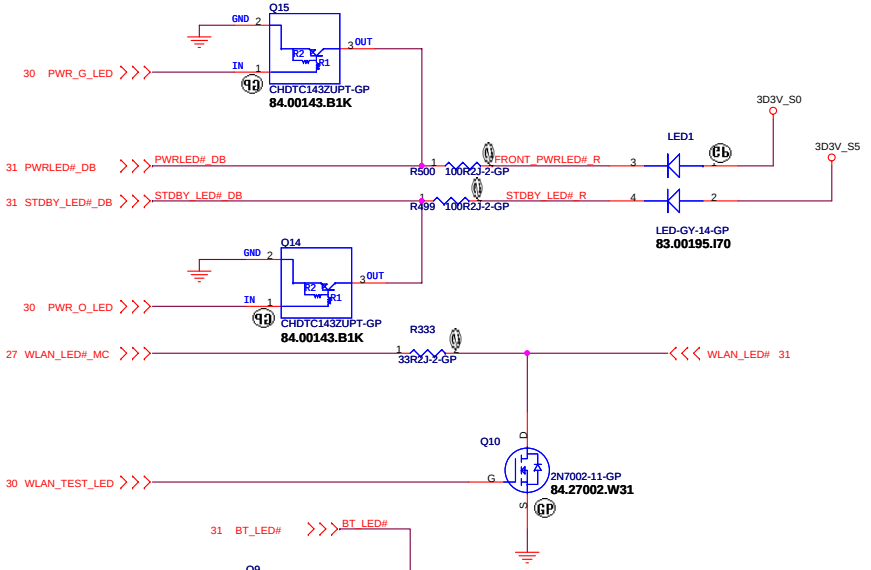
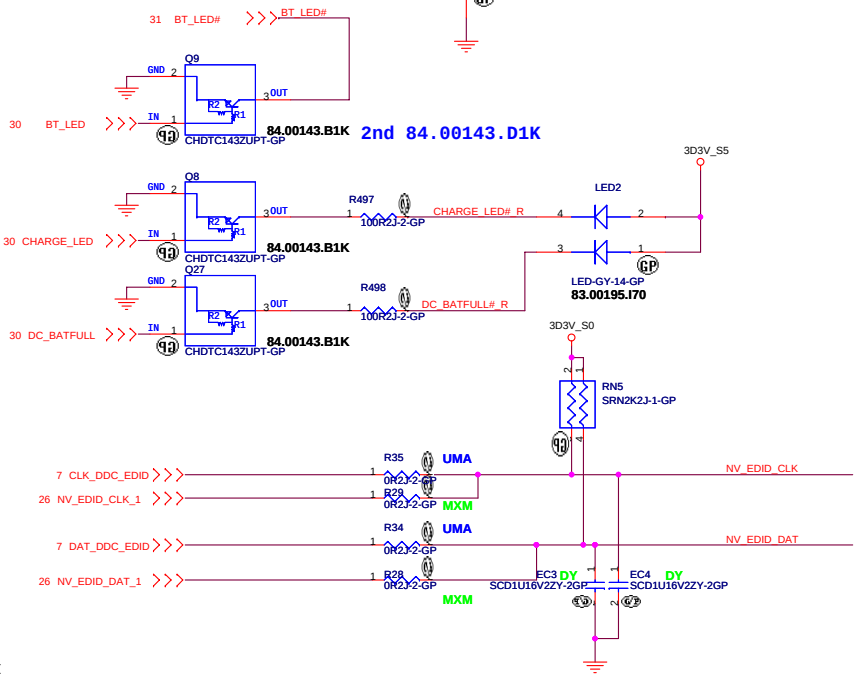
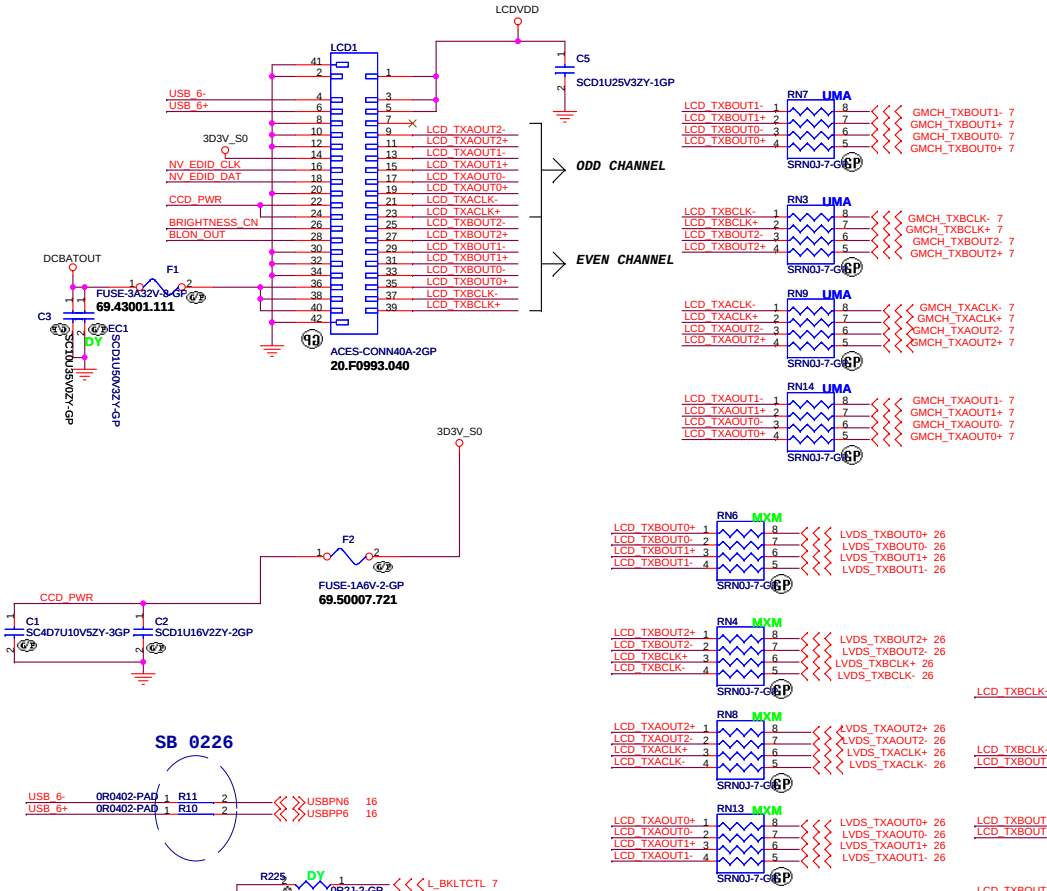
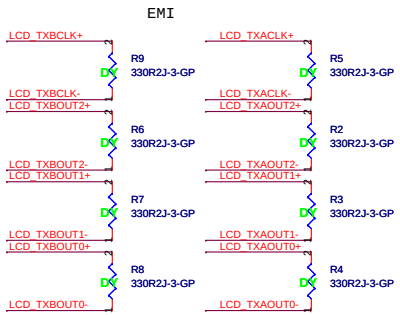
LCD/INVERTER CONN











UMA

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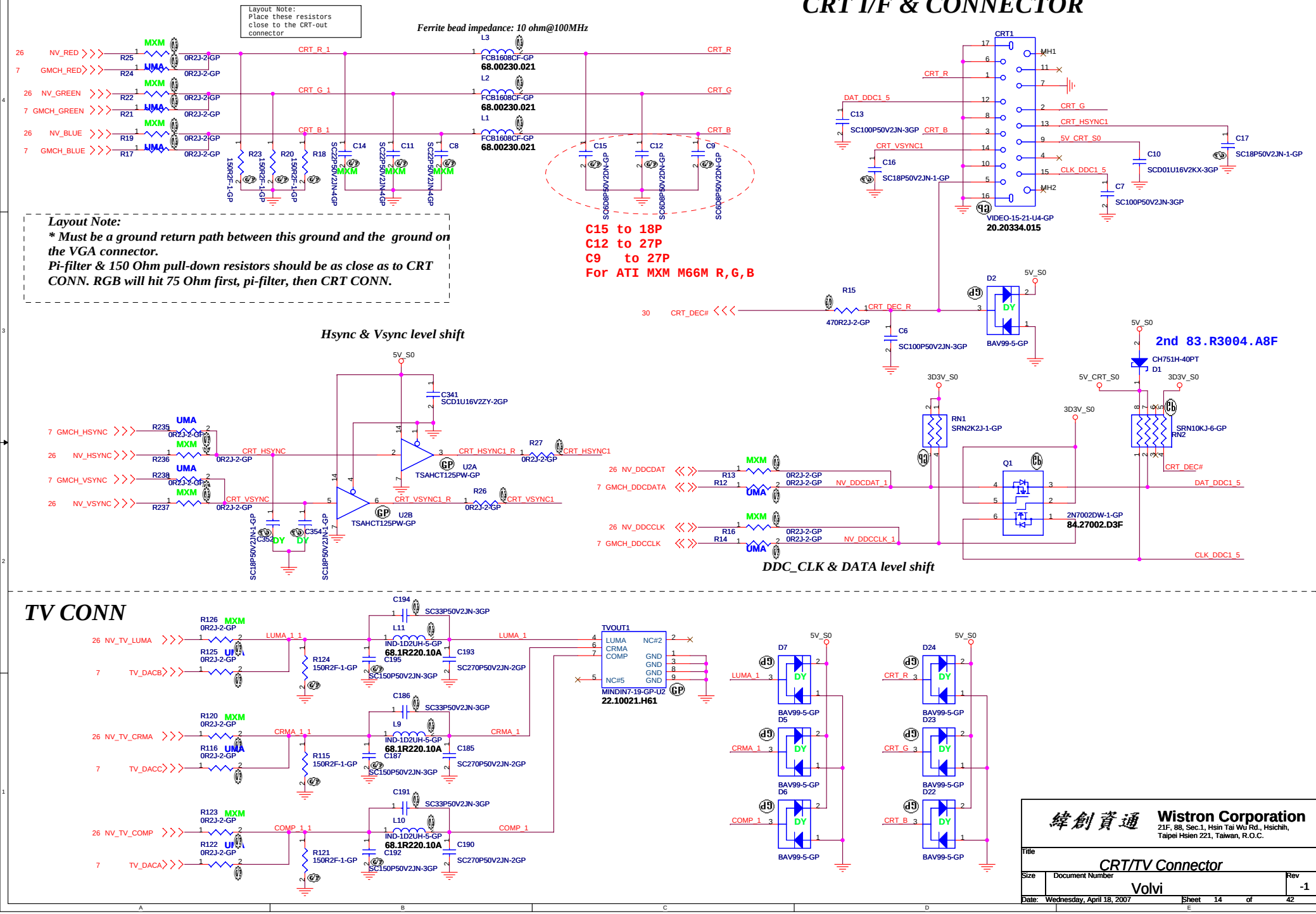
Title	*LCD CONN & LED*	
Size	Document Number: Volvi	Rev: -1
Date: Wednesday, April 18, 2007	Sheet 13 of 42	

CRT I/F & CONNECTOR



TV CONN

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Title: CRT/TV Connector

Size | Document Number: Volvi | Rev: -1

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SB 0305

RTC circuitry

SB 0313 for EMI

0130

-1 0411

Change to KI.80101.017

Open R for Dothan A step
Shunt for Dothan B step
& all Yonah

Layout Note: R568 needs to placed within 2" of ICH7, R568 must be placed within 2" of R169 w/o stub.

Place within 500 mils of ICH7ball

P.H. for internal VCCSUS1_05

	INTVRMEN
Enable	1
Disable	0

Placement Note:
Diatance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

ICH7-M-GP
71.ICH7M.00U

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Title: ICH7-M (1 of 4)

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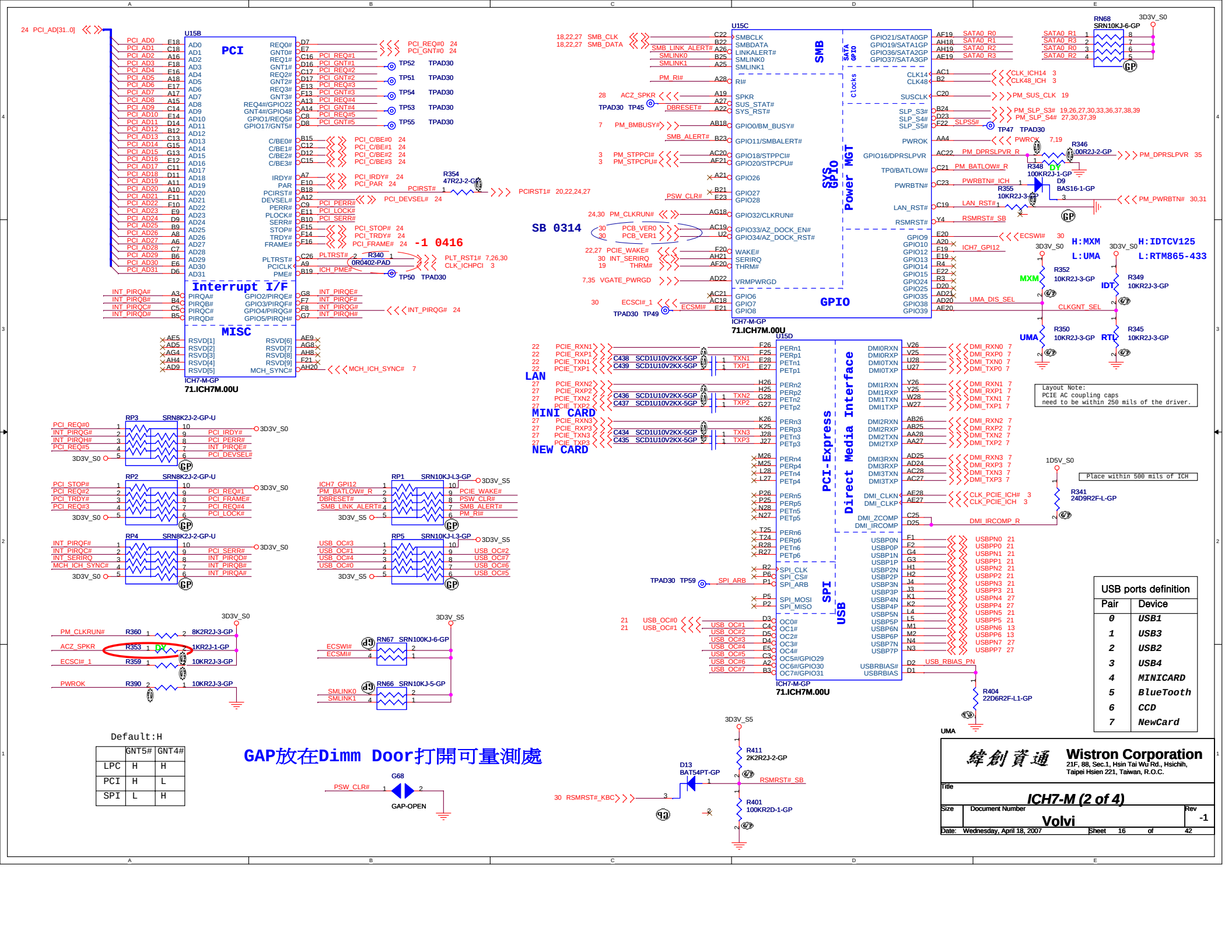
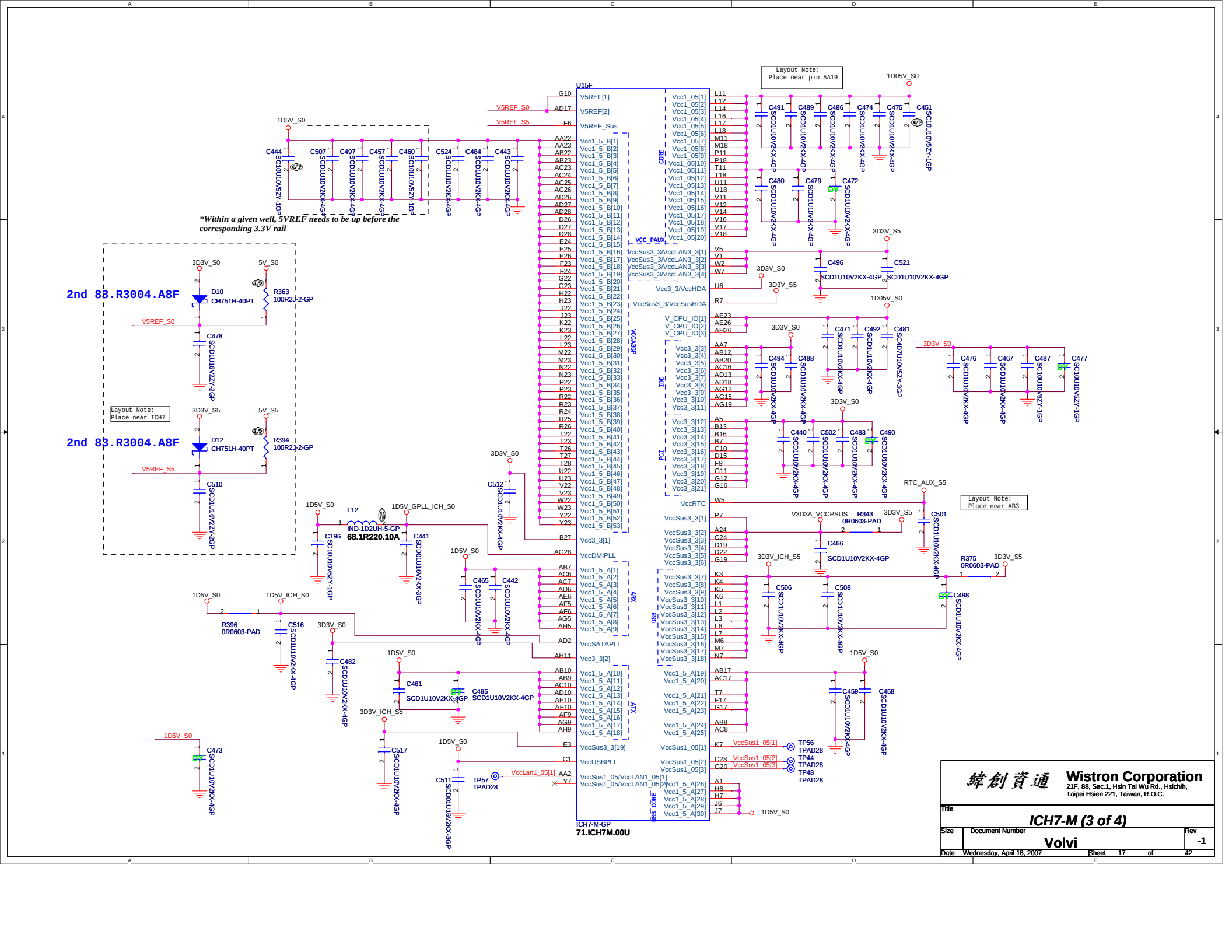

U15B
PCI
Interrupt I/F
MISC
ICH7-M-GP
71.ICH7M.00U
U15C
SMB
GPIO
Power MGT
SYS
SB 0314
-1 0416
LAN
MINI CARD
NEW CARD
U15D
PCI-Express
Direct Media Interface
SPI
USB
H:MXM
L:UMA
H:IDTCV125
L:RTM865-433
MXM
IDT
UMA
RTL
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
USB ports definition
Pair | Device
0 USB1
1 USB3
2 USB2
3 USB4
4 MINICARD
5 BlueTooth
6 CCD
7 NewCard
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
GAP放在Dimm Door打開可量測處
GAP-OPEN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size
Document Number
Volvi
Rev
-1
Date: Wednesday, April 18, 2007
Sheet 16 of 42


U15F
ICH7-M-GP
71.ICH7M.00U
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
2nd 83.R3004.A8F
2nd 83.R3004.A8F
Layout Note: Place near ICH7
Layout Note: Place near pin AA19
Layout Note: Place near AB3
D10 CH751H-40PT
D12 CH751H-40PT
R363 100R2J-2-GP
R394 100R2J-2-GP
L12 IND-1D2UH-5-GP 68.1R220.10A
R396 0R0603-PAD
R343 0R0603-PAD
R375 0R0603-PAD
TP56 TPAD28
TP44 TPAD28
TP48 TPAD28
TP57 TPAD28
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size
Document Number
Volvi
Rev
-1
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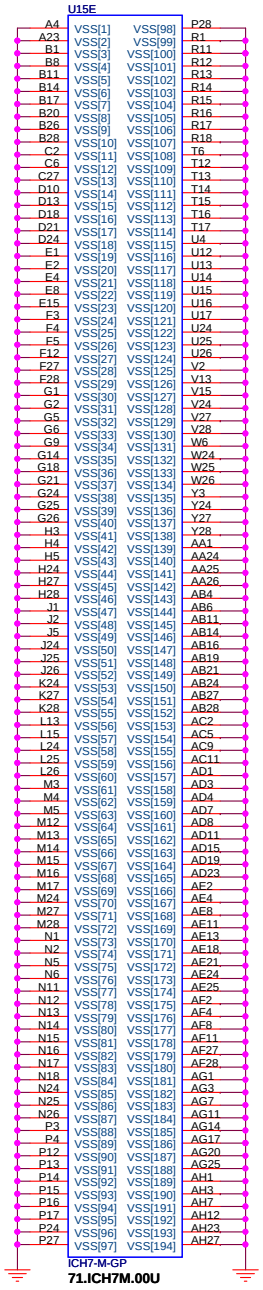

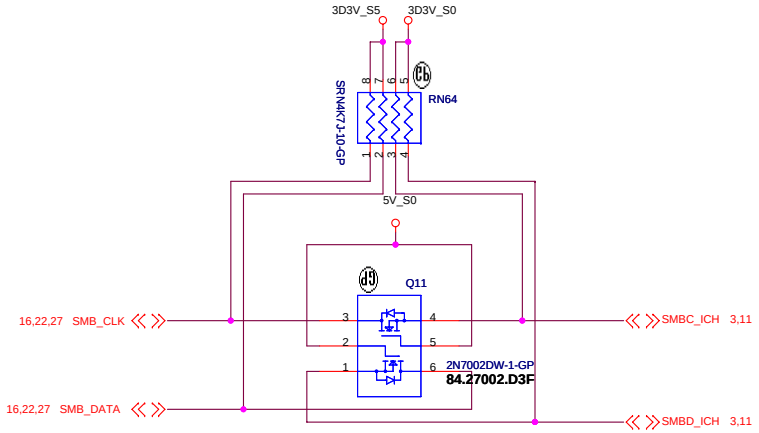

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ICH7-M (4 of 4)*		
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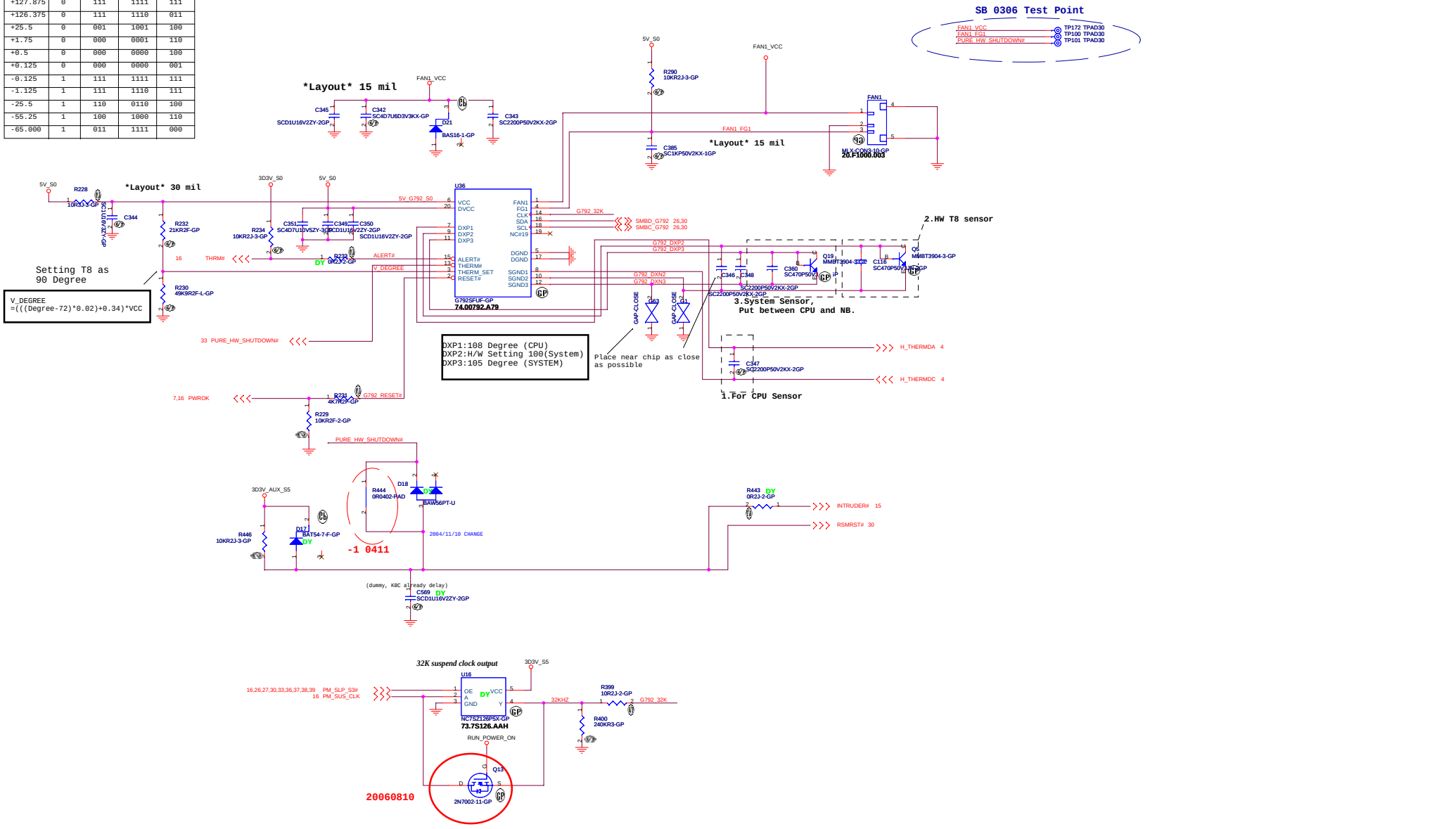
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



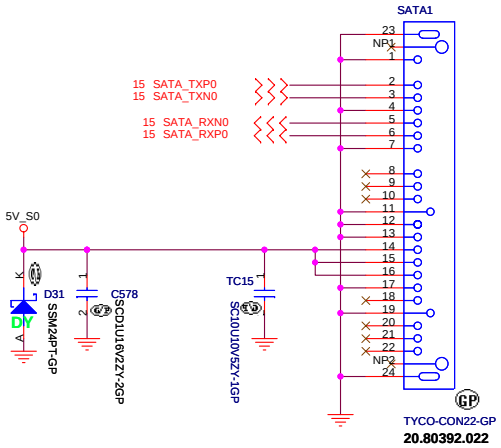
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

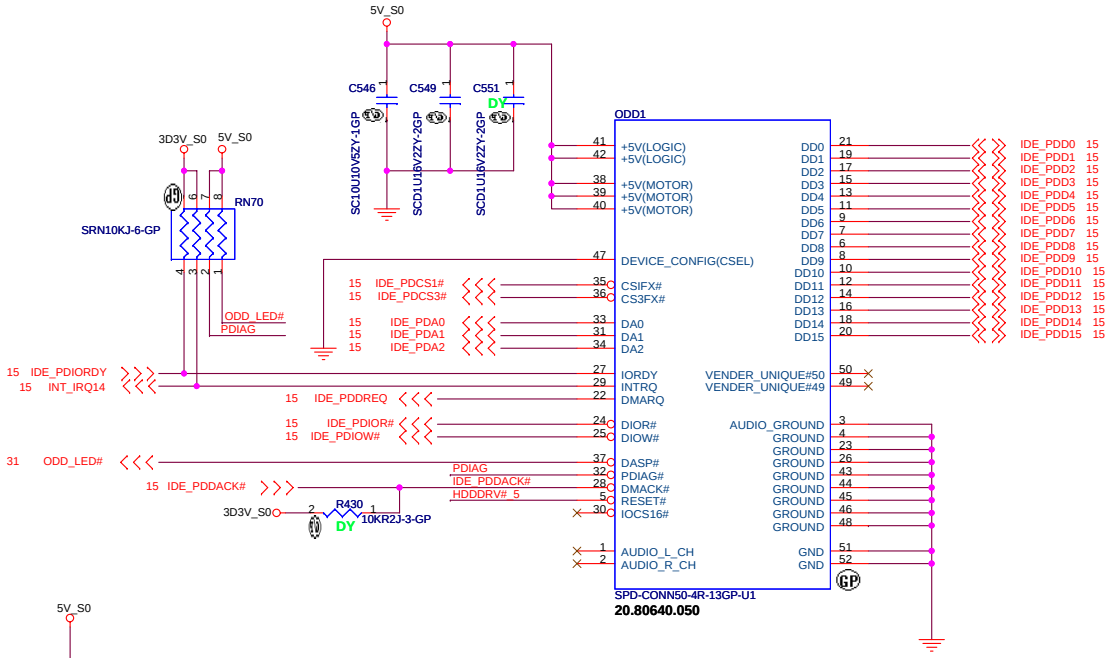
Size | Document Number: Volvi | Rev: -1

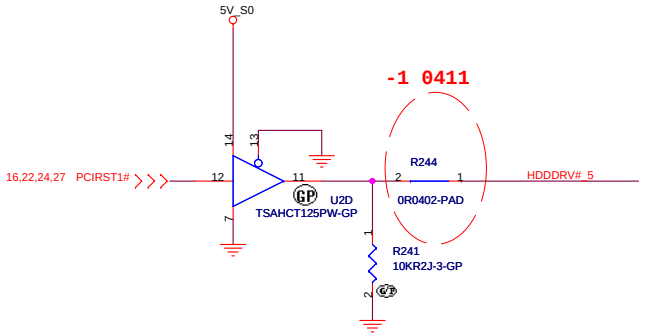
Date: Wednesday, April 18, 2007 | Sheet 19 of 42

SATA HD Connector



ODD Connector





UMA

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Title: HDD and CDROM		
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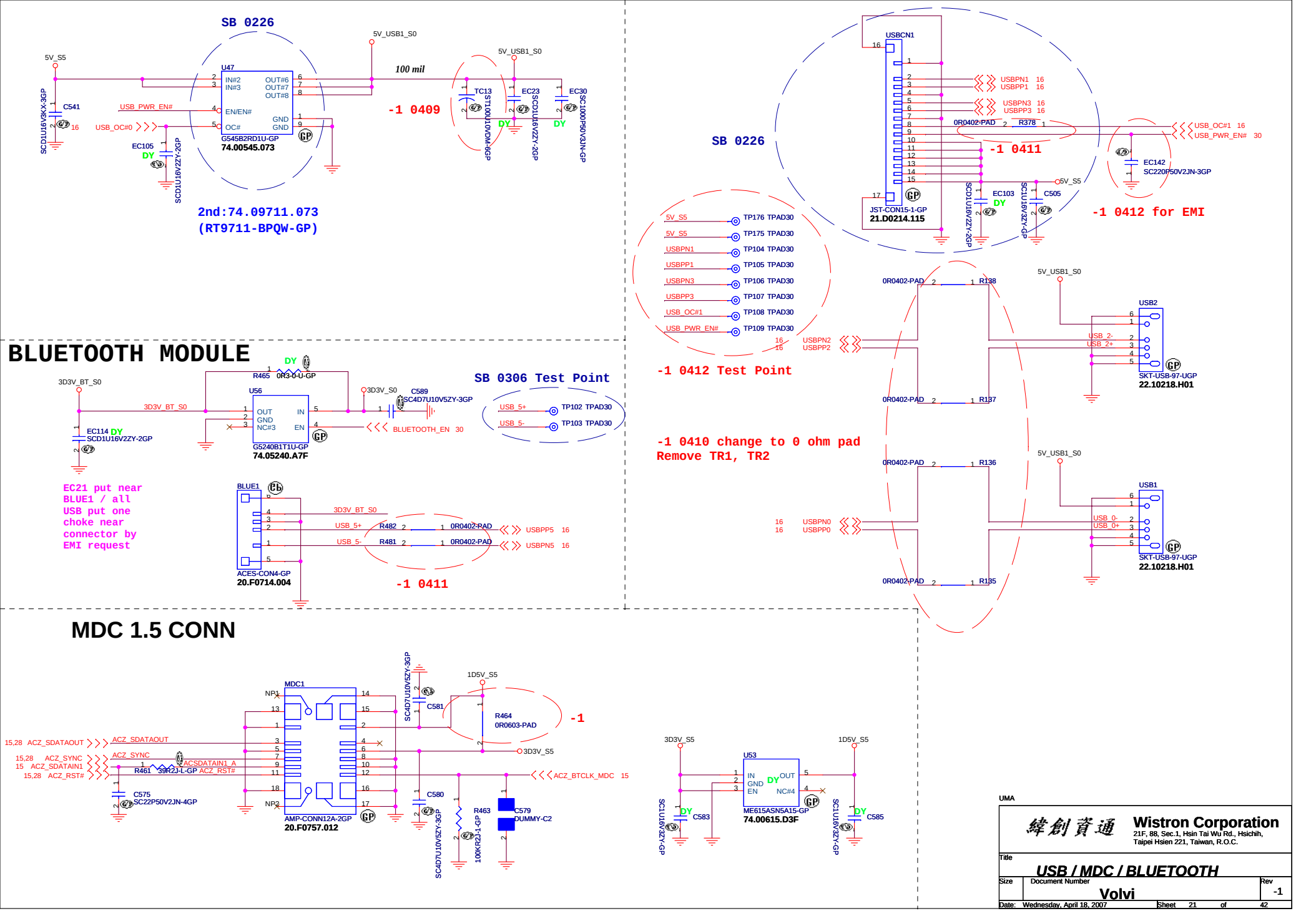
SB 0226
5V_S5
5V_USB1_S0
100 mil
-1 0409
C541
SCD1U16V3KX-3GP
USB_PWR_EN#
USB_OC#0
U47
IN#2
IN#3
EN/EN#
OC#
OUT#6
OUT#7
OUT#8
GND
G545B2RD1U-GP
74.00545.073
EC105
DY
SCD1U16V2ZY-2GP
TC13
EC23
EC30
SC1000P50V2KN-GP
2nd:74.09711.073
(RT9711-BPQW-GP)
USBCN1
USBPN1
USBPP1
USBPN3
USBPP3
0R0402-PAD
R378
USB_OC#1
USB_PWR_EN#
-1 0411
JST-CON15-1-GP
21.D0214.115
EC103
C505
SC220P50V2JN-3GP
-1 0412 for EMI
TP176 TPAD30
TP175 TPAD30
TP104 TPAD30
TP105 TPAD30
TP106 TPAD30
TP107 TPAD30
TP108 TPAD30
TP109 TPAD30
-1 0412 Test Point
BLUETOOTH MODULE
3D3V_BT_S0
R465 0R3-0-U-GP
U56
OUT
GND
NC#3
IN
EN
BLUETOOTH_EN
G5240B1T1U-GP
74.05240.A7F
C589
SC4D7U10V5ZY-3GP
EC114 DY
SCD1U16V2ZY-2GP
SB 0306 Test Point
USB_5+
USB_5-
TP102 TPAD30
TP103 TPAD30
EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request
BLUE1
ACES-CON4-GP
20.F0714.004
R482
R481
0R0402-PAD
USBPP5
USBPN5
-1 0411
-1 0410 change to 0 ohm pad
Remove TR1, TR2
R138
R137
R136
R135
USB2
USB1
SKT-USB-97-UGP
22.10218.H01
USBPN2
USBPP2
USBPN0
USBPP0
MDC 1.5 CONN
MDC1
AMP-CONN12A-2GP
20.F0757.012
ACZ_SDATAOUT
ACZ_SYNC
ACZ_RST#
ACSDATAIN1_A
R461 39R2J-L-GP
C575
SC22P50V2JN-4GP
C581
R464
0R0603-PAD
-1
1D5V_S5
3D3V_S5
ACZ_BTCLK_MDC
C580
R463
100KR2J-1-GP
C579
DUMMY-C2
SC4D7U10V5ZY-3GP
U53
ME615ASN5A15-GP
74.00615.D3F
C583
C585
SC1U16V3ZY-GP
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB / MDC / BLUETOOTH
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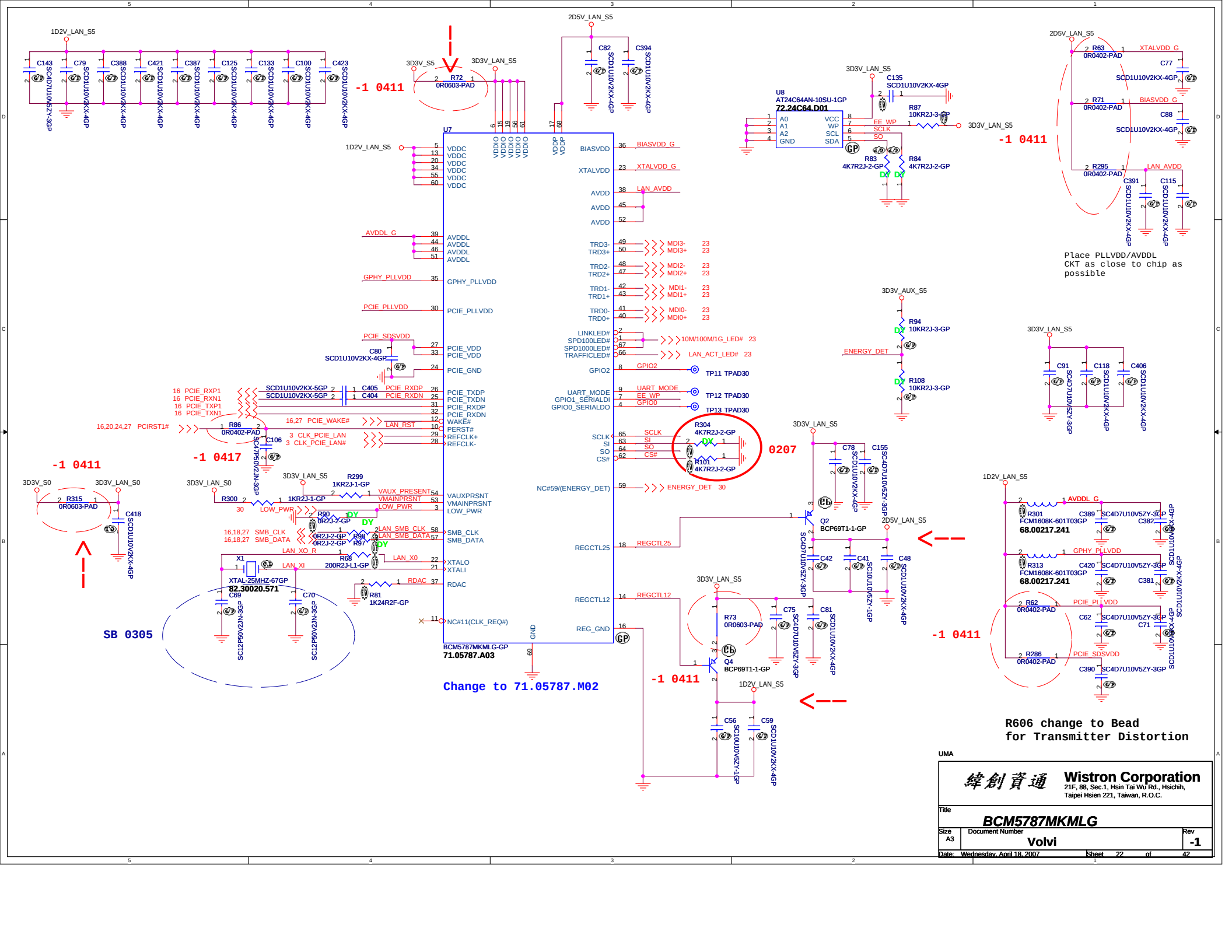
1D2V_LAN_S5
2D5V_LAN_S5
3D3V_S5
3D3V_LAN_S5
3D3V_S0
3D3V_LAN_S0
3D3V_AUX_S5
U7
BCM5787MKMLG-GP
71.05787.A03
U8
AT24C64AN-10SU-1GP
72.24C64.D01
-1 0411
-1 0417
0207
SB 0305
Change to 71.05787.M02
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R606 change to Bead
for Transmitter Distortion
UMA
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Title
BCM5787MKMLG
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LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

-1 0331 Test Point

TIP_C
RING_C
TP174 TPAD30
TP173 TPAD30

RJ1
RJ45-107-GP-U
22.10245.J01

22 LAN_ACT_LED#
22 10M/100M/1G_LED#
CONN_PWR_2
CONN_PWR_1
TIP
RING

A3:Green
B2:YELLOW

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

TRING1
ACES-CON2-GP-U
20.F0714.002

L5 HFB1608VF-102-GP
L6 HFB1608VF-102-GP

-1 0416

GIGA Lan Transformer

-1 0413

2D5V_LAN_S5
R67 0R0402-PAD
-1 0411

C97 SCD1U16V2ZY-2GP
C384 SCD1U16V2ZY-2GP
C400 SCD1U16V2ZY-2GP
C407 SCD1U16V2ZY-2GP

XRF_TDC

XF1
XFORM-271-GP
68.HD081.301

XF2
XFORM-271-GP
68.HD081.301

MDI1+
MDI1-
MDI0+
MDI0-
MDI3+
MDI3-
MDI2+
MDI2-

RJ45_3
MCT2
RJ45_6
RJ45_1
MCT1
RJ45_2
RJ45_7
MCT4
RJ45_8
RJ45_4
MCT3
RJ45_5

For EMI

L7
SRN0J-5-GP

L8
SRN0J-5-GP

Tahoe

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

MCT1
MCT2
MCT4
MCT3
RN50
SRN75J-1-GP
LAN_TERMINAL
C395
SC1KP2KV8KX-GP

3D3V_LAN_S5
R278 470R2J-2-GP
R296 470R2J-2-GP
CONN_PWR_1
CONN_PWR_2

ERC2
SRC100P50V-2-GP
77.61012.02L

CLOSE TO TRANSFORMER

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3
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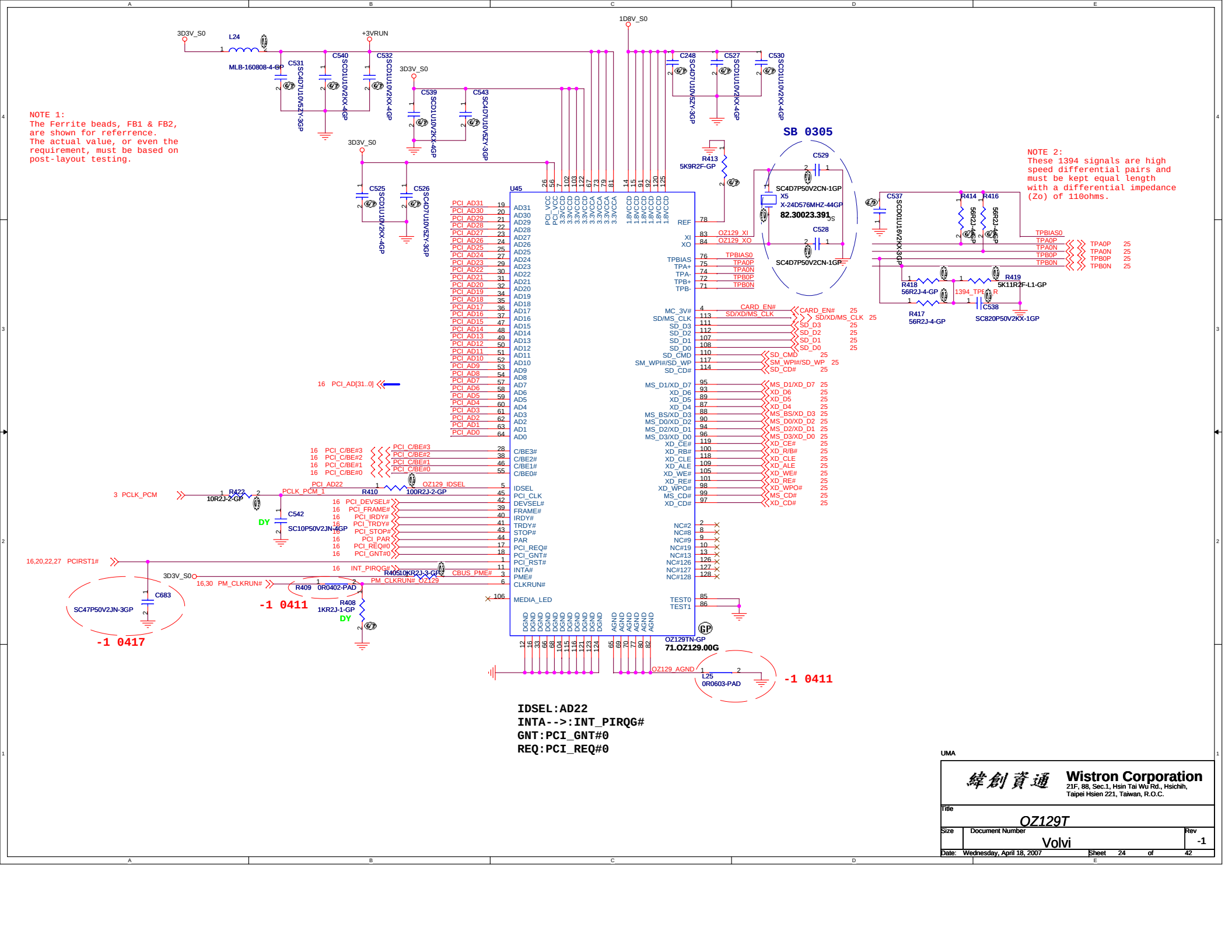
NOTE 1:
The Ferrite beads, FB1 & FB2, are shown for referrence. The actual value, or even the requirement, must be based on post-layout testing.
NOTE 2:
These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.
SB 0305
U45
OZ129TN-GP
71.OZ129.00G
-1 0411
-1 0417
IDSEL:AD22
INTA-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
UMA
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OZ129T
Volvi
-1
Wednesday, April 18, 2007
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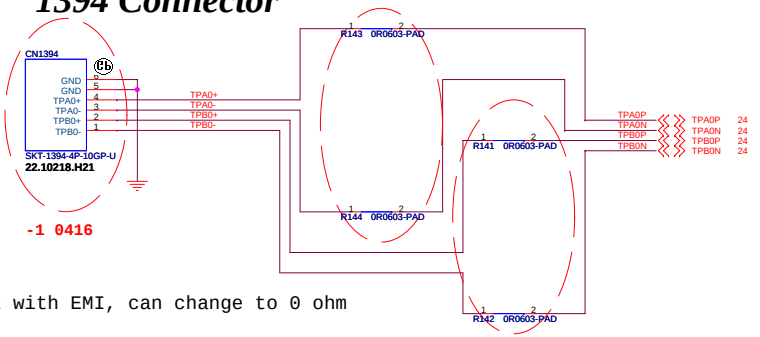
1394 Connector

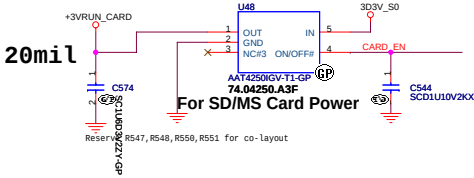
-1 0411 del L22 and L23



-1 0416

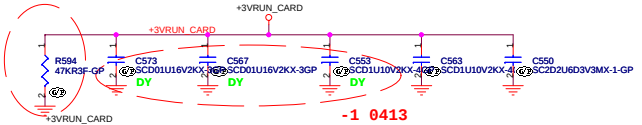
check with EMI, can change to 0 ohm

20mil

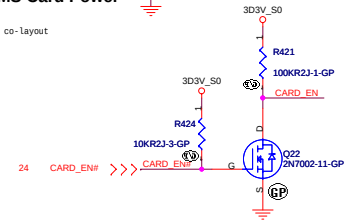


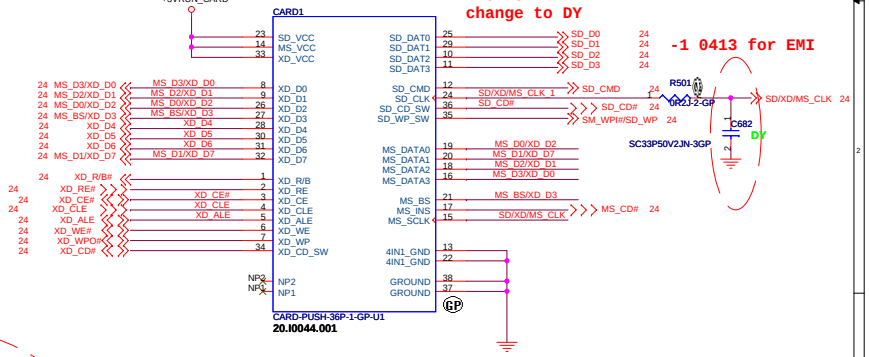
For SD/MS Card Power

-1 0413
+3VRUN_CARD discharging



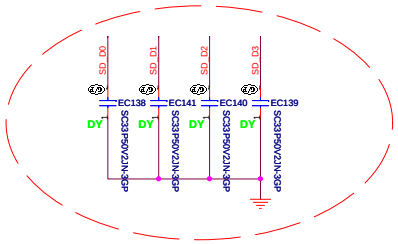
-1 0413
change to DY





-1 0413 for EMI

-1 0413 for EMI



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1394 / CARD READER*

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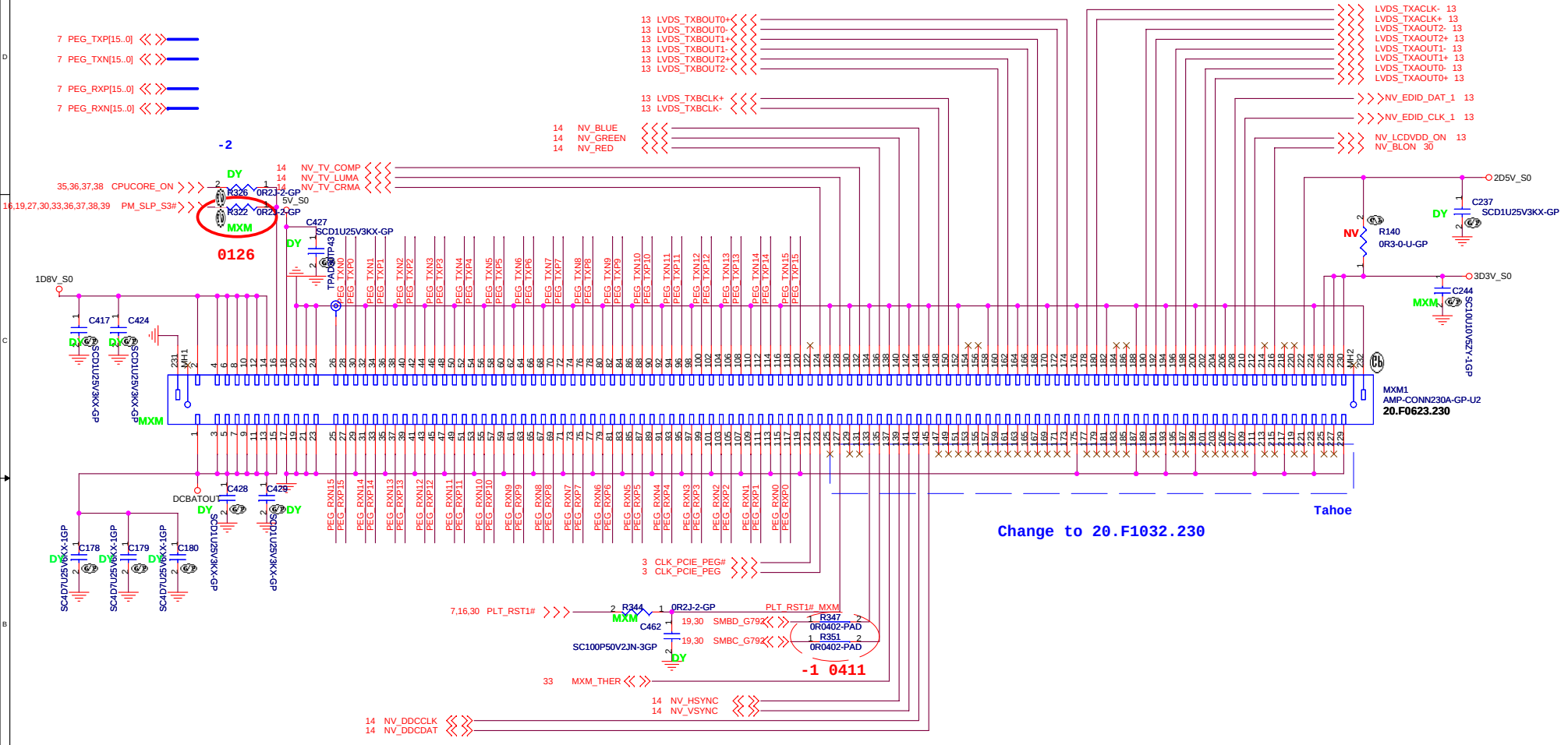
NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector



UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Graphic MXM CONN	
Size A3	Document Number Volvi	Rev -1
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Mini Card Connector

NEWCARD Connector

SB 0226

SK1
CARDBUS-SKT95-GP
21.H0153.001

Reserve the symbol for bottom side connector

NEW1
FCI-CON26-4-GP-U
62.10081.011

SB 0312

MINIC1
SKT-MINI52P-8-GP
62.10043.391

SB 0312

U50
W83L351YG-GP
74.83351.073

-1 0417

Place them Near to Chip

Place them Near to Connector

Place near MINIC1

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / NEW CARD

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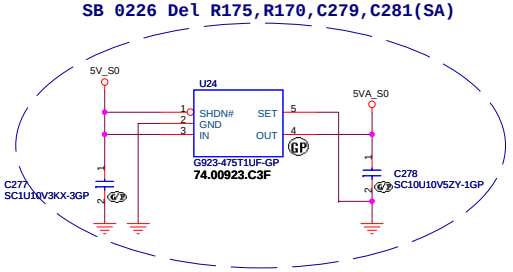
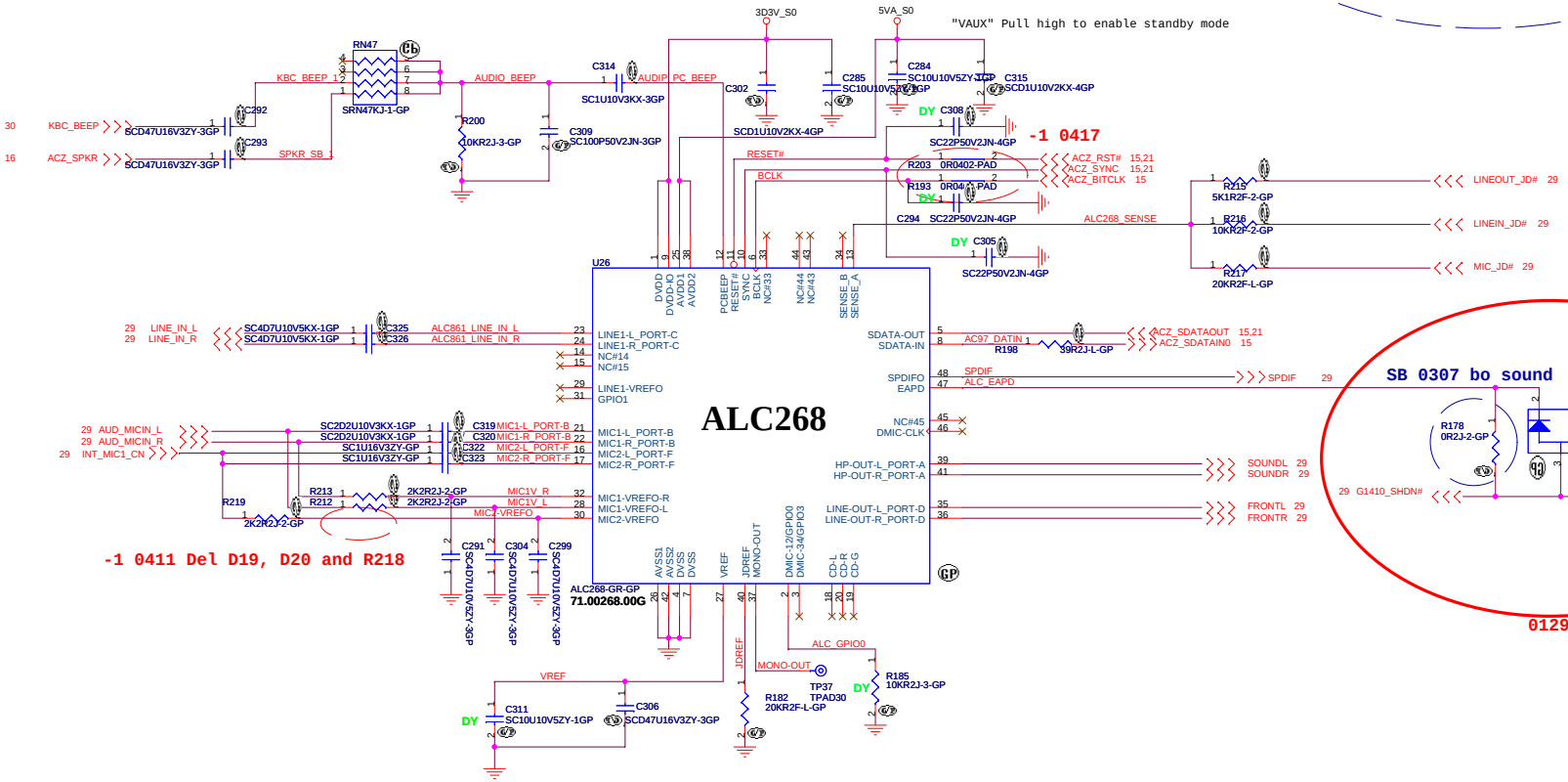
SB 0226 Del R175,R170,C279,C281(SA)



"VAUX" Pull high to enable standby mode



-1 0411 Del D19, D20 and R218

SB 0307 bo sound

0129

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AZALIA CODEC - ALC268

Size | Document Number: Volvi | Rev: -1

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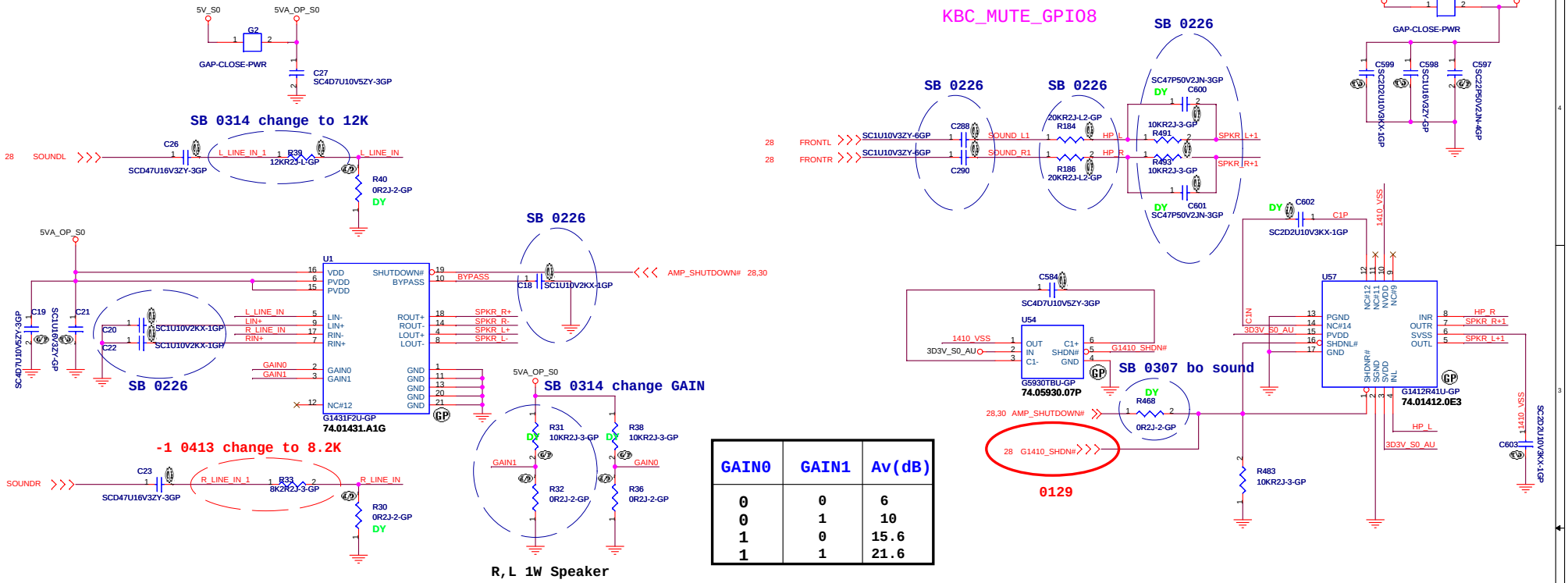
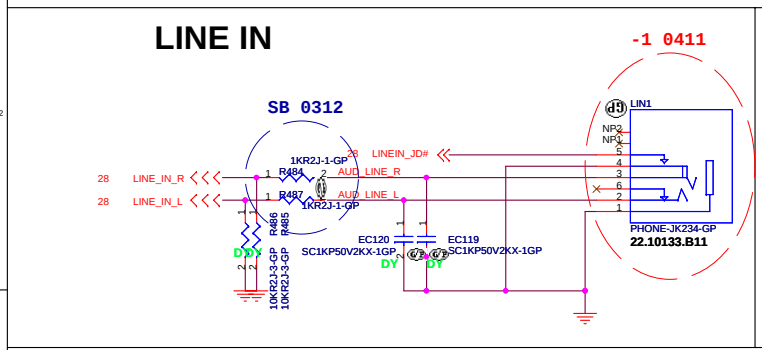
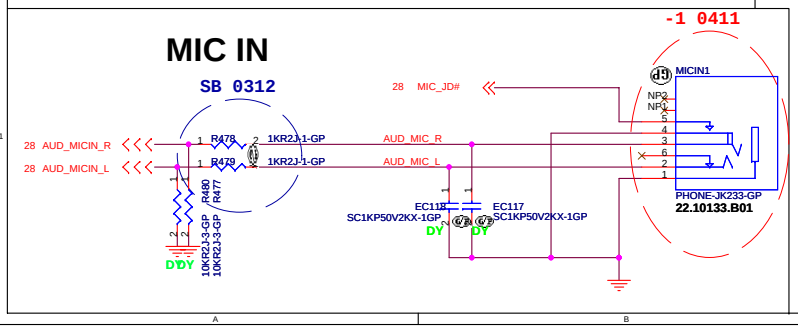
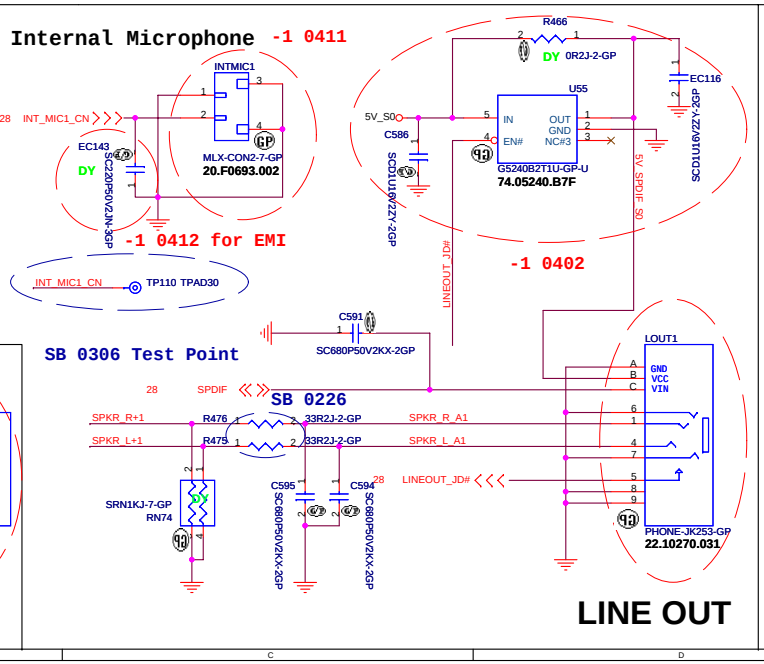
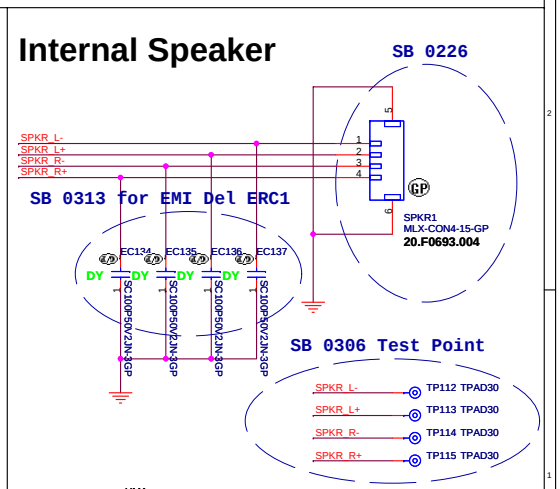
AUDIO OP AMPLIFIER











UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO AMP AND JACK*

Size | Document Number: Volvi | Rev: -1

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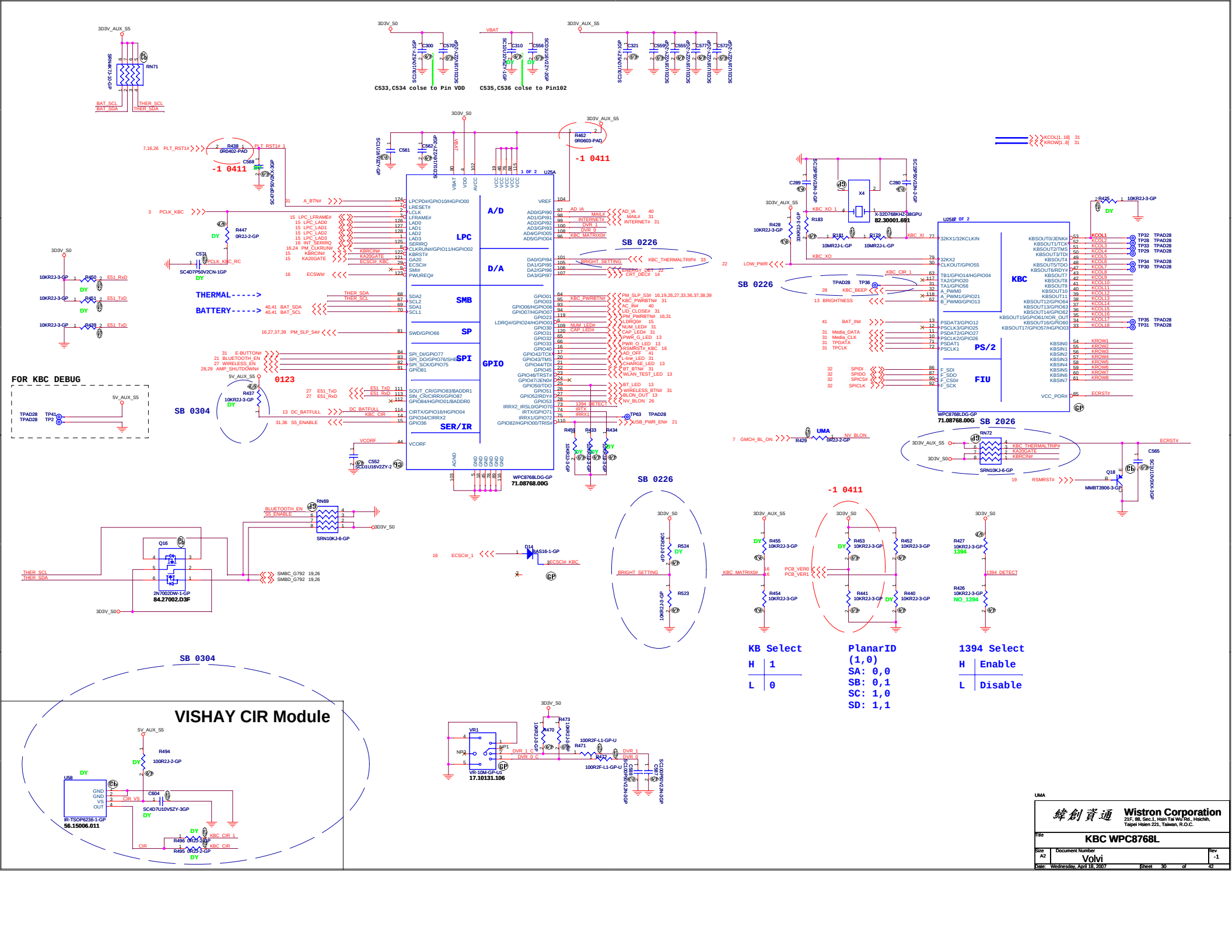
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
-1 0411
SB 0226
SB 0304
SB 2026
FOR KBC DEBUG
THERMAL----->
BATTERY----->
0123
LPC
SMB
SP
SPI
SER/IR
A/D
D/A
GPIO
PS/2
FIU
KBC
WPC8768LDG-GP
71.08768.00G
VISHAY CIR Module
IR-TSOP6236-1-GP
56.15006.011
2N7002DW-1-GP
84.27002.D3F
VR-10M-GP-U1
17.10131.106
X-32D768KHZ-38GPU
82.30001.691
MMBT3906-3-GP
KB Select
H | 1
L | 0
PlanarID (1,0)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1
1394 Select
H | Enable
L | Disable
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Volvi
Wednesday, April 18, 2007
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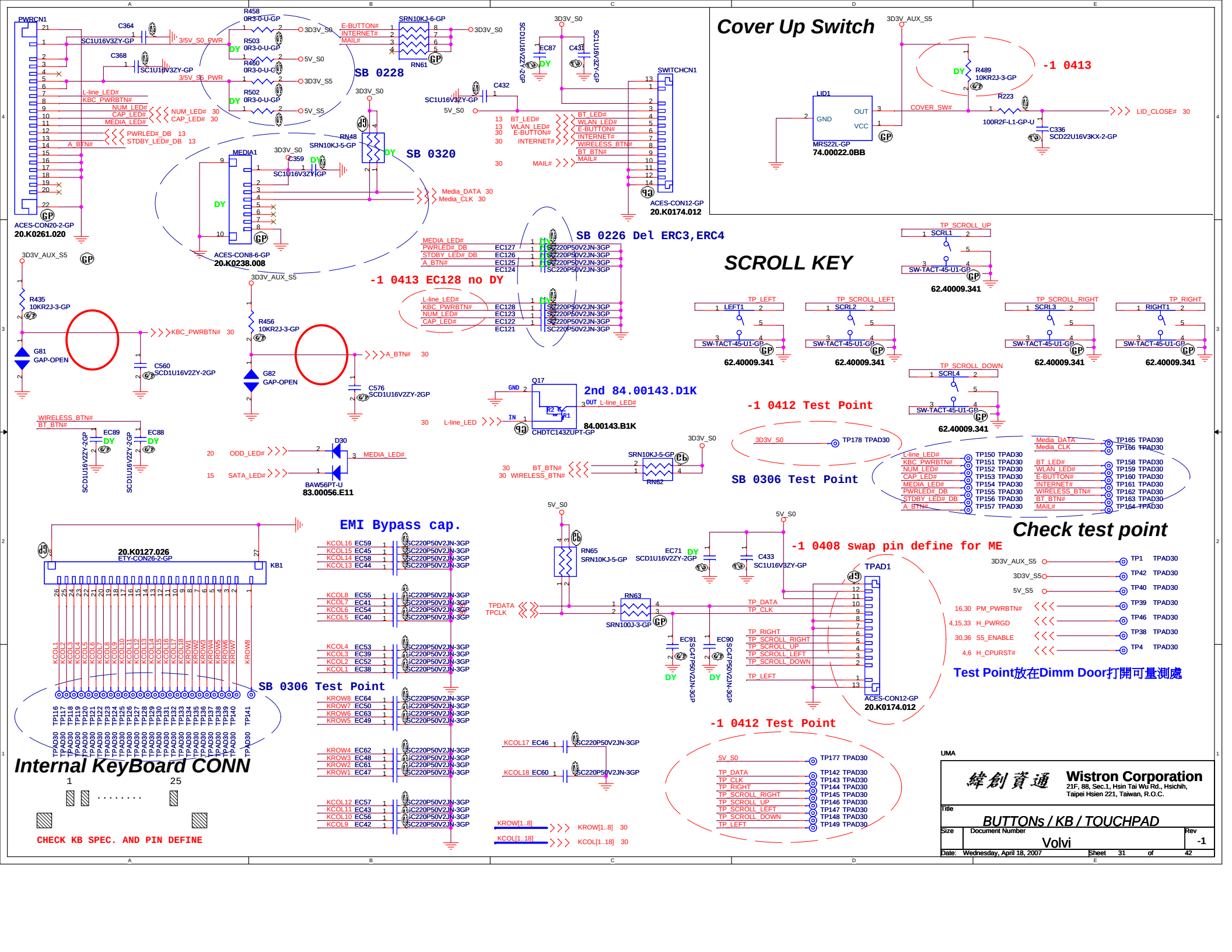
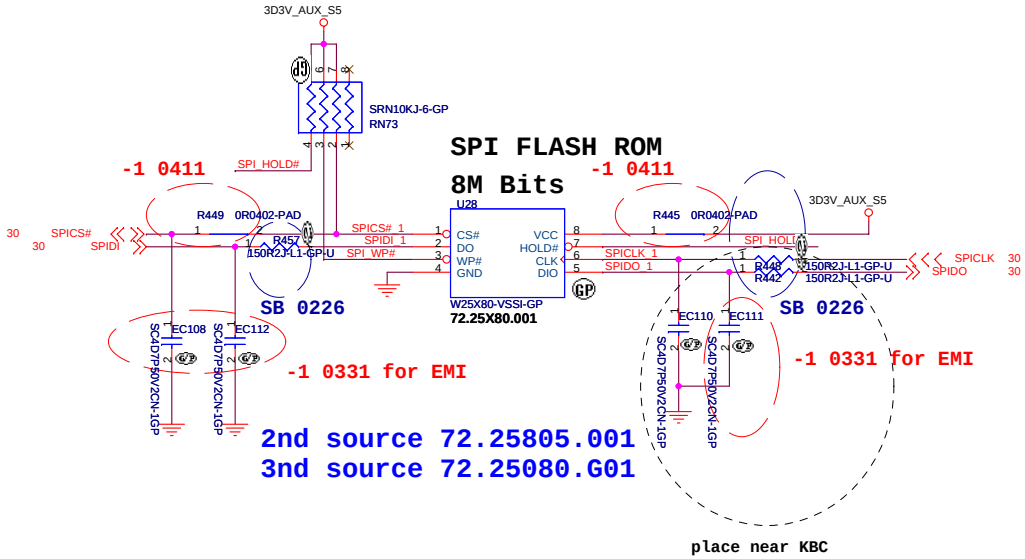

Cover Up Switch
-1 0413
SB 0228
SB 0320
SB 0226 Del ERC3,ERC4
-1 0413 EC128 no DY
SCROLL KEY
2nd 84.00143.D1K
-1 0412 Test Point
SB 0306 Test Point
Check test point
EMI Bypass cap.
-1 0408 swap pin define for ME
Test Point放在Dimm Door打開可量測處
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
Wistron Corporation
BUTTONs / KB / TOUCHPAD
Volvi



UMA

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Title: BIOS		
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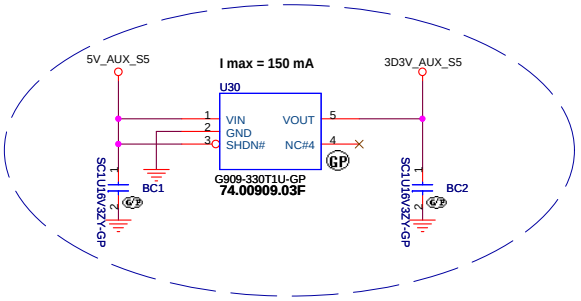
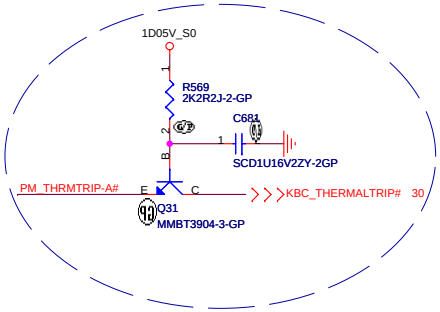
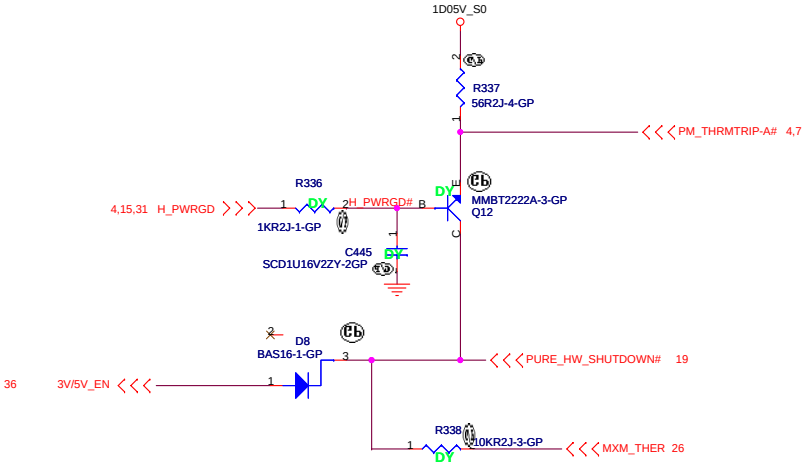
Aux Power

3D3V_AUX_S5



SB 0216

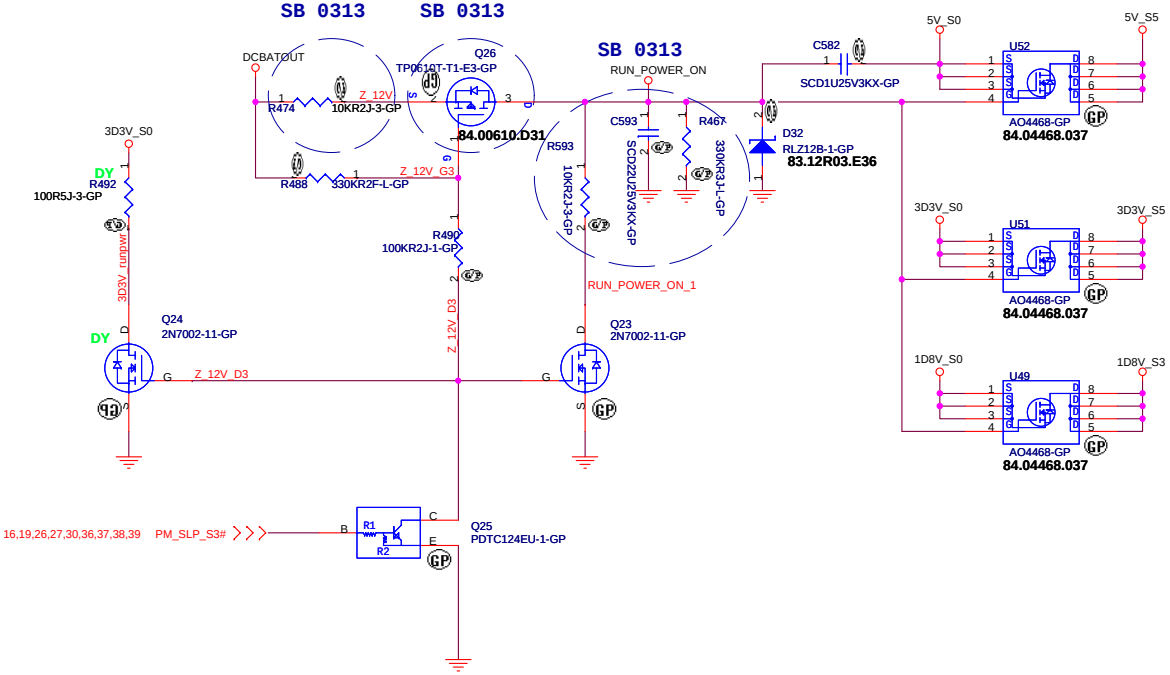




SB 0226 Del R458,R460,BC3 (SA)

Run Power

SB 0313 SB 0313 SB 0313



UMA

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Title	RUN POWER and 3D3V_AUX_S5	
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CPU_CORE
MAX8770

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6

VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)
VID6(I / 1.05V)

PSI#
CPUCORE_ON
PM_DPRSLPVR
H_DPRSTP#

Input Signal
PSI# (I / 3.3V)
SHDN#(I / 3.3V)
DPRSLPVR (I / 3.3V)
DPRSTP# (I / 3.3V)

VCC_SENSE
VSS_SENSE

Voltage Sense
CCI(I / Vcore)
GNDS(I / Vcore)

DCBATOUT_6262
5V_S0
5V_S0

Input Power
VCC(I)
VCC(I)
VDD(I)

Output Signal
PWRG(OD / 3.3V)
VGATE_PWRGD

Output Power
VCC_CORE_PWR(O)
VCC_CORE_S0(Imax=44A)

MAX8717
1D8V_S3 / 1D05V_S0

2007.1.19

5V_S0
DCBATOUT
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (8A)

TPS51100
DDR_VREF_S0

PM_SLP_S3#
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

DDR_VREF_S0 (1.2A)
DDR_VREF_S3

APL5912
1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN
1D5V(O)
POK

1D5V_S0 (3.6A)
CPUCORE_ON

5V_S5
1D8V_S3

MAX8744
5V_S5 / 3D3V_S5

8744_SHDN#
S5_ENABLE
S5_ENABLE

Input Signal
SHDN#
ON3
ON5

DCBATOUT

Input Power
VIN

Output Signal
PGOOD1(OD / 5V)
PGOOD2(OD / 5V)

CPUCORE_ON
CPUCORE_ON

Output Power
PGOOD5(O)
PGOOD3(O)

5V_S5 (5A)
3D3V_S5 (6A)

APL5312
2D5V_S0

3D3V_S0

VIN
VOUT

2D5V_S0 (130mA)

Charger MAX8731A

CHGON#/OFF
BT_TH
AD+

Input Signal
ICTL
PKPRES

Input Power
ACIN

Output Signal
BATT
ACOK

Output Power
VOUT (O)
VOUT (O)

BT+SENSE
AC_IN
BT+
DCBATOUT

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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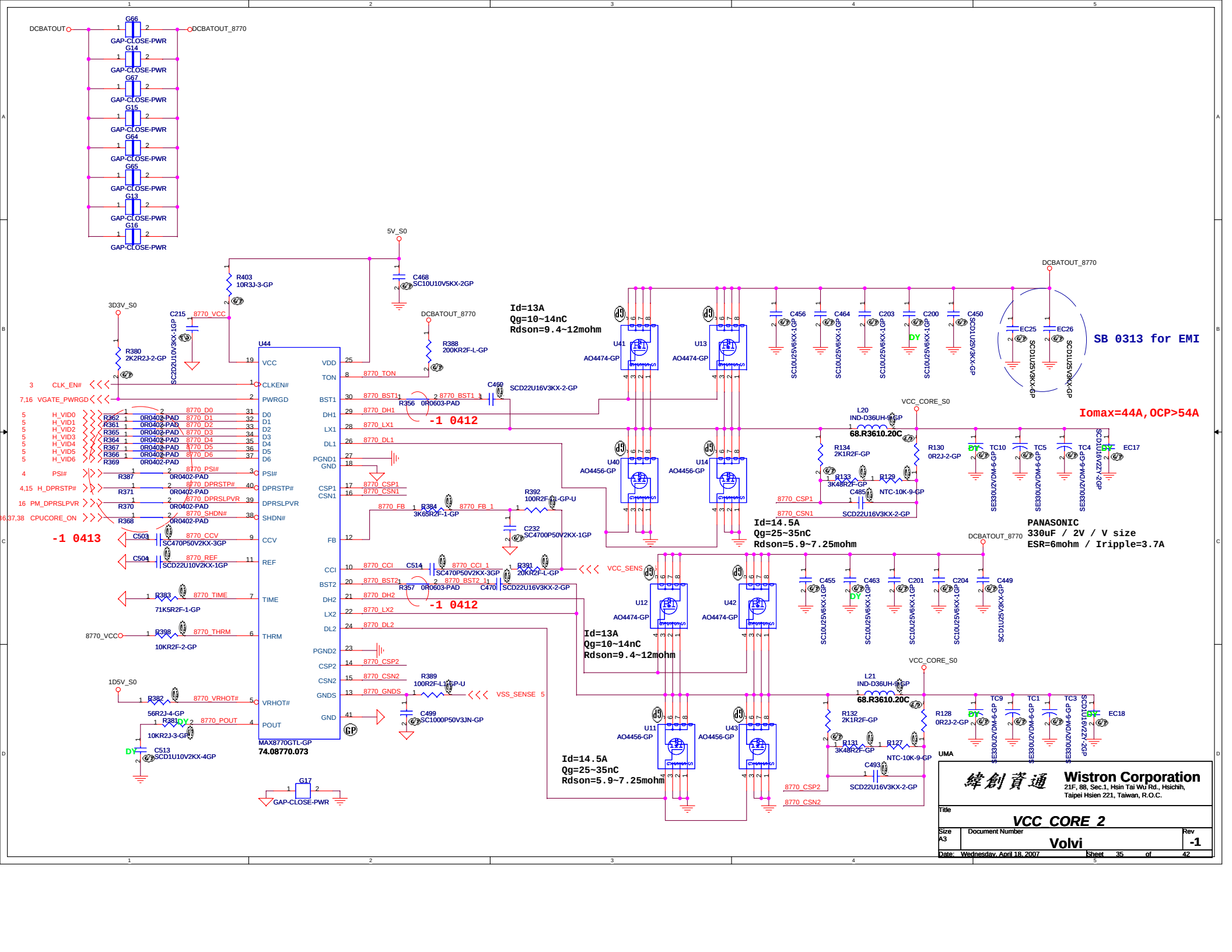
DCBATOUT
DCBATOUT_8770
GAP-CLOSE-PWR
5V_S0
3D3V_S0
1D5V_S0
VCC_CORE_S0
U44
MAX8770GTL-GP
74.08770.073
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
-1 0412
-1 0413
SB 0313 for EMI
Iomax=44A,OCP>54A
68.R3610.20C
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
UMA
Wistron Corporation
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VCC_CORE_2
Volvi
Size A3
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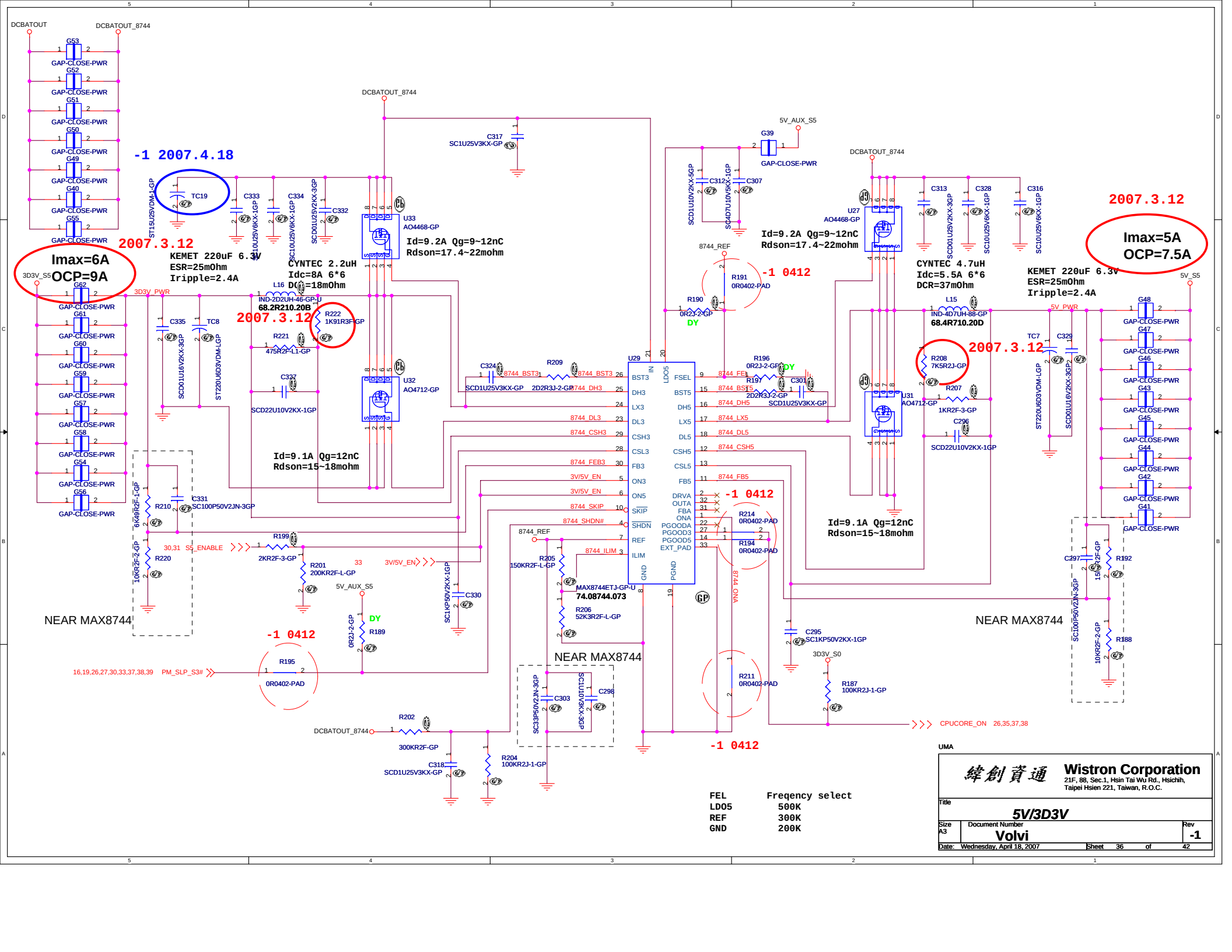
DCBATOUT
DCBATOUT_8744
-1 2007.4.18
2007.3.12
KEMET 220uF 6.3V
ESR=25mOhm
Iripple=2.4A
Imax=6A
OCP=9A
3D3V_S5
3D3V_PWR
CYNTEC 2.2uH
Idc=8A 6*6
DCR=18mOhm
68.2R210.20B
Id=9.2A Qg=9~12nC
Rdson=17.4~22mohm
Id=9.1A Qg=12nC
Rdson=15~18mohm
MAX8744ETJ-GP-U
74.08744.073
NEAR MAX8744
-1 0412
DY
5V_AUX_S5
CYNTEC 4.7uH
Idc=5.5A 6*6
DCR=37mOhm
68.4R710.20D
Imax=5A
OCP=7.5A
5V_S5
5V_PWR
CPUCORE_ON 26,35,37,38
PM_SLP_S3# 16,19,26,27,30,33,37,38,39
SS_ENABLE 30,31
3V/5V_EN 33
8744_REF
8744_ILIM
8744_SKIP
8744_SHDN#
8744_FEB3
8744_CSH3
8744_DL3
8744_DH3
8744_BST3
8744_FEL
8744_BST5
8744_DH5
8744_LX5
8744_DL5
8744_CSH5
8744_FB5
3V/5V_EN
FEL Freqency select
LDO5 500K
REF 300K
GND 200K
UMA
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Taipei Hsien 221, Taiwan, R.O.C.
Title
5V/3D3V
Size A3
Document Number
Volvi
Rev
-1
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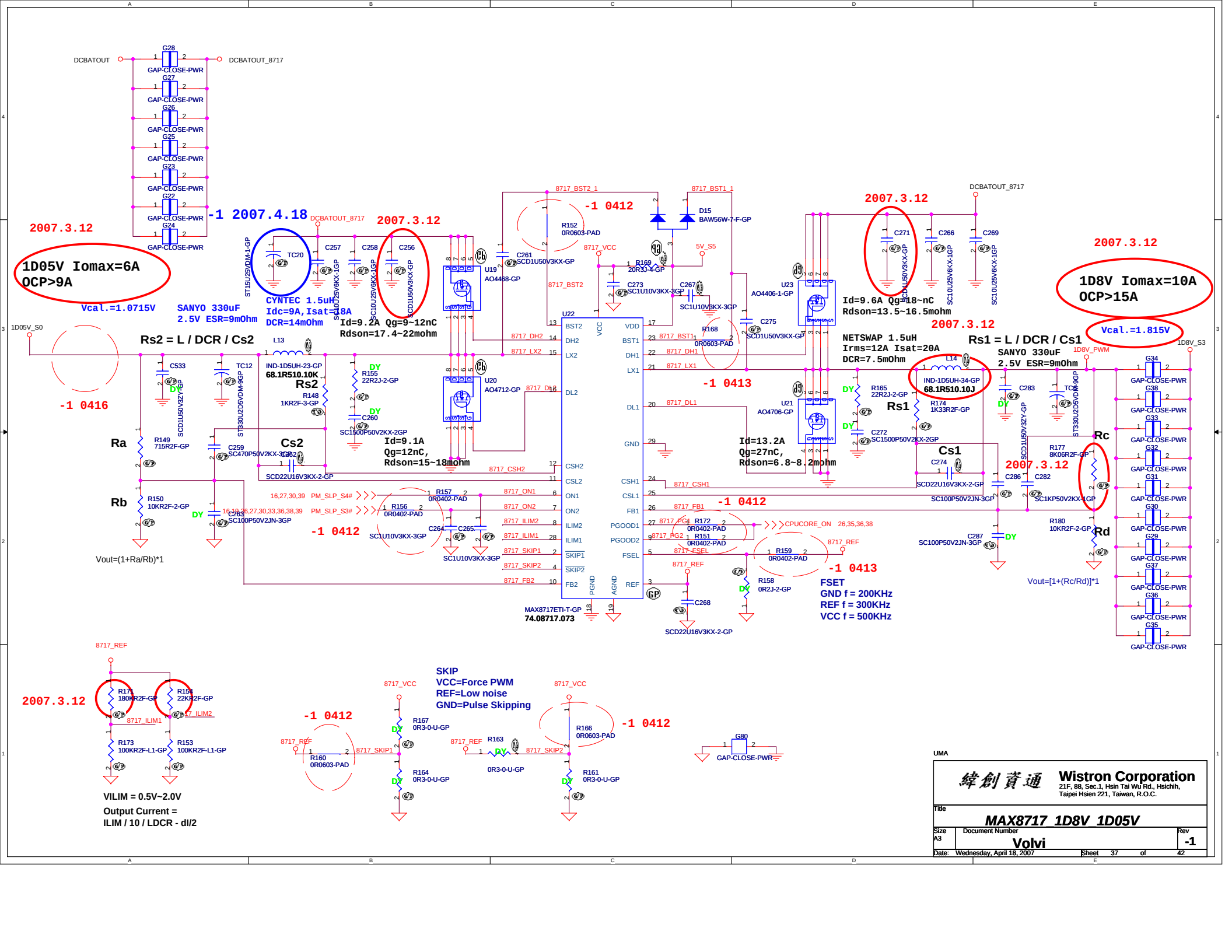
DCBATOUT
DCBATOUT_8717
G28 G27 G26 G25 G23 G22 G24
GAP-CLOSE-PWR
2007.3.12
1D05V Iomax=6A
OCP>9A
Vcal.=1.0715V
SANYO 330uF
2.5V ESR=9mOhm
-1 2007.4.18
CYNTEC 1.5uH
Idc=9A,Isat=18A
DCR=14mOhm
Id=9.2A Qg=9~12nC
Rdson=17.4~22mohm
2007.3.12
-1 0412
1D05V_S0
Rs2 = L / DCR / Cs2
-1 0416
Ra
Rb
Vout=(1+Ra/Rb)*1
Cs2
Id=9.1A
Qg=12nC,
Rdson=15~18mohm
-1 0412
MAX8717ETI-T-GP
74.08717.073
-1 0413
Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm
2007.3.12
NETSWAP 1.5uH
Irms=12A Isat=20A
DCR=7.5mOhm
Rs1 = L / DCR / Cs1
SANYO 330uF
2.5V ESR=9mOhm
Vcal.=1.815V
1D8V Iomax=10A
OCP>15A
Rc
Rd
Vout=[1+(Rc/Rd)]*1
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dI/2
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MAX8717_1D8V_1D05V
Size A3
Document Number
Volvi
Rev
-1
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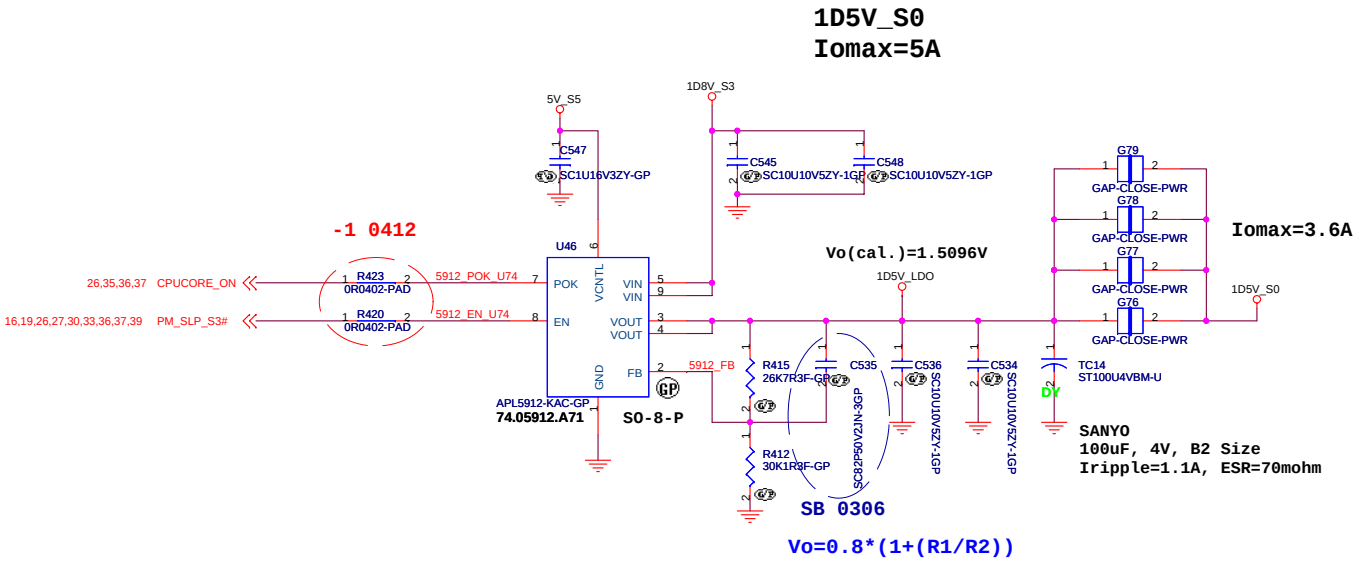

UMA

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Title	***APW5912_1D5V***	
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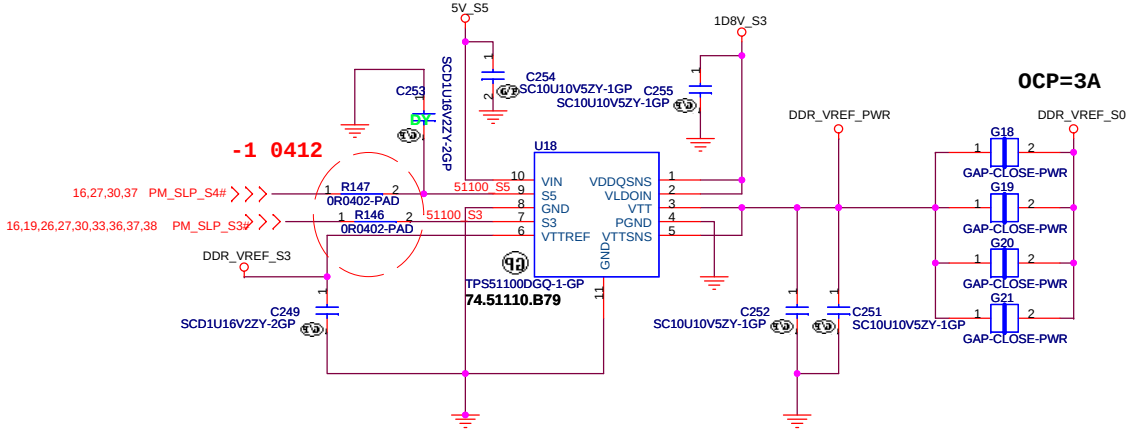
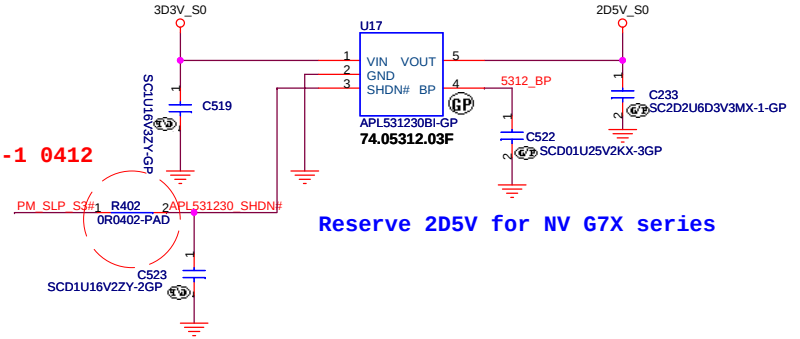
0D9V_S3
Iomax=0.5A



2D5V
Iomax=130mA



Reserve 2D5V for NV G7X series

UMA

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Title: *2D5V / 0D9V*		
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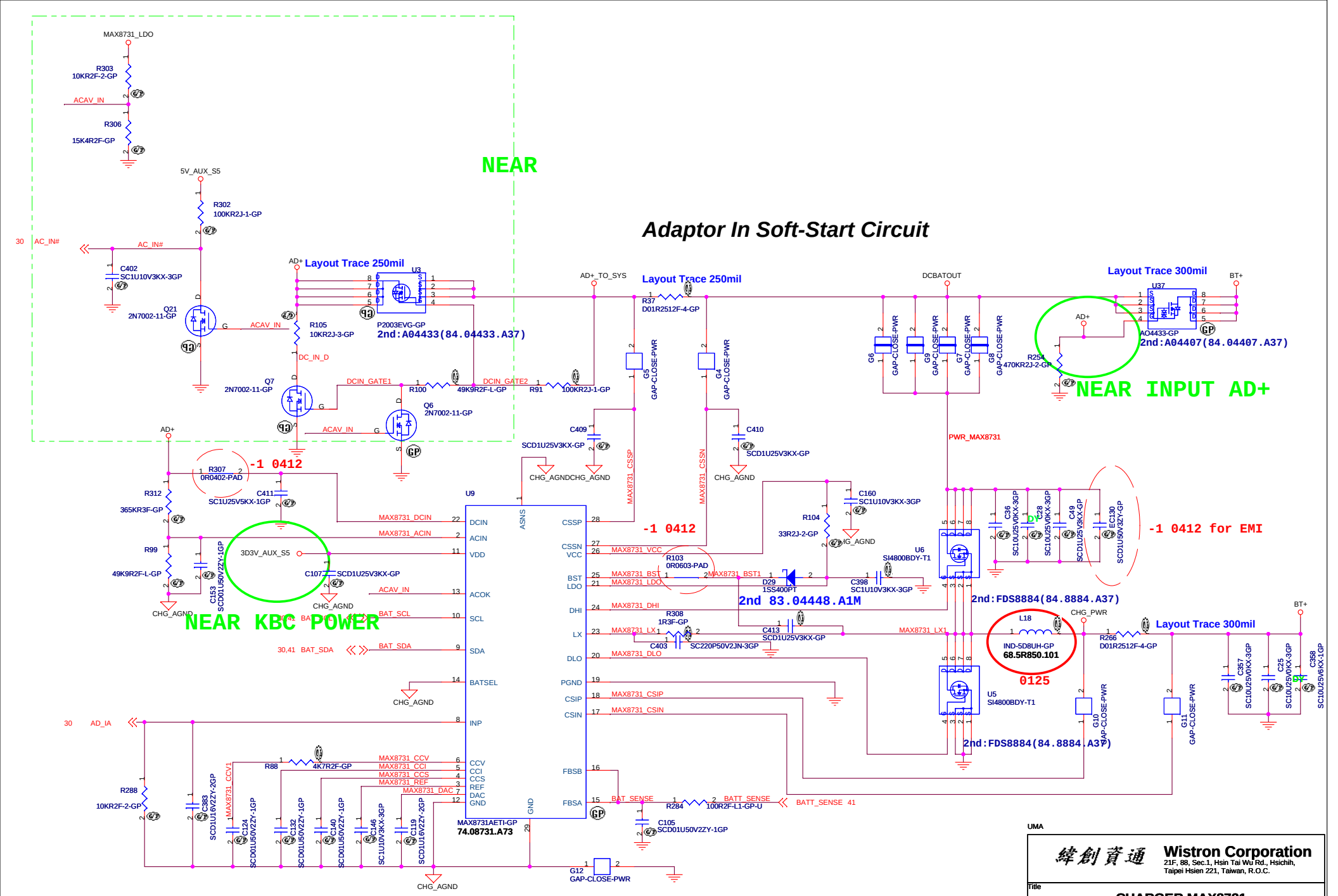

Need Check MAXIM Sming Use MAX8731 or MAX8731A

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8731**

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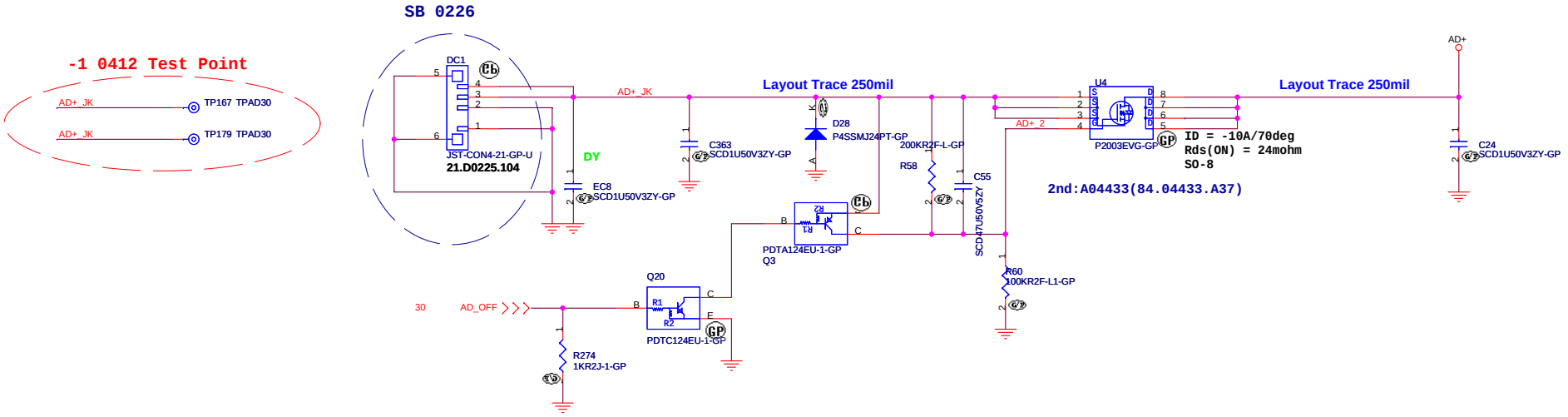
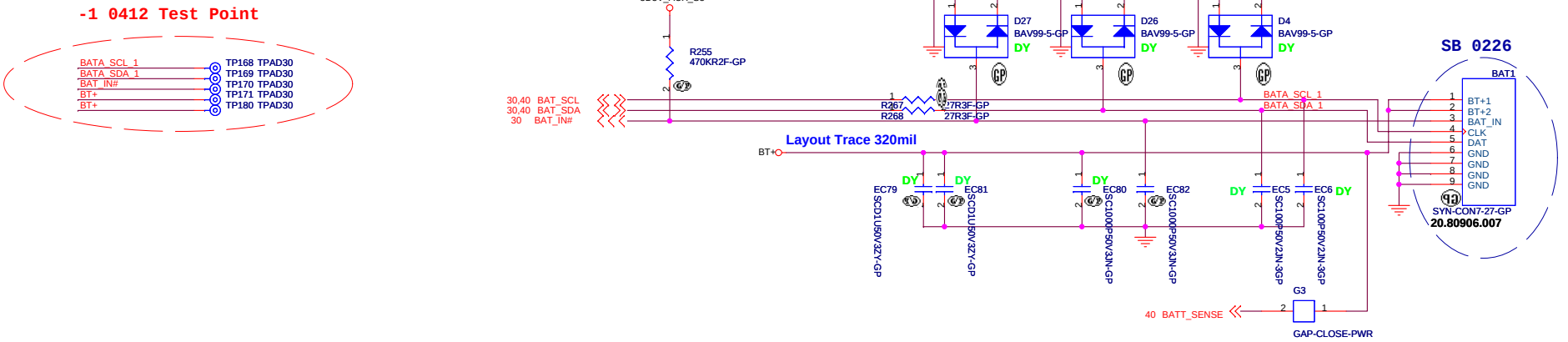
Adaptor in to generate DCBATOUT





UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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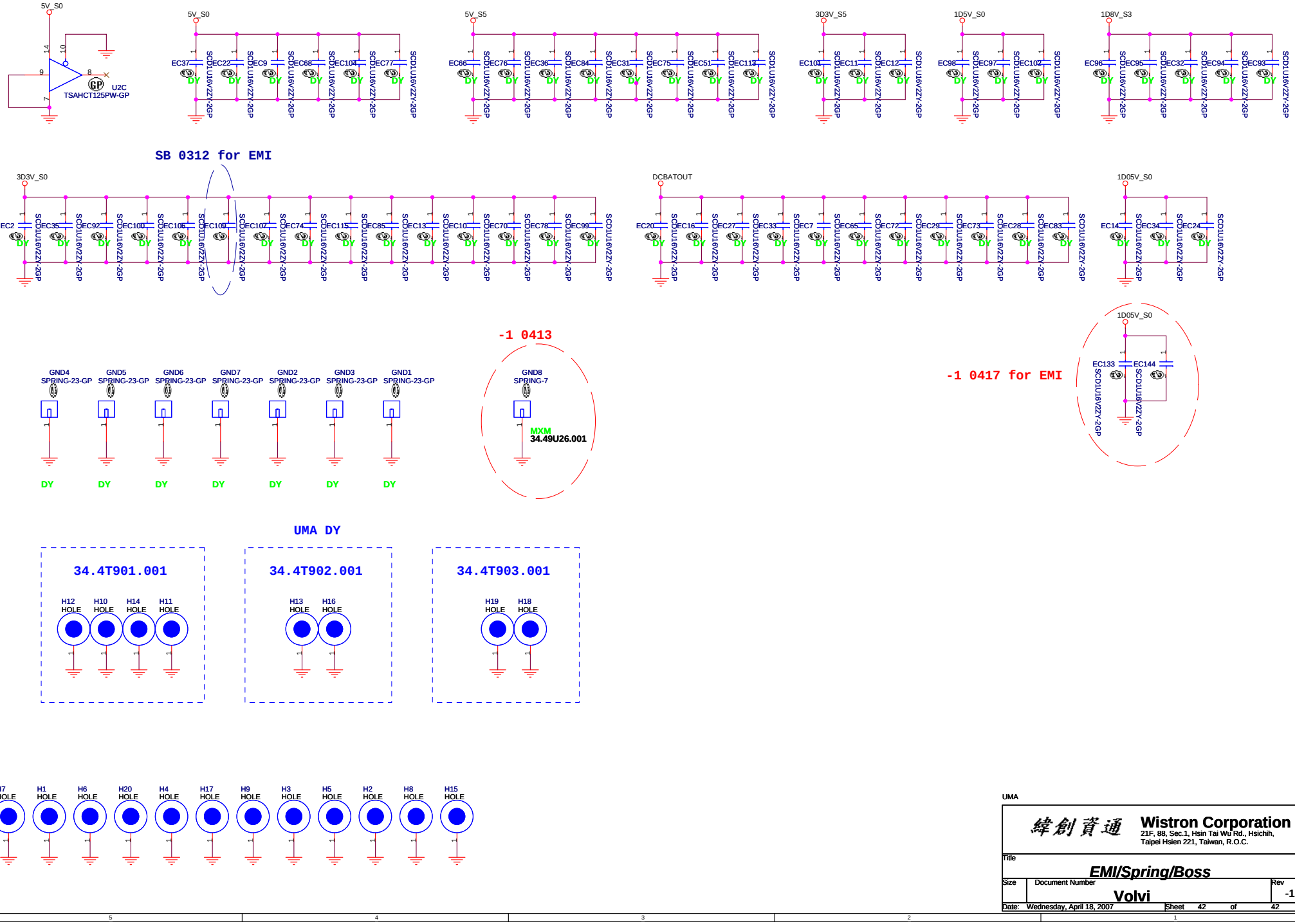

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

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