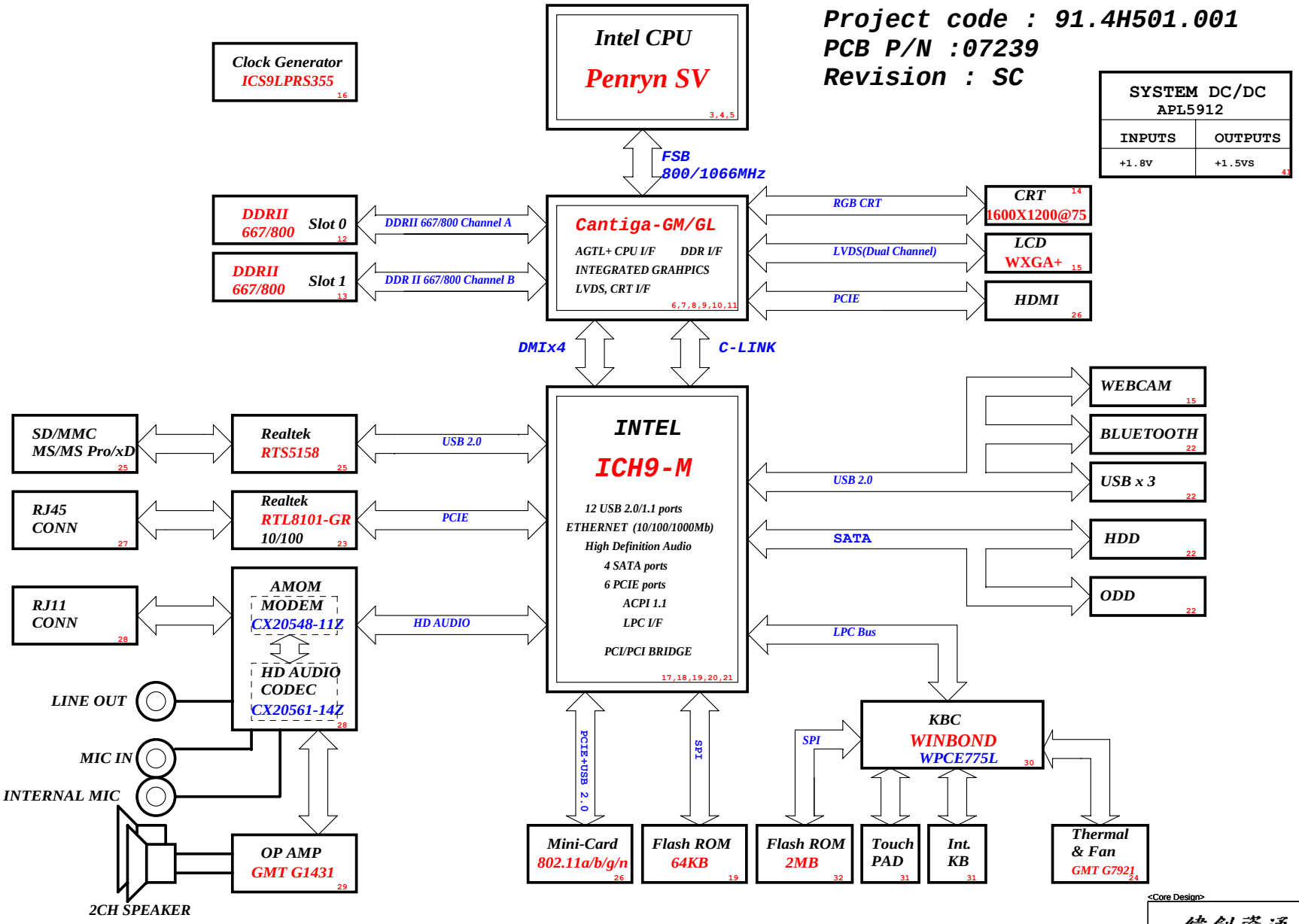
Warrior Intel UMA Block Diagram

Project code : 91.4H501.001
PCB P/N :07239
Revision : SC



SYSTEM DC/DC APL5912

INPUTS	OUTPUTS
+1.8V	+1.5VS 43

SYSTEM DC/DC TPS51120

INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 38

SYSTEM DC/DC TPS51116

INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V 39

SYSTEM DC/DC SC412A

INPUTS	OUTPUTS
+5VALW	+1.05V 40

MAXIM CHARGER MAX8731

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 34

CPU DC/DC ISL6269CCRZ

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A 36,37

PCB LAYER

L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

<Core Design>

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Title: Block Diagram

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

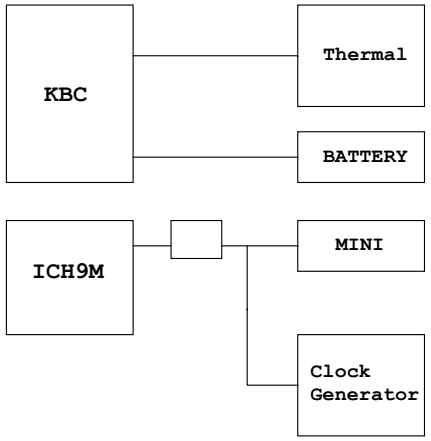
PCIE Routing page 19

LANE1	**LAN**
LANE2	**MiniCard WLAN**

USB Table page 19

USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus



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Title: **Table of Content**

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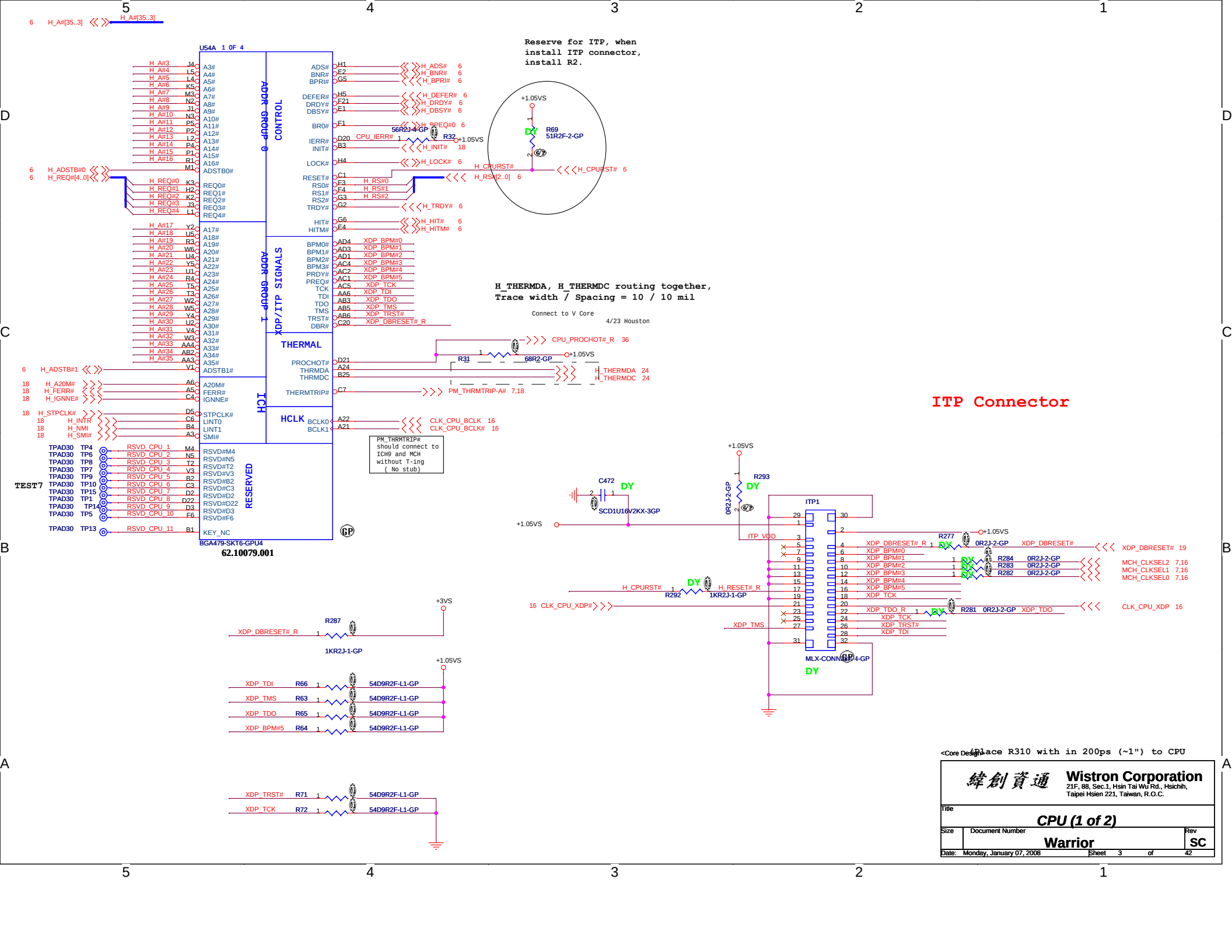
U54A 1 OF 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
ICH
HCLK
RESERVED
BGA479-SKT6-GPU4
62.10079.001
Reserve for ITP, when install ITP connector, install R2.
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil
Connect to V Core
4/23 Houston
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
ITP Connector
MLX-CONN-SD-4-GP
Place R310 with in 200ps (~1") to CPU
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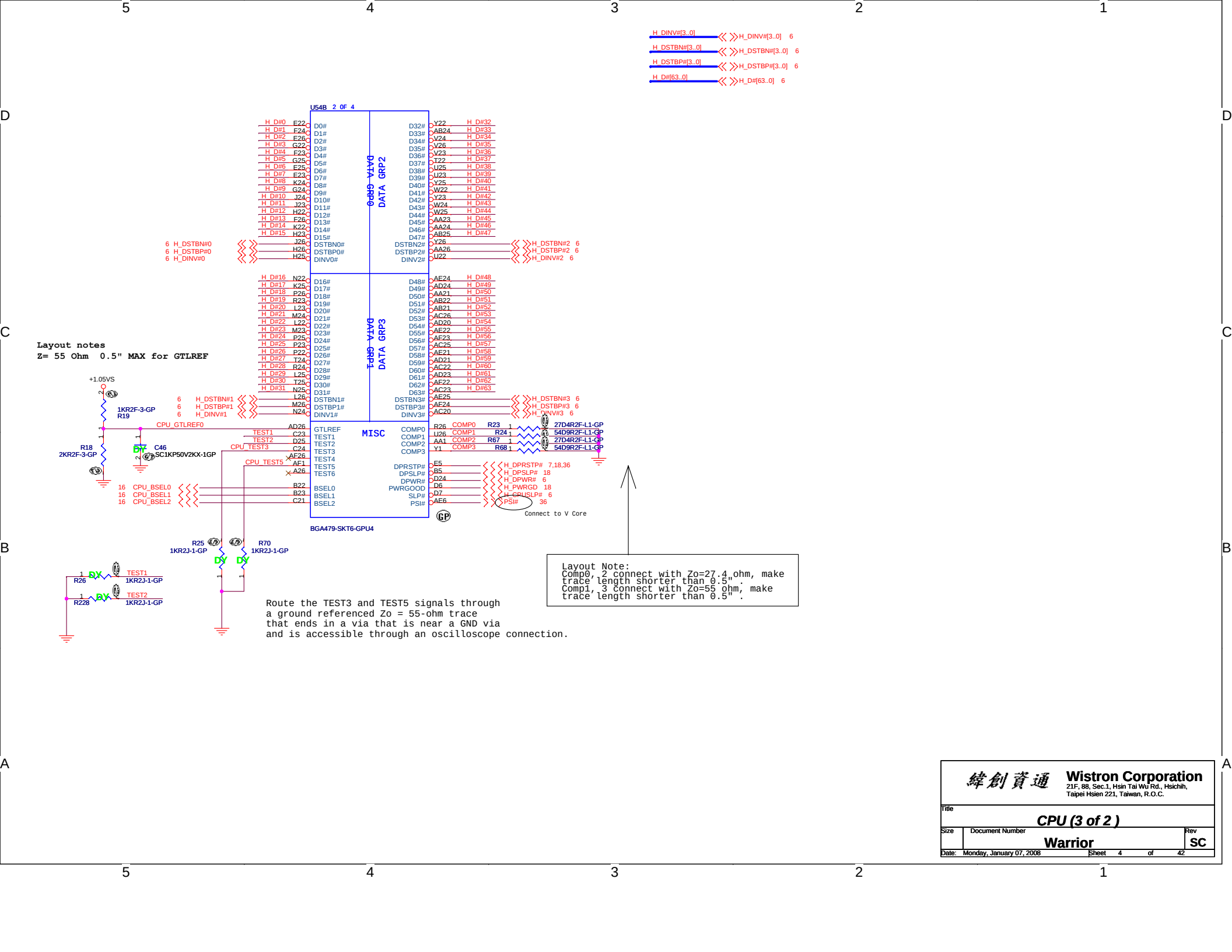
H_DINV#[3..0]
H_DINV#[3..0] 6
H_DSTBN#[3..0]
H_DSTBN#[3..0] 6
H_DSTBP#[3..0]
H_DSTBP#[3..0] 6
H_D#[63..0]
H_D#[63..0] 6
U54B 2 OF 4
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
BGA479-SKT6-GPU4
Layout notes
Z= 55 Ohm 0.5" MAX for GTLREF
+1.05VS
1KR2F-3-GP
R19
R18
2KR2F-3-GP
C46
SC1KP50V2KX-1GP
CPU_GTLREF0
TEST1
TEST2
CPU_TEST3
CPU_TEST5
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
R25
1KR2J-1-GP
R70
1KR2J-1-GP
R26
R228
Route the TEST3 and TEST5 signals through
a ground referenced Zo = 55-ohm trace
that ends in a via that is near a GND via
and is accessible through an oscilloscope connection.
Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make
trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make
trace length shorter than 0.5".
Connect to V Core
27D4R2F-L1-GP
54D9R2F-L1-GP
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Please these inside socket cavity on L8(North side Secondary)

Please these inside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(North side Primary)

Please these outside socket cavity on L8(North side Secondary)

Please these outside socket cavity on L8(South side Secondary)

Please these inside socket cavity on L8(South side Primary)

Please these inside socket cavity on L8(North side Secondary)

layout note: "1D5V_VCCA_S0" as short as possible

Layout Note:
Place as close as possible to the CPU VCCA pin.

Connect to V Core

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

NCTF PIN

U54C 3 OF 4

BGA479-SKT6-GPU4

U54D 4 OF 4

BGA479-SKT6-GPU4

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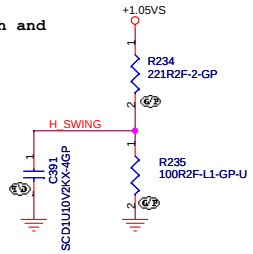
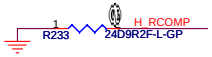
H_SWING routing Trace width and
Spacing use 10 / 20 mil

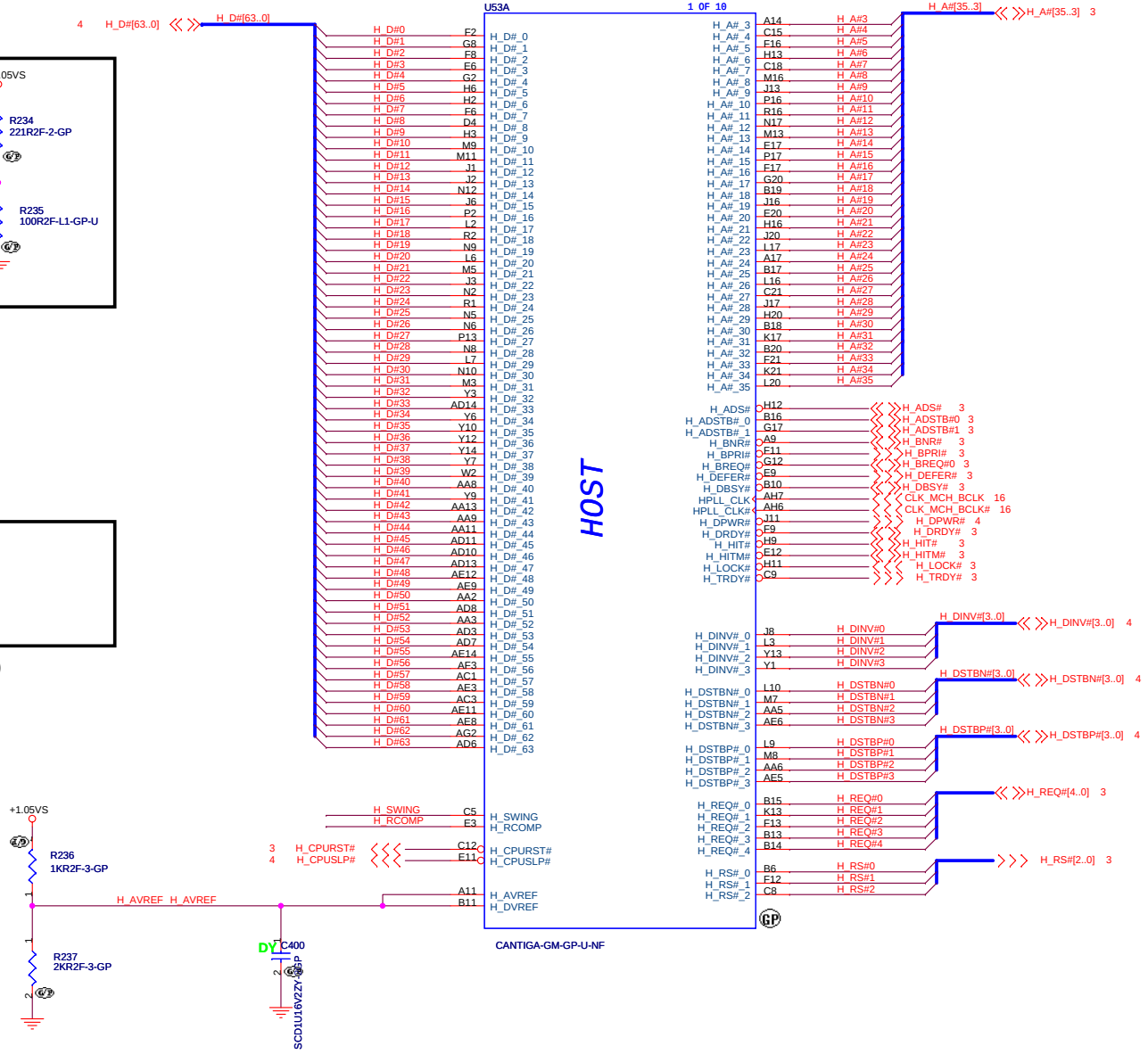
H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)

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Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.

FSB setting

DMI Lane Reversal
MCH_CFG_19 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

PCI Express Graphics Lane
MCH_CFG_9 Low = Normal (default)
High = Lanes Reversed
Cantiga = 2.2K

FOR Cantiga: 1.02k_1% ohm
CRT_IREF routing Trace width use 20 mil

CL_VREF ~= 0.35V

DDPC/SDVO for HDMI used

CRT Termination/EMI Filter

Place Close GMCH

Place Close Connector

Please Close GMCH

Please Close to U22

0104 SI

1231 SI

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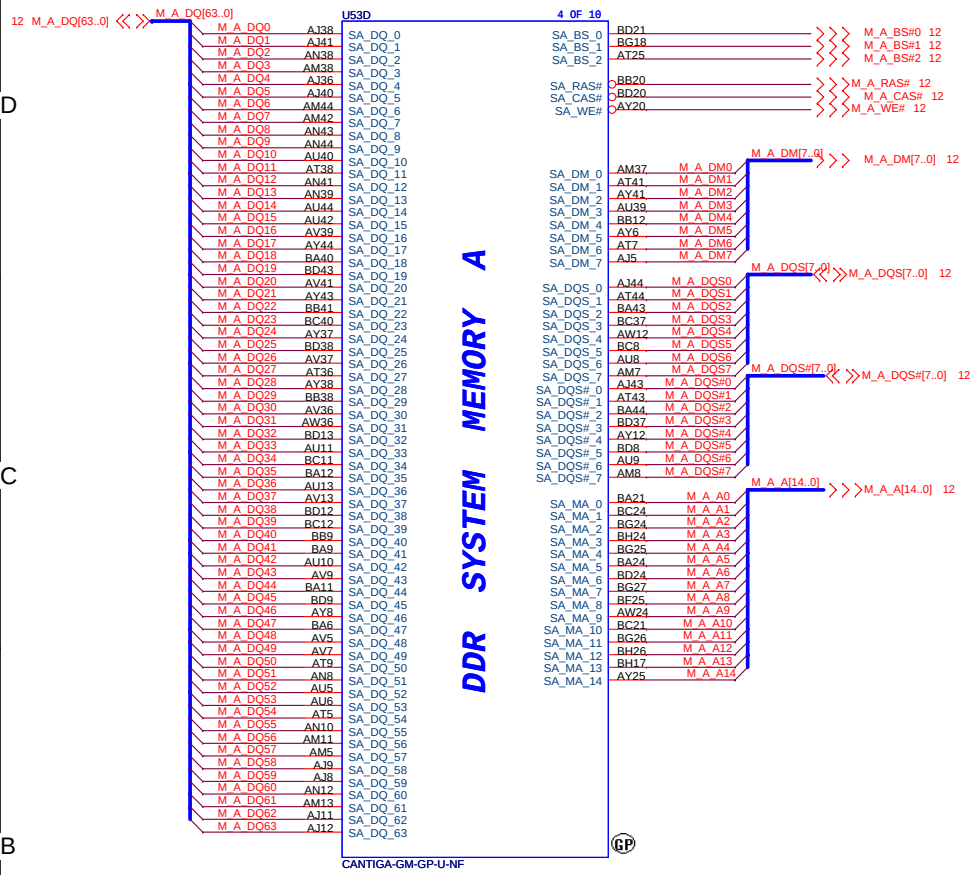

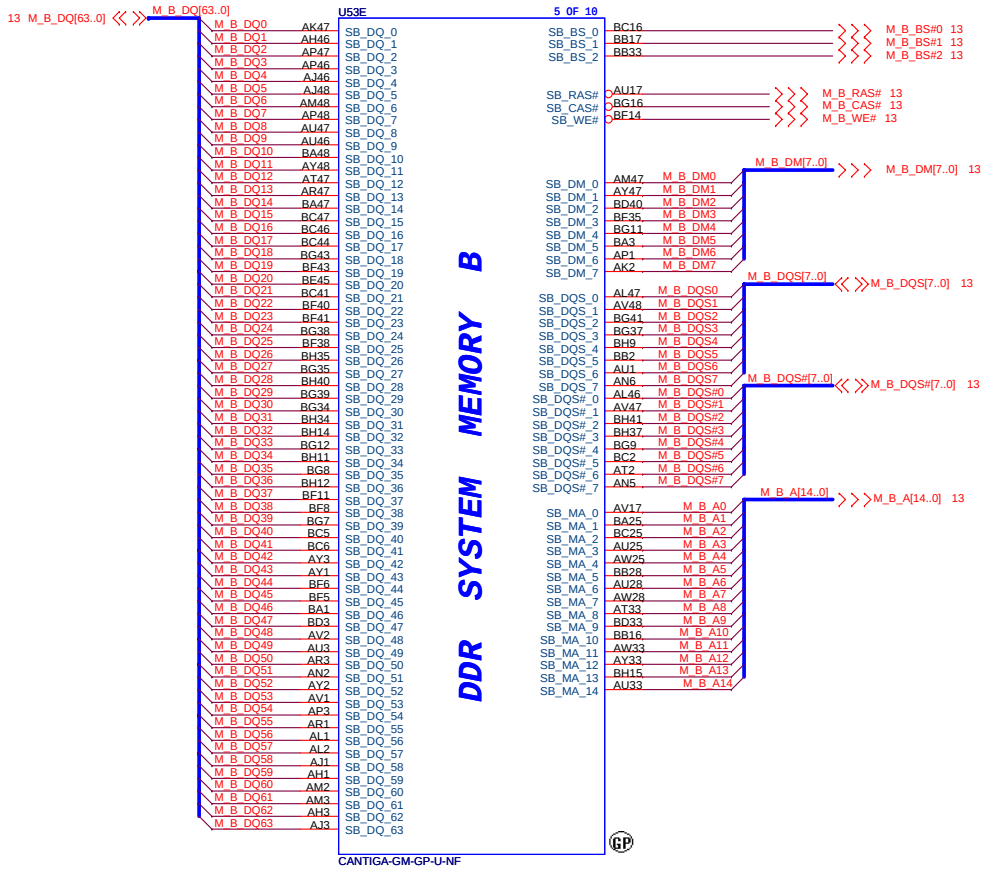

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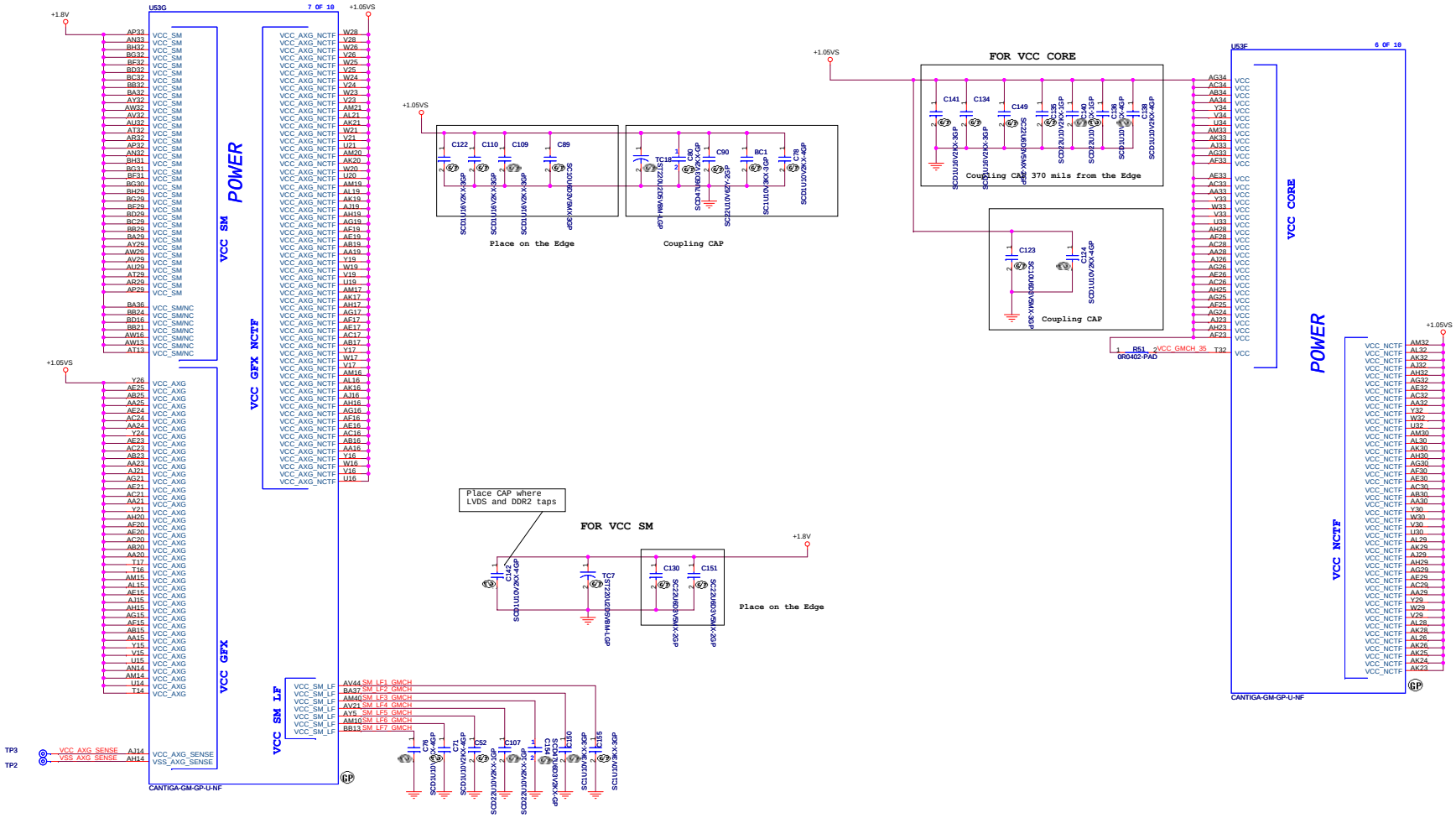

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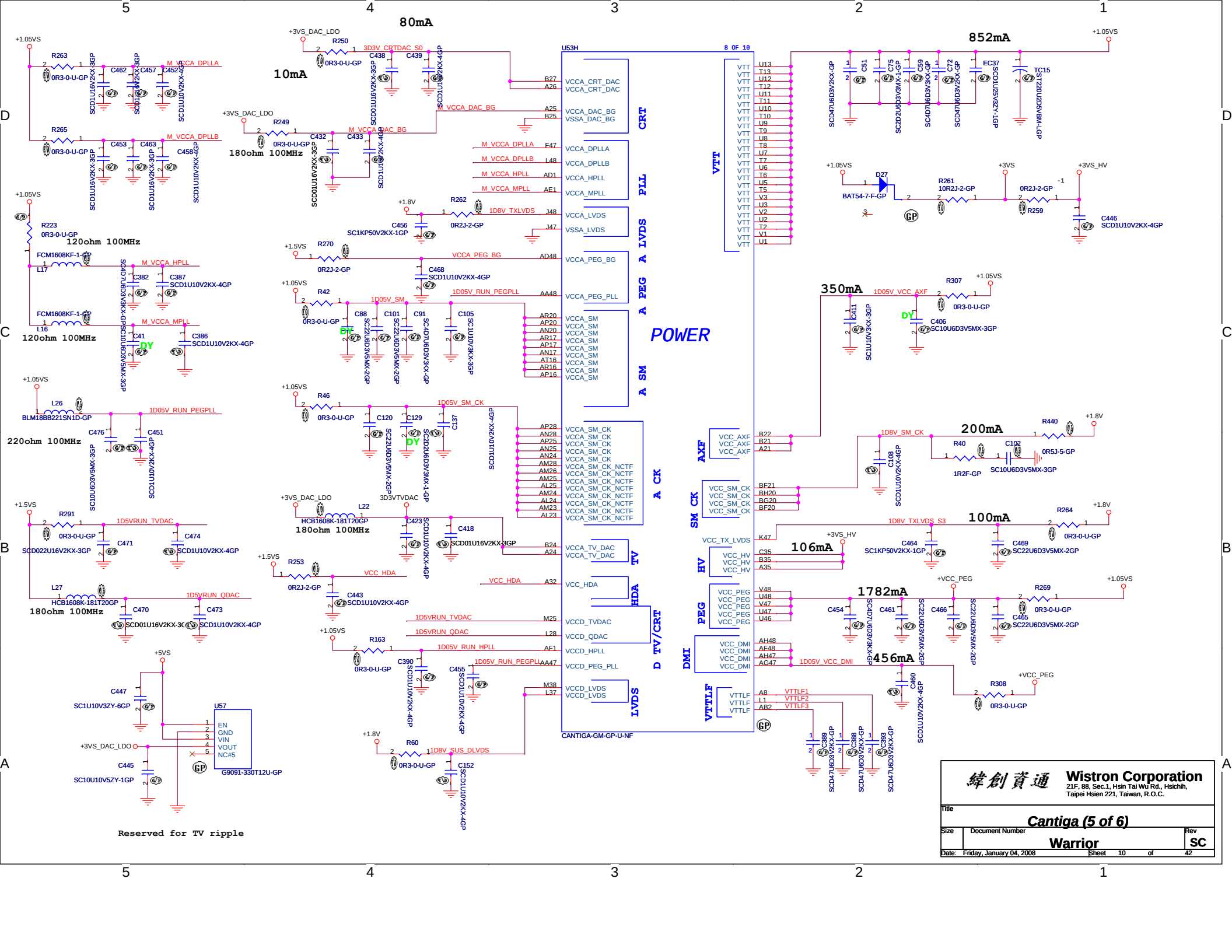
80mA
10mA
180ohm 100MHz
120ohm 100MHz
220ohm 100MHz
852mA
350mA
200mA
100mA
106mA
1782mA
456mA
U53H
8 OF 10
CANTIGA-GM-GP-U-NF
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
Reserved for TV ripple
G9091-330T12U-GP
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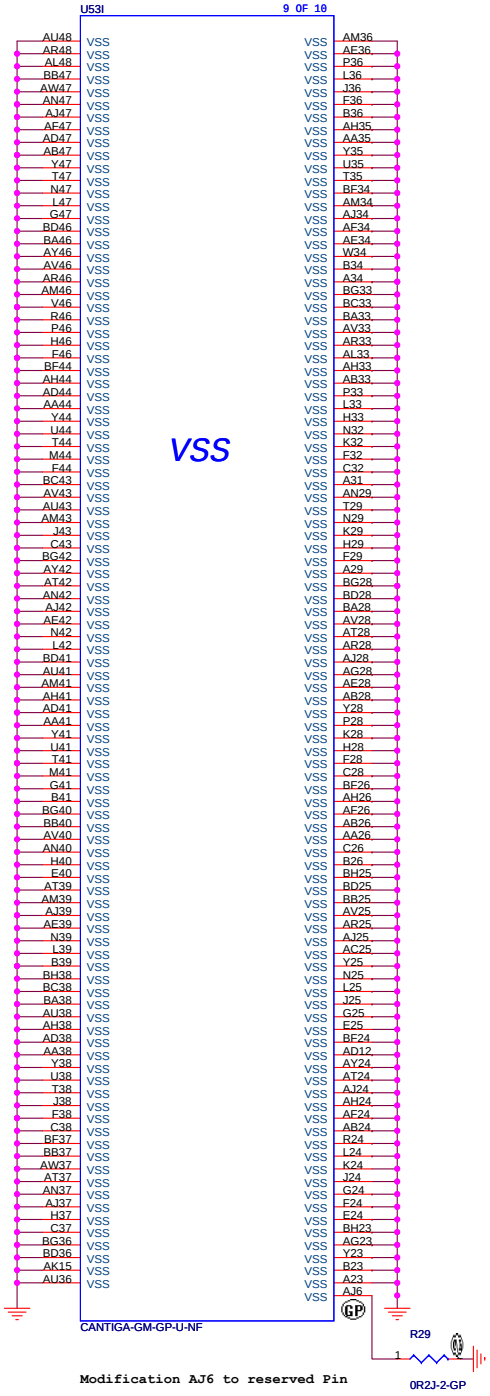

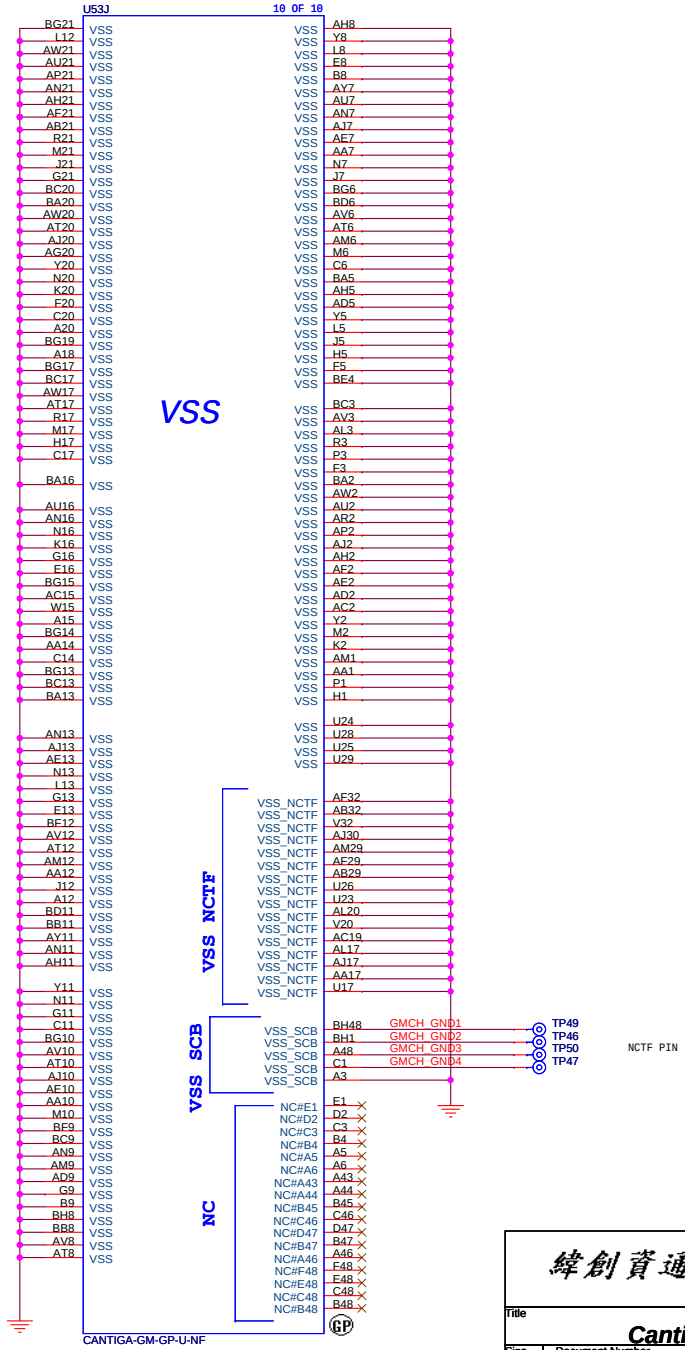

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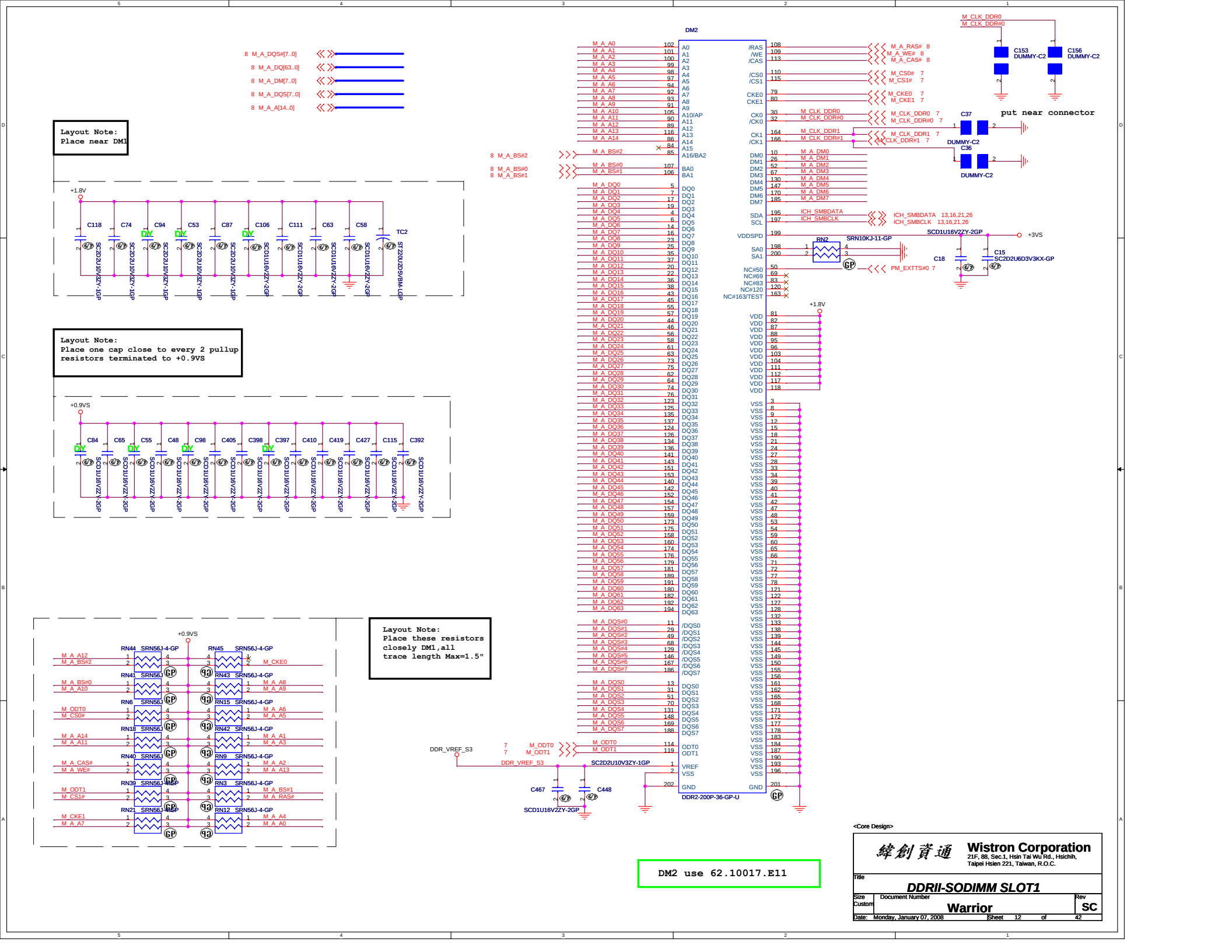
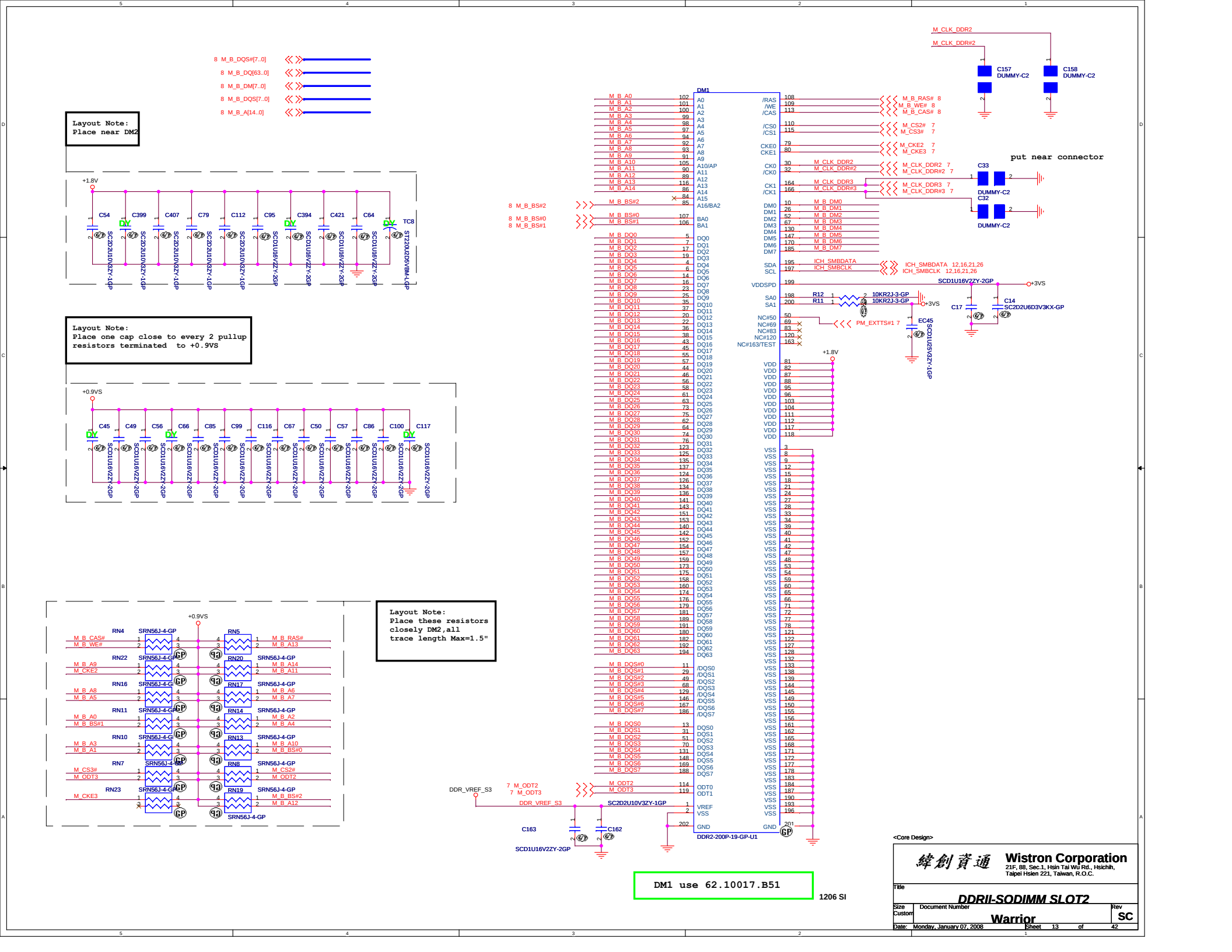
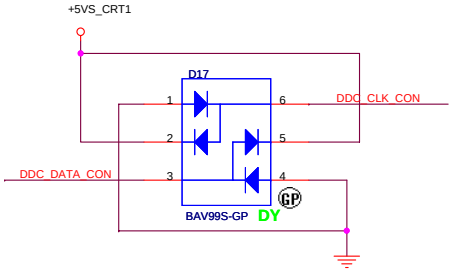
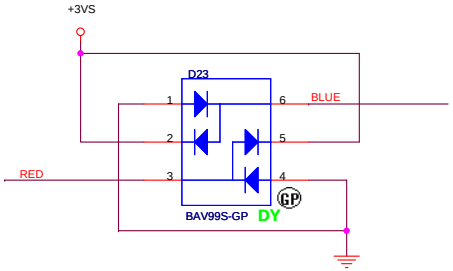
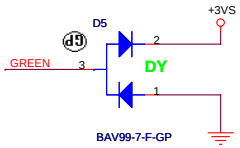

8 M_A_DQS#[7..0]
8 M_A_DQ[63..0]
8 M_A_DM[7..0]
8 M_A_DQS[7..0]
8 M_A_A[14..0]
Layout Note:
Place near DM1
+1.8V
C118 C74 C94 C53 C87 C106 C111 C63 C58 TC2
DIY
SC2D2U10V2ZY-1GP
SC1U16V2ZY-2GP
ST220U2D5VBM-1GP
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS
+0.9VS
C84 C65 C55 C48 C98 C405 C398 C397 C410 C419 C427 C115 C392
SCD1U16V2ZY-2GP
+0.9VS
RN44 SRN56J-4-GP
RN45 SRN56J-4-GP
RN41 SRN56J-4-GP
RN43 SRN56J-4-GP
RN6 SRN56J-4-GP
RN15 SRN56J-4-GP
RN18 SRN56J-4-GP
RN42 SRN56J-4-GP
RN40 SRN56J-4-GP
RN9 SRN56J-4-GP
RN39 SRN56J-4-GP
RN3 SRN56J-4-GP
RN21 SRN56J-4-GP
RN12 SRN56J-4-GP
M_A_A12
M_A_BS#2
M_CKE0
M_A_BS#0
M_A_A10
M_A_A8
M_A_A9
M_ODT0
M_CS0#
M_A_A6
M_A_A5
M_A_A14
M_A_A11
M_A_A1
M_A_A3
M_A_CAS#
M_A_WE#
M_A_A2
M_A_A13
M_ODT1
M_CS1#
M_A_BS#1
M_A_RAS#
M_CKE1
M_A_A7
M_A_A4
M_A_A0
Layout Note:
Place these resistors closely DM1,all trace length Max=1.5"
DM2
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14
M_A_BS#2
M_A_BS#0
M_A_BS#1
M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7 M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15 M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31 M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7
M_ODT0 M_ODT1
DDR_VREF_S3
SC2D2U10V3ZY-1GP
C467 C448
SCD1U16V2ZY-2GP
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2
BA0 BA1
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
/DQS0 /DQS1 /DQS2 /DQS3 /DQS4 /DQS5 /DQS6 /DQS7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
ODT0 ODT1
VREF VSS
GND
DDR2-200P-36-GP-U
/RAS /WE /CAS /CS0 /CS1 CKE0 CKE1 CK0 /CK0 CK1 /CK1 DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 SDA SCL VDDSPD SA0 SA1 NC#50 NC#69 NC#83 NC#120 NC#163/TEST
VDD
VSS
M_A_RAS# 8
M_A_WE# 8
M_A_CAS# 8
M_CS0# 7
M_CS1# 7
M_CKE0 7
M_CKE1 7
M_CLK_DDR0 7
M_CLK_DDR#0 7
M_CLK_DDR1 7
M_CLK_DDR#1 7
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 13,16,21,26
ICH_SMBCLK 13,16,21,26
SCD1U16V2ZY-2GP
+3VS
RN2 SRN10KJ-11-GP
C18 C15 SC2D2U6D3V3KX-GP
PM_EXTTS#0 7
+1.8V
M_CLK_DDR0
M_CLK_DDR#0
C153 DUMMY-C2
C156 DUMMY-C2
C37 DUMMY-C2
C36 DUMMY-C2
put near connector
DM2 use 62.10017.E11
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT1
Size Custom
Document Number
Warrior
Rev SC
Date: Monday, January 07, 2008
Sheet 12 of 42

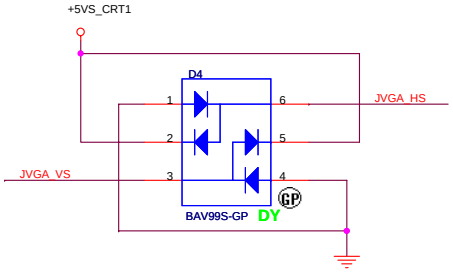

8 M_B_DQS#[7..0]
8 M_B_DQ[63..0]
8 M_B_DM[7..0]
8 M_B_DQS[7..0]
8 M_B_A[14..0]
Layout Note:
Place near DM2
+1.8V
C54 C399 C407 C79 C112 C95 C394 C421 C64 TC8
DIV
SC2D2U10V3ZY-1GP
SCD1U16V2ZY-2GP
ST220U2D5VM-1GP
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
+0.9VS
C45 C49 C56 C66 C85 C99 C116 C67 C50 C57 C86 C100 C117
SCD1U16V2ZY-2GP
Layout Note:
Place these resistors
closesly DM2,all
trace length Max=1.5"
+0.9VS
RN4 SRN56J-4-GP M_B_CAS# M_B_WE#
RN22 M_B_A9 M_CKE2
RN16 M_B_A8 M_B_A5
RN11 M_B_A0 M_B_BS#1
RN10 M_B_A3 M_B_A1
RN7 M_CS3# M_ODT3
RN23 M_CKE3
RN5 M_B_RAS# M_B_A13
RN20 M_B_A14 M_B_A11
RN17 M_B_A6 M_B_A7
RN14 M_B_A2 M_B_A4
RN13 M_B_A10 M_B_BS#0
RN8 M_CS2# M_ODT2
RN19 M_B_BS#2 M_B_A12
SRN56J-4-GP
DM1
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14
8 M_B_BS#2
8 M_B_BS#0
8 M_B_BS#1
M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15 M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39 M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47 M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55 M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63
M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7
M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7
7 M_ODT2
7 M_ODT3
M_ODT2 M_ODT3
DDR_VREF_S3
SC2D2U10V3ZY-1GP
C163 C162
SCD1U16V2ZY-2GP
/RAS /WE /CAS
M_B_RAS# 8
M_B_WE# 8
M_B_CAS# 8
/CS0 /CS1
M_CS2# 7
M_CS3# 7
CKE0 CKE1
M_CKE2 7
M_CKE3 7
CK0 /CK0
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR2 7
M_CLK_DDR#2 7
CK1 /CK1
M_CLK_DDR3
M_CLK_DDR#3
M_CLK_DDR3 7
M_CLK_DDR#3 7
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
M_B_DM0 M_B_DM1 M_B_DM2 M_B_DM3 M_B_DM4 M_B_DM5 M_B_DM6 M_B_DM7
SDA SCL
ICH_SMBDATA
ICH_SMBCLK
ICH_SMBDATA 12,16,21,26
ICH_SMBCLK 12,16,21,26
VDDSPD
SCD1U16V2ZY-2GP
+3VS
SA0 SA1
R12 R11
10KR2J-3-GP
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
PM_EXTTS#1 7
EC45
SCD1U25V2ZY-1GP
C17
C14
SC2D2U6D3V3KX-GP
VDD
VSS
DDR2-200P-19-GP-U1
M_CLK_DDR2
M_CLK_DDR#2
C157 DUMMY-C2
C158 DUMMY-C2
put near connector
C33
C32
DUMMY-C2
DM1 use 62.10017.B51
1206 SI
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRII-SODIMM SLOT2
Size Custom
Document Number
Warrior
Rev SC
Date: Monday, January 07, 2008
Sheet 13 of 42

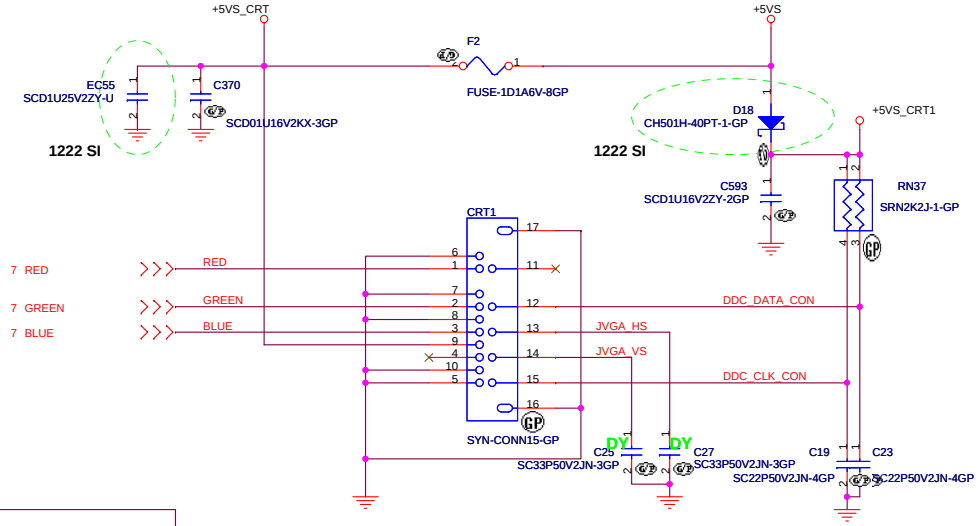
CRT I/F & CONNECTOR

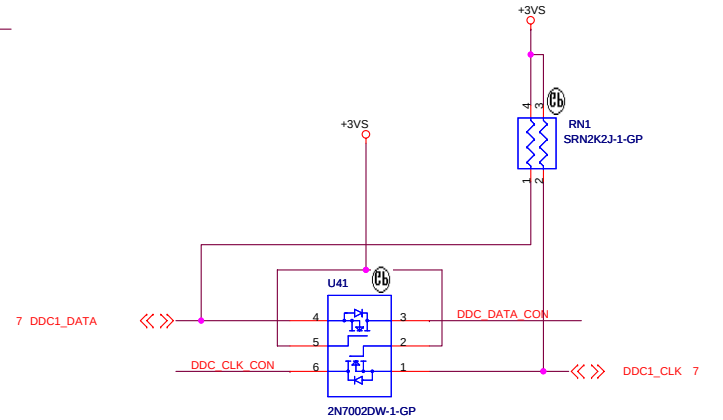






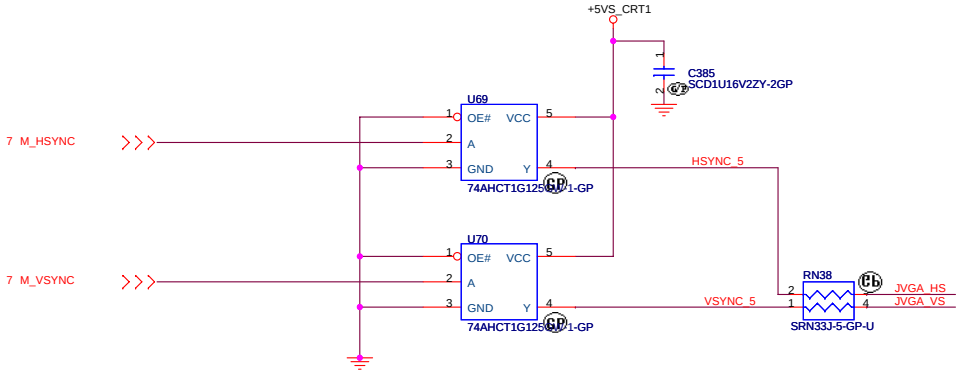






5V @ ext. CRT side

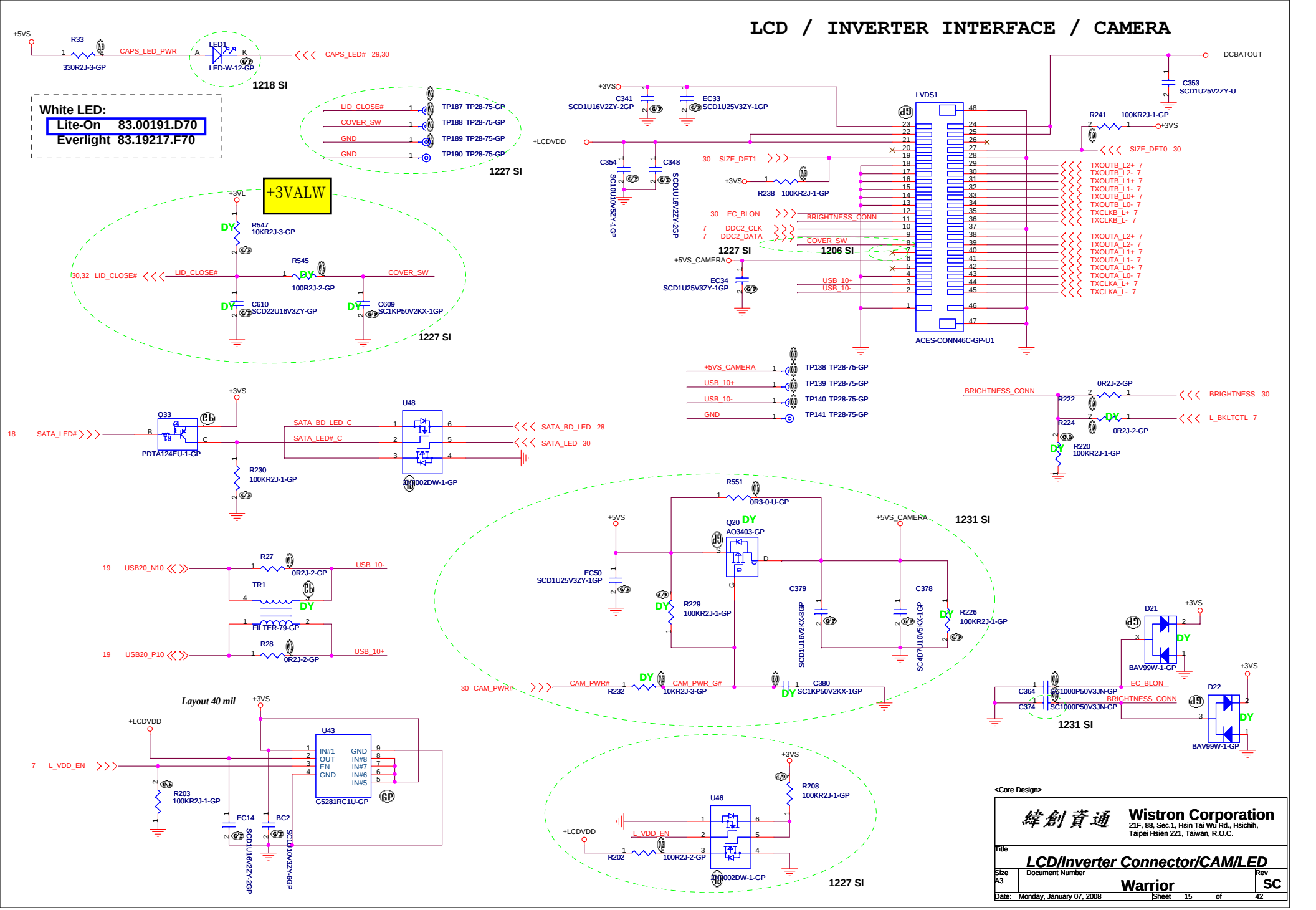
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

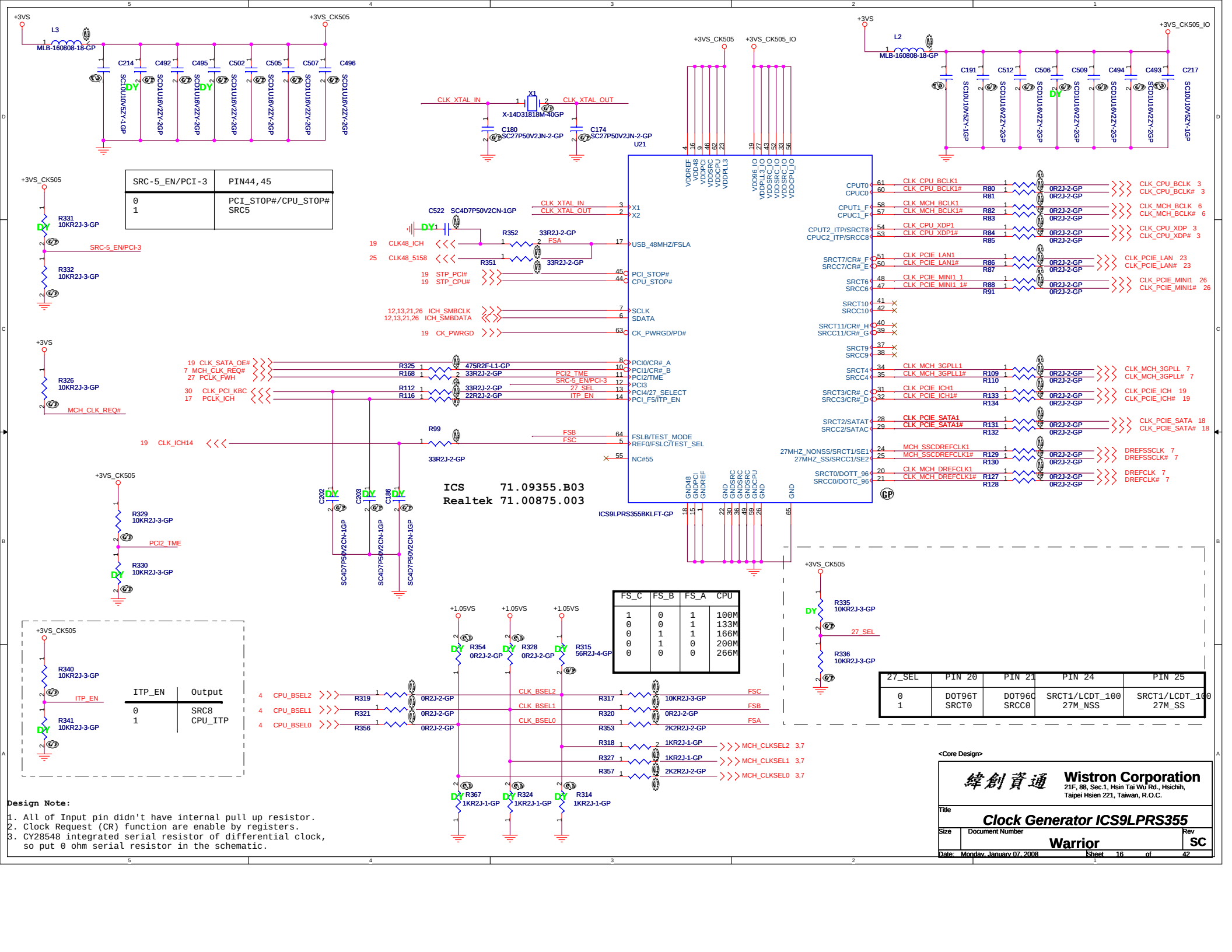


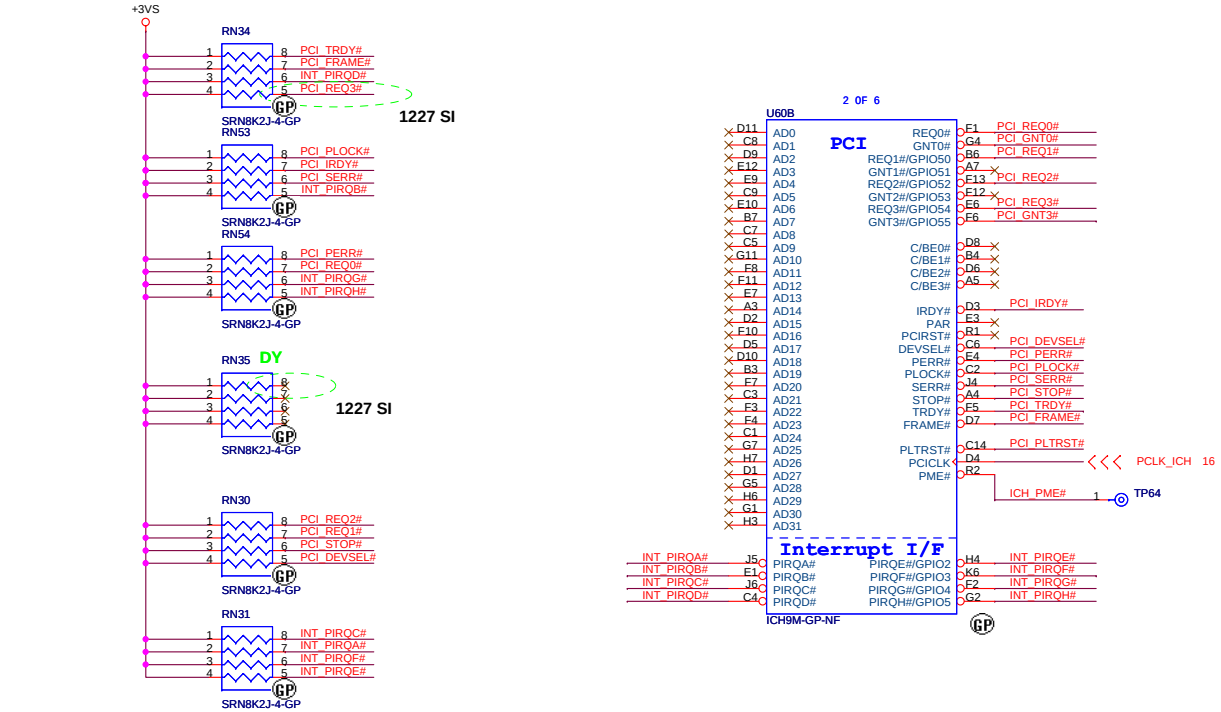
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CRT Connector**
Size: A3	Document Number: **Warrior** — Rev: **SC**
Date: Monday, January 07, 2008	Sheet 14 of 42

LCD / INVERTER INTERFACE / CAMERA




+3VS
+3VS_CK505
+3VS_CK505_IO
L3
MLB-160808-18-GP
L2
C214
C492
C495
C502
C505
C507
C496
C191
C512
C506
C509
C494
C493
C217
SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
DY
X1
X-14D31818M-40GP
CLK_XTAL_IN
CLK_XTAL_OUT
C180
SC27P50V2JN-2-GP
C174
U21
VDDREF
VDD48
VDDPCI
VDDSRC
VDDCPU
VDDPLL3
VDD96_IO
VDDPLL3_IO
VDDSRC_IO
VDDCPU_IO
SRC-5_EN/PCI-3
PIN44,45
0
PCI_STOP#/CPU_STOP#
1
SRC5
R331
10KR2J-3-GP
R332
R326
MCH_CLK_REQ#
C522
SC4D7P50V2CN-1GP
R352
33R2J-2-GP
R351
CLK48_ICH
CLK48_5158
FSA
USB_48MHZ/FSLA
STP_PCI#
STP_CPU#
PCI_STOP#
CPU_STOP#
ICH_SMBCLK
ICH_SMBDATA
SCLK
SDATA
CK_PWRGD
CK_PWRGD/PD#
CLK_SATA_OE#
MCH_CLK_REQ#
PCLK_FWH
CLK_PCI_KBC
PCLK_ICH
R325
R168
R112
R116
475R2F-L1-GP
33R2J-2-GP
22R2J-2-GP
PCI2_TME
SRC-5_EN/PCI-3
27_SEL
ITP_EN
PCI0/CR#_A
PCI1/CR#_B
PCI2/TME
PCI3
PCI4/27_SELECT
PCI_FS/ITP_EN
CLK_ICH14
R99
FSB
FSC
FSLB/TEST_MODE
REF0/FSLC/TEST_SEL
NC#55
ICS 71.09355.B03
Realtek 71.00875.003
ICS9LPRS355BKLFT-GP
R329
R330
C202
C203
C186
SC4D7P50V2CN-1GP
CPU0
CPUC0
CPUT1_F
CPUC1_F
CPUT2_ITP/SRCT8
CPUC2_ITP/SRCC8
SRCT7/CR#_F
SRCC7/CR#_E
SRCT6
SRCC6
SRCT10
SRCC10
SRCT11/CR#_H
SRCC11/CR#_G
SRCT9
SRCC9
SRCT4
SRCC4
SRCT3/CR#_C
SRCC3/CR#_D
SRCT2/SATAT
SRCC2/SATAC
27MHZ_NONSS/SRCT1/SE1
27MHZ_SS/SRCC1/SE2
SRCT0/DOTT_96
SRCC0/DOTC_96
CLK_CPU_BCLK1
CLK_CPU_BCLK1#
CLK_MCH_BCLK1
CLK_MCH_BCLK1#
CLK_CPU_XDP1
CLK_CPU_XDP1#
CLK_PCIE_LAN1
CLK_PCIE_LAN1#
CLK_PCIE_MINI1_1
CLK_PCIE_MINI1_1#
CLK_MCH_3GPLL1
CLK_MCH_3GPLL1#
CLK_PCIE_ICH1
CLK_PCIE_ICH1#
CLK_PCIE_SATA1
CLK_PCIE_SATA1#
MCH_SSCDREFCLK1
MCH_SSCDREFCLK1#
CLK_MCH_DREFCLK1
CLK_MCH_DREFCLK1#
R80
R81
R82
R83
R84
R85
R86
R87
R88
R91
R109
R110
R133
R134
R131
R132
R129
R130
R127
R128
0R2J-2-GP
CLK_CPU_BCLK 3
CLK_CPU_BCLK# 3
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
CLK_CPU_XDP 3
CLK_CPU_XDP# 3
CLK_PCIE_LAN 23
CLK_PCIE_LAN# 23
CLK_PCIE_MINI1 26
CLK_PCIE_MINI1# 26
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
CLK_PCIE_ICH 19
CLK_PCIE_ICH# 19
CLK_PCIE_SATA 18
CLK_PCIE_SATA# 18
DREFSSCLK 7
DREFSSCLK# 7
DREFCLK 7
DREFCLK# 7
GP
R335
R336
27_SEL
27_SEL | PIN 20 | PIN 21 | PIN 24 | PIN 25
0 | DOT96T | DOT96C | SRCT1/LCDT_100 27M_NSS | SRCT1/LCDT_100 27M_SS
1 | SRCT0 | SRCC0
FS_C | FS_B | FS_A | CPU
1 | 0 | 1 | 100M
0 | 0 | 1 | 133M
0 | 1 | 1 | 166M
0 | 1 | 0 | 200M
0 | 0 | 0 | 266M
+1.05VS
R354
R328
R315
56R2J-4-GP
CPU_BSEL2
CPU_BSEL1
CPU_BSEL0
R319
R321
R356
R317
R320
R353
10KR2J-3-GP
2K2R2J-2-GP
FSC
FSB
FSA
R318
R327
R357
1KR2J-1-GP
MCH_CLKSEL2 3,7
MCH_CLKSEL1 3,7
MCH_CLKSEL0 3,7
R367
R324
R314
R340
R341
ITP_EN
ITP_EN | Output
0 | SRC8
1 | CPU_ITP
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator ICS9LPRS355
Size
Document Number
Warrior
Rev
SC
Date: Monday, January 07, 2008
Sheet 16 of 42



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

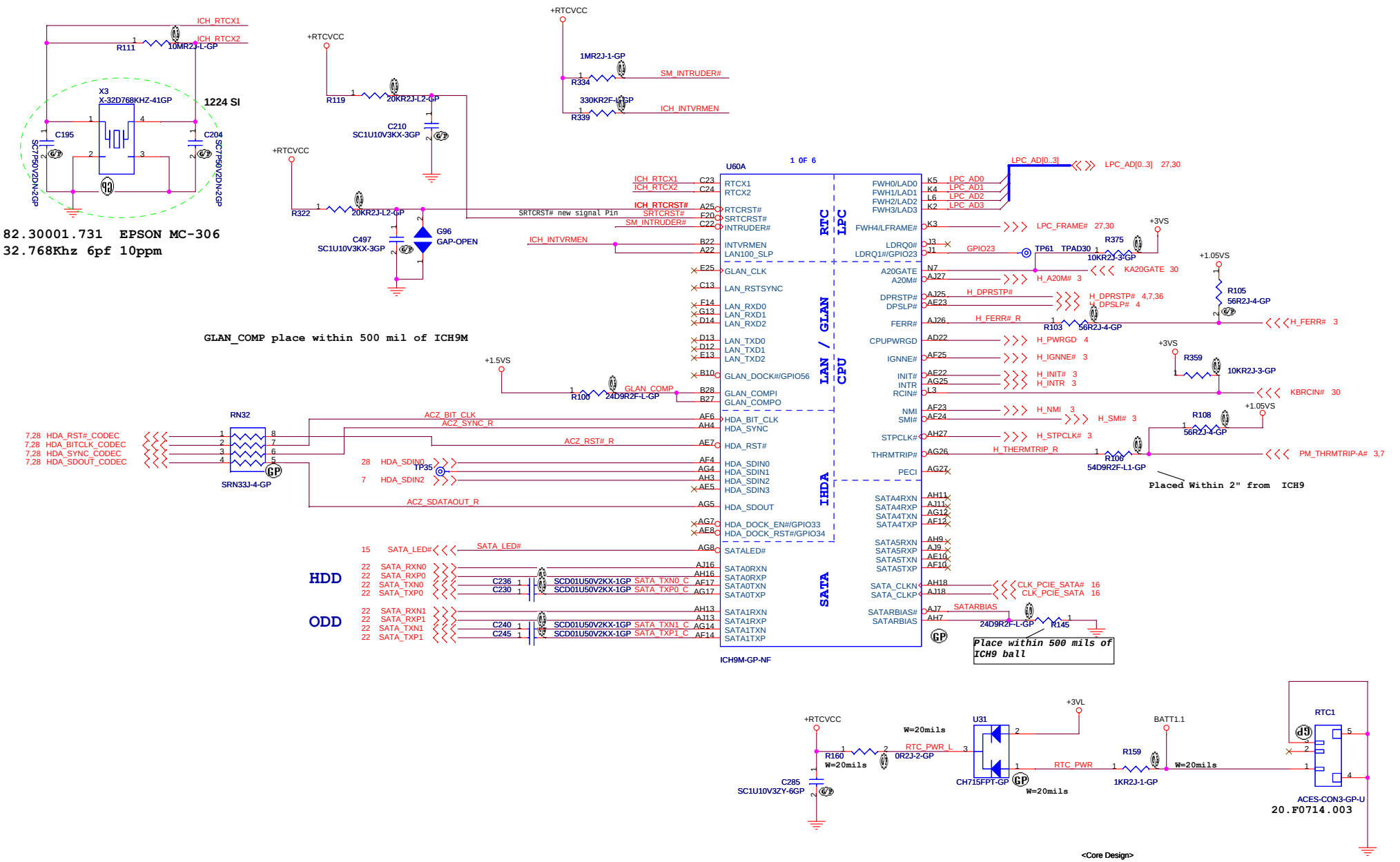
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 5)

Size | Document Number: Warrior | Rev: SC

Date: Monday, January 07, 2008 | Sheet 17 of 42



integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

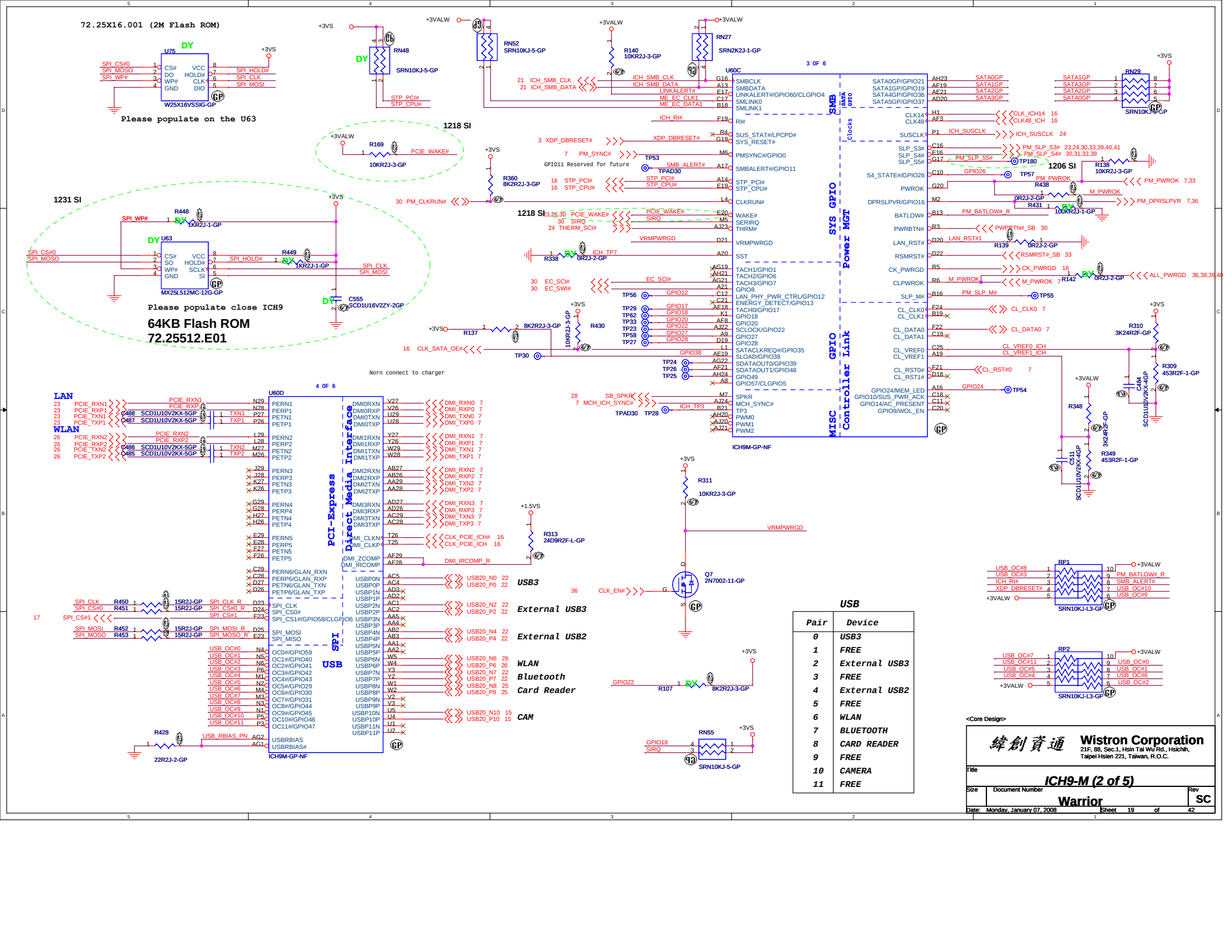
<Core Design>

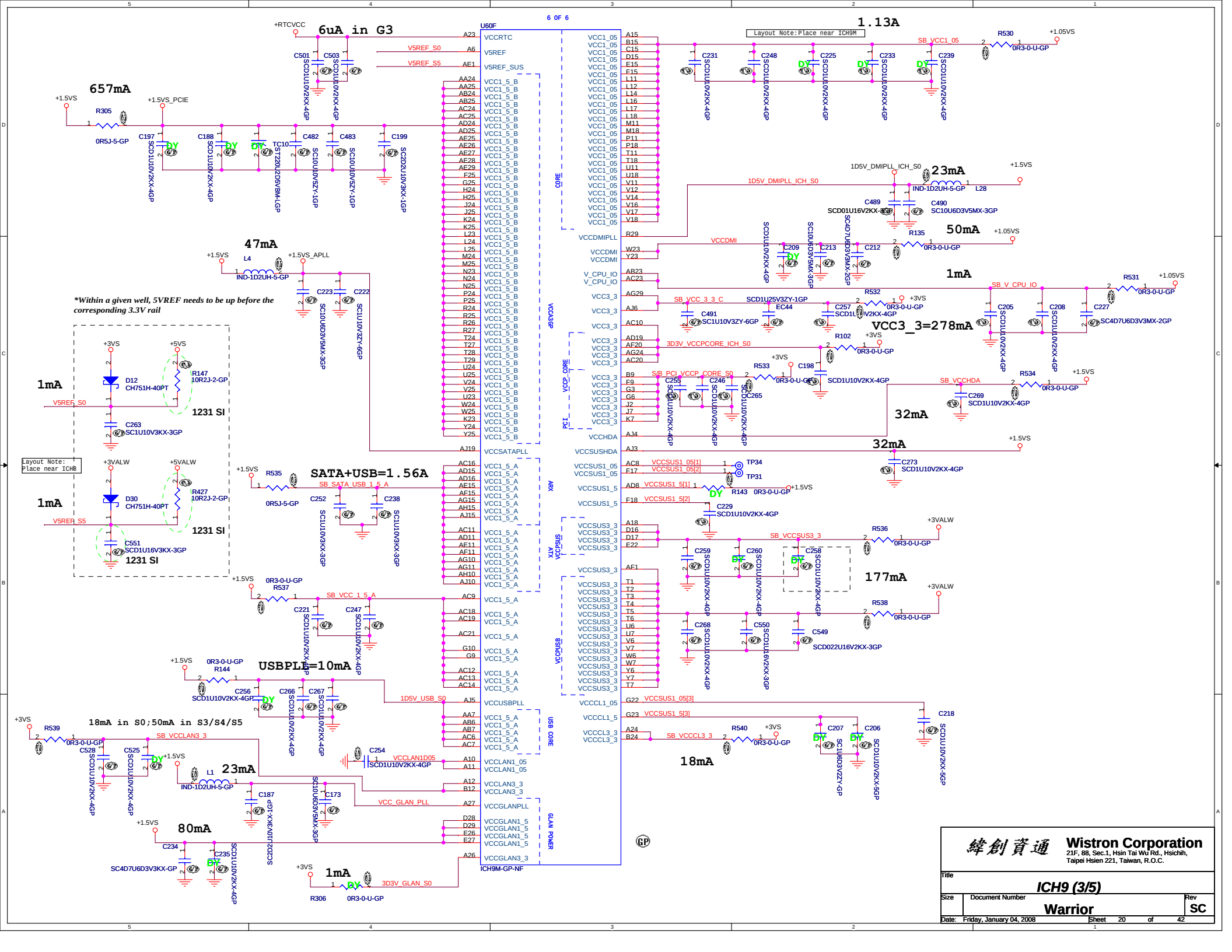
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (2 of 5)

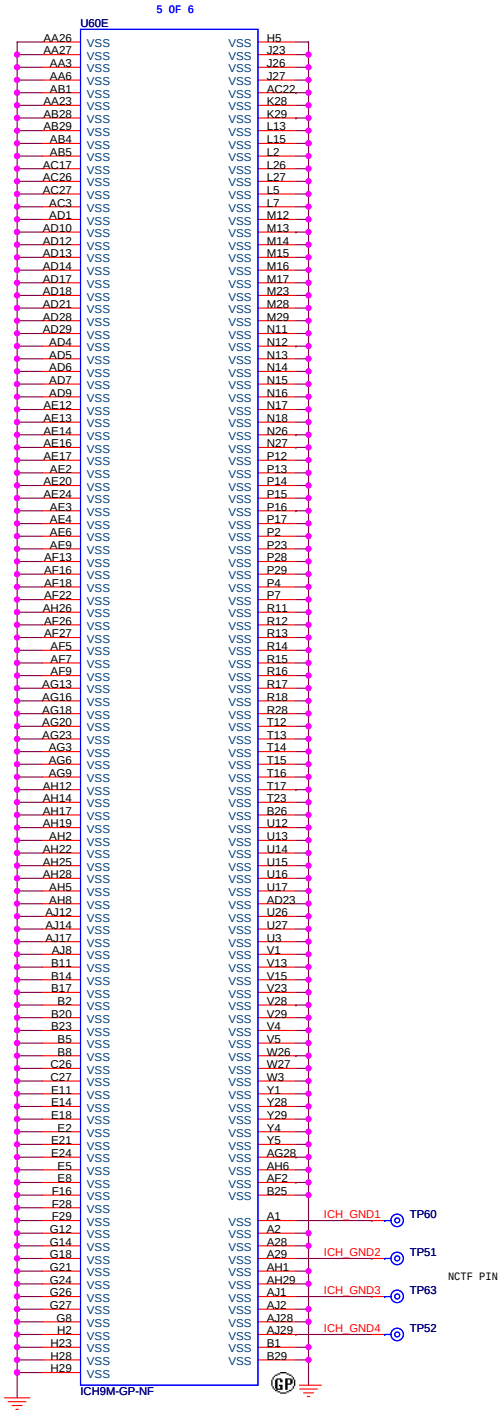
Size	Document Number	Rev
	Warrior	SC

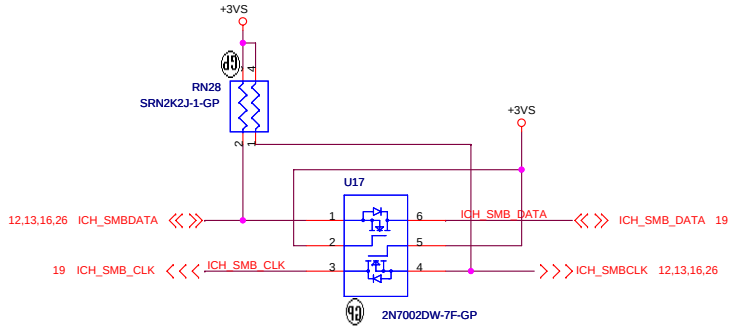
Date: Monday, January 07, 2008 Sheet 18 of 42


72.25X16.001 (2M Flash ROM)
U75
W25X16VSSIG-GP
Please populate on the U63
1218 SI
1231 SI
U63
MX25L512MC-12G-GP
Please populate close ICH9
64KB Flash ROM
72.25512.E01
Norn connect to charger
4 OF 6
U60D
ICH9M-GP-NF
PCI-Express
Direct Media Interface
SPI
USB
LAN
WLAN
USB3
External USB3
External USB2
WLAN
Bluetooth
Card Reader
CAM
3 OF 6
U60C
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
USB
Pair
Device
0
USB3
1
FREE
2
External USB3
3
FREE
4
External USB2
5
FREE
6
WLAN
7
BLUETOOTH
8
CARD READER
9
FREE
10
CAMERA
11
FREE
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 5)
Size
Document Number
Warrior
Rev
SC
Date: Monday, January 07, 2008
Sheet 19 of 42



緯創資通	**Wistron Corporation**		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	*ICH9 (3/5)*		
Size	Document Number: **Warrior**	Rev: SC	
Date: Friday, January 04, 2008	Sheet 20 of 42		





SMBUS

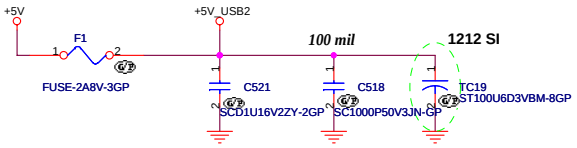
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

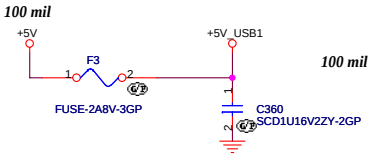
Title: ICH9-M (4 of 4)

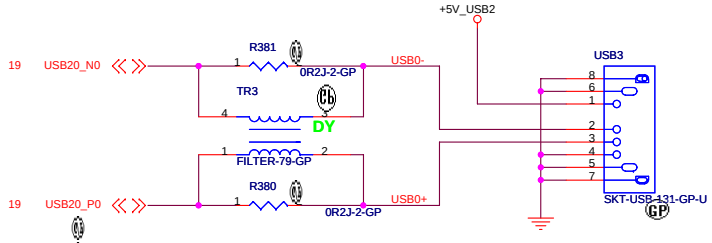
Size	Document Number	Rev
	Warrior	SC

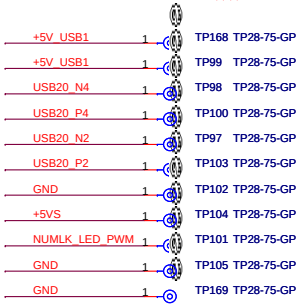
Date: Monday, January 07, 2008 Sheet 21 of 42

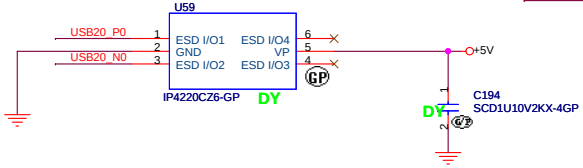
USB PORT

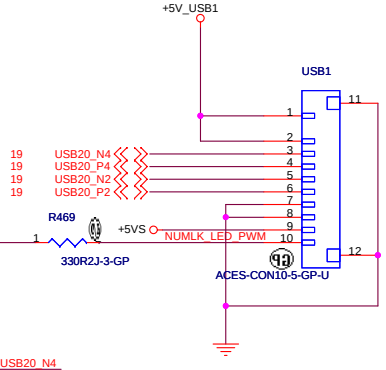




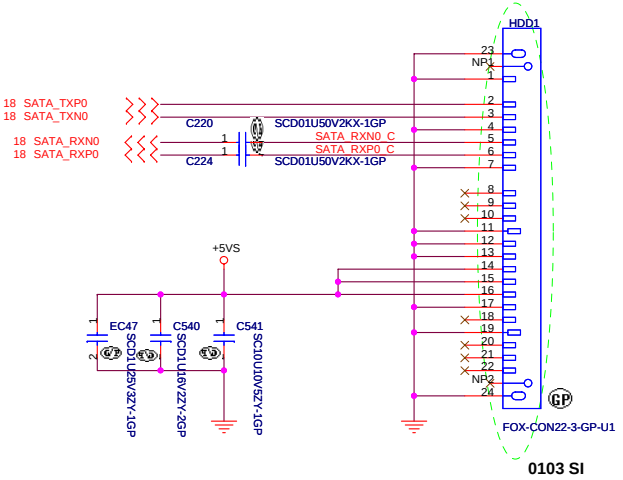




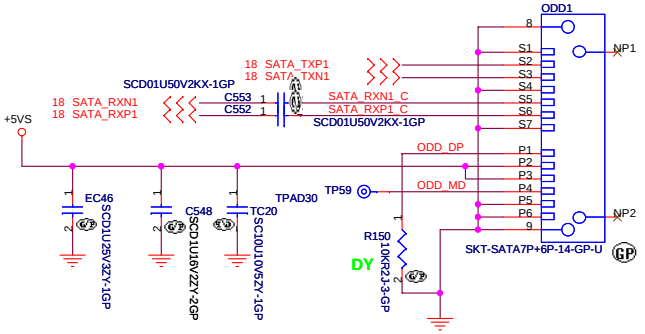




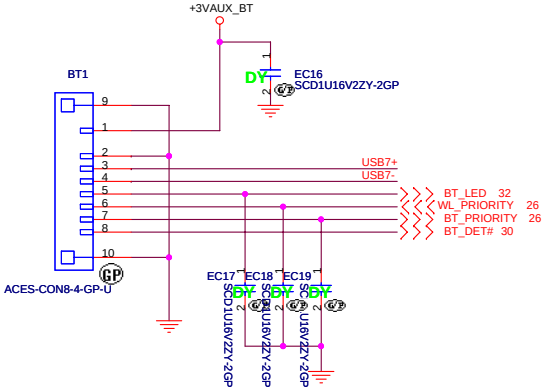
SATA HD Connector

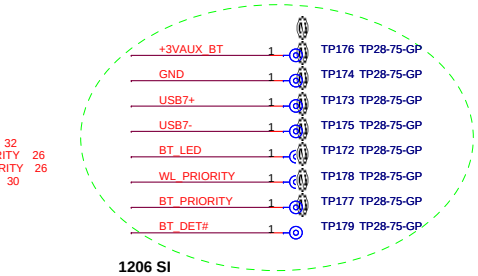


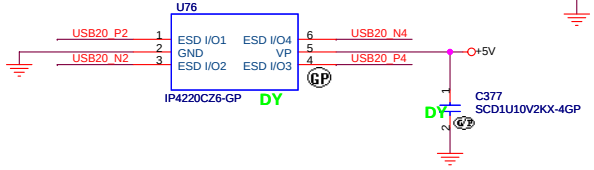
ODD Connector

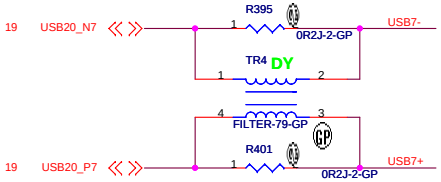


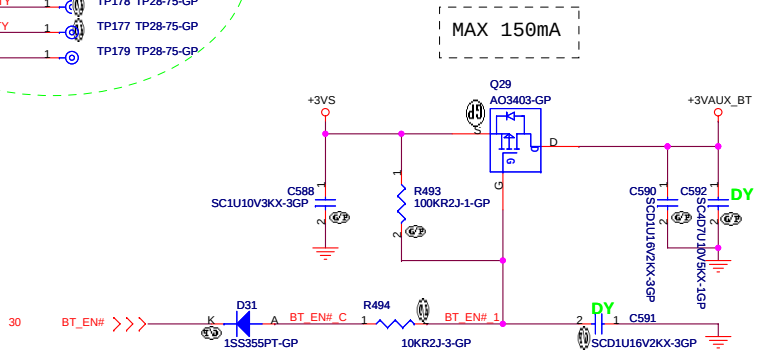
BLUETOOTH











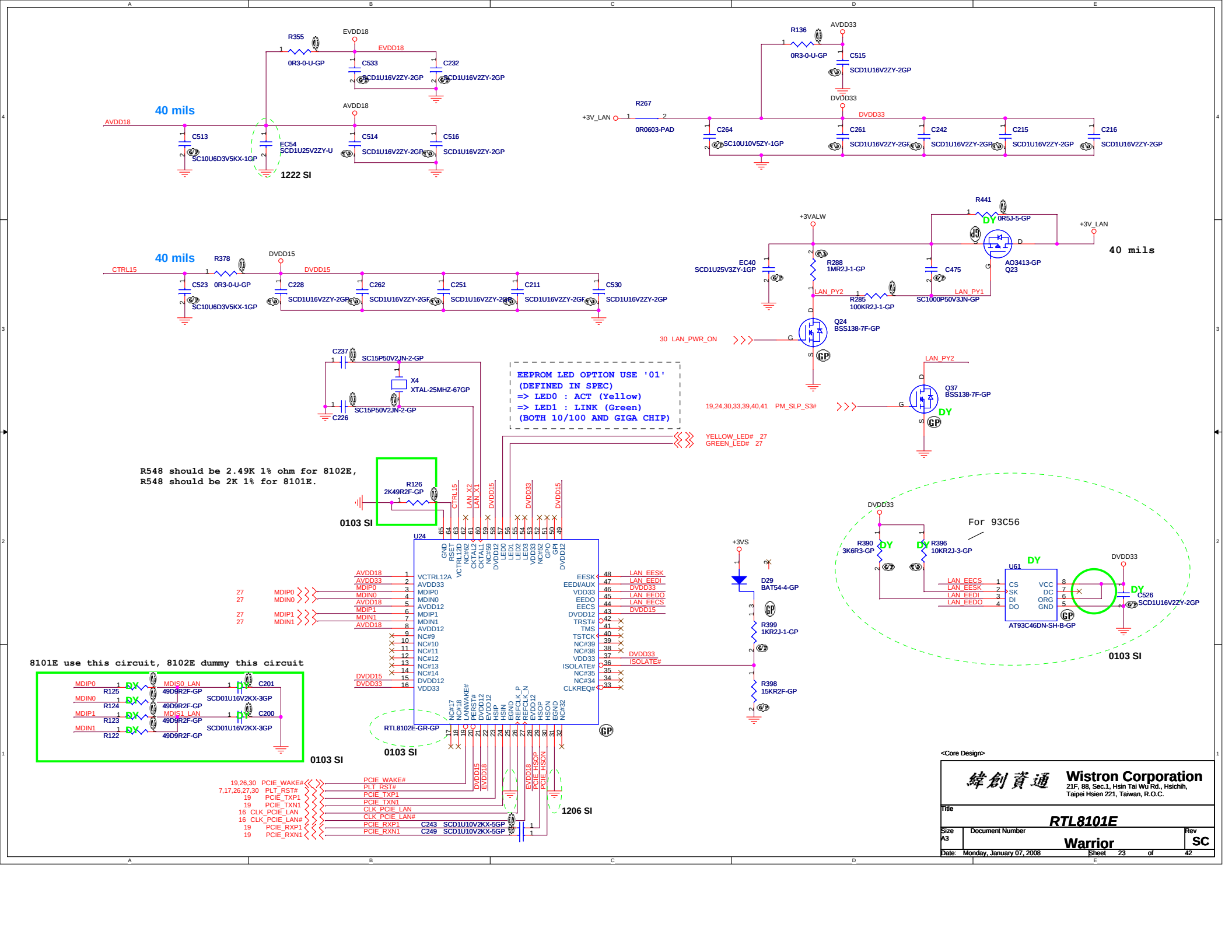
<Core Design>

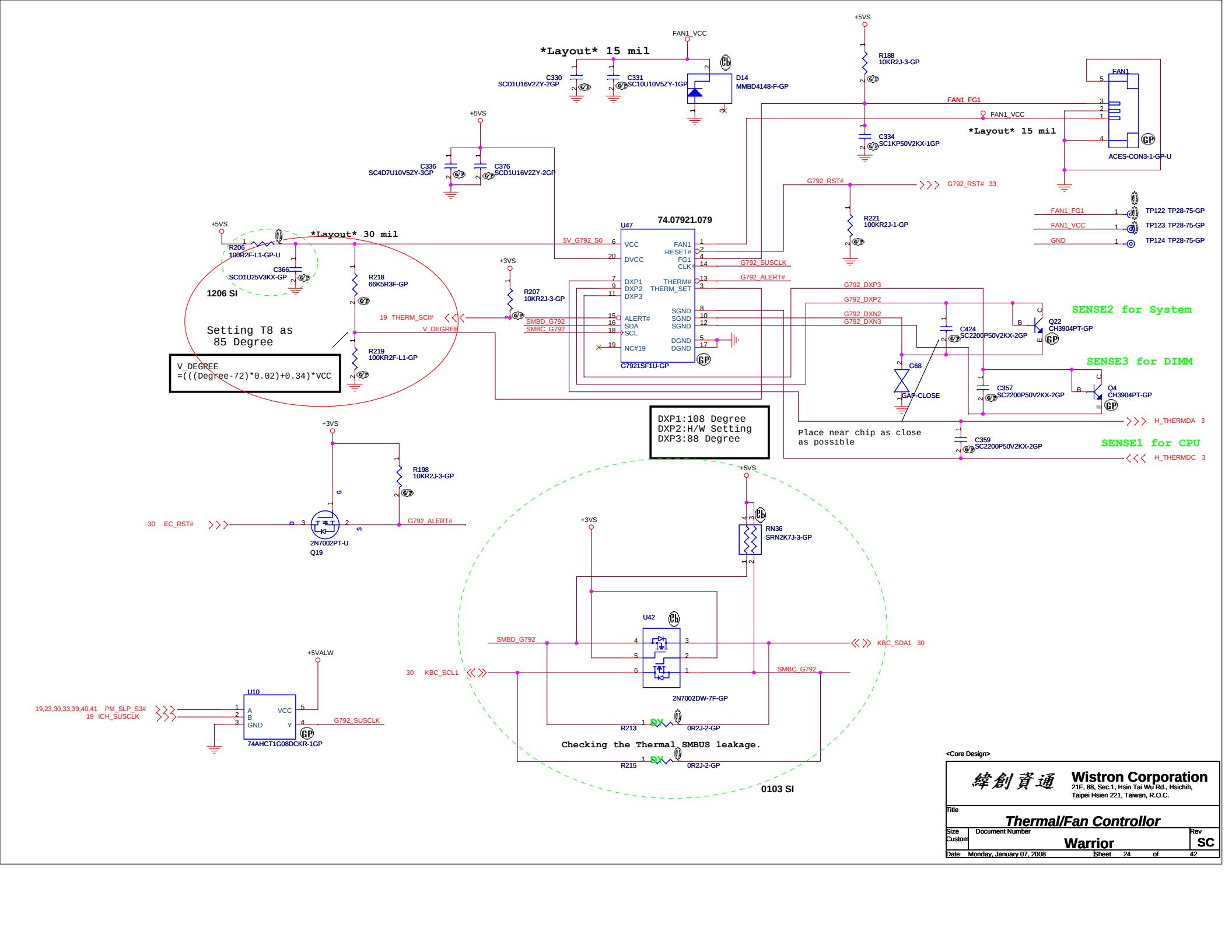
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/CDROM/USB/BT**

Size	Document Number	Rev
A3	Warrior	SC

Date: Monday, January 07, 2008 Sheet 22 of 42


40 mils
1222 SI
40 mils
40 mils
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT (Yellow)
=> LED1 : LINK (Green)
(BOTH 10/100 AND GIGA CHIP)
R548 should be 2.49K 1% ohm for 8102E,
R548 should be 2K 1% for 8101E.
0103 SI
8101E use this circuit, 8102E dummy this circuit
0103 SI
0103 SI
1206 SI
For 93C56
0103 SI
RTL8102E-GR-GP
AT93C46DN-SH-B-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RTL8101E
Warrior
Monday, January 07, 2008



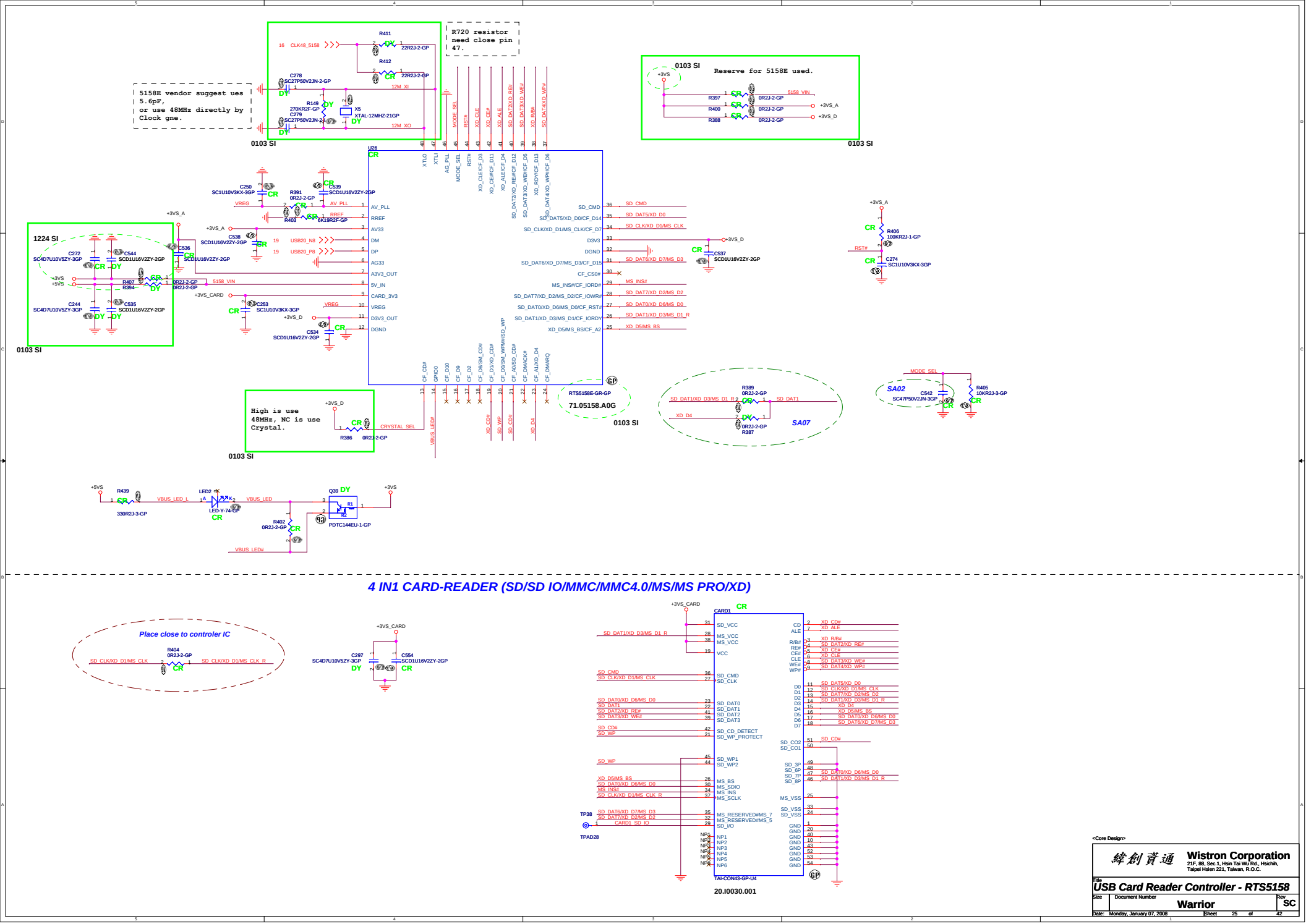
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

Size	Document Number	Rev
Custom	Warrior	SC

Date: Monday, January 07, 2008 Sheet 24 of 42



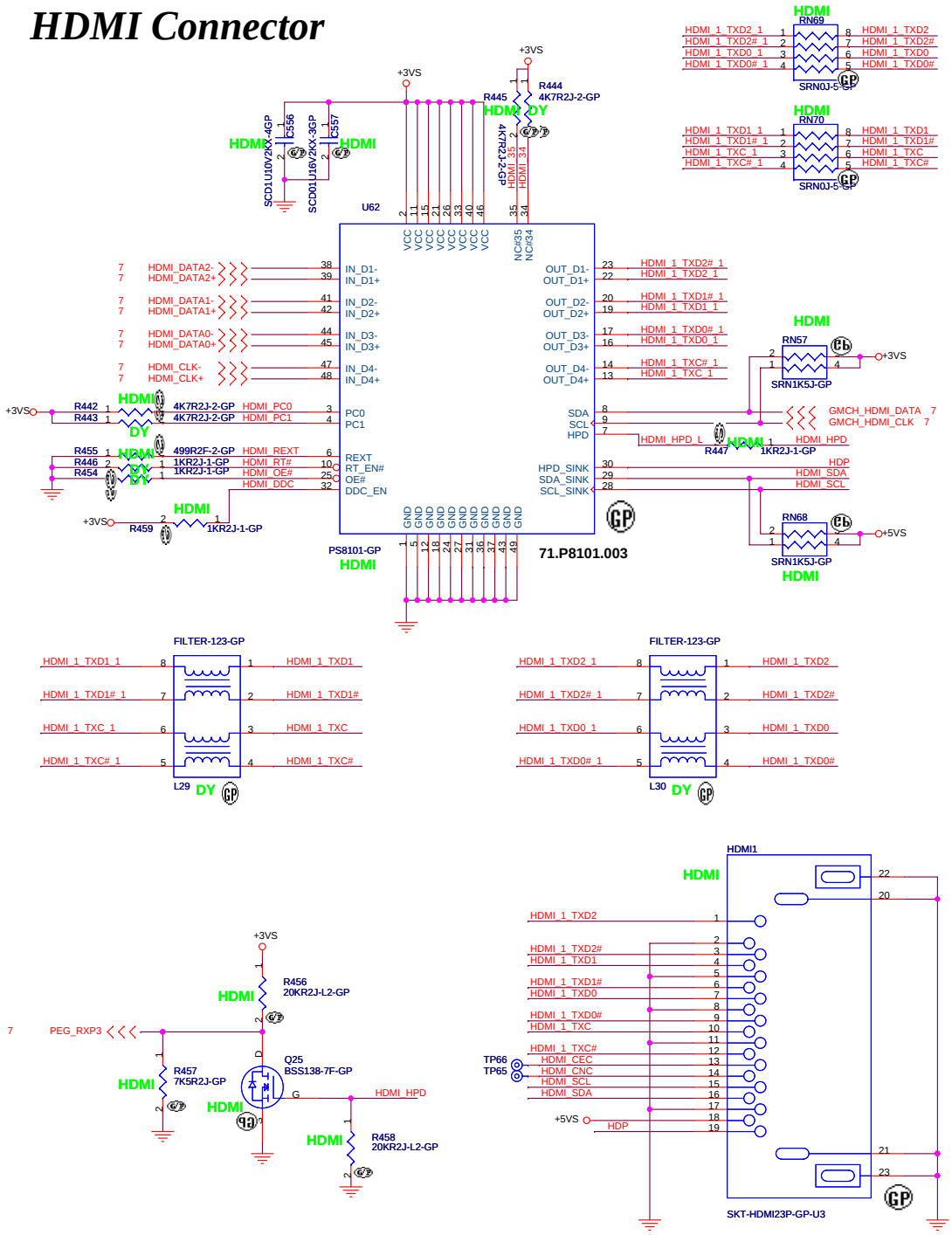
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Card Reader Controller - RTS5158

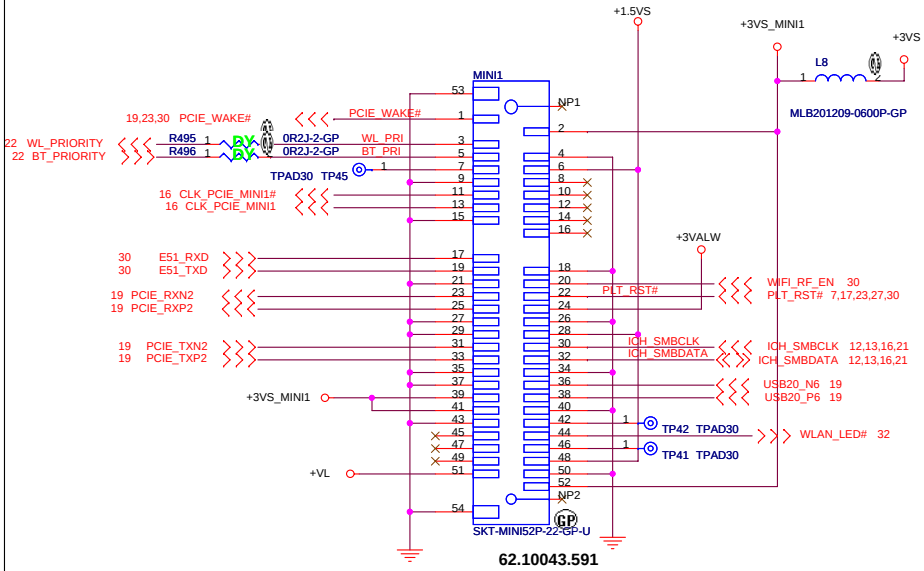
Size: | Document Number: Warrior | Rev: SC

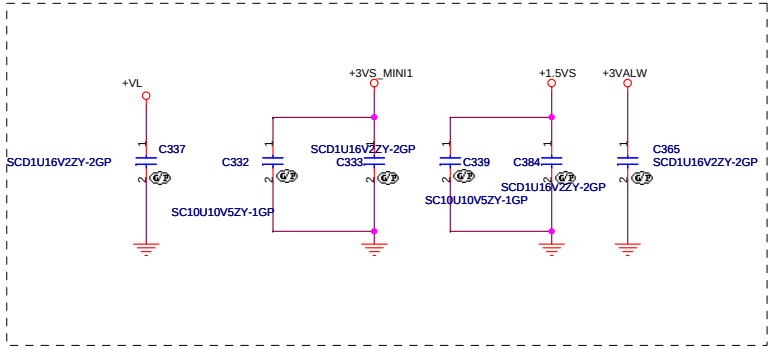
Date: Monday, January 07, 2008 | Sheet 25 of 42

HDMI Connector



Mini Card Connector1(802.11a/b/g)





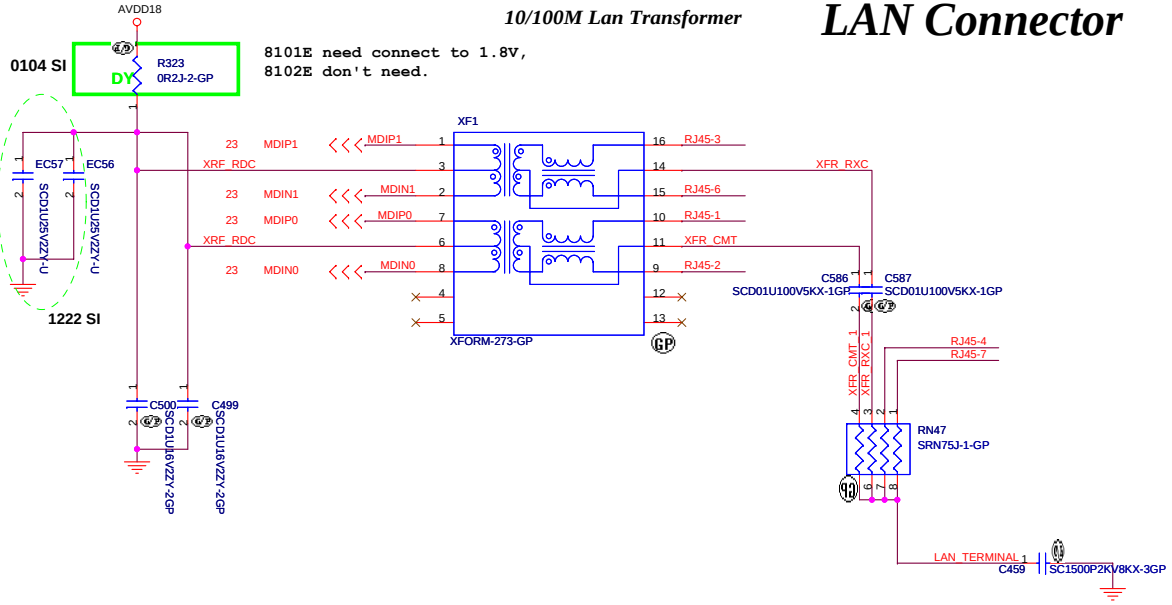
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINI CARD/HDMI CONN .***
Size A3 / Document Number	**Warrior** / Rev **SC**
Date: Monday, January 07, 2008	Sheet 26 of 42

LAN Connector

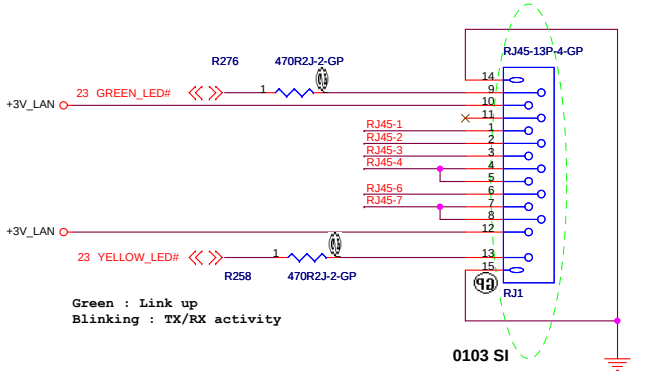
10/100M Lan Transformer

8101E need connect to 1.8V,
8102E don't need.



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Remark:
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.

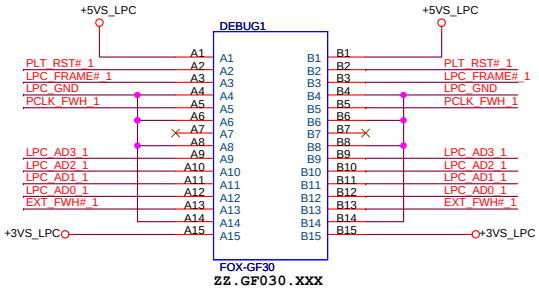
Golden Finger for Debug Board

TOP VIEW (A)

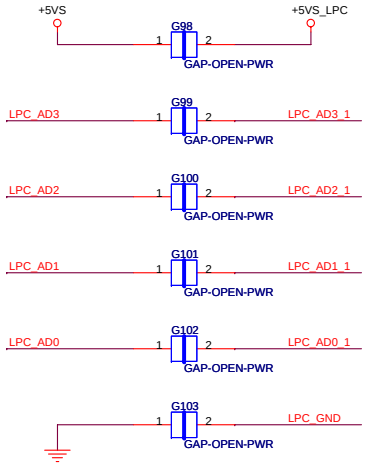
A15 (B1)
A14 (B2)
. .
. .
. .
A2 (B14)
A1 (B15)

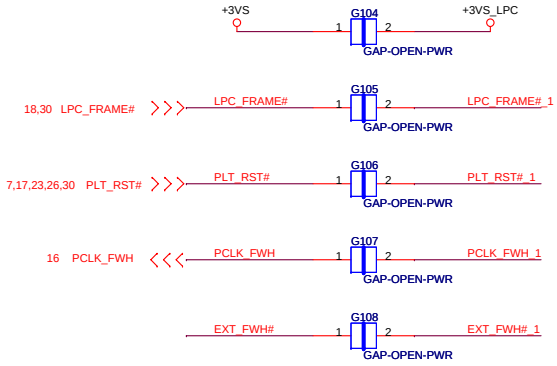
BOTTOM VIEW (B)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



Please put near board edge.





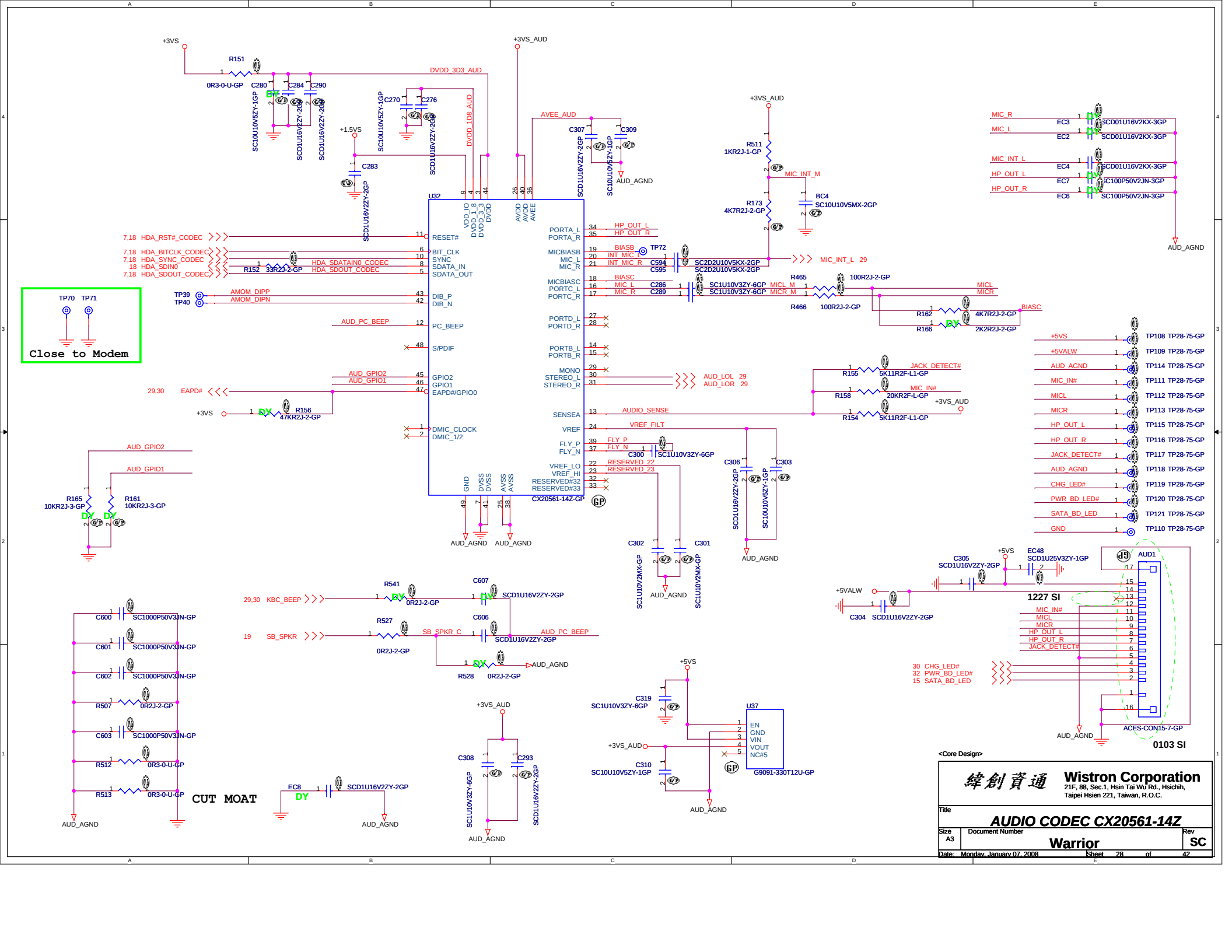
LPC_AD[0..3] 18,30

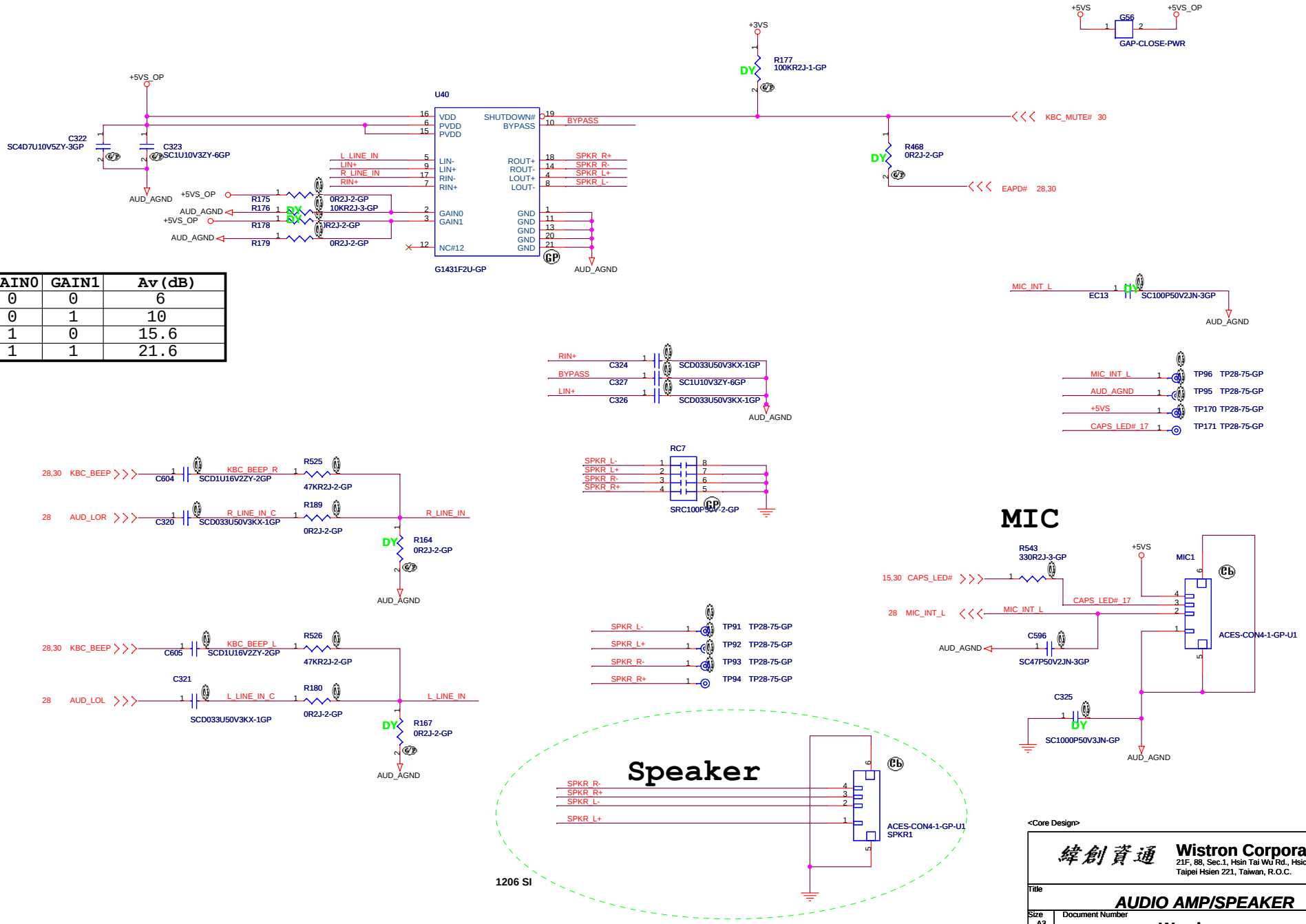
CLOSE TO TRANSFORMER

<Core Design>

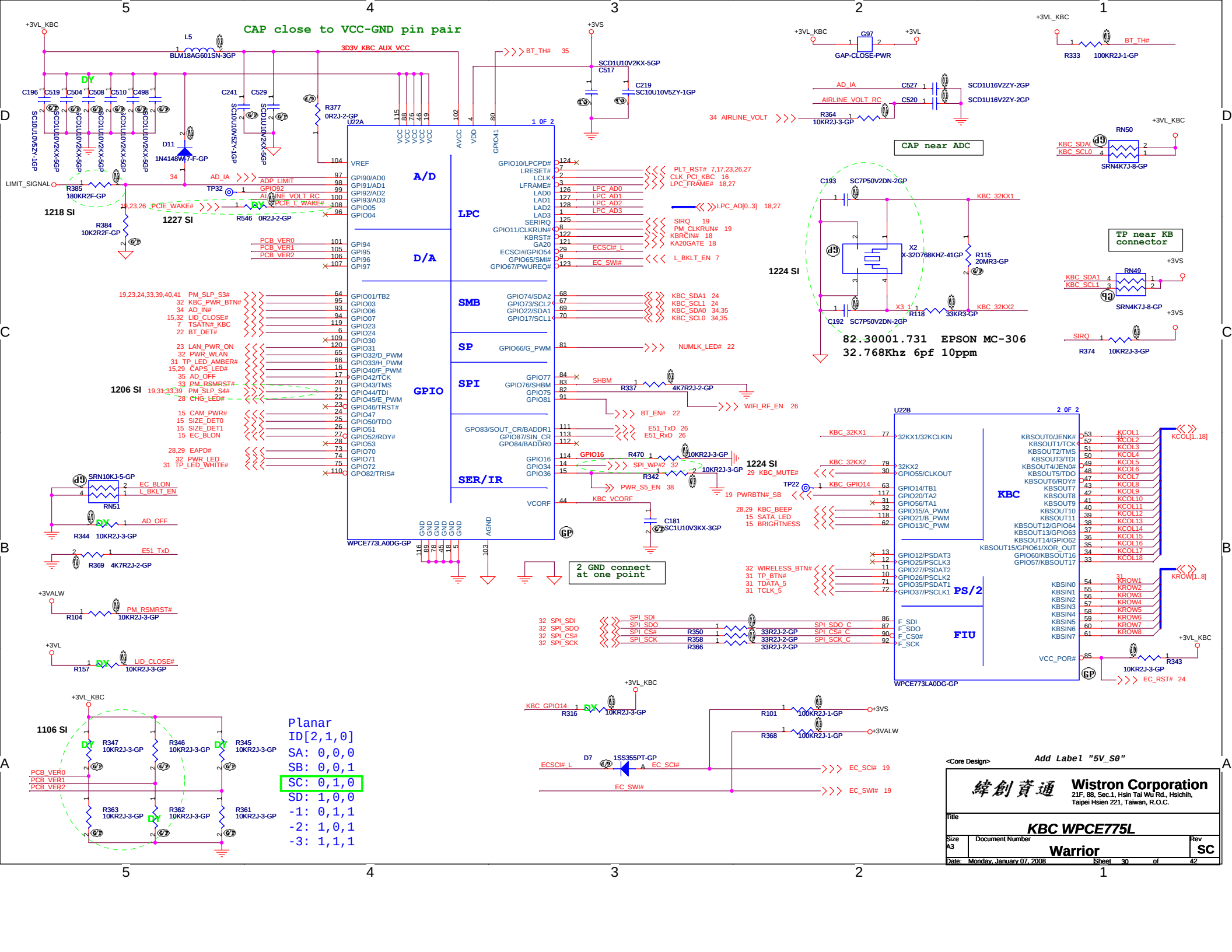
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN/Debug
Size: A3 | Document Number: Warrior | Rev: SC
Date: Monday, January 07, 2008 | Sheet 27 of 42

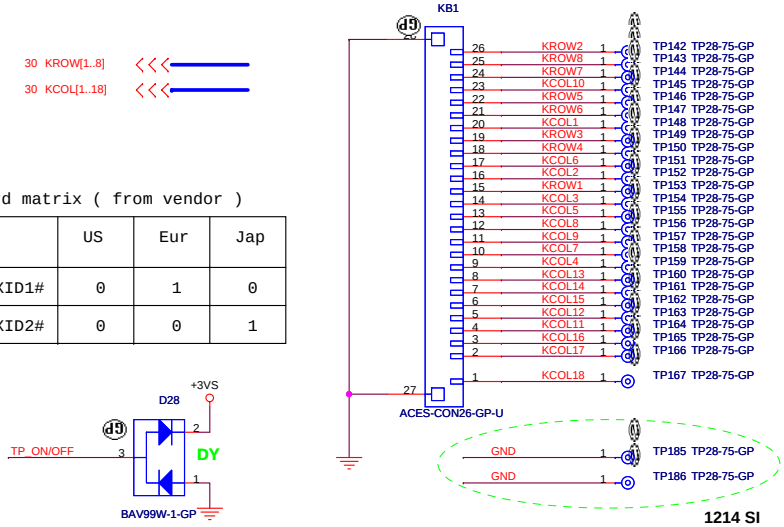

Close to Modem
CUT MOAT
U32
CX20561-14Z-GP
U37
G9091-330T12U-GP
AUD1
ACES-CON15-7-GP
1227 SI
0103 SI
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CODEC CX20561-14Z
Warrior
SC
Monday, January 07, 2008
Sheet 28 of 42



GAIN0	GAIN1	Av(dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6


CAP close to VCC-GND pin pair
U22A
1 0F 2
WPCE773LA0DG-GP
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
2 GND connect at one point
CAP near ADC
TP near KB connector
82.30001.731 EPSON MC-306
32.768Khz 6pf 10ppm
U22B
2 0F 2
KBC
PS/2
FIU
1224 SI
1218 SI
1227 SI
1206 SI
1106 SI
Planar
ID[2,1,0]
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 1,0,0
-1: 0,1,1
-2: 1,0,1
-3: 1,1,1
Add Label "5V_S0"
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPCE775L
Warrior
Monday, January 07, 2008
30
42

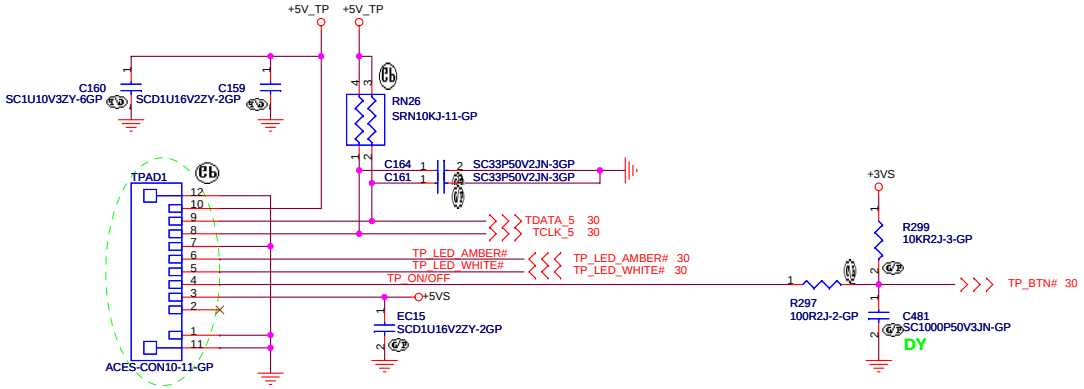
Internal KeyBoard Connector

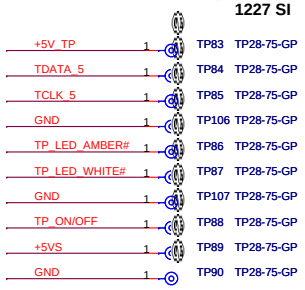


Keyboard matrix (from vendor)

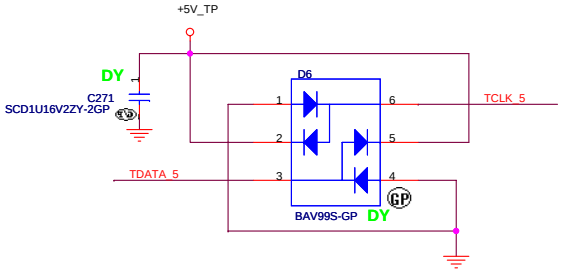
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

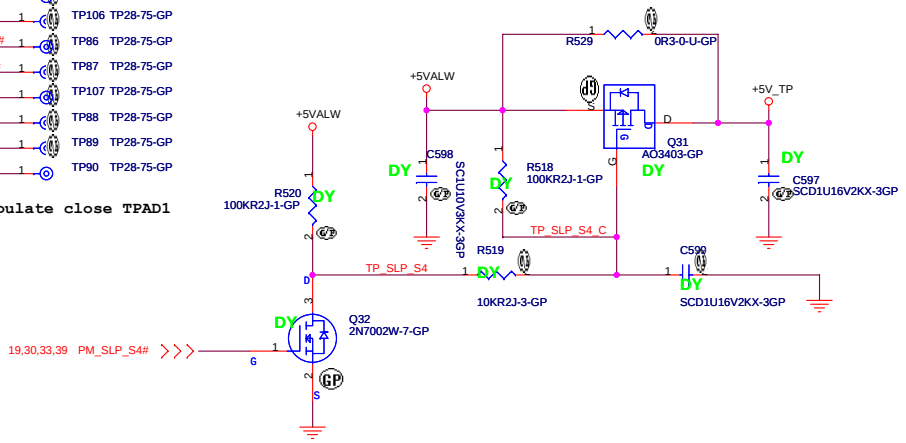
TouchPad Connector

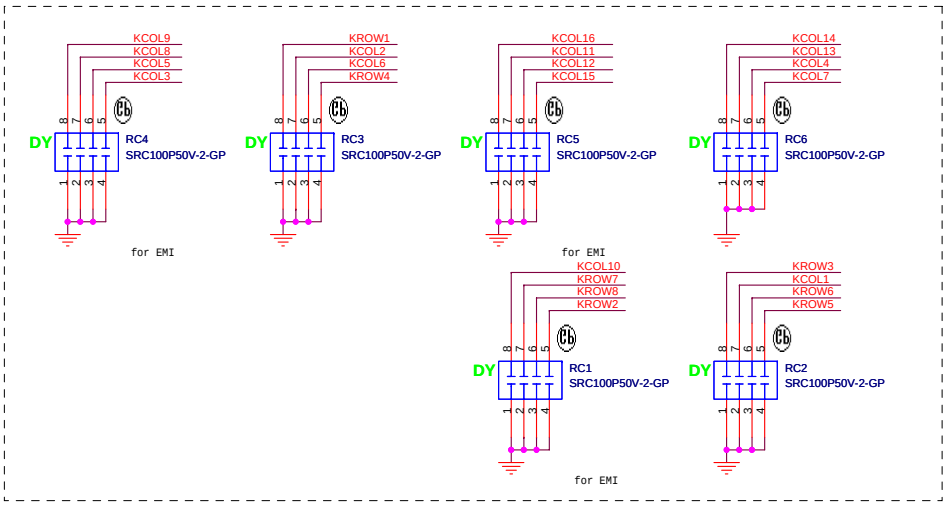




Please populate close TPAD1







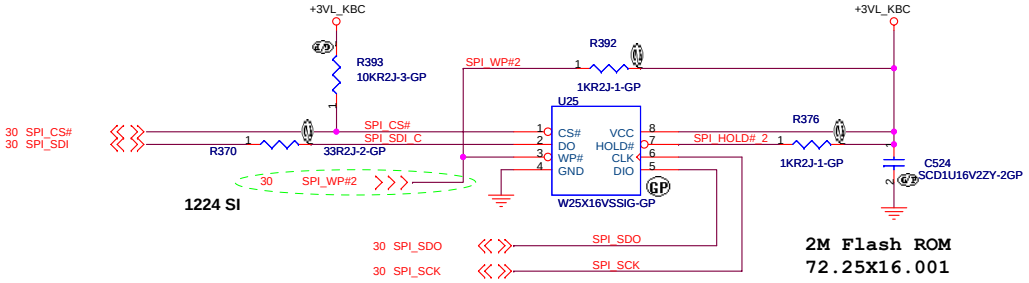
<Core Design>

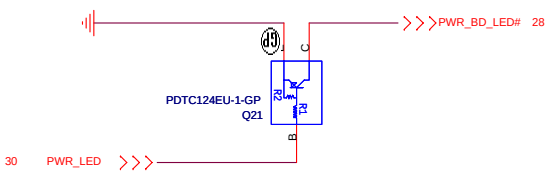
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

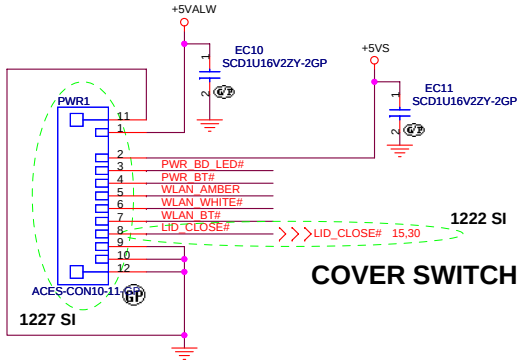
Title: KeyBoard-CONN

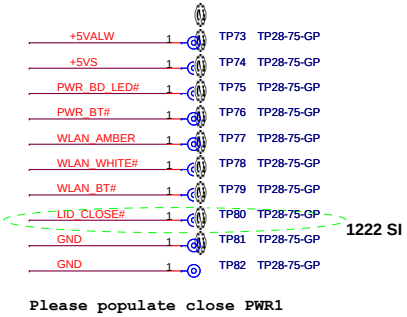
Size: A3 | Document Number: Warrior | Rev: SC

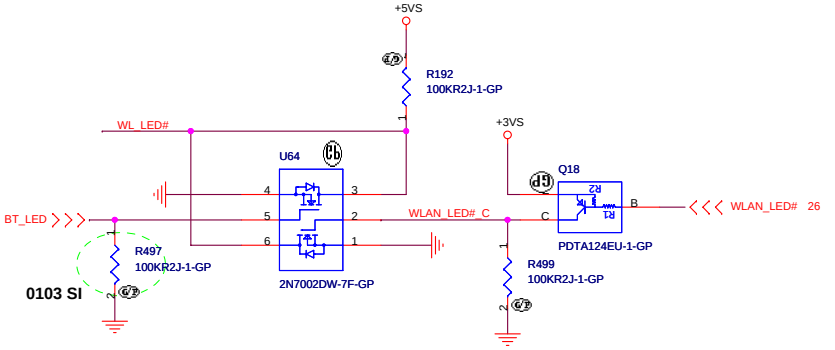
Date: Monday, January 07, 2008 | Sheet 31 of 42

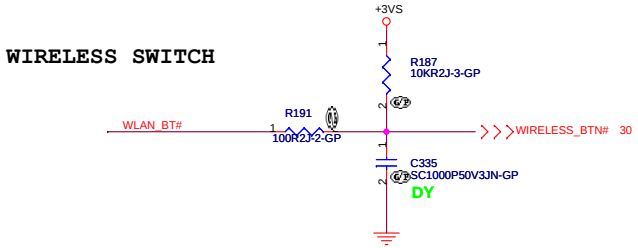


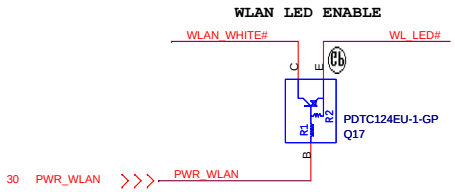


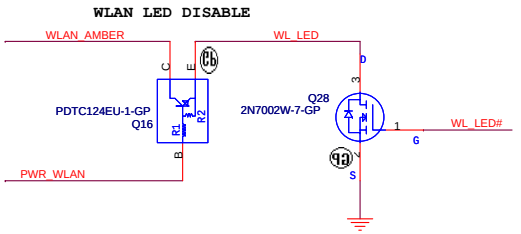


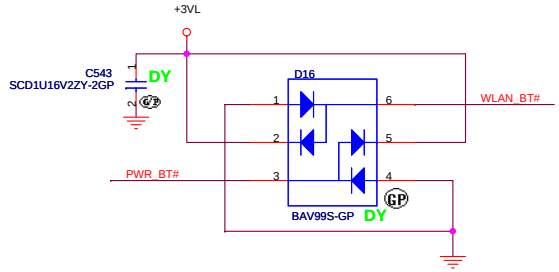


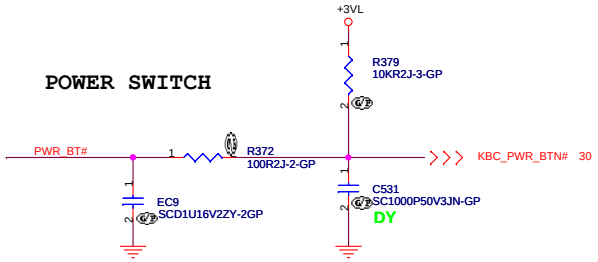






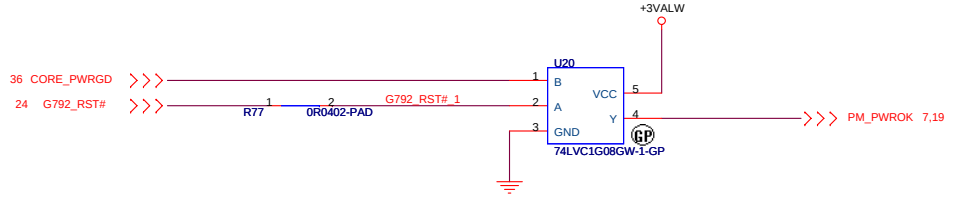


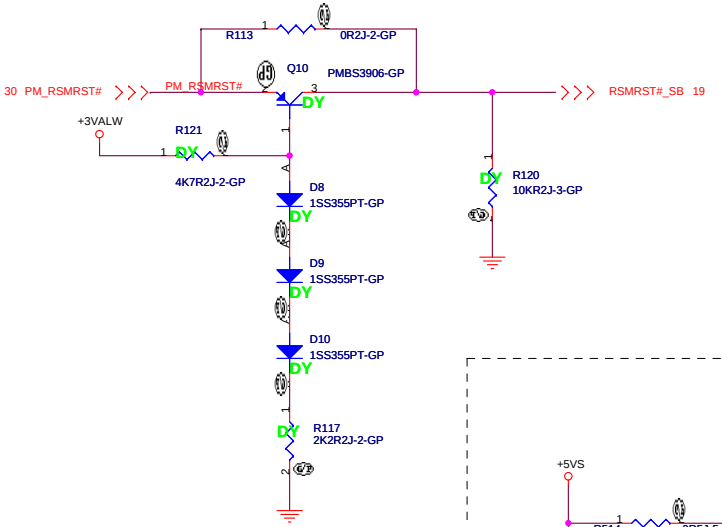




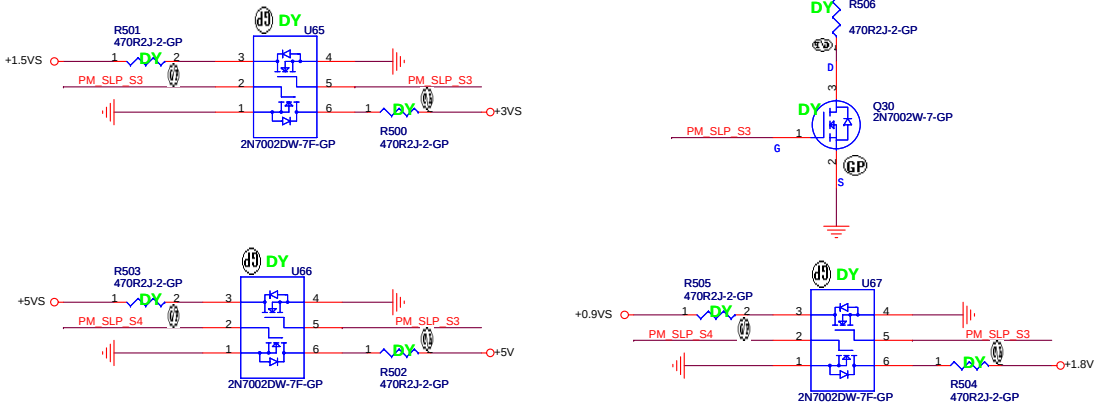
<Core Design>

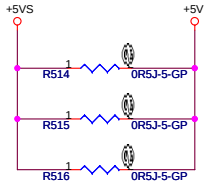
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***FWH and CONN.***	
Size A3	Document Number **Warrior**	Rev **SC**
Date: Monday, January 07, 2008	Sheet 32 of 42	





Discharge Circuit



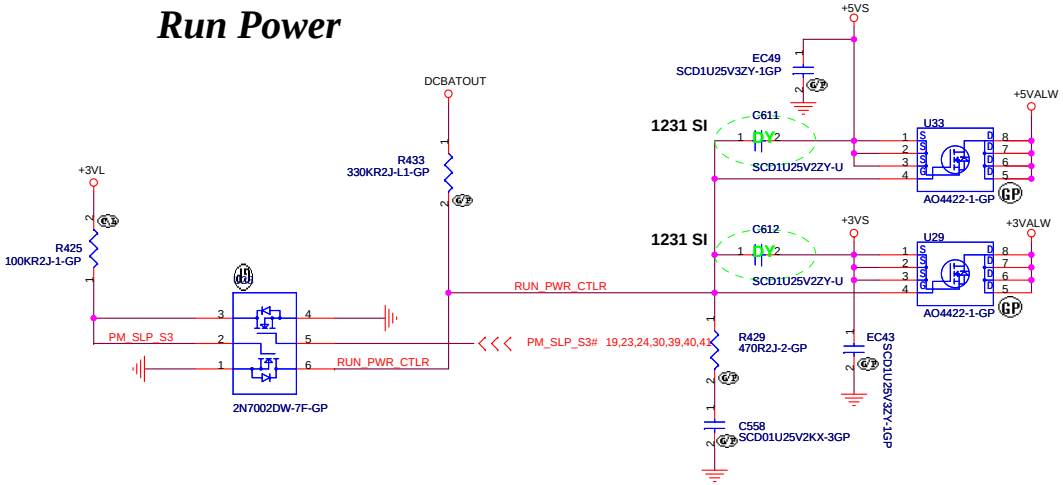


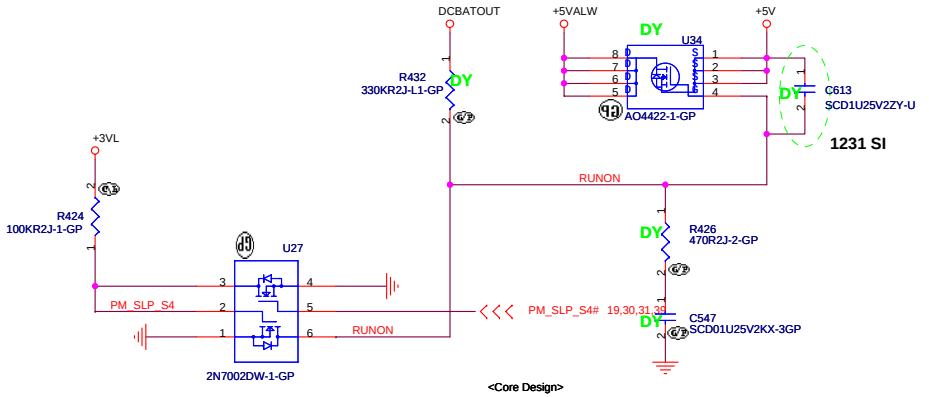
Populate close U34

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer

+5VALW to +5V Transfer

Run Power





<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PWRPLANE		
Size: A3	Document Number: Warrior	Rev: SC
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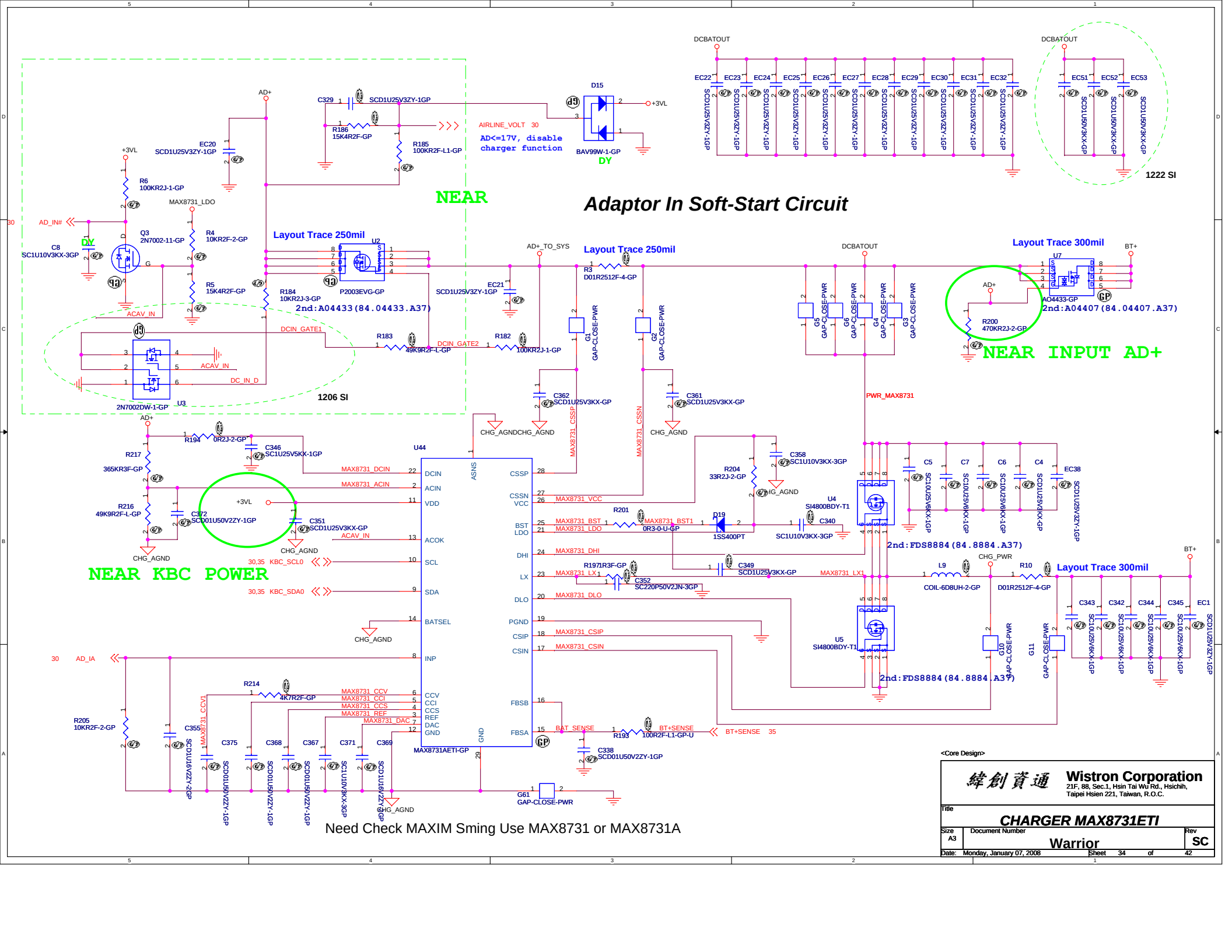
Adaptor In Soft-Start Circuit
NEAR
AIRLINE_VOLT 30
AD<=17V, disable charger function
BAV99W-1-GP
DY
Layout Trace 250mil
2nd:A04433(84.04433.A37)
P2003EVG-GP
1206 SI
2N7002DW-1-GP
Layout Trace 300mil
AO4433-GP
2nd:A04407(84.04407.A37)
NEAR INPUT AD+
PWR_MAX8731
NEAR KBC POWER
MAX8731AETI-GP
SI4800BDY-T1
1SS400PT
COIL-6D8UH-2-GP
2nd:FDS8884(84.8884.A37)
Need Check MAXIM Sming Use MAX8731 or MAX8731A
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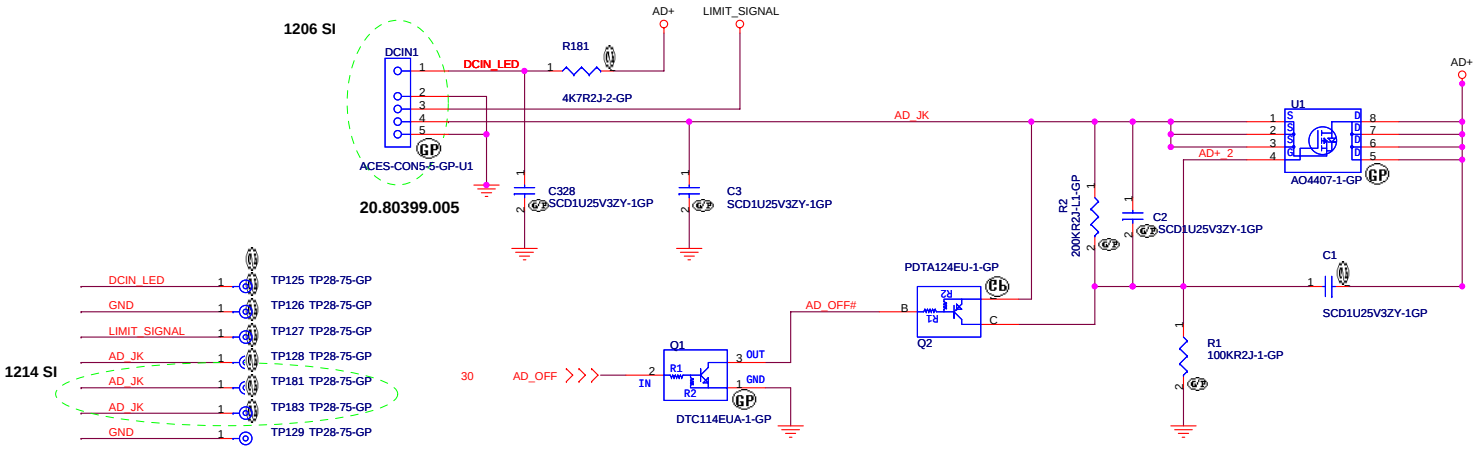
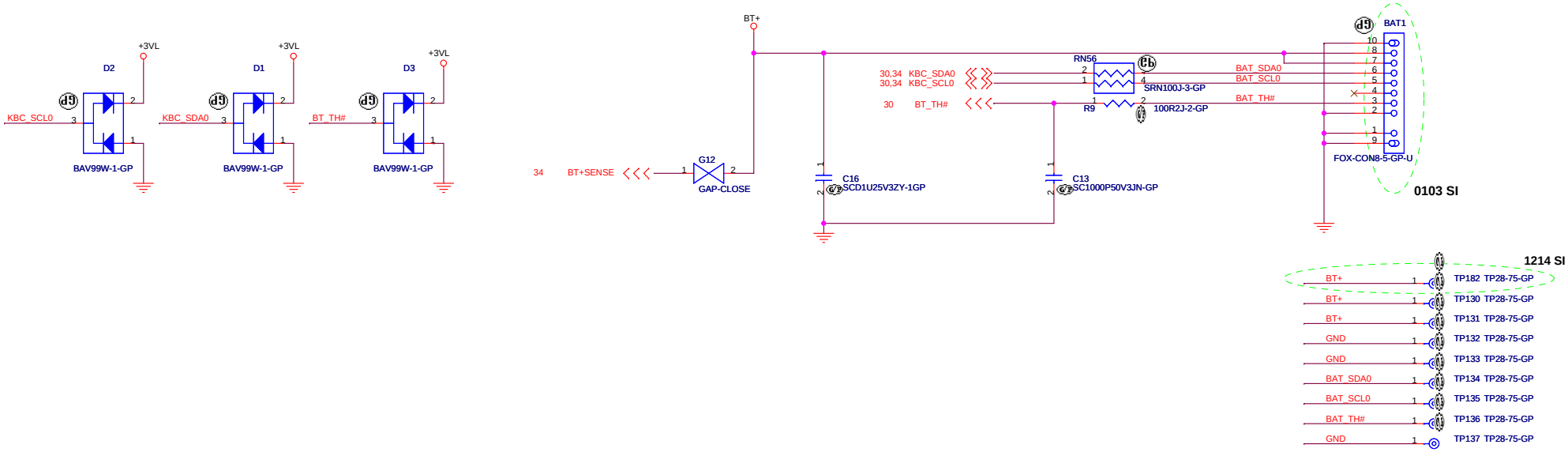
CHARGER MAX8731ETI
Warrior
Monday, January 07, 2008

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Title: ***AD/BATT CONN***

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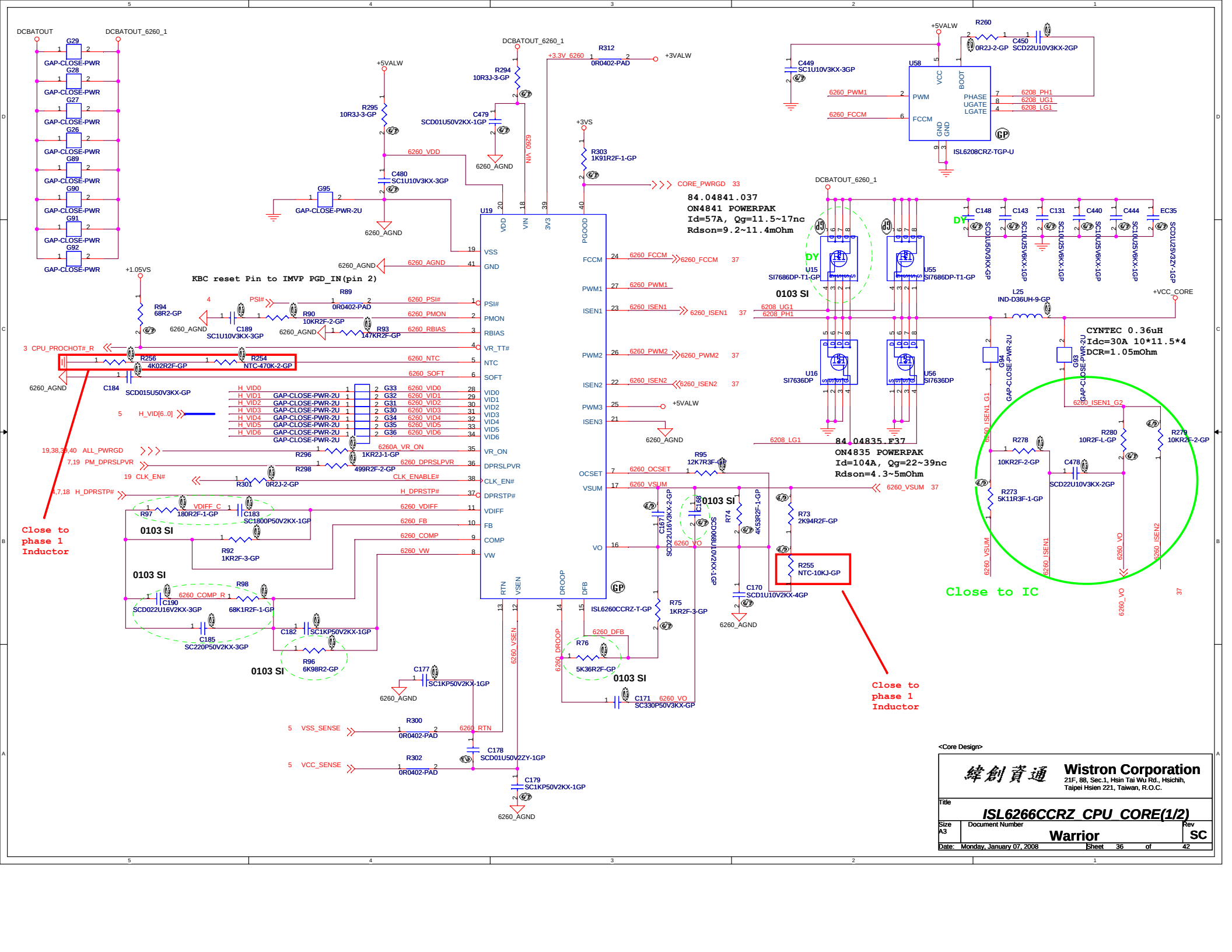
DCBATOUT
DCBATOUT_6260_1
GAP-CLOSE-PWR
+5VALW
+3VALW
+3VS
+1.05VS
+VCC_CORE
6260_AGND
KBC reset Pin to IMVP PGD_IN(pin 2)
84.04841.037
ON4841 POWERPAK
Id=57A, Qg=11.5~17nc
Rdson=9.2~11.4mOhm
84.04835.F37
ON4835 POWERPAK
Id=104A, Qg=22~39nc
Rdson=4.3~5mOhm
CYNTEC 0.36uH
Idc=30A 10*11.5*4
DCR=1.05mOhm
ISL6208CRZ-TGP-U
ISL6260CCRZ-T-GP
SI7686DP-T1-GP
SI7636DP
0103 SI
DY
Close to phase 1 Inductor
Close to IC
Close to phase 1 Inductor
<Core Design>
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Taipei Hsien 221, Taiwan, R.O.C.
ISL6266CCRZ_CPU_CORE(1/2)
Warrior
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Rev SC
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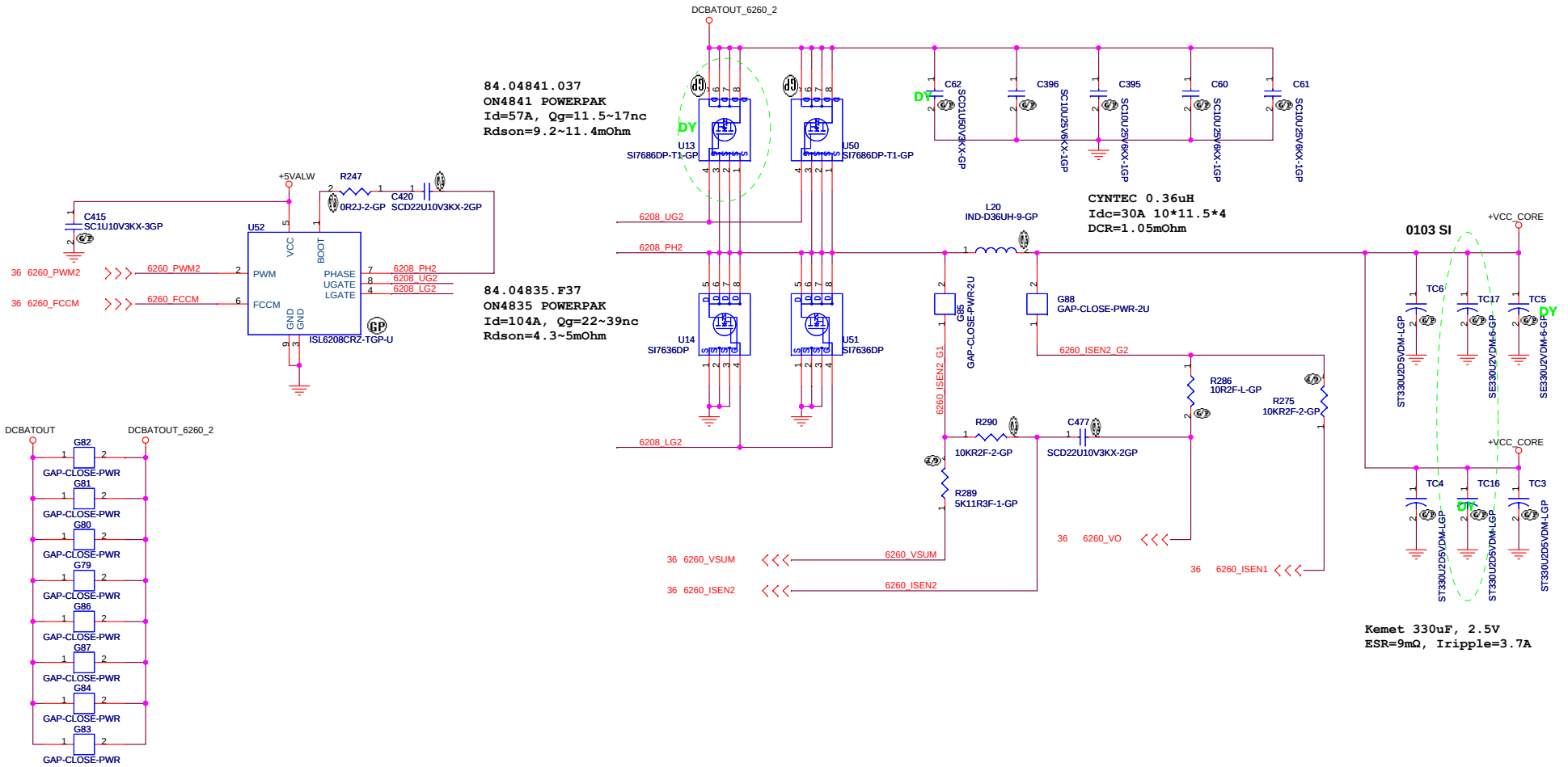

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Title: ISL6260CCRZ_CPU_CORE(2/2)		
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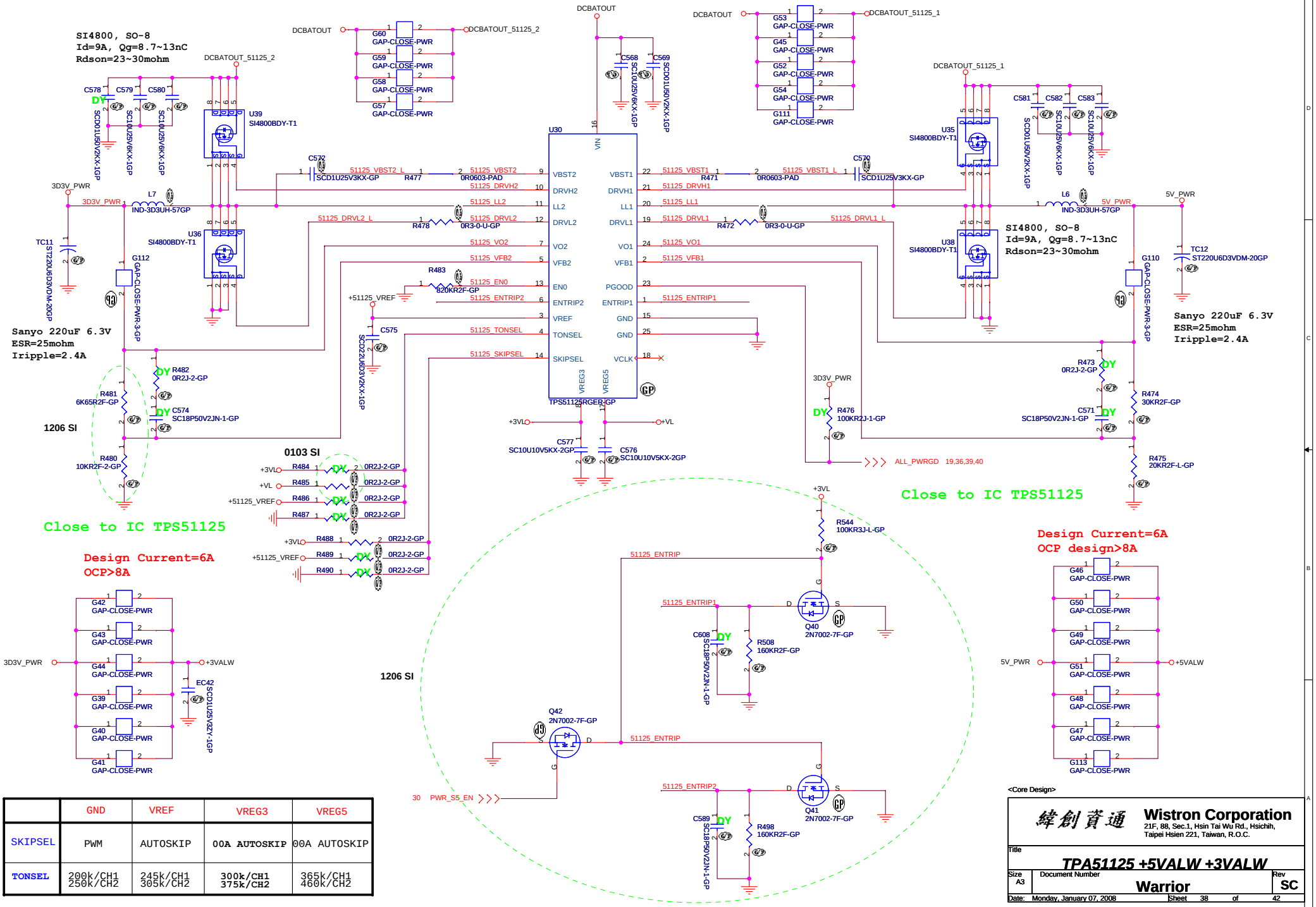

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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Title: TPA51125 +5VALW +3VALW

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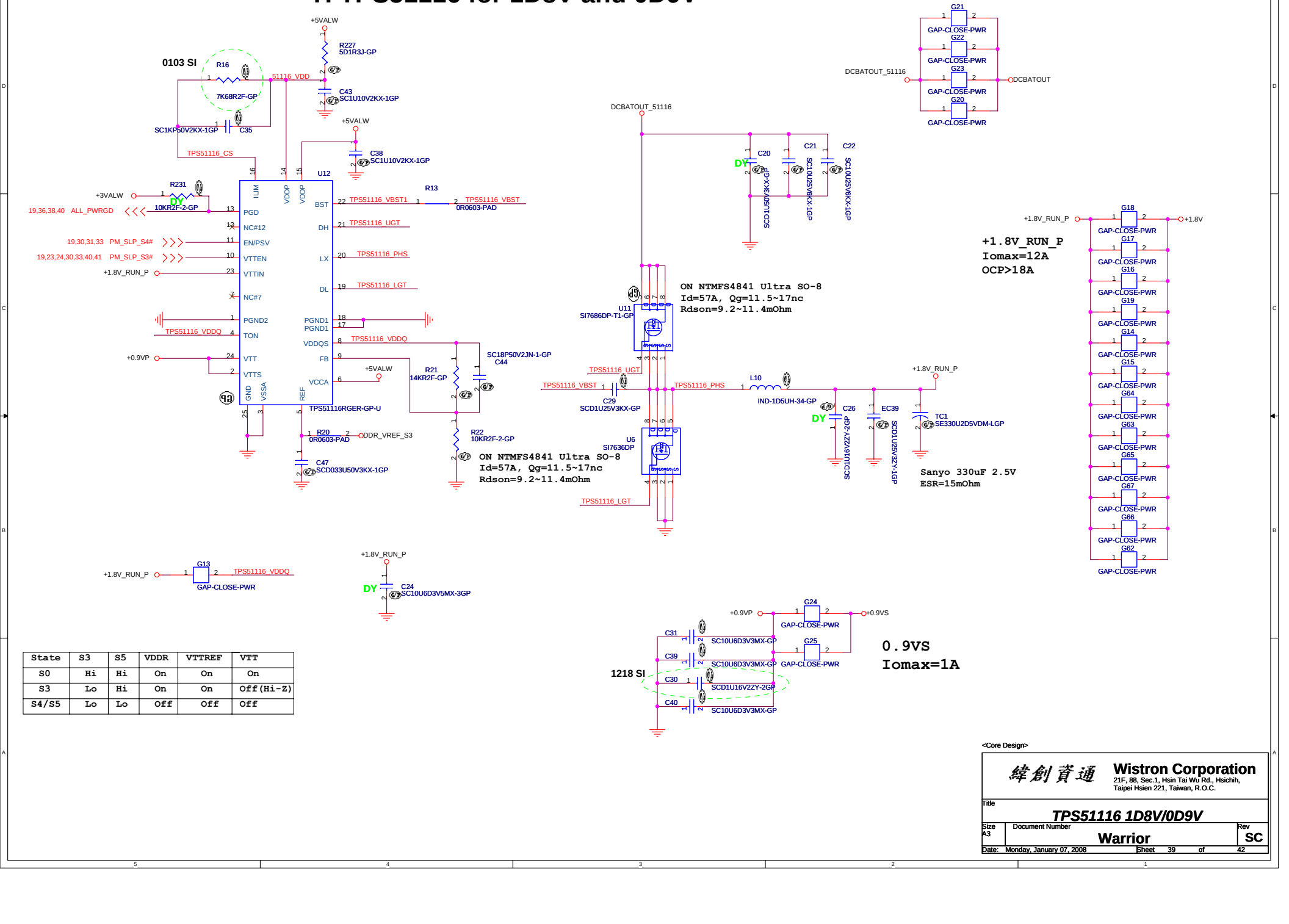
TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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Title: TPS51116 1D8V/0D9V

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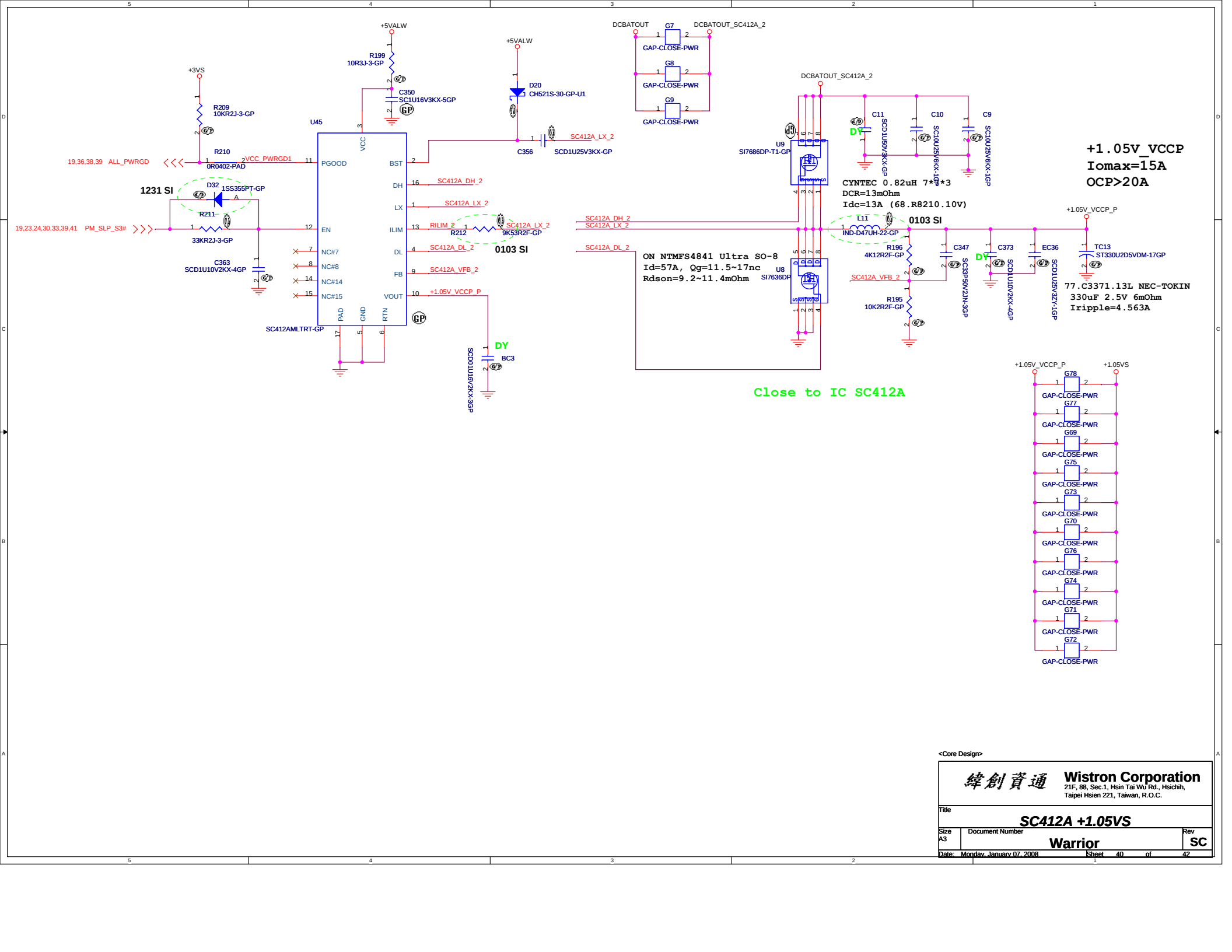

<Core Design>

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Title	***SC412A +1.05VS***	
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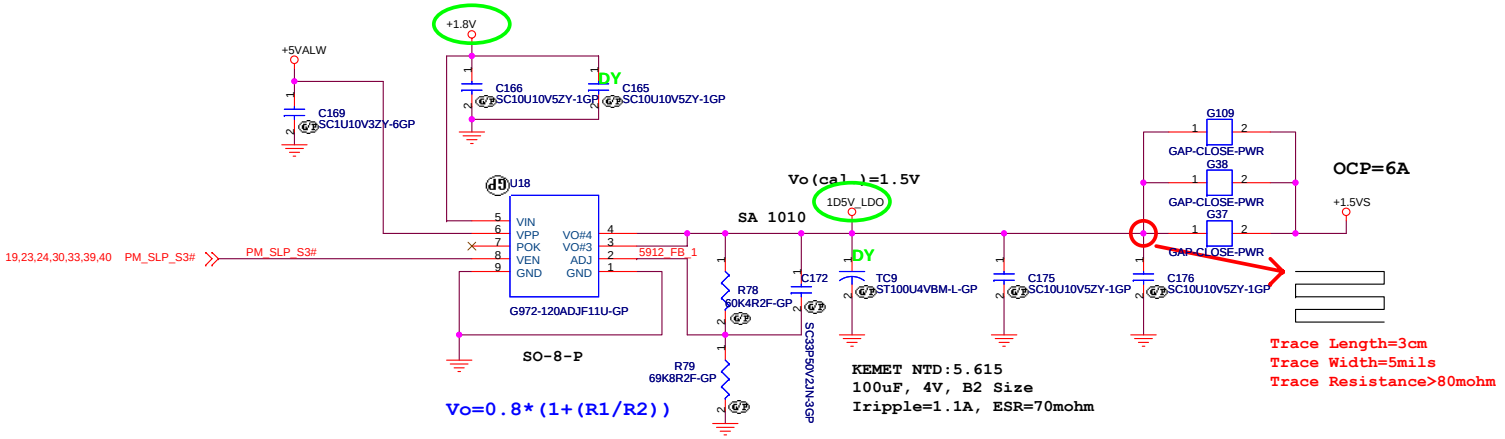

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Title	GMT_1D5V_LDO
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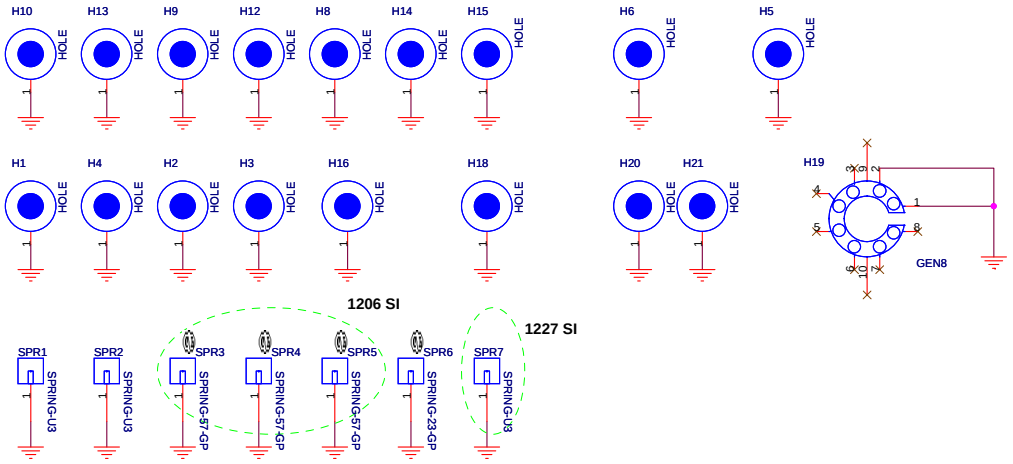

SPR1-2: 34.40U07.001
SPR3-5: 34.42T14.002
SPR6 : 34.39S07.003
SPR7 : 34.40U07.001

<Core Design>

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Title: ***MISC***

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