Weebill_HW
UMA-MUXLESS Schematics Document
Haswell ULT Processor

DY :None Installed

ANNIE: ONLY FOR ANNIE solution.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Variant Name>

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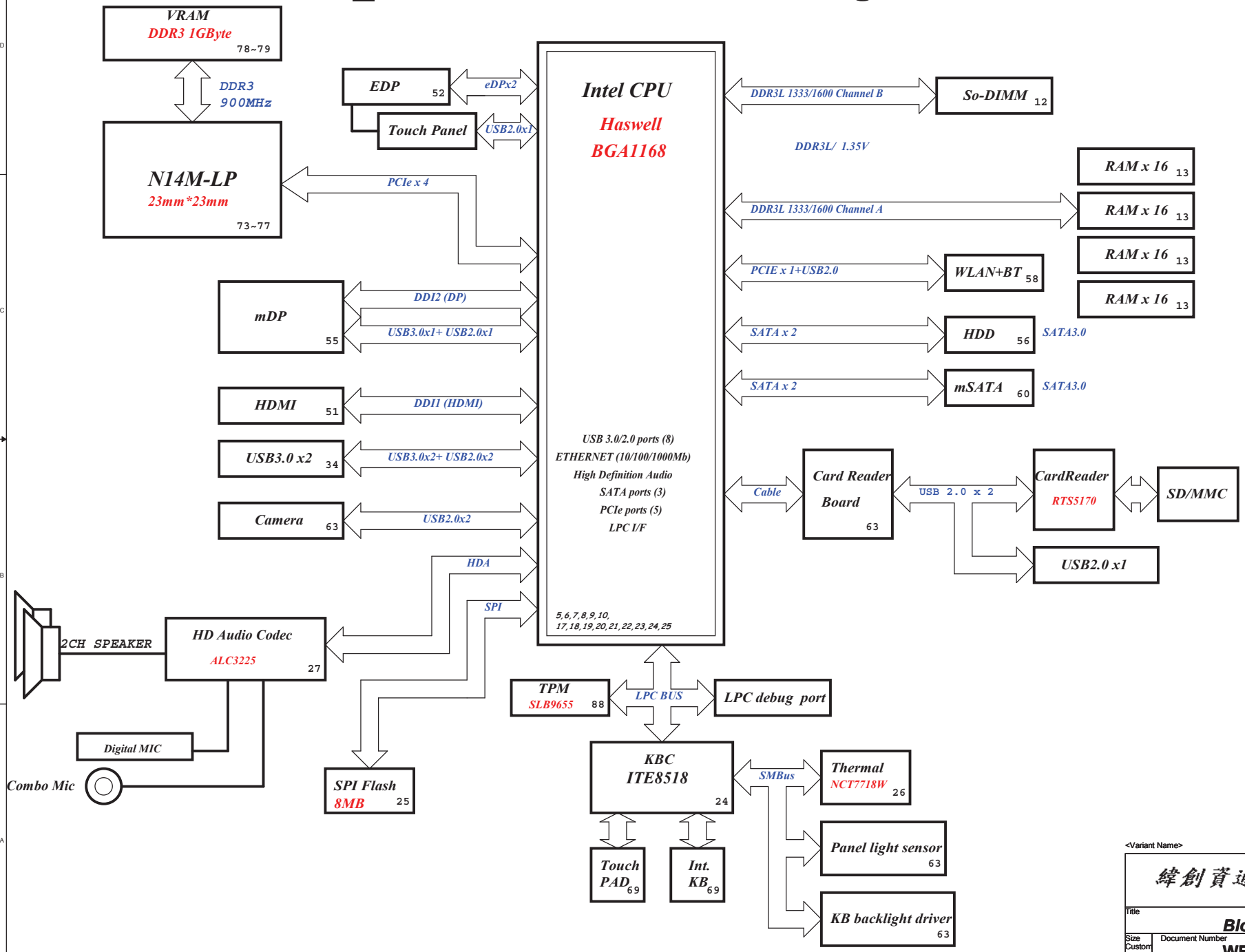
Title	Cover Page	
Size A3	Document Number WEEBILL_HW	Rev SA
Date: Wednesday, September 18, 2013	Sheet 1 of 102	

WEEBILL_HW ULT Board Block Diagram

Project code : 91.4L501.A01
PCB P/N :
Revision : 12265-SB



CHARGER BQ24760	44
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC SYN258B/C	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

CPU DC/DC TPS51622	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC SYS8208A	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51367+TPS51206	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
1D35V_S3	0D675V_S0 DDR_VREF_S3

SYSTEM DC/DC SYW232	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

PCB LAYER

L1:Top	L6:Signal
L2:GND	L7:GND
L3:Signal	L8:Signal
L4:GND	L9:GND
L5:Signal	L10:Bottom

<Variant Name>

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Title: Block Diagram

Size: Custom | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 2 of 102

5 4 3 2 1

D

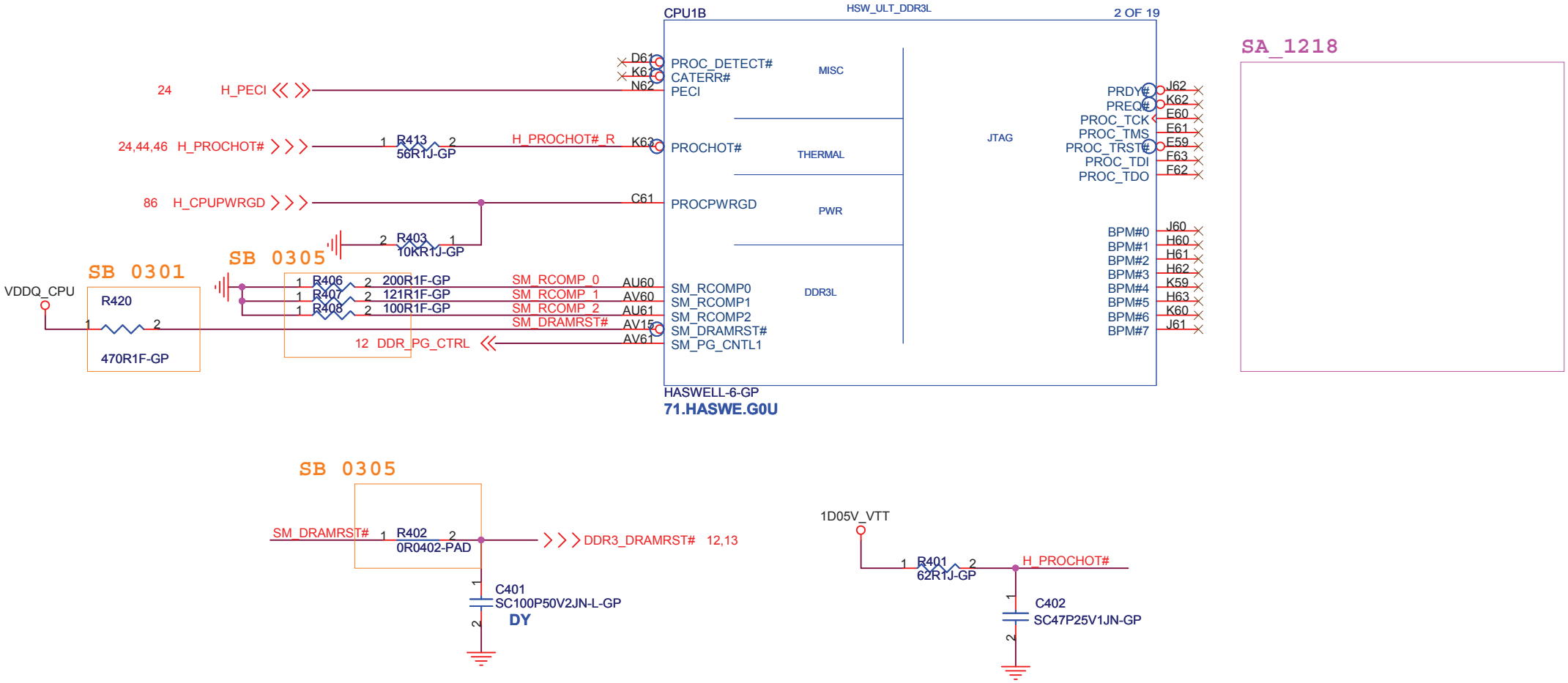
C

B

A

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (Reserved)***	
Size A4	Document Number **WEEBILL_HW**	Rev **SA**
Date: Wednesday, September 18, 2013	Sheet 3 of 102	



<Variant Name>

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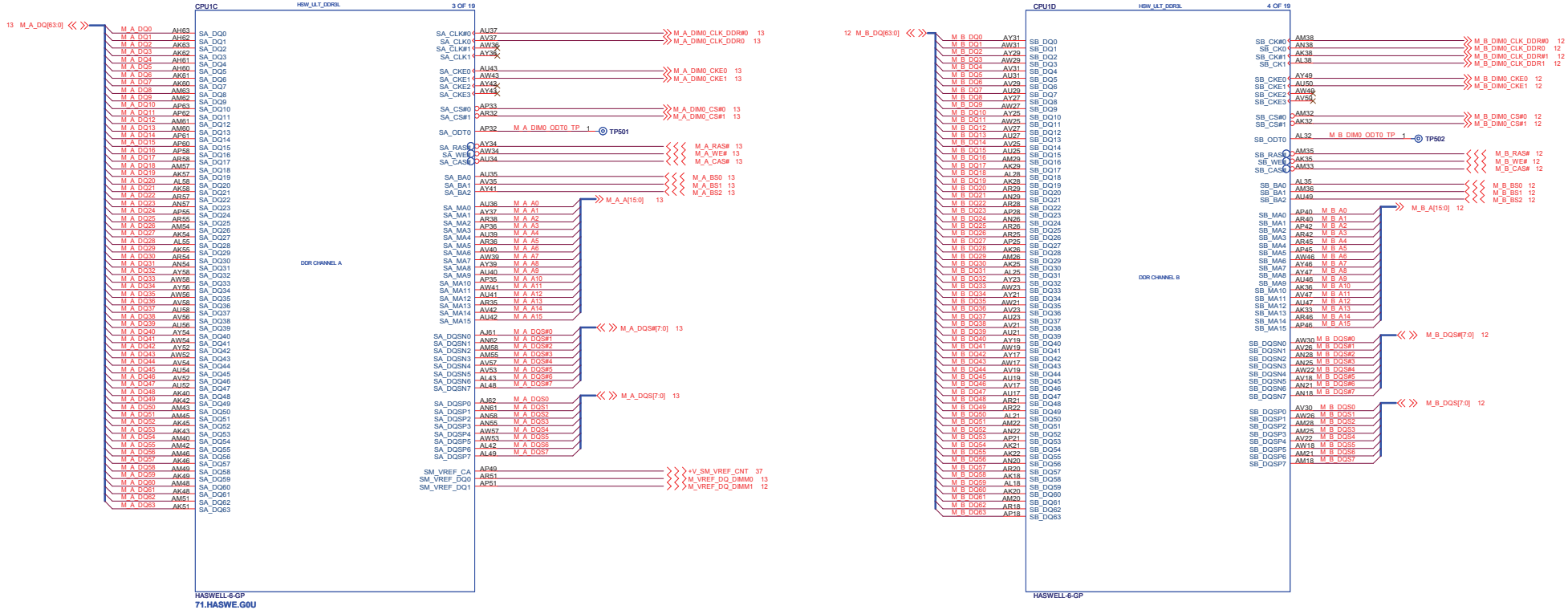
Title: CPU (THERMAL/CLOCK/PM)

Size: A4 | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 4 of 102



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緯創資通 **Wistron Corporation**
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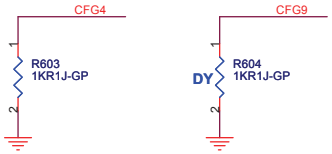
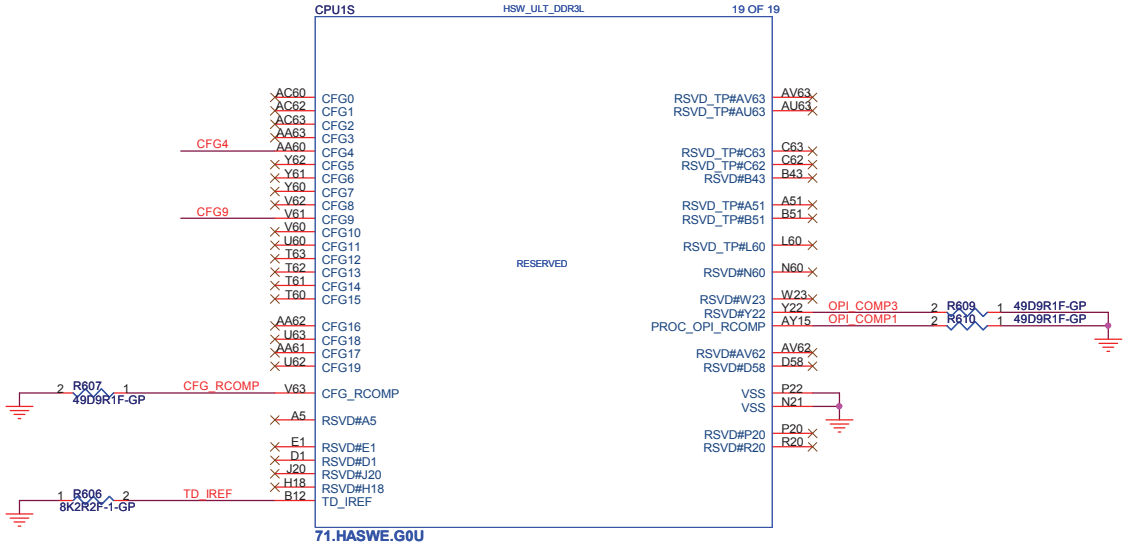
Title: **CPU (DDR)**

Size	Document Number	Rev
A2	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 5 of 102

eDP Enable	
CFG4	1:Disable 0:Enable



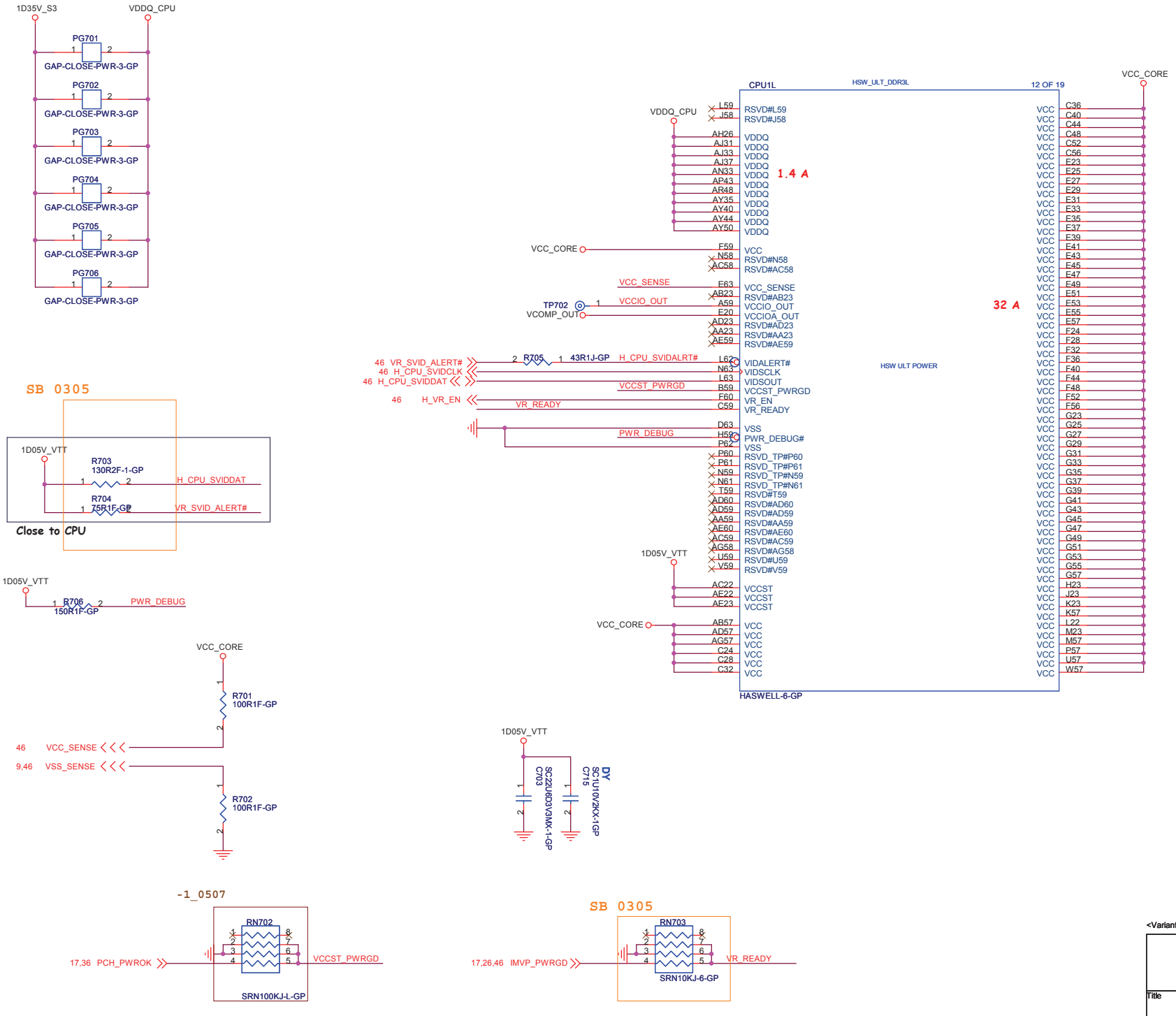


Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
		continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected



<Variant Name>

緯創資通 **Wistron Corporation**
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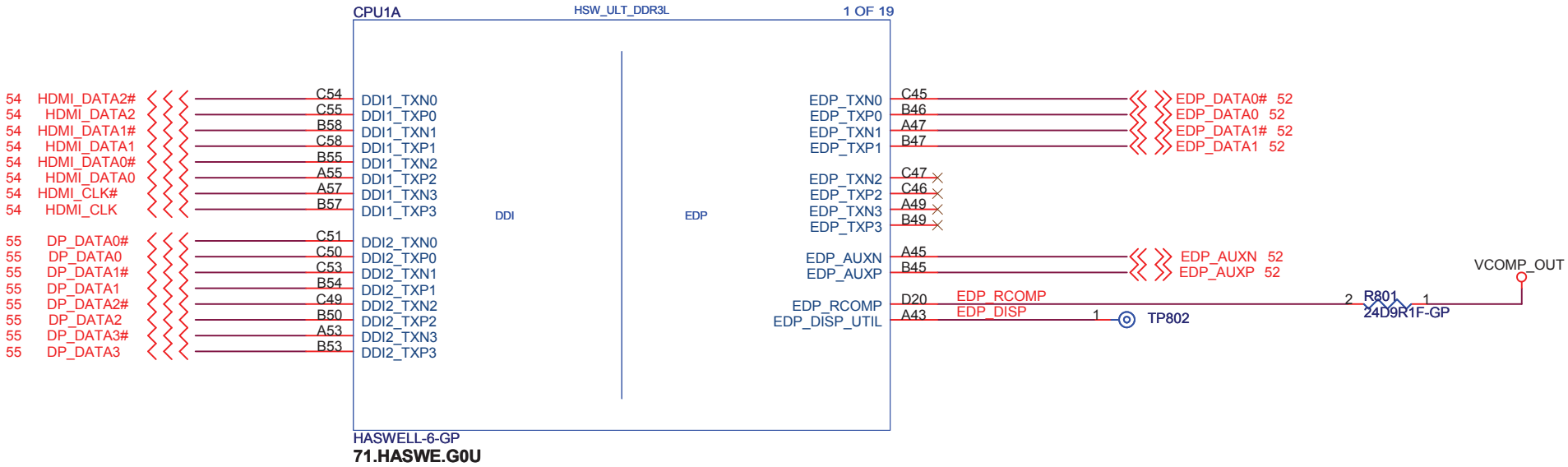
Title: **CPU (VCC_CORE)**

Size	Document Number	Rev
A3	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 7 of 102



<Variant Name>

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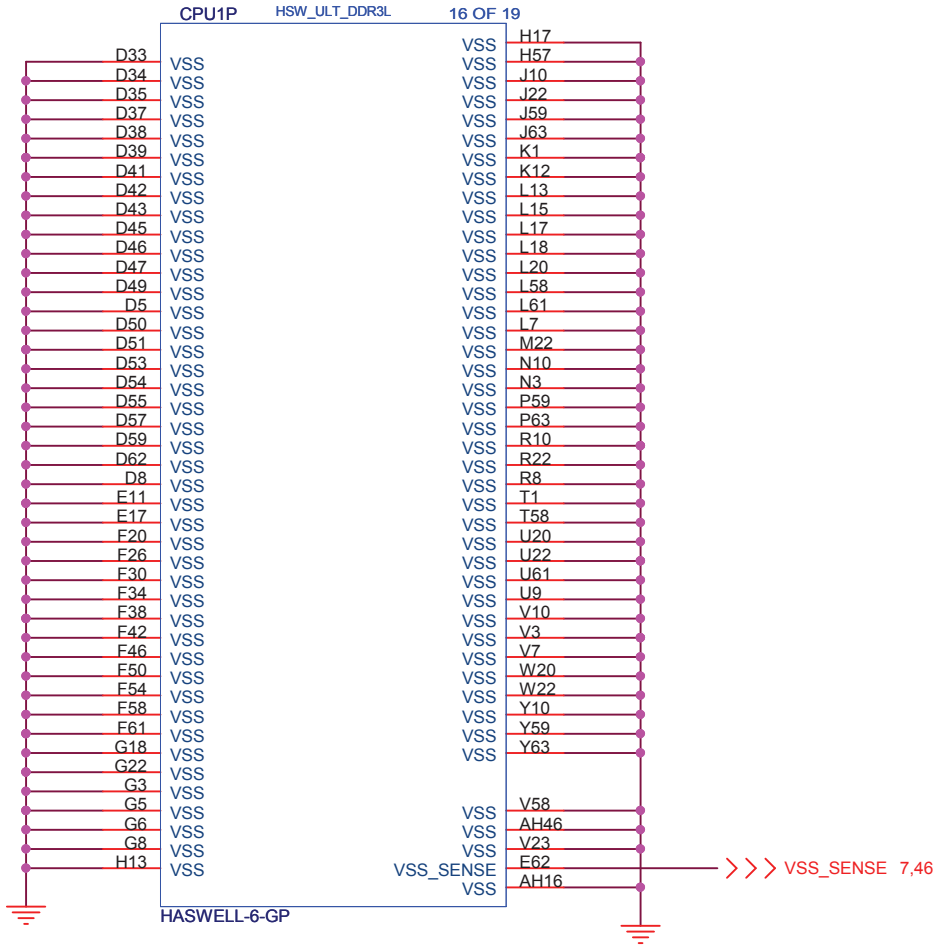
Title

CPU (DDI/EDP)

Size	Document Number	Rev
A4	WEEBILL_HW	SB

Date: Wednesday, September 18, 2013 Sheet 8 of 102



<Variant Name>

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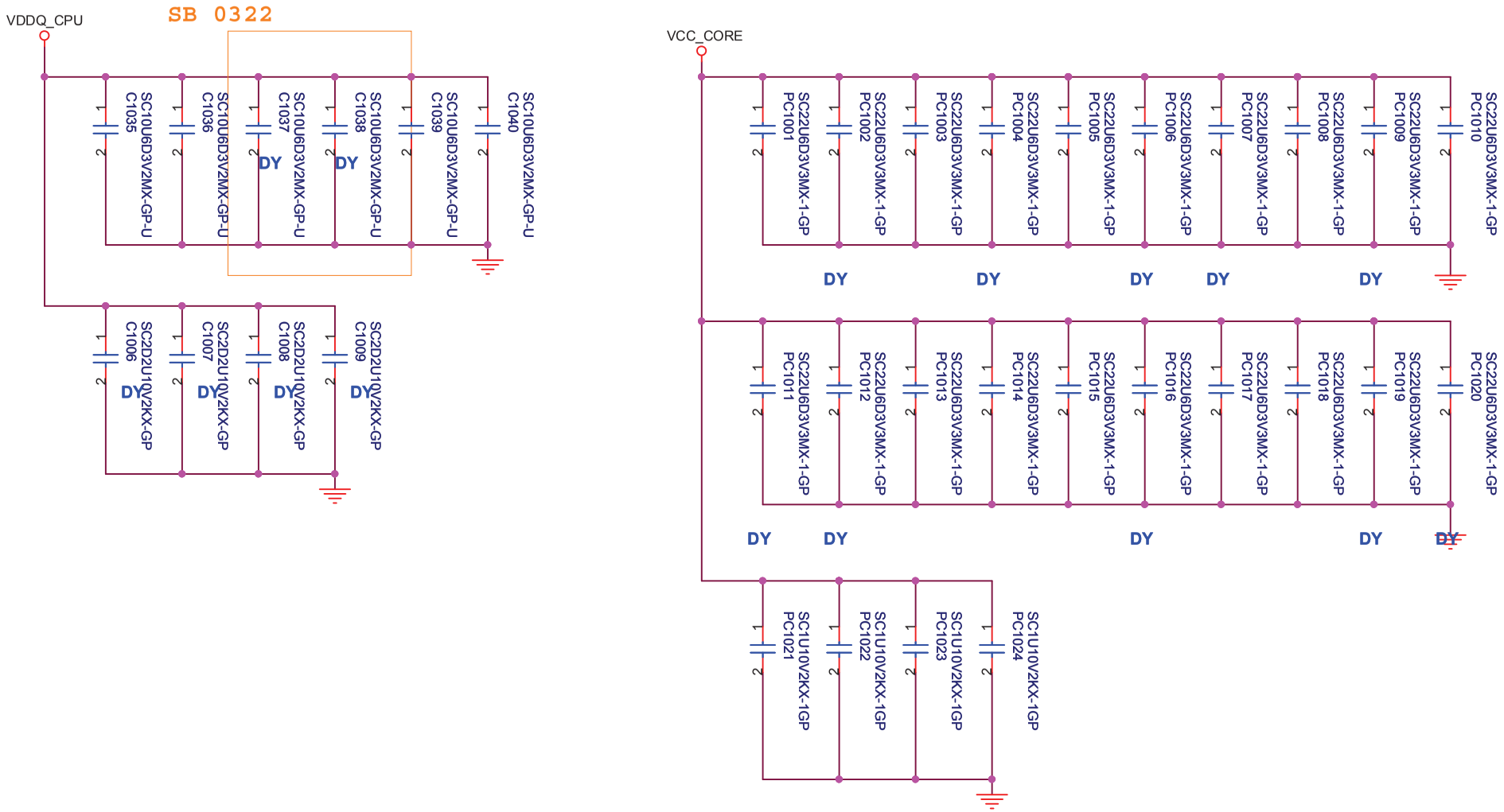
Title: CPU (VSS)

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 9 of 102



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緯創資通 **Wistron Corporation**
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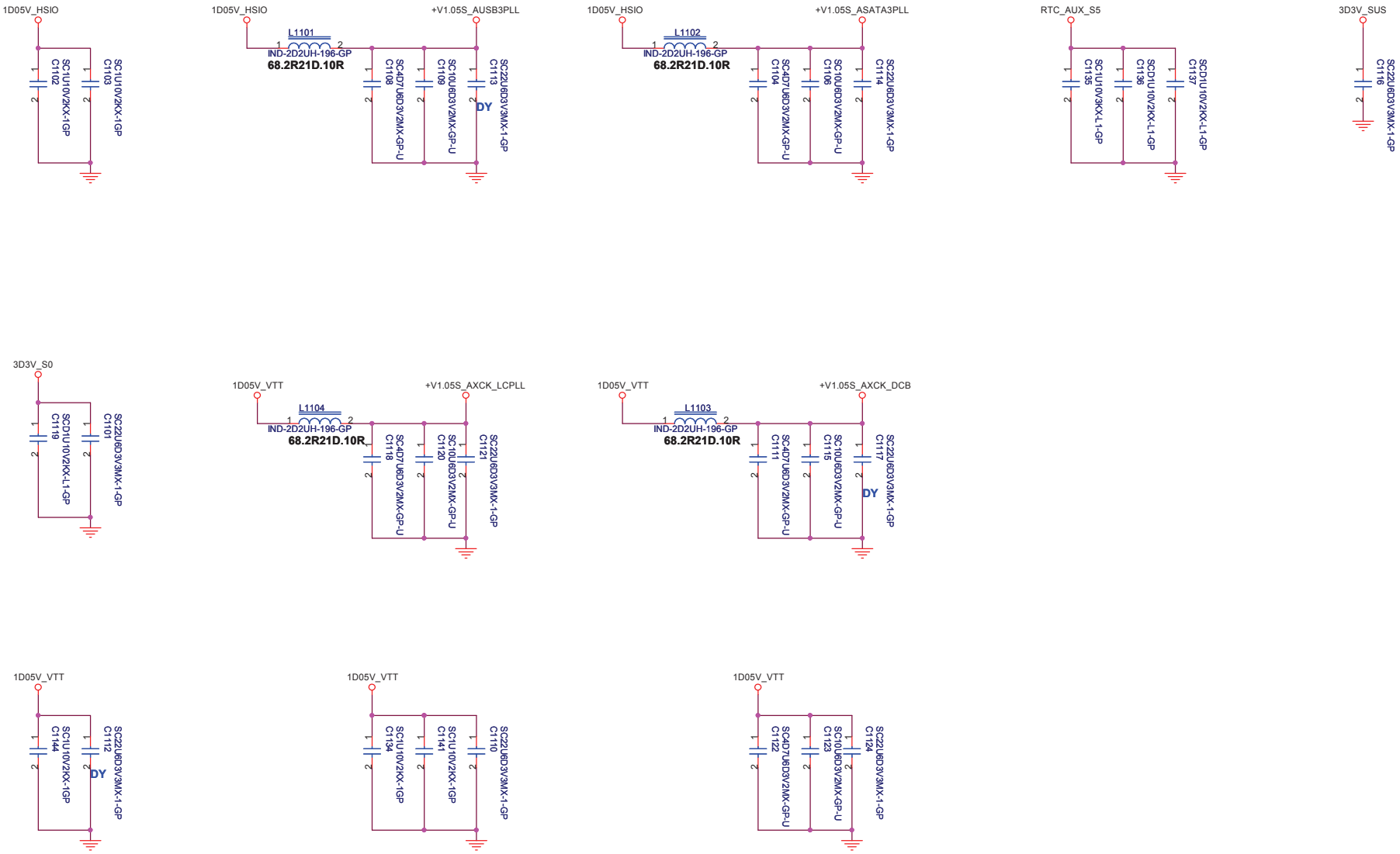
Title: ***CPU (Power CAP1)***

Size	Document Number	Rev
A4	**WEEBILL_HW**	**SA**

Date: Wednesday, September 18, 2013 Sheet 10 of 102



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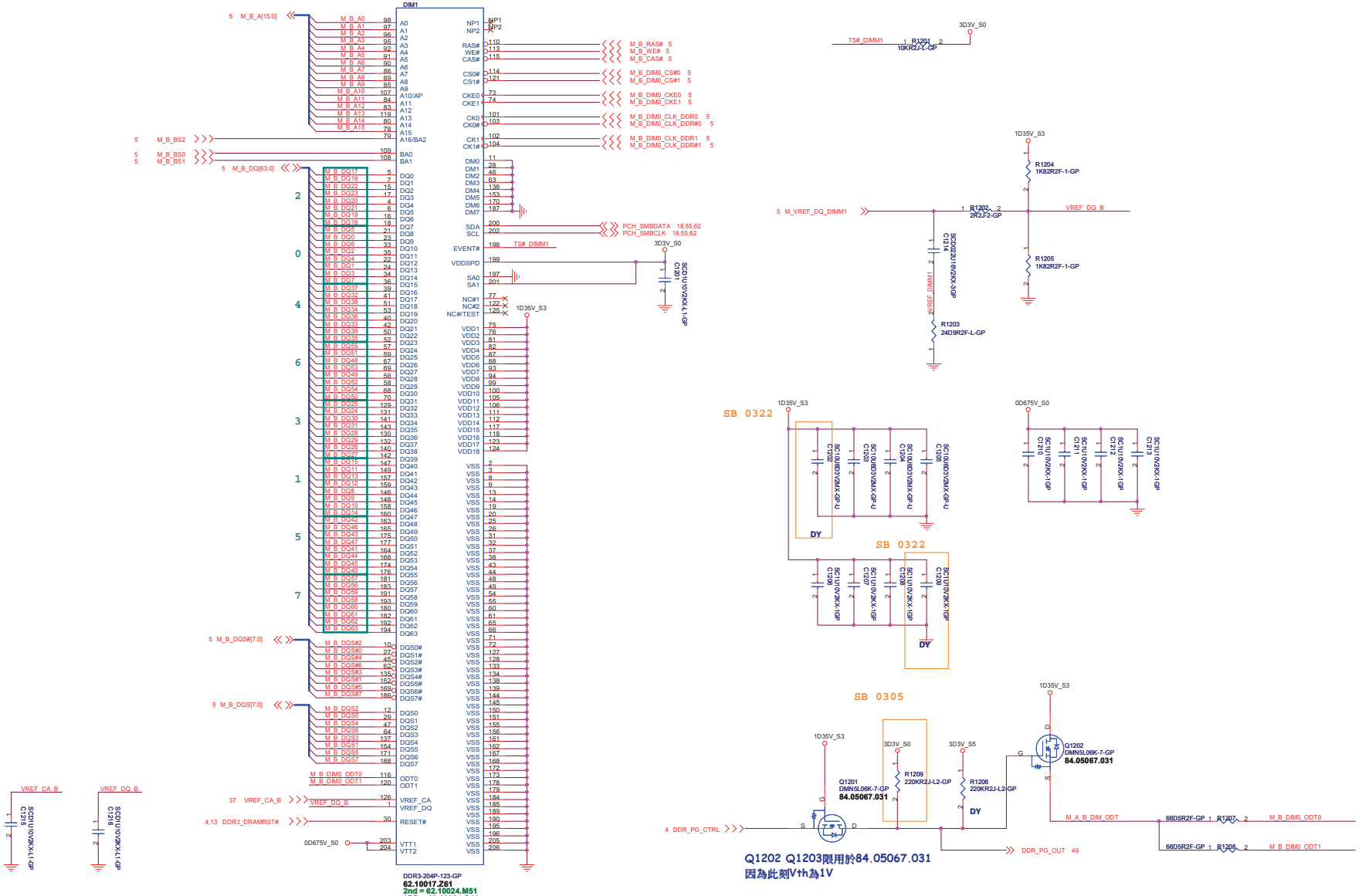
Title: **CPU (Power CAP2)**

Size	Document Number	Rev
A3	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 11 of 102



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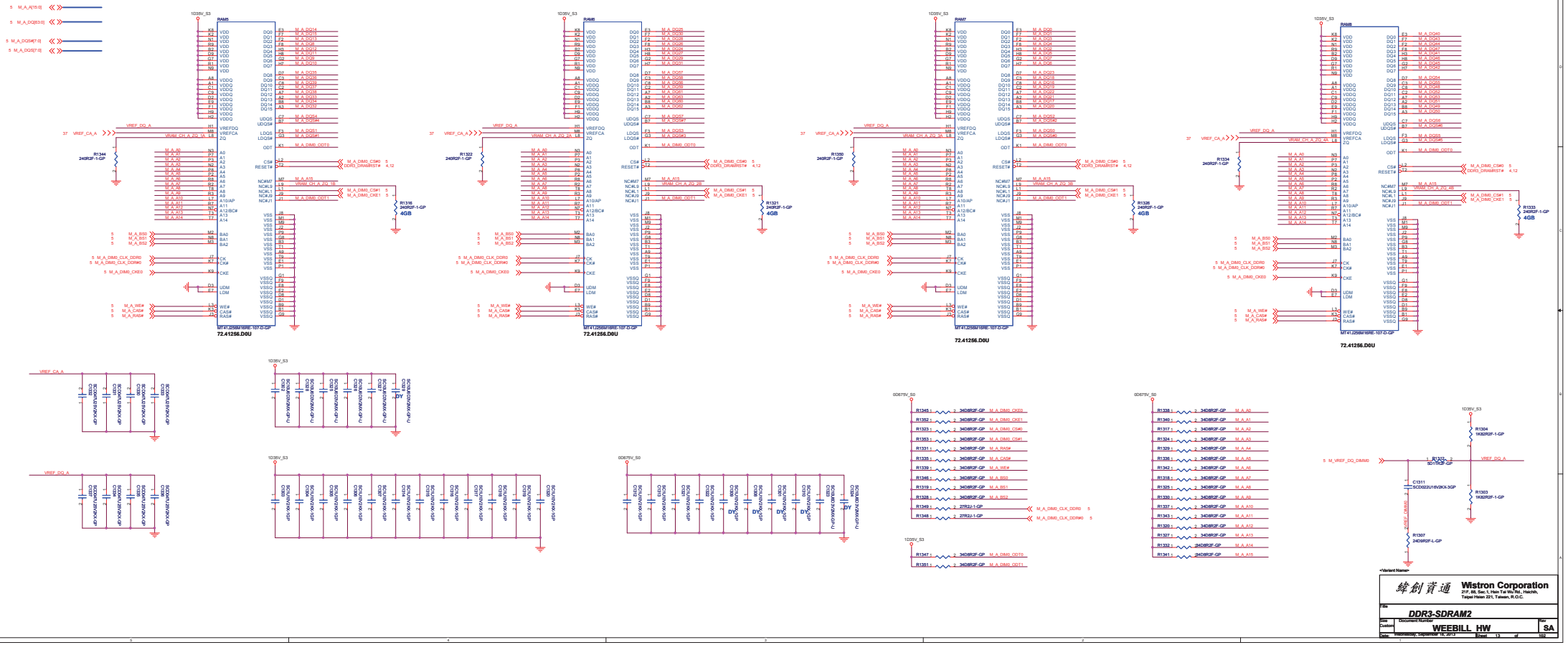
Title: ***DDR3-SDRAM2***

Size	Document Number	Rev
A2	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 12 of 102



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File: **DDR3-SDRAM2**

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Custom	WEEBILL HW	SA

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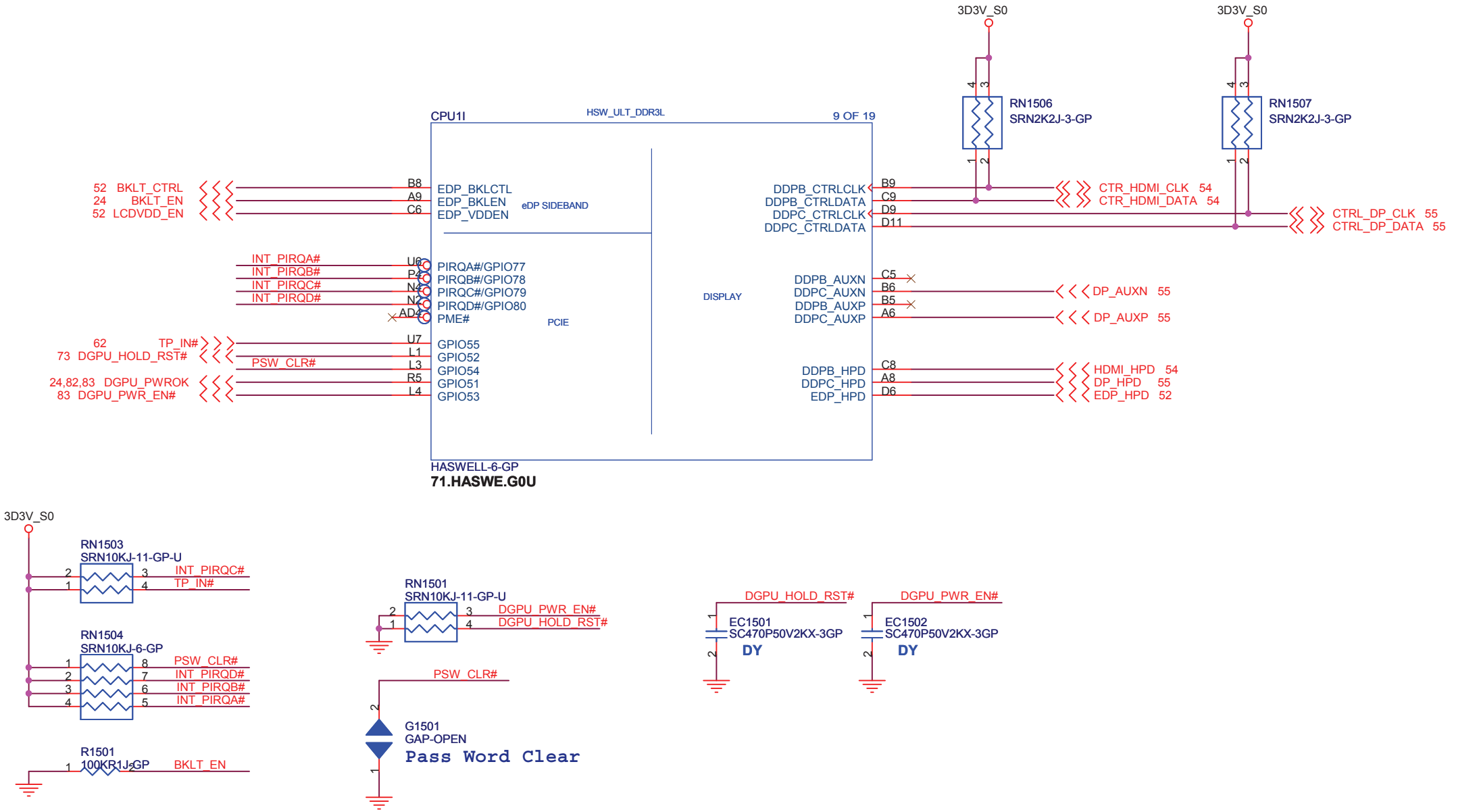
Title
(Reserved)_SODIMM _SODIMM4

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 14 of 102



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Title
CPU(EDP SIDEBAND/GPIO/DDI)

Size	Document Number	Rev
A4	**WEEBILL_HW**	**SA**

Date: Wednesday, September 18, 2013 Sheet 15 of 102

USB2.0 Table

Pair	Device
0	USB3.0 Port 2
1	USB3.0 Port 1
2	DP
3	Cardreader
4	CCD
5	WLAN(Bluetooth)
6	Touch Penal
7	USB2.0 Port 1

USB3.0 Table

Pair	Device
1	USB3.0 Port 1
2	DP
3	USB3.0 Port 2
4	

<Variant Name>

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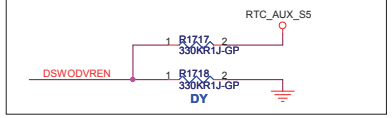
Title: CPU (PCI/USB)

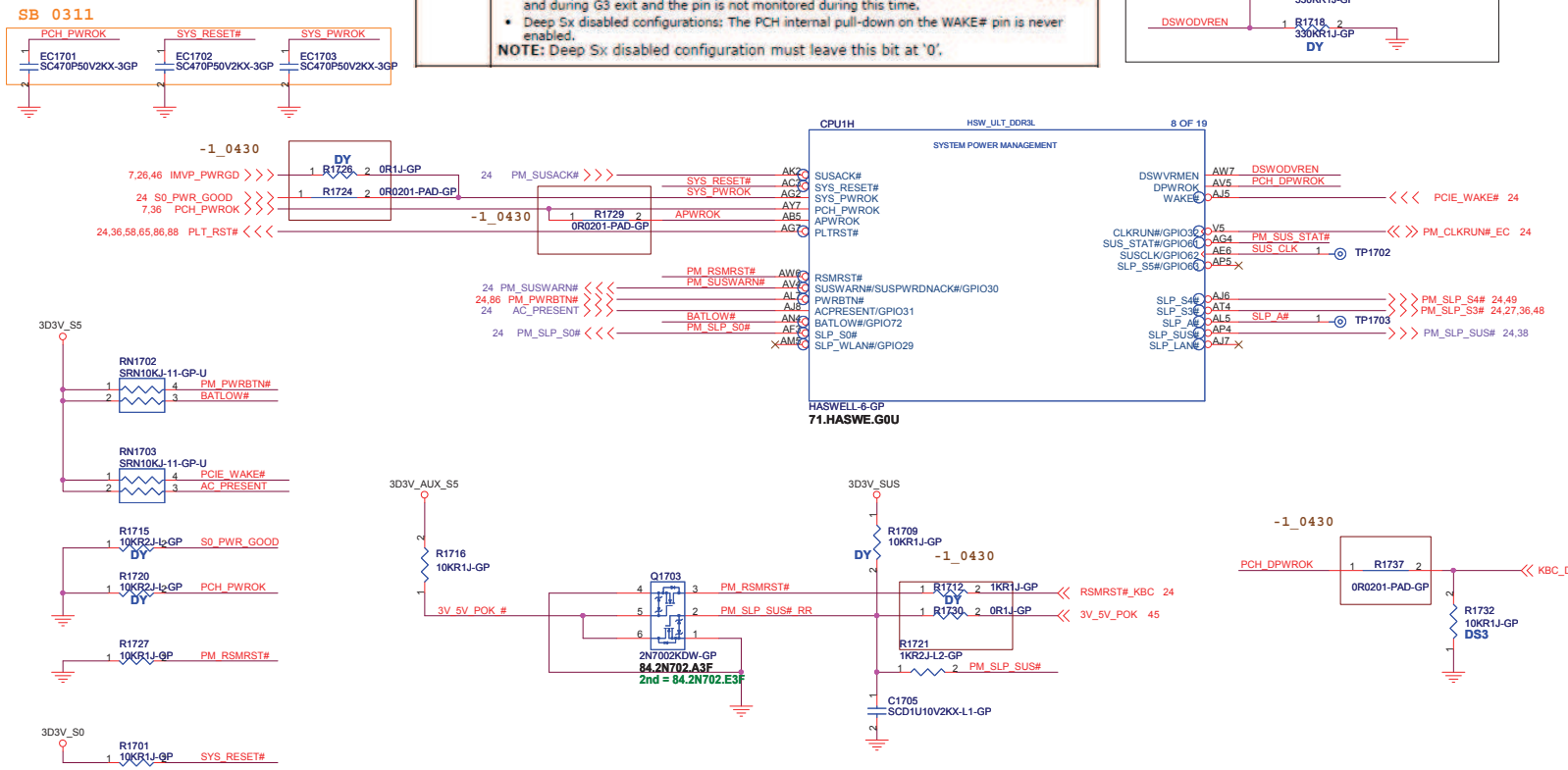
Size: A3 | Document Number: WEEBILL_HW | Rev: SA

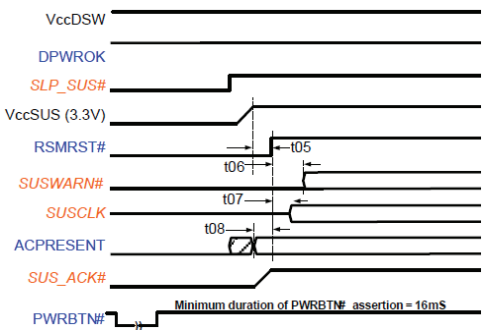
Date: Wednesday, September 18, 2013 | Sheet 16 of 102

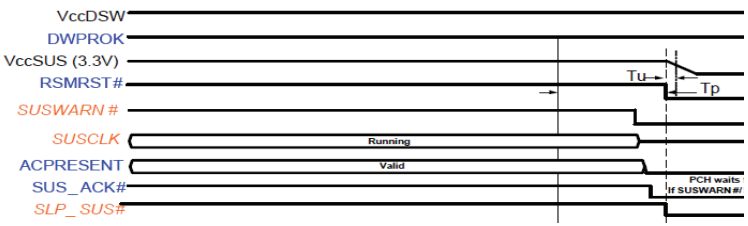
Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled









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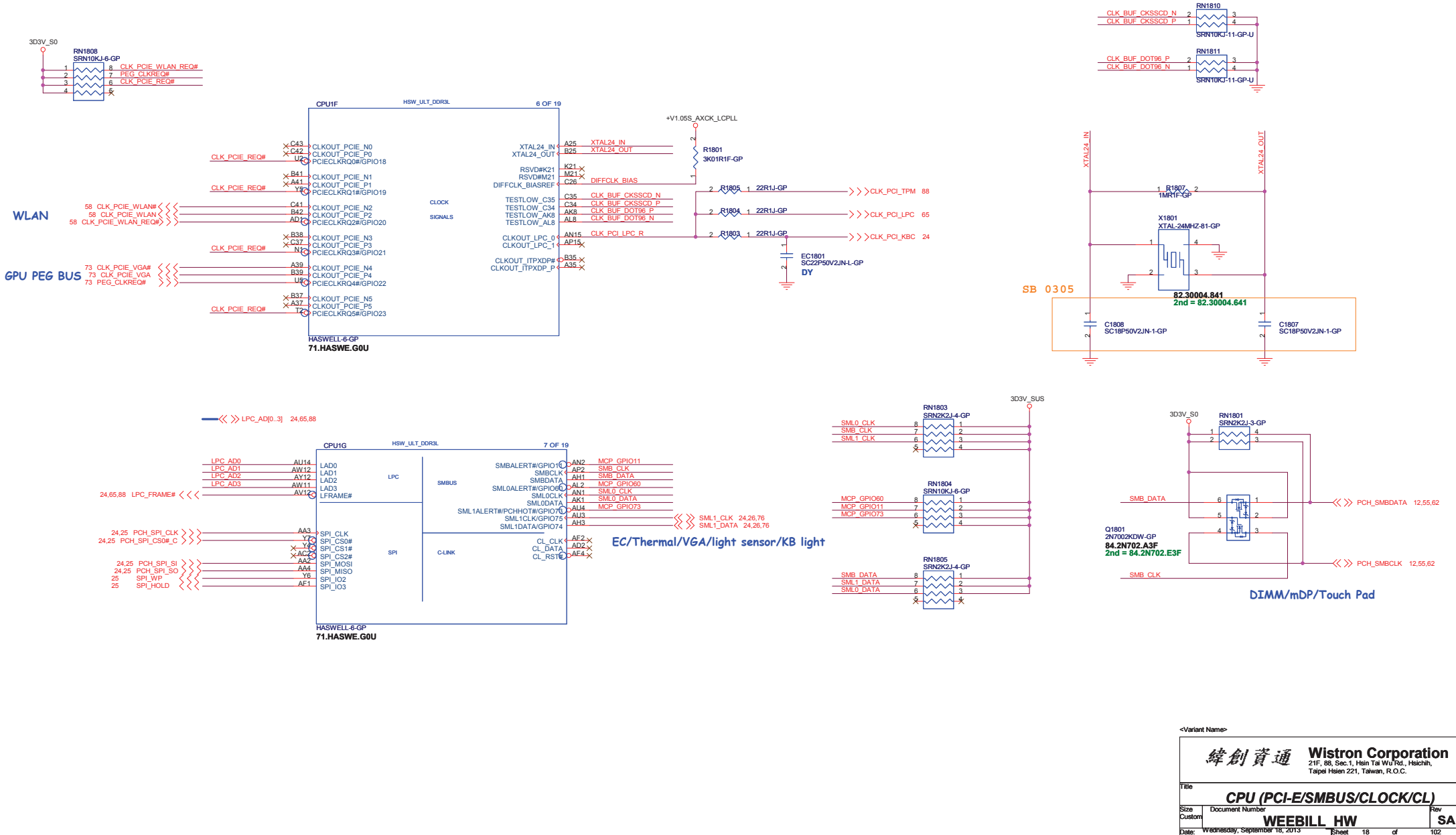
Title: CPU (DMI/FDI/PM)

Size: Custom | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 17 of 102



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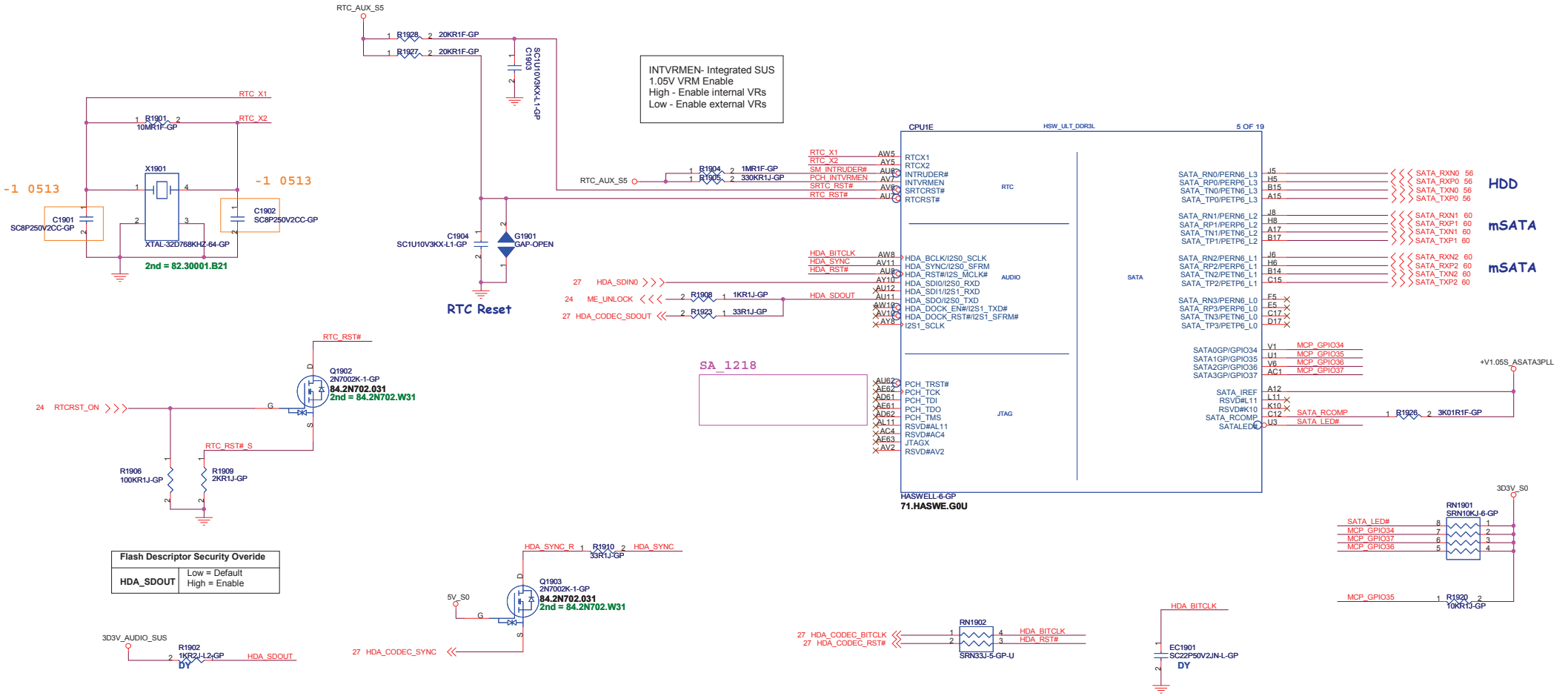
Title	***CPU (PCI-E/SMBUS/CLOCK/CL)***
Size: Custom	Document Number: **WEEBILL_HW** — Rev: **SA**
Date: Wednesday, September 18, 2013	Sheet 18 of 102



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Title: **CPU (RTC/LPC/SATA/HDA)**

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Custom	WEEBILL_HW	SB

Date: Wednesday, September 18, 2013 Sheet 19 of 102

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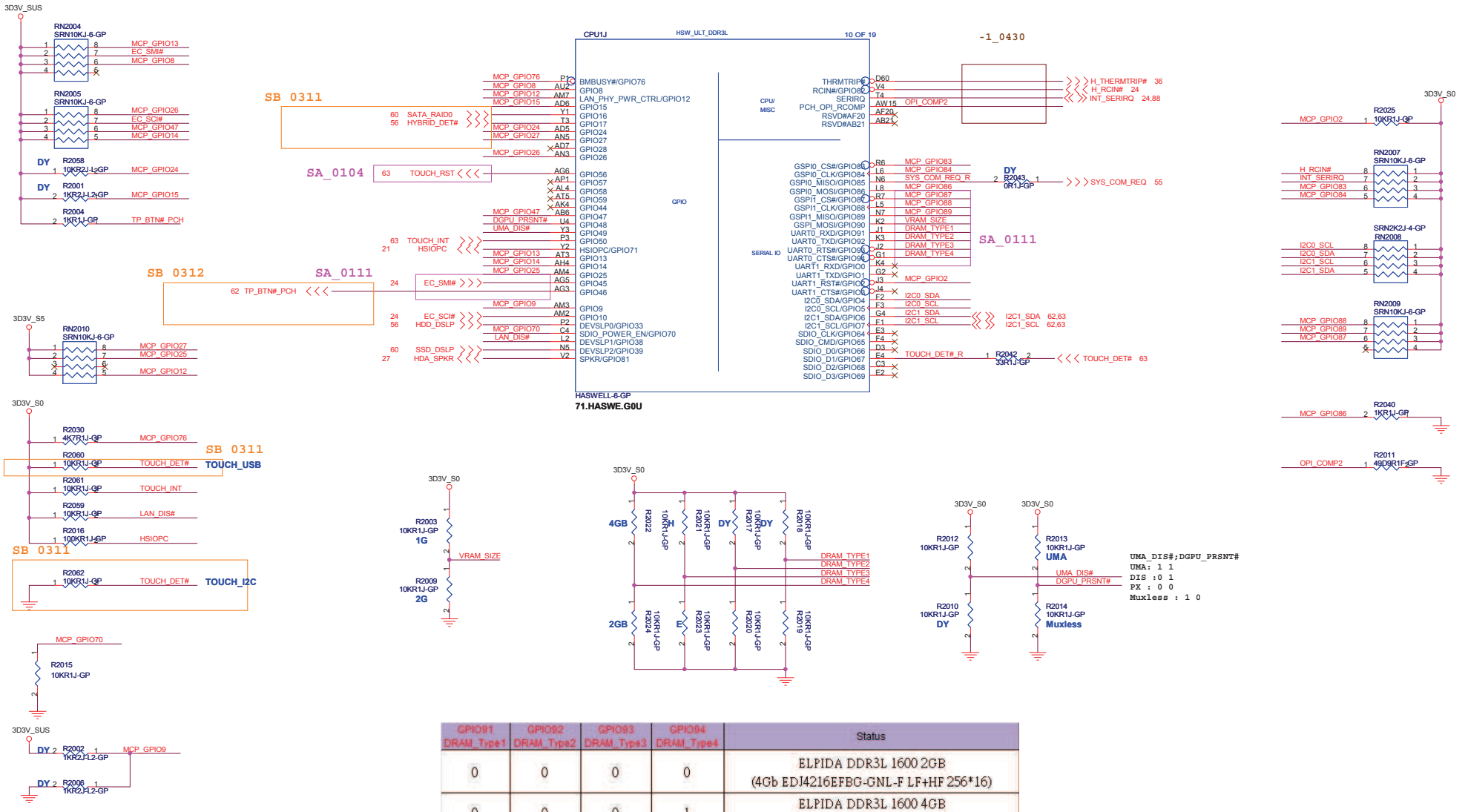

GPIO91 DRAM_Type1	GPIO92 DRAM_Type2	GPIO93 DRAM_Type3	GPIO94 DRAM_Type4	Status
0	0	0	0	ELPIDA DDR3L 1600 2GB (4Gb EDJ4216EFBG-GNL-F LF+HF 256*16)
0	0	0	1	ELPIDA DDR3L 1600 4GB (8Gb EDJ8416E6MB-GNL-F LF+HF 512*16)
0	0	1	0	HYNIX DDR3L 1600 2GB (4Gb H5TC4G63AFR-PBA LF+HF 256*16)
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	

<Variant Name>

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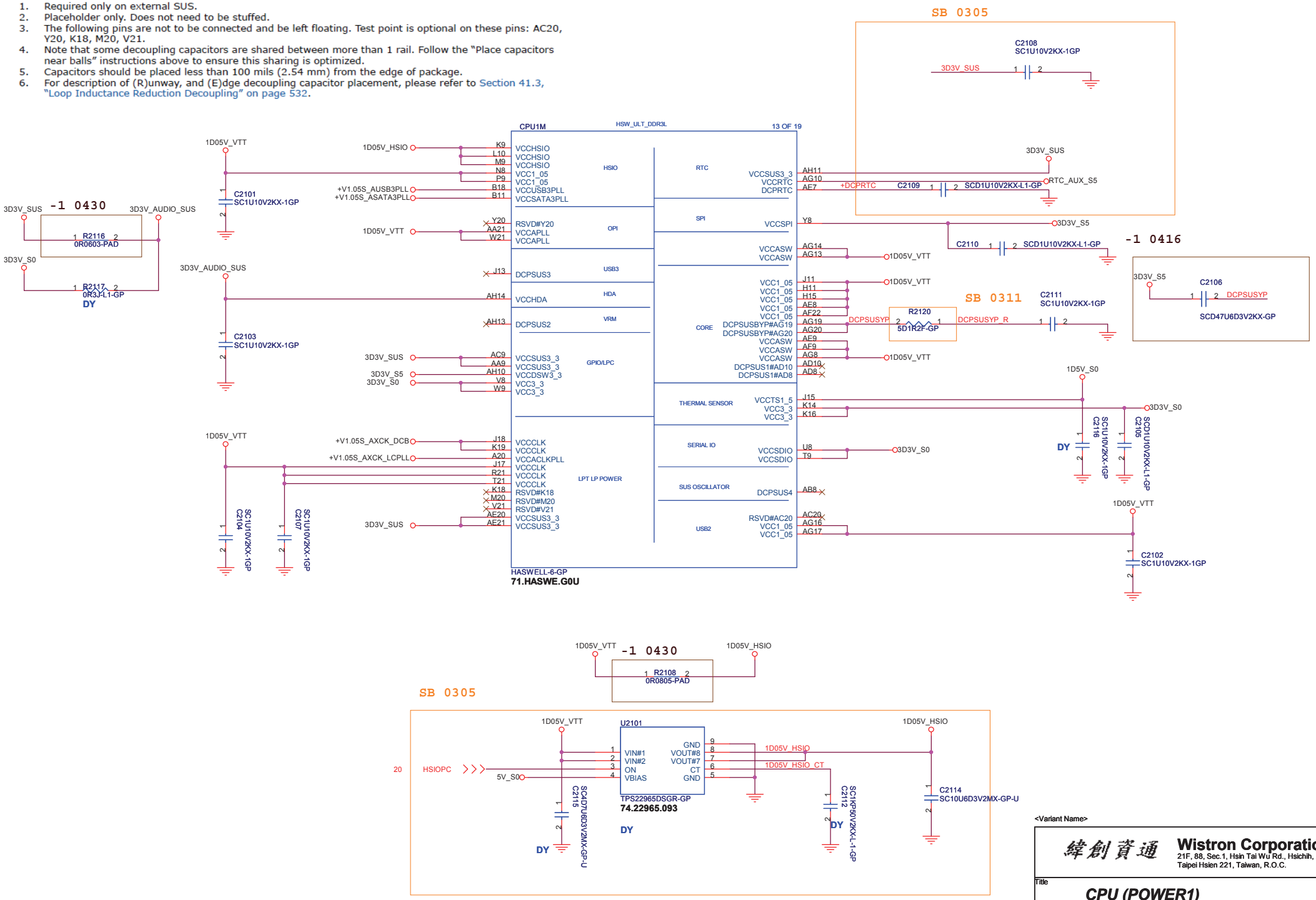
Title: CPU (GPIO/MISC)

Size: Custom | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 20 of 102

Notes:

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



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緯創資通 **Wistron Corporation**
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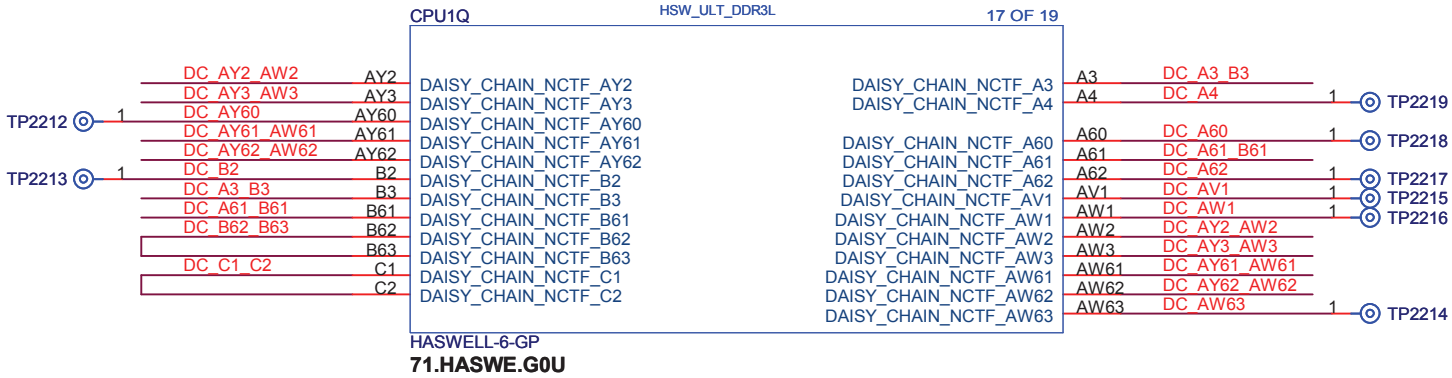
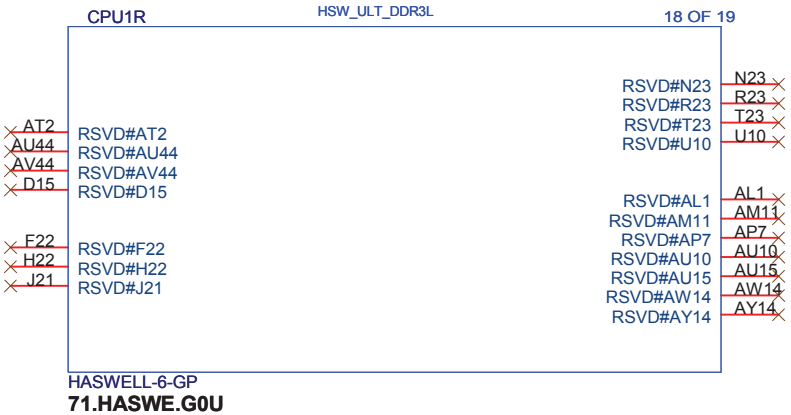
Title: **CPU (POWER1)**

Size	Document Number	Rev
A3	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 21 of 102





<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***CPU (RSVD)***

Size	Document Number	Rev
A4	**WEEBILL_HW**	**SA**

Date: Wednesday, September 18, 2013 Sheet 22 of 102

SSID = PCH

CPU1N HSW_ULT_DDR3L 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

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71.HASWE.G0U

CPU1O HSW_ULT_DDR3L 15 OF 19

AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

HASWELL-6-GP

71.HASWE.G0U

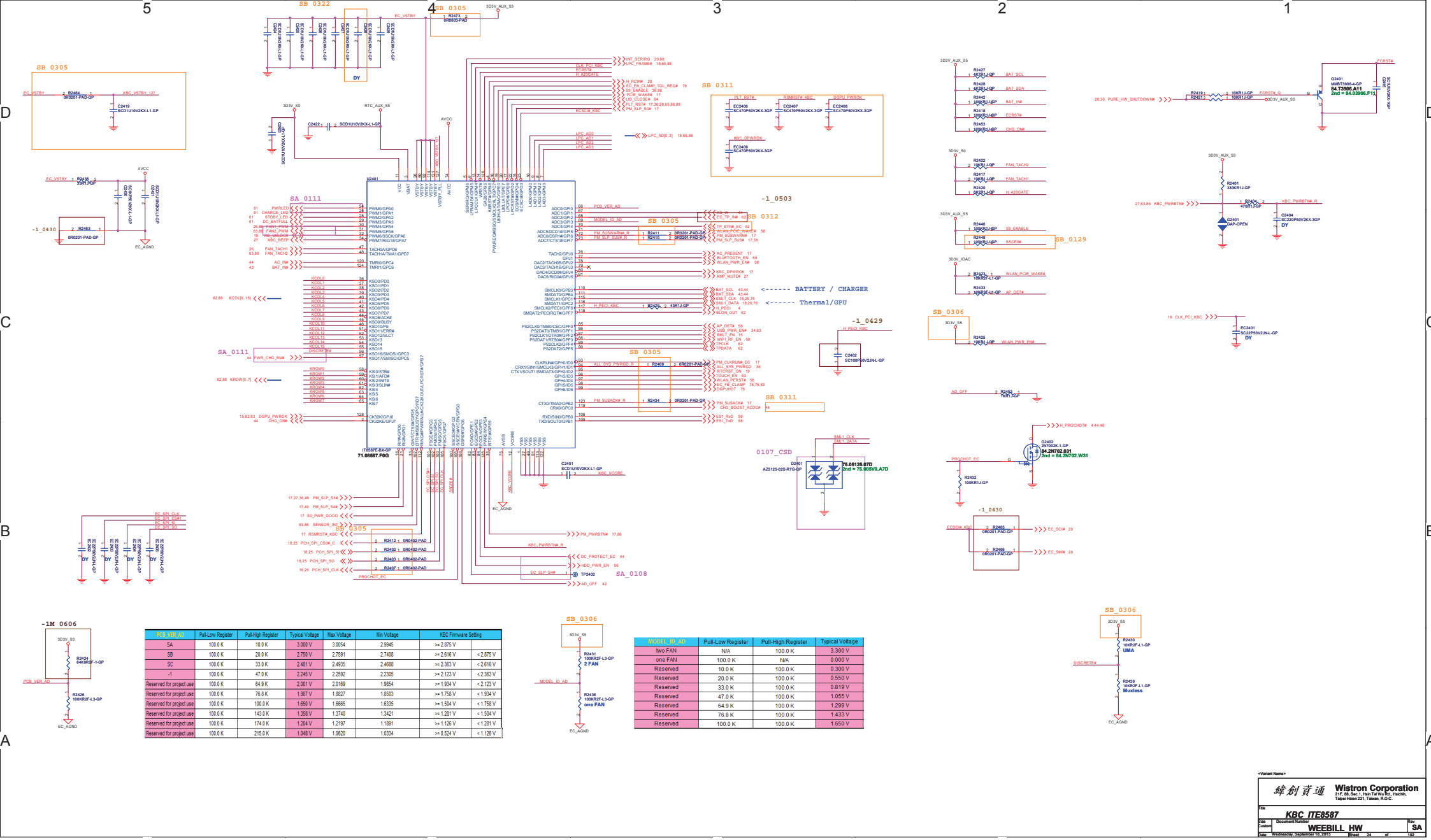
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	**WEEBILL_HW**	**SA**

Date: Wednesday, September 18, 2013 Sheet 23 of 102



PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	>= 0.524 V	< 1.126 V

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
two FAN	N/A	100.0 K	3.300 V
one FAN	100.0 K	N/A	0.000 V
Reserved	10.0 K	100.0 K	0.300 V
Reserved	20.0 K	100.0 K	0.550 V
Reserved	33.0 K	100.0 K	0.819 V
Reserved	47.0 K	100.0 K	1.055 V
Reserved	64.9 K	100.0 K	1.299 V
Reserved	76.8 K	100.0 K	1.433 V
Reserved	100.0 K	100.0 K	1.650 V

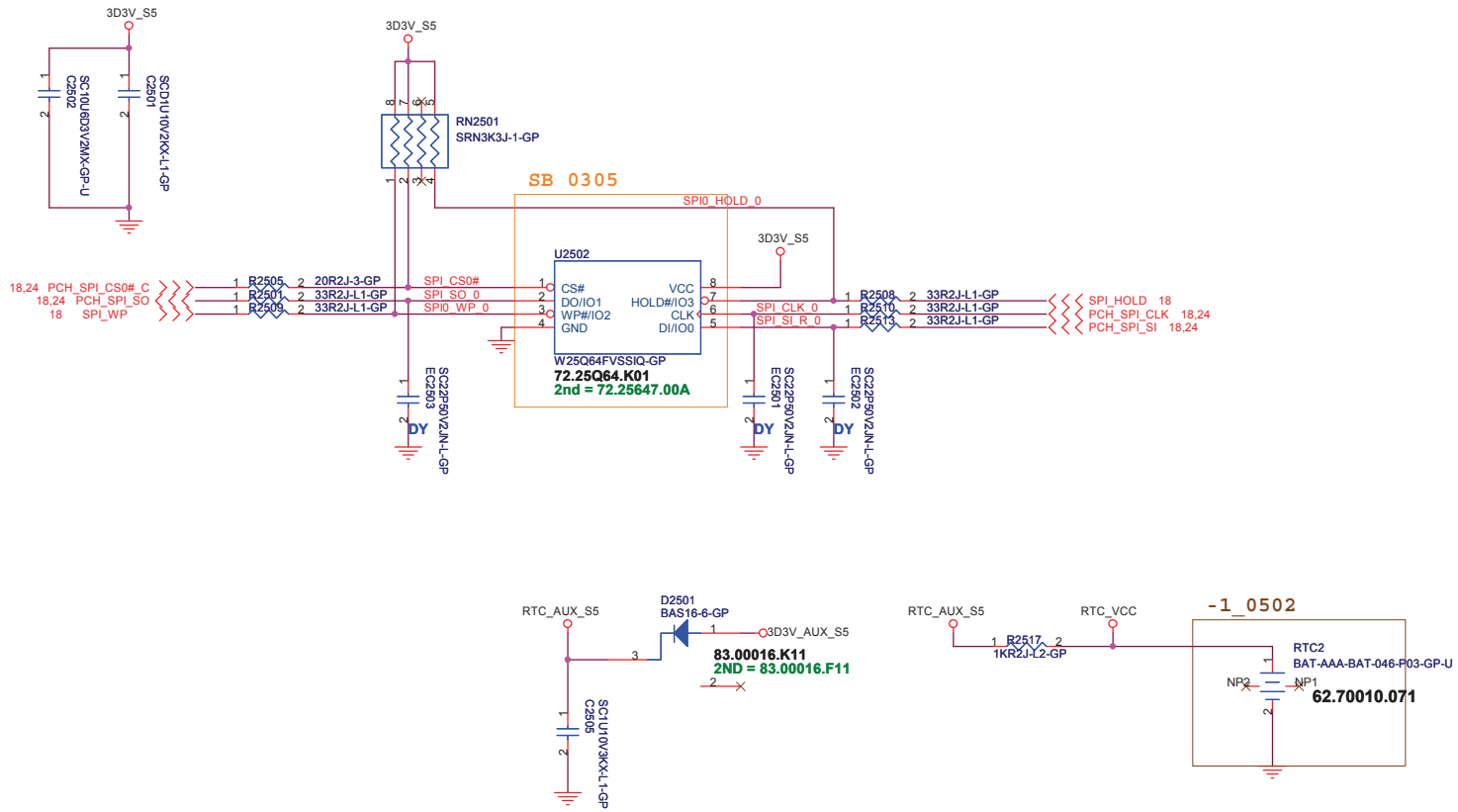
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_ITE8587

Size: Custom | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 24 of 102



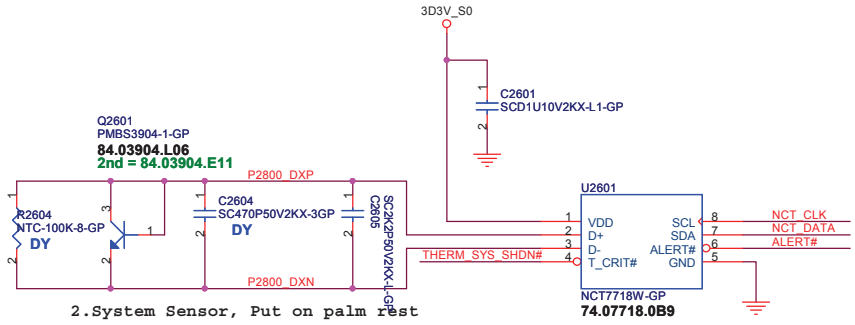
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash(KBC+PCH)/RTC***

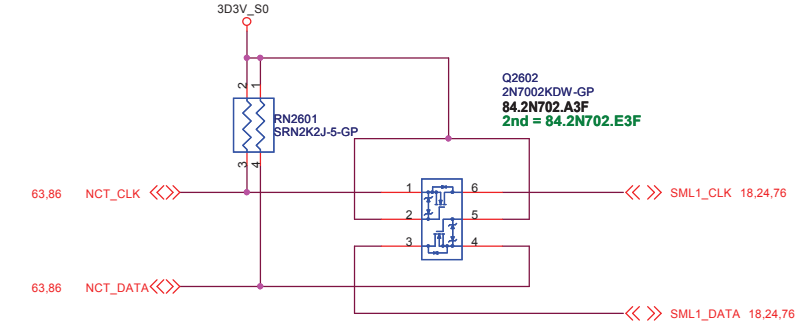
Size: A3 | Document Number: **WEEBILL_HW** | Rev: **SB**

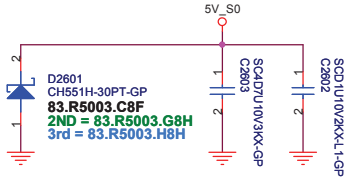
Date: Wednesday, September 18, 2013 | Sheet 25 of 102

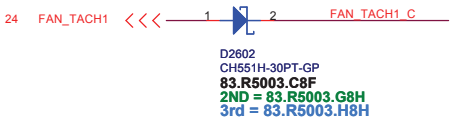


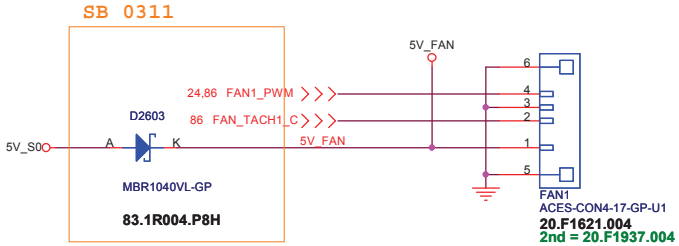
2.System Sensor, Put on palm rest

1.H/W T8 Shutdown







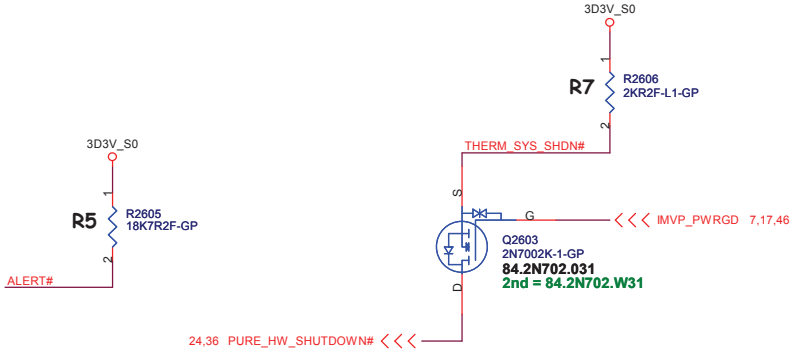


ALERT# /T_CRIT#
Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

T8=85 degree



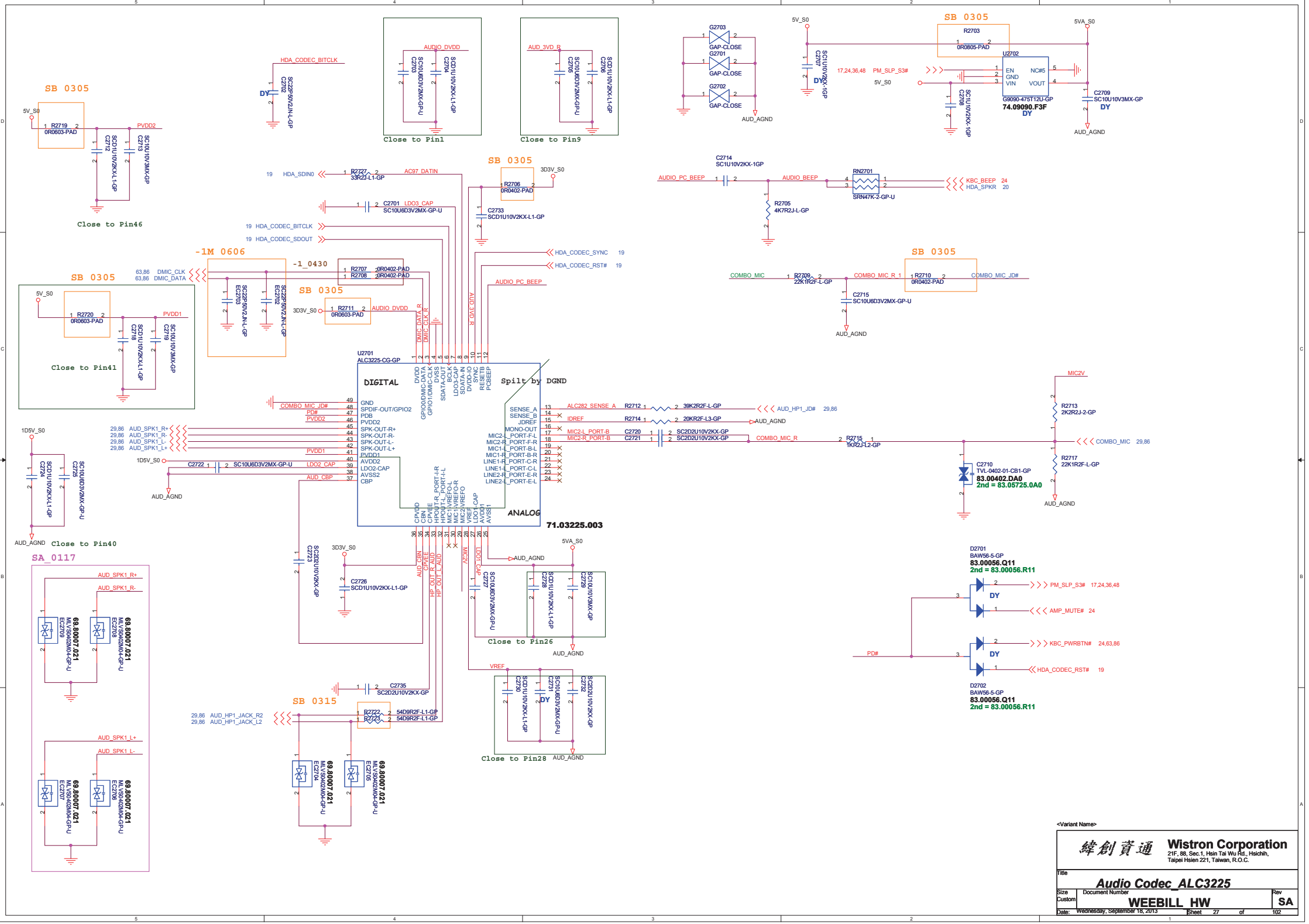
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793

Size: A3 | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 26 of 102


SB 0305
R2719 0R0603-PAD
PVDD2
Close to Pin46
HDA_CODEC_BITCLK
DY
AUDIO_DVDD
Close to Pin1
AUD_3VD_R
Close to Pin9
G2703 GAP-CLOSE
G2701 GAP-CLOSE
G2702 GAP-CLOSE
AUD_AGND
5V_S0
R2703 0R0805-PAD
5VA_S0
U2702
EN GND VIN NC#5 VOUT
G9090-475T12U-GP
74.09090.F3F
C2709 SC10U10V3MX-GP
PM_SLP_S3#
R2706 0R0402-PAD
3D3V_S0
C2714 SC1U10V2KX-1GP
AUDIO_PC_BEEP
RN2701 SRN47K-2-GP-U
KBC_BEEP
HDA_SPKR
R2705 4K7R2J-L-GP
HDA_SDIN0
AC97_DATIN
R2727 33R2J-L1-GP
C2701 LDO3_CAP SC10U6D3V2MX-GP-U
C2733 SCD1U10V2KX-L1-GP
HDA_CODEC_BITCLK
HDA_CODEC_SDOUT
HDA_CODEC_SYNC
HDA_CODEC_RST#
-1M 0606
-1_0430
R2707 0R0402-PAD
R2708 0R0402-PAD
DMIC_CLK
DMIC_DATA
SB 0305
R2720 0R0603-PAD
PVDD1
Close to Pin41
R2711 0R0603-PAD
AUDIO_DVDD
COMBO_MIC
R2709 22K1R2F-L-GP
COMBO_MIC_R_1
R2710 0R0402-PAD
COMBO_MIC_JD#
C2715 SC10U6D3V2MX-GP-U
U2701
ALC3225-CG-GP
DIGITAL
Spilt by DGND
ANALOG
71.03225.003
COMBO_MIC_JD#
PD#
PVDD2
AUD_SPK1_R+
AUD_SPK1_R-
AUD_SPK1_L-
AUD_SPK1_L+
PVDD1
LDO2_CAP
AUD_CBP
ALC282_SENSE_A
R2712 39K2R2F-L-GP
AUD_HP1_JD#
IDREF
R2714 20KR2F-L3-GP
MIC2-L_PORT-B
MIC2-R_PORT-B
C2720 SC2D2U10V2KX-GP
C2721 SC2D2U10V2KX-GP
COMBO_MIC_R
R2715 1KR2J-L2-GP
MIC2V
R2713 2K2R2J-2-GP
COMBO_MIC
R2717 22K1R2F-L-GP
C2710 TVL-0402-01-CB1-GP
83.00402.DA0
2nd = 83.05725.0A0
1D5V_S0
C2722 SC10U6D3V2MX-GP-U
Close to Pin40
SA_0117
69.80007.021
MLVS0402M04-GP-U
EC2709
EC2708
EC2707
EC2704
EC2705
SB 0315
R2722 54D9R2F-L1-GP
R2723 54D9R2F-L1-GP
HP_OUT_R_AUD
HP_OUT_L_AUD
C2735 SC2D2U10V2KX-GP
C2726 SCD1U10V2KX-L1-GP
C2723 SC2D2U10V2KX-GP
C2727 SC10U6D3V2MX-GP-U
C2728 SCD1U10V2KX-L1-GP
C2729 SC10U10V3MX-GP
Close to Pin26
VREF
C2730 SCD1U10V2KX-L1-GP
C2731 SC10U6D3V2MX-GP-U
C2732 SC2D2U10V2KX-GP
Close to Pin28
D2701 BAW56-5-GP
83.00056.Q11
2nd = 83.00056.R11
AMP_MUTE#
KBC_PWRBTN#
HDA_CODEC_RST#
D2702 BAW56-5-GP
83.00056.Q11
2nd = 83.00056.R11
AUD_HP1_JACK_R2
AUD_HP1_JACK_L2
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec_ALC3225
Size Custom
Document Number
WEEBILL_HW
Rev SA
Date: Wednesday, September 18, 2013
Sheet 27 of 102

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<Variant Name>

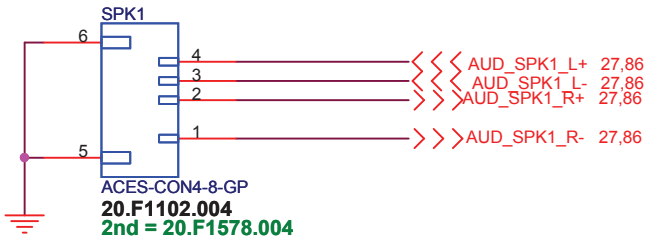
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio AMP_1001

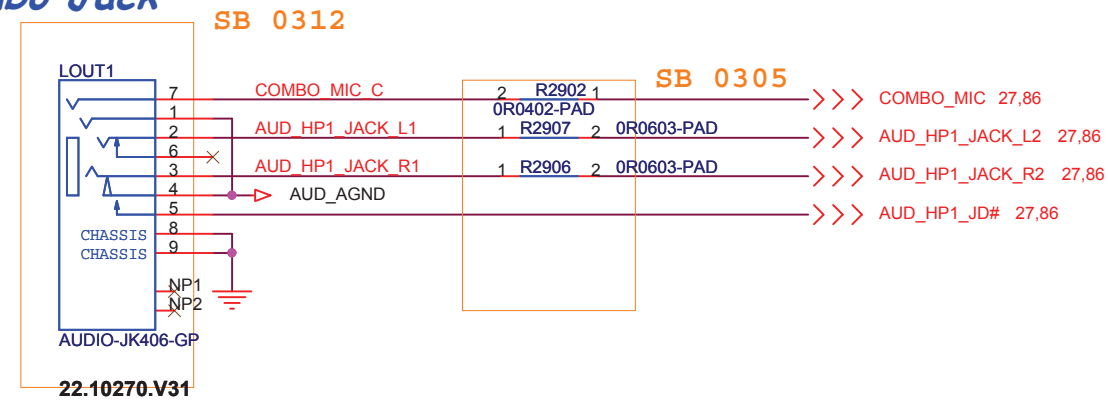
Size	Document Number	Rev
A4	WEEBILL_HW	SA

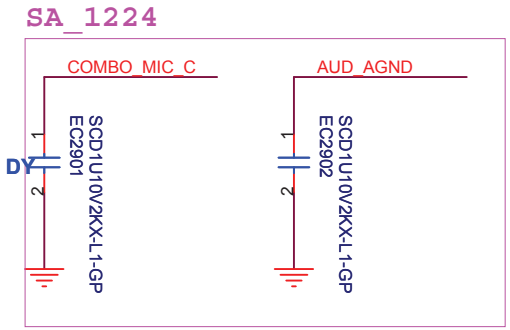
Date: Wednesday, September 18, 2013 Sheet 28 of 102

Speaker



Combo Jack





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 29 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN(RTL8411)

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 30 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(LAN+VGA) CONNECTOR

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 31 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)Card Reader

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 32 of 102

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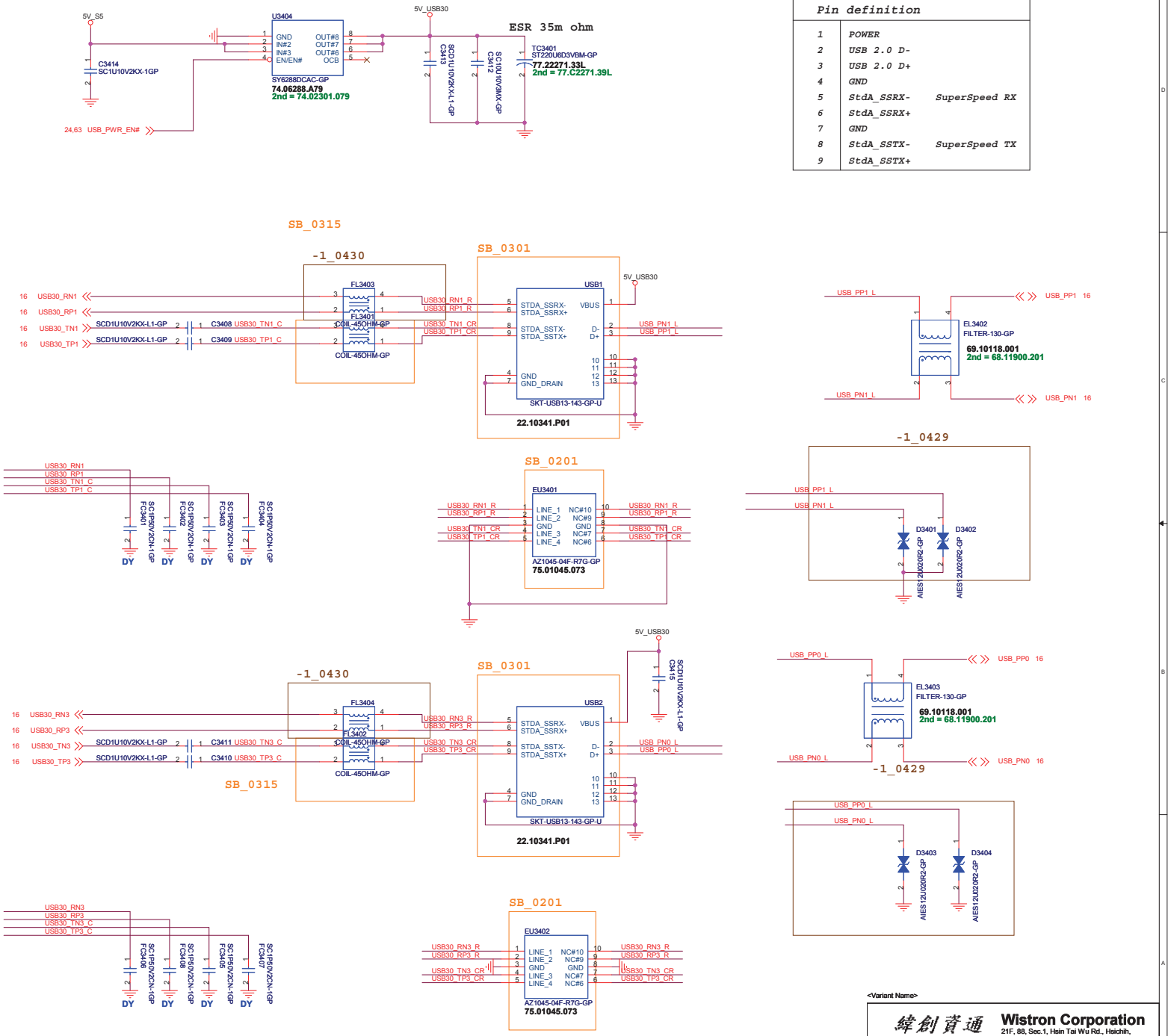
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 33 of 102



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 2.0 / 3.0 Port**

Size: Custom | Document Number: **WEEBILL_HW** | Rev: **SB**

Date: Wednesday, September 18, 2013 | Sheet 34 of 102

Blanking

<Variant Name>

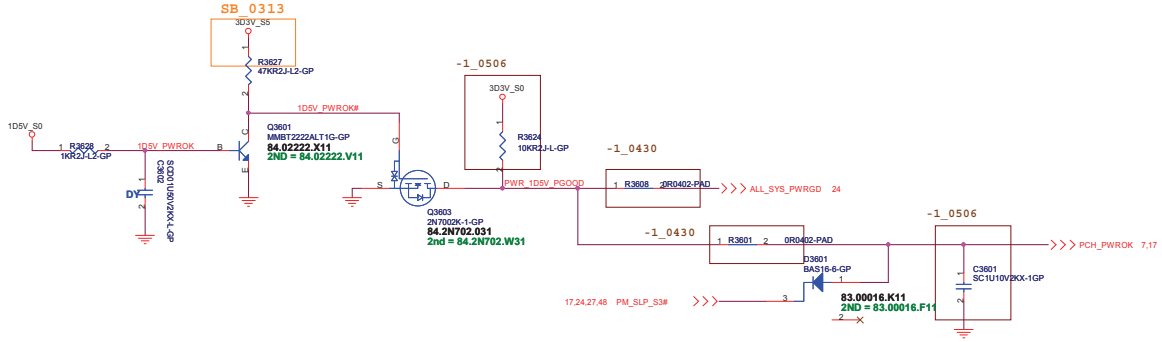
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CHARGER

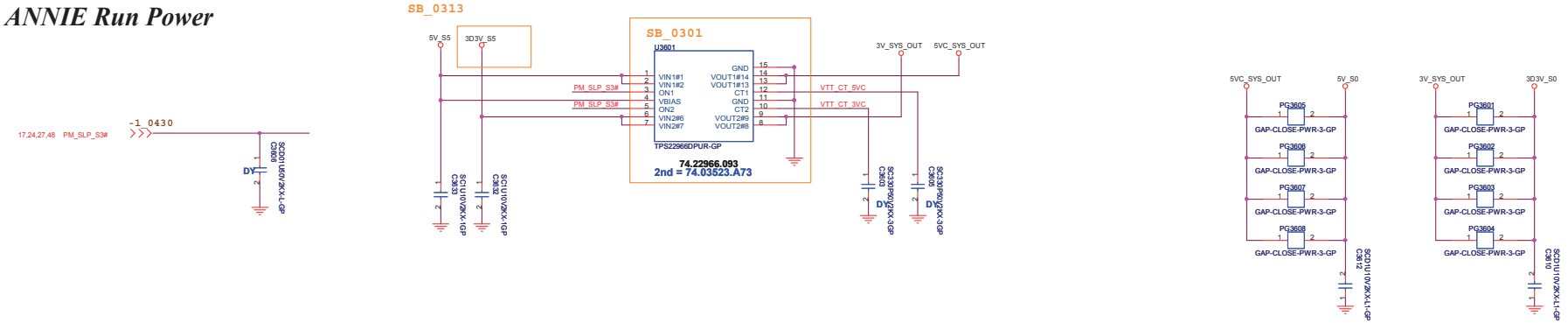
Size	Document Number	Rev
A4	WEEBILL_HW	SA

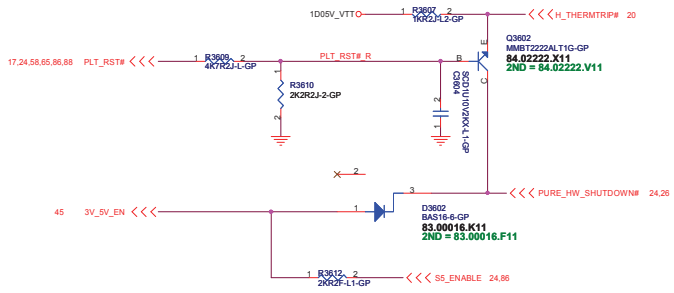
Date: Wednesday, September 18, 2013 Sheet 35 of 102

Power Sequence

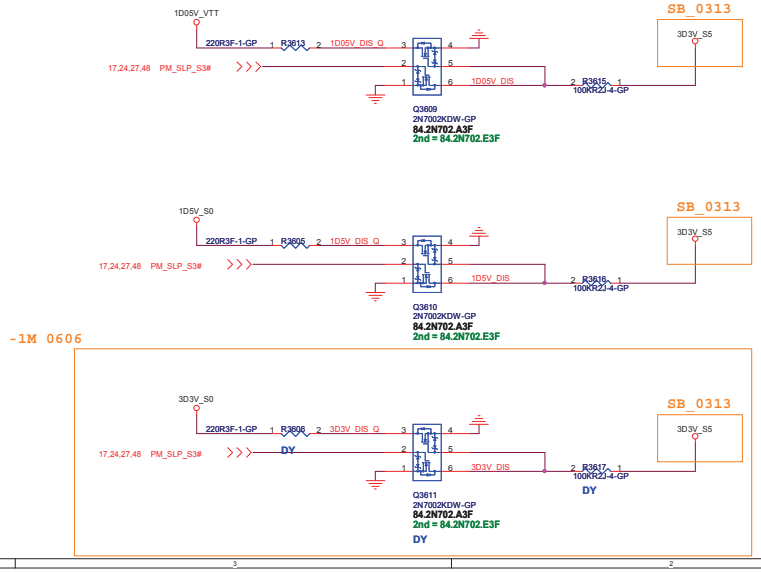


ANNIE Run Power





Discharge circuit



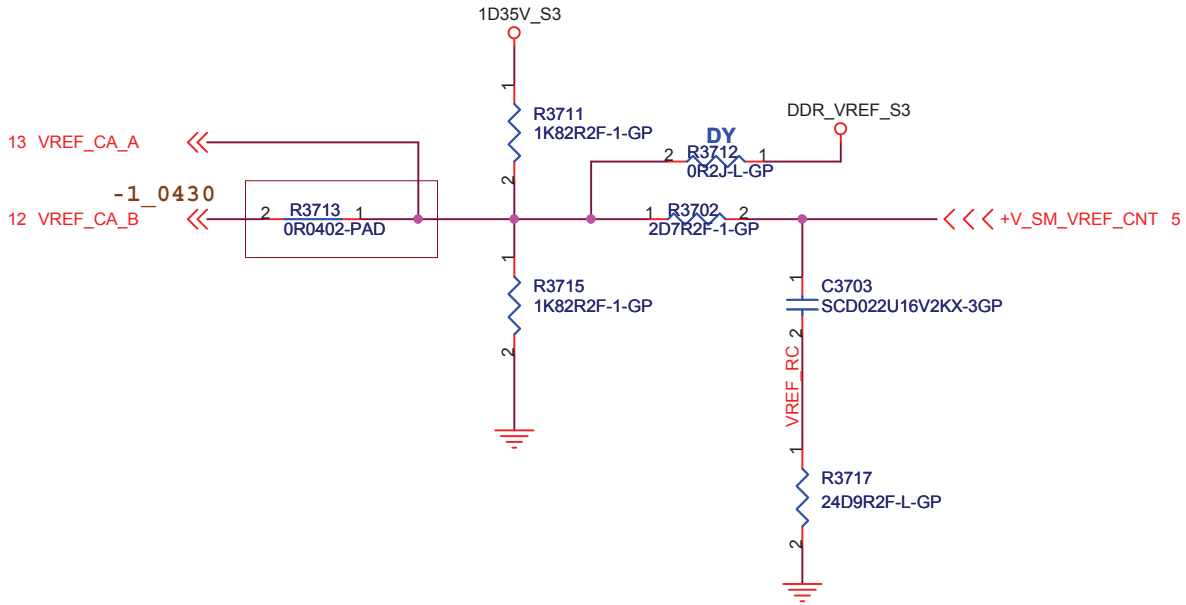
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 36 of 102



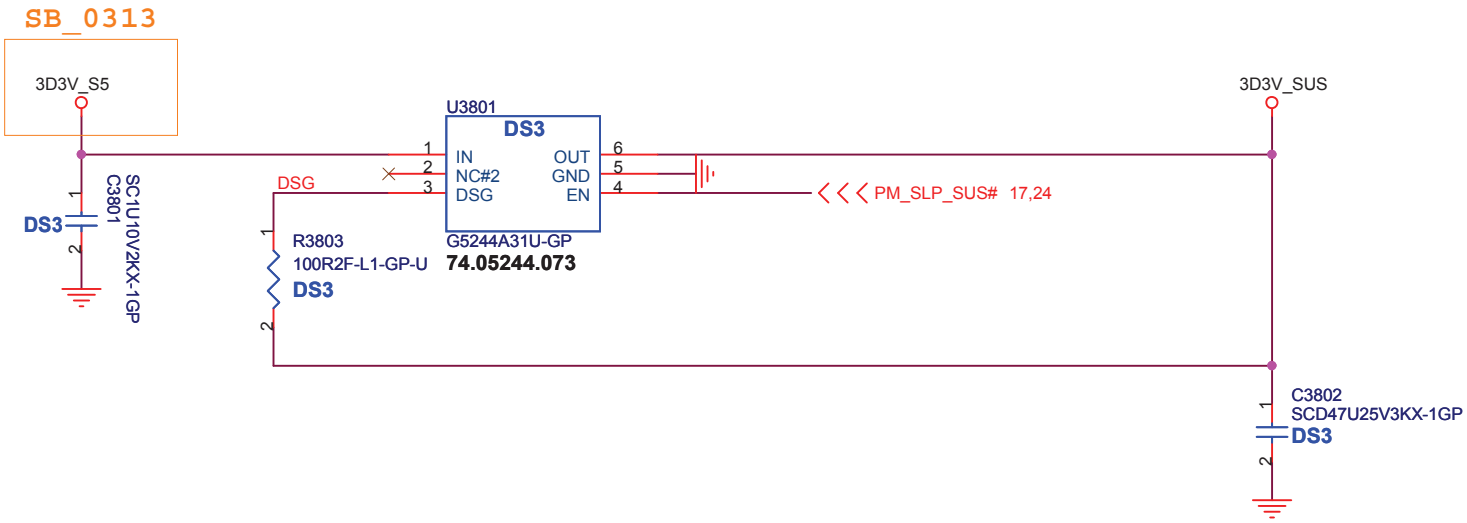
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
ADAPTER OCP / S3 reduction

Size	Document Number	Rev
A4	**WEEBILL_HW**	**SA**

Date: Wednesday, September 18, 2013 Sheet 37 of 102



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DS3***

Size	Document Number	Rev
A4	**WEEBILL_HW**	**SA**

Date: Wednesday, September 18, 2013 Sheet 38 of 102

Power Sequence

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***1D05_M***	
Size A4	Document Number **WEEBILL_HW**	Rev **SA**
Date: Wednesday, September 18, 2013	Sheet 39 of 102	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Connected Standby1

Size	Document Number	Rev
A4	**WEEBILL_HW**	**SA**

Date: Wednesday, September 18, 2013 Sheet 40 of 102

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected Standby2*

Size	Document Number	Rev
A4	WEEBILL_HW	SA

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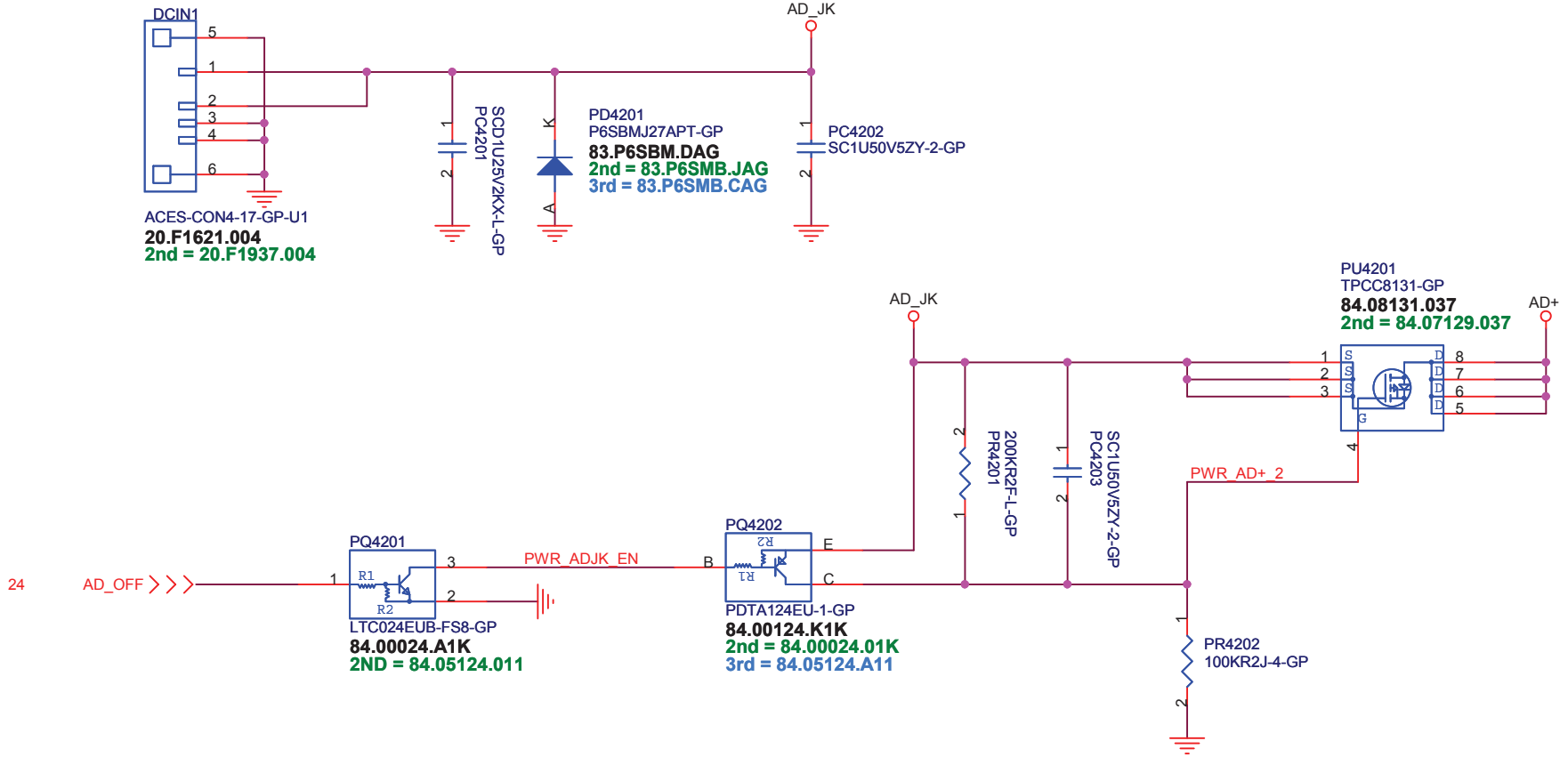
0.4 pitch, AWG#28:2.0 A/pin



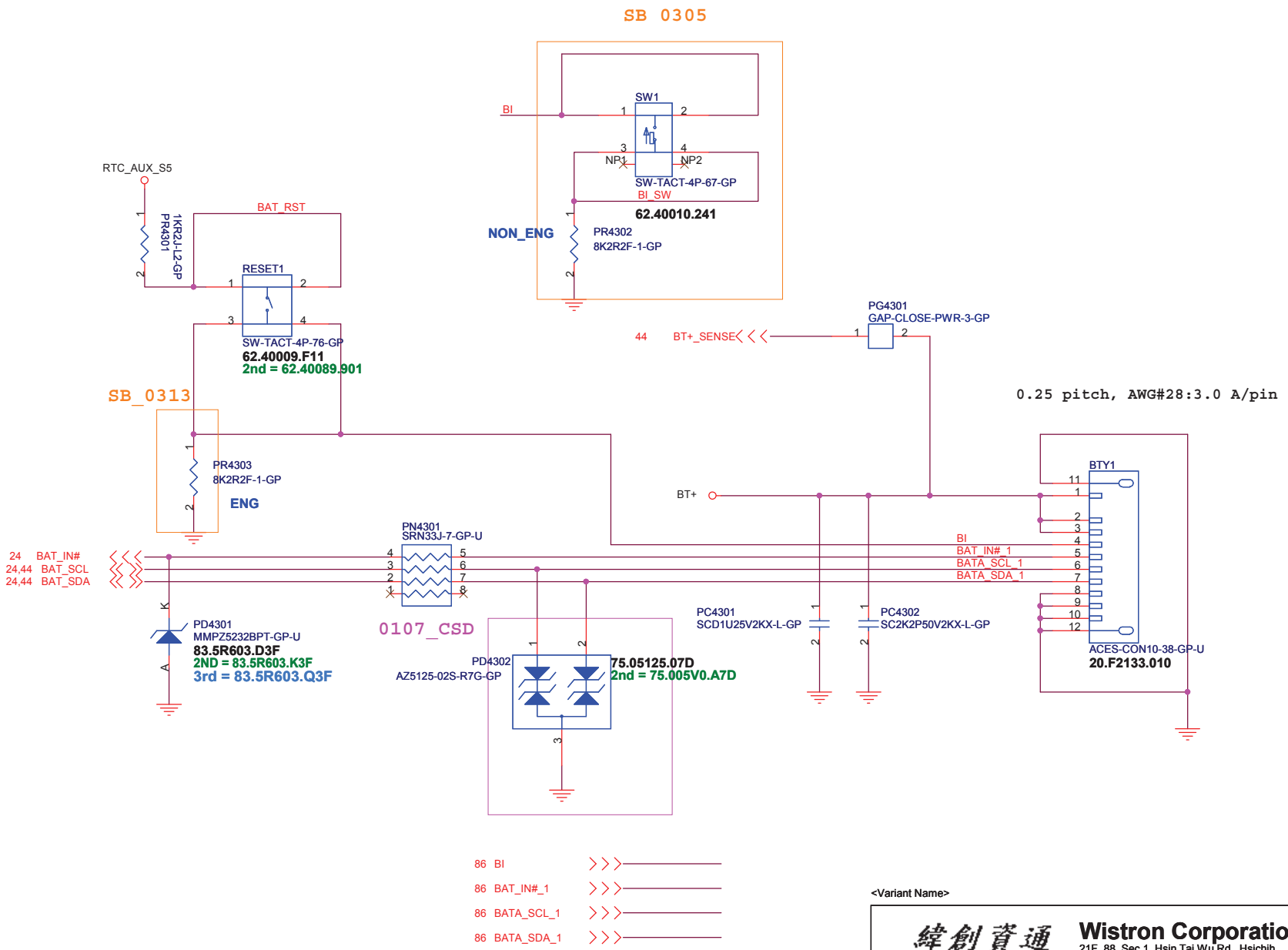
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DCIN JACK***

Size	Document Number	Rev
A4	**WEEBILL_HW**	**SA**

Date: Wednesday, September 18, 2013 Sheet 42 of 102



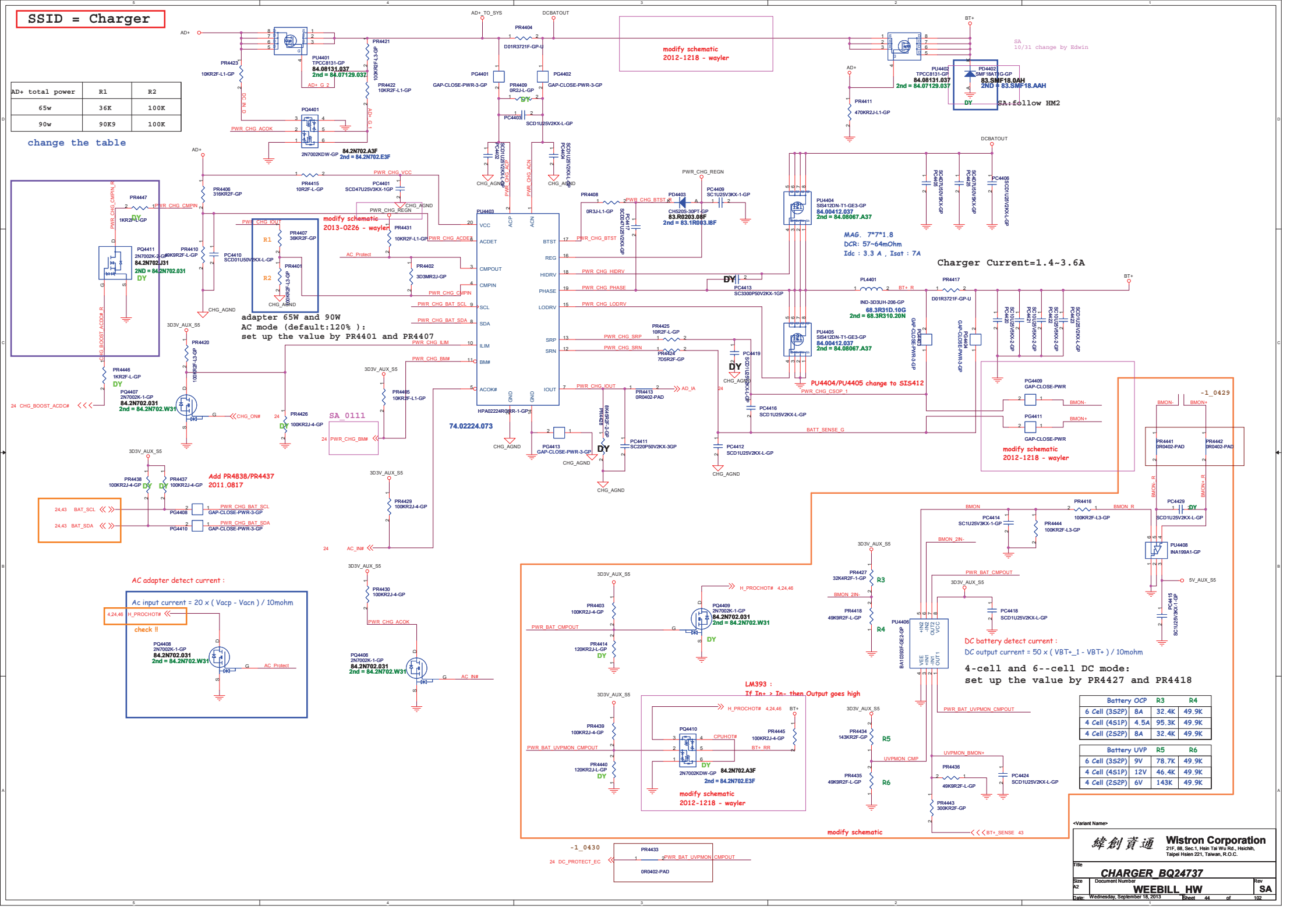
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

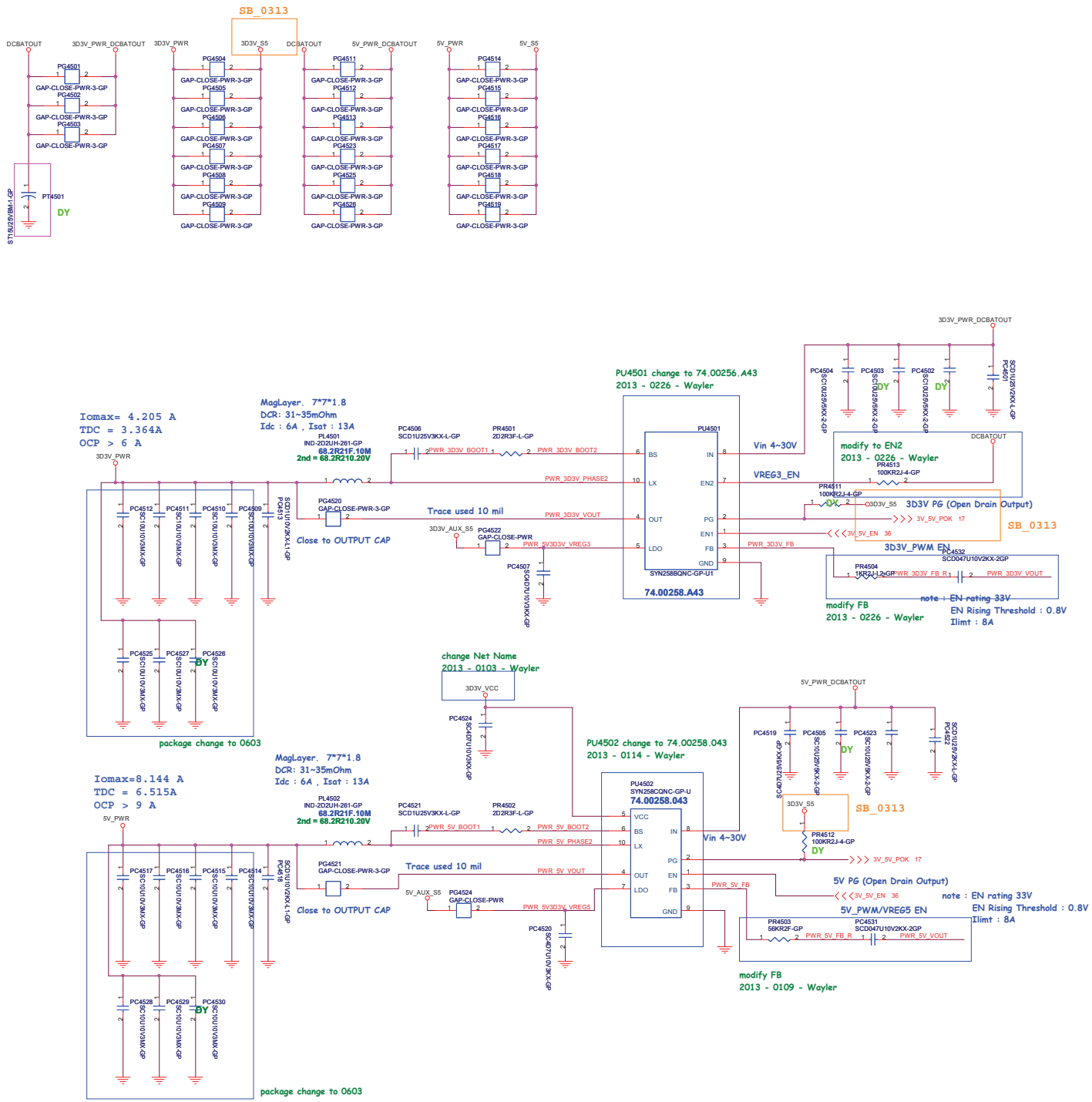
Title: **BATT CONN**

Size	Document Number	Rev
Custom	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 43 of 102


SSID = Charger
AD+ total power | R1 | R2
65w | 36K | 100K
90w | 90K9 | 100K
change the table
modify schematic 2012-1218 - wayler
SA 10/31 change by Edwin
SA:follow HM2
PU4401 TPCC8131-GP 84.08131.037 2nd = 84.07129.037
PD4402 SMF18A1G-GP 83.SMF18.0AH 2nd = 83.SMF18.AAH
PQ4401 2N7002KDW-GP 84.2N702.A3F 2nd = 84.2N702.E3F
modify schematic 2013-0226 - wayler
PU4403 HPA02224RQ8R-1-GP 74.02224.073
PU4404 SIS412DN-T1-GE3-GP 84.00412.037 2nd = 84.08067.A37
PU4405 SIS412DN-T1-GE3-GP 84.00412.037 2nd = 84.08067.A37
MAG. 7*7*1.8
DCR: 57~64mOhm
Idc : 3.3 A , Isat : 7A
Charger Current=1.4~3.6A
PU4404/PU4405 change to SIS412
adapter 65W and 90W
AC mode (default:120%):
set up the value by PR4401 and PR4407
SA_0111
Add PR4838/PR4437 2011.0817
AC adapter detect current :
Ac input current = 20 x (Vacp - Vacn) / 10mohm
check !!
LM393 :
If In+ > In- then Output goes high
modify schematic 2012-1218 - wayler
-1_0429
-1_0430
DC battery detect current :
DC output current = 50 x (VBT+_1 - VBT+) / 10mohm
4-cell and 6--cell DC mode:
set up the value by PR4427 and PR4418
Battery OCP | R3 | R4
6 Cell (3S2P) | 8A | 32.4K | 49.9K
4 Cell (4S1P) | 4.5A | 95.3K | 49.9K
4 Cell (2S2P) | 8A | 32.4K | 49.9K
Battery UVP | R5 | R6
6 Cell (3S2P) | 9V | 78.7K | 49.9K
4 Cell (4S1P) | 12V | 46.4K | 49.9K
4 Cell (2S2P) | 6V | 143K | 49.9K
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CHARGER_BQ24737
WEEBILL_HW
SA
Wednesday, September 18, 2013
Sheet 44 of 102

SSID = PWR.Plane.Regulator_3p3v5v



BVLGARI_WIFI

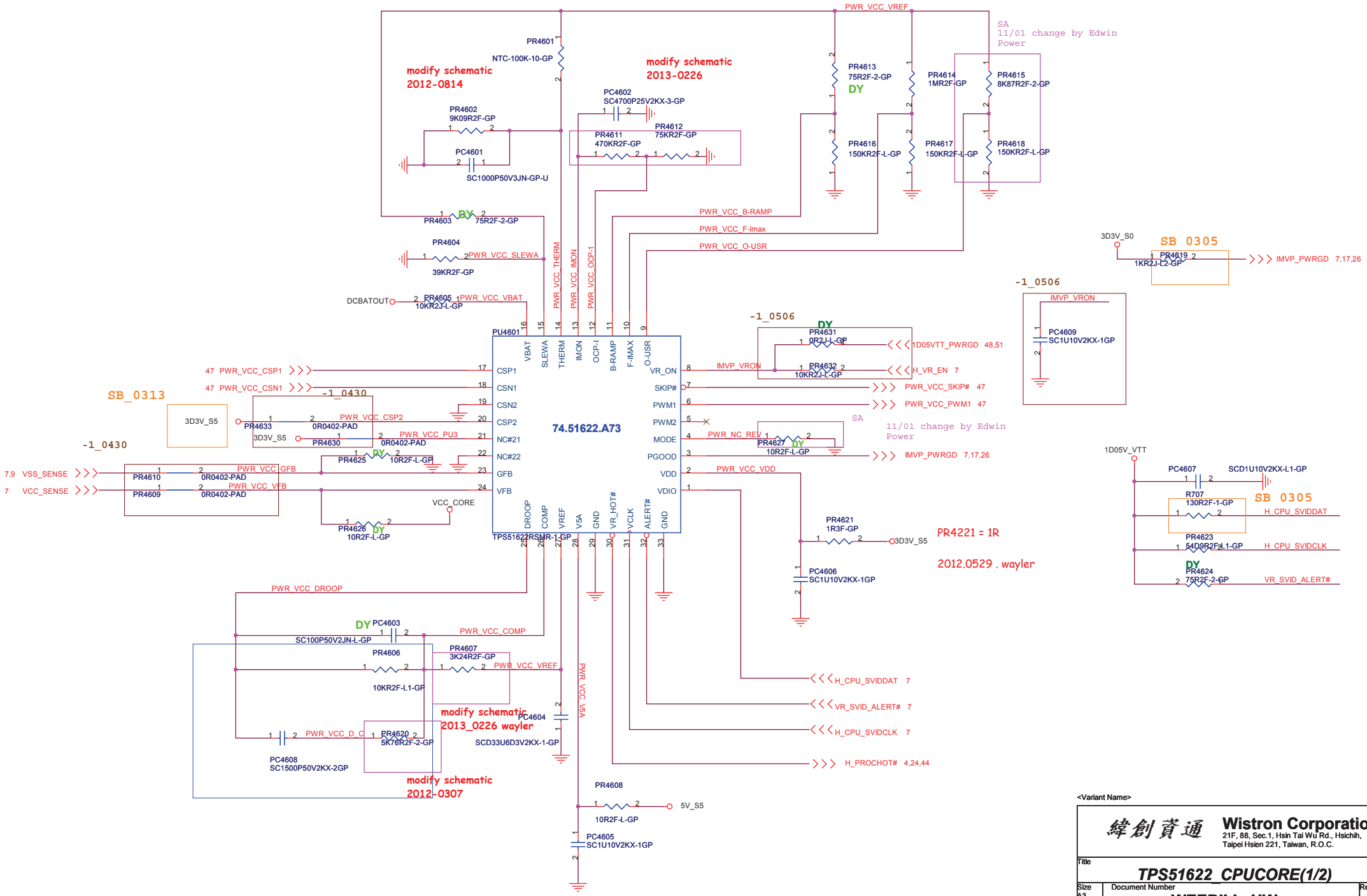
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51225_5V/3D3V

Size: Custom | Document Number: BVLGARI_WIFI | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 45 of 102

SSID = CPU.Regulator

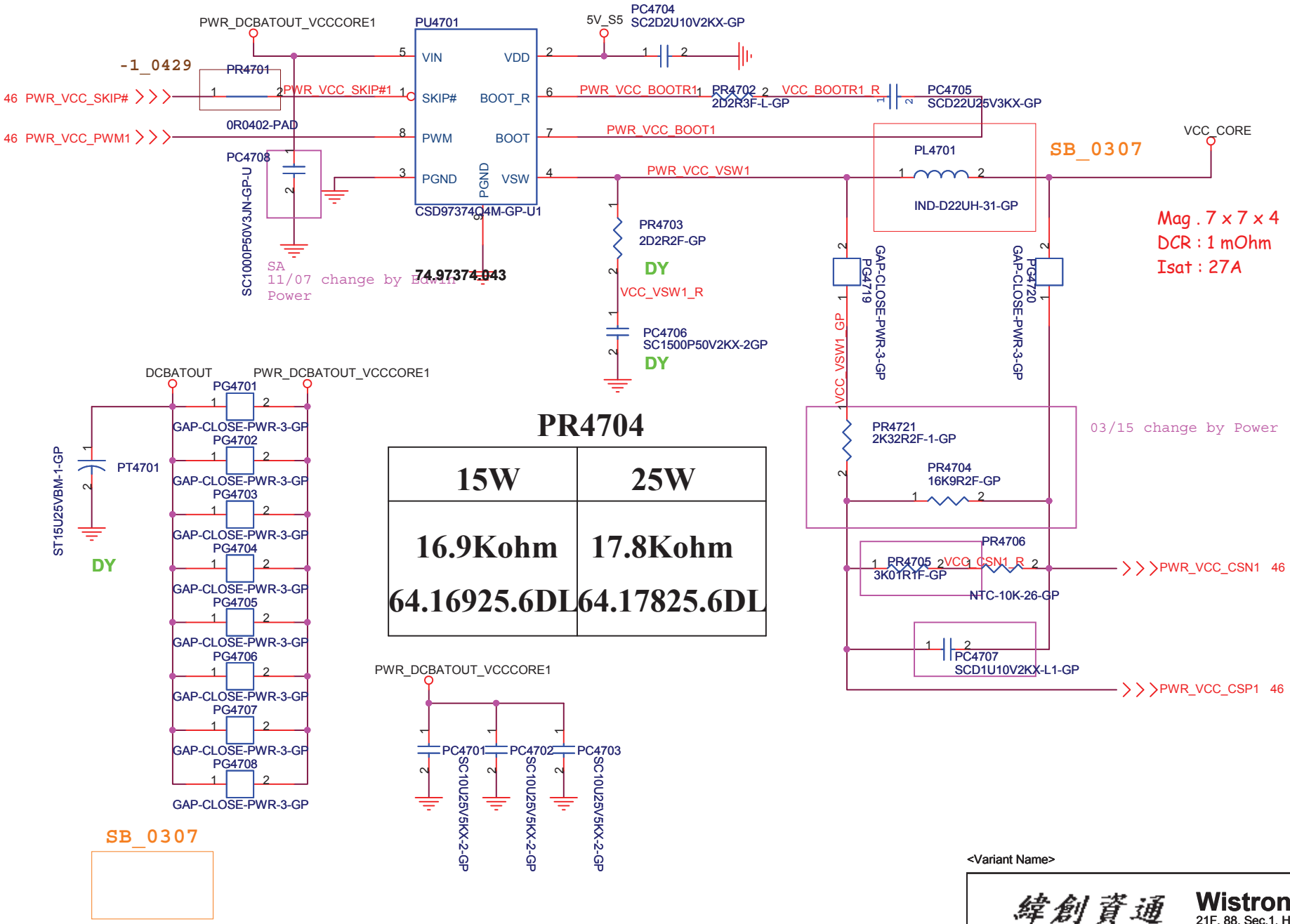


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622_CPUCORE(1/2)

Size: A3 | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 46 of 102



PR4704

15W	25W
16.9Kohm	17.8Kohm
64.16925.6DL	64.17825.6DL

<Variant Name>

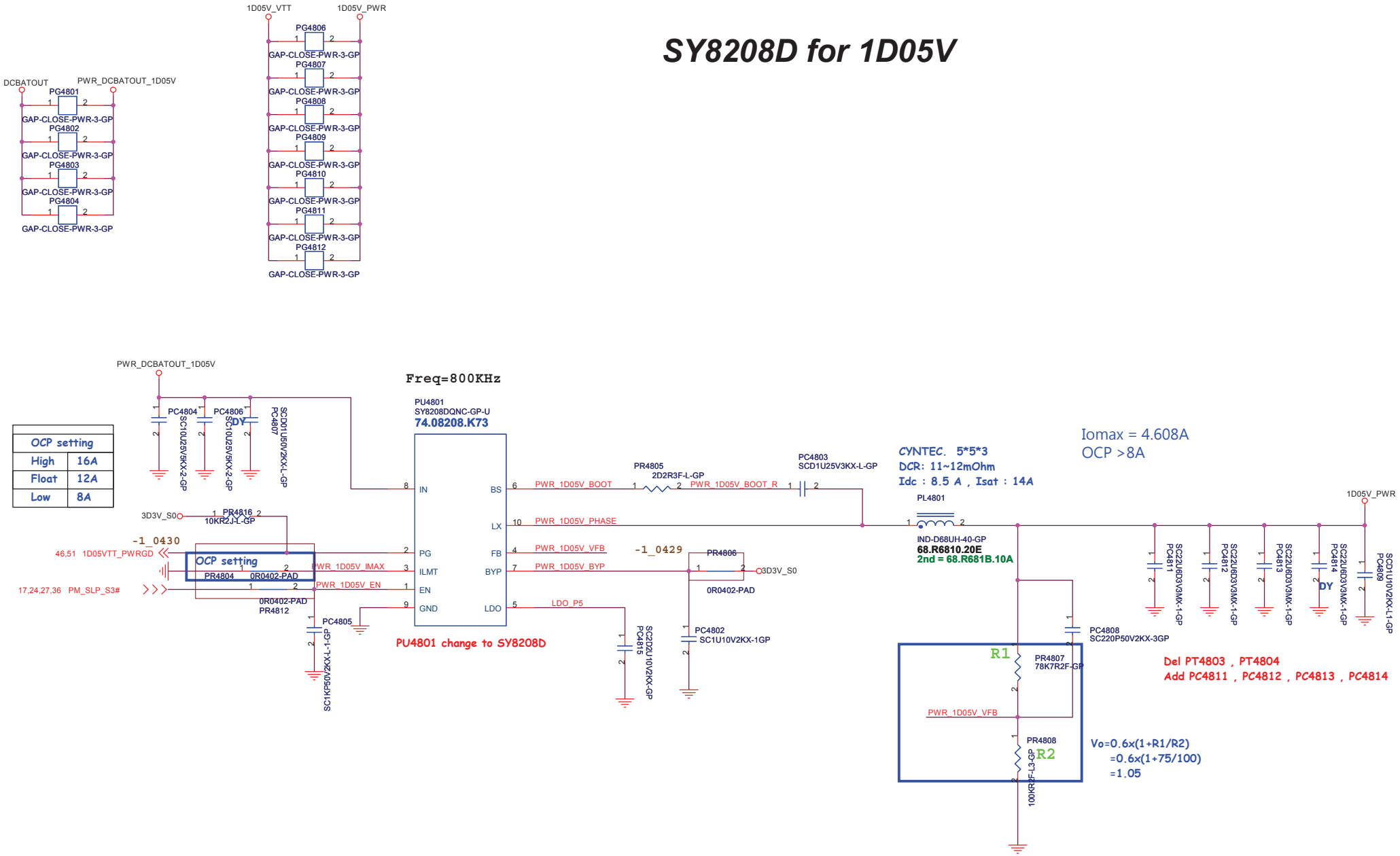
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622_CPUCORE(2/2)

Size: A4 | Document Number: WEEBILL_HW | Rev: SB

Date: Wednesday, September 18, 2013 | Sheet 47 of 102

SY8208D for 1D05V



OCP setting	
High	16A
Float	12A
Low	8A

<Variant Name>

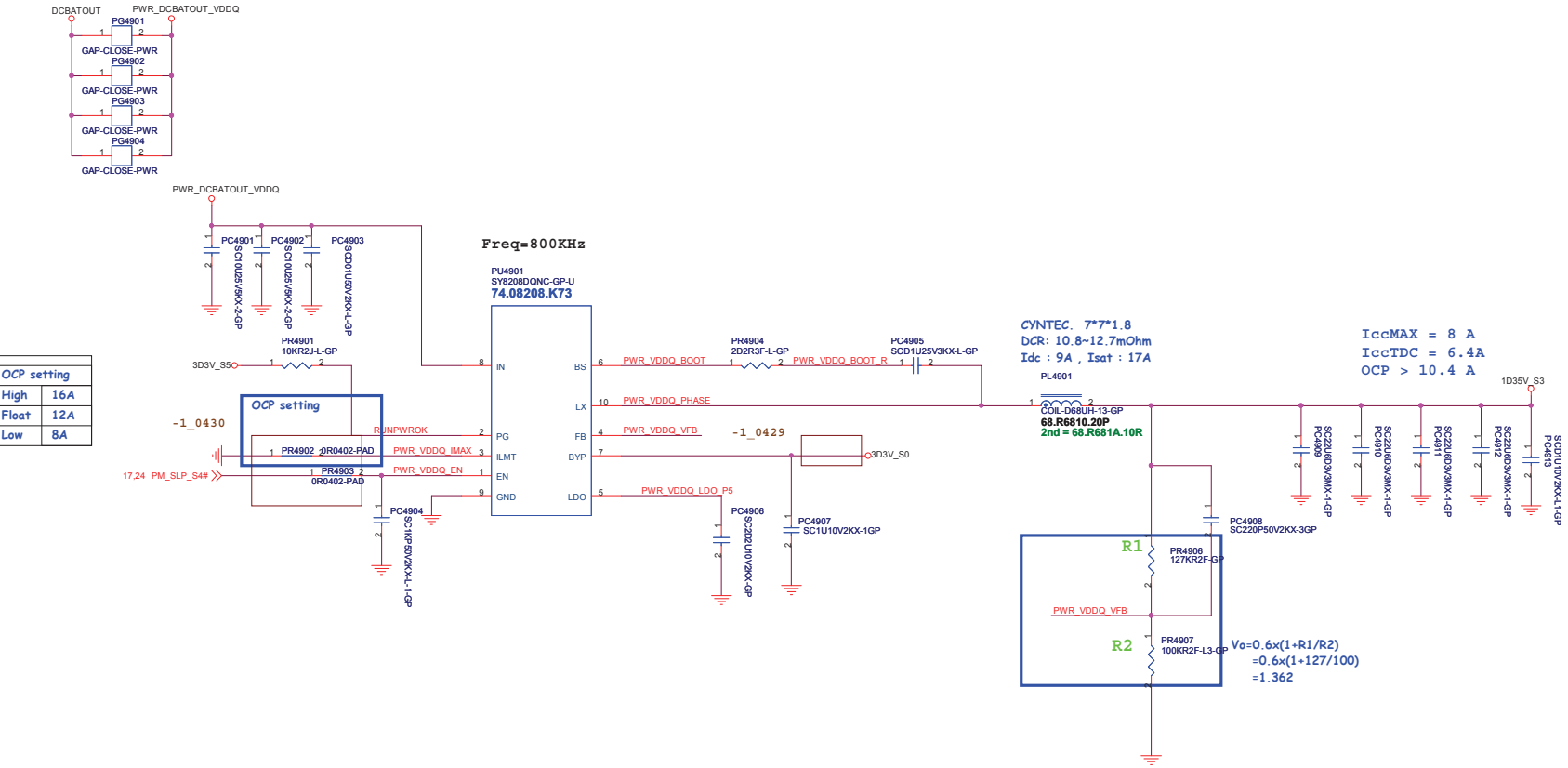
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC_1D05V(SY8208D)

Size: A3 | Document Number: WEEBILL_HW | Rev: SA

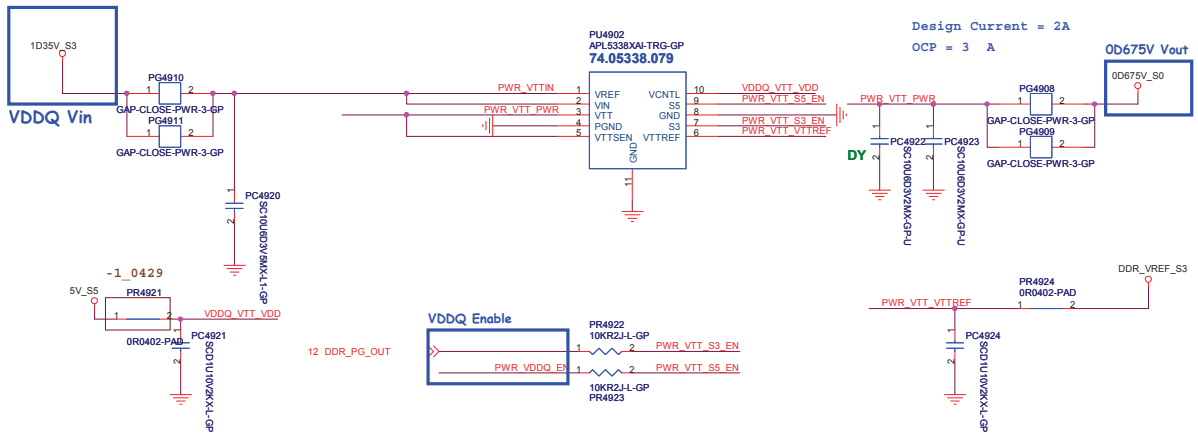
Date: Wednesday, September 18, 2013 | Sheet 48 of 102

SSID = PWR.Plane.Regulator_1p35v0p675v



OCP setting	
High	16A
Float	12A
Low	8A

+0.675VS
Iomax: 1.2A



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8208D+G2997(VDDQ_VTT)

Size: Custom | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 49 of 102

Blanking

<Variant Name>

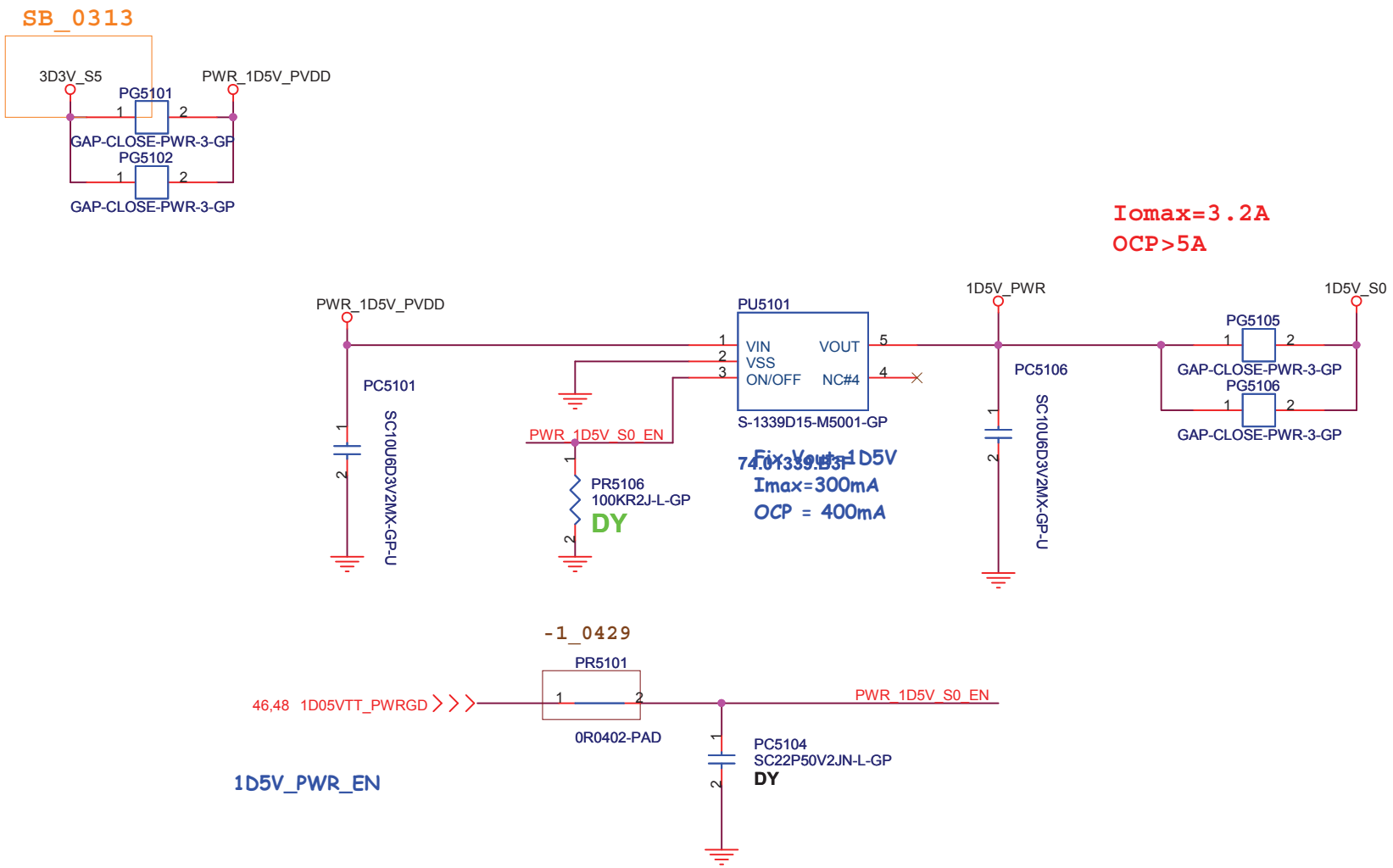
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *iSSD power*

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 50 of 102

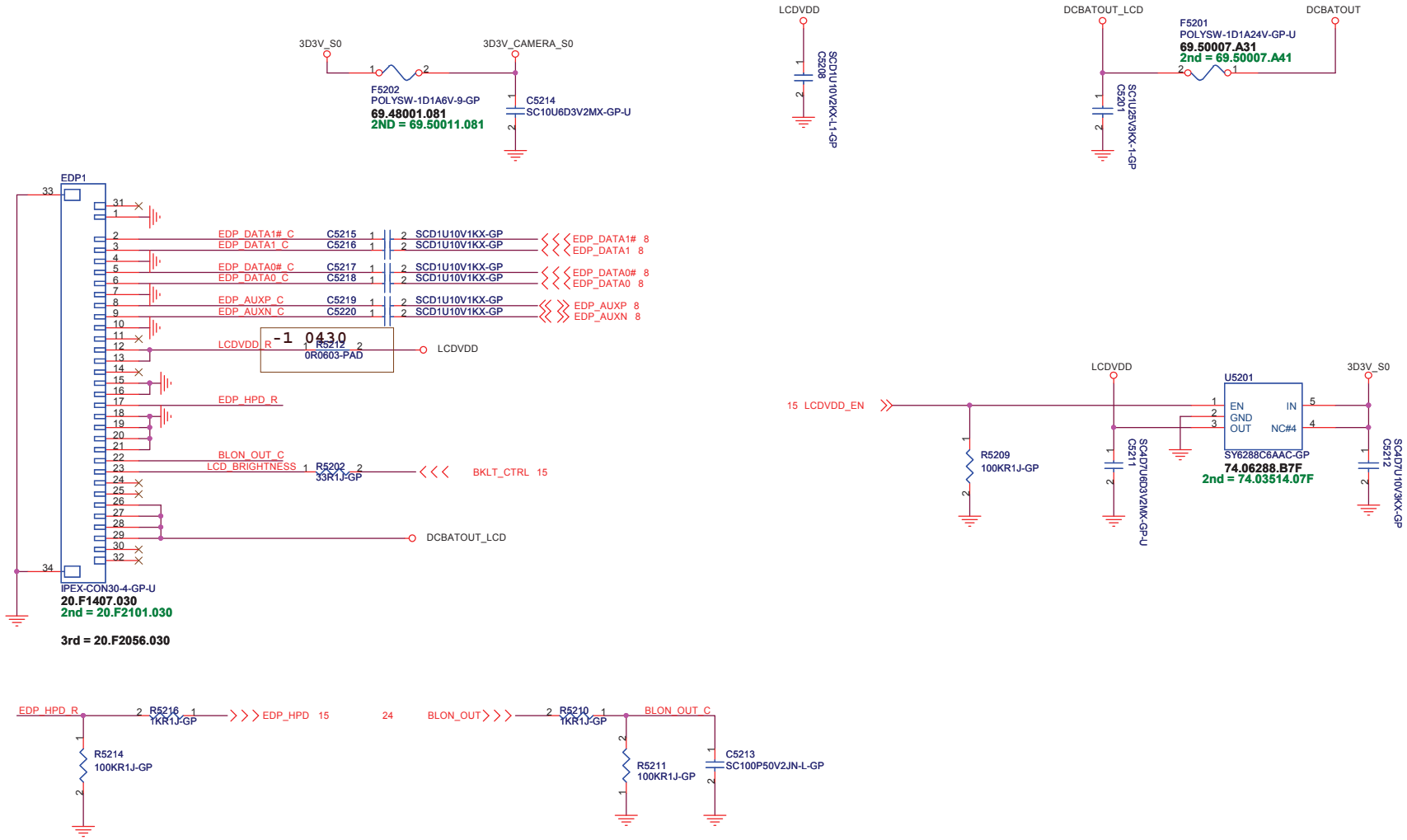
SYW232 for 1D5V_S0



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D5V_S0 SYW232	
Size A4	Document Number WEEBILL_HW	Rev SA
Date: Wednesday, September 18, 2013	Sheet 51 of 102	



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LCD Connector***
Size A3	Document Number **WEEBILL_HW** Rev **SA**
Date: Wednesday, September 18, 2013	Sheet 52 of 102

Blanking

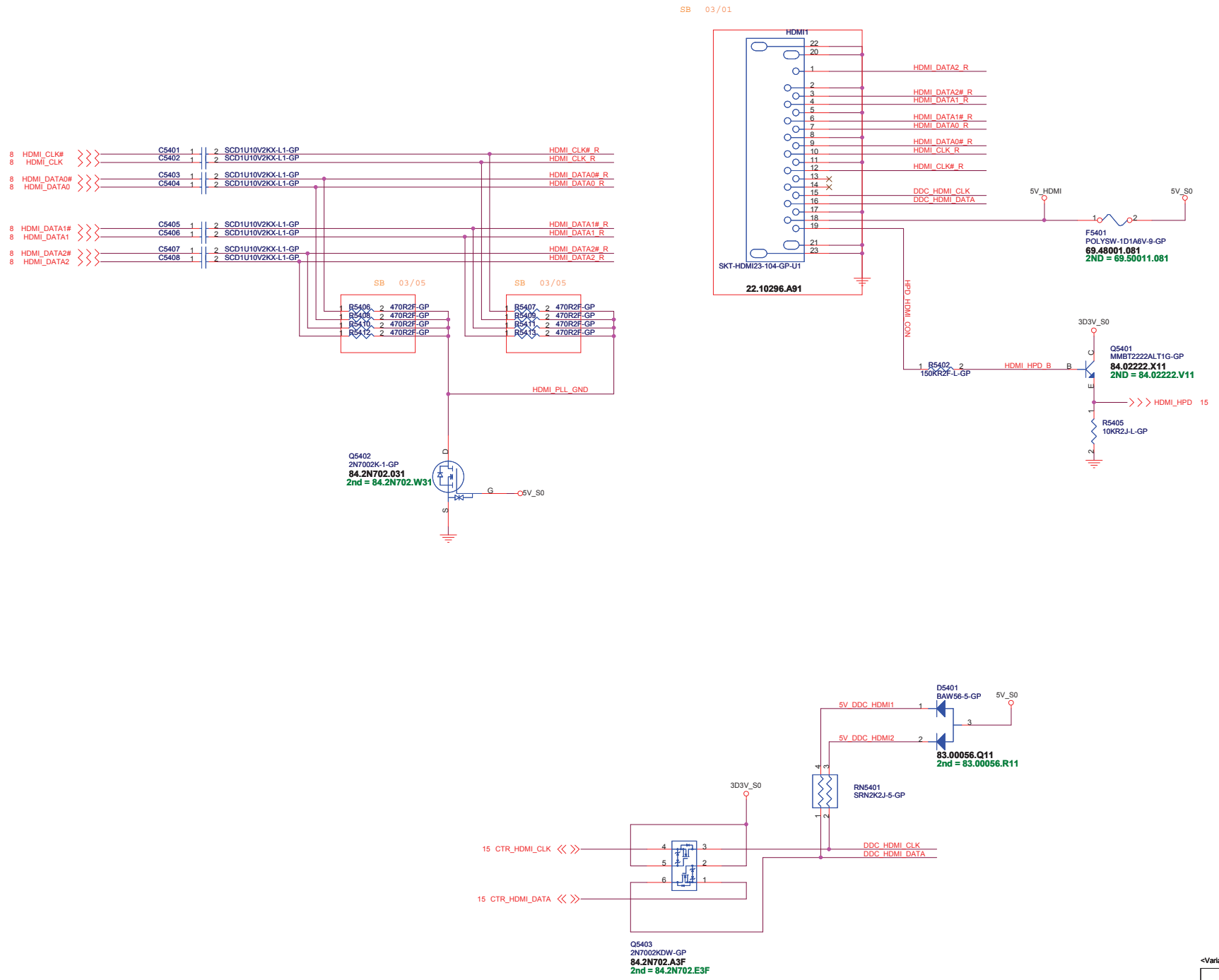
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CRT Board Connector

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 53 of 102



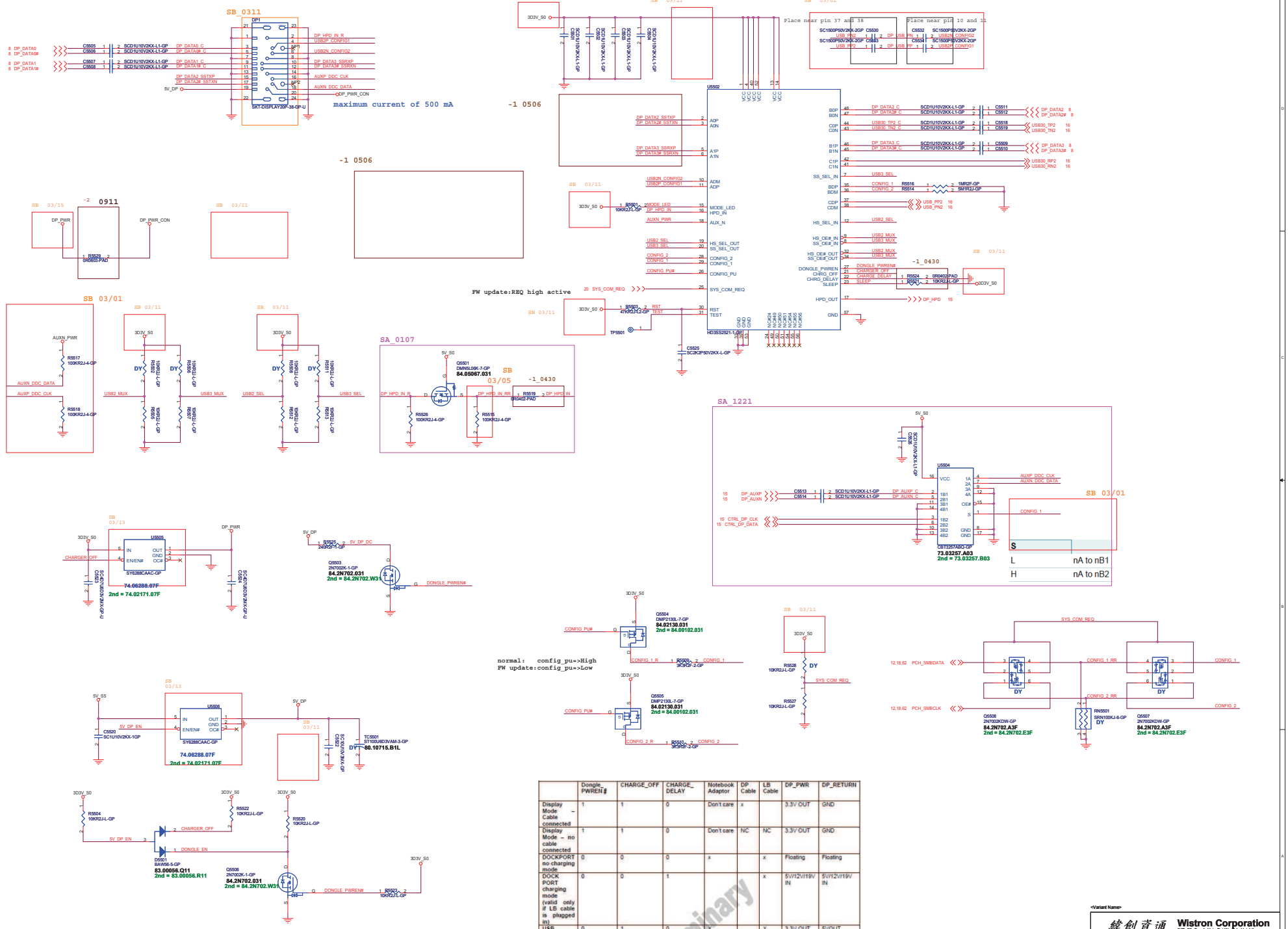
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDMI Level Shifter/Connector***

Size	Document Number	Rev
Custom	**WEEBILL_HW**	**SA**

Date: Wednesday, September 18, 2013 Sheet 54 of 102



	Dongle_PWREN#	CHARGE_OFF	CHARGE_DELAY	Notebook Adaptor	DP Cable	LB Cable	DP_PWR	DP_RETURN
Display Mode – Cable connected	1	1	0	Don't care	x		3.3V OUT	GND
Display Mode – no cable connected	1	1	0	Don't care	NC	NC	3.3V OUT	GND
DOCKPORT no charging mode	0	0	0	x		x	Floating	Floating
DOCK PORT charging mode (valid only if LB cable is plugged in)	0	0	1			x	5V/12V/19V IN	5V/12V/19V IN
USB Charging/ Dongle mode	0	1	0	X		X	3.3V OUT	5VOUT

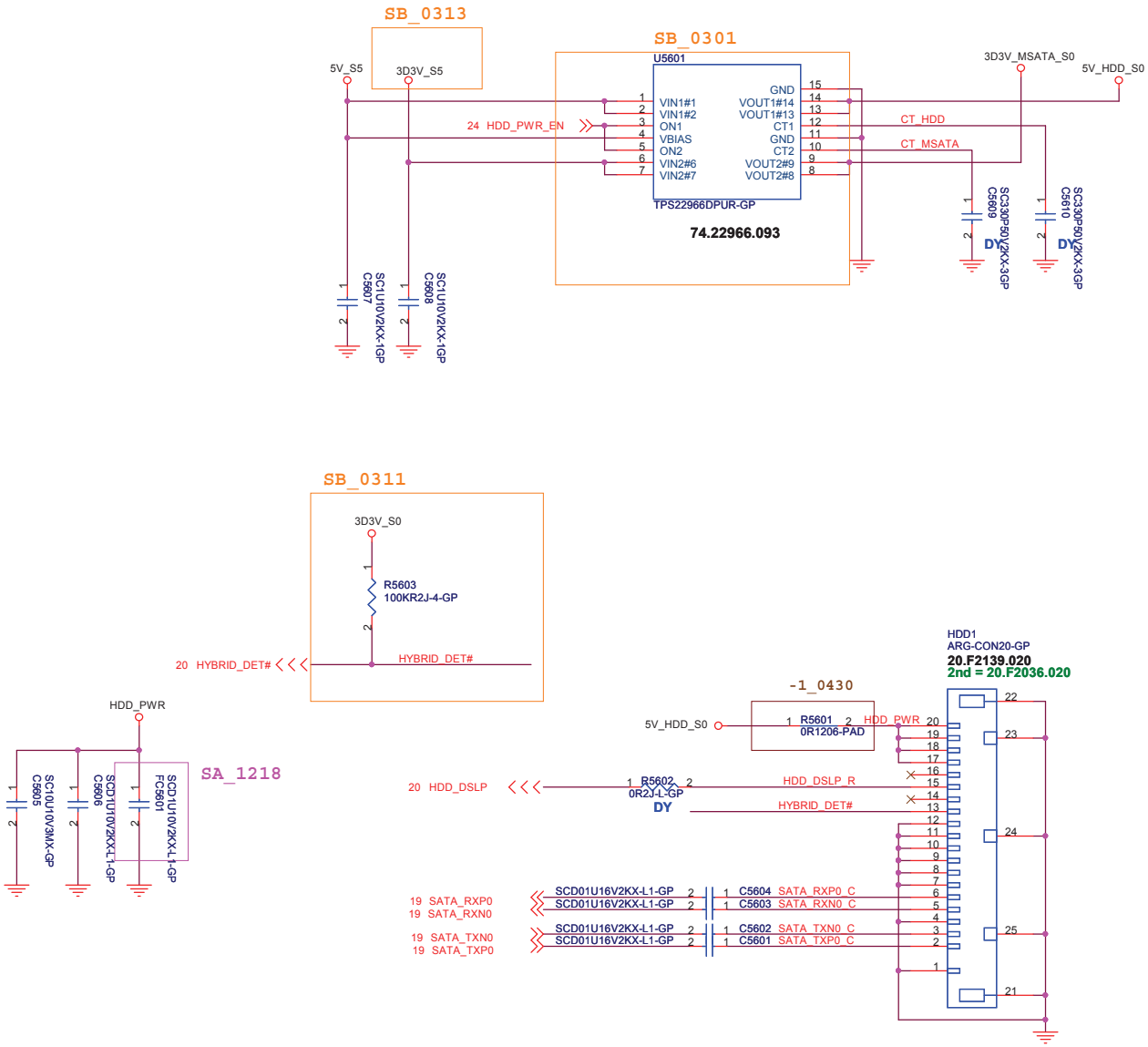
Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: Display Port

Size: Custom | Document Number: WEEBILL_HW | Rev: SA

Date: Wednesday, September 18, 2013 | Sheet 55 of 102



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD / ODD / NGFF_SSD***

Size	Document Number	Rev
A3	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 56 of 102

Blanking

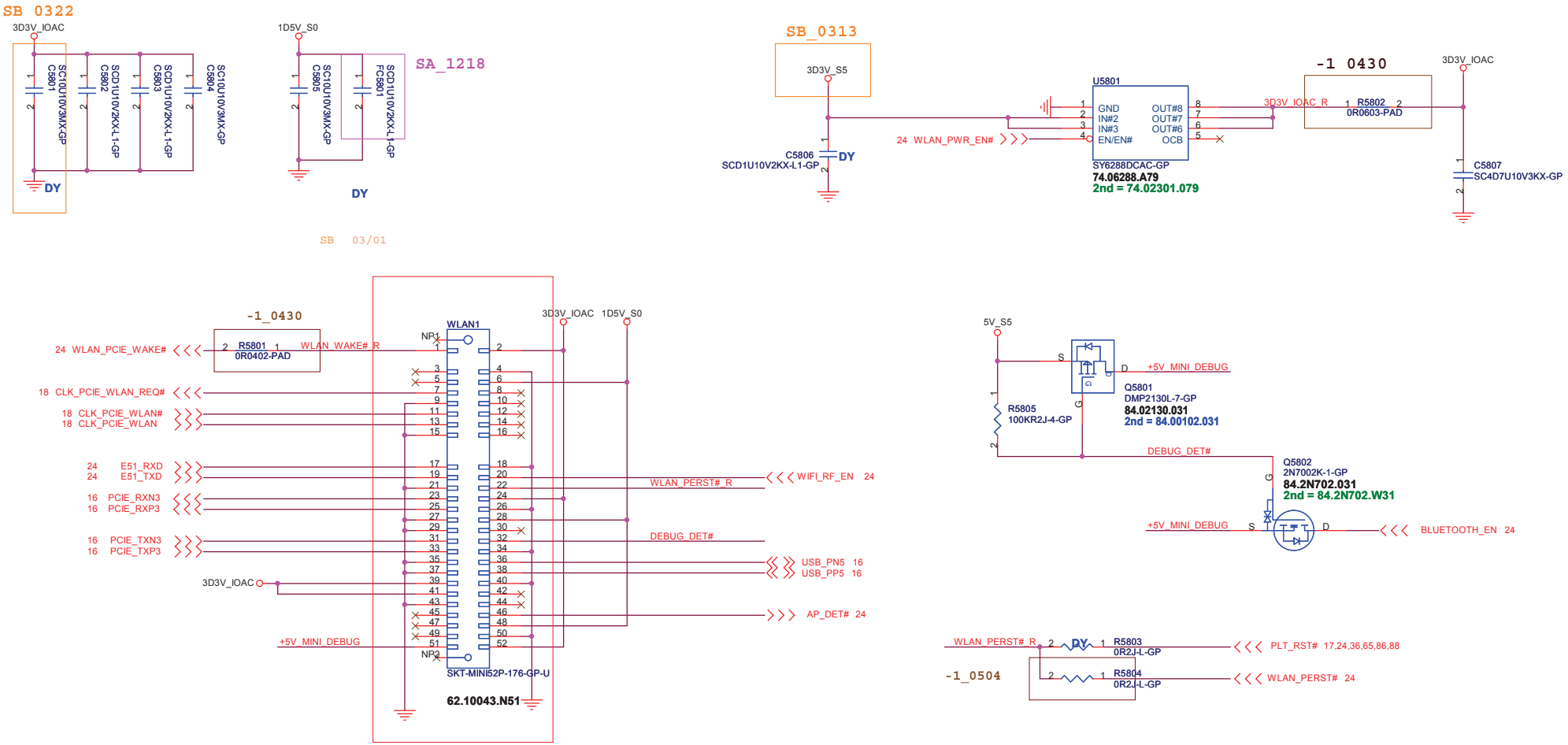
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: E-SATA

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 57 of 102



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN)***

Size	Document Number	Rev
A3	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 58 of 102

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN CONN

Size	Document Number	Rev
A4	**WEEBILL_HW**	**SA**

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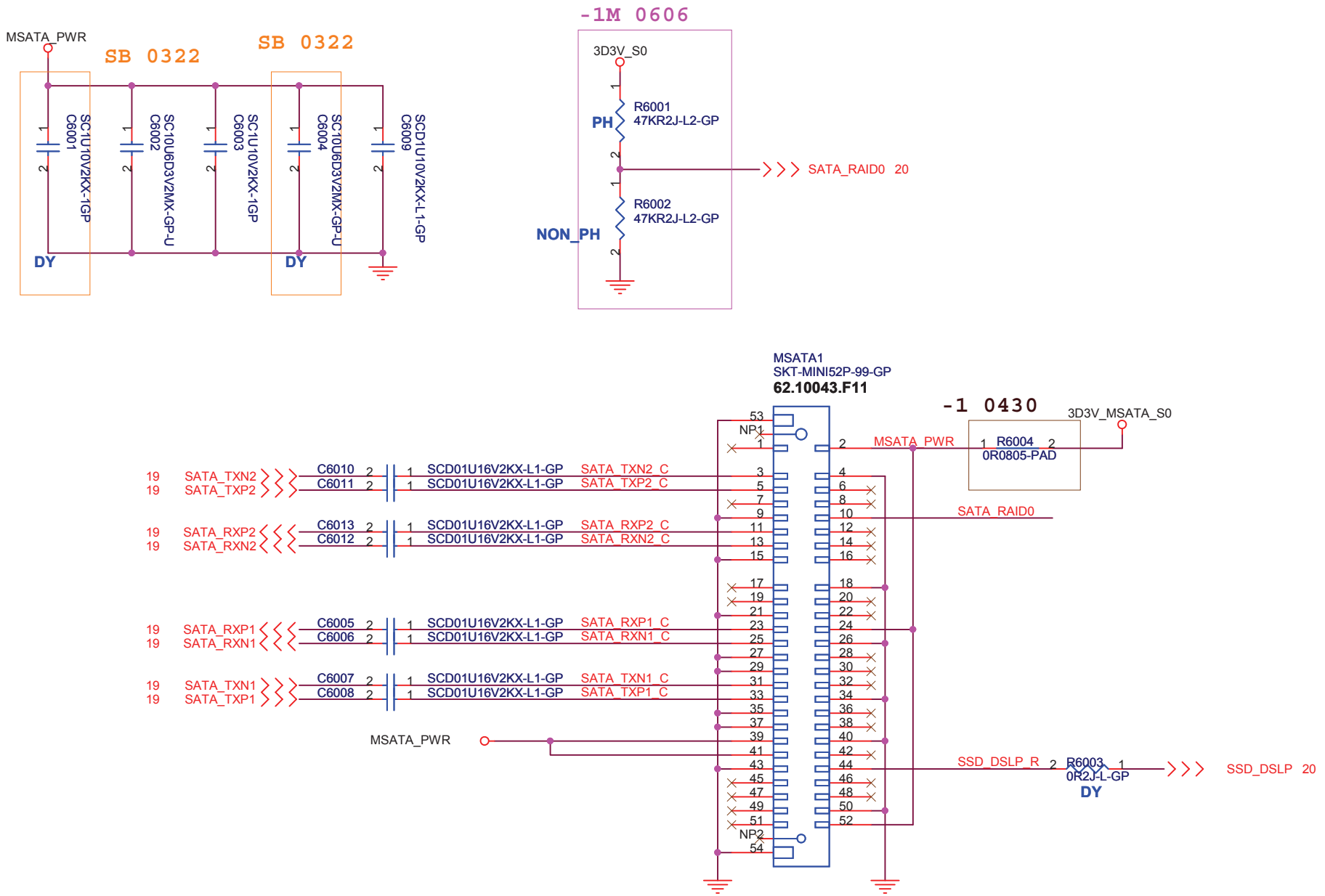

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***mSATA Connector***

Size	Document Number	Rev
A4	WEEBILL_HW	SA

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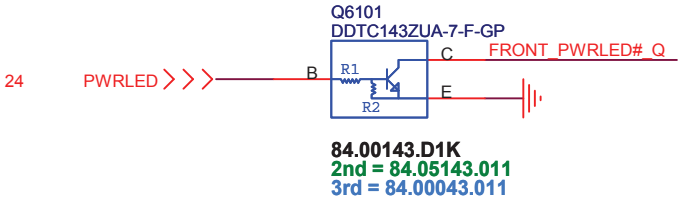
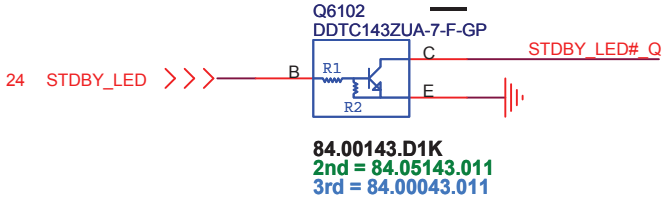
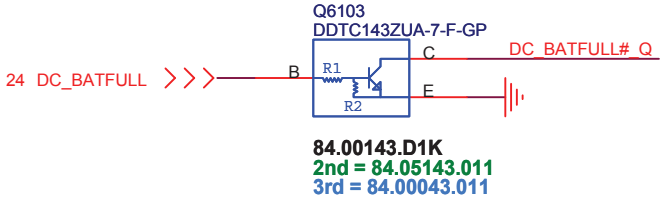
Power LED



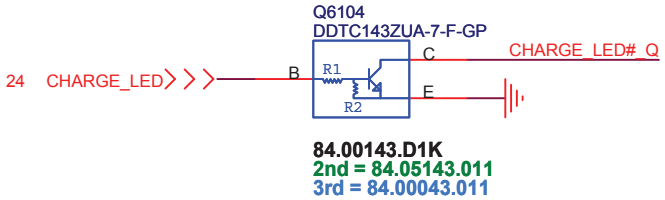
Power STDBY_LED

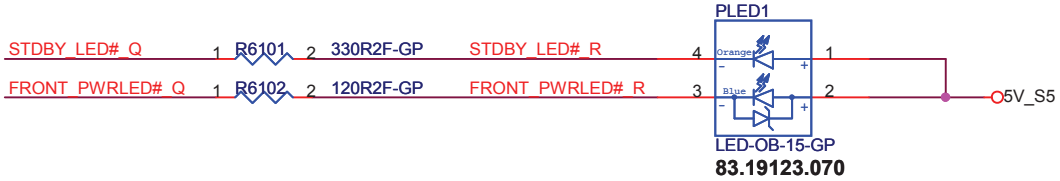


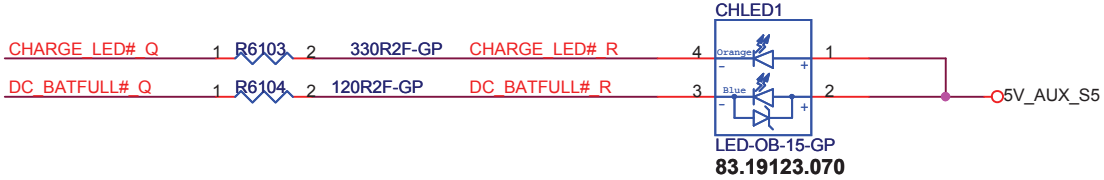
Battery LED (DC_BATFULL)



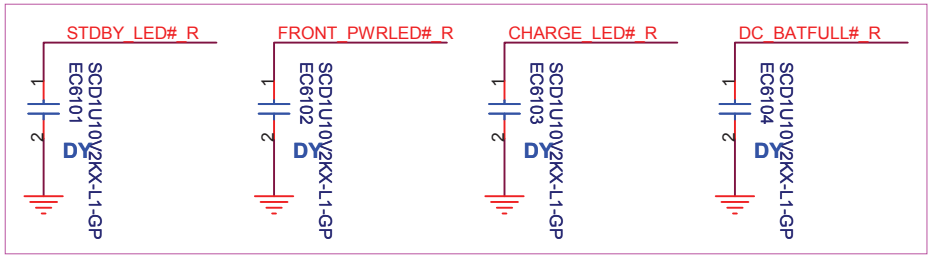
Battery LED (CHARGE)







SA_1224



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
A4	WEEBILL_HW	SA

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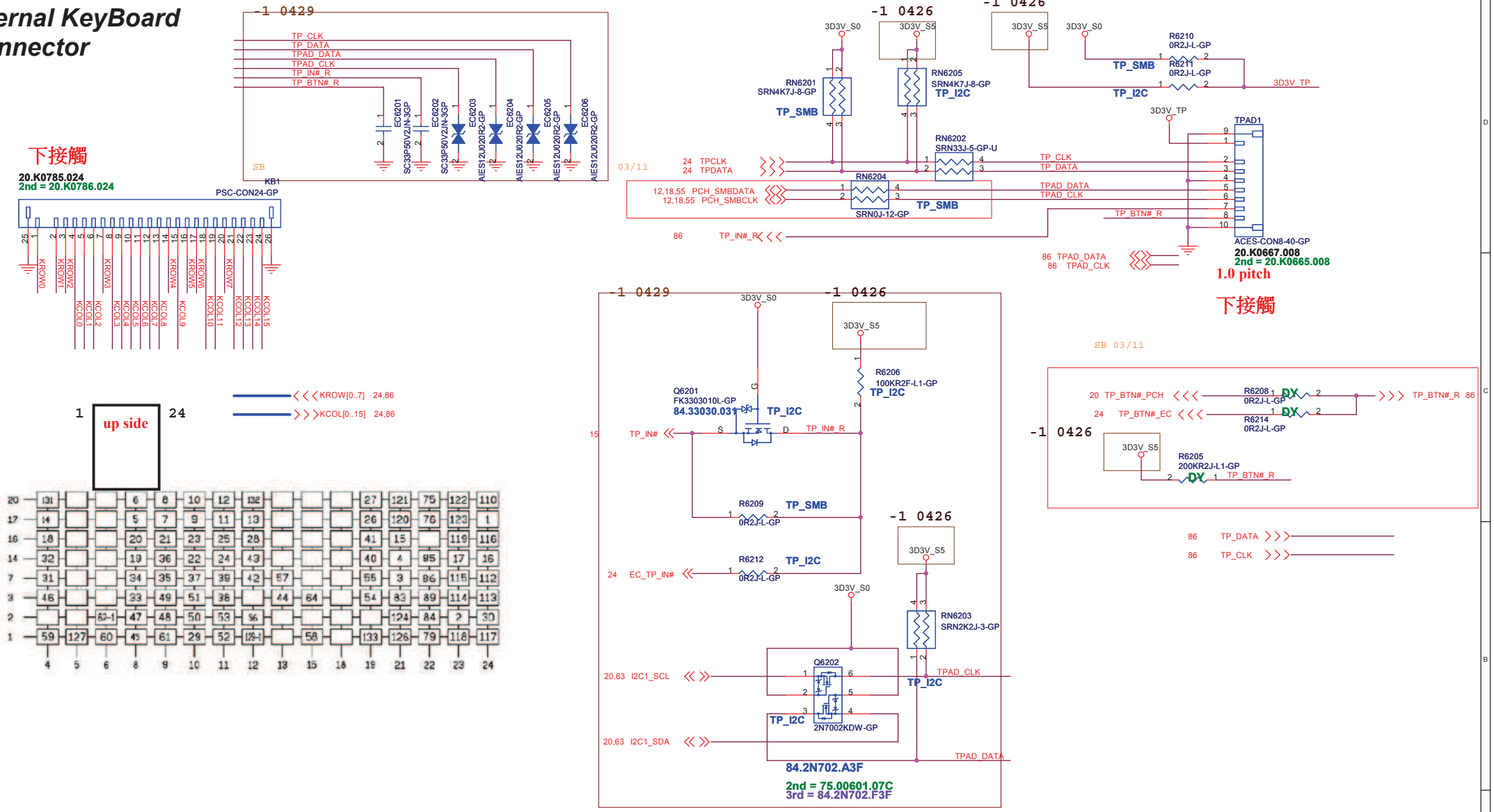
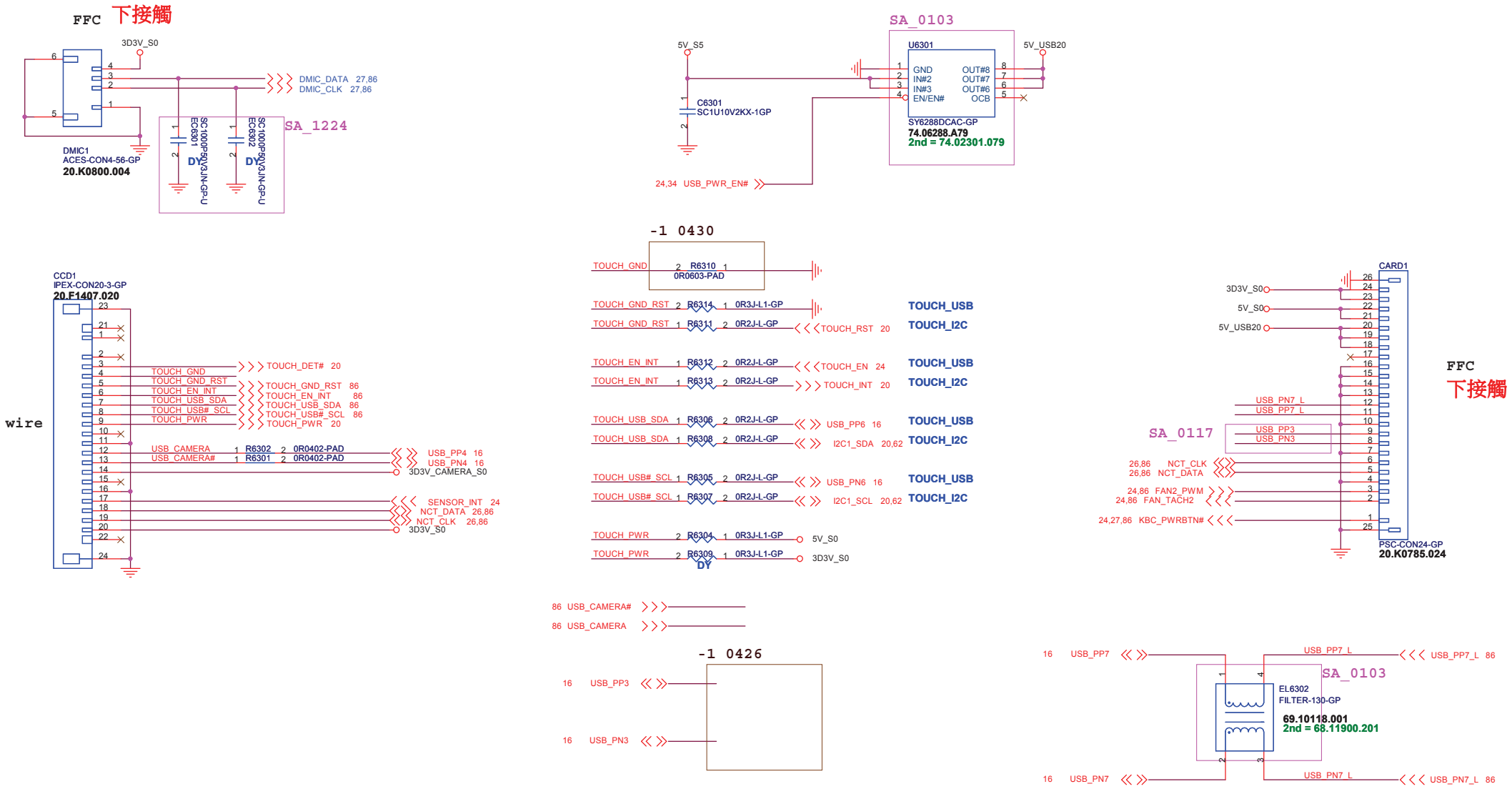
Internal KeyBoard Connector



<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Key Board/Touch Pad
Size A3	Document Number WEEBILL_HW
Rev	SA
Date: Wednesday, September 18, 2013	Sheet 62 of 102



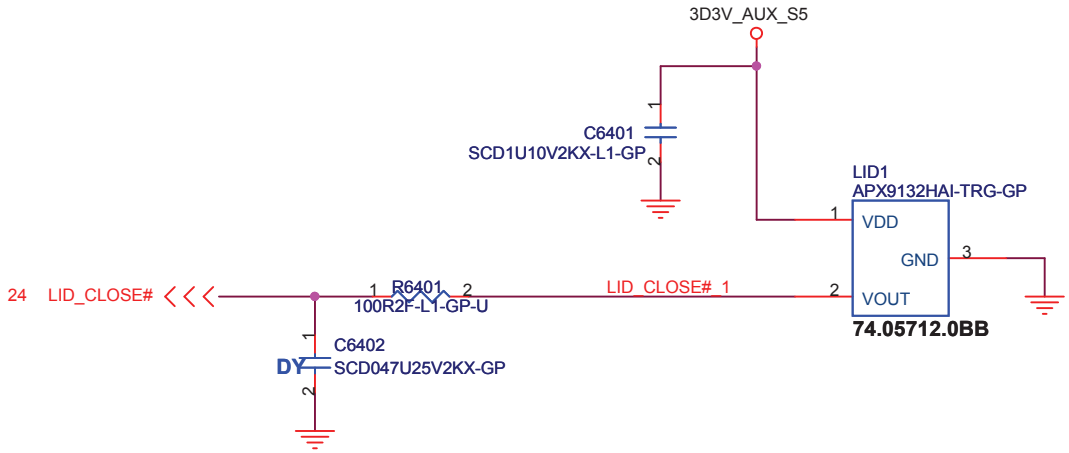
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
A3	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 63 of 102



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 64 of 102

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 65 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
SENSOR HUB

Size	Document Number	Rev
A4	WEEBILL_HW	SA

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Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G Sensor

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 67 of 102

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Thunderbolt (1/5)

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 68 of 102

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (2/5)*

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 69 of 102

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (3/5)*

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 70 of 102

Blanking

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (4/5)*

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 71 of 102

Blanking

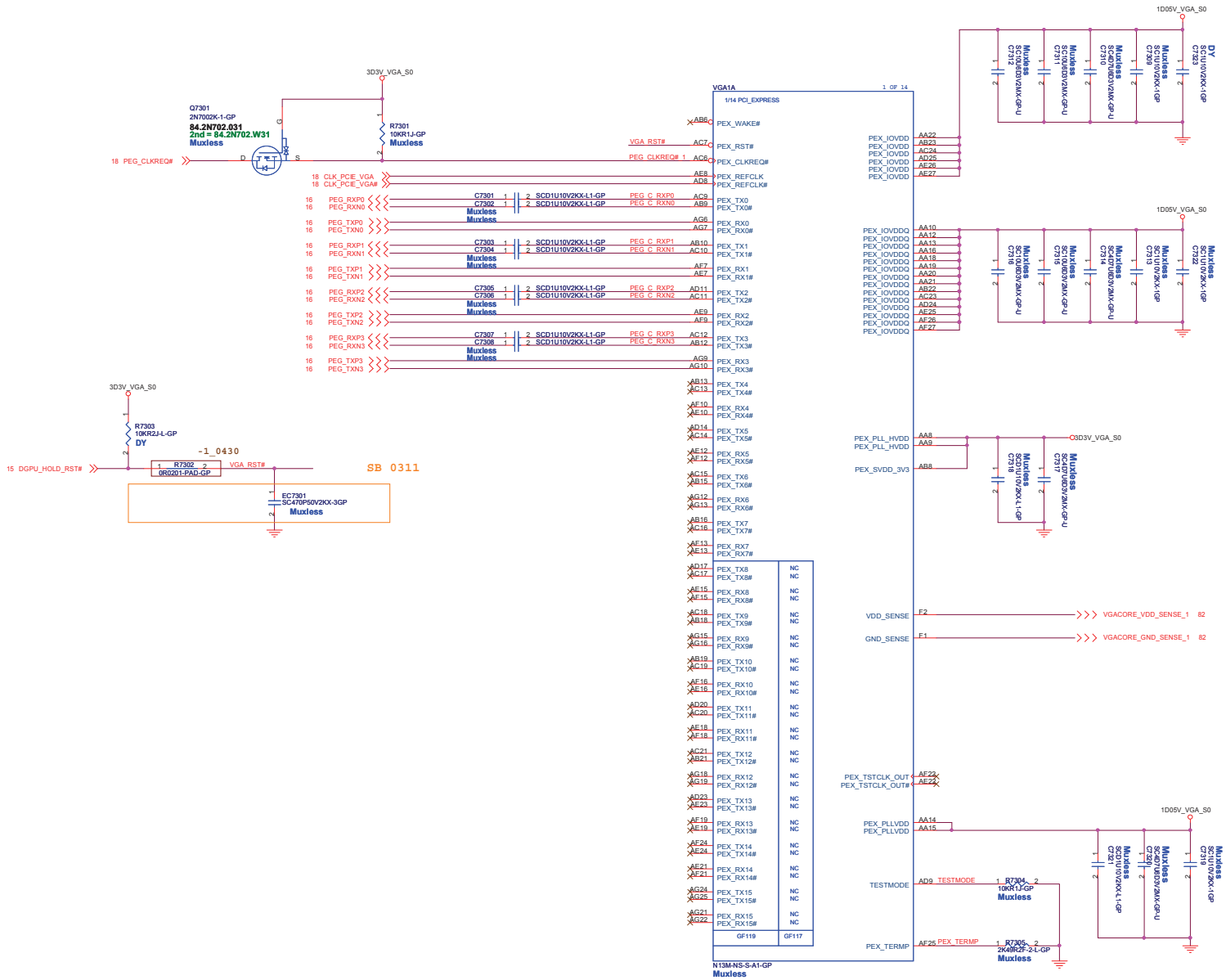
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Thunderbolt (5/5)

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 72 of 102



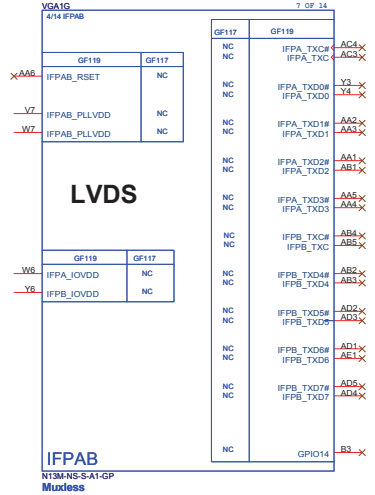
<Variant Name>

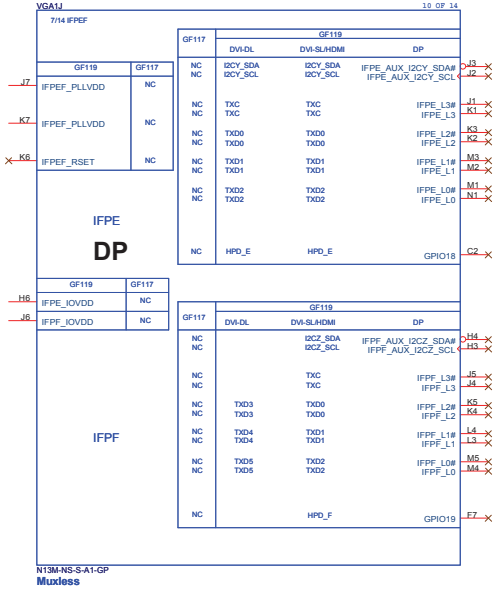
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

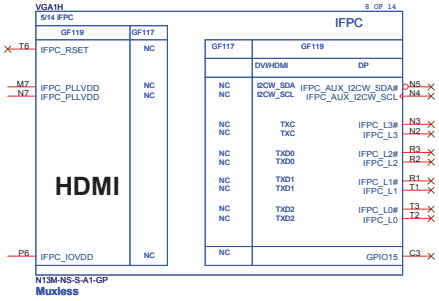
Title: **GPU(PEG)**

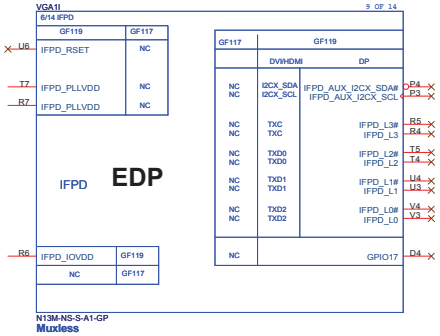
Size	Document Number	Rev
A2	WEEBILL_HW	SA

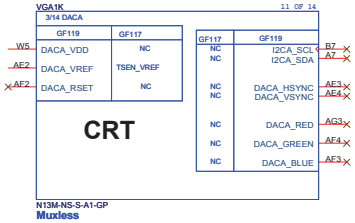
Date: Wednesday, September 18, 2013 Sheet 73 of 102











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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (DIGITALOUT)***

Size	Document Number	Rev
A2	WEEBILL_HW	SA

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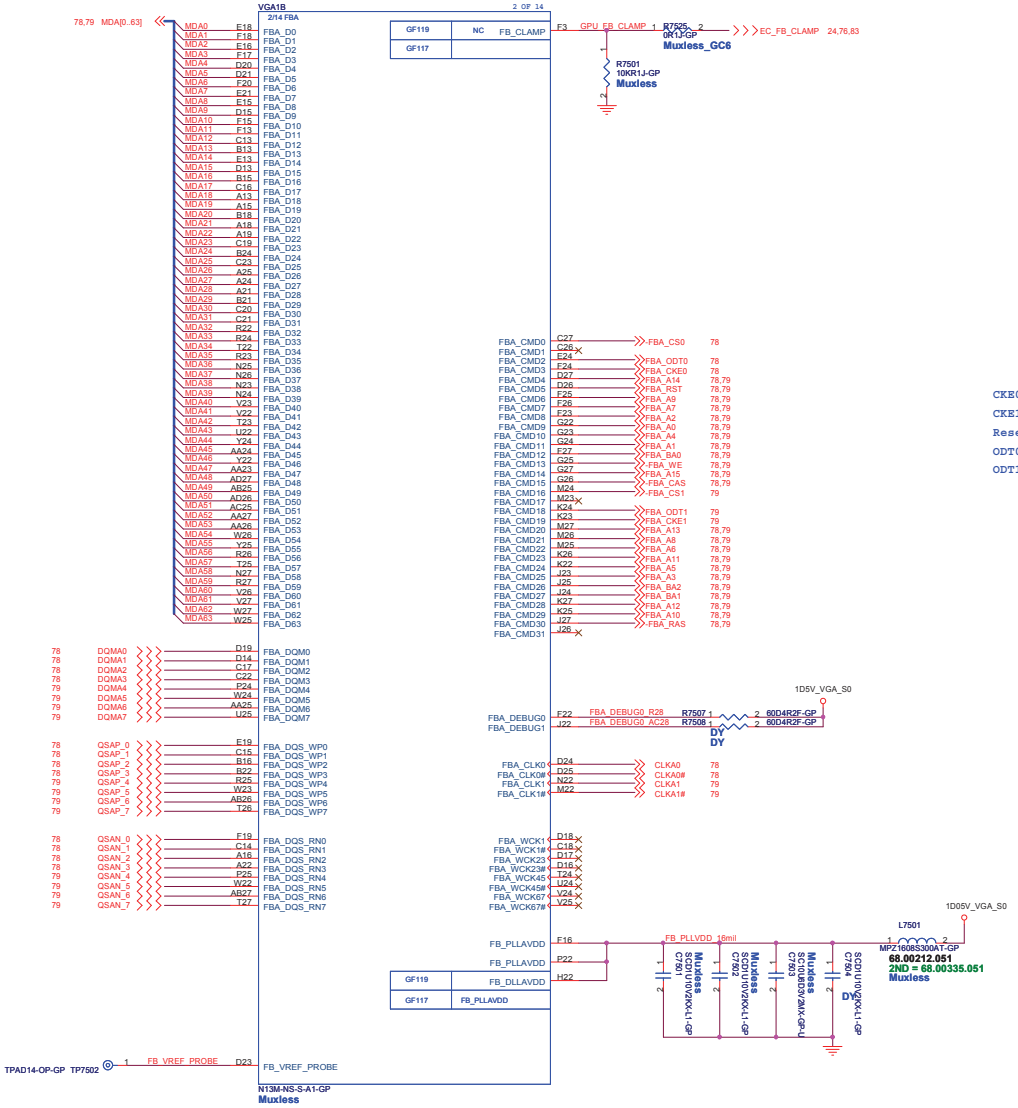

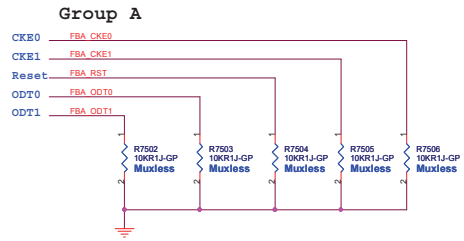

N14x DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (VRAM I/F)

Size: A2 | Document Number: WEEBILL_HW | Rev: SA

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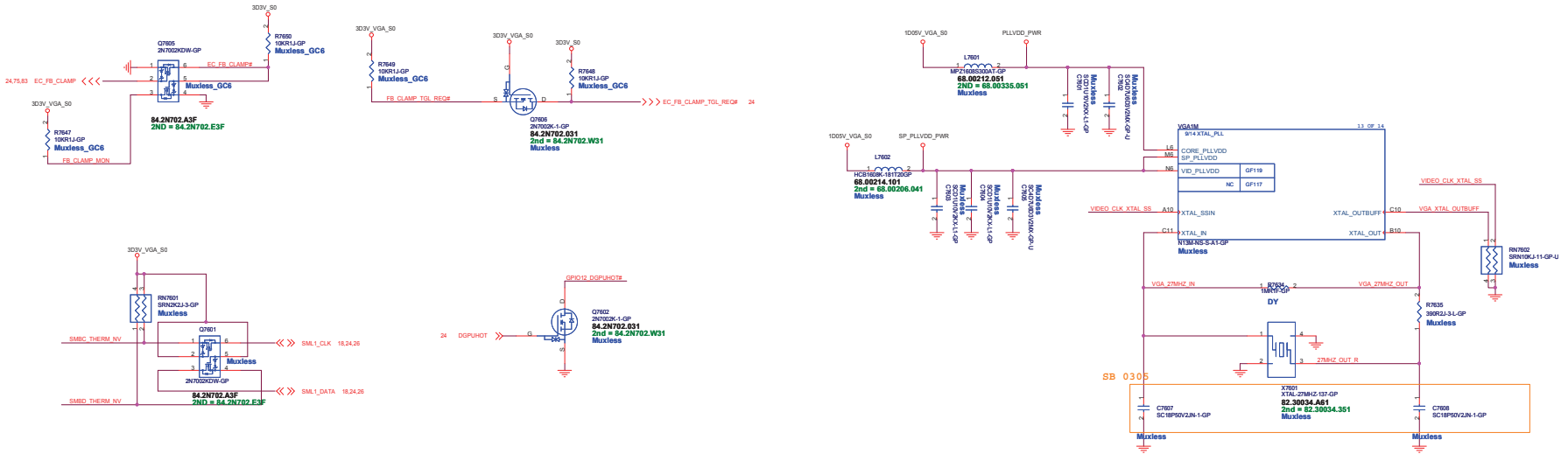

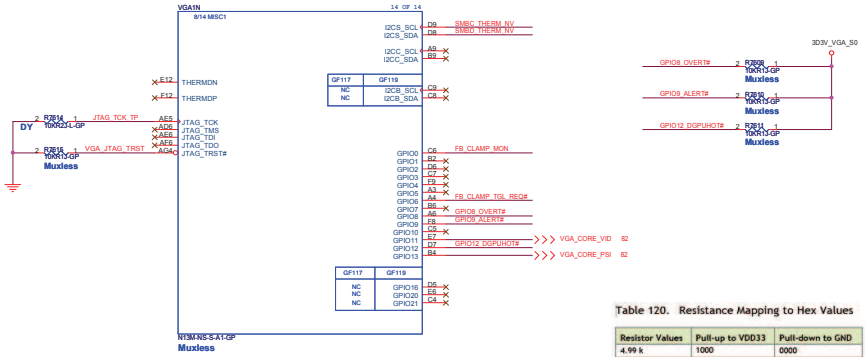

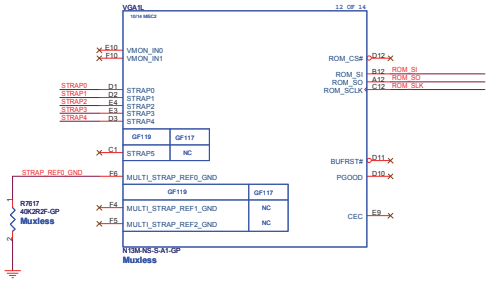

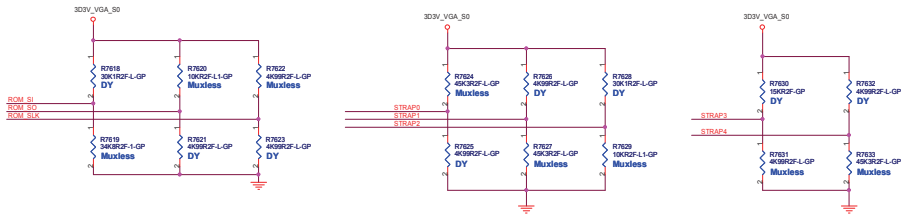

Table 120. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

VRAM Table(N14M-LP)

	Hynix 2G 0110(0x6) H5TQ2G	Hynix 2G 0100(0x4) H5TC2G
ROM_SI	34.8Kohm 64.34825.6DL	24.9Kohm 64.24925.6DL

Table 114. GB2-64 and GB4-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: Strap to boot FBVDD/Q
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	Reserved			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	PSI	O	Phase Shedding	PSI: 10k pull-up to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 73
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 73
GPIO16	FRM_LCK	O	JT Frame Lock signal	
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 73
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 73
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB used as DisplayPort	See Figure 73
GPIO20	Reserved			
GPIO21	Reserved			

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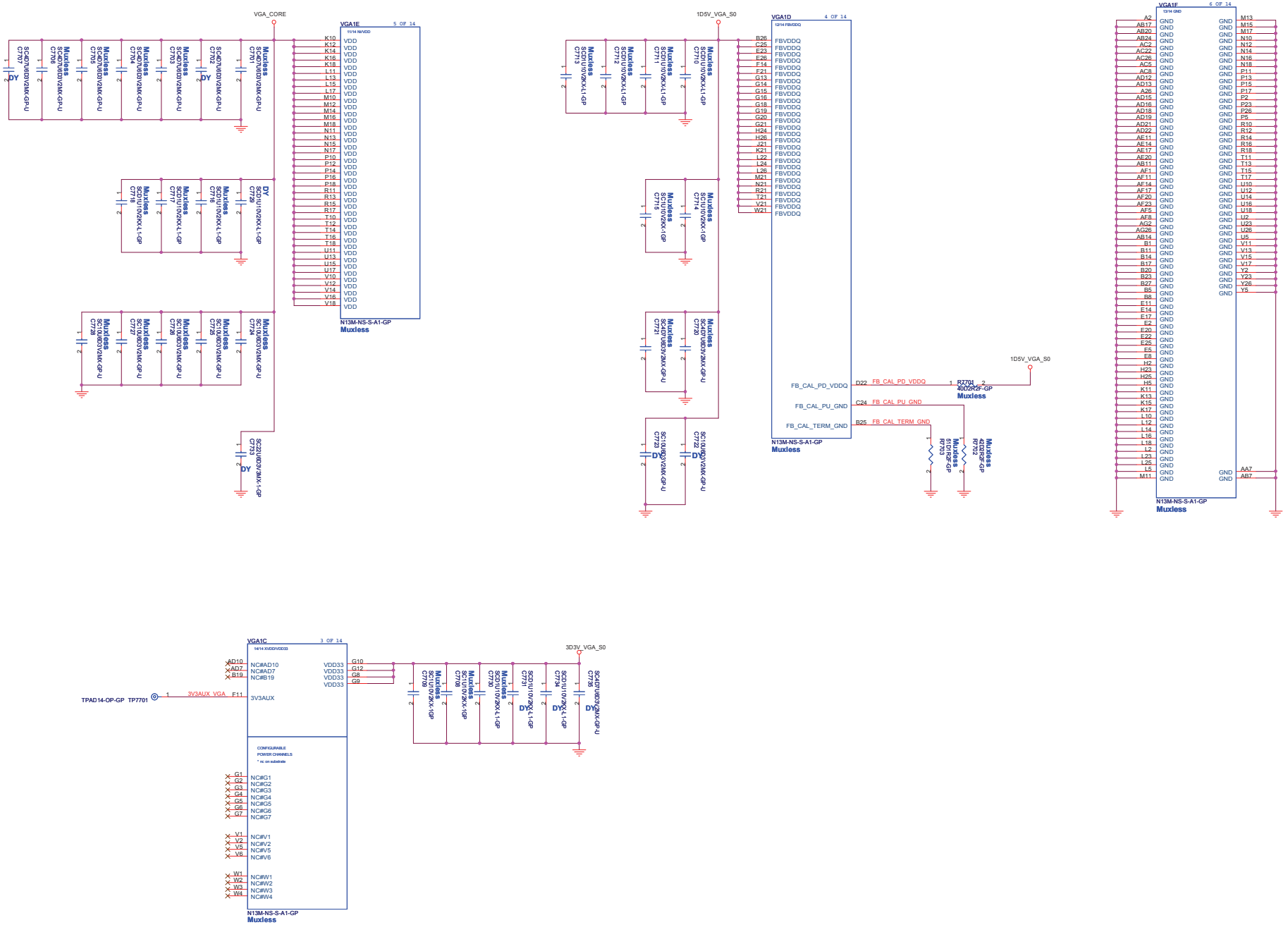

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (POWER/GND)

Size	Document Number	Rev
A2	WEEBILL_HW	SA

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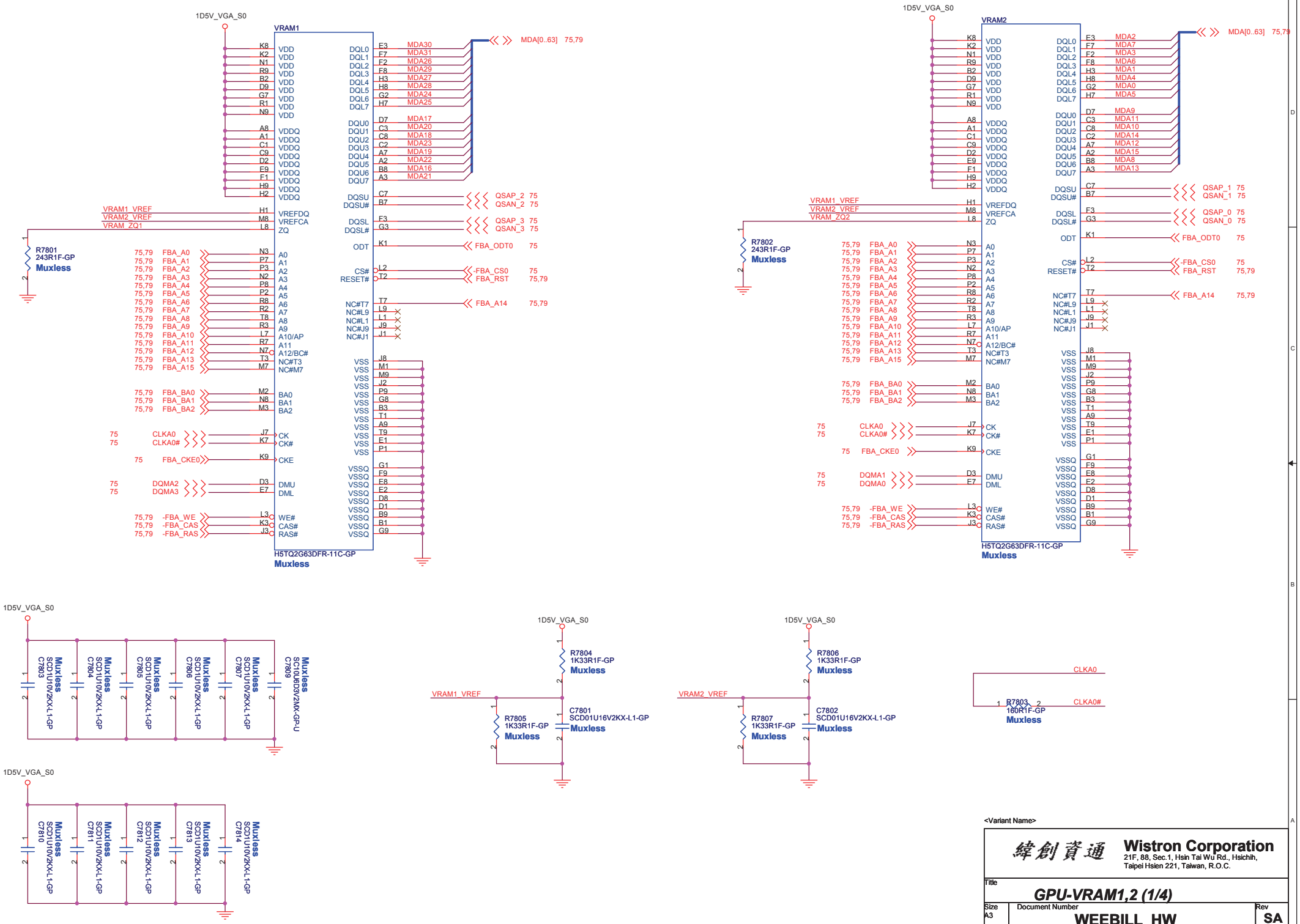

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM1,2 (1/4)**

Size: A3 | Document Number: **WEEBILL_HW** | Rev: **SA**

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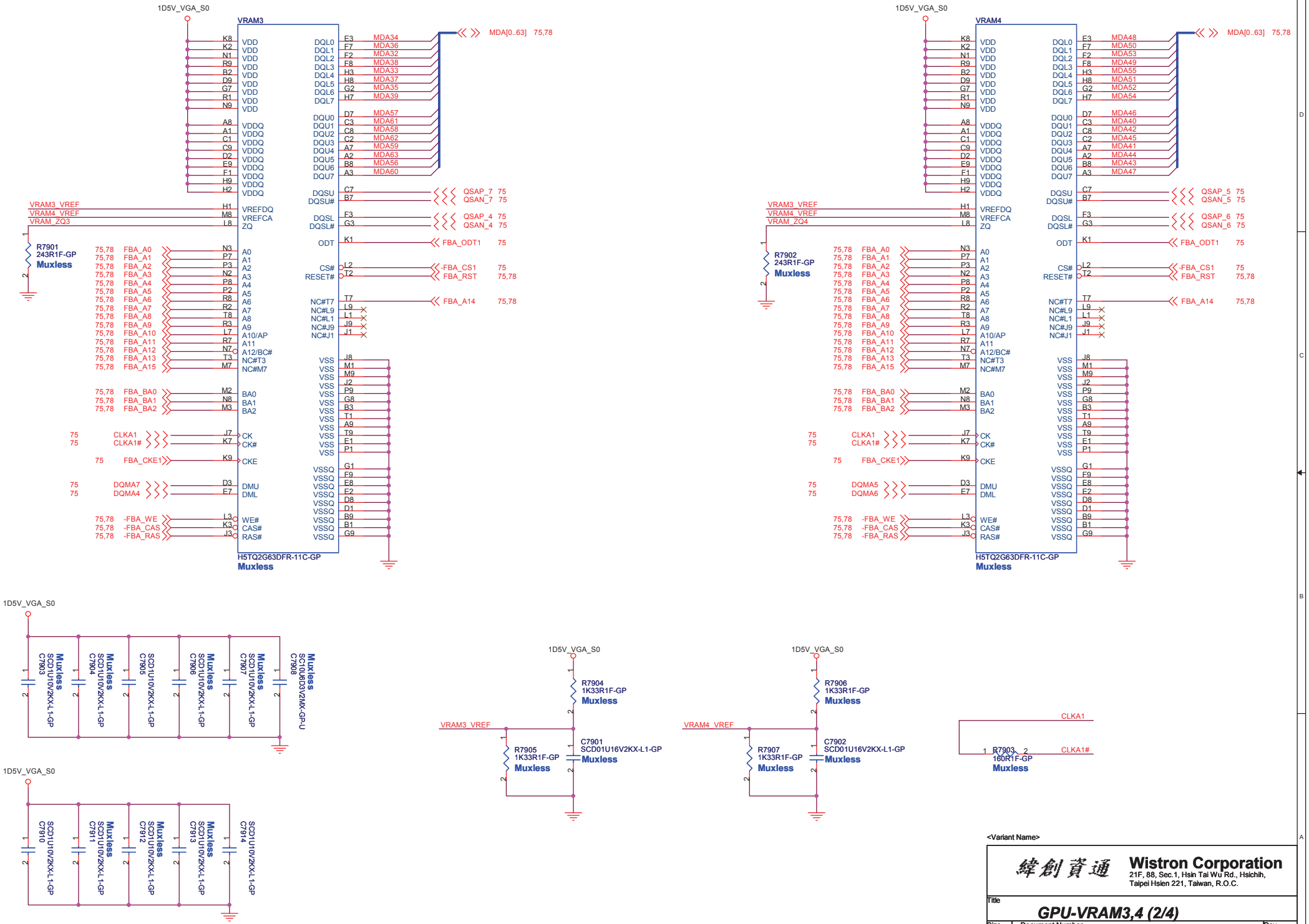

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: A3 | Document Number: WEEBILL_HW | Rev: SA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A4	WEEBILL_HW	SA

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A4	WEEBILL_HW	SA

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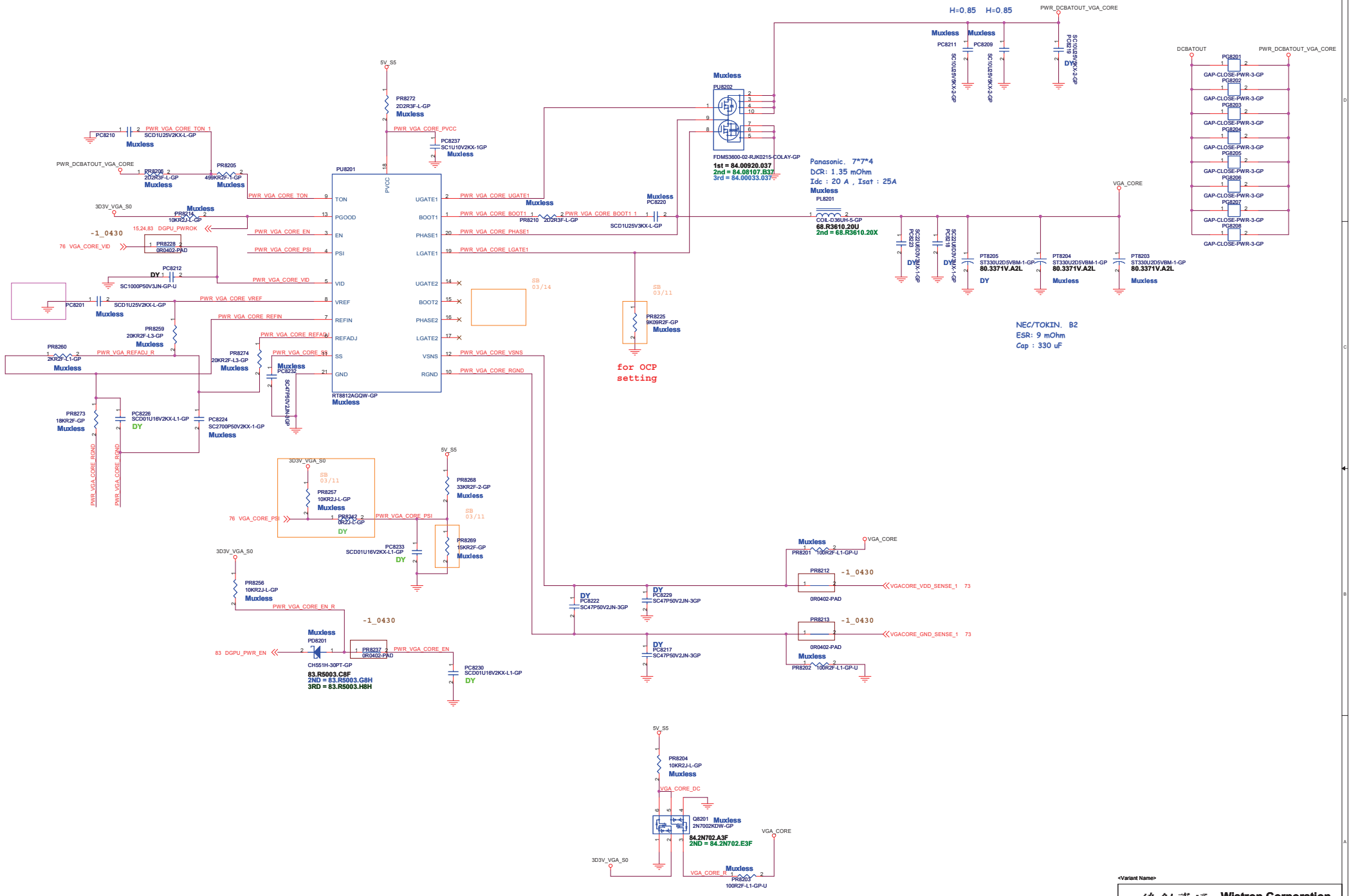

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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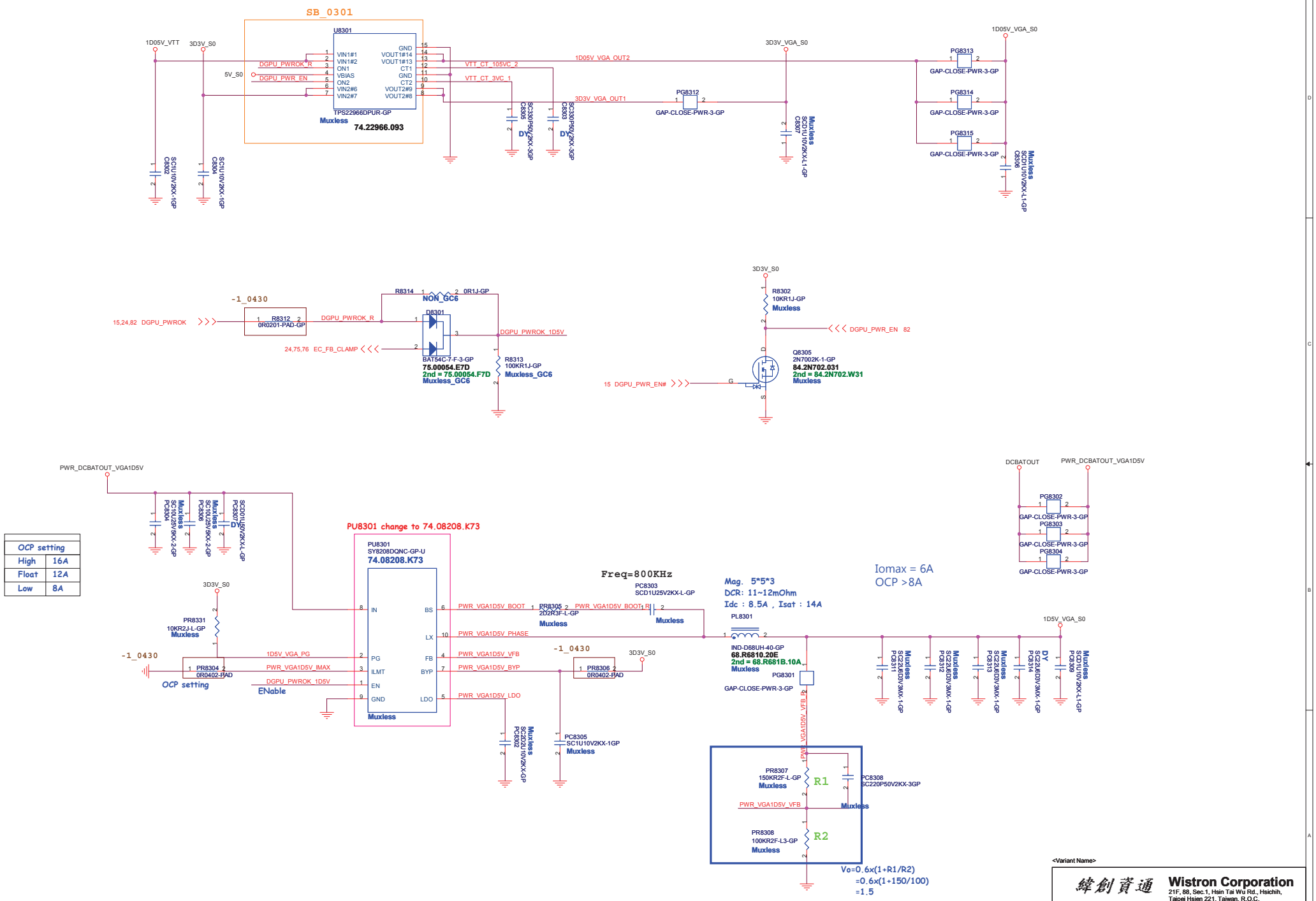
Size: A2 | Document Number: WEEBILL_HW | Rev: SB

Date: Wednesday, September 18, 2013 | Sheet 82 of 102



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DISCRETE VGA POWER**

Size: Custom | Document Number: **WEEBILL_HW** | Rev: **SA**

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Switchable GFX LCD(1/2)

Size	Document Number	Rev
A4	WEEBILL_HW	SA

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Switchable GFX LCD(2/2)

Size	Document Number	Rev
A4	WEEBILL_HW	SA

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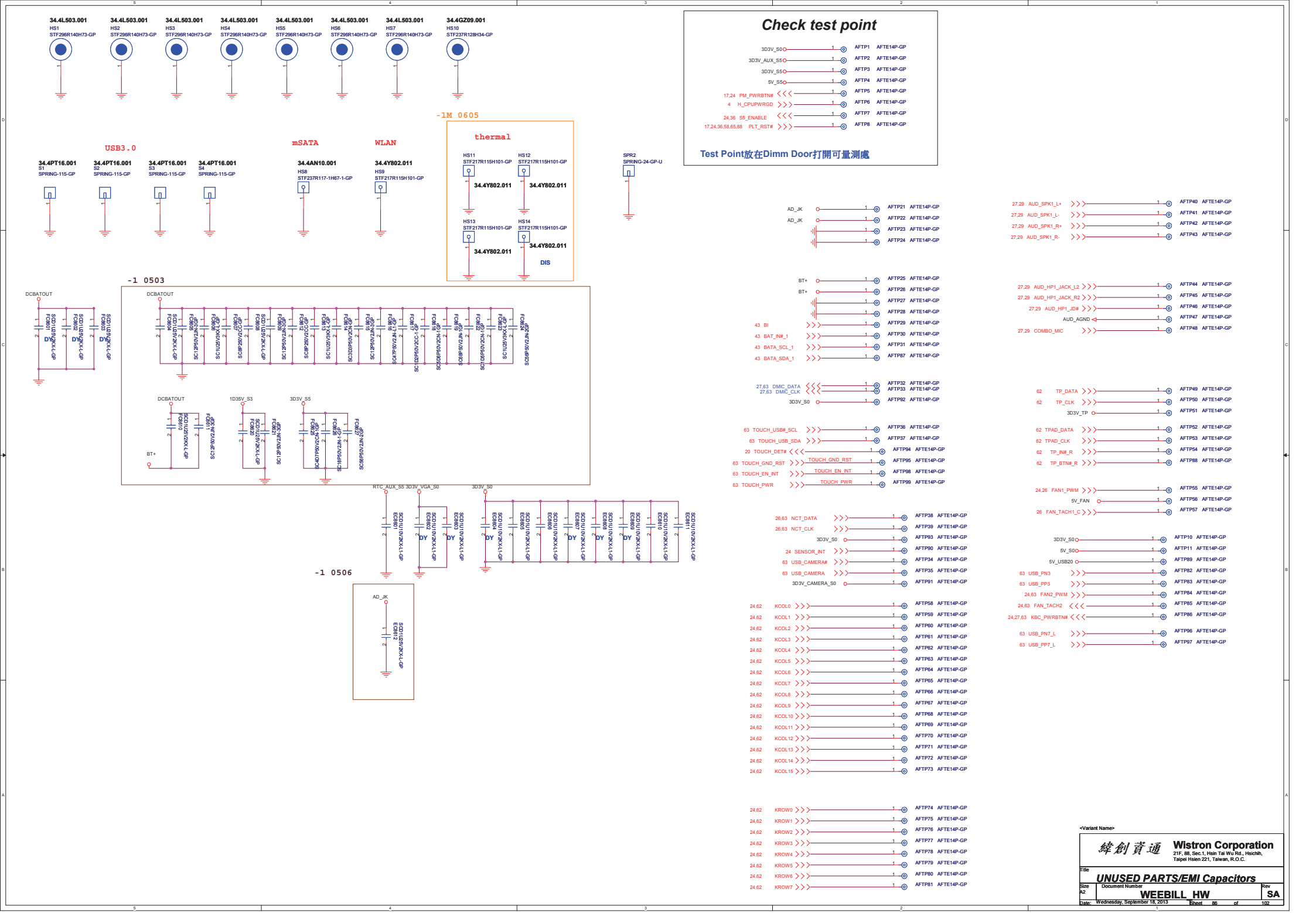
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USB3.0
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mSATA
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WLAN
34.4Y802.011 HS9 STF217R115H101-GP
-1M 0605
thermal
HS11 STF217R115H101-GP 34.4Y802.011
HS12 STF217R115H101-GP 34.4Y802.011
HS13 STF217R115H101-GP 34.4Y802.011
HS14 STF217R115H101-GP 34.4Y802.011
DIS
SPR2 SPRING-24-GP-U
Check test point
3D3V_S0 AFTP1 AFTE14P-GP
3D3V_AUX_S5 AFTP2 AFTE14P-GP
3D3V_S5 AFTP3 AFTE14P-GP
5V_S5 AFTP4 AFTE14P-GP
17,24 PM_PWRBTN# AFTP5 AFTE14P-GP
4 H_CPUPWRGD AFTP6 AFTE14P-GP
24,36 S5_ENABLE AFTP7 AFTE14P-GP
17,24,36,58,65,88 PLT_RST# AFTP8 AFTE14P-GP
Test Point放在Dimm Door打開可量測處
-1 0503
DCBATOUT
BT+
1D35V_S3
3D3V_S5
-1 0506
RTC_AUX_S5
3D3V_VGA_S0
3D3V_S0
AD_JK
AD_JK AFTP21 AFTE14P-GP
AD_JK AFTP22 AFTE14P-GP
AFTP23 AFTE14P-GP
AFTP24 AFTE14P-GP
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24,27,63 KBC_PWRBTN# AFTP86 AFTE14P-GP
63 USB_PN7_L AFTP96 AFTE14P-GP
63 USB_PP7_L AFTP97 AFTE14P-GP
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Size A2 Document Number WEEBILL_HW Rev SA
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NFC

Size: A4 | Document Number: WEEBILL_HW | Rev: SA

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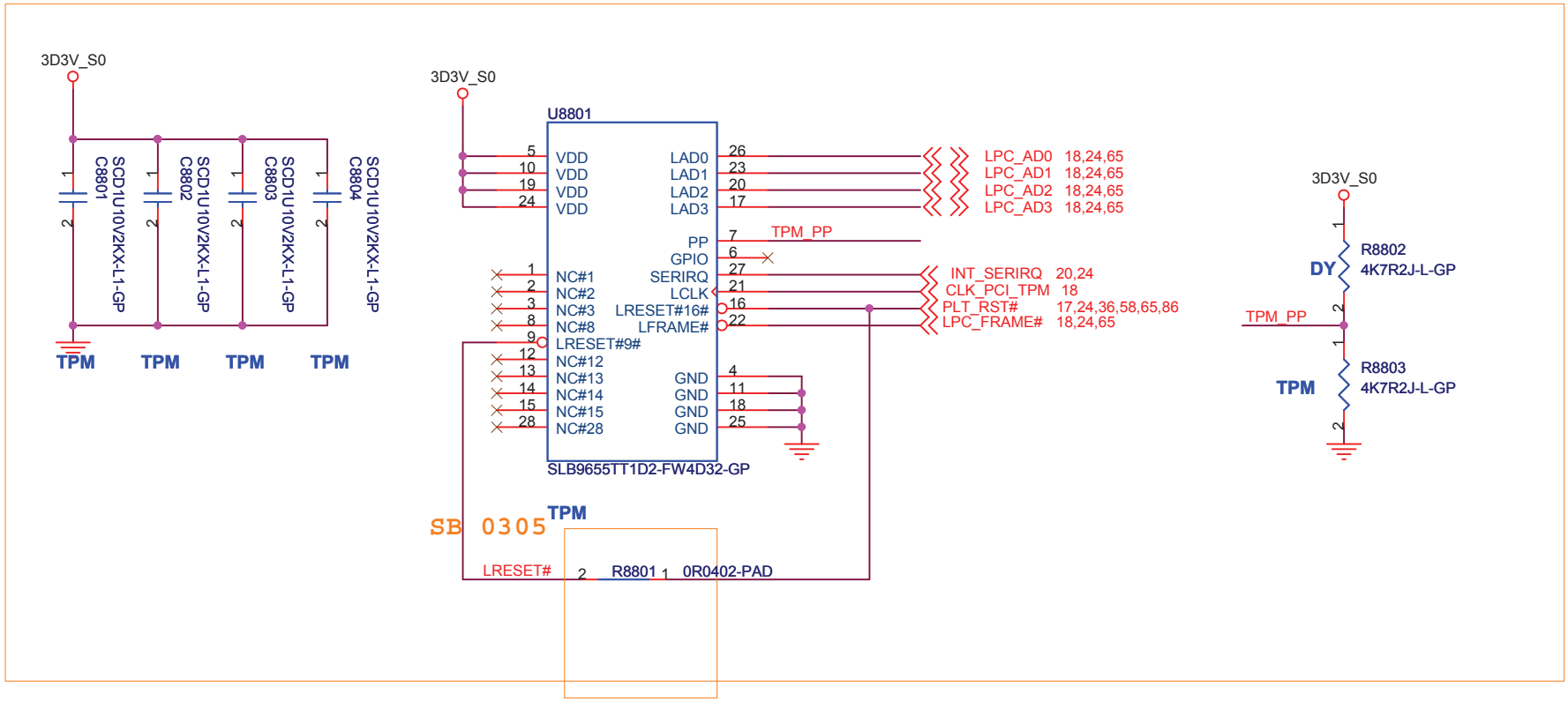

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Size A4	Document Number **WEEBILL_HW**	Rev **SA**
Date: Wednesday, September 18, 2013	Sheet 88 of 102	

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Finger Print*

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 89 of 102

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Express Card*

Size	Document Number	Rev
A4	WEEBILL_HW	SA

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Smart Card socket

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 91 of 102

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<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Switchable GFX eDP*

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 92 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Bottom Docking

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 93 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Inter LAN WG1217LM*

Size	Document Number	Rev
A4	WEEBILL_HW	SA

Date: Wednesday, September 18, 2013 Sheet 94 of 102

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN Switch*

Size	Document Number	Rev
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0[1]	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST#[1]	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4[1]	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST#[1]	0	System	18	HOOK7	DBR#[1]	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

<Variant Name>

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Title: PCH_XDP

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Blanking

Blanking

<Variant Name>

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Title: *Change History*

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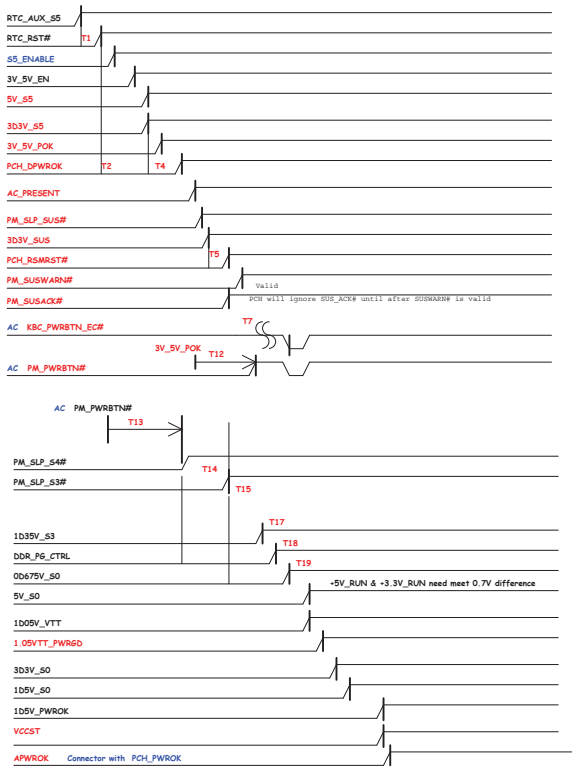
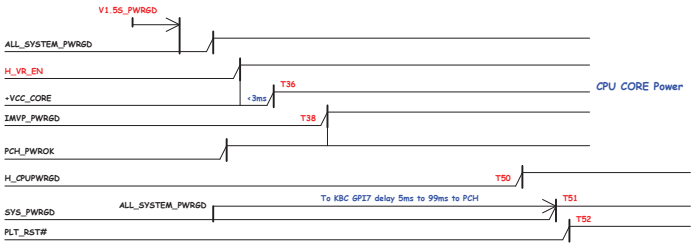
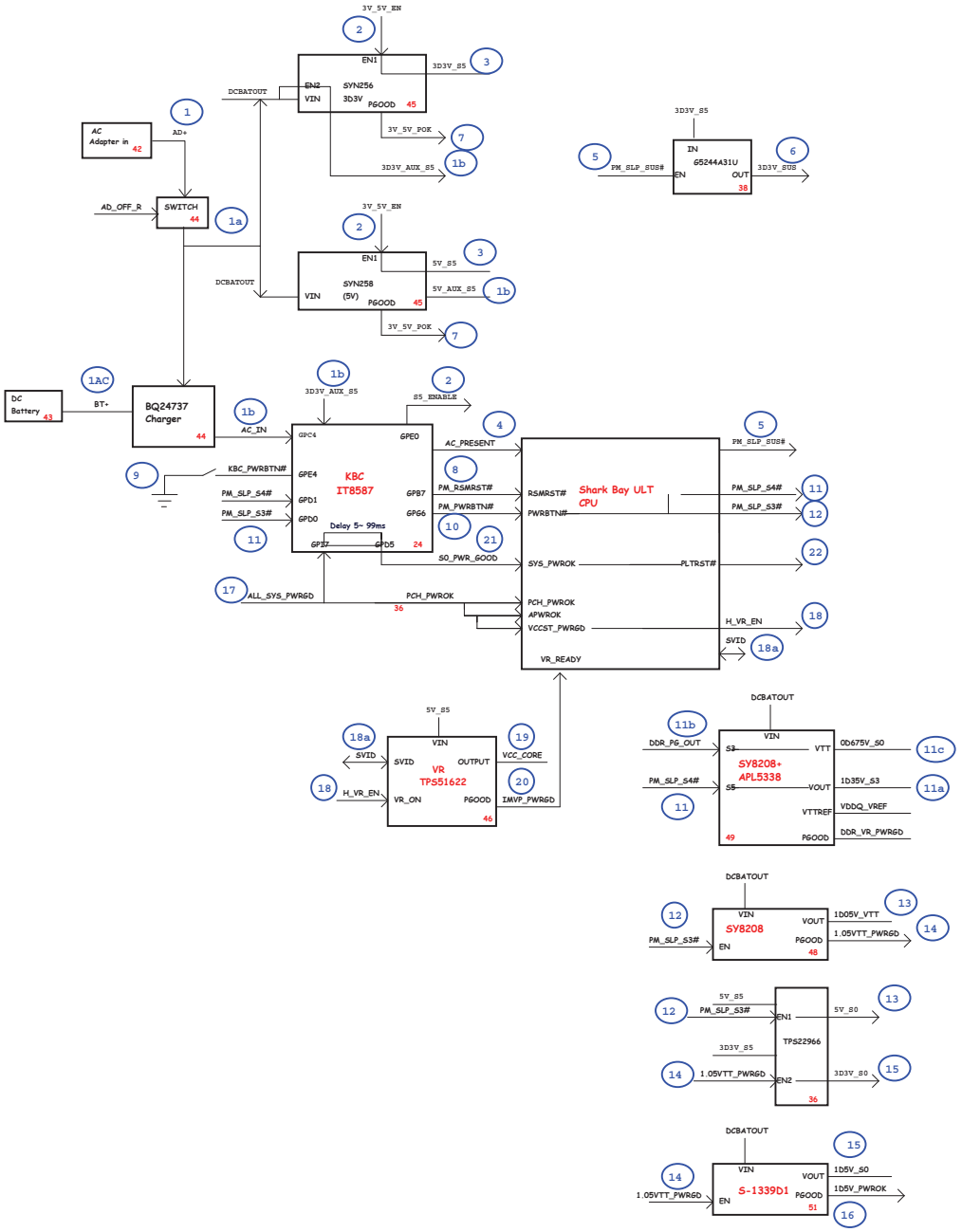
Intel-Power Up Sequence

(AC mode)





SHARK BAY POWER UP SEQUENCE DIAGRAM



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Title: Power Sequence

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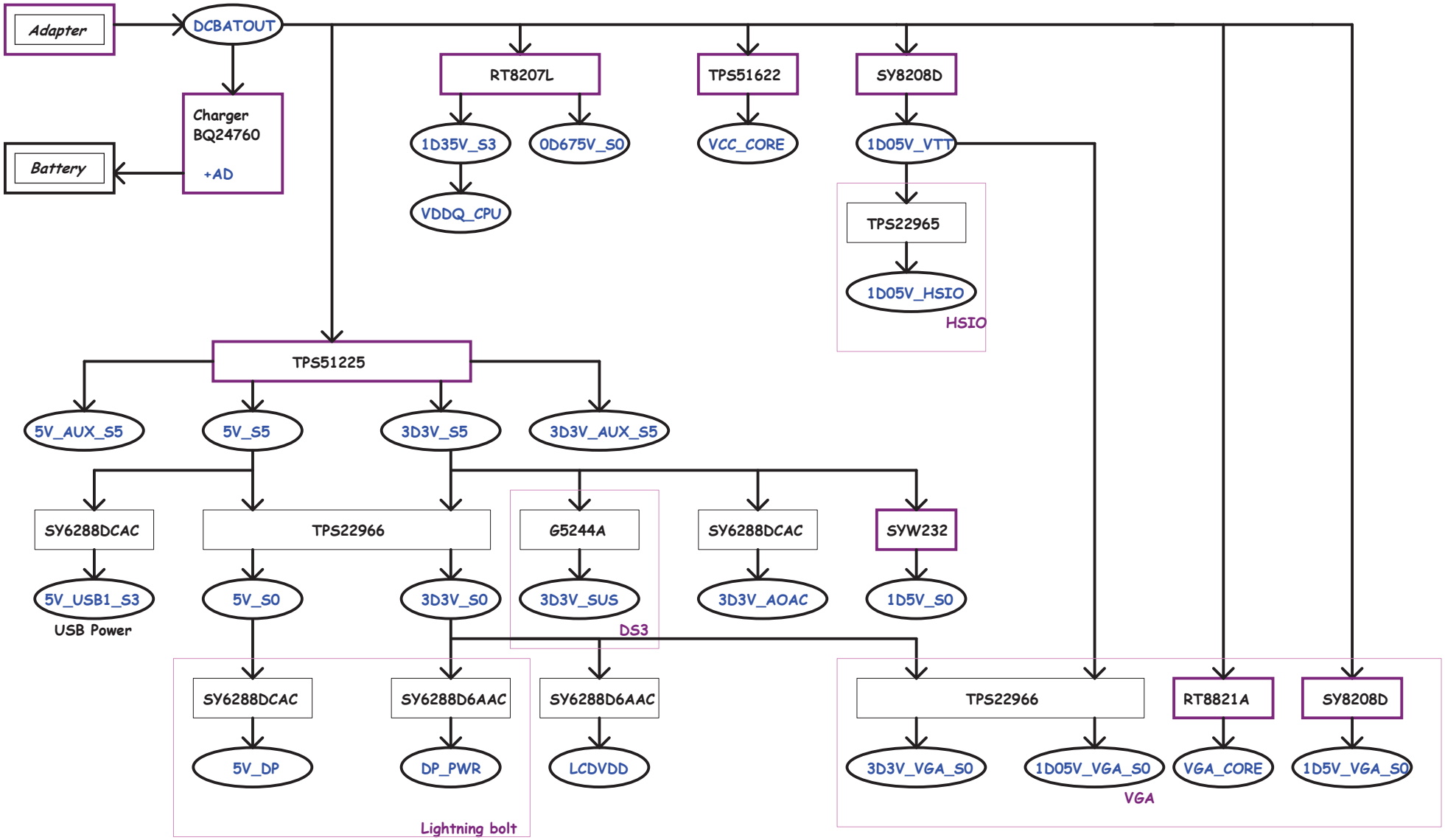

Power Shape

Regulator	LDO	Switch

<Variant Name>

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Title: **Power Block Diagram**

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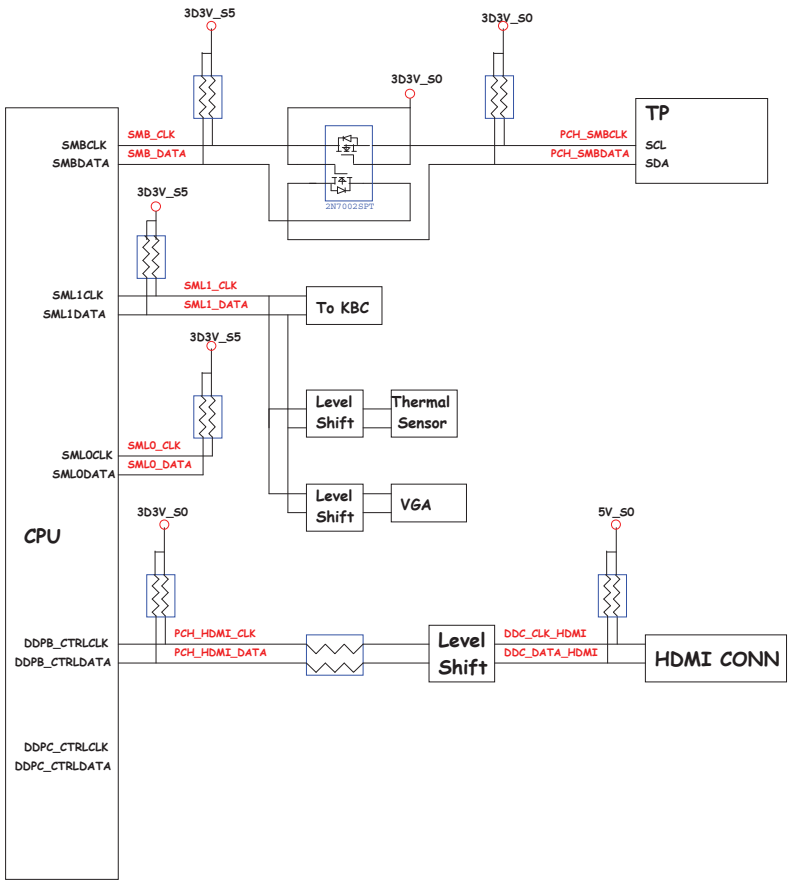
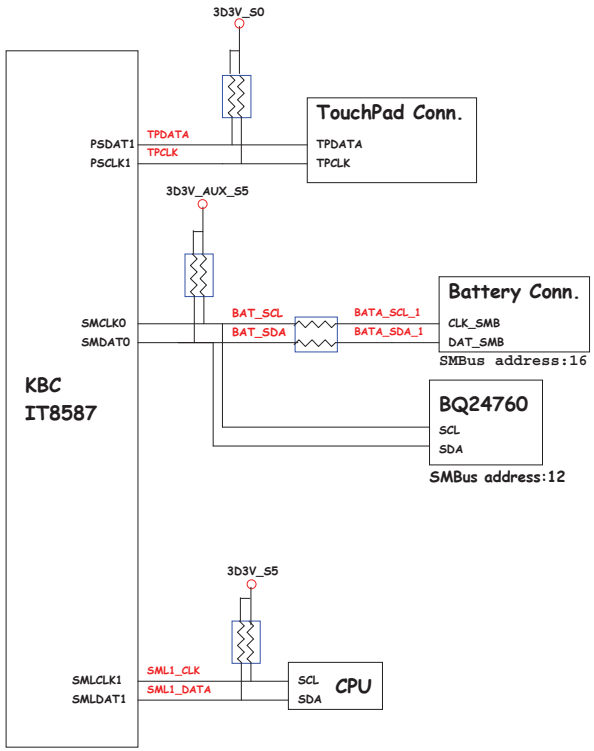
PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Variant Name>

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Title: SMBUS BLOCK DIAGRAM

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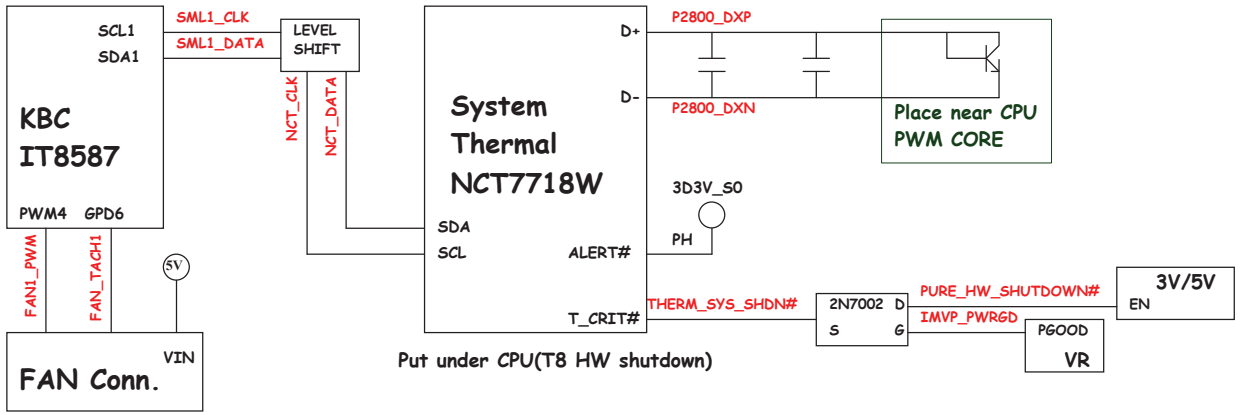
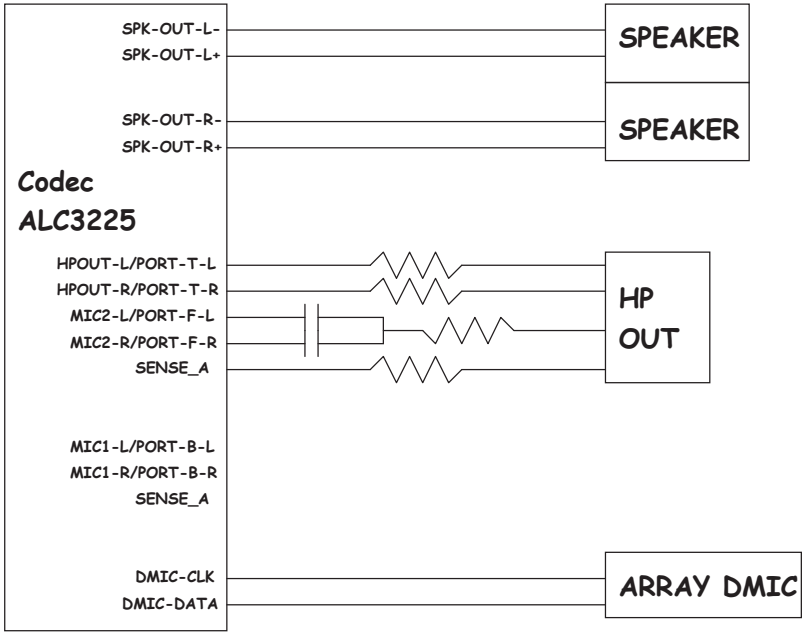
Thermal Block Diagram



Audio Block Diagram



<Variant Name>

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Title: THERMAL/AUDIO BLOCK DIAGRAM

Size	Document Number	Rev
Custom	WEEBILL HW	SA

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