

Yukon Block Diagram

Project code: 91.4BC01.001
PCB P/N : 48.4BC01.001
REVISION : 08226- -1

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
BLOCK DIAGRAM

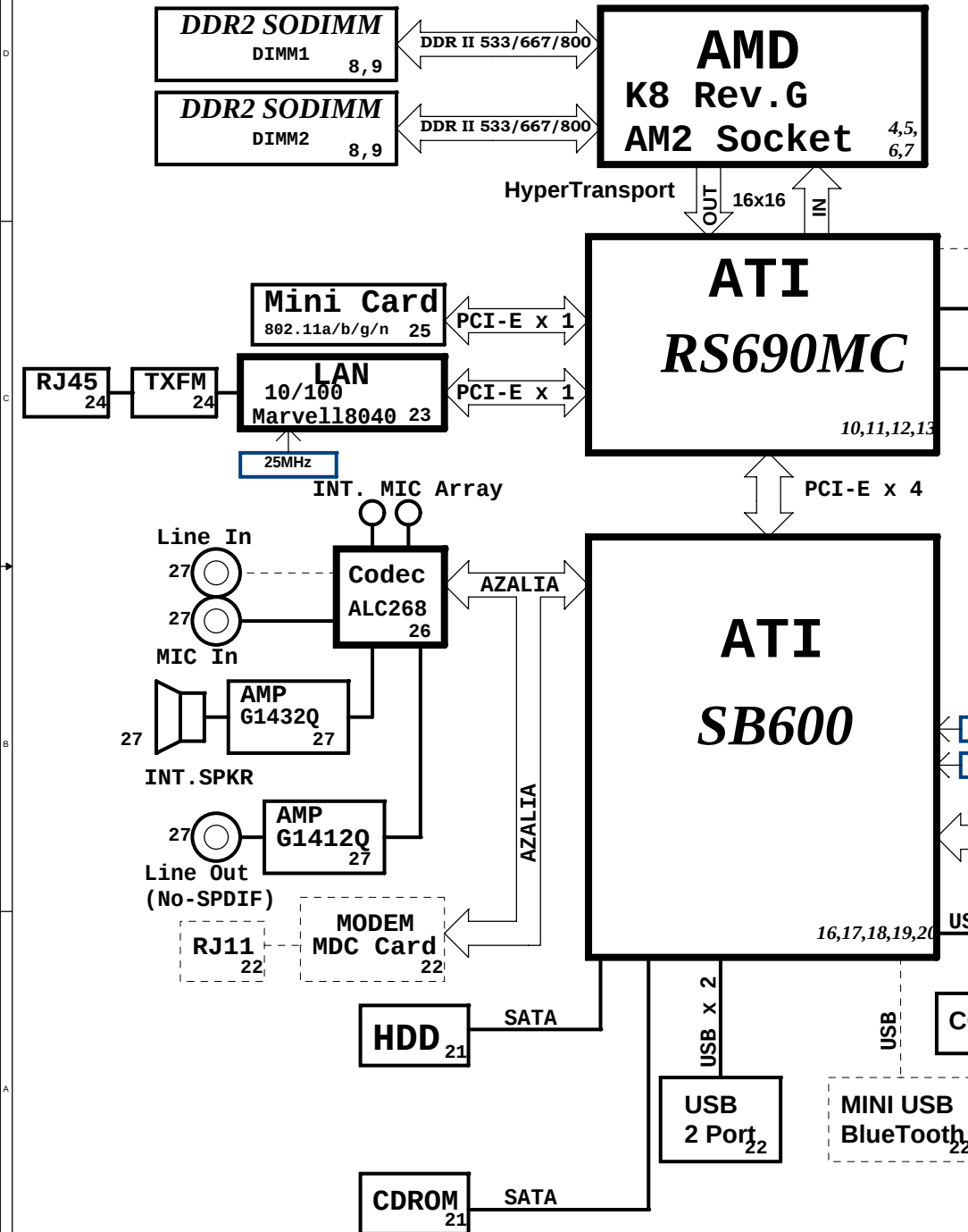
Size A3 Document Number

Yukon

Date: Tuesday, August 12, 2008

Sheet 1 of 43

Rev
-1

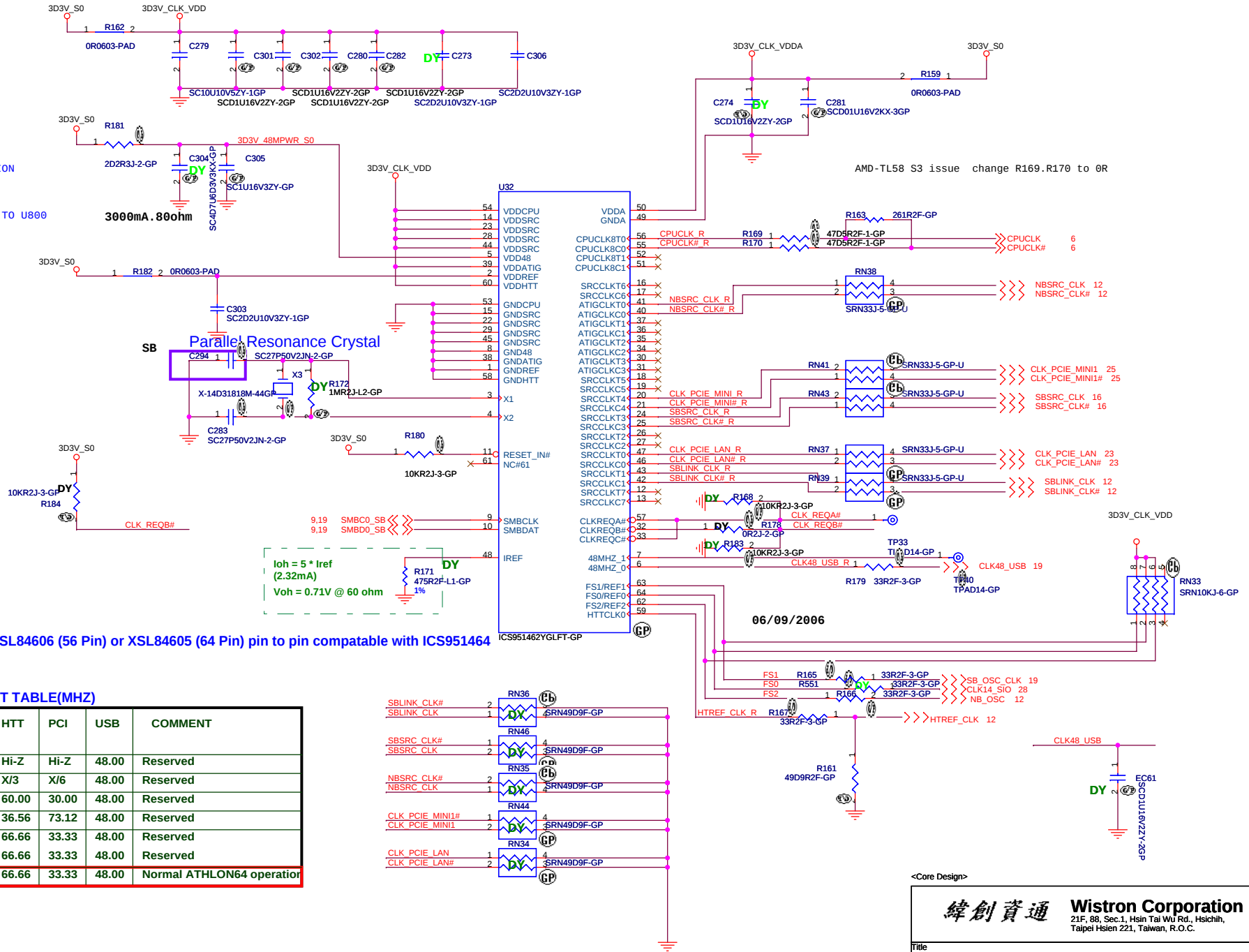


	5	4	3	2	1
D					
C					
B					
A					

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CHANGE HISTORY			
Size	Document Number		Rev
A3	Yukon		-1
Date:	Wednesday, August 06, 2008		Sheet 2 of 43

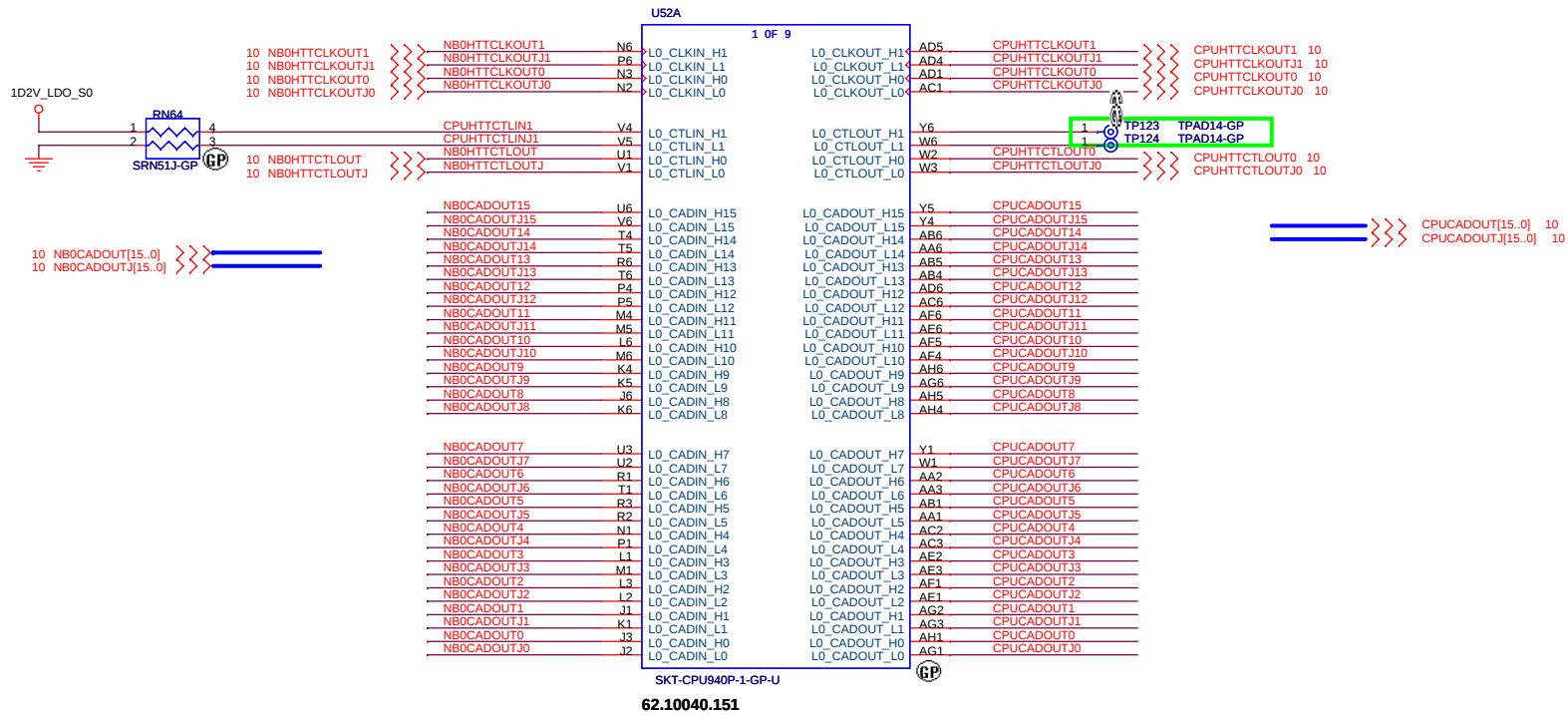
- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



<Core Design>

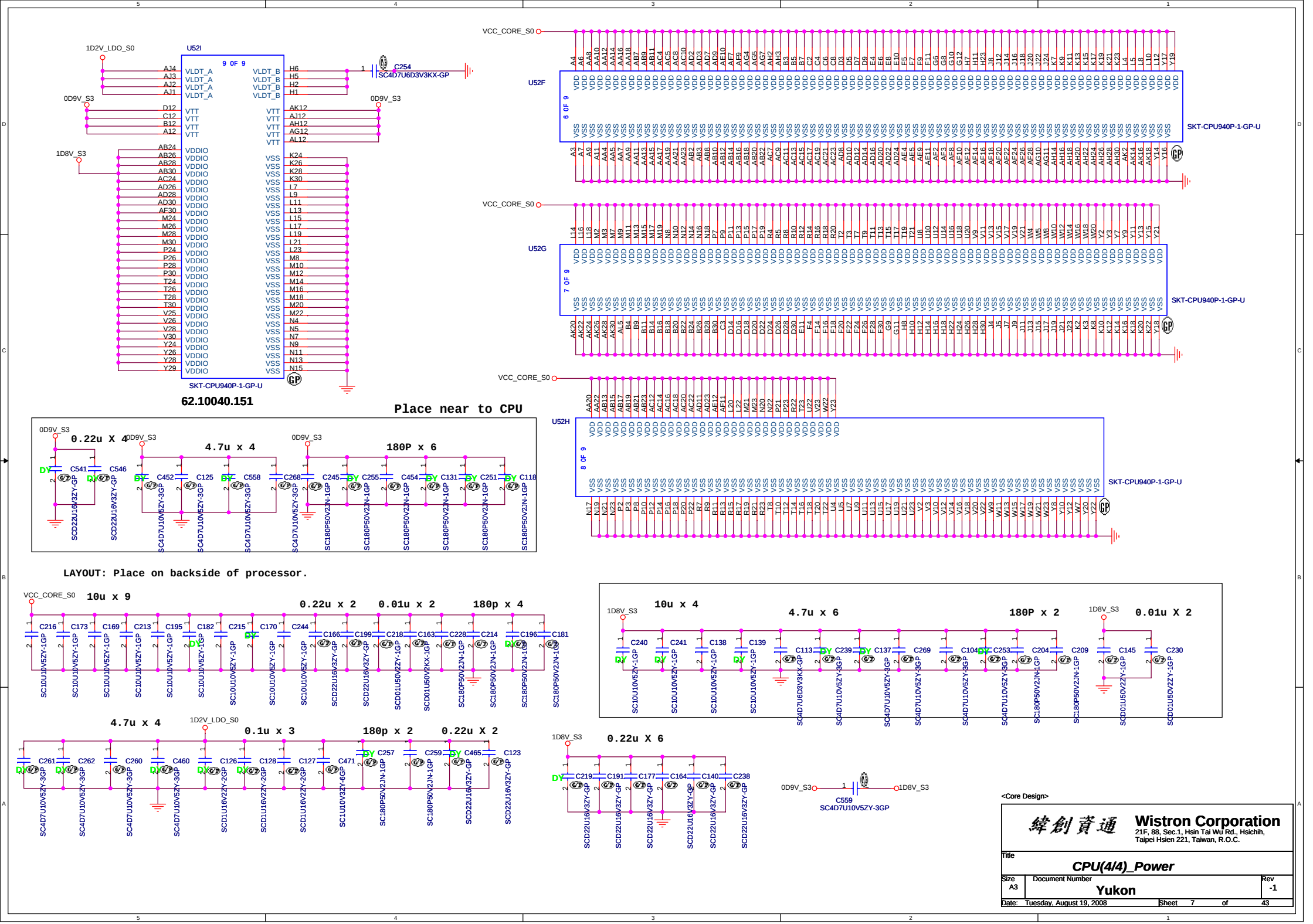
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CLKGEN_ICS951412			
Size	Document Number		Rev
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Date:	Thursday, August 14, 2008	Sheet 3 of	43

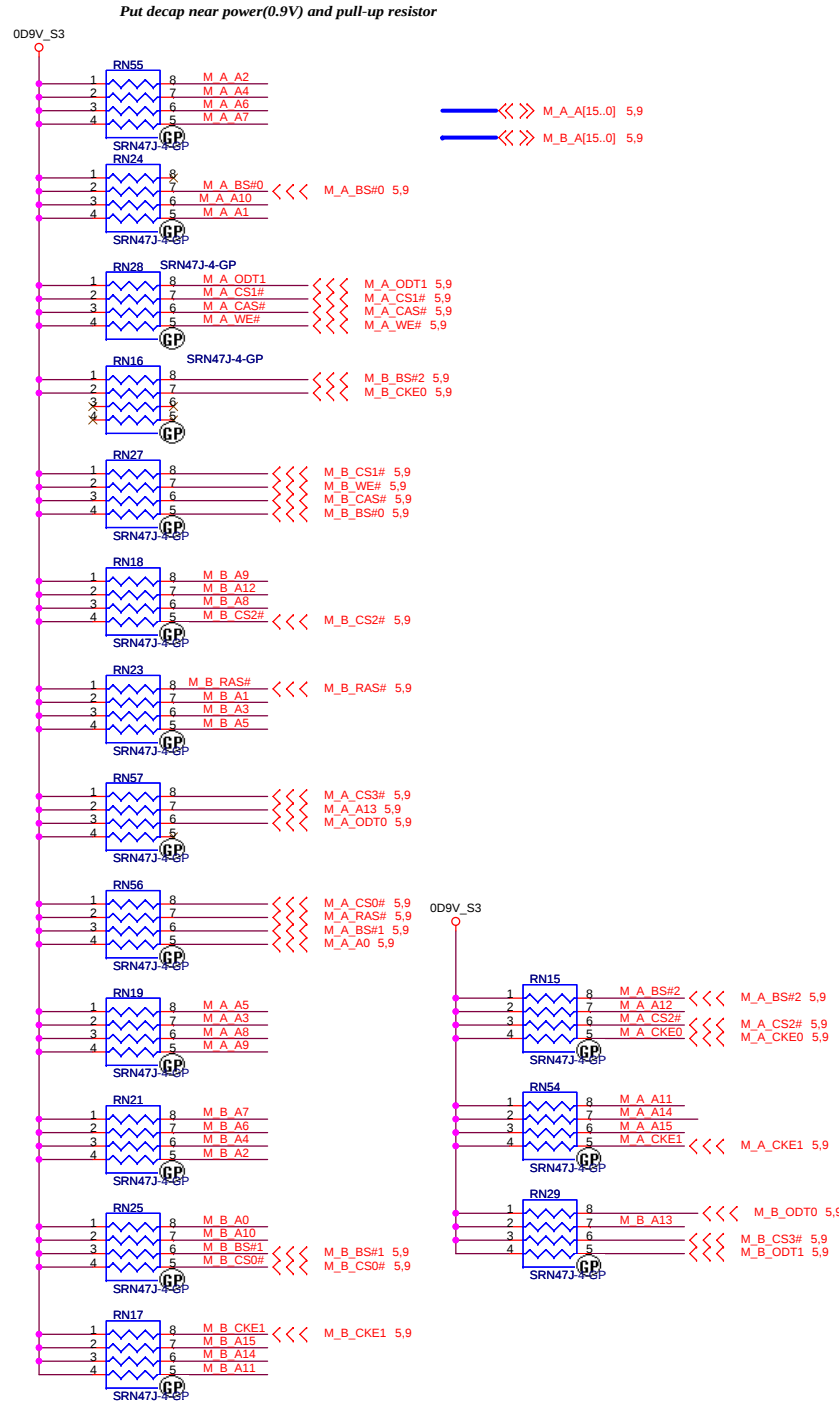


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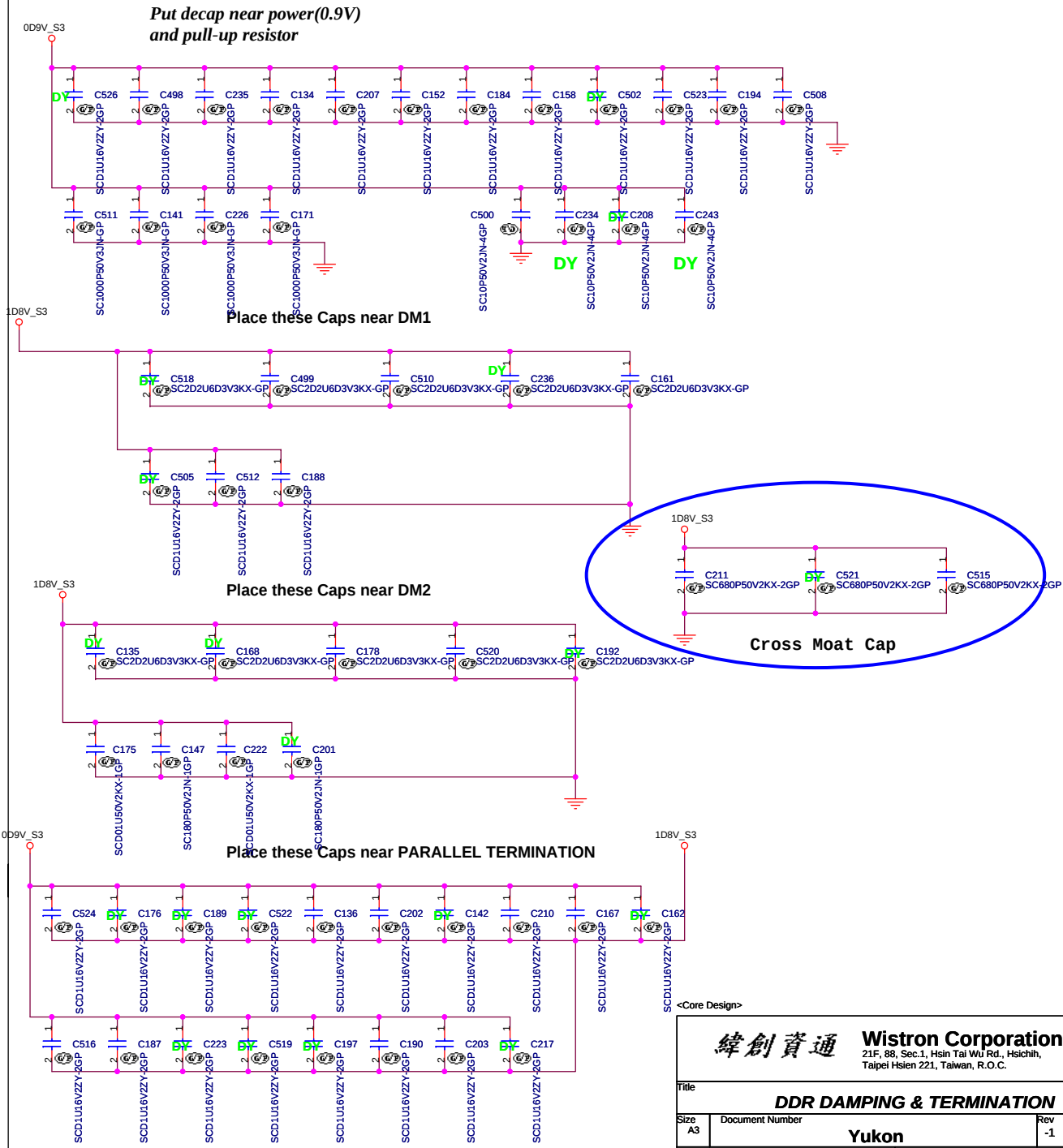
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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CPU(1/4)_HyperTransport I/F			
Size	Document Number		Rev
A3	Yukon		-1
Date:	Thursday, August 14, 2008	Sheet	4 of 43

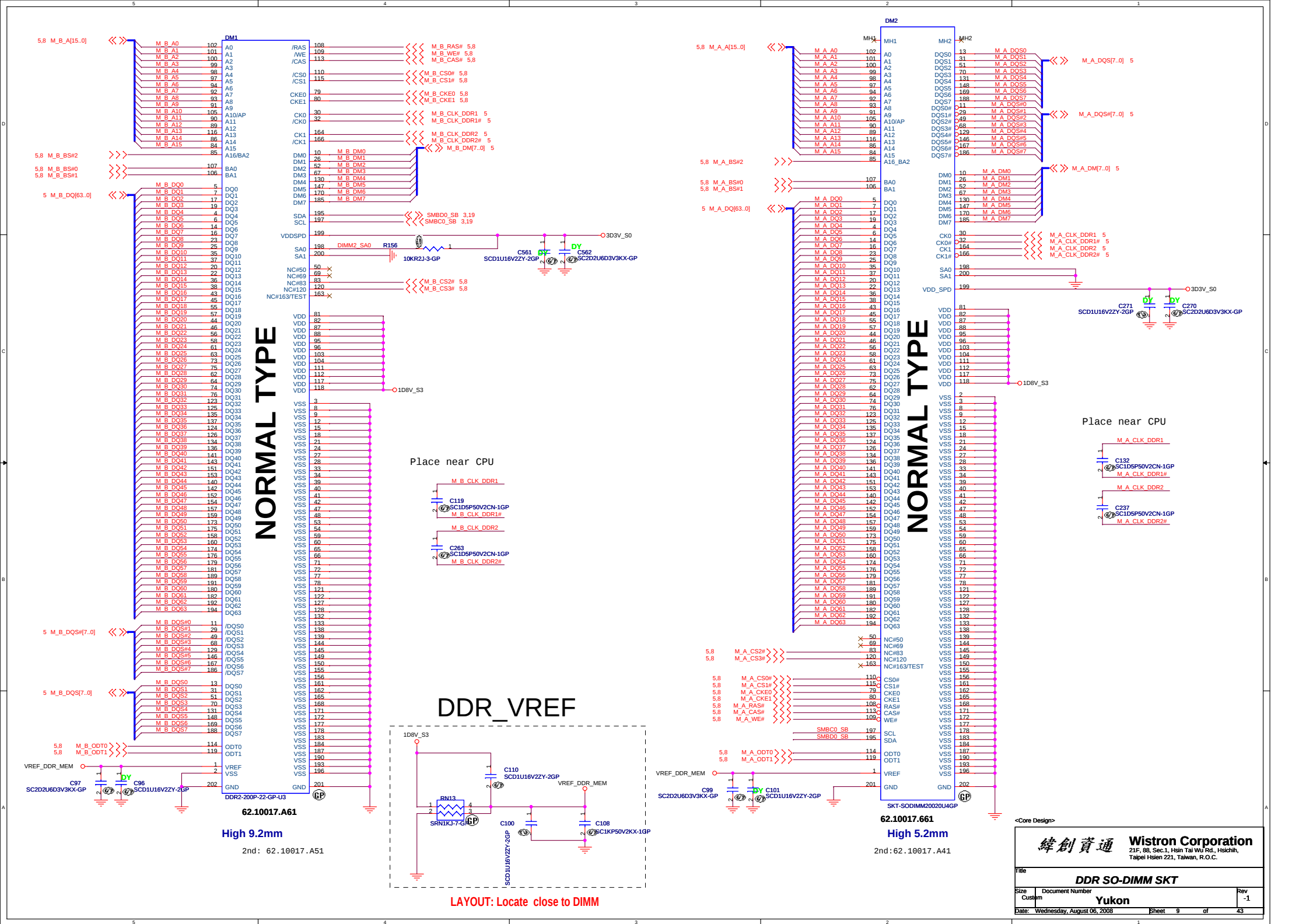


PARALLEL TERMINATION



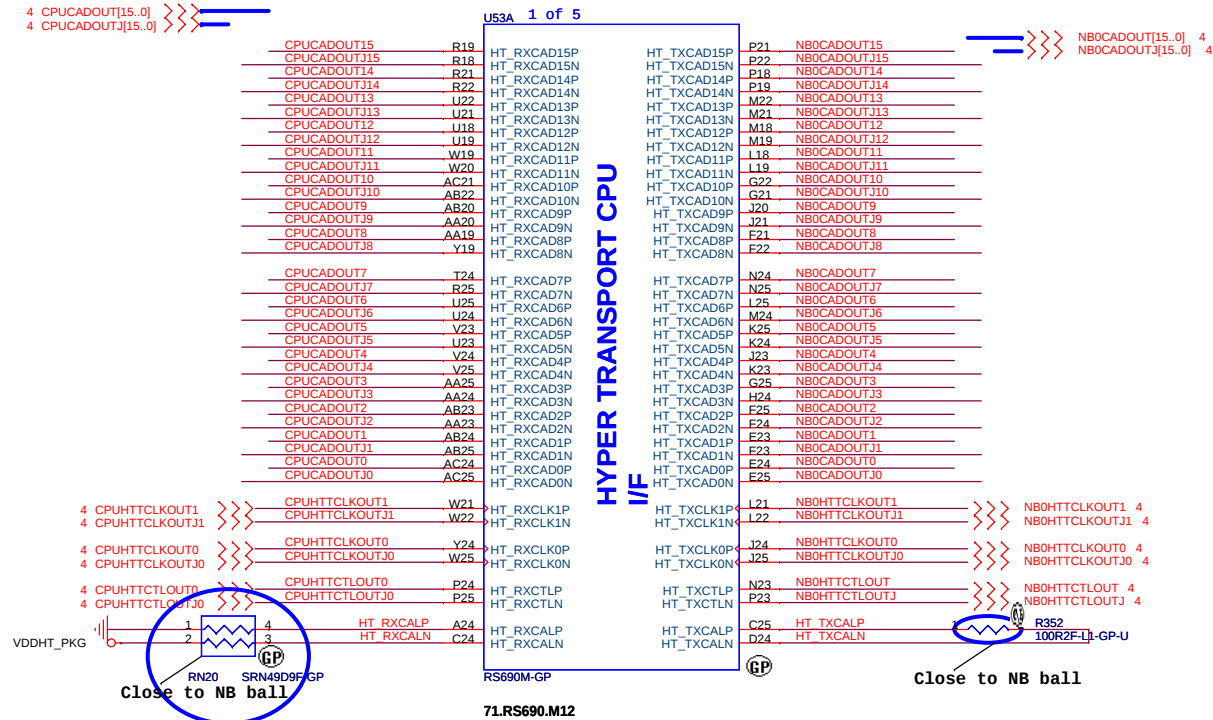
Decoupling Capacitor





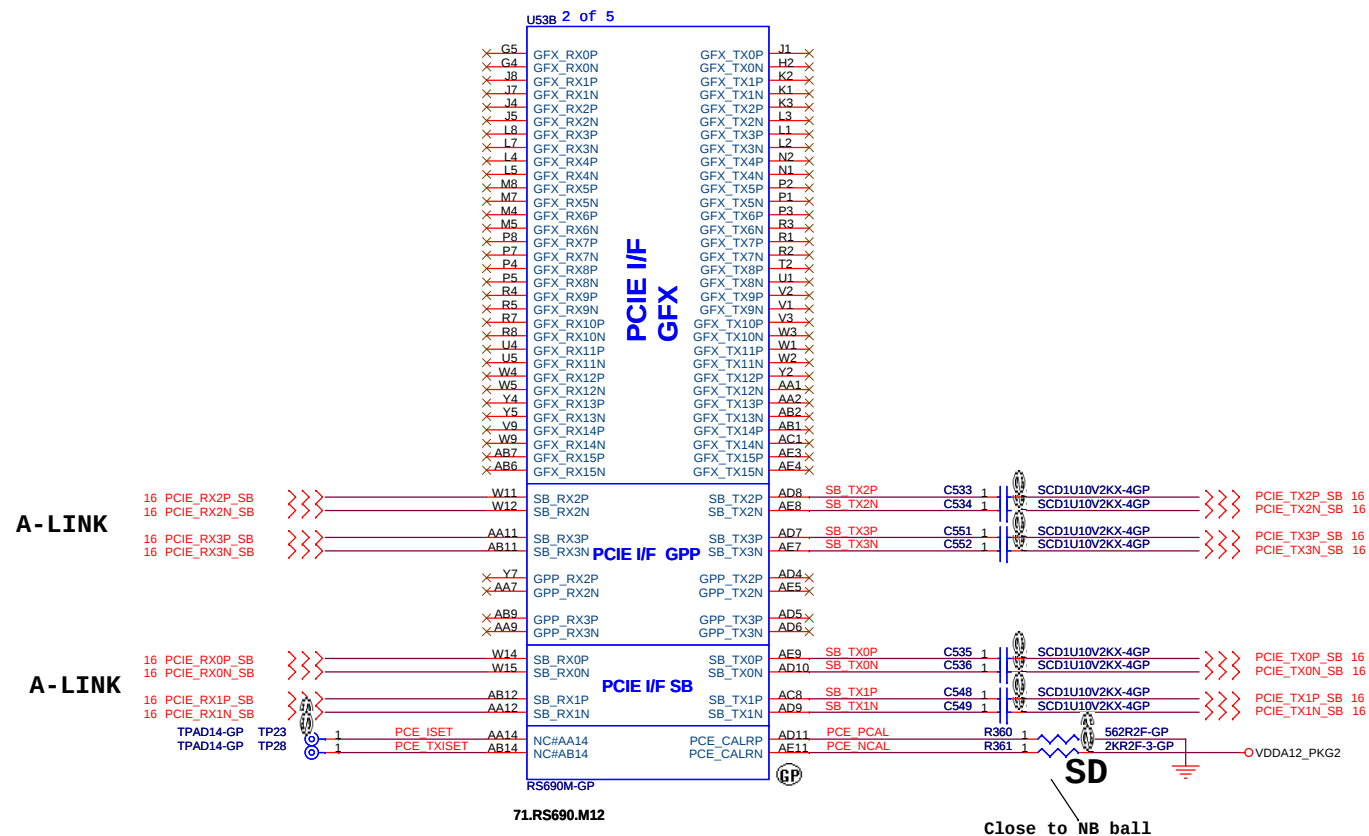
CLAW HAMMER TO NB

NB TO CLAW HAMMER



<Core Design>

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Title			
NB-RS690M HT			
Size	Document Number	Rev	
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Date:	Wednesday, August 06, 2008	Sheet	10 of 43

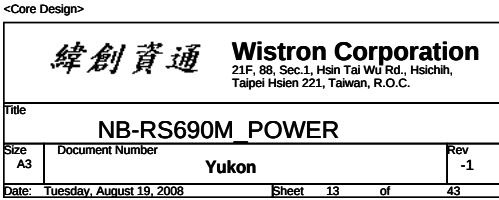


A-LINK
CLOSE TO NB

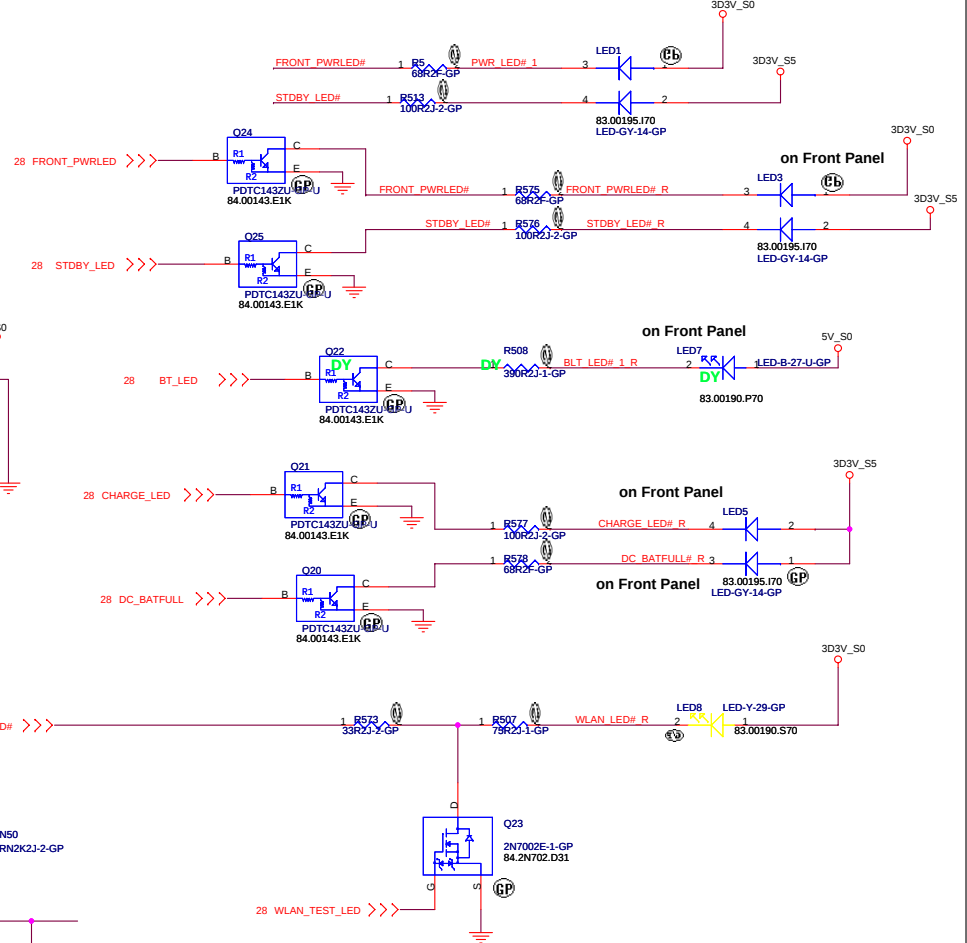
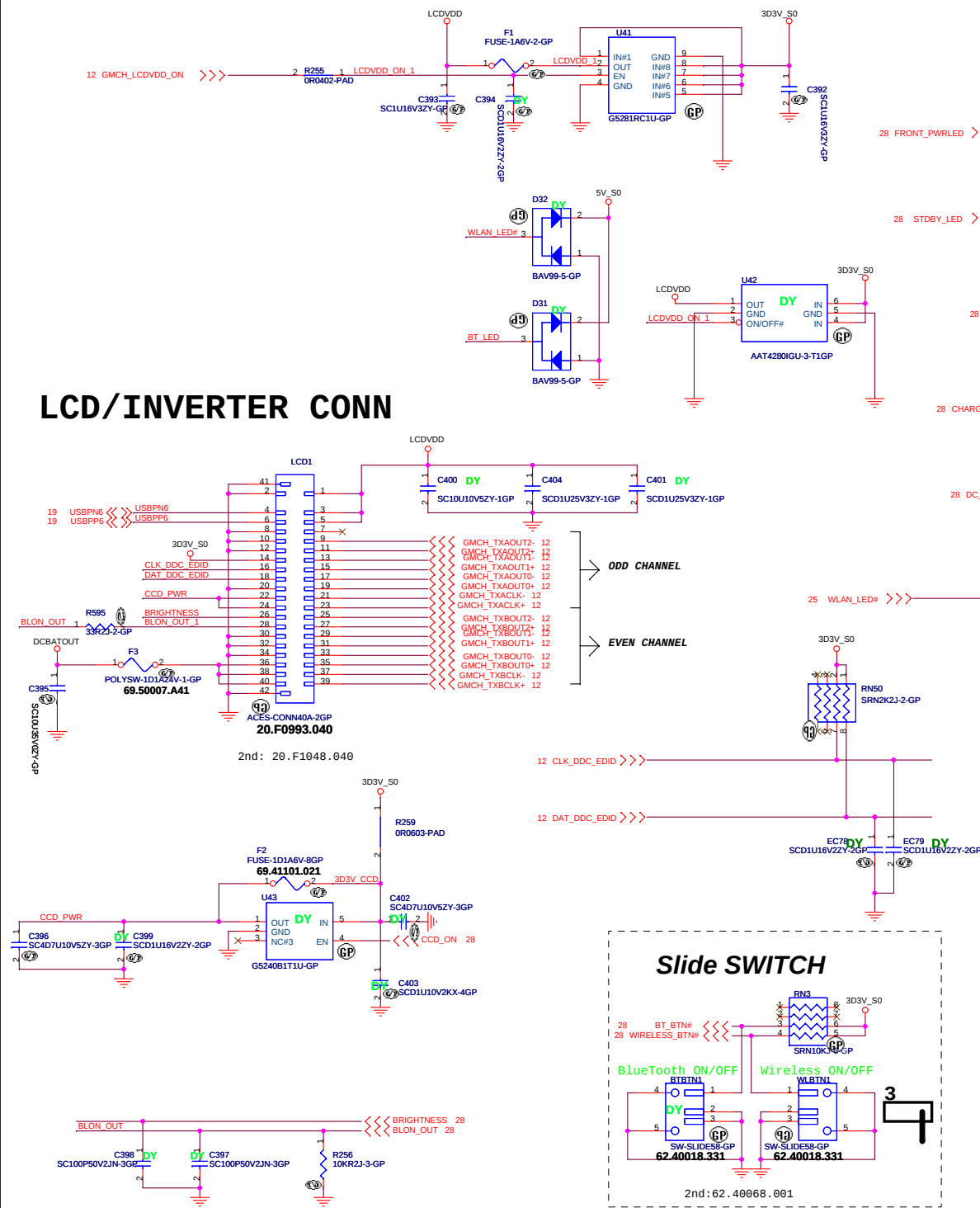
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NB-RS690M MEM/PCIE LINK I/F			
Size	Document Number		Rev
A3	Yukon		-1
Date:	Thursday, August 14, 2008	Sheet 11 of 43	

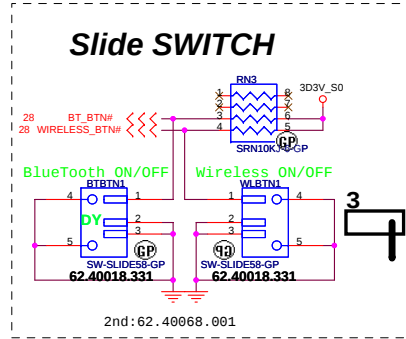
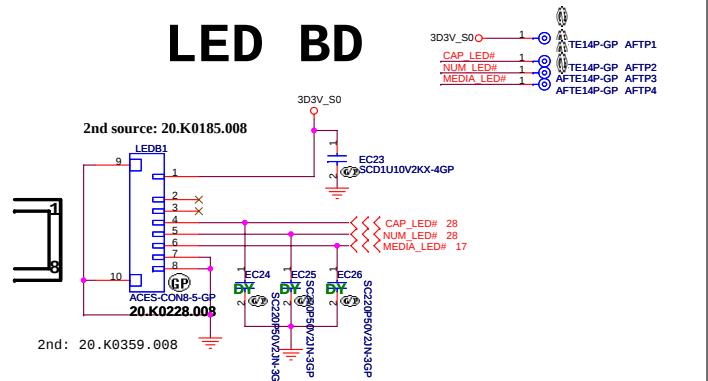




LCD/INVERTER CONN



LED BD



<Variant Name>

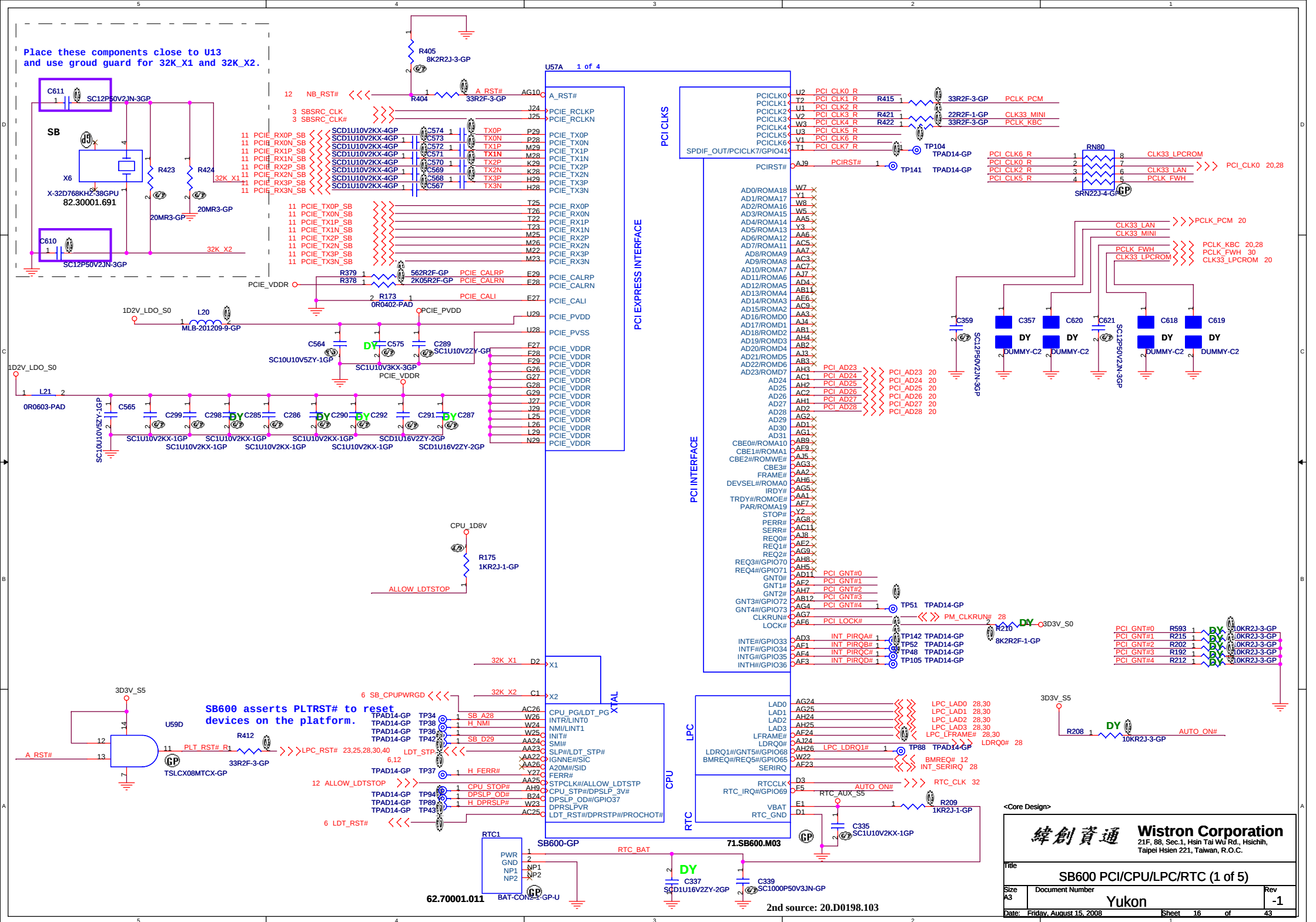
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN & LED**

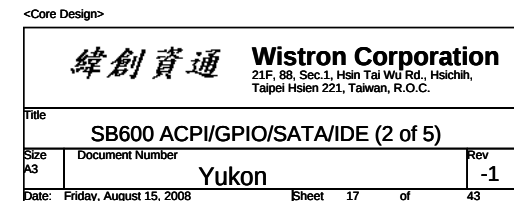
Size: Document Number: **Yukon** Rev: **-1**

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Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.



U57B 2 of 4



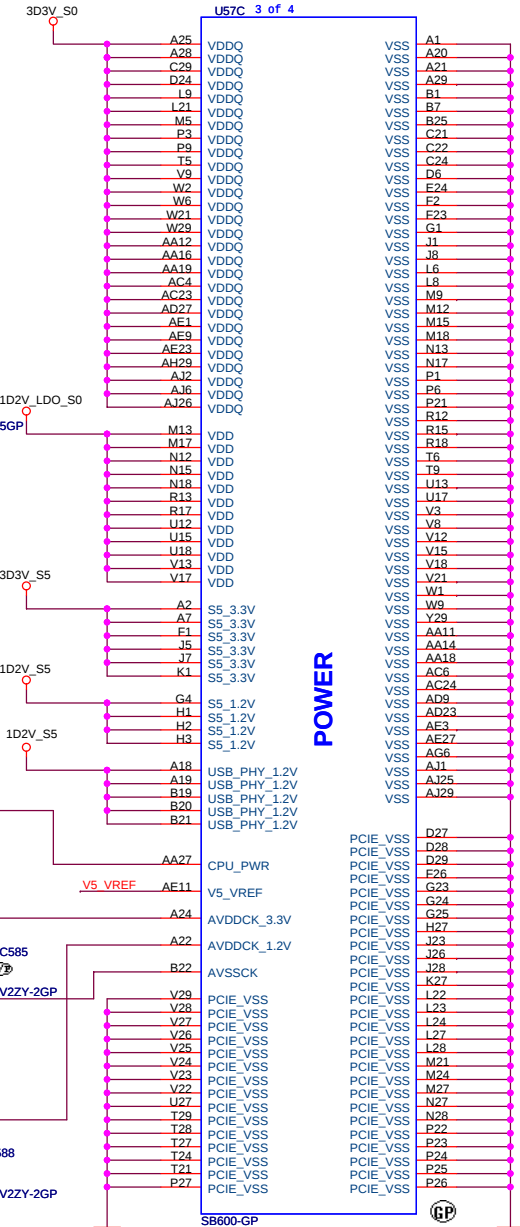
1D2V_S5 Iomax=1A

Vo(cal.)=1.2085V

OCP>=1.8A

$$Vo=0.8*(1+(R1/R2))$$

Place near to SB600

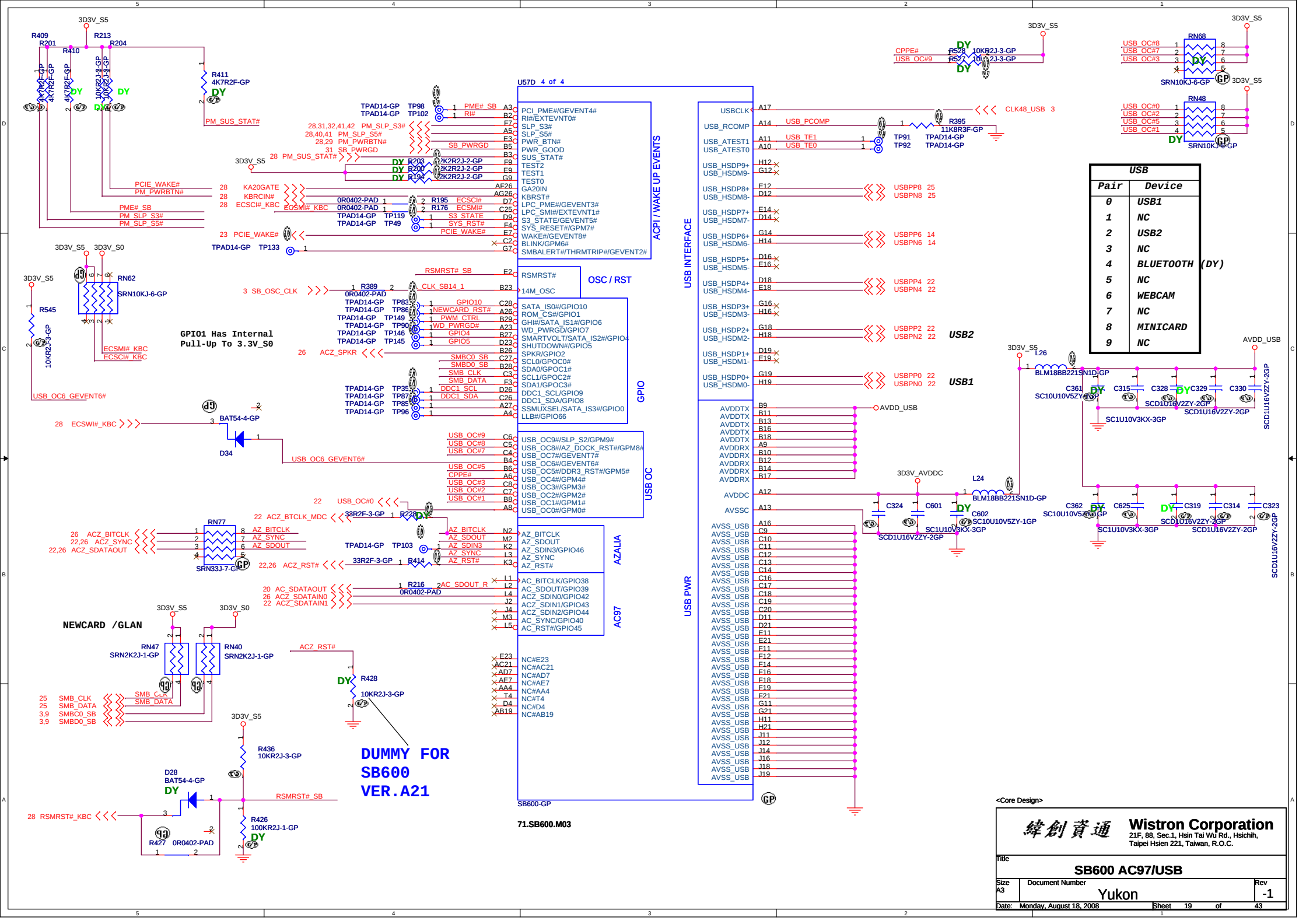


71.SB600.M03

<Core Design>

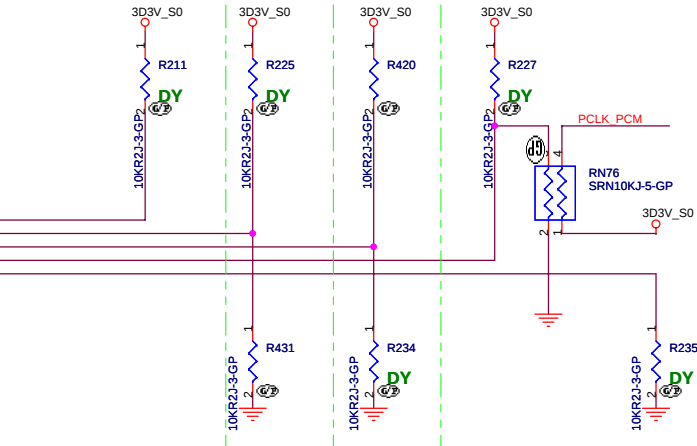
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
SB600 POWER/DECOUPLING			
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PCI_CLK4
PCI_CLK6
PCI_CLK0
PCI_CLK1

19 AC_SDATAOUT
16,28 PCLK_KBC
15 CLK33_LPCROM
16,28 PCI_CLK0
16 PCLK_PCM

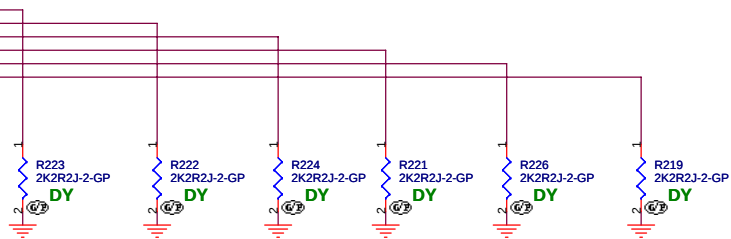


REQUIRED SYSTEM STRAPS

		SB600				
		AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

16 PCI_AD28
16 PCI_AD27
16 PCI_AD26
16 PCI_AD25
16 PCI_AD24
16 PCI_AD23



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

緯創資通

Wistron Corporation

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Title

SB600 STRAPPING PIN

Size A3

Document Number

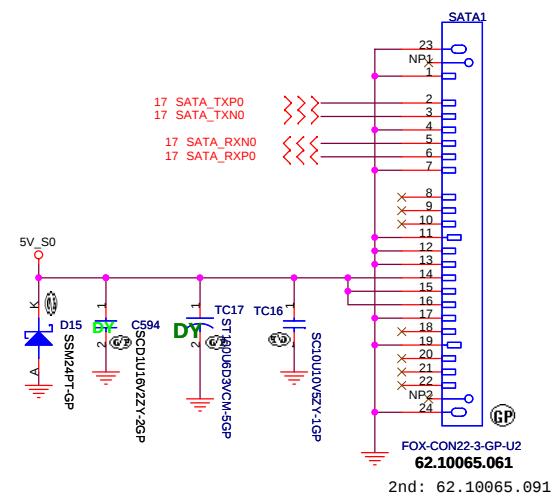
Yukon

Rev -1

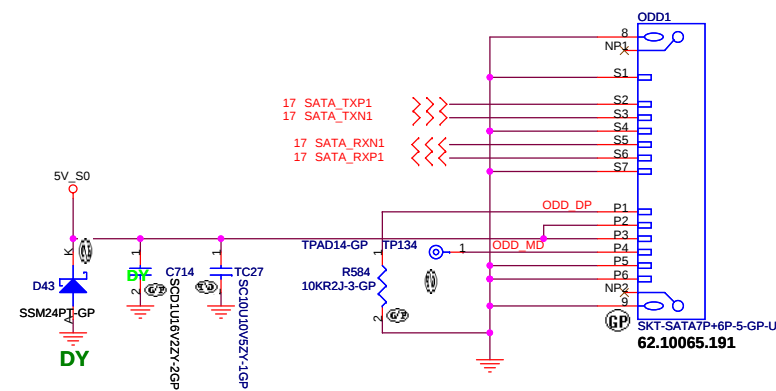
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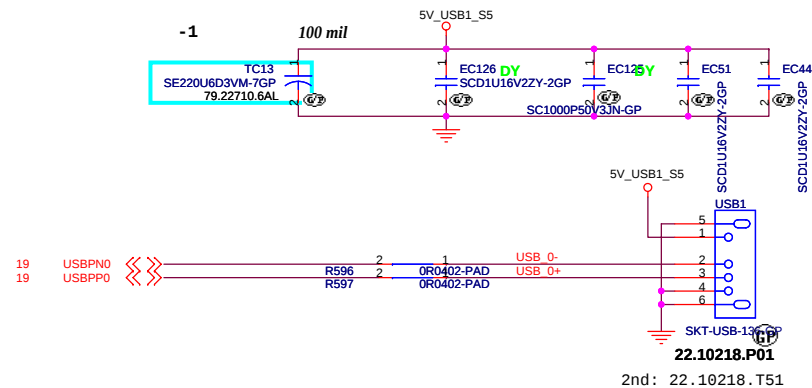
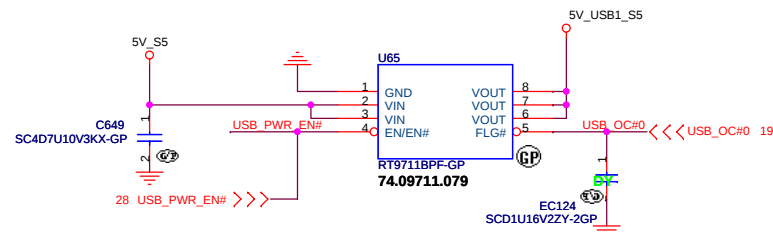
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SATA HD Connector

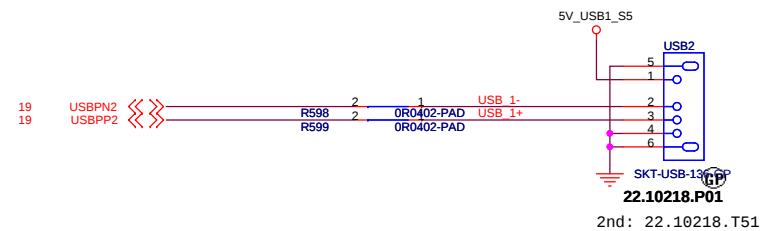
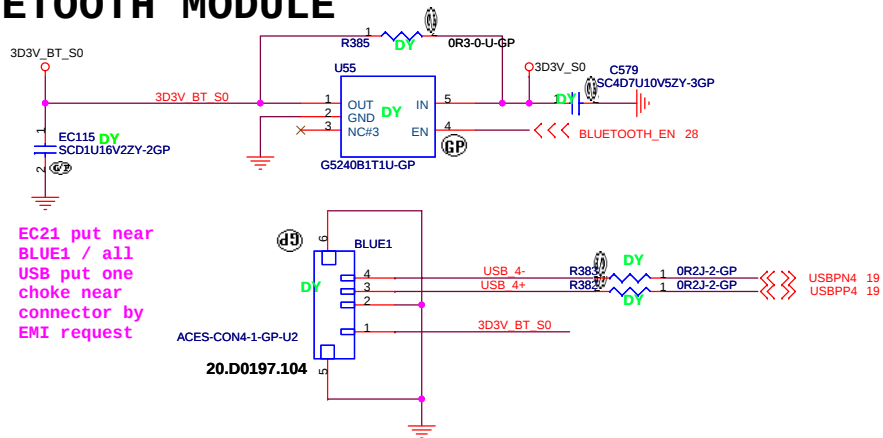


SATA ODD Connector

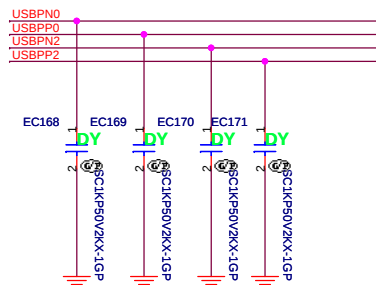
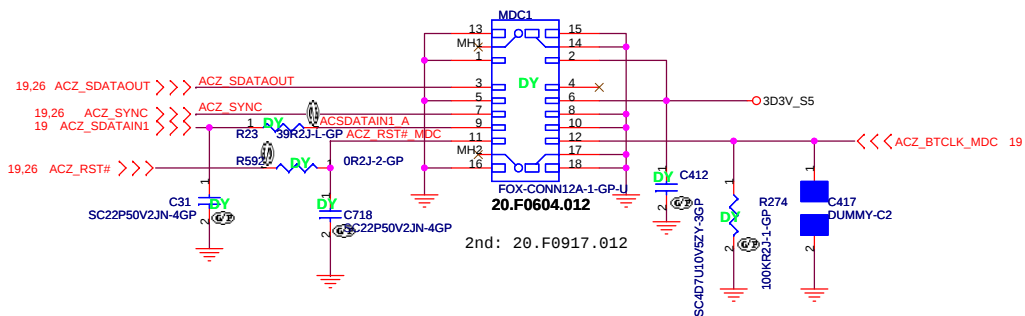




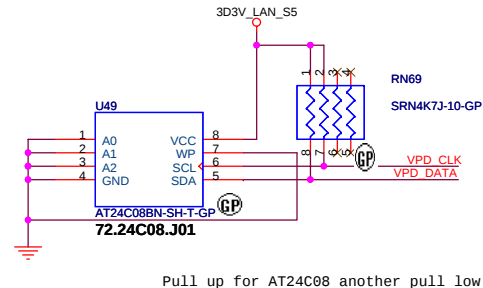
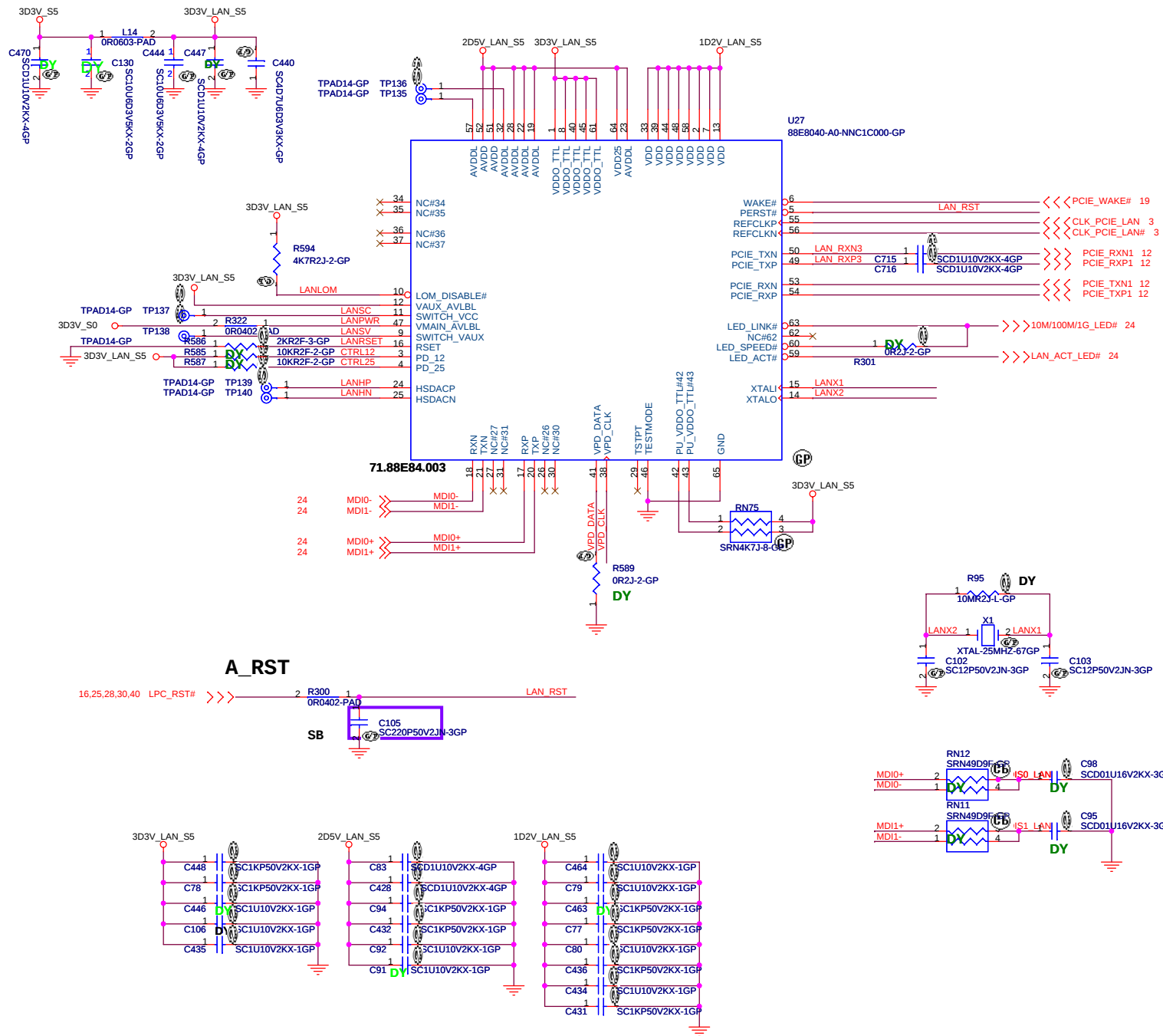
BLUETOOTH MODULE



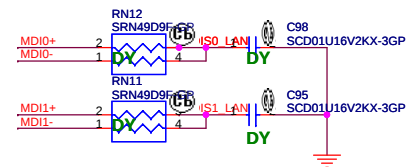
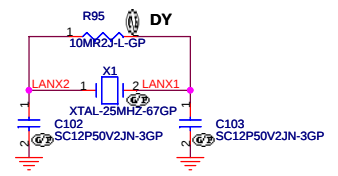
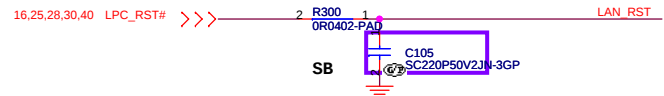
MDC 1.5 CONN



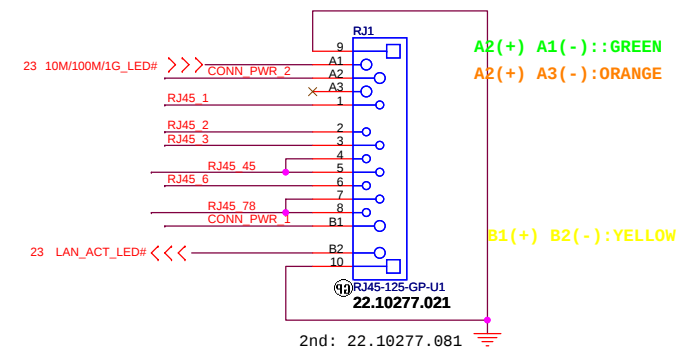
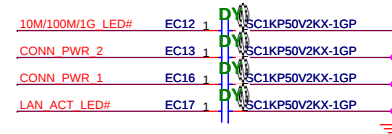
bom1



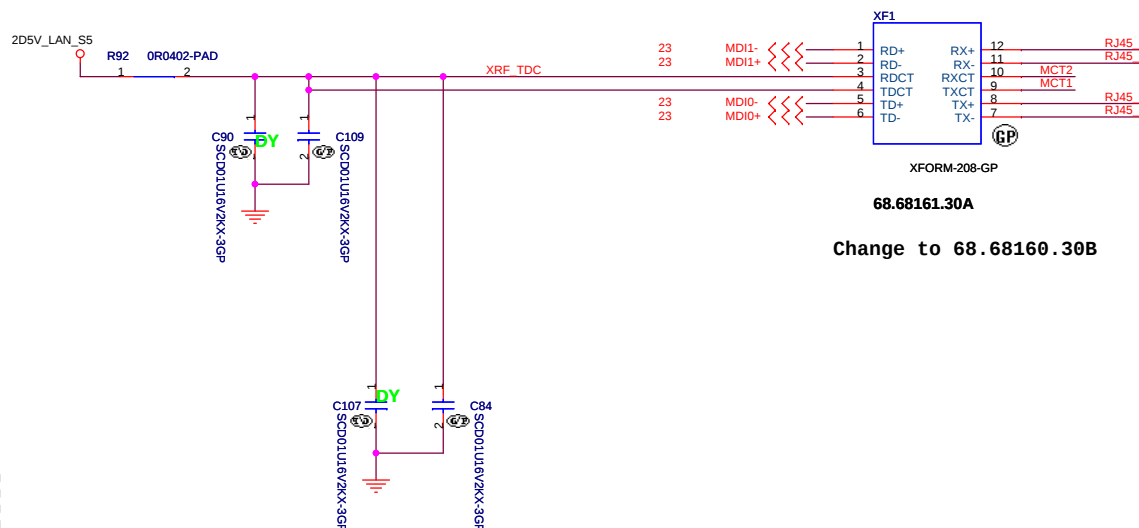
A_RST



LAN Connector



10/100 Lan Transformer



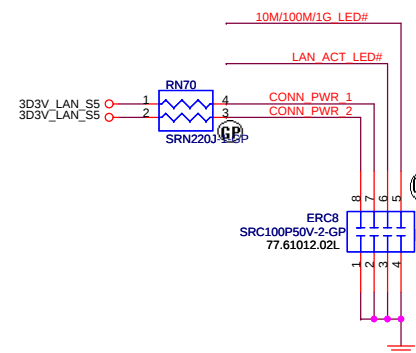
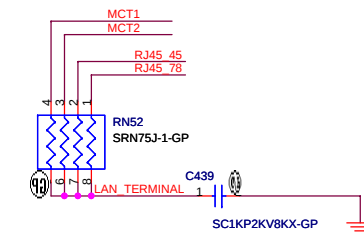
Change to 68.68160.30B

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

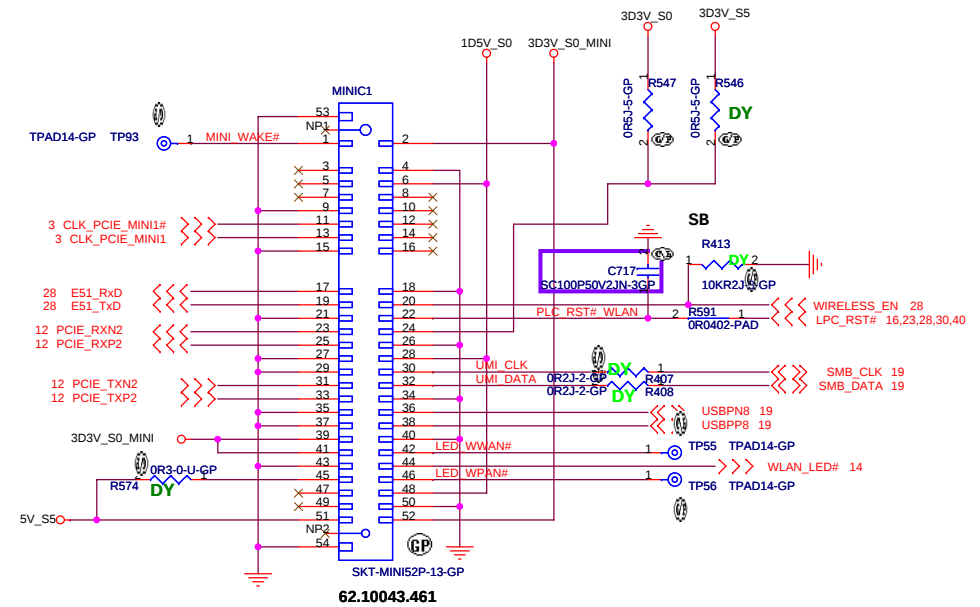


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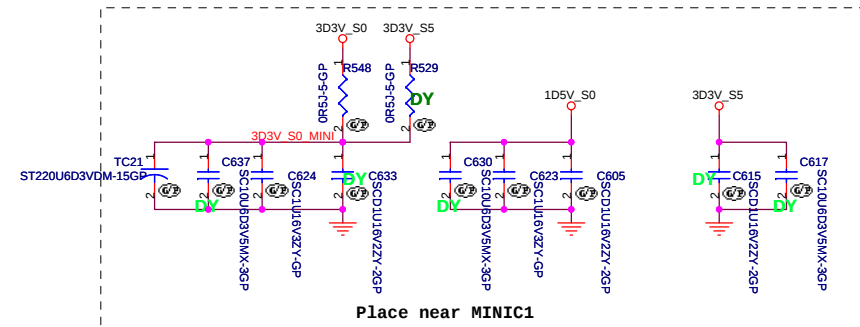
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title LAN Connector		
Size A3	Document Number Yukon	Rev -1
Date: Wednesday, August 13, 2008	Sheet 24 of 43	

Mini Card Connector



2nd:20.F1049.052

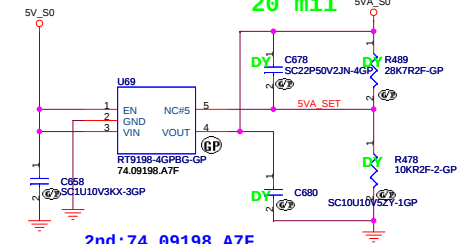


bom1

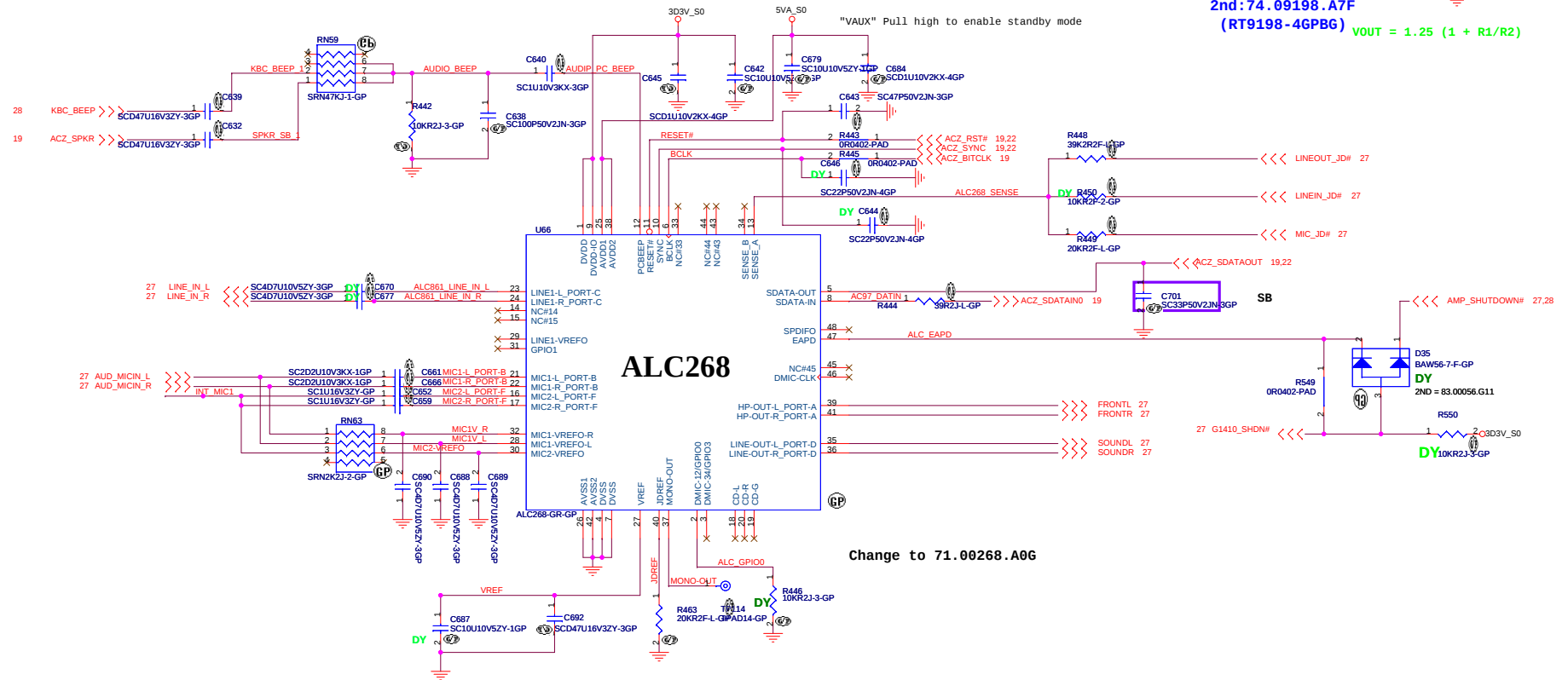
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
MINI CARD			
Size	Document Number		Rev
	Yukon		-1
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POWER GENERATE

Layout
20 mil

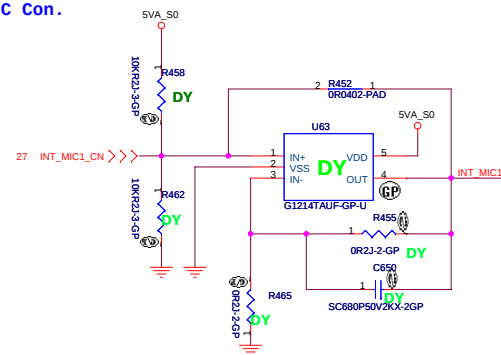


2nd: 74.09198.A7F
(RT9198-4GPBG) $V_{OUT} = 1.25 (1 + R1/R2)$



Change to 71.00268.A0G

Near INTMIC Con.



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

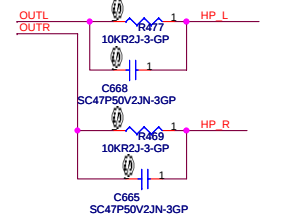
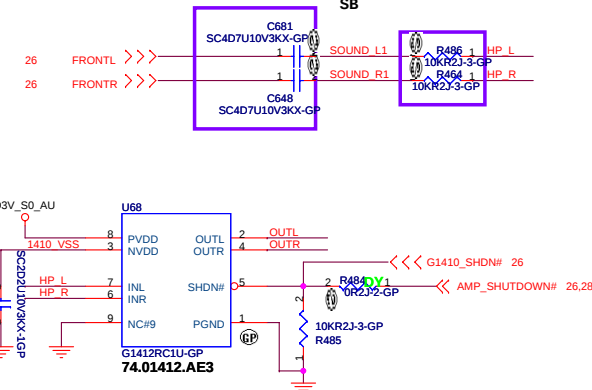
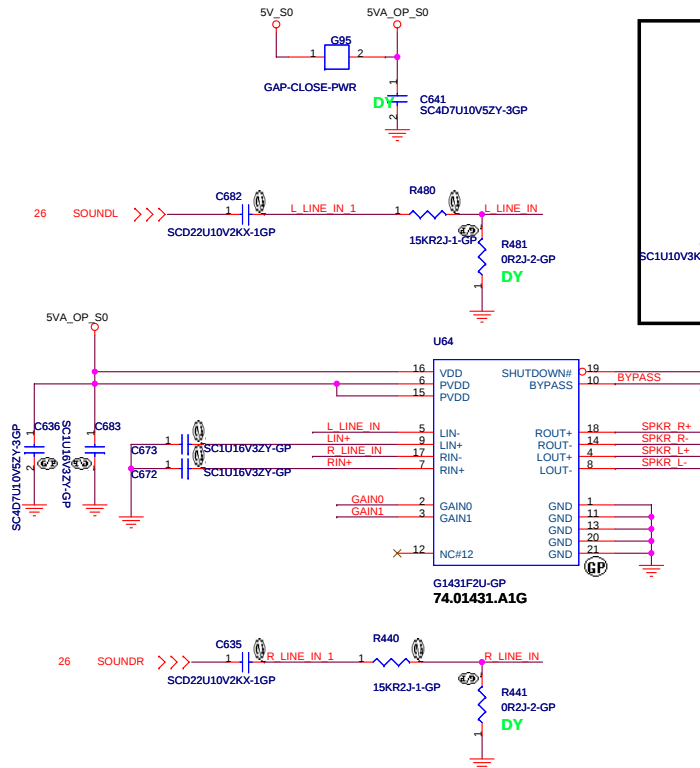
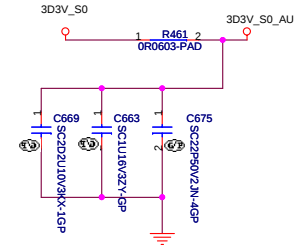
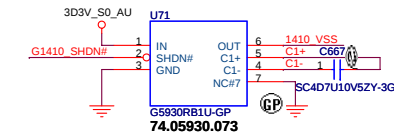
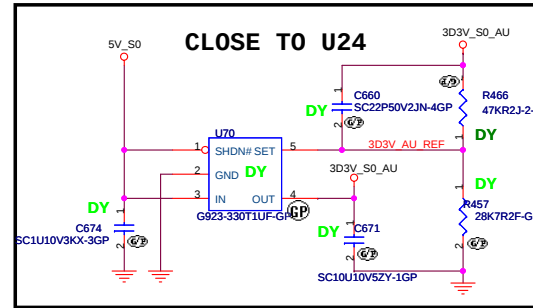
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Size	Document Number	Rev
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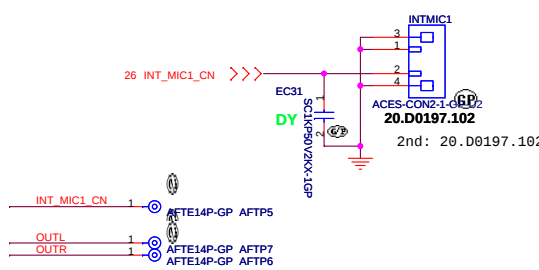
Date: Thursday, August 14, 2008 Sheet 26 of 43

AUDIO OP AMPLIFIER

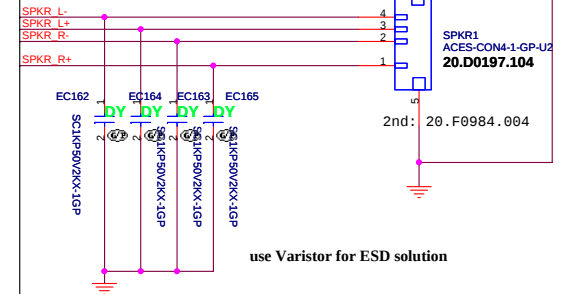
KBC_MUTE_GPIO8



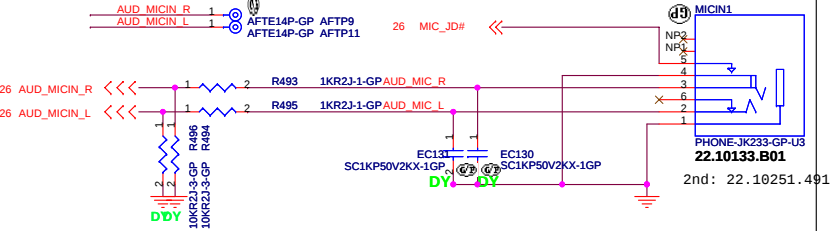
Internal Microphone



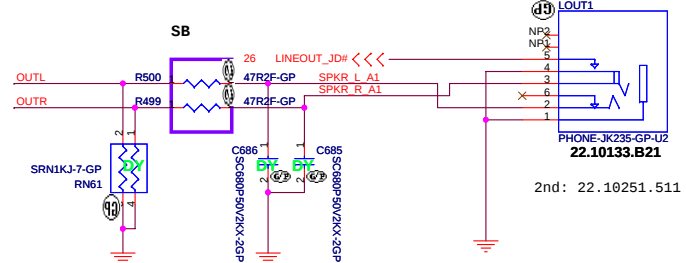
Internal Speaker

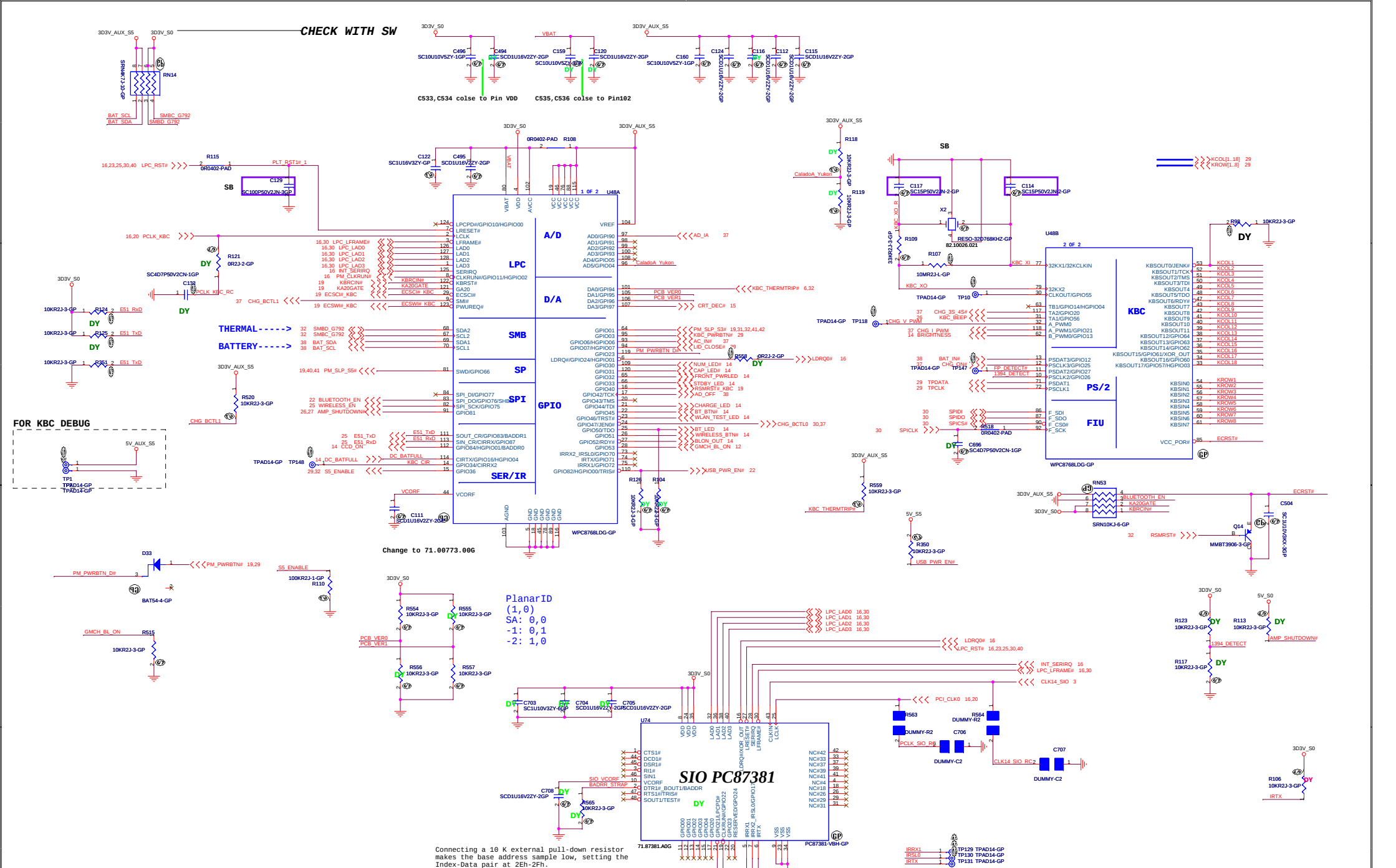


MIC IN



LINE OUT

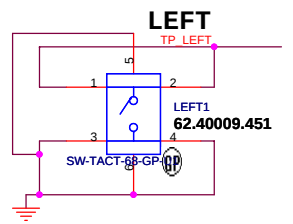
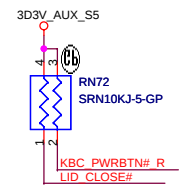
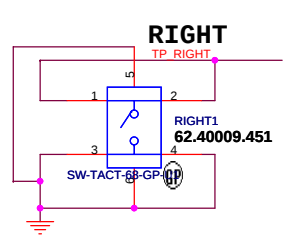
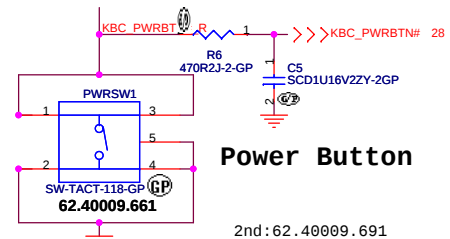




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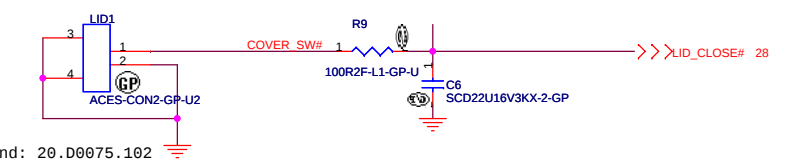
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
 Taipei Hsinchu 300, Taiwan, R.O.C.

Rev: **KBC WPC8768L**
 Size: **A2**
 Document Number: **Yukon**
 Date: Tuesday, August 19, 2008 Sheet 28 of 43

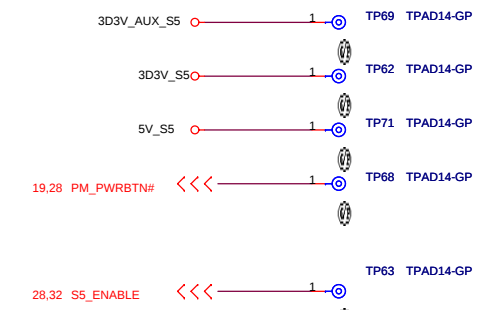


Cover Up Switch

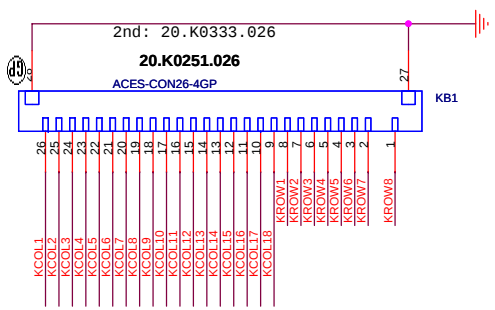
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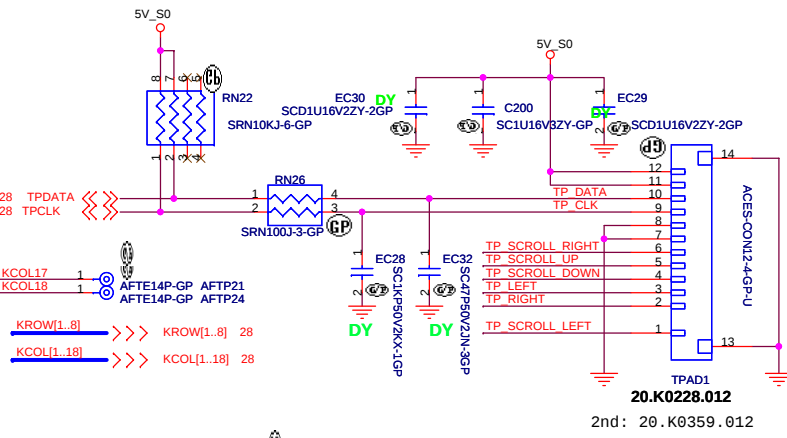
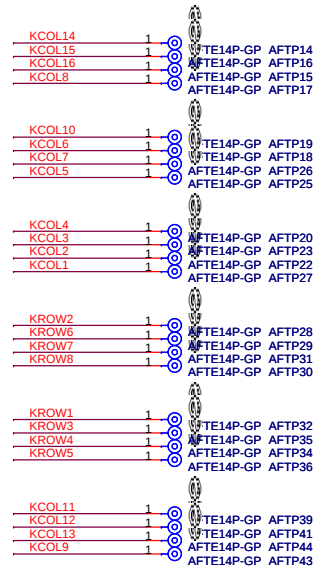
Check test point



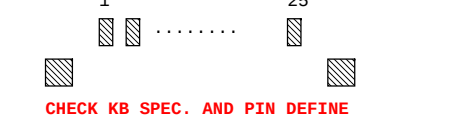
Test Point 放在 Dimm Door 打開可量測處



EMI Bypass cap.

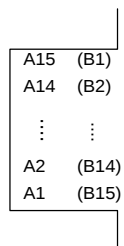


Internal KeyBoard CONN



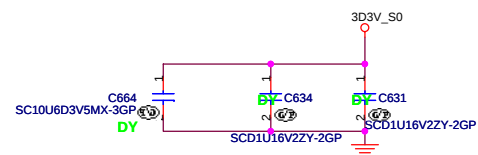


TOP VIEW

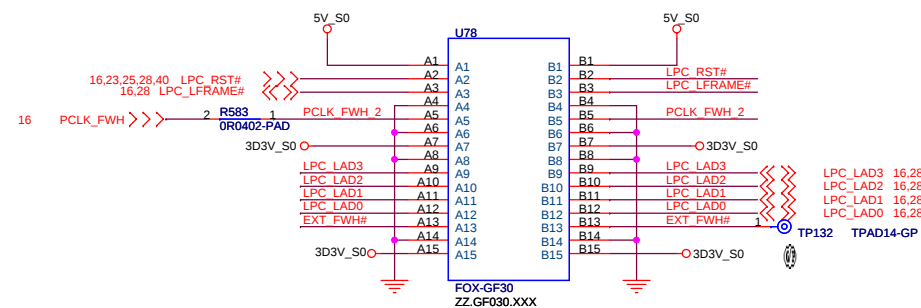


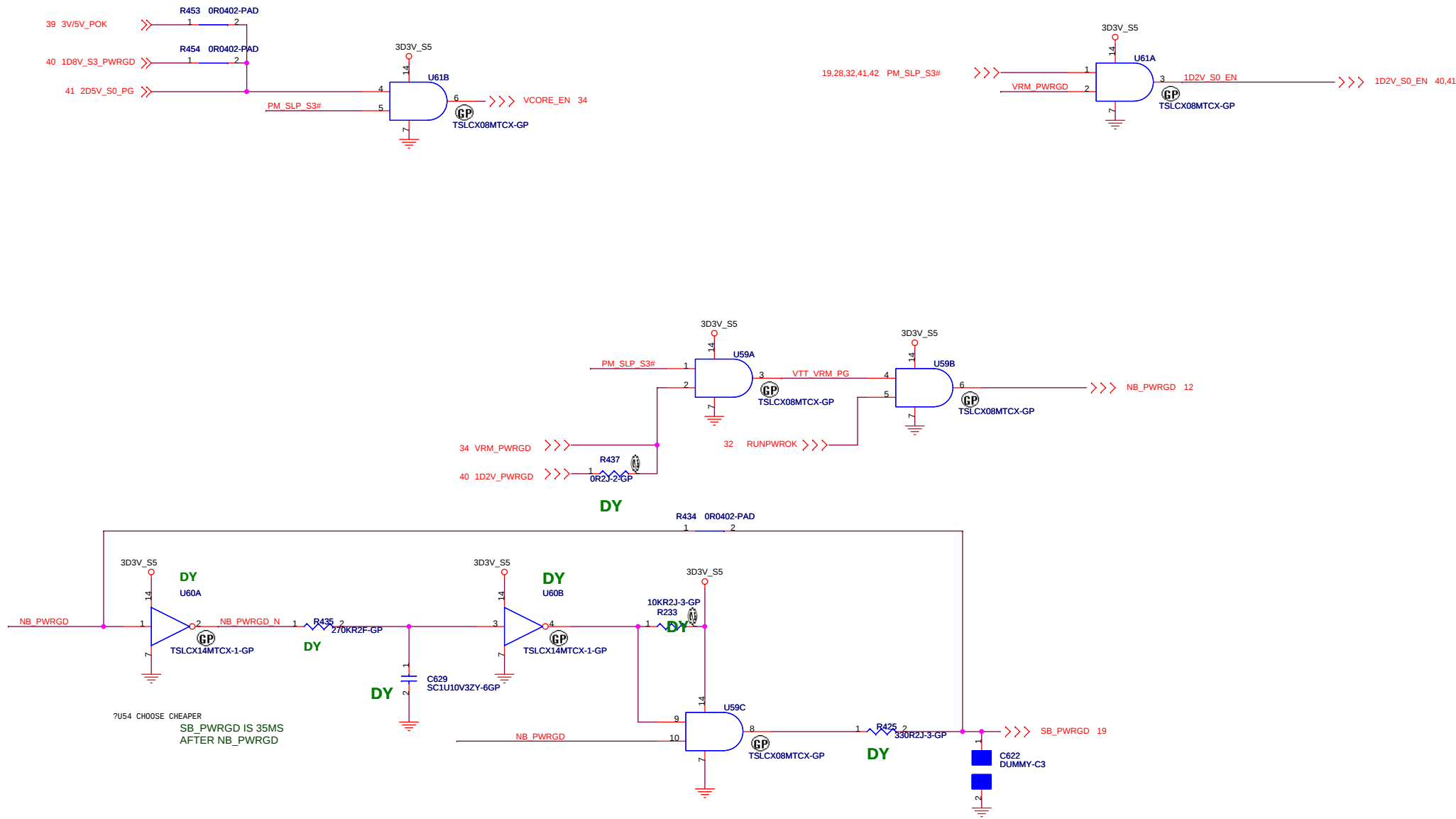
(BOTTOM VIEW)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



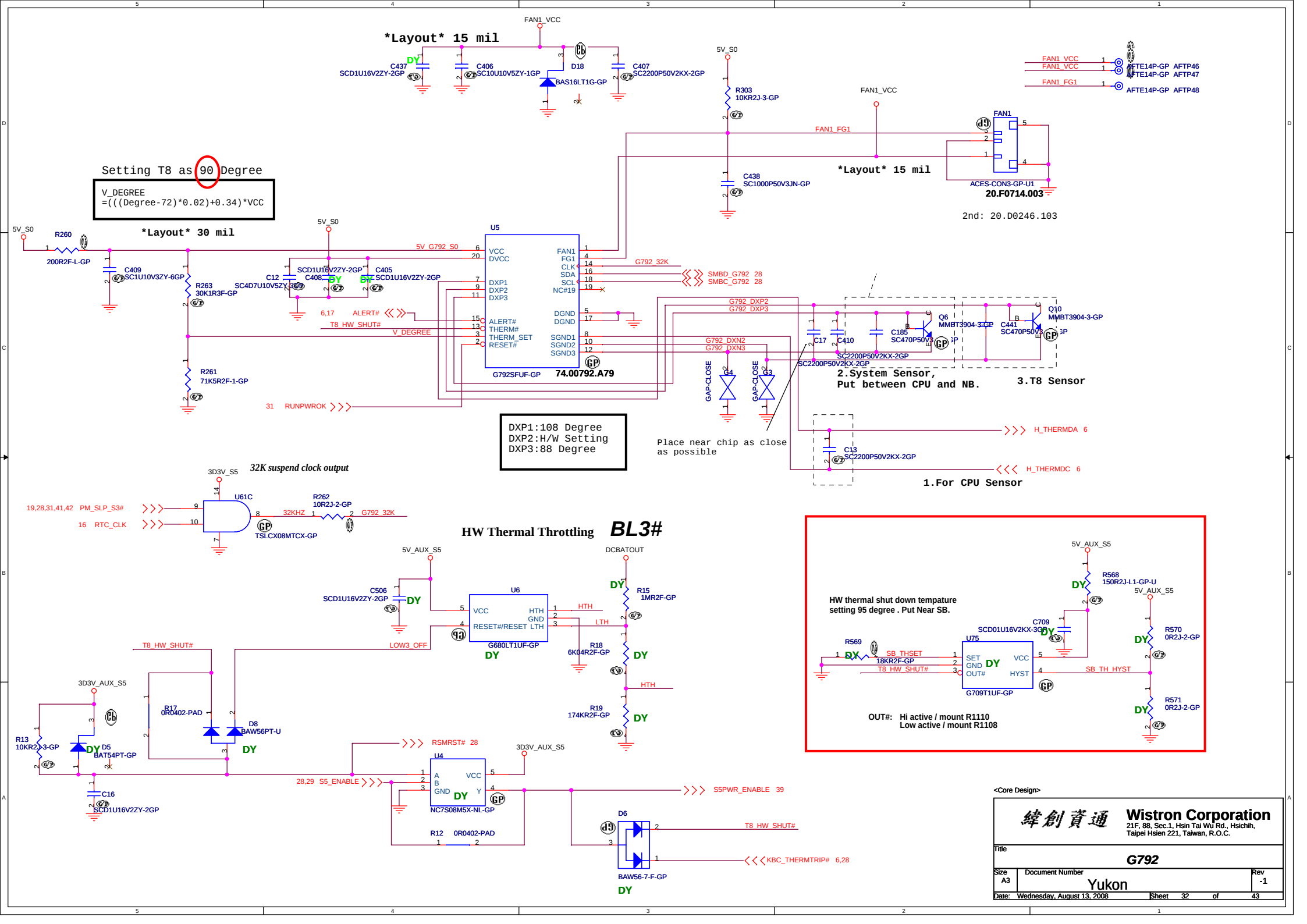
GOLDEN FINGER FOR DEBUG BOARD



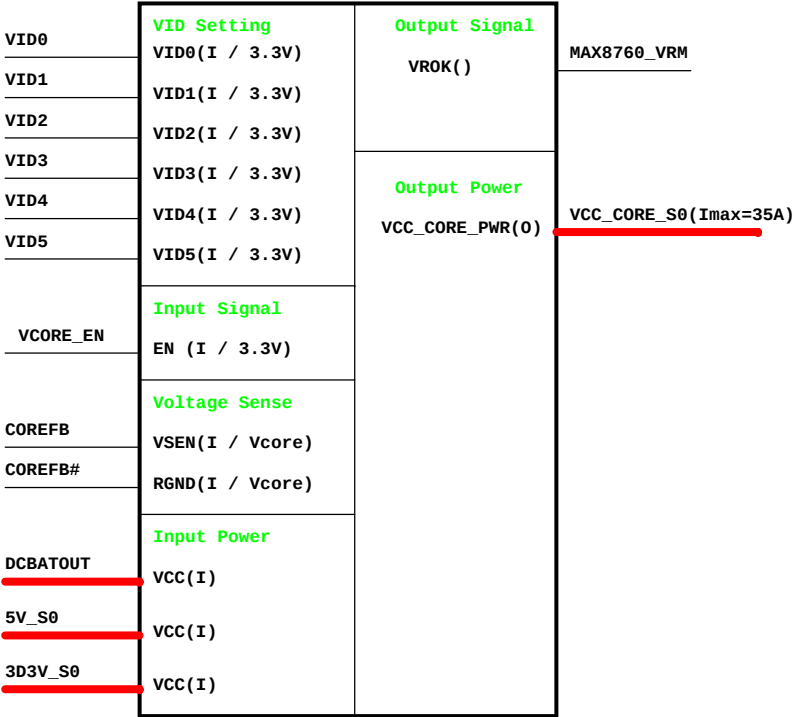


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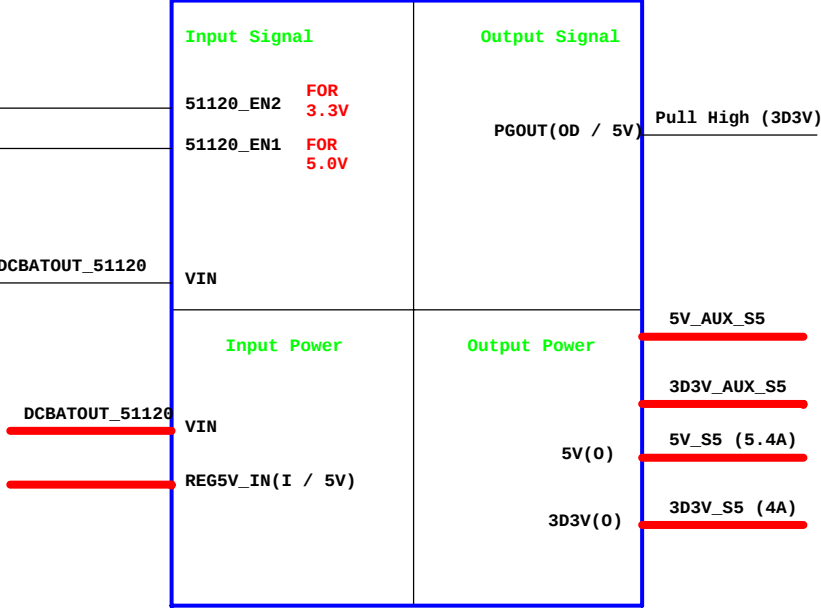
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Title			
POWERGOOD&ENABLES(1/2)			
Size	Document Number		Rev
A3	Yukon		-1
Date:	Wednesday, August 13, 2008	Sheet 31 of 43	



CPU_CORE
ISL6264CRZ



TI TPS51120
3D3V/5V



2D5V_S0



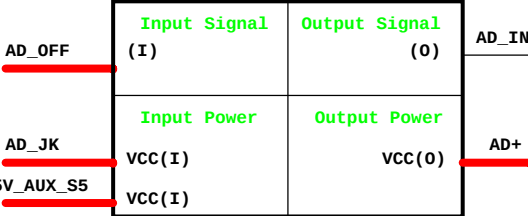
APL5913

1D8V_S5

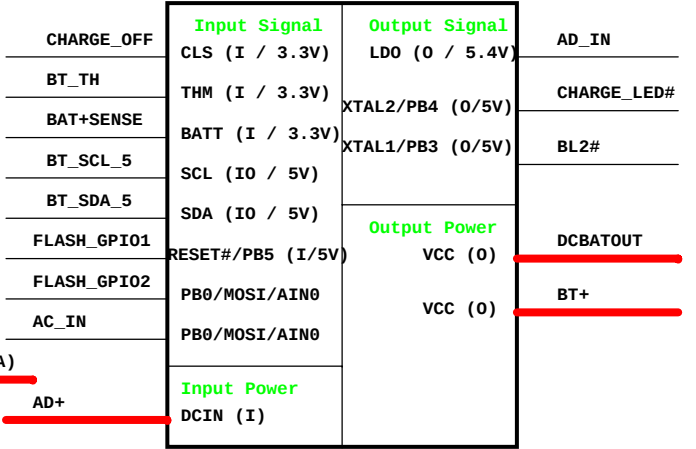


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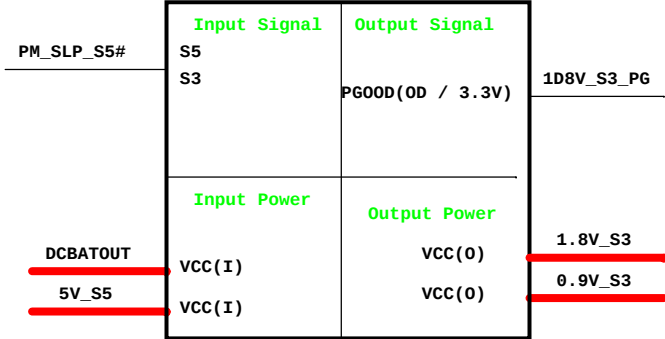
Adapter



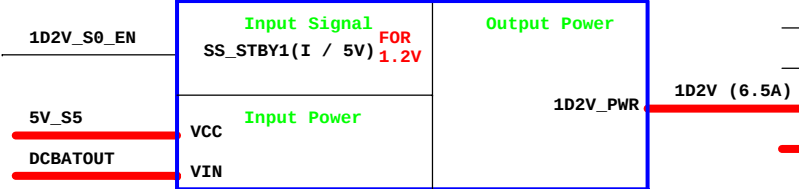
Charger_ISL6255



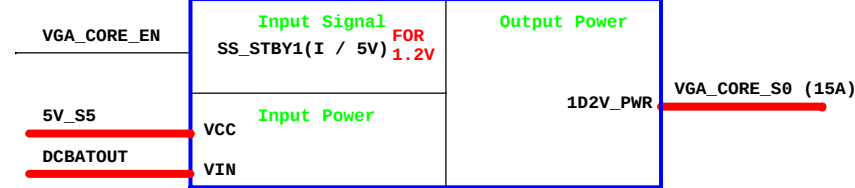
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



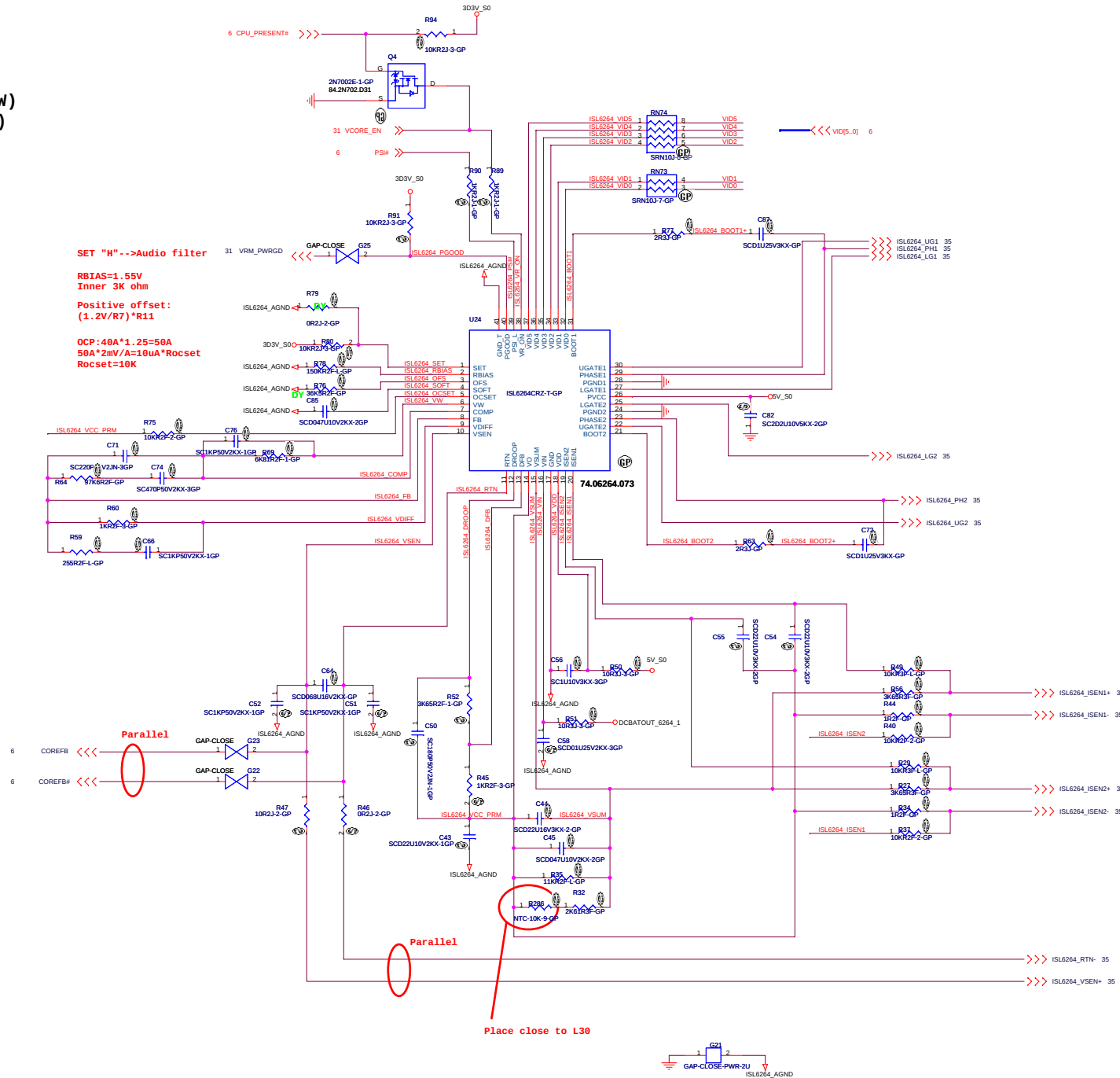
ISL6268_VGA_CORE



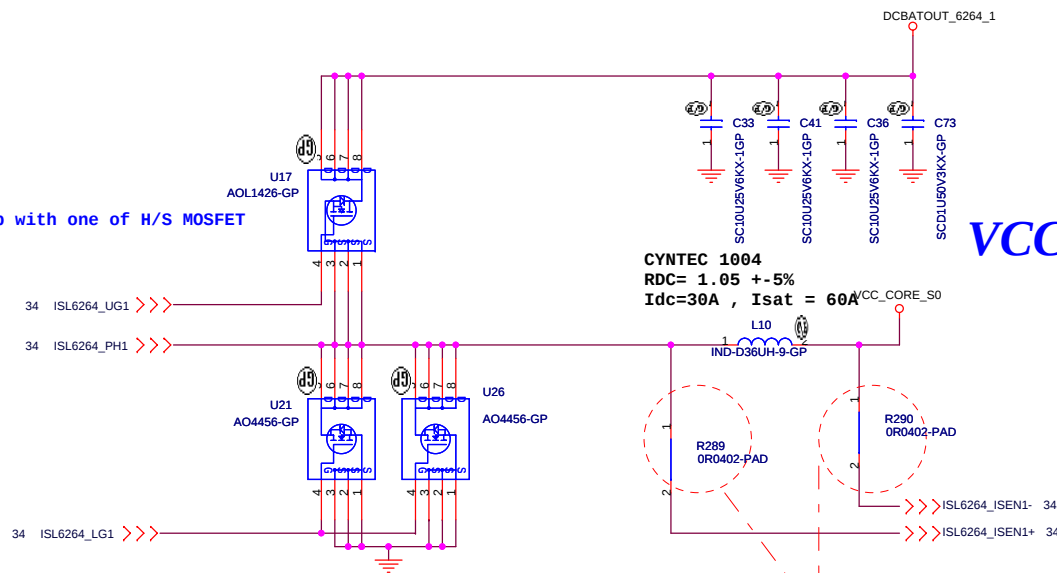
CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.750
1	0	0	0	0	1	0.7375
1	0	0	0	1	0	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375

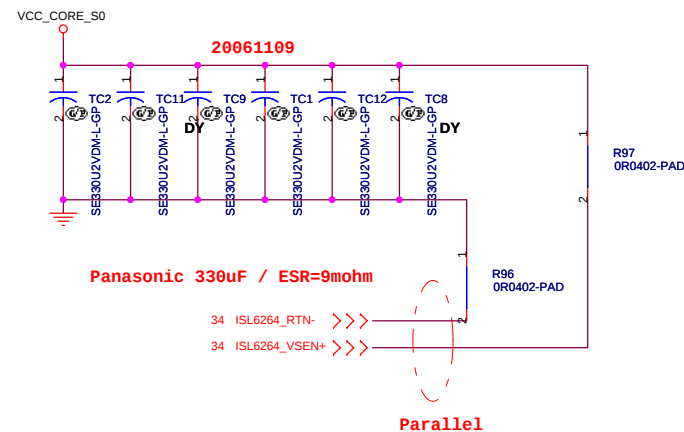
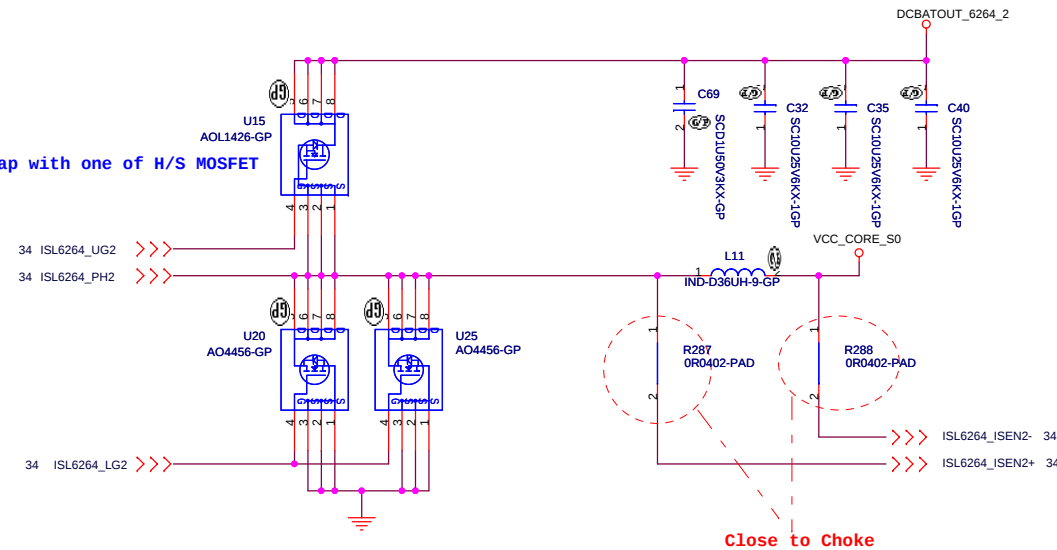


Overlap with one of H/S MOSFET



VCC_CORE_S0

Overlap with one of H/S MOSFET

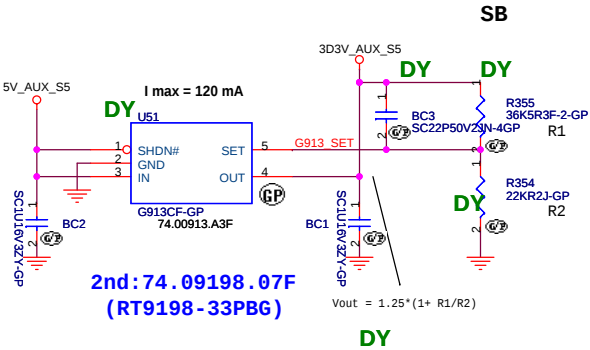


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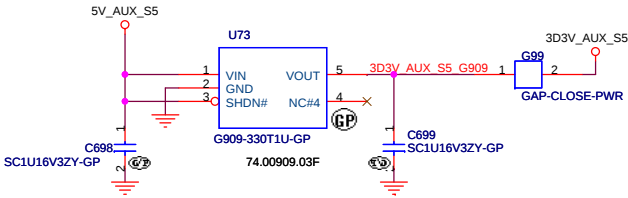
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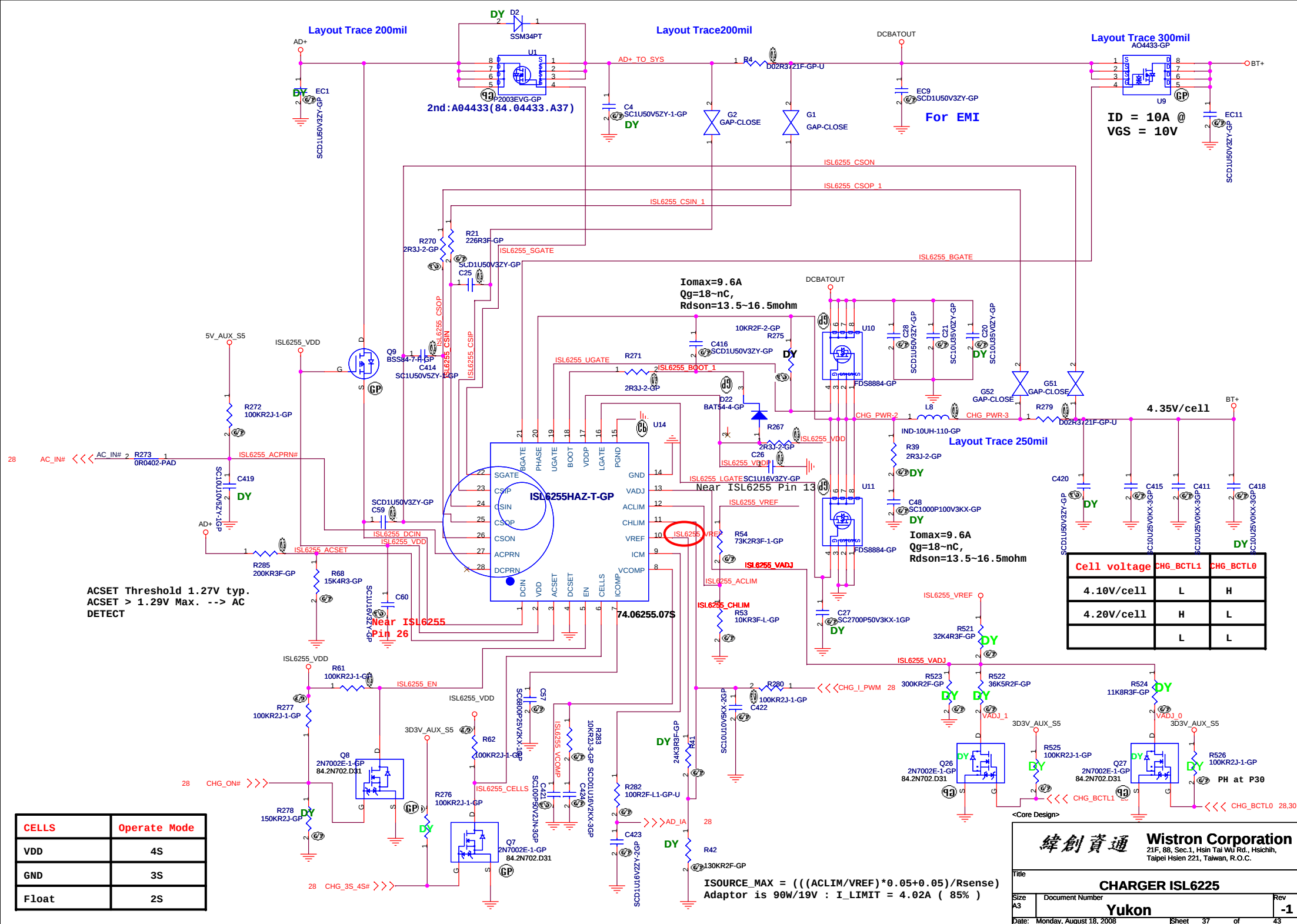
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CPU Vcore Power_2		
Size	Document Number	Rev
A3		-1
Yukon		
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Aux Power
3D3V_AUX_S5

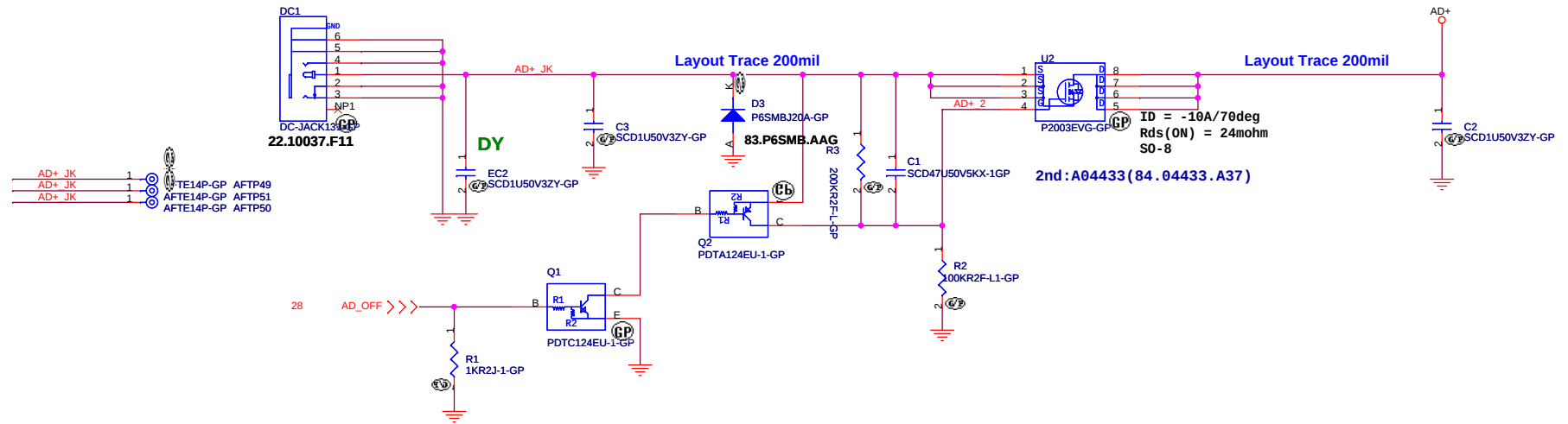


Aux Power 3D3V_AUX_S5

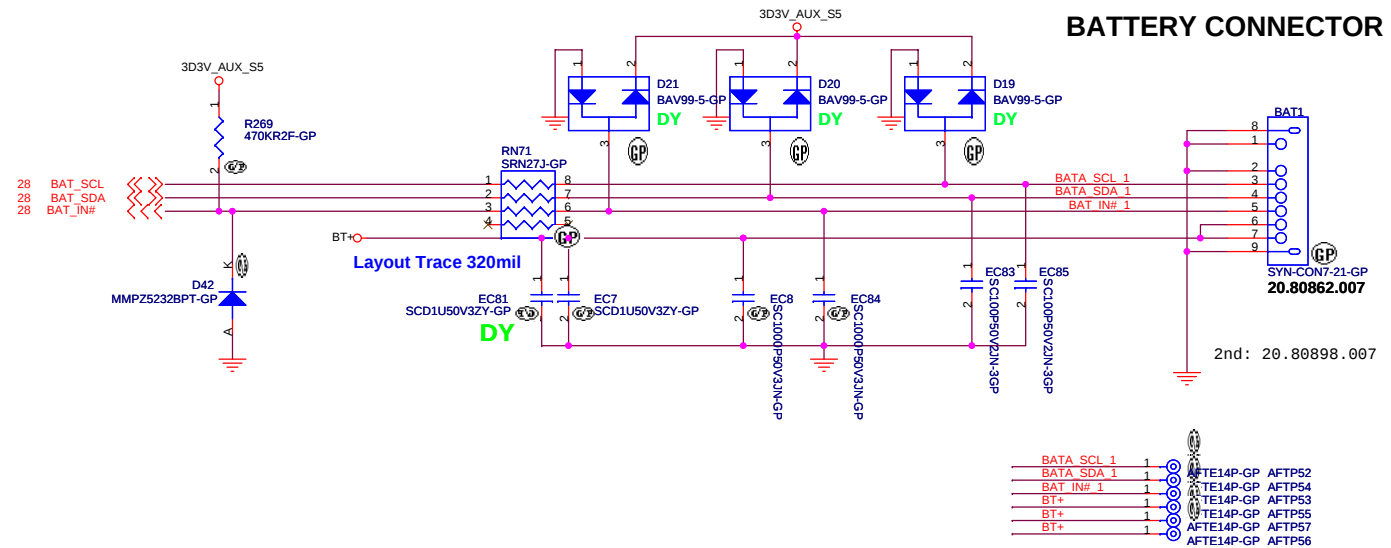


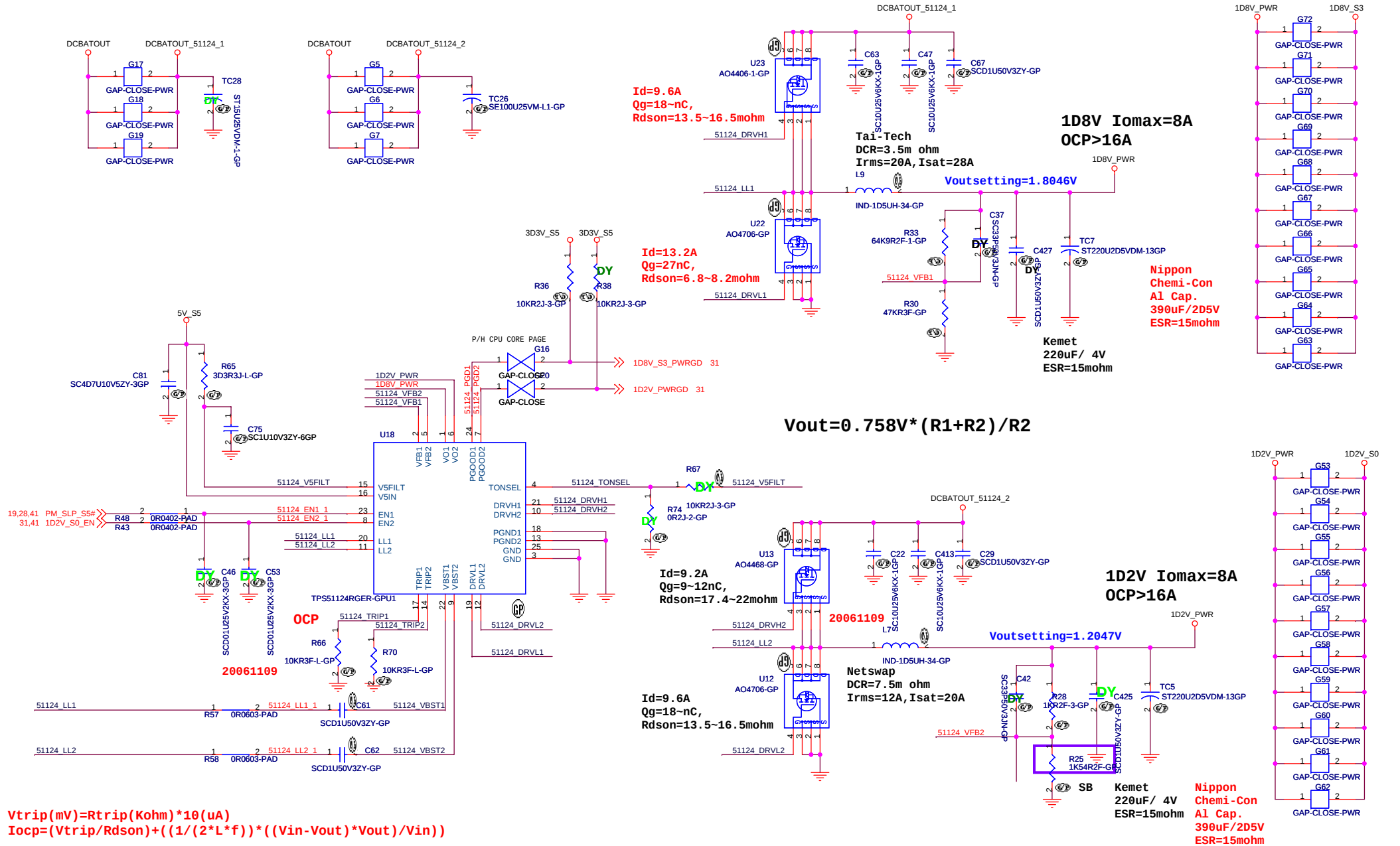


Adaptor in to generate DCBATOUT



BATTERY CONNECTOR





	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

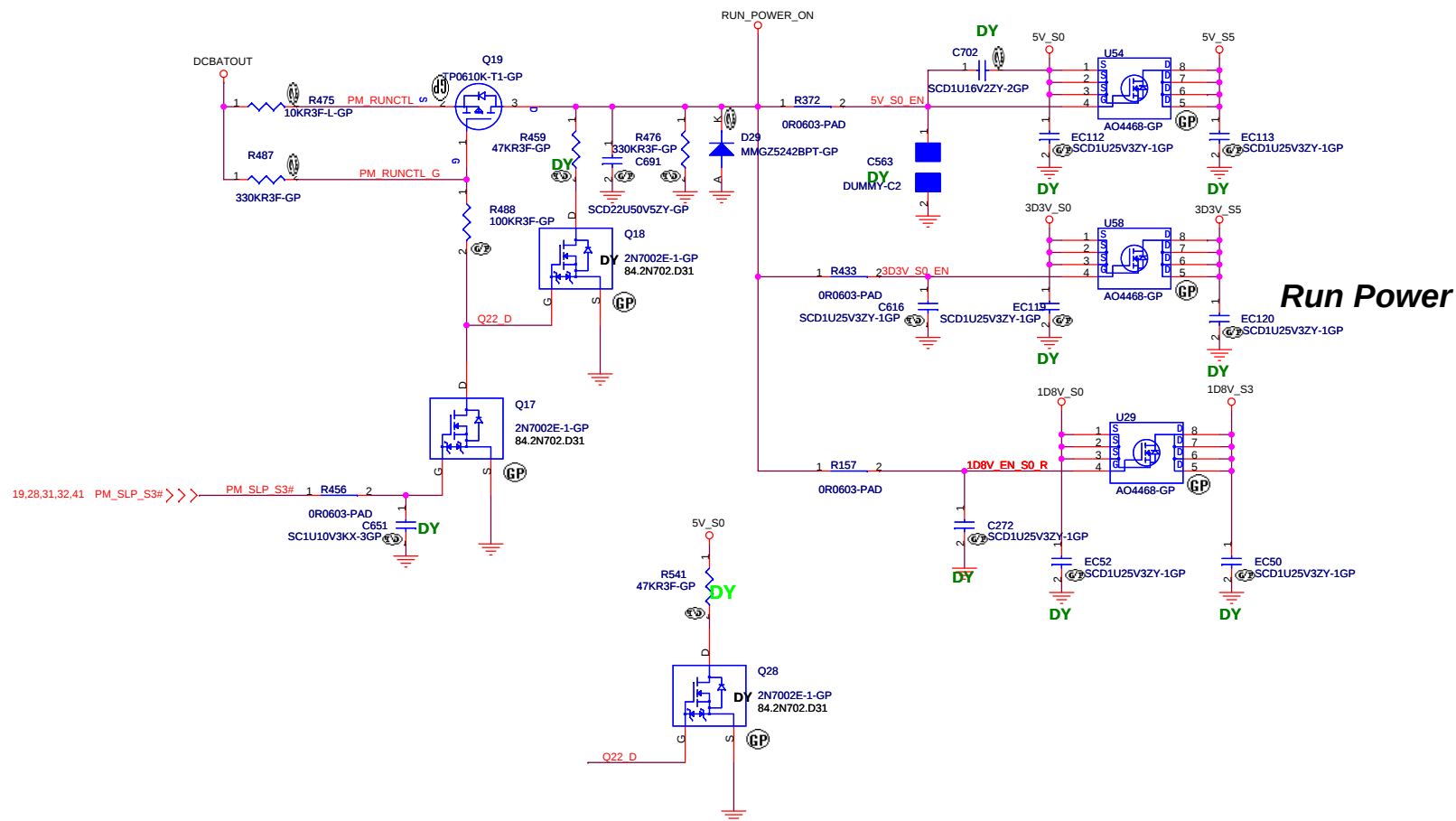
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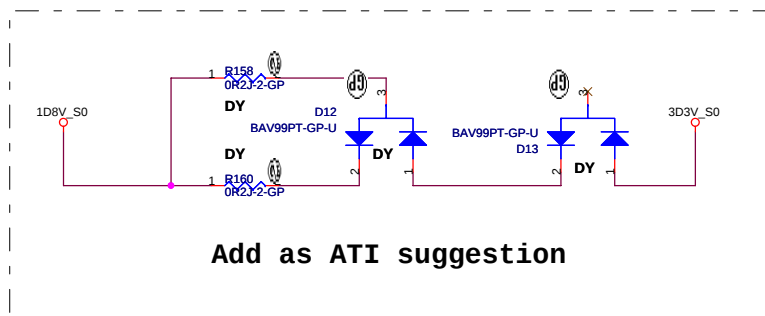
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Size: A3 Document Number: **Yukon** Rev: **-1**

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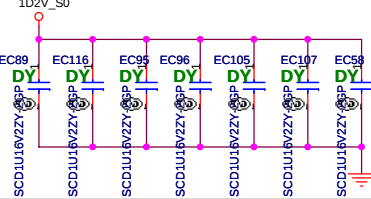
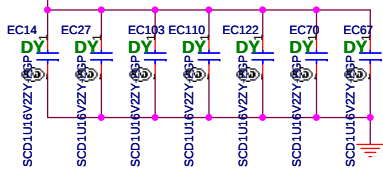
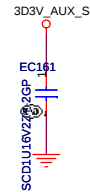
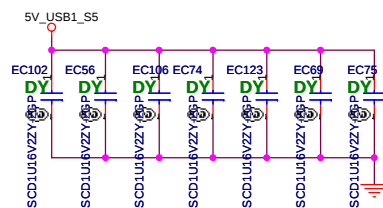
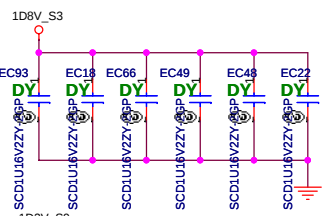
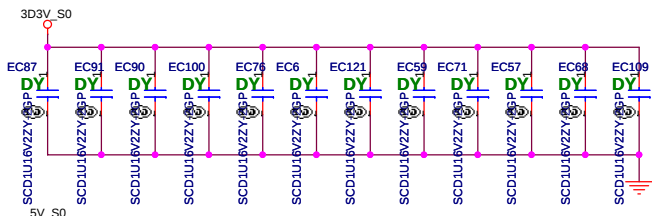
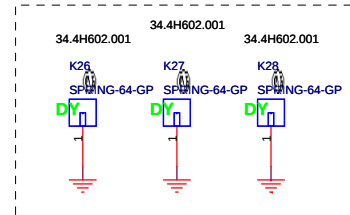
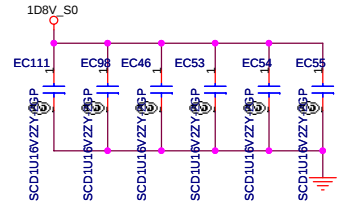
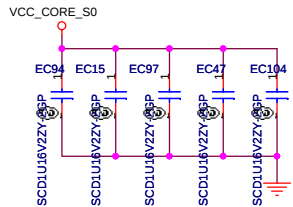
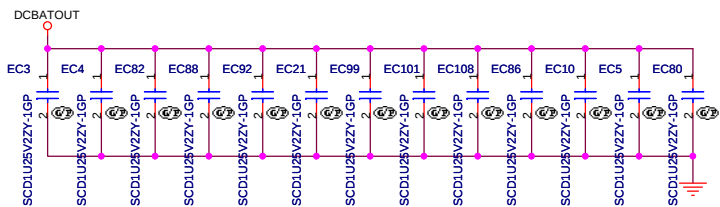
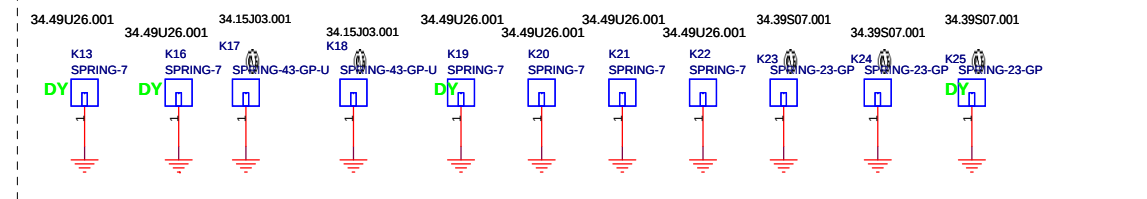
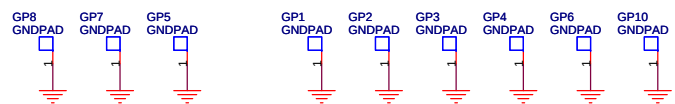
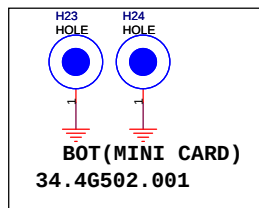
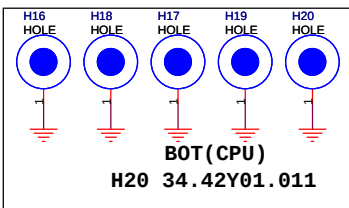
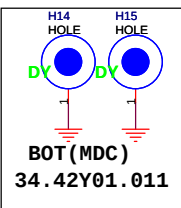
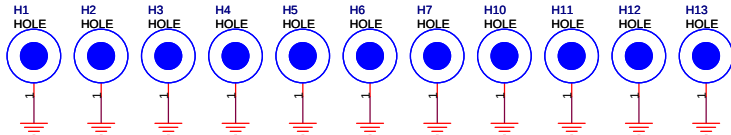
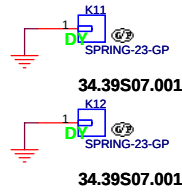
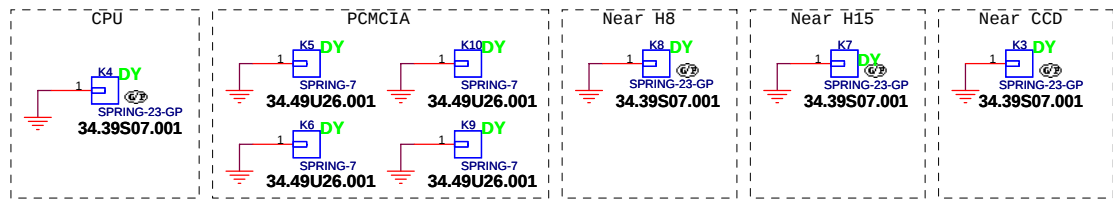
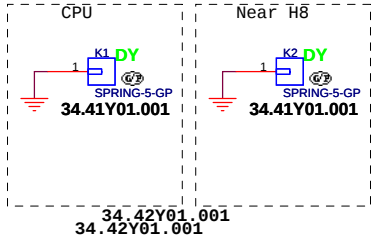
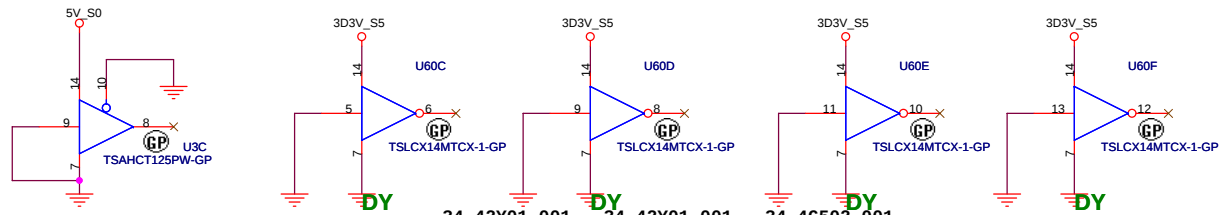
Run Power



Power On Logic

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Title			
RUB POWER			
Size A3	Document Number		Rev -1
Yukon			
Date: Wednesday, August 06, 2008		Sheet 42 of	43



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Title		Rev
EMI/Spring/Boss		
Size	Document Number	-1
Yukon		
Date	Tuesday, August 19, 2008	
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