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HSF Property:ROHS or Halogen-Free(5L3?)

DAKAR10F/FG/R/RG

2011.10.28

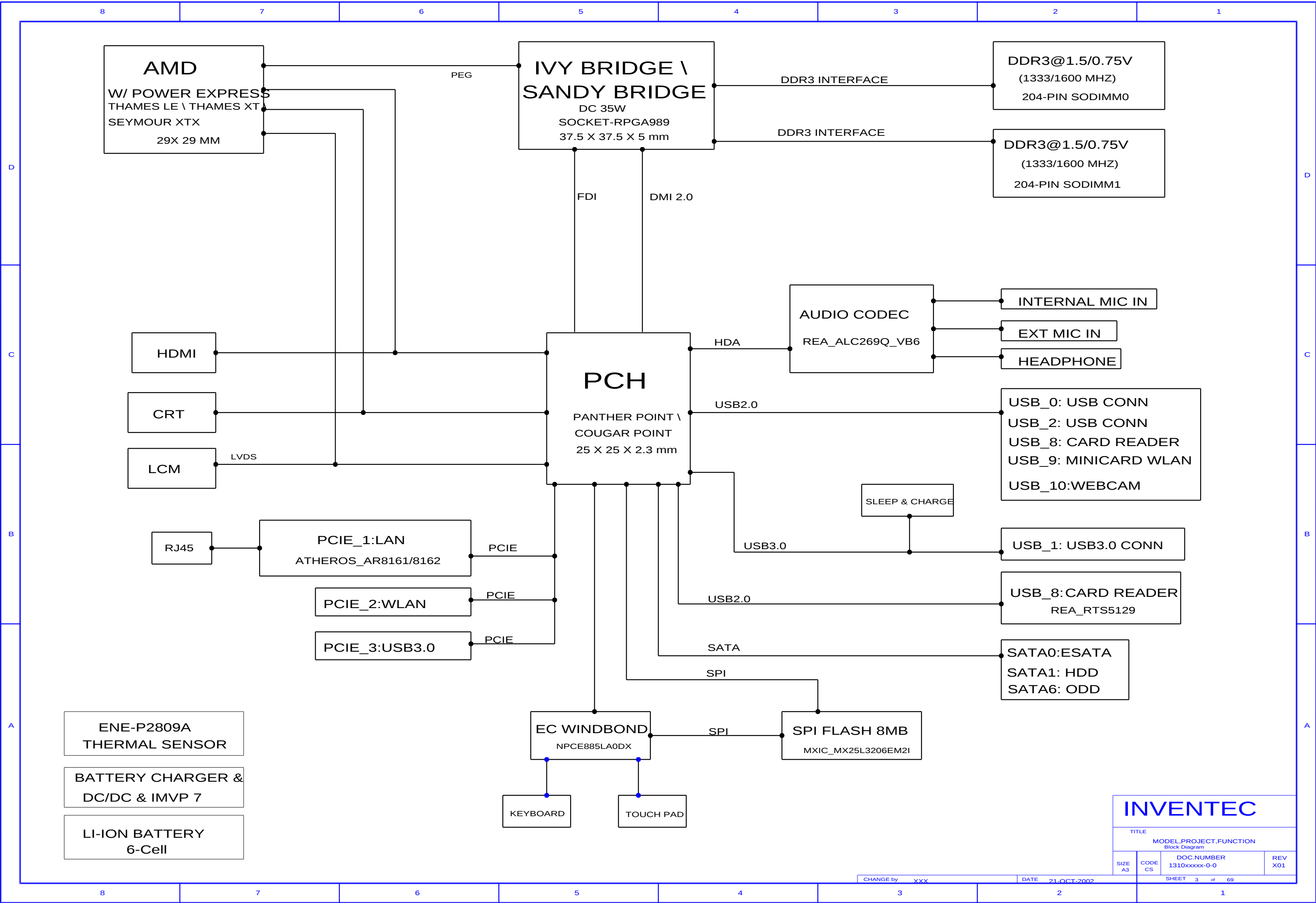
21-OCT-2002		
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	INVENTEC TITLE MODEL,PROJECT,FUNCTION Everest Main Board			
DRAWER								
DESIGN								
CHECK								
RESPONSIBLE								
SIZE#					SIZE			
FILE NAME:			VER:	CODE	DOC NUMBER			
P/N	xxx				C	CS	1310xxxxx-0-0	REV
					X01			
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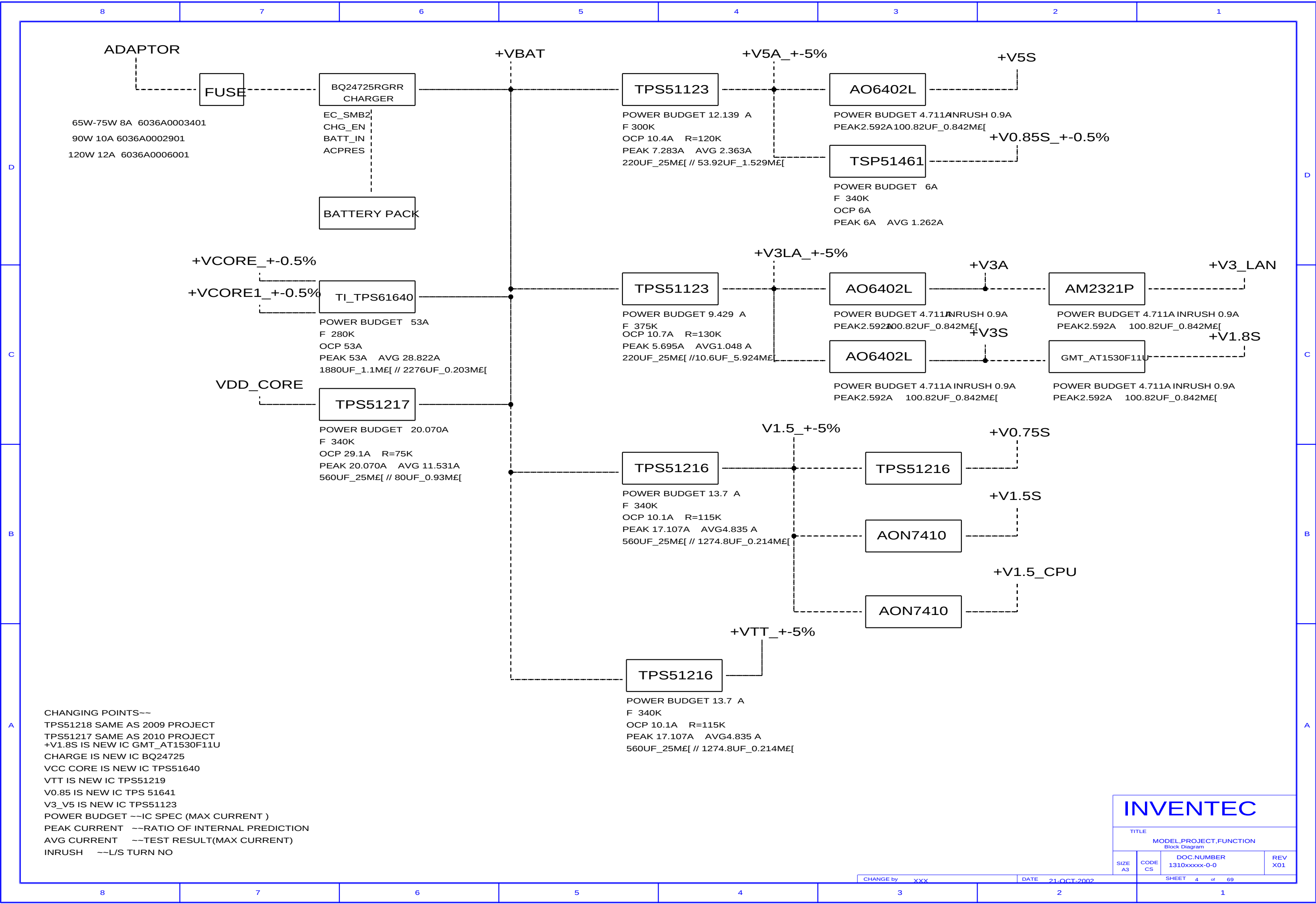
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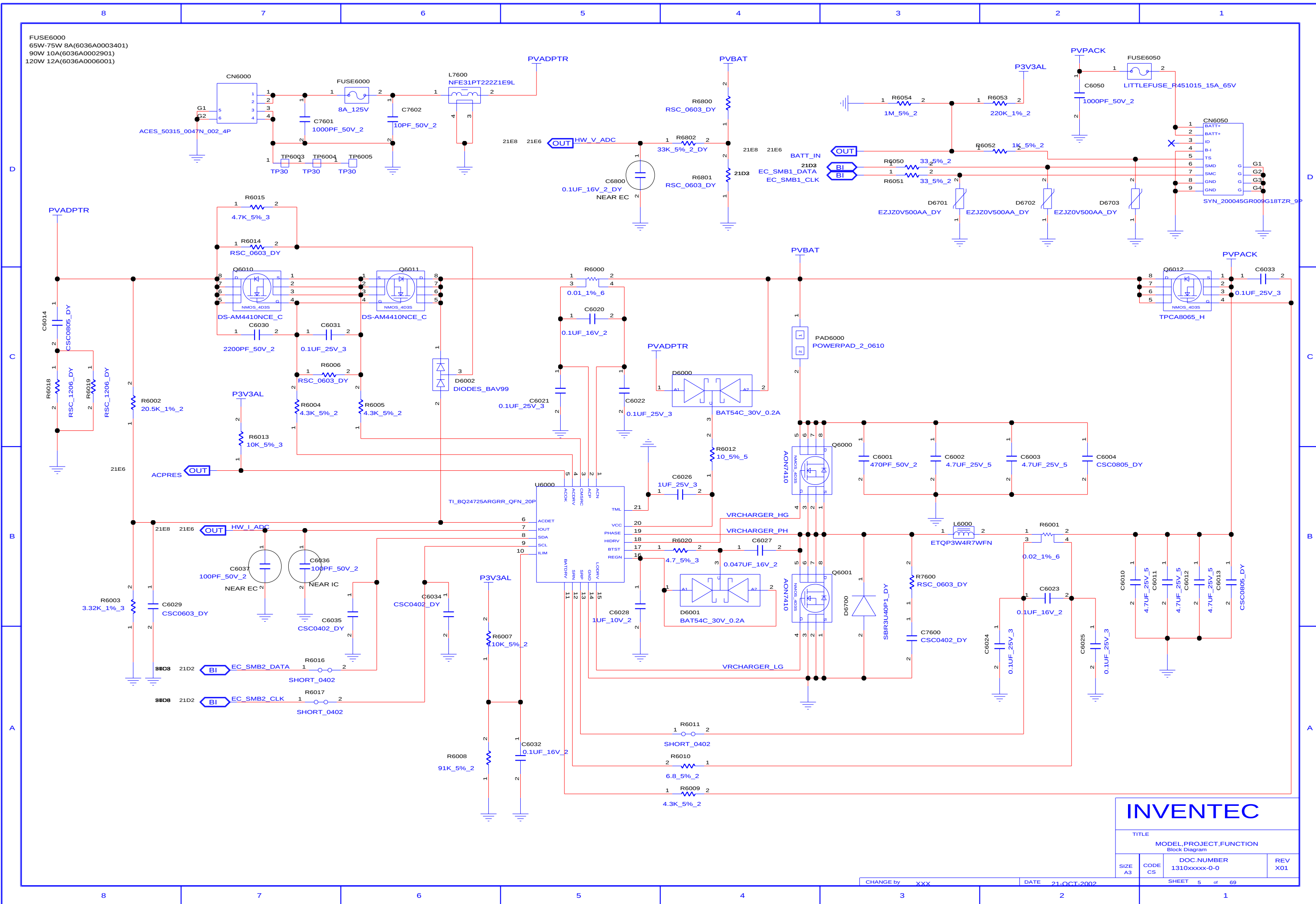


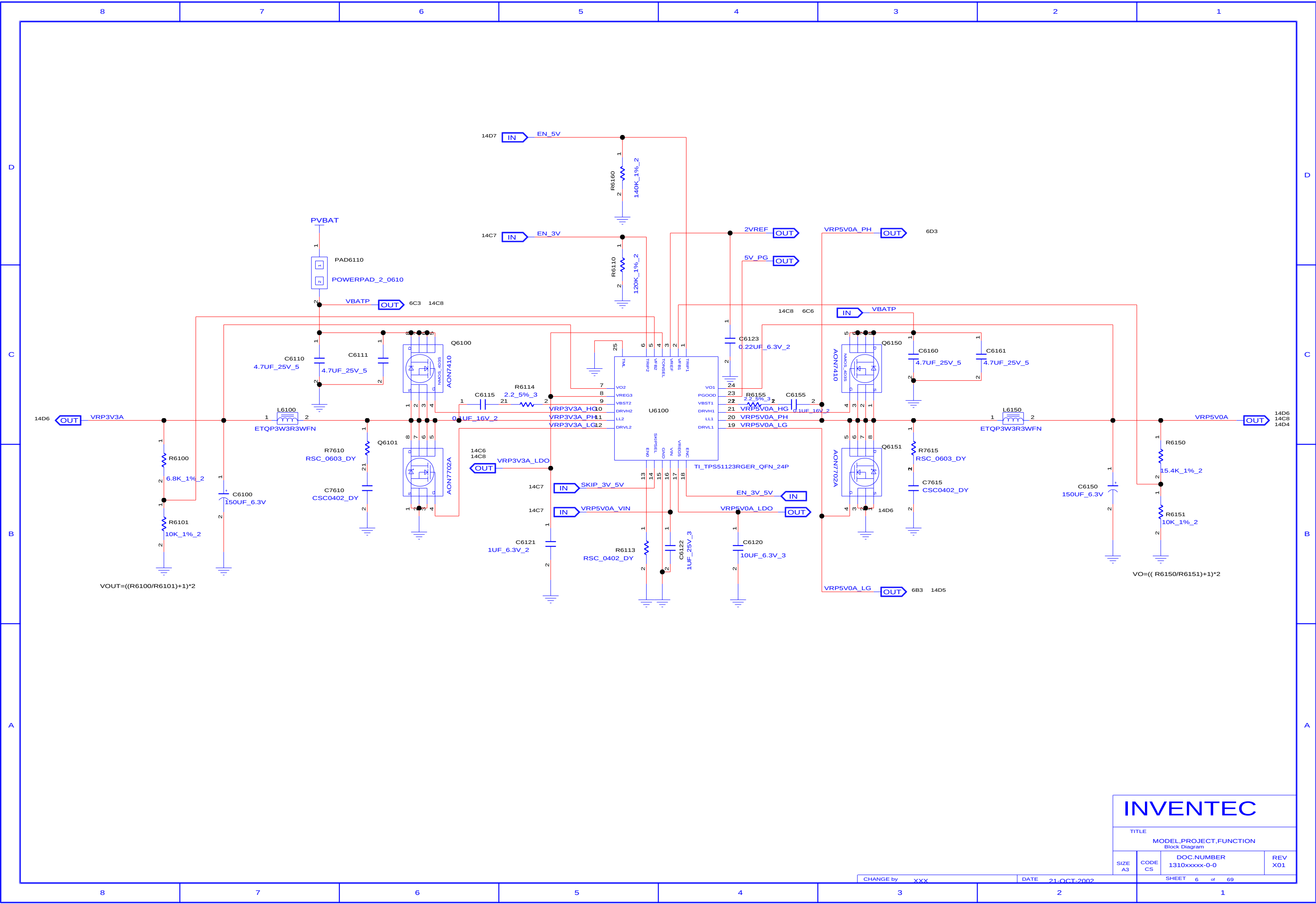
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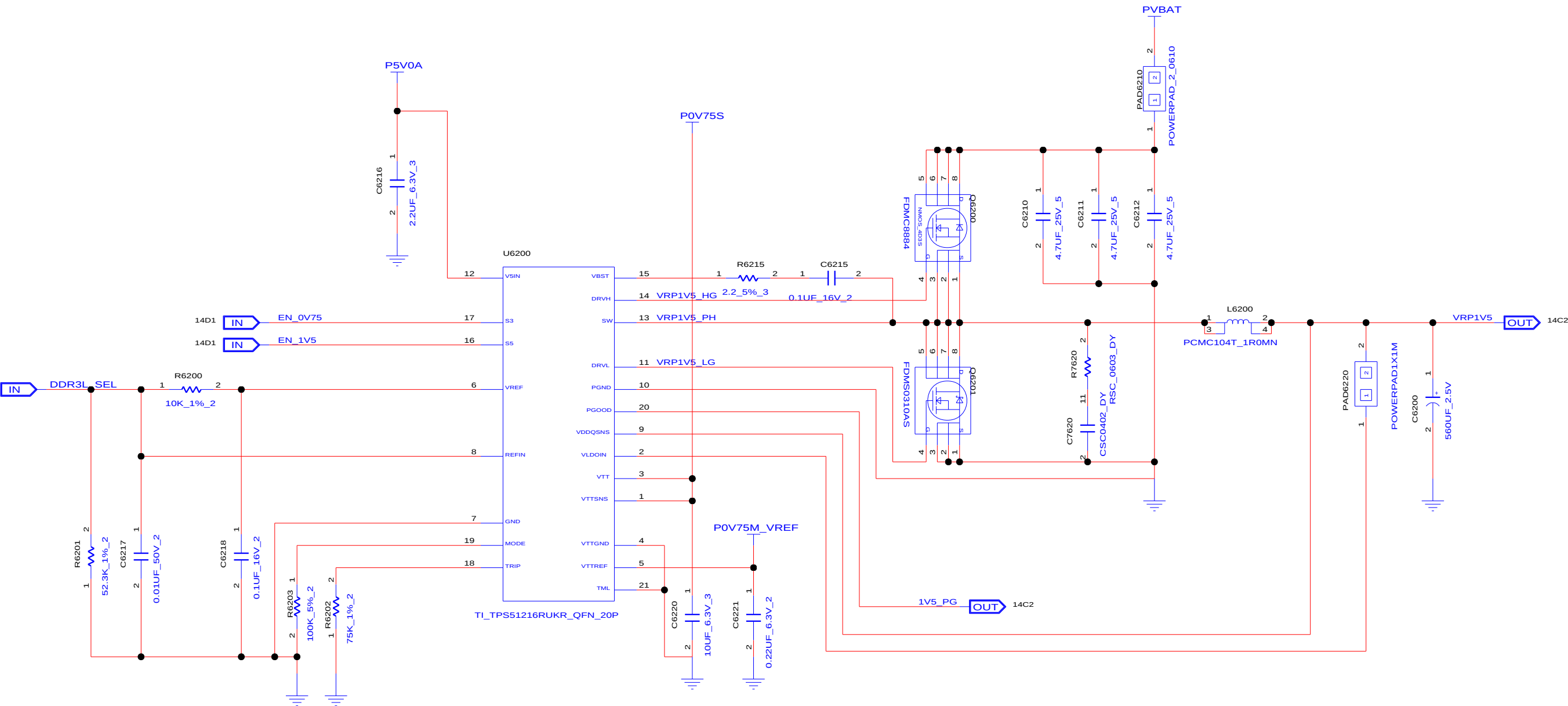
CHANGING POINTS~~
TPS51218 SAME AS 2009 PROJECT
TPS51217 SAME AS 2010 PROJECT
+V1.8S IS NEW IC GMT_AT1530F11U
CHARGE IS NEW IC BQ24725
VCC CORE IS NEW IC TPS51640
VTT IS NEW IC TPS51219
V0.85 IS NEW IC TPS 51641
V3_V5 IS NEW IC TPS51123
POWER BUDGET ~~IC SPEC (MAX CURRENT)
PEAK CURRENT ~~RATIO OF INTERNAL PREDICTION
AVG CURRENT ~~TEST RESULT(MAX CURRENT)
INRUSH ~~L/S TURN NO

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$$VOUT=REFIN=1.8*(R6201/(R6200+R6201))$$

MODE=100KOHM:TRACKING DISCHARGE

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

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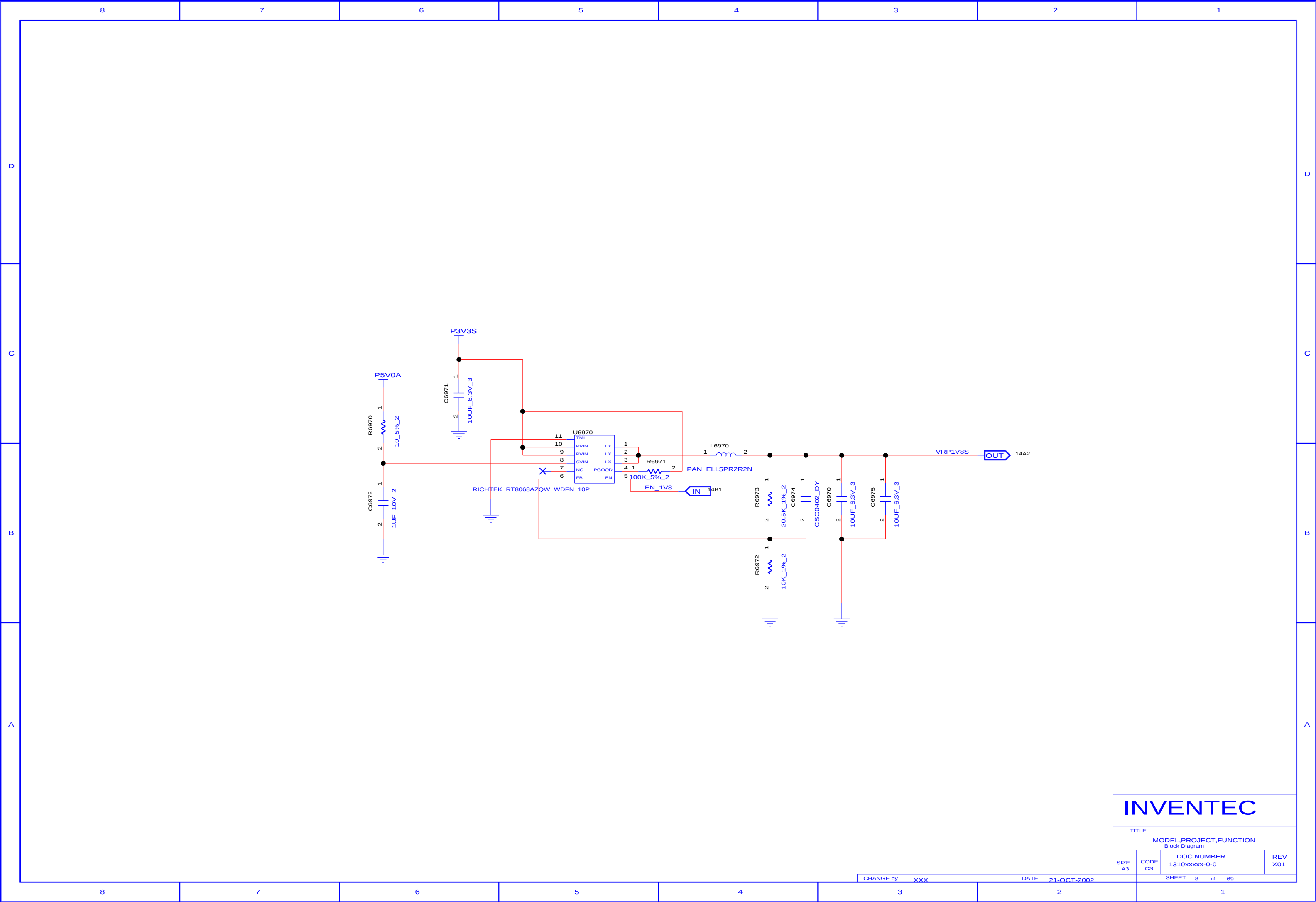
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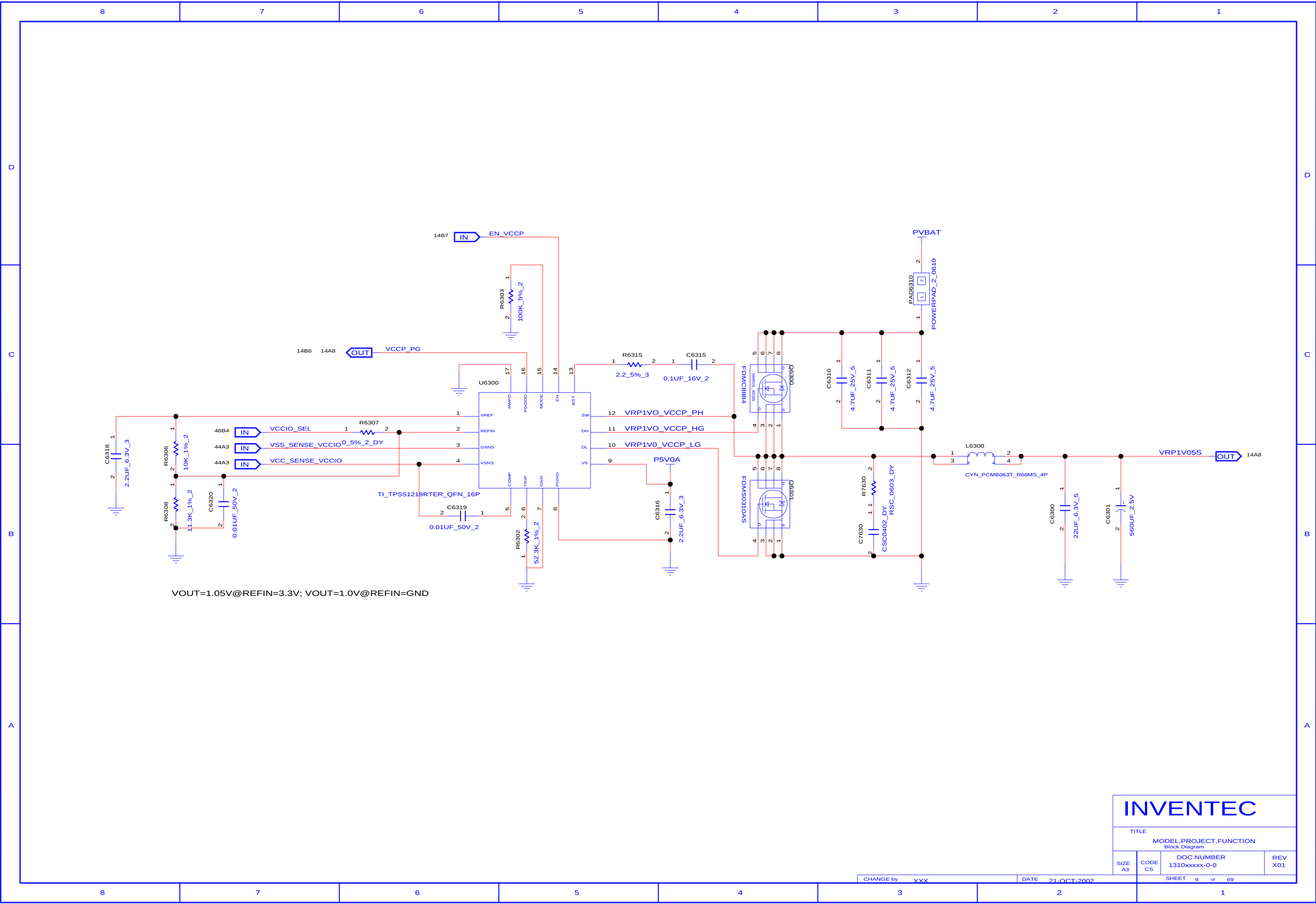
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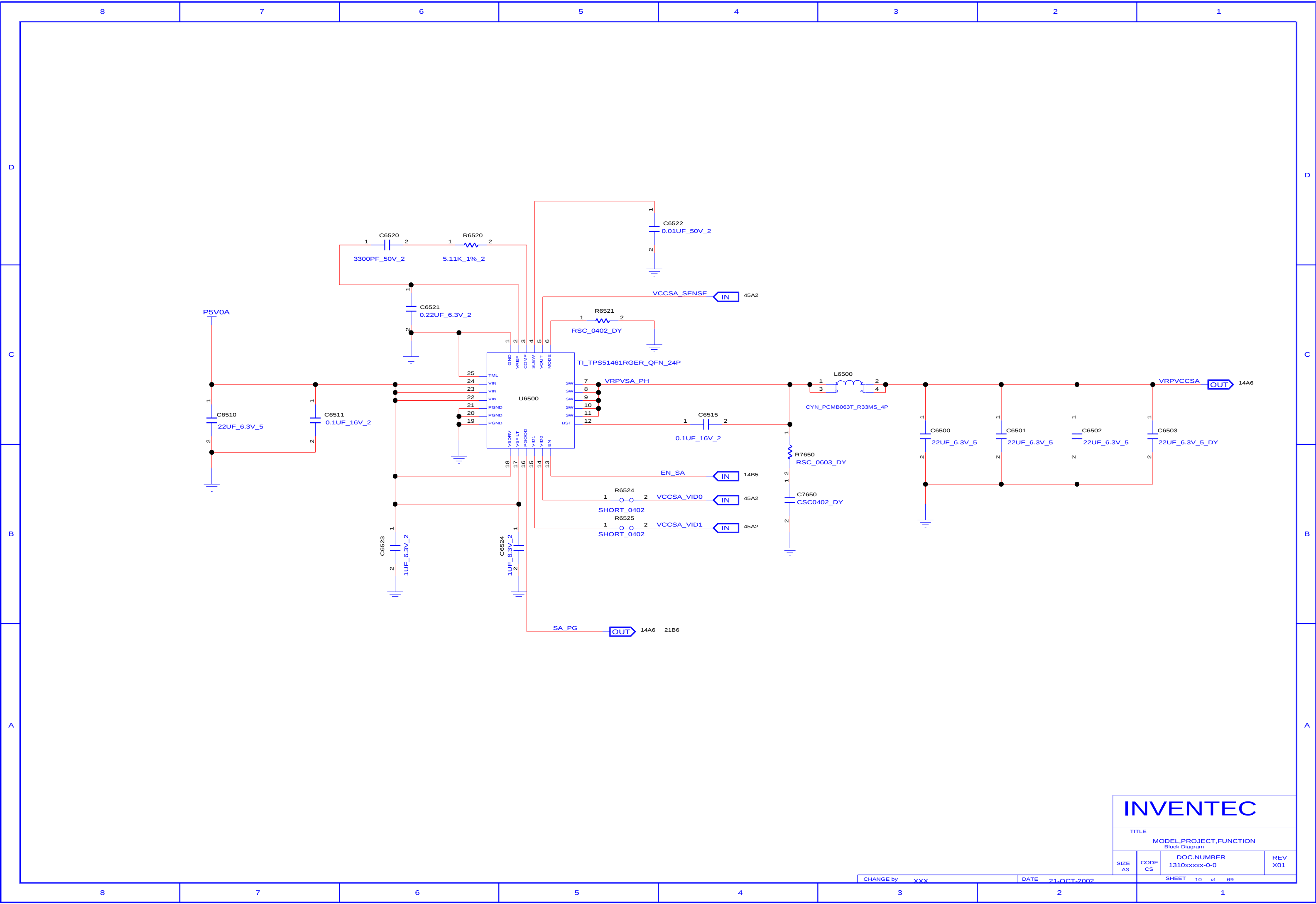




VOUT=1.05V@REFIN=3.3V; VOUT=1.0V@REFIN=GND

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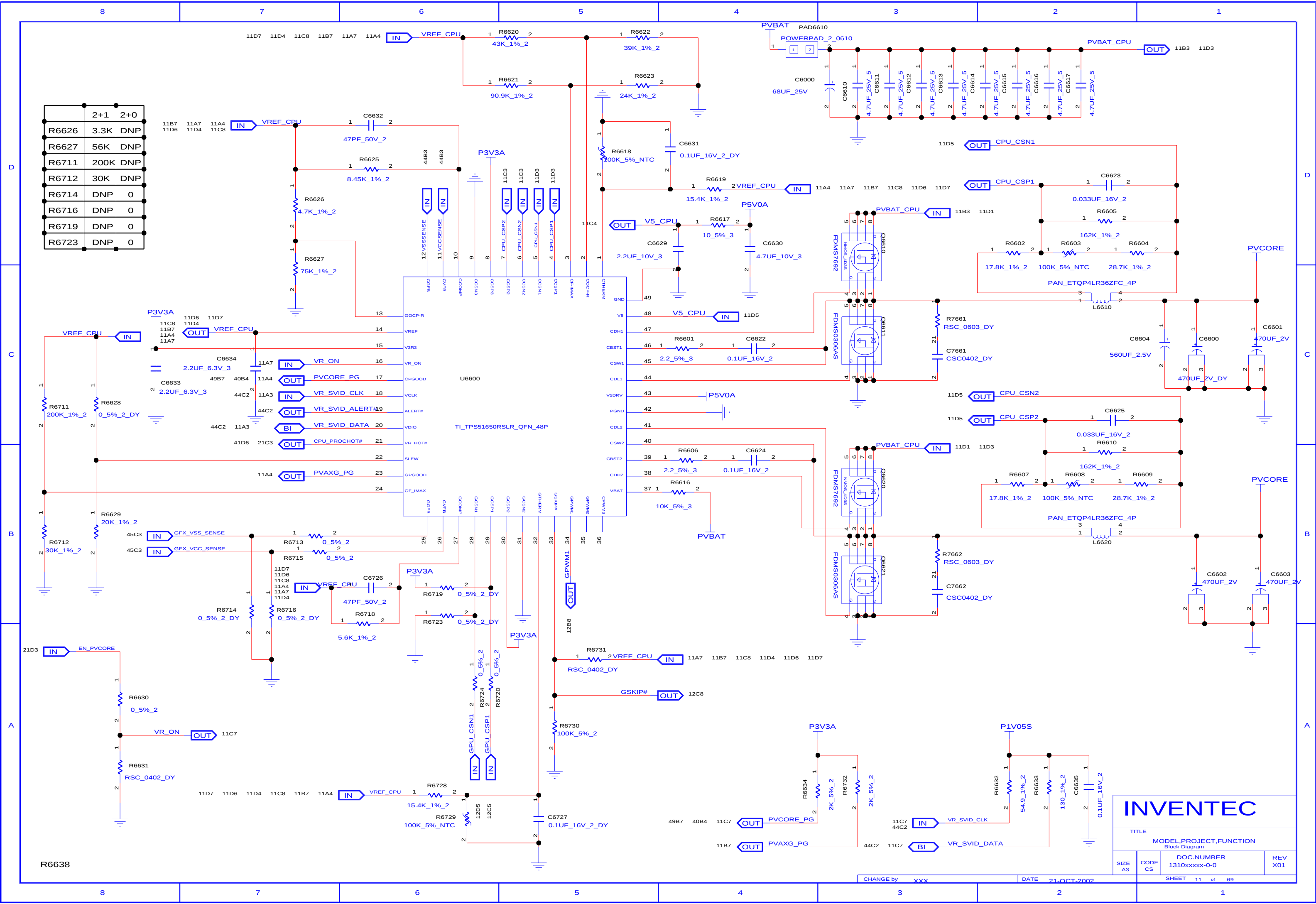
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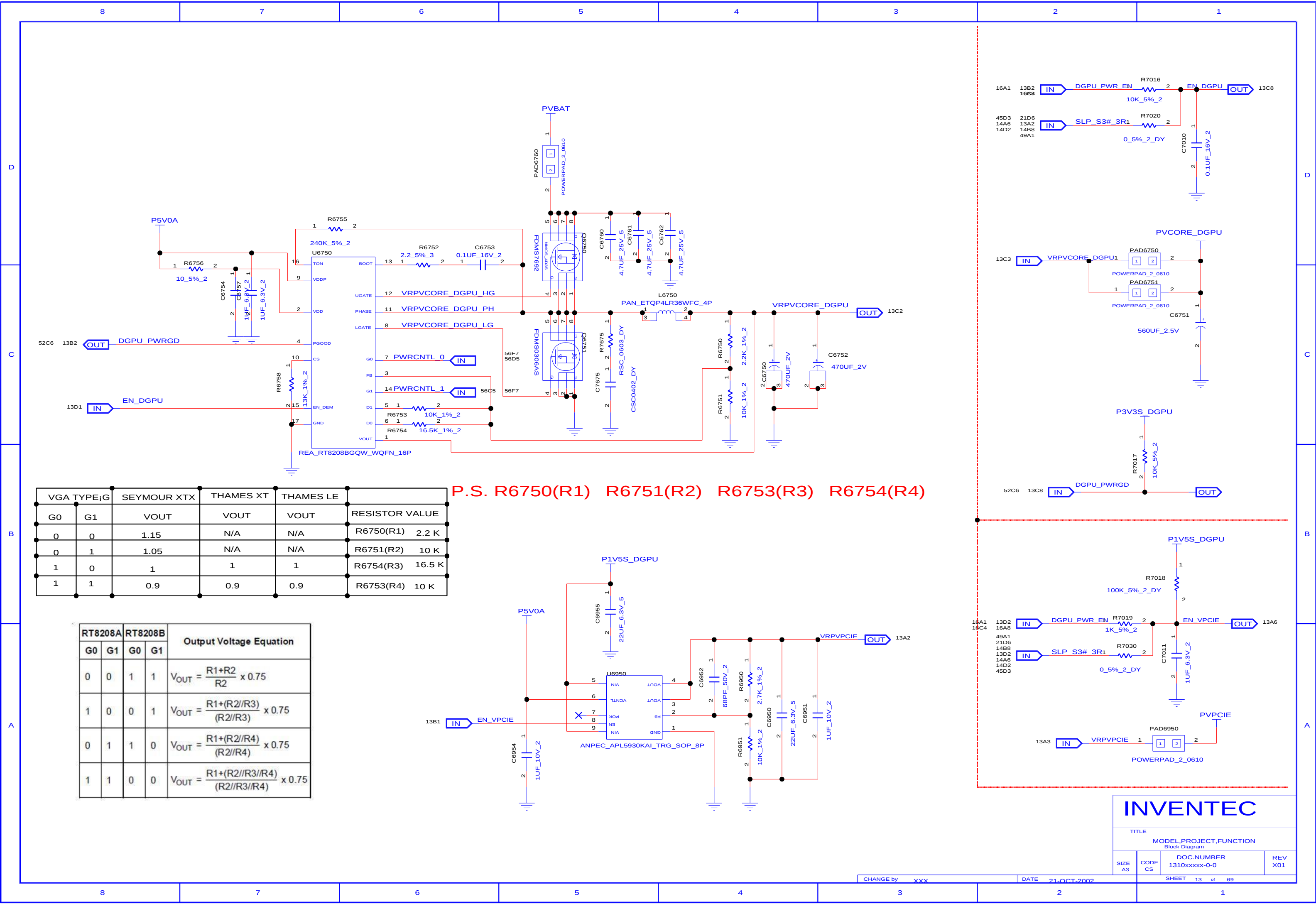
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	2+1	2+0
R6626	3.3K	DNP
R6627	56K	DNP
R6711	200K	DNP
R6712	30K	DNP
R6714	DNP	0
R6716	DNP	0
R6719	DNP	0
R6723	DNP	0



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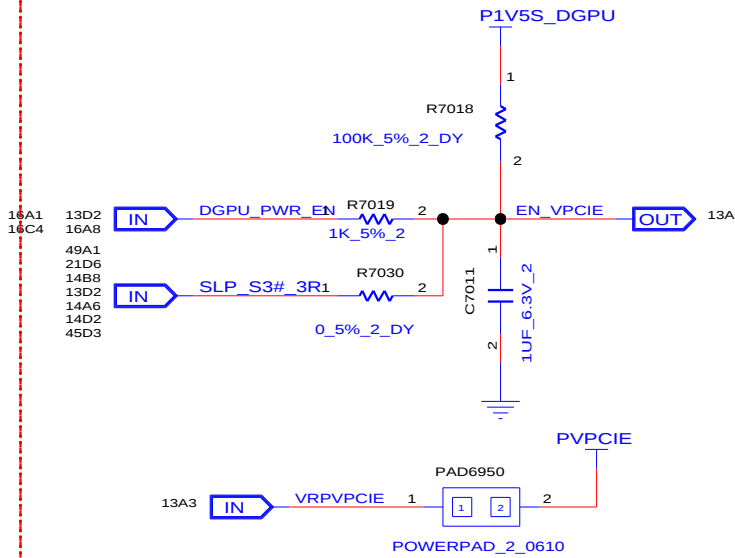
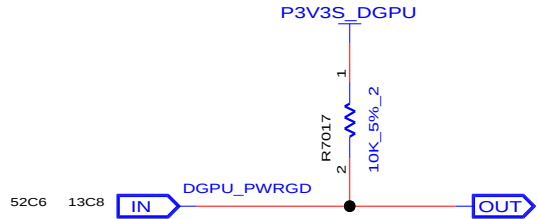
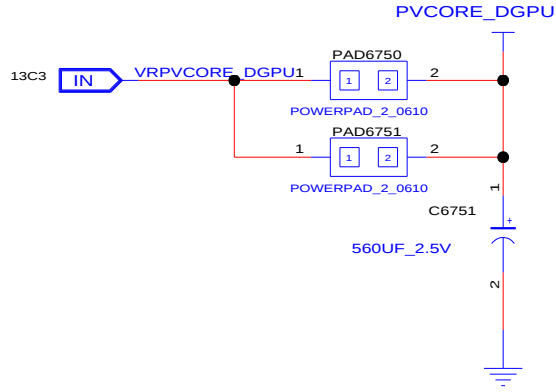
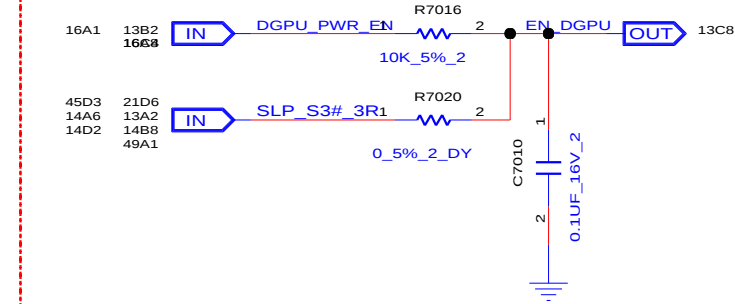
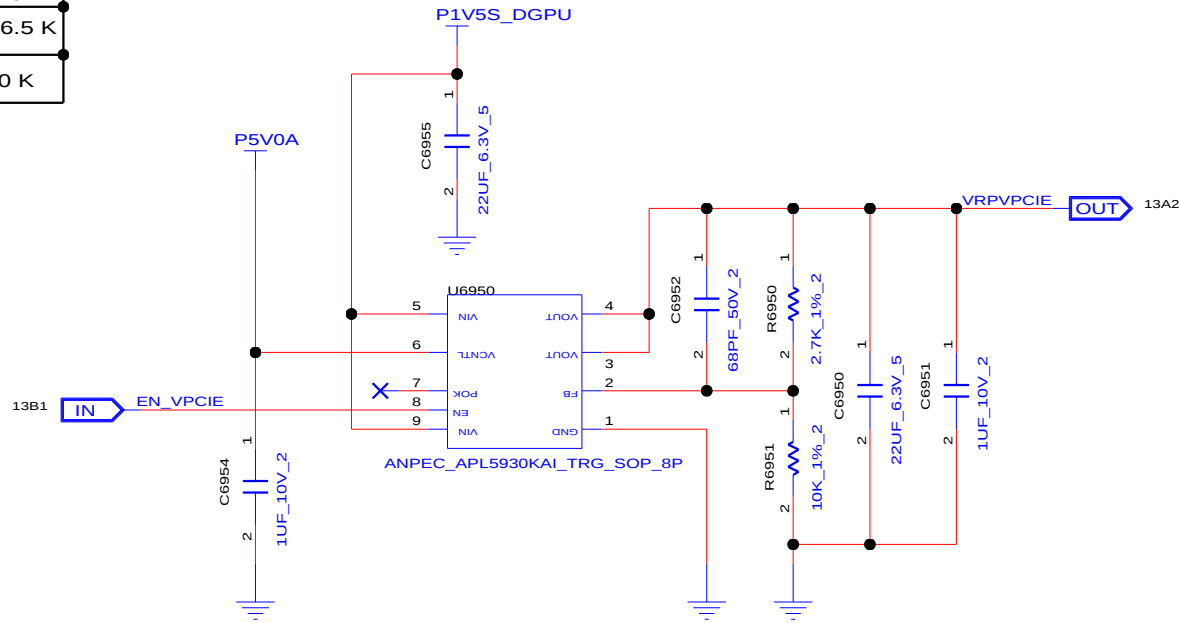
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VGA TYPEiG		SEYMOUR XTX	THAMES XT	THAMES LE		
G0	G1	VOUT	VOUT	VOUT	RESISTOR VALUE	
0	0	1.15	N/A	N/A	R6750(R1)	2.2 K
0	1	1.05	N/A	N/A	R6751(R2)	10 K
1	0	1	1	1	R6754(R3)	16.5 K
1	1	0.9	0.9	0.9	R6753(R4)	10 K

P.S. R6750(R1) R6751(R2) R6753(R3) R6754(R4)

RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$



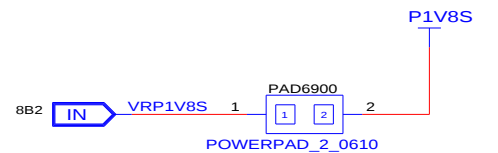
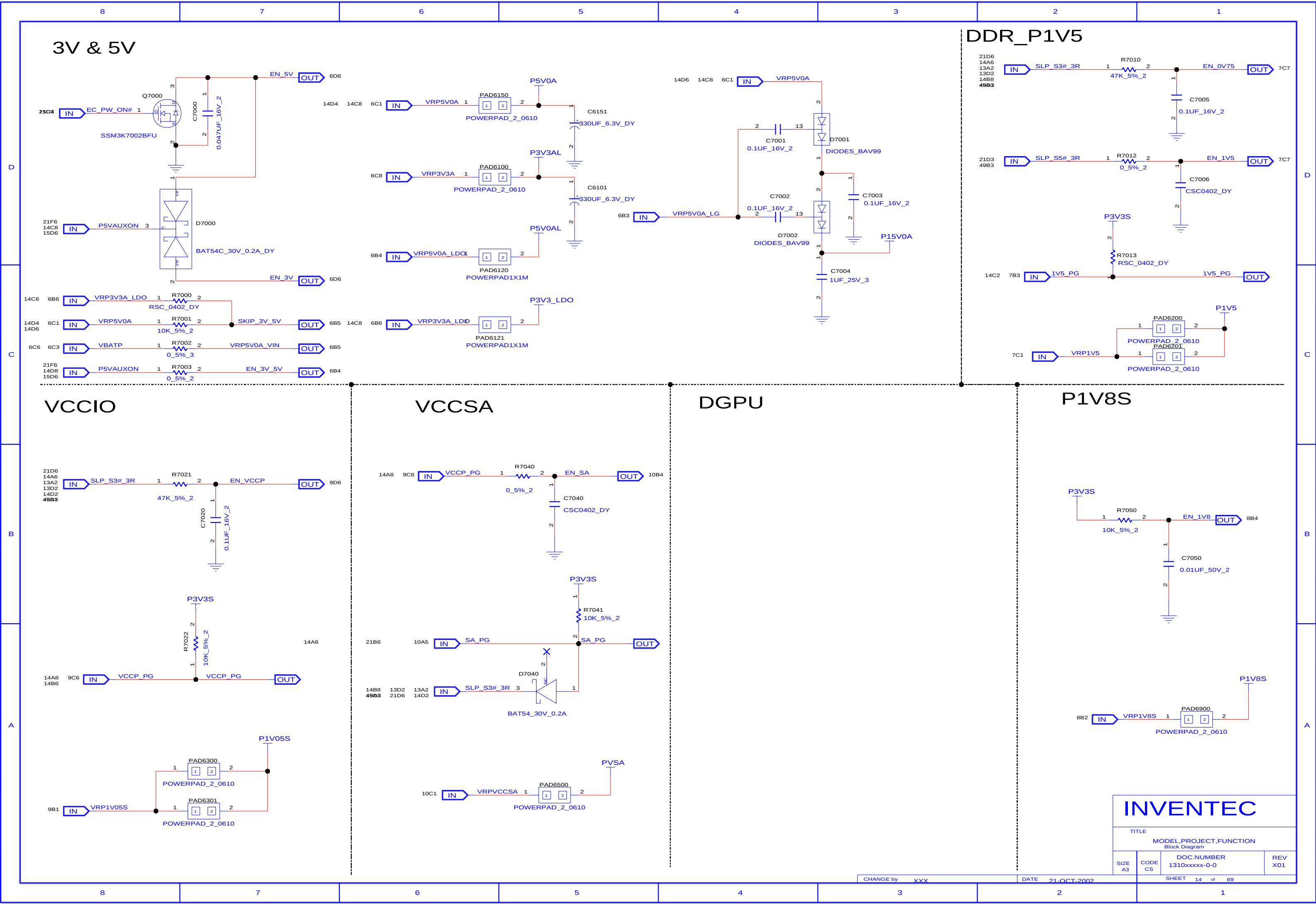
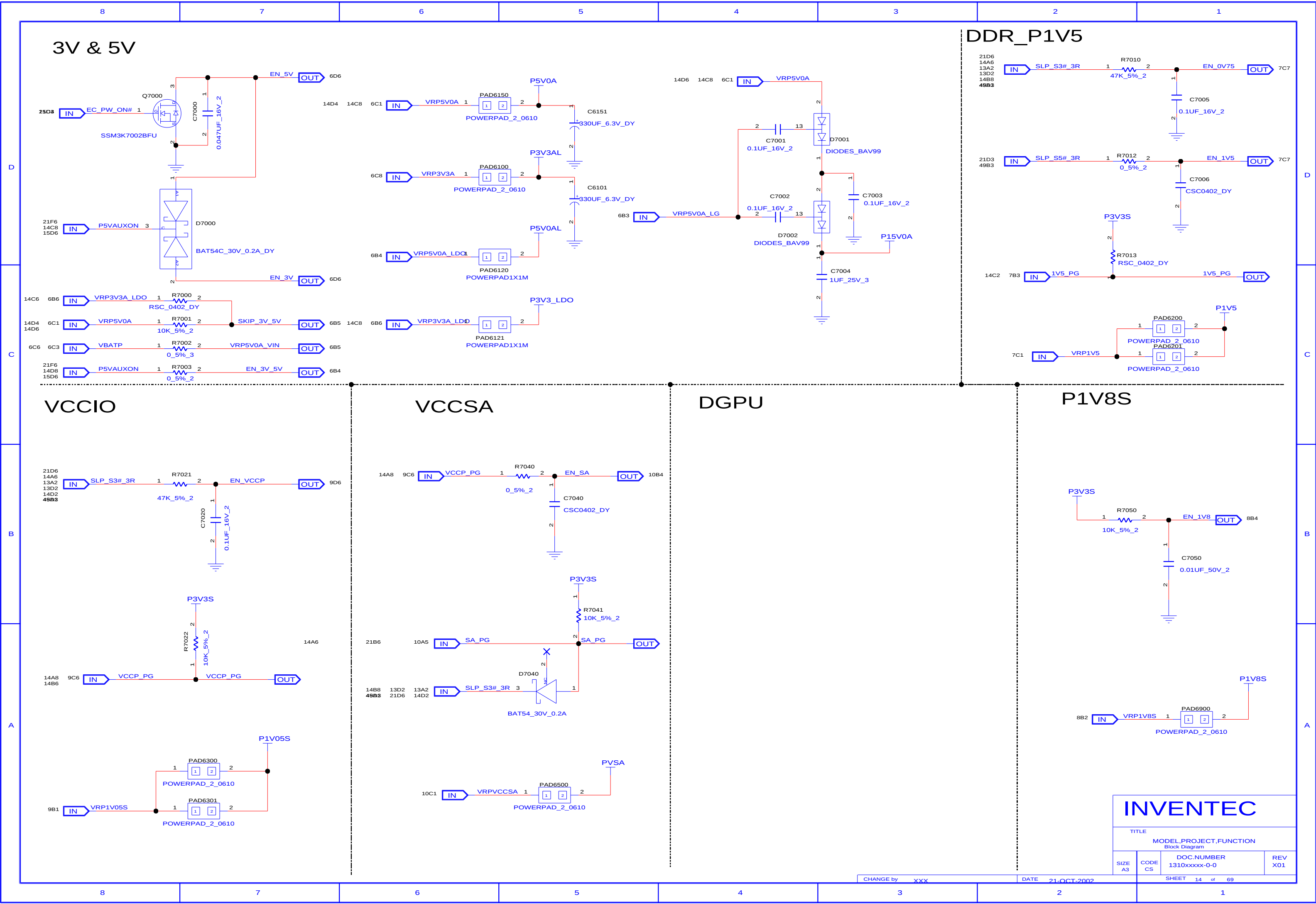
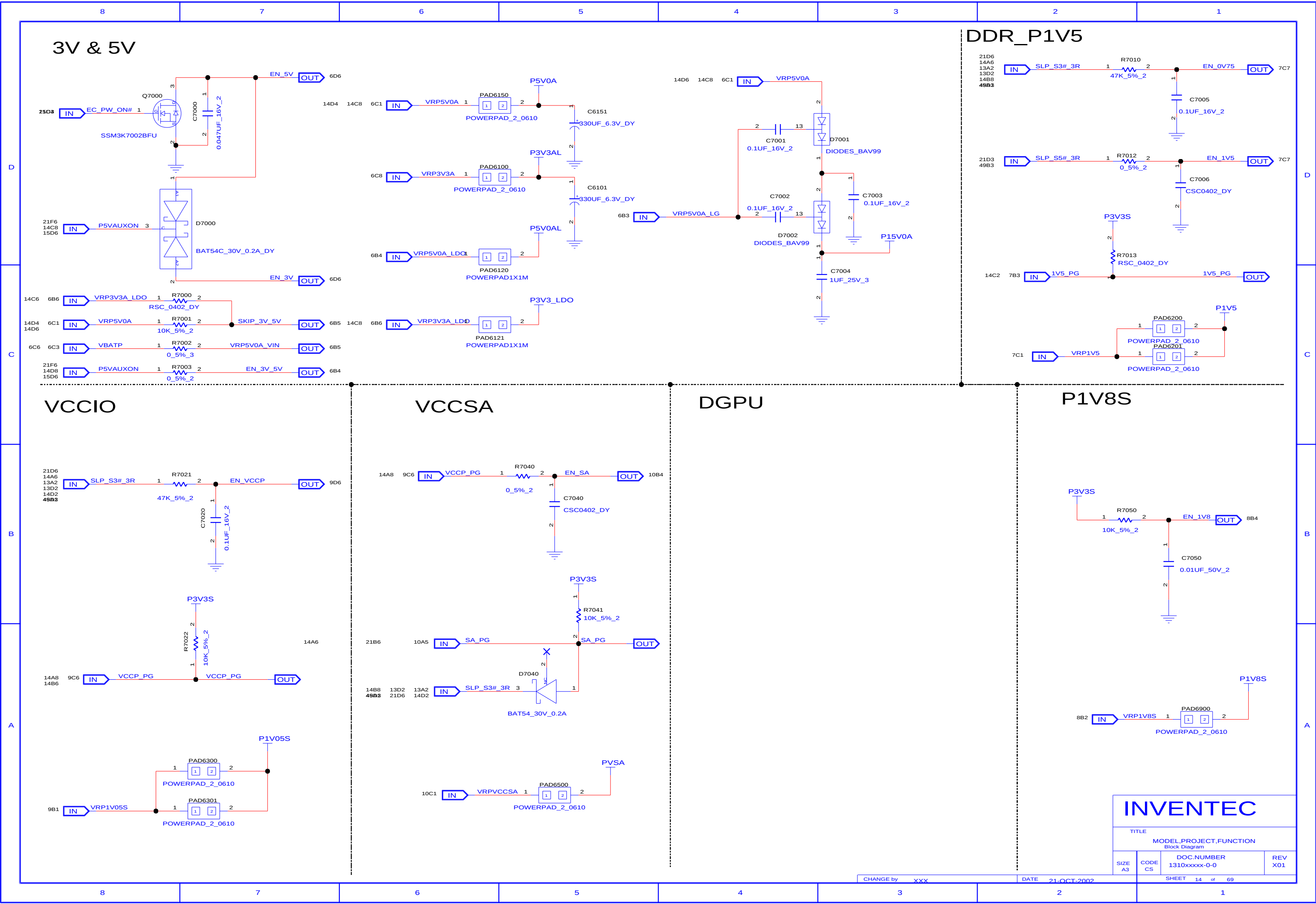
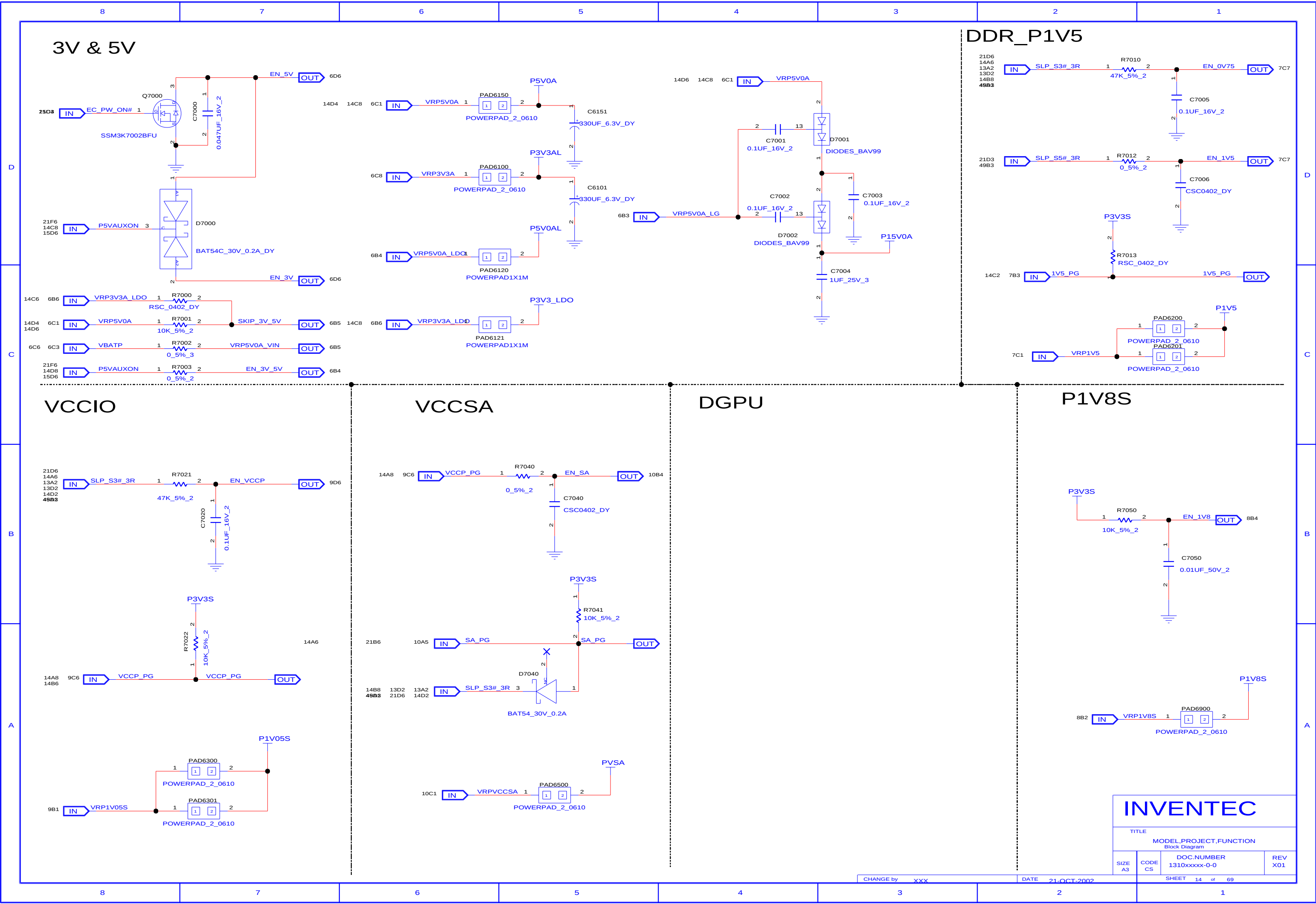
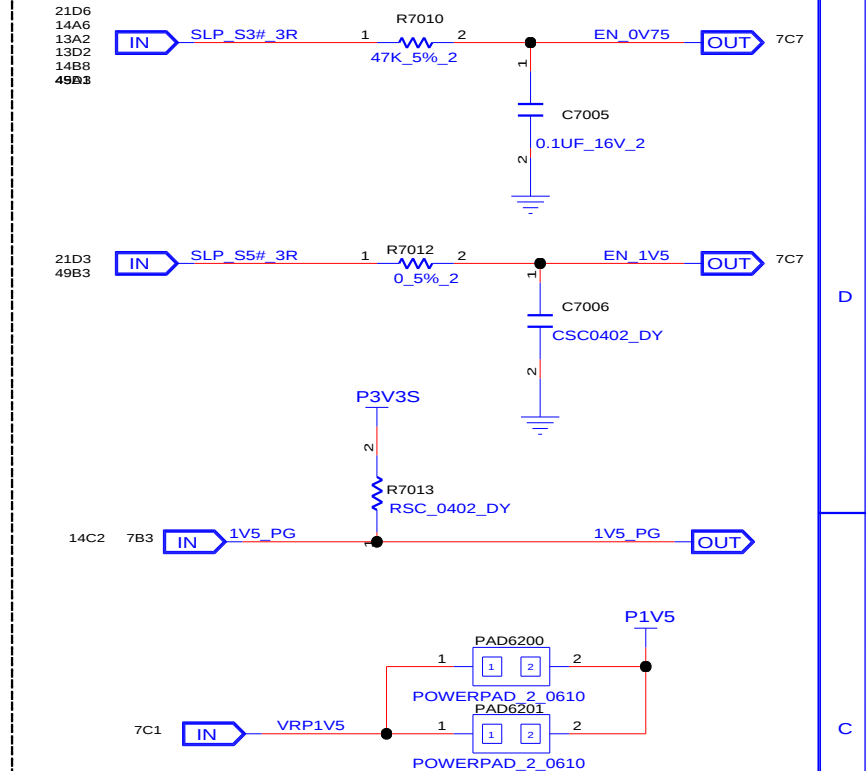
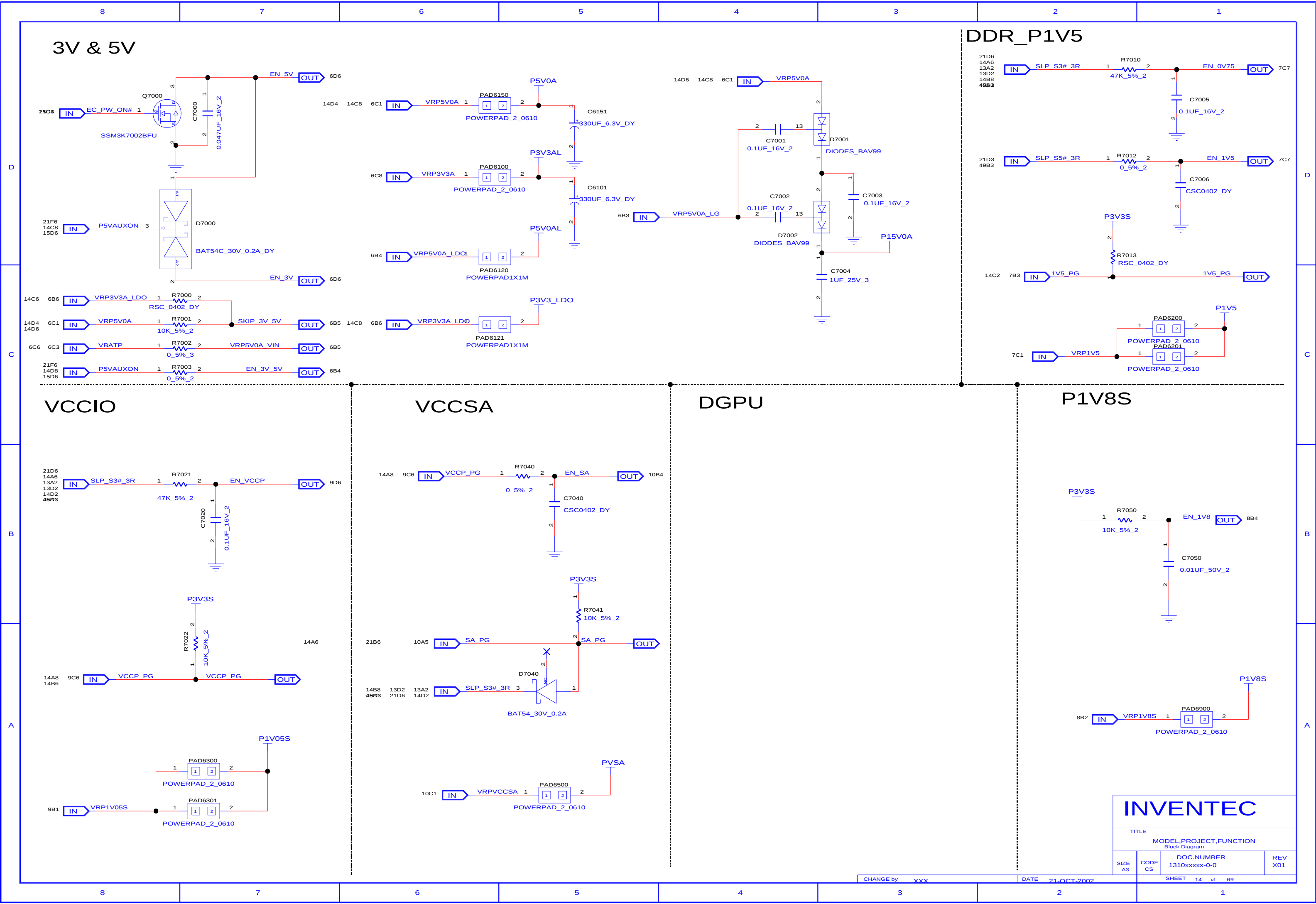
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TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

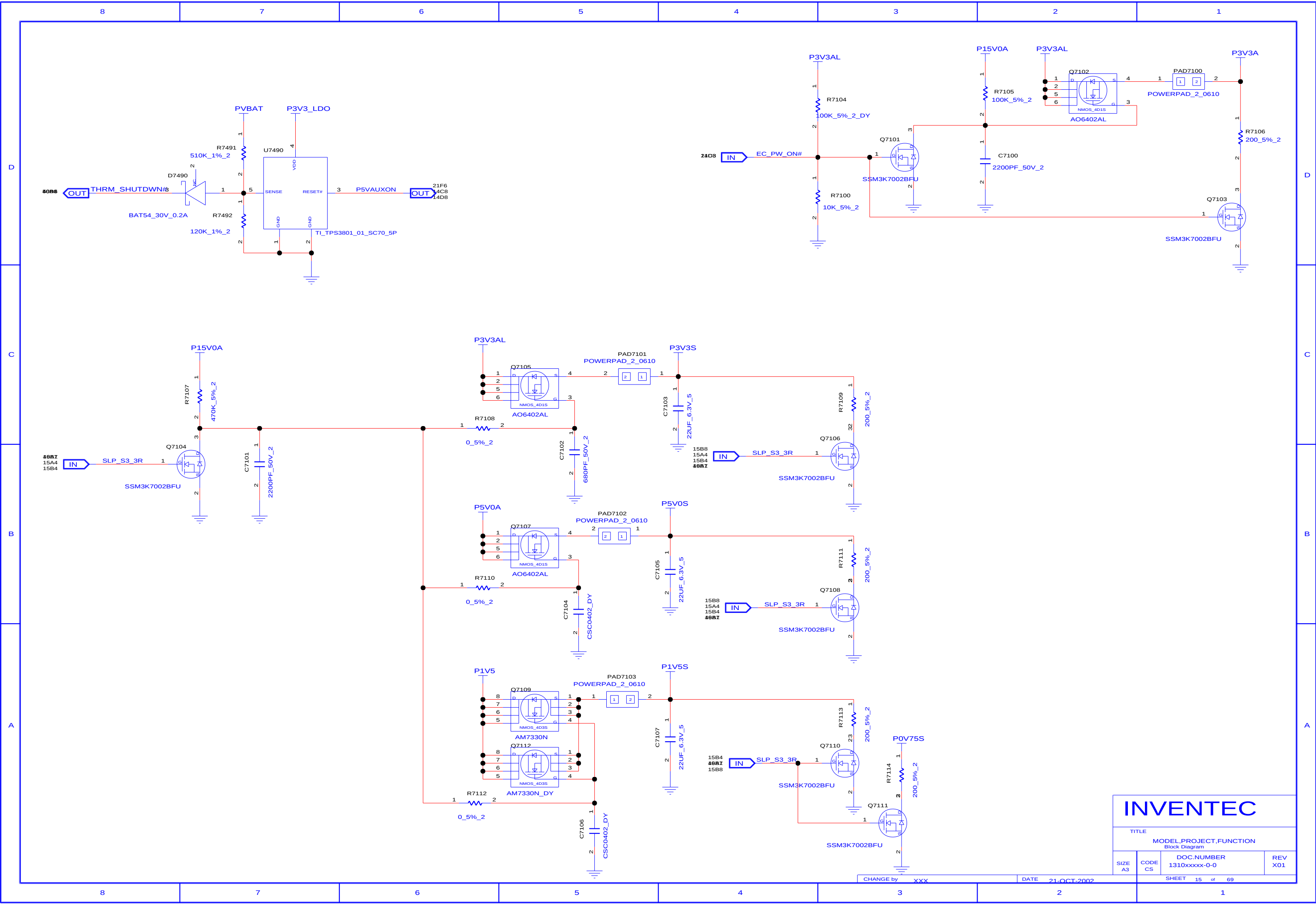
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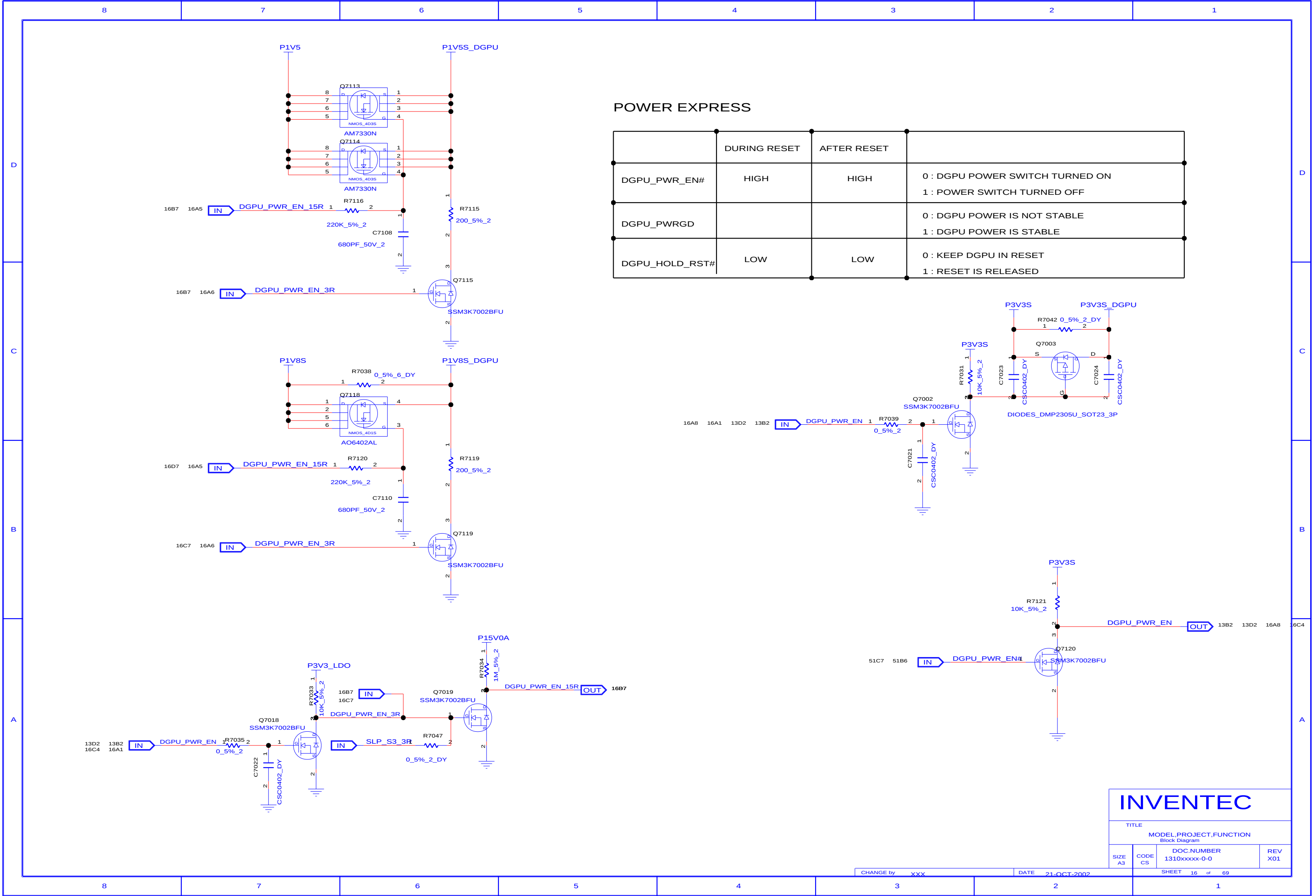
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POWER EXPRESS

	DURING RESET	AFTER RESET	
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PWRGD			0 : DGPU POWER IS NOT STABLE 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED

INVENTEC

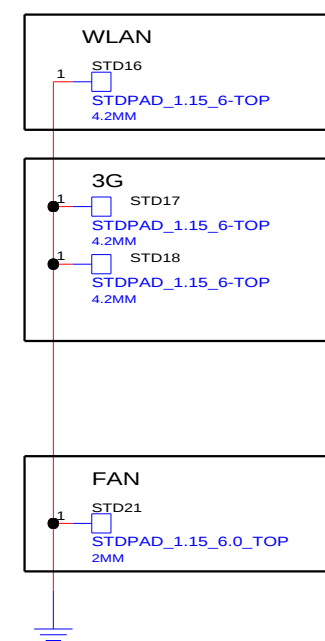
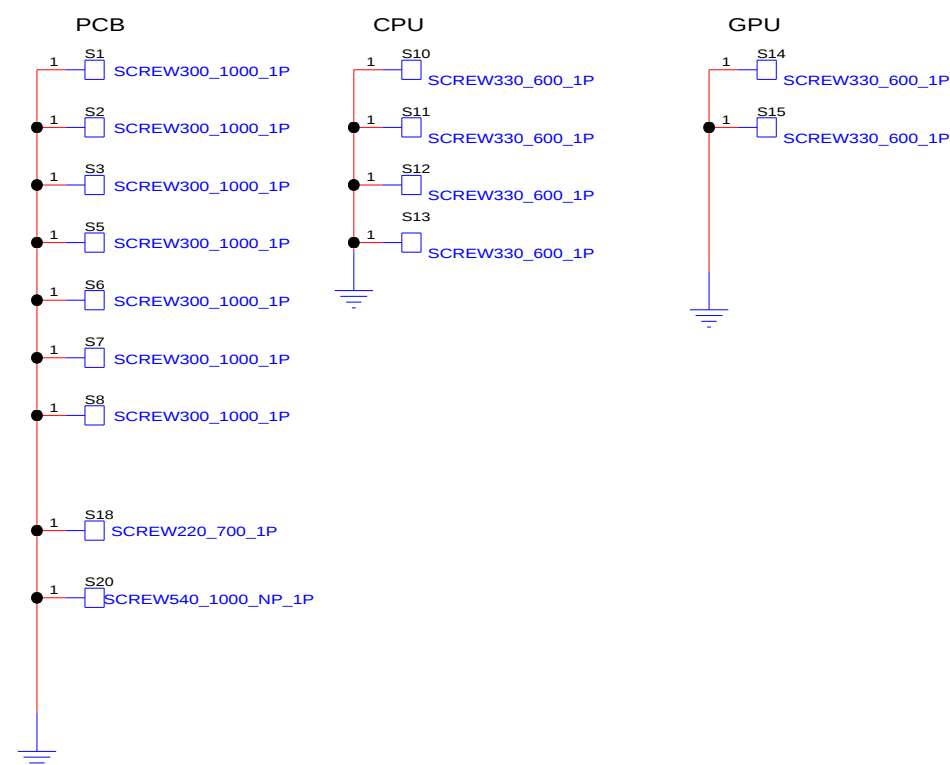
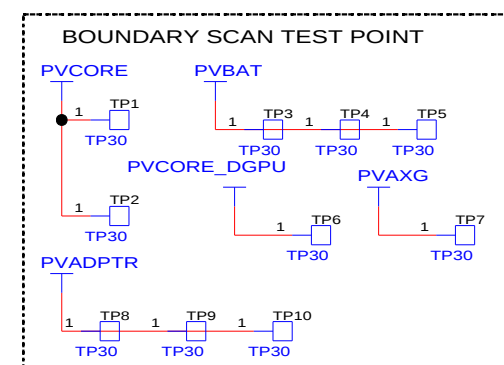
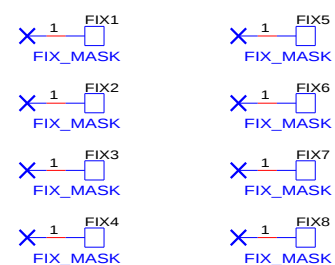
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REFERENCE 0~49(PCB SCREW)



INVENTEC

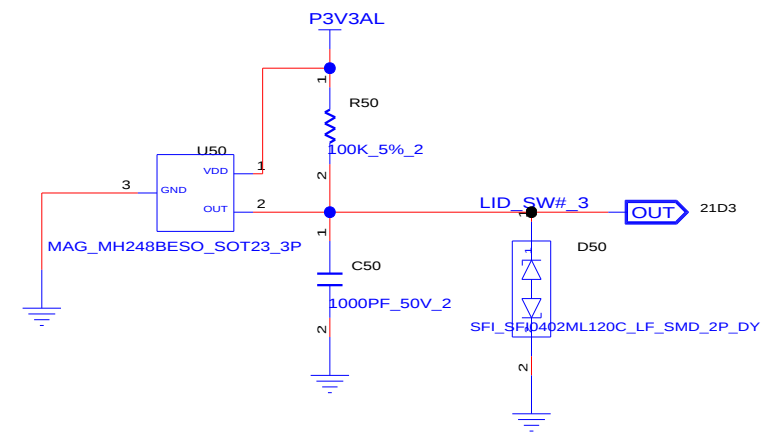
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REFERENCE 50-99(HALL SENSOR)

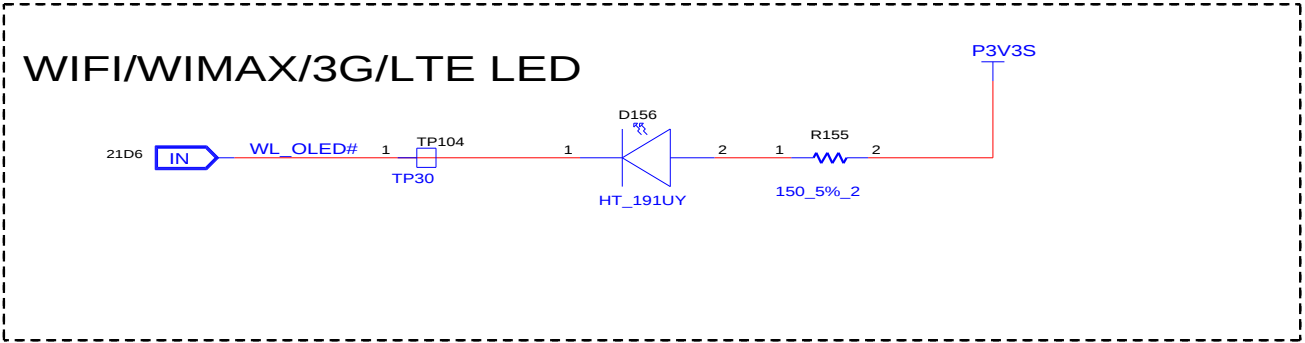
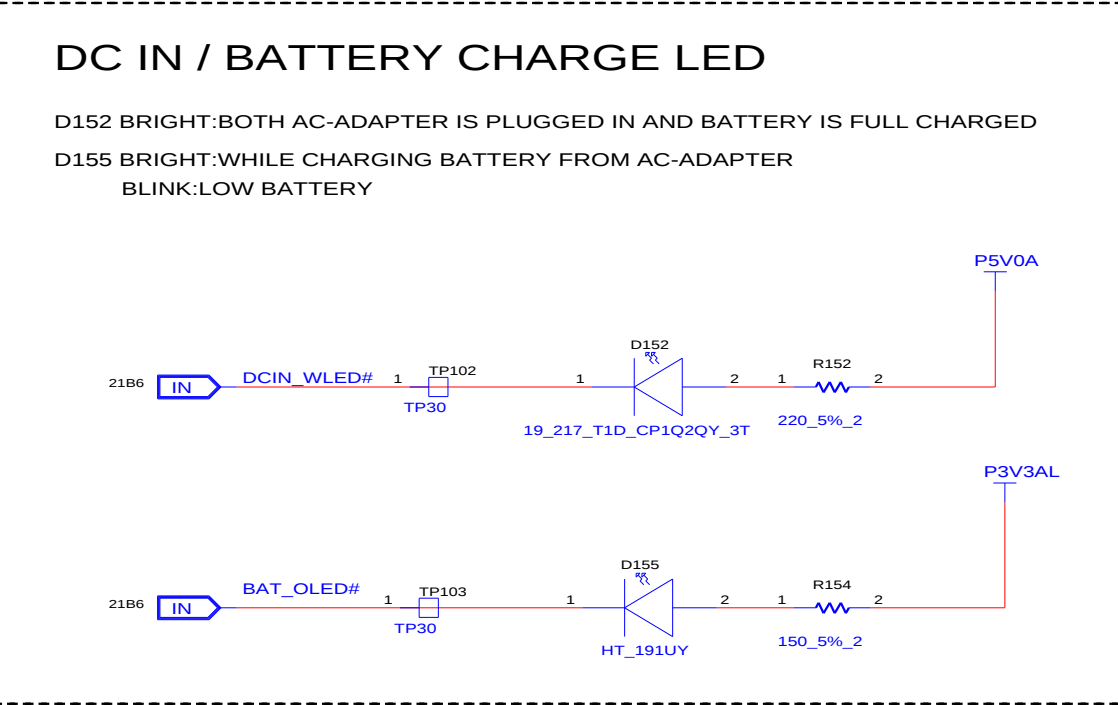
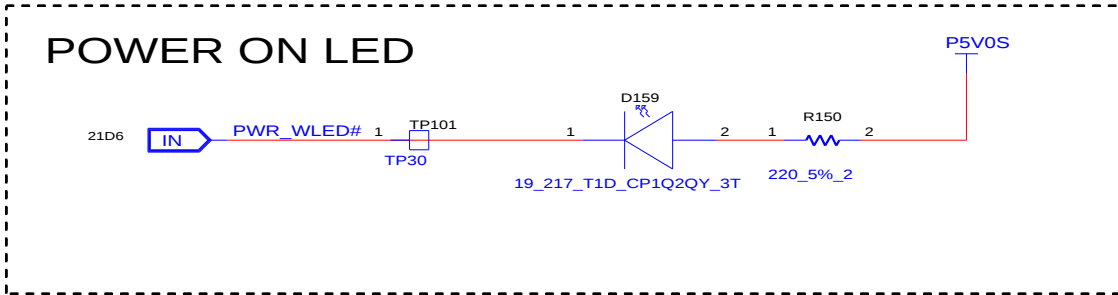
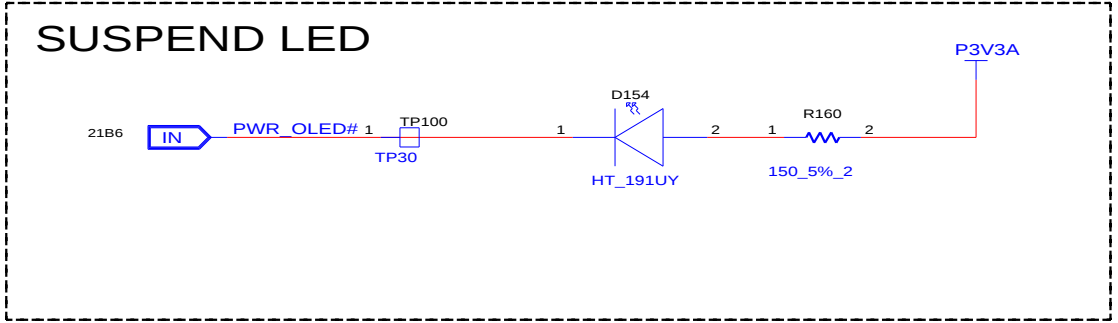


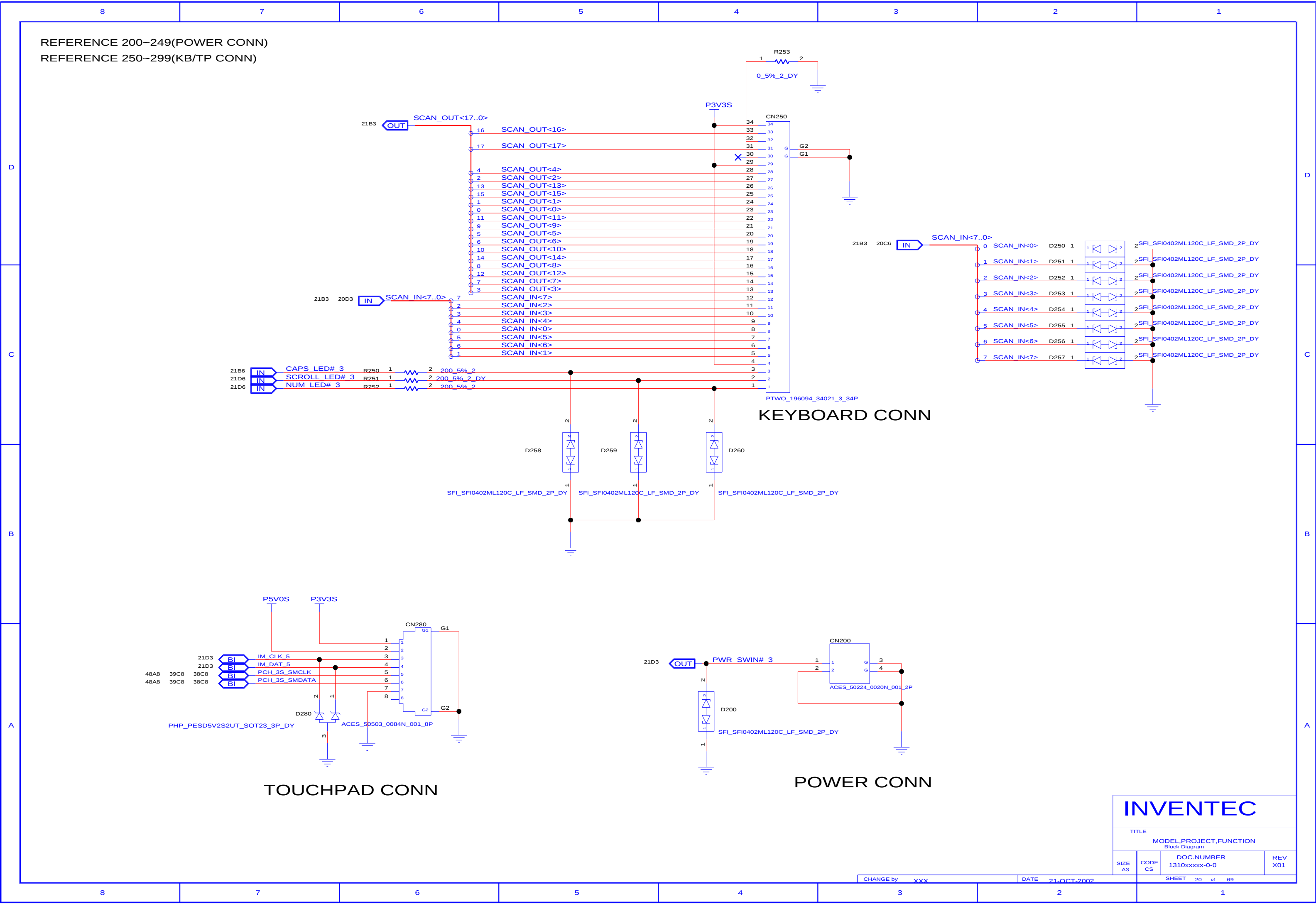
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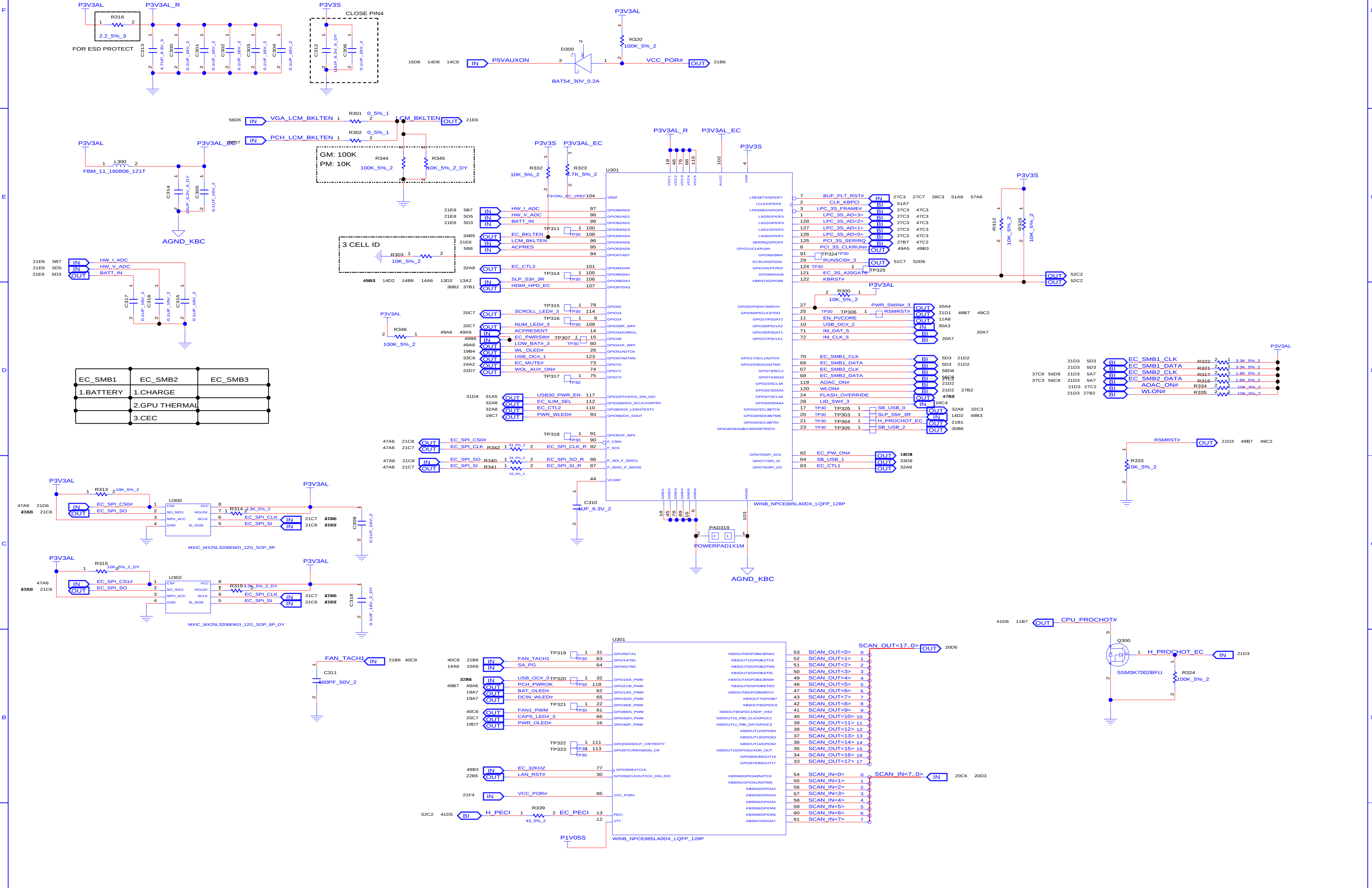
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REFERENCE 300~389(KBC)



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21.OCT.2002

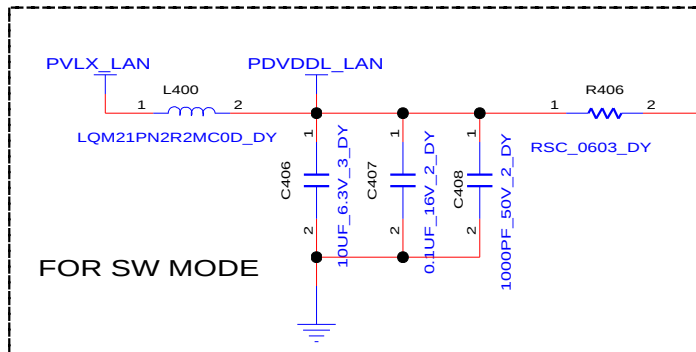
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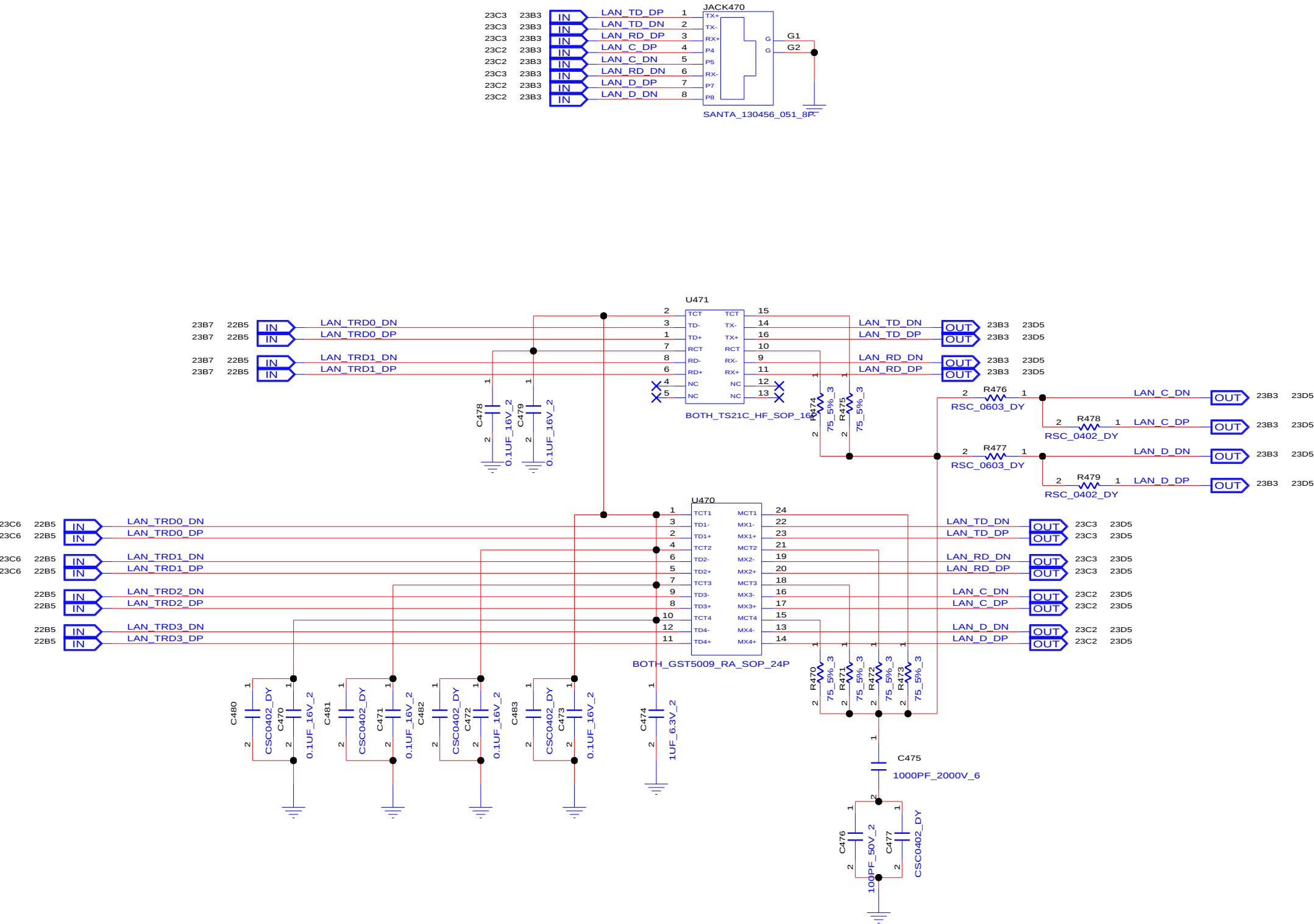
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REFERENCE 400~499(LAN)



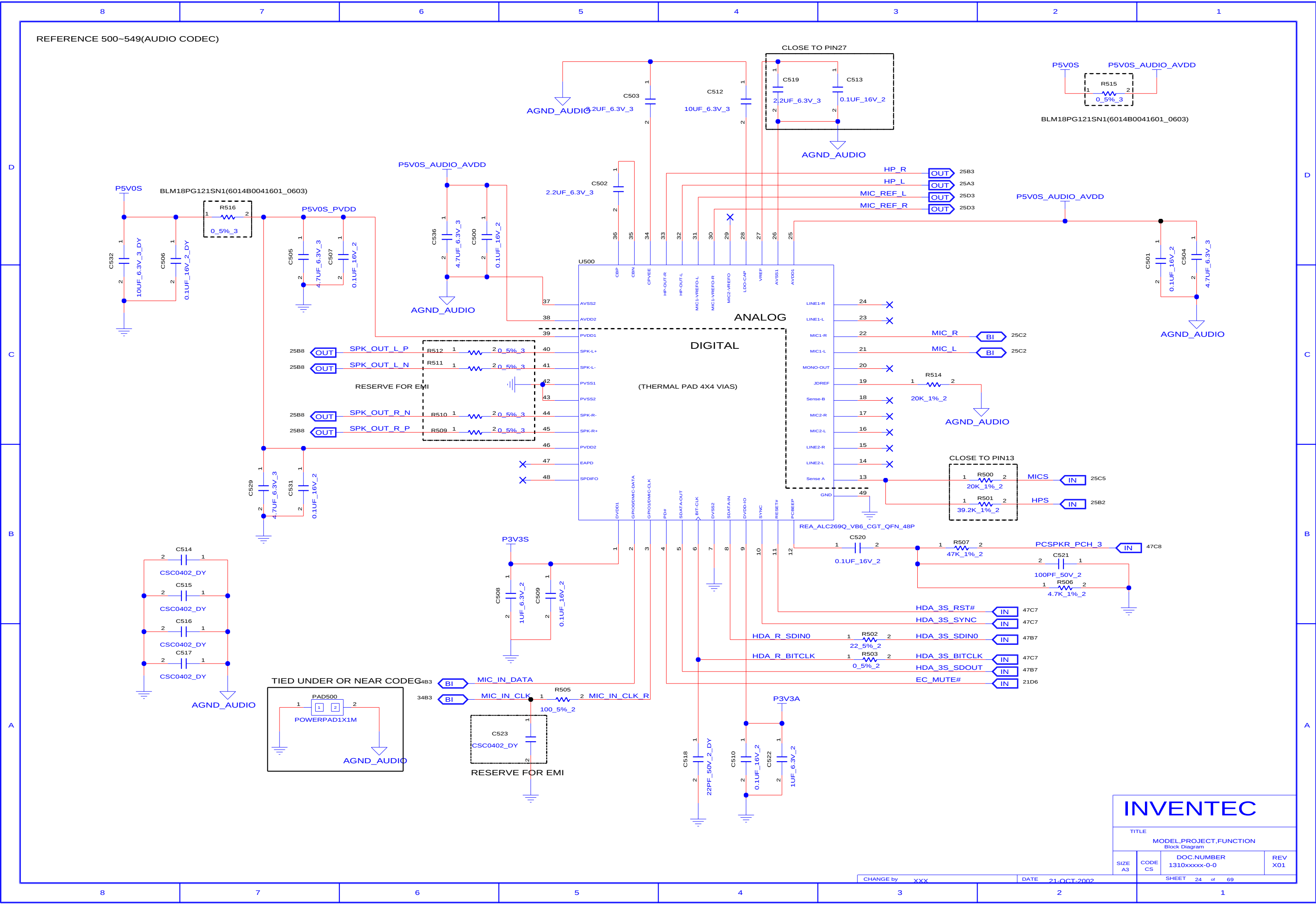
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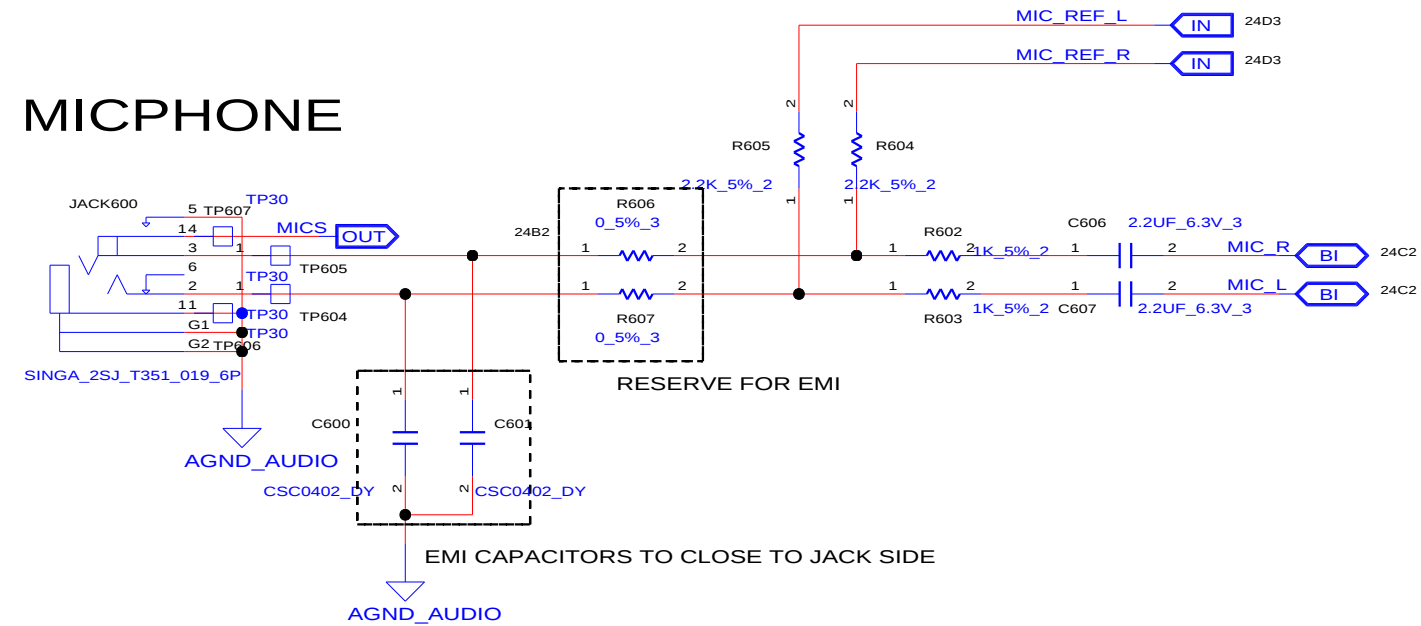


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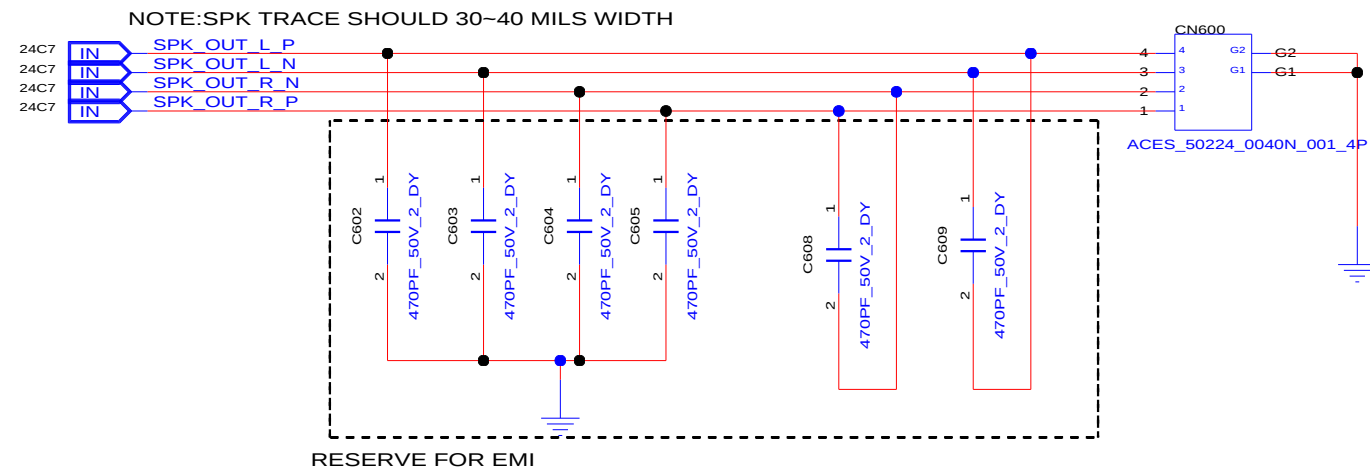
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AUDIO JACKS

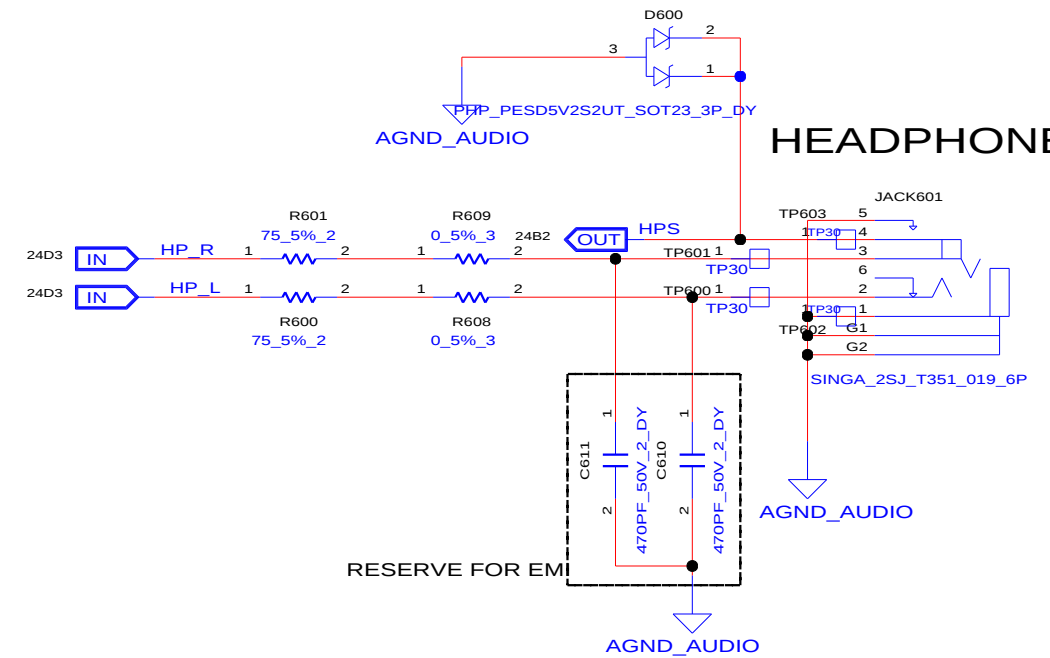
MICPHONE



INTERNAL SPEAKERS



HEADPHONE



INVENTEC

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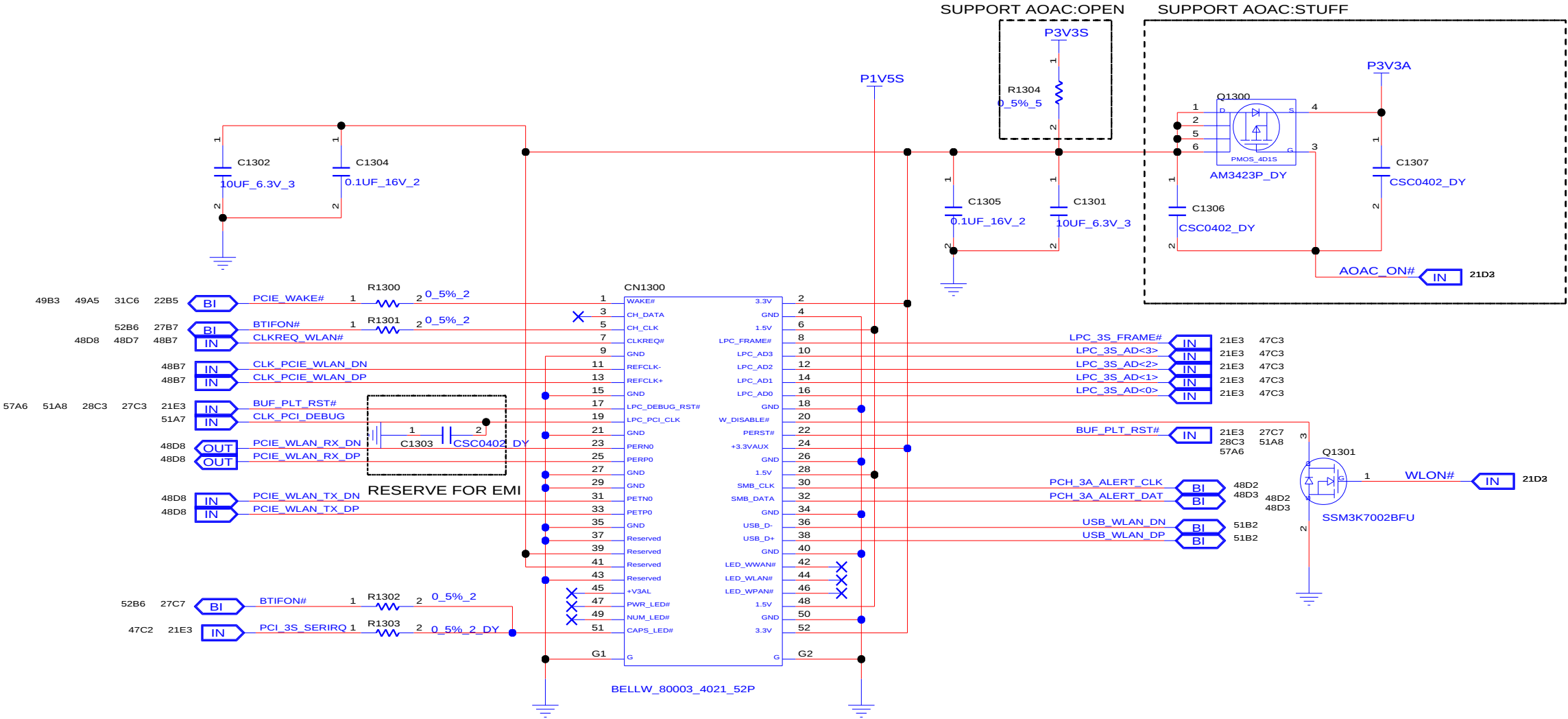
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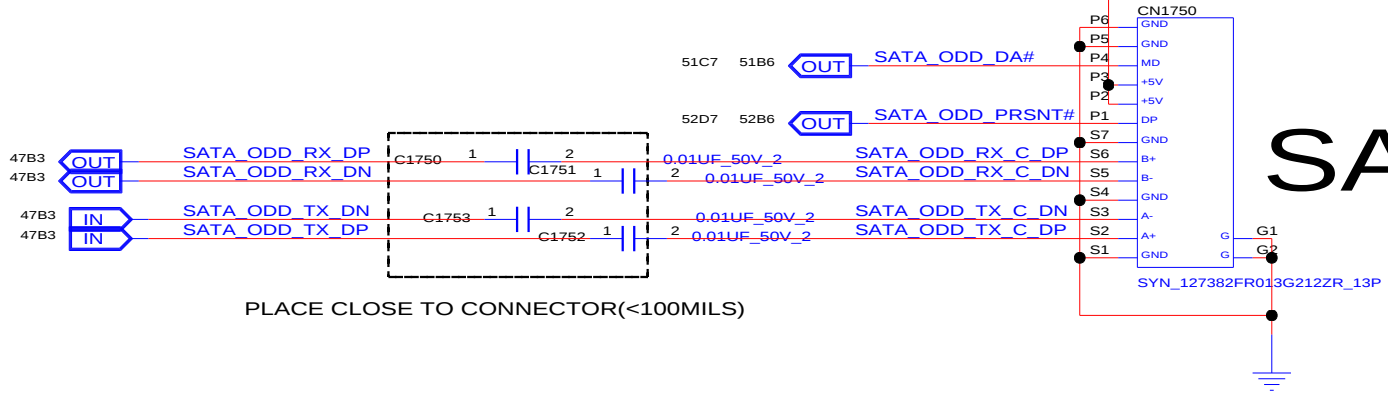
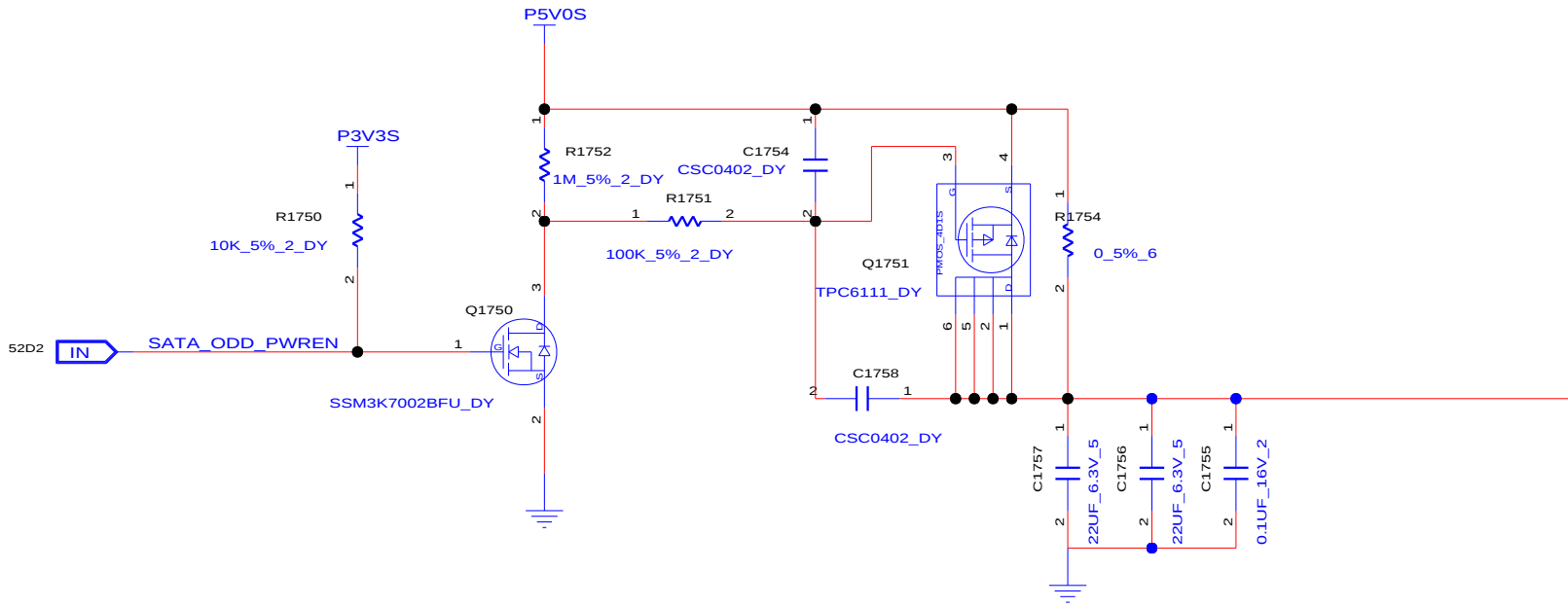
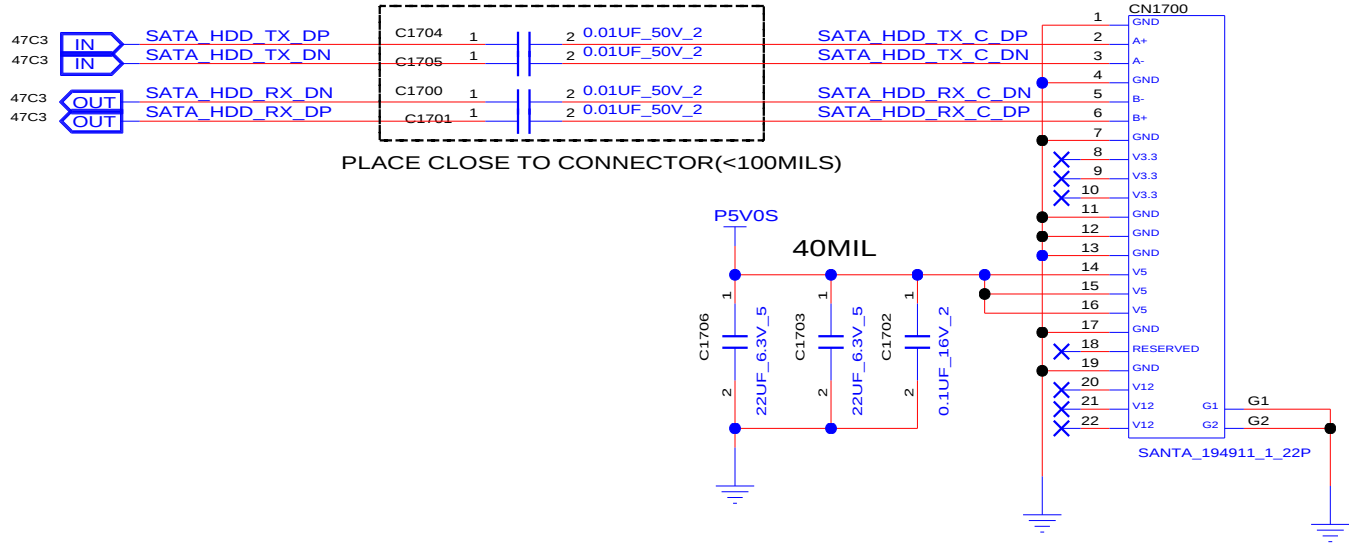


MINI CARD 1(WLAN)

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REFERENCE 1700~1749(HDD)
REFERENCE 1750~1799(ODD)

SATA HDD



SATA ODD

INVENTEC

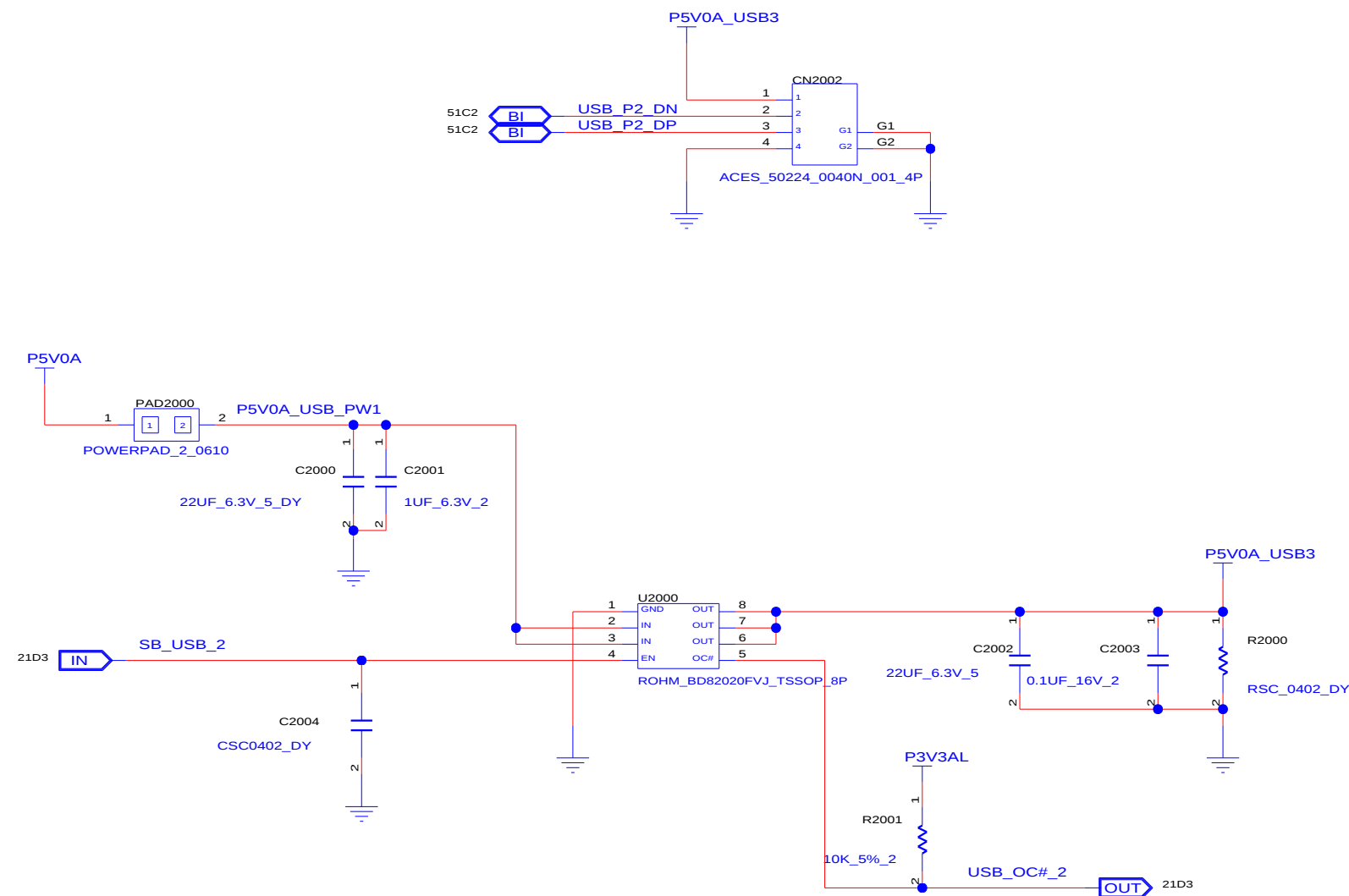
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REFERENCE 2000~2099(USB)



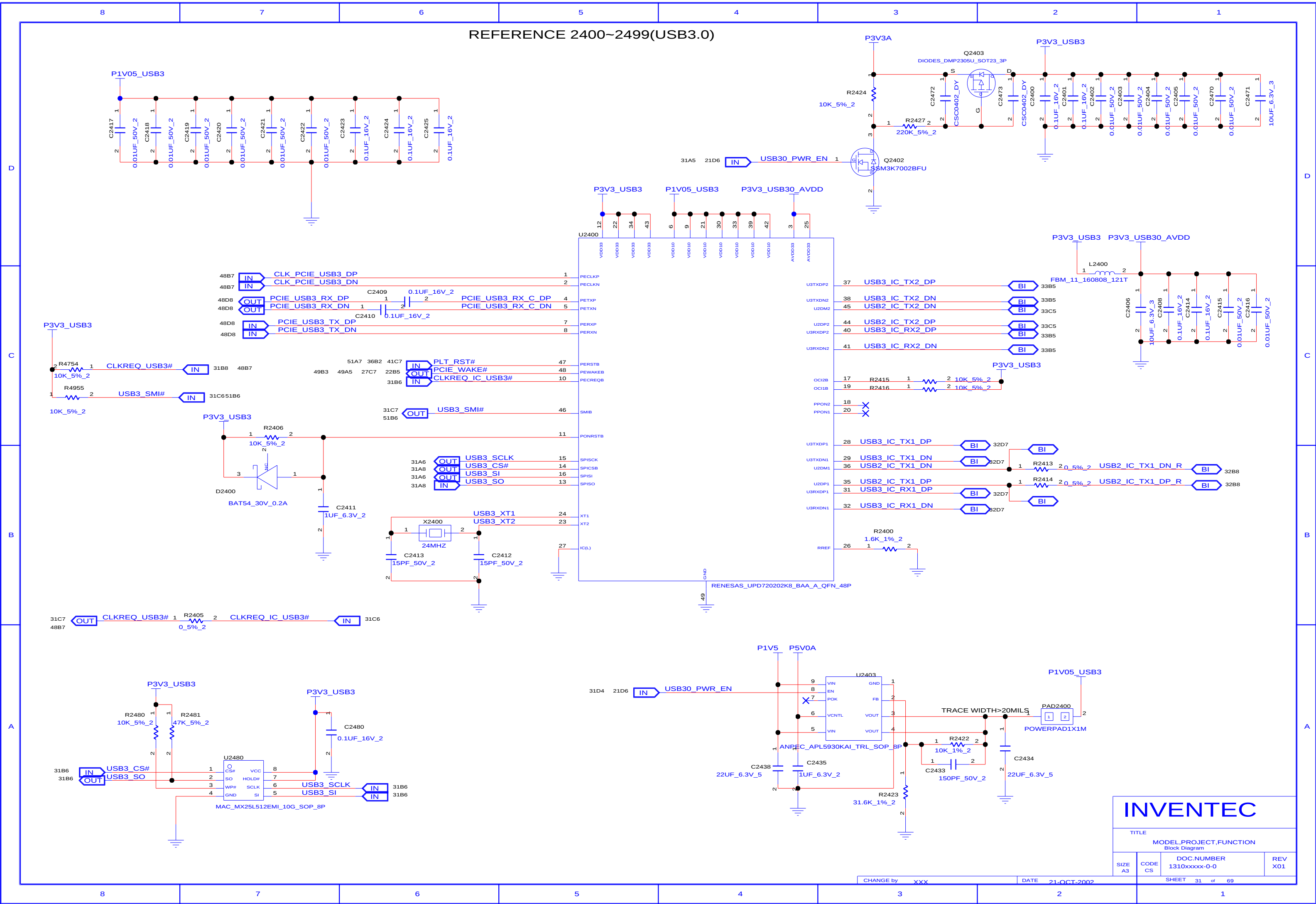
INVENTEC

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SIZE A6	CODE CC	DOC.NUMBER 1310xxxxx-0-0	FIGURE X
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REFERENCE 2400~2499(USB3.0)

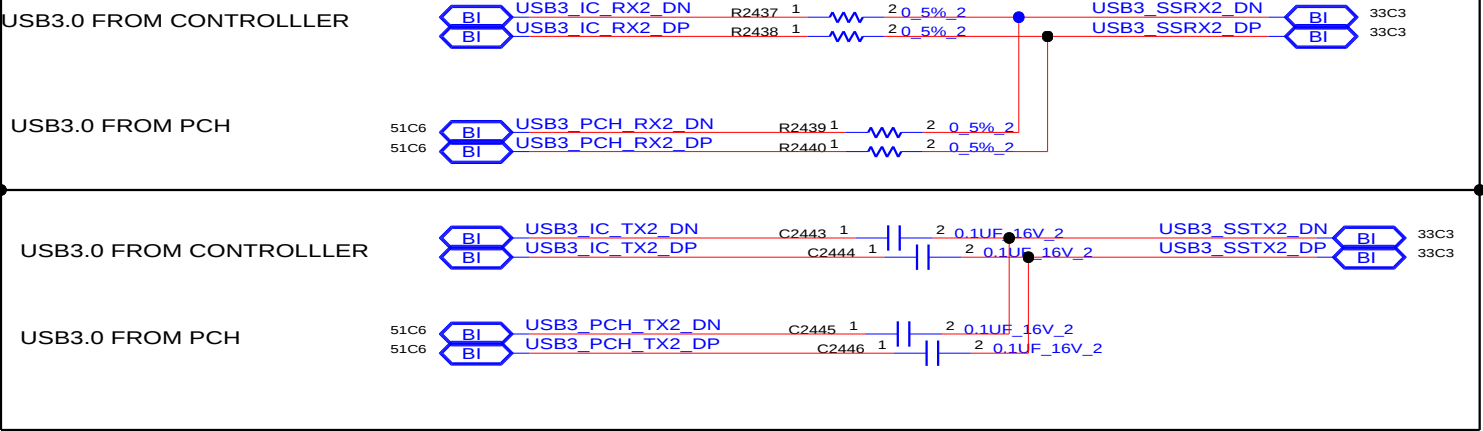
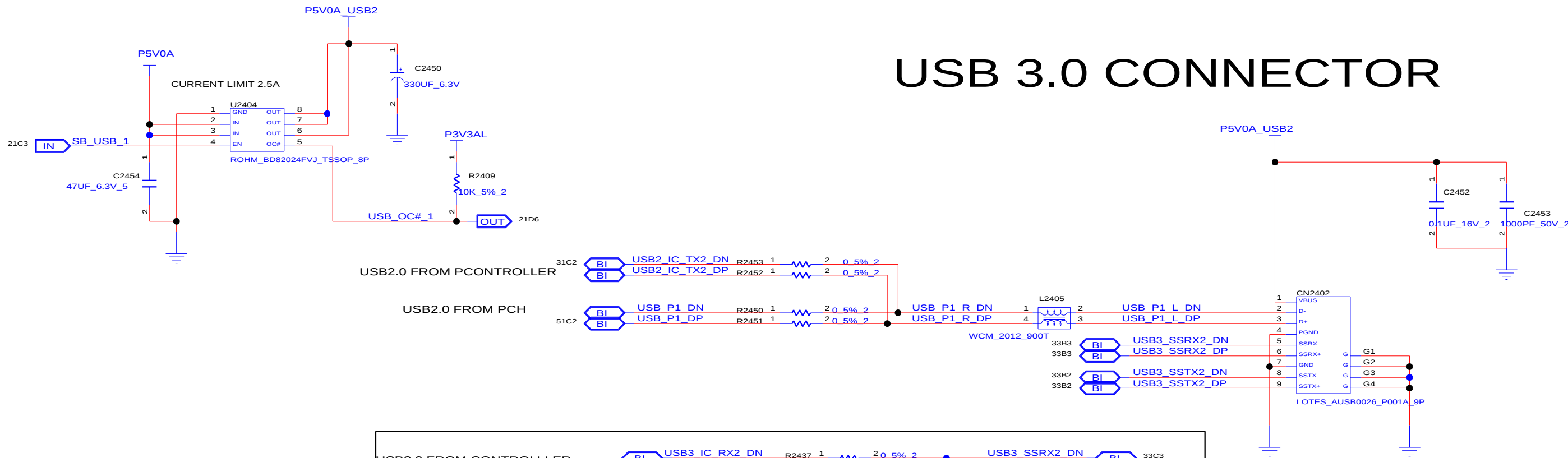


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REFERENCE 2400~2499(USB3.0)

USB 3.0 CONNECTOR



USB3.0

INVENTEC

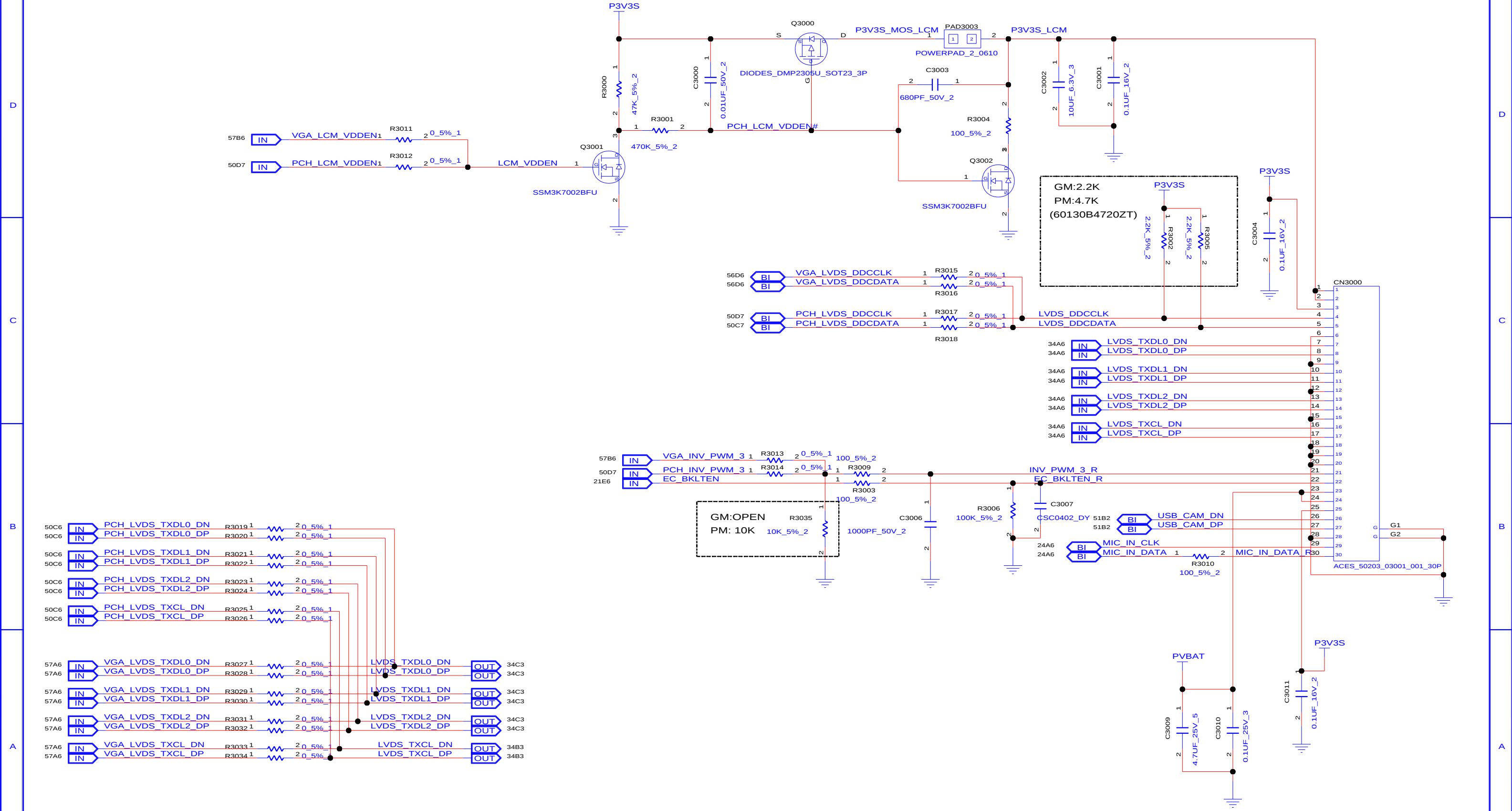
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REFERENCE 3000~3049(LCM)

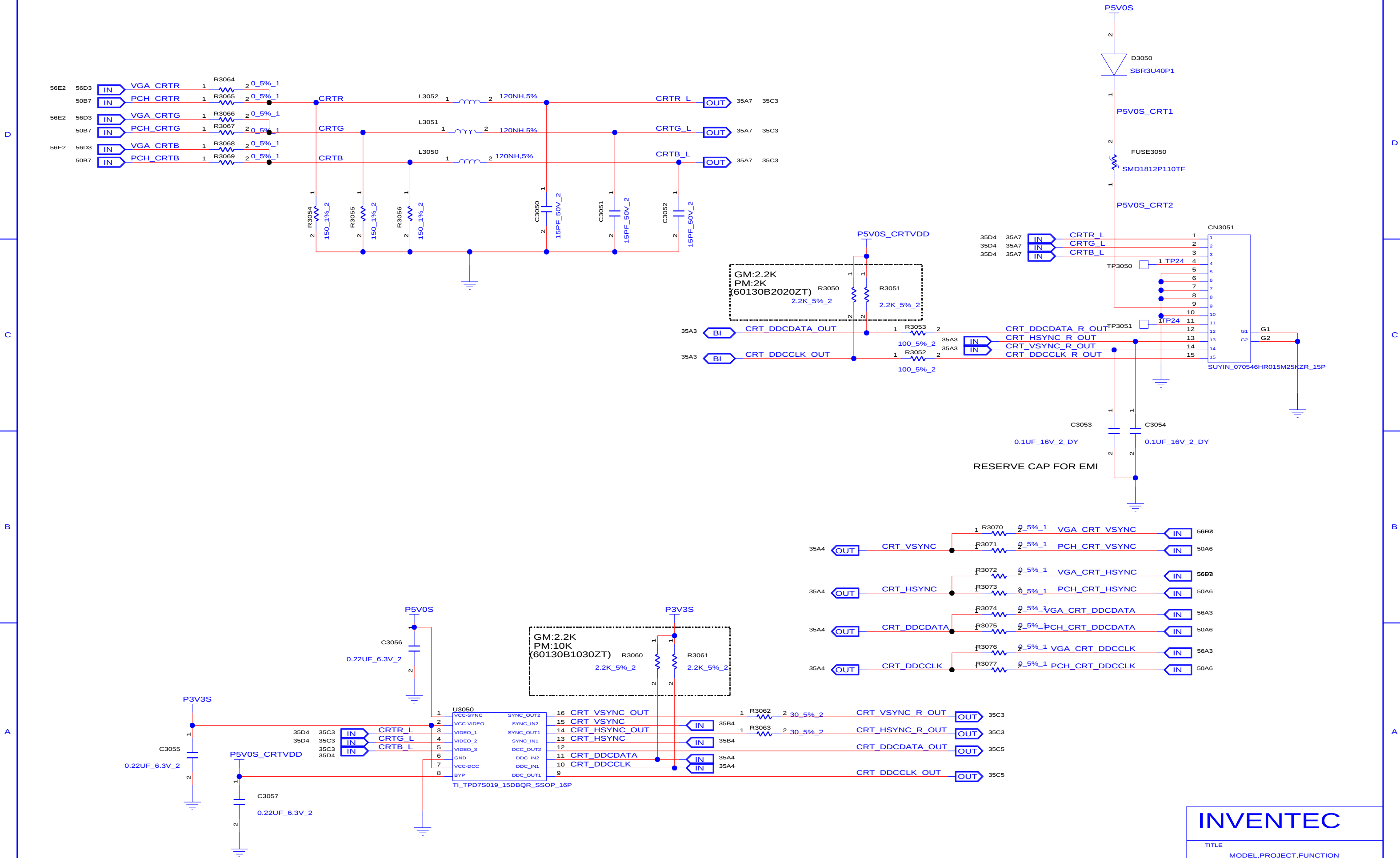


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Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 34 of 69

REFERENCE 3050~3099(CRT)



INVENTEC

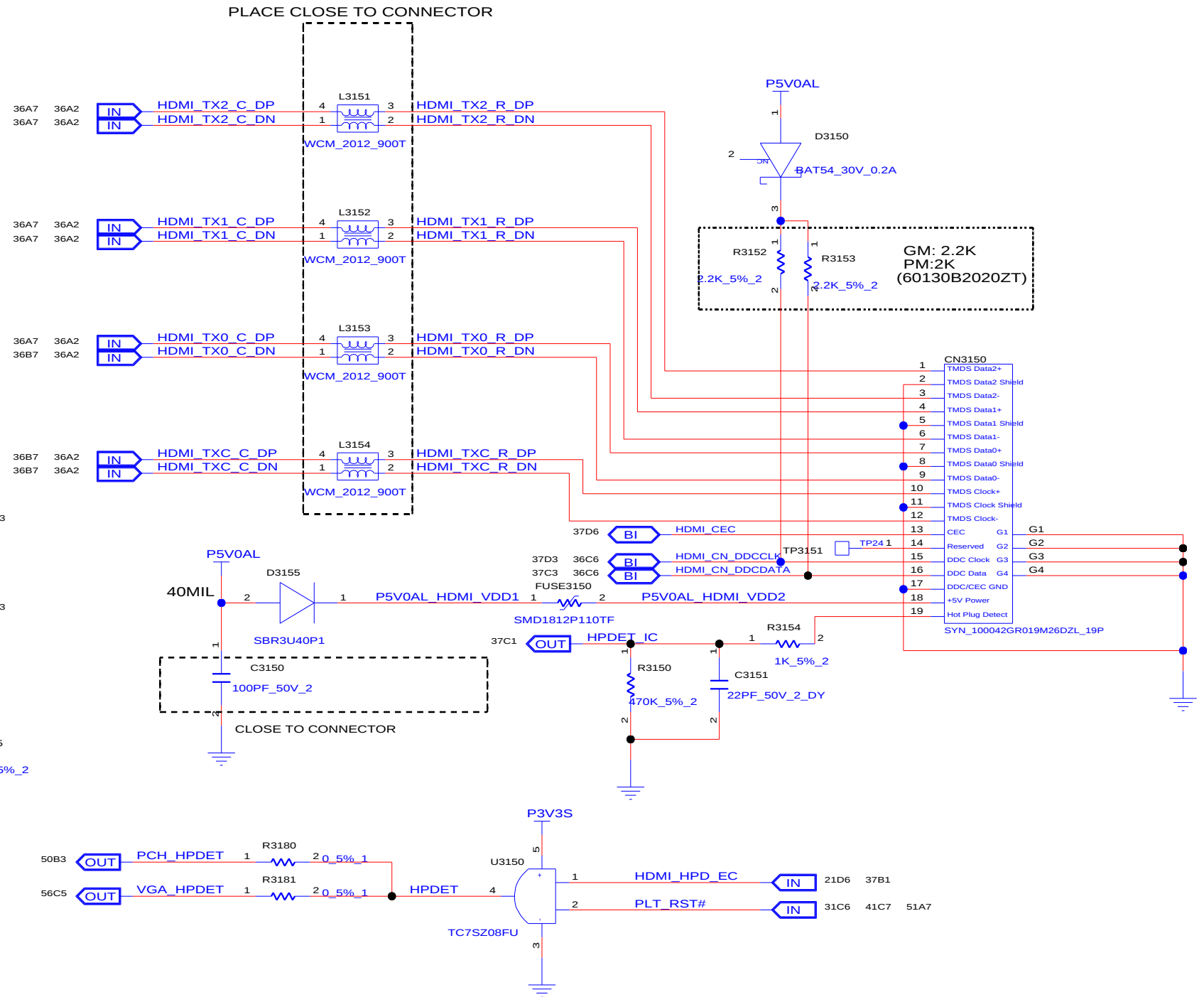
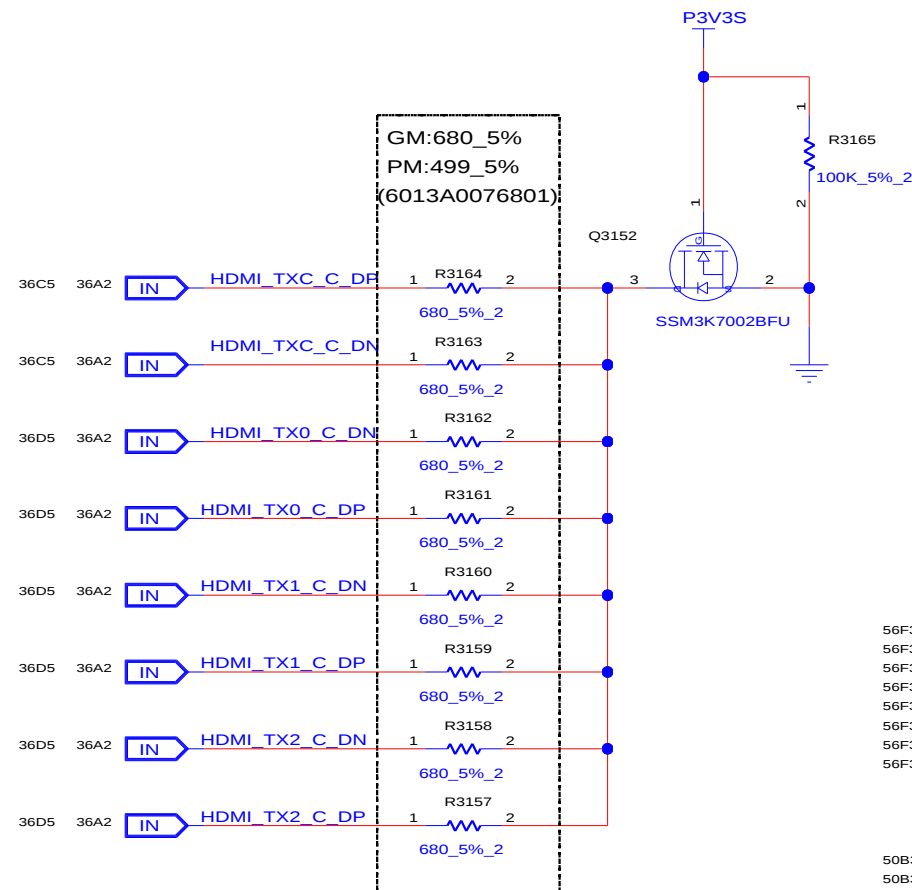
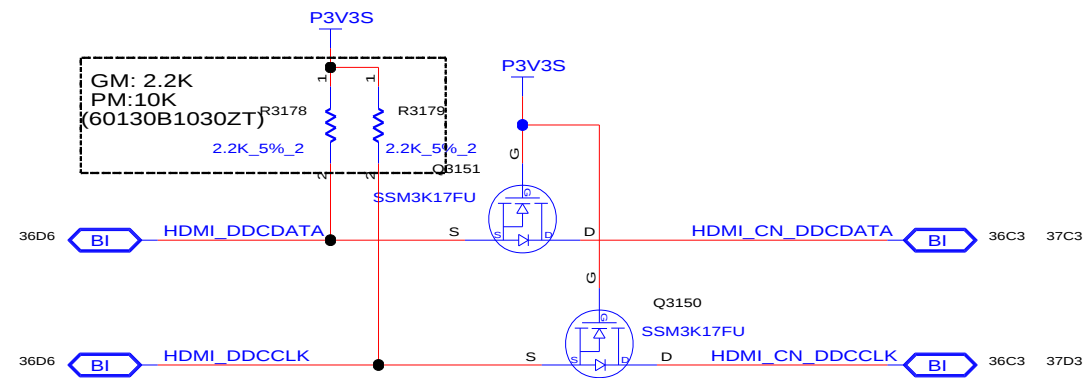
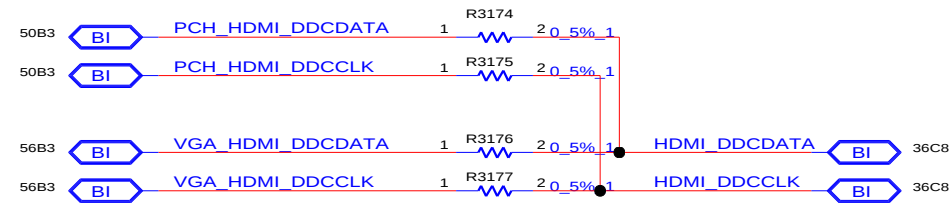
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002

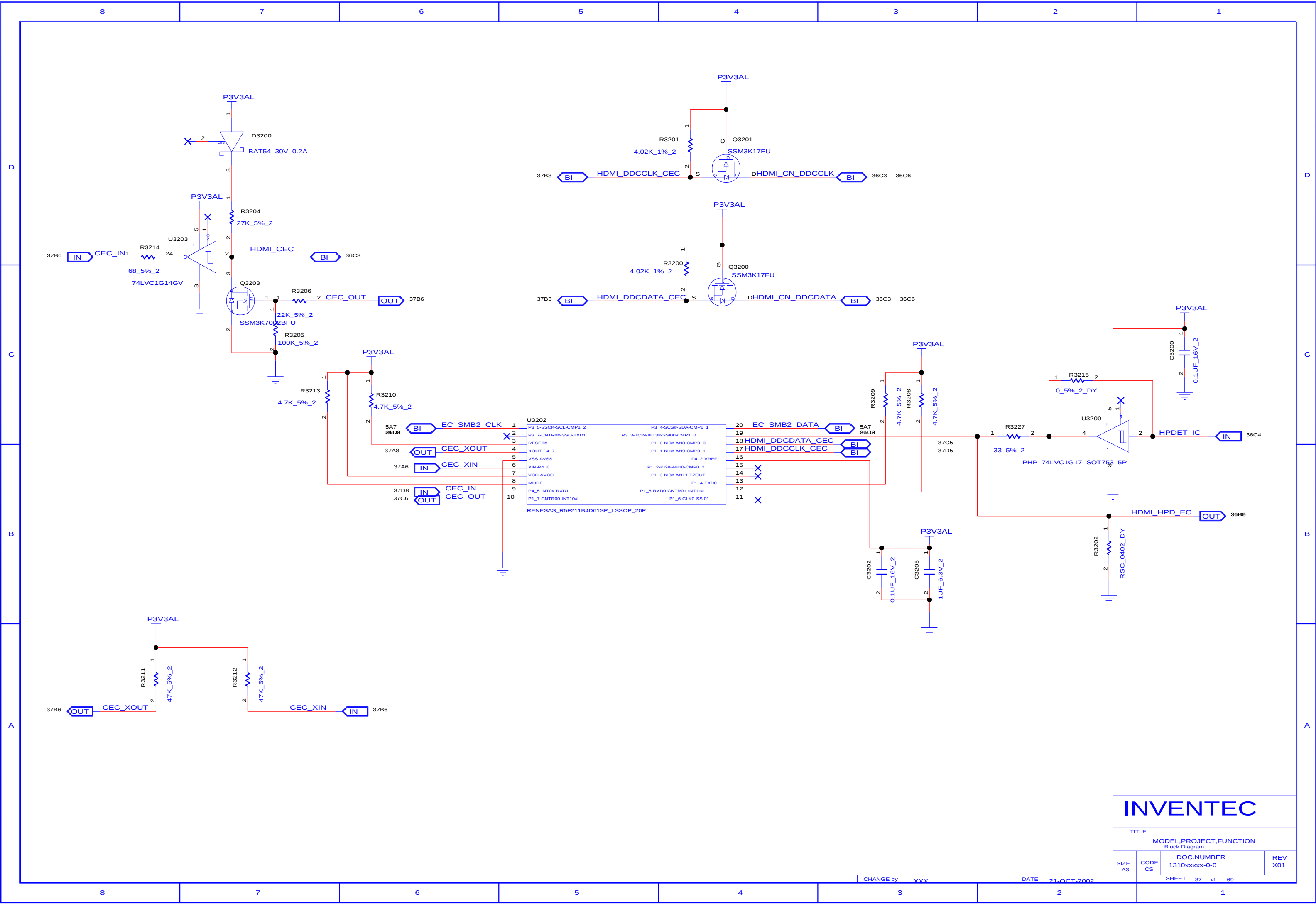
SHEET 35 of 69

REFERENCE 3150~3199(HDMI)



INVENTEC

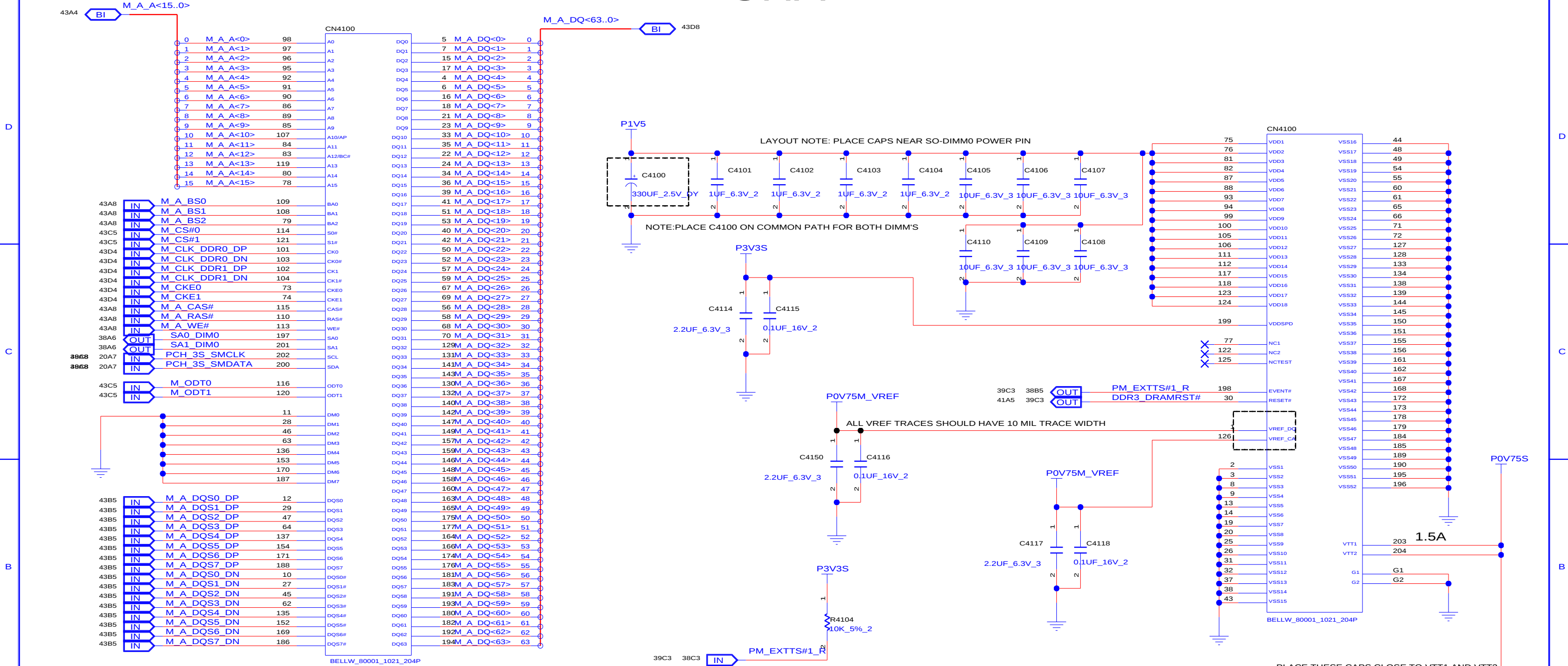
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 36 of 69			



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHA

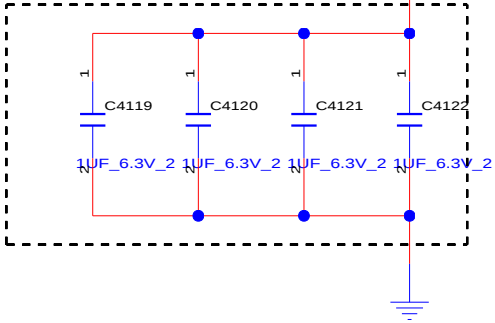
REFERENCE 4100-4299(DDR)



NOTE:

IF SA0_DIM0=1 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA2
SO-DIMMA TS ADDRESS IS 0X32

IF SA0_DIM0=0 , SA1_DIM0=0
SO-DIMMA SPD ADDRESS IS 0XA0
SO-DIMMA TS ADDRESS IS 0X30



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

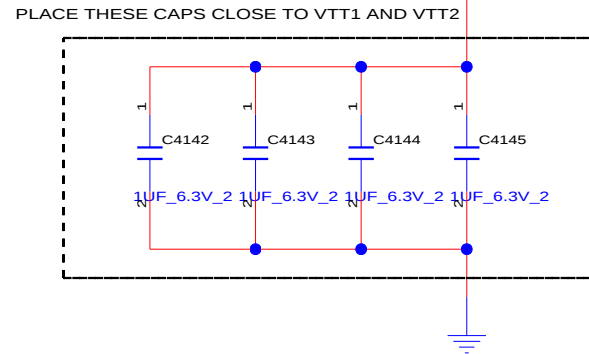
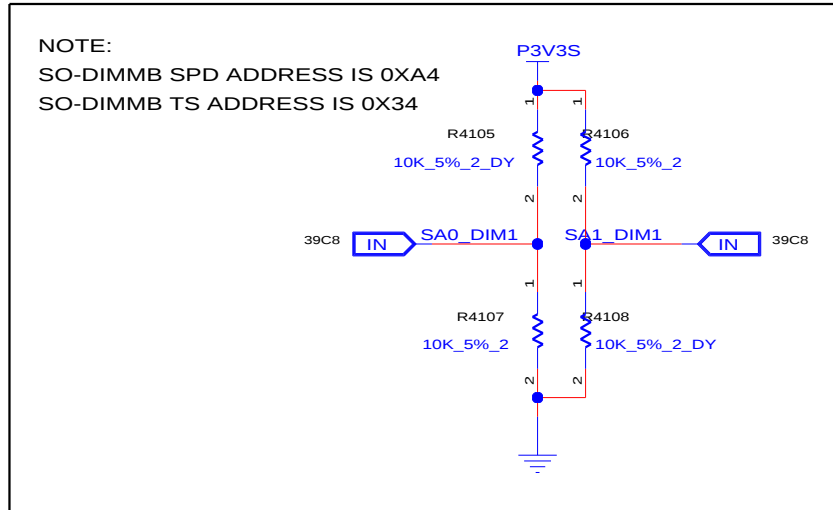
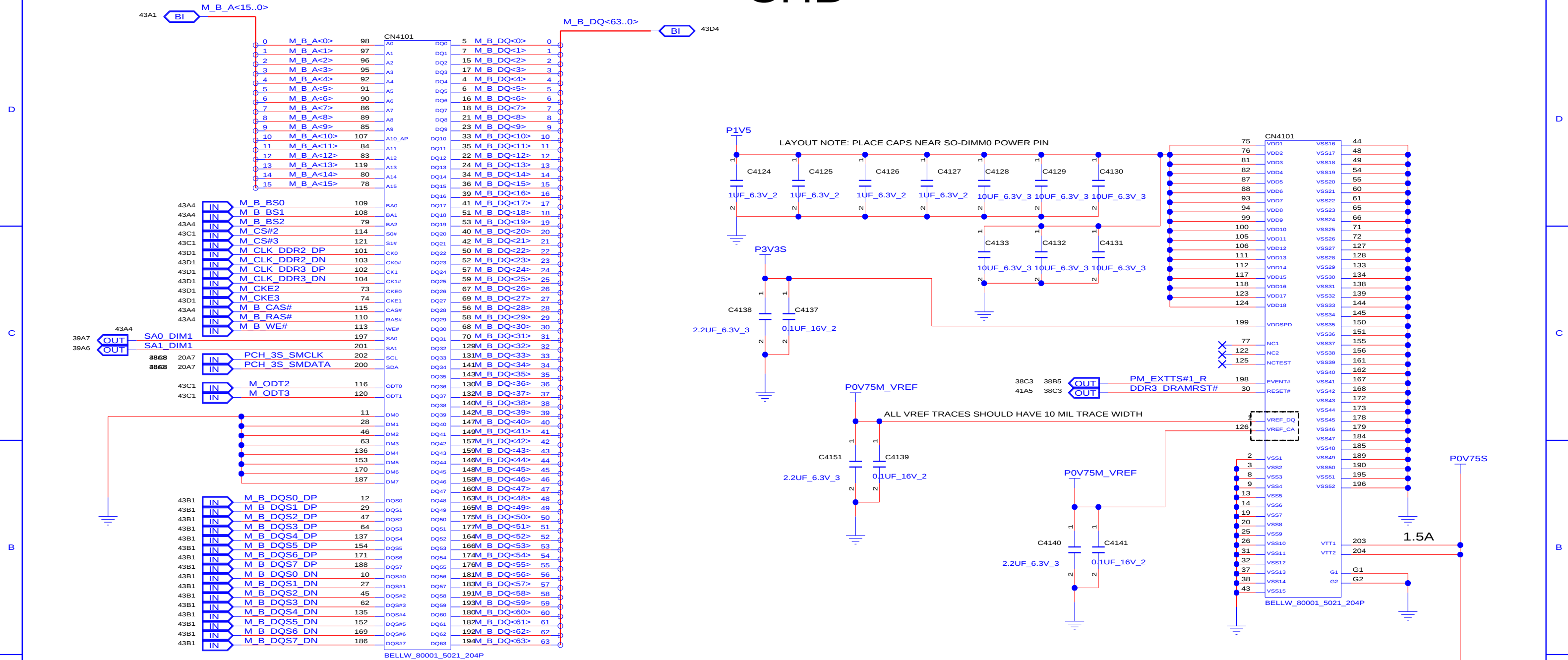
SIZE A3 CODE CS DOC.NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 38 of 69

REFERENCE 4100~4299(DDR)

CHB



INVENTEC

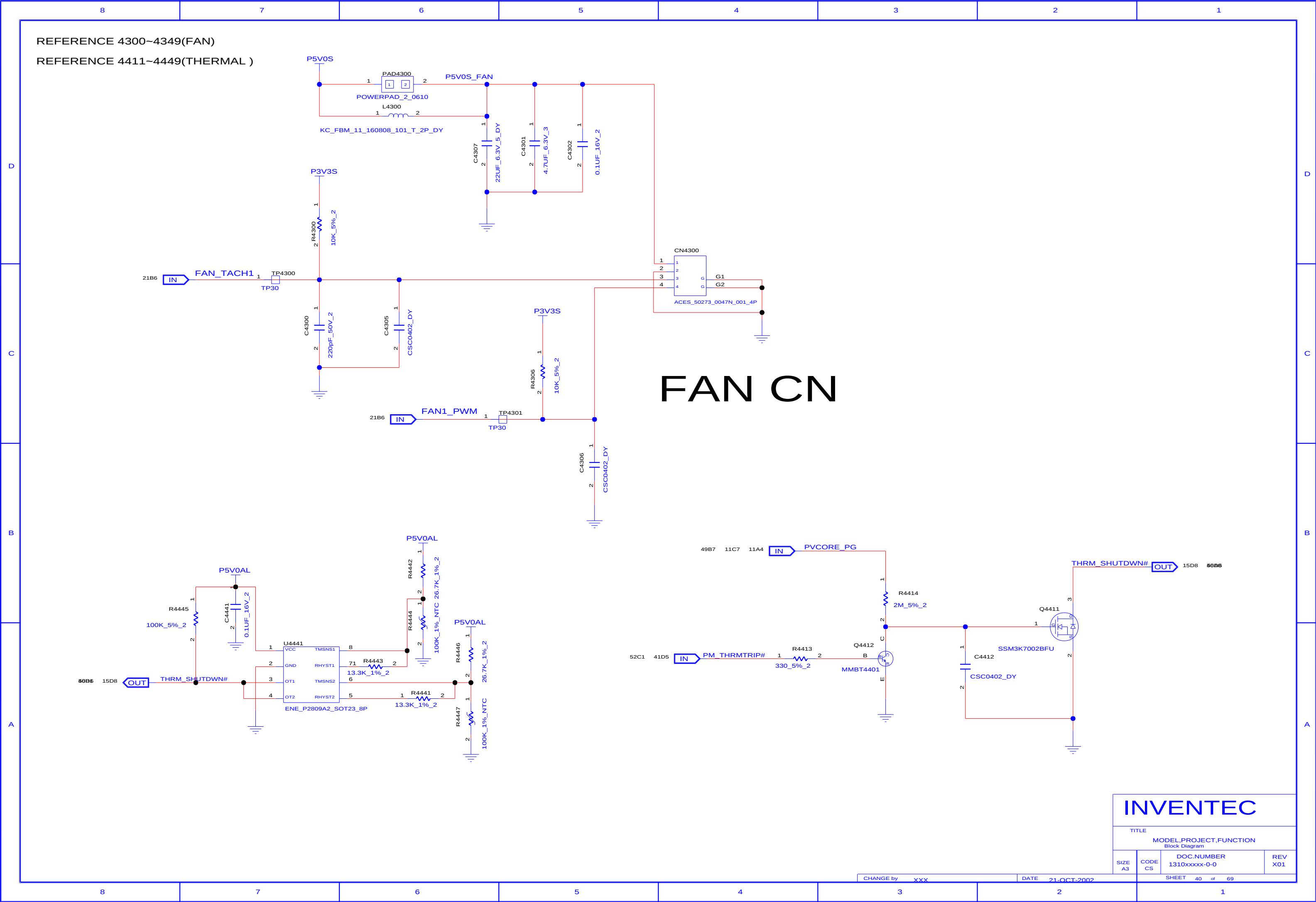
TITLE

MODEL,PROJECT,FUNCTION
Block Diagram

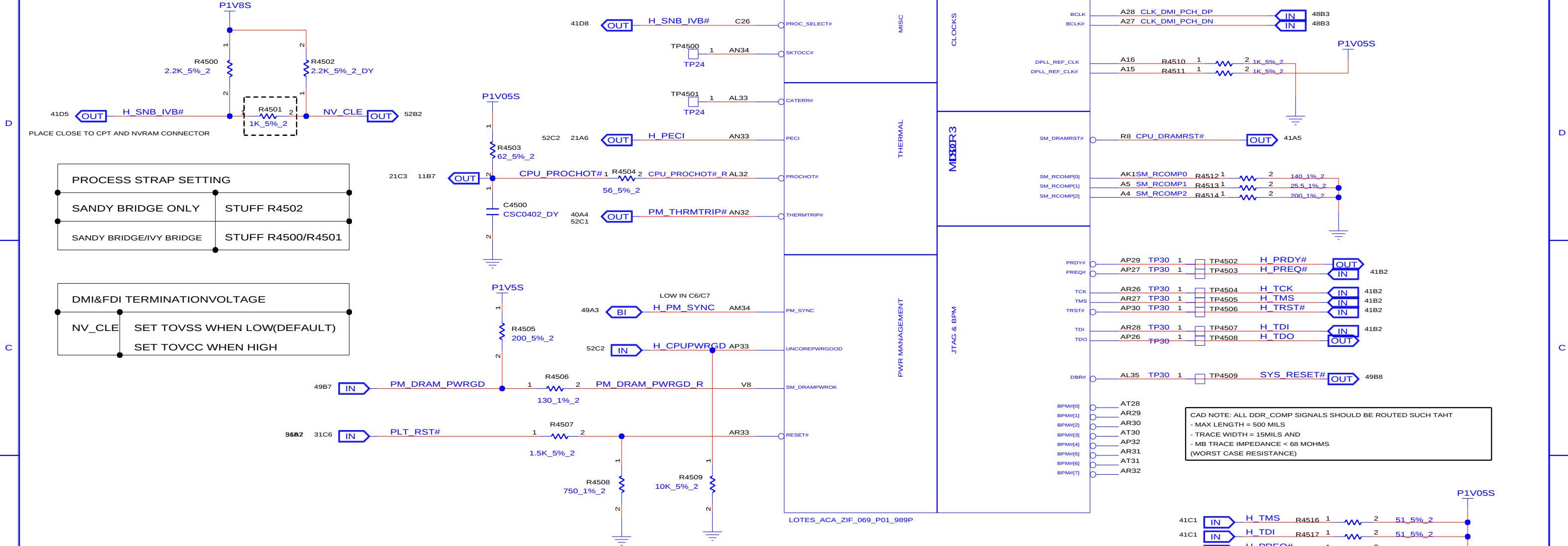
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002

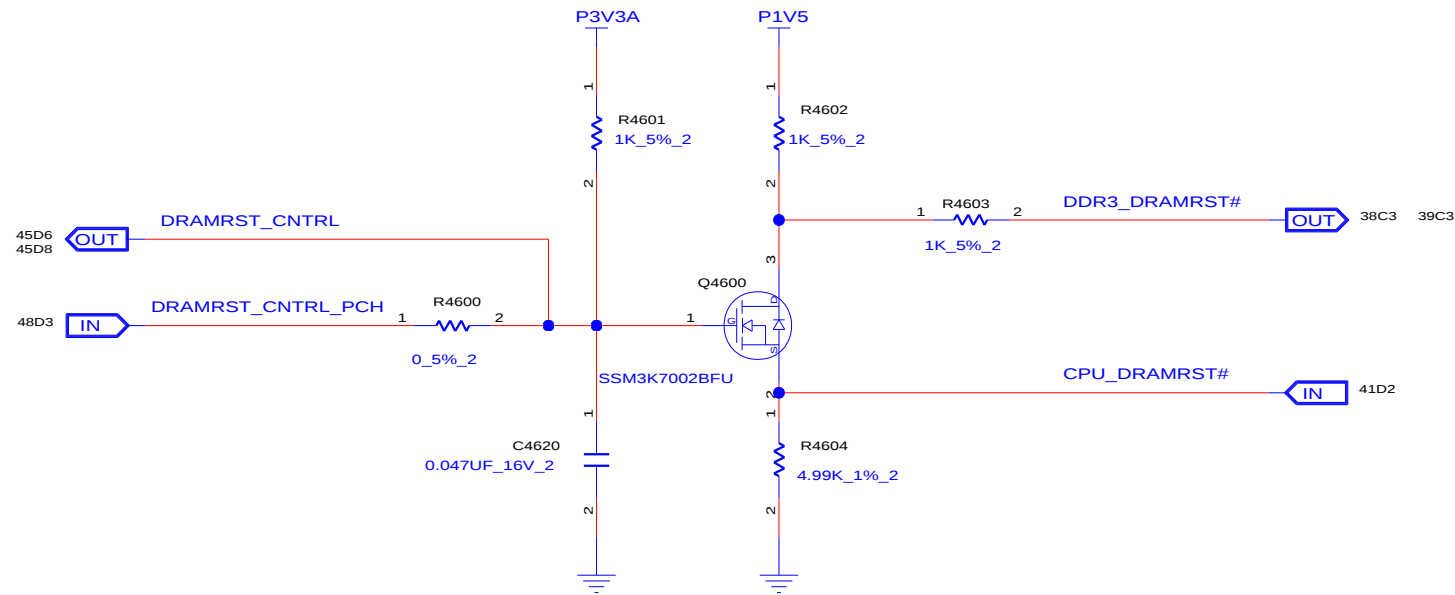
SHEET 39 of 69



REFERENCE 4500~4699(CPU)



S3 CIRCUIT: DRAM_RST# TO MEMORY SHOULD BE HIGH DURING S3



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by	DATE	SHEET	of
XXX	21-OCT-2002	41	69

REFERENCE 4500~4699(CPU)

P1V05S

R4521
24.9_1%_2

CAD NOTE: DP_COMPIO AND ICOMPO SIGNALS
SHOULD BE SHORTED NEAR BALLS AND ROUTED WITH
- TYPICAL IMPEDANCE < 25 MOHMS

CAD NOTE: PEG_ICOMPI AND RCOMPO SIGNALS
SHOULD BE SHORTED AND ROUTED WITH
- MAX LENGTH = 500 MILS
- TYPICAL IMPEDANCE = 43 MOHMS

PEG_ICOMPO SIGNALS SHOULD BE ROUTED WITH
- MAX LENGTH = 500 MILS
- TYPICAL IMPEDANCE = 14.5 MOHMS

CLOSE TO CPU

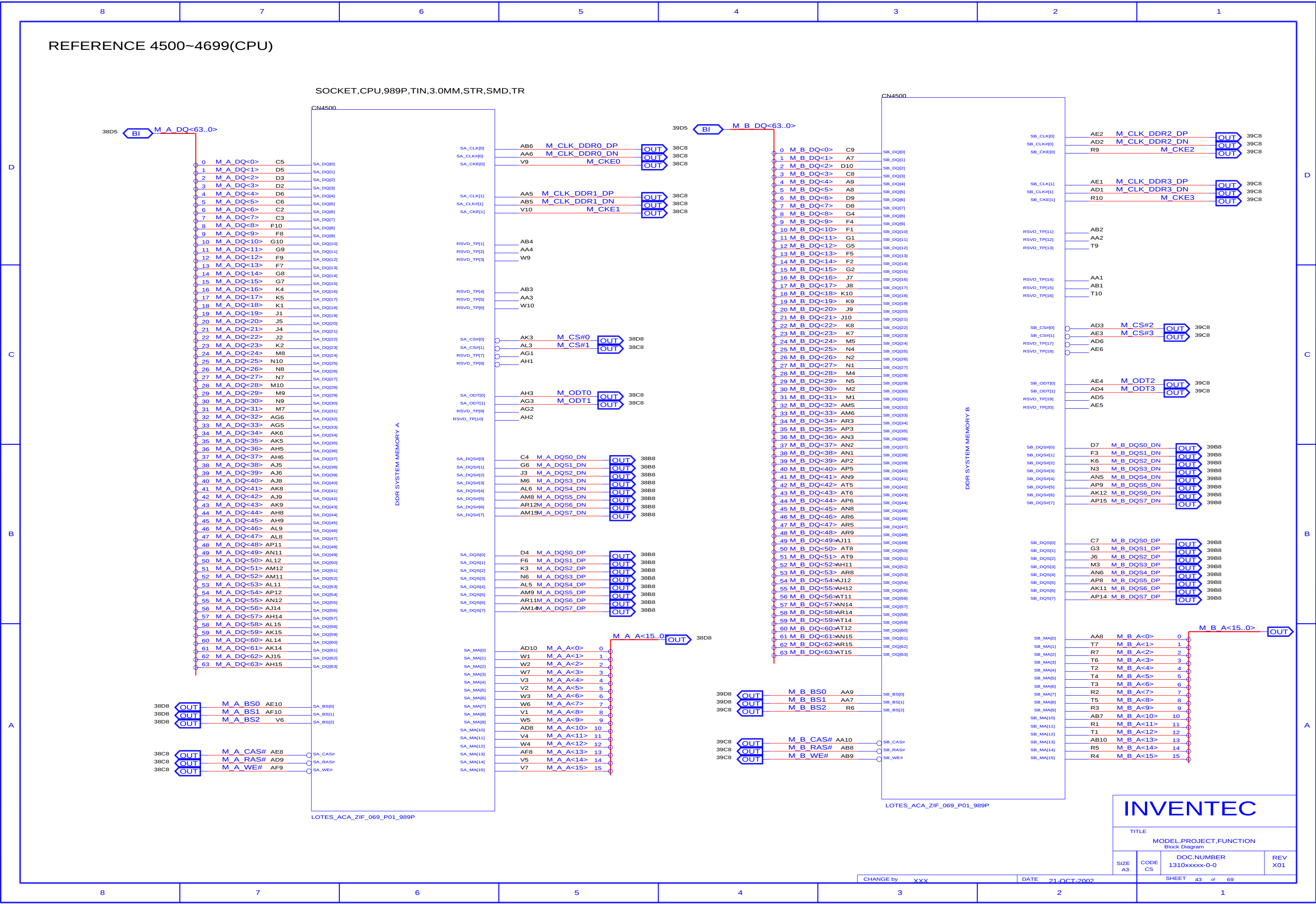
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002

SHEET 42 of 69

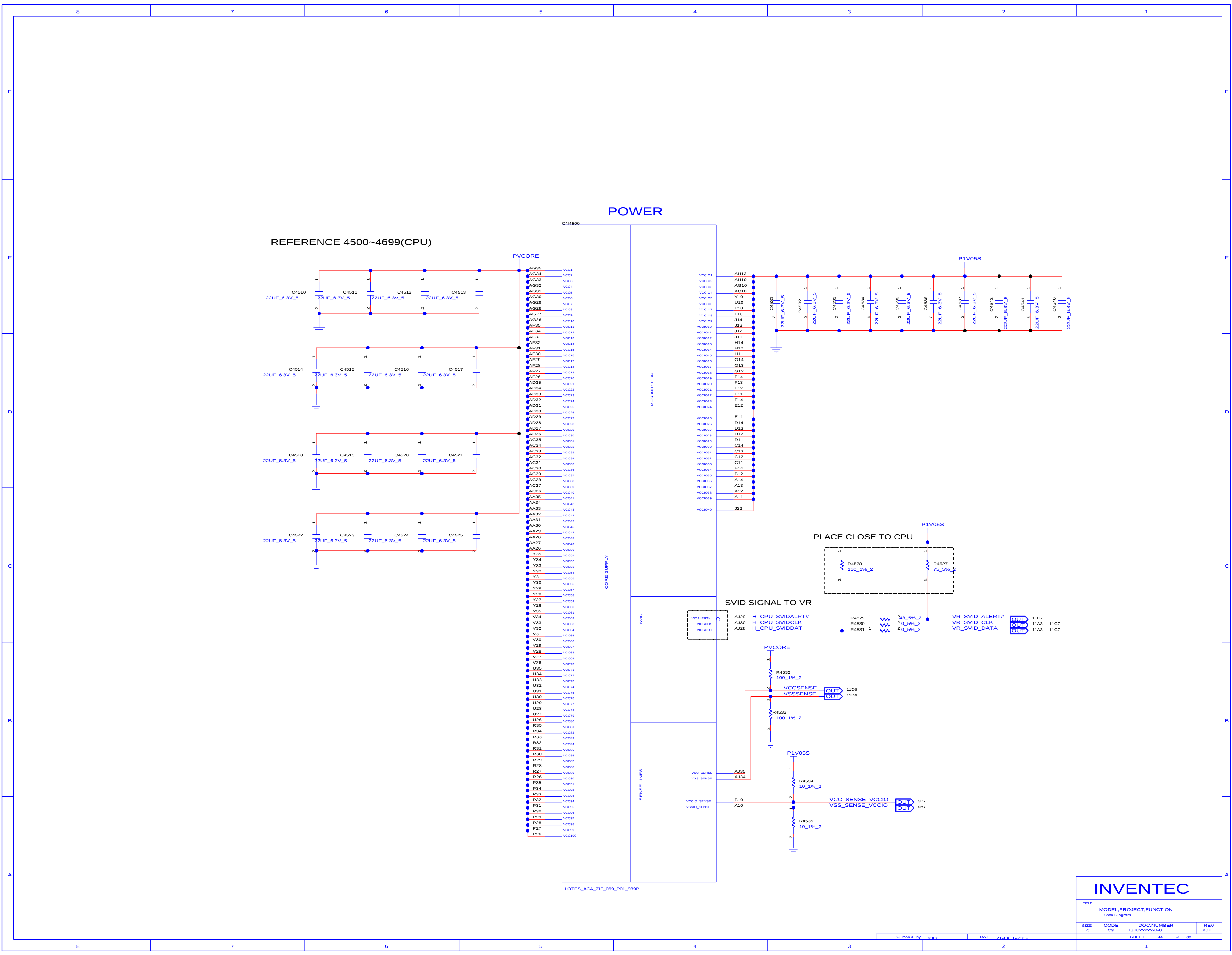


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

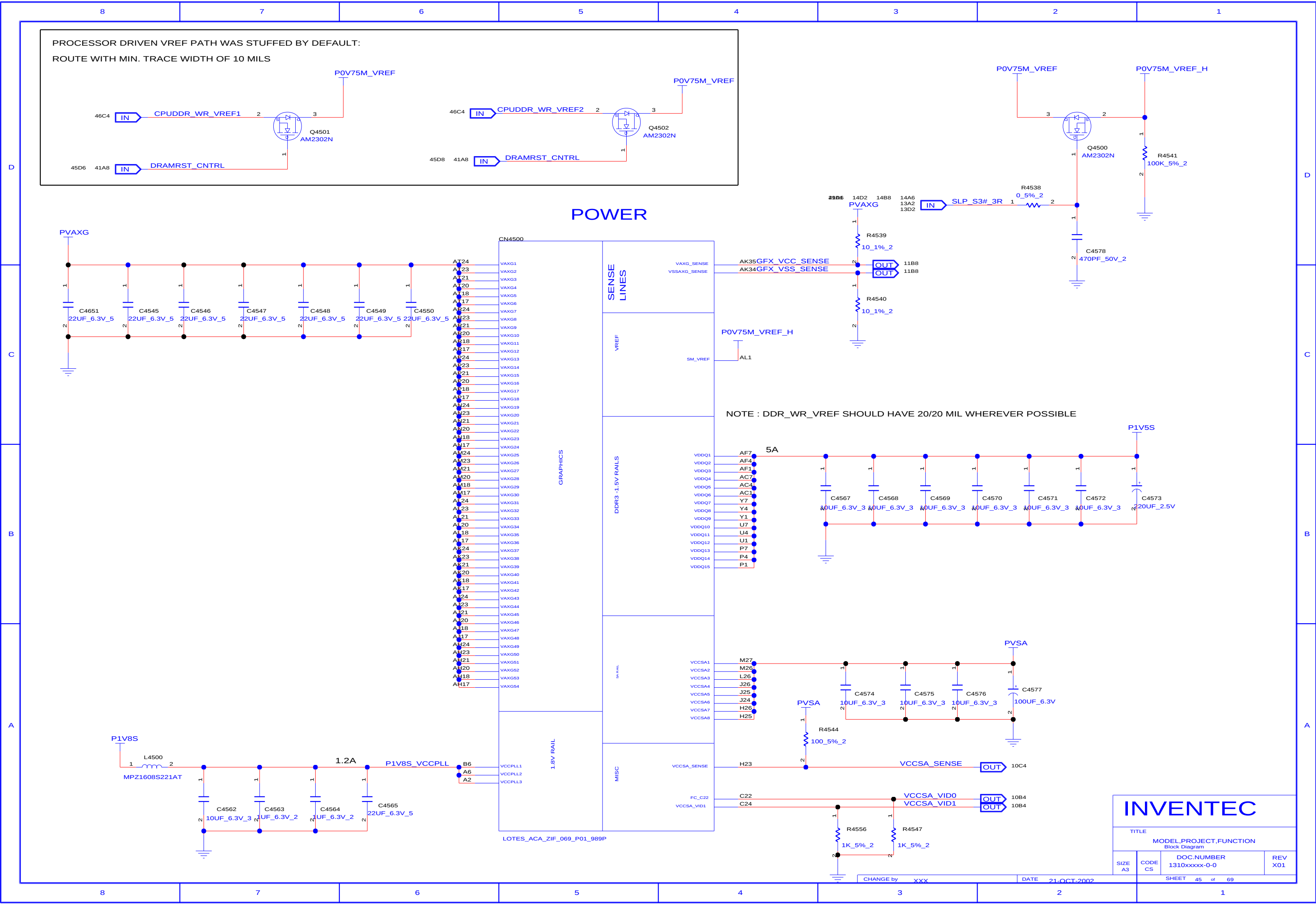
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 43 of 69



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
C	CS	1310XXXX-0-0	X01
SHEET		44	of 69

CHANGE by xxx DATE 21.OCT.2002



POWER

SENSE LINES

VREF

DDR3-1.5V RAILS

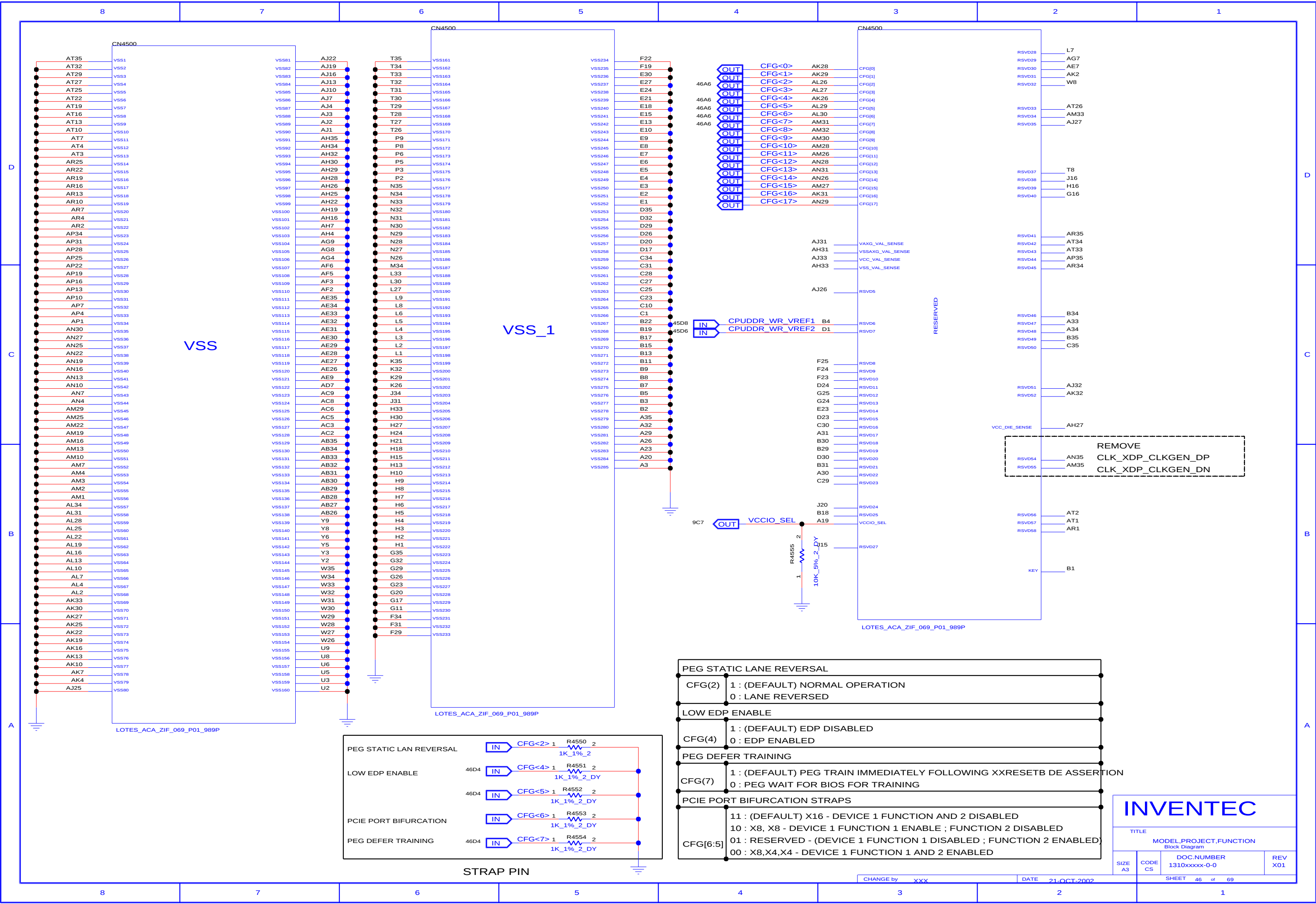
MISC

1.8V RAIL

INVENTEC

TITLE MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

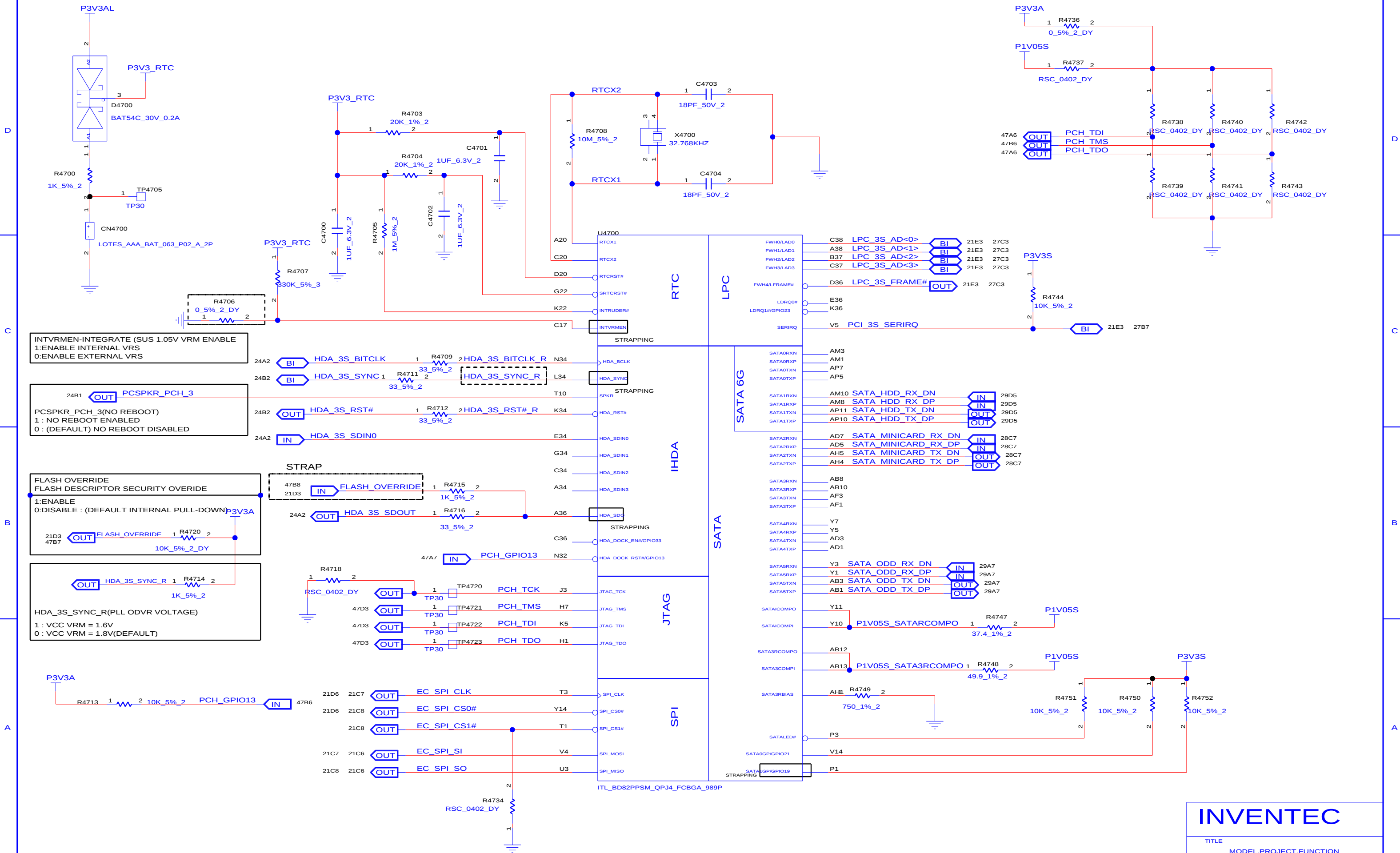


PEG STATIC LANE REVERSAL	
CFG(2)	1 : (DEFAULT) NORMAL OPERATION 0 : LANE REVERSED
LOW EDP ENABLE	
CFG(4)	1 : (DEFAULT) EDP DISABLED 0 : EDP ENABLED
PEG DEFER TRAINING	
CFG(7)	1 : (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DE ASSERTION 0 : PEG WAIT FOR BIOS FOR TRAINING
PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11 : (DEFAULT) X16 - DEVICE 1 FUNCTION AND 2 DISABLED 10 : X8, X8 - DEVICE 1 FUNCTION 1 ENABLE ; FUNCTION 2 DISABLED 01 : RESERVED - (DEVICE 1 FUNCTION 1 DISABLED ; FUNCTION 2 ENABLED) 00 : X8,X4,X4 - DEVICE 1 FUNCTION 1 AND 2 ENABLED

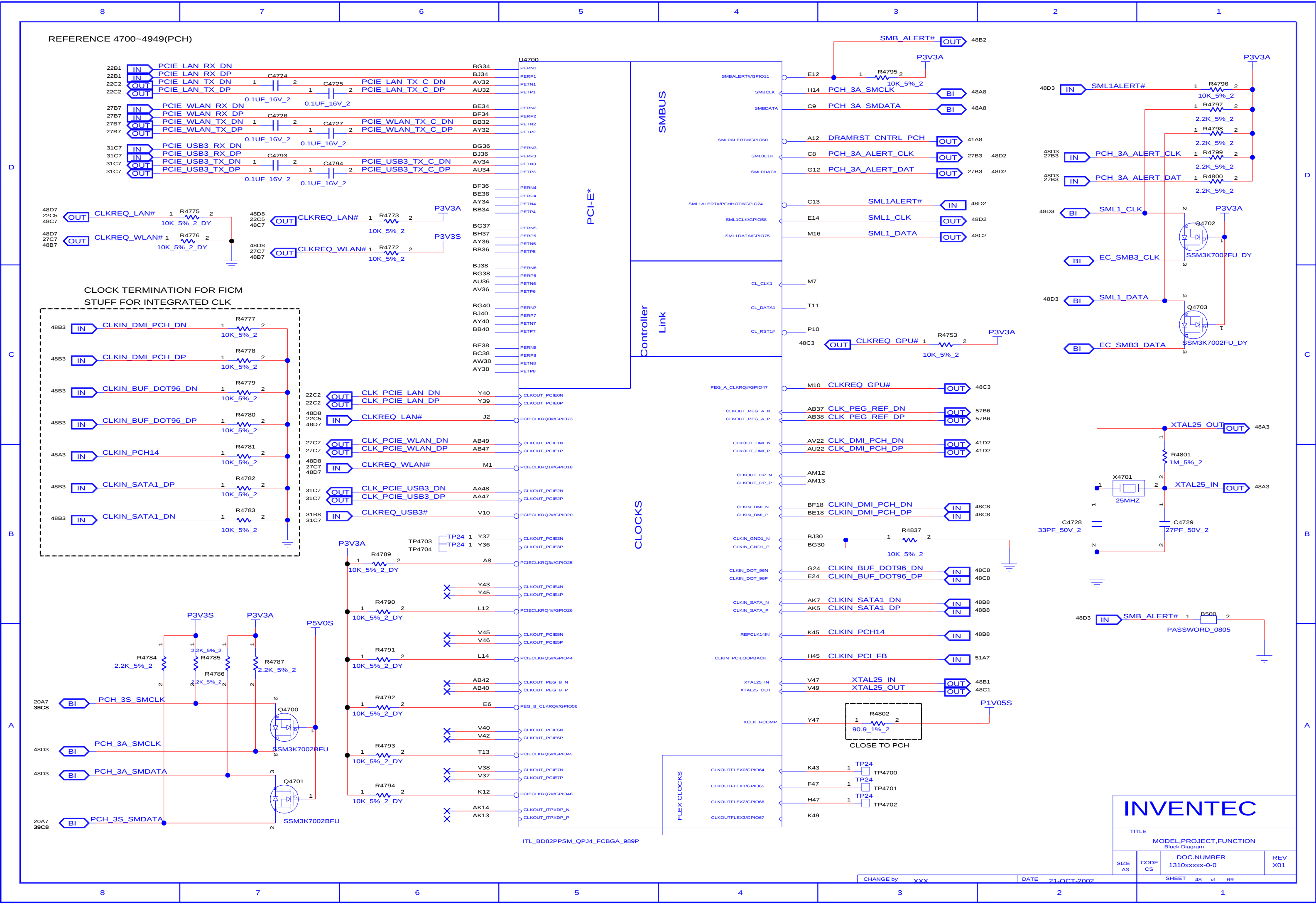
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 46 of 69			

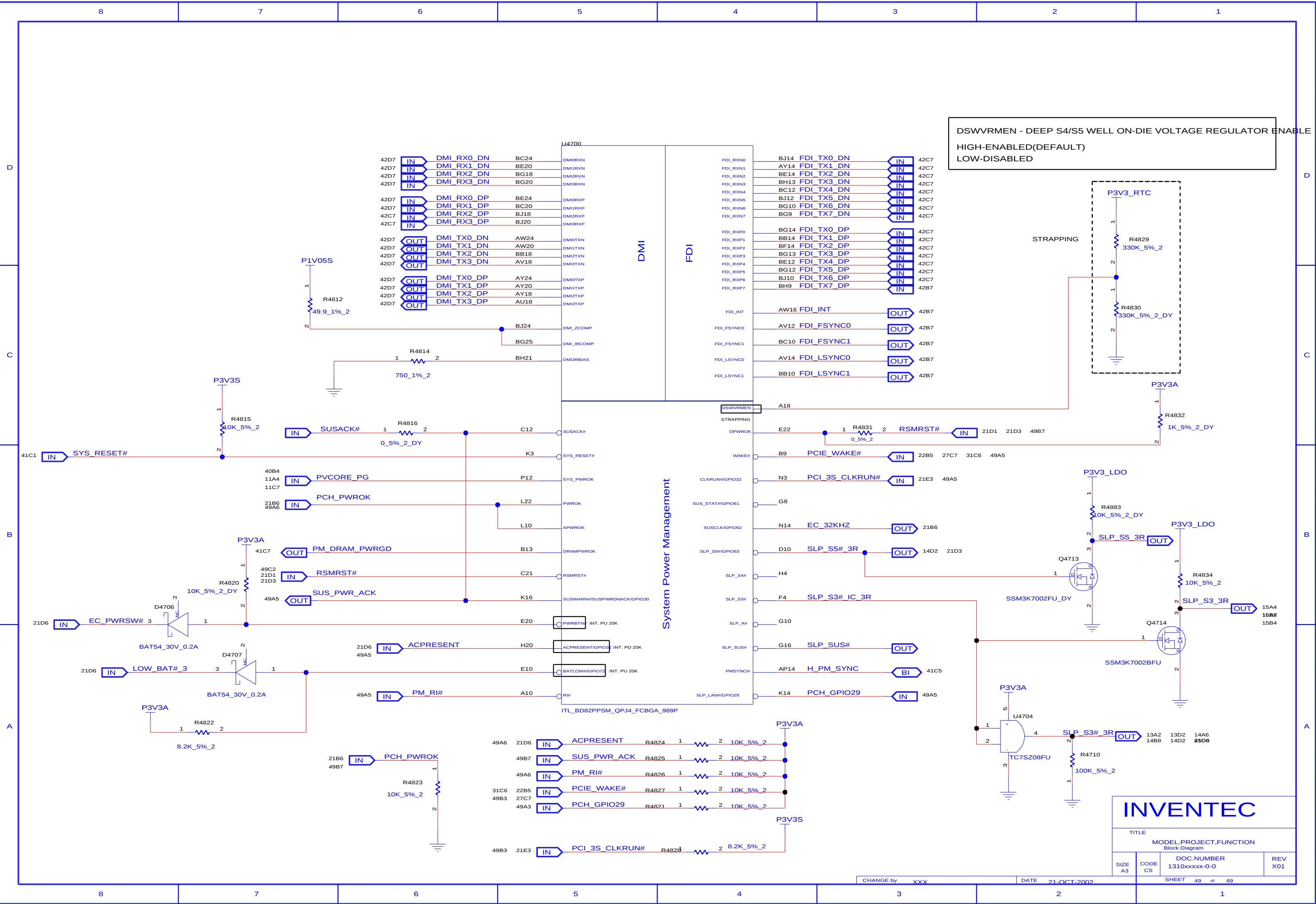
CHANGE by XXX DATE 21-OCT-2002

REFERENCE 4700~4949(PCH)



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 47 of 69			

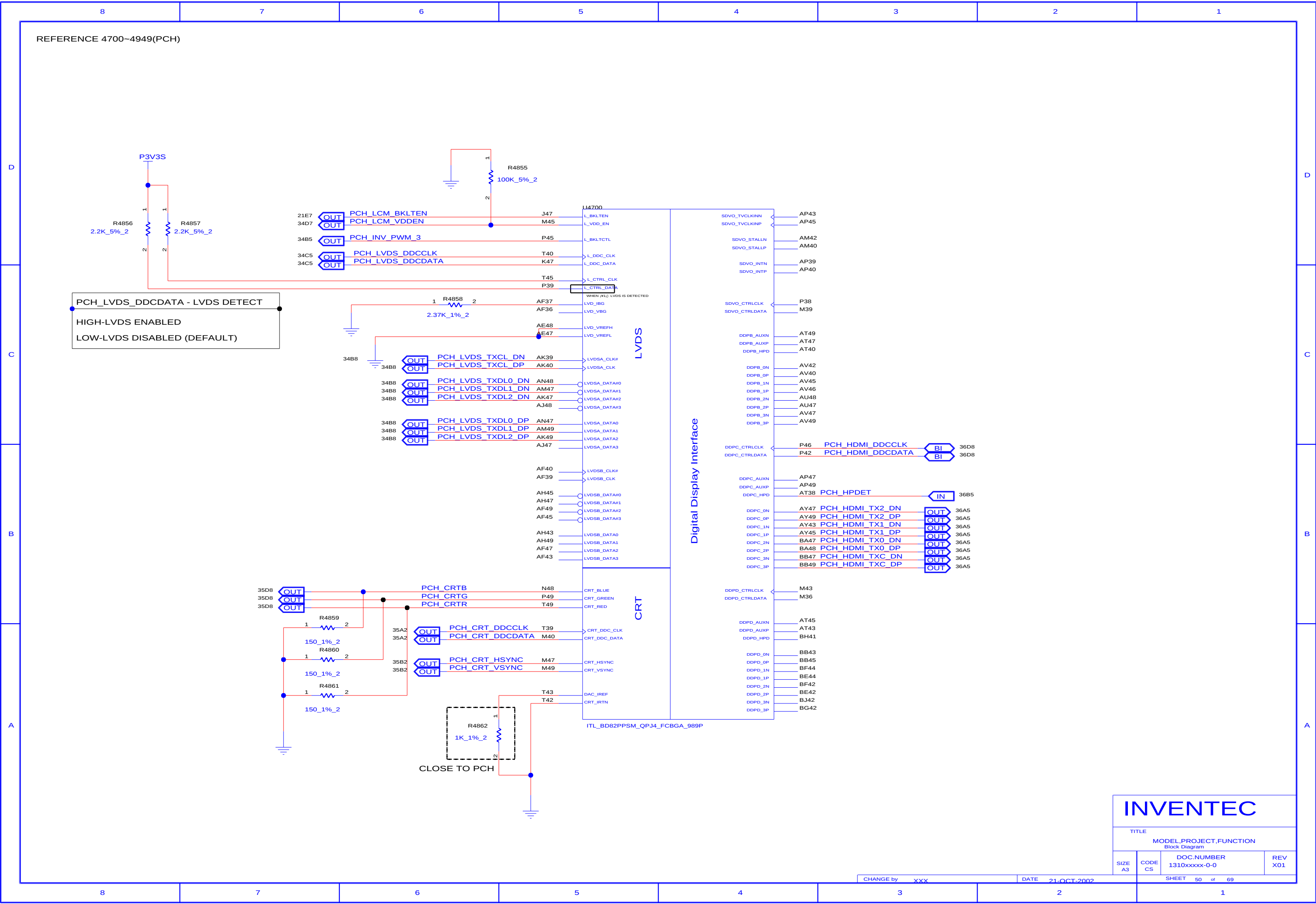


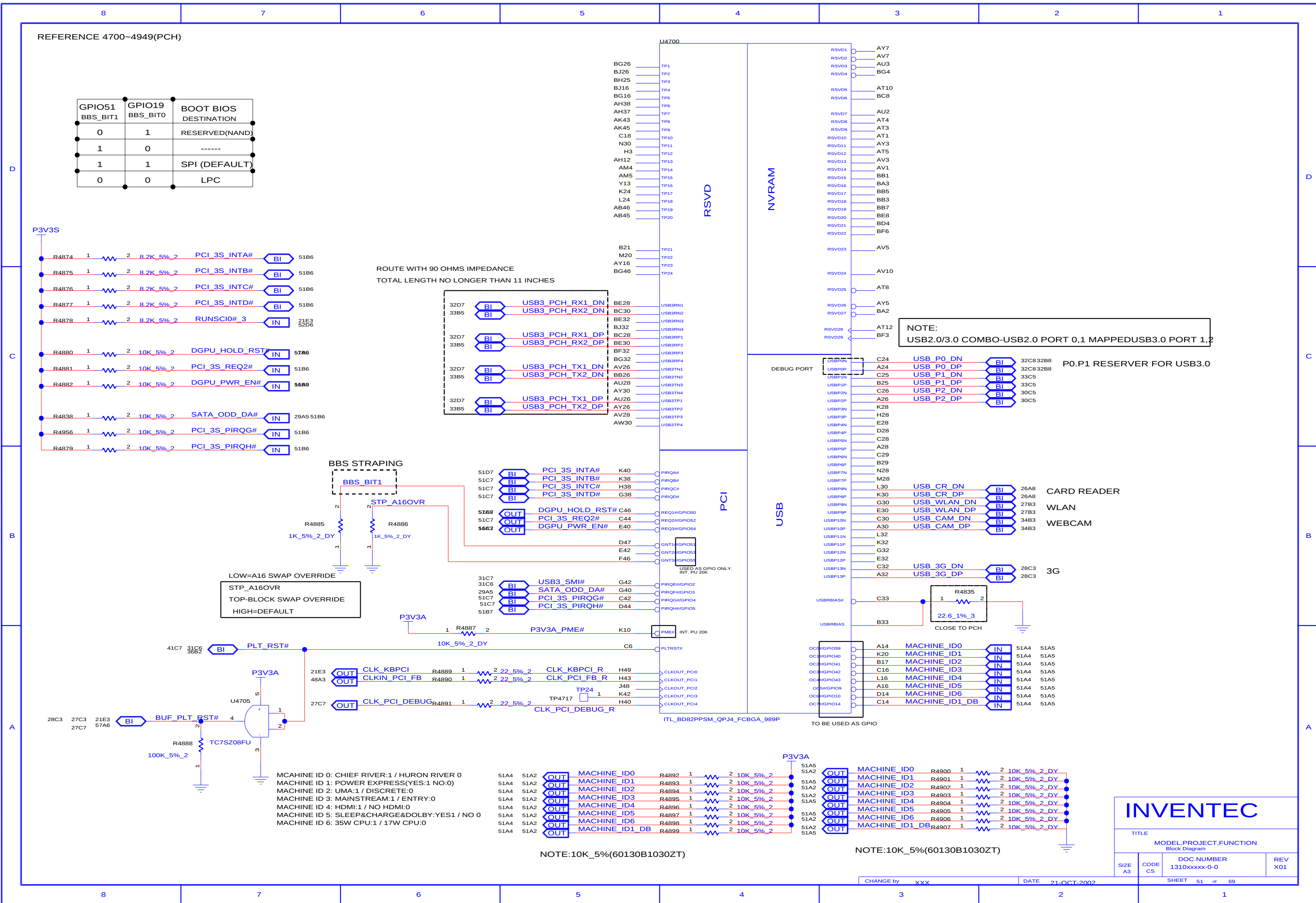


DSWVRMEN - DEEP S4/S5 WELL ON-DIE VOLTAGE REGULATOR ENABLE
HIGH-ENABLED(DEFAULT)
LOW-DISABLED

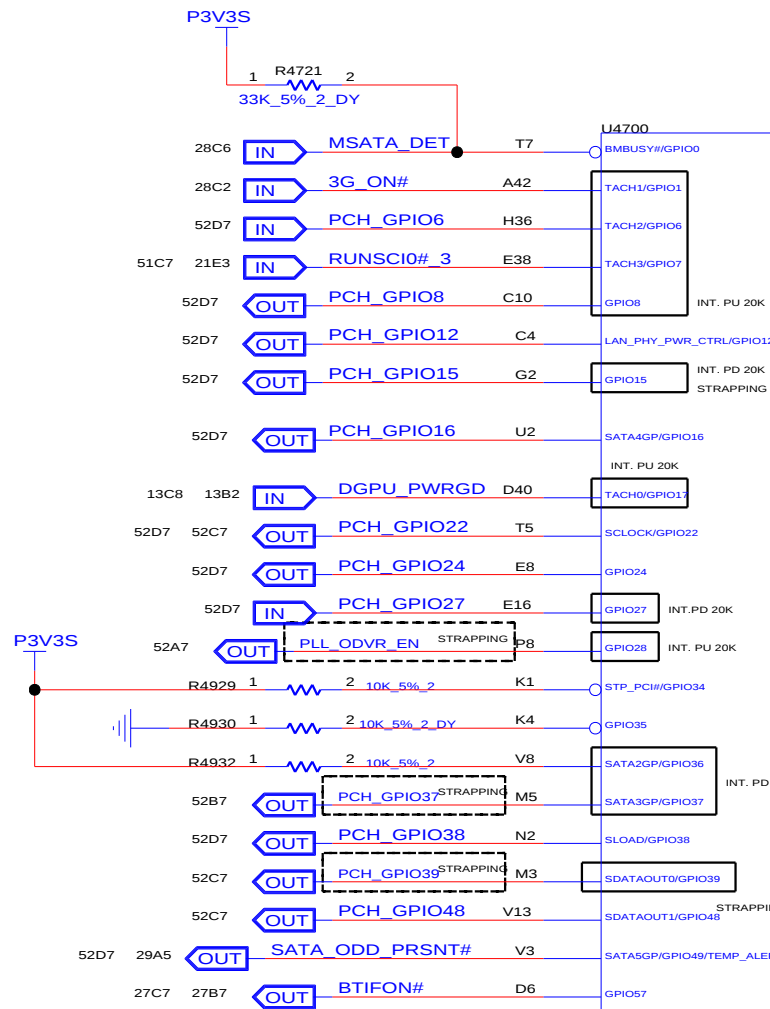
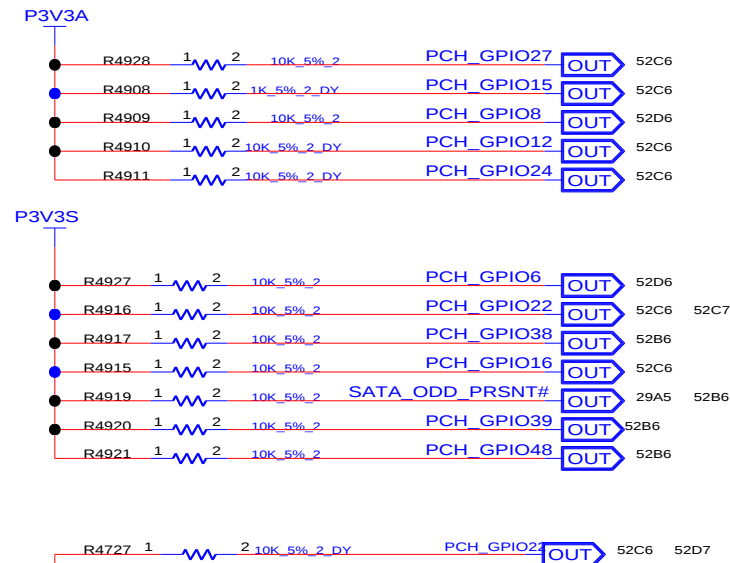
INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01





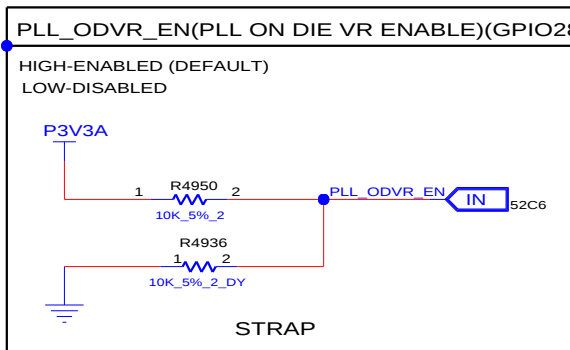
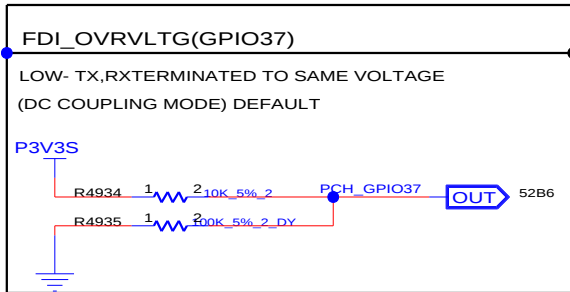
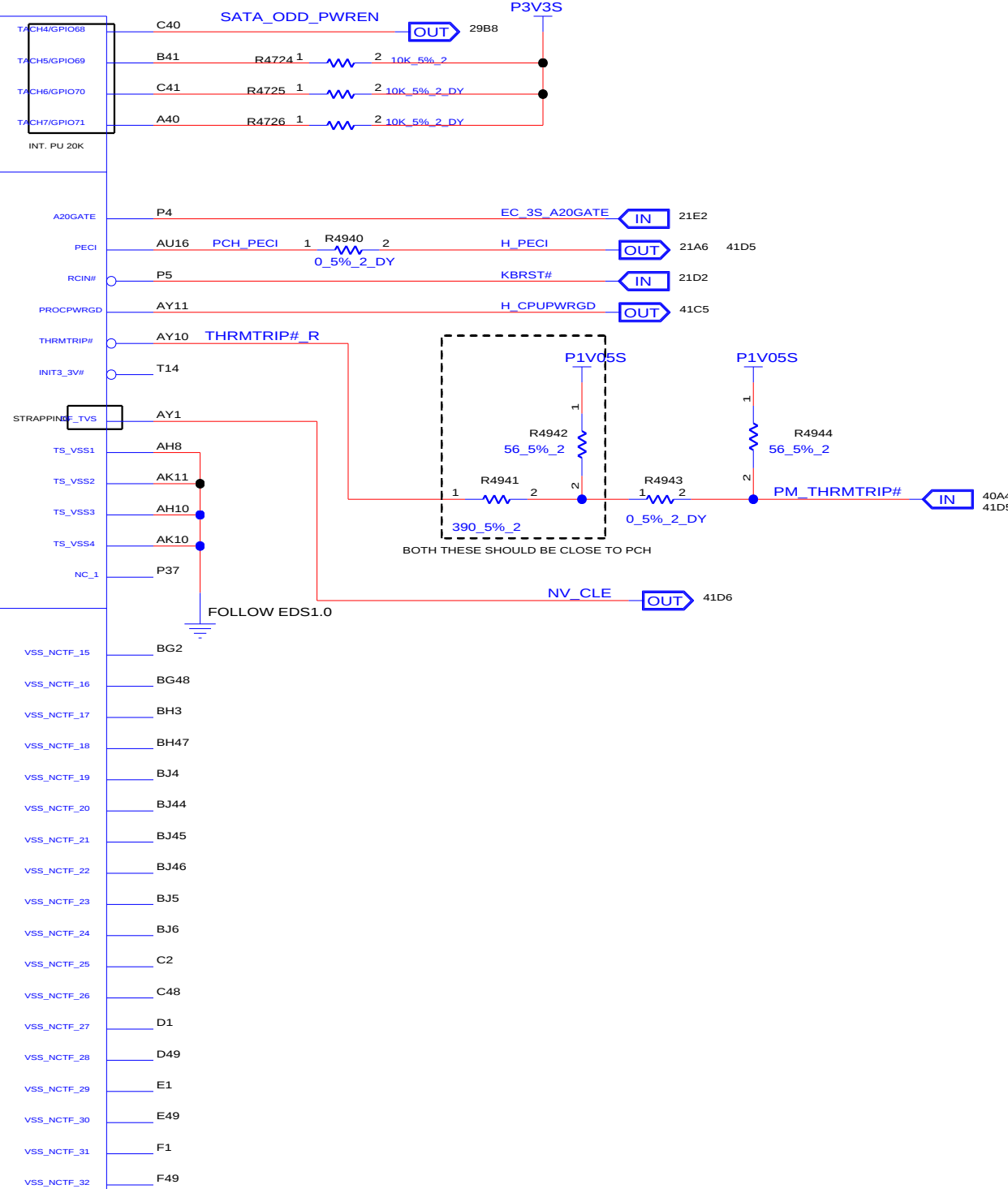
REFERENCE 4700~4949(PCH)



GPIO

CPU/MISC

NCTF

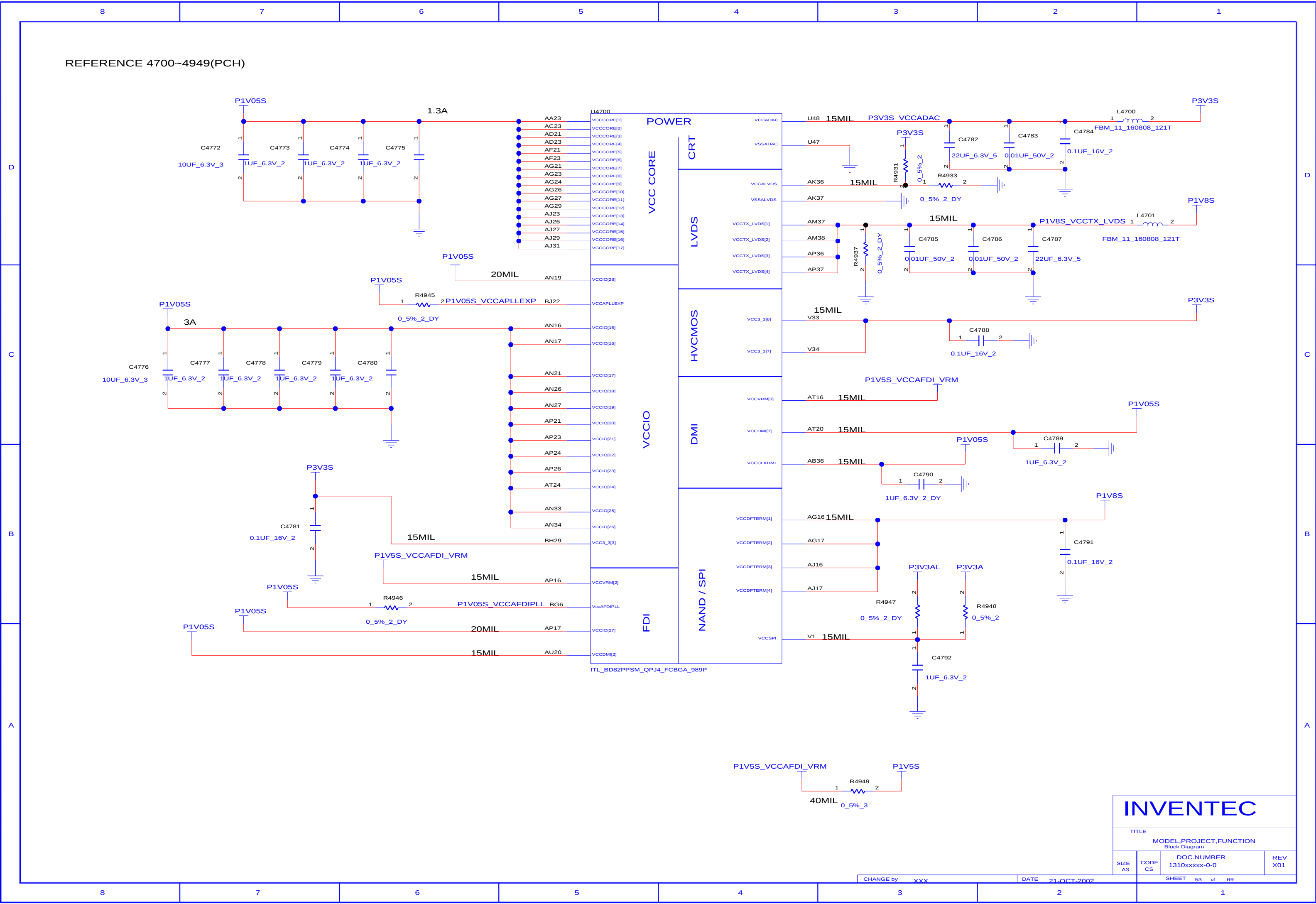


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21.OCT-2002 SHEET 52 of 69

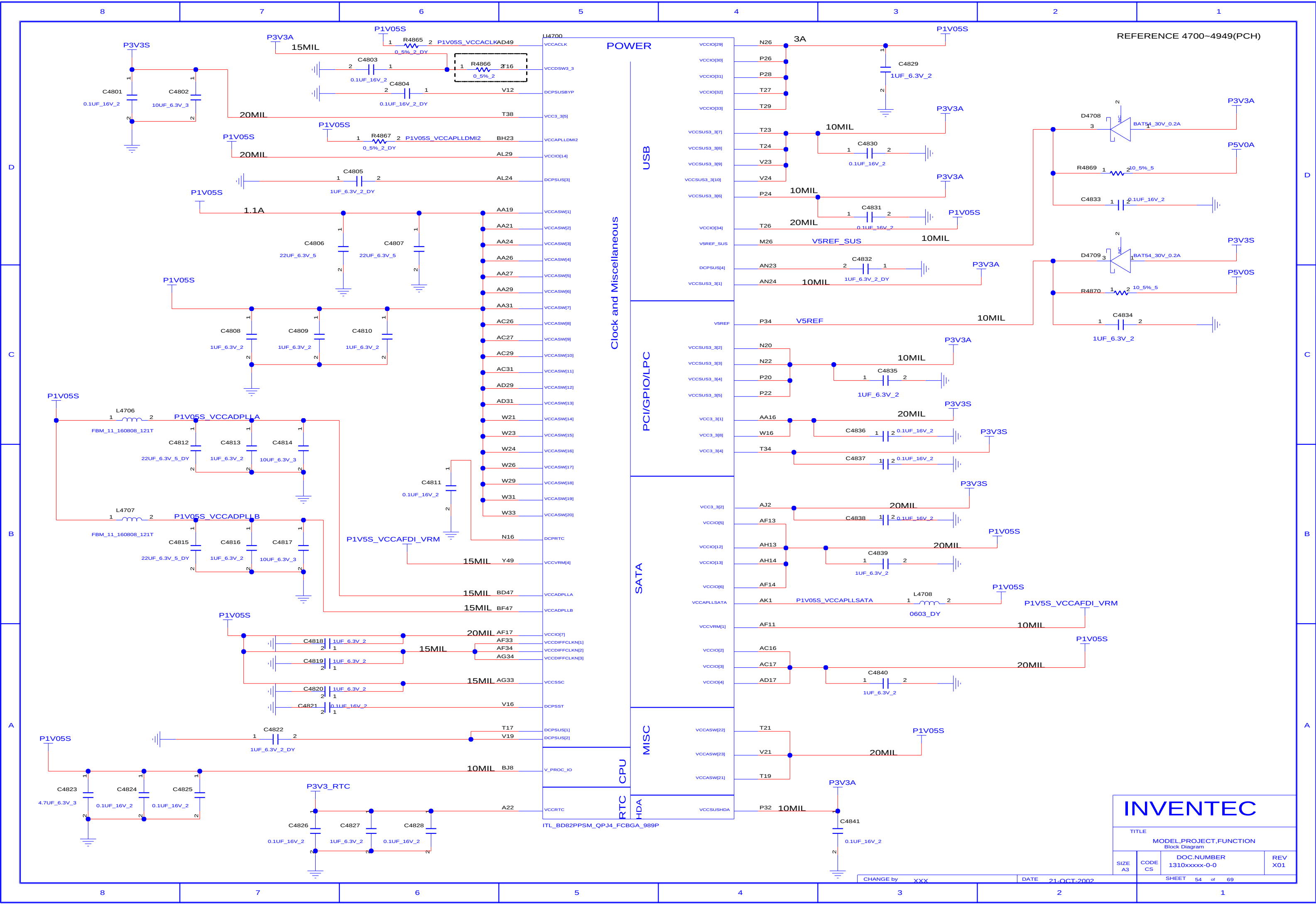


INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
------------	------------	----------------------------	------------

CHANGE by XXX DATE 21-OCT-2002 SHEET 53 of 69

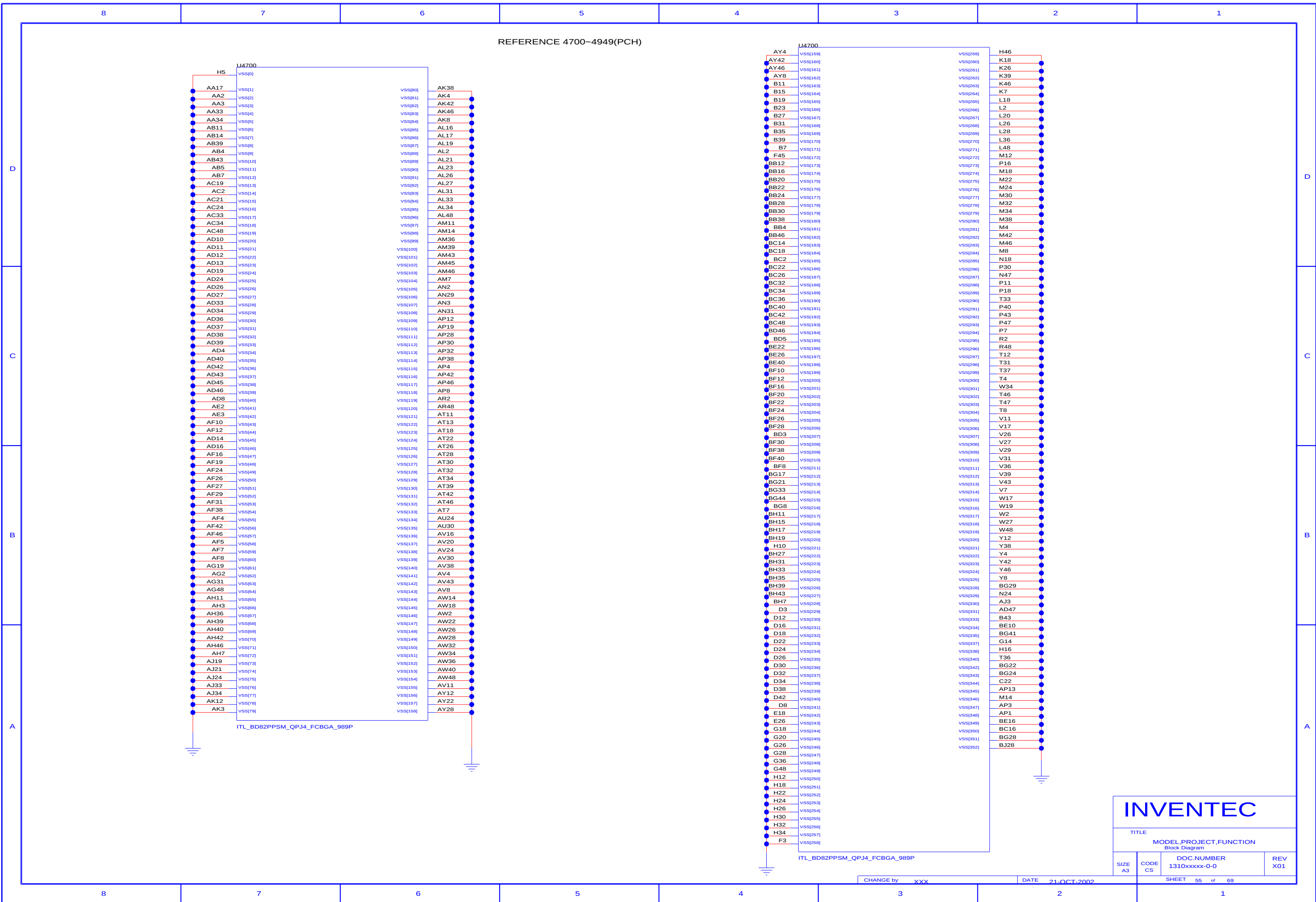


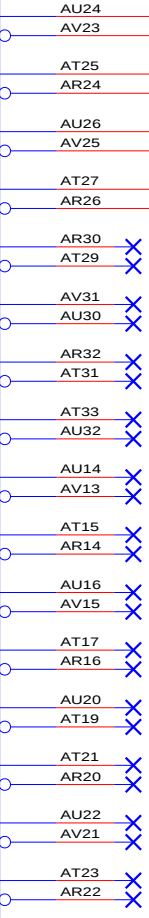
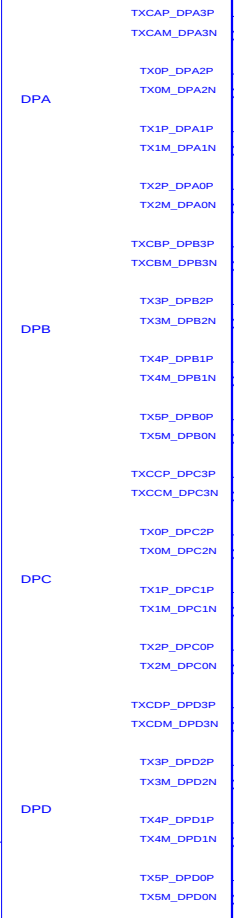
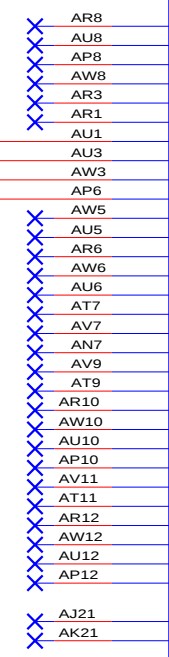
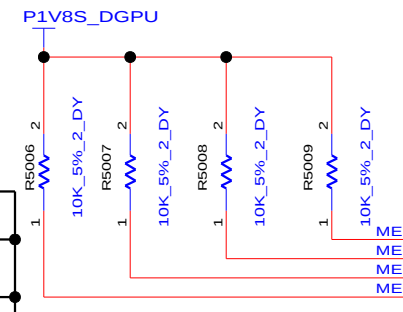
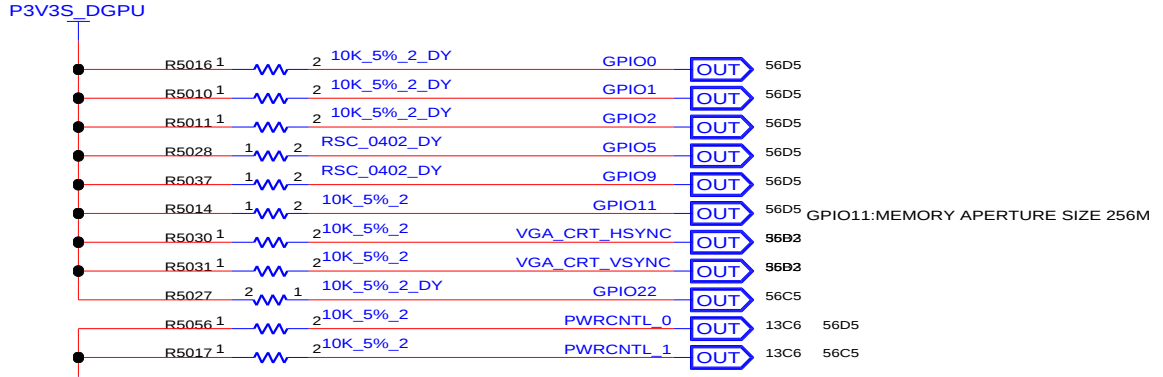
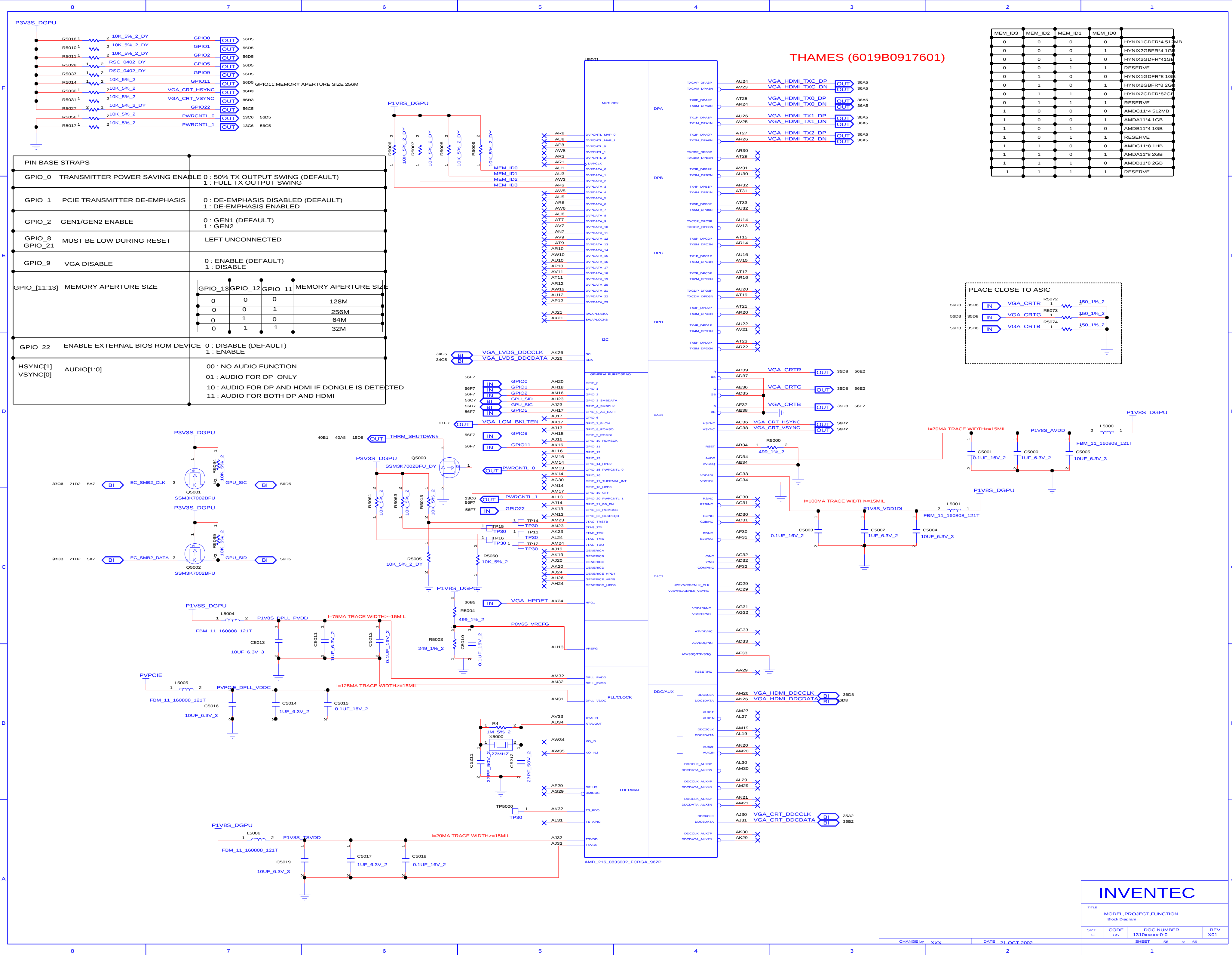
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 54 of 69

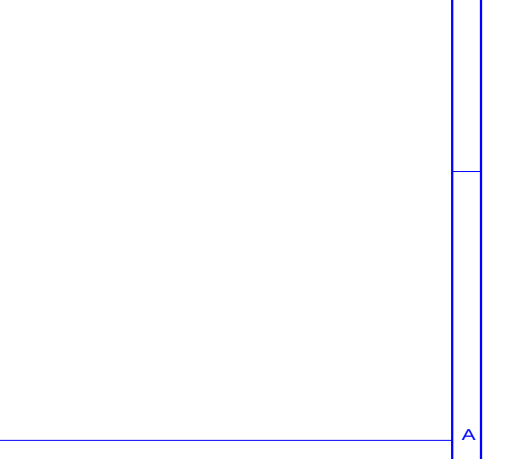
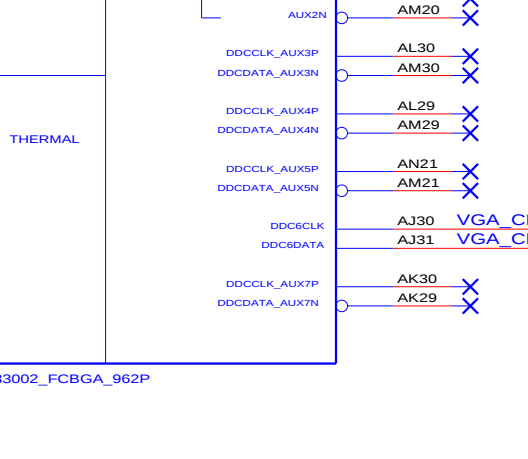
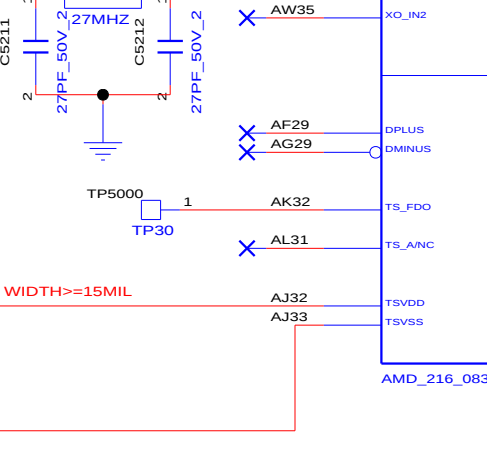
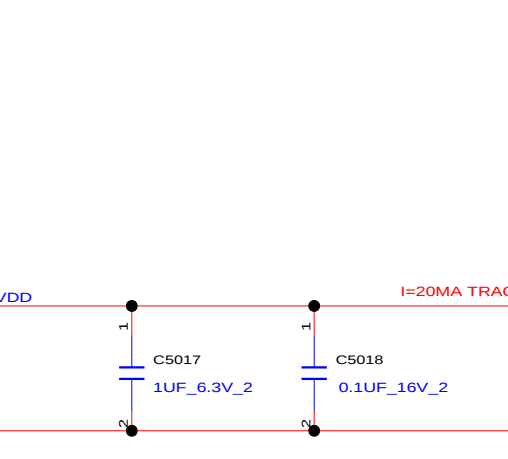
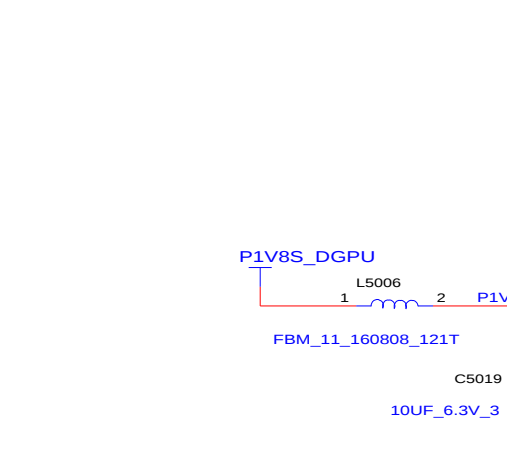
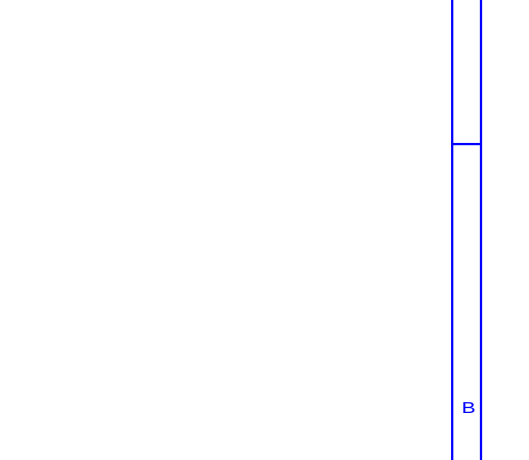
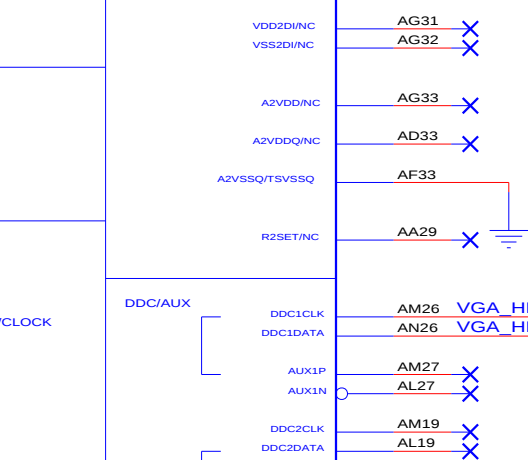
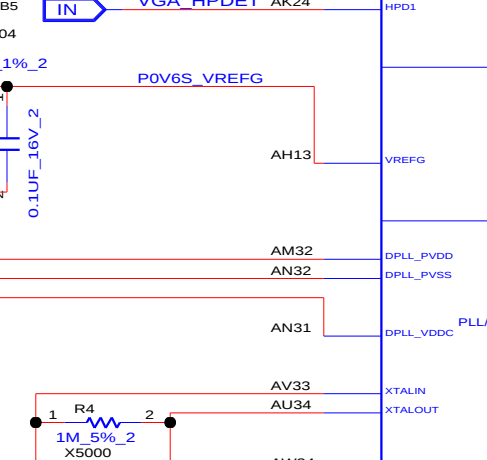
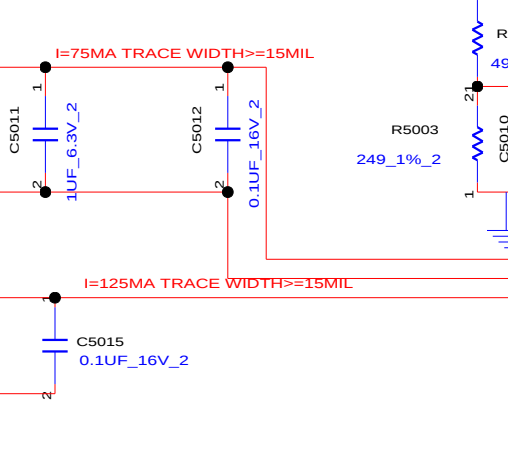
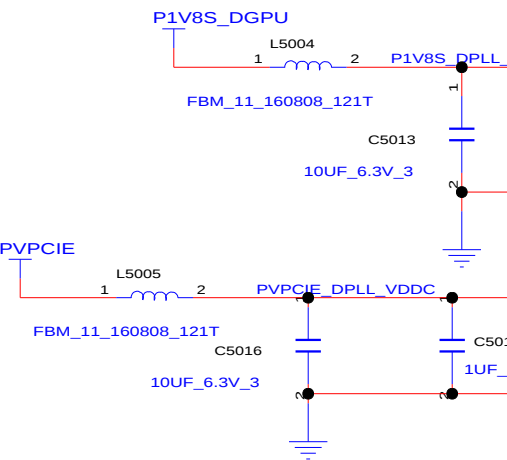
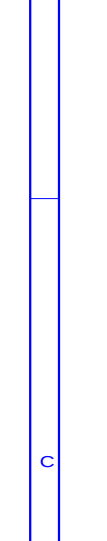
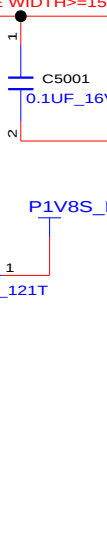
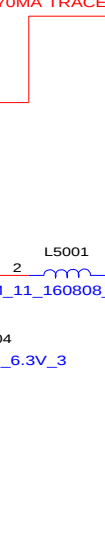
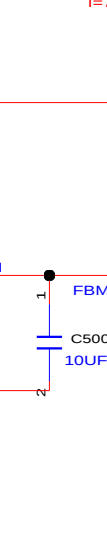
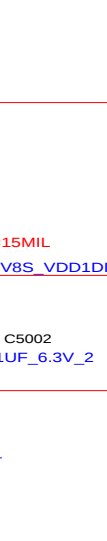
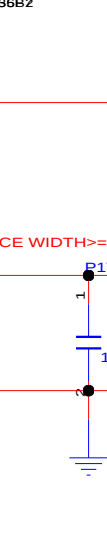
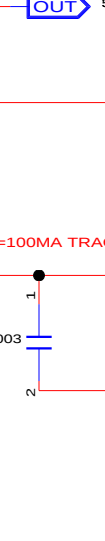
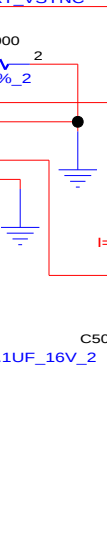
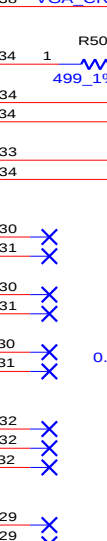
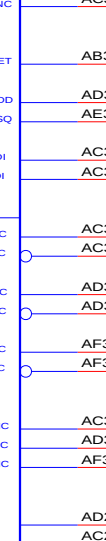
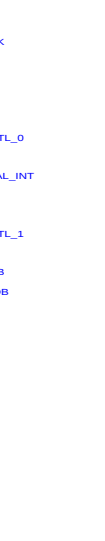
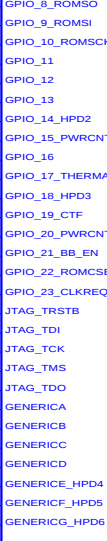
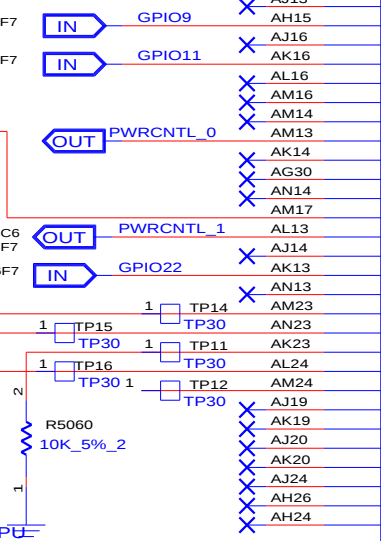
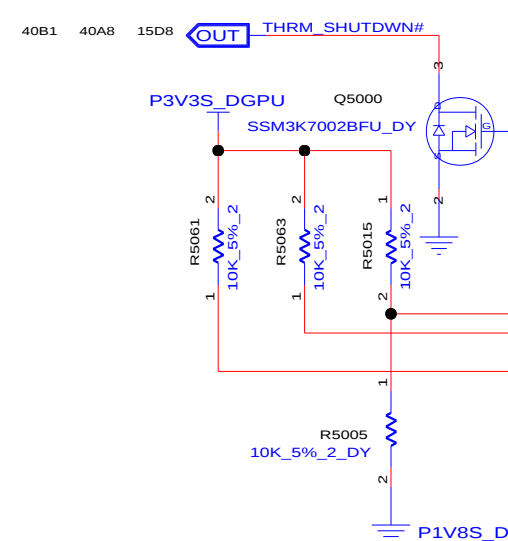
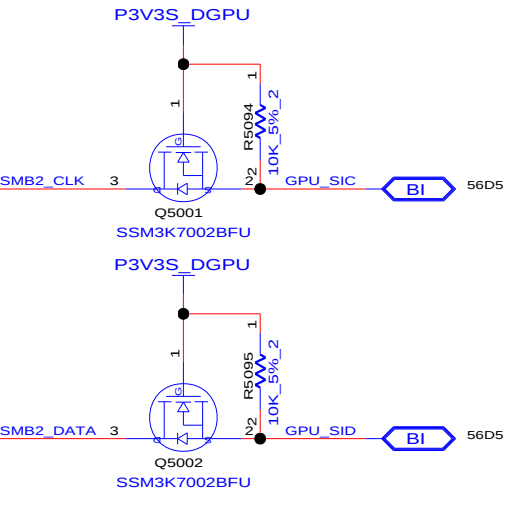
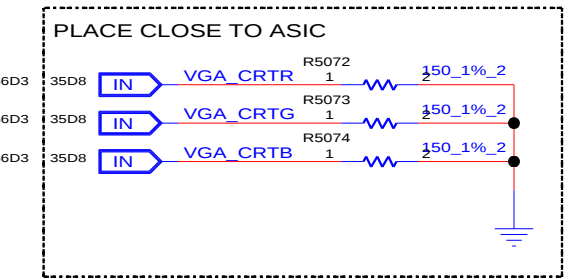




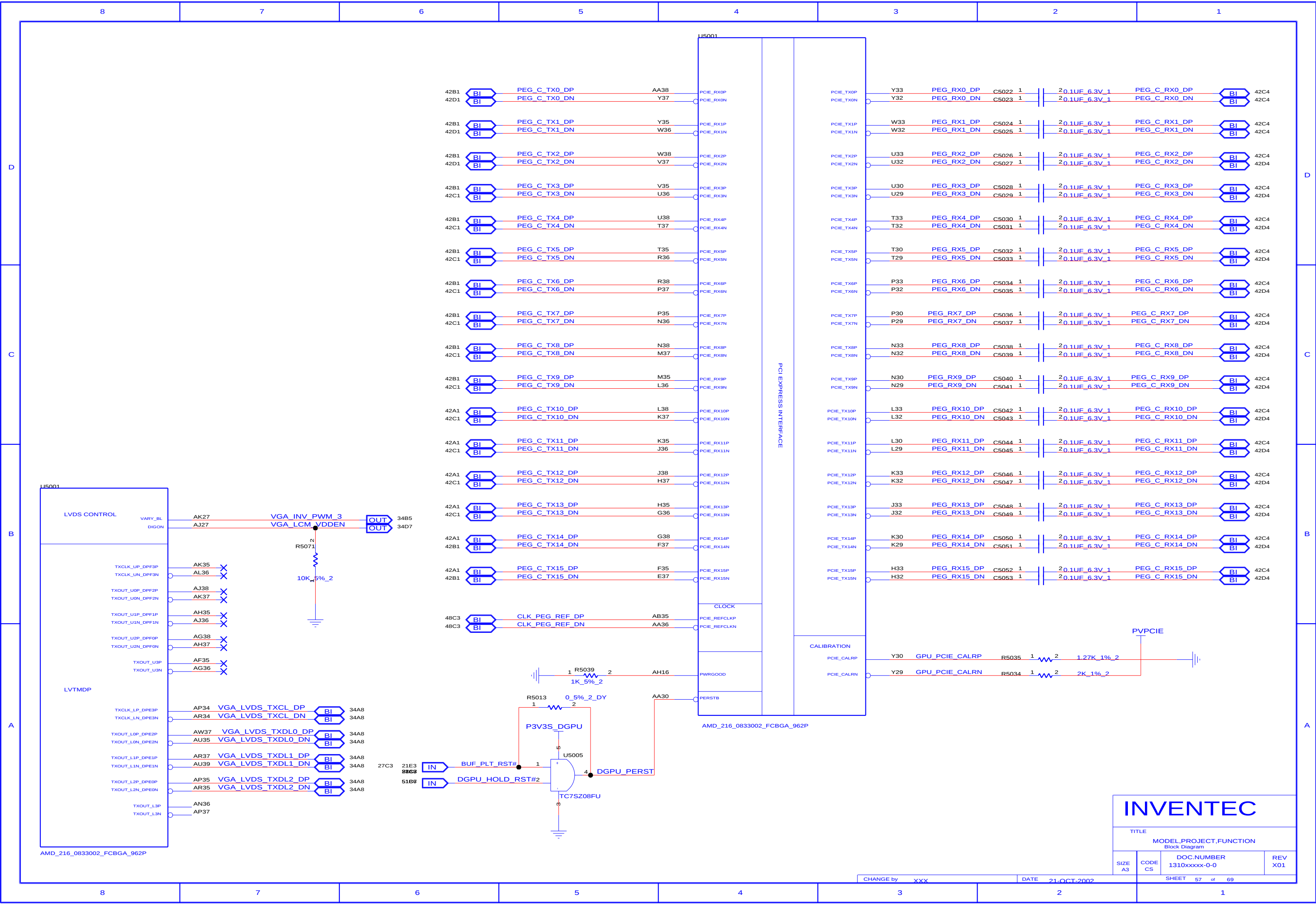
PIN BASE STRAPS																							
GPIO_0	TRANSMITTER POWER SAVING ENABLE	0 : 50% TX OUTPUT SWING (DEFAULT) 1 : FULL TX OUTPUT SWING																					
GPIO_1	PCIE TRANSMITTER DE-EMPHASIS	0 : DE-EMPHASIS DISABLED (DEFAULT) 1 : DE-EMPHASIS ENABLED																					
GPIO_2	GEN1/GEN2 ENABLE	0 : GEN1 (DEFAULT) 1 : GEN2																					
GPIO_8 GPIO_21	MUST BE LOW DURING RESET	LEFT UNCONNECTED																					
GPIO_9	VGA DISABLE	0 : ENABLE (DEFAULT) 1 : DISABLE																					
GPIO_[11:13]	MEMORY APERTURE SIZE	<table><thead><tr><th>GPIO_13</th><th>GPIO_12</th><th>GPIO_11</th><th>MEMORY APERTURE SIZE</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>128M</td></tr><tr><td>0</td><td>0</td><td>1</td><td>256M</td></tr><tr><td>0</td><td>1</td><td>0</td><td>64M</td></tr><tr><td>0</td><td>1</td><td>1</td><td>32M</td></tr></tbody></table>	GPIO_13	GPIO_12	GPIO_11	MEMORY APERTURE SIZE	0	0	0	128M	0	0	1	256M	0	1	0	64M	0	1	1	32M	
GPIO_13	GPIO_12	GPIO_11	MEMORY APERTURE SIZE																				
0	0	0	128M																				
0	0	1	256M																				
0	1	0	64M																				
0	1	1	32M																				
GPIO_22	ENABLE EXTERNAL BIOS ROM DEVICE	0 : DISABLE (DEFAULT) 1 : ENABLE																					
HSYNC[1] VSYNC[0]	AUDIO[1:0]	00 : NO AUDIO FUNCTION 01 : AUDIO FOR DP ONLY 10 : AUDIO FOR DP AND HDMI IF DONGLE IS DETECTED 11 : AUDIO FOR BOTH DP AND HDMI																					

THAMES (6019B0917601)

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	
0	0	0	0	HYNIX1GDFR*4 512MB
0	0	0	1	HYNIX2GBFR*4 1GB
0	0	1	0	HYNIX2GBFR*4 1GB
0	0	1	1	RESERVE
0	1	0	0	HYNIX1GDFR*8 1GB
0	1	0	1	HYNIX2GBFR*8 2GB
0	1	1	0	HYNIX2GBFR*8 2GB
0	1	1	1	RESERVE
1	0	0	0	AMDC11*4 512MB
1	0	0	1	AMDA11*4 1GB
1	0	1	0	AMDB11*4 1GB
1	0	1	1	RESERVE
1	1	0	0	AMDC11*8 1HB
1	1	0	1	AMDA11*8 2GB
1	1	1	0	AMDB11*8 2GB
1	1	1	1	RESERVE



INVENTEC			
TITLE MODEL_PROJECT,FUNCTION Block Diagram			
SIZE C	CODE CS	DOC NUMBER 1310XXXX-0-0	REV X01
CHANGE by xxx		DATE 21.OCT.2002	
SHEET 56 of 69		1	

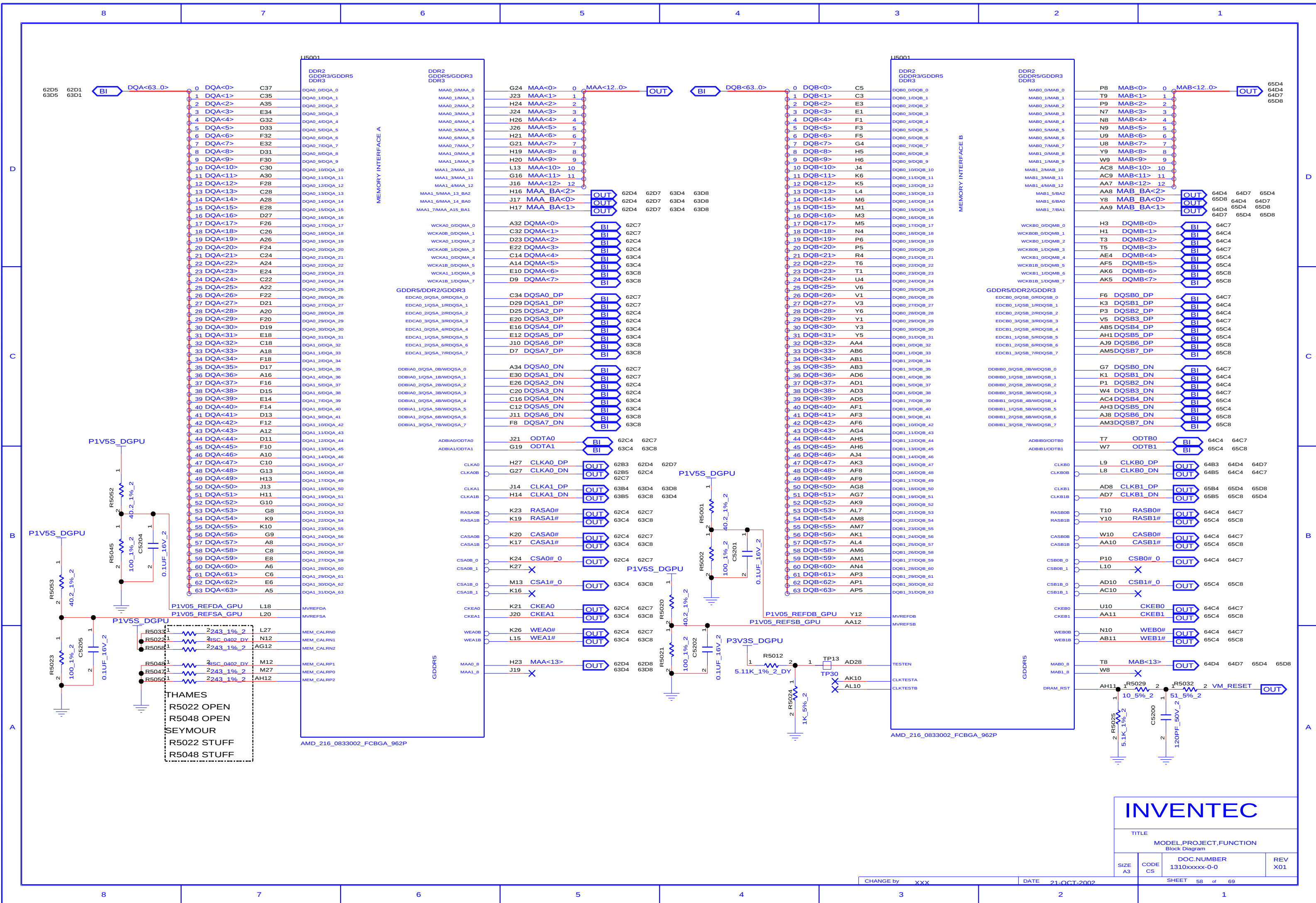


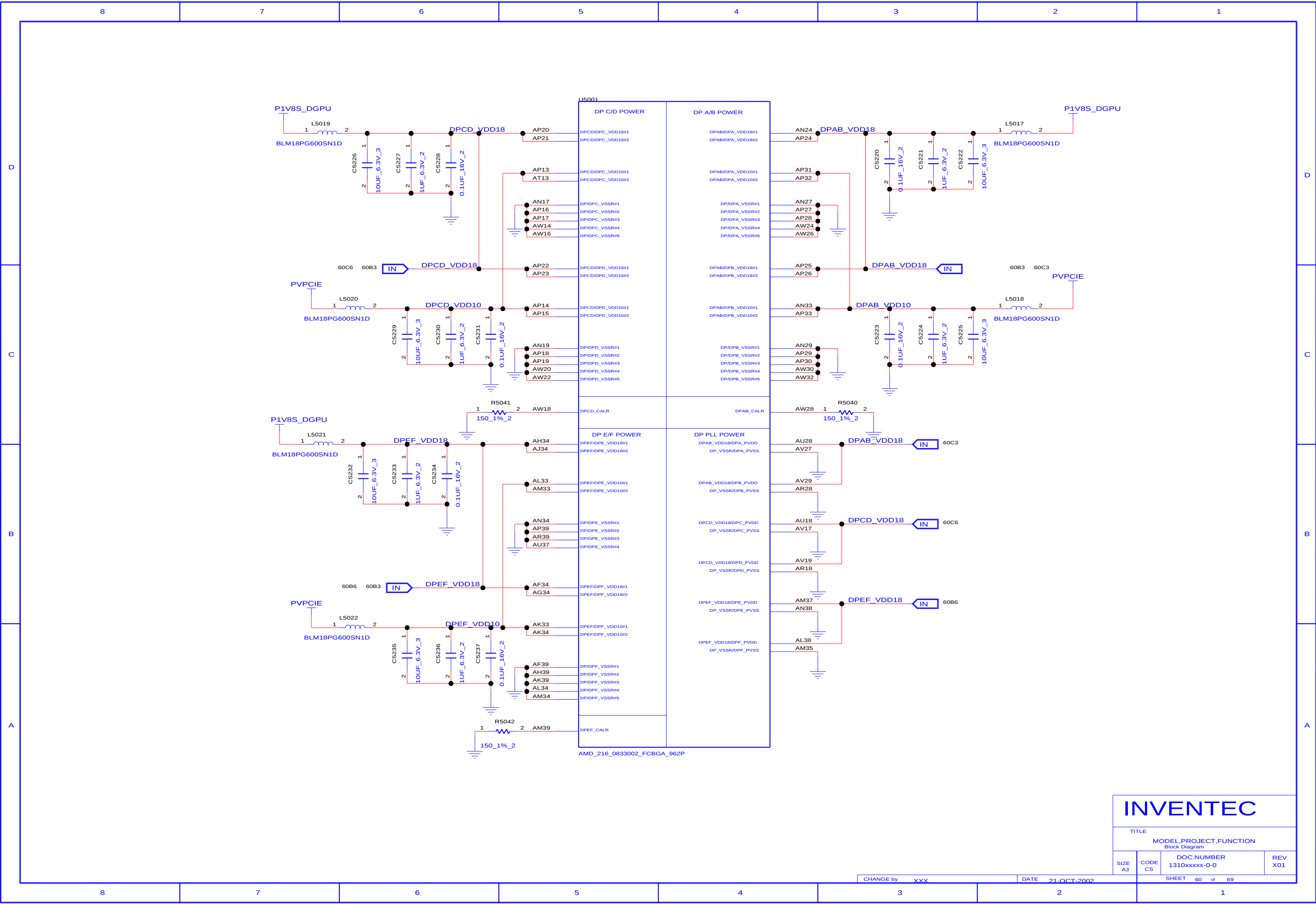
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

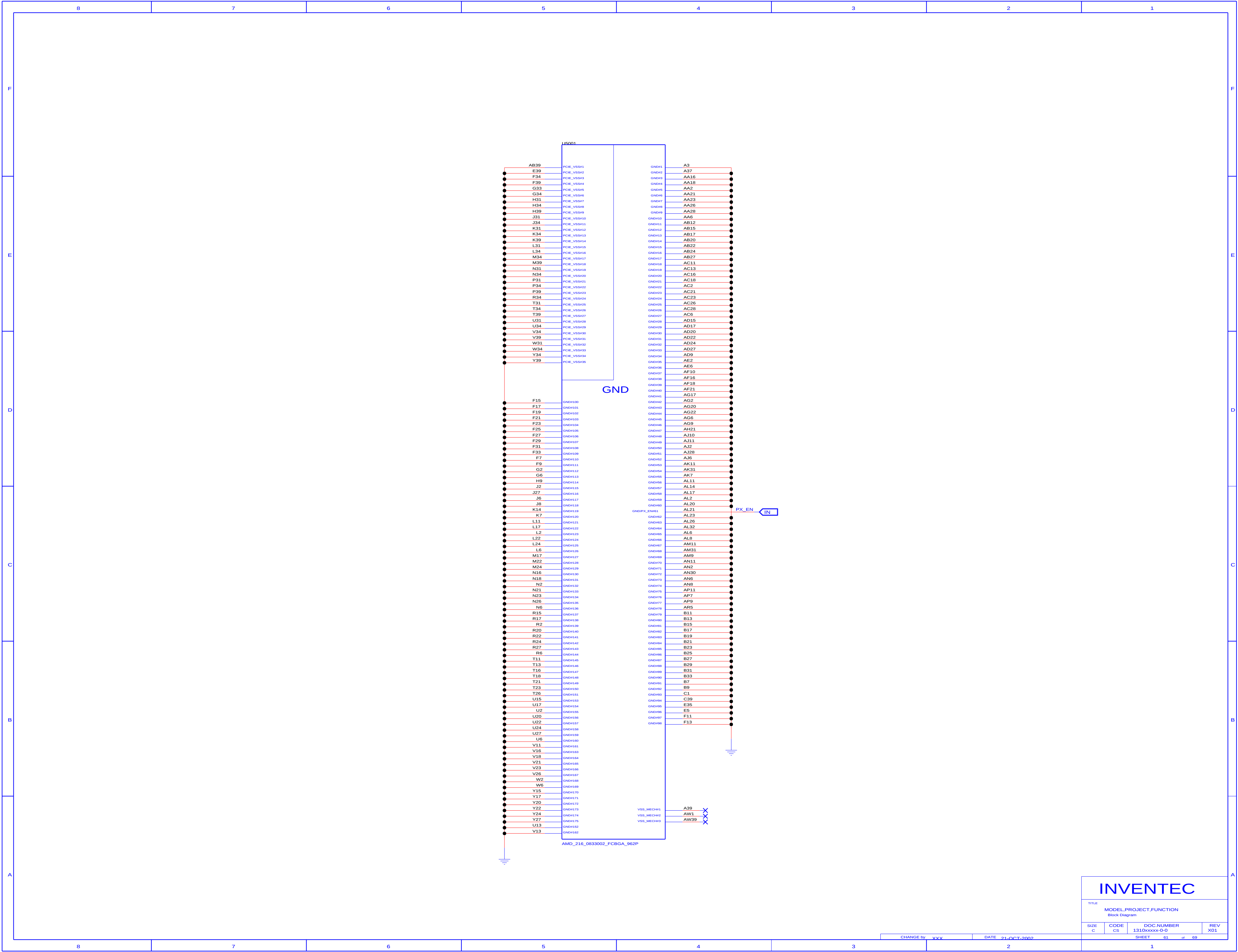
CHANGE by XXX DATE 21-OCT-2002 SHEET 57 of 69

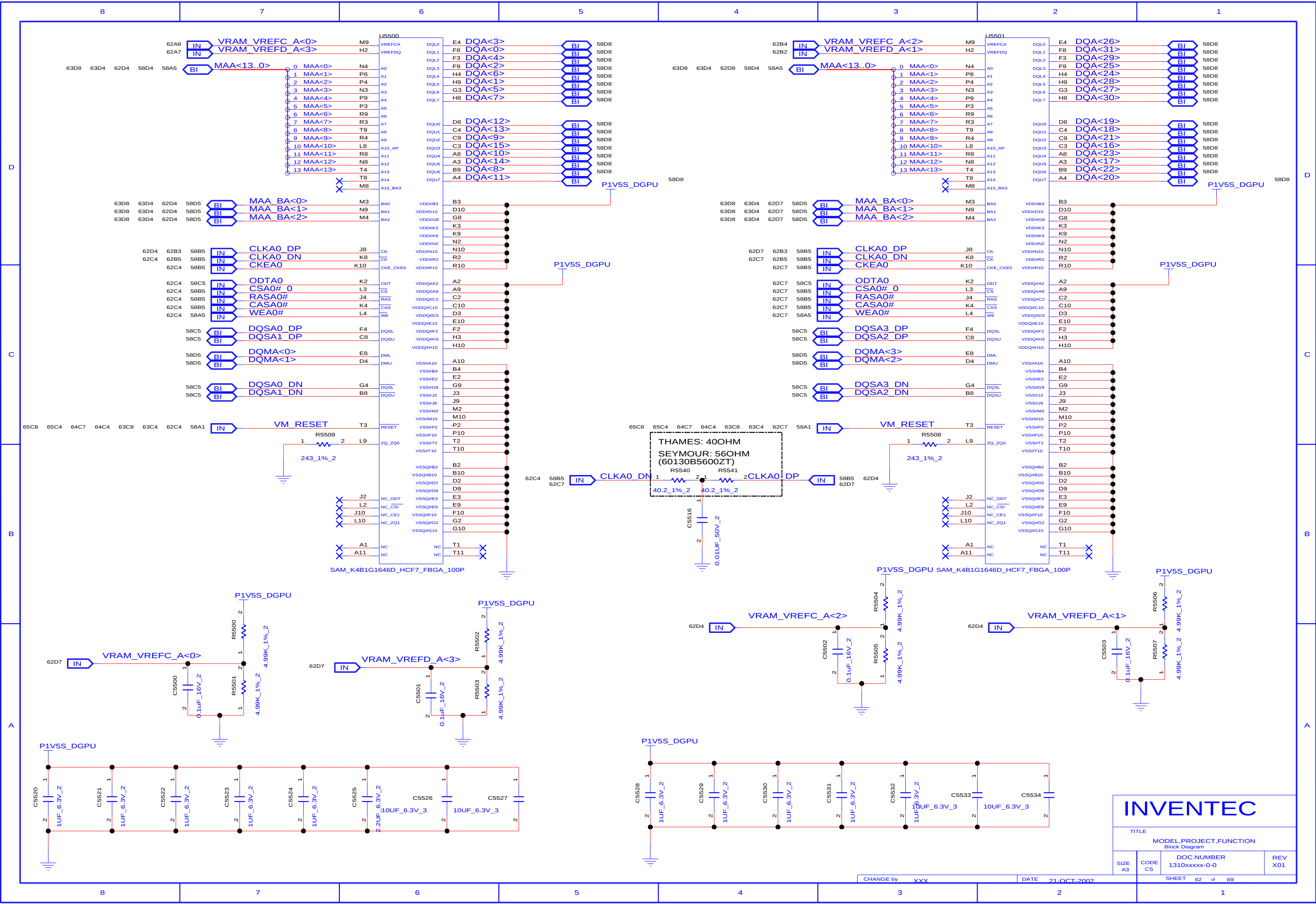




INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
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INVENTEC

TITLE

MODEL,PROJECT,FUNCTION
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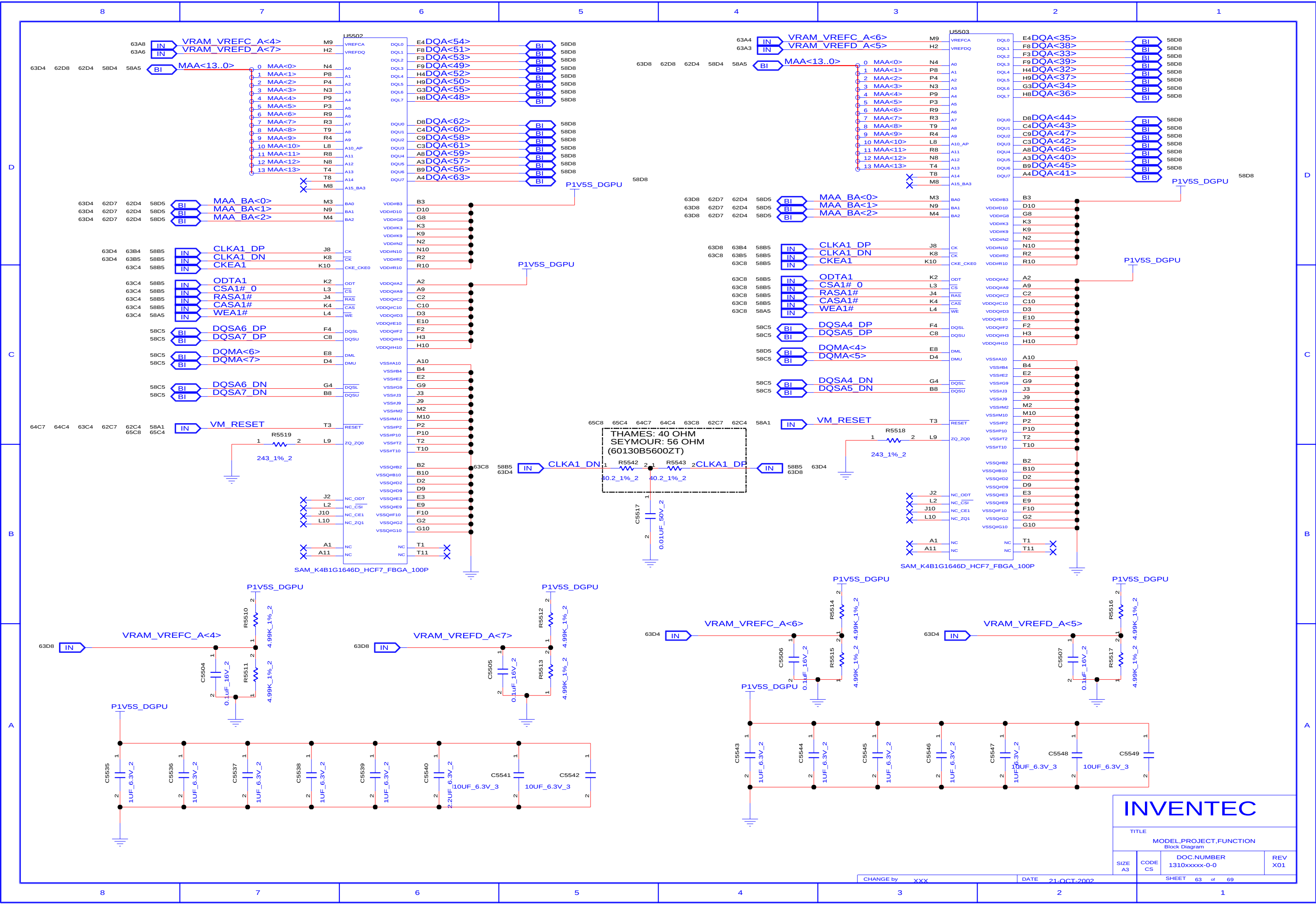
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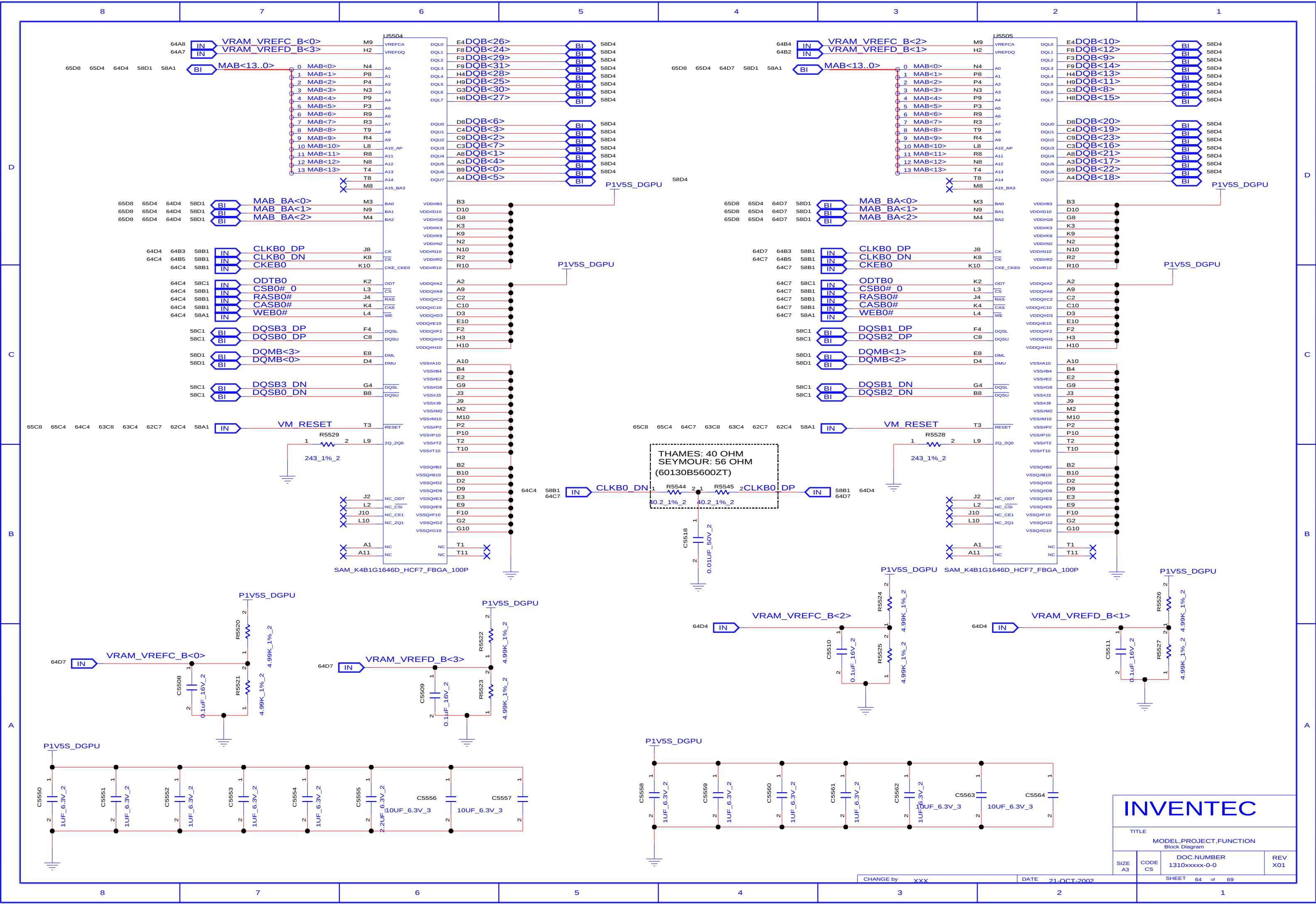
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1310xxxx-0-0

REV
X01

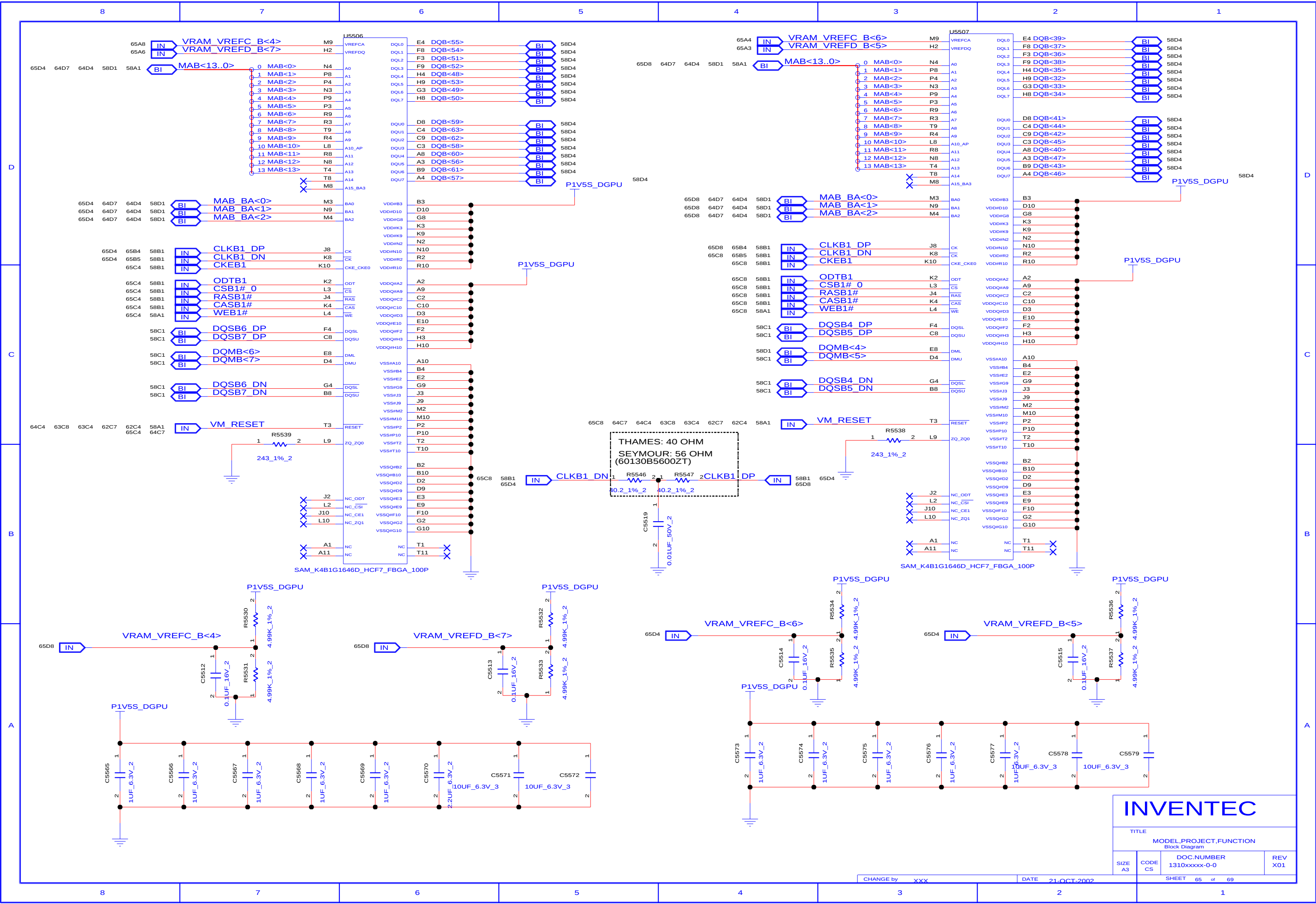
SHEET 62 of 69



INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION Block Diagram				
SIZE	CODE	DOC. NUMBER		REV
A3	CS	1310xxxx-0-0		X01
SHEET 63 of 69				



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01



INVENTEC

TITLE

MODEL,PROJECT,FUNCTION
Block Diagram

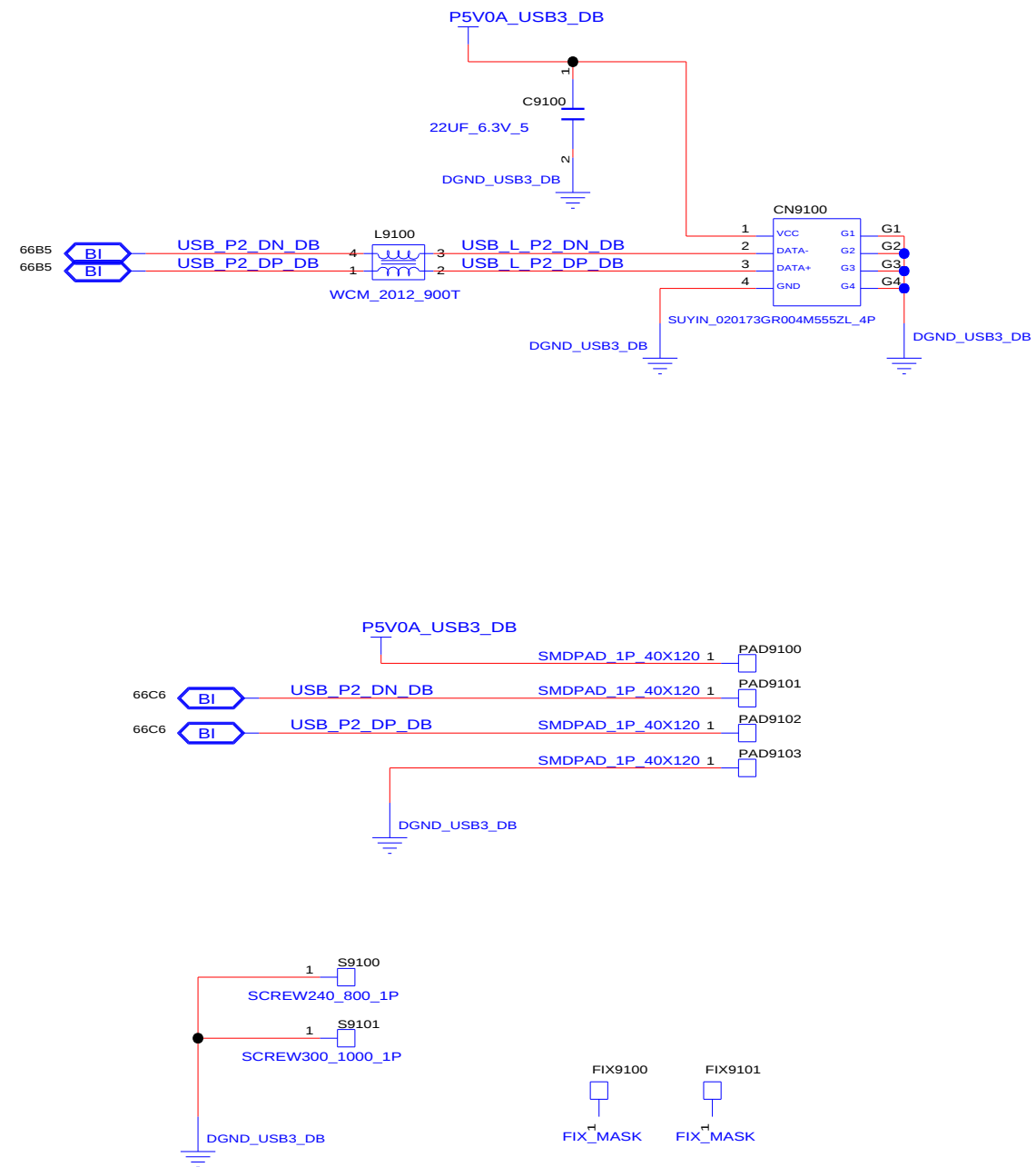
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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CHANGE by
XXX

DATE
21-OCT-2002

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USB BOARD



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

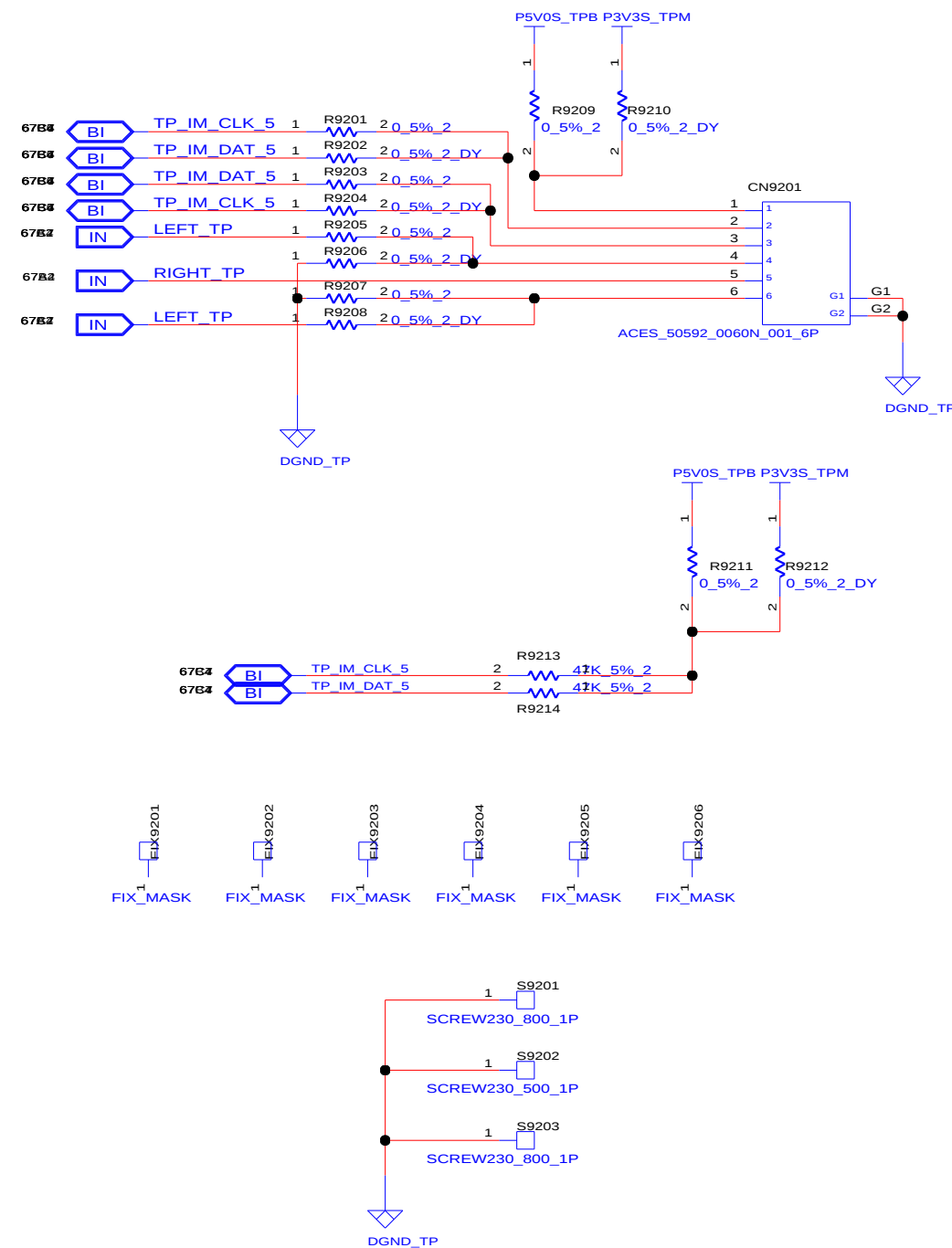
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CHANGE by XXX DATE 21-OCT-2002

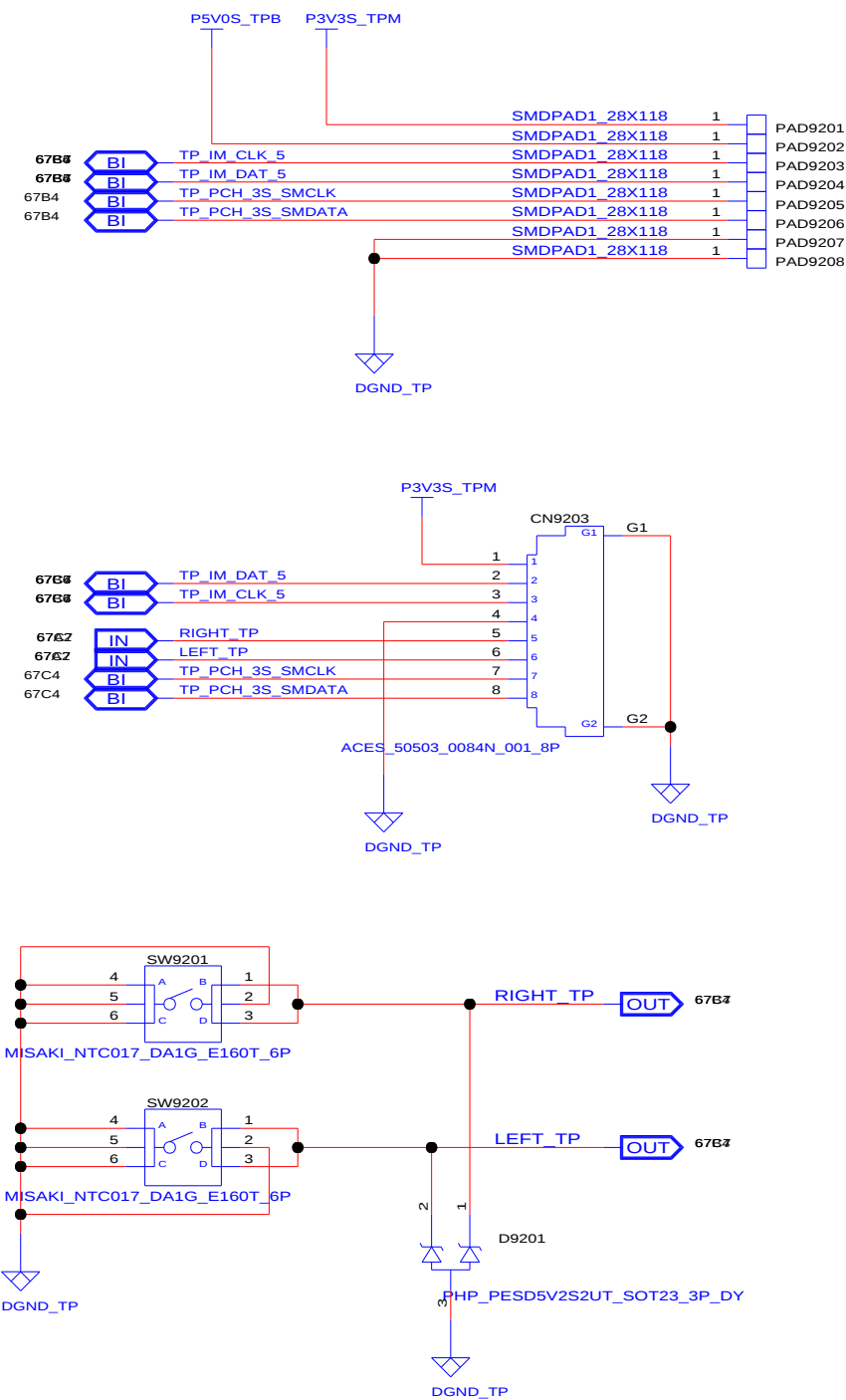
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TPUCH PAD BOARD

TOUCHPAD TO MODULE CONN



TOUCHPAD TO MB CONN



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

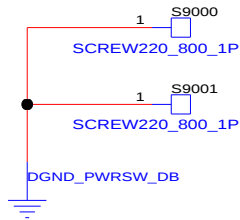
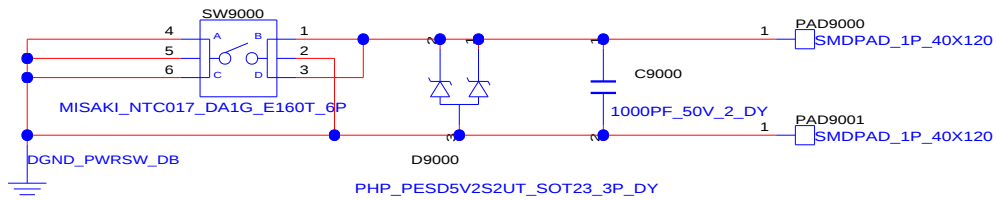
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CHANGE by XXX DATE 21-OCT-2002

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REFERENCE 9000~9999(SMALL BOARD)

POWER BUTTON



INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX DATE 21-OCT-2002 SHEET 68 of 69			

