

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking

TV_OUT
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

PG 31

VAULE DEFINE

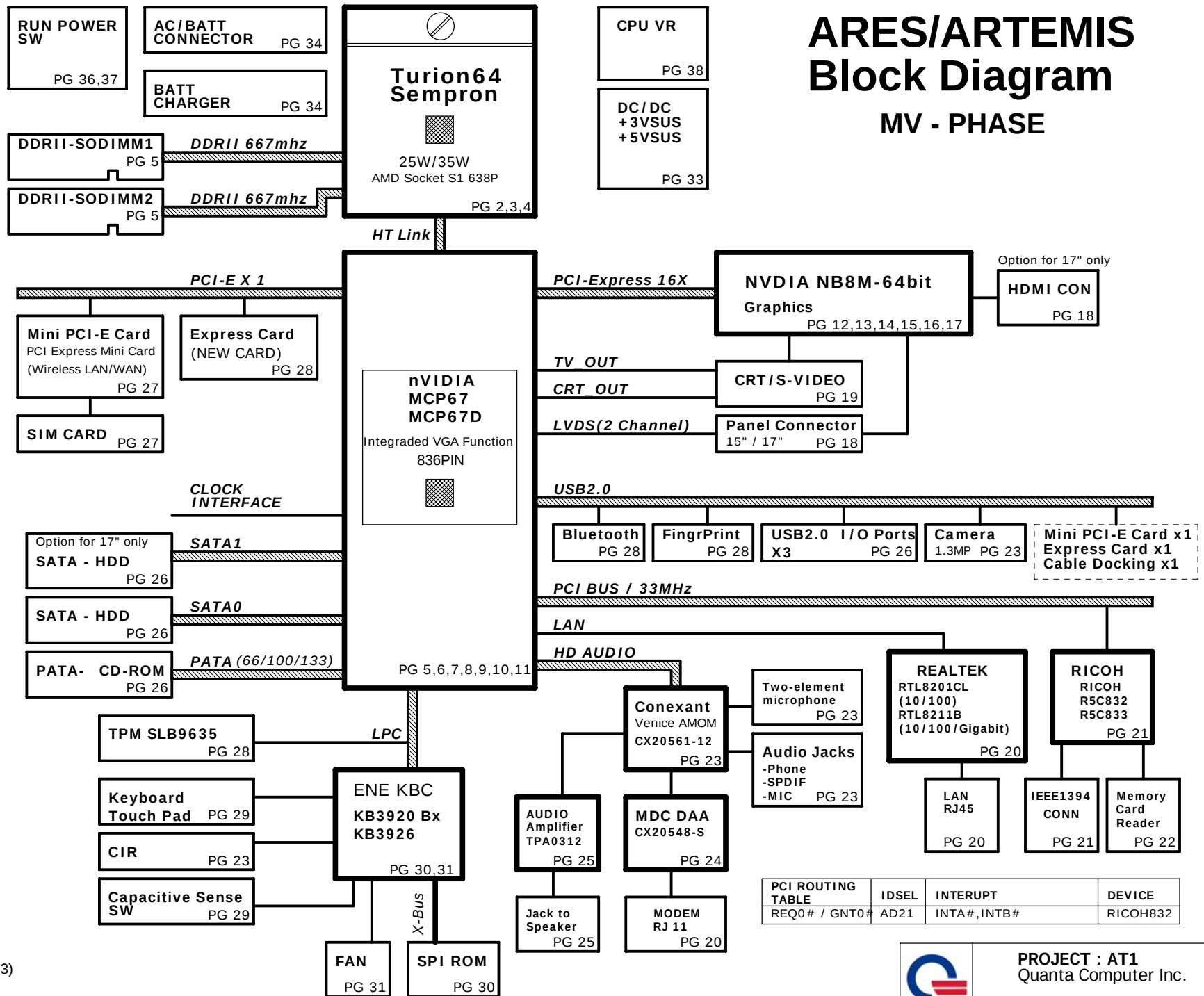
A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402
V=Y5V,U=Y5U,R=X5R,S=X6S,
X=X7R,G=COG,O=NPO

EXAMPLE

10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10F=10ohm(0402 and 1%)

EXAMPLE

0.1U/16V/R=0.1U/16V/X5R(0402)
0.47UA/10V/X=0.47U/10V/X7R(0603)
10UB/10V/U=10U/10V/Y5U(0805)

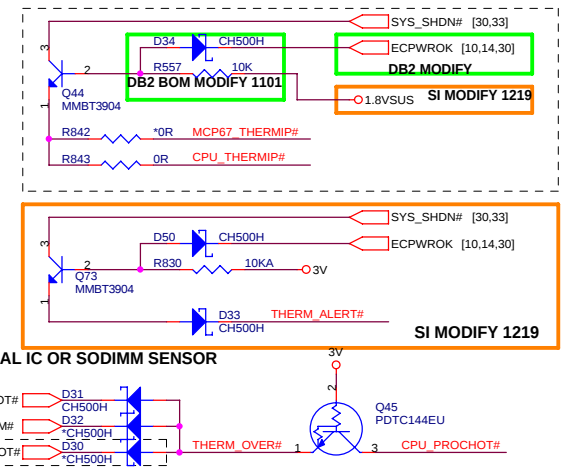
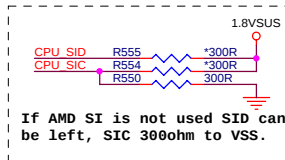
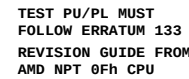


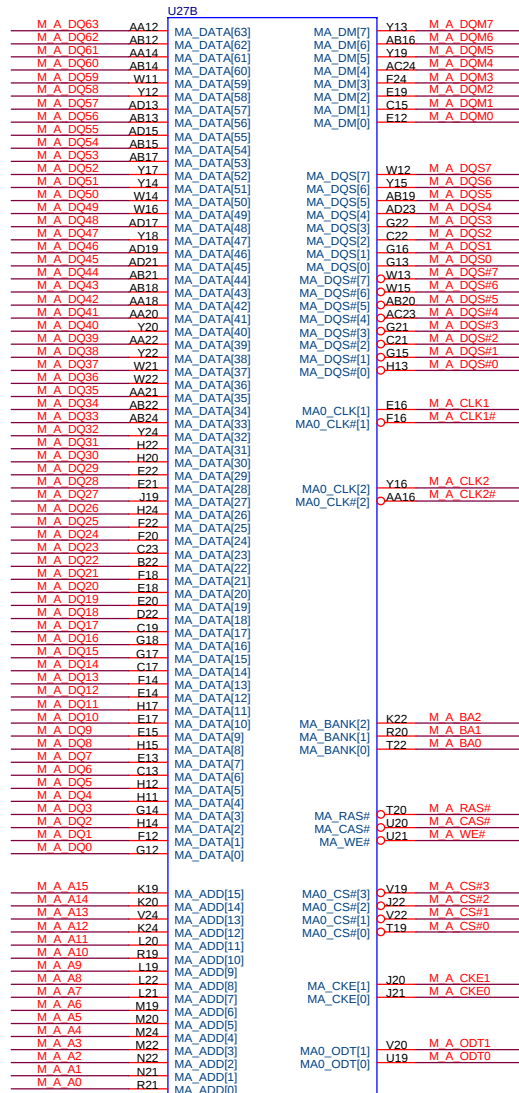
ARES/ARTEMIS Block Diagram MV - PHASE

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

PROJECT : AT1
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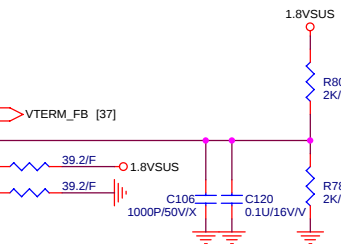
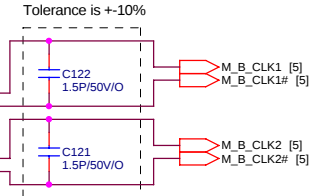
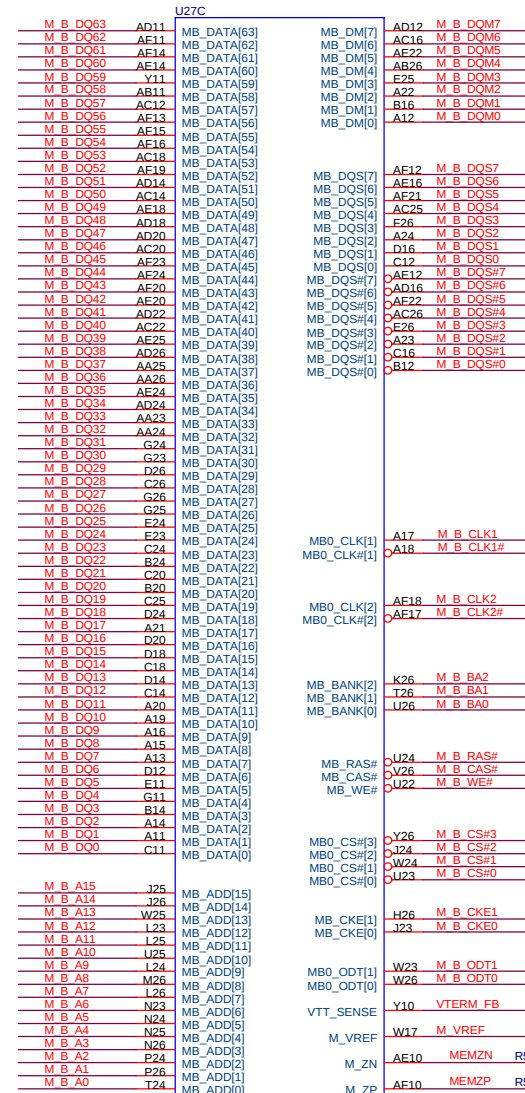
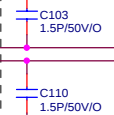
Size Custom	Document Number BLOCK DIAGRAM	Rev MV
Date: Tuesday, August 21, 2007		Sheet 1 of 40



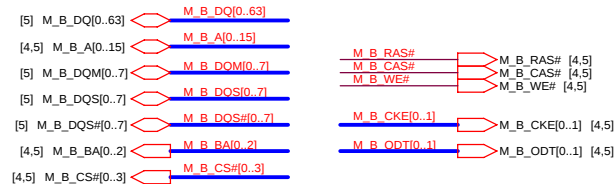
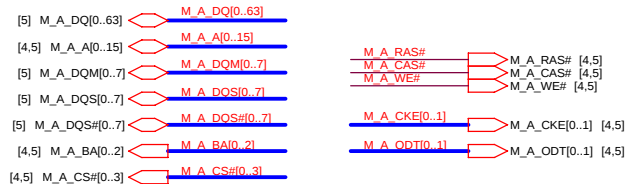


Tolerance is +-10%

TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS

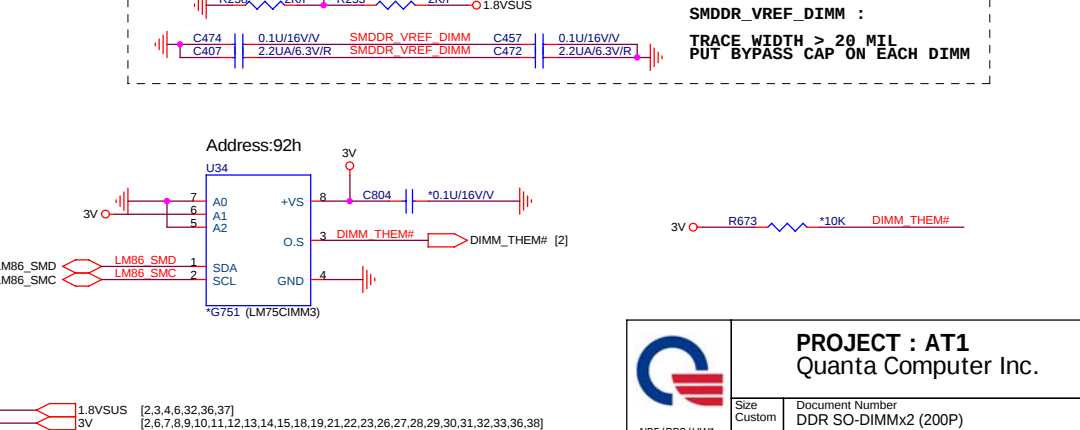
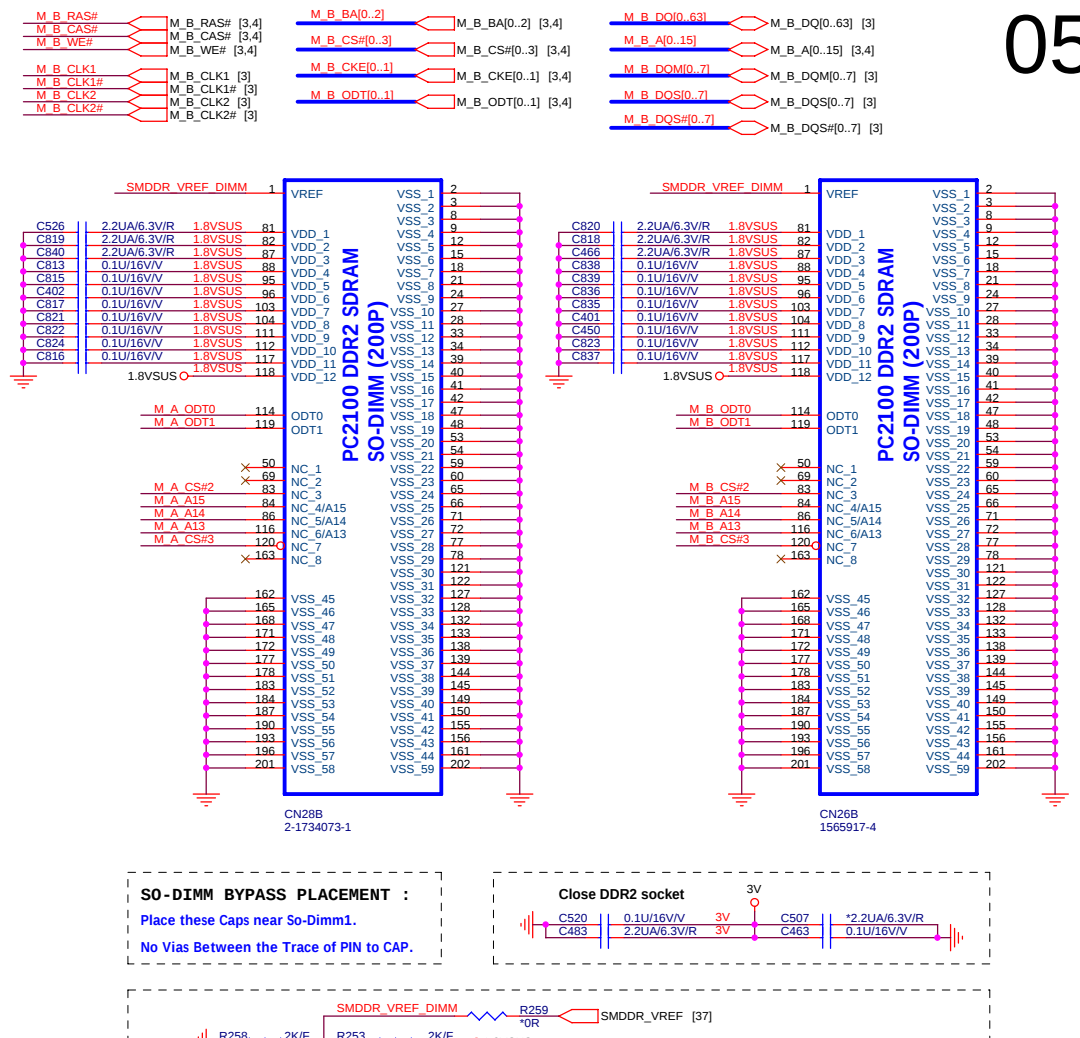


M_VREF : W = 20MIL AND SPACE = 20MIL

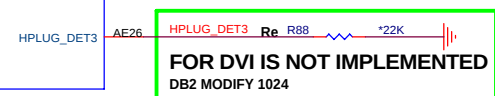
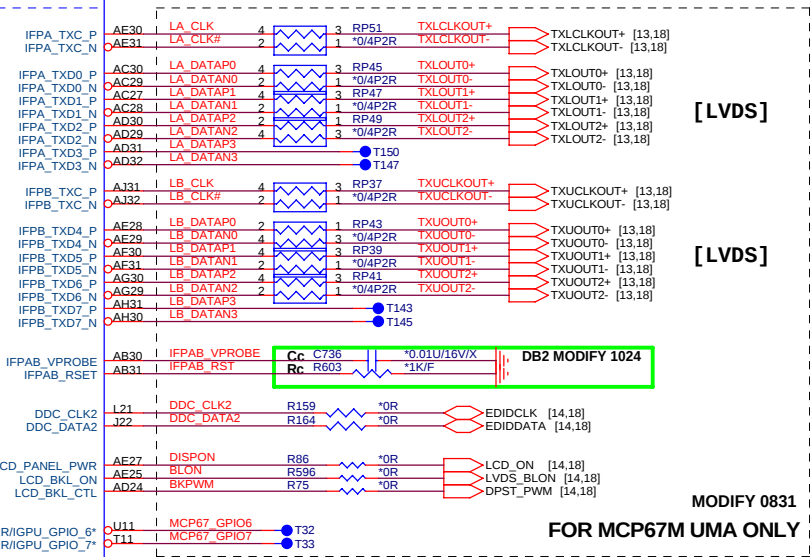
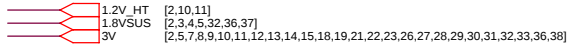
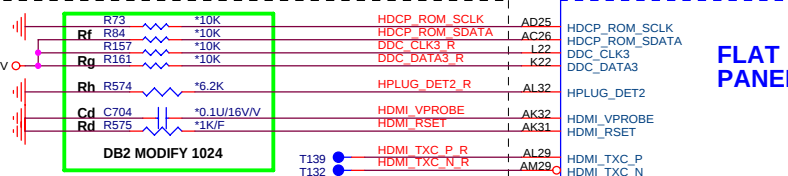
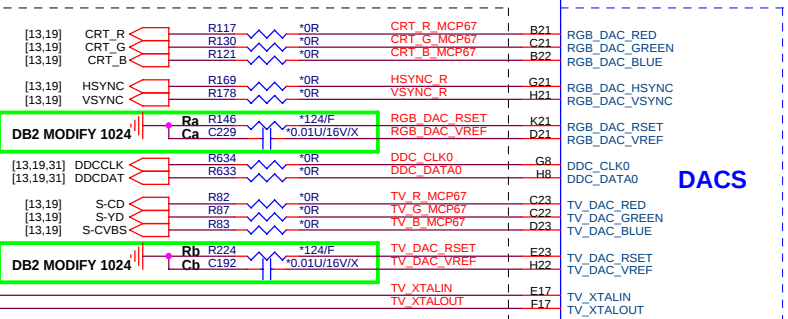
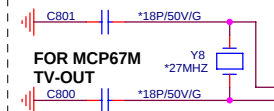
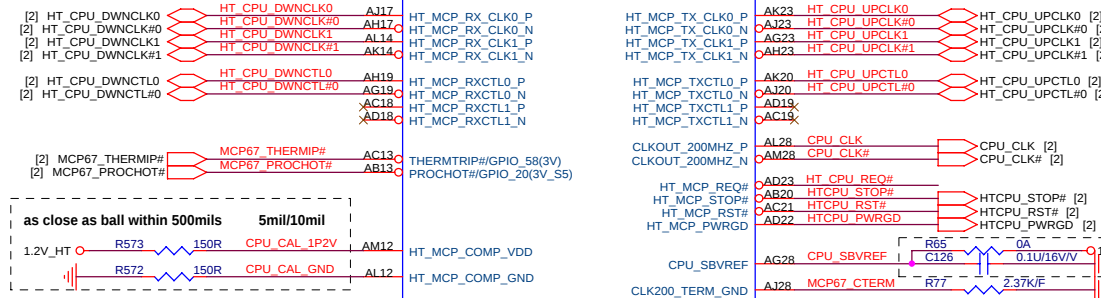
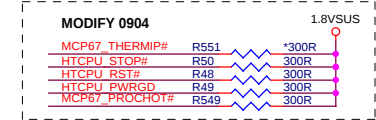
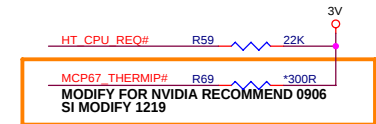
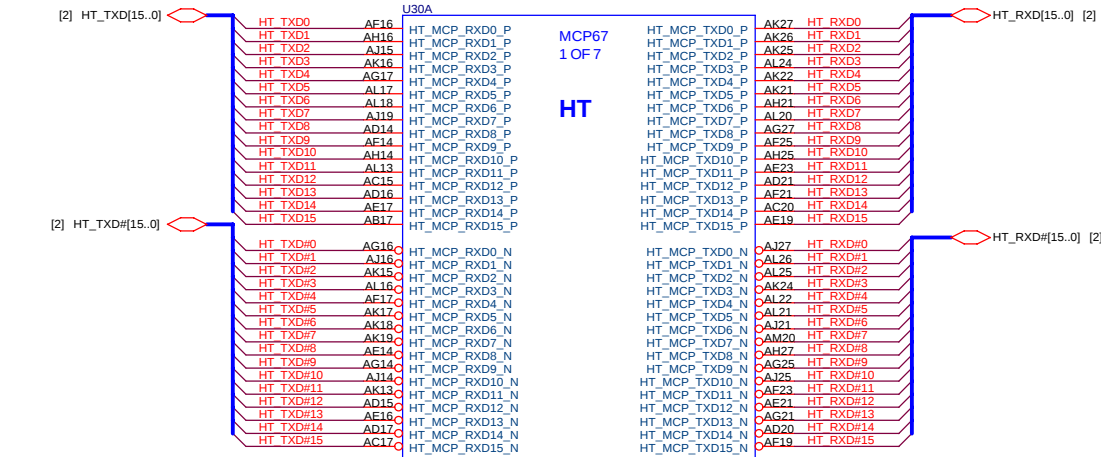


PROJECT : AT1
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Size Custom	Document Number CPU (MEM I/F)	Rev MV
Date: Tuesday, August 21, 2007	Sheet 3 of 40	



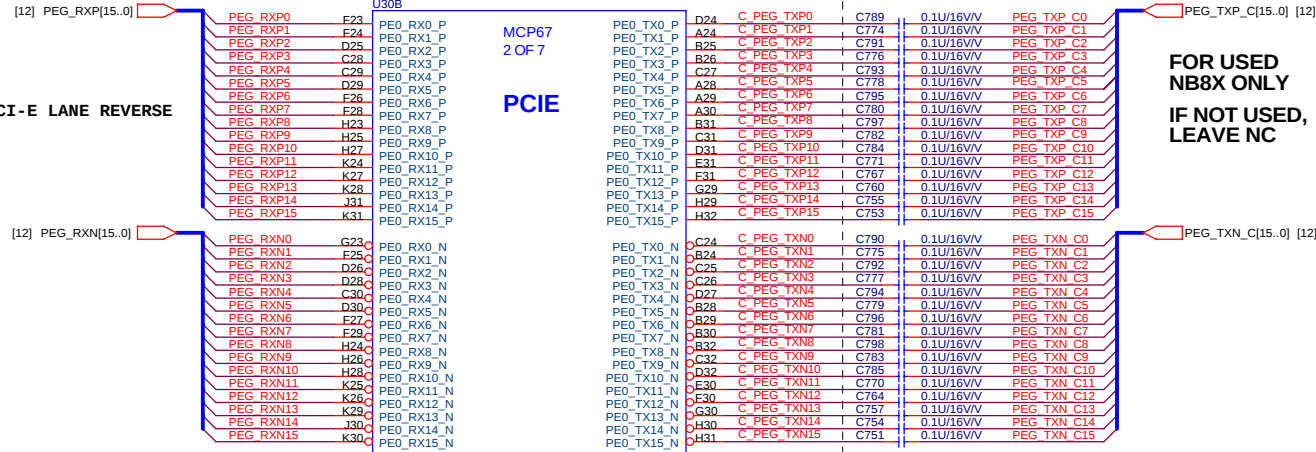
LOCATION	MCP67M (UMA)	MCP67D (DISCRETE)
Ra Ca	124 1% 0.01UF	NC NC
Rb Cb	124 1% 0.01UF	NC NC
Rc Cc Re	1K 1% 0.01UF 22K	NC NC NC
Rd Cd Rf Rg Rh	1K 1% 0.1UF 10K 10K 6.2K	NC NC NC NC NC



PROJECT : AT1
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Size Custom	Document Number MCP67 (HT_I/F,DACS,VGA)	
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C51D SUPPORT PCI-E LANE REVERSE



IF NOT USED NB8X, LEAVE NC

[12] CLK_PCIE_VGA# Rb R649 22R PE0_REFCLK_P R29
[12] CLK_PCIE_VGA# Rc R648 22R PE0_REFCLK_N R30

DB2 MODIFY

[NEW CARD]



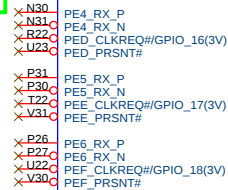
[MINI CARD]



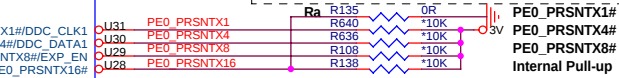
[MINI CARD]



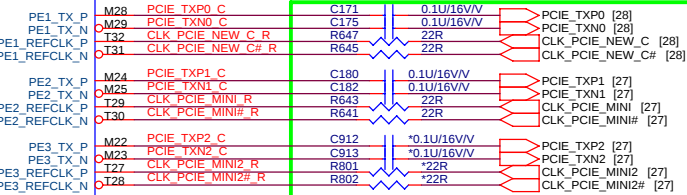
DB2 MODIFY



PE0_PRSTX1#/DDC_CLK1
PE0_PRSTX4#/DDC_DATA1
PE0_PRSTX8#/EXP_EN
PE0_PRSTX16#



PE0_PRSTX1#
PE0_PRSTX4#
PE0_PRSTX8#
Internal Pull-up



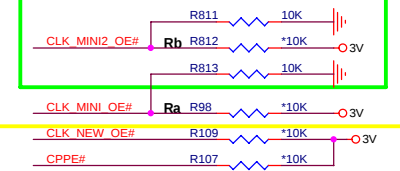
[NEW CARD]

[MINI CARD]

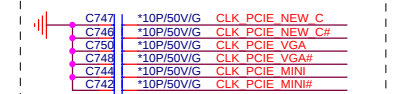
[MINI CARD]
DB2 MODIFY

MV MODIFY 0423

DB2 MODIFY 1025
Ra,Rb IF NOT USED : LEAVE NC (INTERNAL PU)



CLOCK BYPASS

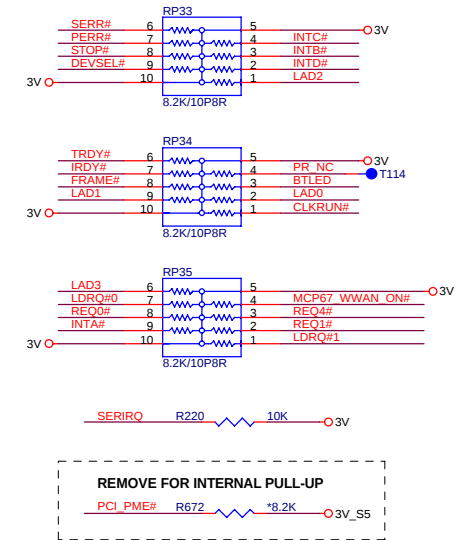


PROJECT : AT1
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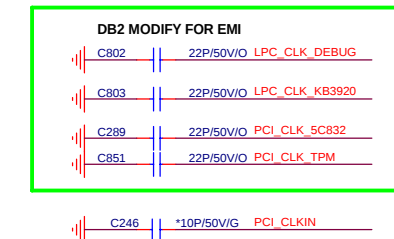
Size Custom	Document Number MCP67 (PCI-E_I/F)	Rev MV
Date: Tuesday, August 21, 2007	Sheet 7 of 40	

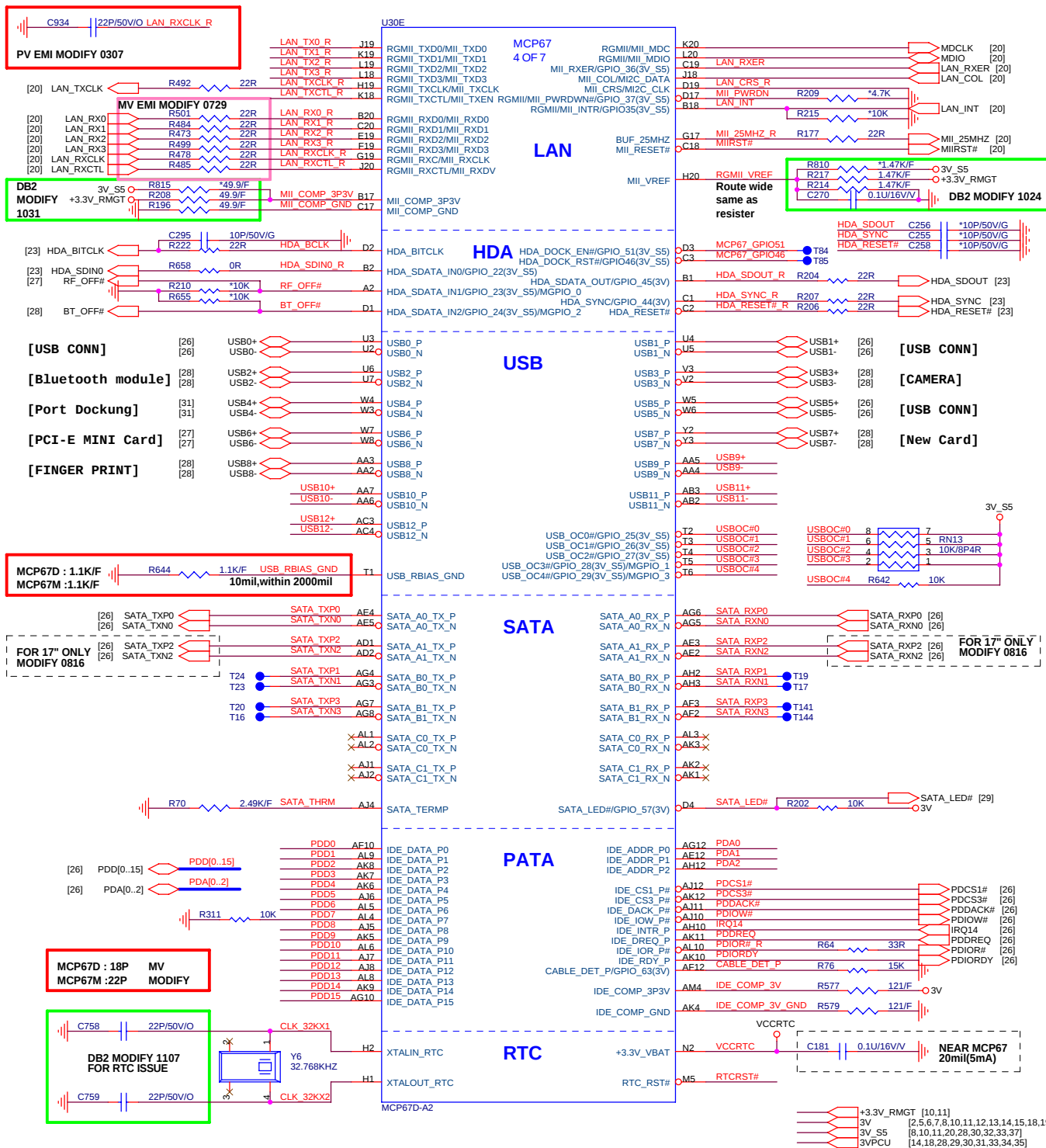
[2,5,6,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

PCI/LPC PULL-UP



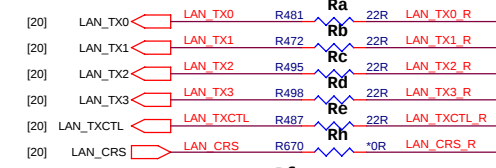
CLOCK BYPASS





10/100 - GIAG LAN STUFF OPTION

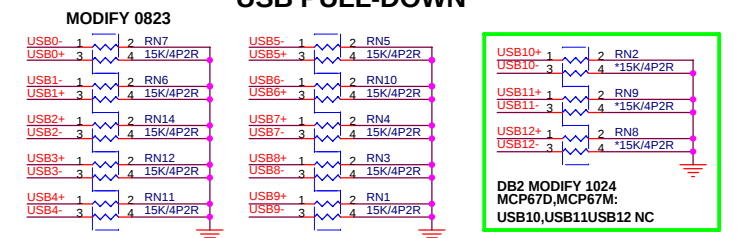
09



MODIFY 0824

	10/100	GIGA
Ra	0R	22R
Rb	0R	22R
Rc	0R	22R
Rd	0R	22R
Re	0R	22R
Rf	0R	22R
Rg	0R	22R
Rh	0R	22R

USB PULL-DOWN



MCP67 STRAPPING

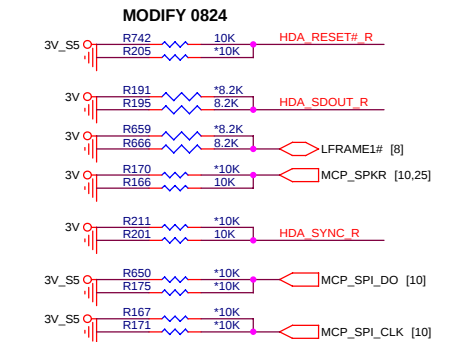
HDA RESET# (LAN)	
0	MIL
1	RGMIU (DEFAULT)

HDA SDOUT R (LFRAM1# (BIOS))	
00	LPC (DEFAULT)
01	PCI BIOS
10	SPI BIOS
11	RESERVED (SPI)

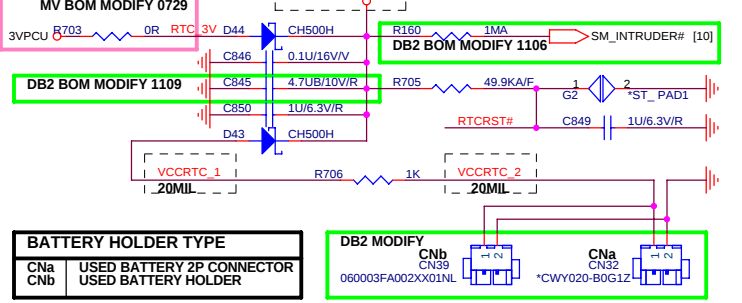
MCP SPKR (Boot MODE)	
0	USER TABLE (DEFAULT)
1	SAFE TABLE

HDA SYNC R (SIO CLOCK)	
0	14.318MHz (DEFAULT)
1	24MHz

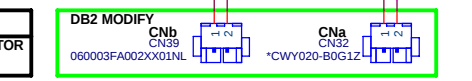
SPI DO, SPI CLK (SPI CLOCK)	
00	31MHz
01	42MHz
10	25MHz
11	1MHz



RTC



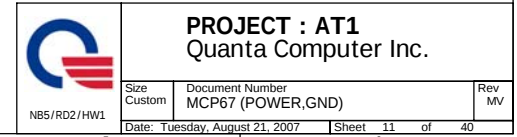
BATTERY HOLDER TYPE	
CNa	USED BATTERY 2P CONNECTOR
CNb	USED BATTERY HOLDER

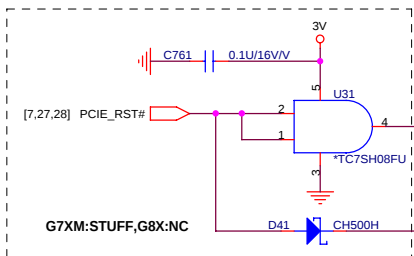


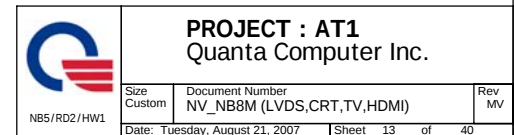
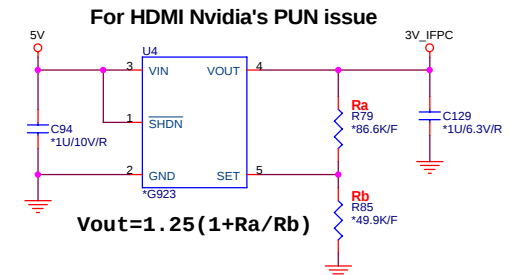
PROJECT : AT1

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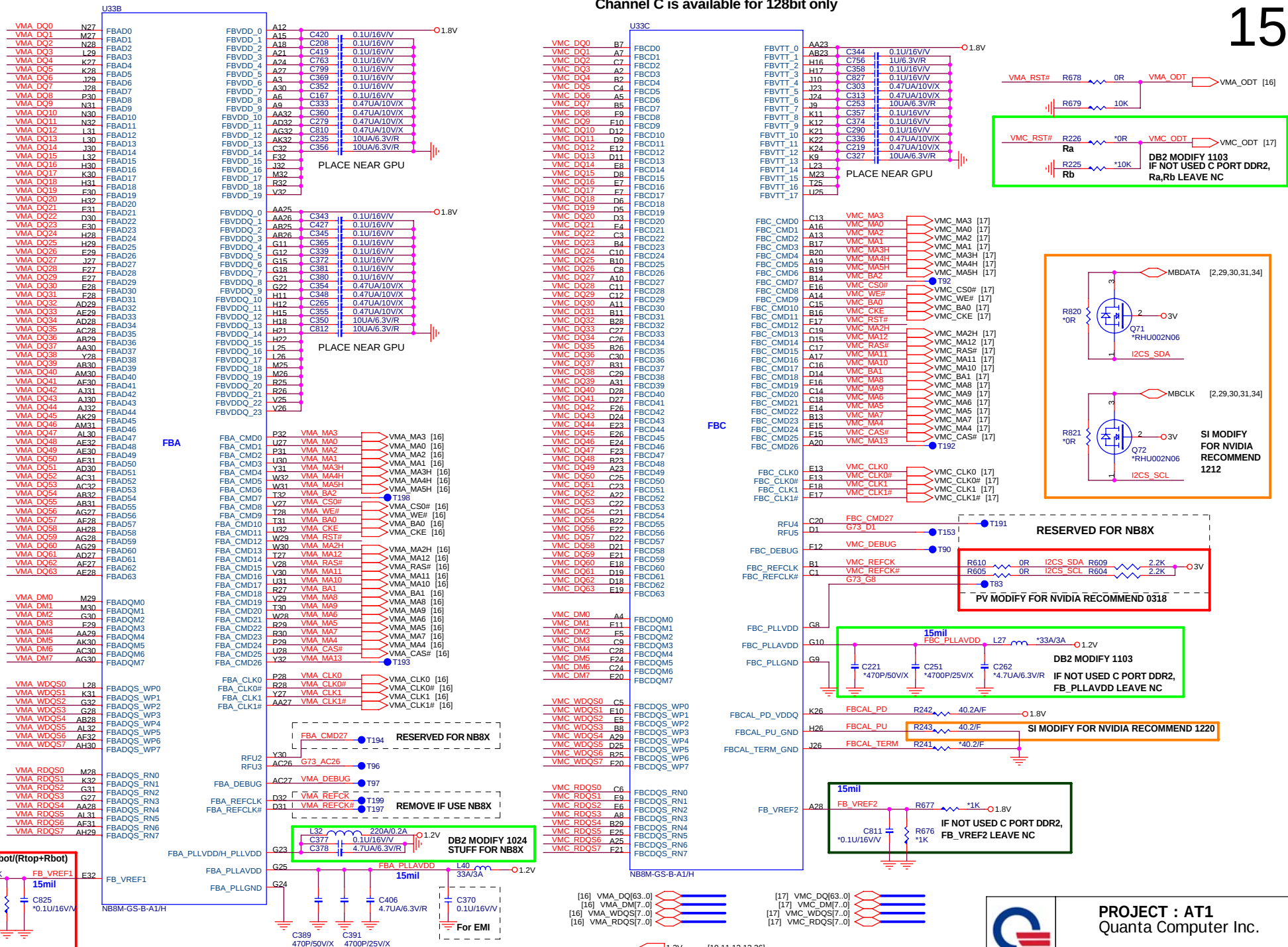
Size	Document Number	Rev
Custom	MCP67 (LAN,HDA,USB,ATA,RTC)	MV
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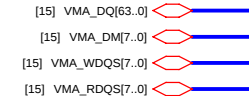
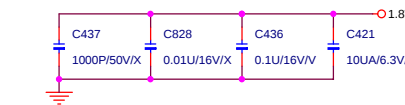
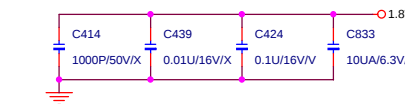
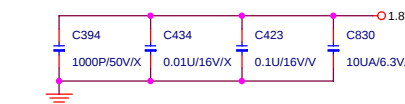
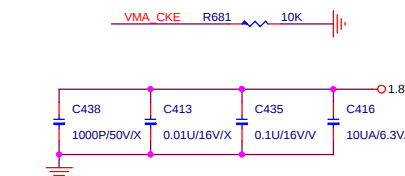
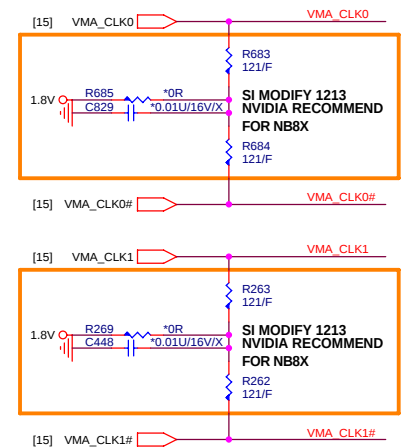






Channel C is available for 128bit only



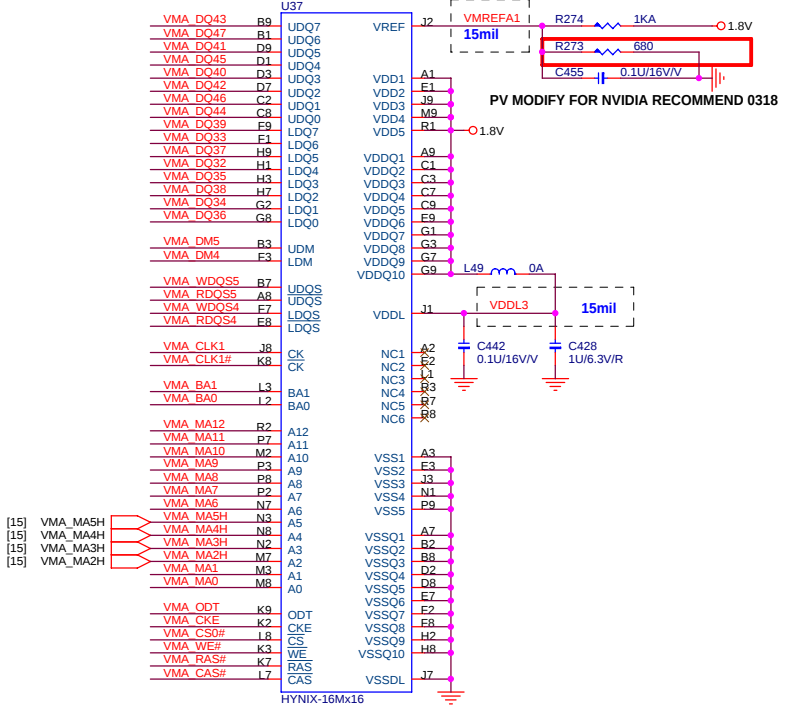
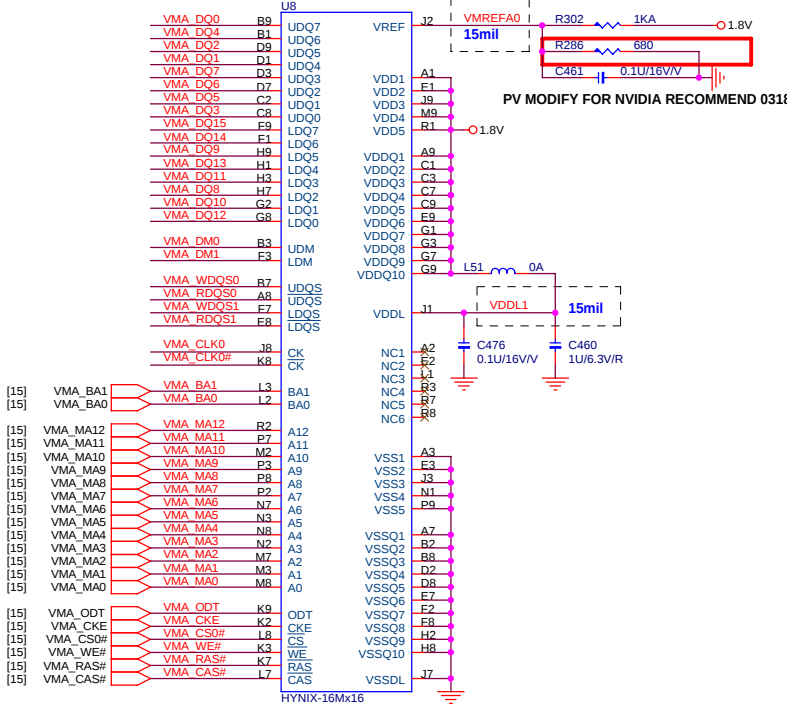
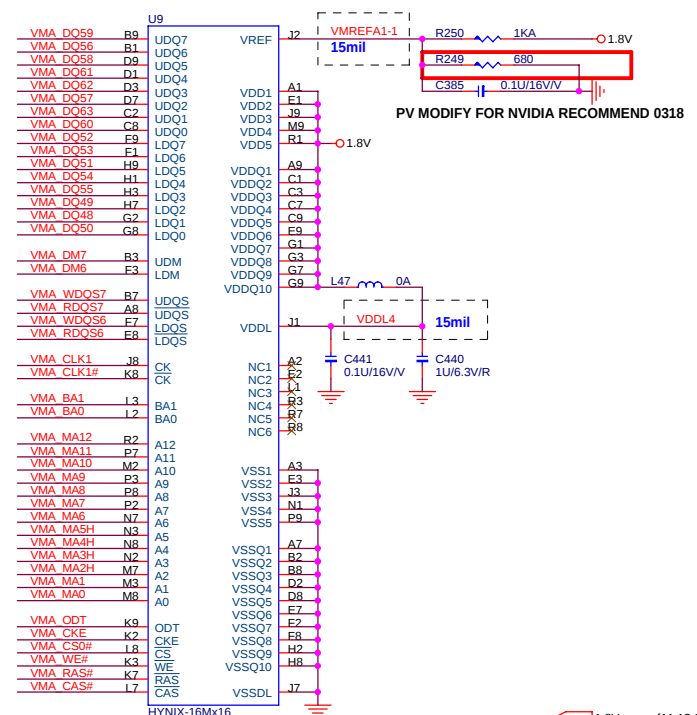
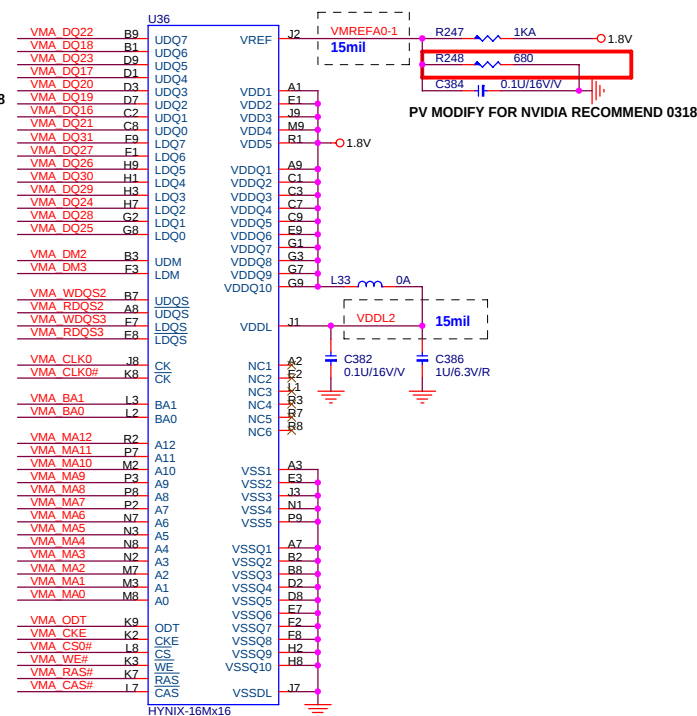


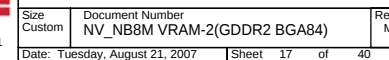
HYNIX-16Mx16 : AKD5JG-TW12 (HY5PS561621AFP-25 1.8V)
INFINEON-16Mx16 : AKD5JG-T08 (HYB18T256161AFL25)
SAMSUNG-16Mx16 : AKD5JG-T514 (K4N561630G-ZC25 1.8V)



PROJECT : AT1
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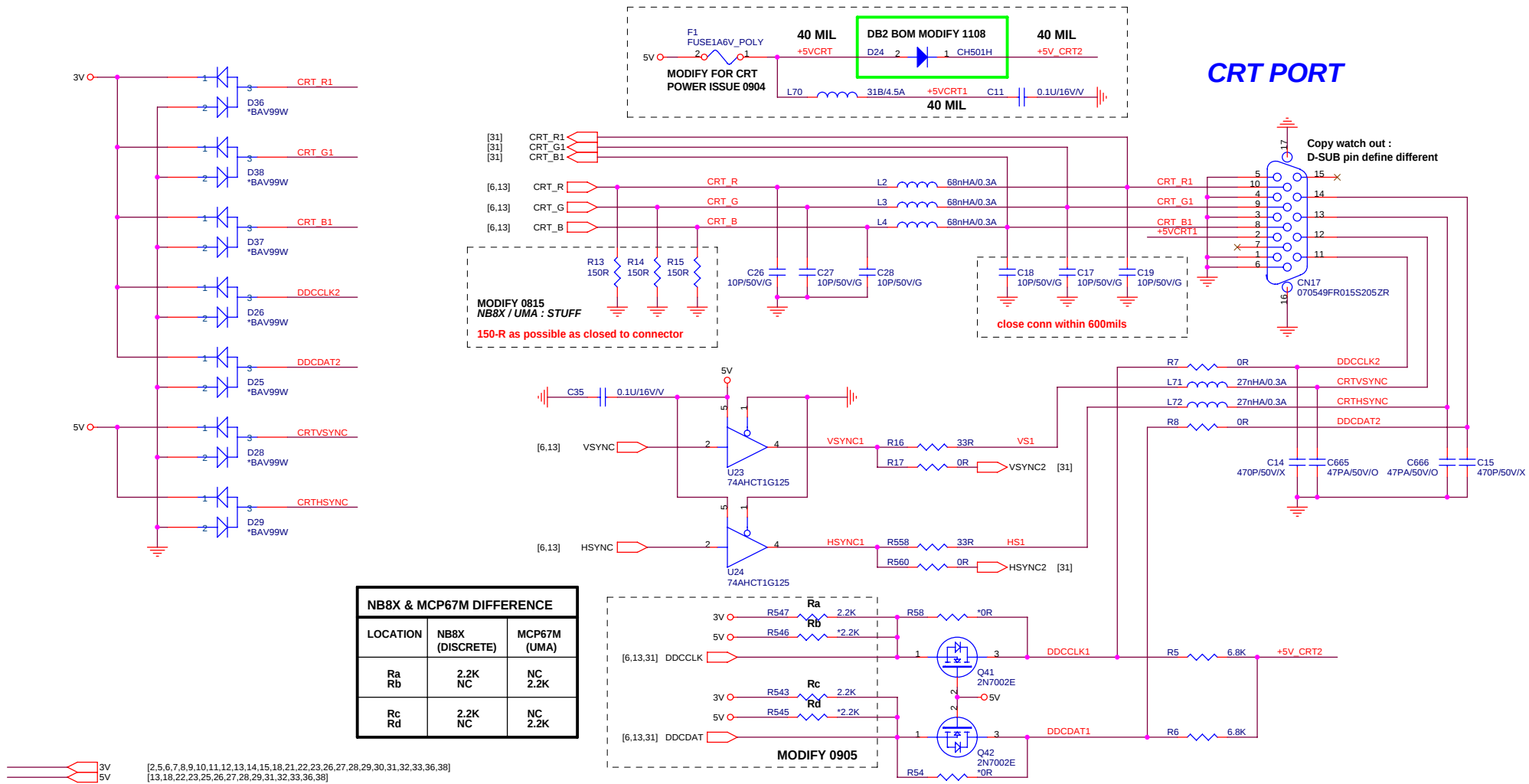
Size Custom	Document Number NV_NB8M VRAM-1(GDDR2 BGA84)	
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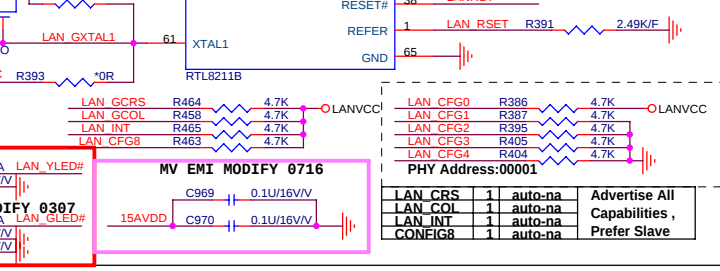
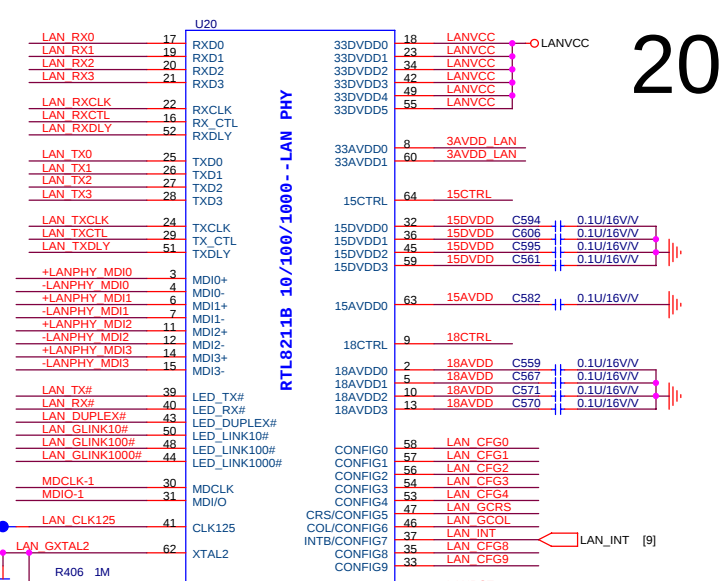
LCD CONNECTOR

HDMI PORT



PROJECT : AT1
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Size Custom	Document Number CRT_TV_OUT	Rev MV
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DB2 MODIFY 1106

[9] MDIO

LANVCC

Q21
*2N7002E

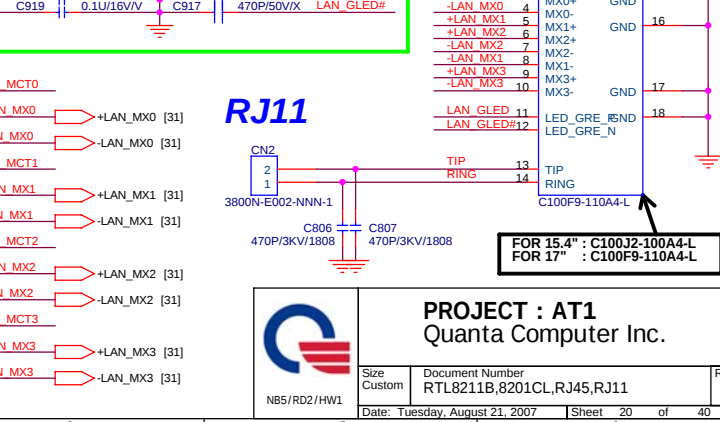
MDIO-1

R383

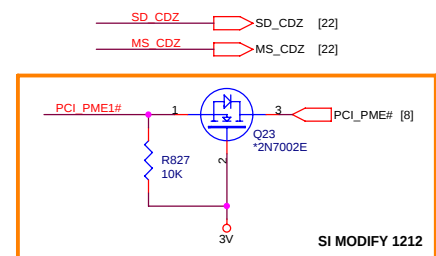
0R

RJ45

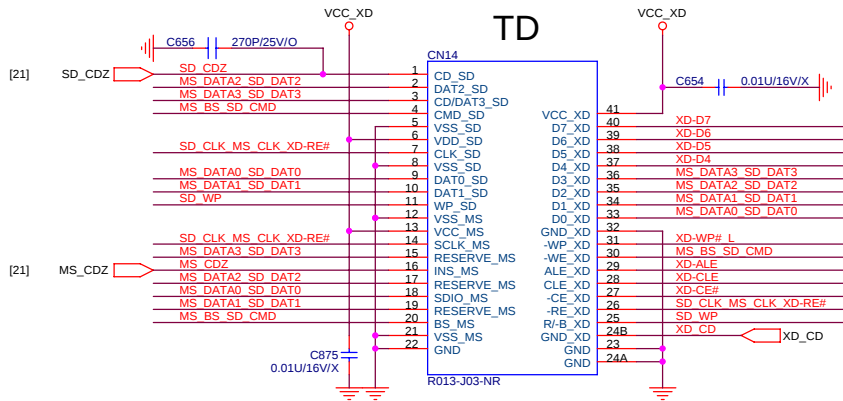
DB2 EMI MODIFY		C914	470P/50V/X	LAN_YLED	1	LED_YEL_P
C915	470P/50V/X	C915	470P/50V/X	LAN_YLED#	2	LED_YEL_N
C916	470P/50V/X	C916	470P/50V/X	LAN_GLED		



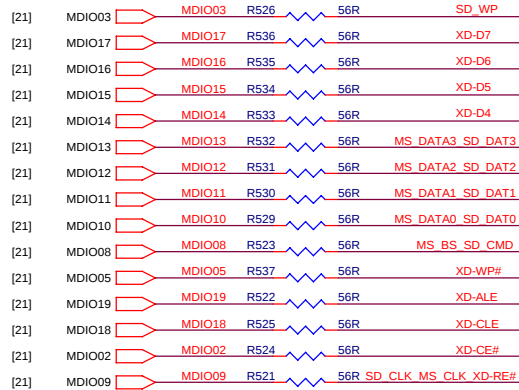
- *TPA/TPA#,TPB/TPB# pair trace : As close as possible.
- *TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layout with shields.
- *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



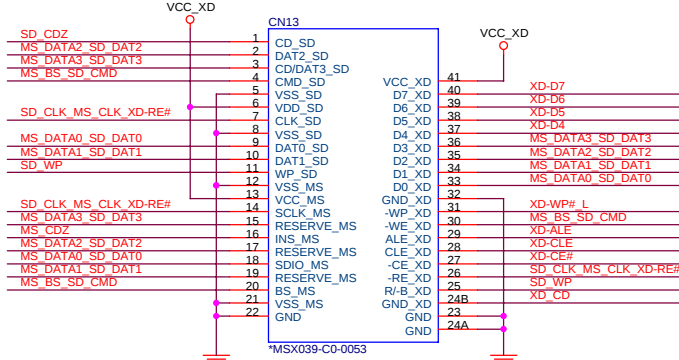
4 IN1 CARD READER XD,MMC/SD,MS/MP



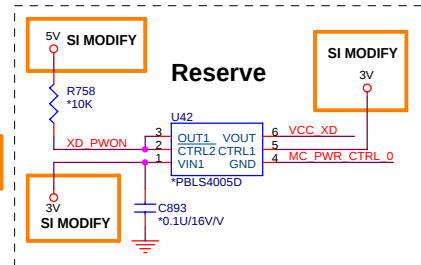
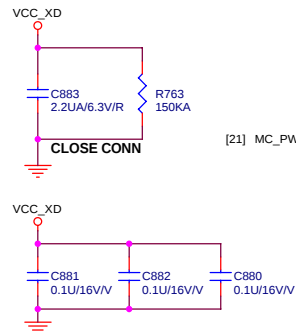
Note: Need to add WP# and CD# pad for Proconn



2ND SOURCE

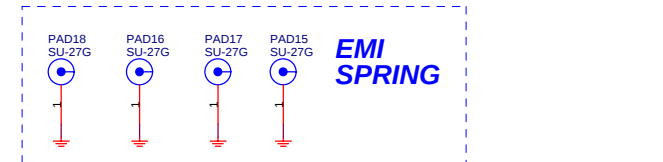
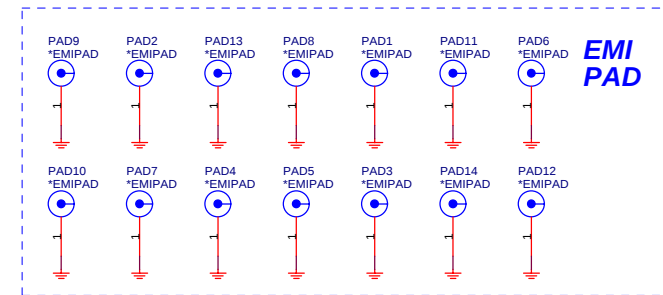
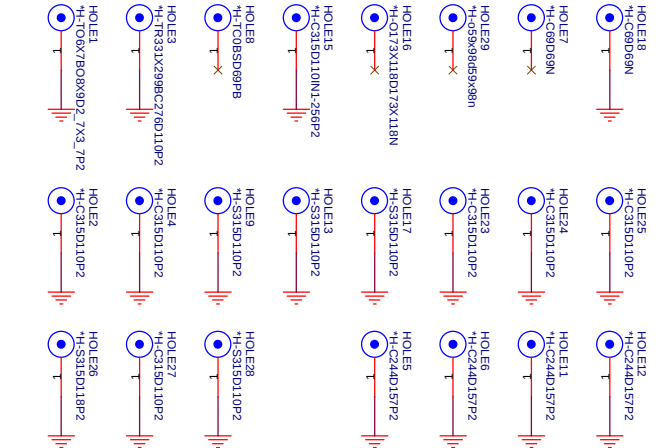
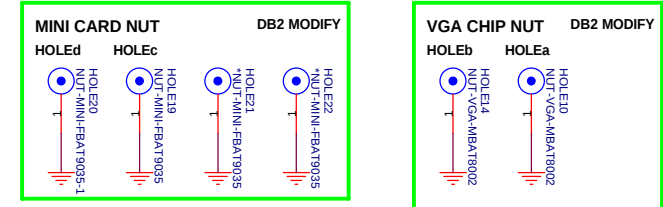


* NOT INSTALL FOR 2ND SOURCE CO-LAYOUT USED



15.4" & 17" AND DISCRETE & UMA		
HOLE	STATUS	NUT
HOLEa	DISCRETE	NUT-VGA-MBAT8002
	15" & 17"	NC
HOLEb	DISCRETE	NUT-VGA-MBAT8002
	UMA 15"	NUT-VGA-MBAT8002
	UMA 17"	NC
HOLEc	15.4"	NUT-MINI-MBAT8004
HOLED	17"	NUT-MINI-FBAT9035

SCREW HOLE



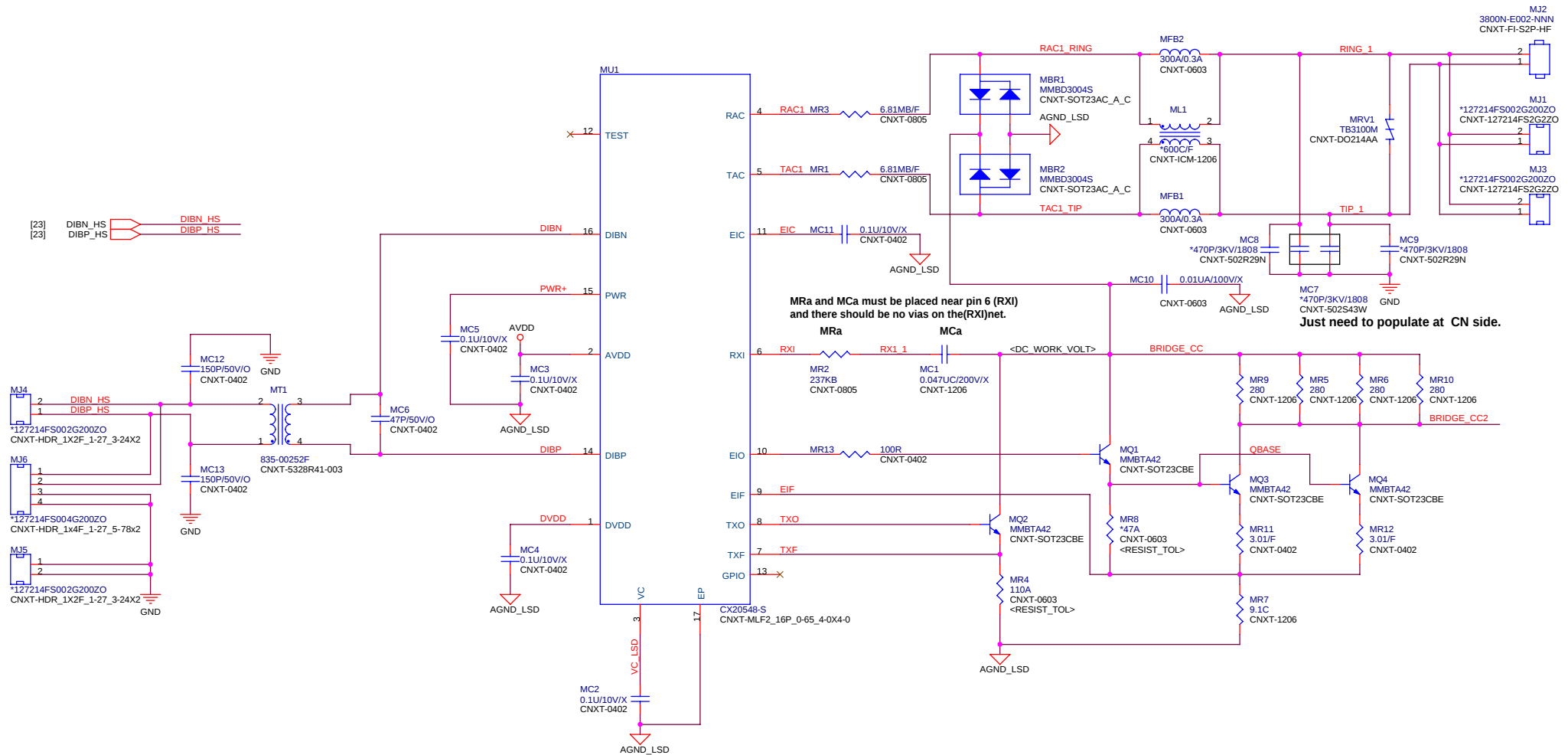
PROJECT : AT1
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Size Custom	Document Number CARD_READER,HOLE,NUT,SPRING	Rev MV
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3AVDD	[25]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,26,27,28,29,30,31,32,33,36,38]
5V	[13,18,19,22,25,26,27,28,29,31,32,33,36,38]
5VPCU	[10,33,34,35,36,37,38]

Revision History

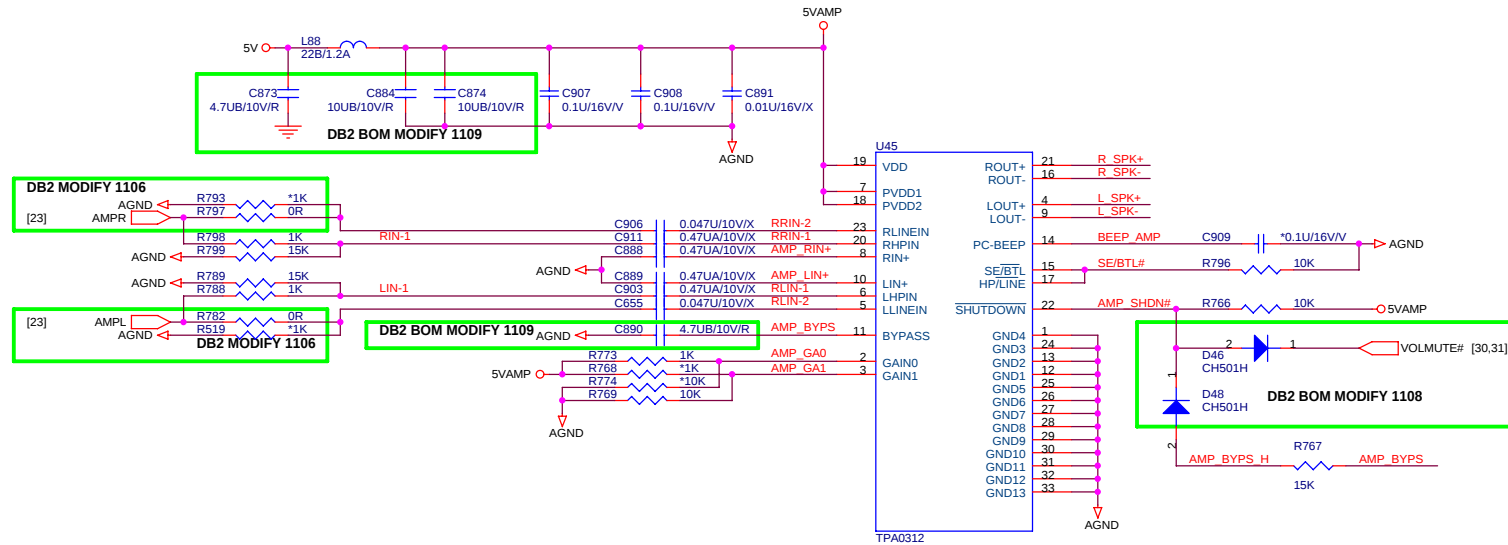
REV	Description	Date
0	Initial Release	April 26, 2005
4		



PROJECT : AT1
Quanta Computer Inc.

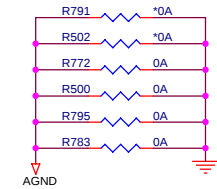
Size Custom	Document Number MODEM(DAA)_CX20548-S	Rev MV
Date: Tuesday, August 21, 2007	Sheet 24 of 40	

AUDIO AMPLIFIER

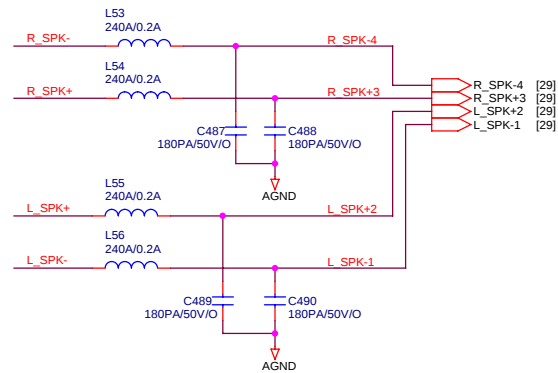


0312 Gain Table

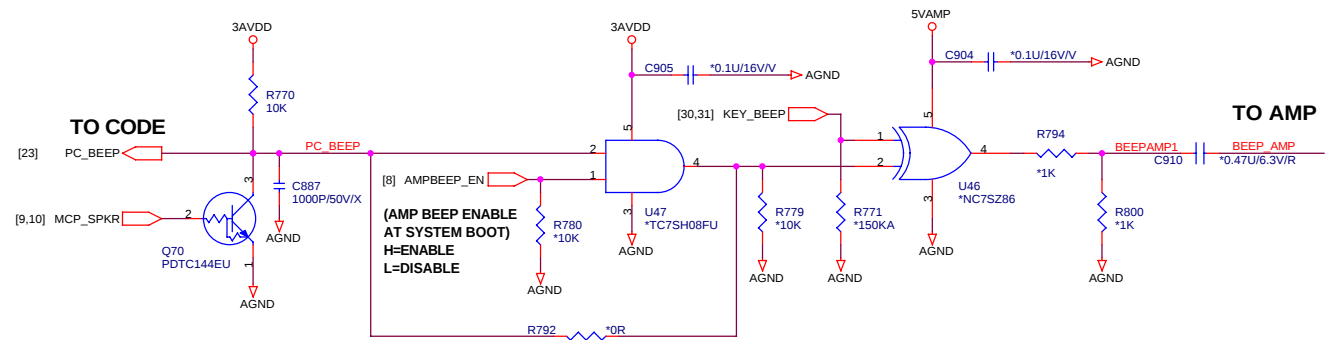
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



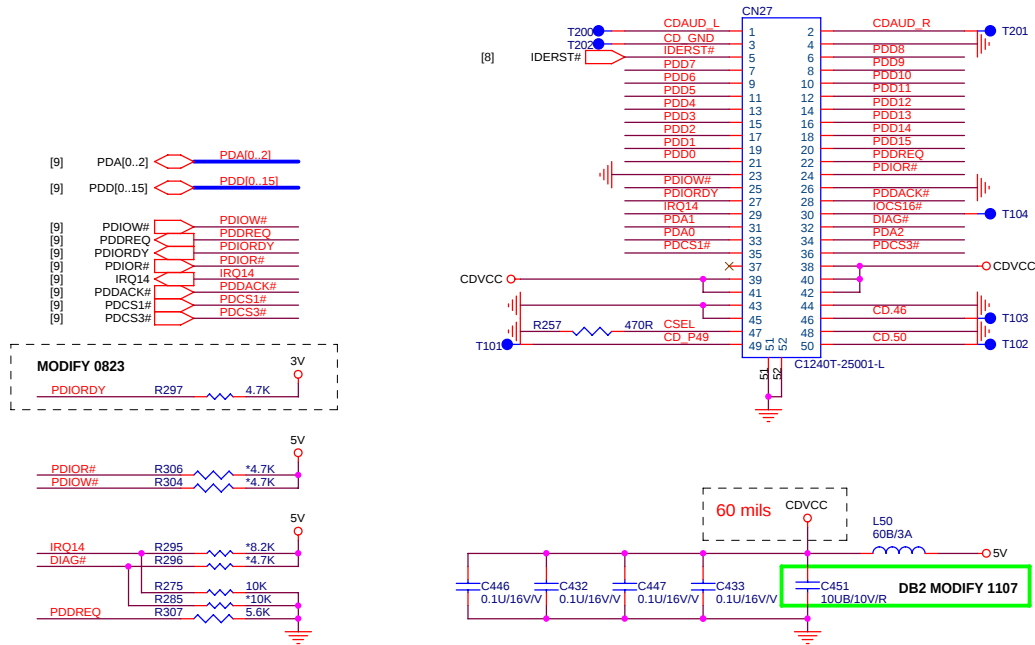
INT. SPEAKER



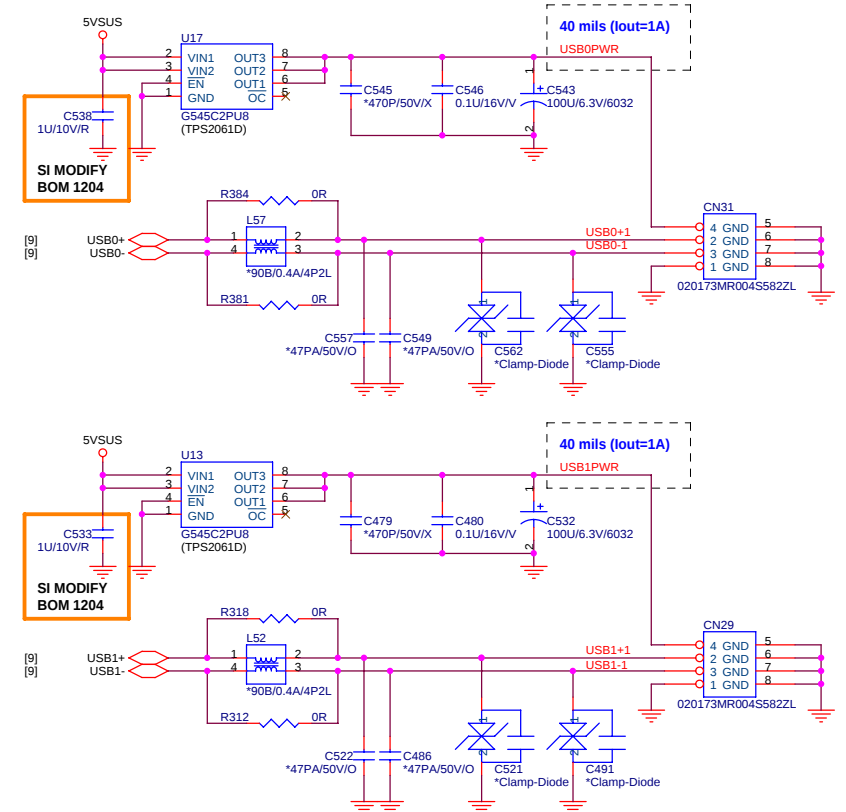
PCSPK BEEP



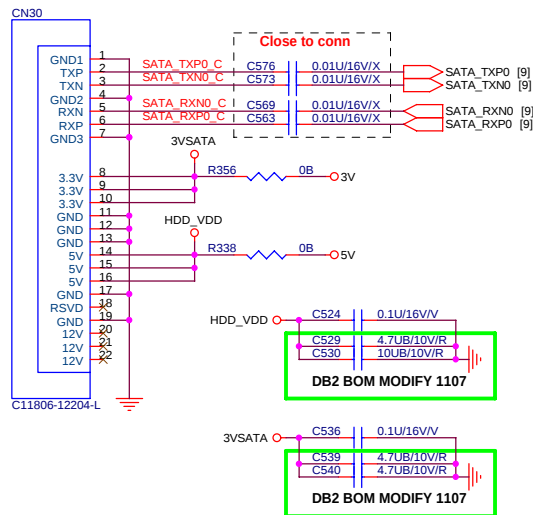
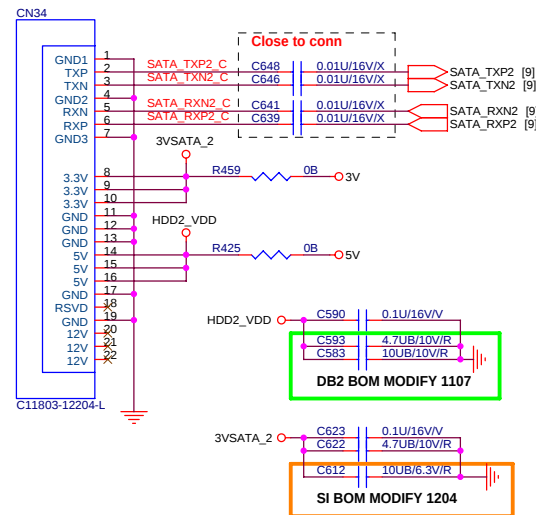
CD-ROM



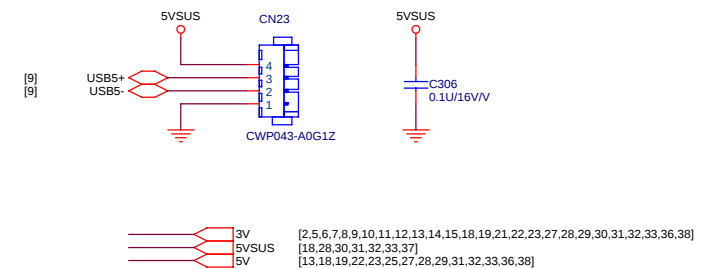
USB DIP CONNECTOR X 2



SATA_1 CONNECTOR

For 17"W Second HDD
SATA_2 CONNECTOR

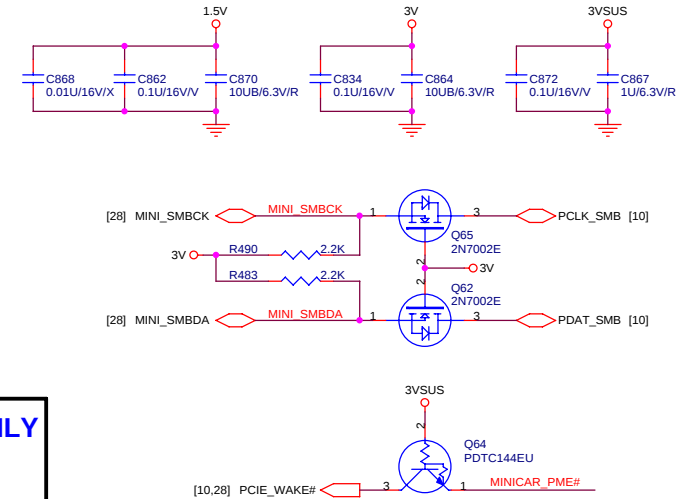
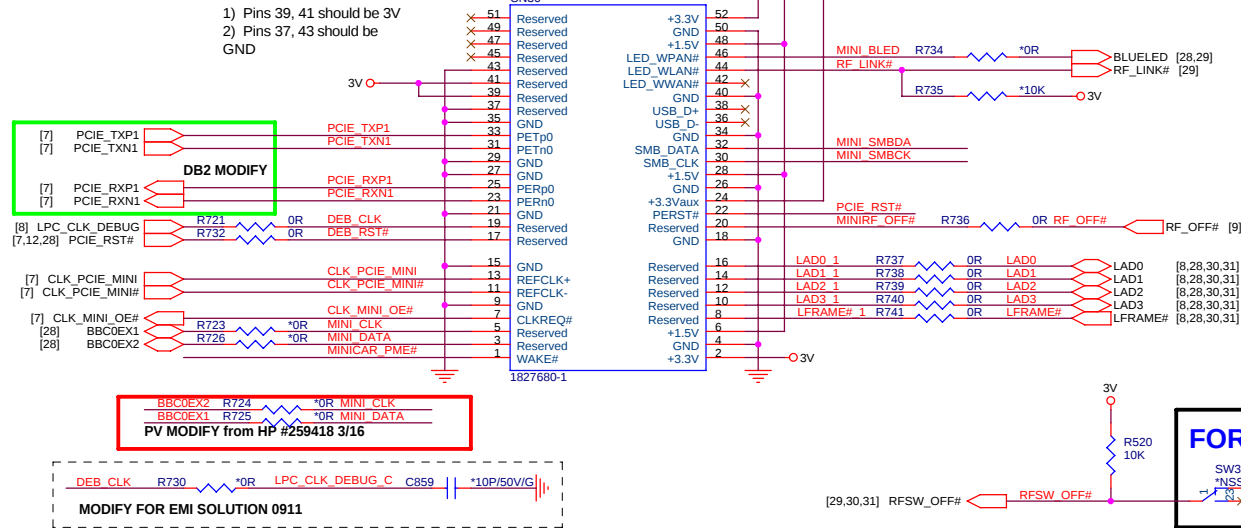
USB WIRE TO DC BOARD X 1



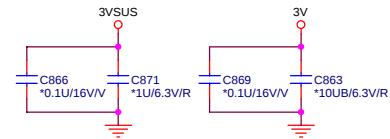
PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number SATA HDDx2,CD-ROM,USBx3	Rev MV
Date: Tuesday, August 21, 2007	Sheet 26 of 40	

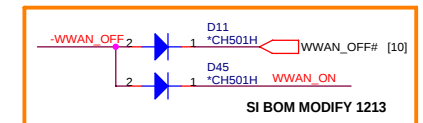
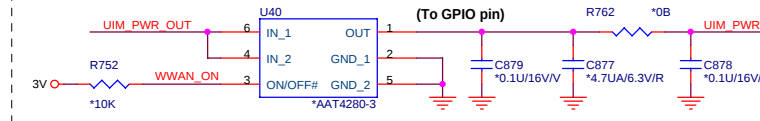
Mini PCI-E Card 1



**Mini PCI-E Card 2
(WWAN/SIM)
FOR 15.4" ONLY (RESERVE)**



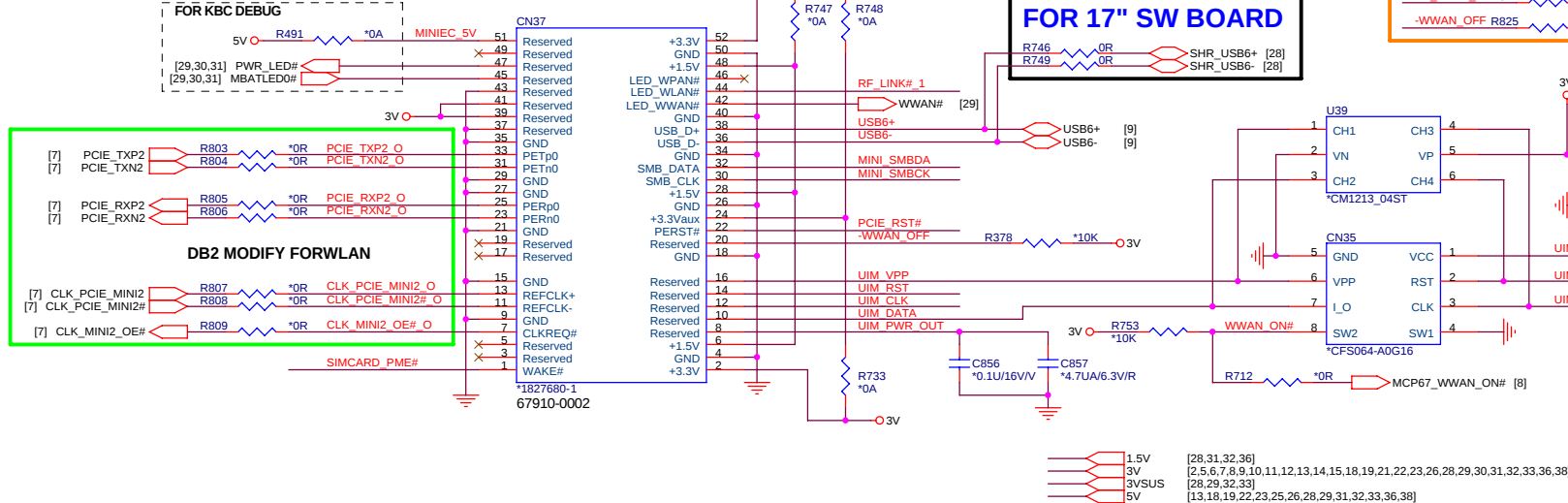
No need to stuff.



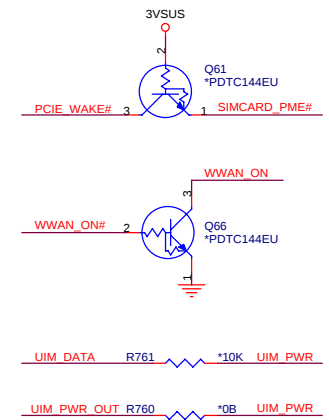
FOR KBC DEBUG

[29,30,31] PWR_LED#

[29,30,31] MBATLED0#



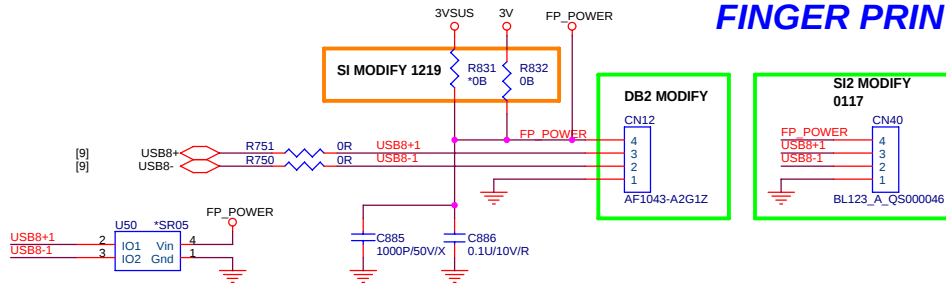
SI MODIFY 1213 FOR WLAN



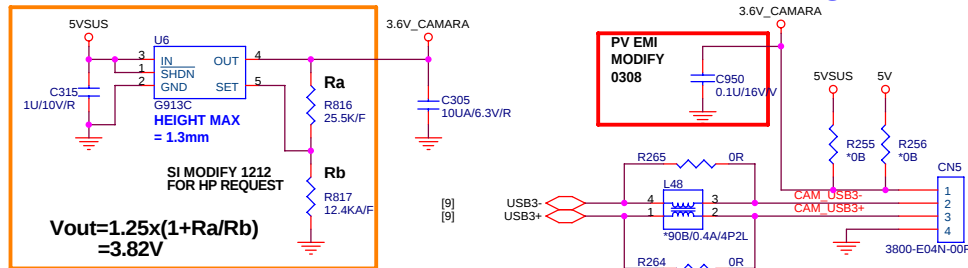
PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number MINI CARDx2 (WLAN,WWAN,SIM)	Rev MV
Date: Tuesday, August 21, 2007		Sheet 27 of 40

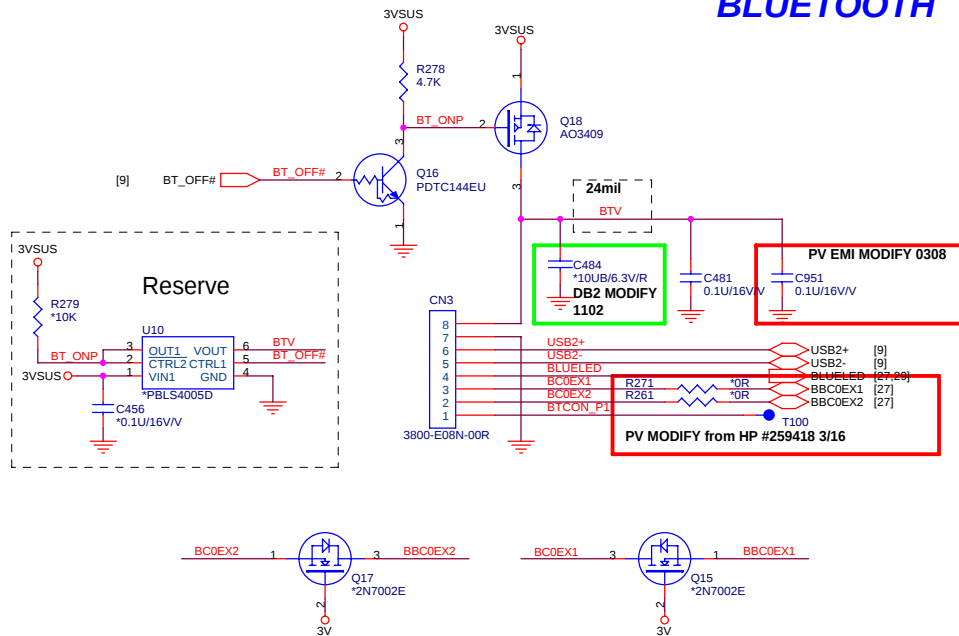
FINGER PRINT

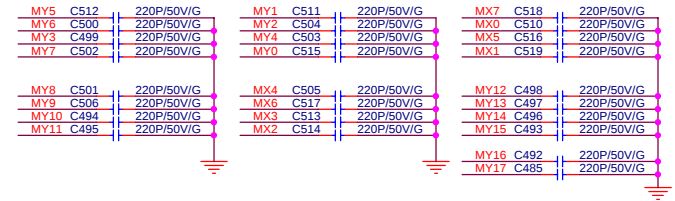


CAMERA



BLUETOOTH





FOR QLB SW BOARD

Pinout for QLB SW BOARD (CN10):

Signal	Pin
3V	1
3VPCU	2
MBCLK	3
NUMLED#	4
MEPACK	5
MEP_DATA	6
MEP_CLK	7
MUTE_LED	8
MBDATA	9
MBDATA	10
MBDATA	11
MBDATA	12

87151-12021

2ND SOURCE

Pinout for 2ND SOURCE (CN7):

Signal	Pin
3V	1
3VPCU	2
MBCLK	3
NUMLED#	4
MEPACK	5
MEP_DATA	6
MEP_CLK	7
MUTE_LED	8
MBDATA	9
MBDATA	10
MBDATA	11
MBDATA	12

*BL121-12R-TAND

* Cnc NOT INSTALL FOR 2ND SOURCE CO-LAYOUT USED

FOR 15.4" LCD :
STUFF LEDa, Ra

FOR 17" LCD :
STUFF LEDb, Rb

FOR CARD Reader LED

LEDa LED1 LED-2P-BL 2 CAP_LED 3V

Ra R200 150R

LEDb LED2 LED-2P-BL 2 CAP_LED 3V

Rb R245 150R

LED9 LED-2P1-BL 2 CARD_LED 3V

R446 150R

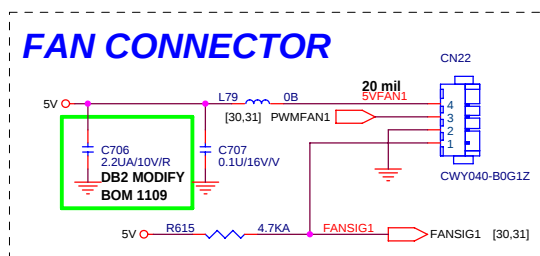
FOR LED DRIVING ISSUE

STUFF	Rc, Qa, Qb, LEDc
NC	Rd

FOR EMI solution 0116
Close to CN7/CN10

3V
3VSUS
3VPCU

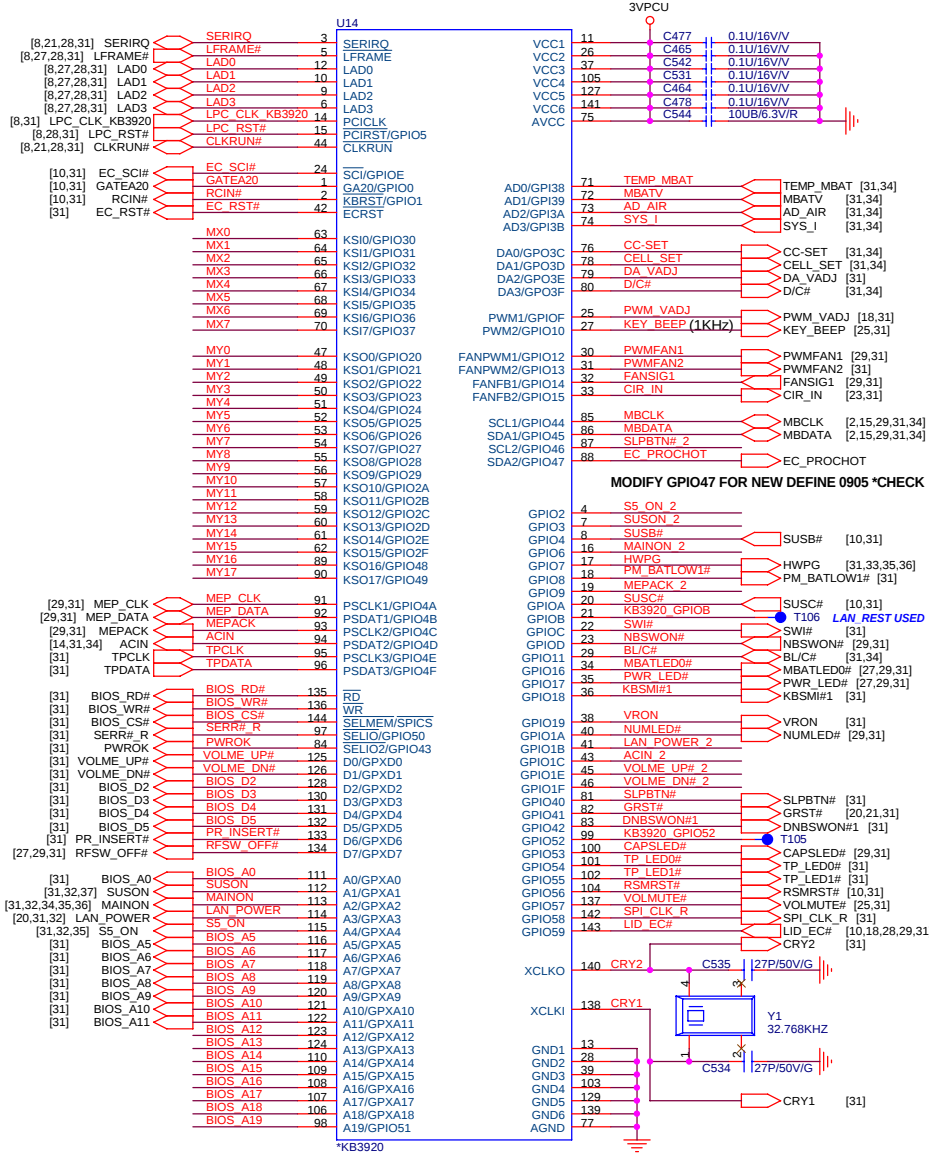
[2,5,6,7,8,9,10,11,12,13,14,15,18,19]
[27,28,32,33]
[9,14,18,28,30,31,33,34,35]



FOR LED DRIVEING ISSUE	
STUFF	Rc,Qa,Qb,LEDc
NC	Rd

EC - KB3920

30



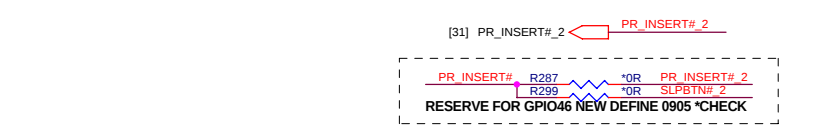
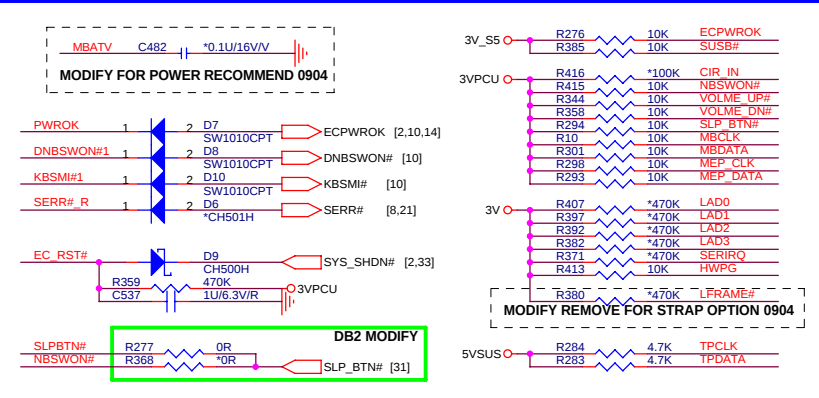
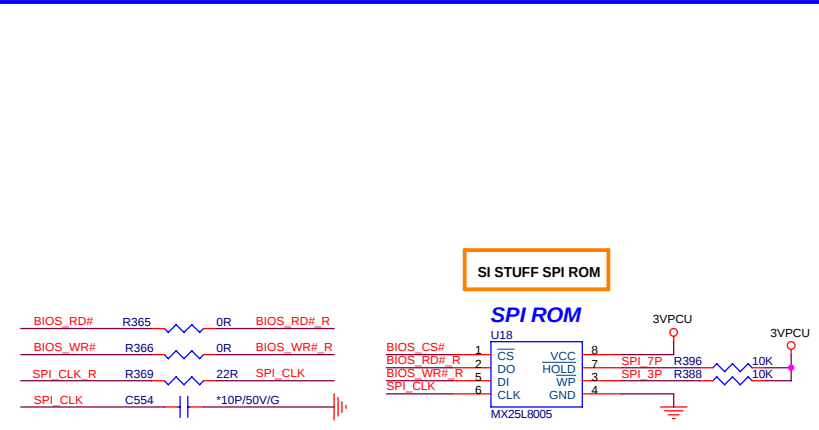
DB2 MODIFY



IF USED KB3920 : Ra stuff 0 ohm

IF USED KB3920 : Ra leave NC

MY0	47	TP_TEST: Clock Test Mode Low: Test Mode. HIGH: *32kHz clock in normal tuning	MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: *Boot from ISA flash part
MY1	48	TP_PLL: DPLL Test Mode Low: Test Mode. HIGH: *Normal operation	MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: *Normal Mode



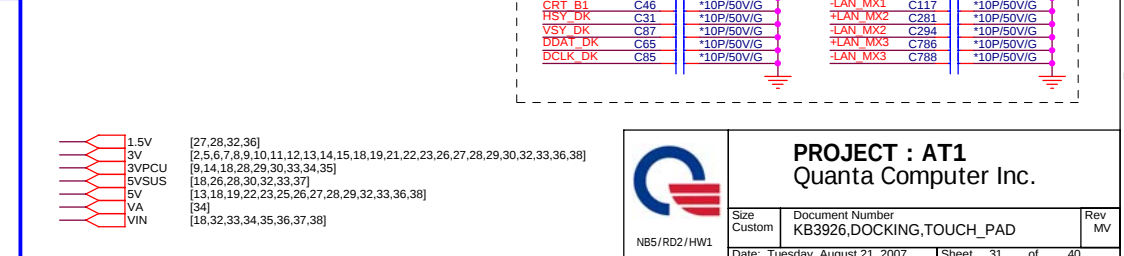
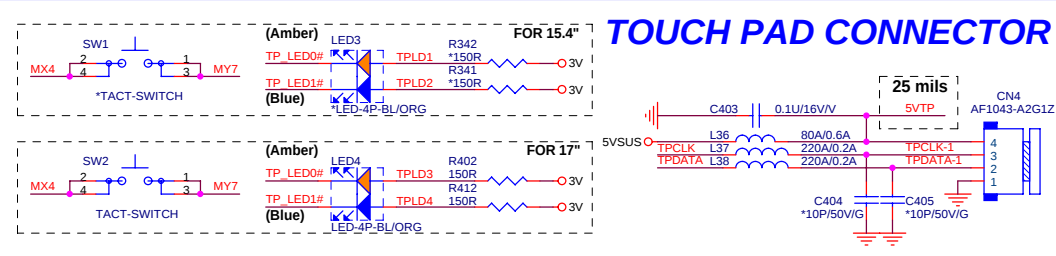
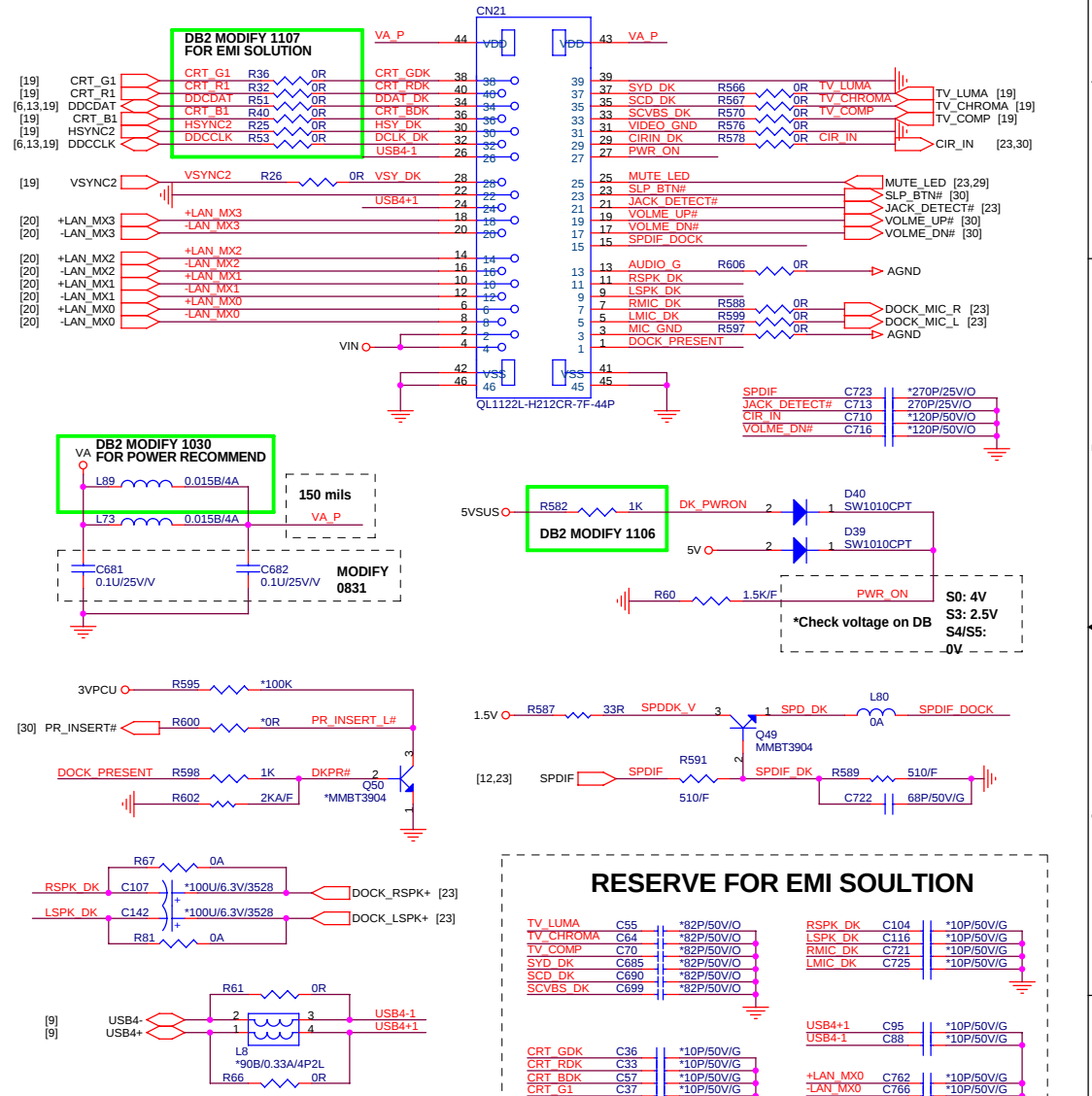
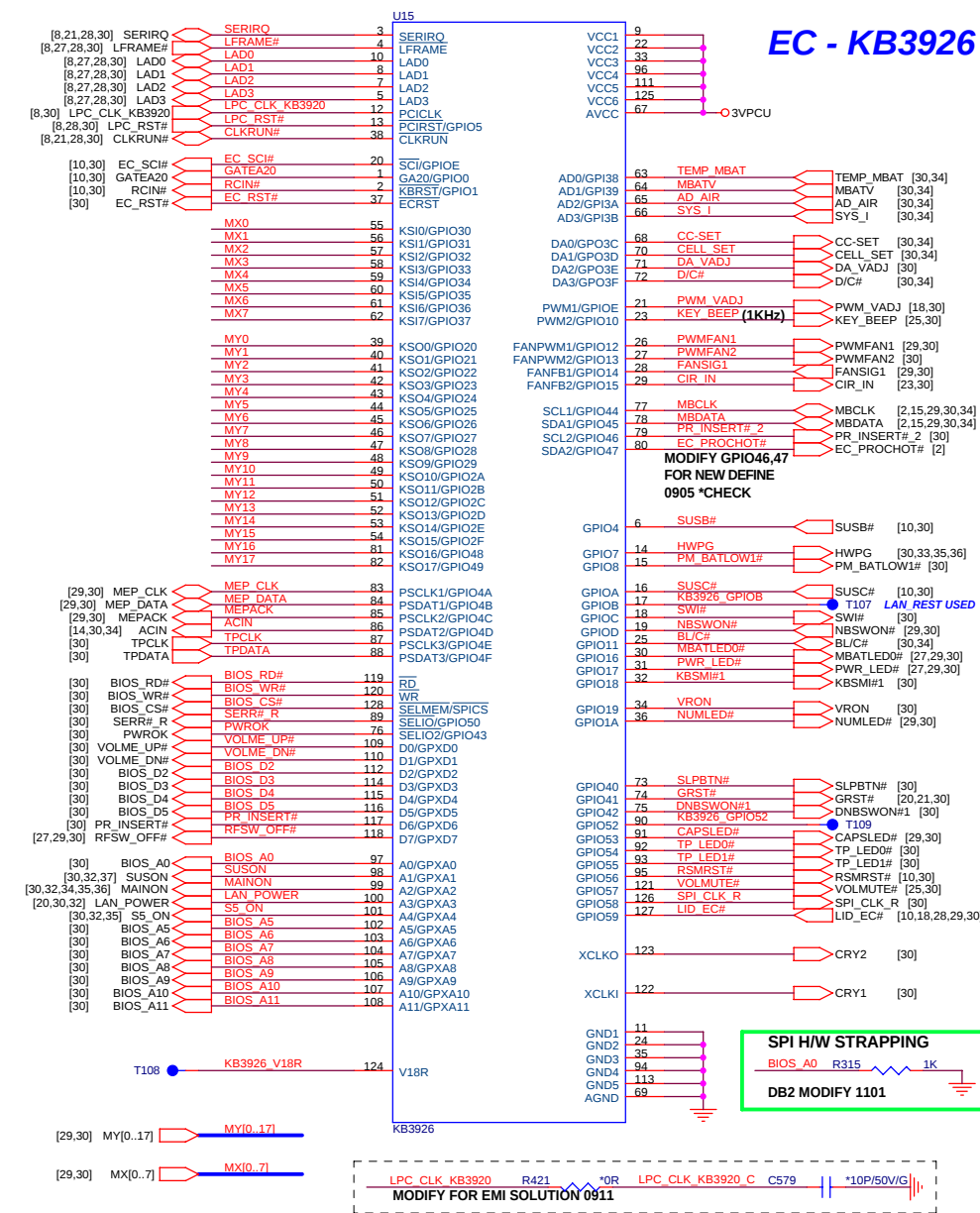
PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number KB3920_SPI_ROM	Rev MV
Date: Tuesday, August 21, 2007	Sheet 30 of 40	

3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,31,32,33,36,38]
3V_S5 [6,9,10,11,20,28,32,33,37]
3VPCU [9,14,18,28,29,31,33,34,35]
5VSUS [18,26,28,31,32,33,37]

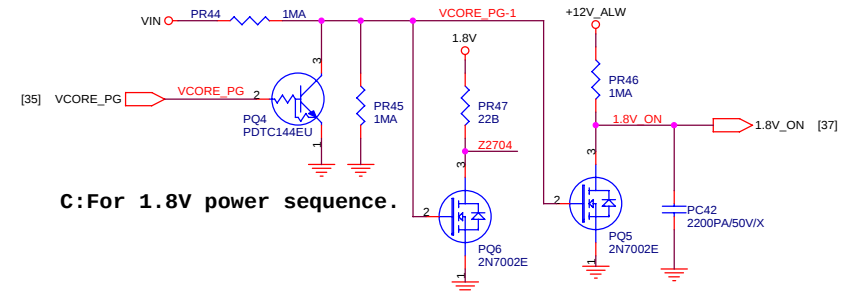
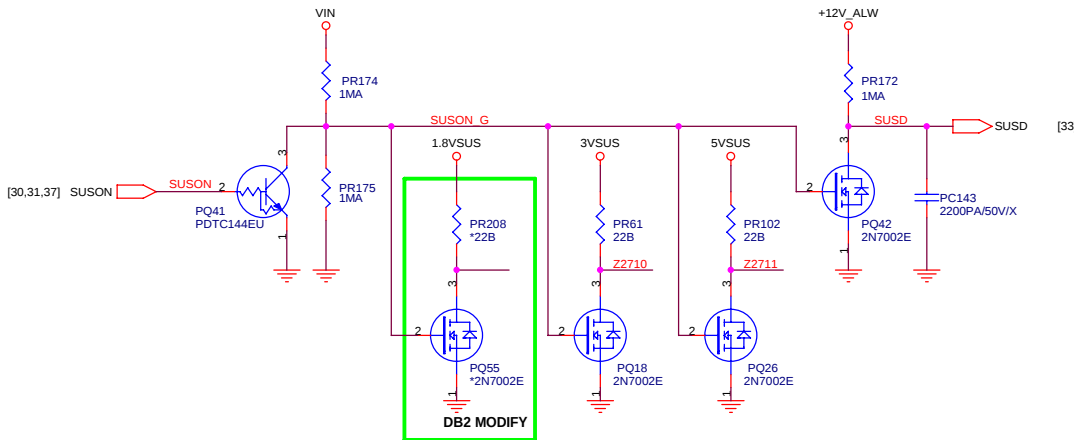
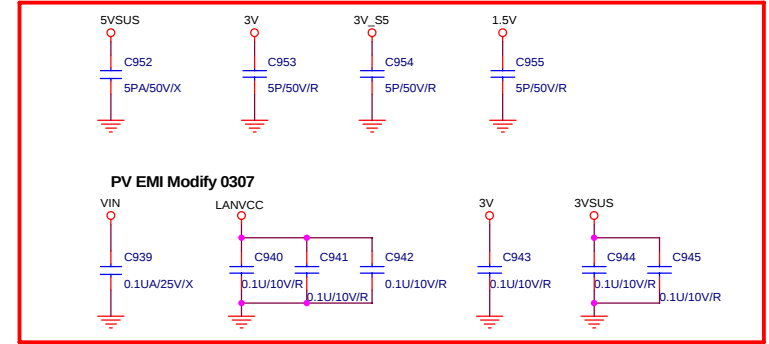
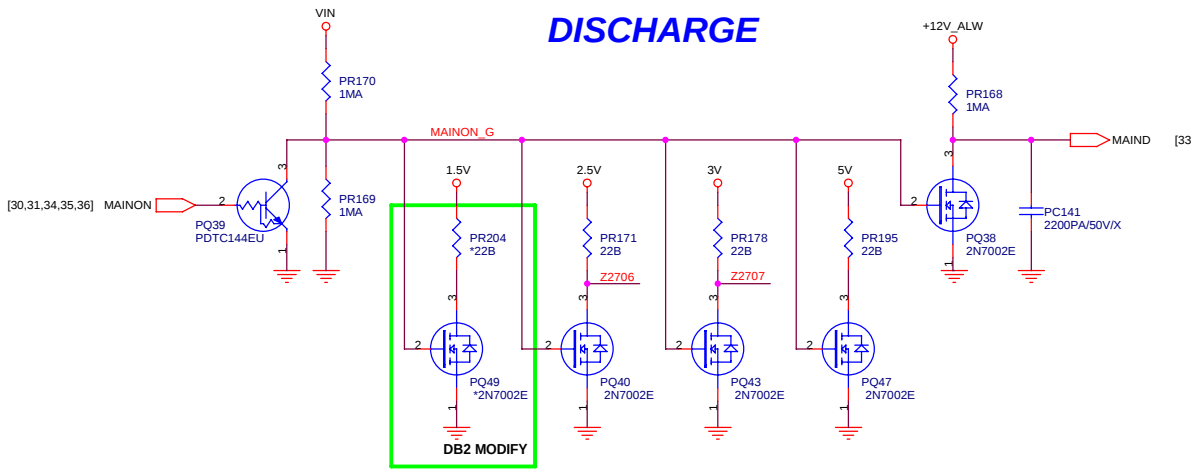
EC - KB3926

CABLE DOCK

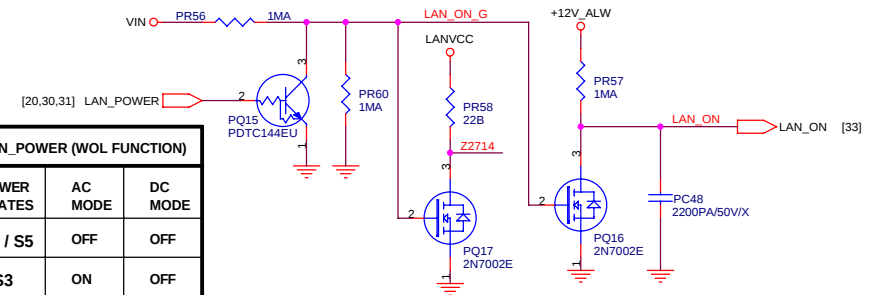


DISCHARGE

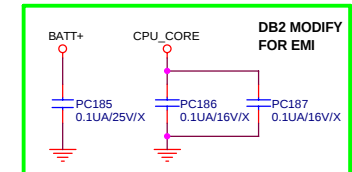
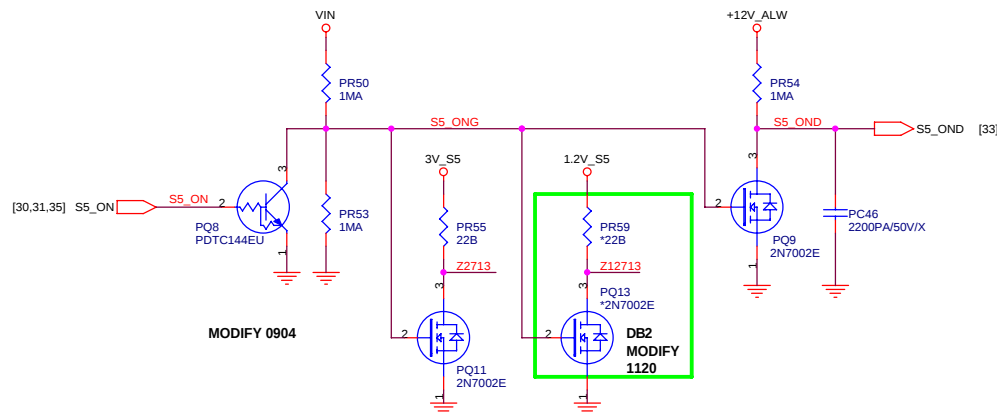
SI POWER MODIFY



C:For 1.8V power sequence.



LAN_POWER (WOL FUNCTION)		
POWER STATES	AC MODE	DC MODE
S4 / S5	OFF	OFF
S3	ON	OFF
S0	ON	ON



- CPU_CORE [4,38]
- 1.2V_S5 [10,11,35]
- 1.5V [27,28,31,36]
- 1.8V [11,13,15,16,17,37]
- 1.8VSUS [2,3,4,5,6,36,37]
- 2.5V [2,13,36]
- LANVCC [20,33]
- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,33,36,38]
- 3VSUS [27,28,29,33]
- 3V_S5 [8,9,10,11,20,28,30,33,37]
- 5V [13,18,19,22,23,25,26,27,28,29,31,33,36,38]
- 5VSUS [18,26,28,30,31,33,37]
- +12V_ALW [10,18,33]
- VIN [18,31,33,34,35,36,37,38]

DC/DC 3VPCU/ 5VPCU/ +12V_ALW

33

5 Volt +/- 5%

5VPCU
C/C:8A
P/C:10A

$V_{out}=0.7(Ra+Rb)/Rb$
Rb around 49.9k

$I_{lim} * MOSFET(R_{DS(on)}) = V_{ILIM}(mV) / 10$
 $V_{ILIM}(mV) = 5uA * R_{ILIM}$

TOPN: OUT1/OUT2
GND=400KHz/500KHz
REF = 400KHz /300KHz
VCC5=200KHz/300KHz

Place these CAPS
close to FETs

3.3 Volt +/- 5%
3VPCU
C/C:8A
P/C:10A

1A S0-S5
1.6A S0-S3

+12V_ALW [10,18,32]
LANVCC [20,32]
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,36,38]
3VSUS [27,28,29,32]
3V_S5 [8,9,10,11,20,28,30,32,37]
3VPCU [9,14,18,28,29,30,31,34,35]
5V [13,18,19,22,23,25,26,27,28,29,31,32,36,38]
5VSUS [18,26,28,30,31,32,37]
5VPCU [10,23,34,35,36,37,38]
VIN [18,31,32,34,35,36,37,38]



PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number ISL6236 (5VPCU,3VPCU)	Rev MV
Date: Tuesday, August 21, 2007	Sheet 33 of 40	

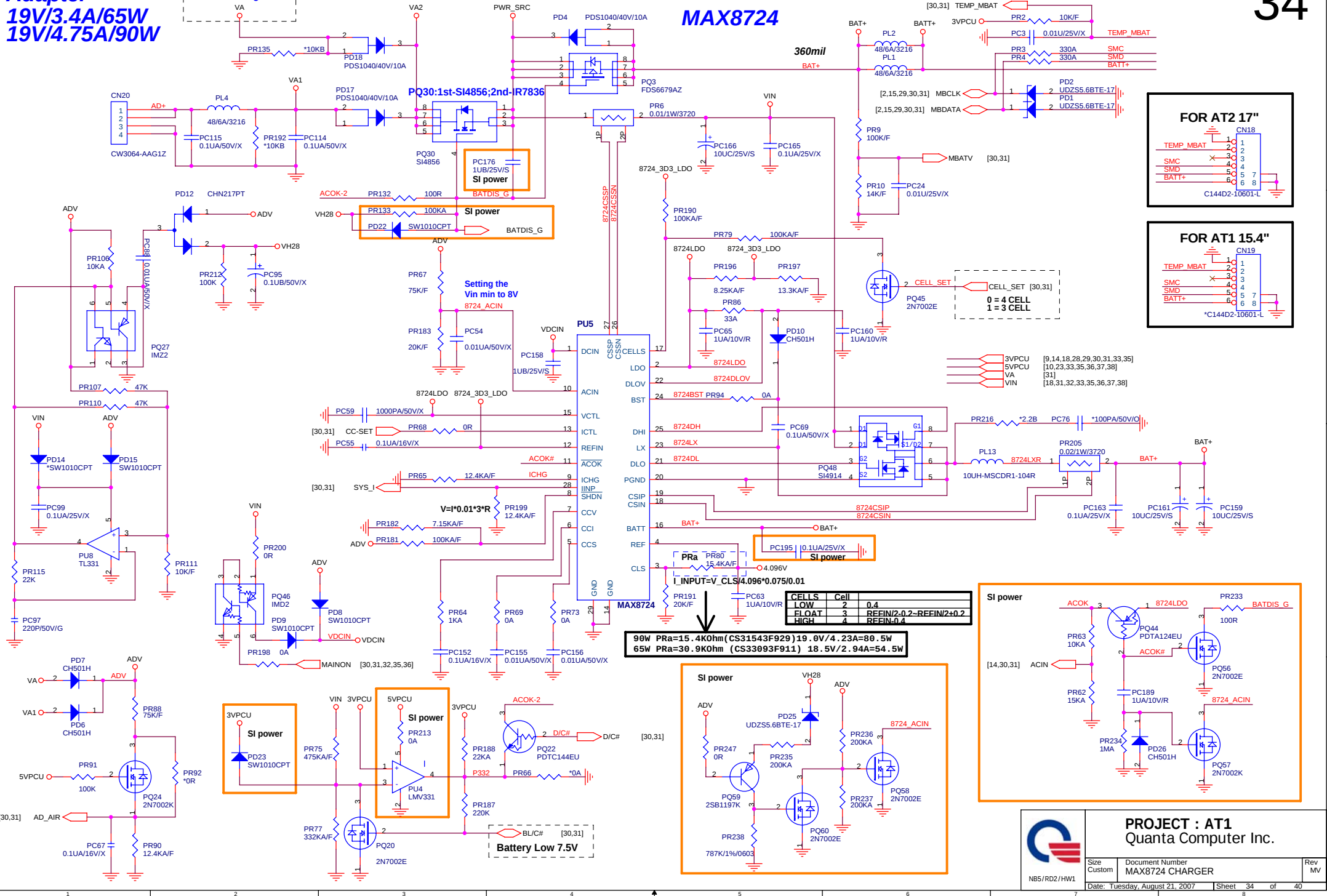
Adapter
19V/3.4A/65W
19V/4.75A/90W

From Docking CNN

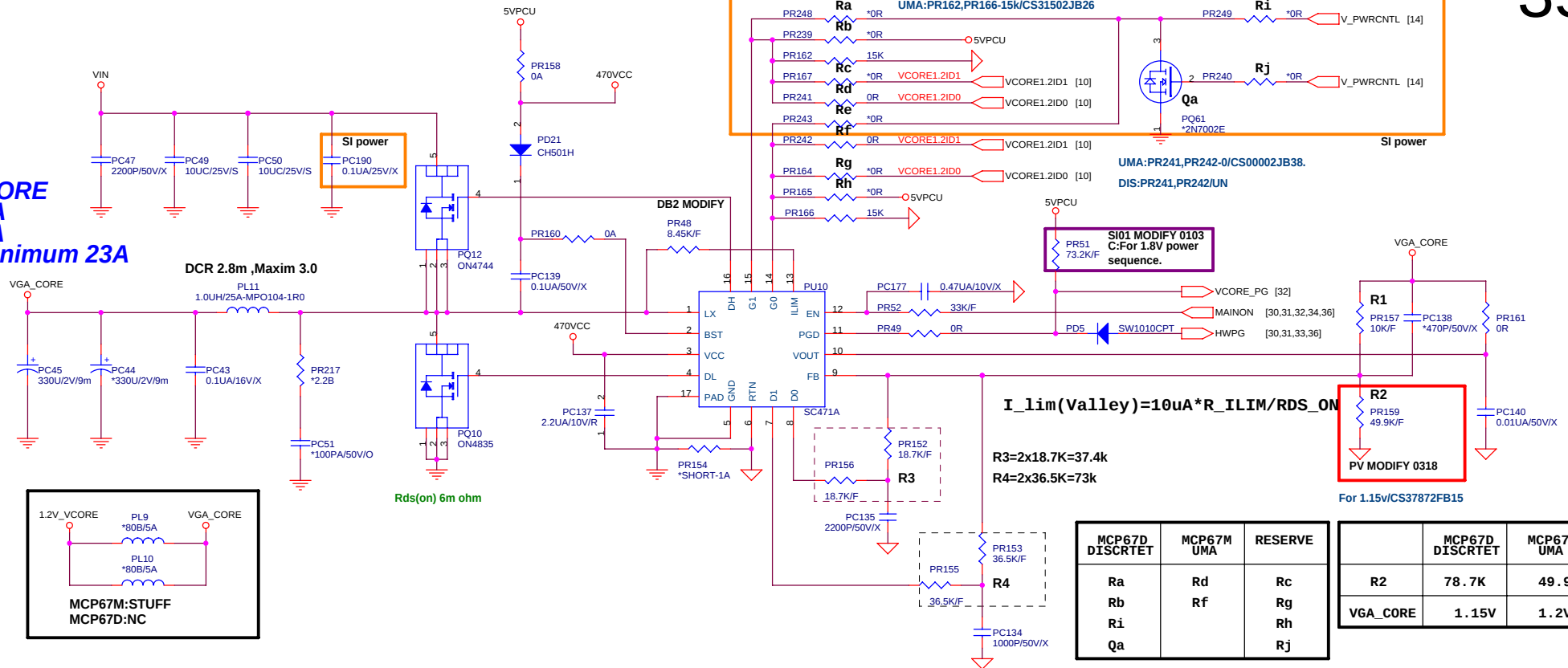
AT1: UN;AT2:install

Battery 6/8/12cell
MAX8724

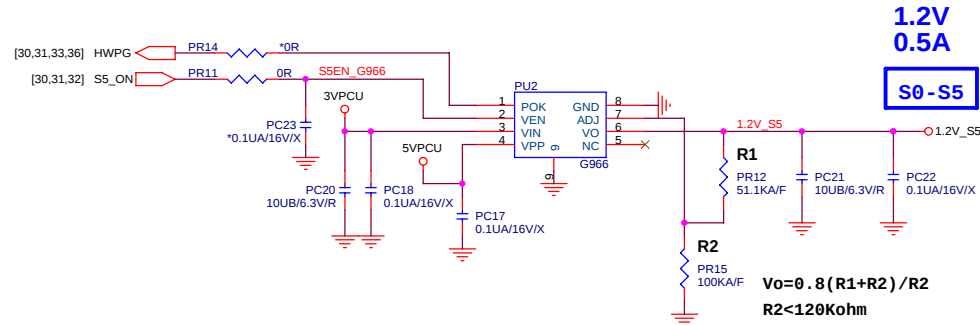
34



VGA_CORE
C/C:12A
P/C:15A
OCP minimum 23A



INPUTS		OUTPUTS			VGA_CORE
VCORE1.2ID1	VCORE1.2ID0	OD1	OD2	OD3	
0	0	$0.75 \times (1 + R1/R2 + R1/R3 + R1/R4)$			1.2V
0	1	$0.75 \times (1 + R1/R2 + R1/R3)$			1.1V
1	0	$0.75 \times (1 + R1/R2 + R1/R4)$			1.0V
1	1	$0.75 \times (1 + R1/R2)$			0.9V

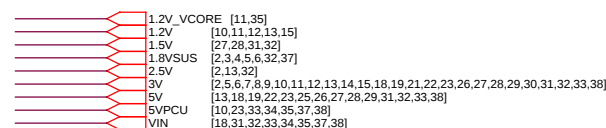


1.2V_S5 [10.11.32]
1.2V_VCORE [11.36]
VGA_CORE [12]
3VPCU [9.14.18.28.29.30.31.33.34]
5VPCU [10.23.33.34.36.37.38]
VIN [18.31.32.33.34.36.37.38]



PROJECT : AT1
Quanta Computer Inc.

Size Custom	Document Number SC471A (VGA_CORE) 1.2V_S5	Rev MV
Date: Tuesday, August 21, 2007	Sheet 35 of 40	



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Size Custom	Document Number MAX8774 (CPU_CORE)	Re M
Date: Tuesday, August 21, 2007		Sheet 38 of 40