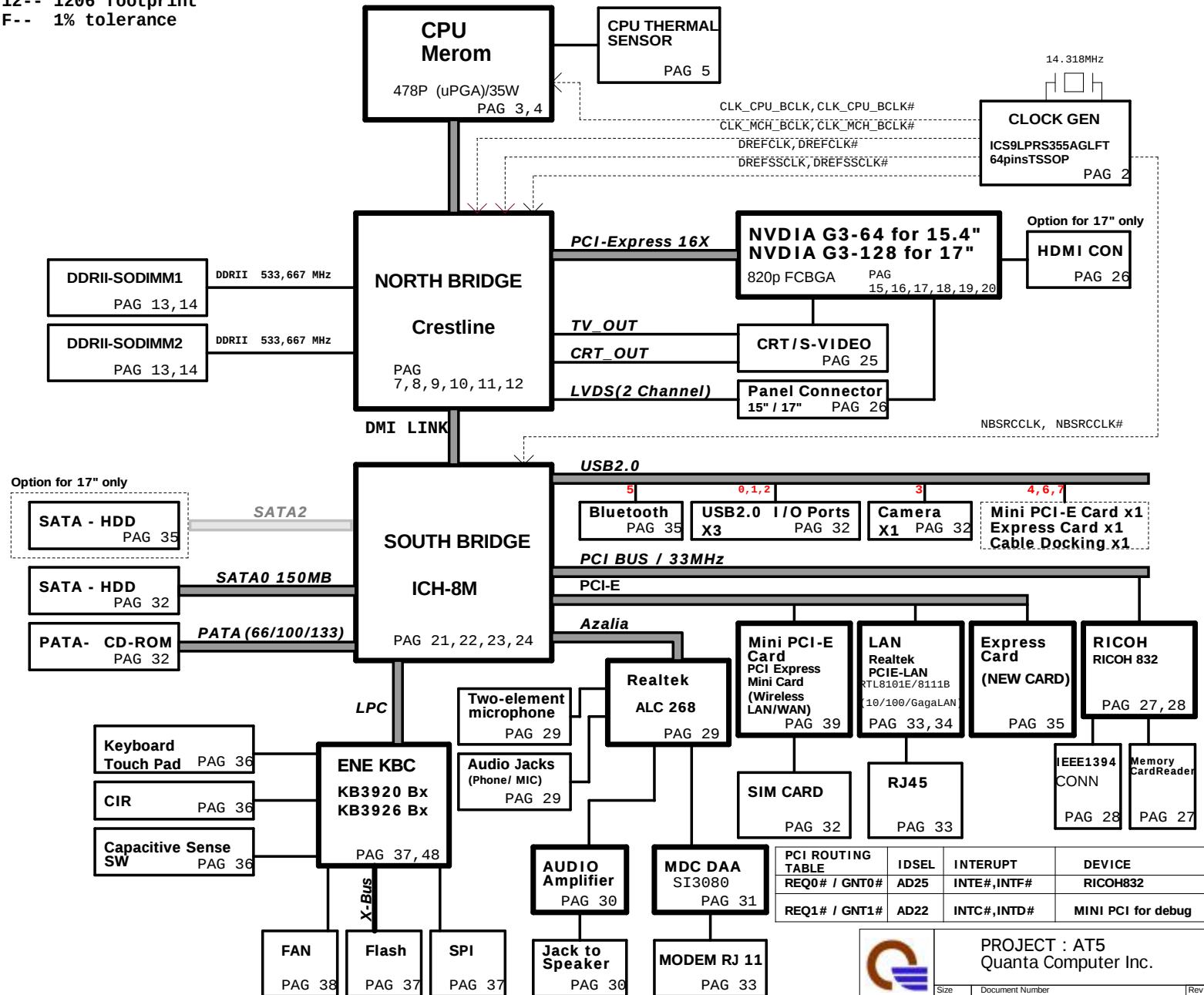


LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking	TV_OUT
	VGA
	RJ-45
	CIR/Pwr btn
	SPDIF Out
	Stereo MIC
	Headphone Jack
	USB Port
PAG 38	VOL Cntr

SYSTEM CHARGER(MAX8724)	PAG 41
SYSTEM POWER MAX8778	PAG 42
DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REG)	PAG 46
VCCP +1.5V AND GMCH 1.05V(MAX8717)	PAG 43
VGACORE(1.025V)MAX1992	PAG 45
CPU CORE MAX8771	PAG 44

01



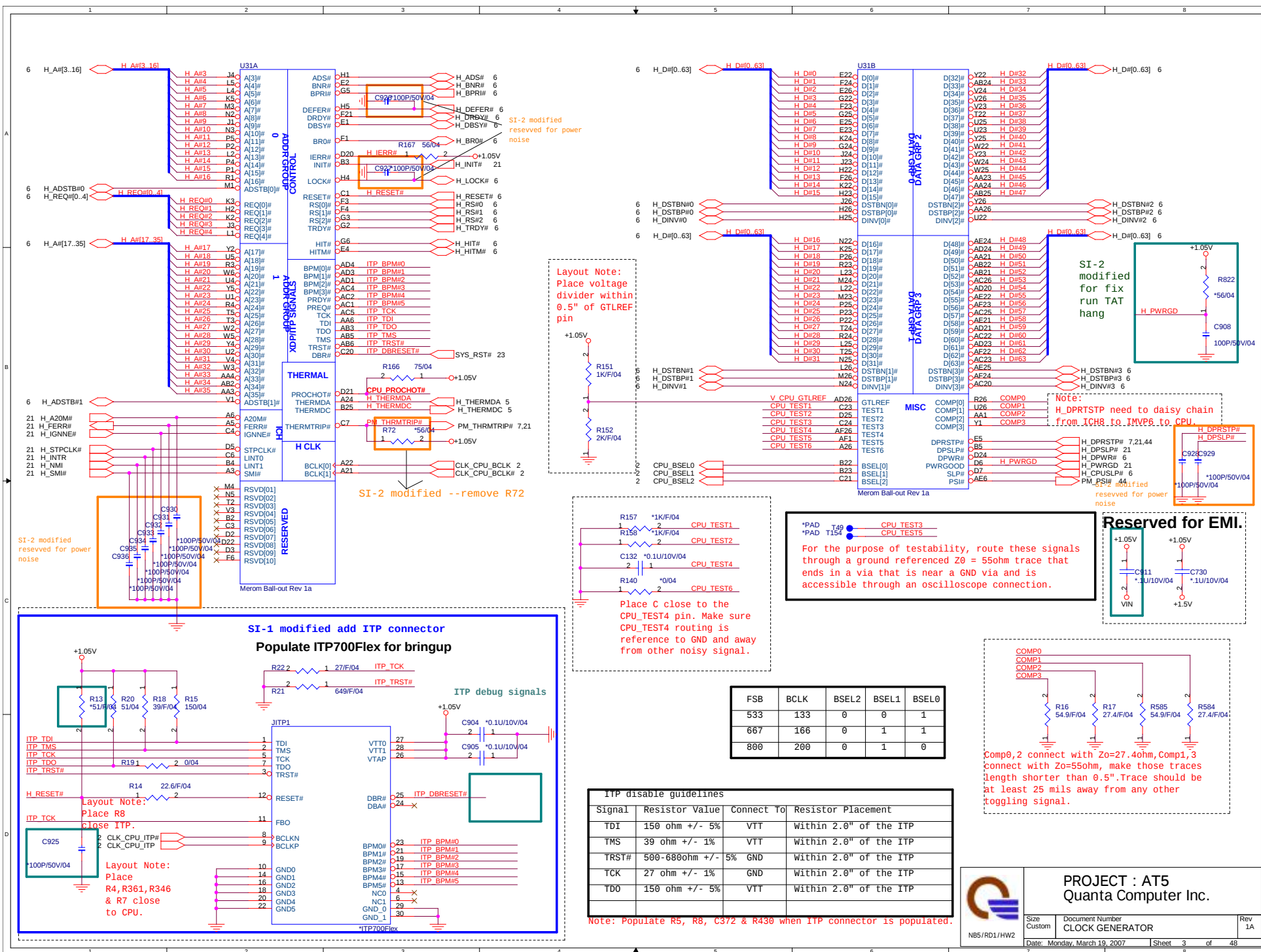
PROJECT : AT5
Quanta Computer Inc.

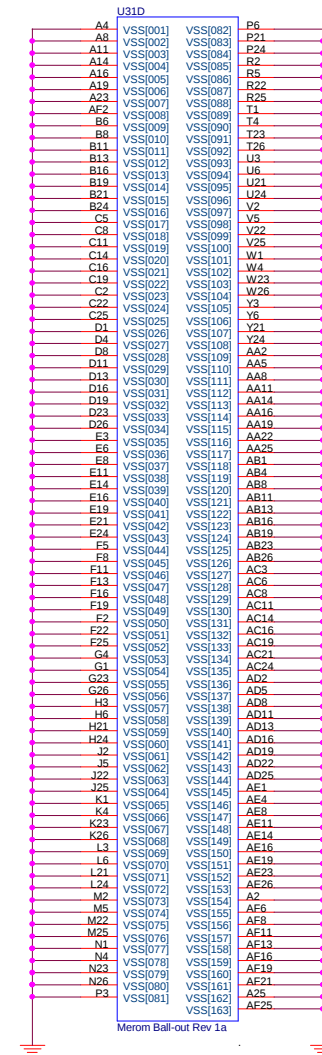
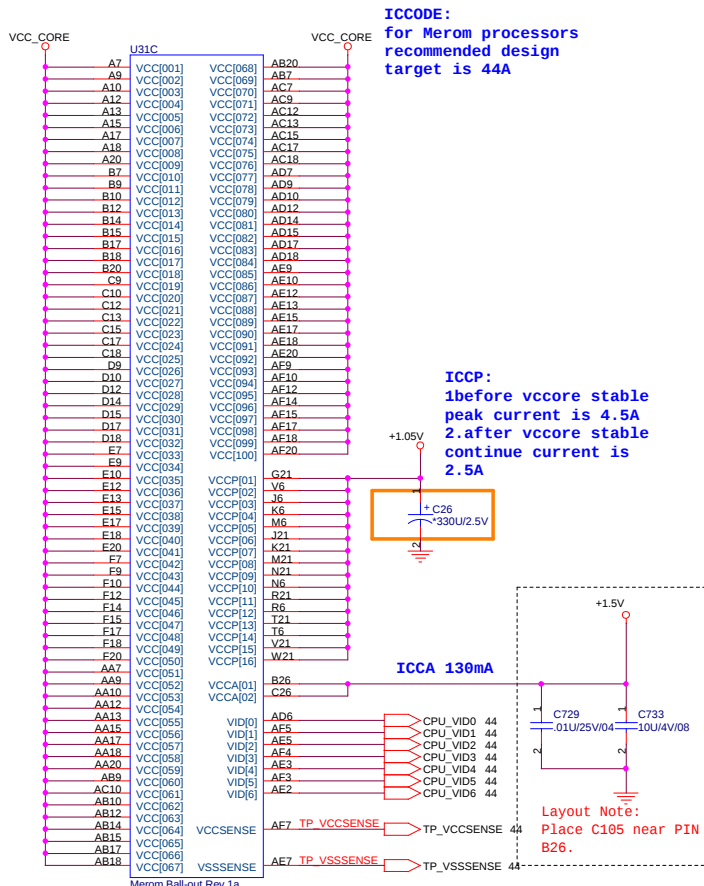
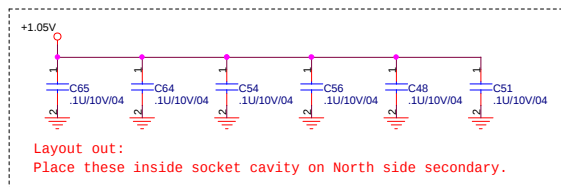
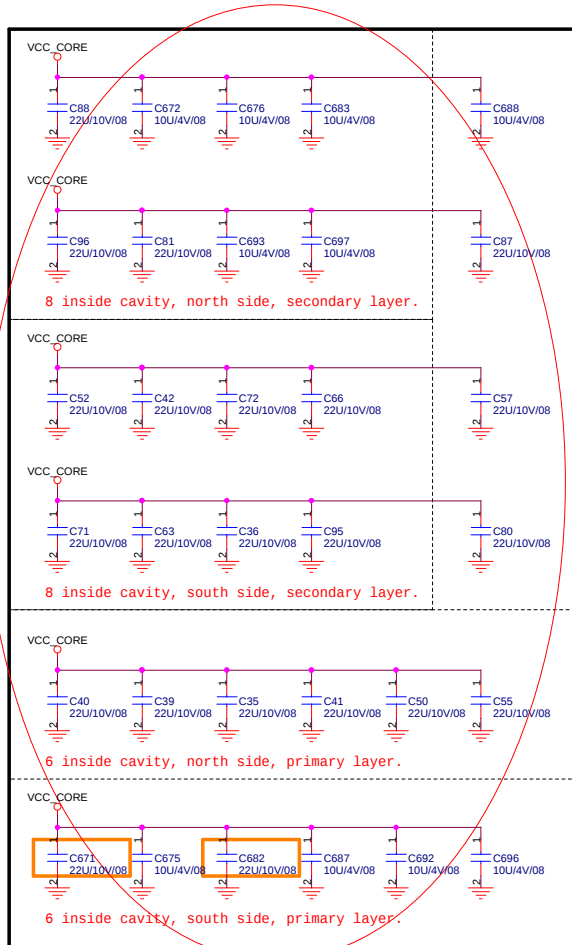
Size Custom	Document Number BLOCK DIAGRAM	Rev 1A
Date: Monday, March 19, 2007		Sheet 1 of 48



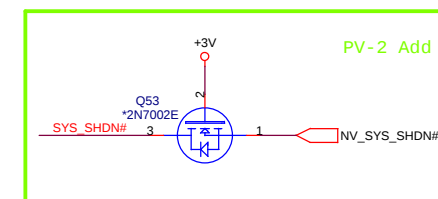
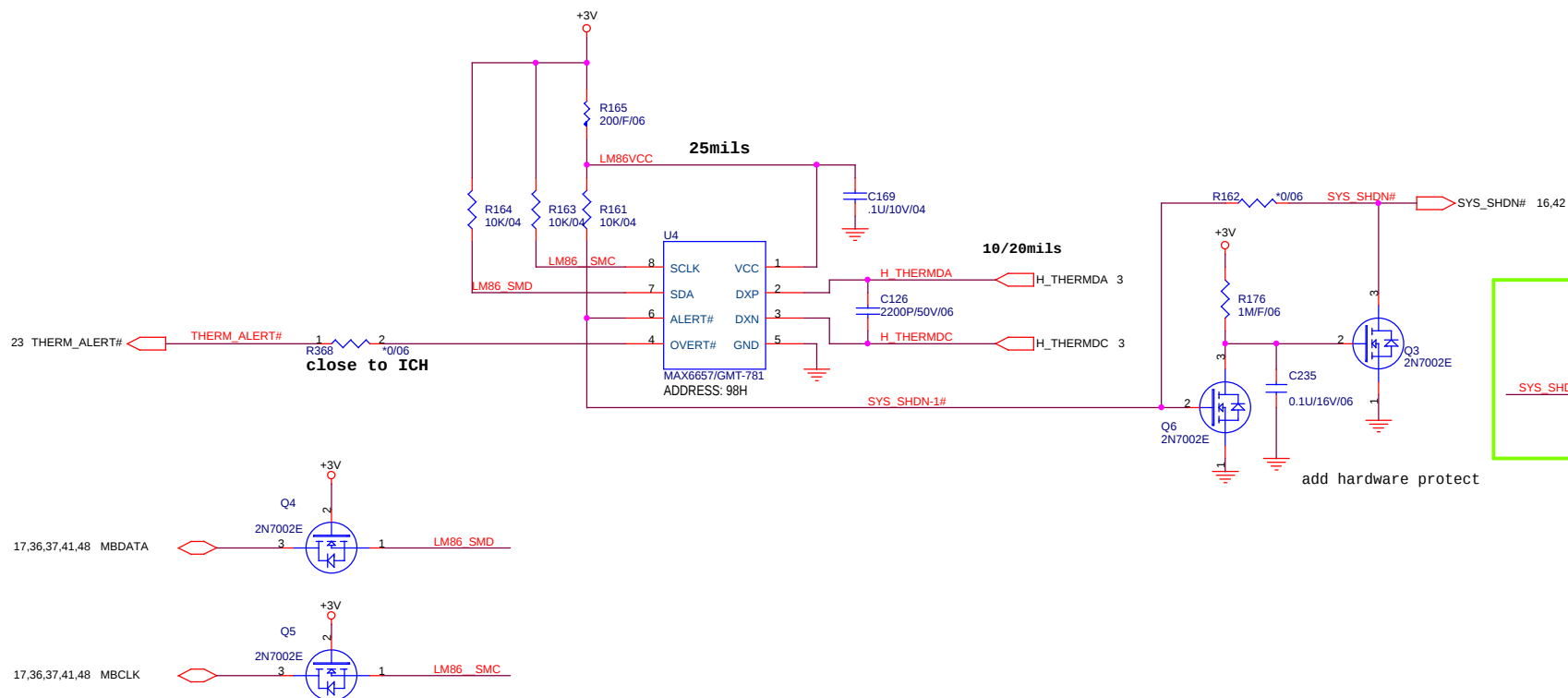
PROJECT : AT5
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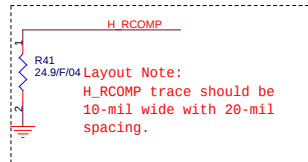
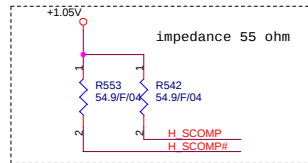
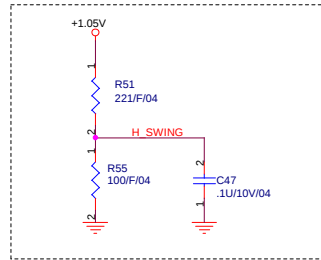
Size Custom	Document Number CLOCK GENERATOR	Re 1
Date: Monday, March 19, 2007	Sheet 2 of 48	



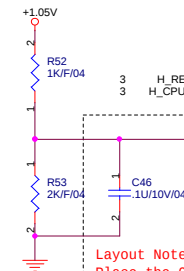


05

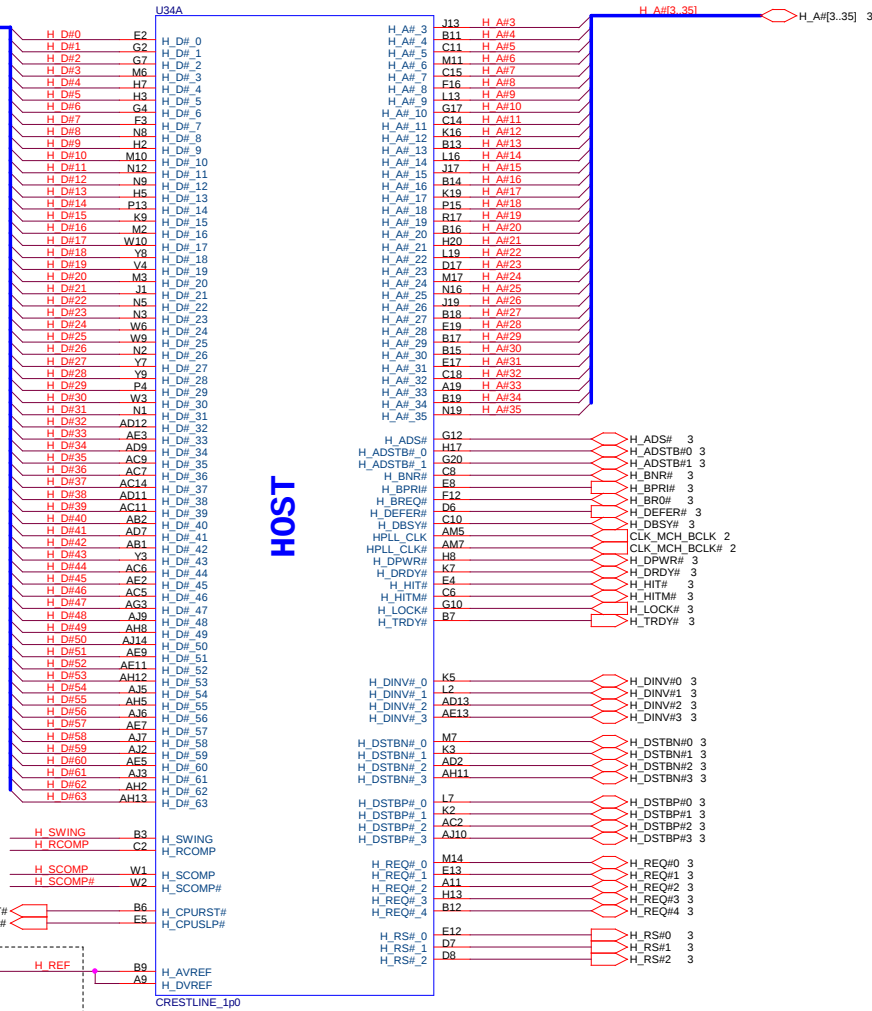




Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.

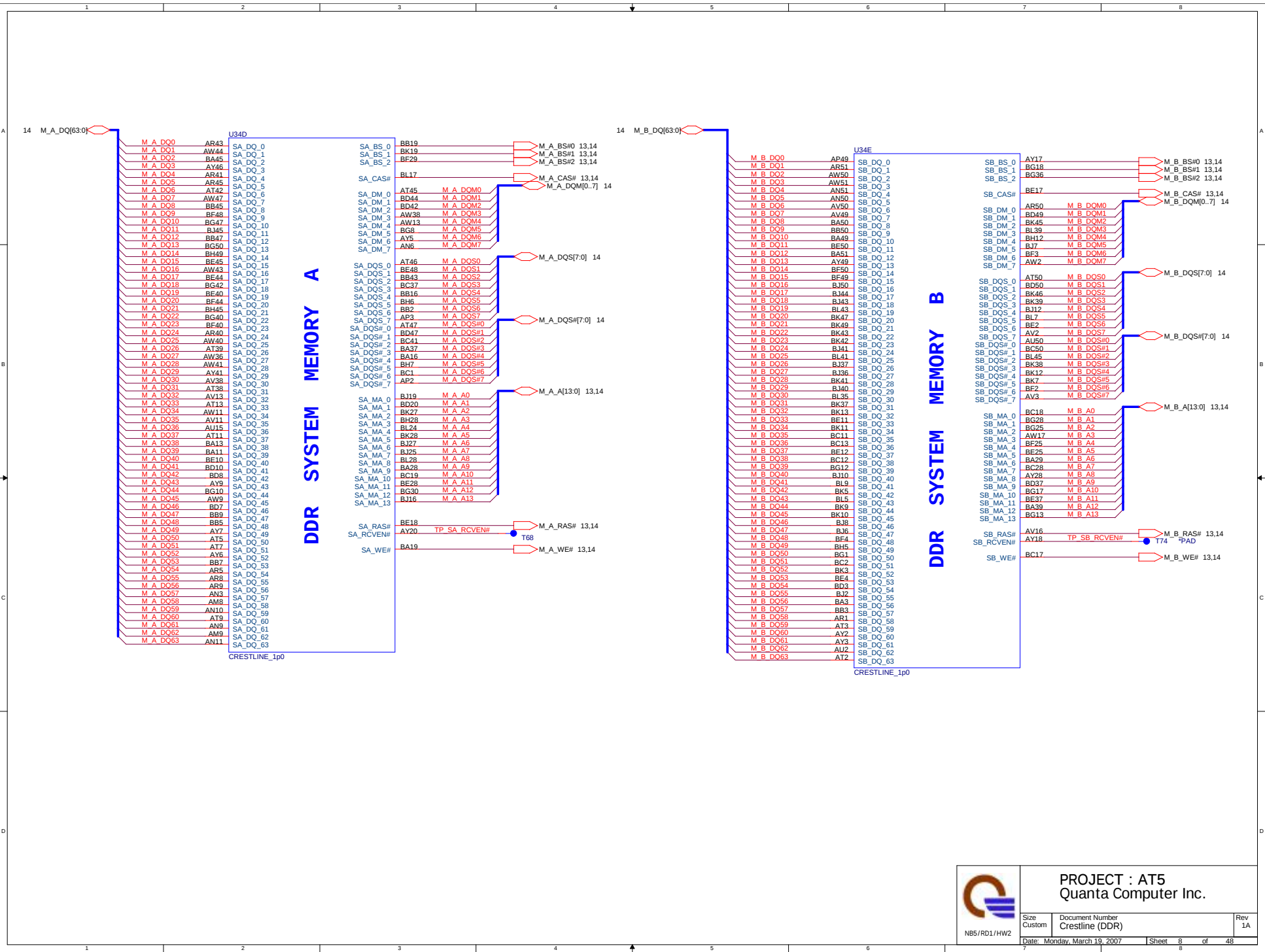


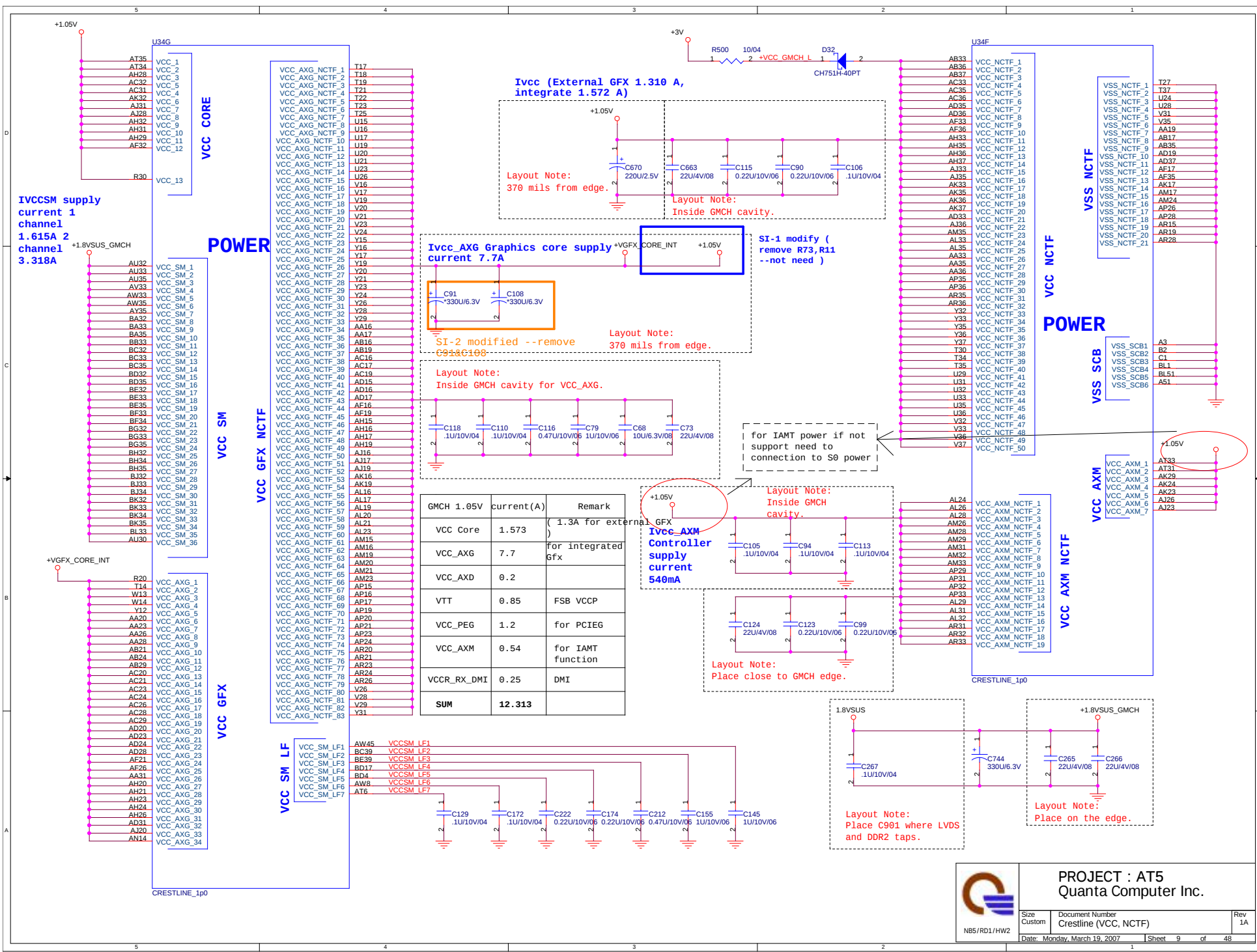
Layout Note:
Place the 0.1 uF
decoupling capacitor
within 100 mils from
GMCH pins.



PROJECT : AT5
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Size Custom	Document Number Crestline (HOST)	Rev 1A
Date: Monday, March 19, 2007	Sheet 6 of 48	

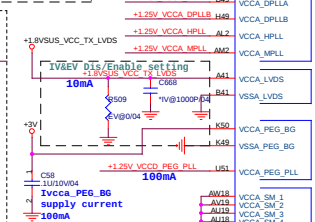
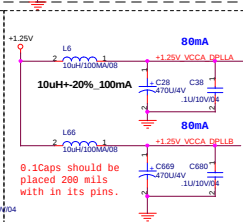
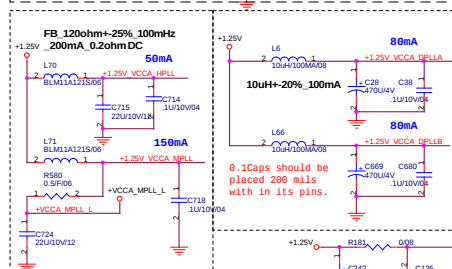
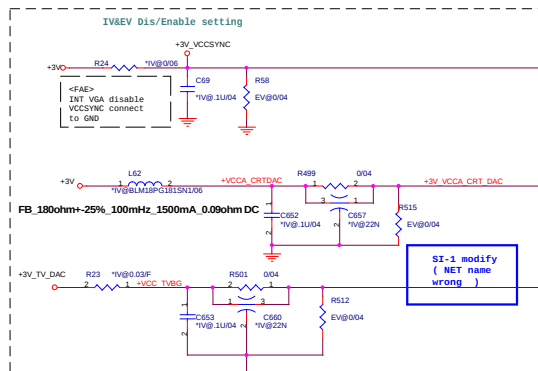




GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	12.313	



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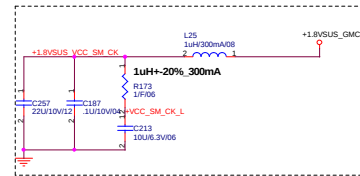
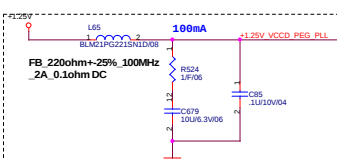
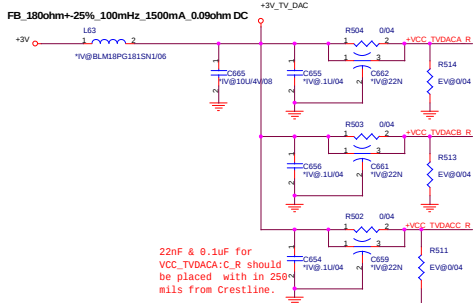
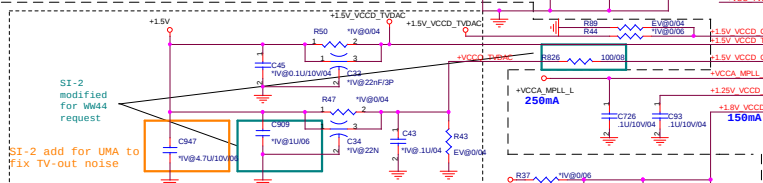
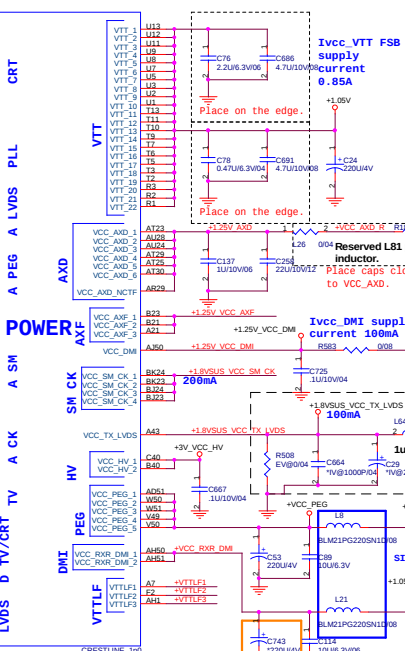
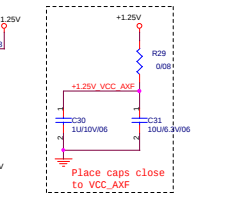
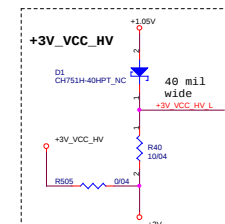


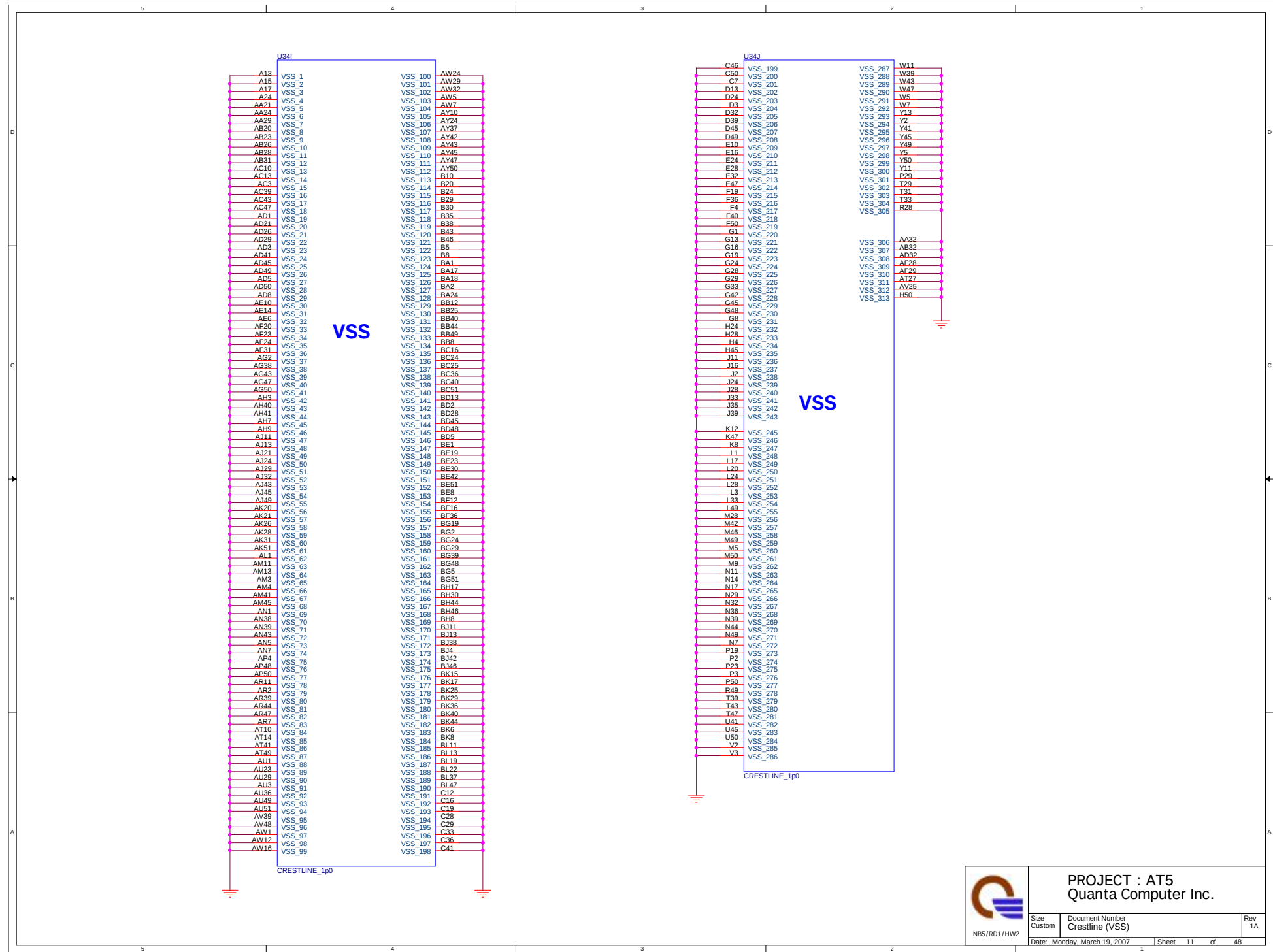
CRT/TV Dis/Enable guideline
External VGA with EV@part, Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TV_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TV_DAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TV_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TV_DAC	3.3V	GND	VCCSYNC	3.3V	GND

LVDS Dis/Enable guideline
External VGA with EV@part, Internal VGA with IV@ part

Signal	If SDVO Dis/Enable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V





PROJECT : AT5
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Size Custom	Document Number Crestline (VSS)	Rev 1A
Date: Monday, March 19, 2007	Sheet 11 of 48	

Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up

CFG[18:19] Have internal Pull-down

Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMX4(Default)
-----------	--------------------------------------

DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--

XOR /ALLz /Clock Un-gating

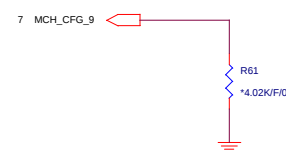
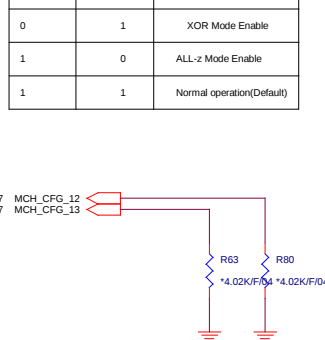
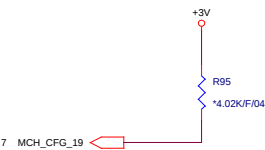
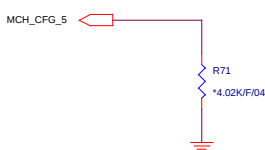
MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

SDVO Present

Strap define at External DVI control page

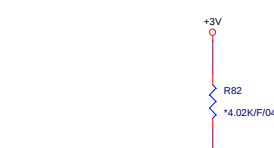
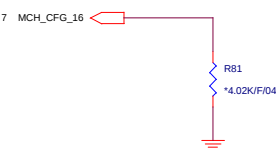


FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---

SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
------------	---

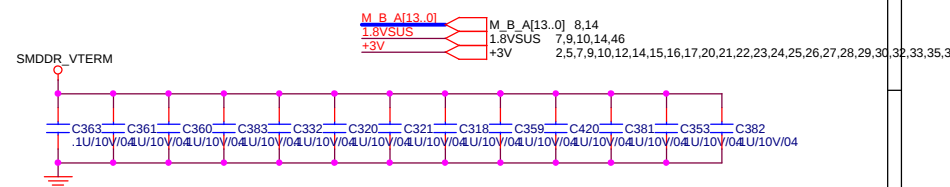


PROJECT : AT5
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Size Custom	Document Number 10 -- GMCH STRAP-3(6 of 6)	Rev 1A
Date: Monday, March 19, 2007	Sheet 12 of 48	

13

DDRII B CHANNEL



7.14 M_A_ODT0

M A ODT0

M A A18

M A A8

M A A5

M A A3

M A A1

RP21

RP13

RP14

1

3

1

3

2

4

56X2

56X2

56X2

56X2

SMDDR_VTMRM

7.14 M_A_CKE1

M A CKE1

M A A11

M A A10

M A BS#0

M A A7

M A A6

M A A2

M A A4

RP23

RP15

RP24

RP18

1

3

1

3

2

4

56X2

56X2

56X2

56X2

SMDDR_VTMRM

8.14 M_A_BS#0

M A BS#1

M A A9

M A A12

RP22

RP16

1

3

1

3

2

4

56X2

56X2

SMDDR_VTMRM

8.14 M_A_RAS#

M A BS#1

M A A9

M A A12

RP22

RP16

1

3

1

3

2

4

56X2

56X2

SMDDR_VTMRM

8.14 M_A_WE#

M A CAS#

RP16

1

3

2

4

56X2

SMDDR_VTMRM

7.14 SA_MA14

SB_MA14

R742

R743

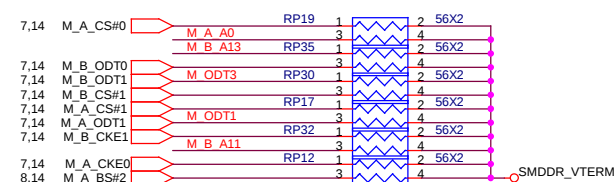
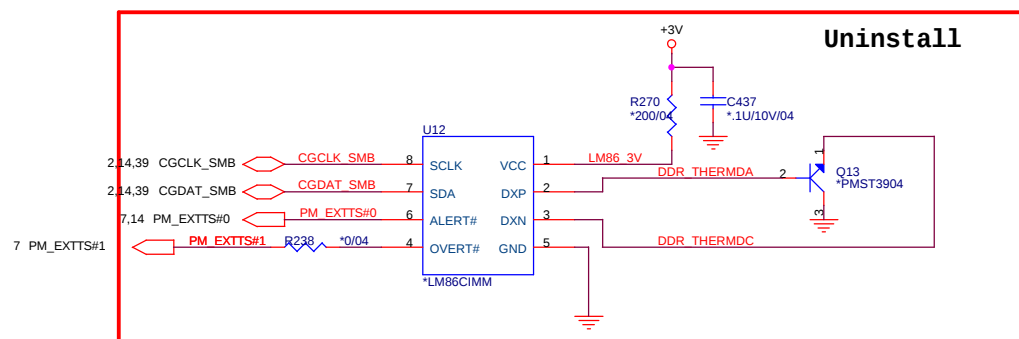
56/04

56/04

SI-1 m (add)

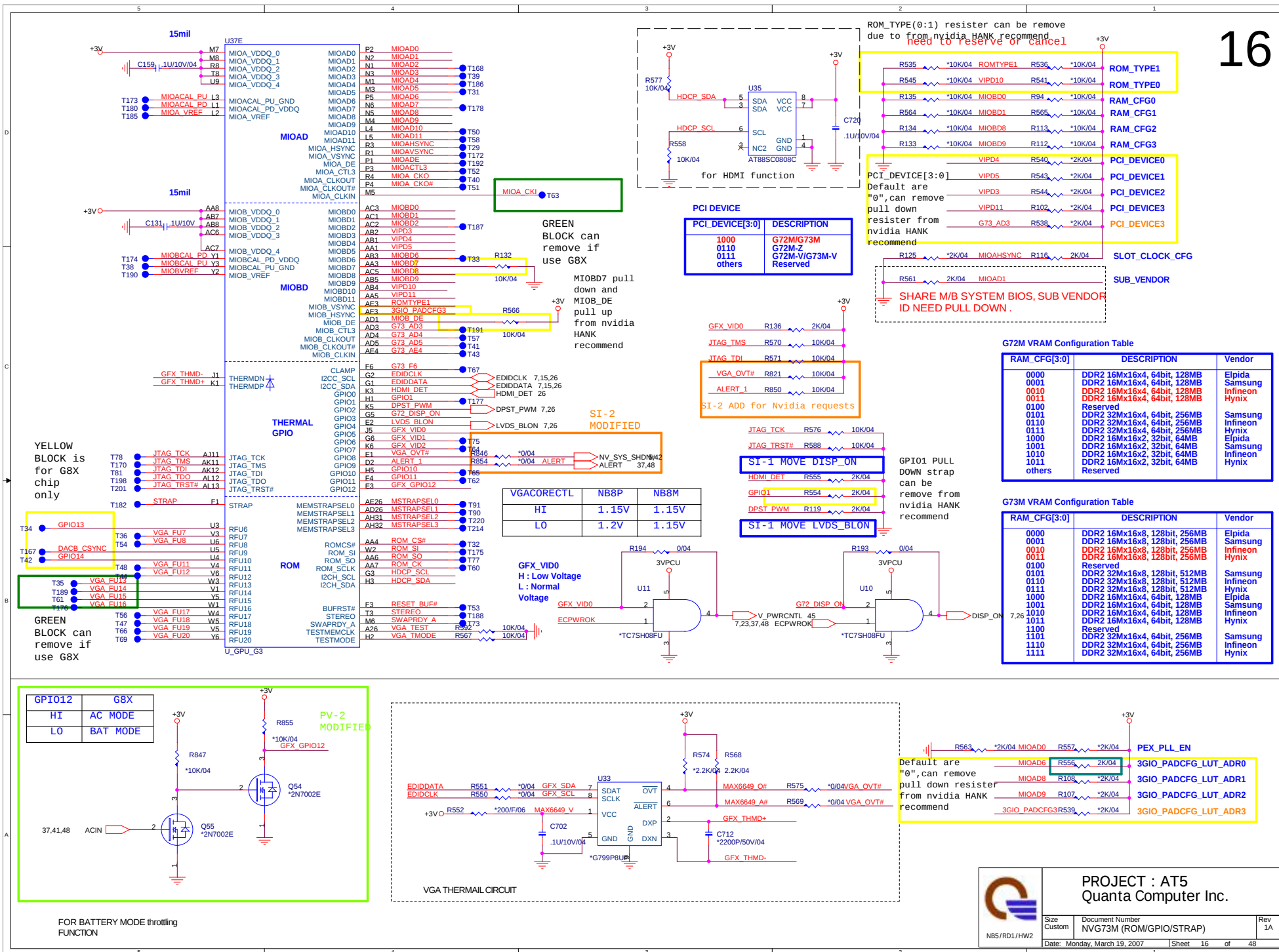
Timing diagram for SMDRR_VTERM signal. The diagram shows multiple input signals (M_B_BS#1, M_B_BS#2, M_B_CKE0, M_B_RAS#, M_B_CS#0, M_B_BS#0, M_B_CAS#, M_B_WE#) and their corresponding output signals (M_B_A0, M_B_A5, M_B_A1, M_B_A8, M_B_A3, M_B_A4, M_B_A2, M_B_A12, M_B_A9, M_B_A7, M_B_A6, M_B_A10) connected to a central block labeled RP37, RP27, RP26, RP36, RP25, RP33, RP31, RP34, RP29, and RP28. The output signals are shown as a series of pulses, with the SMDRR_VTERM signal being the final output. The diagram includes a legend for the signals and a table of signal names and values.

Signal Name	Value
M_B_BS#1	1
M_B_BS#2	1
M_B_CKE0	1
M_B_RAS#	1
M_B_CS#0	1
M_B_BS#0	1
M_B_CAS#	1
M_B_WE#	1



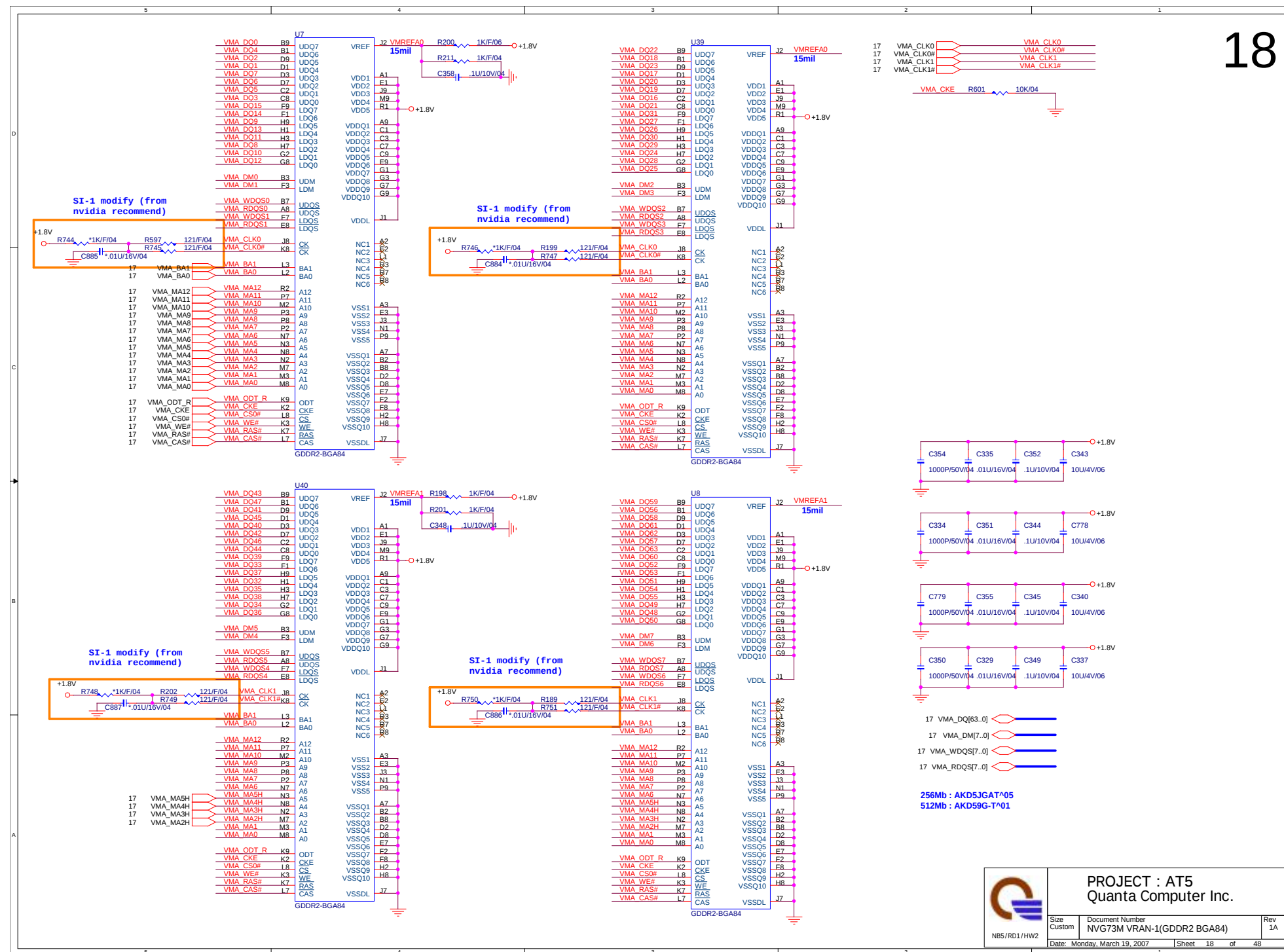
PROJECT : AT5
Quanta Computer Inc.

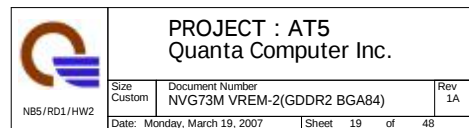
Size B	Document Number DDR II RES.ARRAY	Rev 1A
Date: Monday, March 19, 2007	Sheet 13 of 48	

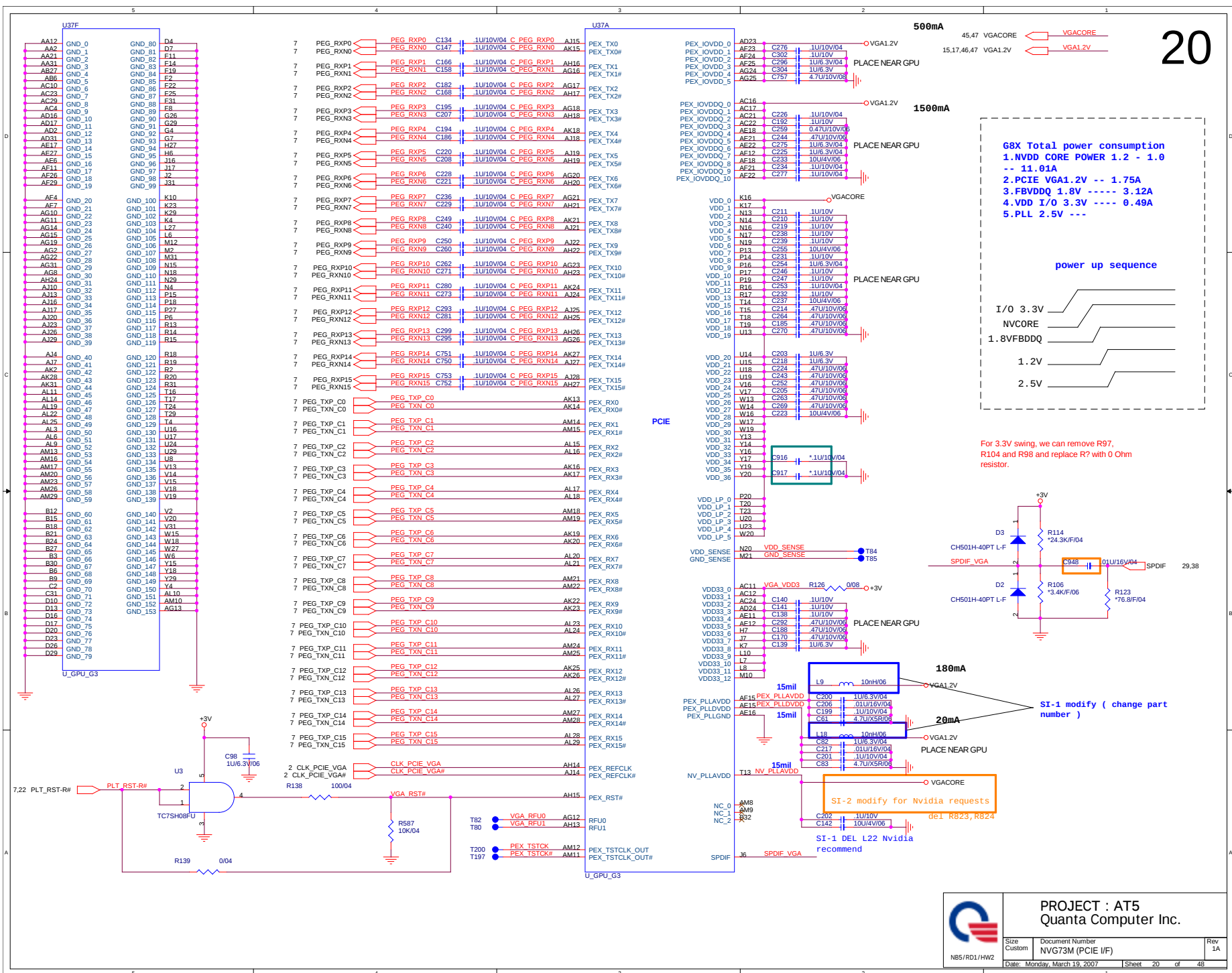




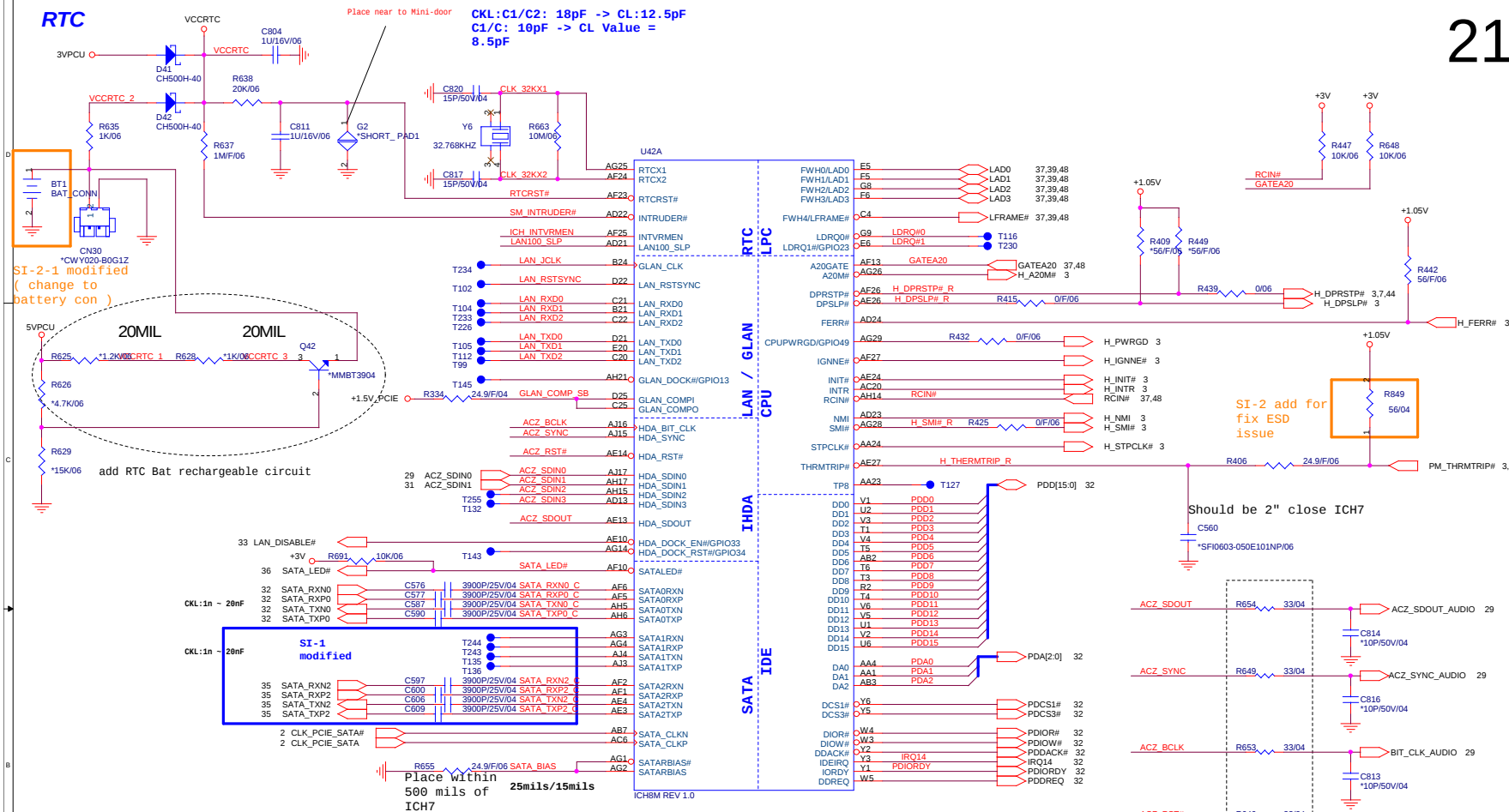
Size Custom	Document Number NVG73M (MEM I/F)	Rev 1A
Date: Monday, March 19, 2007	Sheet 17 of 48	







RTC



SB Strap

ICB8-M Internal VR Enable Strap
(Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

ICB8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

intel check list
define to stuff
330hm



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Size Custom	Document Number ICH7-M HOST(1/4)	Rev 1A
Date: Monday, March 19, 2007	Sheet 21 of 48	

MINI CARD PCI-E
EXPRESS CARD (NEW CARD)

SI-2 Add
for support
RBS0N
card

PCI-E-LAN

PCI-Express
Direct Media Interface

SPI

USB

ICH8M REV 1.0

28,40 AD[0..31]

PCI

Interrupt I/F

ICH8M REV 1.0

25mils/15mils
Place within 500
mils of ICH8

USB Connector
USB Connector
FINGERPRINT
Carama USB
Docking
SI-2-1
swaped
for fix
dash
issue
NEW CARD
USB Connector
USB Connector

A16 SWAP Override strap

PCI_GNT#3 Low = A16 swap override enabled
High = Default

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

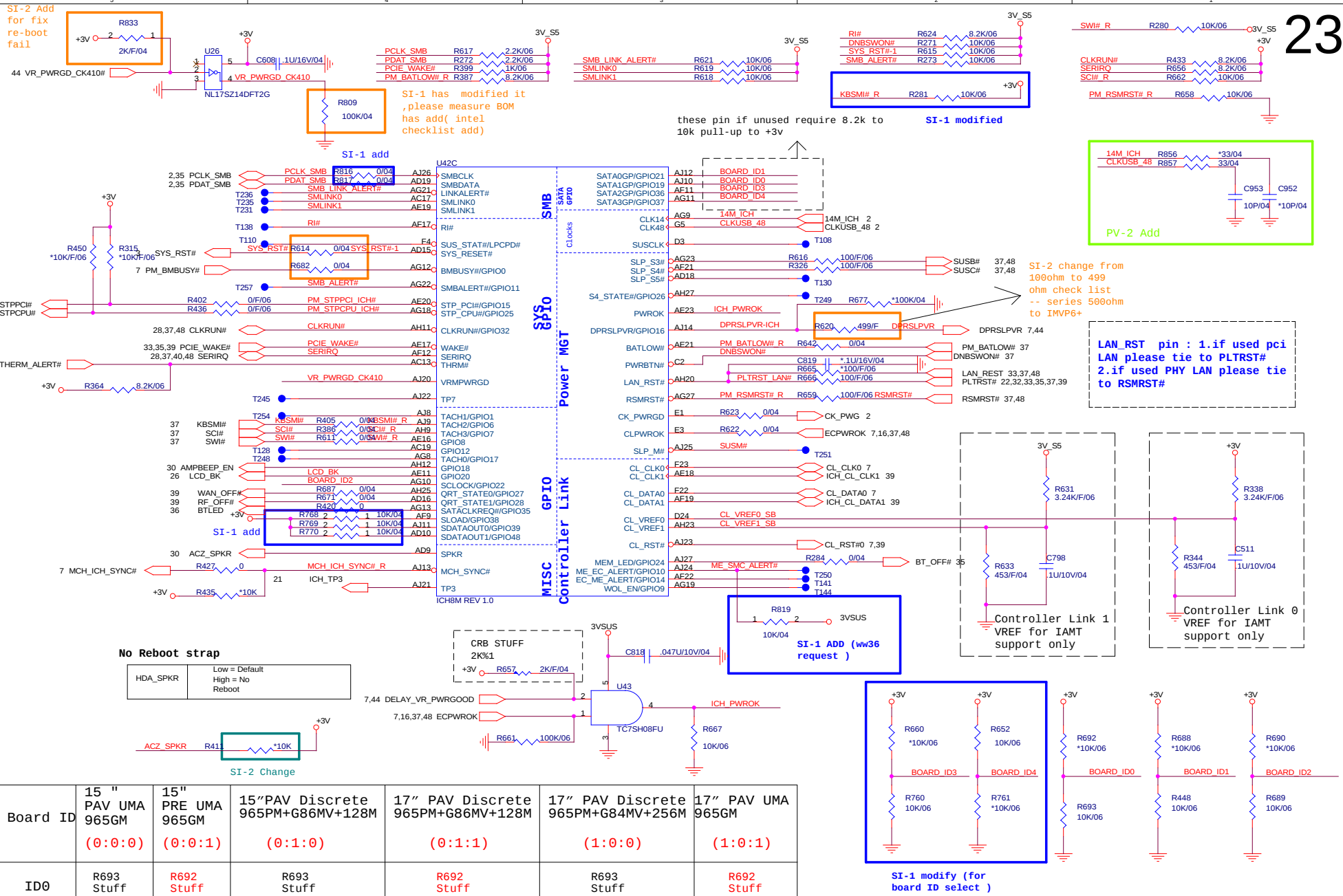
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#.,INTD#	MINI PCI for debug

Don't connect to PCI device / Express card

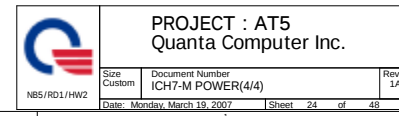


PROJECT : AT5
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Size Custom Document Number ICH7-M M PCI E(2/4) Rev 1A
Date: Monday, March 19, 2007 Sheet 22 of 48



Board ID	15" PAV UMA 965GM	15" PRE UMA 965GM	15"PAV Discrete 965PM+G86MV+128M	17" PAV Discrete 965PM+G86MV+128M	17" PAV Discrete 965PM+G84MV+256M	17" PAV UMA 965GM
	(0:0:0)	(0:0:1)	(0:1:0)	(0:1:1)	(1:0:0)	(1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R690 Stuff	R690 Stuff



CRT PORT

25

SI-1 modified
for fix CRT
rise time
issue

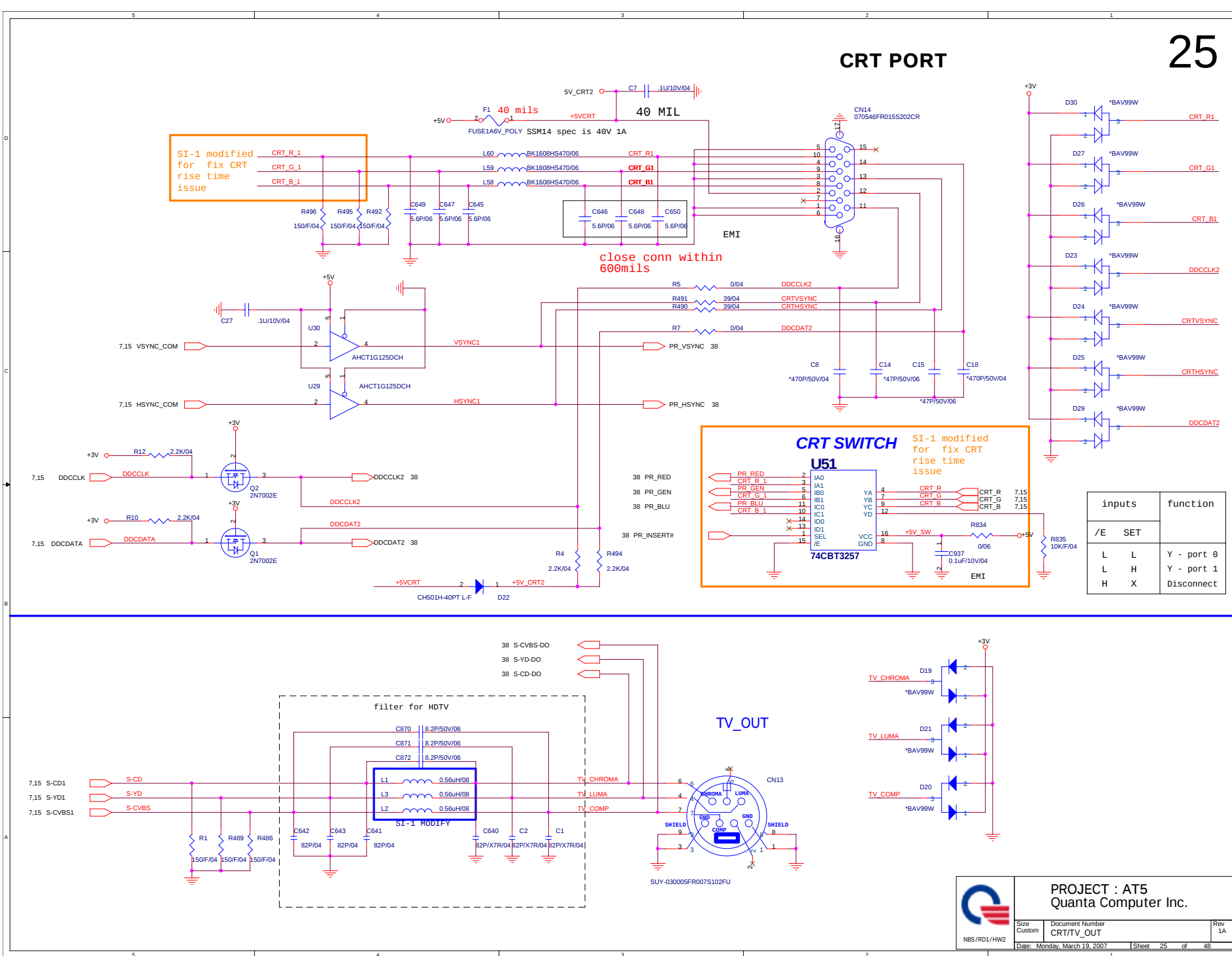
5V_CRT2 C7 1U/10V/04
+5V F1 40 mils
FUSE1A6V_POLY SSM14 spec is 40V 1A
+5VCRT
40 MIL

close conn within
600mils

CRT SWITCH

SI-1 modified
for fix CRT
rise time
issue

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

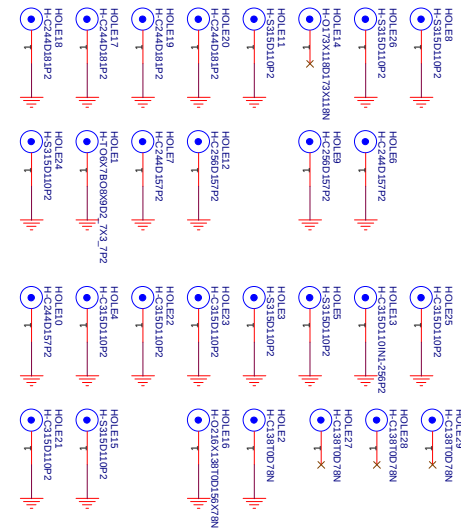


PROJECT : AT5
Quanta Computer Inc.

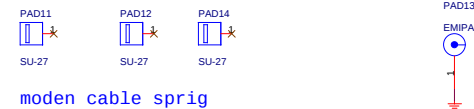
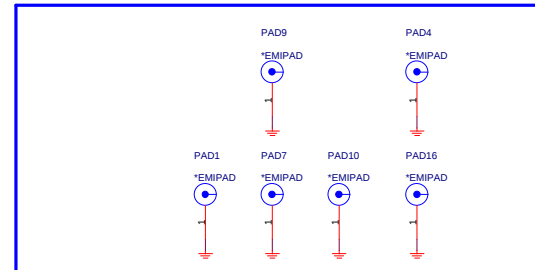
Size Custom	Document Number CRT/TV_OUT	Rev 1A
Date: Monday, March 19, 2007 Sheet 25 of 48		

5 IN1 CARD READER XD, MMC/SD, MS/MSP

SCREW HOLE

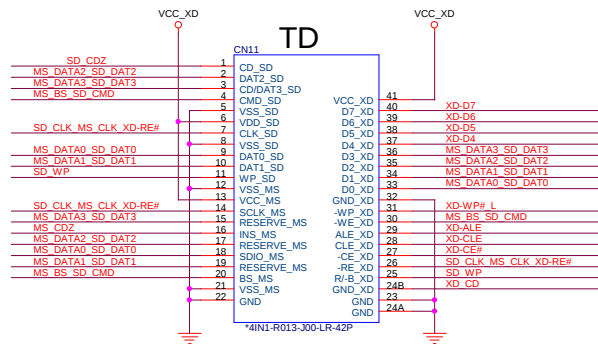
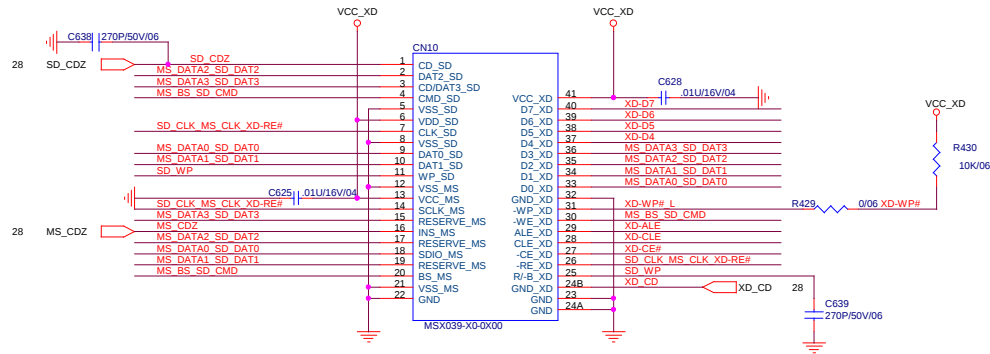


EMI PAD

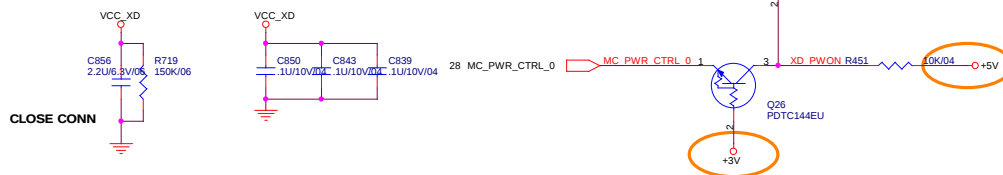
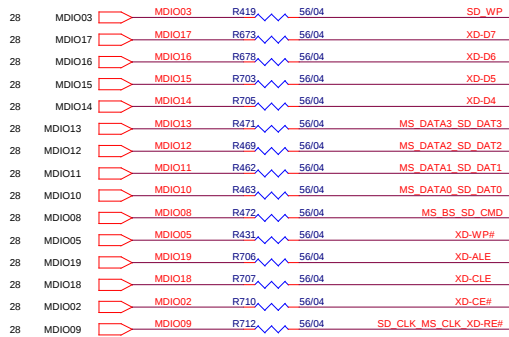


moden cable sprig

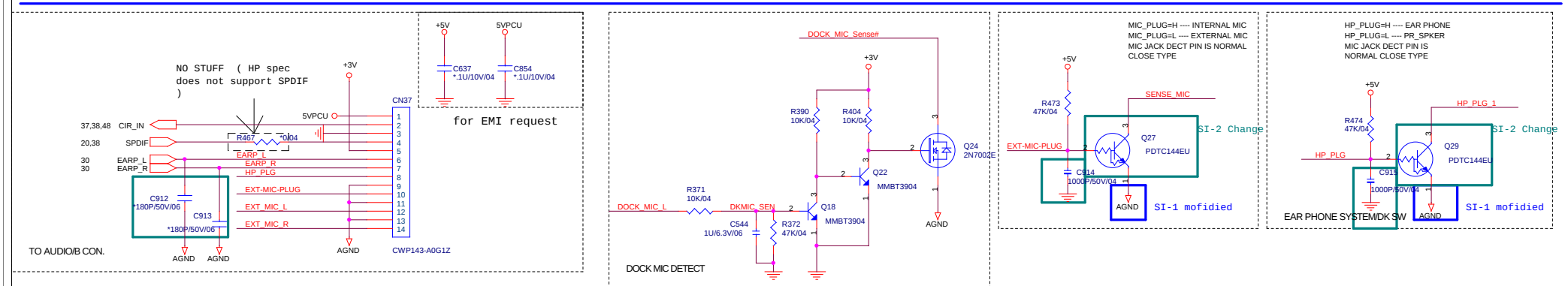
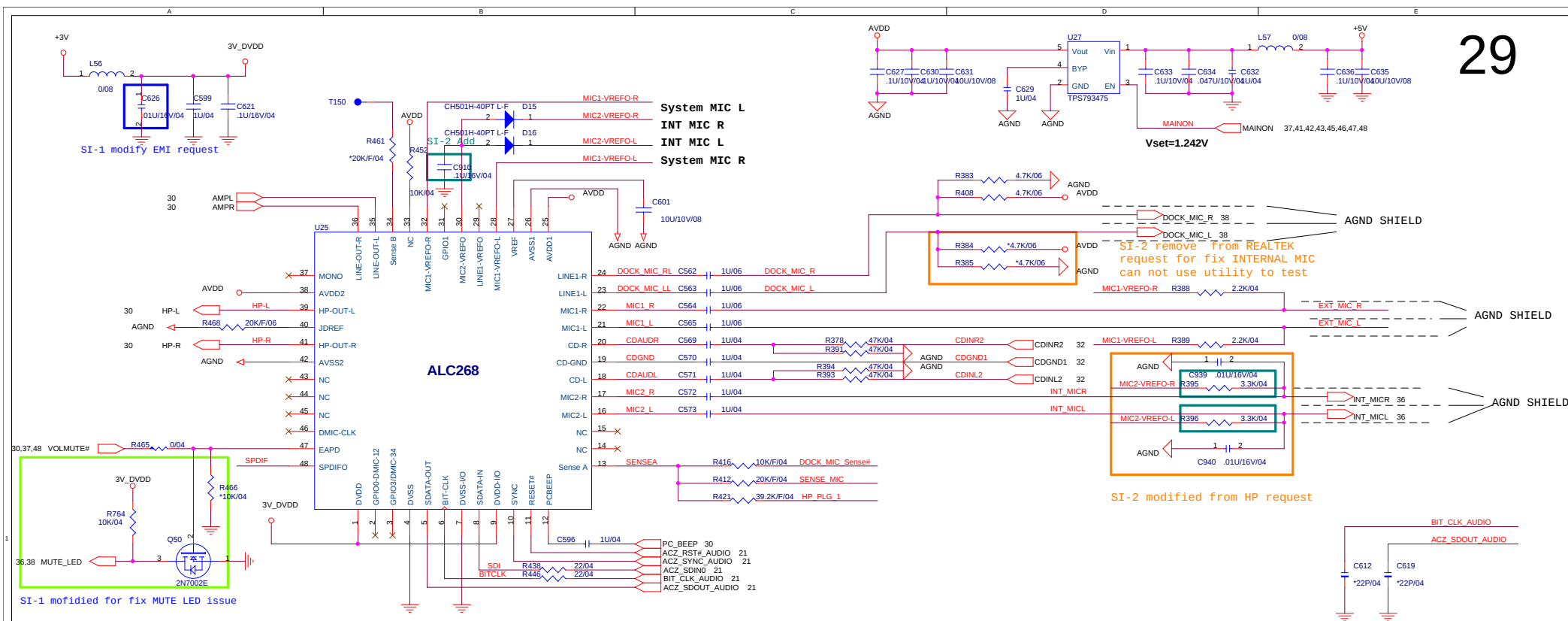
 NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.			
	Size Custom	Document Number CARD READER/HOLE		Rev 1
	Date: Monday, March 19, 2007	Sheet 27 of 48		

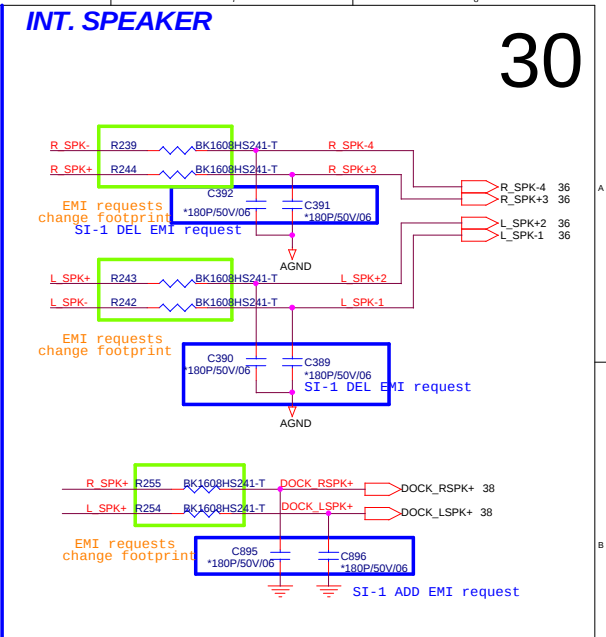
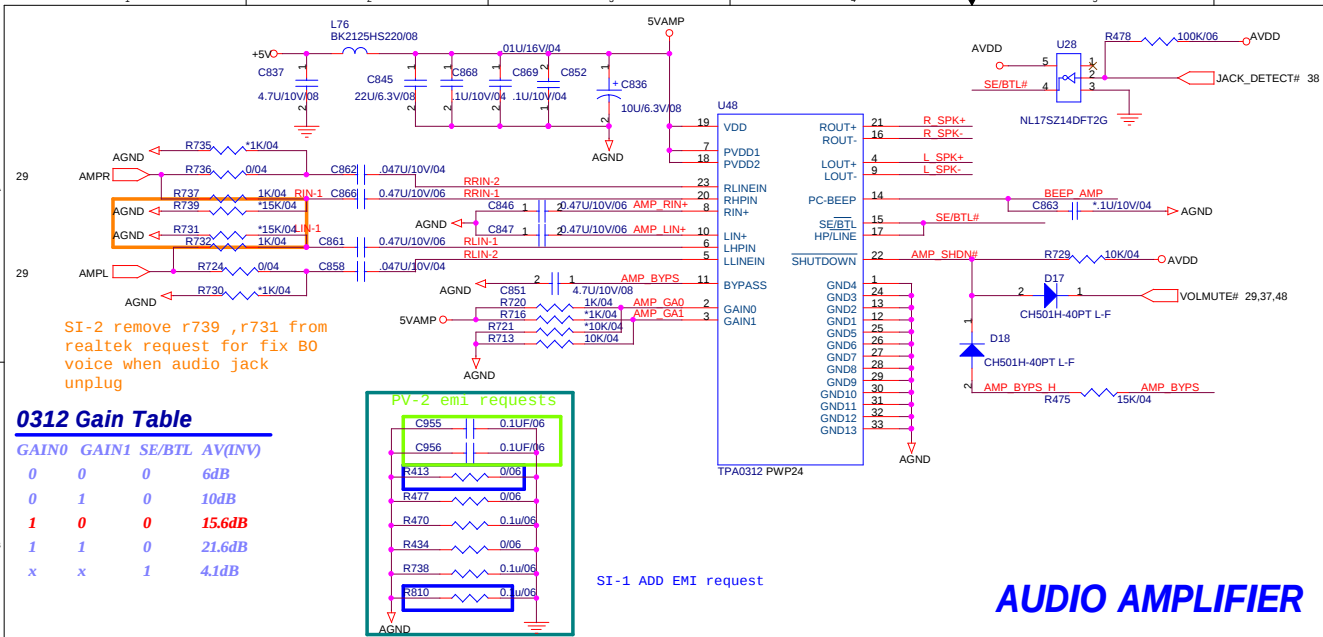


bom create 2'nd source



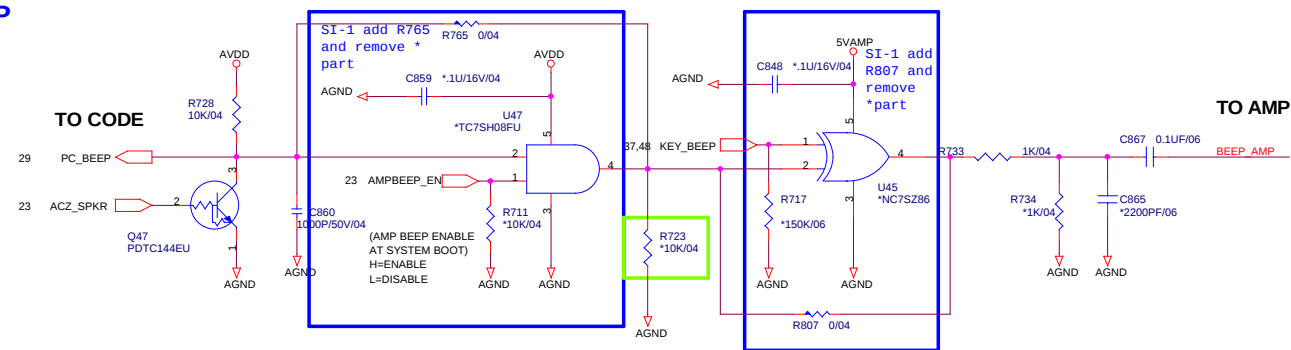




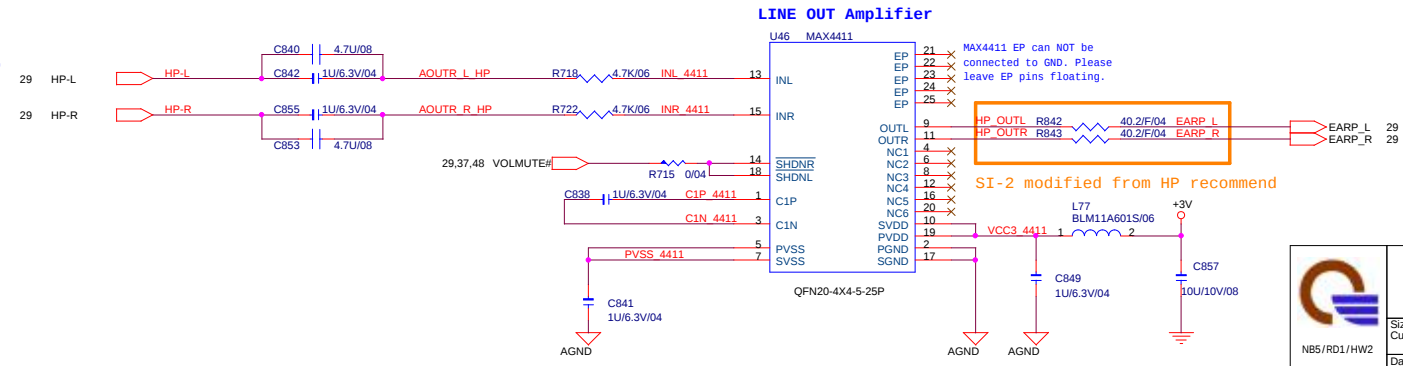


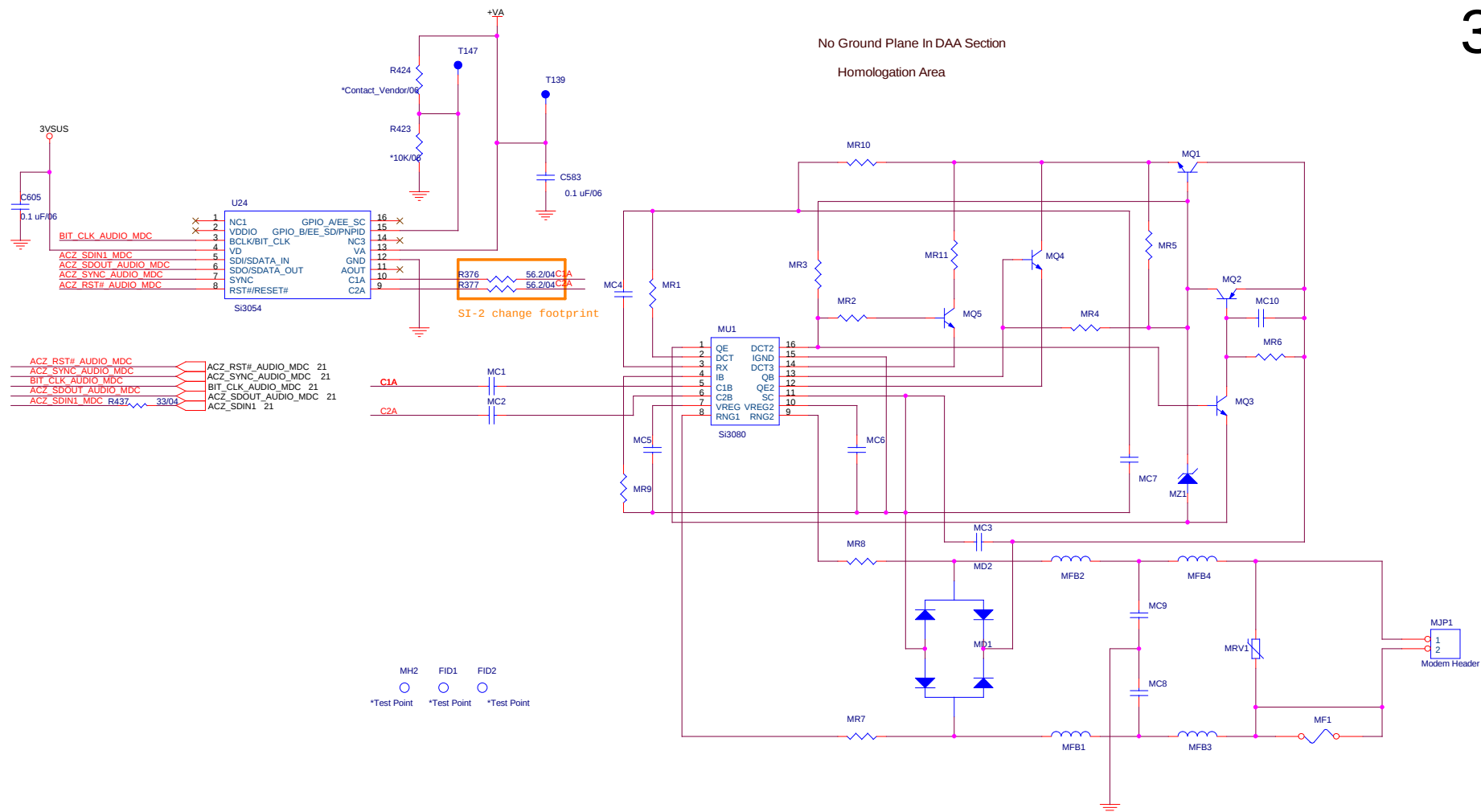
AUDIO AMPLIFIER

PCSPK BEEP



LINE OUT Amplifier

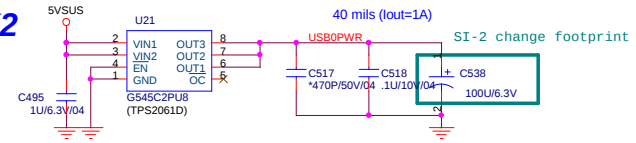




DESIGN SUBJECT TO CHANGE

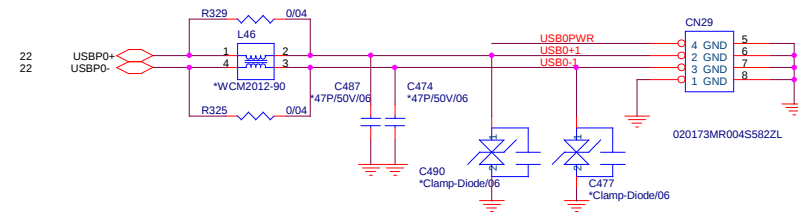
SILICON LABORATORIES CONFIDENTIAL

USBX2

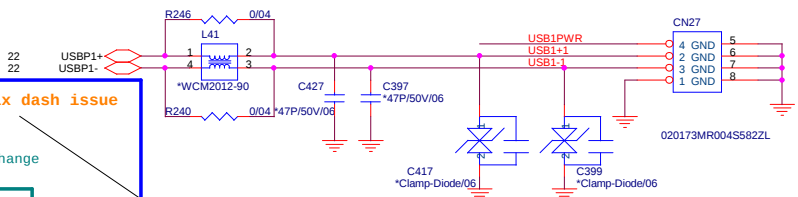


32

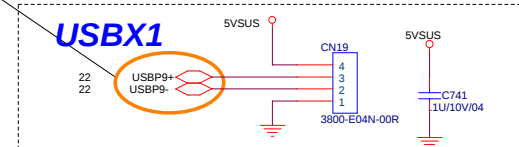
USB 0



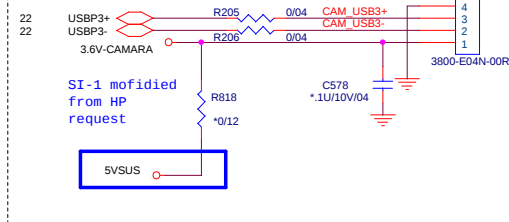
USB 1



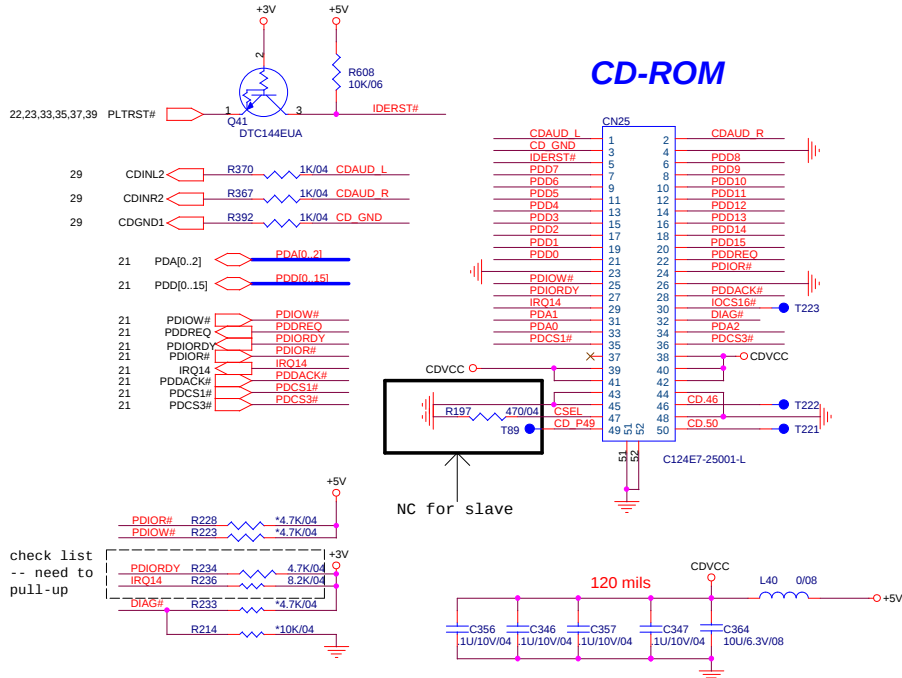
USBX1



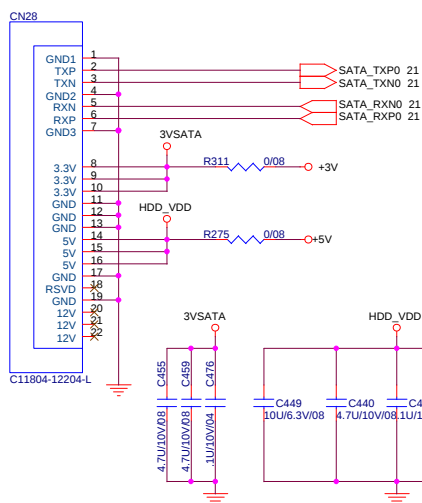
USB CAMERA CONNECT



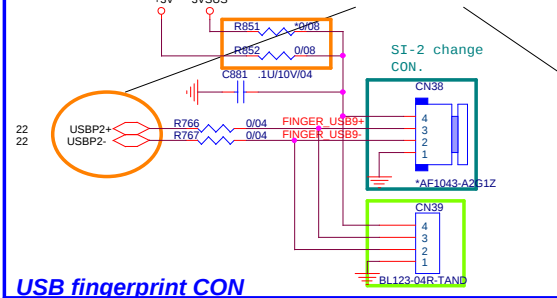
CD-ROM



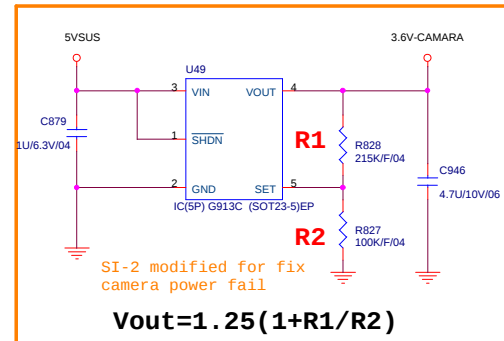
SATA_1 CONNECTOR



SI-1 add



USB fingerprint CON



$$V_{out} = 1.25(1 + R1/R2)$$



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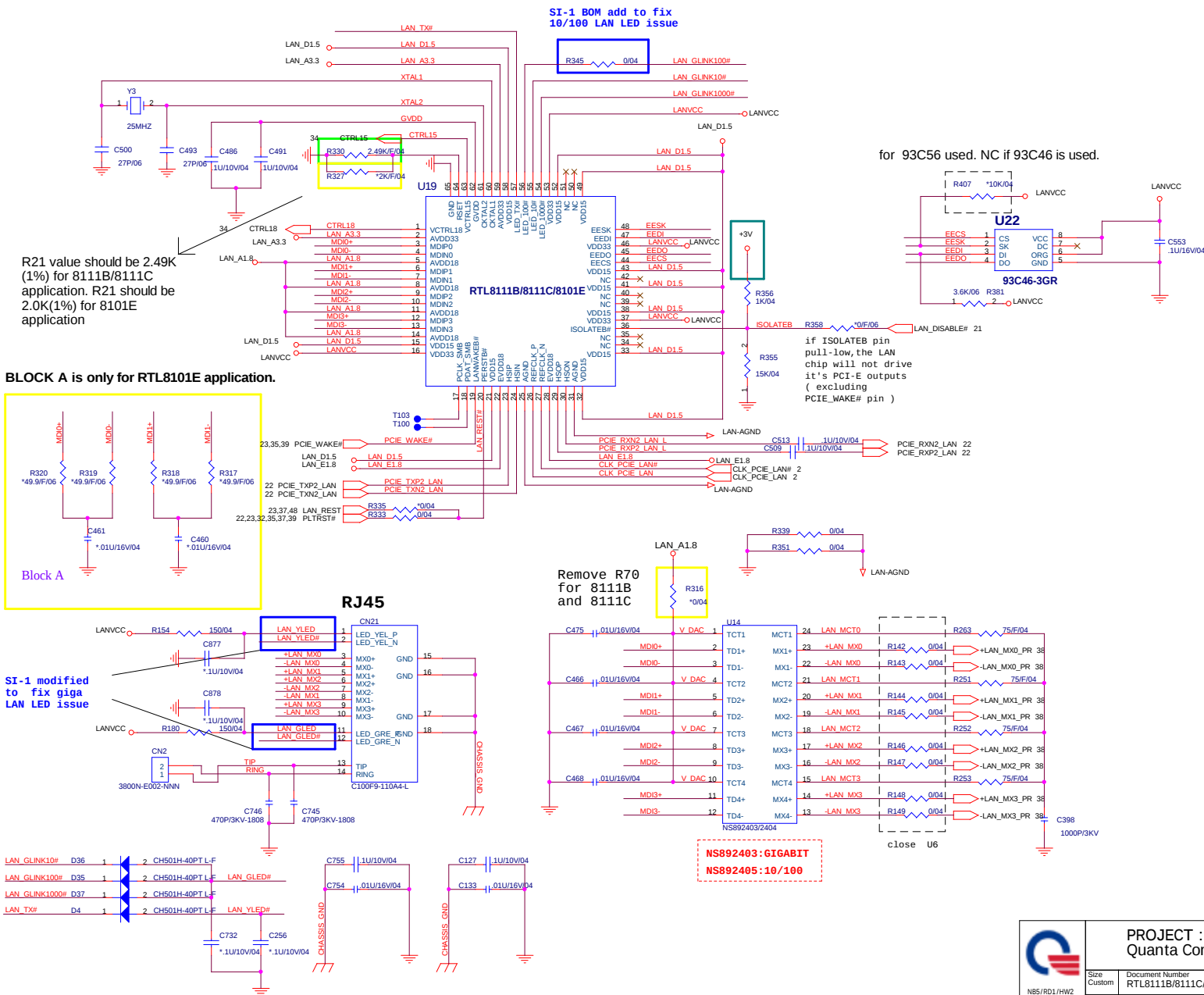
Size Custom	Document Number SATA HDD/CD-ROM/USBX3	Rev 1A
Date: Monday, March 19, 2007	Sheet 32 of 48	

T : Stuffed for RTL8111B(10/100/1000)

giga LAN part number AJ081110006

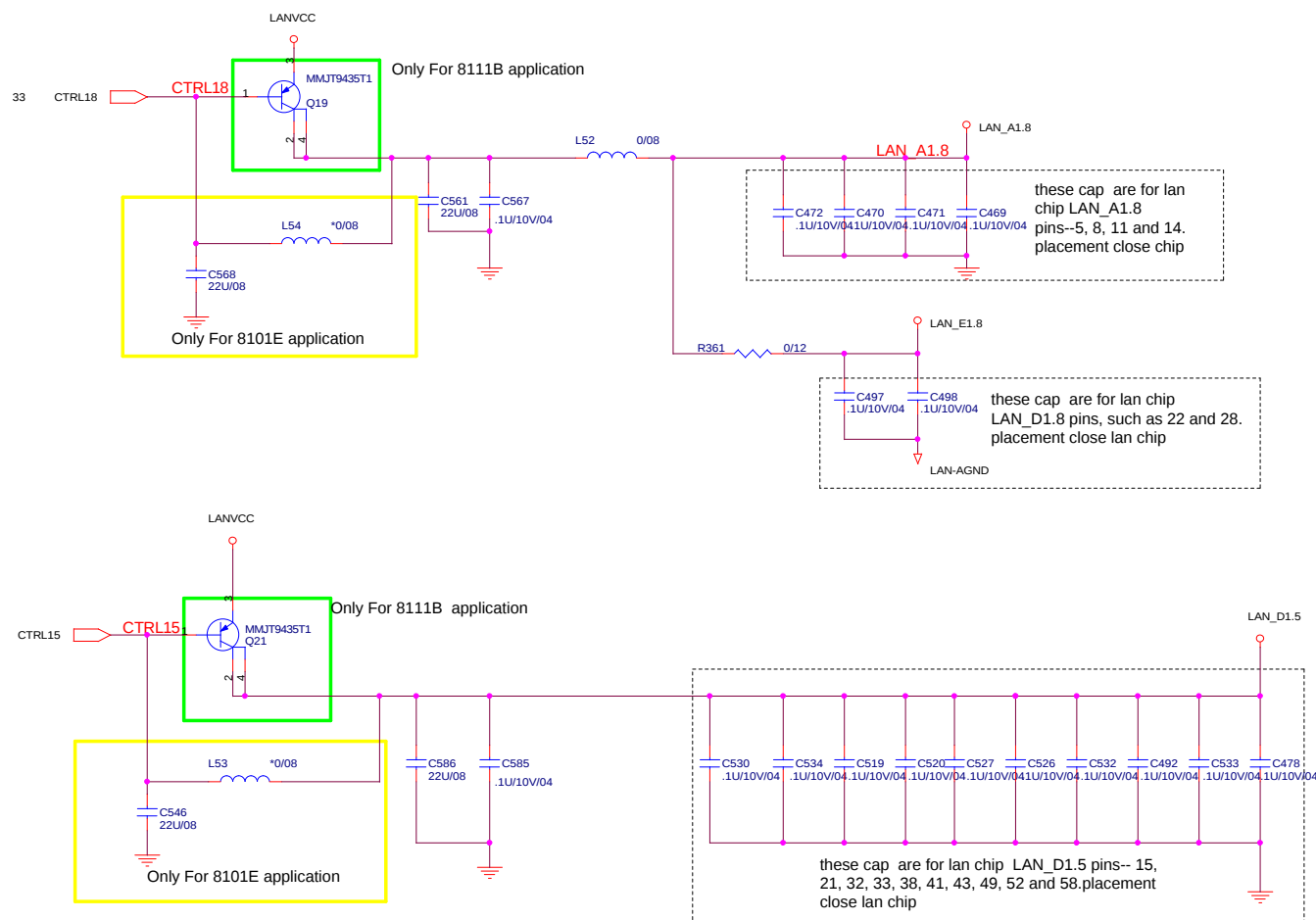
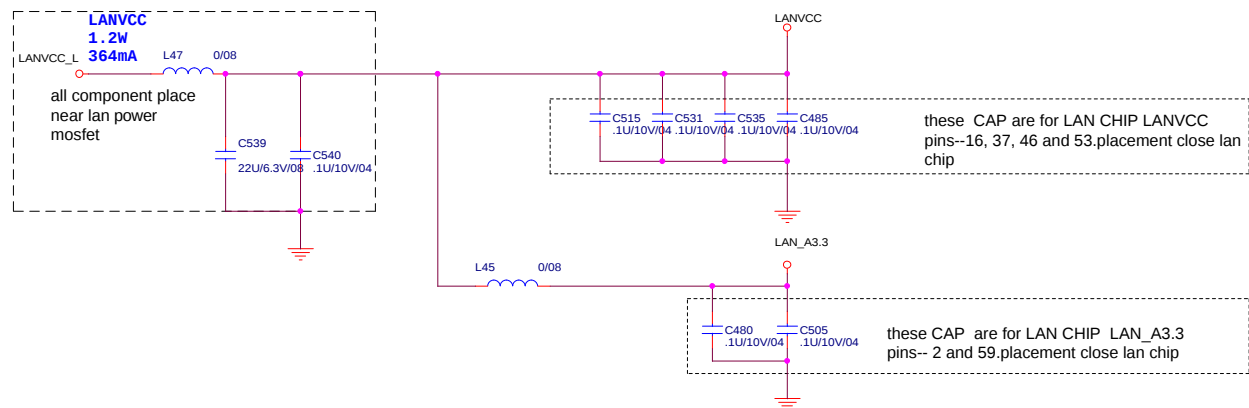
E : Stuffed for 8101E(10/100)

33



T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

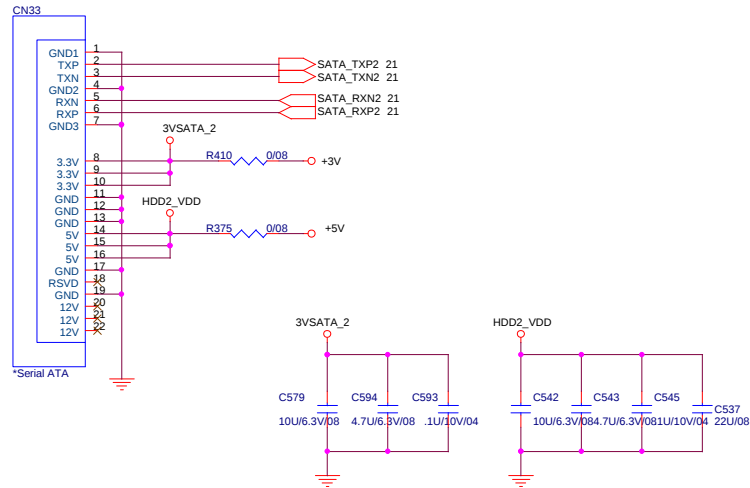
	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A



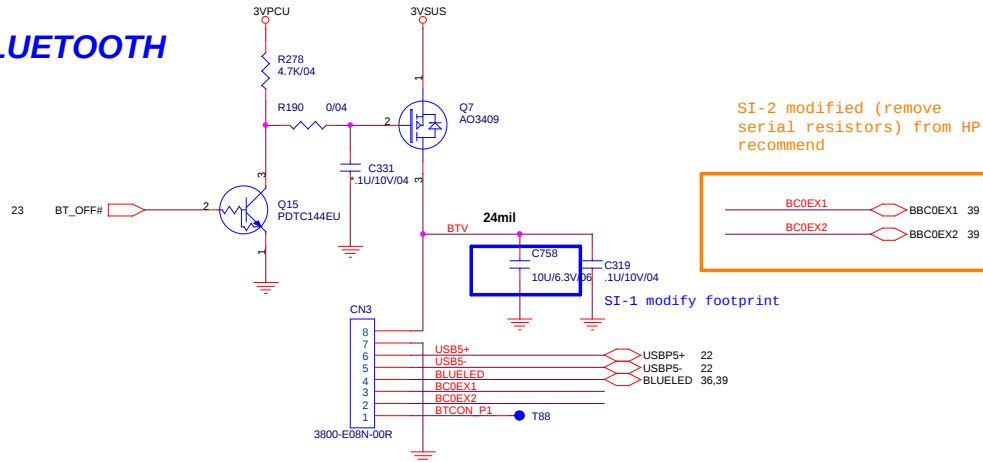
PROJECT : AT5
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Size A3	Document Number LAN POWER	Rev 1A
Date: Monday, March 19, 2007	Sheet 34 of 48	

SATA_2 CONNECTOR For 17"W Second HDD

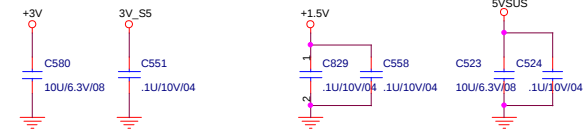
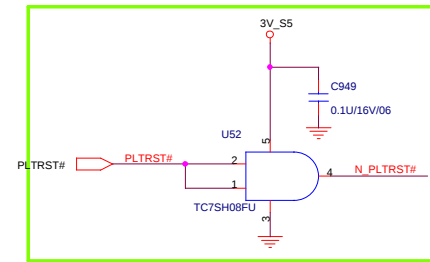
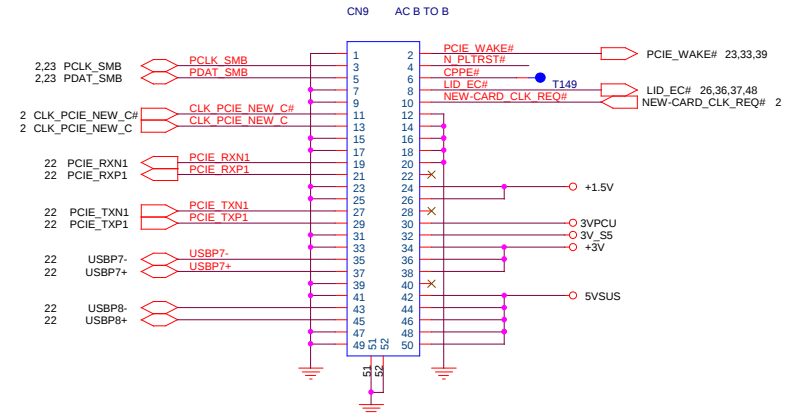


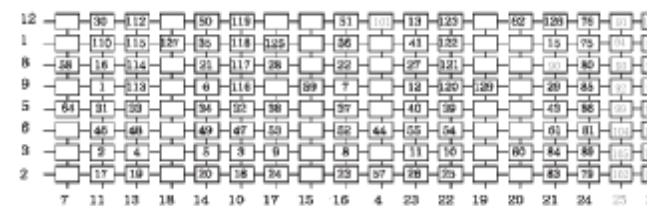
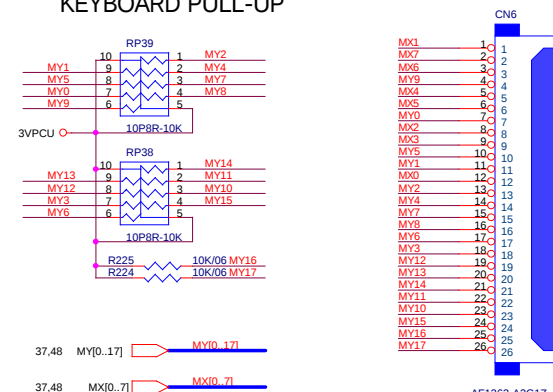
BLUETOOTH

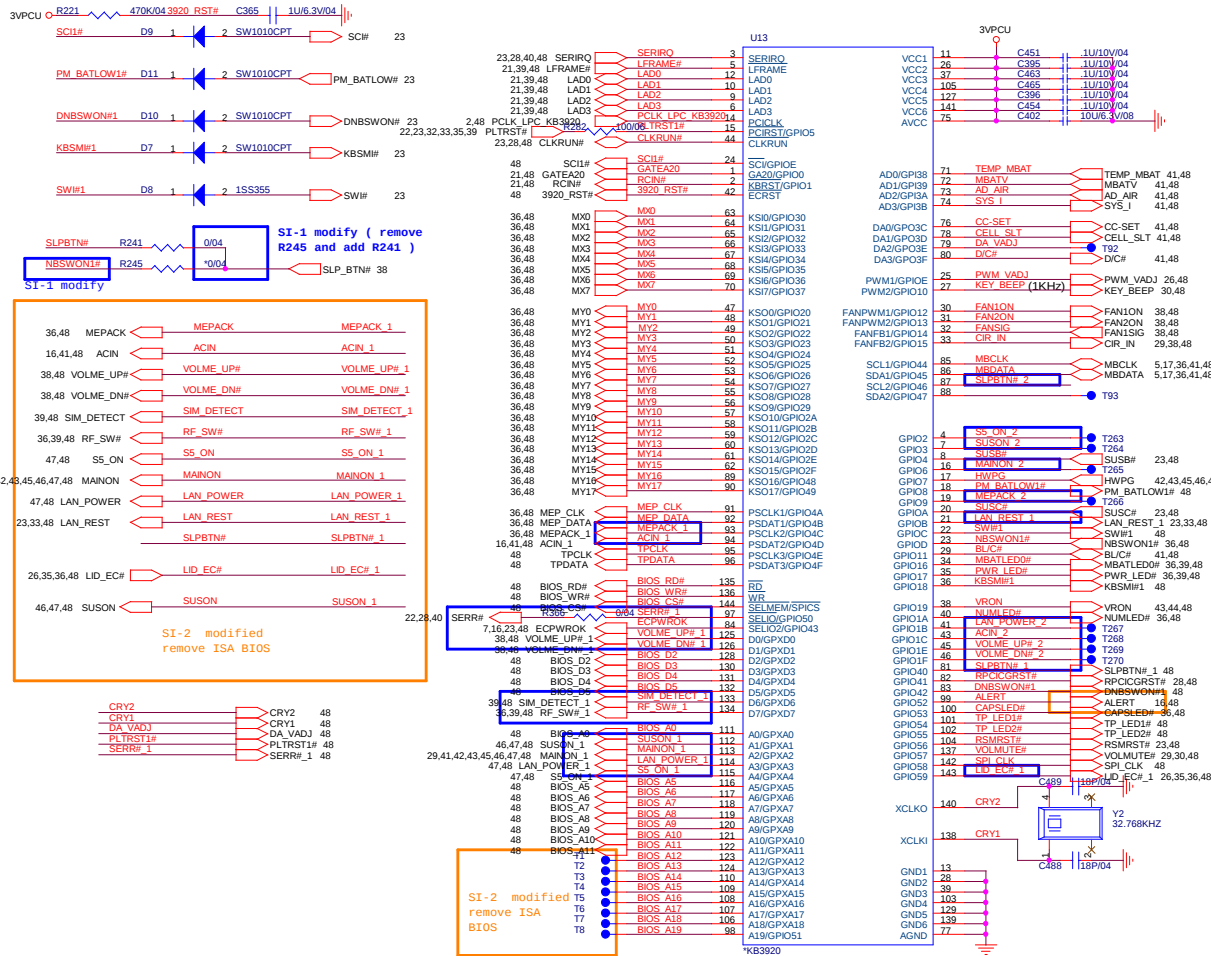


NEWCARD

35







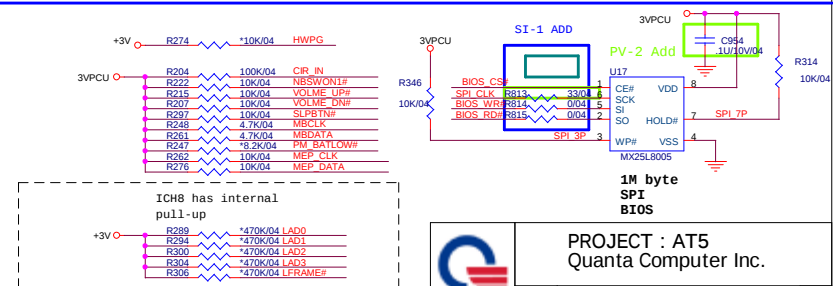
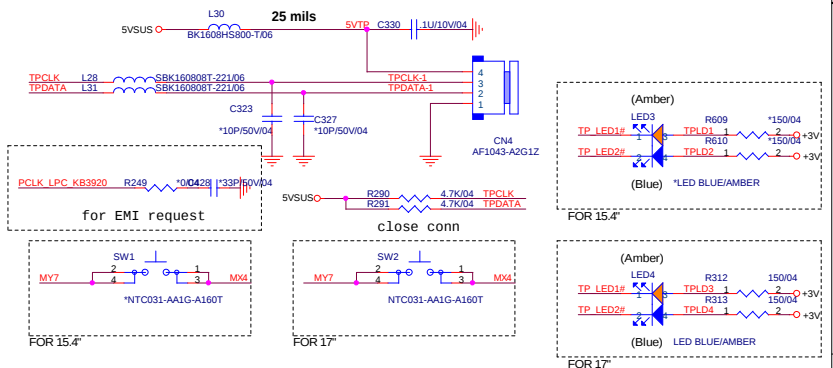
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

MY3 R212 *0/04

All hardware straps
 default internal
 pull-up, so don't
 need pull-UP outside.
 A TEST need try
 --andrew ???

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI-2 modified
remove ISA
BIOS

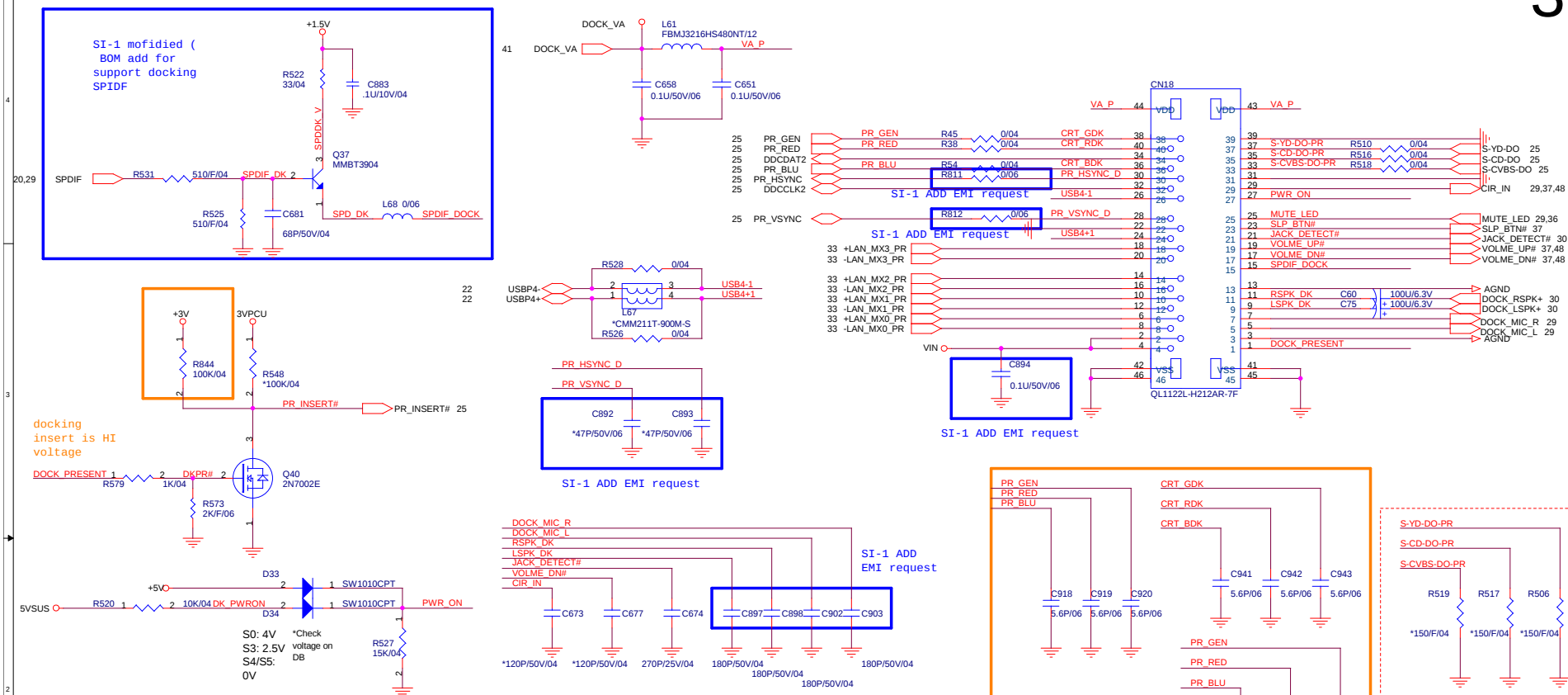


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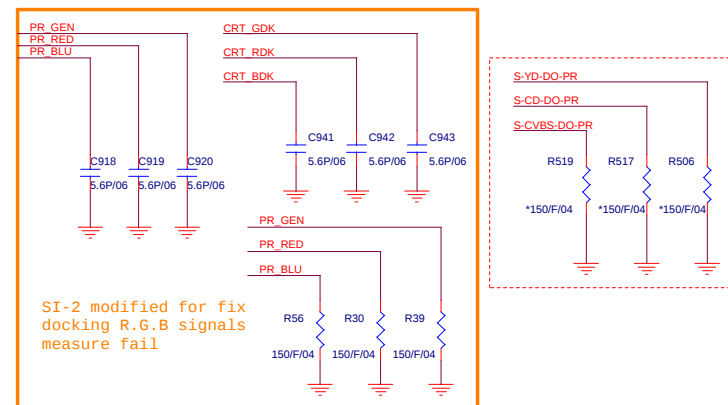
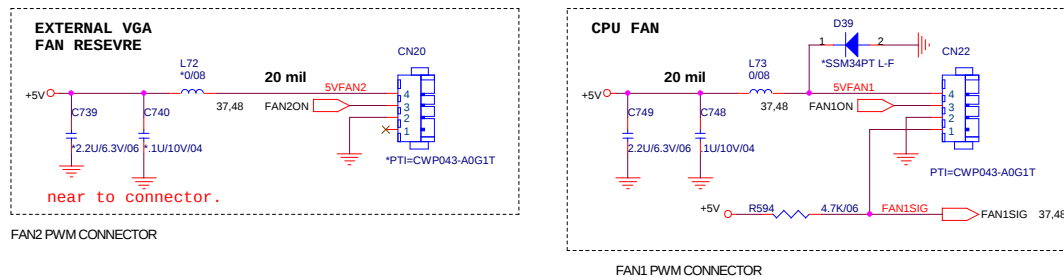


CABLE DOCK

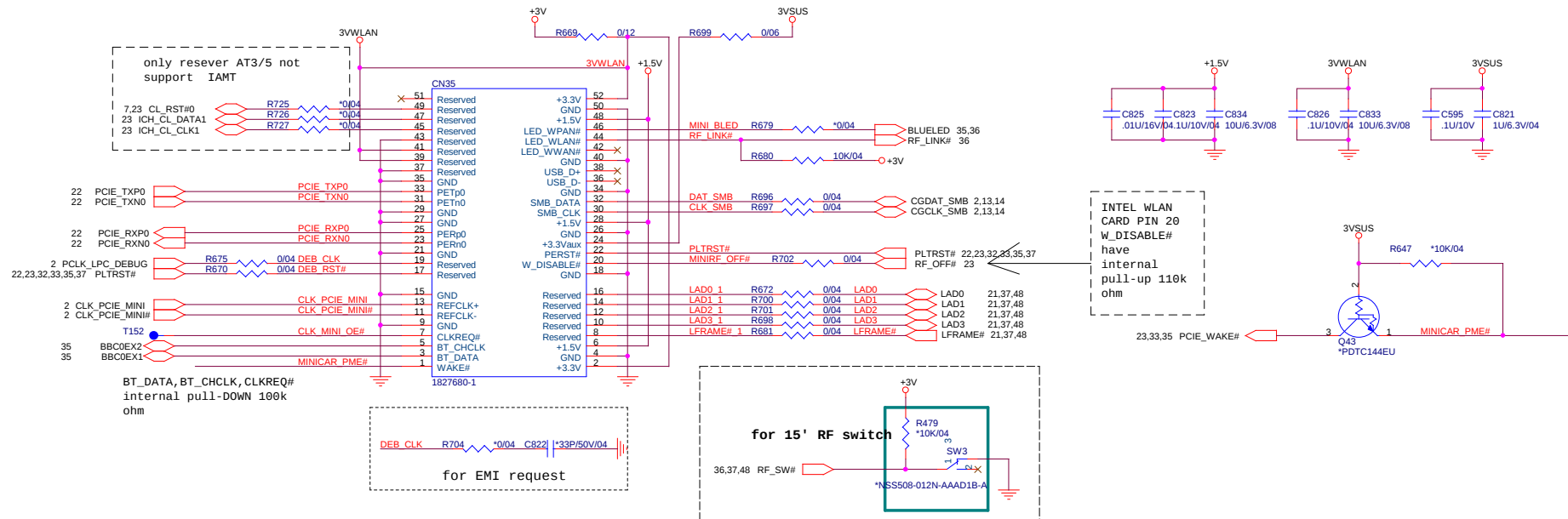
38



FAN



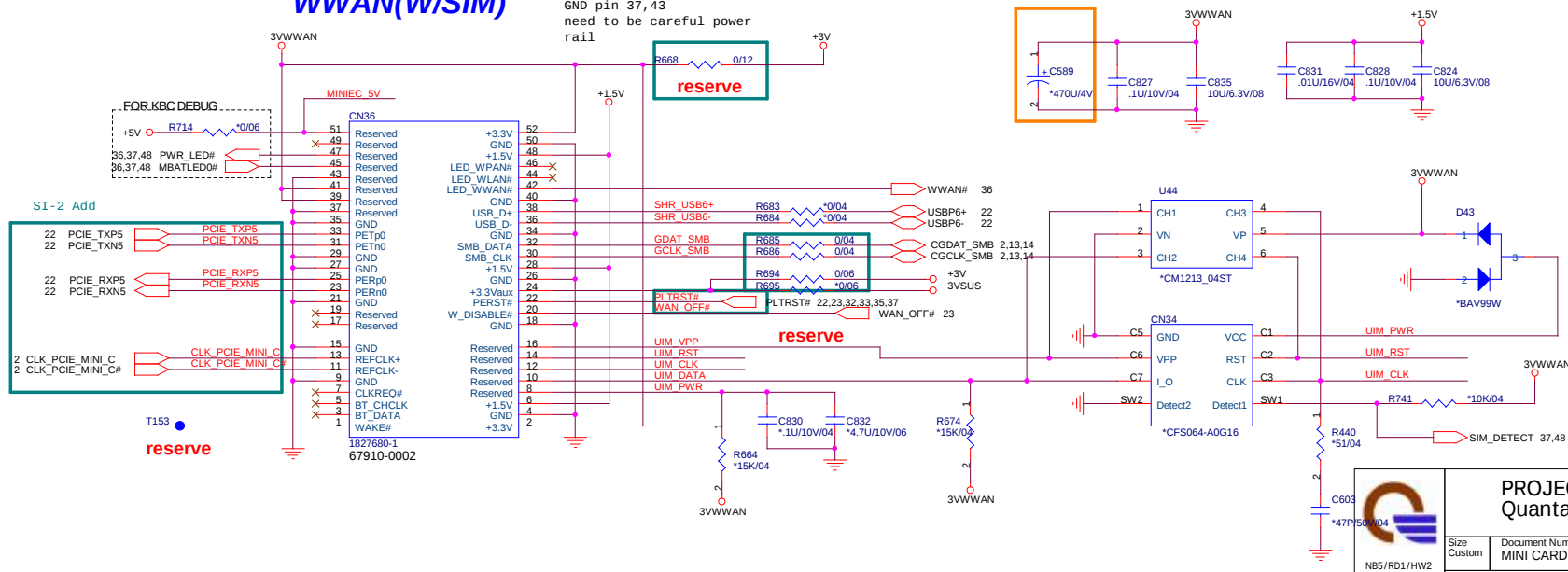
Mini PCI-E Card 1 WLAN



**Mini PCI-E Card 2
WWAN(W/SIM)**

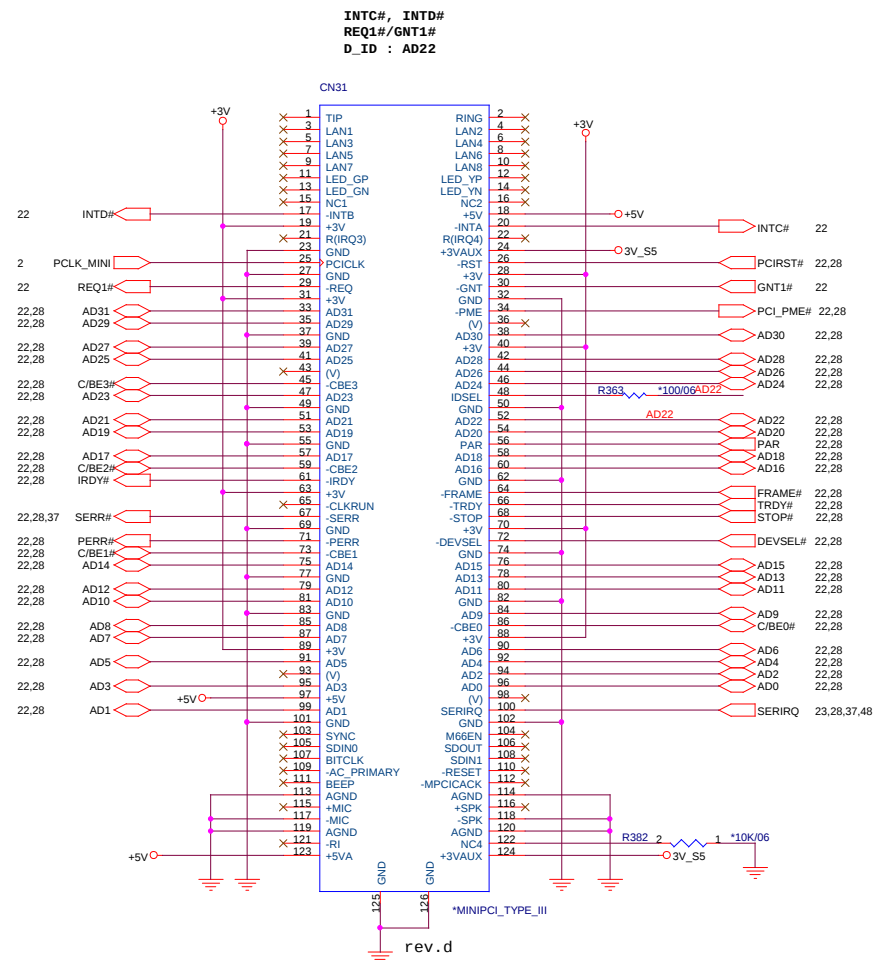
WWAN -- have 2.8A 7W power
consumption
power pin 24,39,41
GND pin 37,43
need to be careful power
rail

SI-2 modified
(BOM remove C589
)

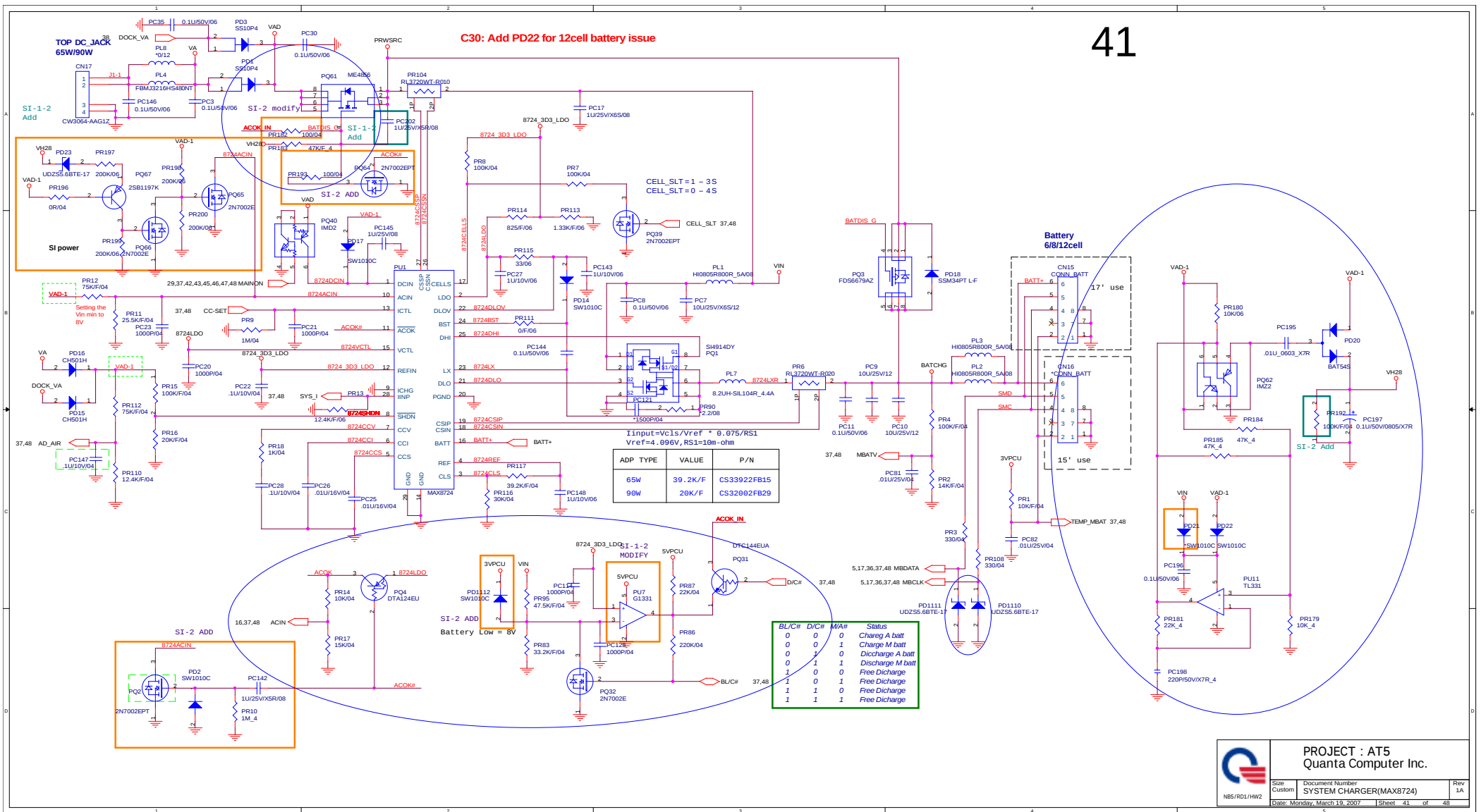


MINI PCI TYPE III SLOT

40



C30: Add PD22 for 12cell battery issue



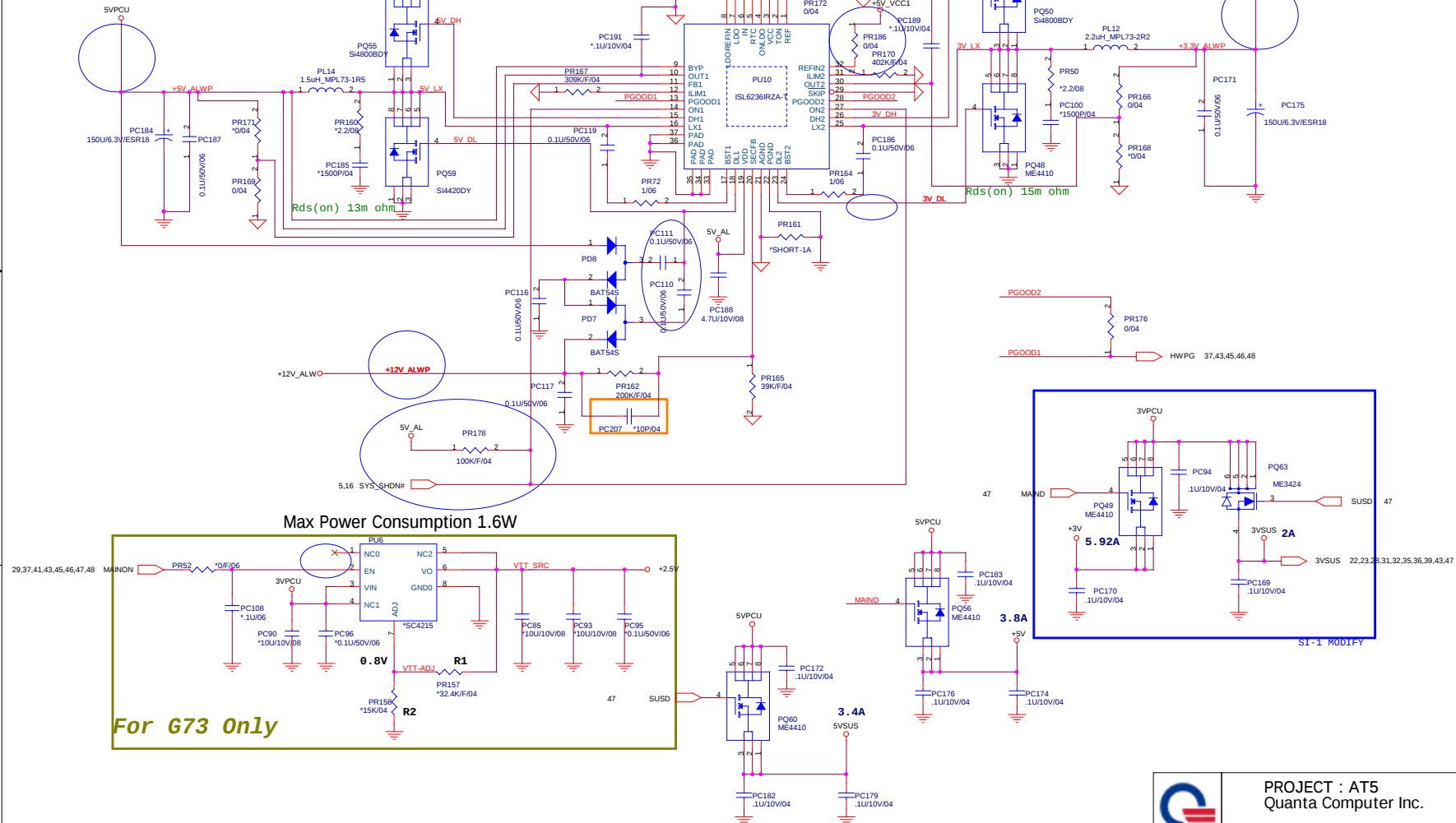
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

**Place these CAPs
close to FETs**

Place these CAPs
close to FETs

5 Volt +/- 5%
Continue current:8A
Peak current:11A
OCP minimum 13A

100/25V
3.3 Volt +/- 5%
Continue current:5A
Peak current:7.5A
OCP minimum 10A

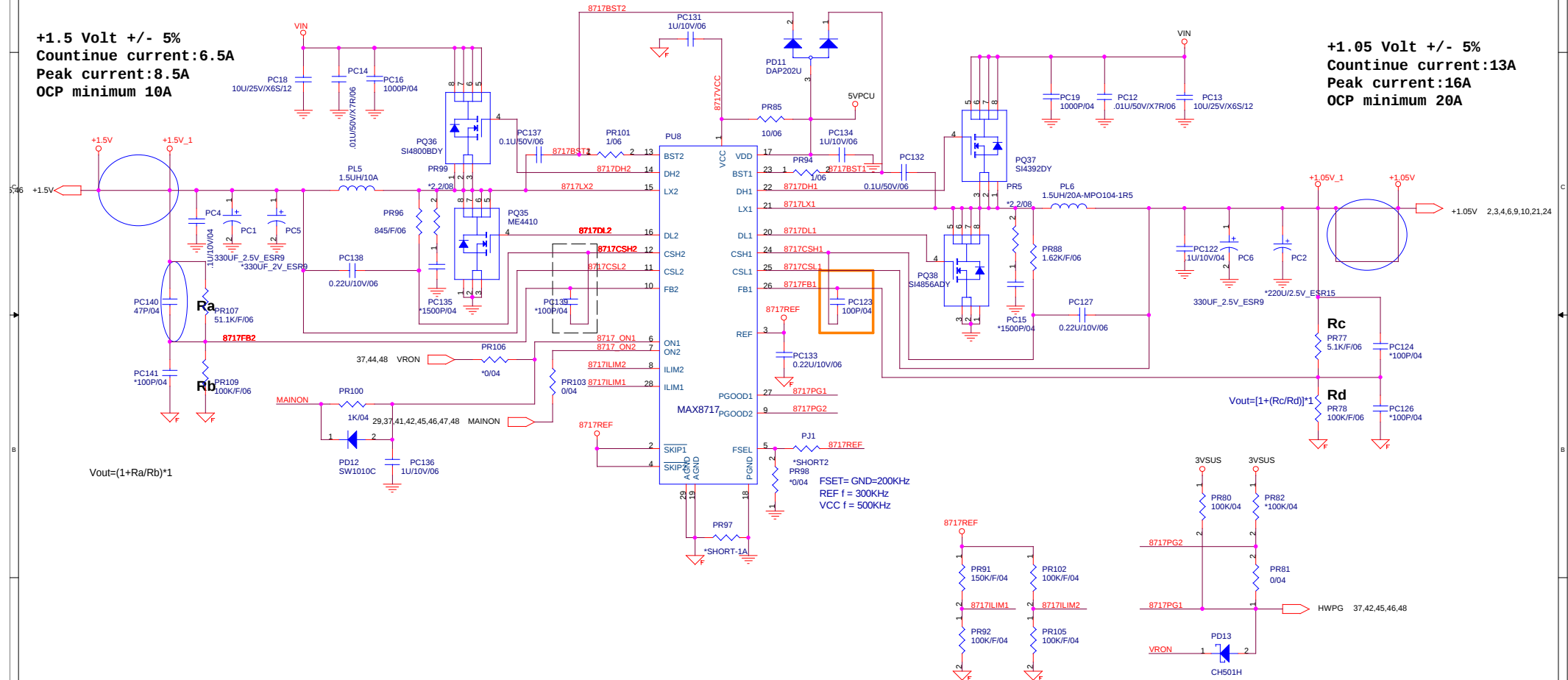


Max Power Consumption 1.6W

For G73 Only

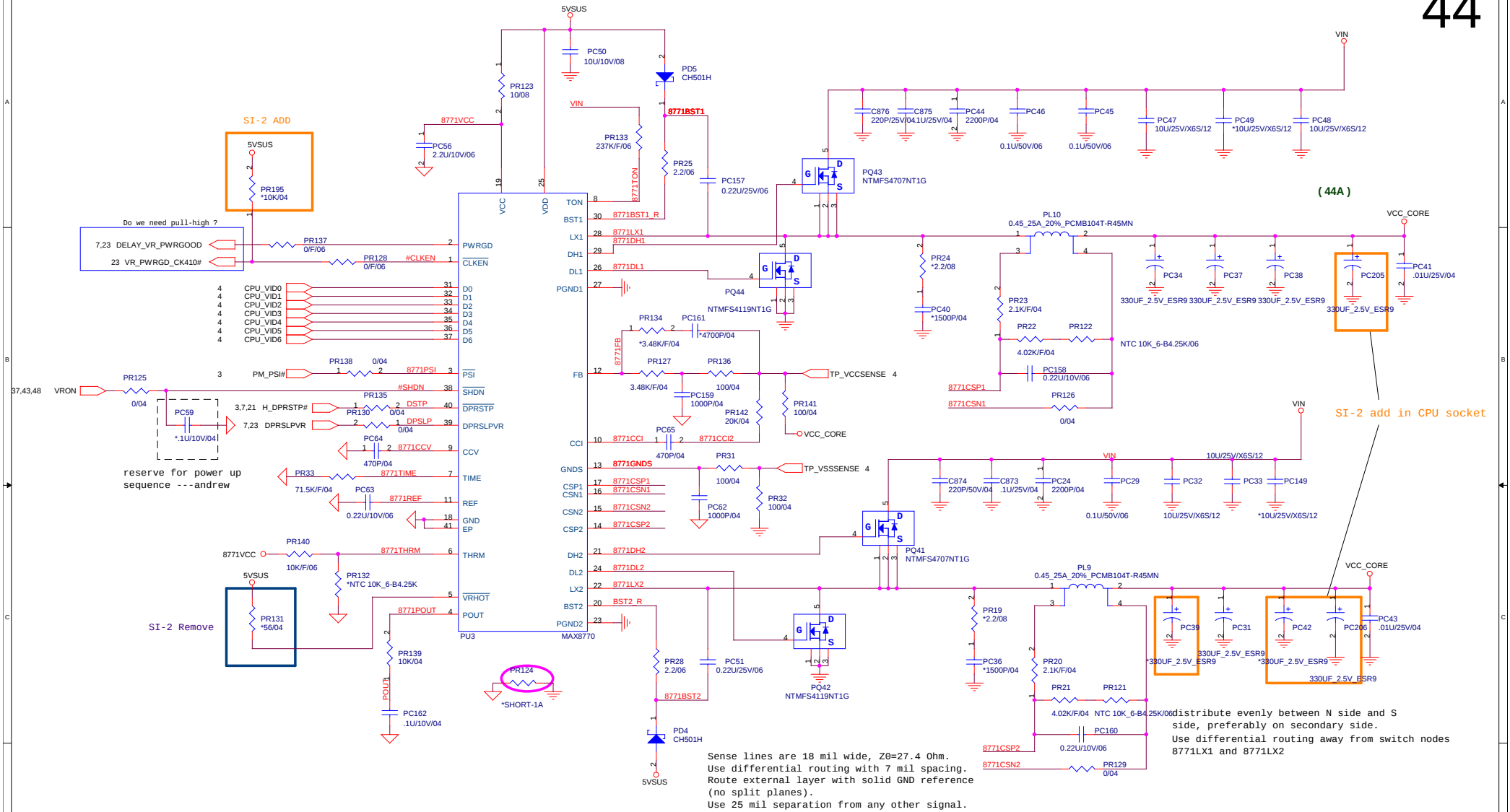
PROJECT : AT5
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+1.05 Volt +/- 5%
Continue current:13A
Peak current:16A
OCP minimum 20A



PROJECT : AT5
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Size Custom	Document Number +1.5V & VCCP+1.05V(MAX8743)	Rev 1A
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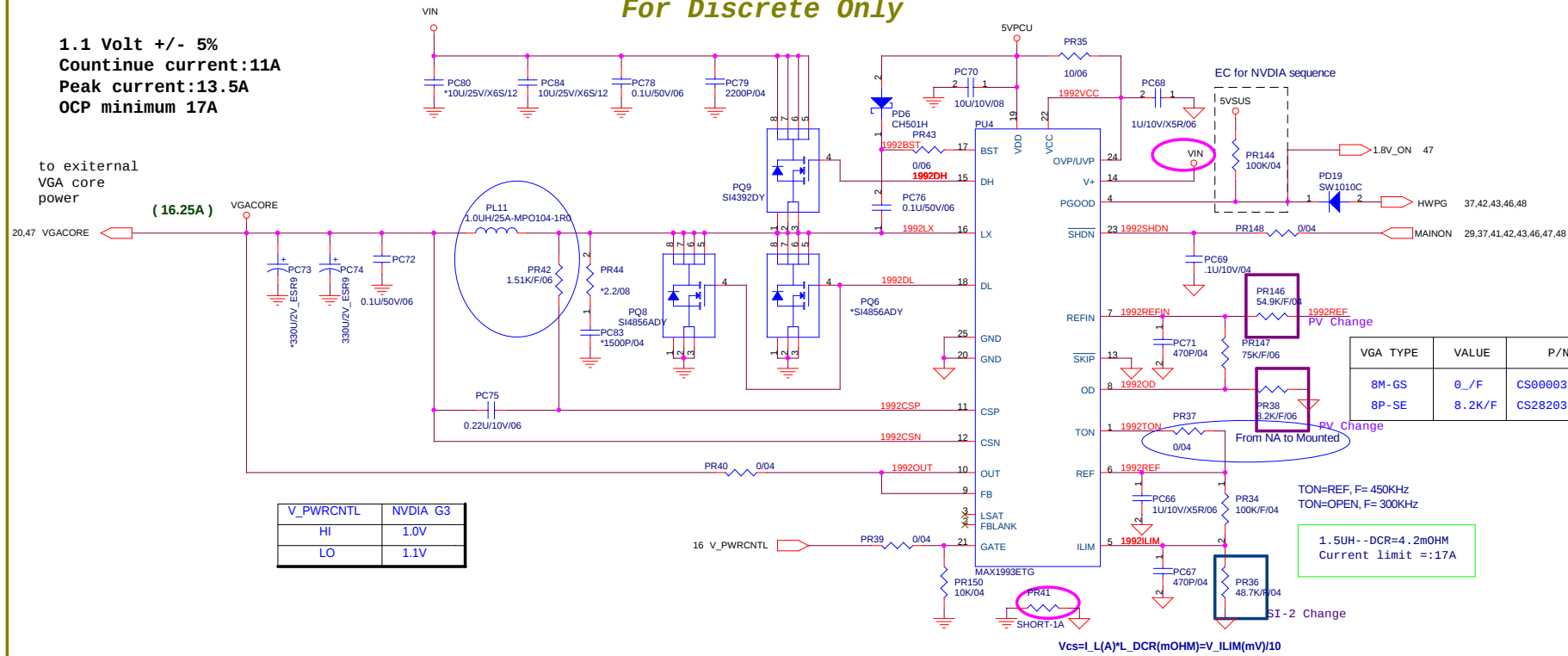


PROJECT : AT5 Quanta Computer Inc.		
Size Custom	Document Number CPU_CORE(MAX8771)	Rev 1A
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For Discrete Only

1.1 Volt +/- 5%
Continue current:11A
Peak current:13.5A
OCP minimum 17A

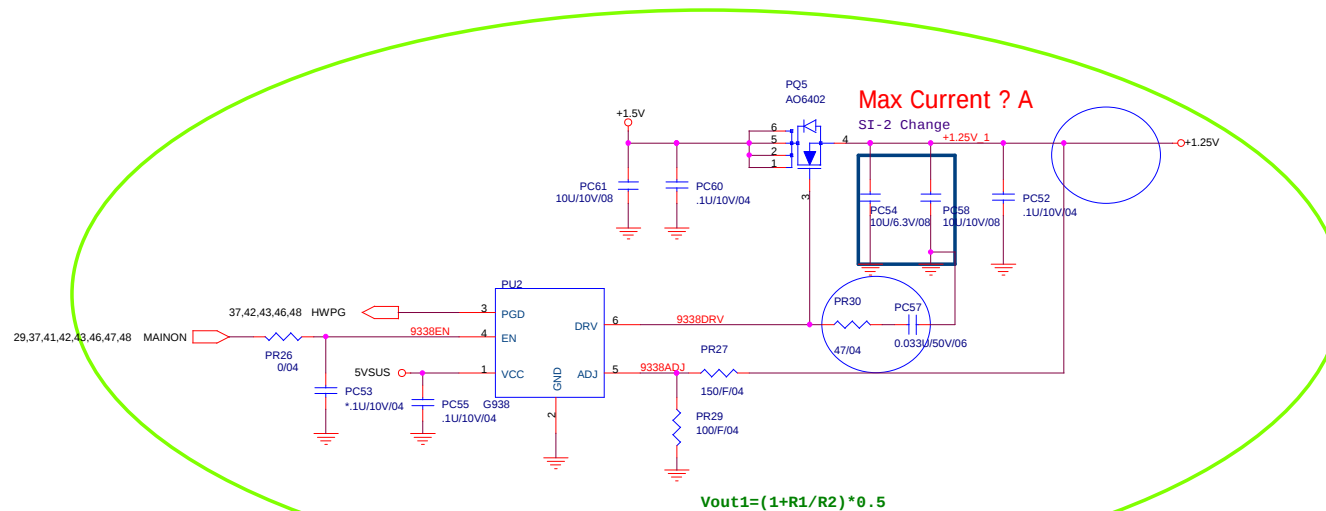
```
to external
VGA core
power
```



VGA TYPE	VALUE	P/N
8M-GS	0_/F	CS00003J951
8P-SE	8.2K/F	CS28203F919

1.5UH - -DCR=4.2mOHM
Current limit =:17A

$$V_{cs} = I_L(A) * L_{DCR}(m\Omega) = V_{ILIM}(mV) / 10$$

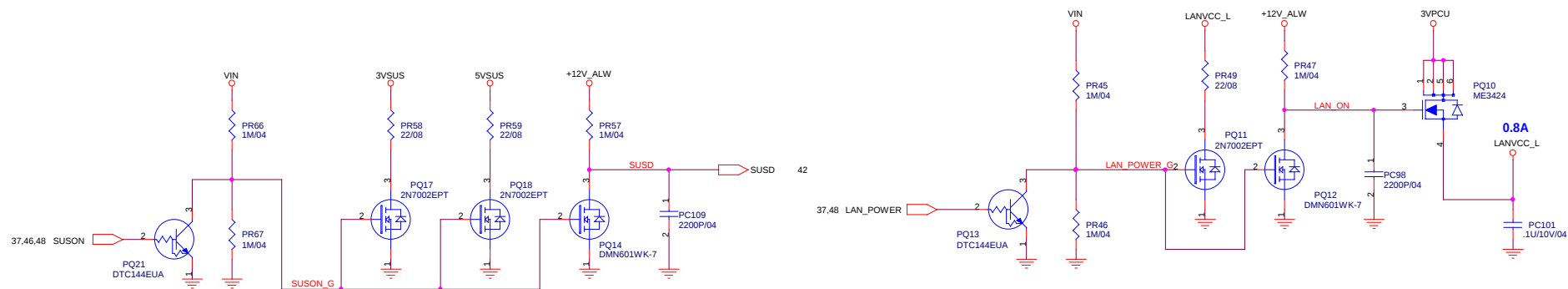
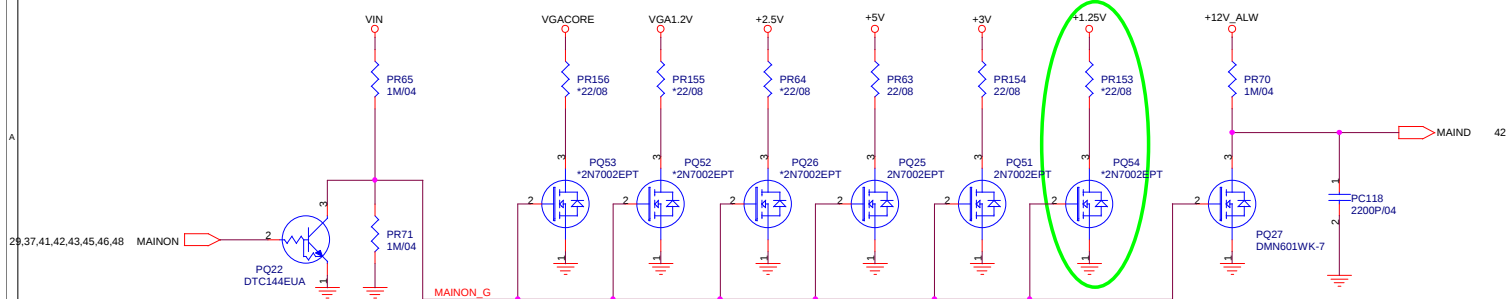


$$V_{out1} = (1 + R1/R2) * 0.5$$

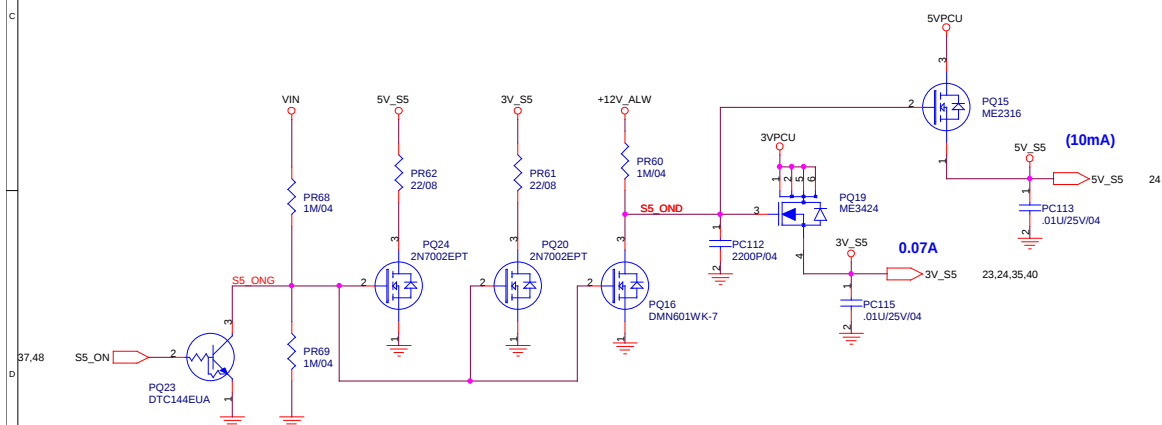
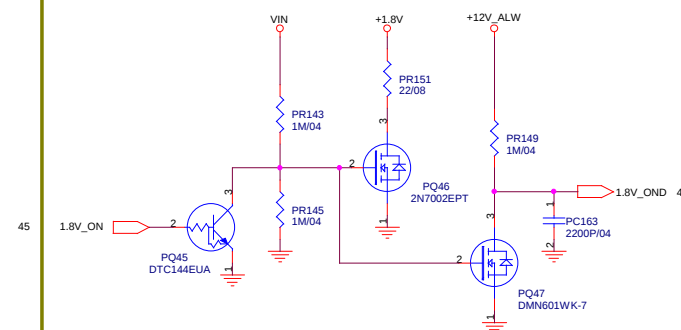


PROJECT : AT5
Quanta Computer Inc.

Size Custom	Document Number VGACORE (MAX1993)	Rev 1A
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For Discrete Only



PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	1A
Date: Monday, March 19, 2007		Sheet 47 of 48

