

# COMPAL CONFIDENTIAL

COMPAL P/N :

PCB NO : *LA-1761*

Revision : *2.0*

DATE :

## LA-1761 Schematics Document

### uFCBGA/uFCPGA Northwood

2003-03-12

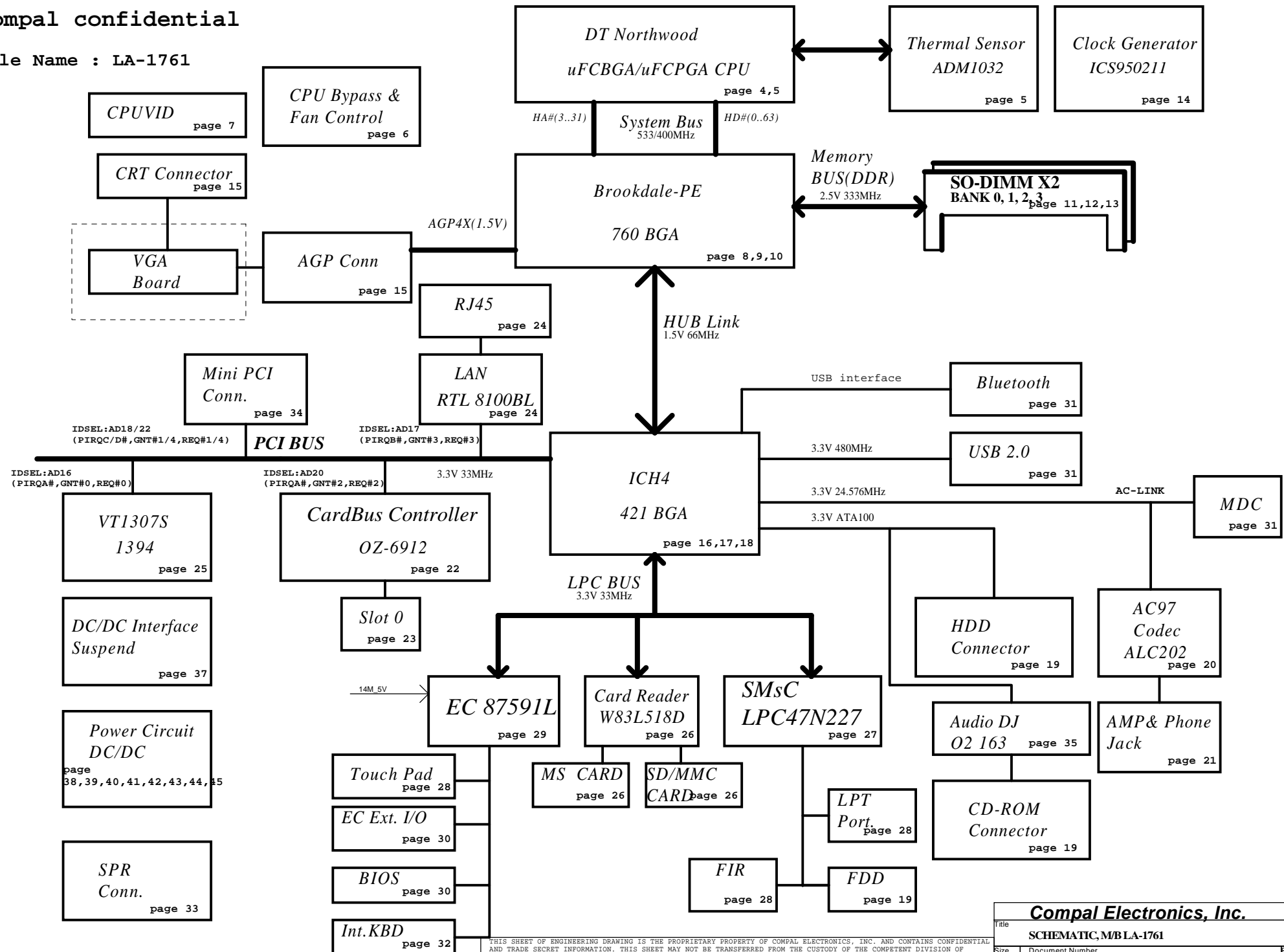
REV: 2.0

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Title		
<b>SCHEMATIC, M/B LA-1761</b>		
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	<b>401248</b>	2A
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Compal confidential

File Name : LA-1761



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**SCHEMATICS VERSION LIST**

VERSION	ISSUE DATE	REMARK

**Power Managment table**

Signal State	+3VALW +5VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.5VS +1.2VP +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	PCB Rev	CHIPS Rev
SST-Build	0.1	
PT-Build		
ST-Build		
QT-Build		

**Ceramic Capacitor Spec Guide:**

**Temperature Characteristics:**

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NP0	C0G		BJ	CH	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

**Tolerance:**

Symbol	A	B	C	D	F	G	H	J
CODE	+/-0.05PF	+/-0.1PF	+/-0.25PF	+/-0.5PF	+/-1PF	+/-2%	+/-3%	+/-5%

K	M	N	P	Q	v	X	Z	
+/-10%	+/-20%	+/-30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

**SMBUS Control Table**

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (U43)	THERMAL SENSOR (U91)	SODIMM	CLK CHIP	MINI PCI
SMB_EC_CK1 SMB_EC_DA1	NS 87591	✓	✓	✓ (1010)	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	NS 87591	✗	✗	✗	✓	✓	✗	✗	✗
SMB_CLK SMB_DATA	ICH4	✗	✗	✗	✗	✗	✓	✓	✓

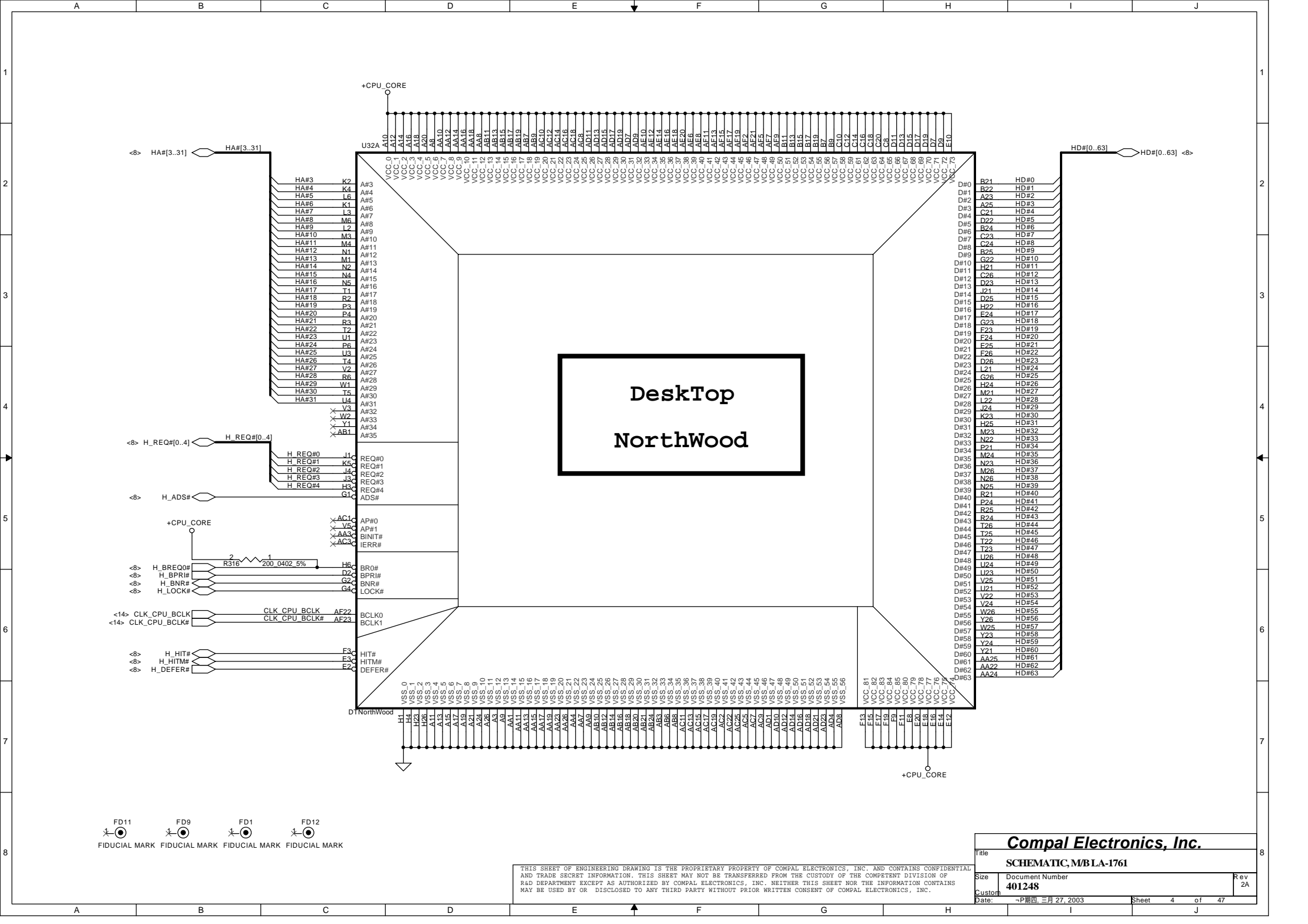
**NOTE1:**

**@XX : Depop component**

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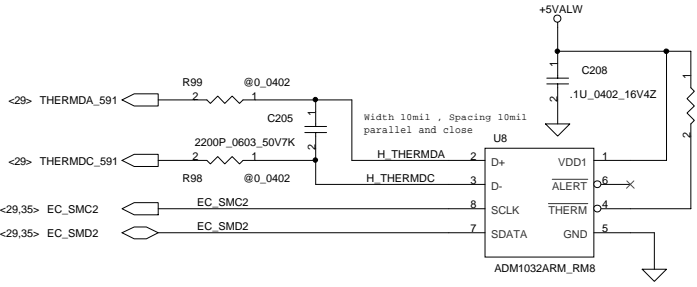
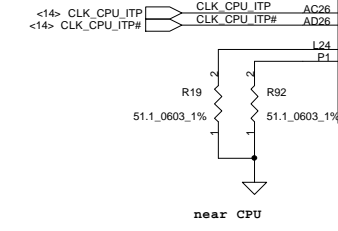
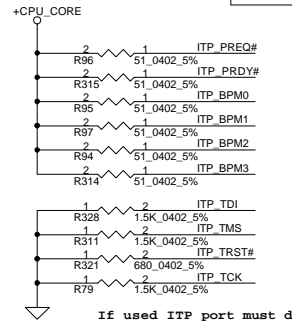
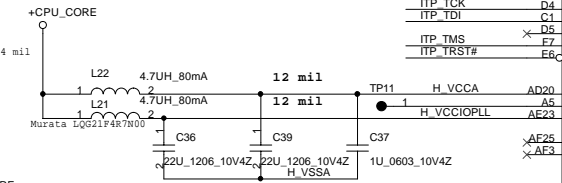
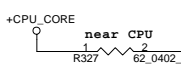
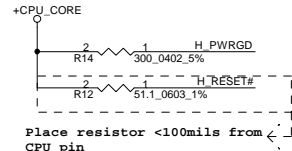
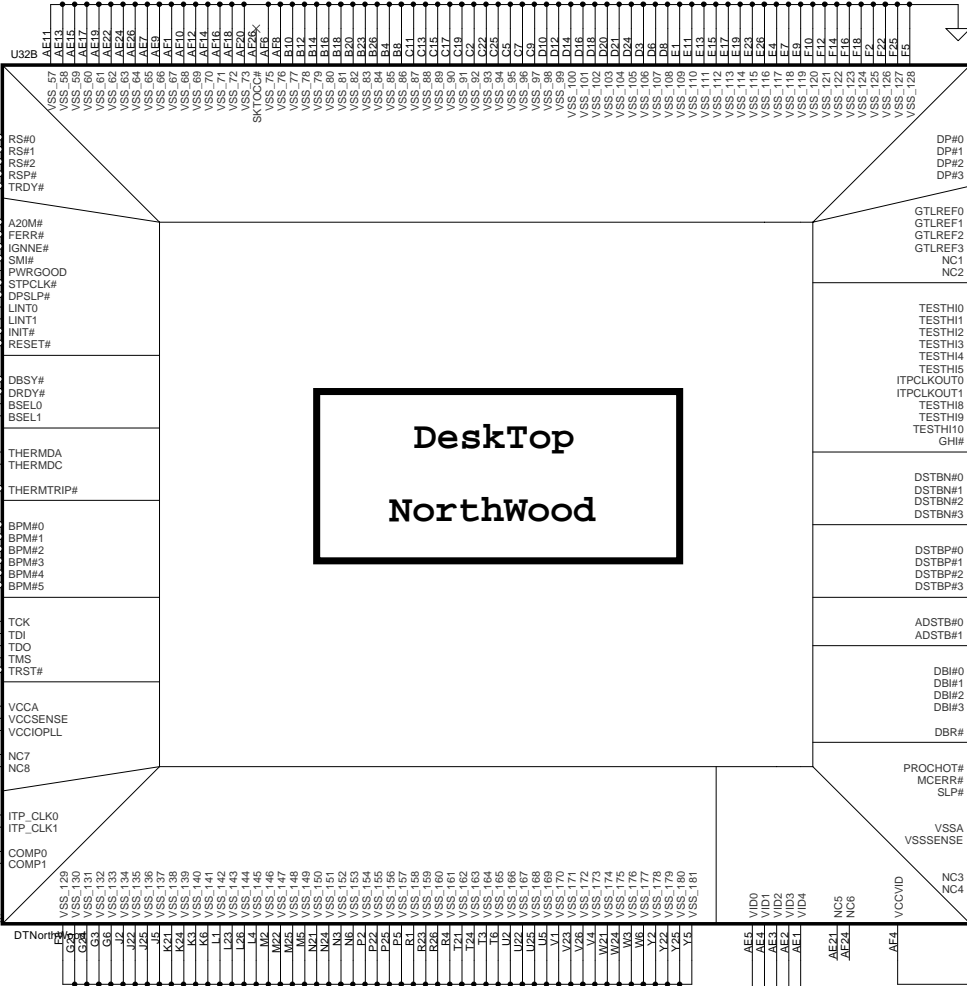


**DeskTop  
NorthWood**

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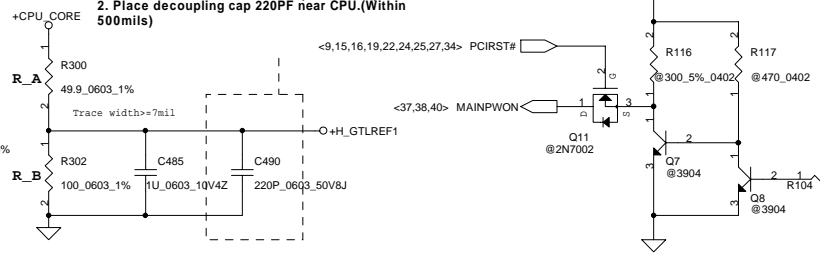
# DeskTop NorthWood



**GTL Reference Voltage**

Layout note :

- Place R\_A and R\_B near CPU (Within 1.5")
- Place decoupling cap 220PF near CPU.(Within 500mils)



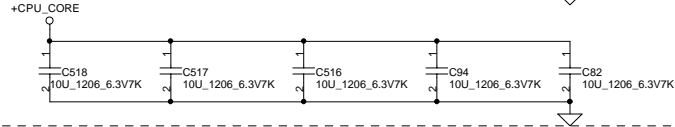
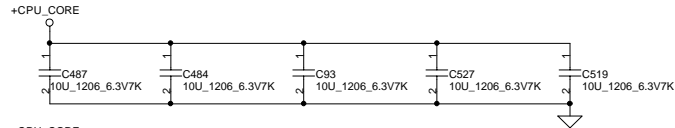
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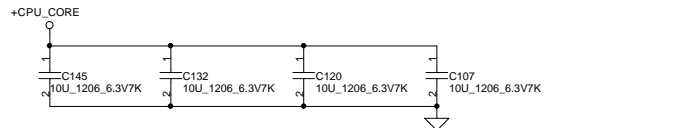
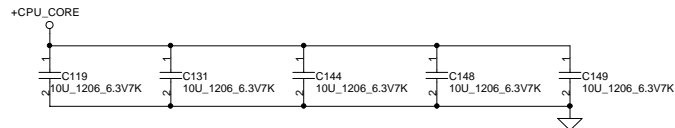
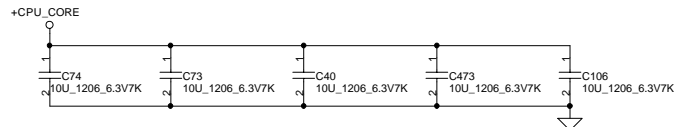
**Layout note :**

Place close to CPU, Use 2-3 vias per PAD.  
Place .22uF caps underneath balls on solder side.  
Place 10uF caps on the peripheral near balls.  
Use 2-3 vias per PAD.

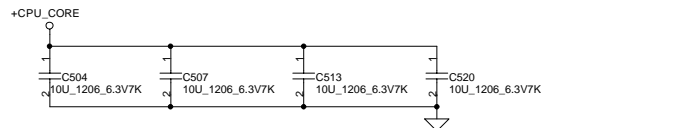
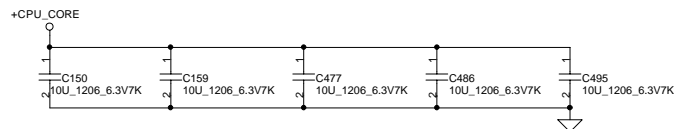
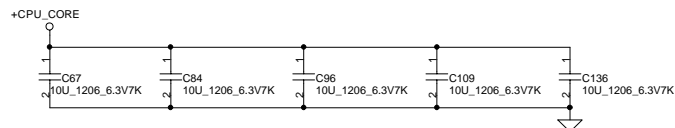
Please place these cap in the socket cavity area



Please place these cap on the socket north side



Please place these cap on the socket south side



**Layout note :**

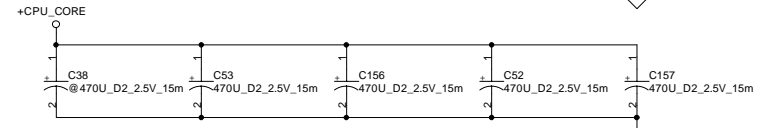
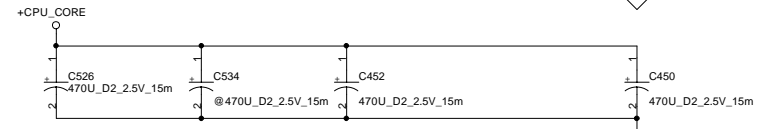
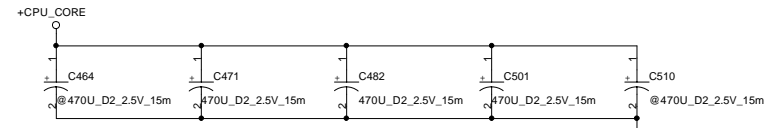
Place close to CPU power and ground pin as possible (<1inch)

**For Desktop's CPU:**

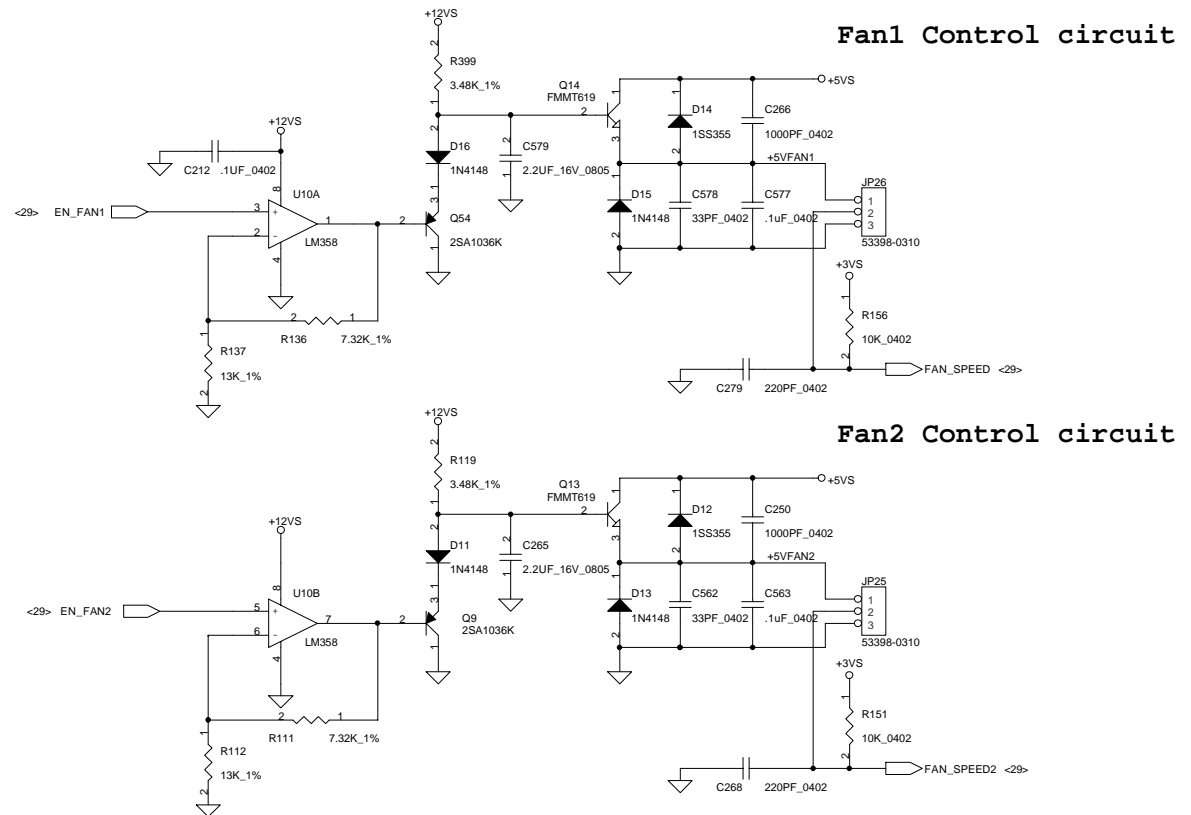
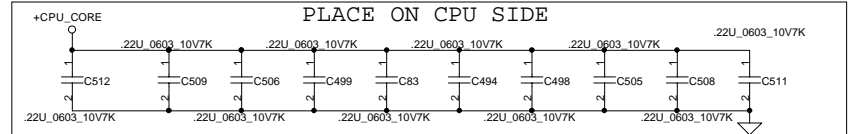
ESR total=0.75m ohm  
C total=6350uF

**For Mobile's CPU:**

ESR total=1.875m ohm  
C total=2590uF



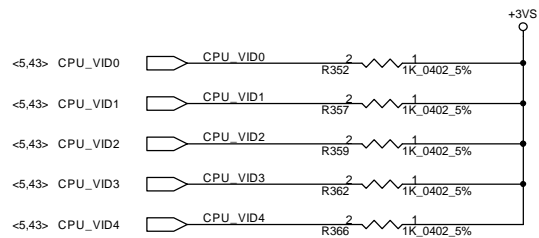
**PLACE ON CPU SIDE**



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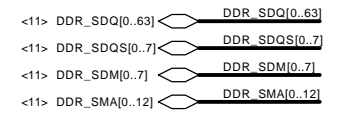
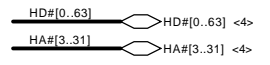
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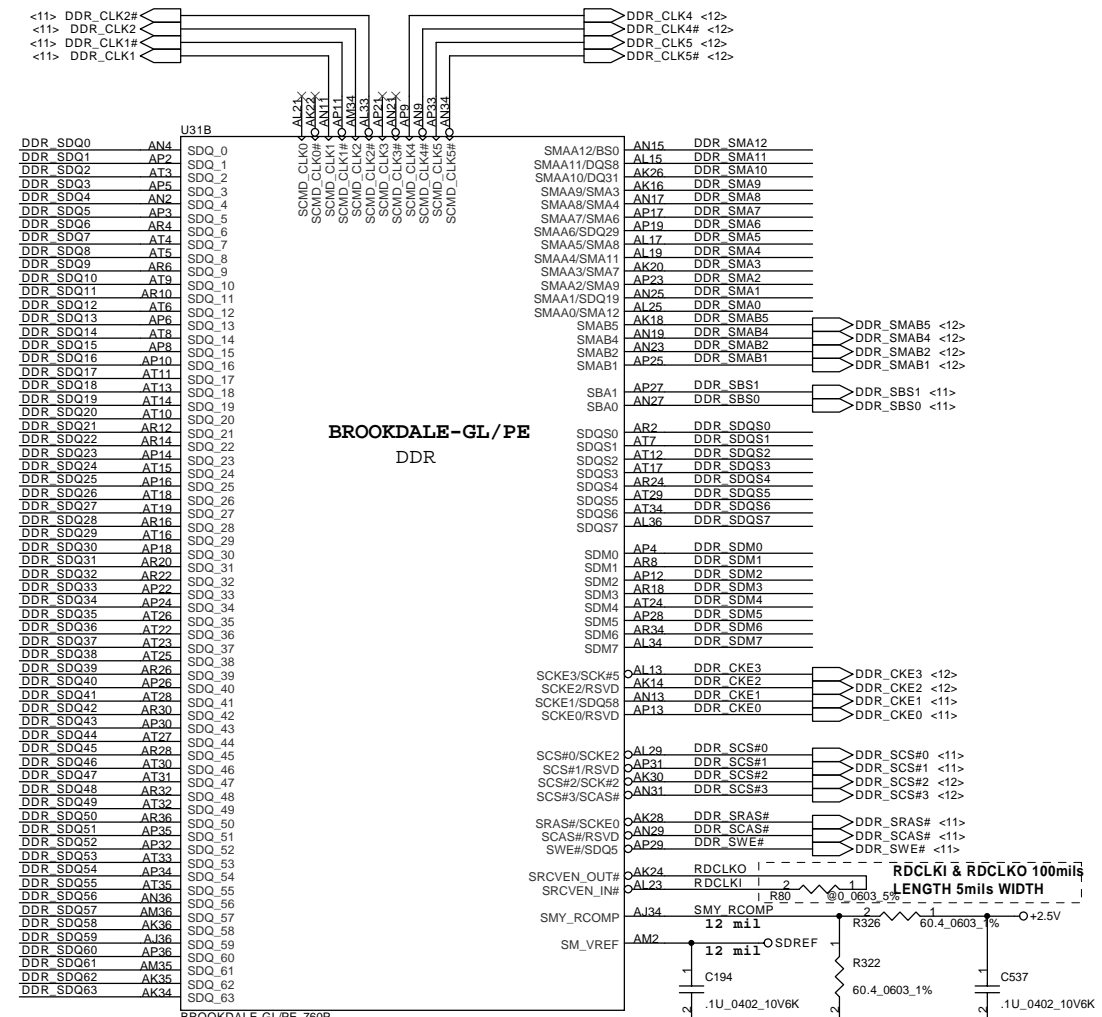
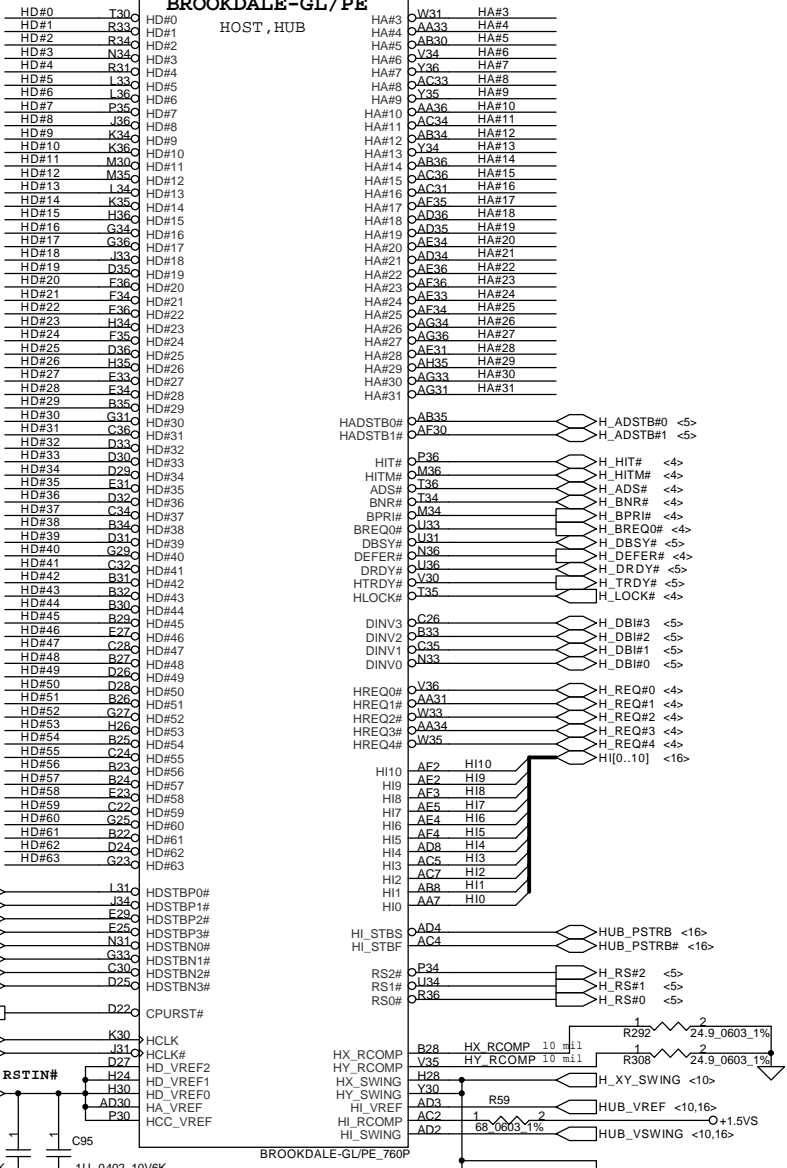
VCC	Desktop CPU				
	VID 4	3	2	1	0
1.750V	0	0	1	0	0
1.700V	0	0	1	1	0
1.650V	0	1	0	0	0
1.600V	0	1	0	1	0
1.550V	0	1	1	0	0
1.500V	0	1	1	1	0
1.450V	1	0	0	0	0
1.400V	1	0	0	1	0
1.350V	1	0	1	0	0
1.300V	1	0	1	1	0
1.250V	1	1	0	0	0
1.200V	1	1	0	1	0
1.150V	1	1	1	0	0
1.100V	1	1	1	1	0
1.050V	X	X	X	X	X
1.000V	X	X	X	X	X
0.975V	X	X	X	X	X
0.950V	X	X	X	X	X
0.925V	X	X	X	X	X
0.900V	X	X	X	X	X
0.875V	X	X	X	X	X
0.850V	X	X	X	X	X
0.825V	X	X	X	X	X
0.800V	X	X	X	X	X
0.775V	X	X	X	X	X
0.750V	X	X	X	X	X
0.725V	X	X	X	X	X
0.700V	X	X	X	X	X
0.675V	X	X	X	X	X
0.650V	X	X	X	X	X
0.625V	X	X	X	X	X
0.600V	X	X	X	X	X
VRM output off	1	1	1	1	1

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U31A  
**BROOKDALE-GL/PE**  
 HOST, HUB



- Layout note :**
- HX\_RCOMP, HY\_RCOMP Trace width 10 mil.
  - Terminator Max 500 mil.

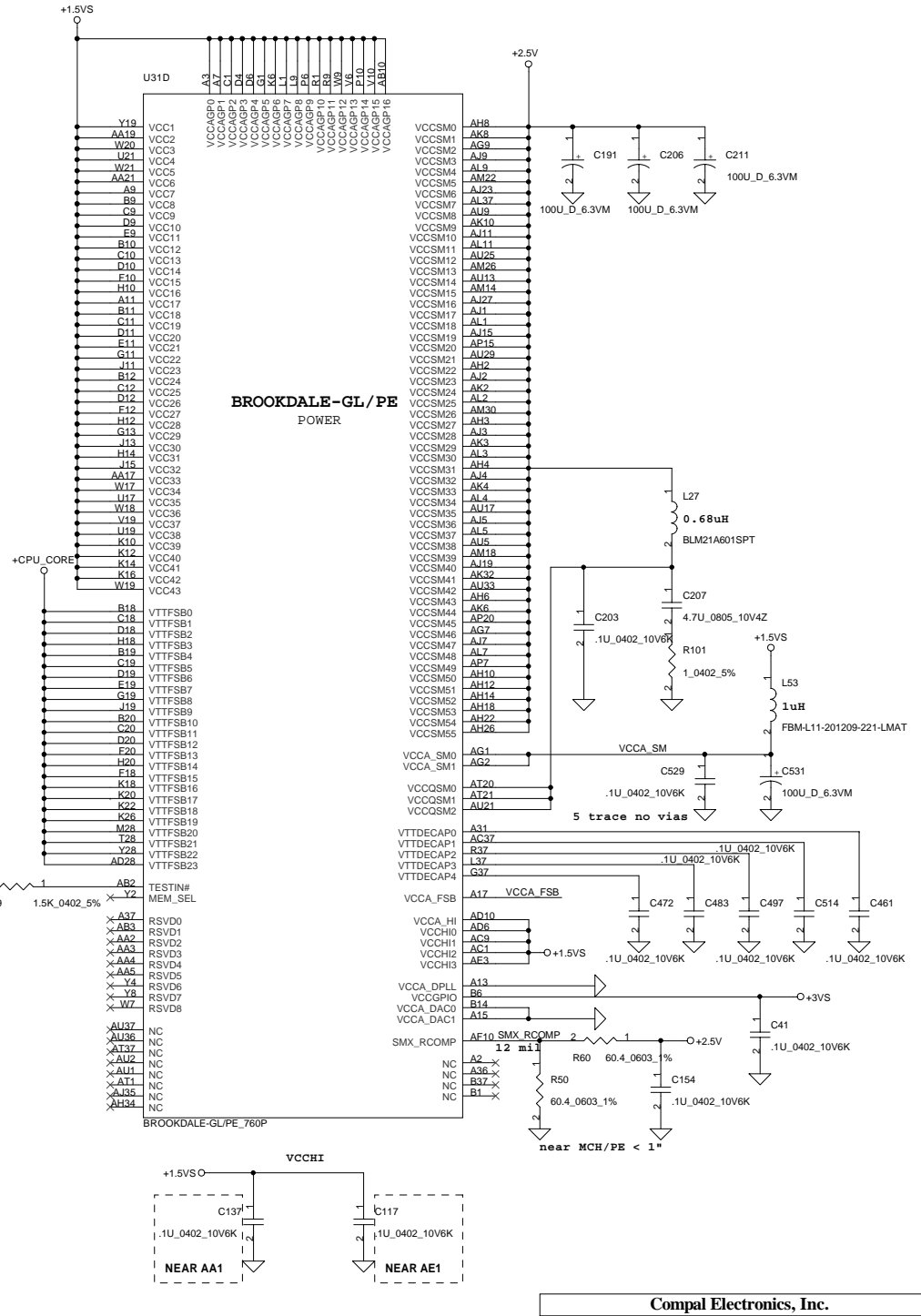
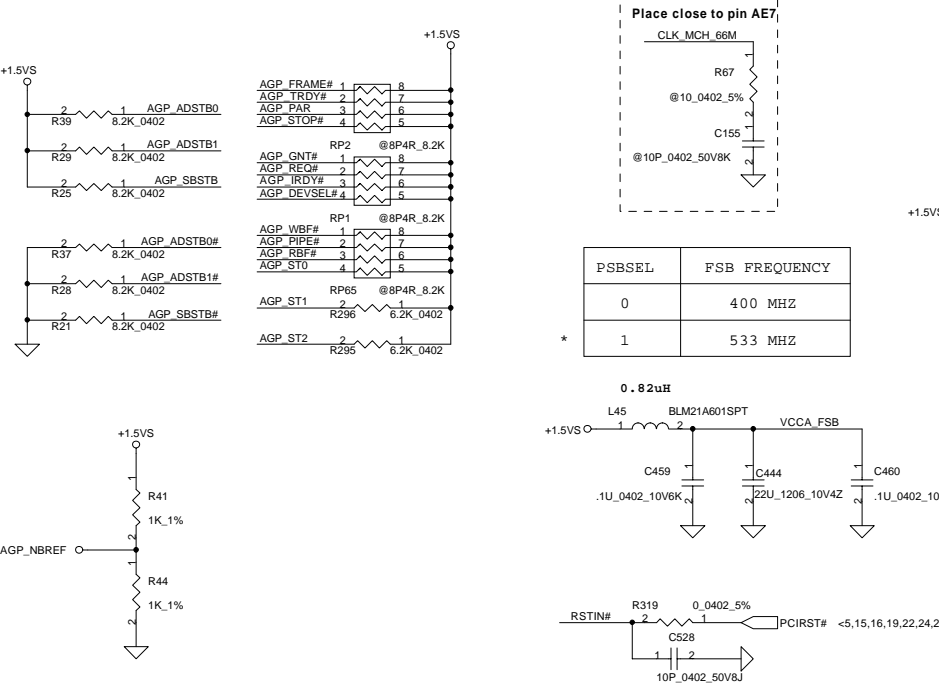
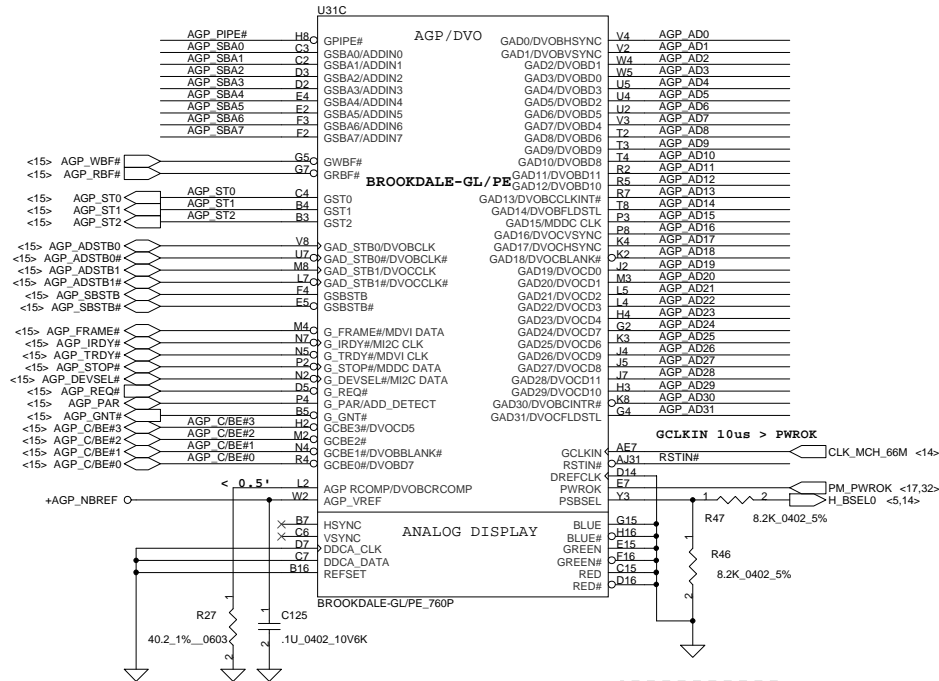
Close to H28  
 Close to Y30

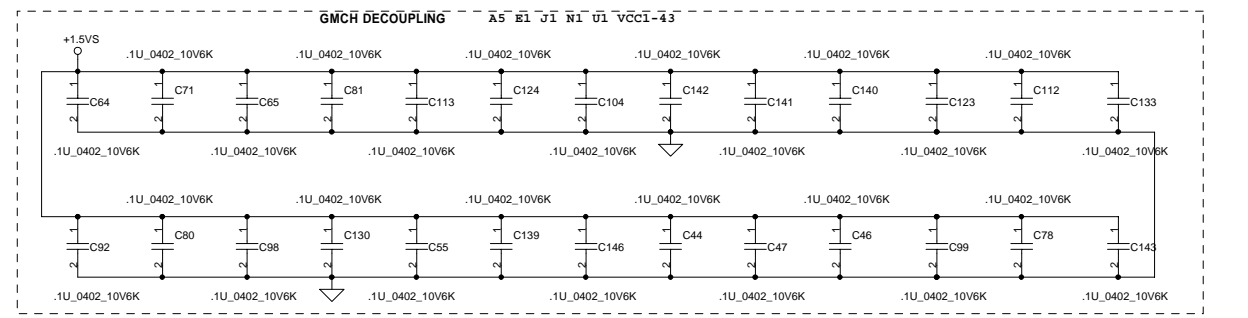
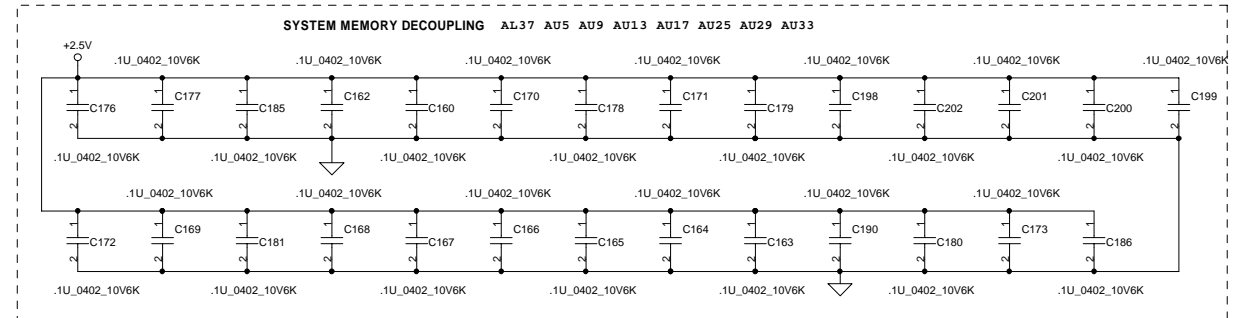
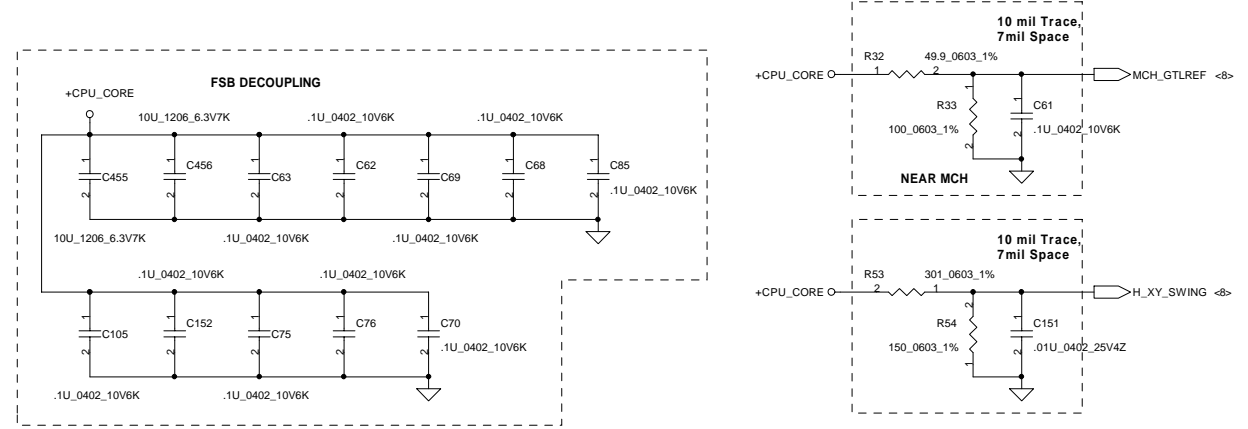
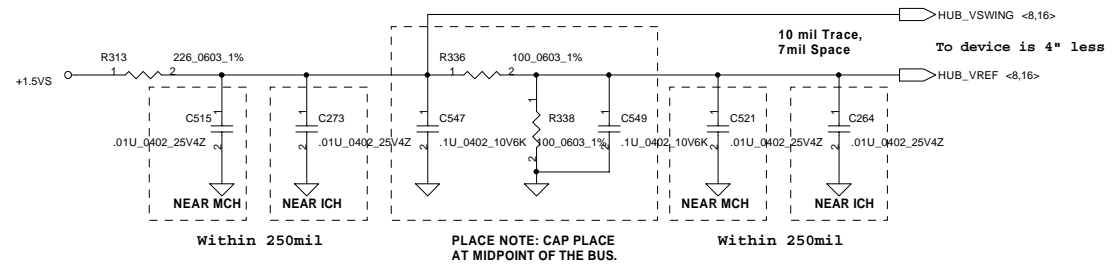
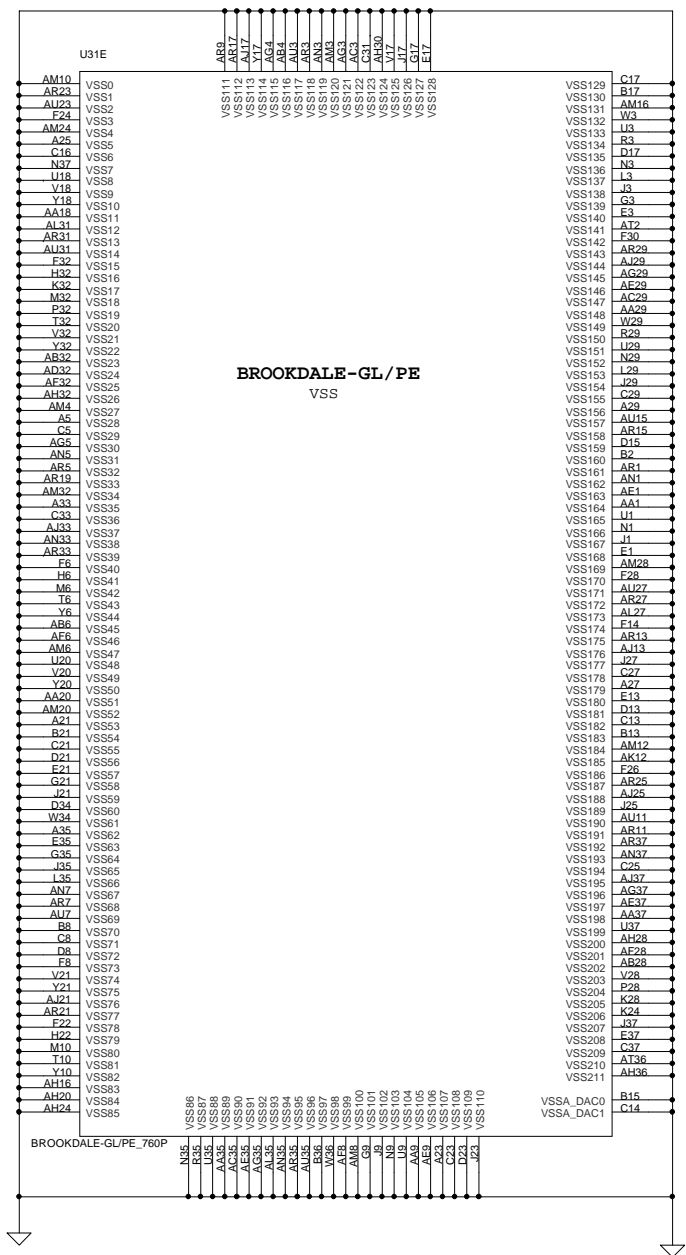
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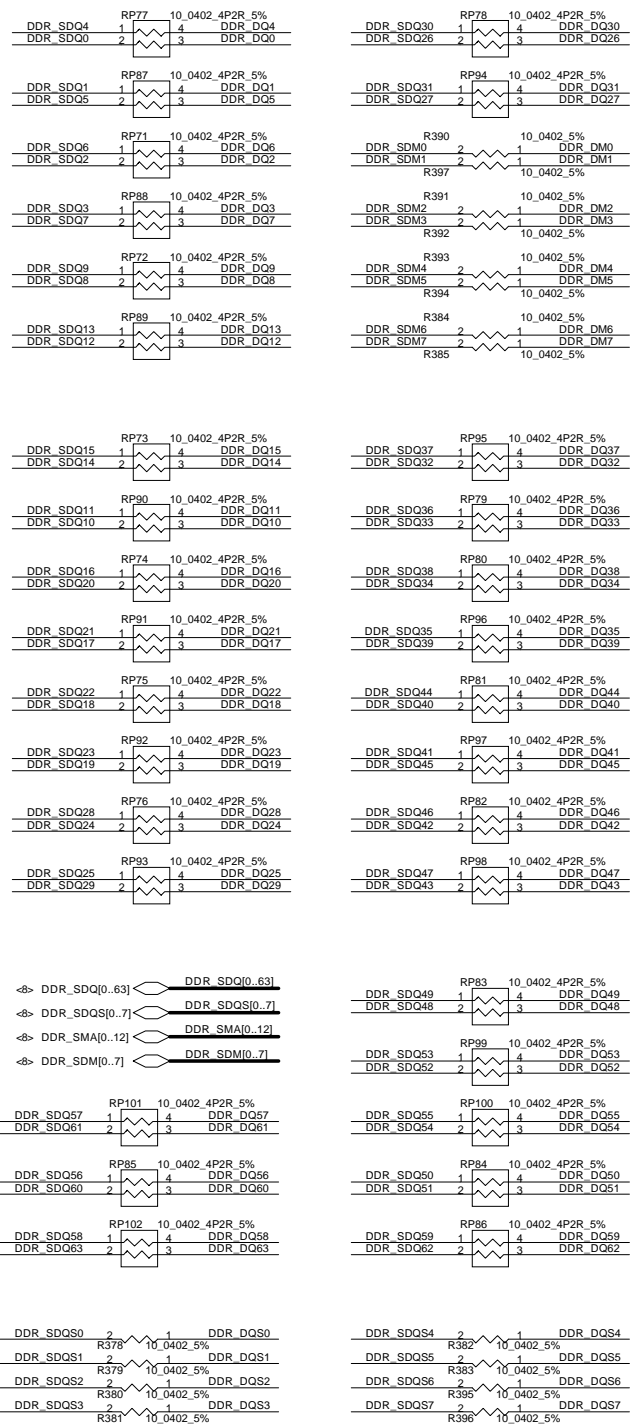
<15> AGP\_AD[0..31] AGP\_AD[0..31]  
 <15> AGP\_SBA[0..7] AGP\_SBA[0..7]





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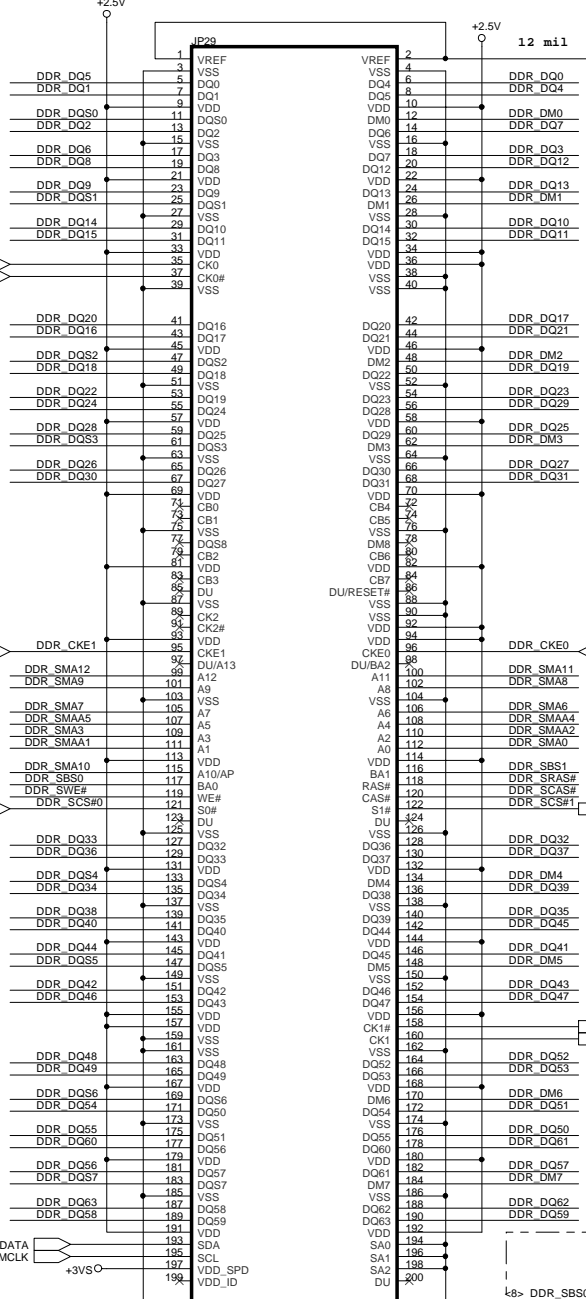
<8> DDR\_CLK1  
<8> DDR\_CLK1#

<8> DDR\_CKE1

<8> DDR\_SCS#0

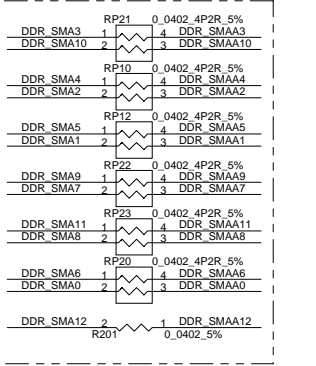
<8> DDR\_SQ[0..63]  
<8> DDR\_SQS[0..7]  
<8> DDR\_SMA[0..12]  
<8> DDR\_SDM[0..7]

**Layout note**  
Place these resistors  
close to DIMM0,  
all trace length<500 mil



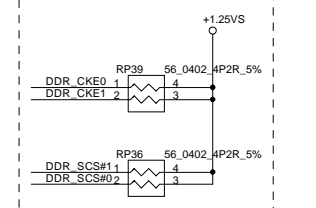
**DIMM0**  
Front side / H=5.2mm

<8> DDR\_DQ[0..63]  
<8> DDR\_DQS[0..7]  
<8> DDR\_DM[0..7]  
<8> DDR\_SMAA[0..12]



**Note:**  
Place Close to DIMM0

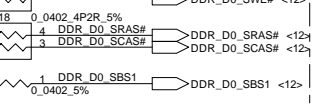
**Layout note**  
Place these resistor  
close to DIMM0,  
all trace length  
Max=1.4"



<8> DDR\_CLK2#  
<8> DDR\_CLK2



**Note: Place Close to DIMM0**



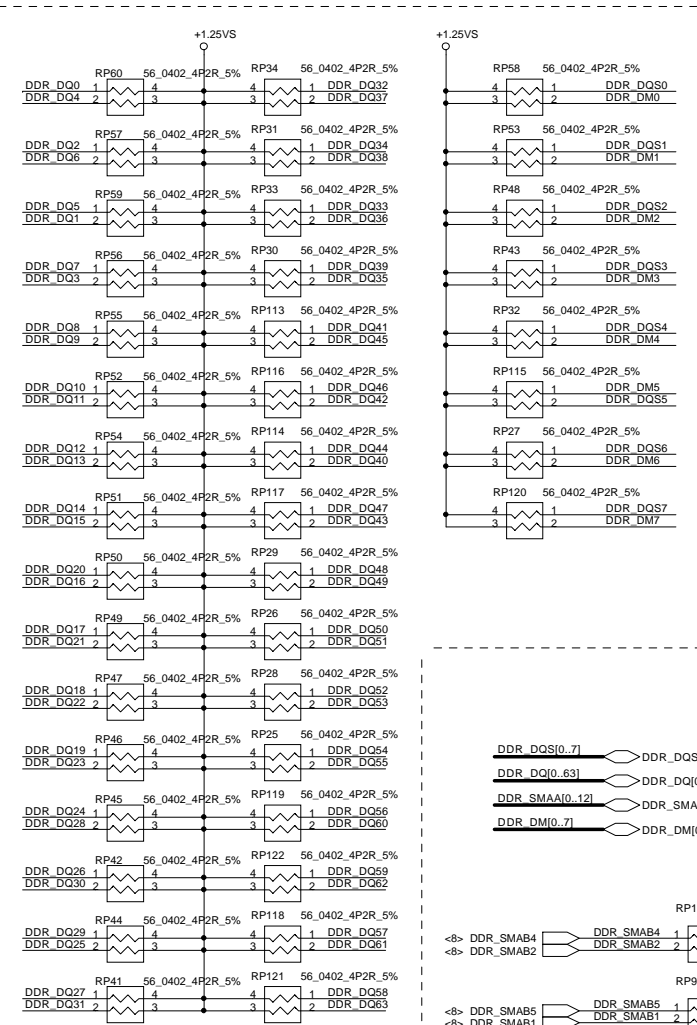
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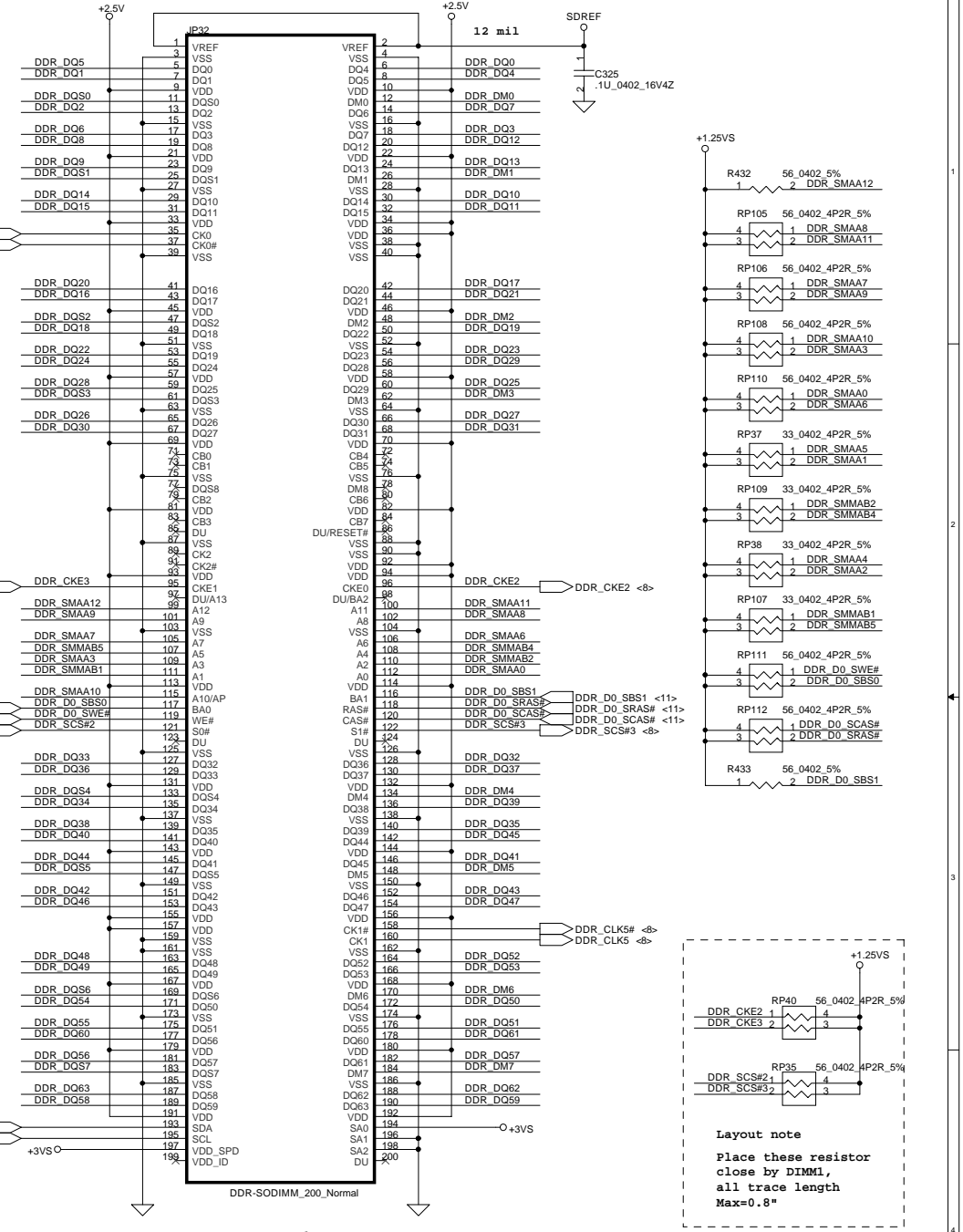
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**Layout note**  
Place these resistor closely DIMM1, all trace length<=800mil

DDR\_DQS[0..7] <11>  
DDR\_DQ[0..63] <11>  
DDR\_SMAA[0..12] <11>  
DDR\_DM[0..7] <11>

RP11 0\_0402\_4P2R\_5%  
RP9 0\_0402\_4P2R\_5%



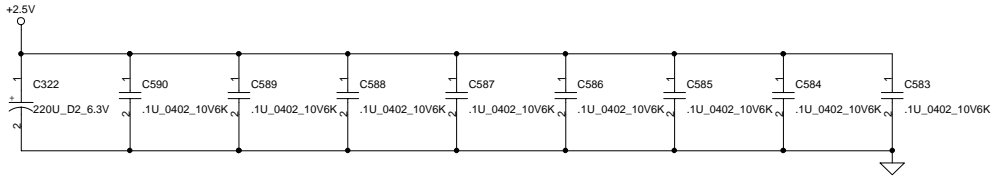
**DIMM1**  
Back side / H=9.2mm

**Layout note**  
Place these resistor close by DIMM1, all trace length Max=0.8"

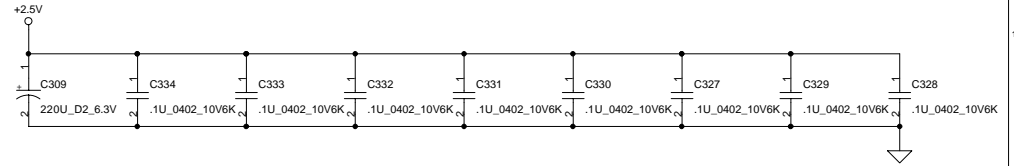
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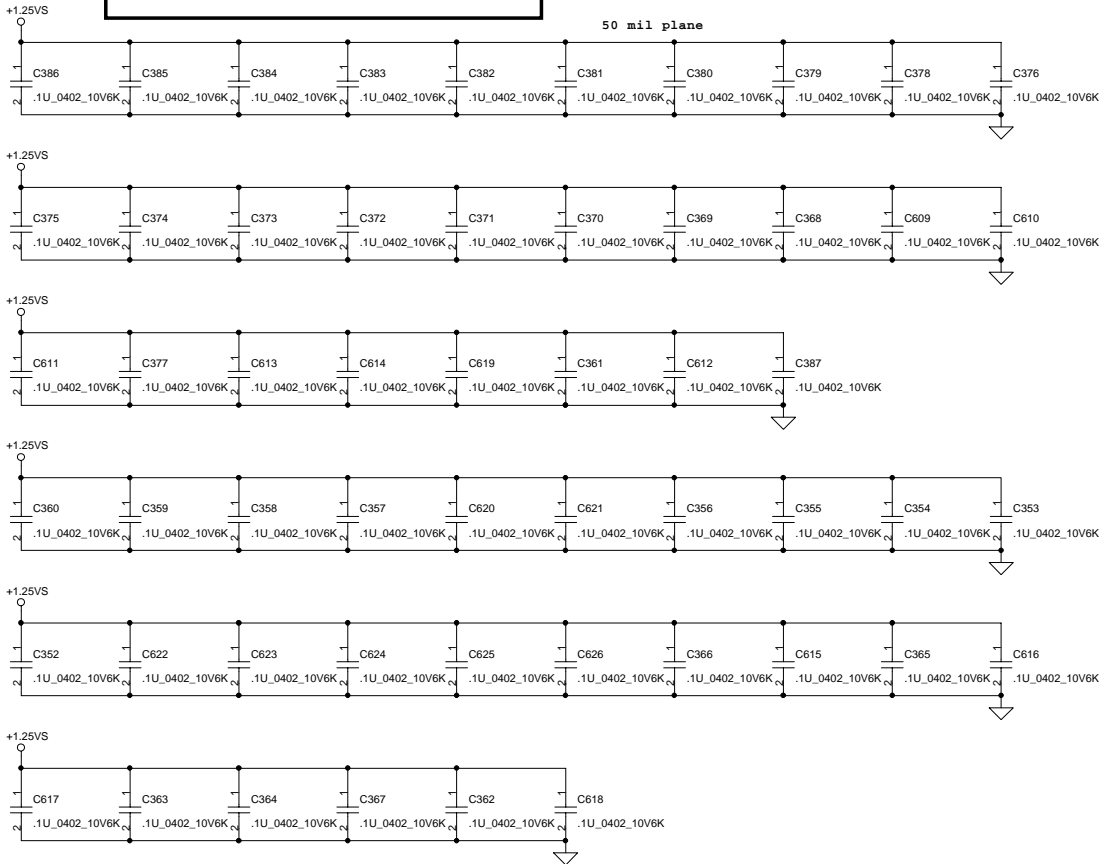
**Layout note :**  
Distribute as close as possible to DDR-SODIMM0.



**Layout note :**  
Distribute as close as possible to DDR-SODIMM1.



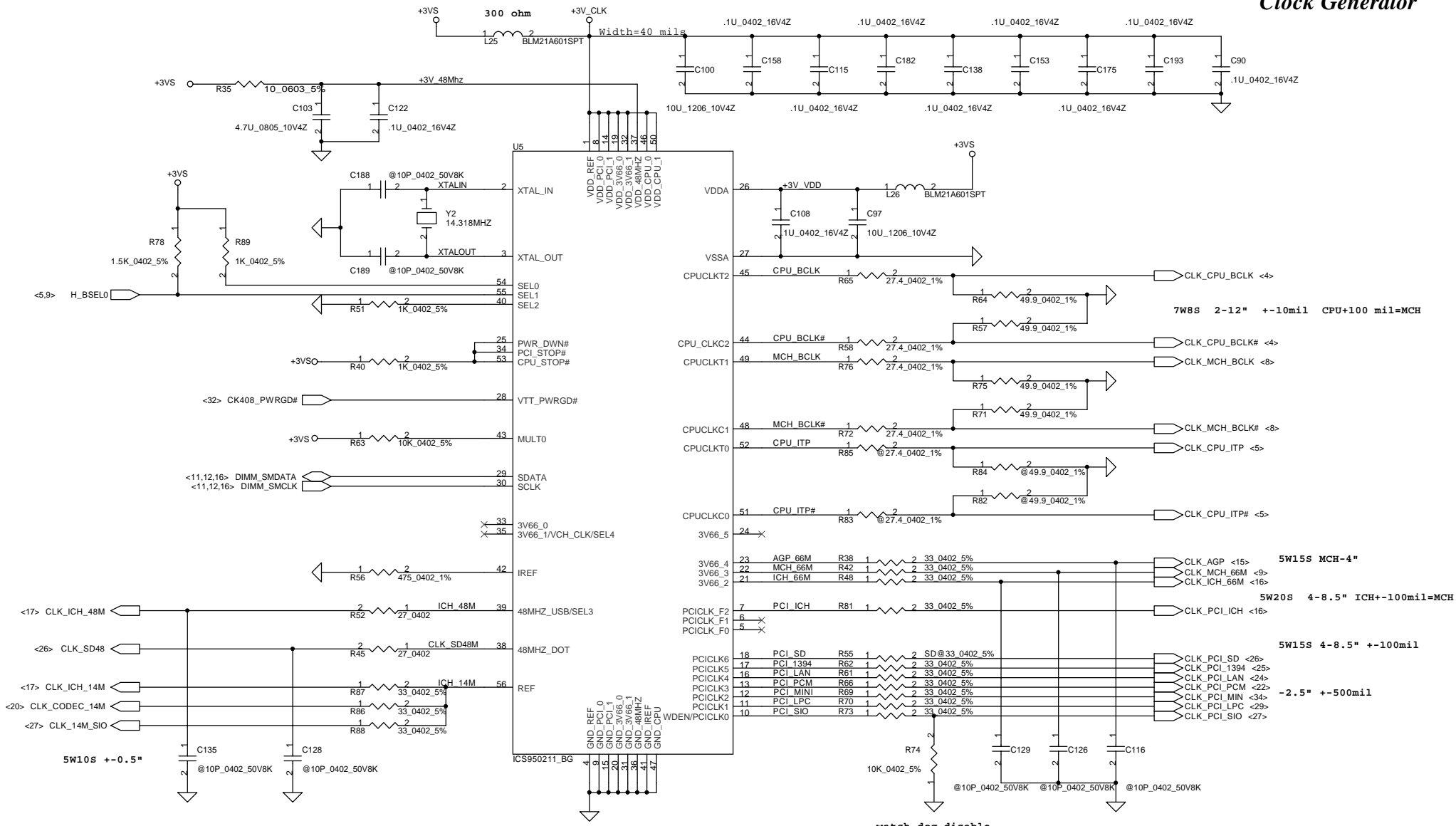
**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +1.25VS



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# Clock Generator



**CPU Frequency Select Table**

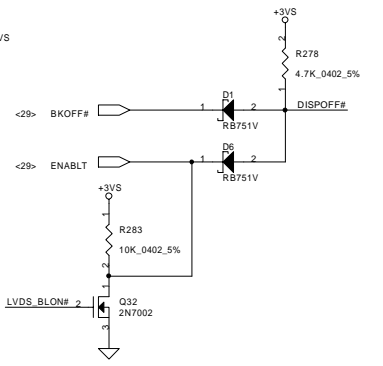
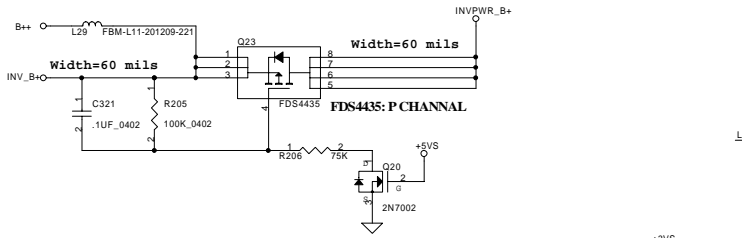
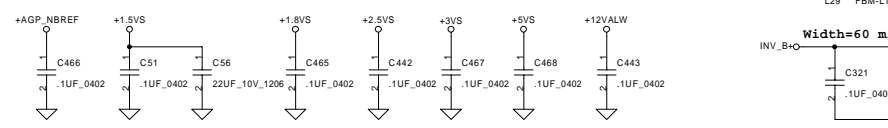
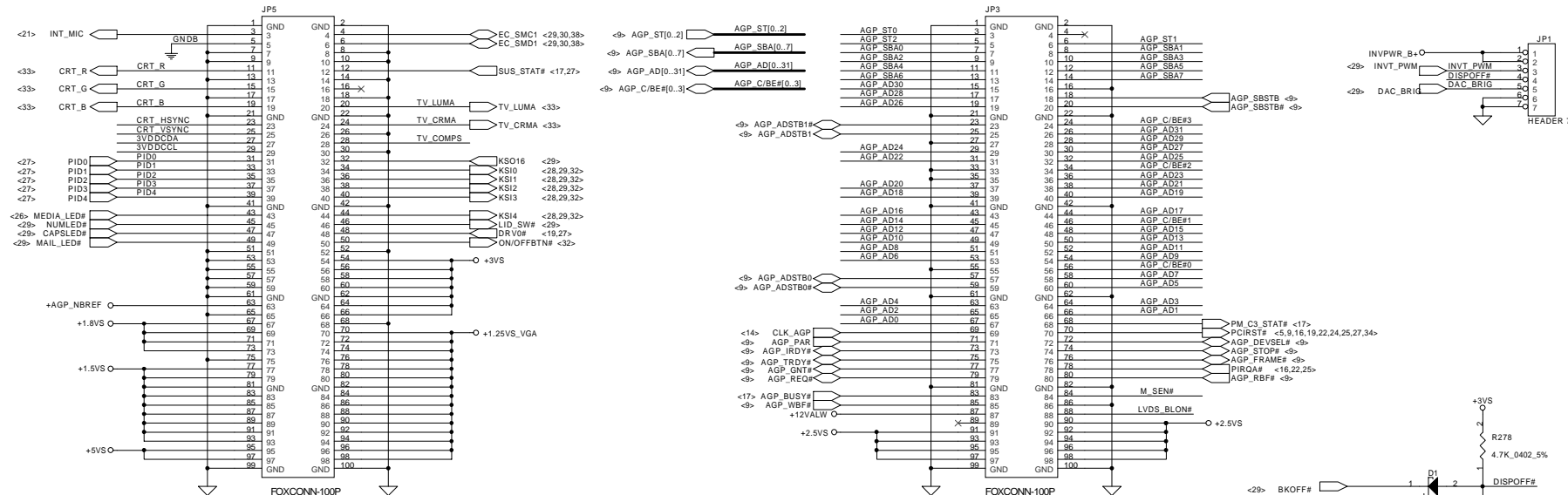
SEL[2:0]	CK-408 Speed
001	100 MHZ
* 011	133 MHZ

ground plane inside the part pads  
one power plane inside the part pads

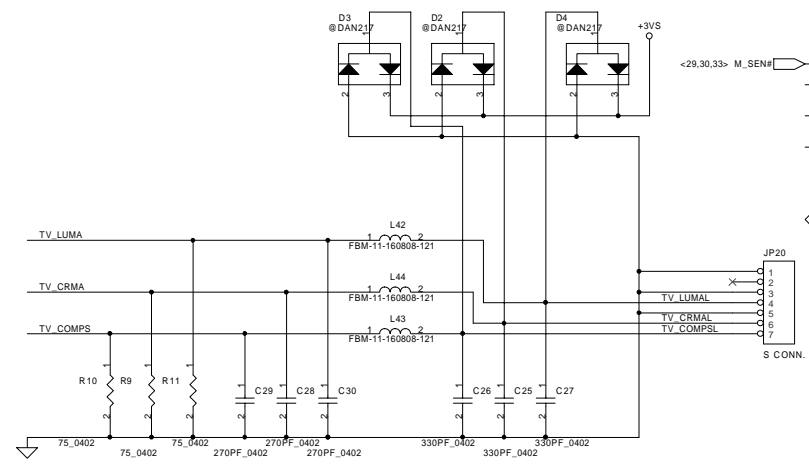
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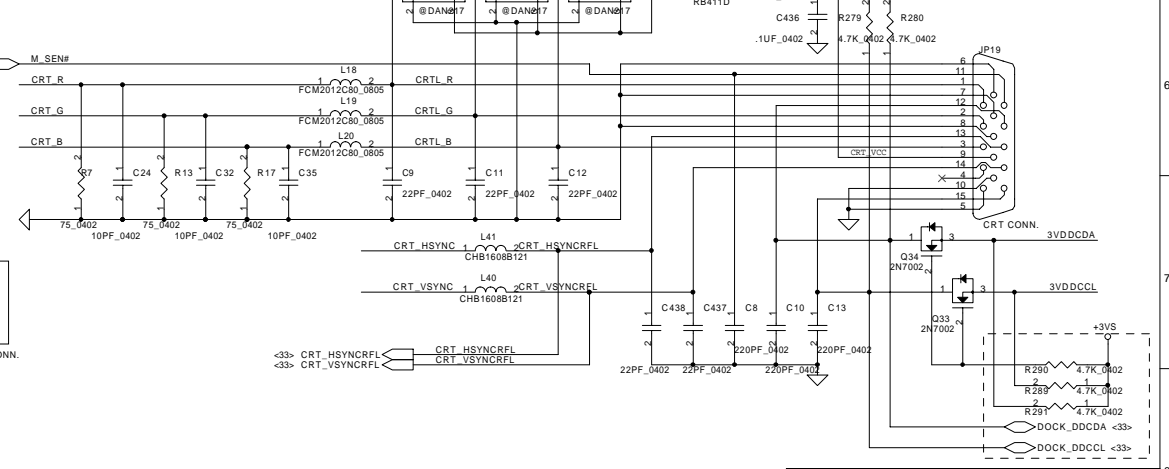
# AGP 100X2 Pin connector

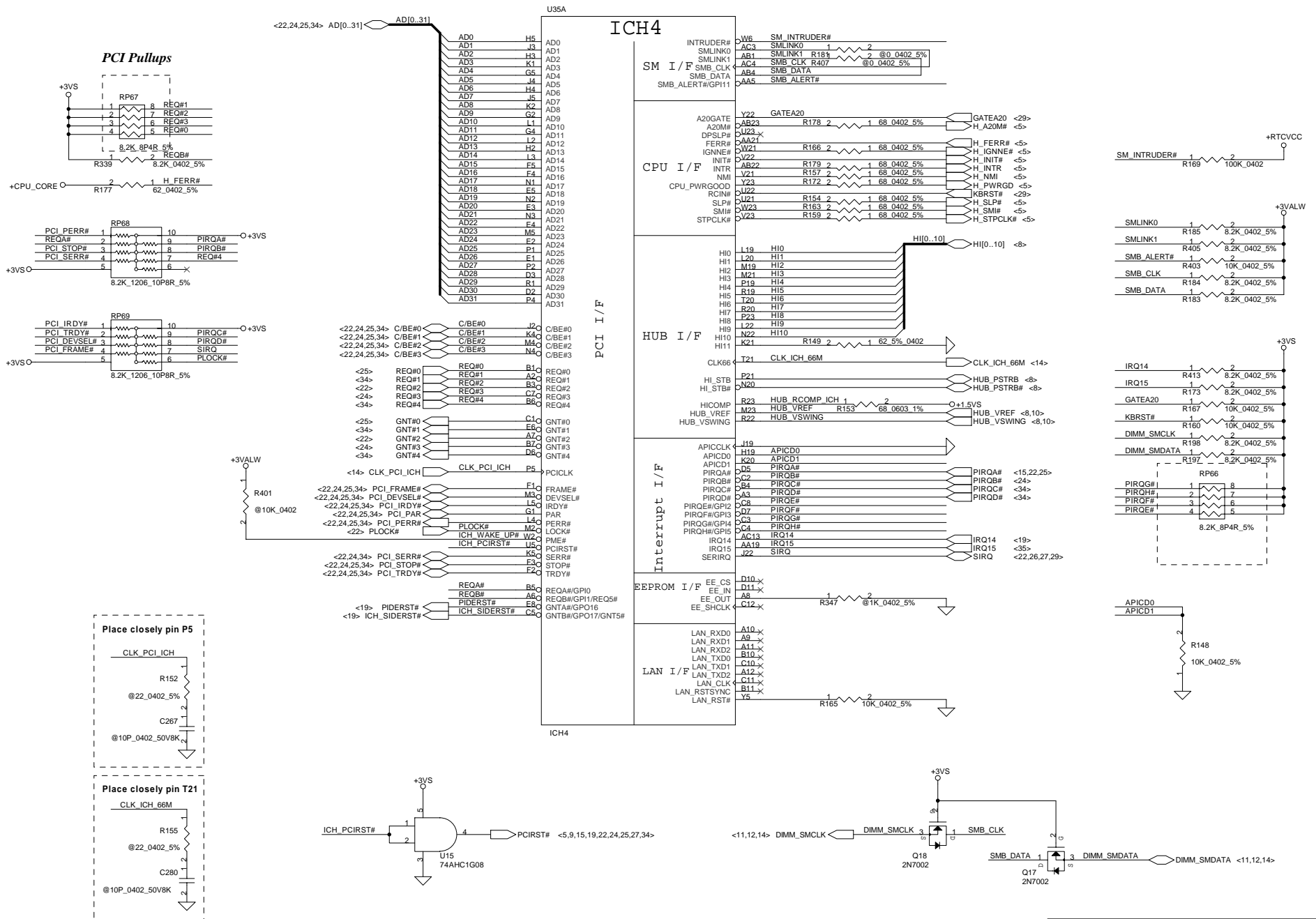


# TV\_OUT CONNECTOR

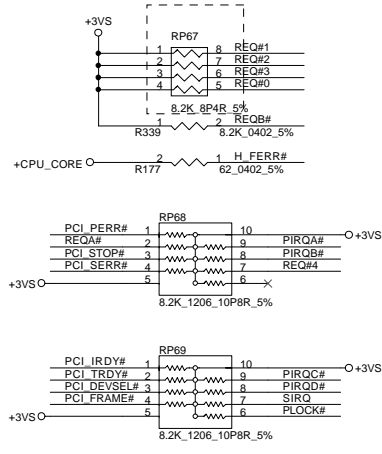


# CRT CONNECTOR

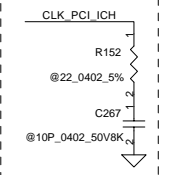




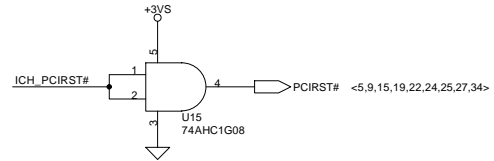
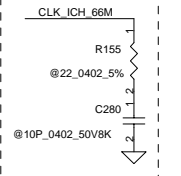
**PCI Pullups**



**Place closely pin P5**



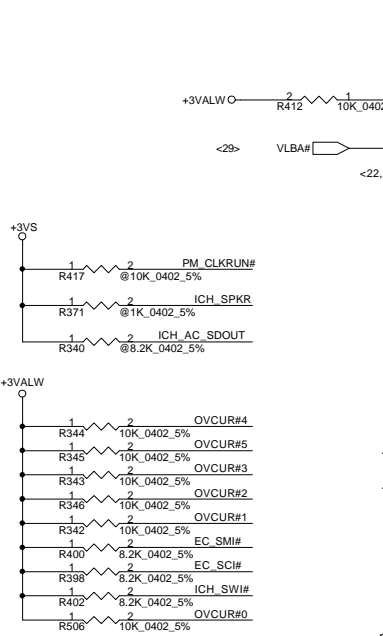
**Place closely pin T21**



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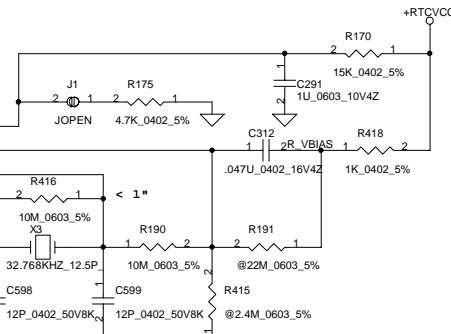
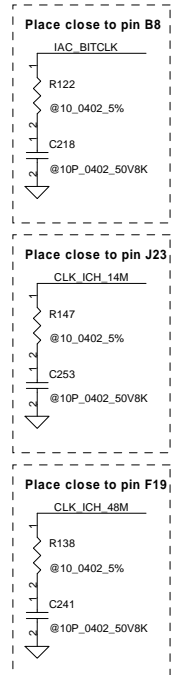
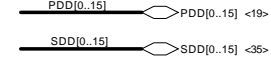
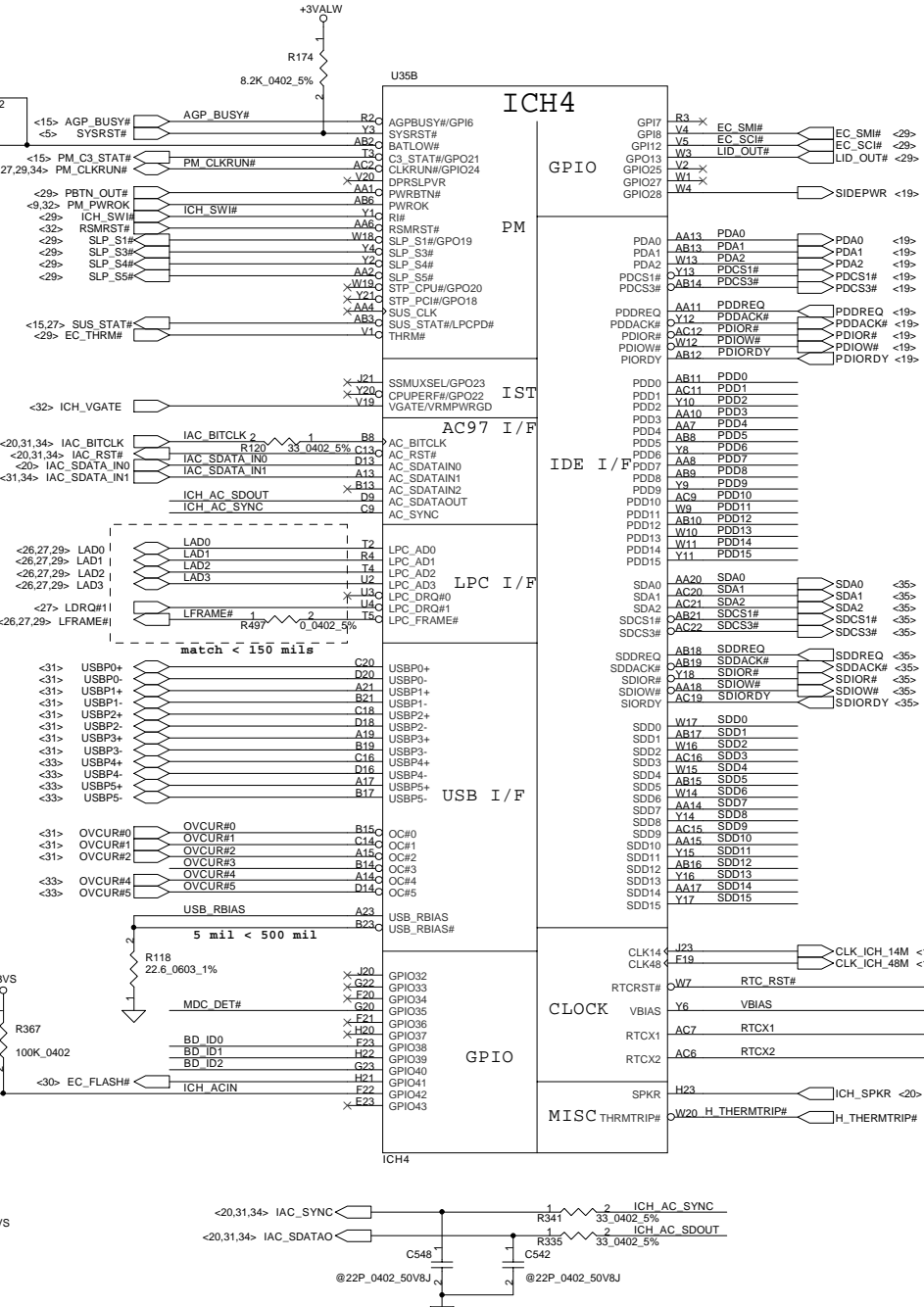
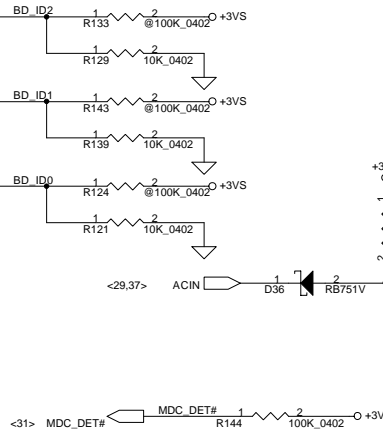
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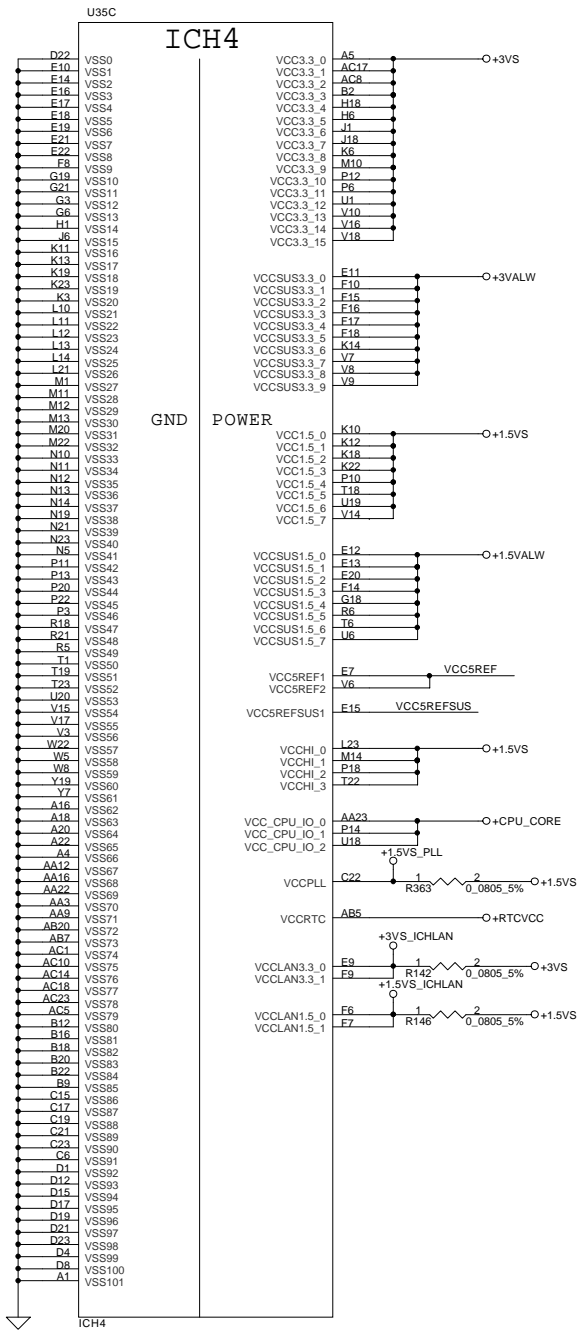
**BOARD ID**

	BD_ID2	BD_ID1	BD_ID0
SST	0	0	0
PT	0	0	1
ST	0	1	0
QT	0	1	1

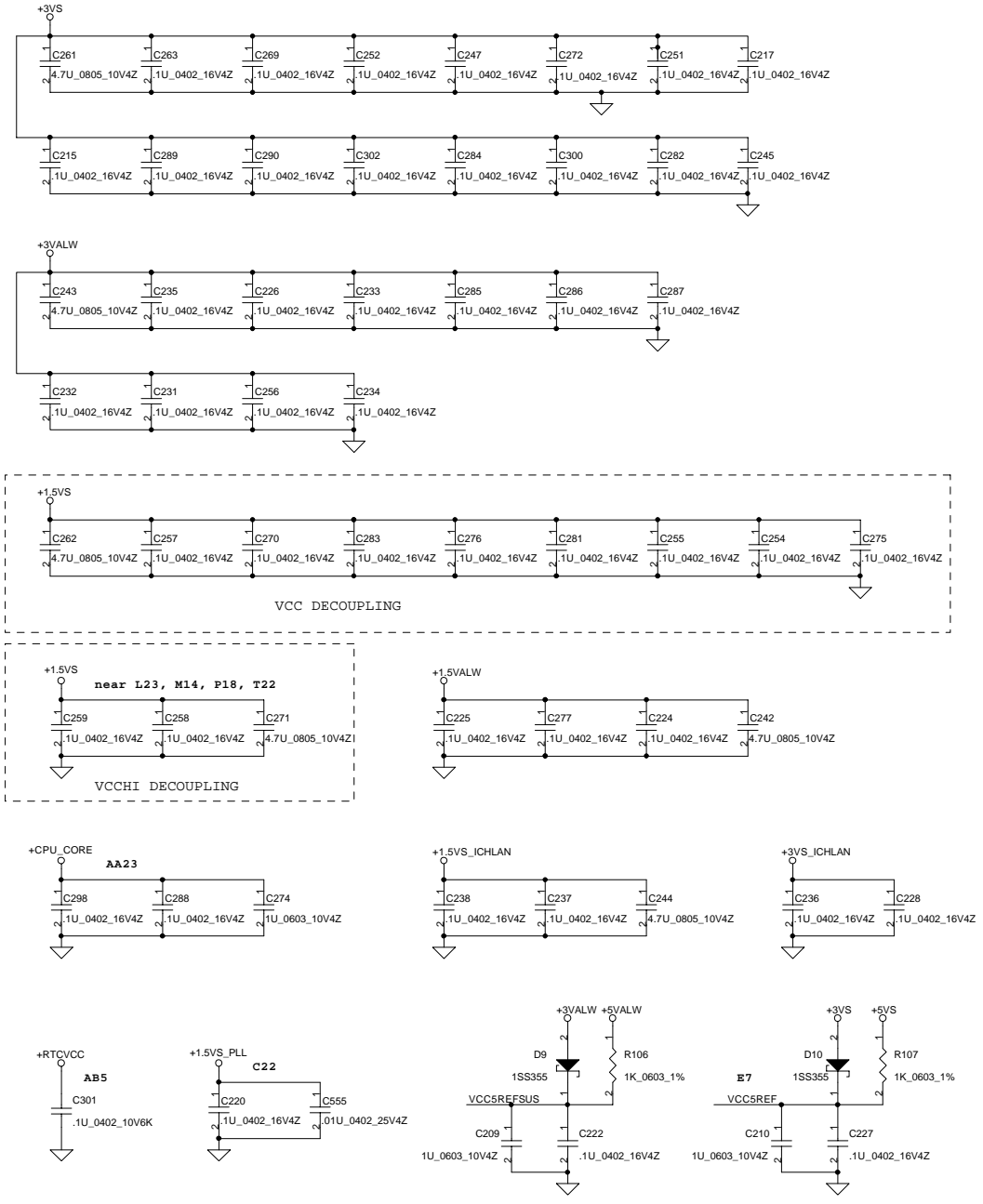


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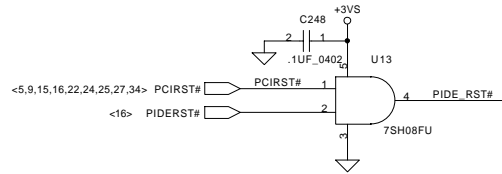


A4 A1 H1 T1 AC10 AC18 A22 AC5 K23 C23 A16 AC1 A16 T23 N23

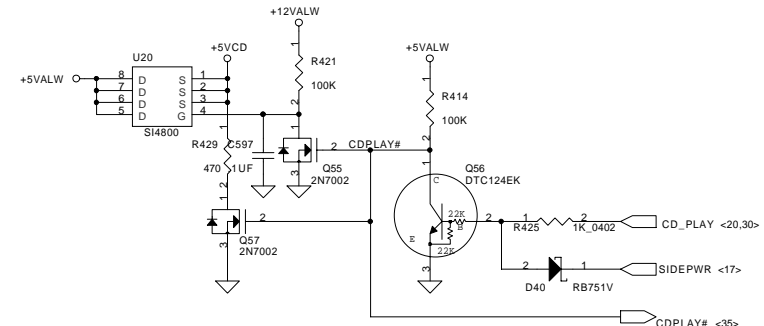
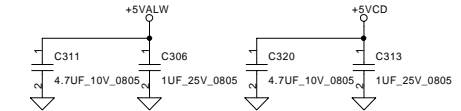
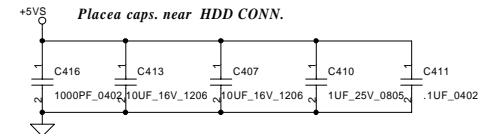
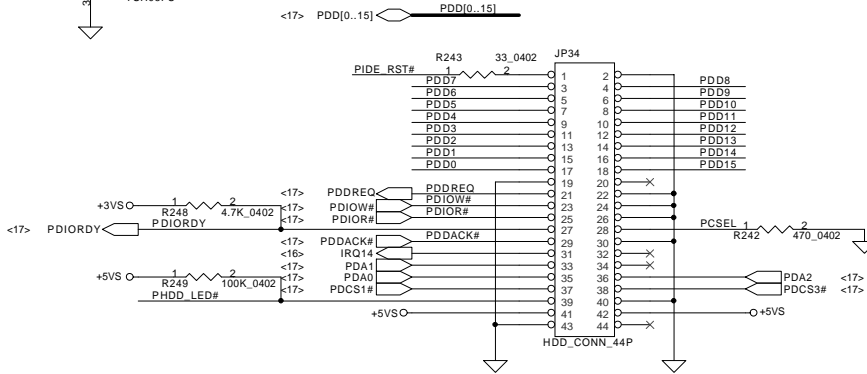
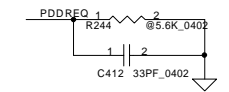
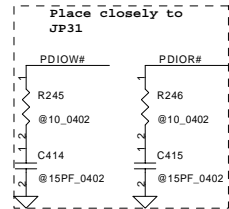


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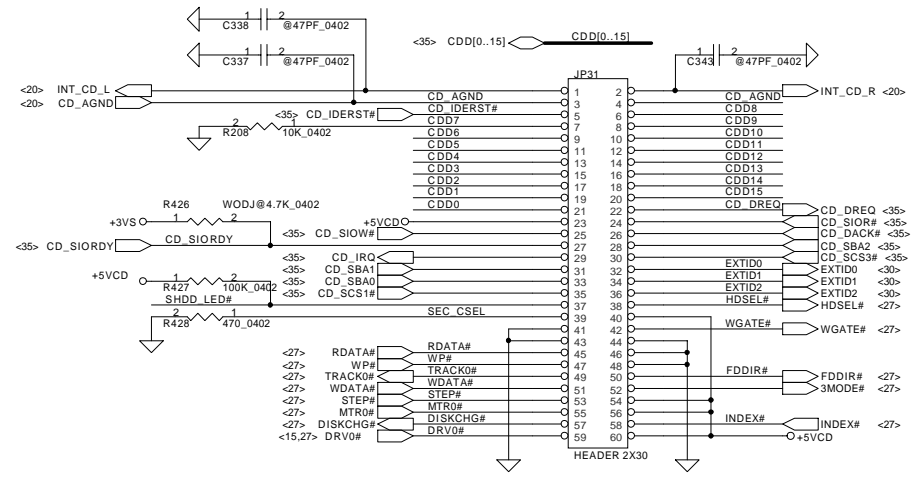
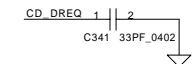
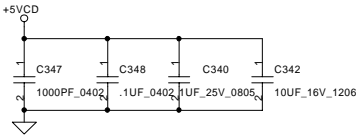
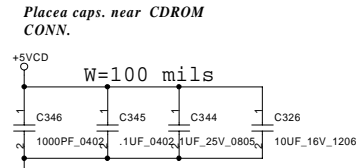
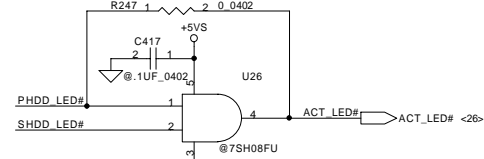
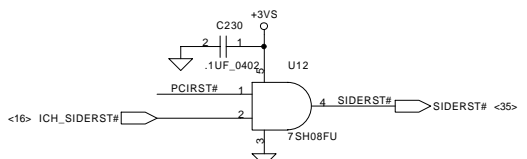
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### HDD Connector



### CD-ROM Connector



### Place caps. near CDROM CONN.

### Extend Module ID list

DEVICE	EXTID2	EXTID1	EXTID0
FDD	0	0	0
CD-ROM	0	0	1
LS-120	0	1	0
2'nd HDD	0	1	1
NONE	1	1	1

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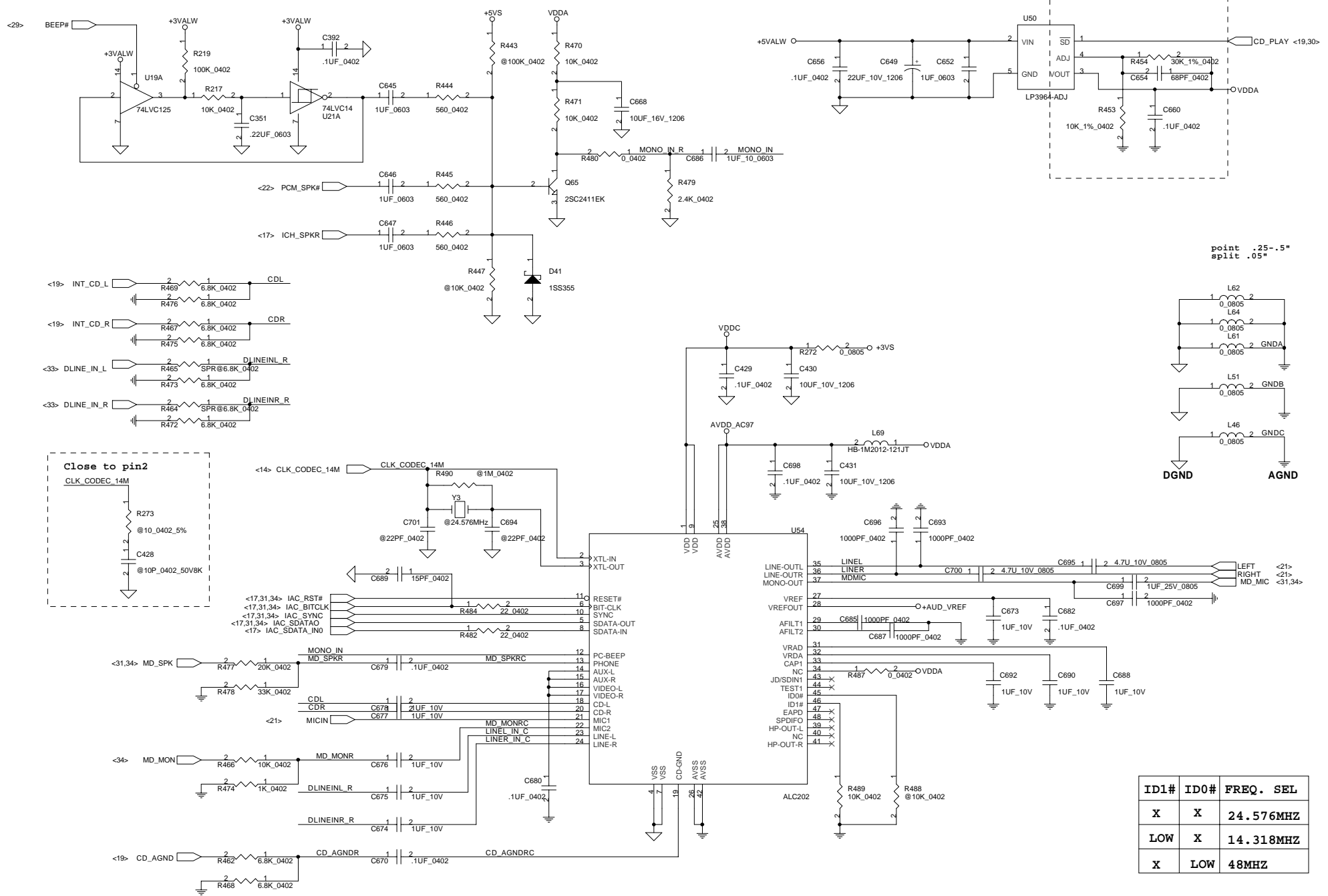
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Size: Document Number 401248

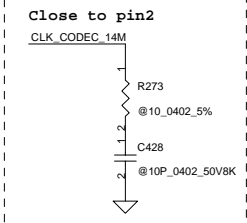
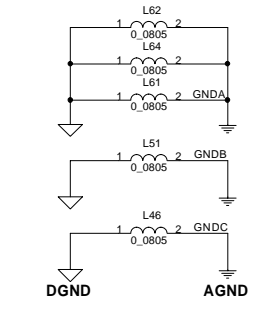
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point .25-.5"  
split .05"



IDI#	ID0#	FREQ. SEL
X	X	24.576MHZ
LOW	X	14.318MHZ
X	LOW	48MHZ

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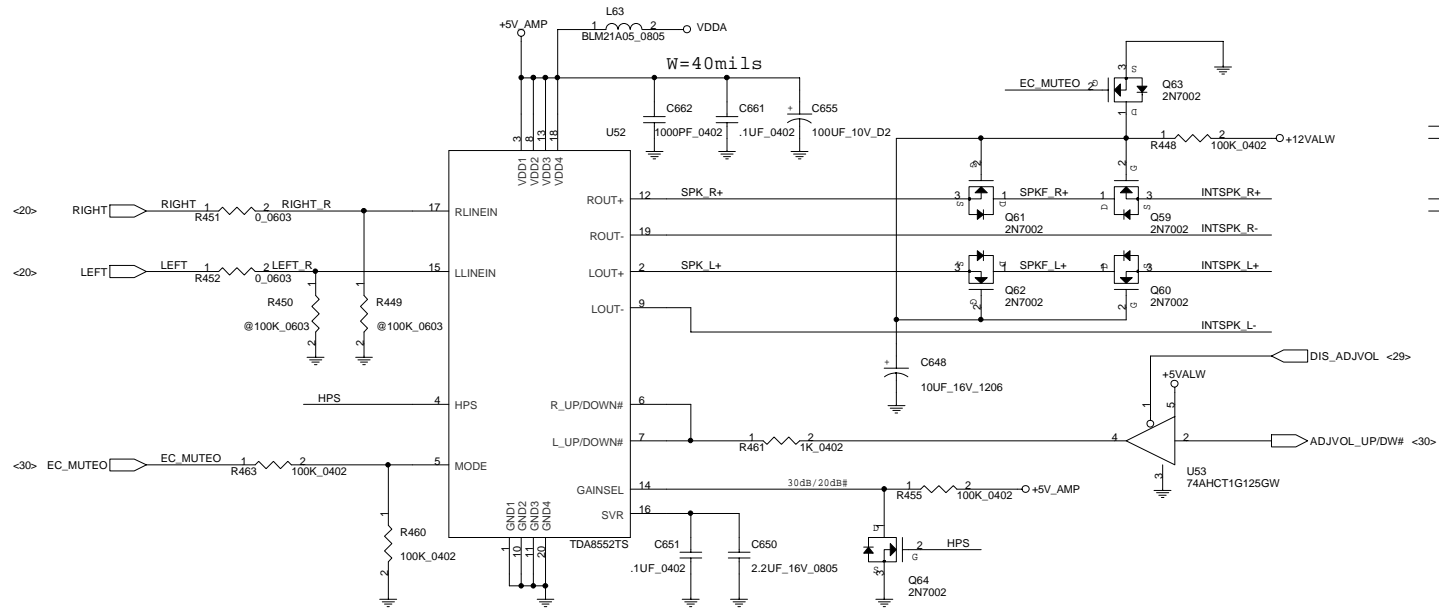
Size: Document Number 401248

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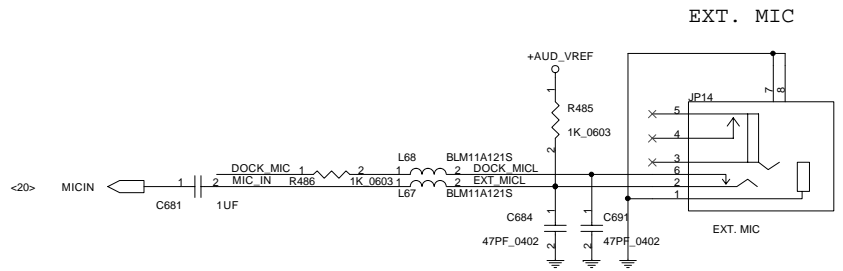
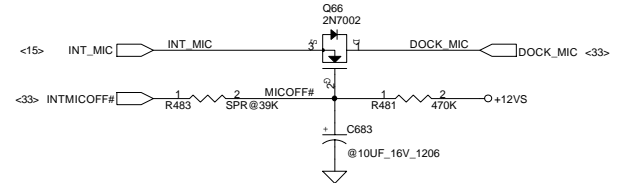
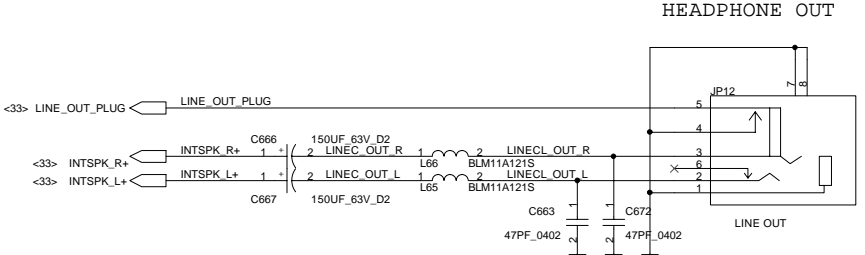
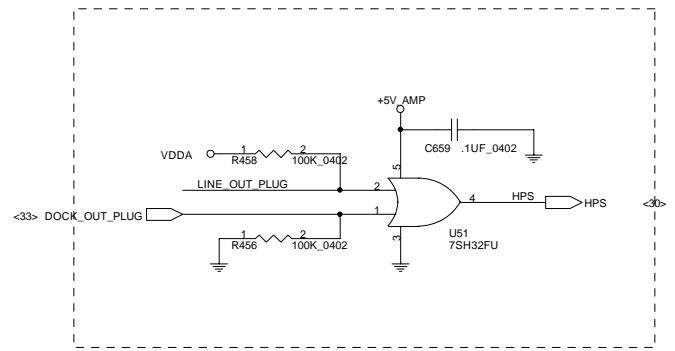
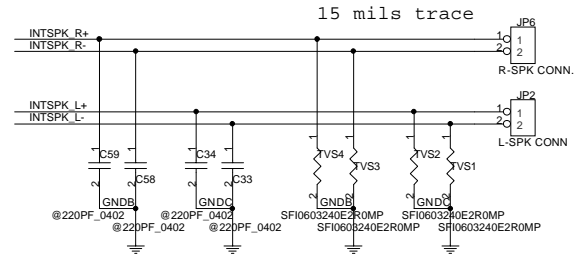
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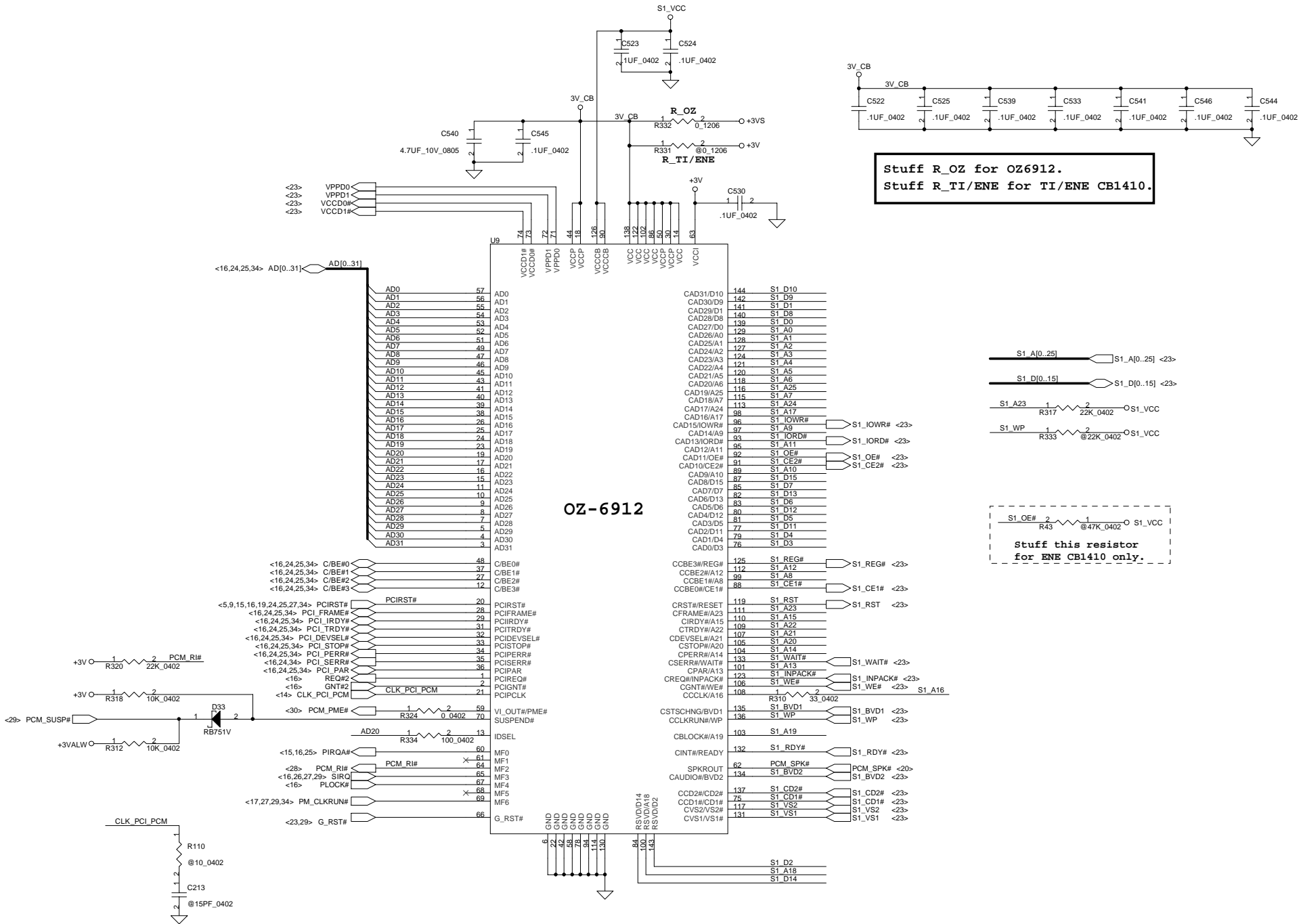


**Layout note:**  
 Trace width=15 mils.  
 1. SPK\_R+, SPK\_L+, SPKF\_R+, SPKF\_L+  
 2. INTSPK\_R+/-, INTSPK\_L+/-  
 3. LINEOUT\_L, LINEOUT\_R



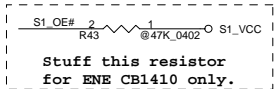
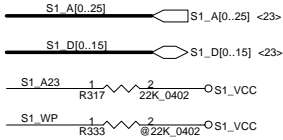
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**OZ-6912**

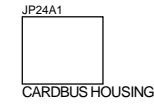
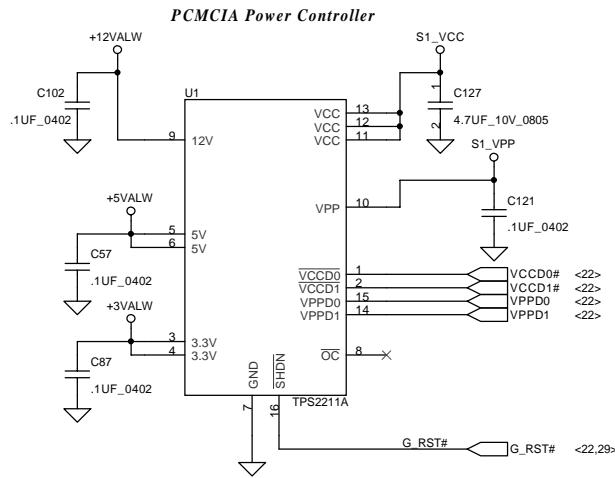
**Stuff R\_OZ for OZ6912.  
Stuff R\_TI/ENE for TI/ENE CBL410.**



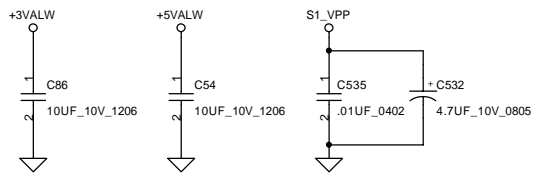
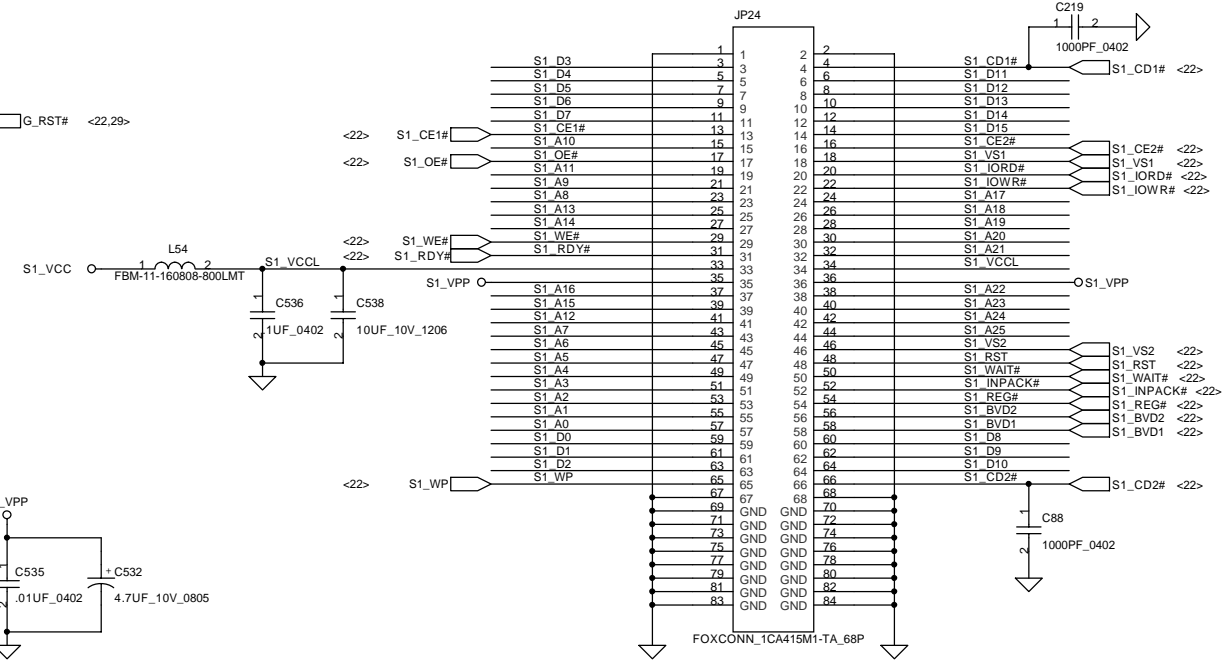
**Stuff this resistor  
for ENE CBL410 only.**

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**CardBus Socket**



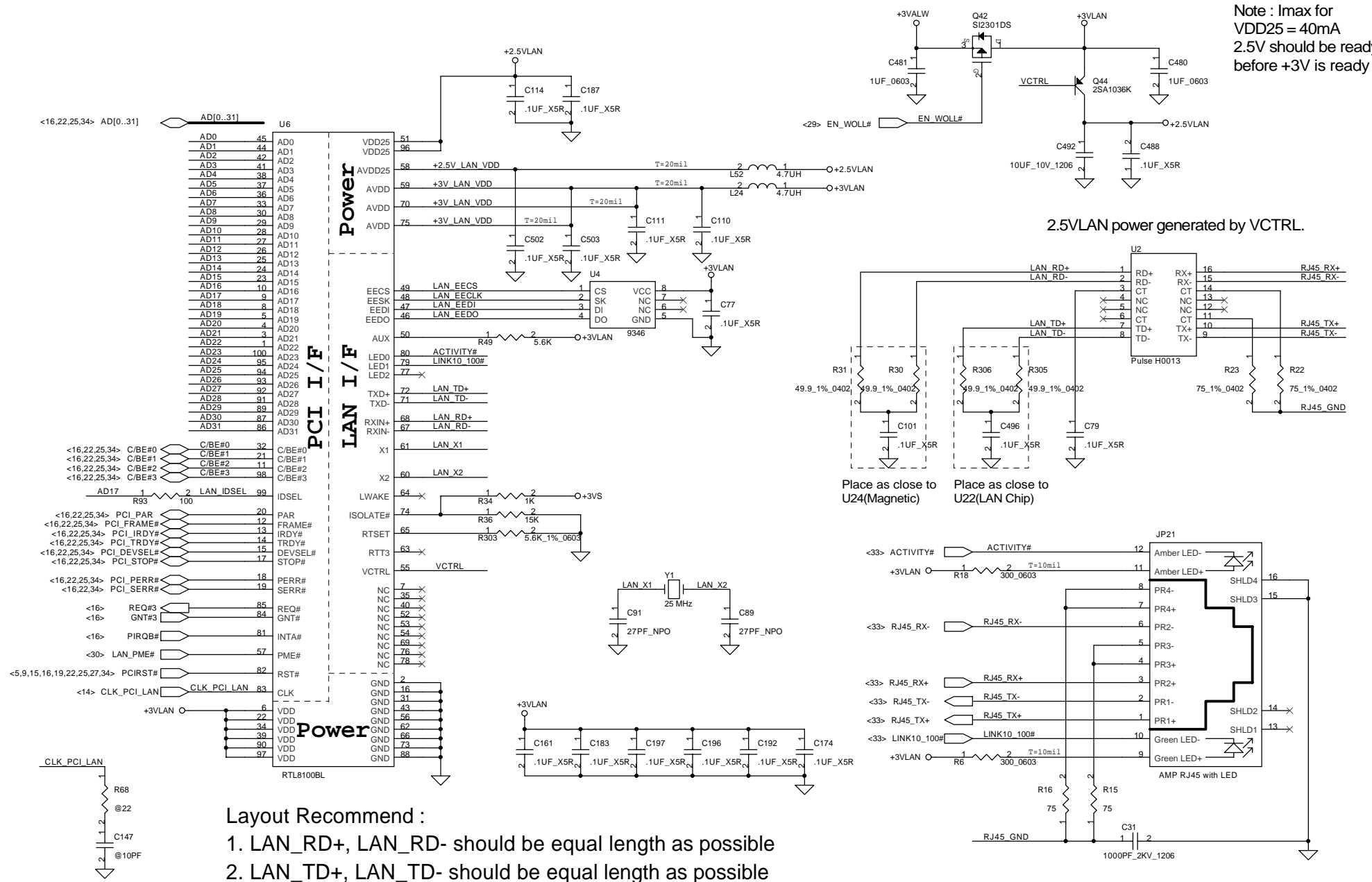
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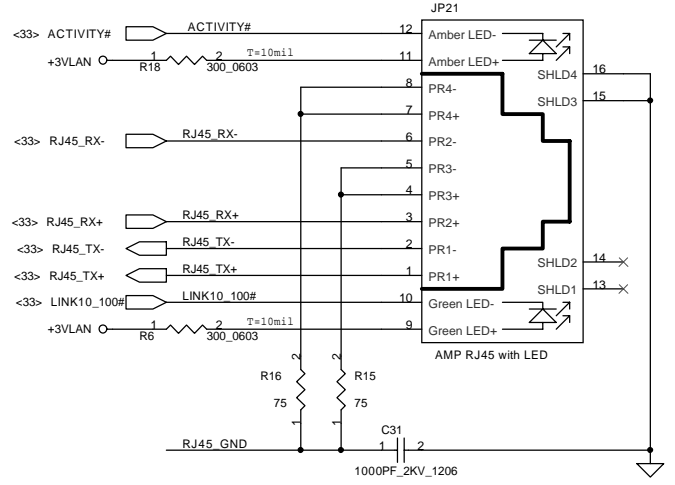
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Note : I<sub>max</sub> for VDD25 = 40mA  
2.5V should be ready before +3V is ready

2.5VLAN power generated by VCTRL.

Place as close to U24(Magnetic)  
Place as close to U22(LAN Chip)



Layout Recommend :

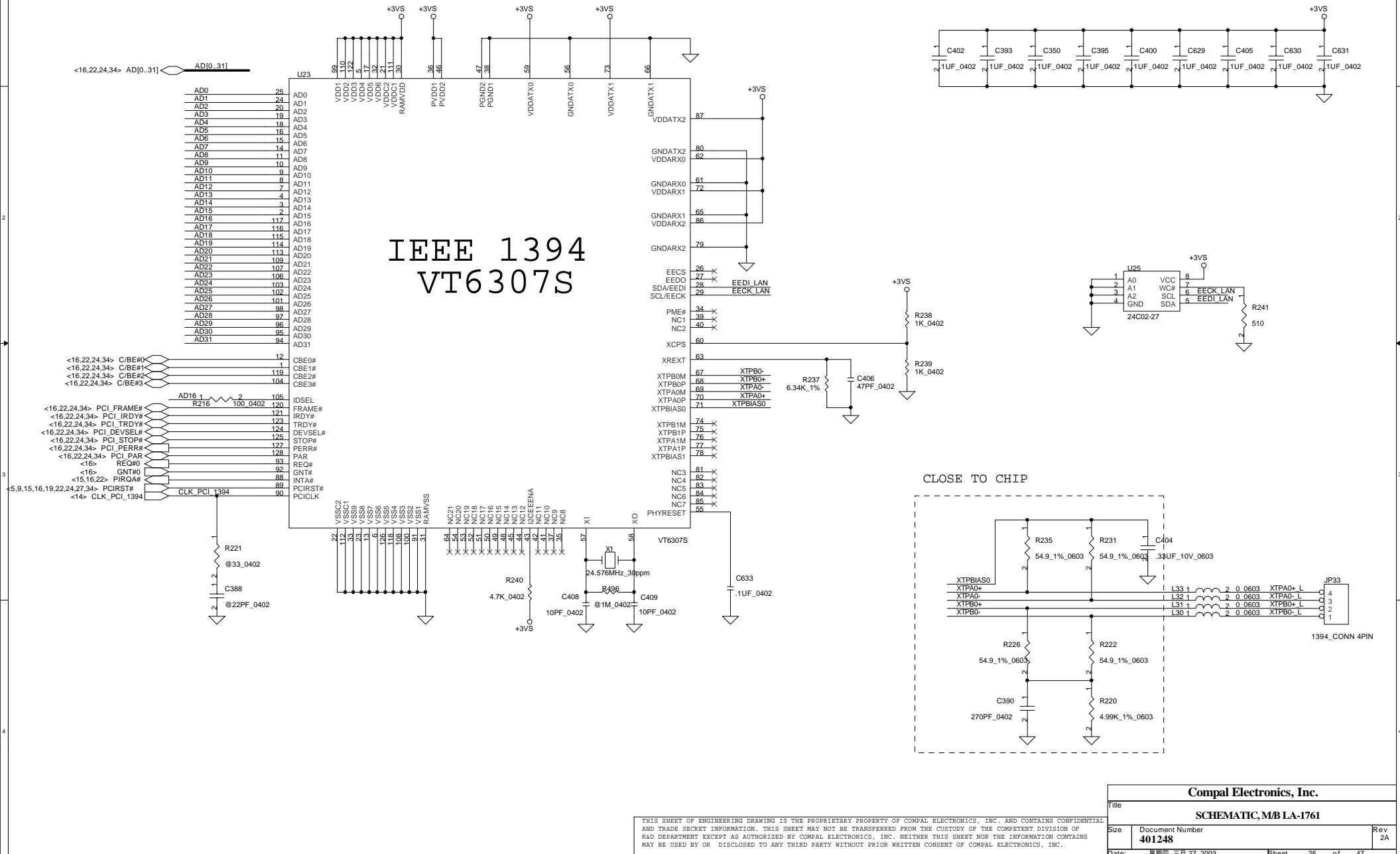
1. LAN\_RD+, LAN\_RD- should be equal length as possible
2. LAN\_TD+, LAN\_TD- should be equal length as possible
3. The Maximum trace length between LAN chip(U22) and Magnetic(U24) is 12cm(4.7")
4. The distance between RJ45(Conn.) and Magnetic(U24) should be as short as possible

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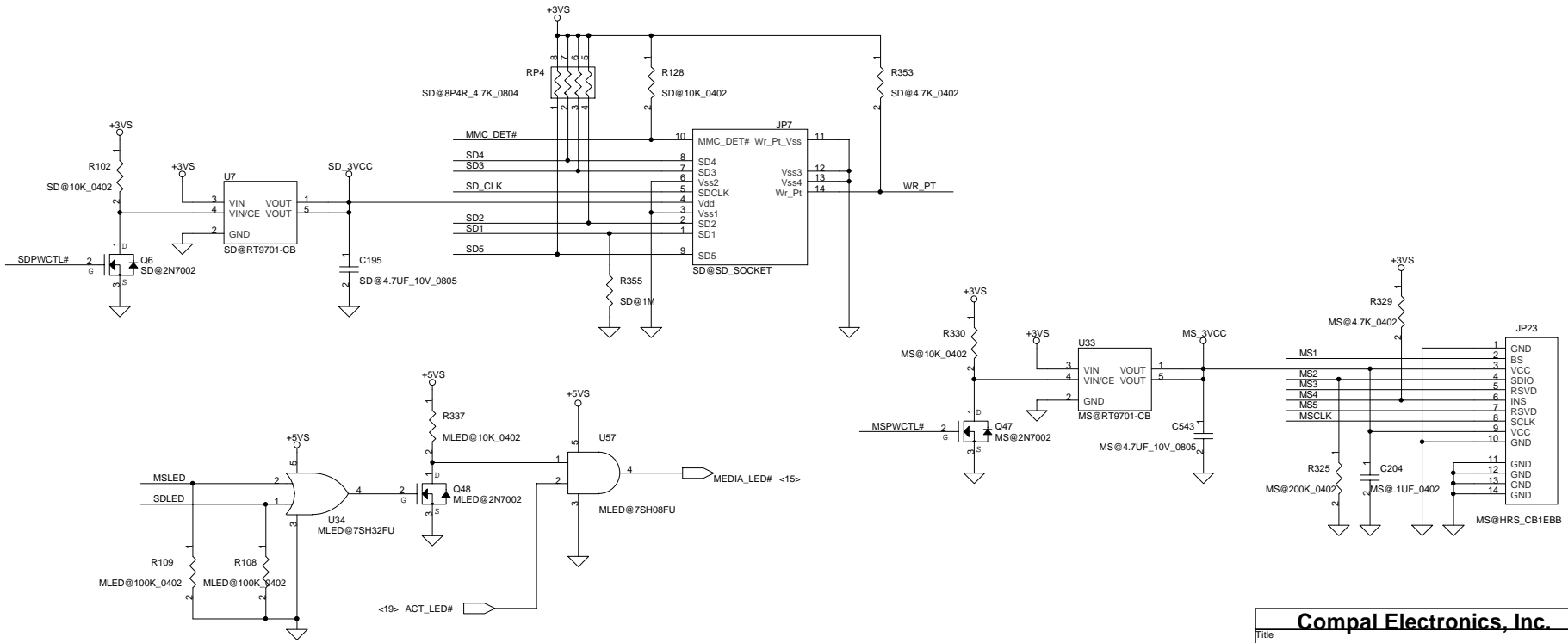
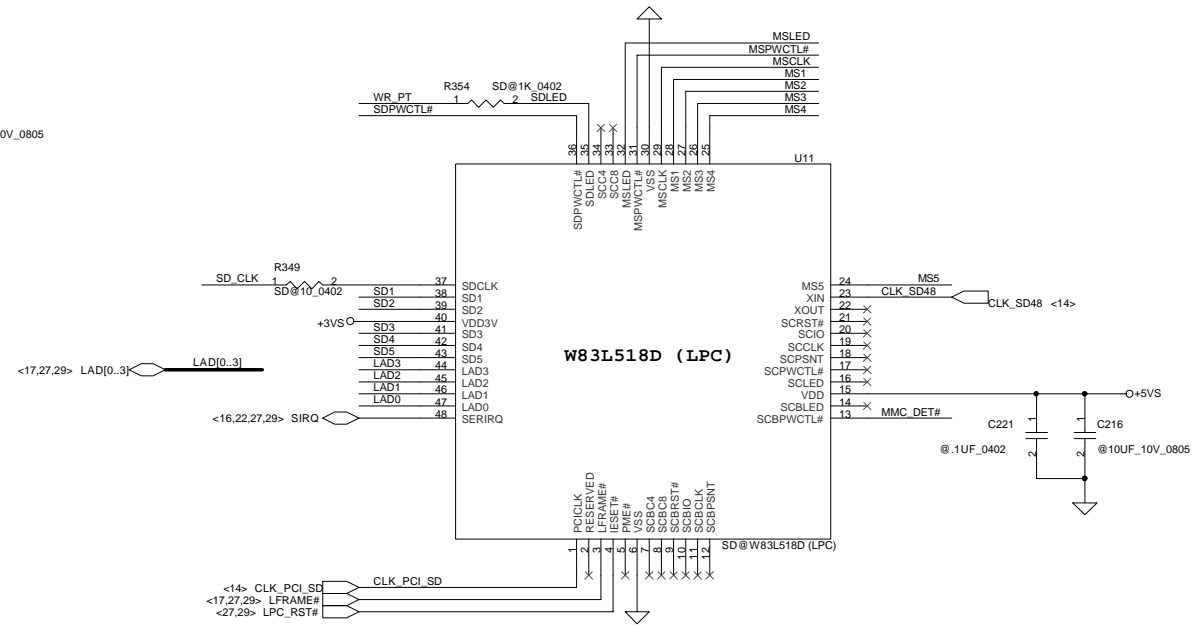
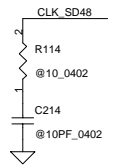
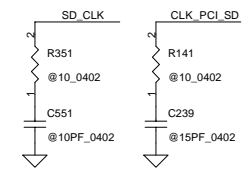
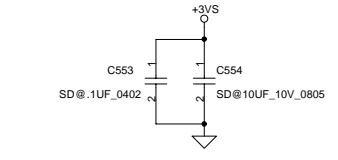


# IEEE 1394 VT6307S



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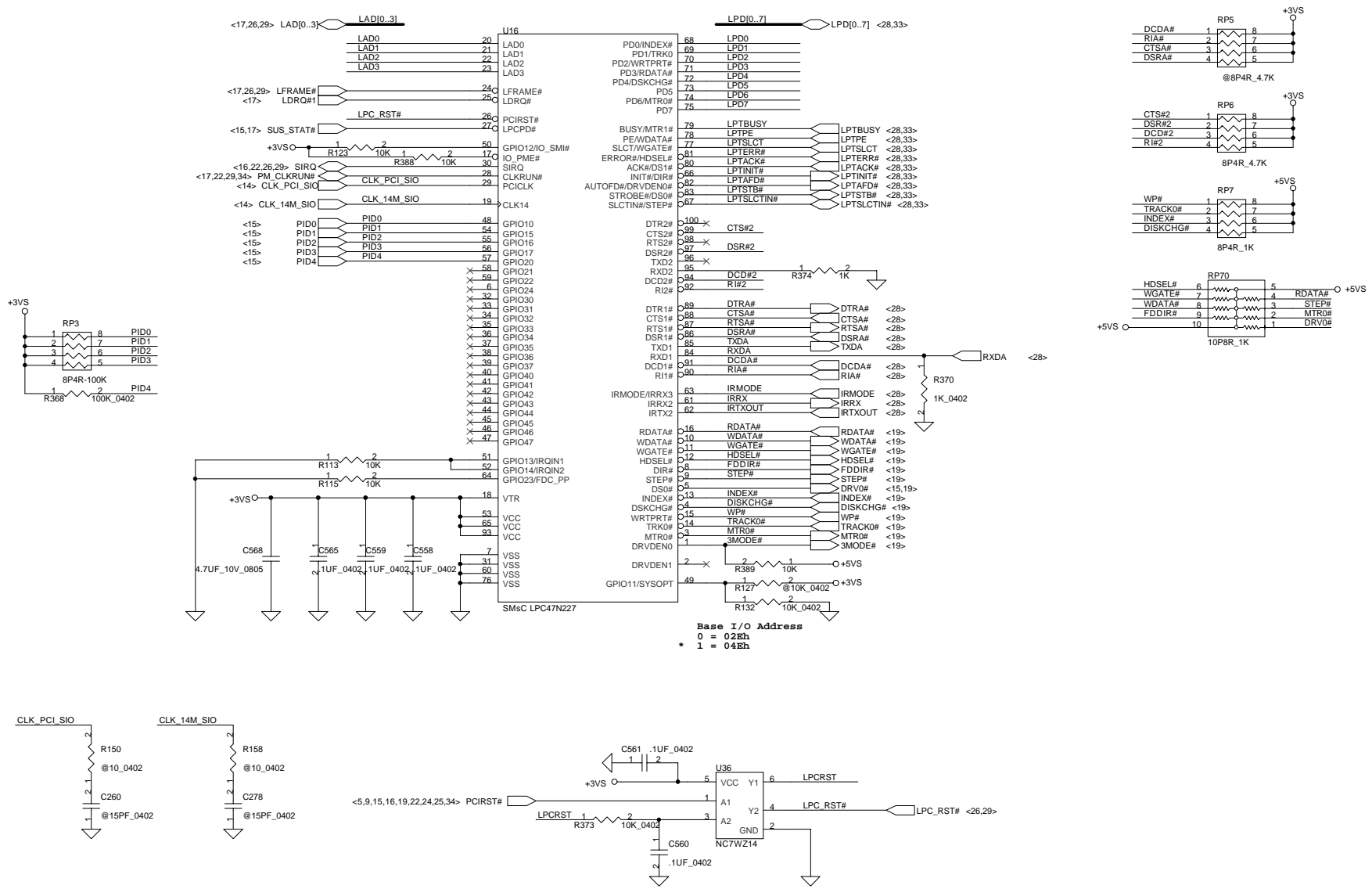
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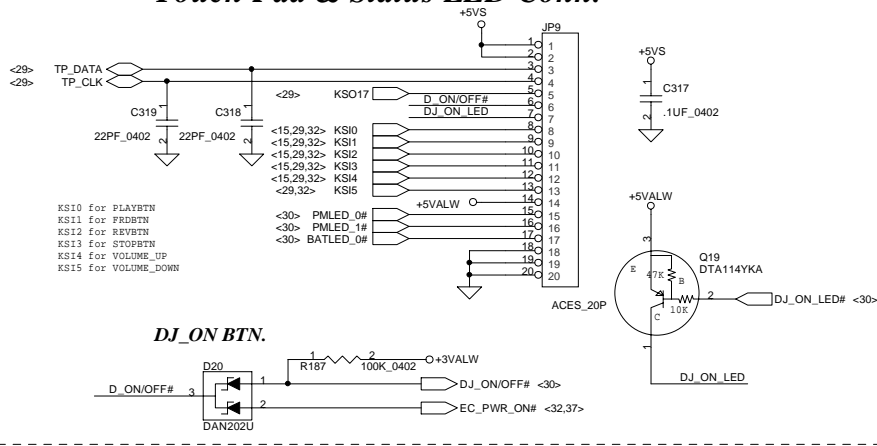
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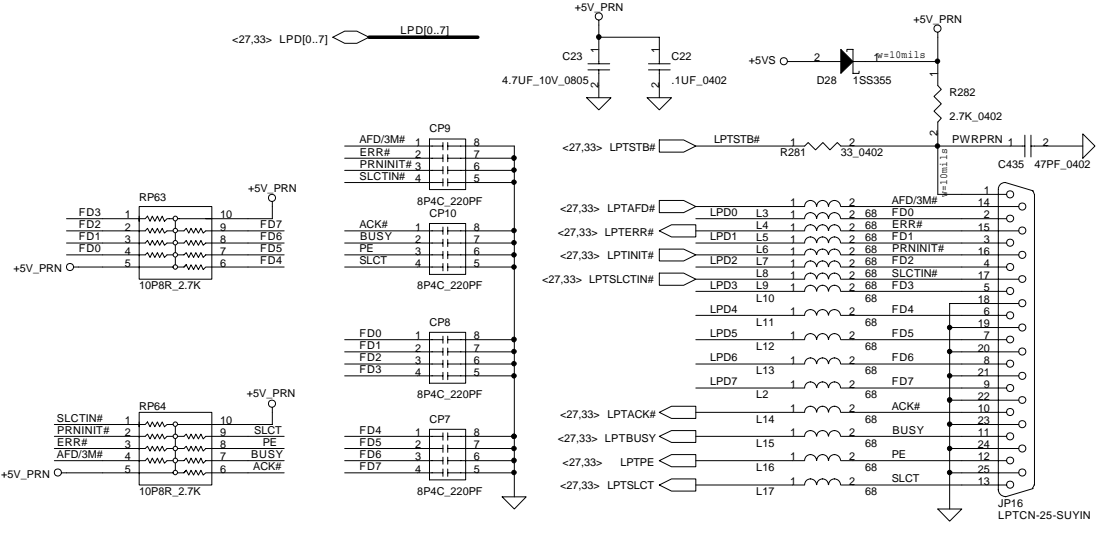
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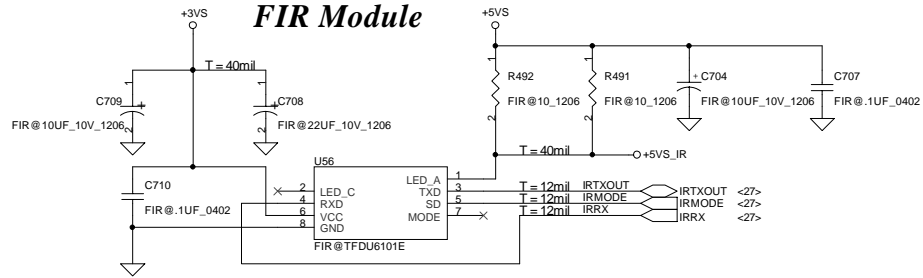
### Touch Pad & Status LED Conn.



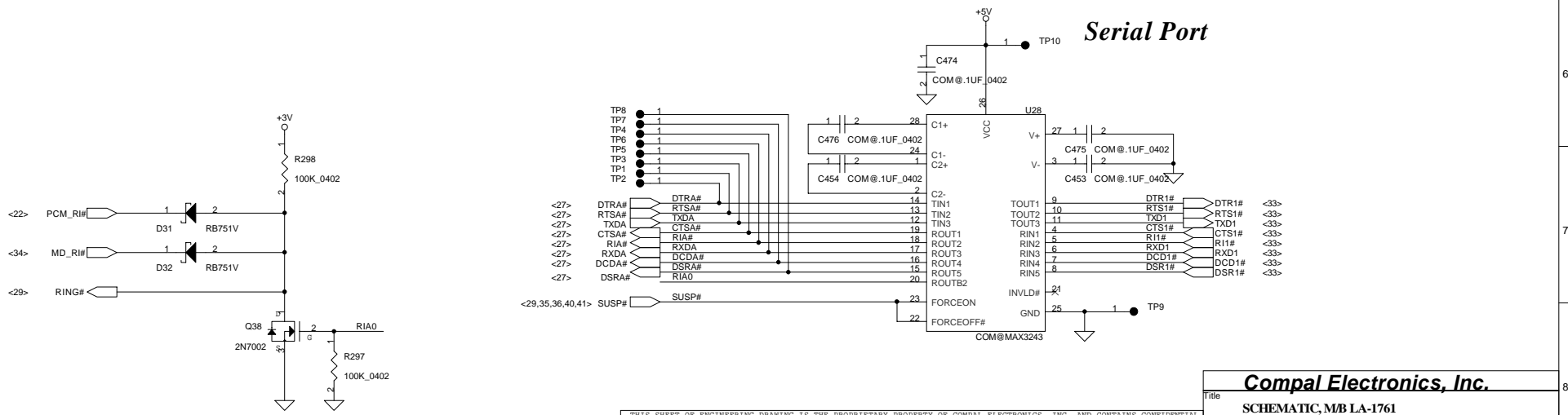
### Parallel Port



### FIR Module

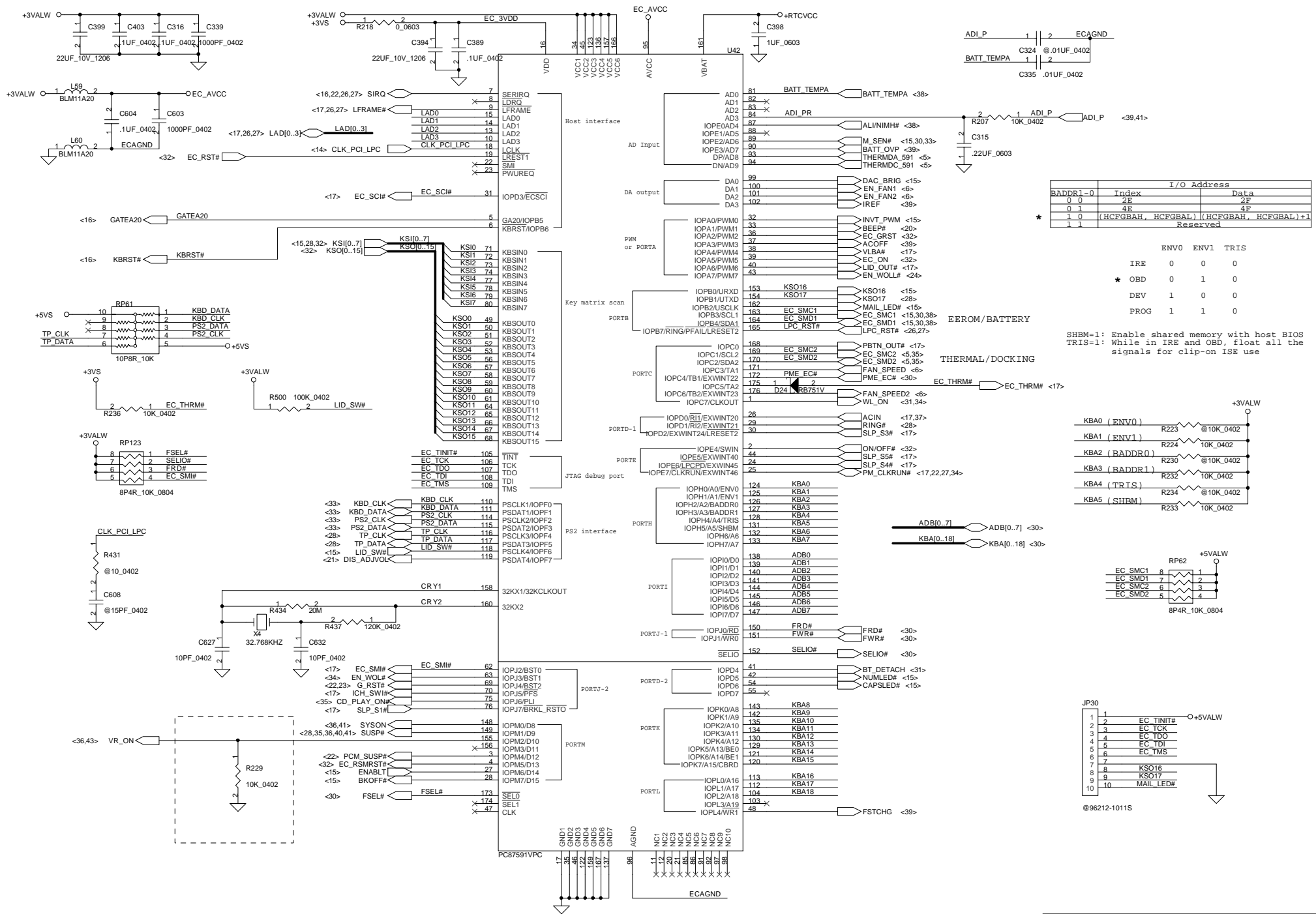


### Serial Port



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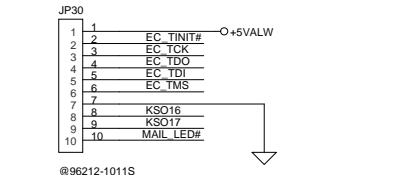
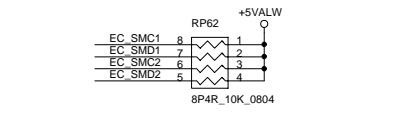
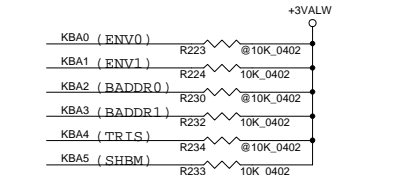
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BADDR1-0	Index	I/O Address	Data
0 0	2E		2F
0 1	4E		4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGGBAH, HCFGGBAL)+1	
1 1		Reserved	

	ENV0	ENV1	TRIS
IRE	0	0	0
OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM=1: Enable shared memory with host BIOS  
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use



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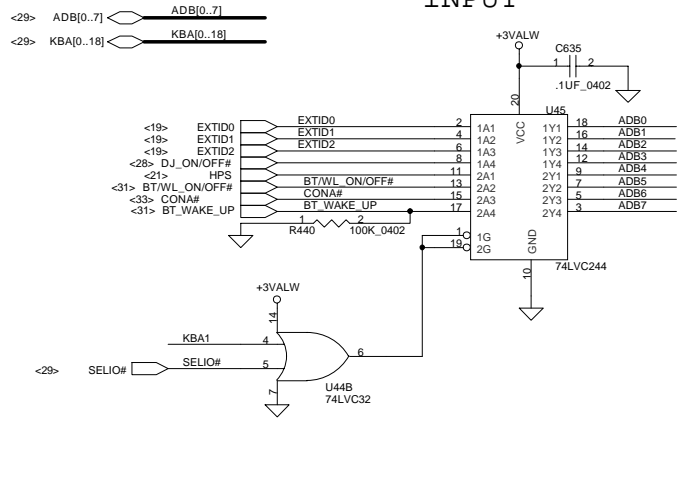
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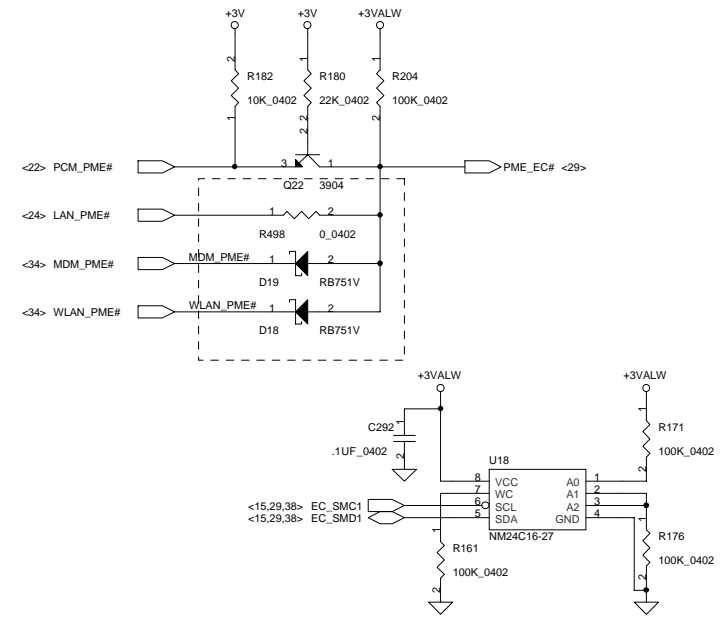
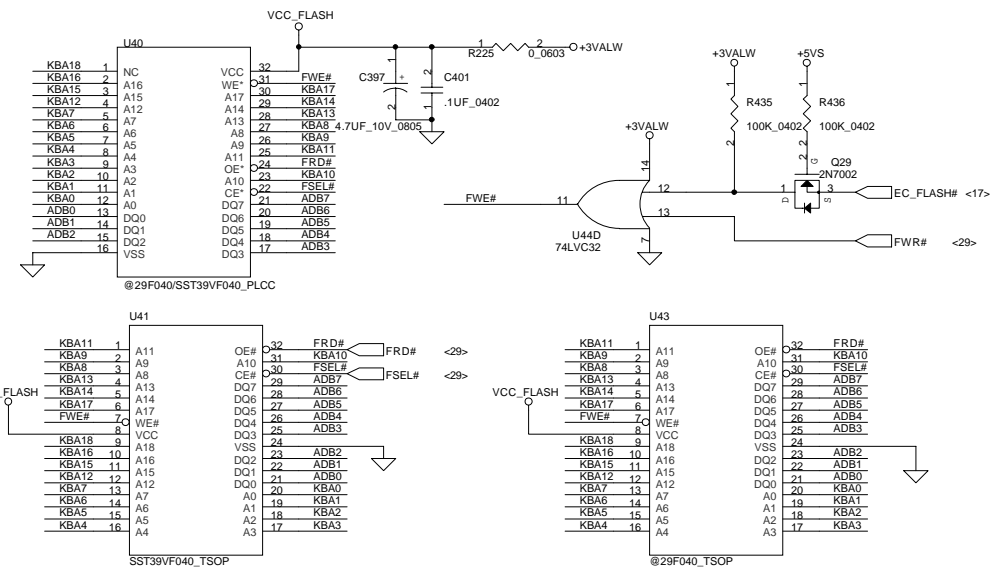
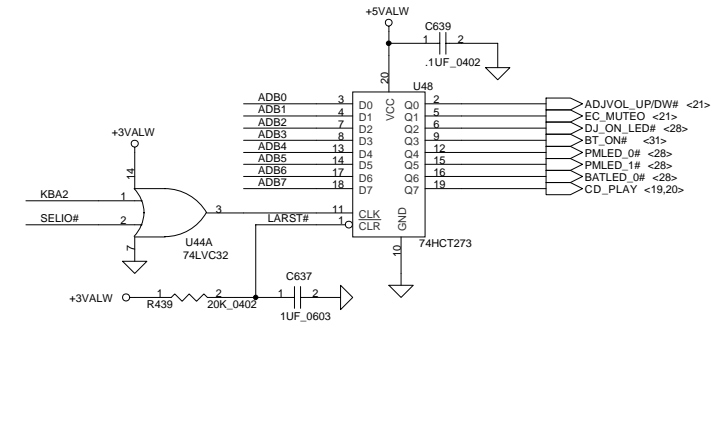
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# INPUT



# OUTPUT



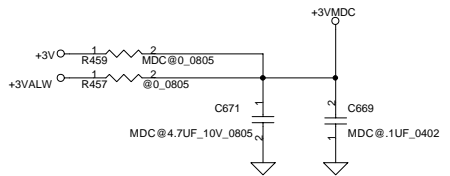
TSOP 8x14

TSOP 8x20

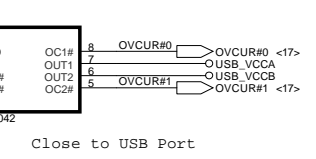
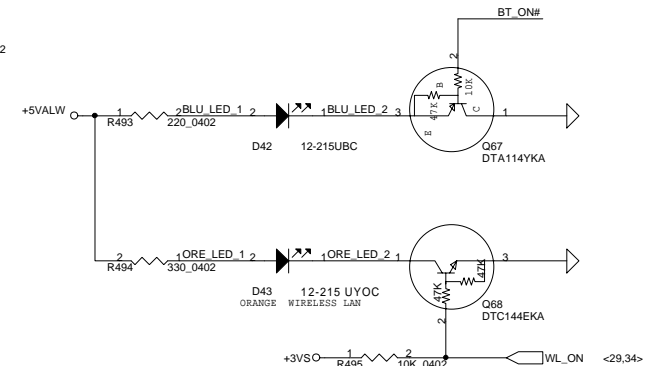
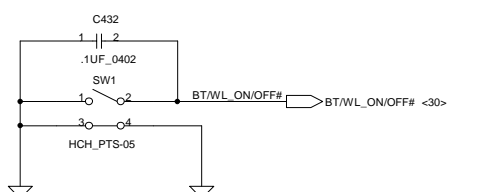
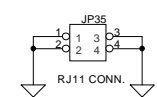
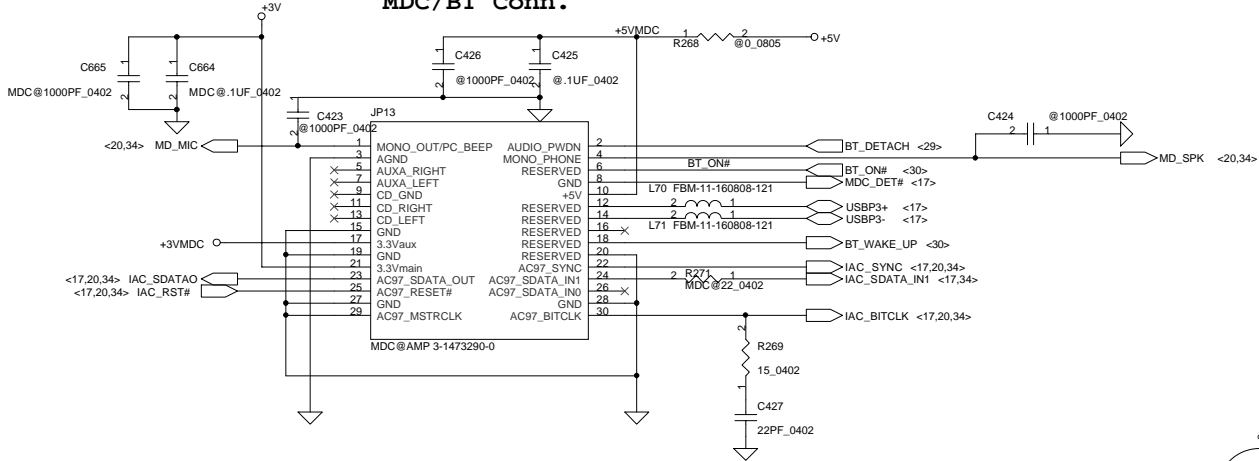
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**MDC Note**  
 Pin 1 is NC for Pctel and connexant MDC modem  
 Pin 2 is NC for Pctel and connexant MDC modem

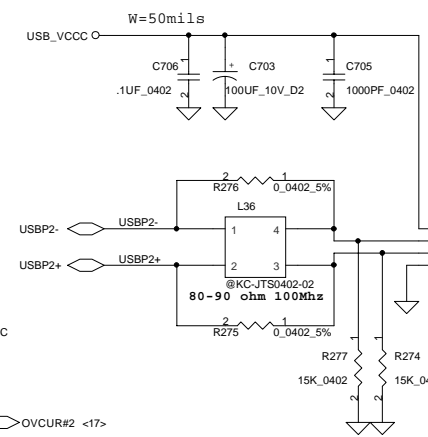


**MDC/BT Conn.**

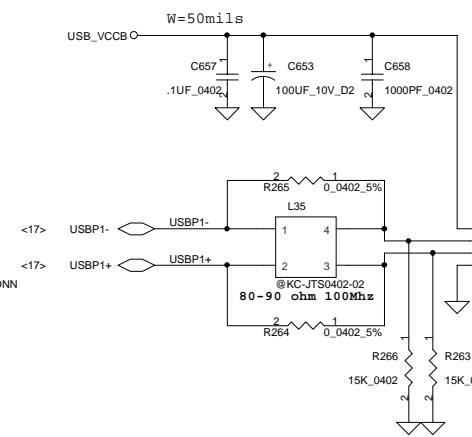


Close to USB Port

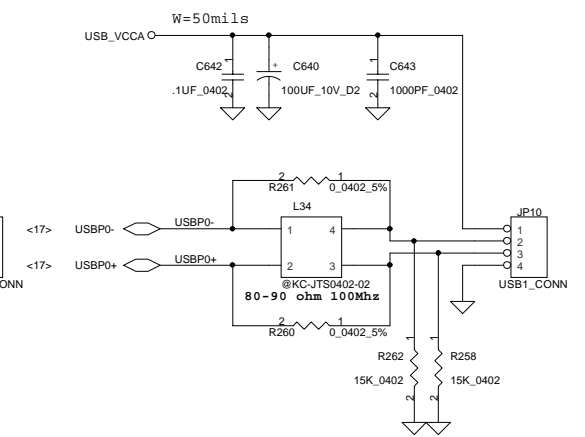
**USB CONNECTOR 3**



**USB CONNECTOR 2**



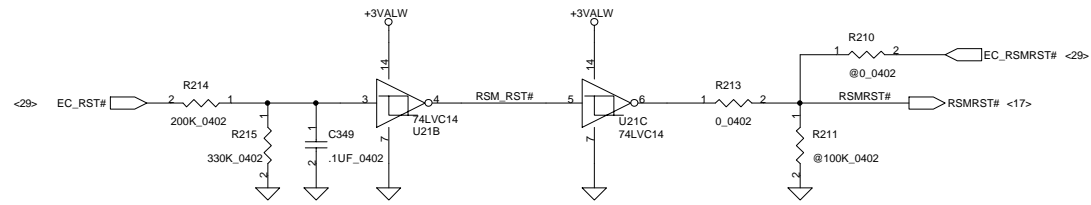
**USB CONNECTOR 1**



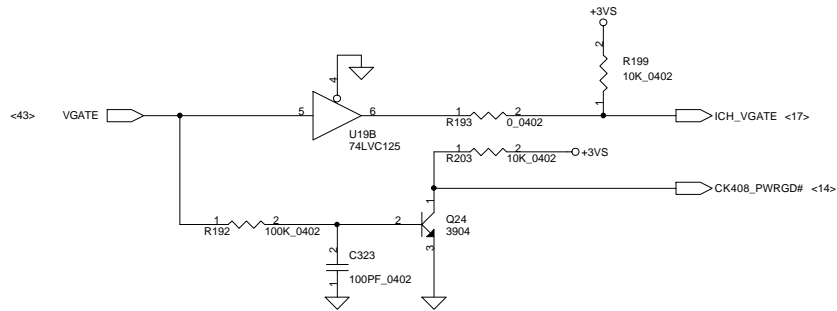
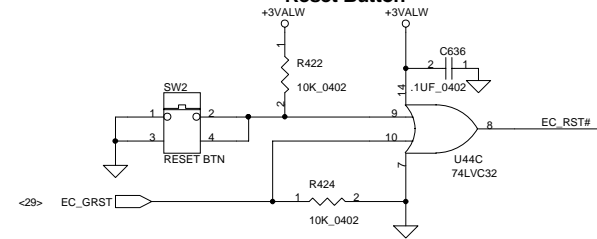
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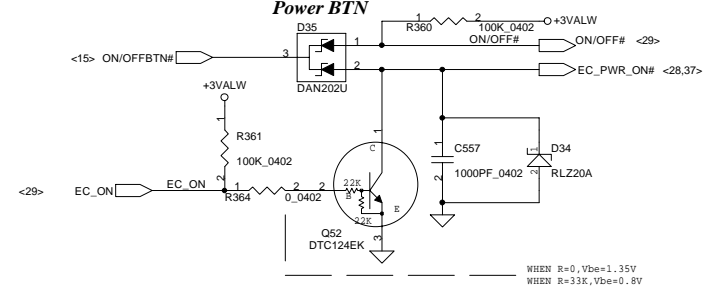
**Power ON Circuit**



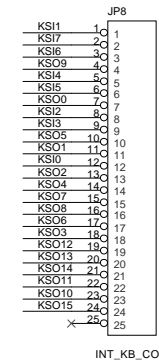
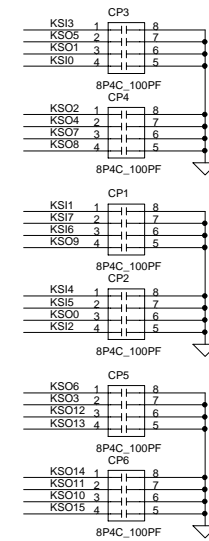
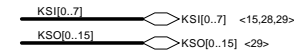
**Reset Button**



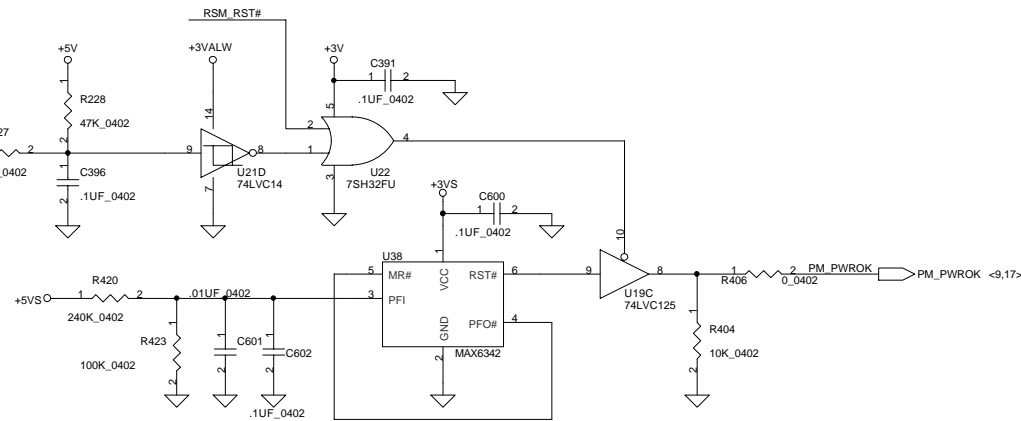
**Power BTN**



**INT\_KBD CONN.**



DT : INSTALL



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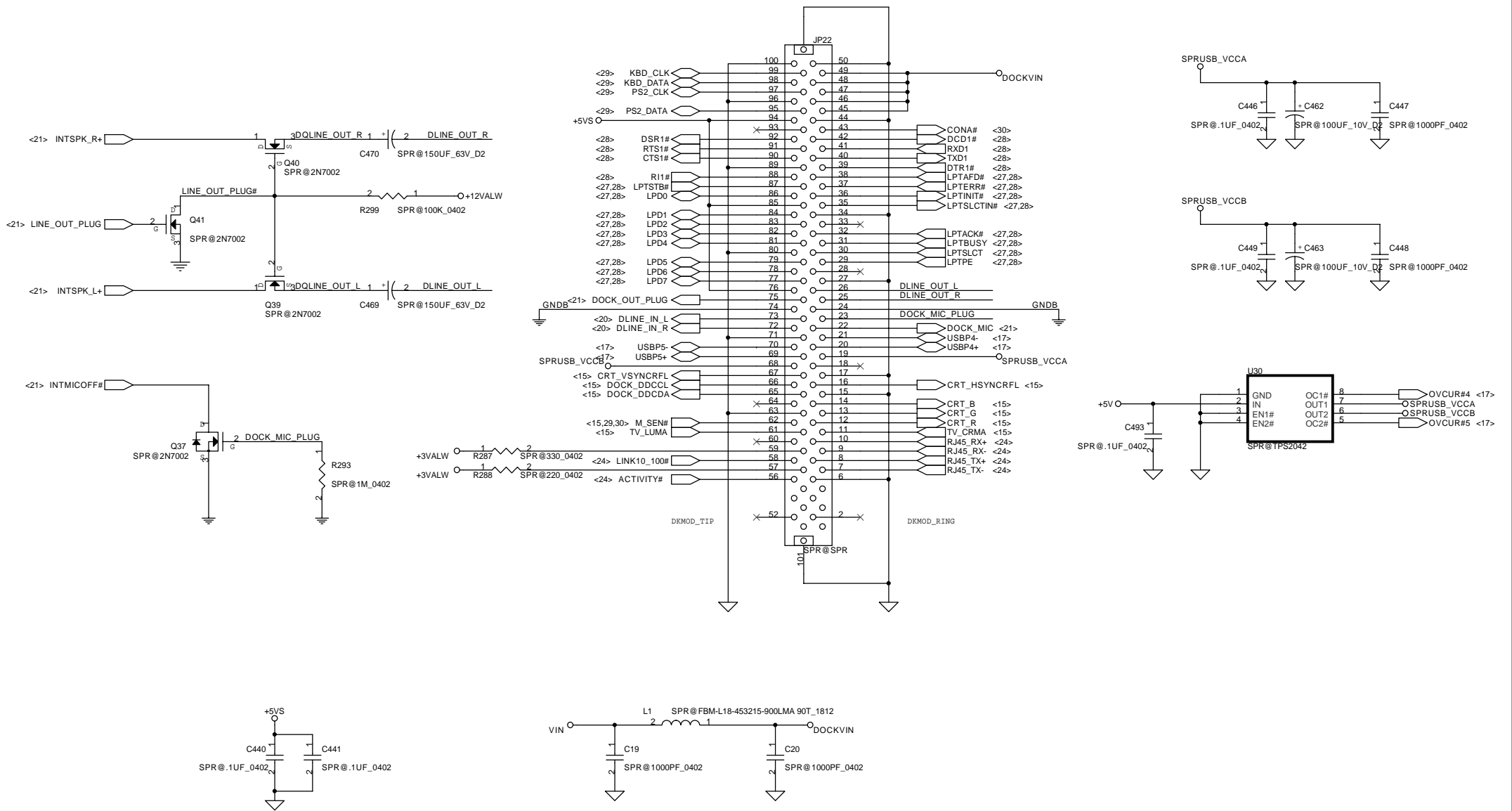
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# SPR 102 PIN

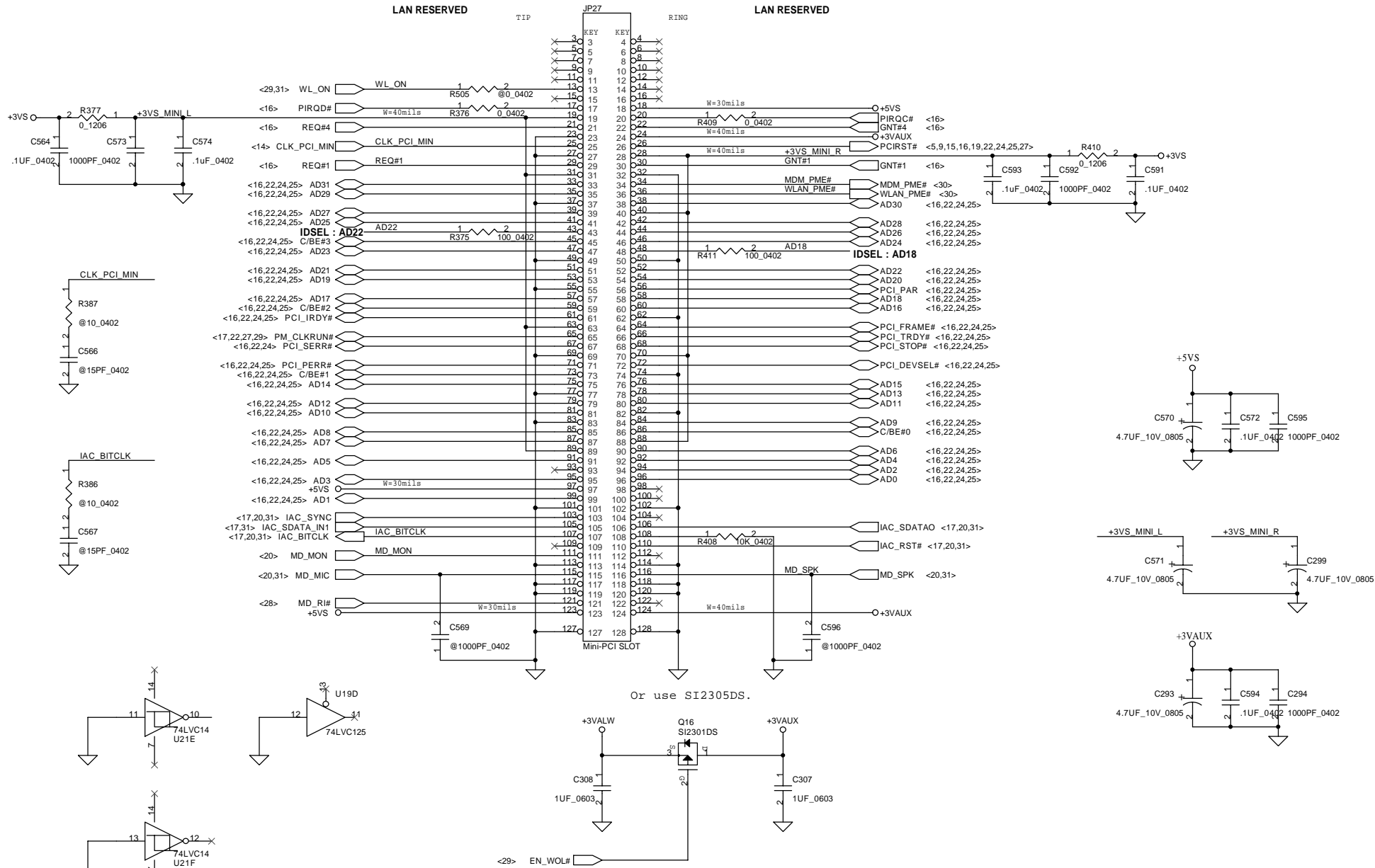


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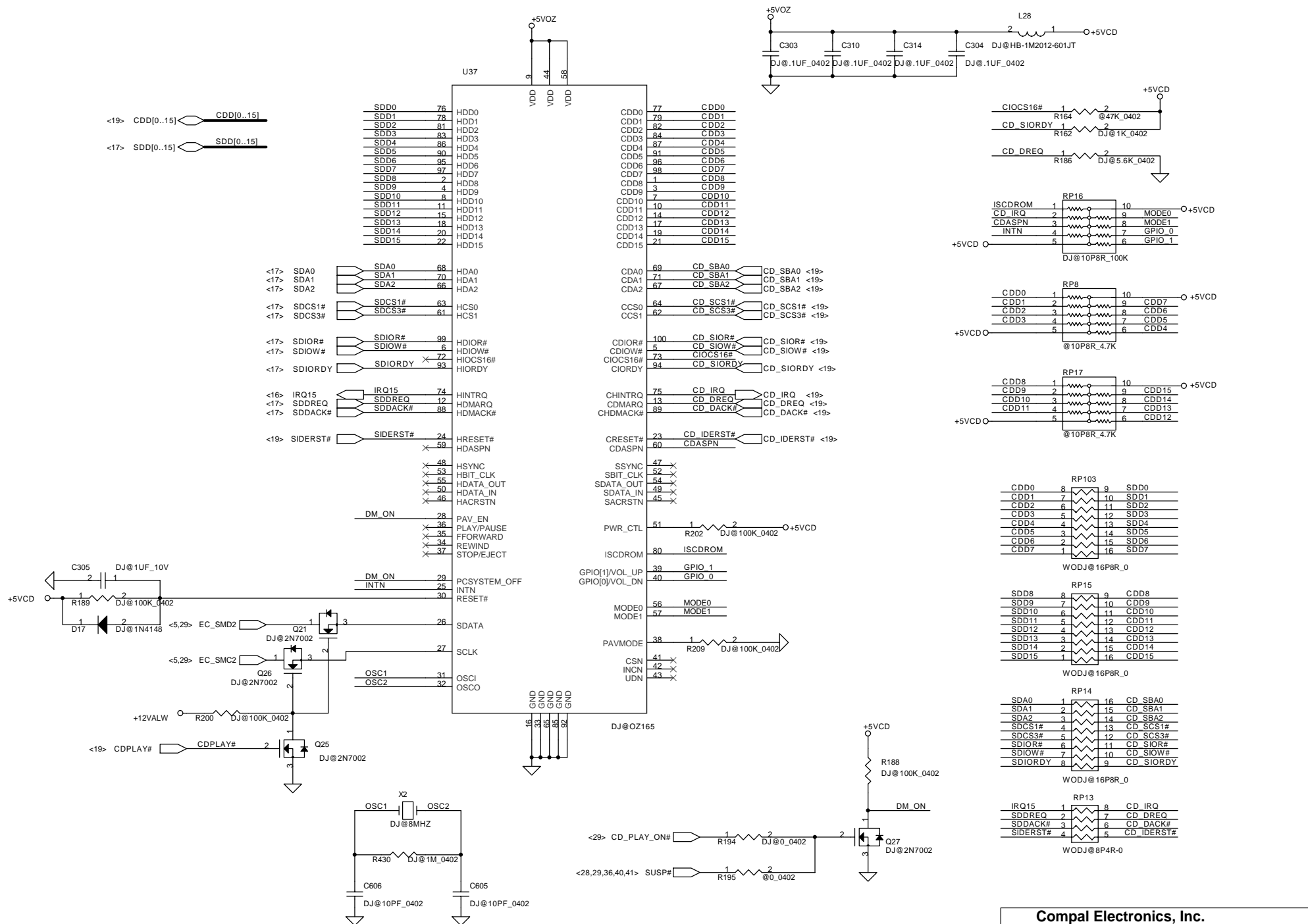
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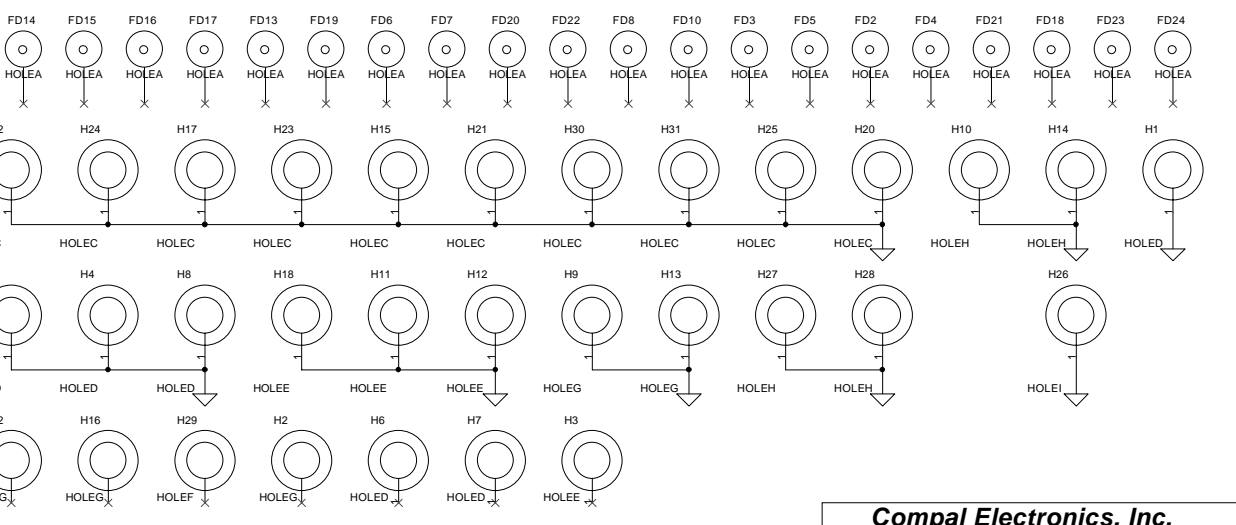
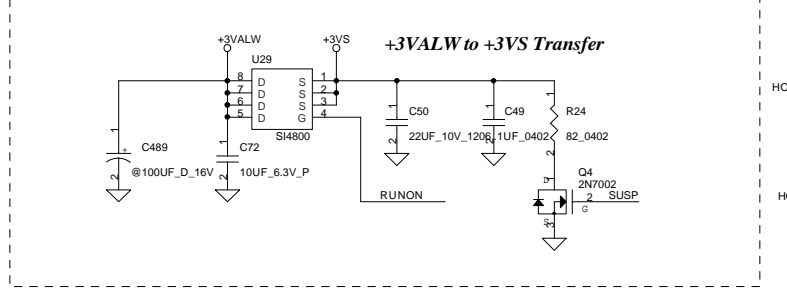
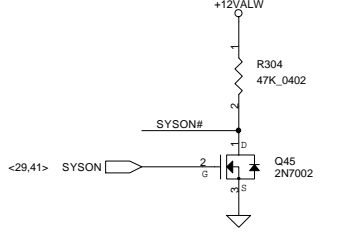
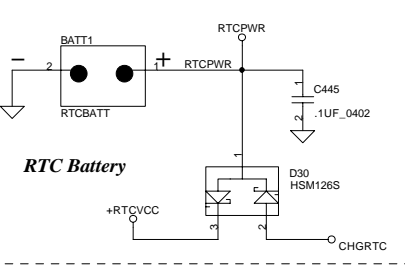
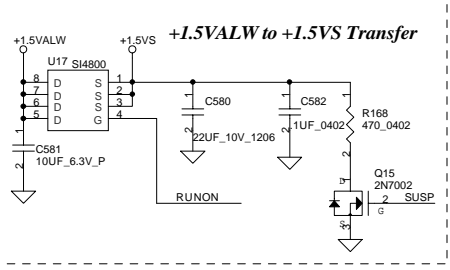
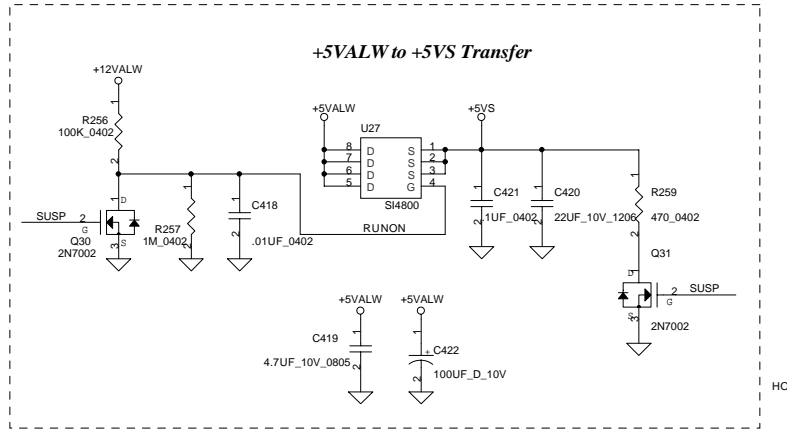
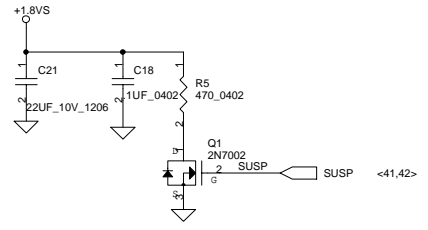
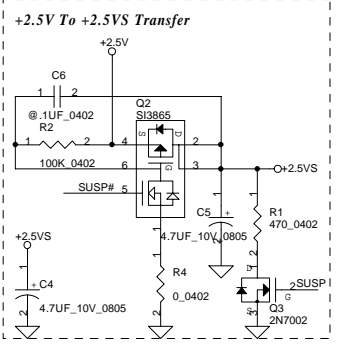
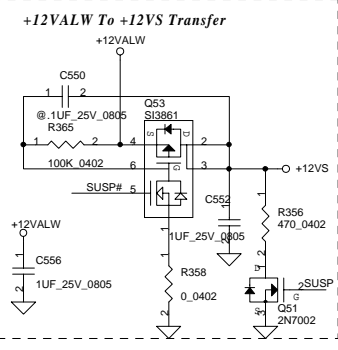
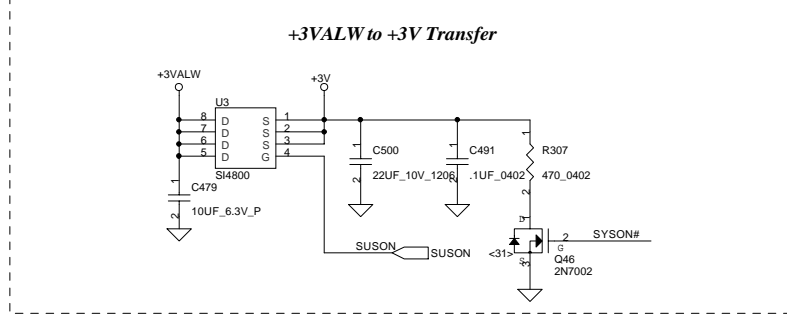
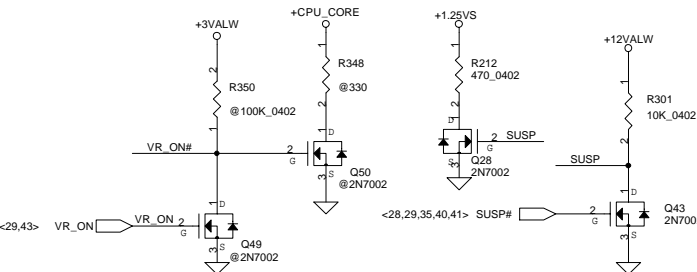
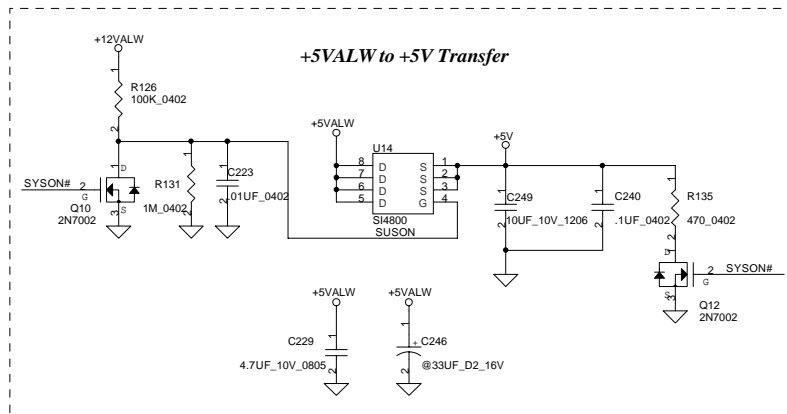


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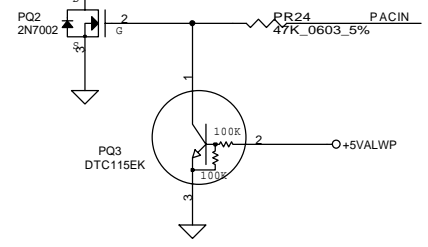
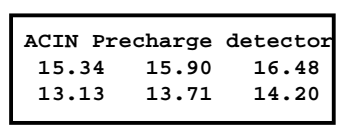
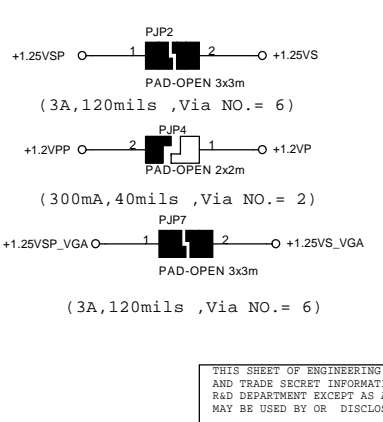
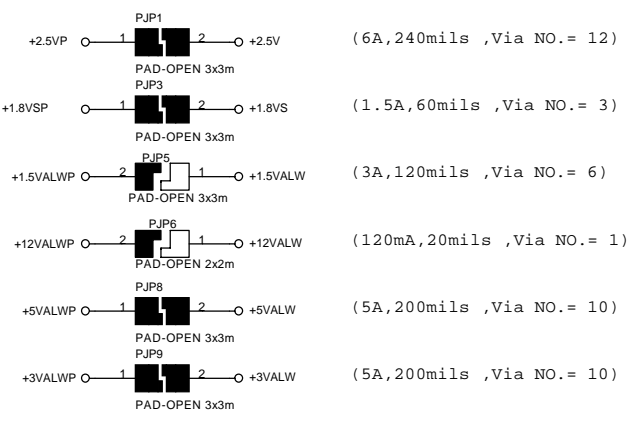
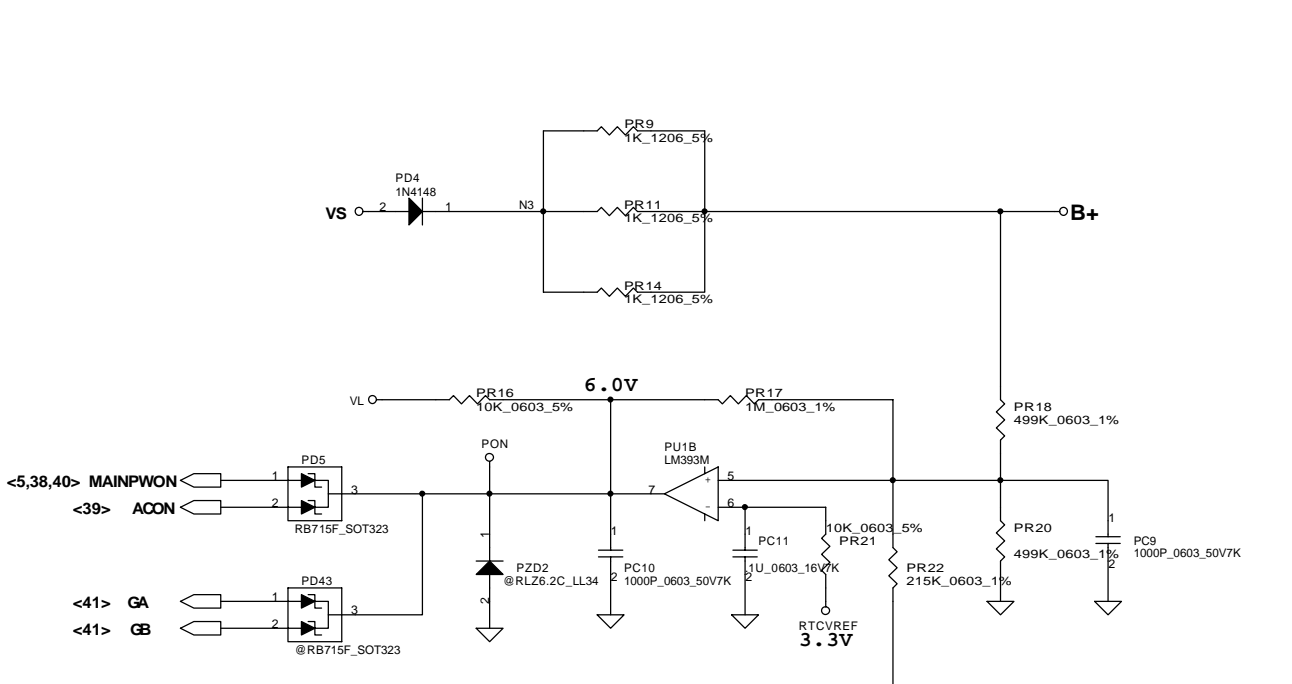
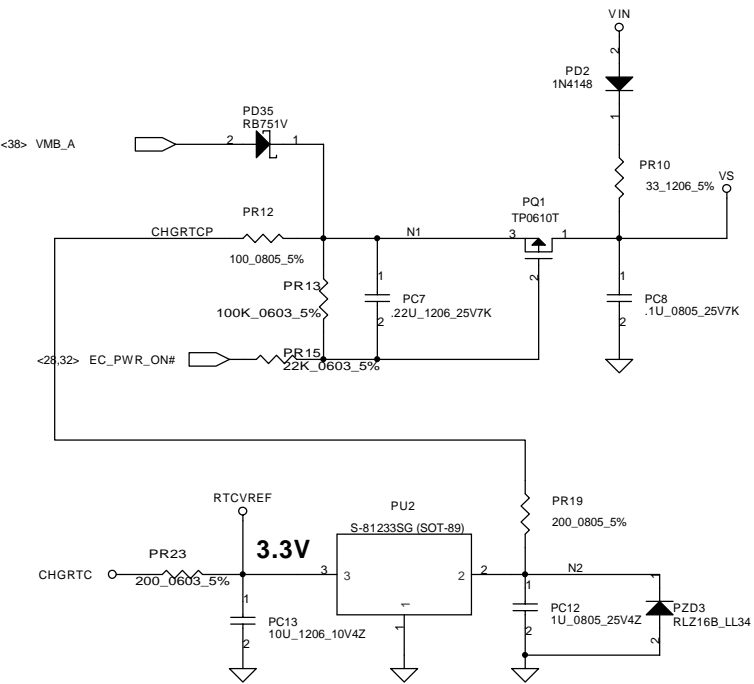
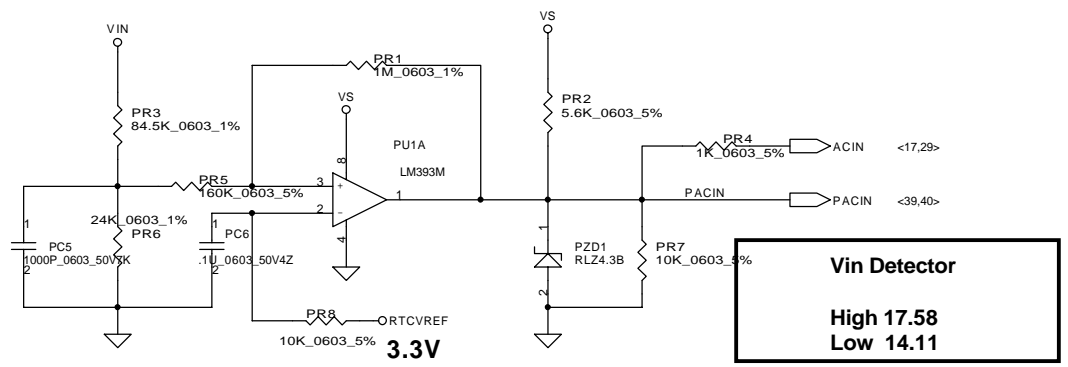
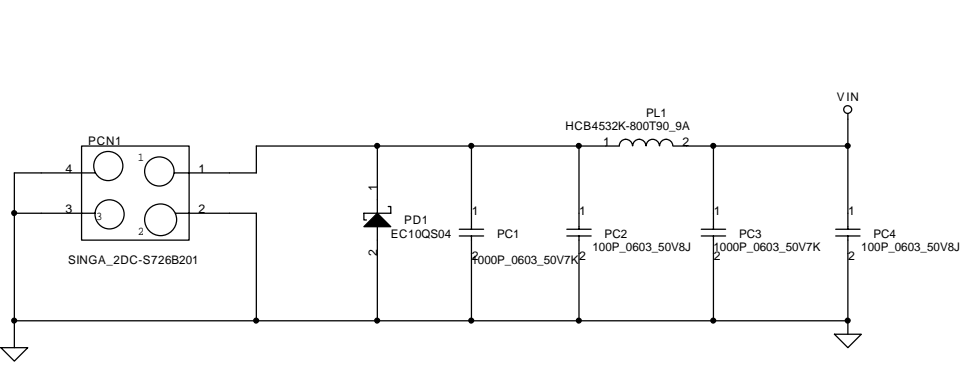


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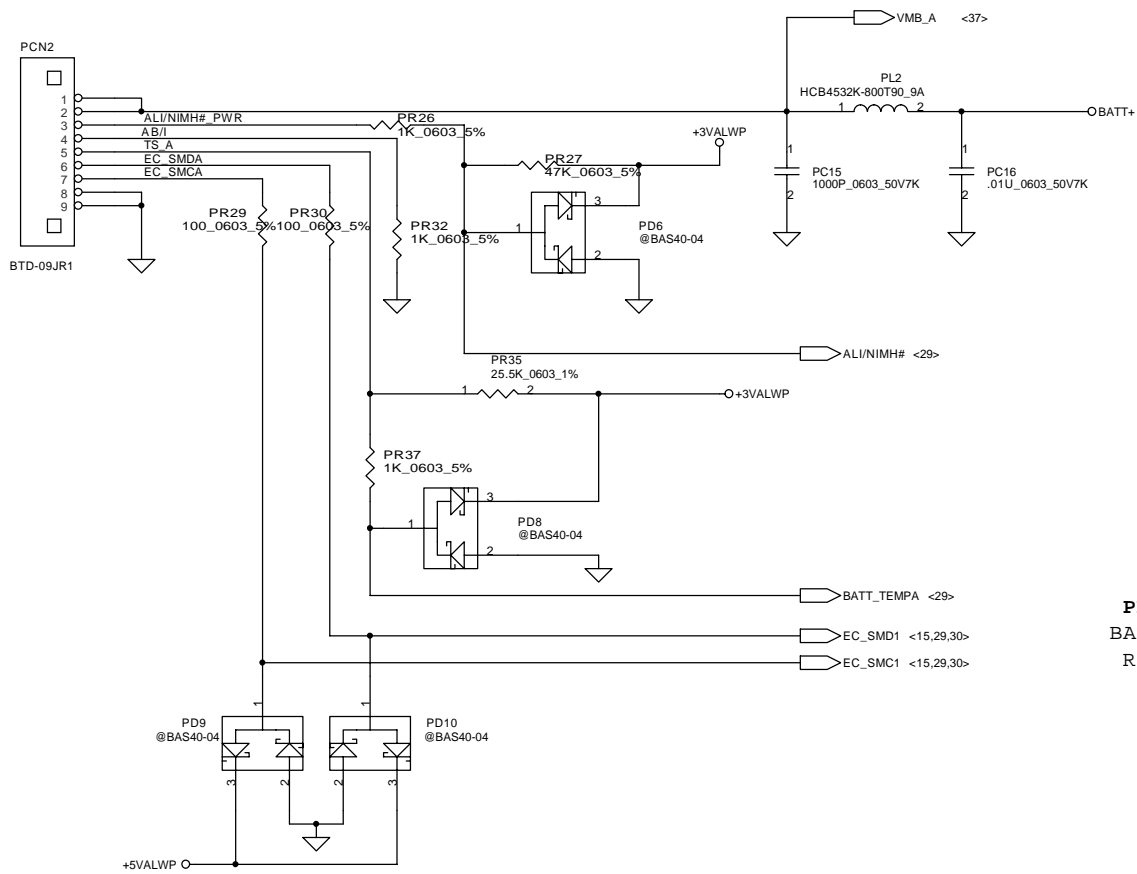


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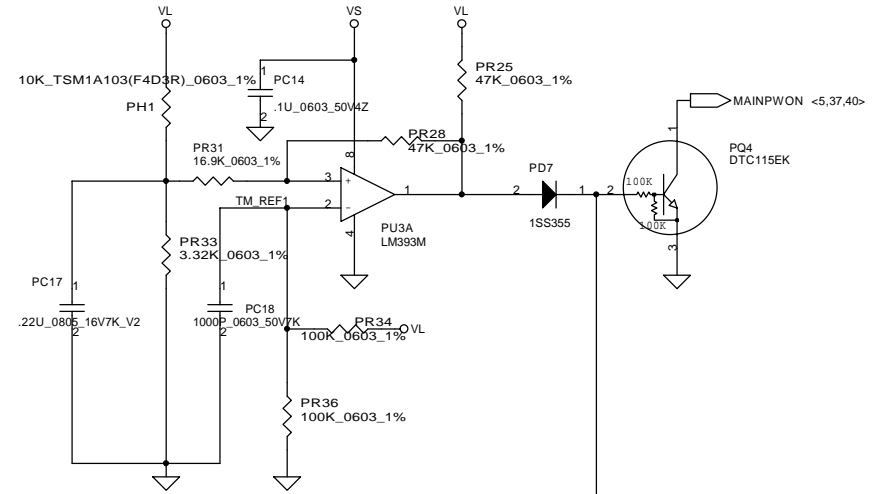
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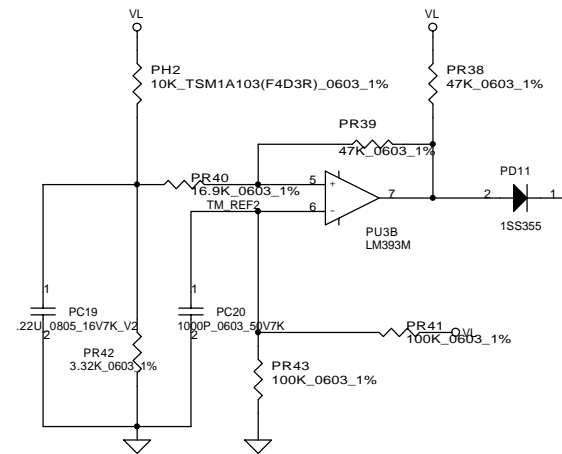
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**PH1 under CPU bottom side :**  
 CPU thermal protection at 84 degree C  
 Recovery at 45 degree C

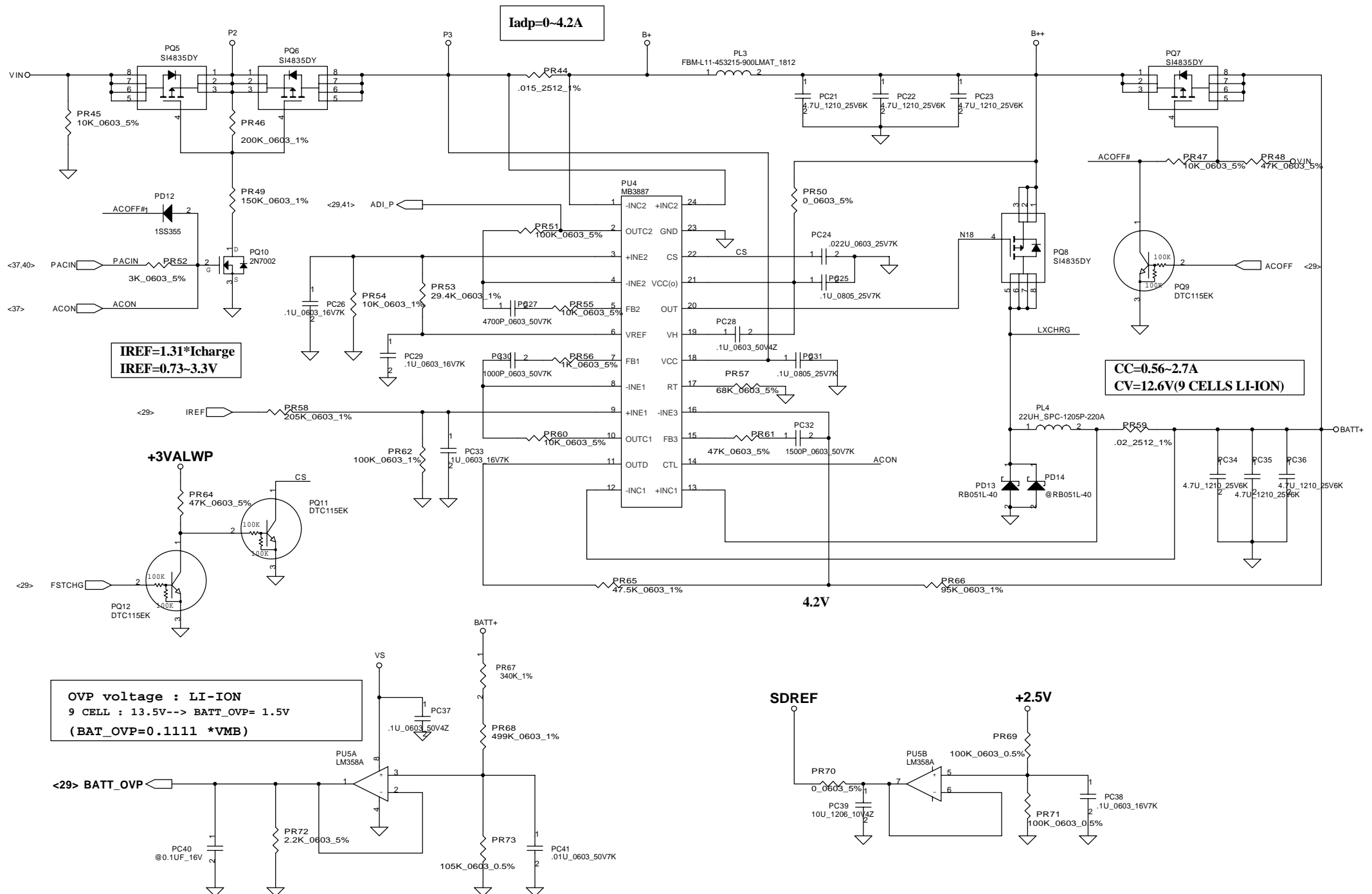


**PH2 near main Battery CONN :**  
 BAT. thermal protection at 84 degree C  
 Recovery at 45 degree C



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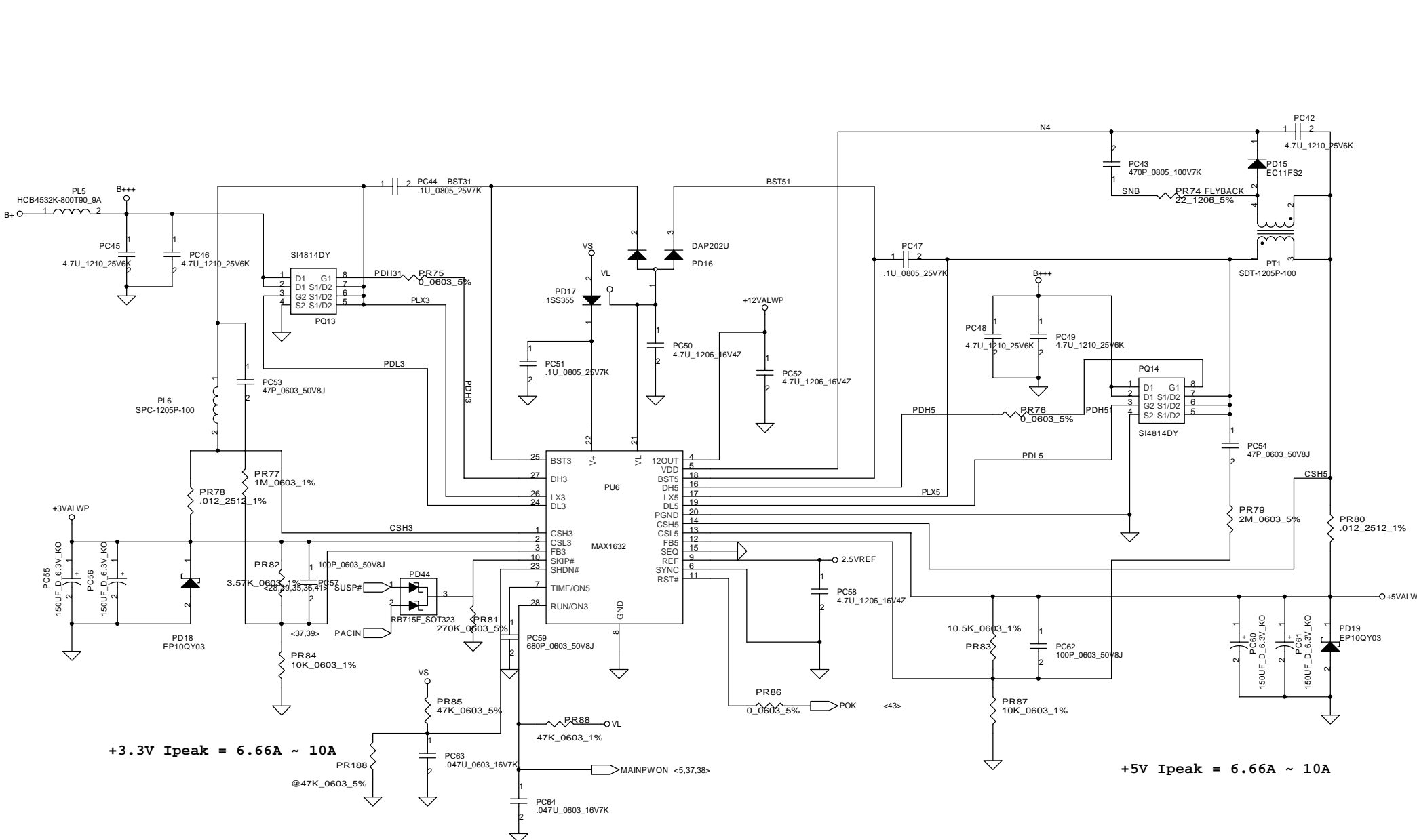
**IREF=1.31\*Icharge**  
**IREF=0.73~3.3V**

**CC=0.56~2.7A**  
**CV=12.6V(9 CELLS LI-ION)**

**OVP voltage : LI-ION**  
**9 CELL : 13.5V--> BATT\_OVP= 1.5V**  
**(BAT\_OVP=0.1111 \*VMB)**

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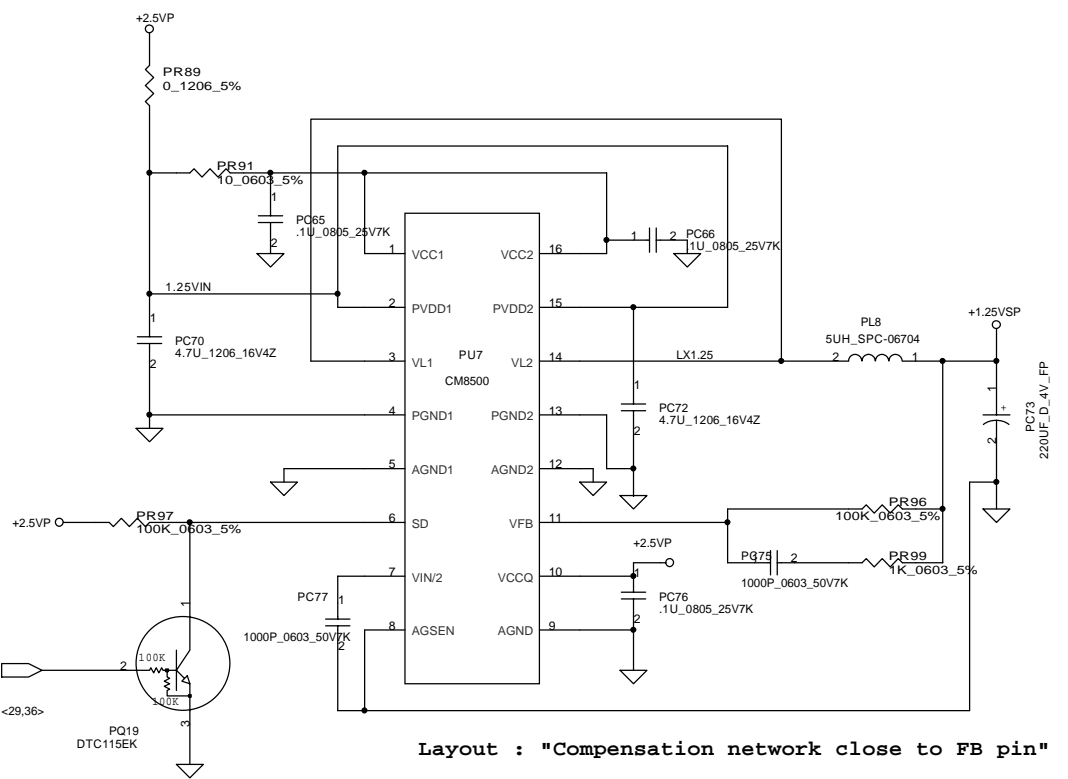
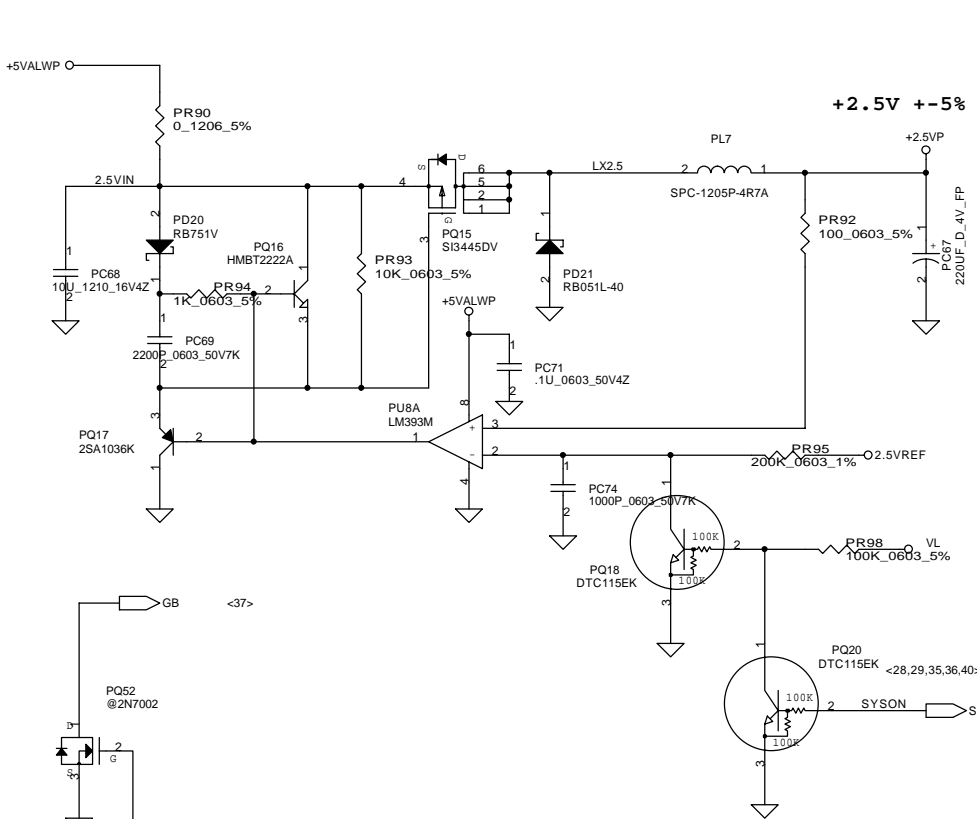
**+3.3V Ipeak = 6.66A ~ 10A**

**+5V Ipeak = 6.66A ~ 10A**

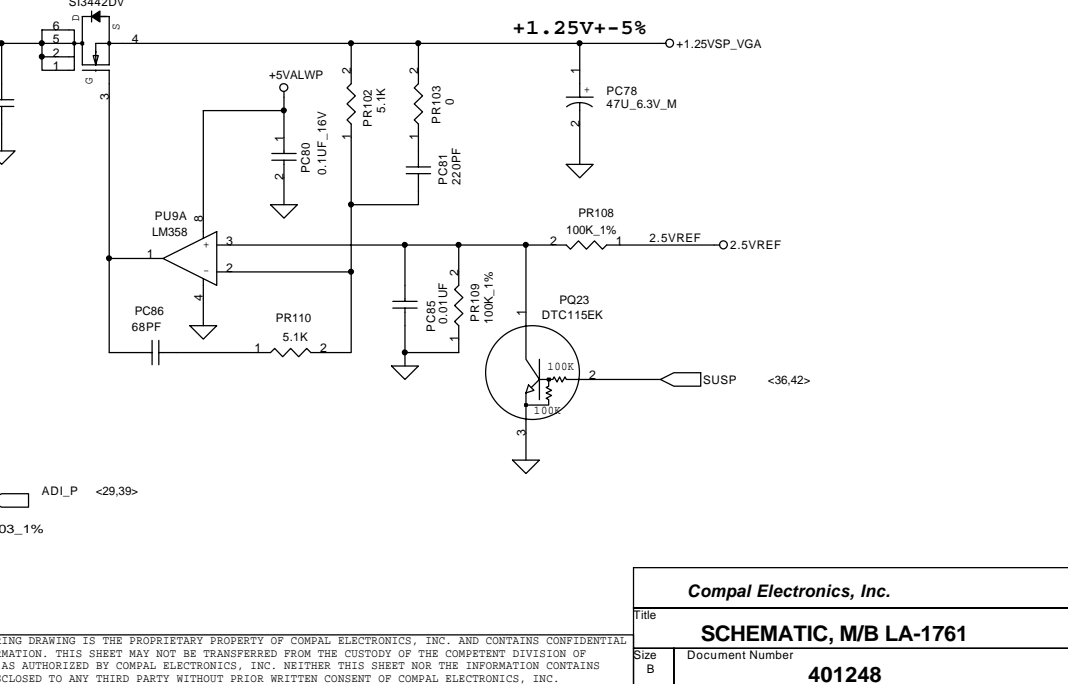
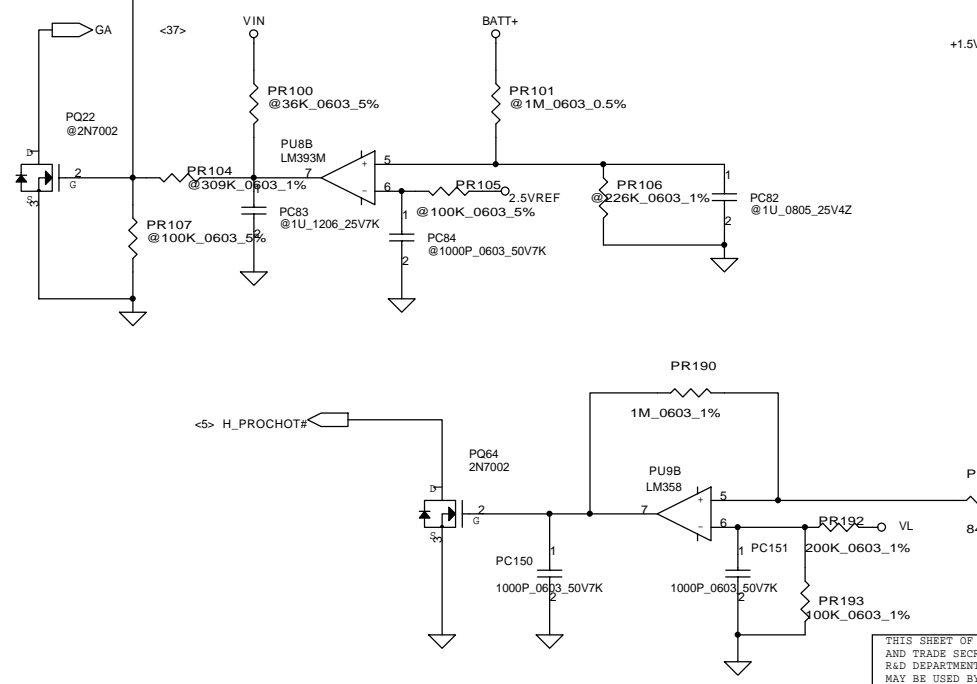
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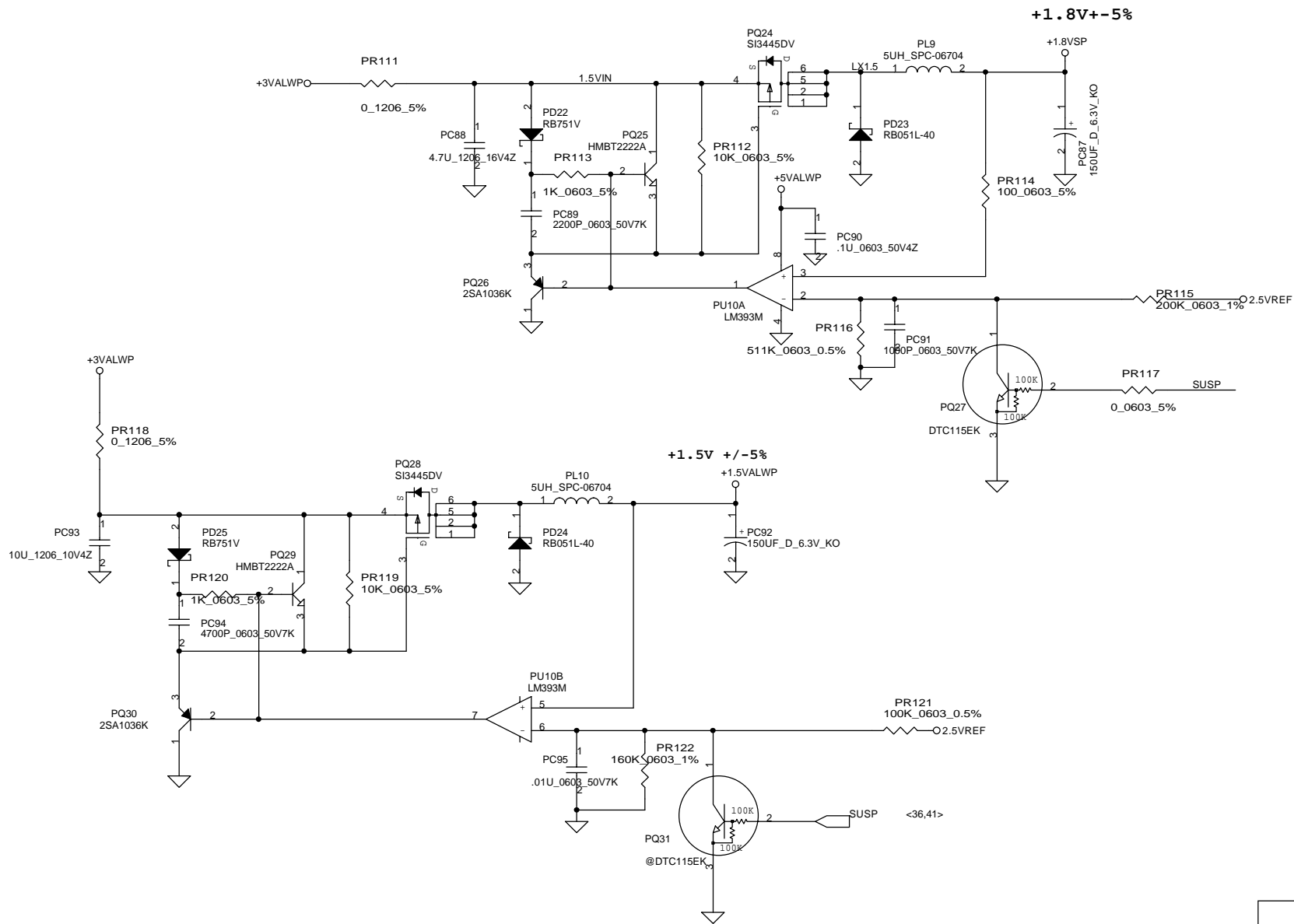


Layout : "Compensation network close to FB pin"



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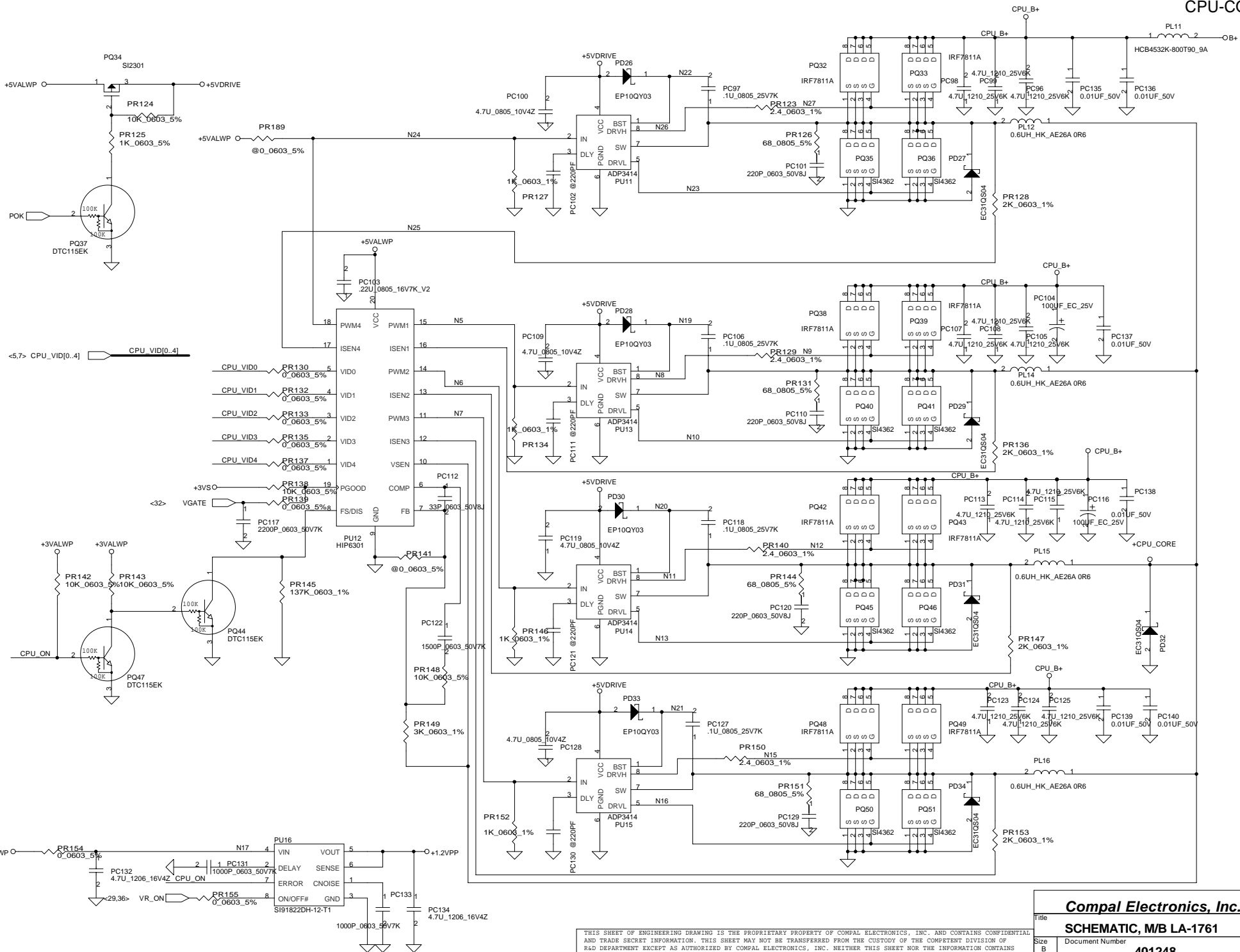
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# CPU-CORE



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*Version change list (P.I.R. List)*

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B Ver.
1		improve CPU core voltage drop	43	change PR149 from 3.9K_0603_1% to 3K_0603_1%	0.2
2		delete second battery component	38,44	delete PC142 , add PC16	0.2

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Delete useless components	5 24 17	Delete Q7, Q8, Q11, R104, R116 and R117 Delete C43 and C48 Delete D39	0.2
2		Change BIOS ROM type	30	Delete U40, Add U41	0.2
3		Separate CD-ROM LED from Media LED	19	Delete U26 and C417, ADD R247	0.2
4		Delete second battery circuit	29	Delete C336; Pin 55, 82, 88, 156 of U42 change to be NC pin	0.3
5		For WNC wireless lan card only	34	Reserve R505 (un-populate)	0.3
6		Solve USB fail issue	17	Add R506	2.0

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