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PBL80 Project

LA-7441P REV 0.1 Schematic

Intel Sandy Bridge/Cougar Point

N12P-GV/GS-Optimus Only

2011-01-21 Rev. 0.1

Security Classification	Compal Secret Data		
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Title: Cover Page

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

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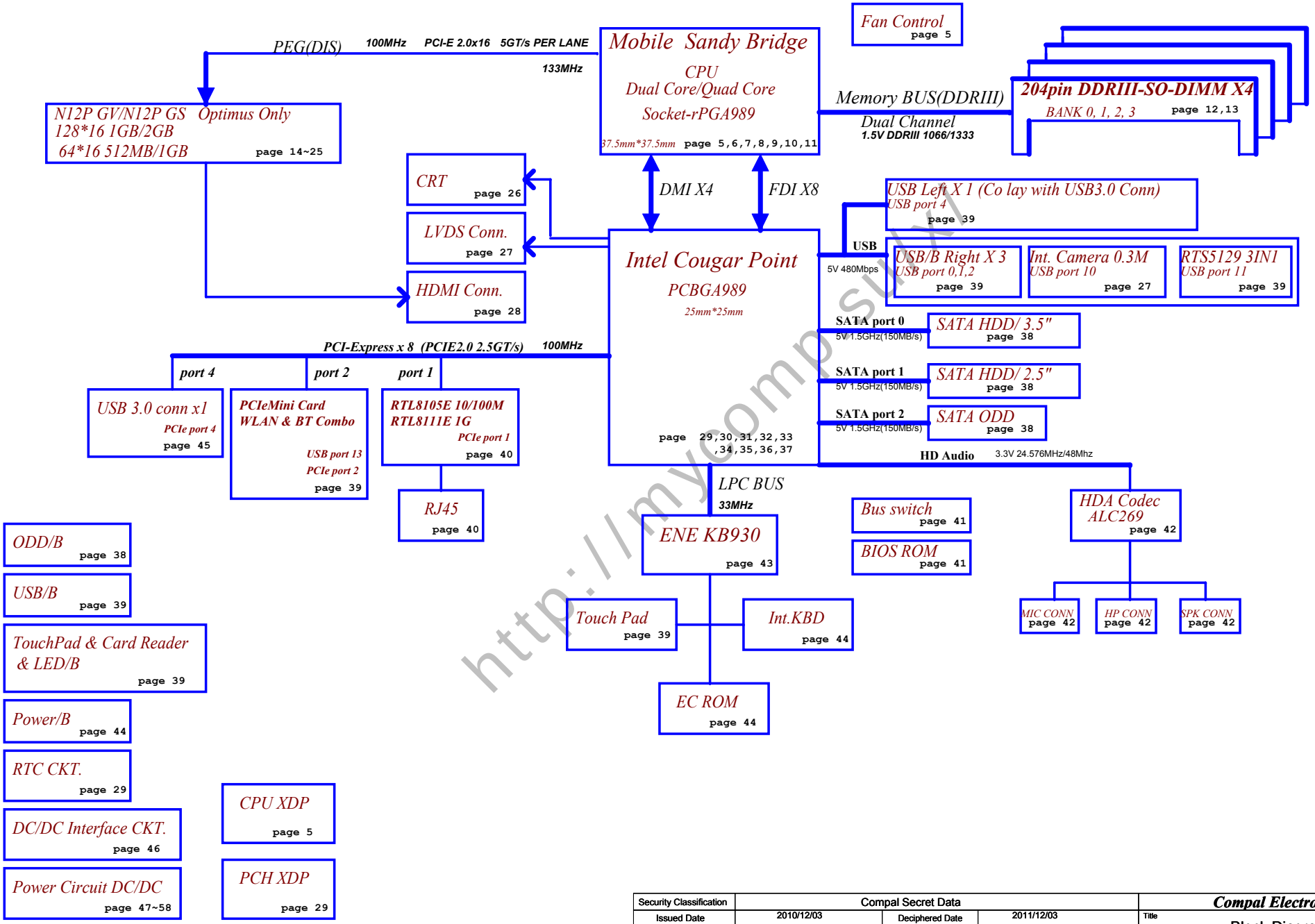
Model Name : PBL80

File Name : LA-7441PR01



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Title: Block Diagrams

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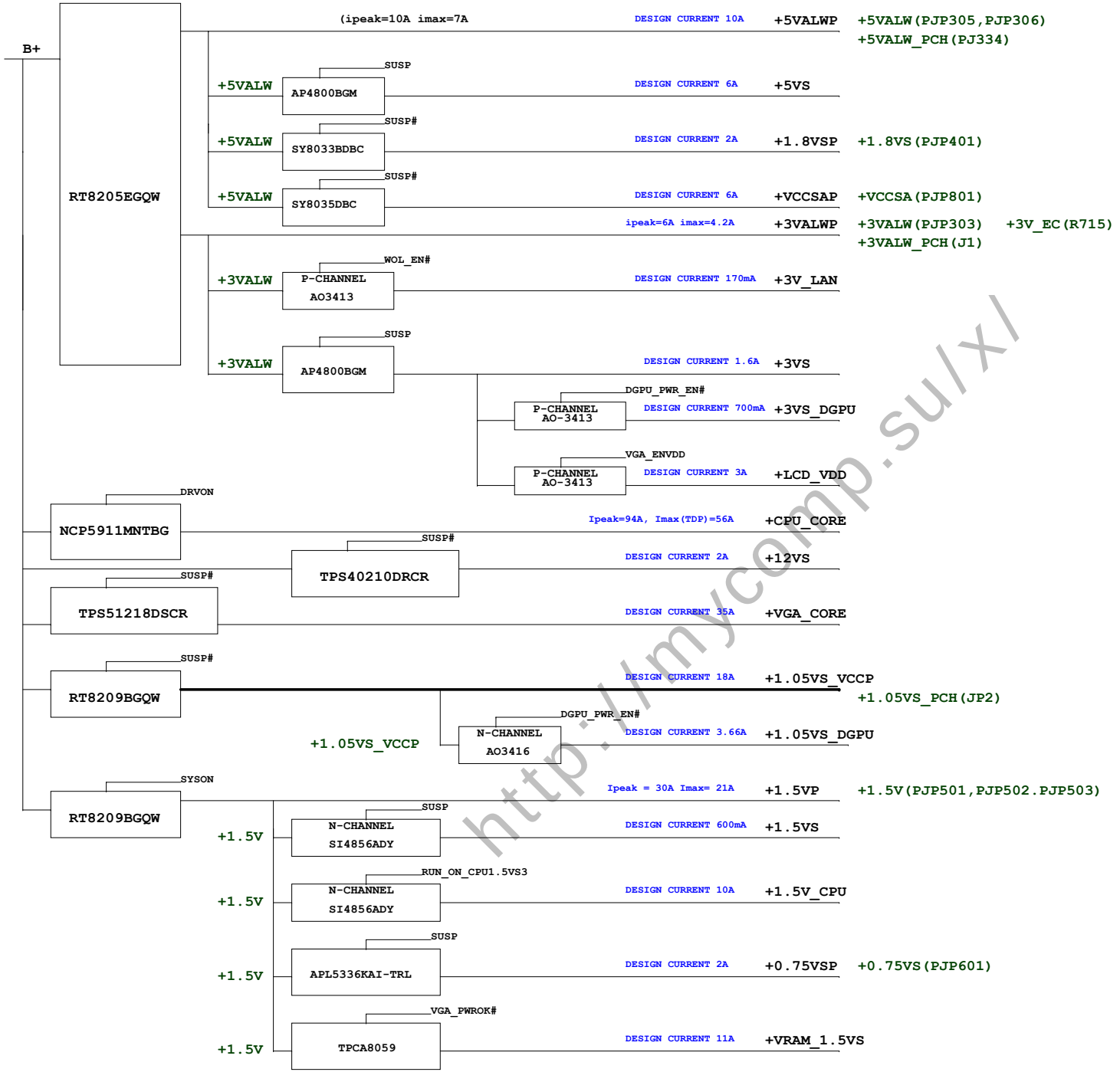

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Title: Power Map

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +5VALW_PCH +3VALW_PCH +3V_LAN +3V_EC +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS_VCCP +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VCCSA +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +12VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

Function	VRAM					GPU		Board ID
description	VRAM	Samsung 64bits	Hynix 64bits	Samsung 128bits	Hynix 128bits	N12P-GS	N12P-GV	Adaptor
explain	VRAM	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Adaptor
BTO	8PCS@	PD 20K	PD 15K	PD 45.3K	PD 34.8K	N12PGS@	N12PGV@	90W@, 120W@

Function	Crisis recovery	HDMI	WLAN+BT		LAN	
description	BUS SWITCH	HDMI	WLAN+BT(BT pin 51)	WLAN+BT(BT pin 5)	Giga LAN	10/100M LAN
explain	BUS SWITCH	HDMI	WLAN+BT(BT pin 51)	WLAN+BT(BT pin 5)	Strap pin	Strap pin
BTO	Debug@	HDMI@	BT@	COMBO@	8111E@	8105E@

Function	USB3.0/2.0 Colay		SATA3.0 Repeater Chip		SATA Preemphasis		SATA Equalization	
description	USB3.0	USB2.0	MAXIM	TI	Preemphasis		Equalization	
explain	USB3.0	USB2.0	MAX4951	SN75LVCP601	Enable	Disable	Maximum	Normal
BTO	USB3@	USB2@	MAXIM@	TI@	DEN@	NDEN@	EQ@	NEQ@

Function	SATA path	
description	PCH	Repeater
explain	PCH	Repeater
BTO	SATA@	SATARP@

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMMA1	A0 H	1010 0000 b
+3VS	DDR SO-DIMMA2	A0 H	1010 0010 b
+3VS	DDR SO-DIMMB1	A4 H	1010 0100 b
+3VS	DDR SO-DIMMB2	A0 H	1010 0110 b
+3VS	WLAN		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	VGA Thermal Sensor	9A H	1001 1010 b

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Title: Notes List

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Support Dual Core/ Quad Core

C1 @ 220P_0402_25V8J — H_PWRGOOD
C2 @ 220P_0402_25V8J — H_PROCHOT#

JCPUB

<33> H_SNB_IVB#	C26	SNB_IVB#	MISC
T1 PAD @ TP_SKTOCC#	AN34	SKTOCC#	MISC
T2 PAD @ H_CATERR#	AL33	CATERR#	THERMAL
<34,43> H_PECI	AN33	PECI	THERMAL
<43> H_PROCHOT# — R6 56_0402_5% H_PROCHOT#_R	AL32	PROCHOT#	THERMAL
<34> H_THERMTRIP# — R10 0_0402_5% H_THERMTRIP#_R	AN32	THERMTRIP#	THERMAL
<31> H_PM_SYNC	AM34	PM_SYNC	PWR MANAGEMENT
<34> H_PWRGOOD	AP33	UNCOREPWRGOOD	PWR MANAGEMENT
PM_SYS_PWRGD_BUF — R22 130_0402_5% PM_DRAM_PWRGD_R	V8	SM_DRAMPWROK	PWR MANAGEMENT
BUF_CPU_RST#	AR33	RESET#	PWR MANAGEMENT

Sandy Bridge_rPGA_Rev0p61
CONN@

CLOCKS

BCLK	A28	CLK_CPU_DMI <30>
BCLK#	A27	CLK_CPU_DMI# <30>
DPLL_REF_SSCLK	A16	R3 1K_0402_5% +1.05VS_VCCP — eDP
DPLL_REF_SSCLK#	A15	R4 1K_0402_5% +1.05VS_VCCP — eDP

If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor

DDR3 MISC

SM_DRAMRST#	R8	H_DRAMRST# <7>
SM_RCOMP[0]	AK1	SM_RCOMP_0 R7 140_0402_1%
SM_RCOMP[1]	A5	SM_RCOMP_1 R8 25.5_0402_1%
SM_RCOMP[2]	A4	SM_RCOMP_2 R9 200_0402_1%

DDR3 Compensation Signals Layout Note:Please these resistors near Processor
from DDR

JTAG & BPM

PRDY#	AP29	XDP_PRDY#_R	R11 @ 0_0402_5% XDP_PRDY#
PREQ#	AP27	XDP_PREQ#_R	R12 @ 0_0402_5% XDP_PREQ#
TCK	AR26	XDP_TCK_R	R13 @ 0_0402_5% XDP_TCK
TMS	AR27	XDP_TMS_R	R14 @ 0_0402_5% XDP_TMS
TRST#	AP30	XDP_TRST#_R	R15 @ 0_0402_5% XDP_TRST#
TDI	AR28	XDP_TDI_R	R16 @ 0_0402_5% XDP_TDI
TDO	AP26	XDP_TDO_R	R18 @ 0_0402_5% XDP_TDO
DBR#	AL35	XDP_DBRESET#_R	R21 @ 0_0402_5% XDP_DBRESET#
BPM#[0]	AT28	XDP_BPM#0_R	R24 @ 0_0402_5% XDP_BPM#0
BPM#[1]	AR29	XDP_BPM#1_R	R25 @ 0_0402_5% XDP_BPM#1
BPM#[2]	AR30	XDP_BPM#2_R	R26 @ 0_0402_5% XDP_BPM#2
BPM#[3]	AT30	XDP_BPM#3_R	R27 @ 0_0402_5% XDP_BPM#3
BPM#[4]	AP32	XDP_BPM#4_R	R28 @ 0_0402_5%
BPM#[5]	AR31	XDP_BPM#5_R	R30 @ 0_0402_5%
BPM#[6]	AT31	XDP_BPM#6_R	R32 @ 0_0402_5%
BPM#[7]	AR32	XDP_BPM#7_R	R34 @ 0_0402_5%

Routed as a single daisy chain
R20 1K_0402_5% +3VS — XDP_DBRESET# <29,31>
CFG12 <10>, CFG13 <10>, CFG14 <10>, CFG15 <10>
Close to CPU side

Processor Pullups

+1.05VS_VCCP
R17 62_0402_5% H_PROCHOT#
R23 10K_0402_5% H_PWRGOOD

Follow DG 0.71

+3VALW
C3 0.1U_0402_16V4Z
U1 74AHC1G09GW_TSSOP5
<31> PWROK — R37 0_0402_5%
<31> DRAMPWROK
PM_SYS_PWRGD_BUF
+1.5V_CPU
R36 200_0402_5%
@ R38 39_0402_5%
<46,53> SUSP — @ Q1 2N7002_SOT23
FIT 1.5V POWER PLANE OF CPU
CHANGE U5 TO OPEN DRAIN MOS,OUTPUT=1.5V

PU/PD for JTAG signals

+1.05VS_VCCP
XDP_TMS_R R39 51_0402_5%
XDP_TDI_R R40 51_0402_5%
XDP_TDO_R R41 51_0402_5%
XDP_TCK_R R42 51_0402_5%
XDP_TRST#_R R43 51_0402_5%

Buffered reset to CPU

+3VS
C6 0.1U_0402_16V4Z
+1.05VS_VCCP
R50 75_0402_5%
U3 SN74LVC1G07DCKR_SC70-5
R55 0_0402_5%
<33,39> PLT_RST#
R52 43_0402_1%
BUFO_CPU_RST# — BUF_CPU_RST#
@ R53 0_0402_5%

XDP Connector

JXDP1 @ ACES_87152-26051

XDP_PREQ#	XDP_PRDY#	
XDP_BPM#0	XDP_BPM#1	
XDP_BPM#2	XDP_BPM#3	
H_PWRGOOD	R44 1K_0402_5%	XDP_CPU_HOOK0
<29,31,43> PBTN_OUT#	R45 0_0402_5%	XDP_CPU_HOOK1
<10> CFG0	R46 1K_0402_5%	XDP_CPU_HOOK2
<31,43,55> VGATE	R47 0_0402_5%	XDP_CPU_HOOK3
<10,30> CLK_RES_ITP		
<10,30> CLK_RES_ITP#		
+1.05VS_VCCP		
PLT_RST#	R48 1K_0402_5%	XDP_CPU_HOOK6
		XDP_DBRESET#
		XDP_TDO
		XDP_TRST#
		XDP_TDI
		XDP_TMS
		XDP_TCK

C8 0.1U_0402_10V6K @

FAN Control Circuit

+5VS — 1A
C4 10U_0805_10V4Z
U2 G996P11U SOP 8P (EN, VIN, VOUT, VSET, GND)
<43> EN_DFAN1 — R49 330_0402_5%
+FAN_VCC
C7 0.047U_0402_16V7K
C5 @ 1000P_0402_50V7K
20mil
JFAN — CVILU_CI4403M1HRT-NH @
R51 10K_0402_5% +3VS
FAN_SPEED1 <43>
C9 @ 0.01U_0402_25V7K

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Title	Sandy Bridge(1/6)-CLK/MISC/JTAG/XDP/FAN		
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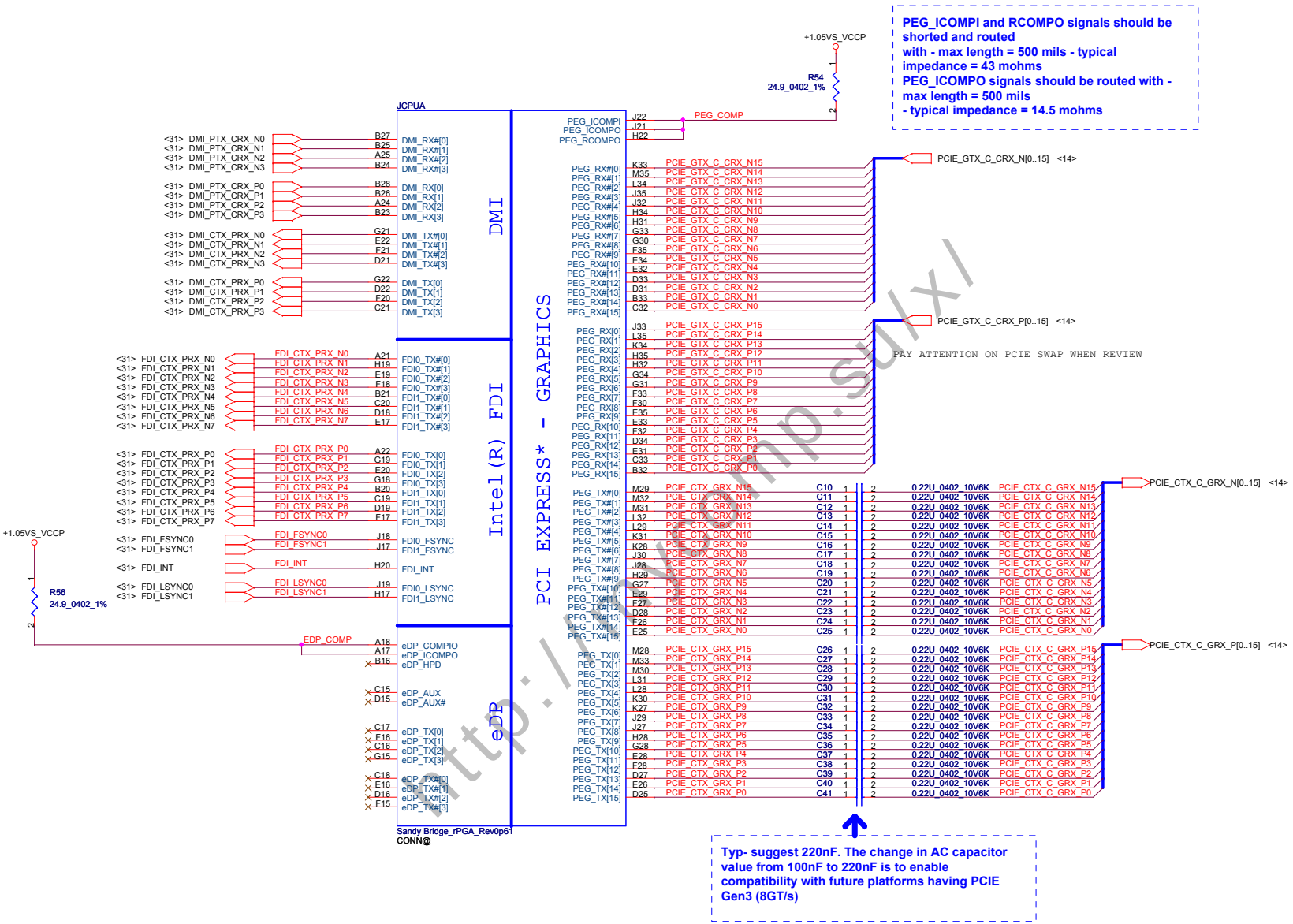

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Compal Electronics, Inc.

Title: Sandy Bridge(2/6)-DMI/FDI/PEG/eDP

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

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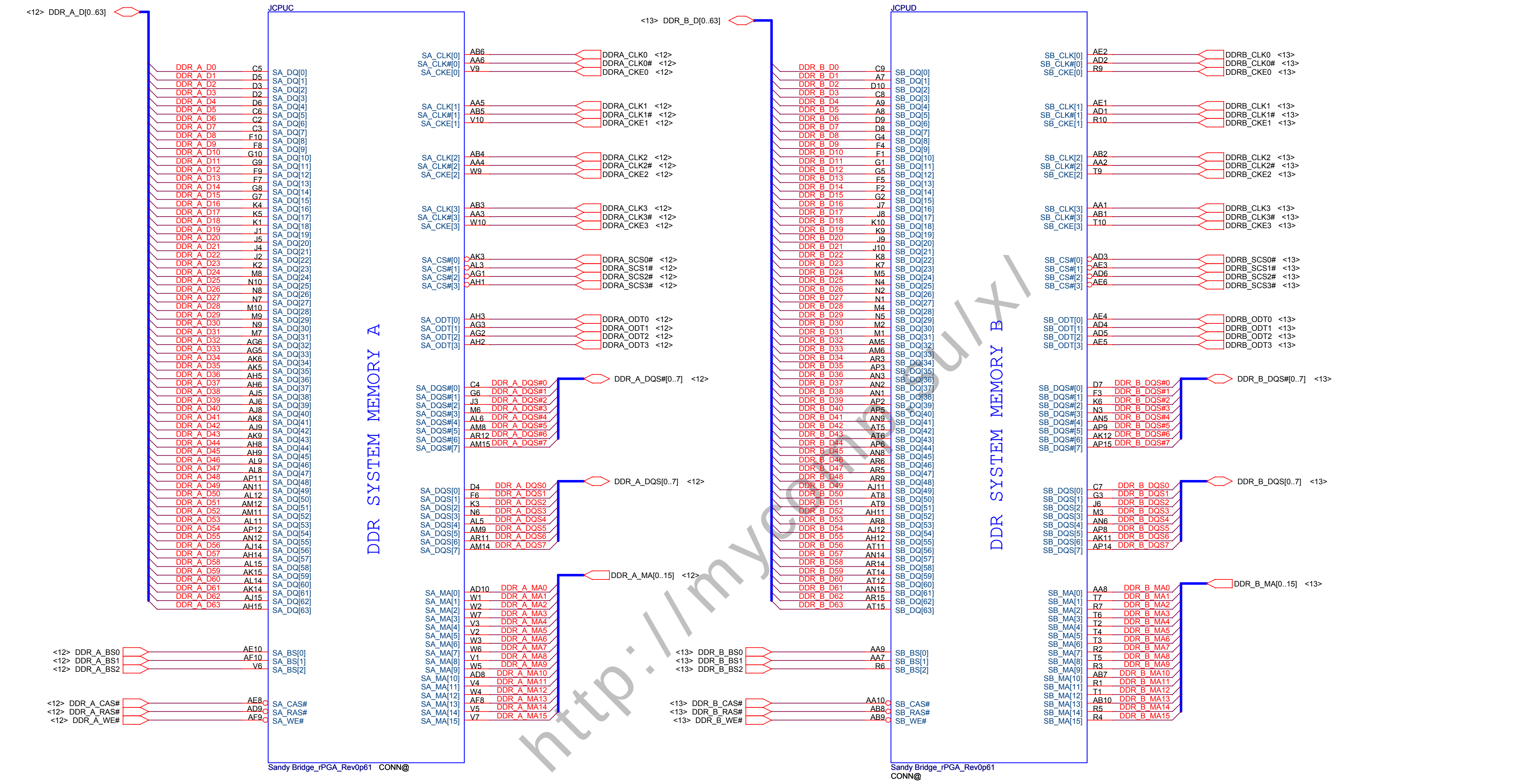

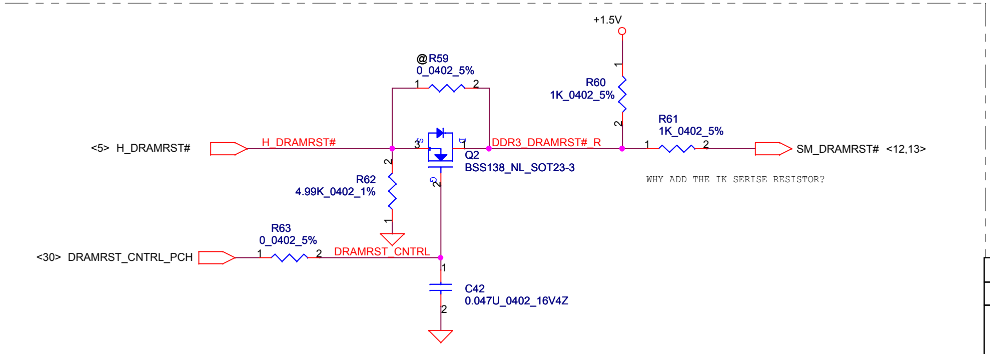

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Compal Electronics, Inc.

Title: Sandy Bridge(3/6)-DDR III

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Group1

POWER

+CPU_CORE

JCPUF

94A

18A

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

AG35	VCC1	VCCIO1	AH13
AG34	VCC2	VCCIO2	AH10
AG33	VCC3	VCCIO3	AG10
AG32	VCC4	VCCIO4	AC10
AG31	VCC5	VCCIO5	Y10
AG30	VCC6	VCCIO6	U10
AG29	VCC7	VCCIO7	P10
AG28	VCC8	VCCIO8	L10
AG27	VCC9	VCCIO9	J14
AG26	VCC10	VCCIO10	J13
AF35	VCC11	VCCIO11	J12
AF34	VCC12	VCCIO12	J11
AF33	VCC13	VCCIO13	H14
AF32	VCC14	VCCIO14	H12
AF31	VCC15	VCCIO15	H11
AF30	VCC16	VCCIO16	G14
AF29	VCC17	VCCIO17	G13
AF28	VCC18	VCCIO18	G12
AF27	VCC19	VCCIO19	F14
AF26	VCC20	VCCIO20	F13
AD35	VCC21	VCCIO21	F12
AD34	VCC22	VCCIO22	F11
AD33	VCC23	VCCIO23	E14
AD32	VCC24	VCCIO24	E12
AD31	VCC25	VCCIO25	E11
AD30	VCC26	VCCIO26	D14
AD29	VCC27	VCCIO27	D13
AD28	VCC28	VCCIO28	D12
AD27	VCC29	VCCIO29	D11
AD26	VCC30	VCCIO30	C14
AC35	VCC31	VCCIO31	C13
AC34	VCC32	VCCIO32	C12
AC33	VCC33	VCCIO33	C11
AC32	VCC34	VCCIO34	B14
AC31	VCC35	VCCIO35	B12
AC30	VCC36	VCCIO36	A14
AC29	VCC37	VCCIO37	A13
AC28	VCC38	VCCIO38	A12
AC27	VCC39	VCCIO39	A11
AC26	VCC40	VCCIO40	J23
AA35	VCC41		
AA34	VCC42		
AA33	VCC43		
AA32	VCC44		
AA31	VCC45		
AA30	VCC46		
AA29	VCC47		
AA28	VCC48		
AA27	VCC49		
AA26	VCC50		
Y35	VCC51		
Y34	VCC52		
Y33	VCC53		
Y32	VCC54		
Y31	VCC55		
Y30	VCC56		
Y29	VCC57		
Y28	VCC58		
Y27	VCC59		
Y26	VCC60		
V35	VCC61		
V34	VCC62		
V33	VCC63		
V32	VCC64		
V31	VCC65		
V30	VCC66		
V29	VCC67		
V28	VCC68		
V27	VCC69		
V26	VCC70		
U35	VCC71		
U34	VCC72		
U33	VCC73		
U32	VCC74		
U31	VCC75		
U30	VCC76		
U29	VCC77		
U28	VCC78		
U27	VCC79		
U26	VCC80		
R35	VCC81		
R34	VCC82		
R33	VCC83		
R32	VCC84		
R31	VCC85		
R30	VCC86		
R29	VCC87		
R28	VCC88		
R27	VCC89		
R26	VCC90		
P35	VCC91		
P34	VCC92		
P33	VCC93		
P32	VCC94		
P31	VCC95		
P30	VCC96		
P29	VCC97		
P28	VCC98		
P27	VCC99		
P26	VCC100		

Sandy Bridge_rPGA_Rev0p61

CONN@

Material Note (+1.05VS_VCCP)

2 x 330 µF
(3x 330 µF for 2012 capable designs)
Top Socket Cavity 22U 0805 *7
Bottom Socket Cavity 22U 0805 *5

+1.05VS_VCCP

C43 22U_0805_6.3V6M
C44 22U_0805_6.3V6M
C45 22U_0805_6.3V6M
C46 22U_0805_6.3V6M
C47 22U_0805_6.3V6M
C48 22U_0805_6.3V6M
C49 22U_0805_6.3V6M
C50 22U_0805_6.3V6M
C51 22U_0805_6.3V6M
C52 22U_0805_6.3V6M
C53 22U_0805_6.3V6M
C54 22U_0805_6.3V6M
C62 330U_D2_2V_Y
C63 330U_D2_2V_Y
@C64 330U_D2_2V_Y

Cap quantity follow 439028_HR_PDDG_R1_51

+1.05VS_VCCP

C83 330U_2.5V_M_R17
C73 @ 330U_2.5V_M_R17

reserve for test
please co-layout with C62,C63

+1.05VS_VCCP +1.05VS_VCCP

R65 130_0402_5%
R66 75_0402_5%
R67 43_0402_1%

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK R68 0_0402_5%
VIDSOUT AJ28 H_CPU_SVIDDAT R69 0_0402_5%

VR_SVID_ALRT# <55>
VR_SVID_CLK <55>
VR_SVID_DAT <55>

Resistors close to CPU

Close to CPU

+CPU_CORE

VCCSENSE R70 100_0402_1%
VSSSENSE R71 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R R72 0_0402_5% VCCSENSE
VSS_SENSE AJ34 VSSSENSE_R R73 0_0402_5% VSSSENSE

VCCSENSE <55>
VSSSENSE <55>

VCCIO_SENSE B10
VSSIO_SENSE A10

VCCIO_SENSE <52>
R74 10_0402_5%

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Title: Sandy Bridge(4/6)-PWR

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POWER Group2

Material Note (GFXCORE)
2 x 330 µF on Bottom socket edge
Bottom Socket Cavity 22U 0805 *2
Bottom Socket Edge 22U 0805 *4
Top Socket Cavity 22U 0805 *2
Top Socket Edge 22U 0805 *4

+GFX_CORE
C217 330U_D2_2V_Y
C225 330U_D2_2V_Y
22U_0805_6.3V6M: C284 C285 C286 C414 C415 C416 C364 C365 C410 C412 C411 C413

JCPUG
26A
AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

SENSE LINES
VAXG_SENSE → AK35
VSSAXG_SENSE → AK34
R131 100_0402_1% +GFX_CORE
R129 100_0402_1%
VCC_AXG_SENSE <55>
VSS_AXG_SENSE <55>

VREF
SM_VREF → AL1
+1.5V_CPU
R76 0_0402_5%
R75 1K_0402_1%
R77 1K_0402_1%
+V_SM_VREF_CNT
+V_SM_VREF
@ Q3 AP2302GN-HF_SOT23-3
RUN_ON_CPU1.5VS3
C65 0.1U_0402_16V4Z

Follow DG V1.5 P.109
+V_SM_VREF should have 20 mil trace width

DDR3 -1.5V RAILS
5A
VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15
AF7 AF4 AE1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1
+1.5V_CPU
@ JP1 JUMP_43X118 +1.5V
10U_0603_6.3V6M: C66 C67 C68 C69 C70 C71
330U_D2_2V_Y C72

Material Note (VDDQ)
Bottom Socket Edge
1 x 330 µF
10U 0805 *6

SA RAIL
6A
VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8
M27 M26 L26 J26 J25 J24 H26 H25
+VCCSA
10U_0805_6.3V6M: C74 C75 C76
R78 0_0402_5%
330U_D2_2V_Y C78
VCCSA_SENSE

Material Note (VCCSA)
1 x 330 µF
Bottom Socket Cavity 10U 0805 *2
Bottom Socket Edge 10U 0805 *1

MISC
VCCSA_SENSE → H23
VCCSA_SENSE <54>
FC_C22 → C22
VCCSA_VID1 → C24
H_FC_C22
VCCSA_SEL <54>
R79 10K_0402_5%
@R80 0_0402_5%

1.8V RAIL
+1.8VS R124 0_0805_5%
C79 330U_D2_2V_Y @
C80 10U_0603_6.3V6M
C81 1U_0402_6.3V6K
C82 1U_0402_6.3V6K
+1.8VS_VCCPLL
VCCPLL1 → B6
VCCPLL2 → A6
VCCPLL3 → A2

Material Note (+1.8VS_VCCPLL)
1 x 330 µF
Bottom Socket Edge
1U 0402 *1
10U 0805 *1

Sandy Bridge_rPGA_Rev0p61
CONN@

+1.5V_CPU Source

+3VALW
R83 100K_0402_5%
R84 0_0402_5%
<43> CPU1.5V_S3_GATE
@R86 0_0402_5%
<43,46,50,52,54,57,58> SUSP#
RUN_ON_CPU1.5VS3#
Q35A 2N7002DW-T/R7_SOT363-6

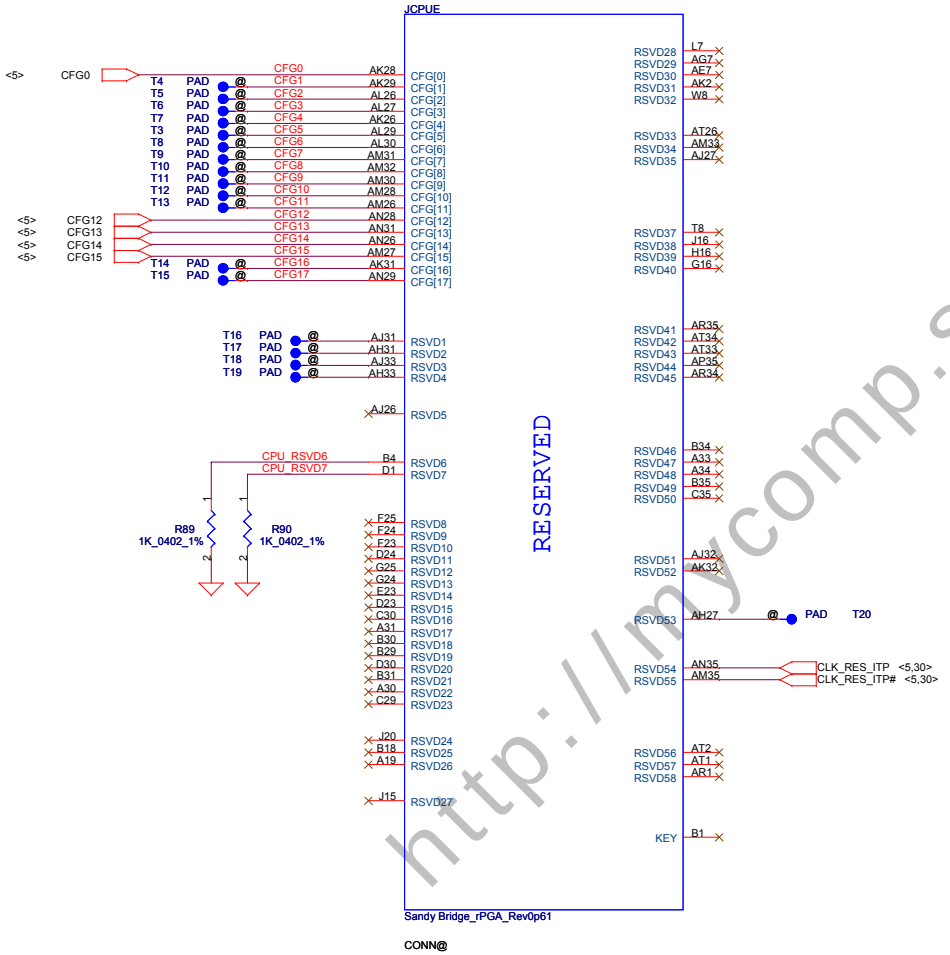
+VSB
R81 100K_0402_5%
+1.5V
Q4 SI4634DY-T1-GE3_SO8
RUN_ON_CPU1.5VS3
Q35B 2N7002DW-T/R7_SOT363-6
R85 330K_0402_5%
C86 0.1U_0402_16V4Z

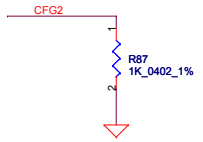
+1.5V_CPU
R82 470_0603_5%
RUN_ON_CPU1.5VS3#
Q6 2N7002H 1N SOT23-3

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

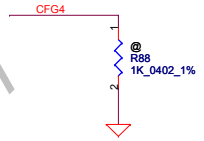
Compal Electronics, Inc.
Title: Sandy Bridge(4/6)-PWR
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1
Date: Friday, January 21, 2011 | Sheet 9 of 58

CFG Straps for Processor

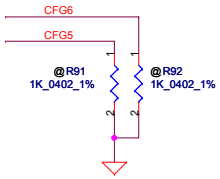




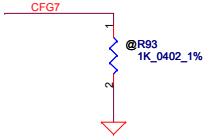
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



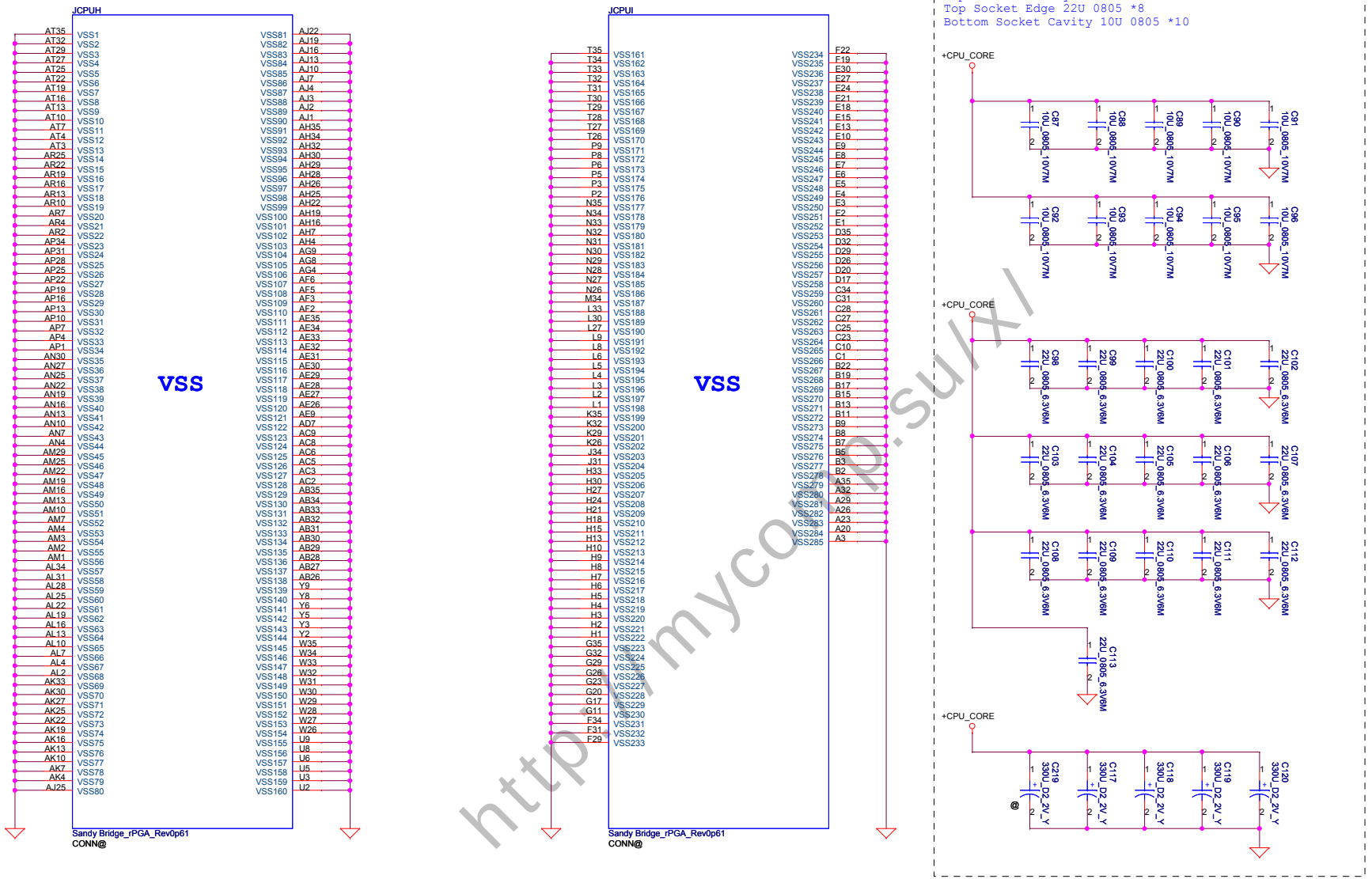
PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

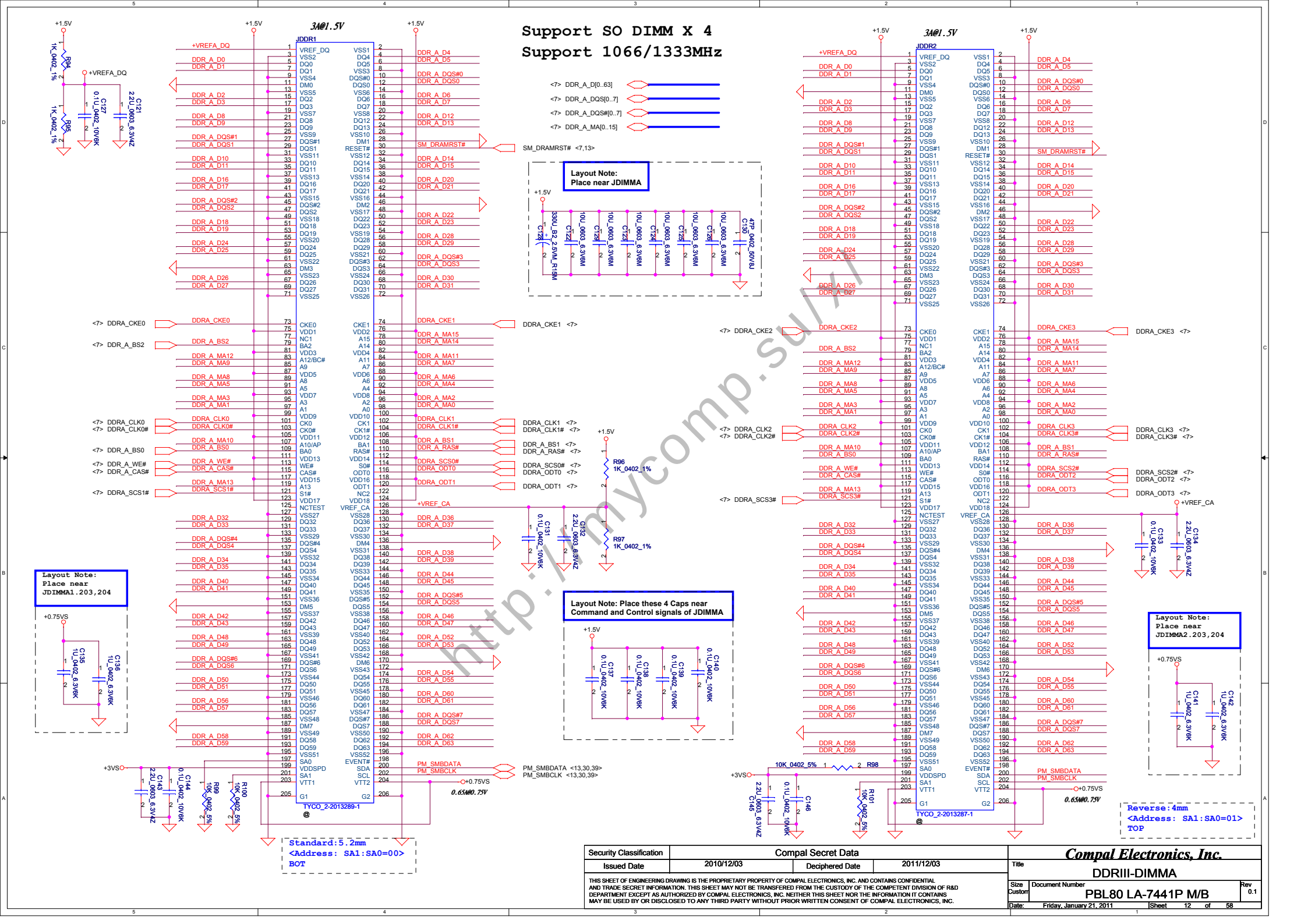
Compal Electronics, Inc.			
Title	Sandy Bridge(5/6) Reserve		
Size: Custom	Document Number: PBL80 LA-7441P M/B		Rev: 0.1
Date: Friday, January 21, 2011	Sheet 10 of 58		



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

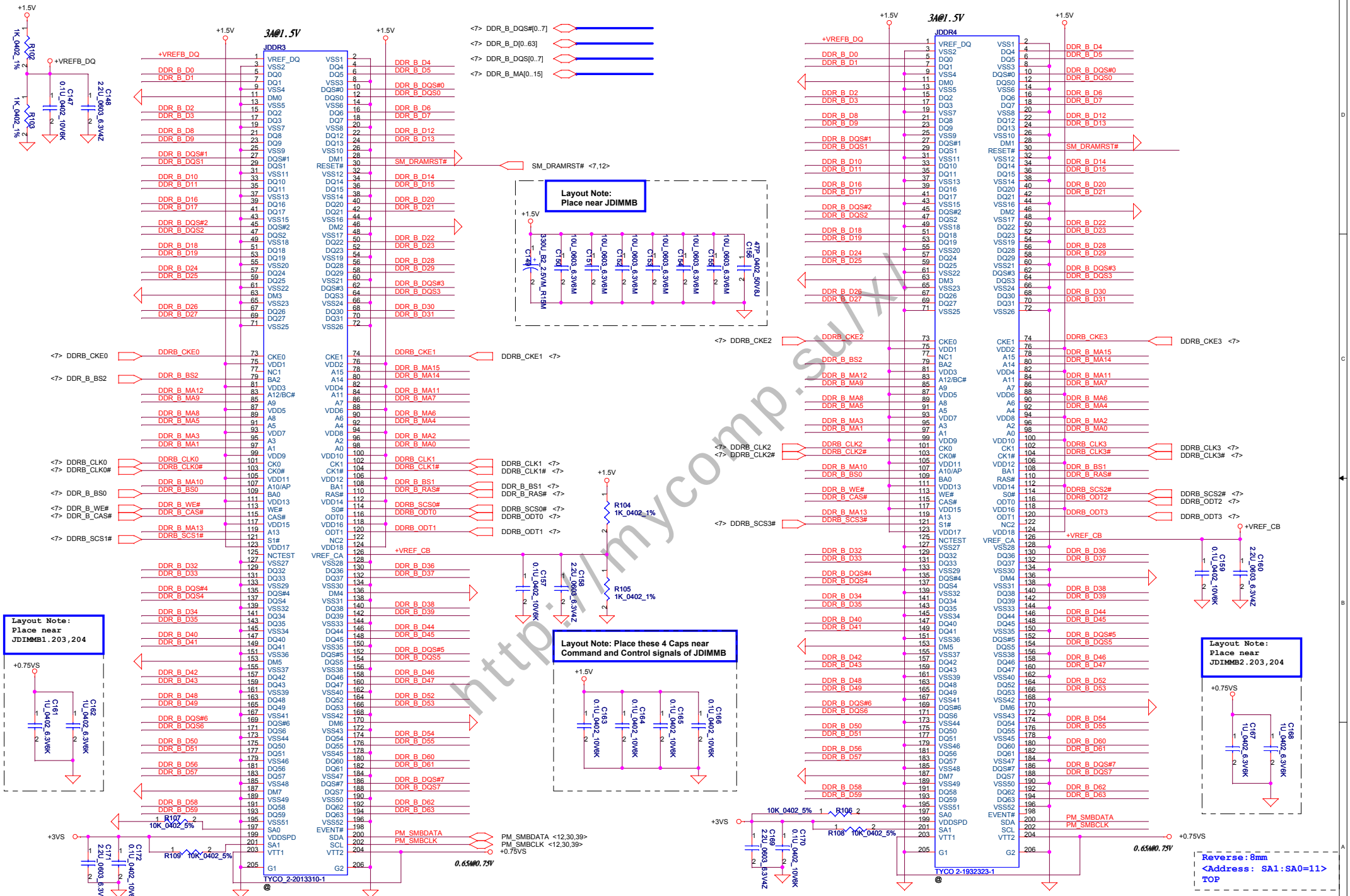
Title	Sandy Bridge(6/6)-GND	
Size: Custom	Document Number: PBL80 LA-7441P M/B	Rev: 0.1
Date: Friday, January 21, 2011	Sheet 11 of 58	



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

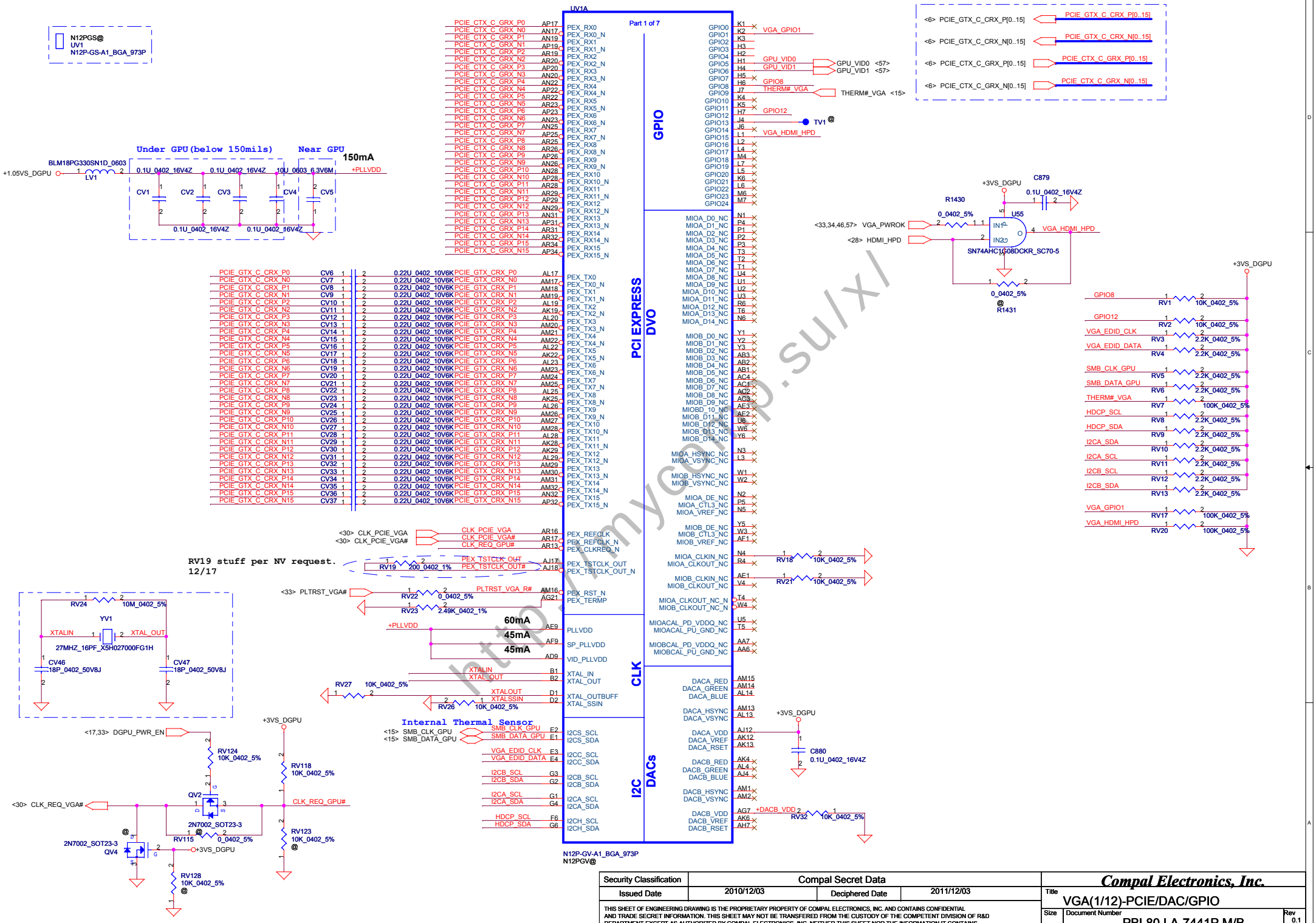
Title	DDRIII-DIMMA	
Size: Custom	Document Number: PBL80 LA-7441P M/B	Rev: 0.1
Date: Friday, January 21, 2011	Sheet 12 of 58	



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title	DDRIII-DIMMB	
Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1
Date: Friday, January 21, 2011	Sheet 13 of 58	



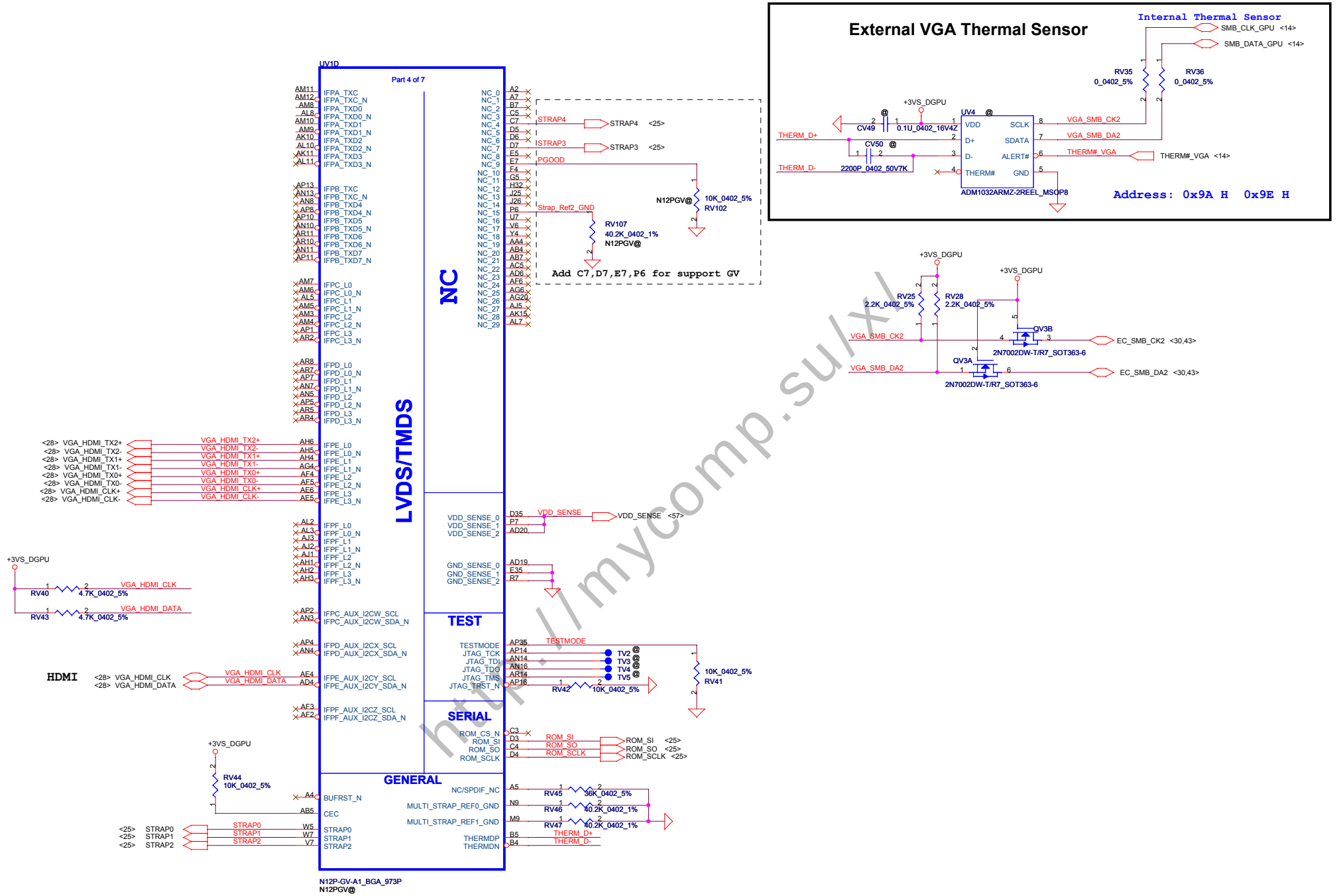
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(1/12)-PCIE/DAC/GPIO

Size: | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 14 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.	
Title	VGA(2/12)-LVDS/HDMI/DP/THM
Size	Document Number: PBL80 LA-7441P M/B
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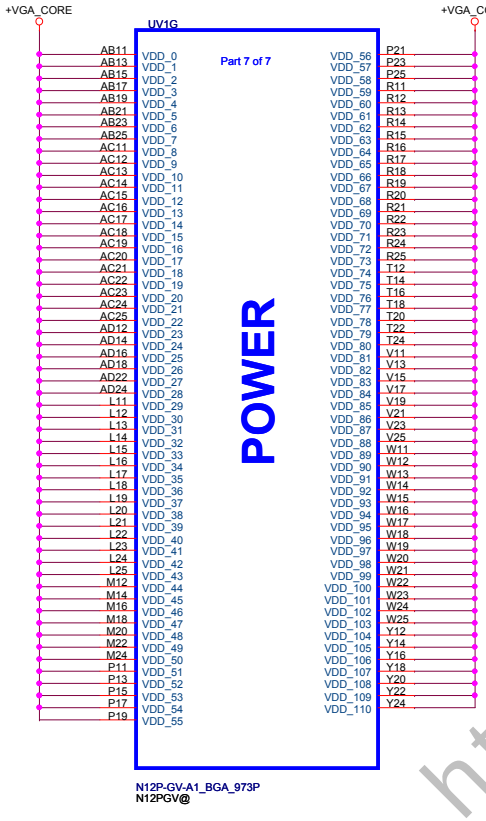
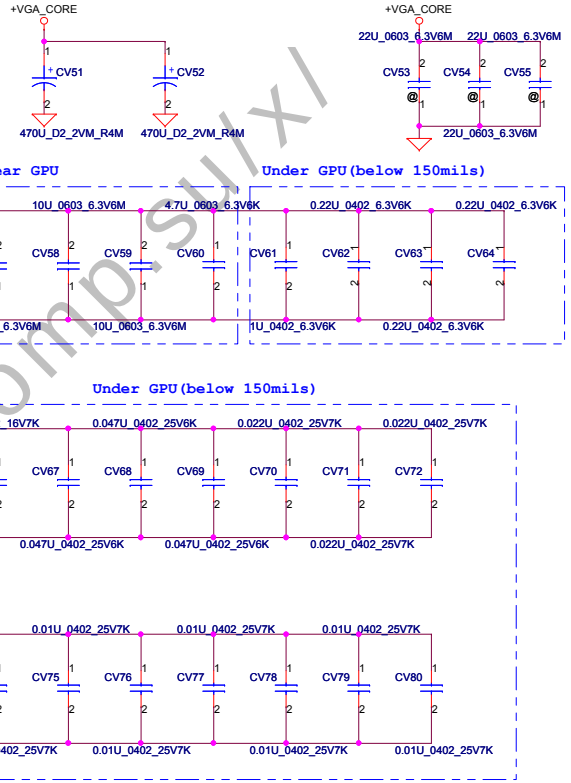
Pstate	GPU_VID0	GPU_VID1	N12P-GS	N12P-GV
P8-P12	0	0	0.825V	0.85V
P0(Hot)	1	0	0.975V	1V
	0	1		
P0(cold)	1	1	1V	1.025V



GS EDP Peak is 35.32A
GV EDP Peak is 21.56A



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title	VGA(3/12)-VGA CORE
Size	Document Number: PBL80 LA-7441P M/B
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GS is 5.49A
GV is 2.99A

GS is 2.95A
GV is 3.51A

Near GPU

Under GPU(below 150mils)

UV1E

Part 5 of 7

POWER

120mA

240mA (120mA each)

120mA(12~16mils)

220mA

570mA

+3VS to +3VS_DGPU

N12PGV@ N12P-GV-A1_BGA_973P

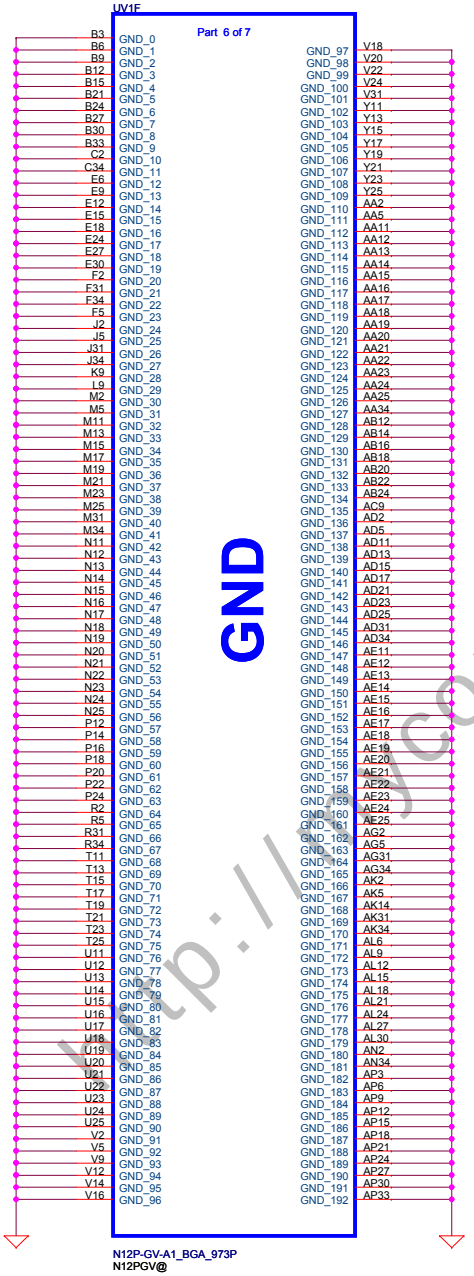
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(4/12)-POWER

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 17 of 58



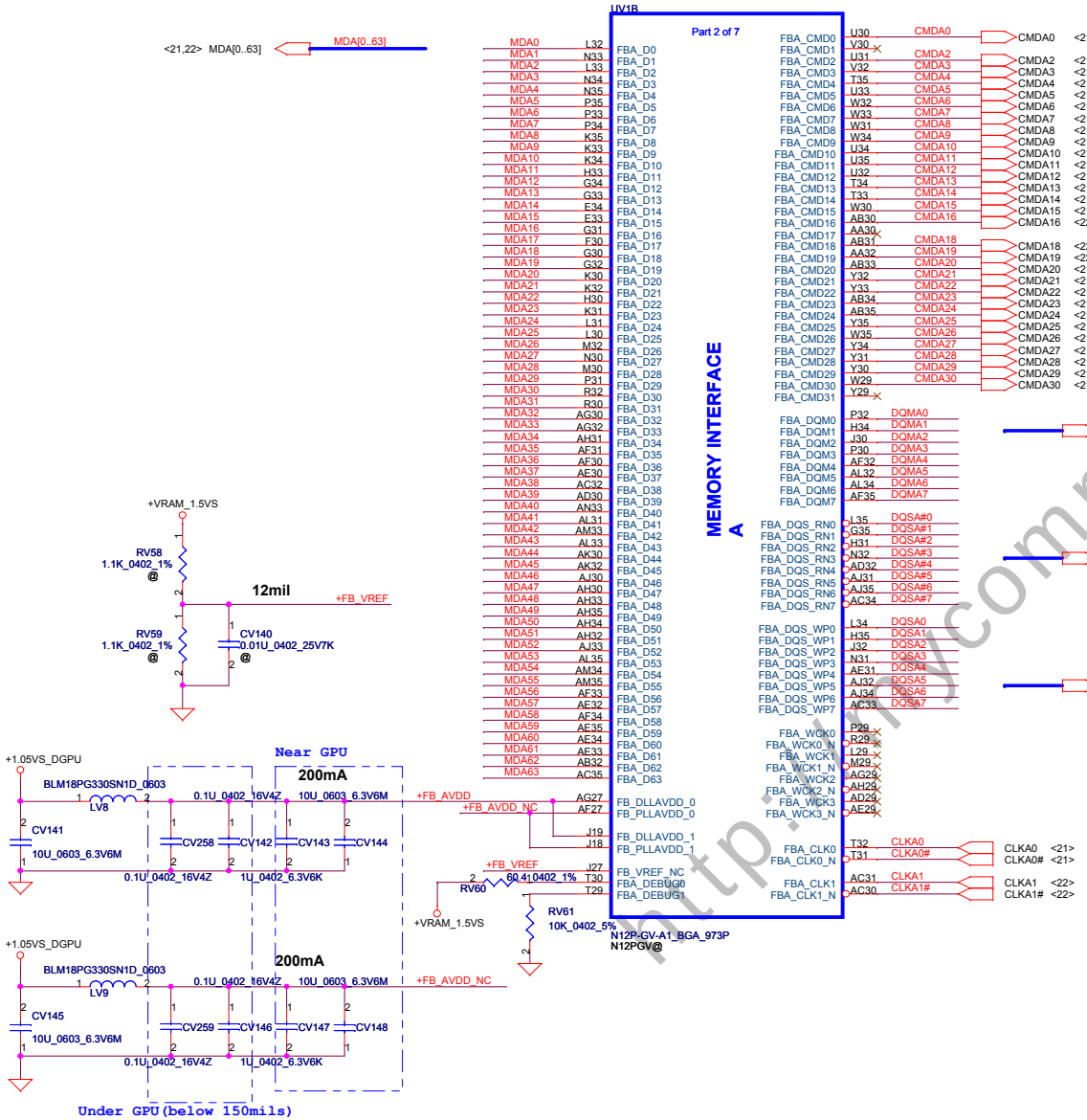
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(5/12)-GND

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 18 of 58



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

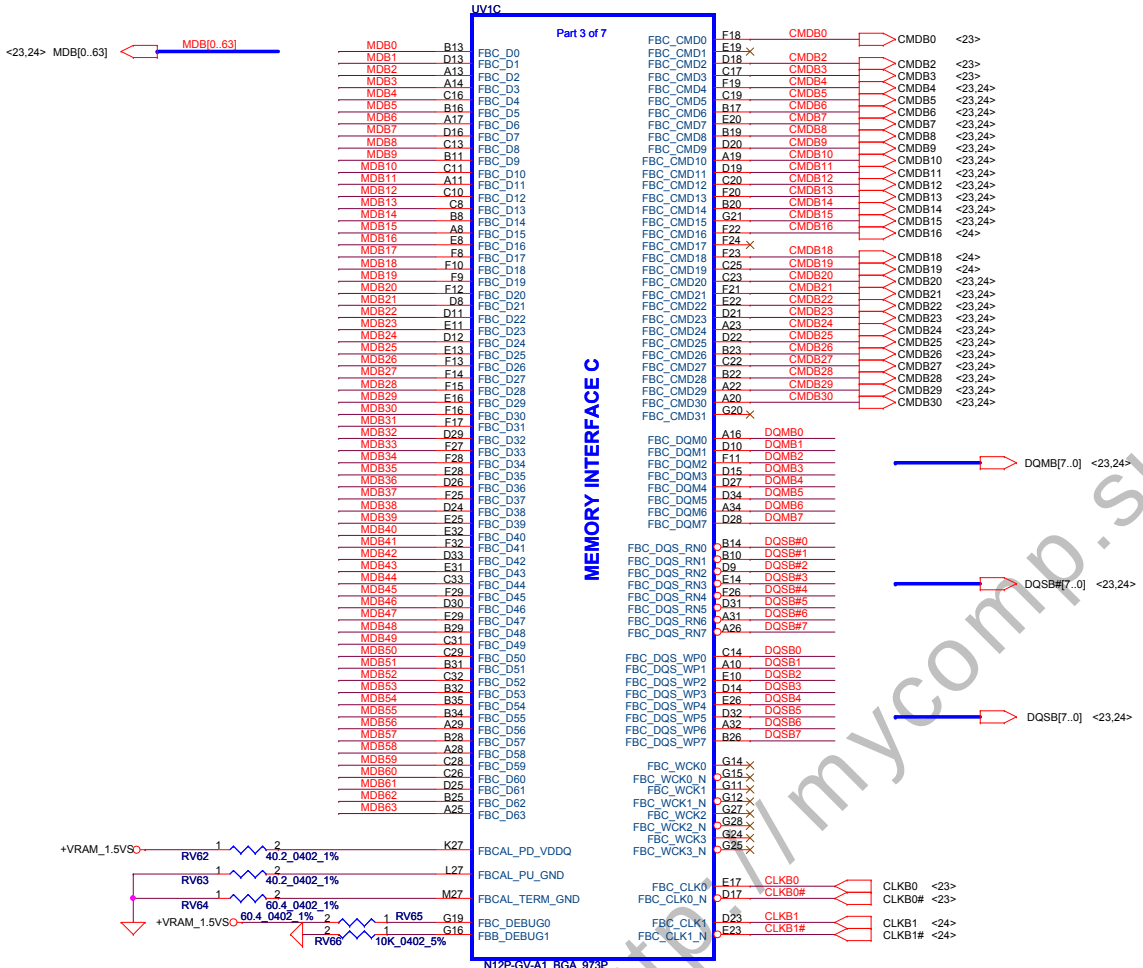
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(6/12)-MEM Interface A

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 19 of 58



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(7/12)-MEM Interface C

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

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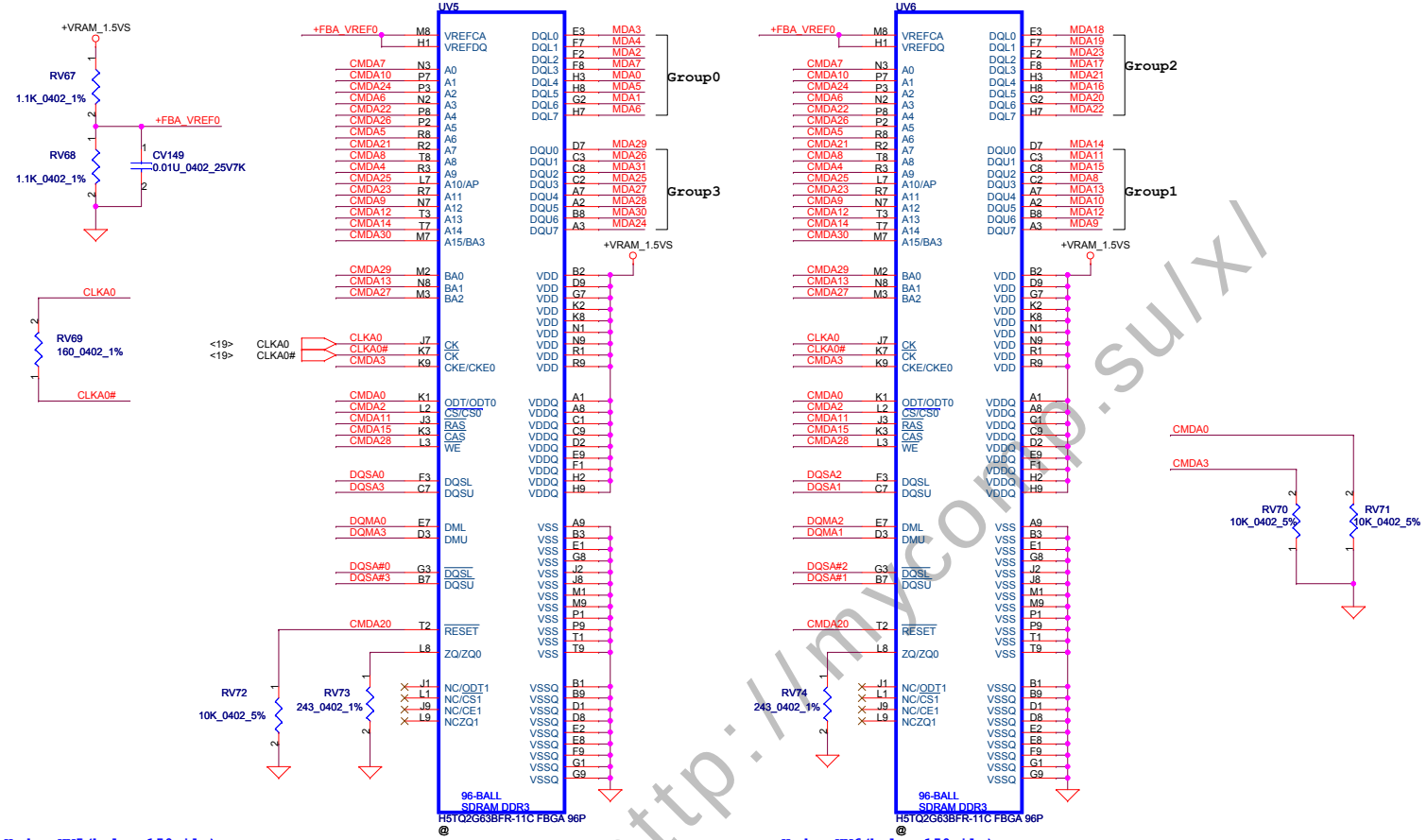
Memory Partition A - Lower 32 bits

Support N12P-GV/GS
Support Max VRAM 2G

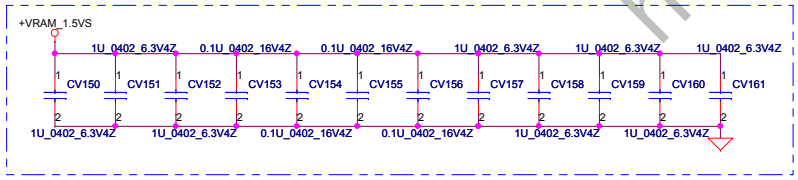


MDA[0..63] <19,22>
CMDA[30..0] <19,22>
DQMA[7..0] <19,22>
DQSA[7..0] <19,22>
DQSA#[7..0] <19,22>

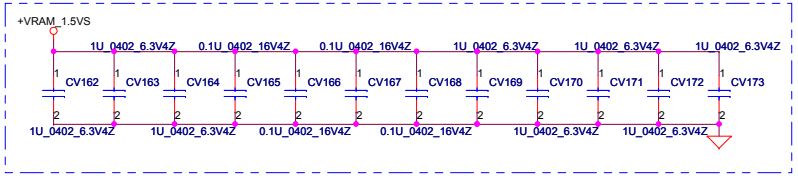
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Under UV5(below 150mils)



Under UV6(below 150mils)



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(8/12)-VRAM A Lower

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

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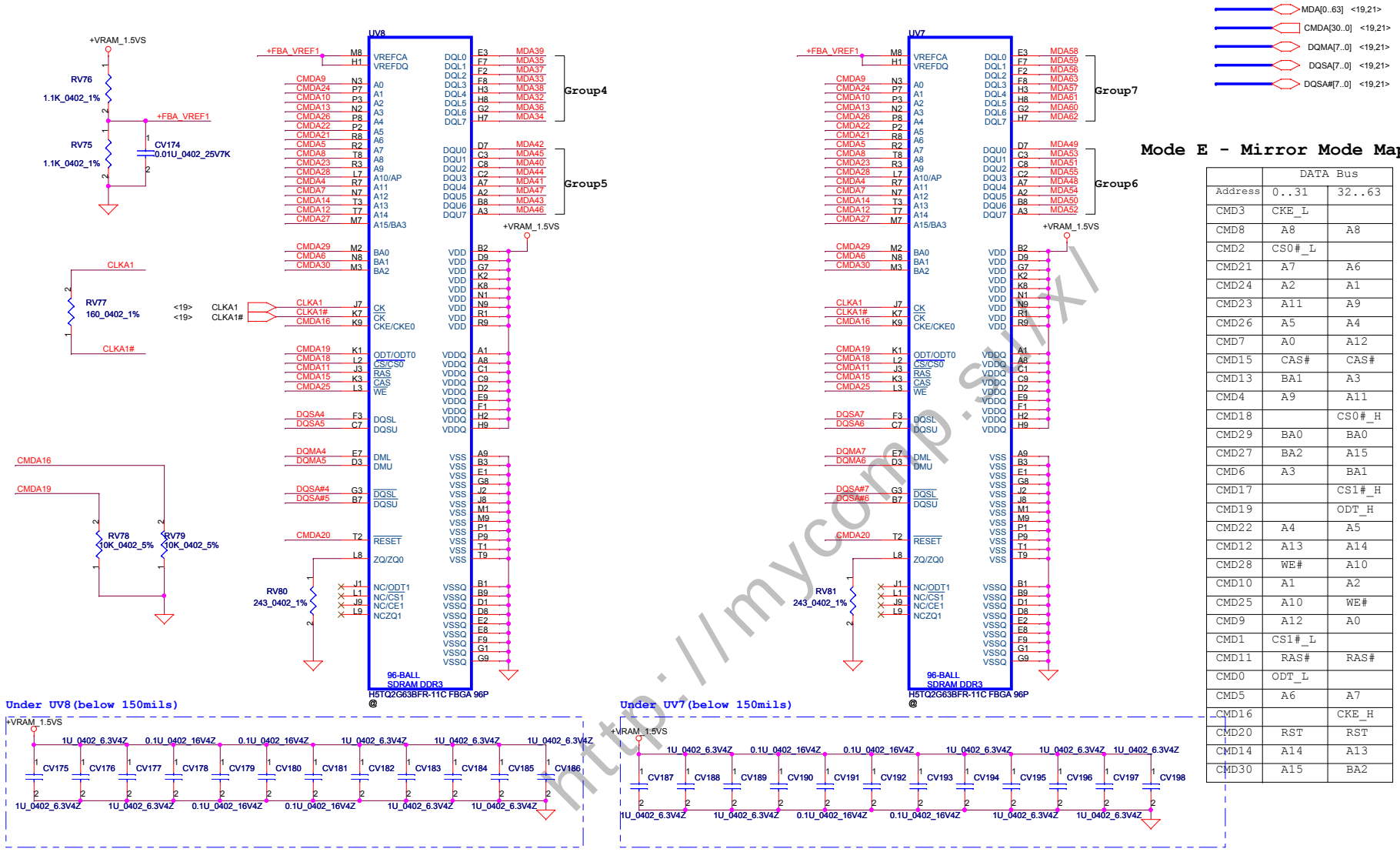
Memory Partition A - Upper 32 bits



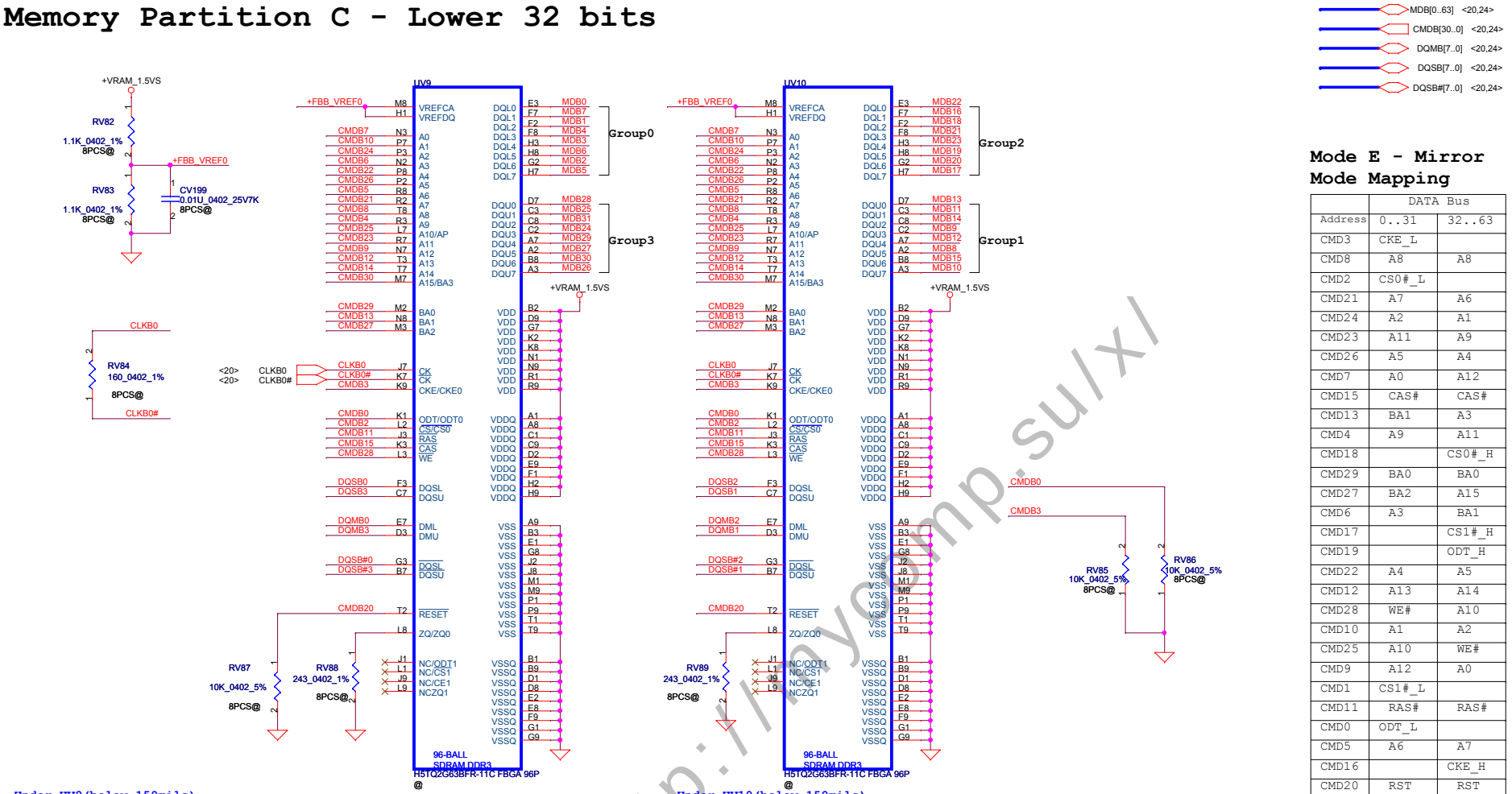
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.		
Title	VGA(9/12)-VRAM A Upper	
Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1
Date: Friday, January 21, 2011	Sheet 22 of 58	

Memory Partition C - Lower 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(10/12)-VRAM C Lower

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

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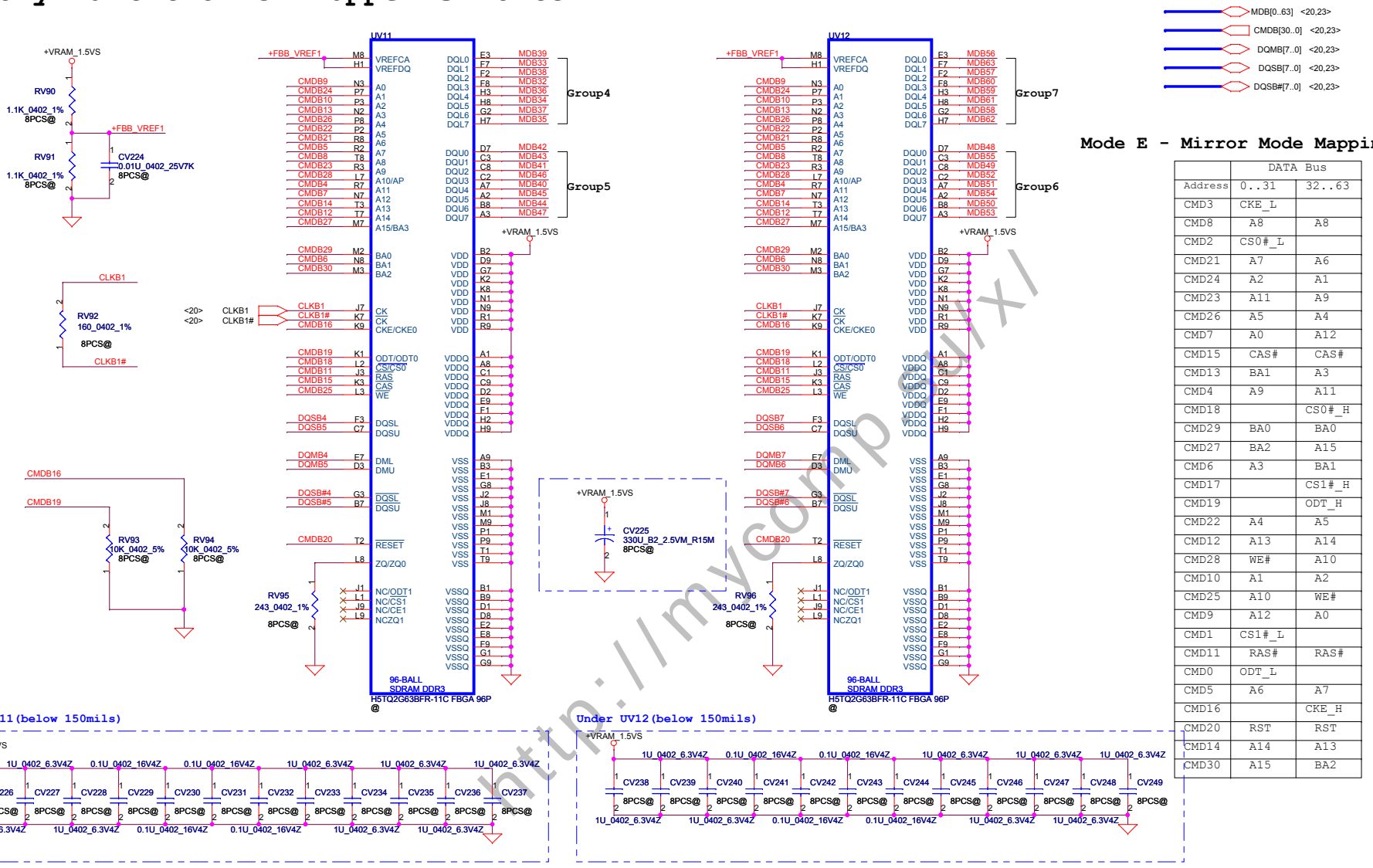
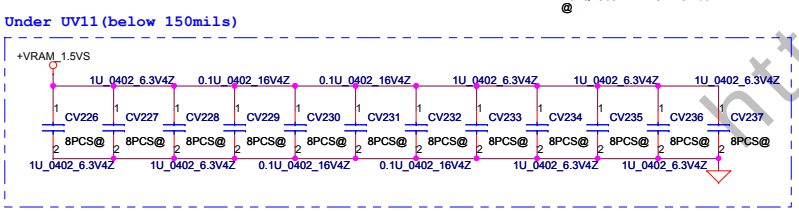
Memory Partition C - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: VGA(11/12)-VRAM C Upper

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

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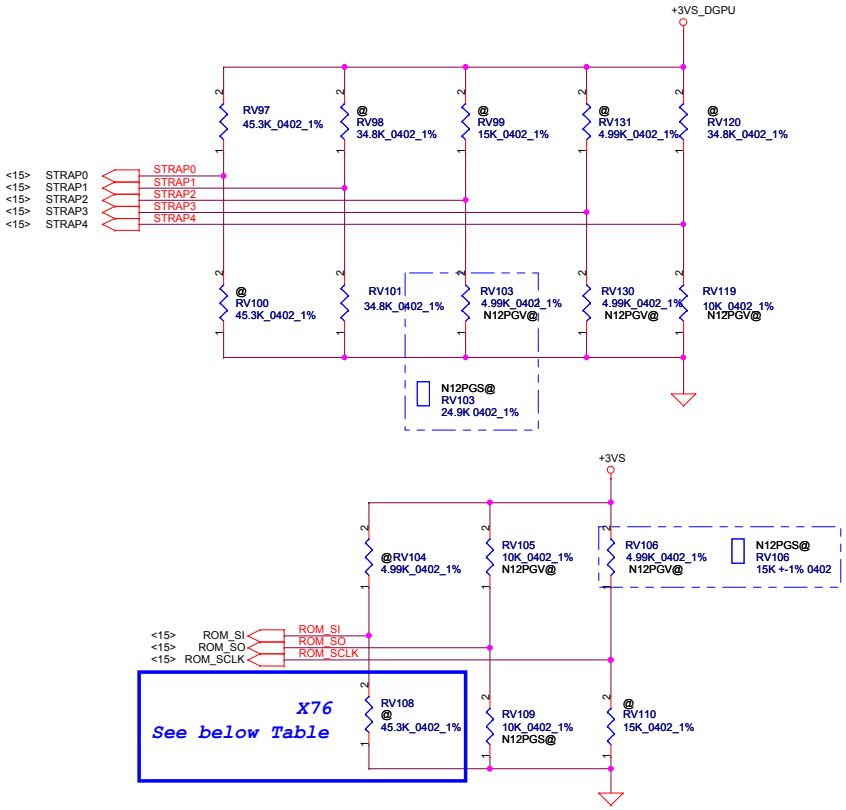


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SI	ROM_SCLK	ROM_SO	STRAP0
N12P-GS	0x0DF4	Below Table	Pull up 15K	Pull down 10K	Pull up 45K
N12P-GV	0x1050	Below Table	Pull up 5K	Pull up 10K	Pull up 45K

GPU	DeviceID	STRAP1	STRAP2	STRAP3	STRAP4
N12P-GS	0x0DF4	Pull down 35K	Pull down 25K		
N12P-GV	0x1050	Pull down 35K	Pull down 5K	Pull down 5K	Pull down 10K

GPU	DDR3 Type	VRAM		RAMCFG[3..0]		RV108
N12P-GS	64M16 900MHz	Hynix H5TQ1G63DFR-11C SA000041S20	512MB 1GB	0010	PD 15K	SD034154280
		Samsung K4W1G1646E-HC11 SA000041T00	512MB 1GB	0011	PD 20K	SD034200280
	128M16 900MHz	Hynix H5TQ2G63BFR-11C SA00003YO00	1GB 2GB	0110	PD 34.8K	SD034348280
		Samsung K4W2G1646C-HC11 SA000047Q00	1GB 2GB	0111	PD 45.3K	SD034453280
N12P-GV	64M16 800MHz	Hynix H5TQ1G63DFR-12C SA0000324C0	512MB	0010	PD 15K	SD034154280
		Samsung K4W1G1646G-BC12 SA00004HS00	512MB	0011	PD 20K	SD034200280
	128M16 800MHz	Hynix H5TQ2G63BFR-12C SA00003VS00	1GB	0110	PD 34.8K	SD034348280
		Samsung K4W2G1646C-HC12 SA00003MQ40	1GB	0111	PD 45.3K	SD034453280

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

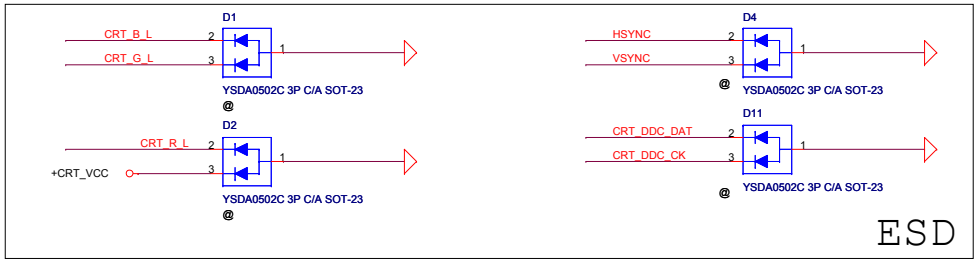
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

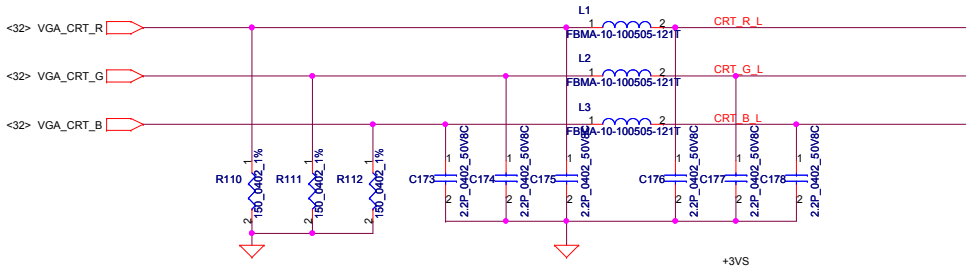
Compal Electronics, Inc.

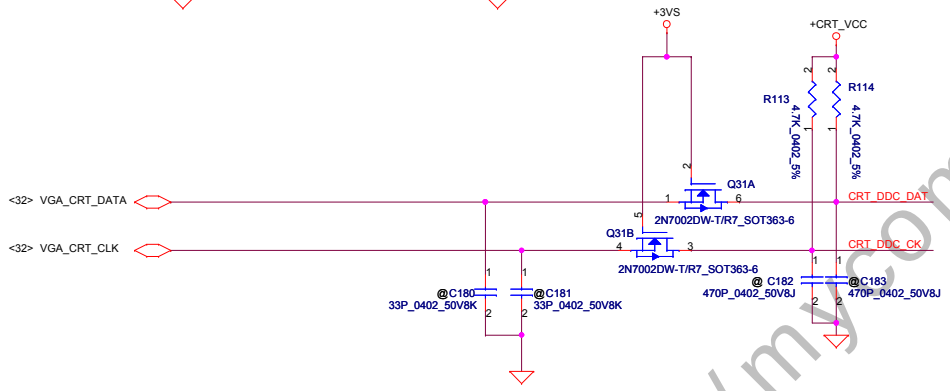
Title: VGA(12/12)-MISC

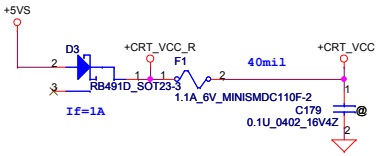
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

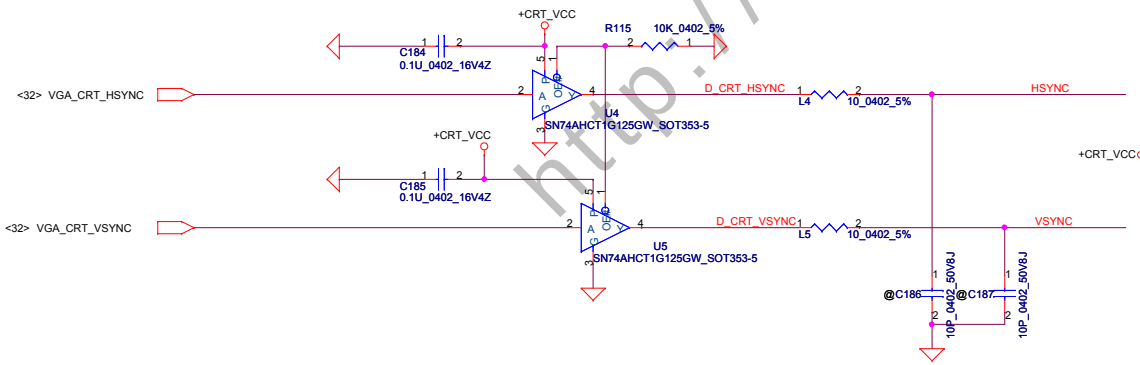
Date: Friday, January 21, 2011 | Sheet 25 of 58



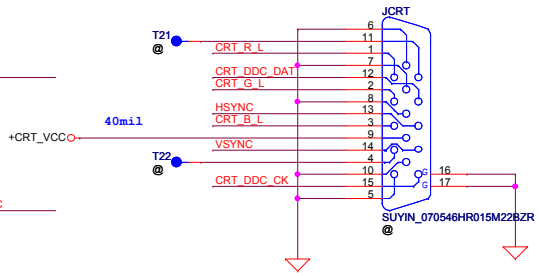






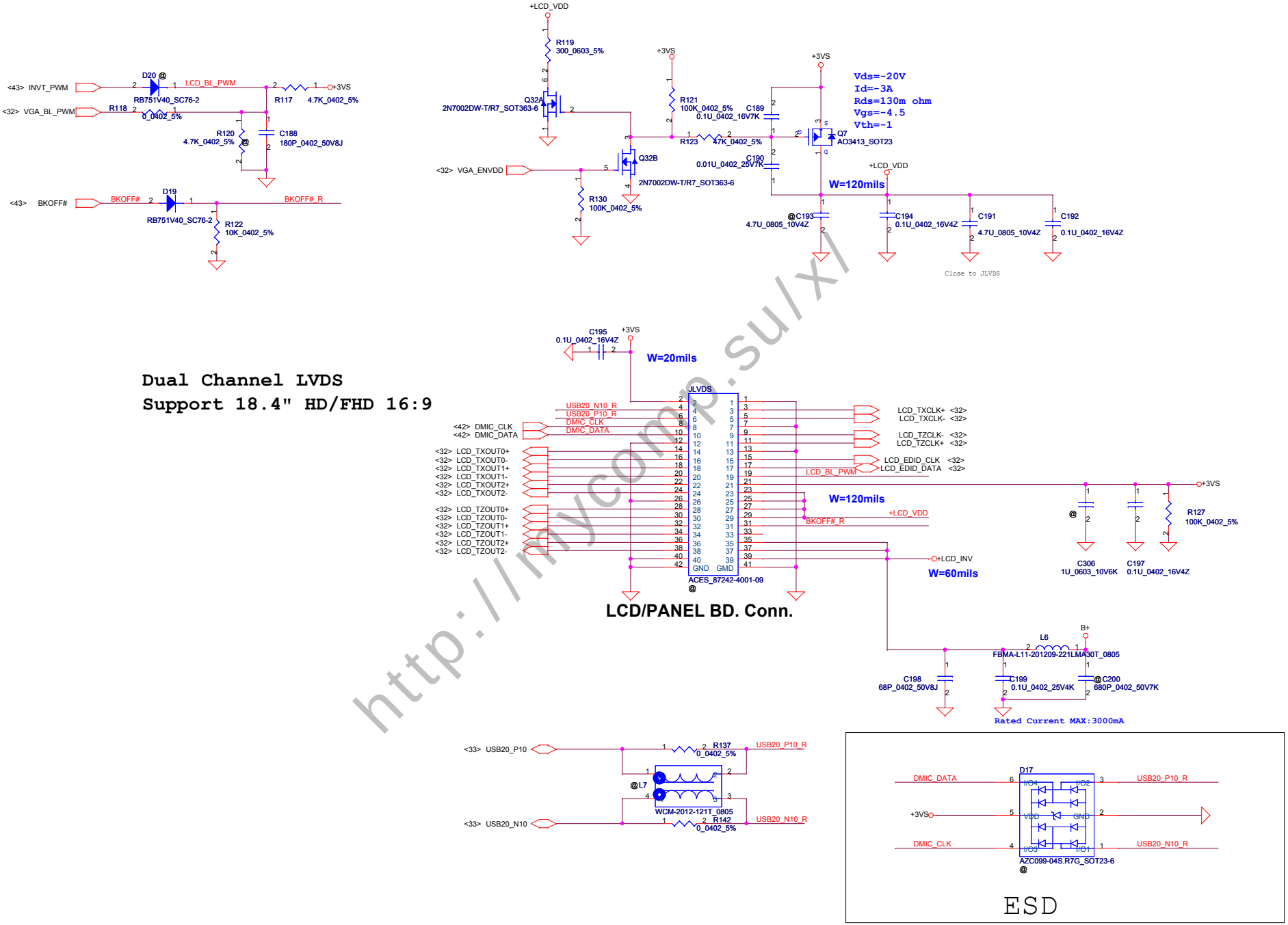


CRT CONNECTOR



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

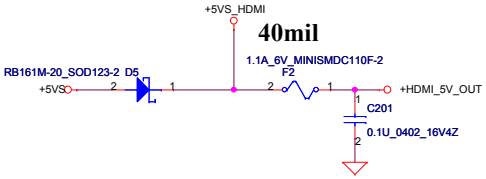
Compal Electronics, Inc.			
Title	CRT		
Size	Document Number	PBL80 LA-7441P M/B	Rev 0.1
Date: Friday, January 21, 2011	Sheet 26 of 58		

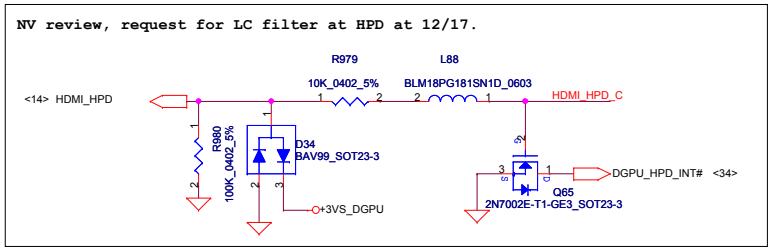


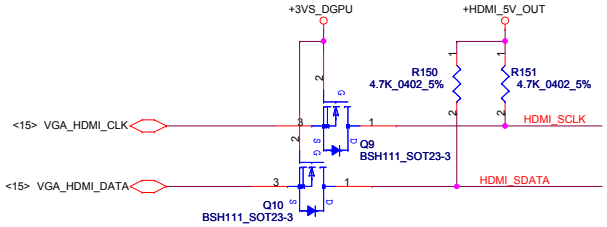
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

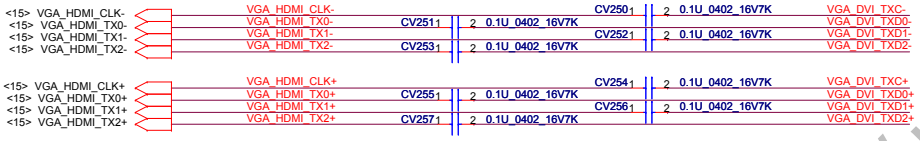
Compal Electronics, Inc.			
Title	LVDS		
Size	Document Number	PBL80 LA-7441P M/B	Rev 0.1
Date: Friday, January 21, 2011	Sheet 27 of 58		

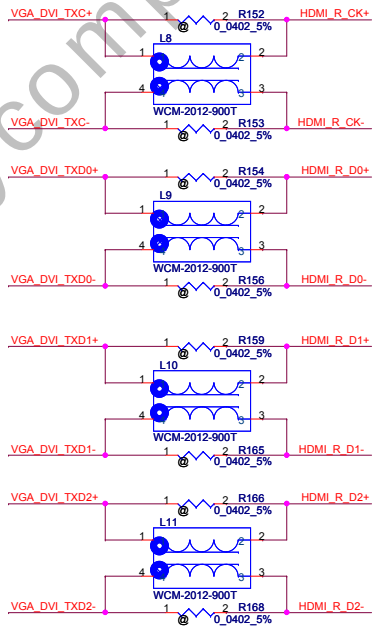
HDMI Connector

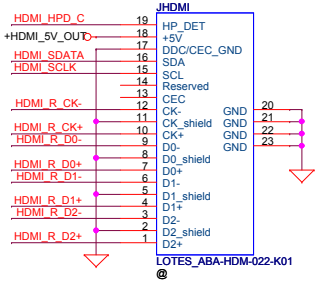


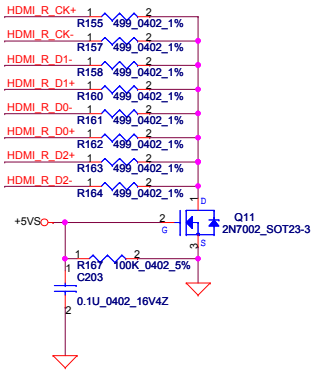


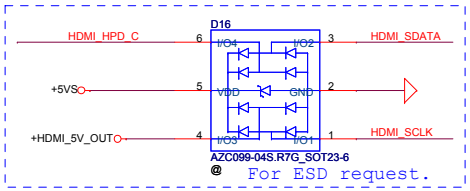


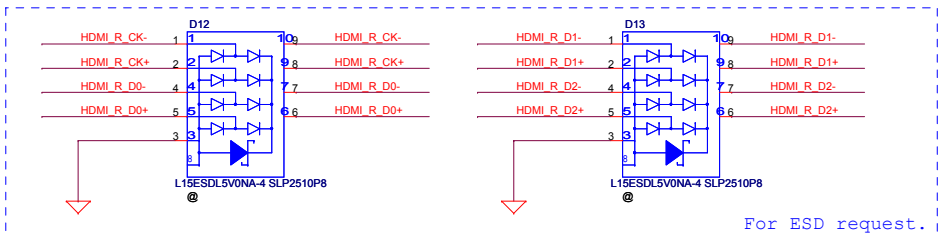












Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1

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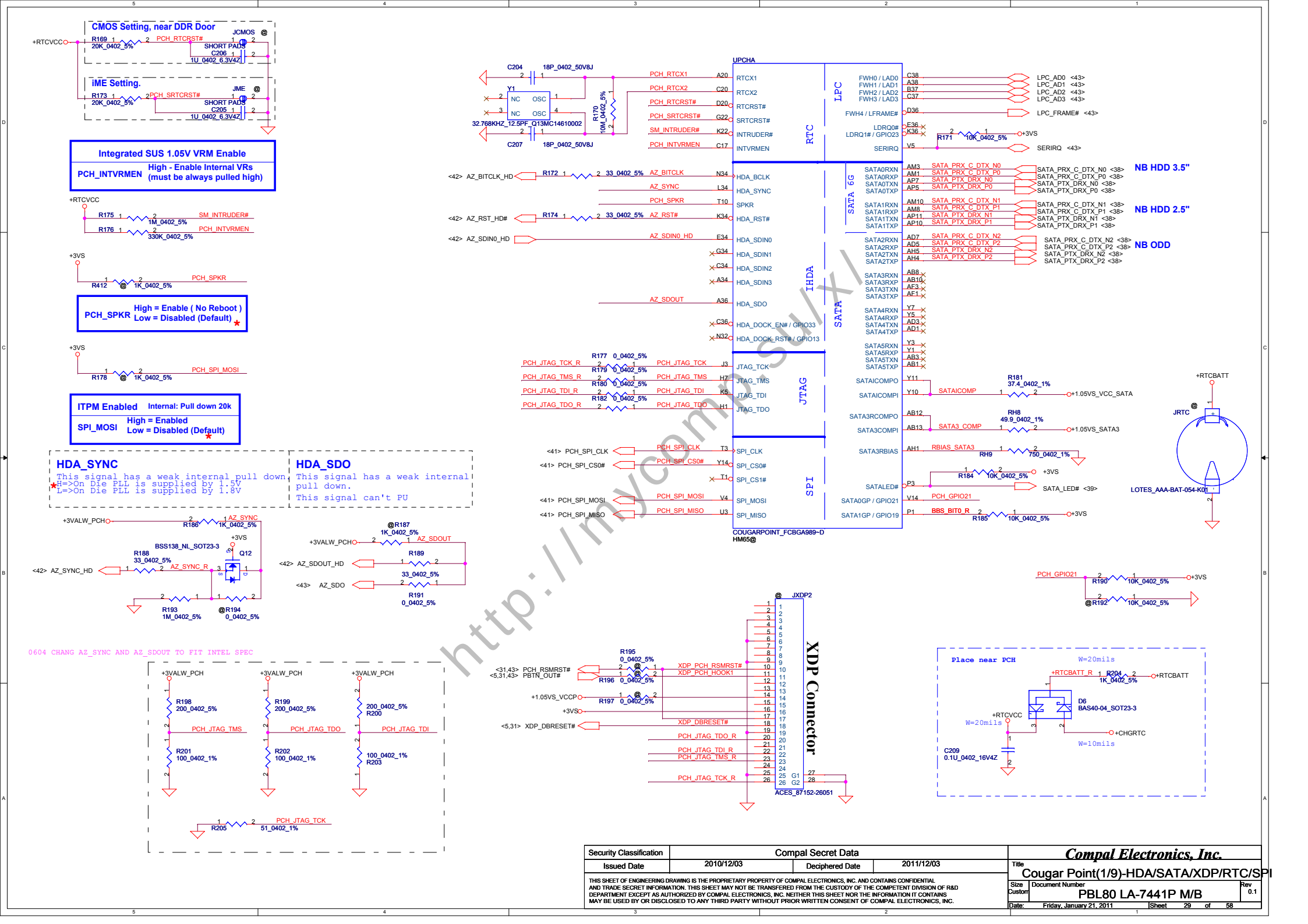
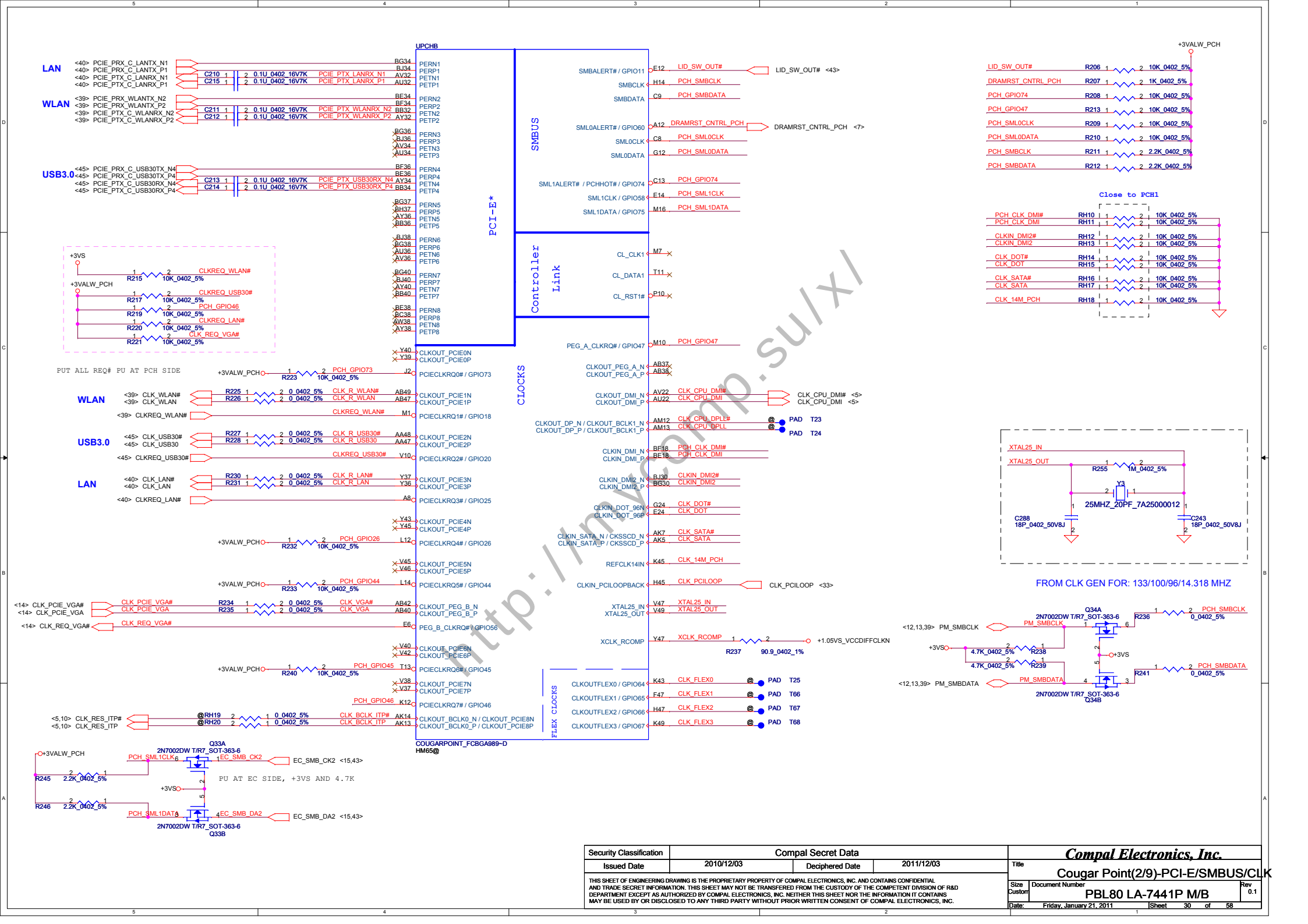




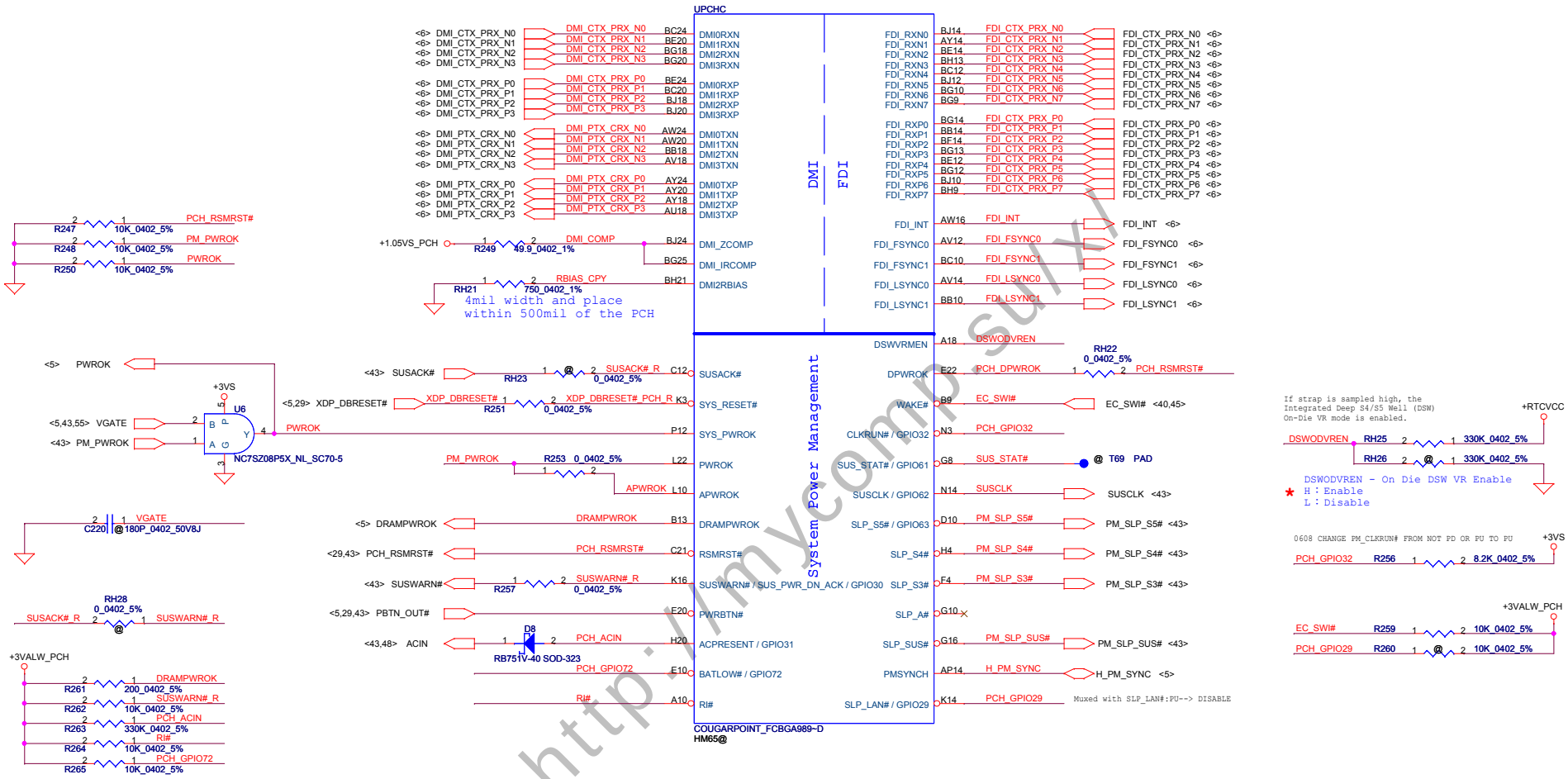
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(2/9)-PCI-E/SMBUS/CLK

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 30 of 58



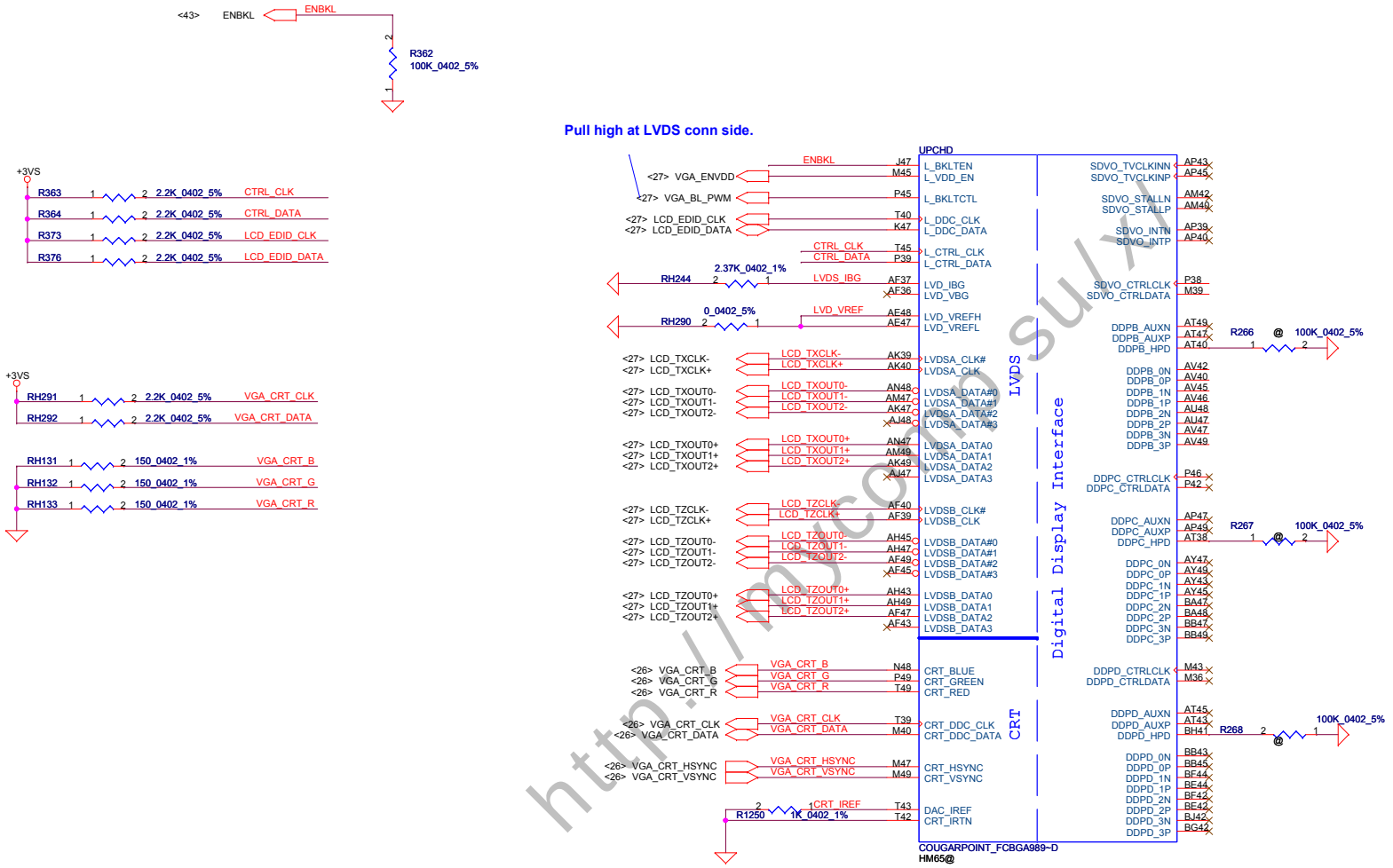
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(3/9)-DMI/FDI/PWM

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 31 of 58



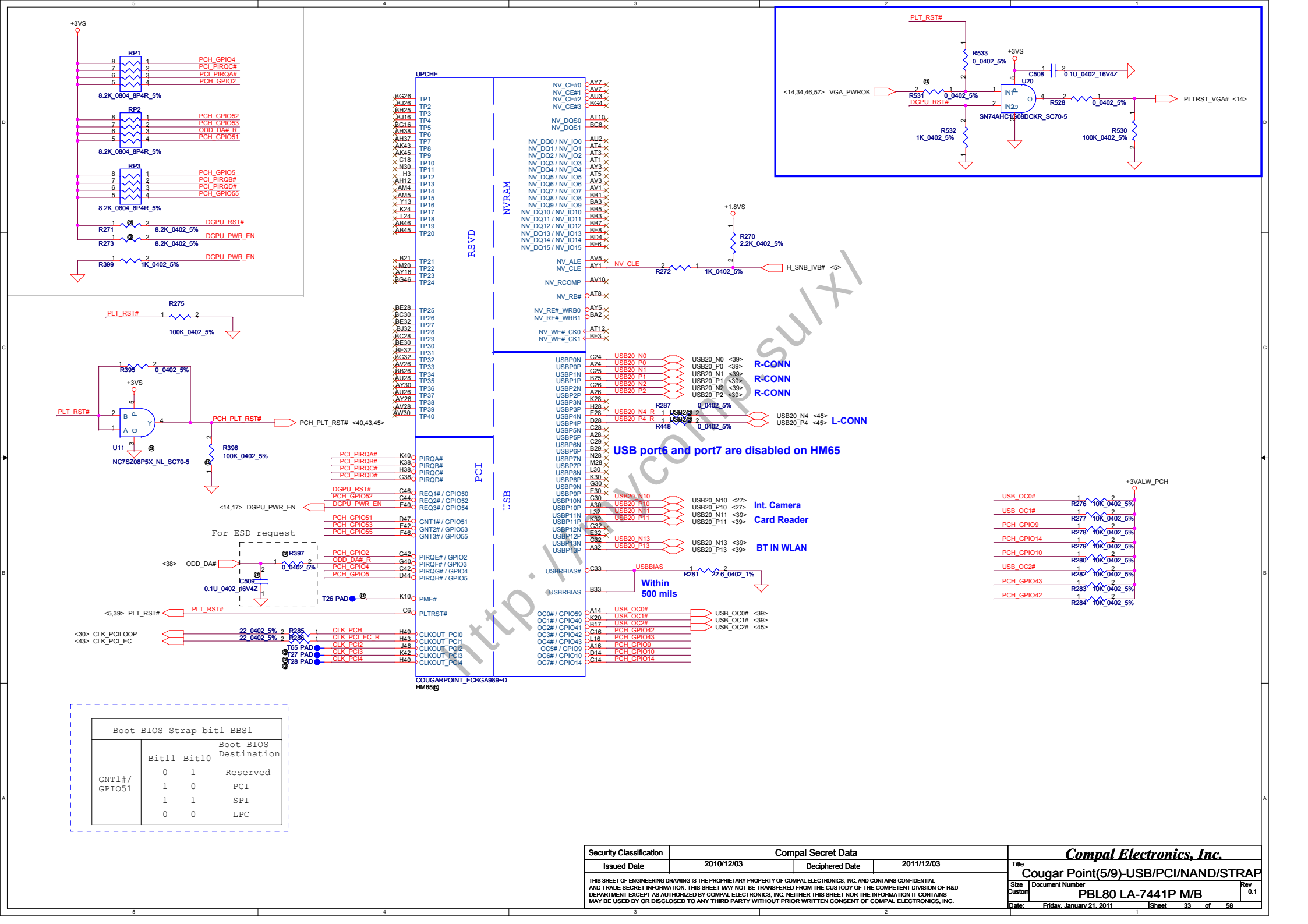
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(4/9)-CRT/LVDS/HDMI/DP

Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 32 of 58



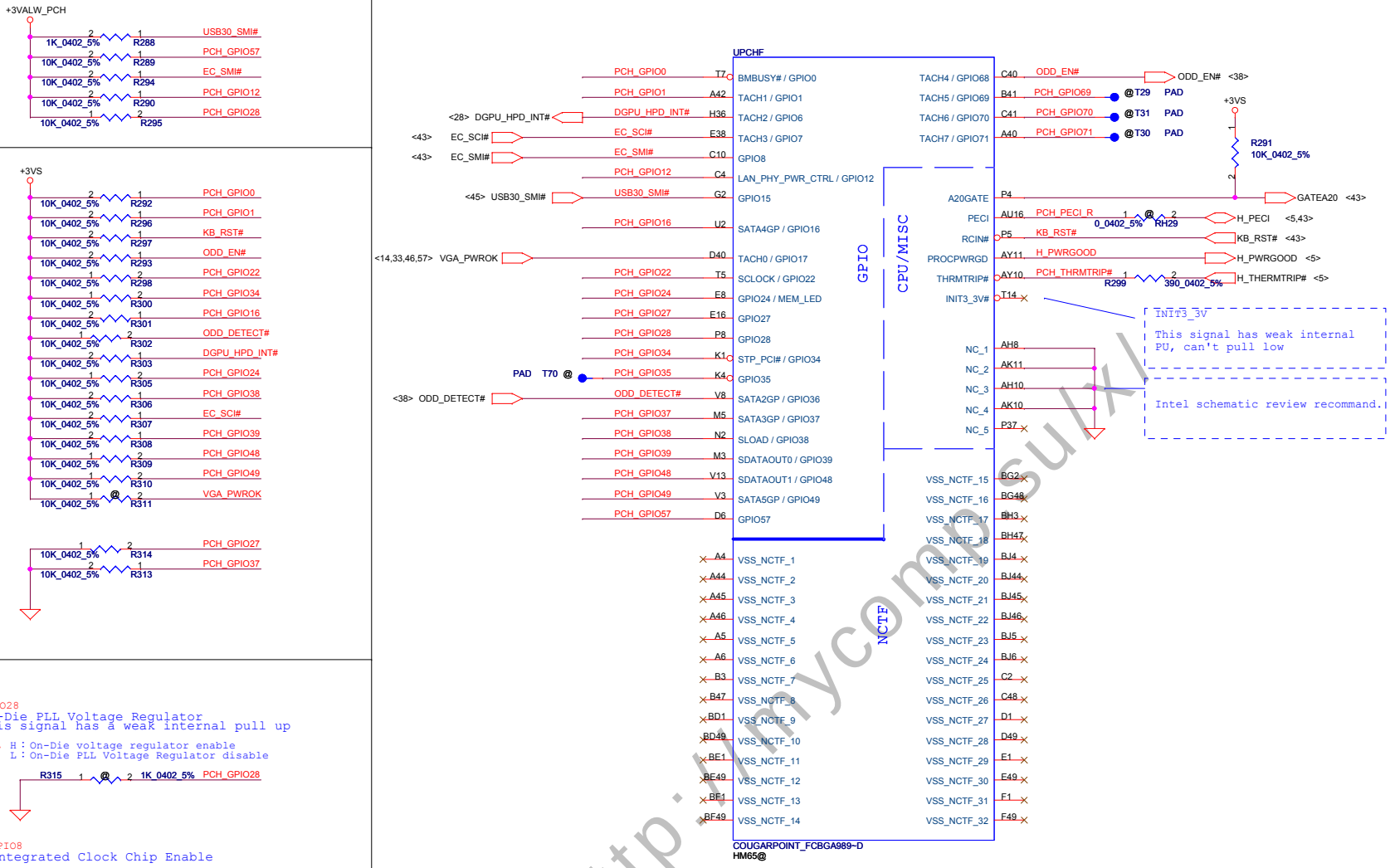
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(5/9)-USB/PCI/NAND/STRAP

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 33 of 58



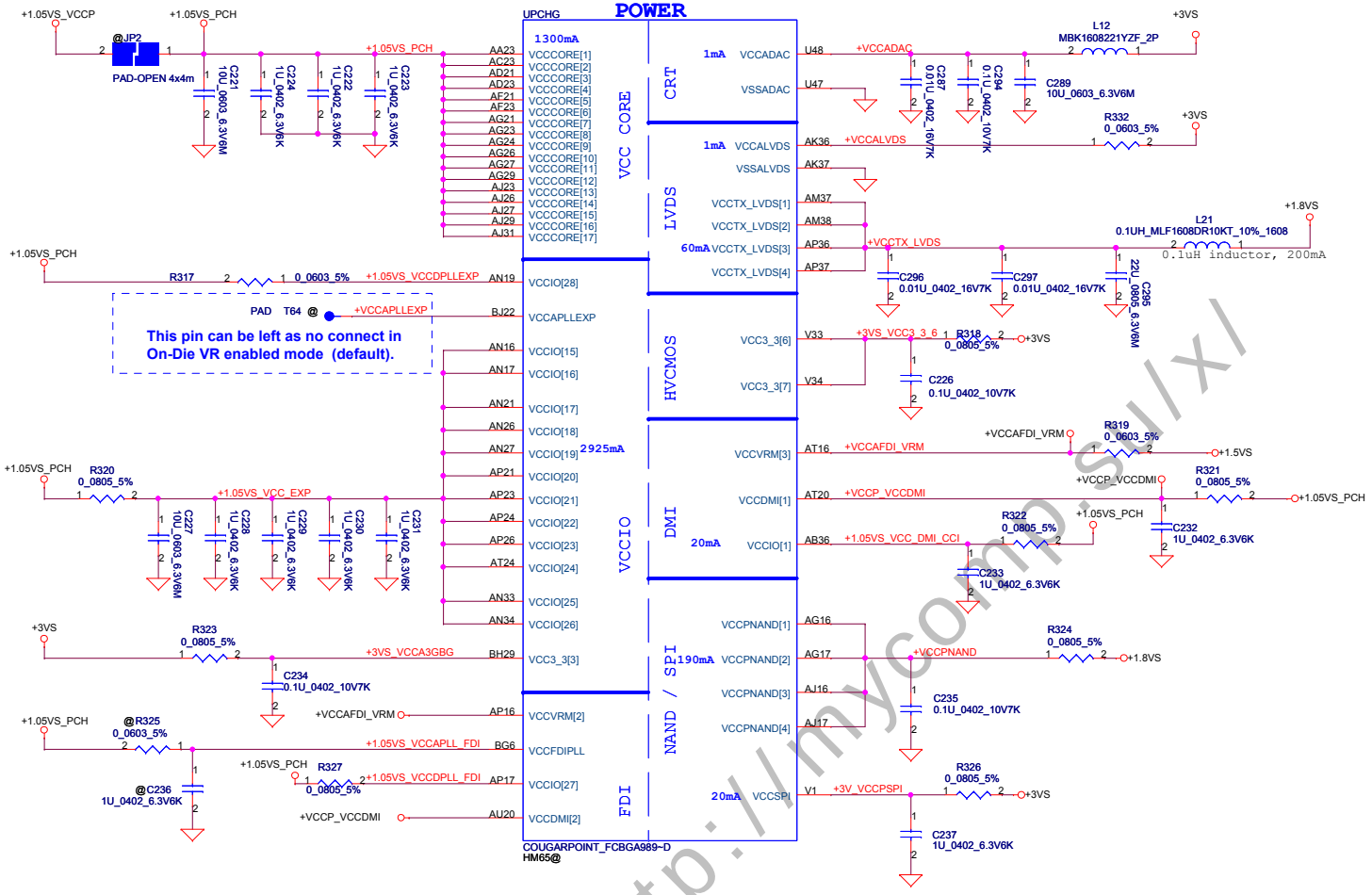
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(6/9)-CPU/GPIO/MISC

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 34 of 58



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: Cougar Point(7/9)-PWR1

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

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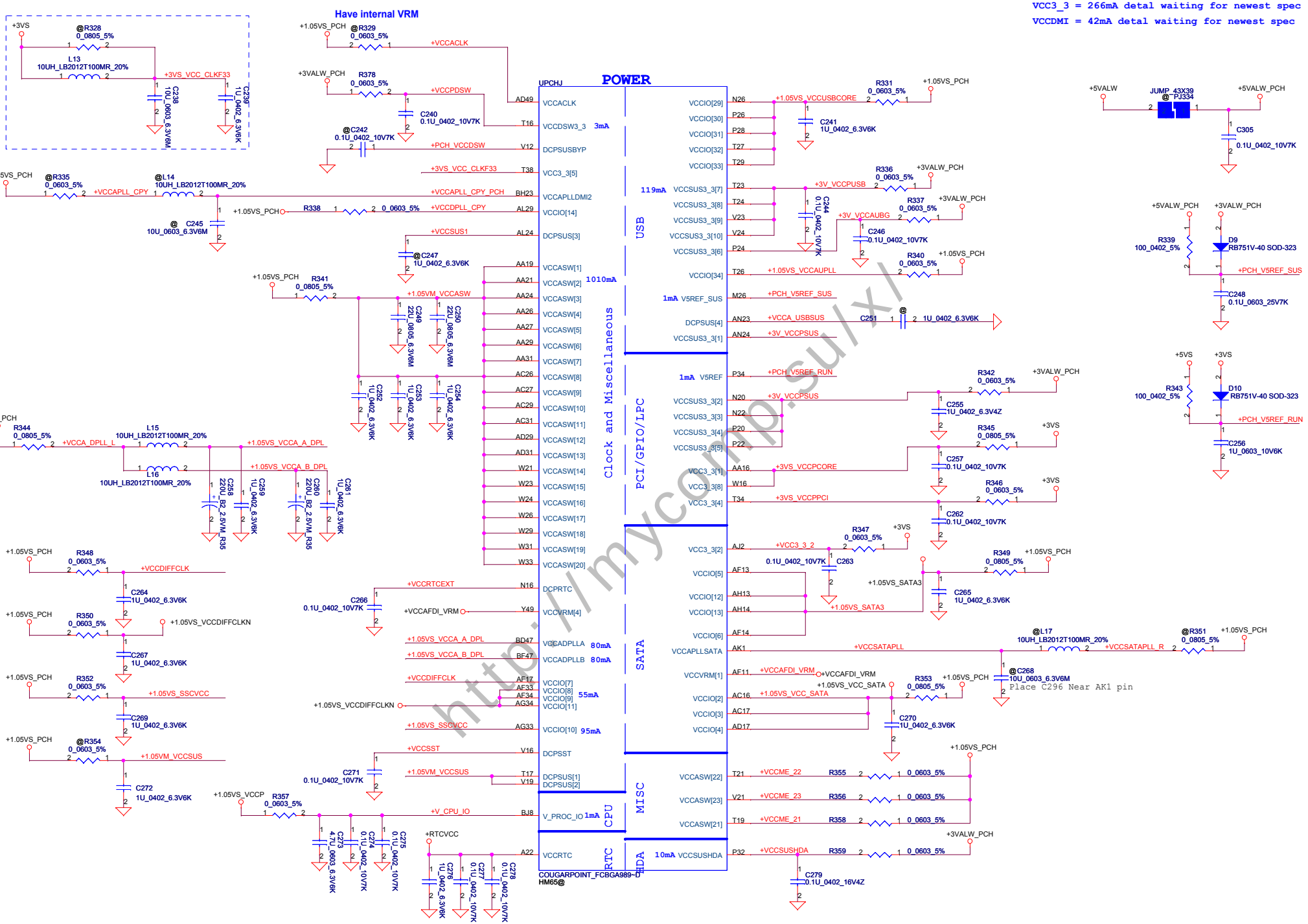
VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

Have internal VRM

POWER



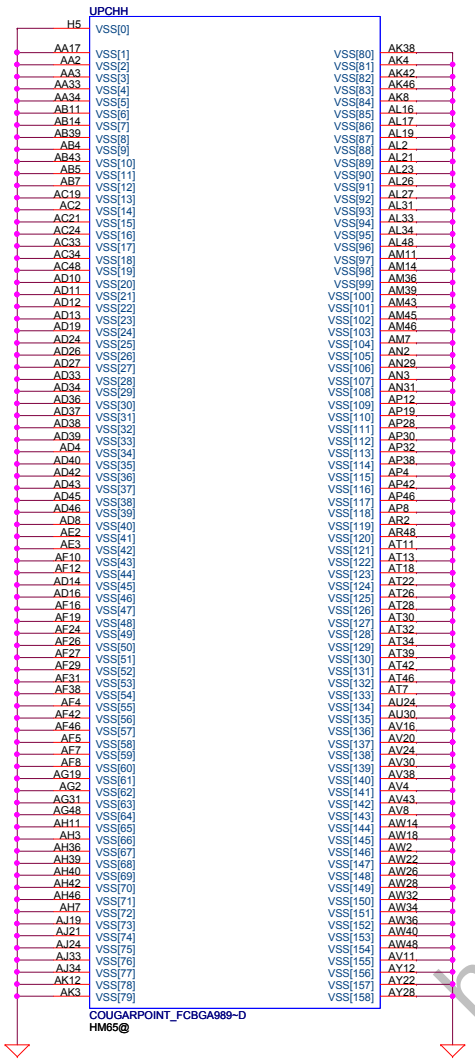
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

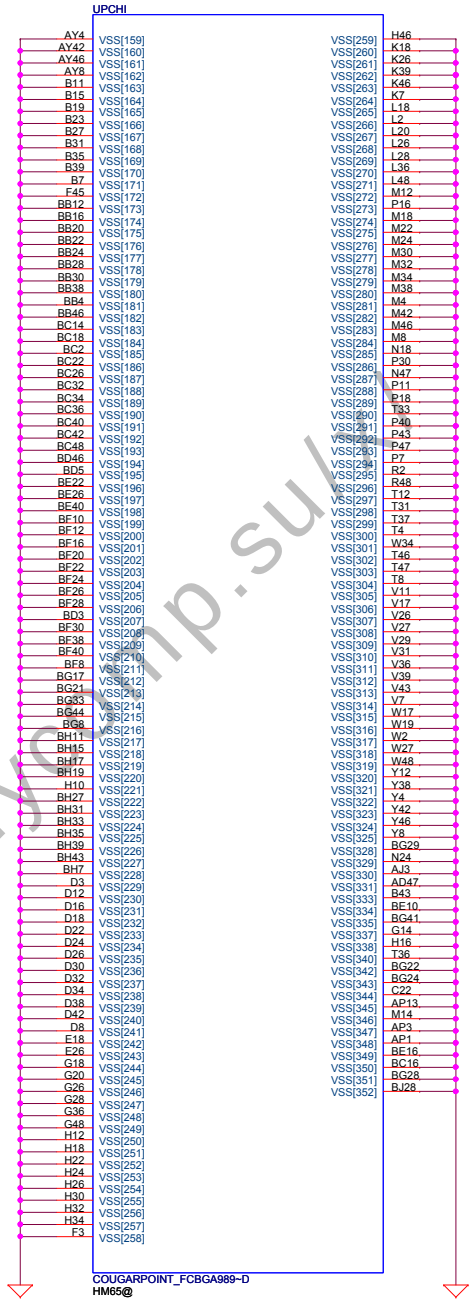
Compal Electronics, Inc.

Title: Cougar Point(8/9)-PWR2

Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 36 of 58





Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

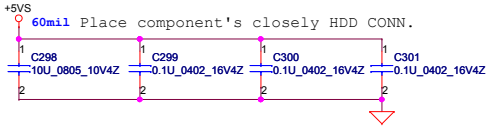
Compal Electronics, Inc.

Title: Cougar Point(9/9)-GND

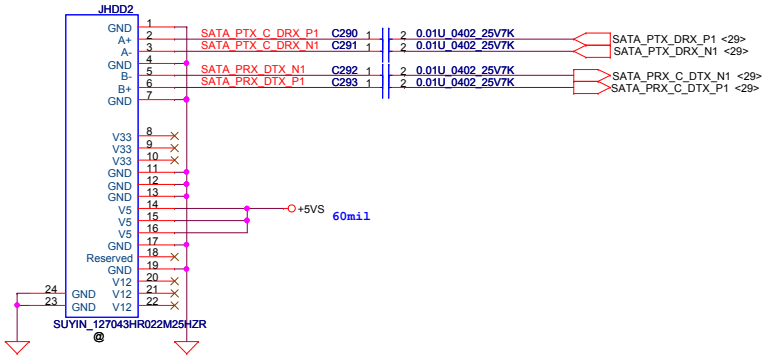
Size: Custom | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 37 of 58

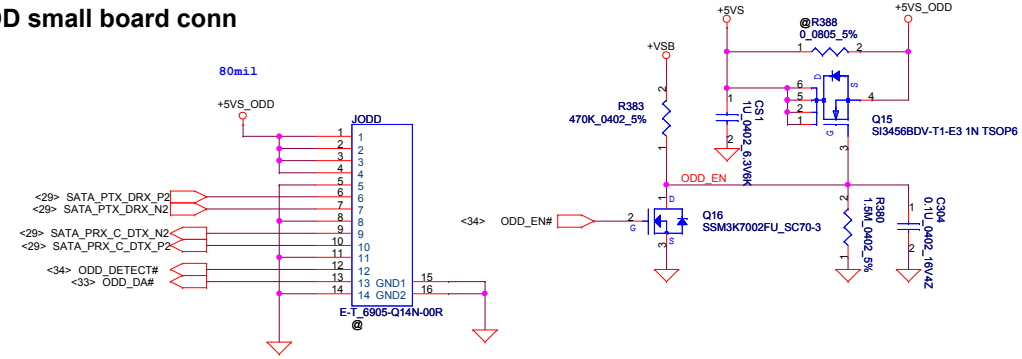
SATA HDD 2.5" Conn.



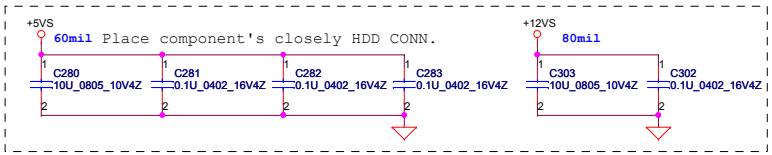
HDD



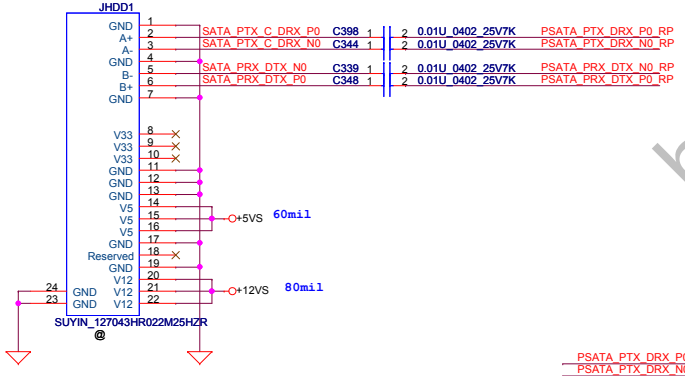
ODD small board conn



SATA HDD 3.5" Conn.

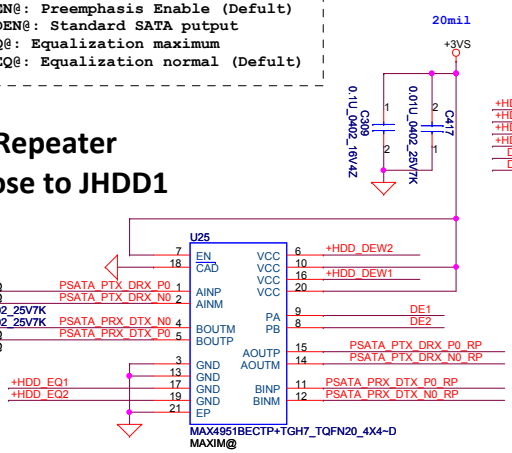


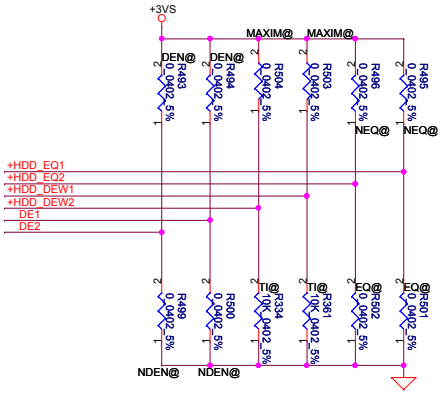
HDD



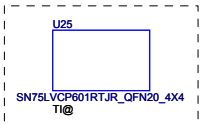
MAXIM@: MAX4951BECTP+TGH7 (Defult)
TI@: SN75LVCP601TJR
DEN@: Preemphasis Enable (Defult)
NDEN@: Standard SATA putput
EQ@: Equalization maximum
NEQ@: Equalization normal (Defult)

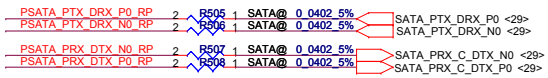
HDD Repeater
All close to JHDD1





Note: +HDD_DEW1, +HDD_DEW2, +HDD_EQ1, +HDD_EQ2 need to route 10 mils





Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: SATA-HDD&ODD/B

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

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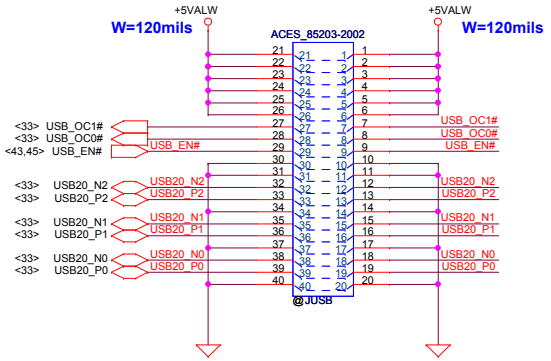
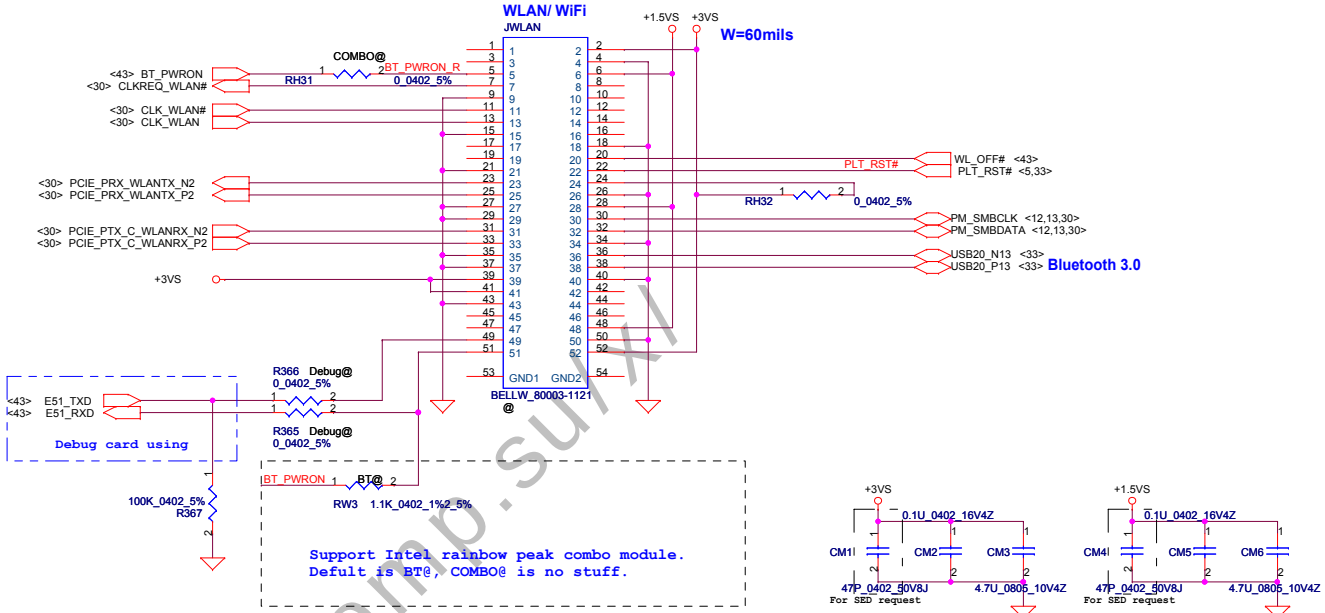
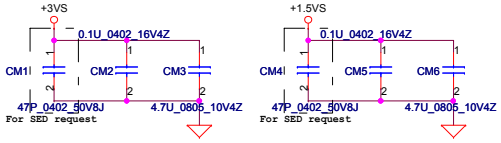
USB/B
Right USB X 3

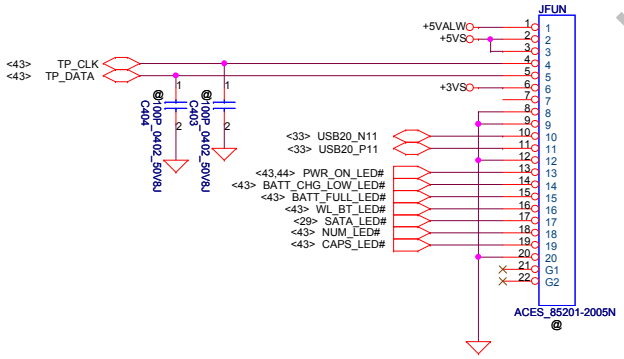


Slot 1 Half PCIe Mini Card-WLAN & BT3.0

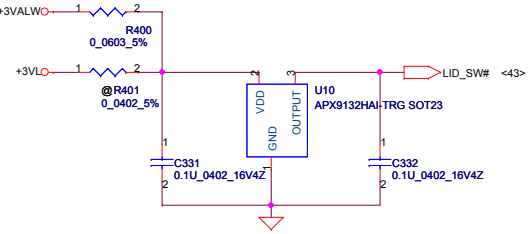




Touch pad & LID &
Card Reader & LED small board Connector

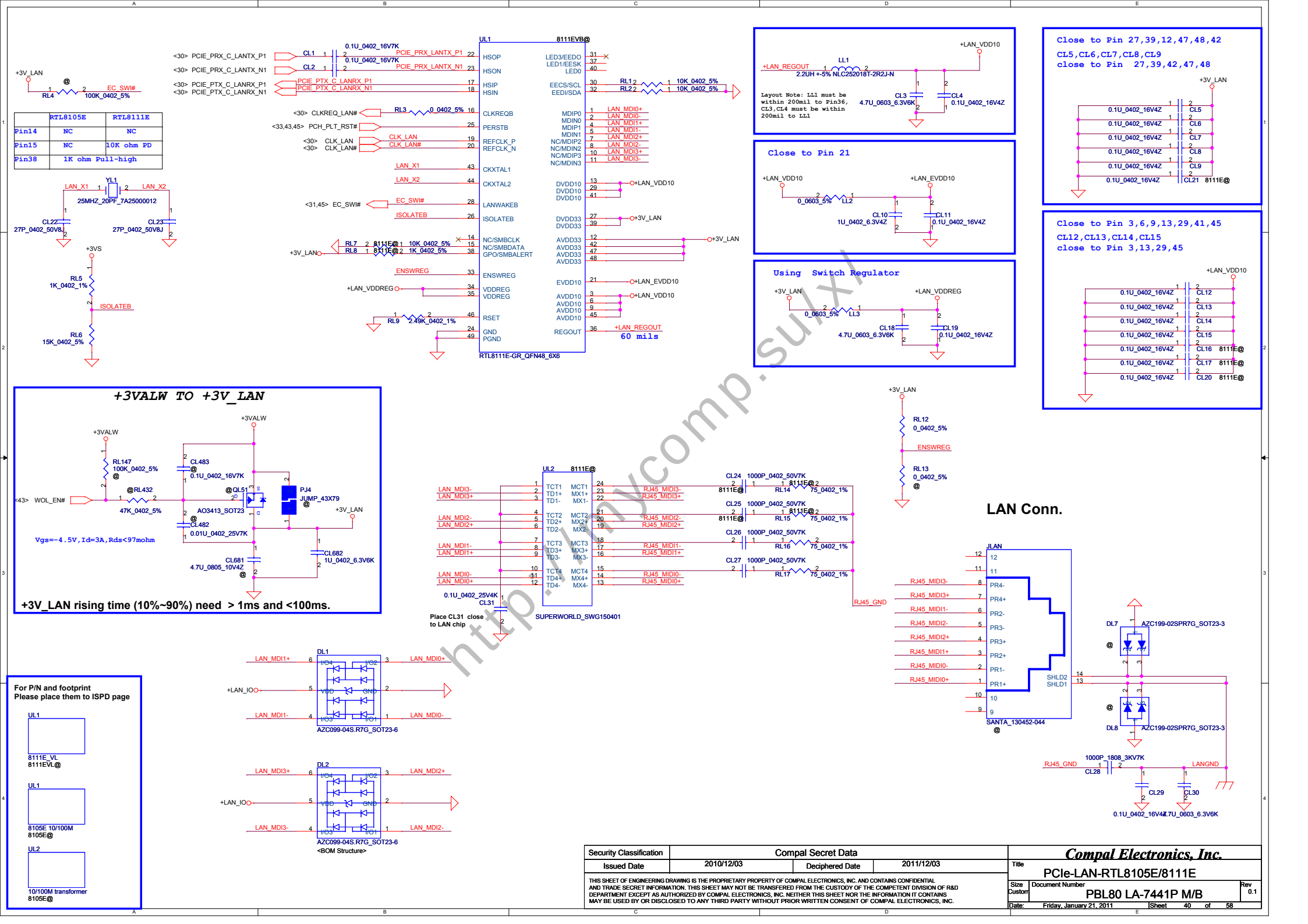


Lid SW



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.			
Title	USB/B&TP/LED/CR/B&LID&PCIe-WLAN		
Size	Document Number		Rev
	PBL80 LA-7441P M/B		0.1
Date: Friday, January 21, 2011	Sheet 39 of 58		



BIOS Bus switch

SPI ROM For Basic ME ROM size 4MByte

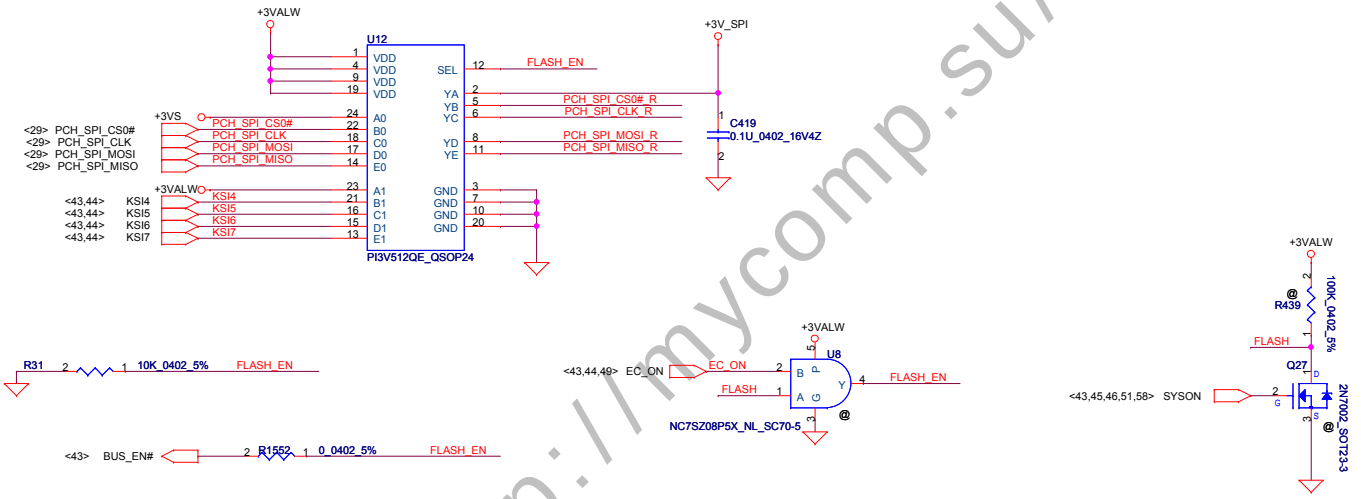
1. When Flash EC ROM.
   KSO2 to Low (Test mode)
   KSO3 to Low (ISP mode)---------FDA mode
   EC_ON->Low, BUS_EN#->Low
   U11 : Y->A0, PCH to BIOS ROM.
   KSI4,5,6,7 direct to EC_SPI

2. When Flash BIOS ROM.
   KSO2 to High
   KSO3 to Low (ISP mode)
   EC_ON->High, BUS_EN#->High.
   U11 : Y->A1, KSI4,5,6,7 to BIOS ROM.
   +3V_SPI from +3VALW
   Set EC pin KSI4,5,6,7 to HiZ.

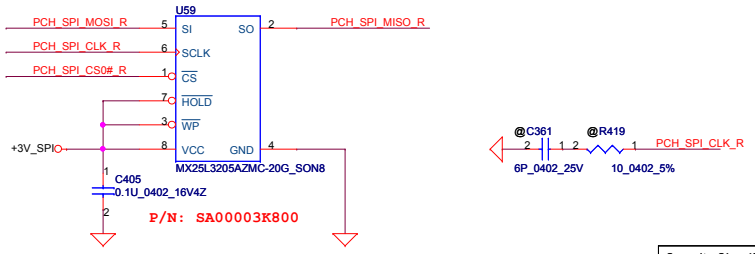
3.When normal operation.
   EC_ON->High , BUS_EN#->Low.
   U11 : Y->A0, PCH direct to BIOS ROM.
   +3V_SPI from +3VS.

4. When enter S3,4
   EC_ON->High, BUS_EN#->Low.
   U11 : Y->A1, PCH direct to BIOS ROM.
   But +3V_SPI from +3VS is no power.

** BUS_EN# only high when test mode.
   And must make sure it's low when FDA mode.
   Or HW use 10K pull down to GND.



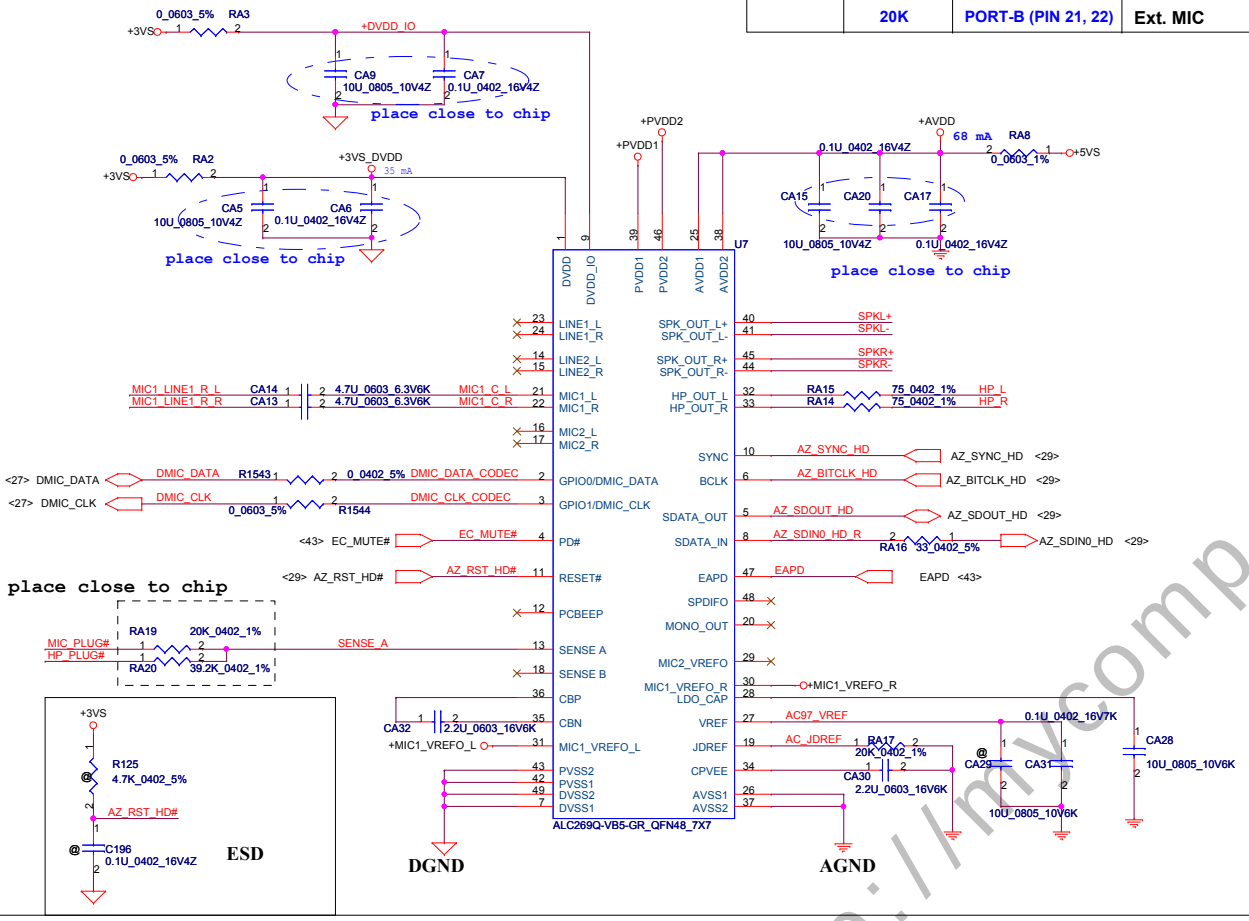
BIOS SPI Flash (4MByte*1)

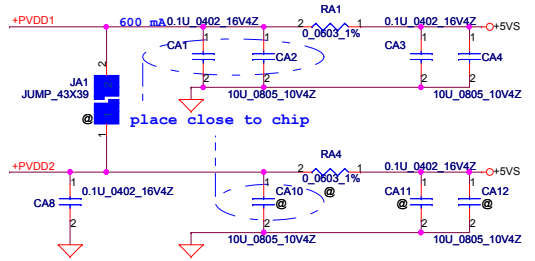


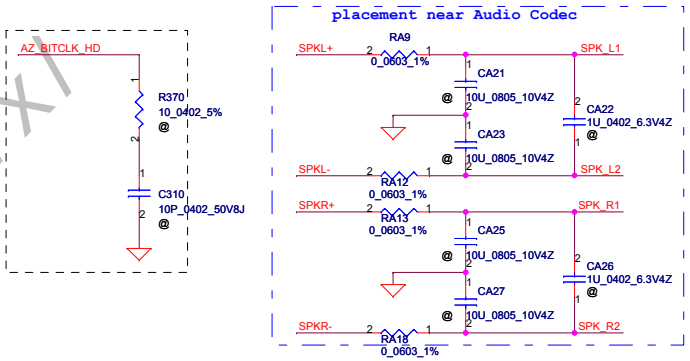
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.		
Title: Bus switch&BIOSROM		
Size	Document Number: PBL80 LA-7441P M/B	Rev: 0.1
Date: Friday, January 21, 2011	Sheet 41 of 58	

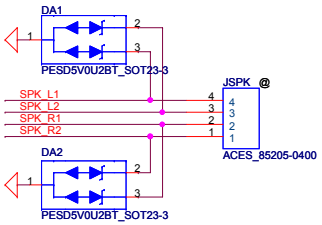
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC

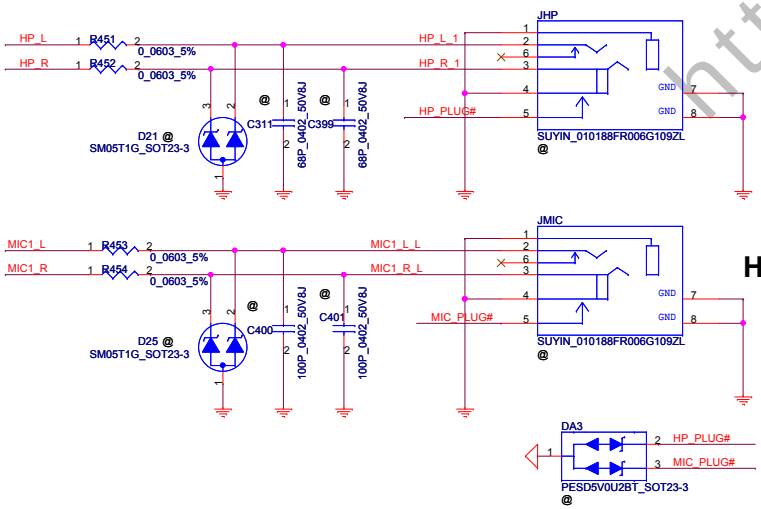






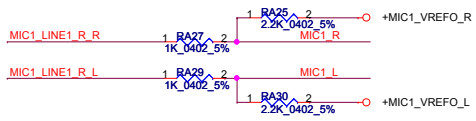
SPEAKER CONN

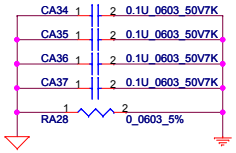




HP CONN & MIC CONN

Ext.MIC/LINE IN JACK





Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: HD CODEC ALC269

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

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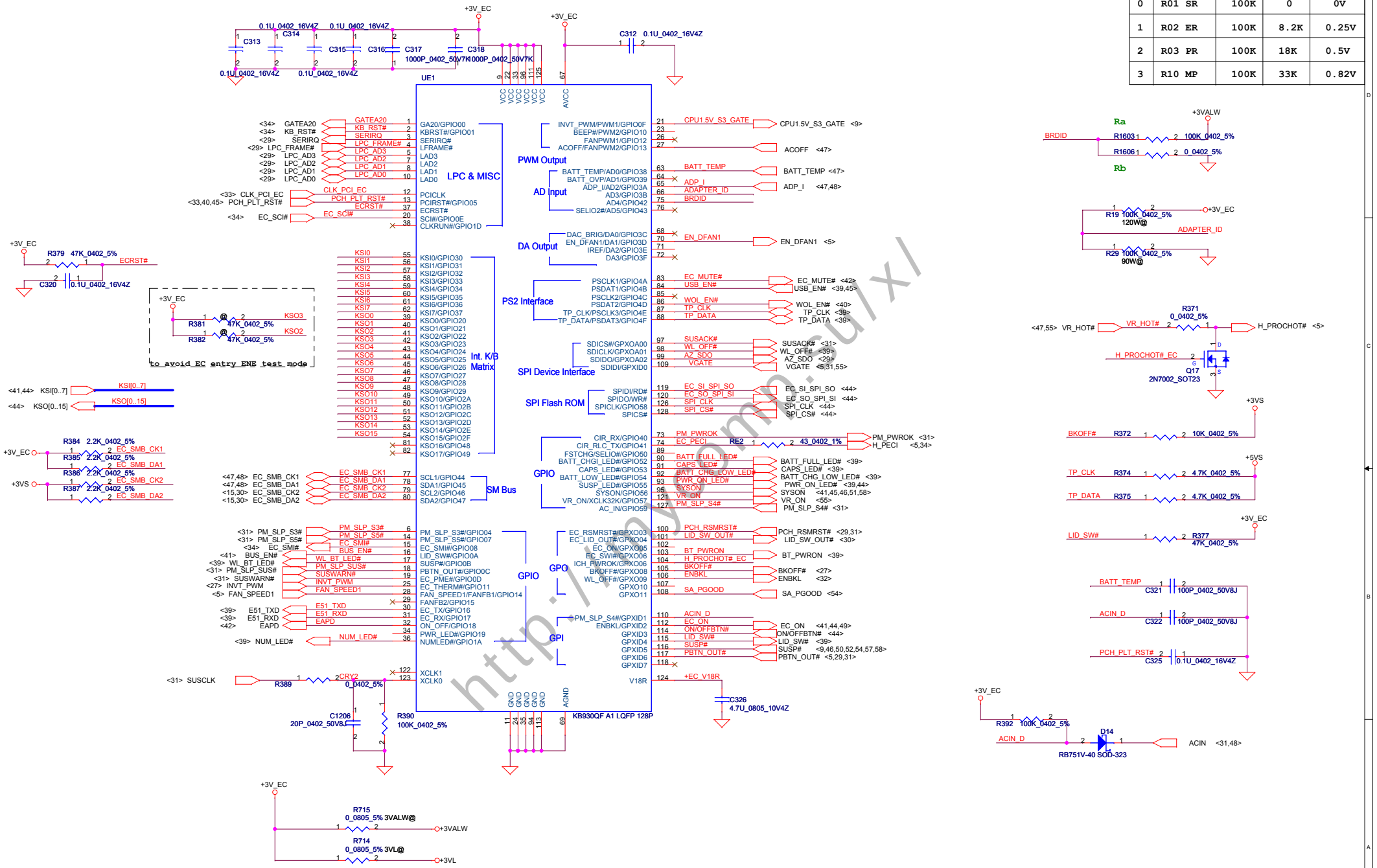
ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V

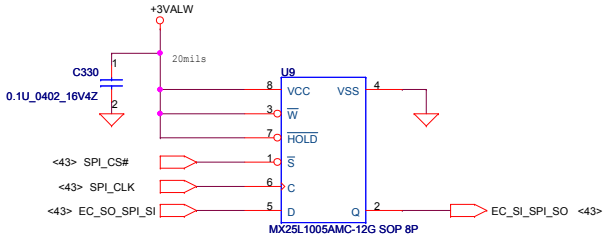


Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

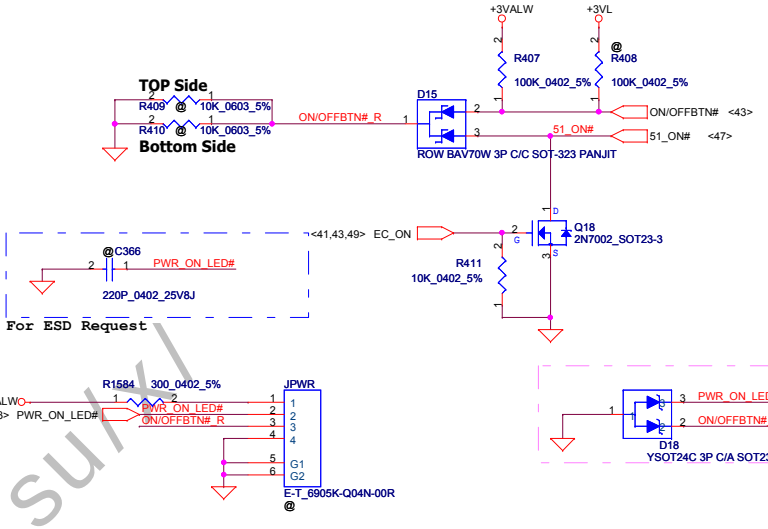
Title	ENE-KB930
Size	Document Number: PBL80 LA-7441P M/B
Rev	0.1
Date:	Friday, January 21, 2011
Sheet	43 of 58

SPI Flash (1MByte*1)

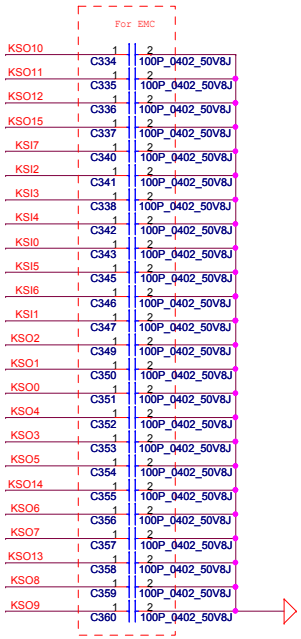


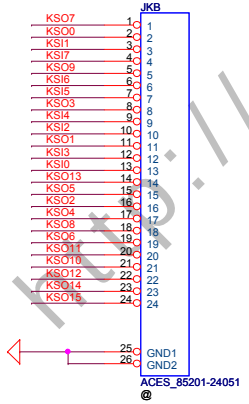
P/N :SA00003GK00 & SA00003GM10

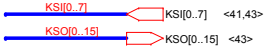
Power Button/ PWR/B



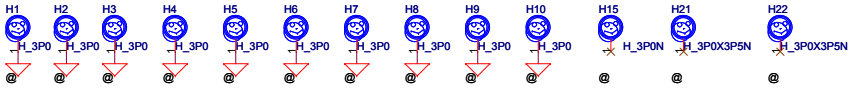
KEYBOARD CONN.



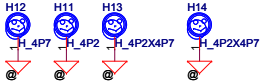




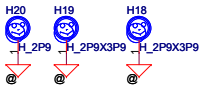
Screw Hole



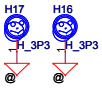
CPU

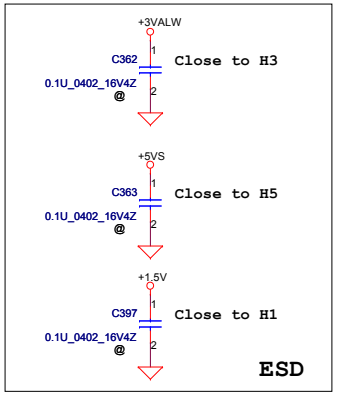


VGA



WLAN

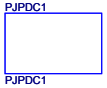




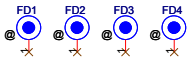
ISPD

PCB

DC-IN



PCB Fedical Mark PAD



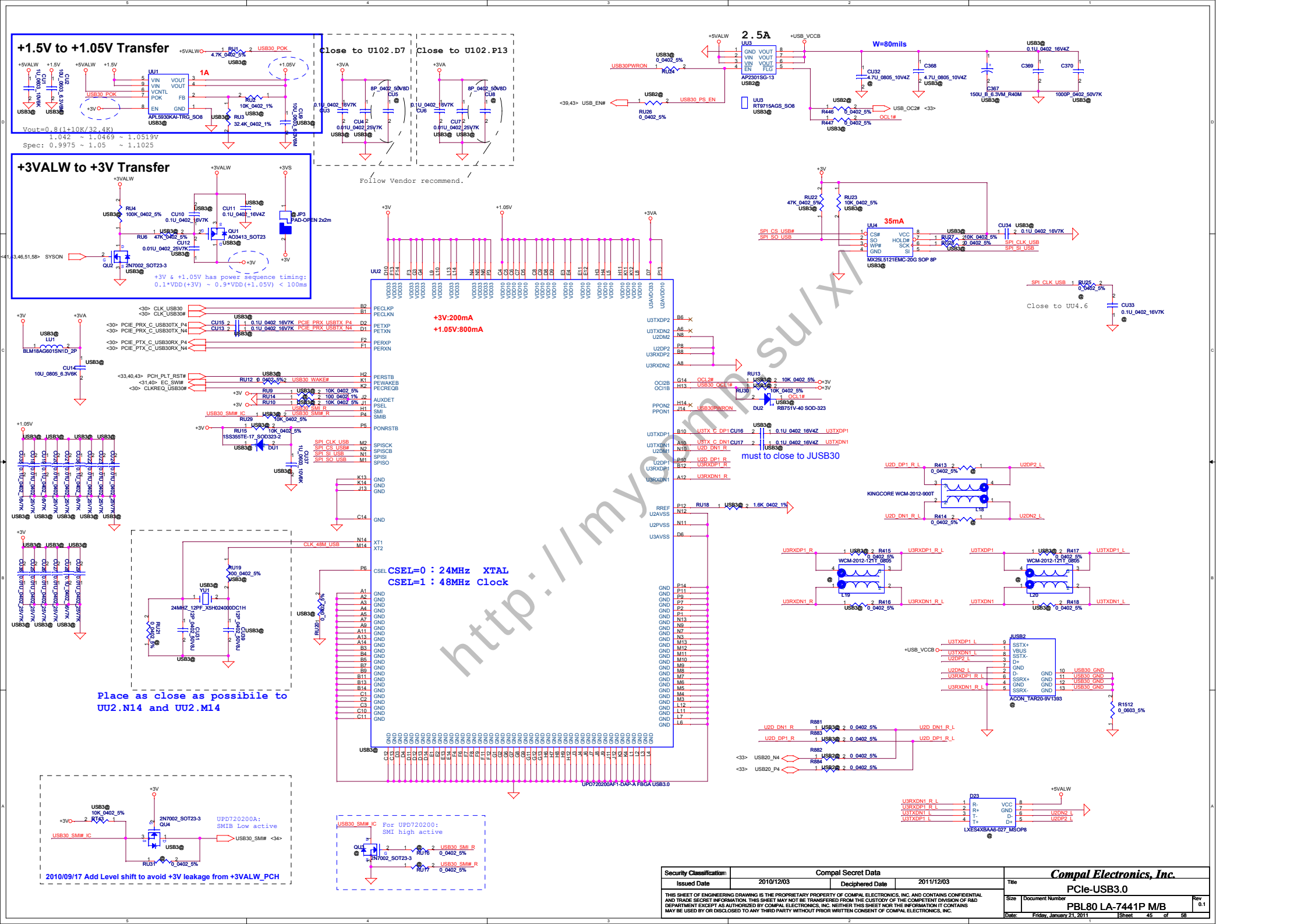
Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: ECROM/KB/PWR/B/SCREW

Size: | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 44 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

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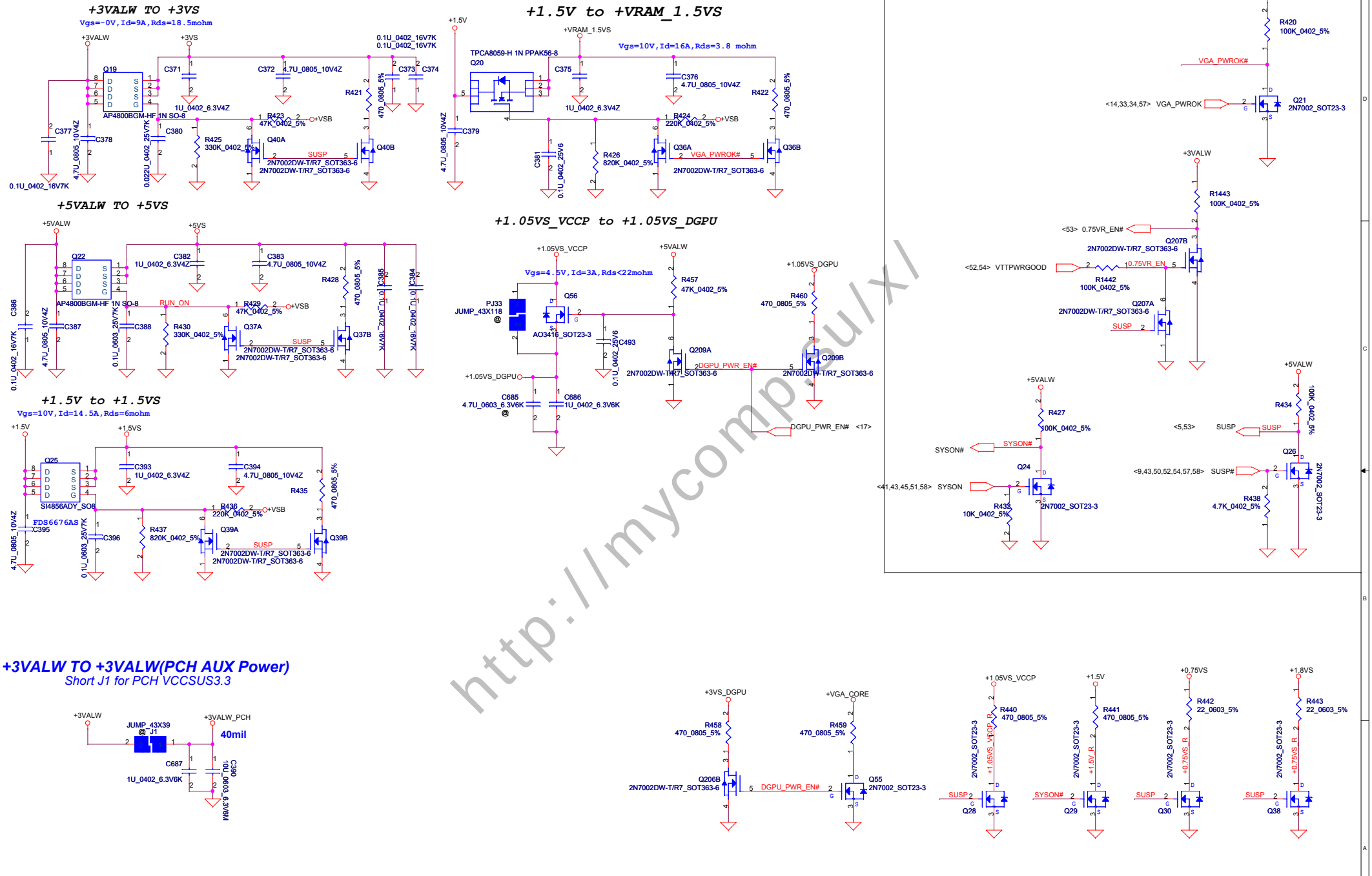
Compal Electronics, Inc.

Title: PCIe-USB3.0

Size | Document Number: PBL80 LA-7441P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 45 of 58



Security Classification	Compal Secret Data		
Issued Date	2010/12/03	Deciphered Date	2011/12/03

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1

Date: Friday, January 21, 2011 Sheet 46 of 58

DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

need confirm: ME give us battery connector P/N is DC040000800

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

If EC use 3VL and can not detect VGATE, must connect EN0

Reserve when EC use +3VL.
Install when EC use +3VALW.

(120mA,40mils ,Via NO.= 1)

3.3V

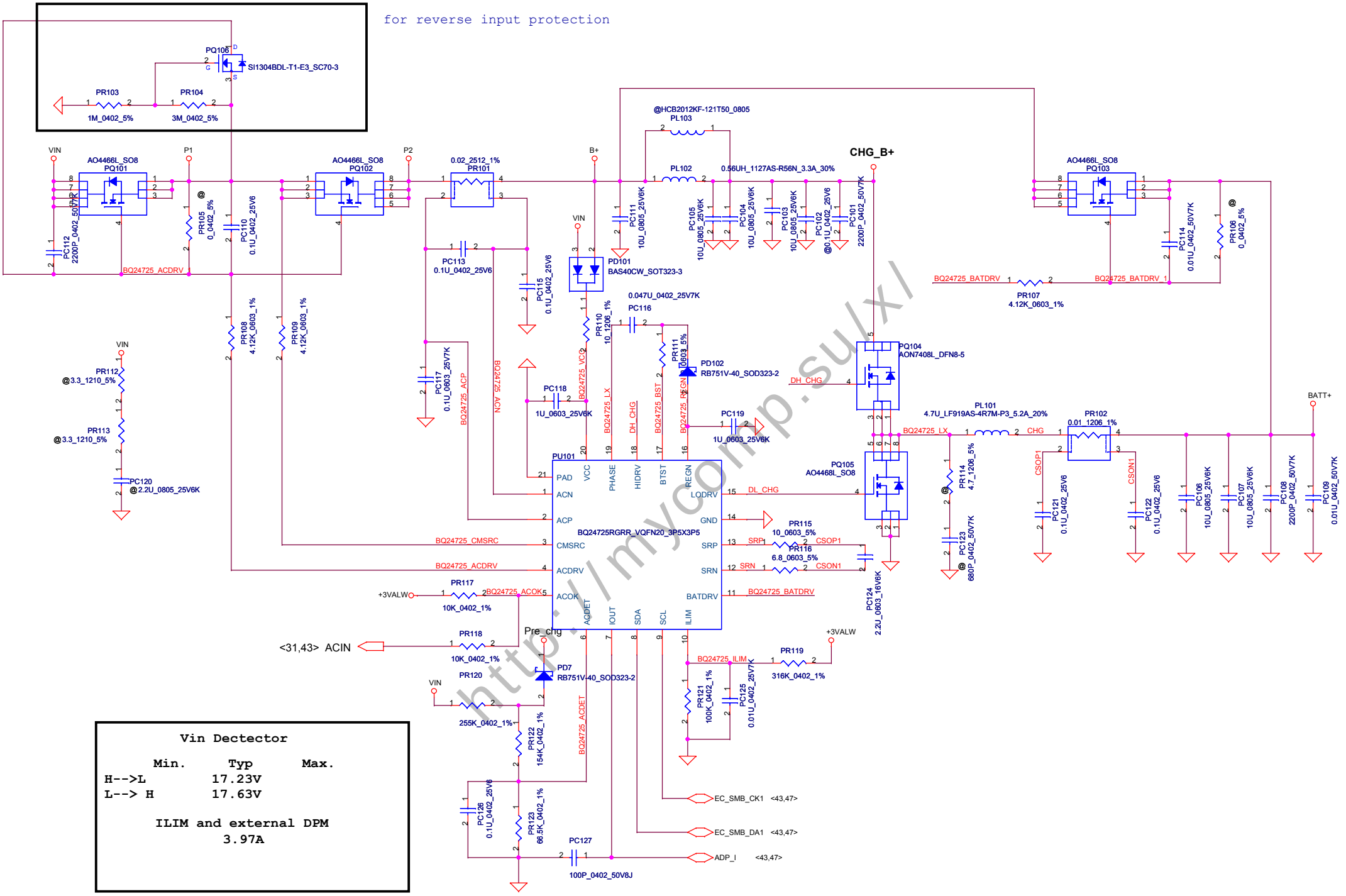
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Friday, January 21, 2011 | Sheet 47 of 58



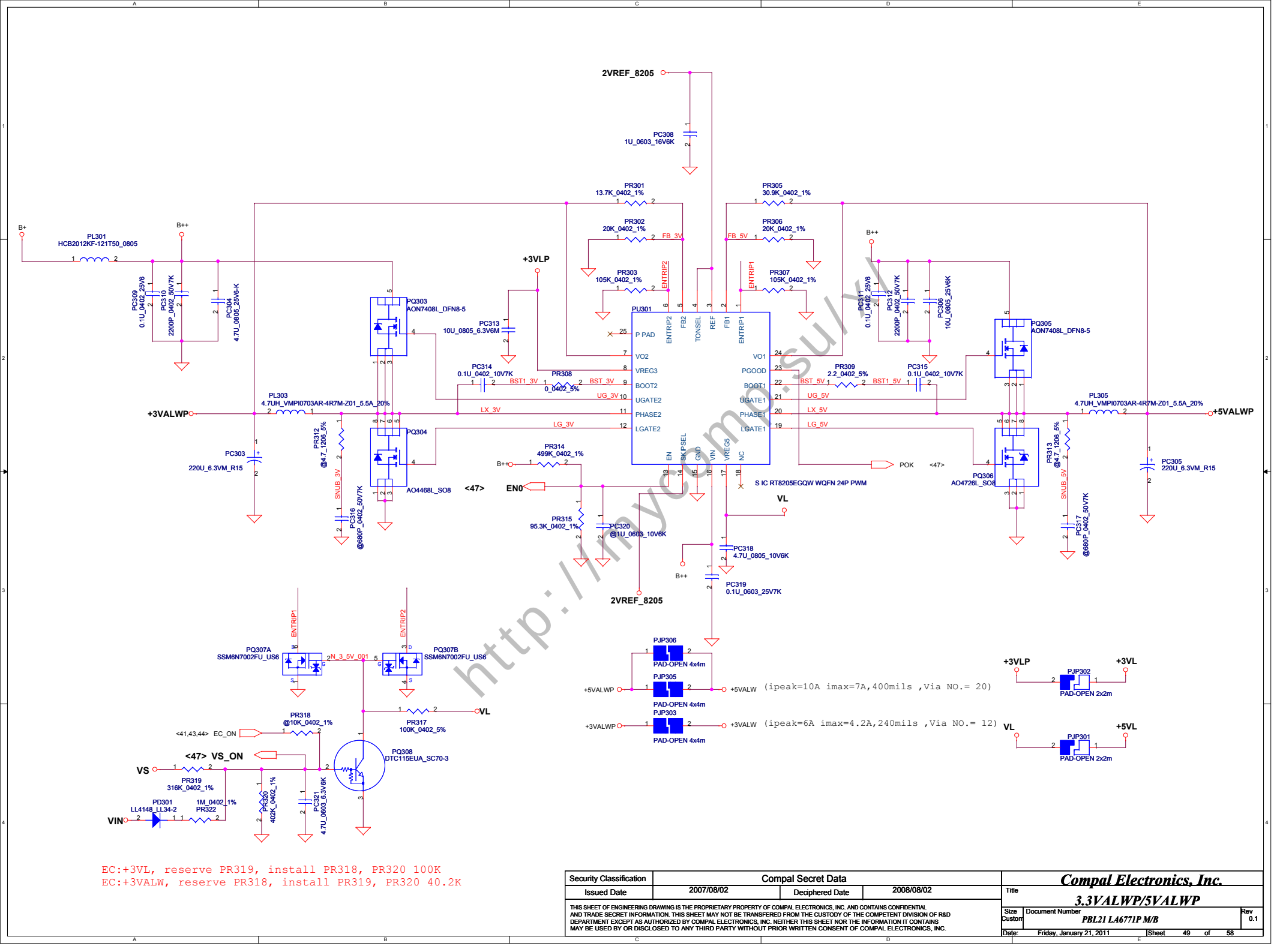
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size	Document Number	Rev
Custom	LA-7221P	0.1

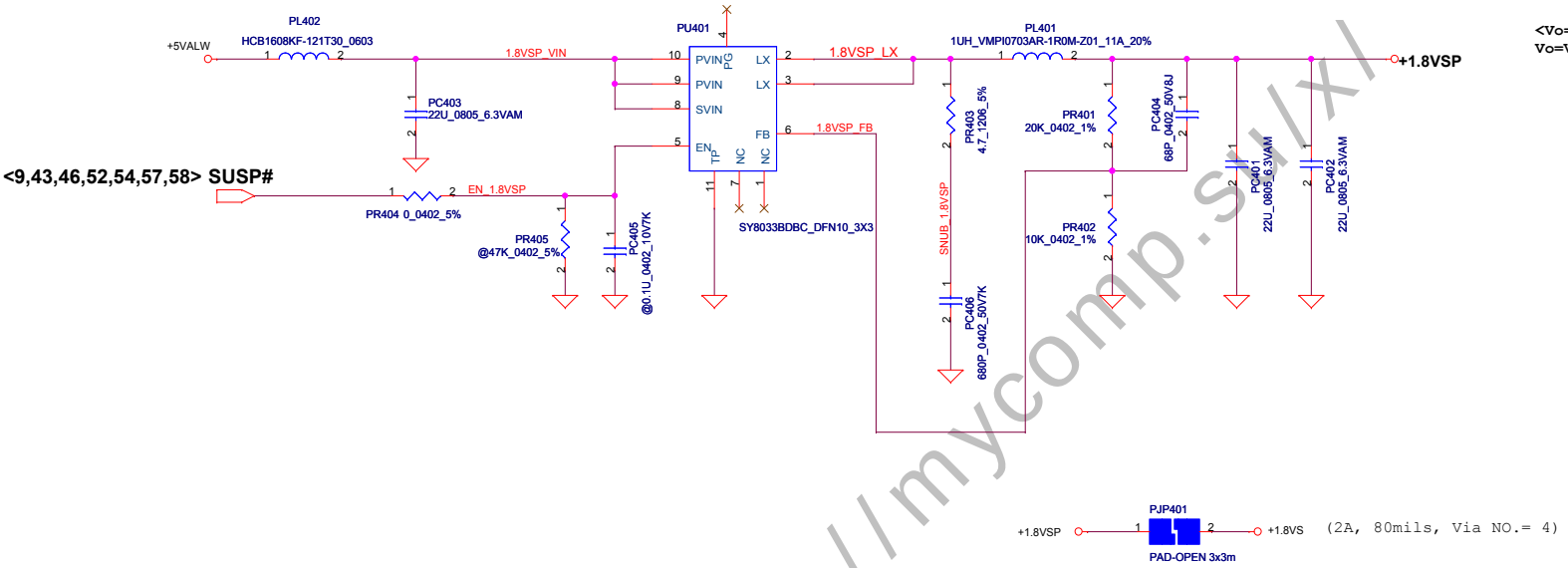
Date: Friday, January 21, 2011 Sheet 48 of 58



EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size: Custom	Document Number: PBL21 LA6771P M/B		Rev: 0.1
Date: Friday, January 21, 2011	Sheet 49 of 58		



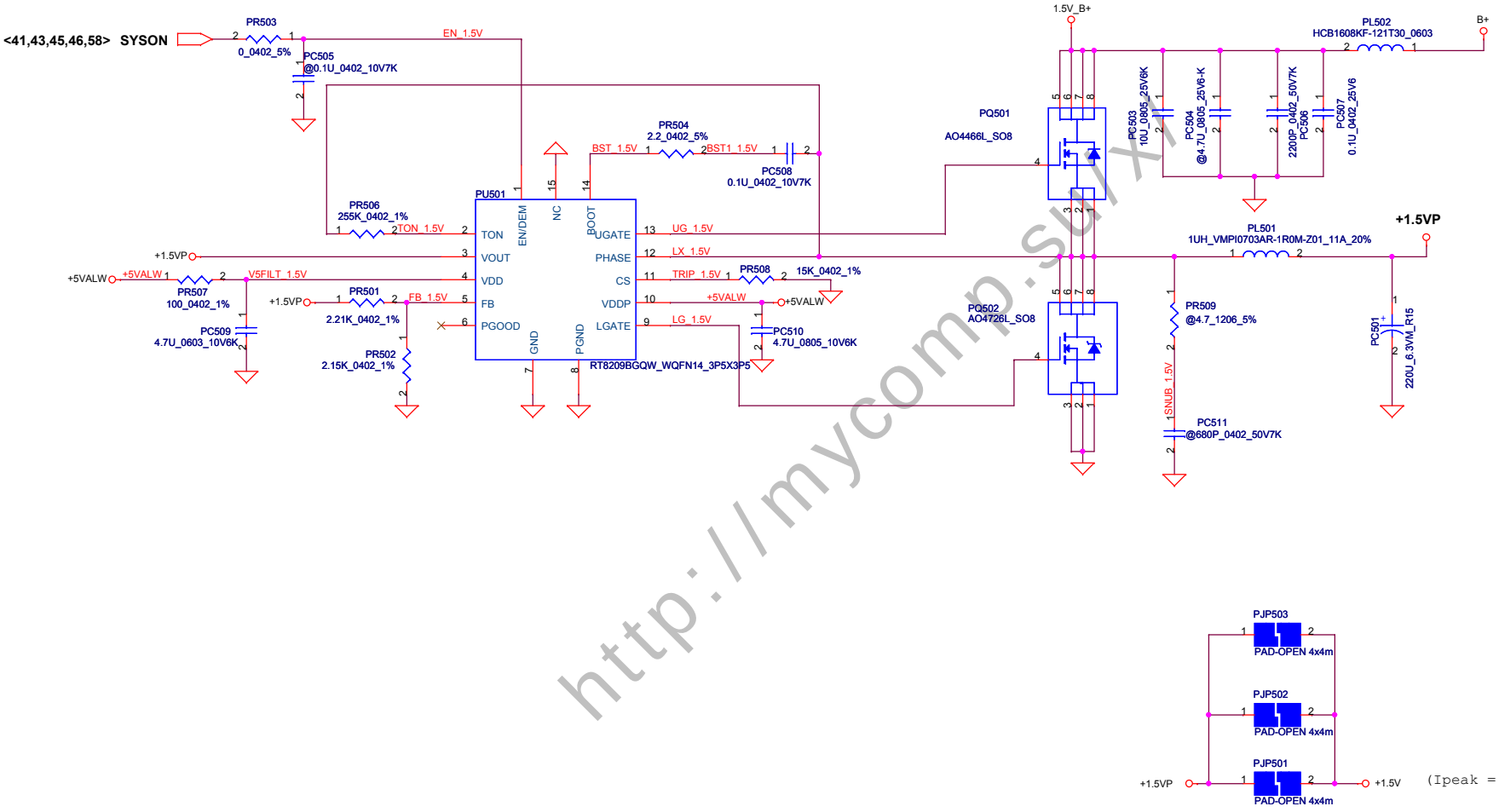
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.8VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.1

Date: Friday, January 21, 2011 | Sheet 50 of 58



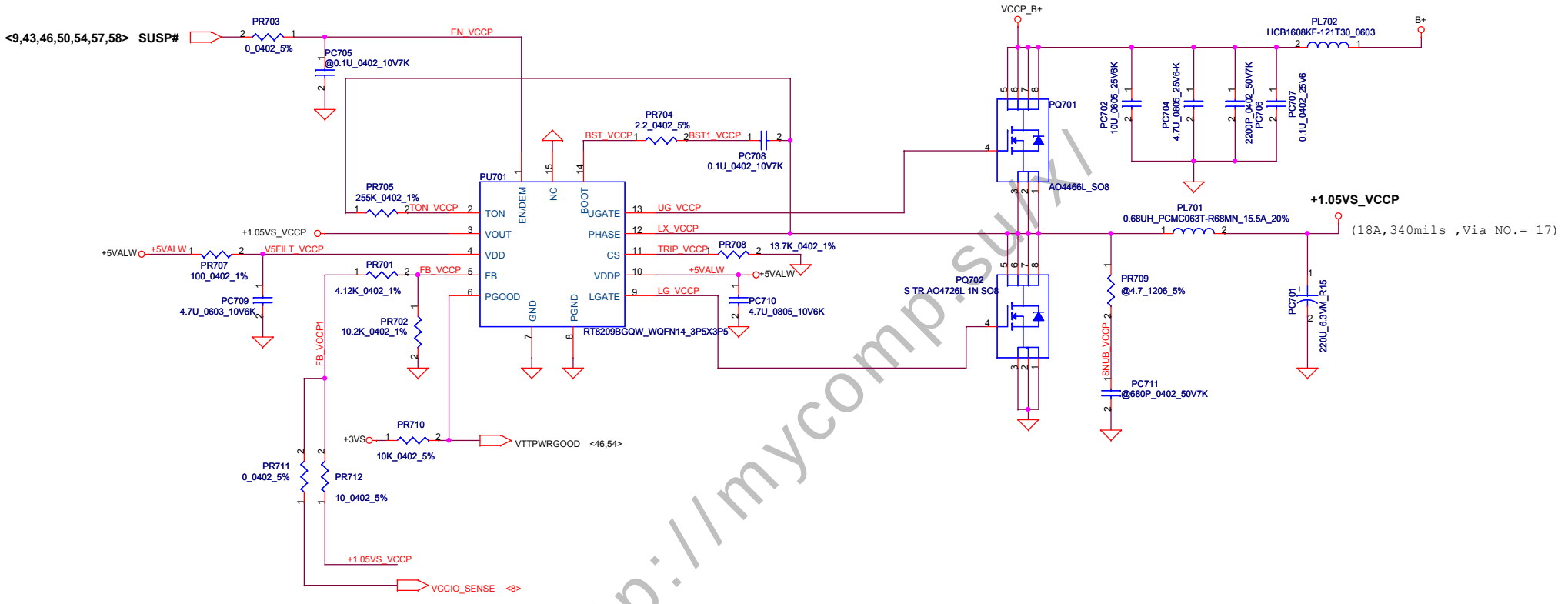
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	PBL21 LA6771P M/B	0.1

Date: Friday, January 21, 2011 | Sheet 51 of 58



VSSIO_SENSE connect to GND directly.

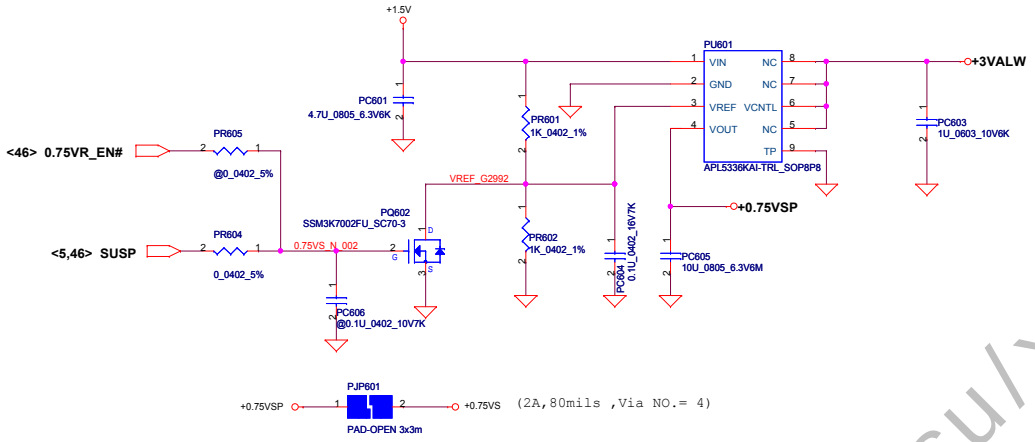
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR+1.05VSP/+VCCPP

Size: Custom | Document Number: PBL21 LA6771P M/B | Rev: 0.1

Date: Friday, January 21, 2011 | Sheet 52 of 58



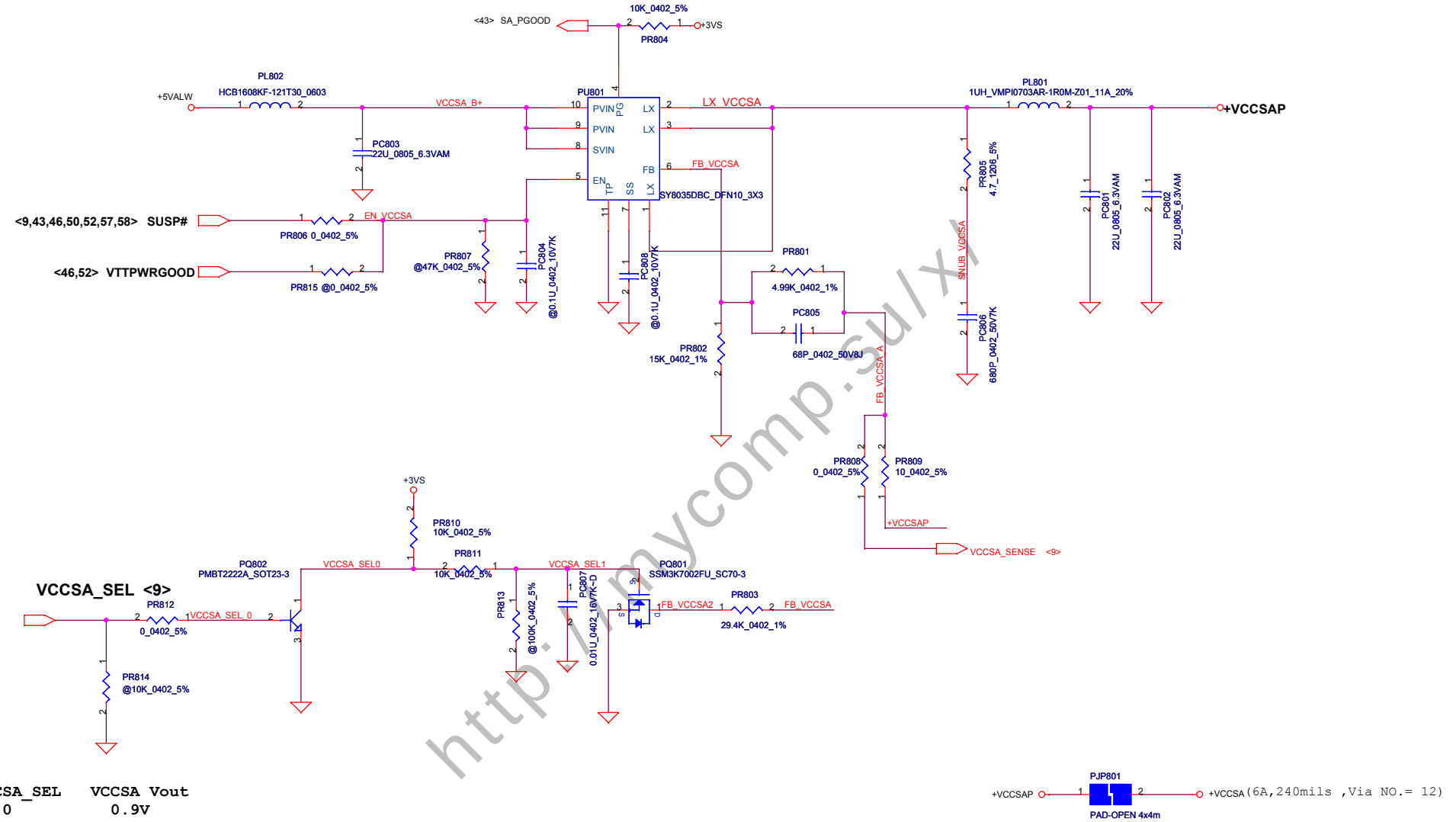
Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: 0.75VSP/1.2VSP

Size | Document Number: PBL21 LA6771P M/B | Rev: 0.1

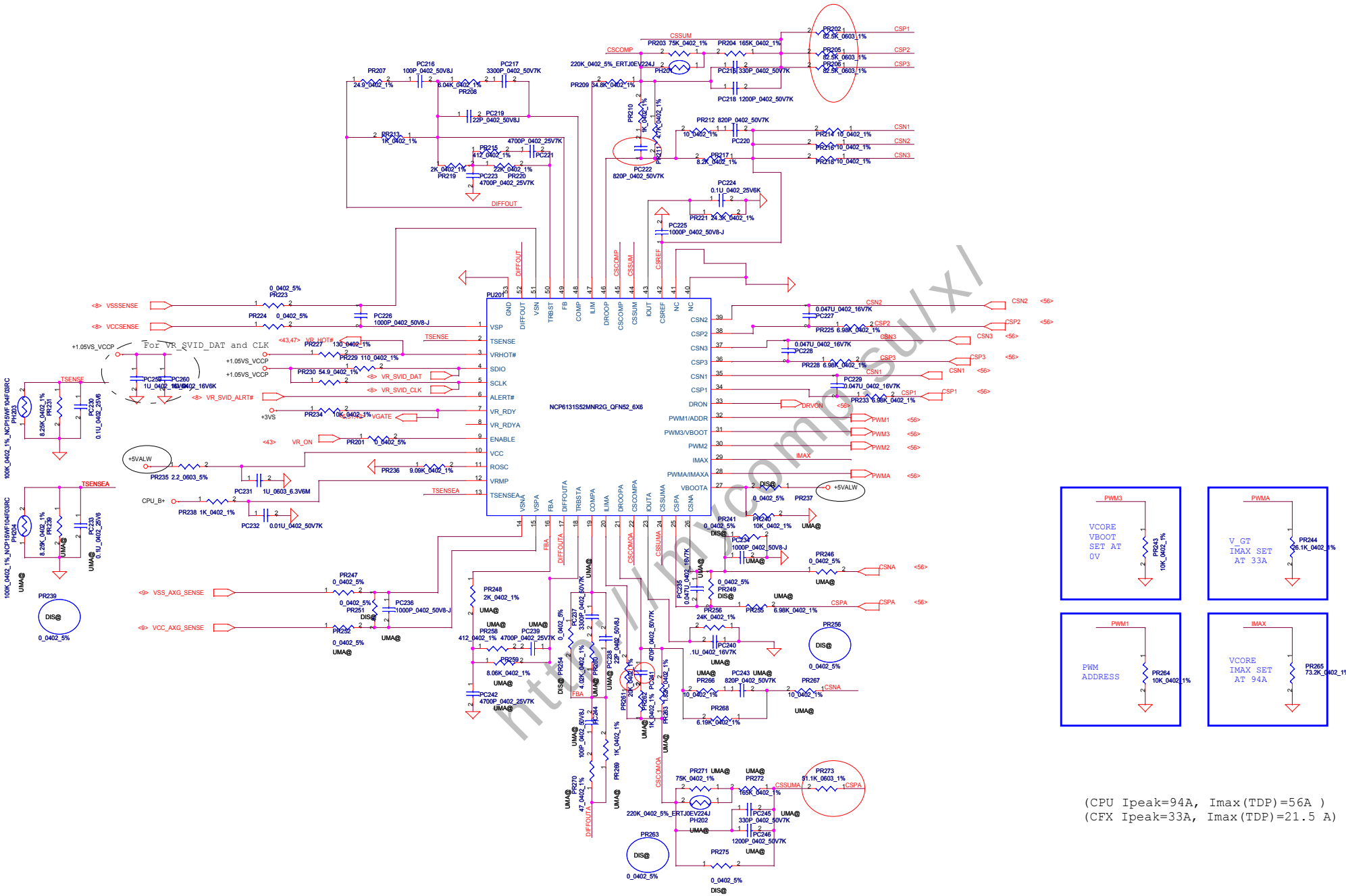
Date: Friday, January 21, 2011 | Sheet 53 of 58



VCCSA_SEL	VCCSA Vout
0	0.9V
1	0.8V

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

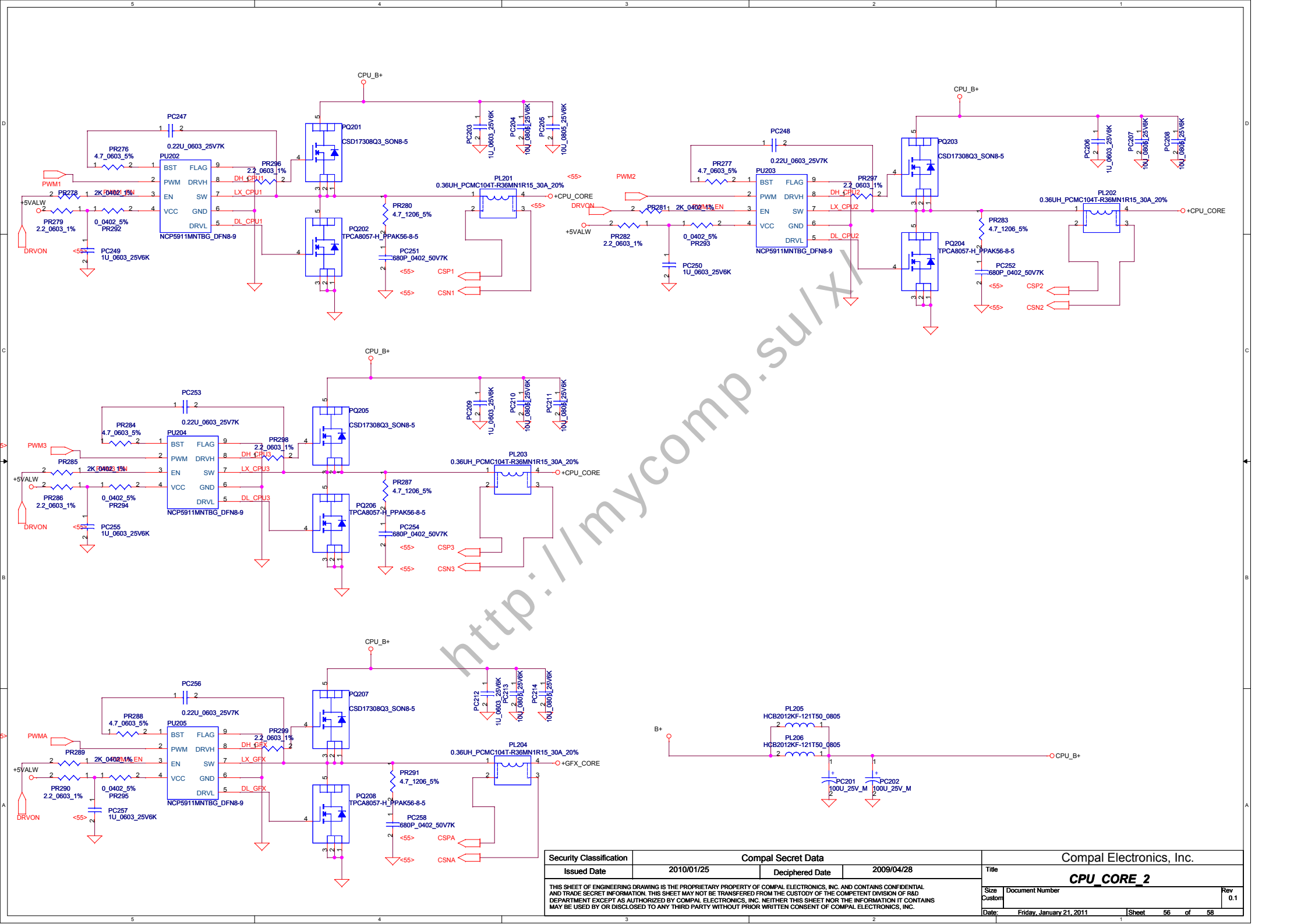
Compal Electronics, Inc.			
Title: PWR+VCCSAP			
Size: Custom	Document Number: PBL21 LA6771P M/B		Rev: 0.1
Date: Friday, January 21, 2011	Sheet 54 of 58		



(CPU Ipeak=94A, Imax(TDP)=56A)
(CFX Ipeak=33A, Imax(TDP)=21.5 A)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Title	CPU_CORE_1		
Size	Document Number		Rev
C	PCA60/70 LA-7001P M/B		0.1
Date:	Friday, January 21, 2011	Sheet	55 of 58



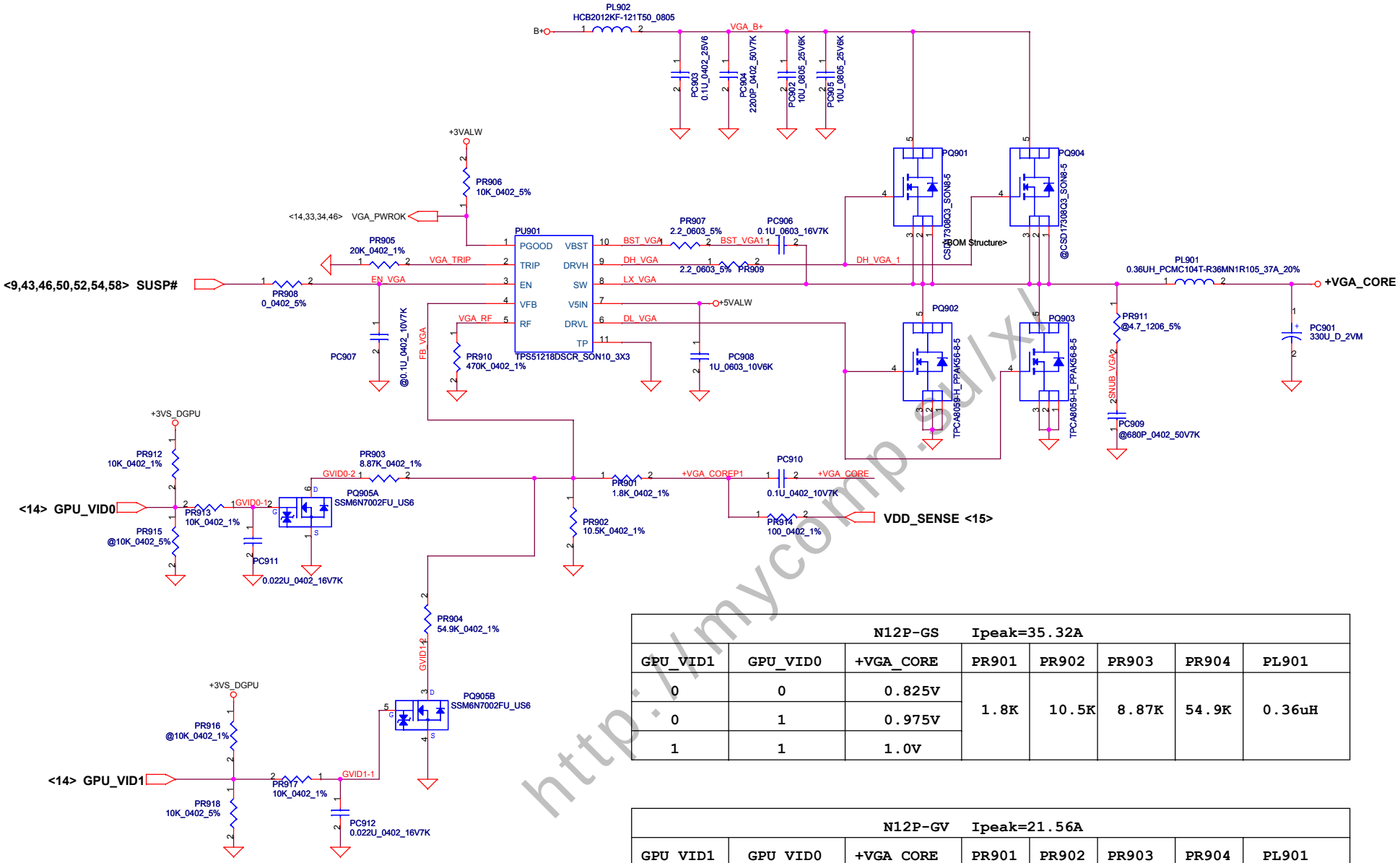
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: **CPU_CORE_2**

Size	Document Number	Rev
Custom		0.1

Date: Friday, January 21, 2011 | Sheet 56 of 58

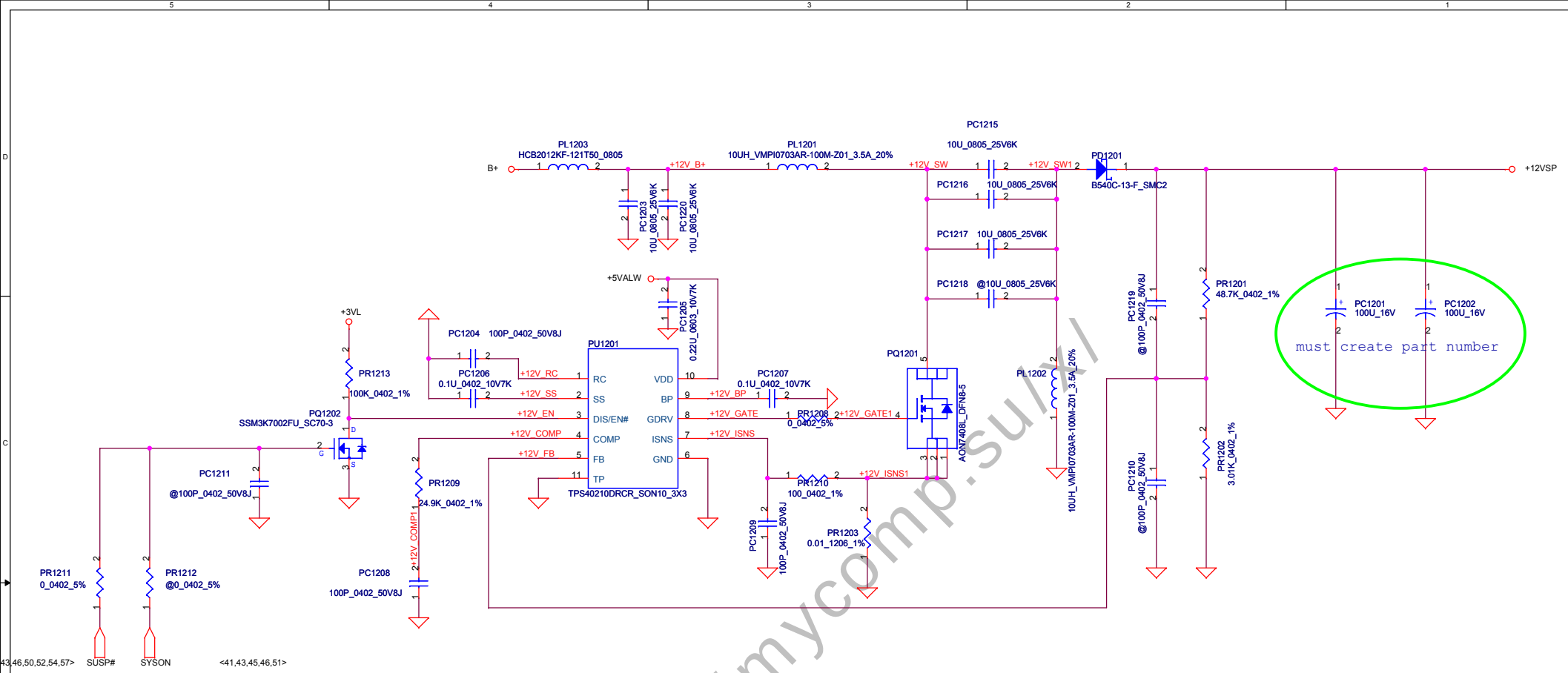


N12P-GS Ipeak=35.32A							
GPU_VID1	GPU_VID0	+VGA_CORE	PR901	PR902	PR903	PR904	PL901
0	0	0.825V	1.8K	10.5K	8.87K	54.9K	0.36uH
0	1	0.975V					
1	1	1.0V					

N12P-GV Ipeak=21.56A							
GPU_VID1	GPU_VID0	+VGA_CORE	PR901	PR902	PR903	PR904	PL901
0	0	0.85V	1.8K	10.5K	8.87K	54.9K	0.36uH
0	1	1.0V					
1	1	1.025V					

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2009/09/15

Compal Electronics, Inc.			
Title	+VGA_COREP		
Size	Document Number	PBL21 LA6771P M/B	Rev 0.1
Date: Friday, January 21, 2011	Sheet 57 of 58		



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PWR+12V_SEPIC			
Size: Custom	Document Number: PBL21 LA6771P M/B		Rev: 0.1
Date: Friday, January 21, 2011	Sheet 58 of 58		