

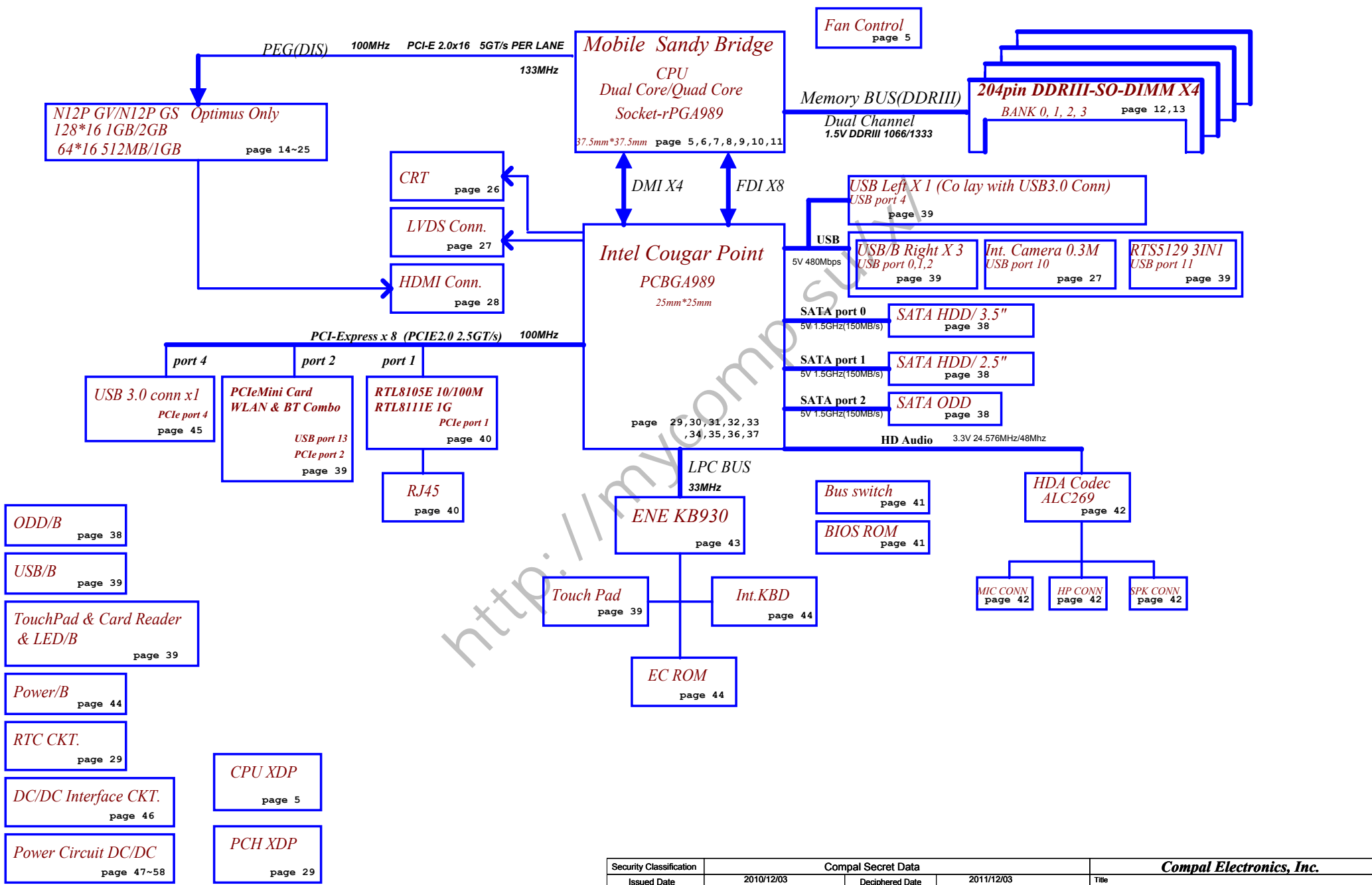
Compal Confidential

PBL80 Project

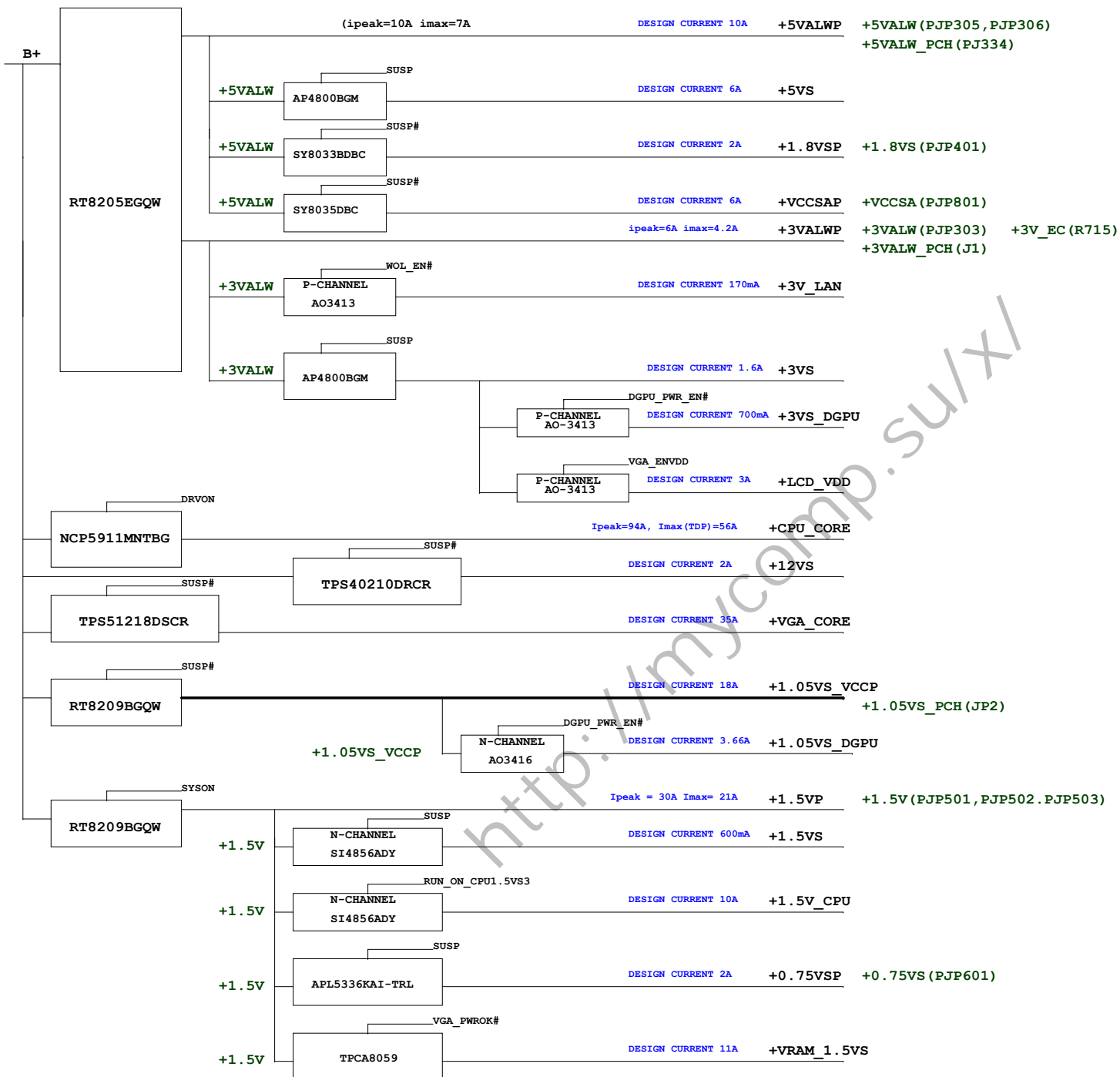
LA-7441P REV 0.1 Schematic

Intel Sandy Bridge/Cougar Point
N12P-GV/GS-Optimus Only
2011-01-21 Rev. 0.1

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Issued Date	2010/12/03	Deciphered Date	2011/12/03	Title Cover Page		
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					PBL80 LA-7441P M/B	0.1
				Date:	Friday, January 21, 2011	Sheet 1 of 58



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				Block Diagrams		
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				PBL80 LA-7441P M/B 0.1		
				Date:	Friday, January 21, 2011	Sheet 2 of 58



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				PBL80 LA-7441P M/B	
				Date	Friday, January 21, 2011
				Sheet	3 of 58

http://mycomp.su/xl

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +5VALW_PCH +3VALW_PCH +3V_LAN +3V_EC +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS_VCCP +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VCCSA +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +1.2VS
State						
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMMA1	A0 H	1010 0000 b
+3VS	DDR SO-DIMMA2	A0 H	1010 0010 b
+3VS	DDR SO-DIMMB1	A4 H	1010 0100 b
+3VS	DDR SO-DIMMB2	A0 H	1010 0110 b
+3VS	WLAN		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
				+3VS	VGA Thermal Sensor	9A H	1001 1010 b

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

Function	VRAM					GPU		Board ID
description	VRAM	Samsung 64bits	Hynix 64bits	Samsung 128bits	Hynix 128bits	N12P-GS	N12P-GV	Adaptor
explain	VRAM	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Strap pin	Adaptor
BTO	8PCS@	PD 20K	PD 15K	PD 45.3K	PD 34.8K	N12PGS@	N12PGV@	90W@, 120W@

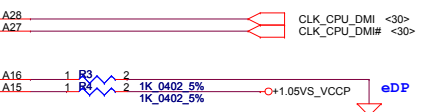
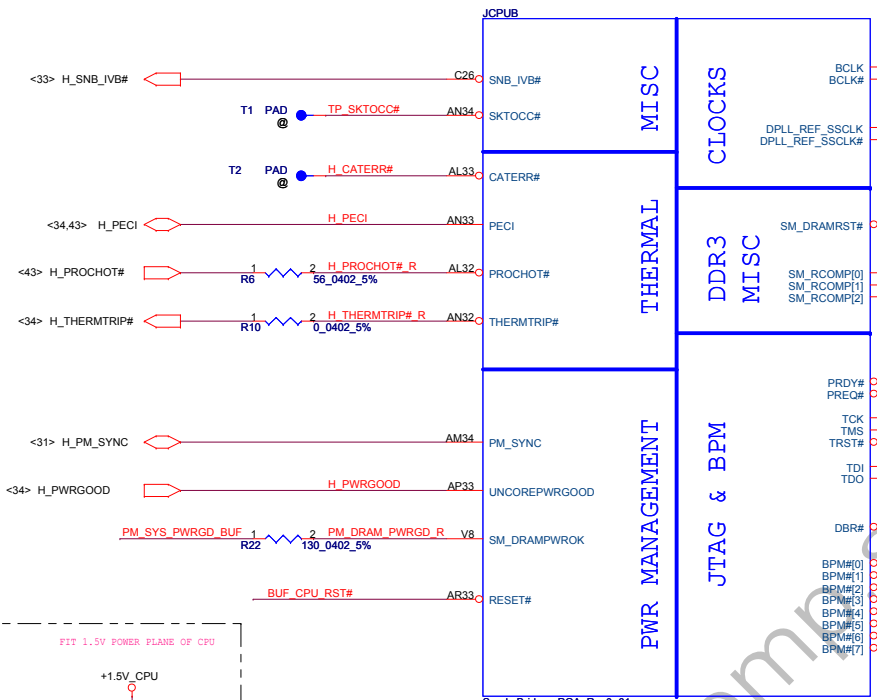
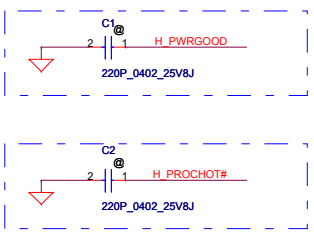
Function	Crisis recovery	HDMI	WLAN+BT		LAN	
description	BUS SWITCH	HDMI	WLAN+BT (BT pin 51)	WLAN+BT (BT pin 5)	Giga LAN	10/100M LAN
explain	BUS SWITCH	HDMI	WLAN+BT (BT pin 51)	WLAN+BT (BT pin 5)	Strap pin	Strap pin
BTO	Debug@	HDMI@	BT@	COMBO@	8111E@	8105E@

Function	USB3.0/2.0 Celay		SATA3.0 Repeater Chip		SATA Preemphasis		SATA Equalization	
description	USB3.0	USB2.0	MAXIM	TI	Preemphasis		Equalization	
explain	USB3.0	USB2.0	MAX4951	SN75LVCP601	Enable	Disable	Maximum	Normal
BTO	USB3@	USB2@	MAXIM@	TI@	DEN@	NDEN@	EQ@	NEQ@

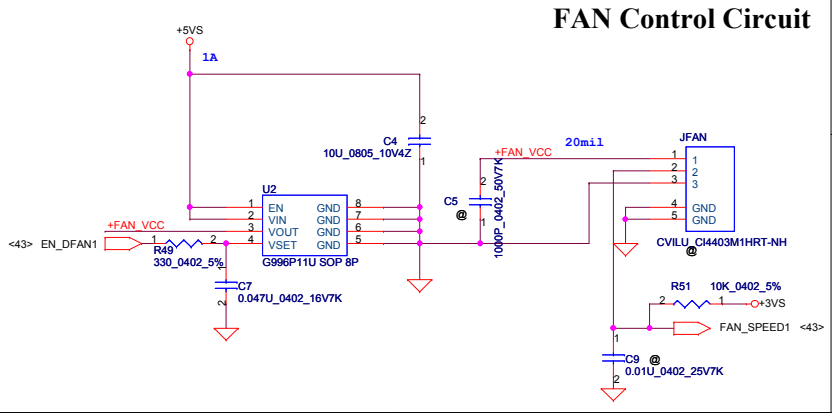
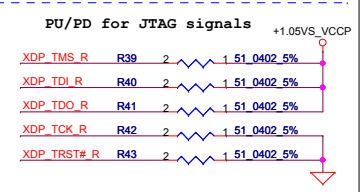
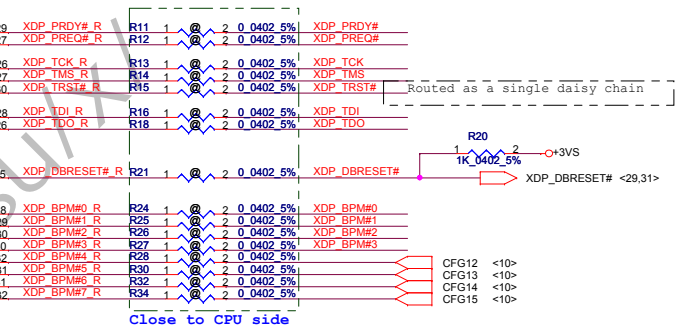
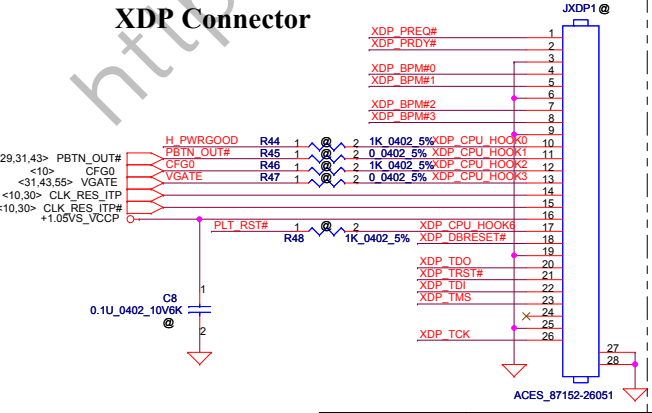
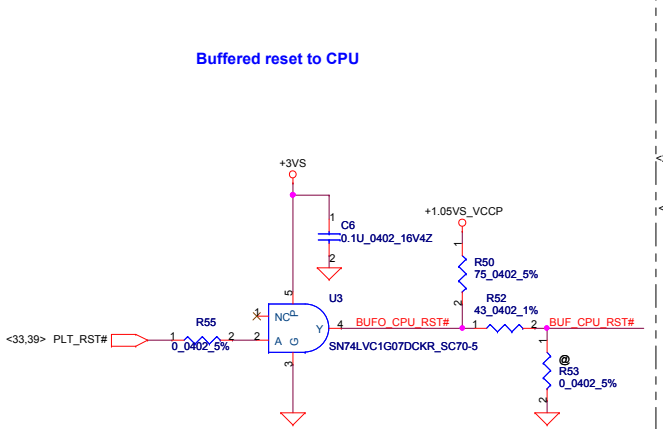
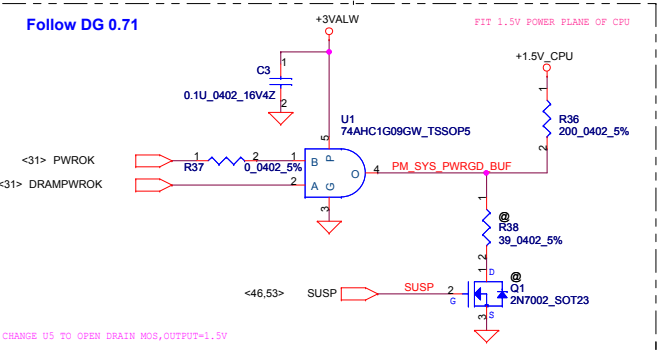
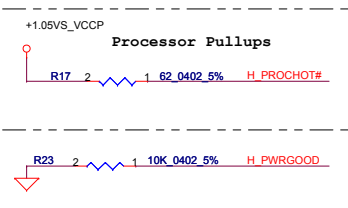
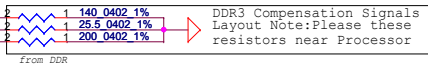
Function	SATA path	
description	PCH	Repeater
explain	PCH	Repeater
BTO	SATA@	SATARP@

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				Notes List		
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				Date:	Friday, January 21, 2011	Sheet

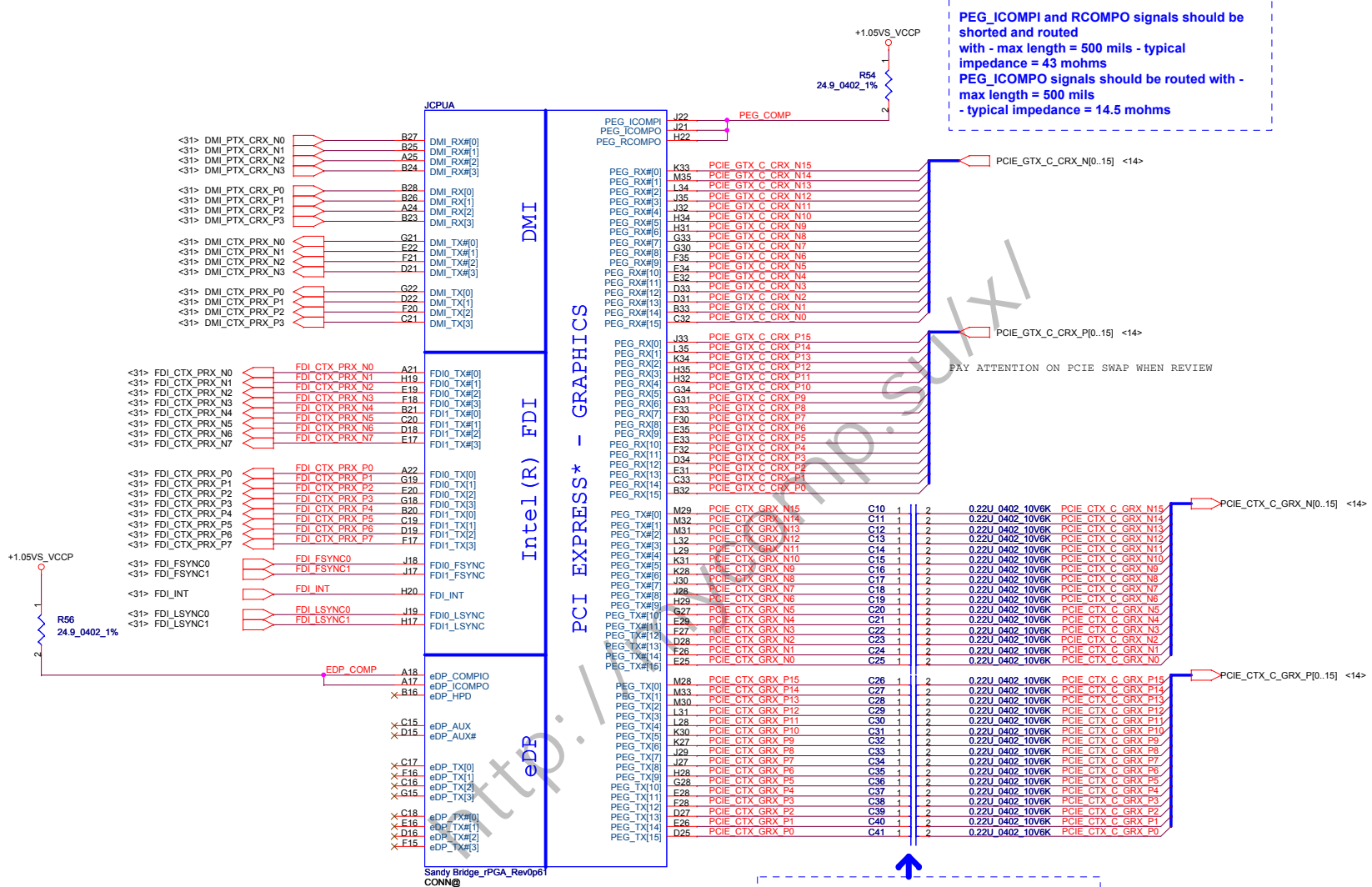
Support Dual Core/ Quad Core



If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1k +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1k +/- 5% resistor



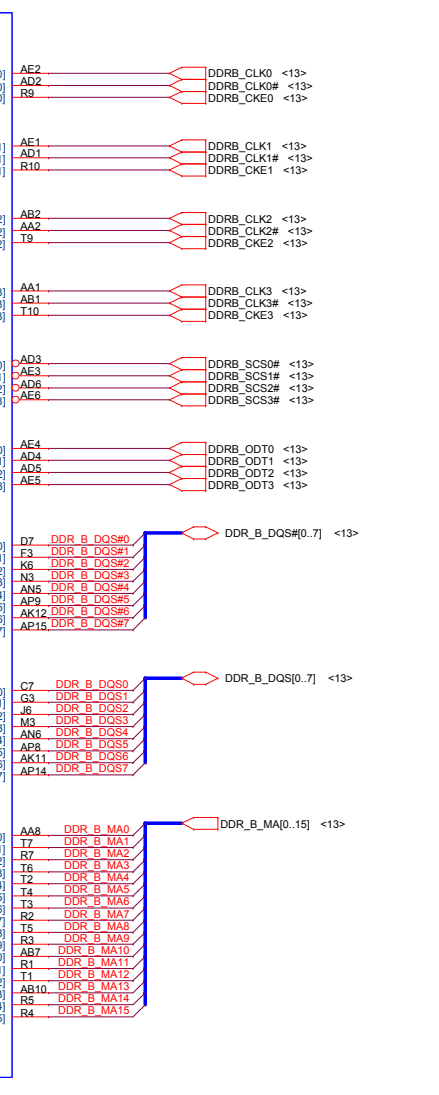
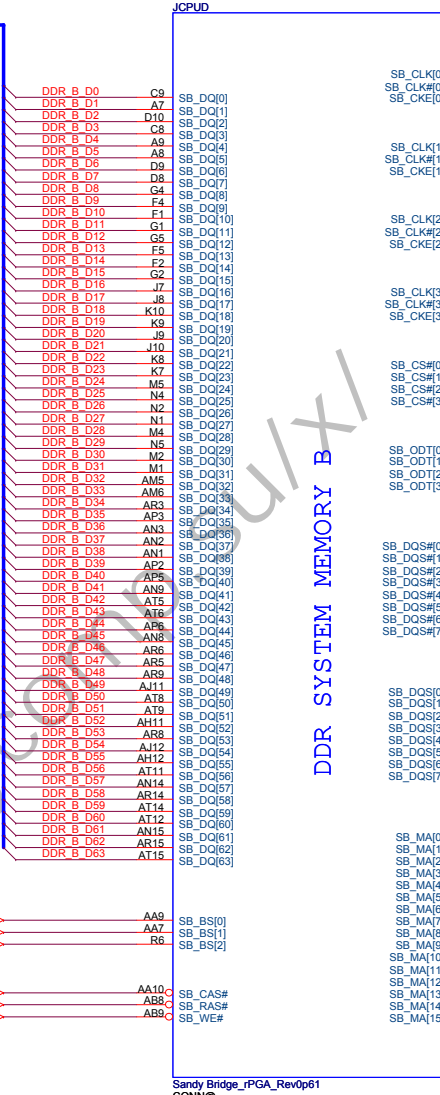
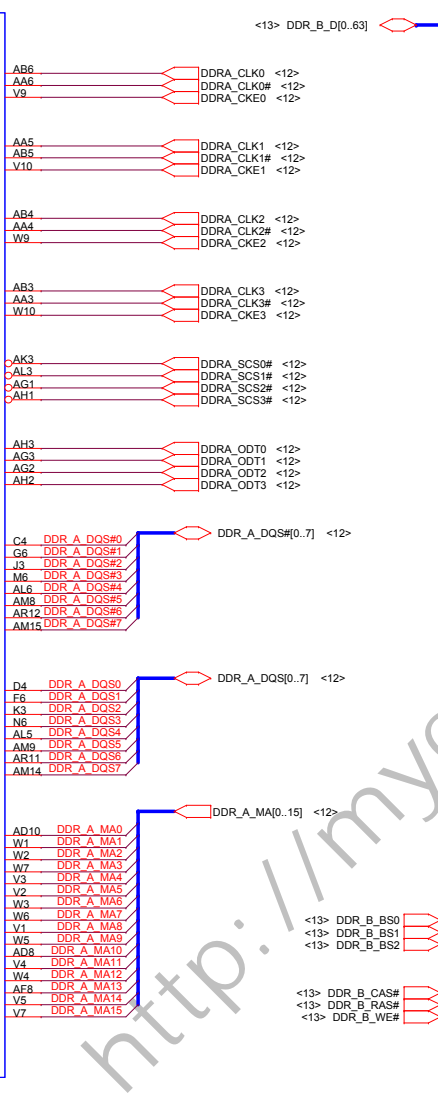
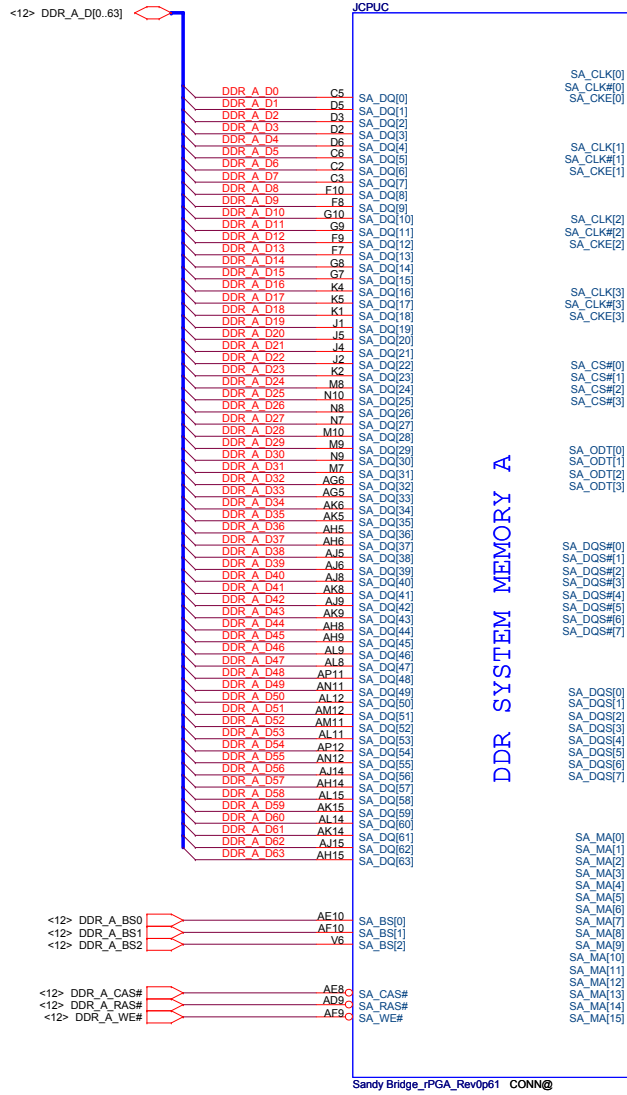
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Issued Date	2010/12/03	Deciphered Date	2011/12/03	Sandy Bridge(1/6)-CLK/MISC/JTAG/XDP/FAN
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Size	Document Number	PBL80 LA-7441P M/B		Rev
Custom				0.1
Date:	Friday, January 21, 2011	Sheet	5	of 58



PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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Date:	Friday, January 21, 2011	Sheet	6	of 58

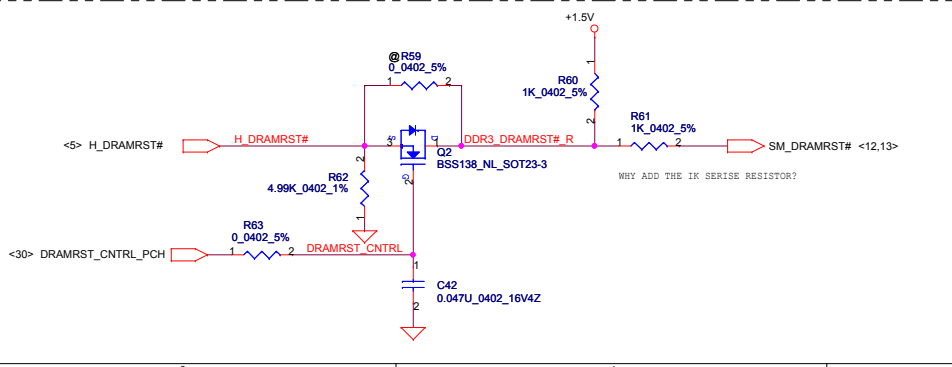


DDR SYSTEM MEMORY A

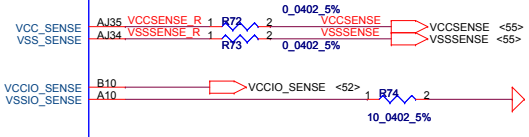
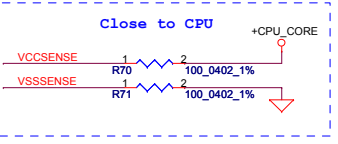
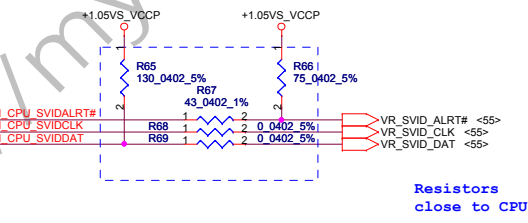
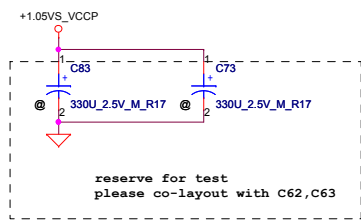
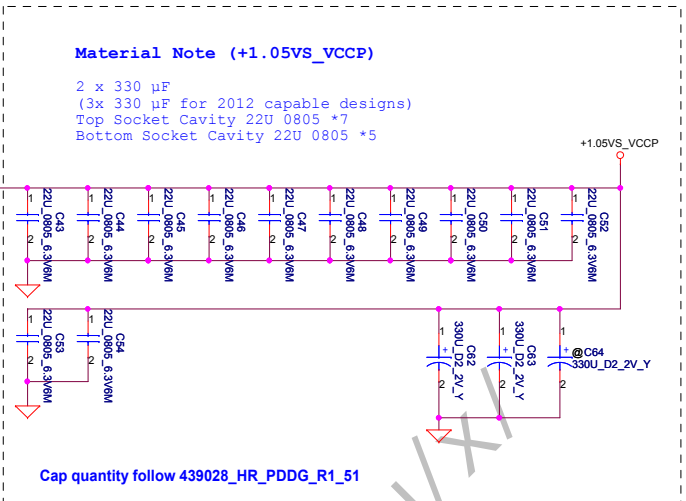
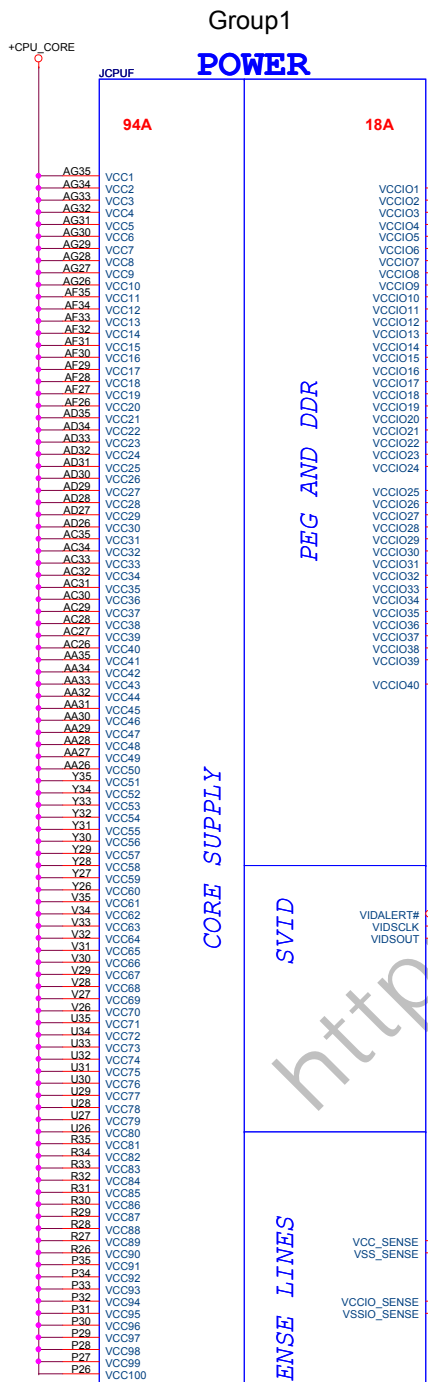
DDR SYSTEM MEMORY B

Sandy Bridge_rPGA_Rev0p61 CONN@

Sandy Bridge_rPGA_Rev0p61 CONN@



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				Document Number: PBL80 LA-7441P M/B
				Rev: 0.1
				Date: Friday, January 21, 2011
				Sheet 7 of 58

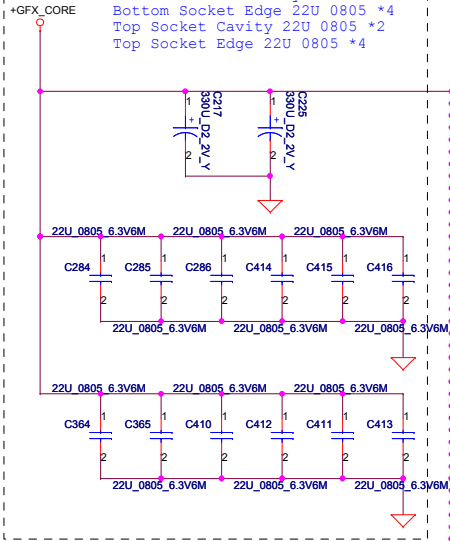


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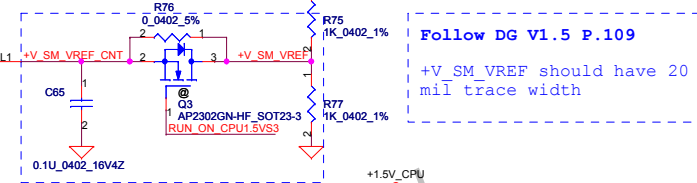
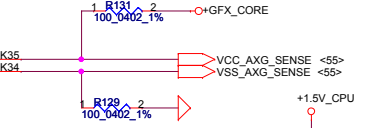
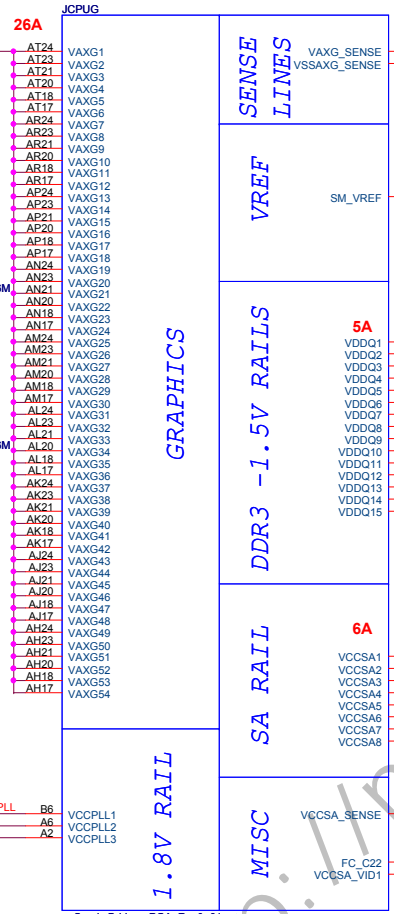
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Sandy Bridge(4/6)-PWR		
Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1
Date:	Friday, January 21, 2011	Sheet 8 of 58

Sandy Bridge_rPGA_Rev0p61
CONN@

Material Note (GFXCORE)
 2 x 330 µF on Bottom socket edge
 Bottom Socket Cavity 22U 0805 *2
 Bottom Socket Edge 22U 0805 *4
 Top Socket Cavity 22U 0805 *2
 Top Socket Edge 22U 0805 *4

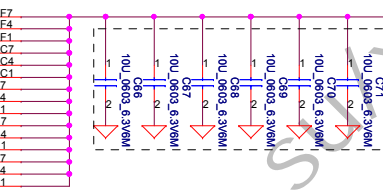


POWER Group2

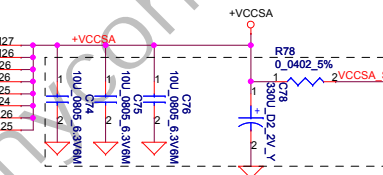


Follow DG v1.5 P.109

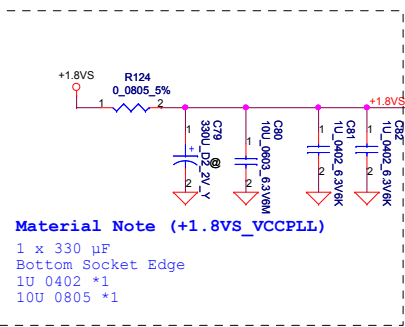
+V_SM_VREF should have 20 mil trace width



Material Note (VDDQ)
 Bottom Socket Edge
 1 x 330 µF
 10U 0805 *6

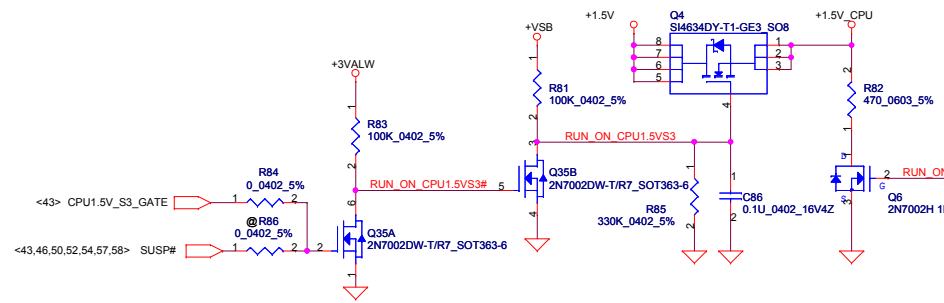


Material Note (VCCSA)
 1 x 330 µF
 Bottom Socket Cavity 10U 0805 *2
 Bottom Socket Edge 10U 0805 *1



Material Note (+1.8VS_VCCPLL)
 1 x 330 µF
 Bottom Socket Edge
 1U 0402 *1
 10U 0805 *1

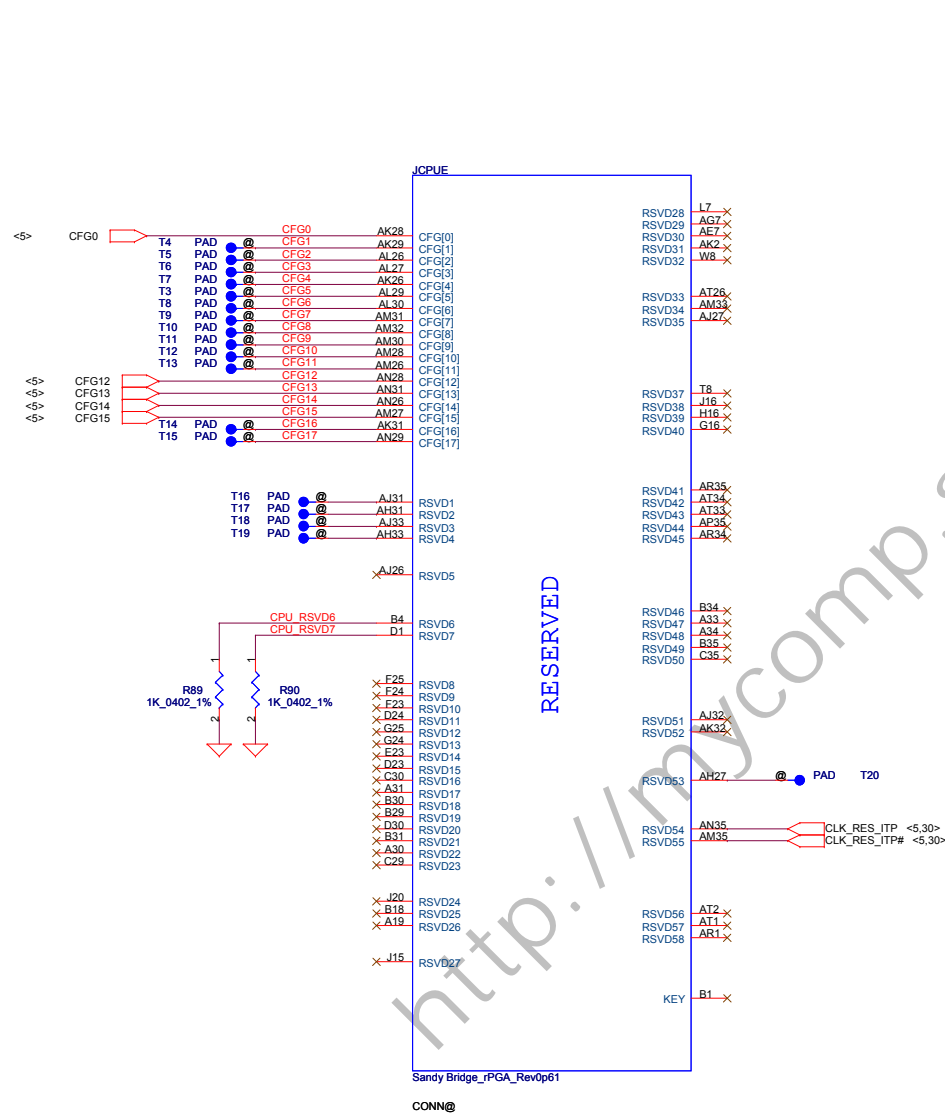
+1.5V_CPU Source



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				Sandy Bridge(4/6)-PWR
Size Custom		Document Number	Rev	
		PBL80 LA-7441P M/B	0.1	
Date		Friday, January 21, 2011	Sheet	9 of 58

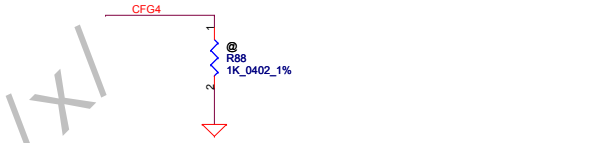
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CFG Straps for Processor



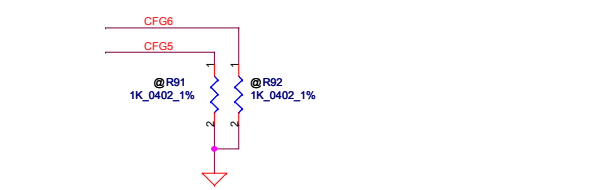
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed
------	--



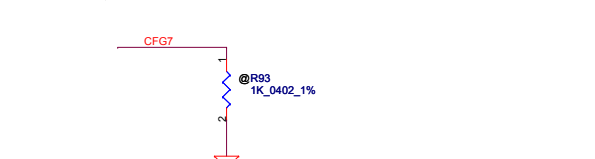
Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--



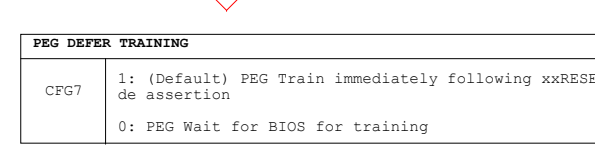
PCIe Port Bifurcation Straps

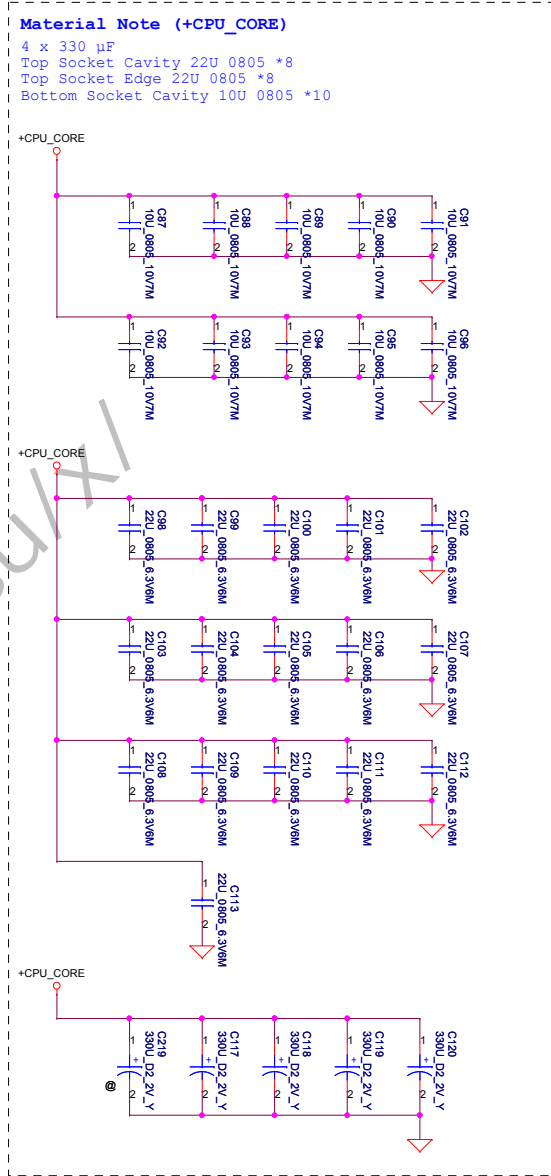
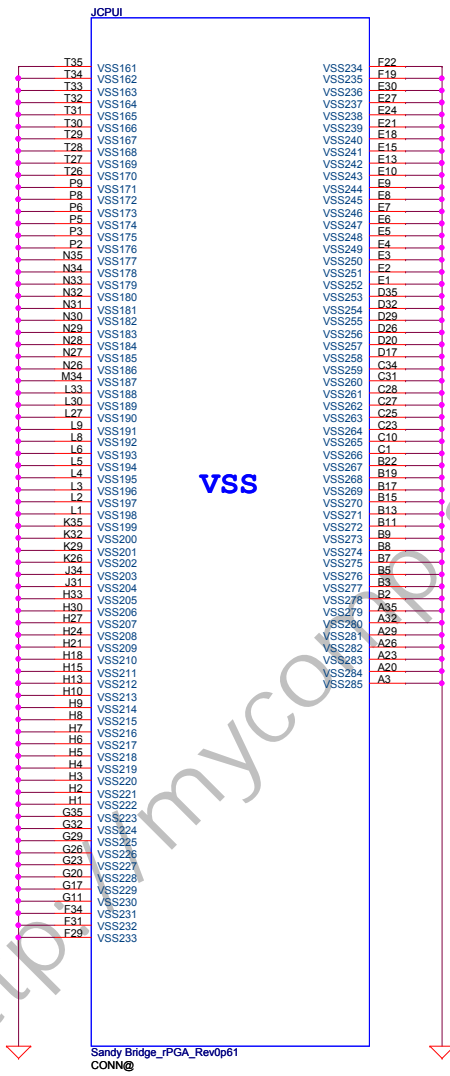
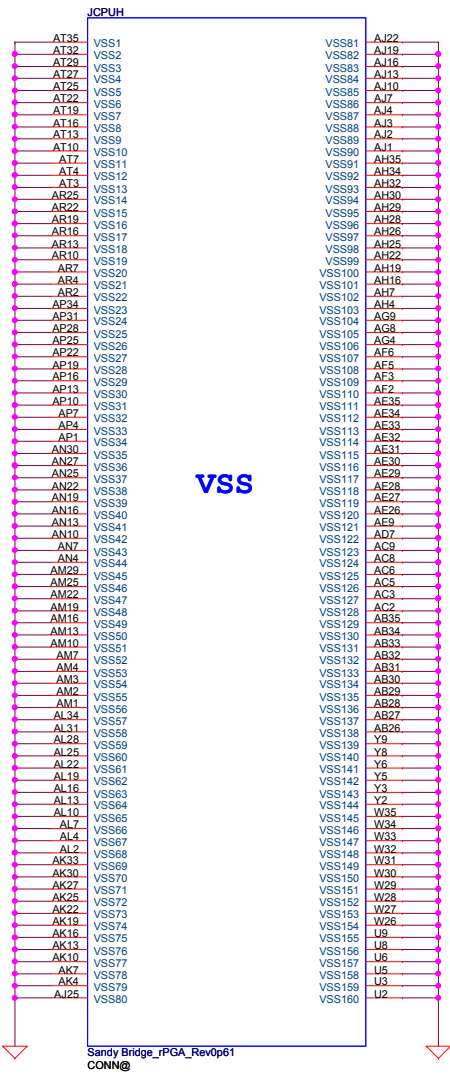
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
----------	--



PEG DEFER TRAINING

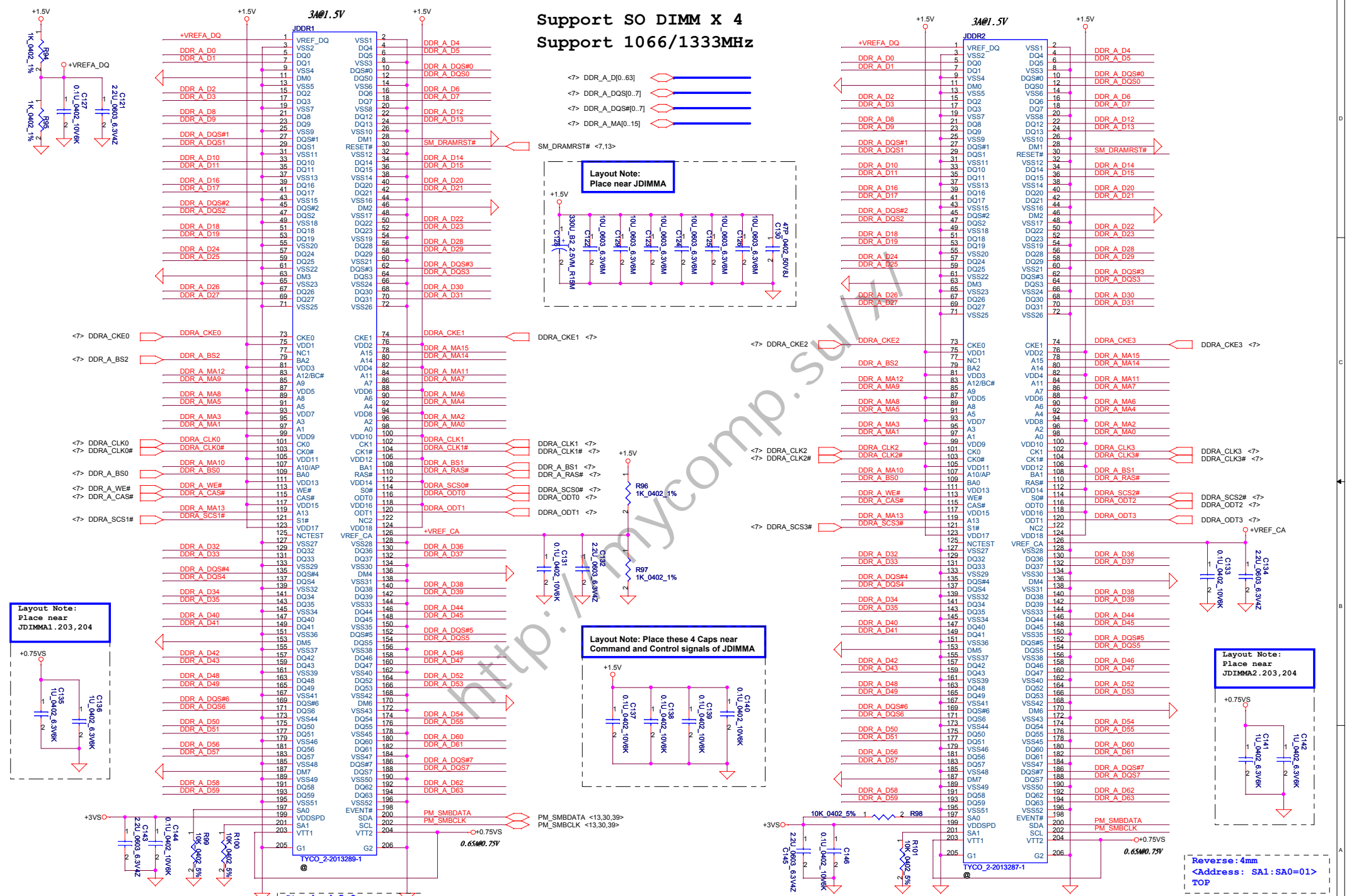
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---





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Support SO DIMM X 4 Support 1066/1333MHz



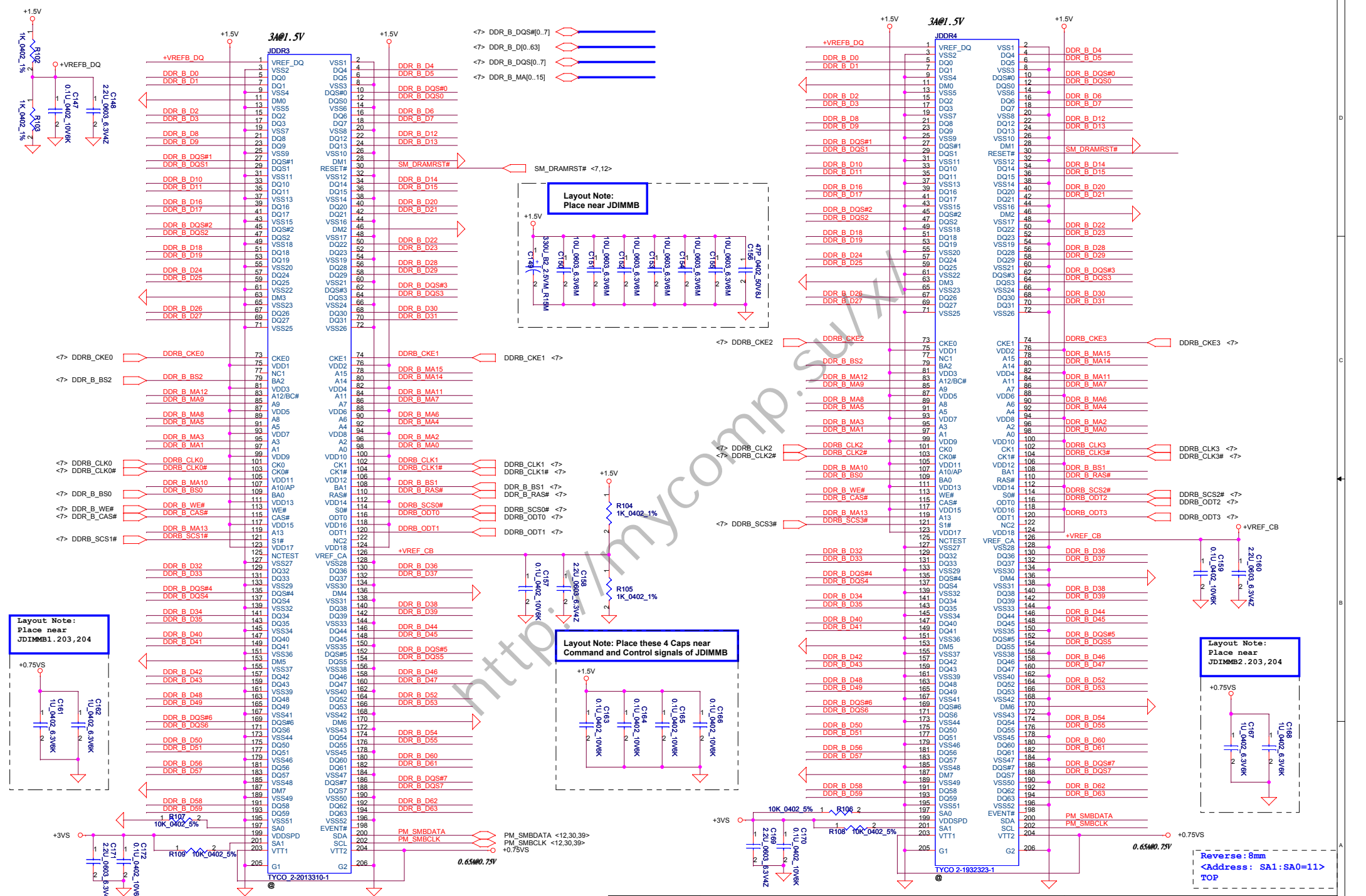
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Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1
Date:	Friday, January 21, 2011	Sheet 12 of 58

Standard: 5.2mm
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BOT

Reverse: 4mm
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TOP



Standard: 9.2mm
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 BOT

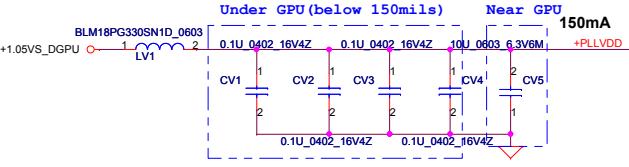
Reverse: 8mm
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		2011/12/03

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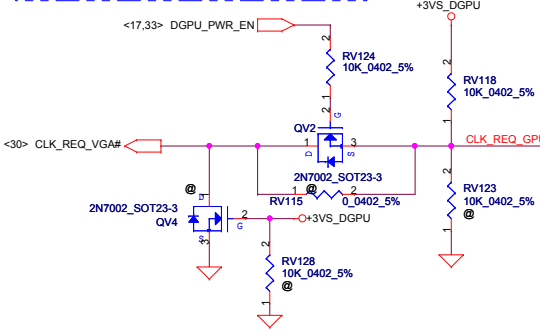
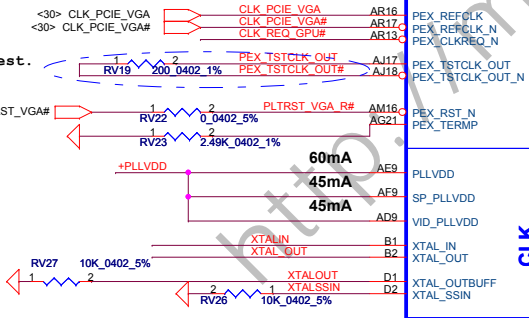
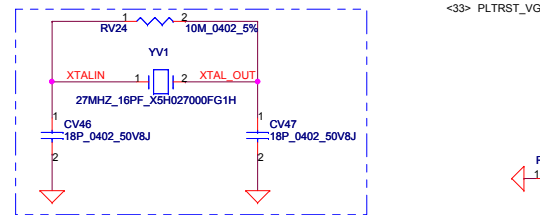
Compal Electronics, Inc.		
DDRIII-DIMMB		
Title	Size	Document Number
		PBL80 LA-7441P M/B
Date:	Friday, January 21, 2011	Rev 0.1
		Sheet 13 of 58

N12PGS@
UV1
N12P-GS-A1_BGA_973P



PCIE GTX C CRX P#	CV#	1	2	0.22U_0402_10V6K	PCIE GTX CRX P#	AL#
PCIE GTX C CRX P0	CV6	1	2	0.22U_0402_10V6K	PCIE GTX CRX P0	AL17
PCIE GTX C CRX N0	CV7	1	2	0.22U_0402_10V6K	PCIE GTX CRX N0	AM17
PCIE GTX C CRX P1	CV8	1	2	0.22U_0402_10V6K	PCIE GTX CRX P1	AM18
PCIE GTX C CRX N1	CV9	1	2	0.22U_0402_10V6K	PCIE GTX CRX N1	AM19
PCIE GTX C CRX P2	CV10	1	2	0.22U_0402_10V6K	PCIE GTX CRX P2	AL19
PCIE GTX C CRX N2	CV11	1	2	0.22U_0402_10V6K	PCIE GTX CRX N2	AK19
PCIE GTX C CRX P3	CV12	1	2	0.22U_0402_10V6K	PCIE GTX CRX P3	AK20
PCIE GTX C CRX N3	CV13	1	2	0.22U_0402_10V6K	PCIE GTX CRX N3	AM20
PCIE GTX C CRX P4	CV14	1	2	0.22U_0402_10V6K	PCIE GTX CRX P4	AM21
PCIE GTX C CRX N4	CV15	1	2	0.22U_0402_10V6K	PCIE GTX CRX N4	AM22
PCIE GTX C CRX P5	CV16	1	2	0.22U_0402_10V6K	PCIE GTX CRX P5	AK21
PCIE GTX C CRX N5	CV17	1	2	0.22U_0402_10V6K	PCIE GTX CRX N5	AK22
PCIE GTX C CRX P6	CV18	1	2	0.22U_0402_10V6K	PCIE GTX CRX P6	AL23
PCIE GTX C CRX N6	CV19	1	2	0.22U_0402_10V6K	PCIE GTX CRX N6	AM23
PCIE GTX C CRX P7	CV20	1	2	0.22U_0402_10V6K	PCIE GTX CRX P7	AK23
PCIE GTX C CRX N7	CV21	1	2	0.22U_0402_10V6K	PCIE GTX CRX N7	AM24
PCIE GTX C CRX P8	CV22	1	2	0.22U_0402_10V6K	PCIE GTX CRX P8	AL24
PCIE GTX C CRX N8	CV23	1	2	0.22U_0402_10V6K	PCIE GTX CRX N8	AK24
PCIE GTX C CRX P9	CV24	1	2	0.22U_0402_10V6K	PCIE GTX CRX P9	AK25
PCIE GTX C CRX N9	CV25	1	2	0.22U_0402_10V6K	PCIE GTX CRX N9	AM25
PCIE GTX C CRX P10	CV26	1	2	0.22U_0402_10V6K	PCIE GTX CRX P10	AM27
PCIE GTX C CRX N10	CV27	1	2	0.22U_0402_10V6K	PCIE GTX CRX N10	AM28
PCIE GTX C CRX P11	CV28	1	2	0.22U_0402_10V6K	PCIE GTX CRX P11	AL28
PCIE GTX C CRX N11	CV29	1	2	0.22U_0402_10V6K	PCIE GTX CRX N11	AK26
PCIE GTX C CRX P12	CV30	1	2	0.22U_0402_10V6K	PCIE GTX CRX P12	AK26
PCIE GTX C CRX N12	CV31	1	2	0.22U_0402_10V6K	PCIE GTX CRX N12	AL29
PCIE GTX C CRX P13	CV32	1	2	0.22U_0402_10V6K	PCIE GTX CRX P13	AM29
PCIE GTX C CRX N13	CV33	1	2	0.22U_0402_10V6K	PCIE GTX CRX N13	AM30
PCIE GTX C CRX P14	CV34	1	2	0.22U_0402_10V6K	PCIE GTX CRX P14	AM31
PCIE GTX C CRX N14	CV35	1	2	0.22U_0402_10V6K	PCIE GTX CRX N14	AM32
PCIE GTX C CRX P15	CV36	1	2	0.22U_0402_10V6K	PCIE GTX CRX P15	AN32
PCIE GTX C CRX N15	CV37	1	2	0.22U_0402_10V6K	PCIE GTX CRX N15	AP32

RV19 stuff per NV request.
12/17



UV1A

PCIE CTX C GRX P#	AP#	PEX_RX0	PEX_RX0_N	PEX_RX1	PEX_RX1_N	PEX_RX2	PEX_RX2_N	PEX_RX3	PEX_RX3_N	PEX_RX4	PEX_RX4_N	PEX_RX5	PEX_RX5_N	PEX_RX6	PEX_RX6_N	PEX_RX7	PEX_RX7_N	PEX_RX8	PEX_RX8_N	PEX_RX9	PEX_RX9_N	PEX_RX10	PEX_RX10_N	PEX_RX11	PEX_RX11_N	PEX_RX12	PEX_RX12_N	PEX_RX13	PEX_RX13_N	PEX_RX14	PEX_RX14_N	PEX_RX15	PEX_RX15_N
PCIE CTX C GRX P0	AP17	PEX_TX0	PEX_TX0_N	PEX_TX1	PEX_TX1_N	PEX_TX2	PEX_TX2_N	PEX_TX3	PEX_TX3_N	PEX_TX4	PEX_TX4_N	PEX_TX5	PEX_TX5_N	PEX_TX6	PEX_TX6_N	PEX_TX7	PEX_TX7_N	PEX_TX8	PEX_TX8_N	PEX_TX9	PEX_TX9_N	PEX_TX10	PEX_TX10_N	PEX_TX11	PEX_TX11_N	PEX_TX12	PEX_TX12_N	PEX_TX13	PEX_TX13_N	PEX_TX14	PEX_TX14_N	PEX_TX15	PEX_TX15_N

Part 1 of 7

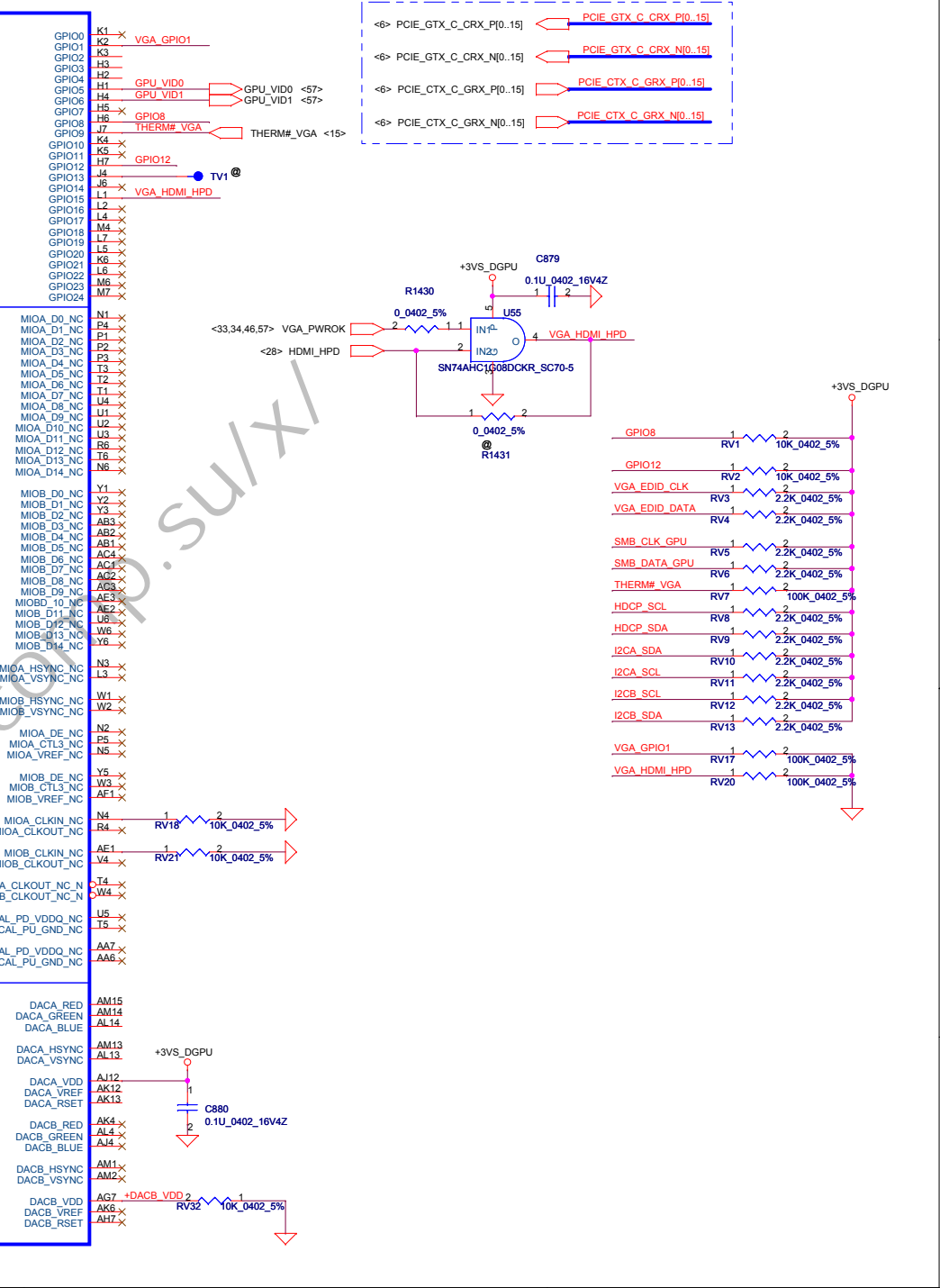
GPIO

PCI EXPRESS

DVO

CLK

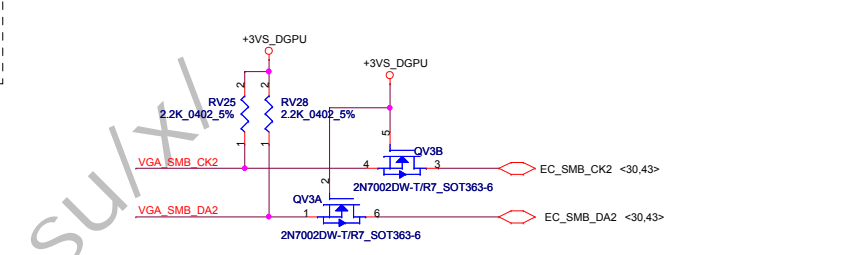
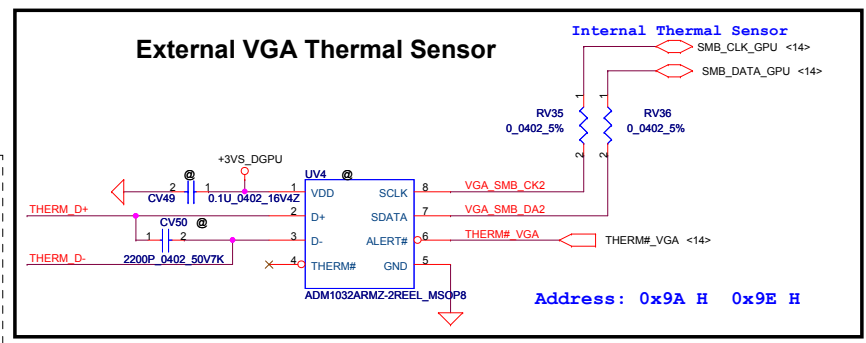
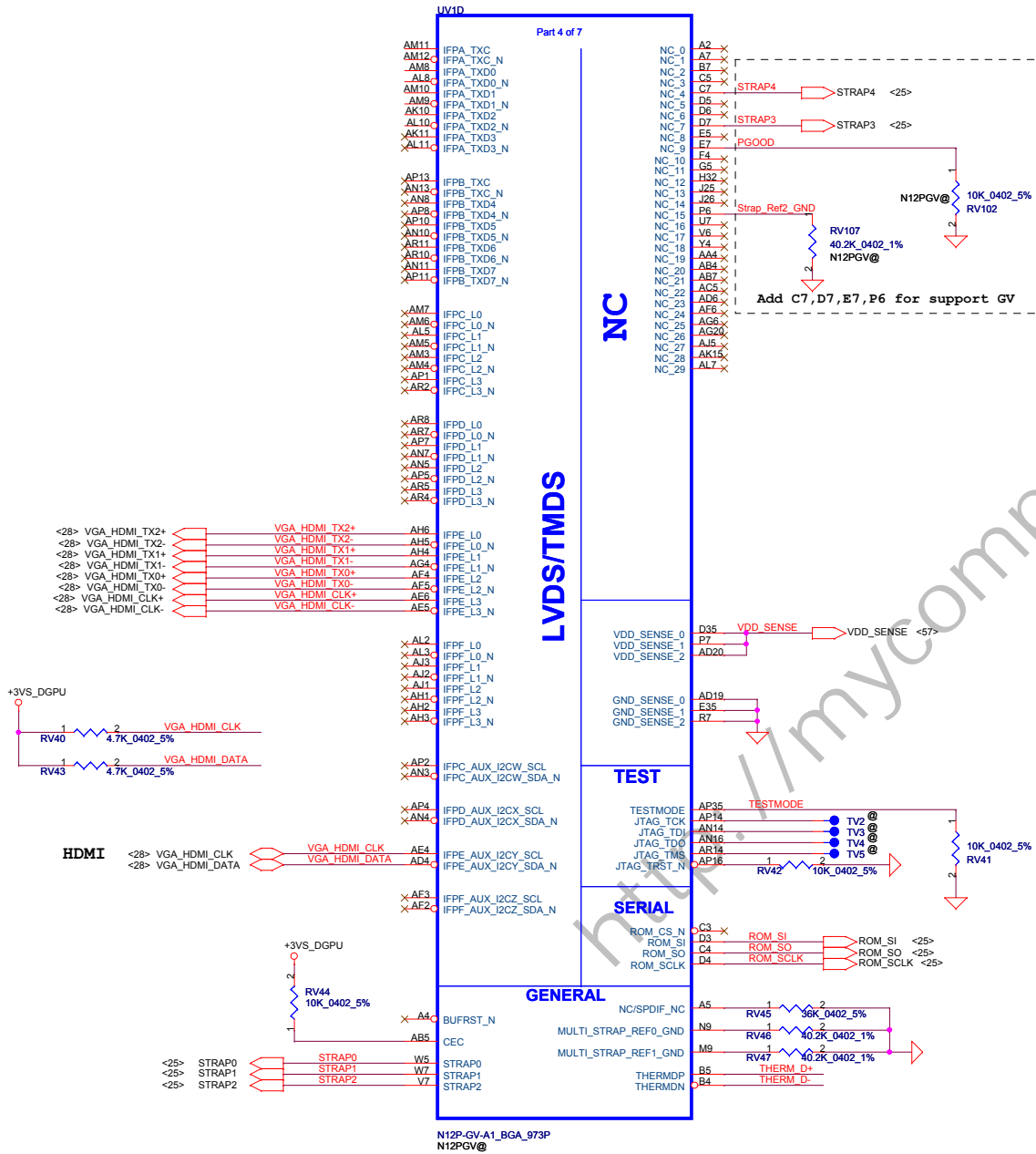
I2C DACs



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Issued Date	2010/12/03	Deciphered Date
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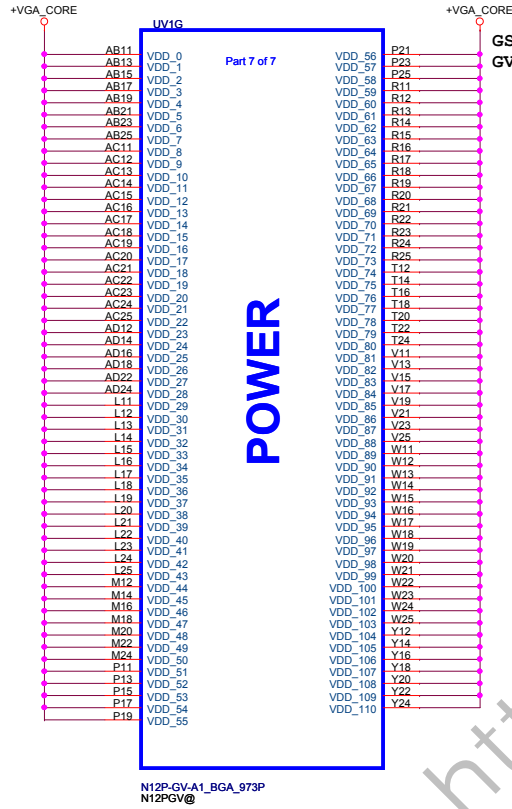
Compal Electronics, Inc.		
Title VGA(1/12)-PCIE/DAC/GPIO		
Size	Document Number	Rev
	PBL80 LA-7441P M/B	0.1
Date:	Friday, January 21, 2011	Sheet 14 of 58

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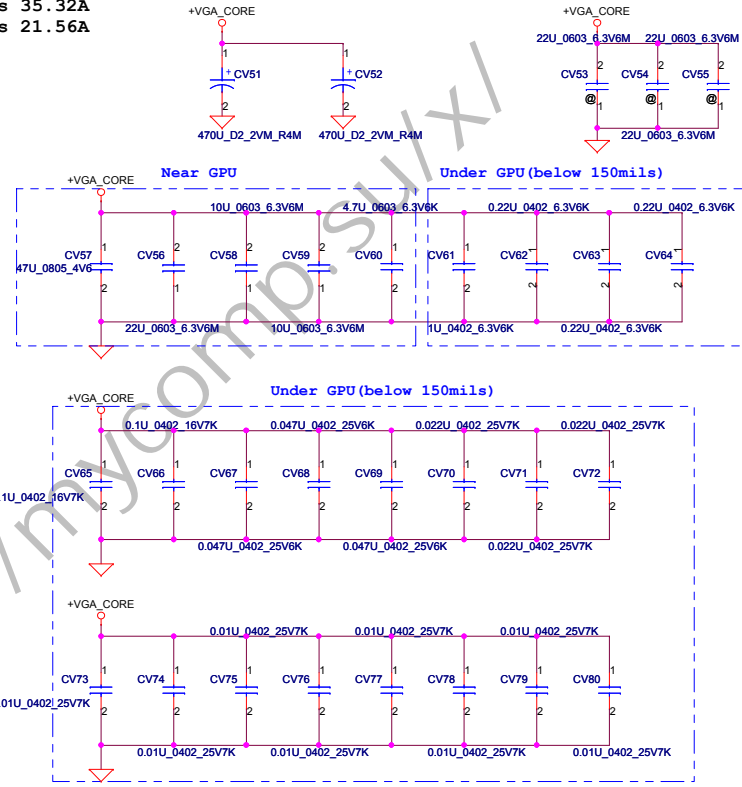


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Issued Date	2010/12/03	Deciphered Date	2011/12/03	Compal Electronics, Inc.
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				Document Number
				PBL80 LA-7441P M/B
				Rev 0.1
				Date: Friday, January 21, 2011 Sheet 15 of 58

Pstate	GPU_VID0	GPU_VID1	N12P-GS	N12P-GV
P8-P12	0	0	0.825V	0.85V
P0 (Hot)	1	0	0.975V	1V
	0	1		
P0 (cold)	1	1	1V	1.025V



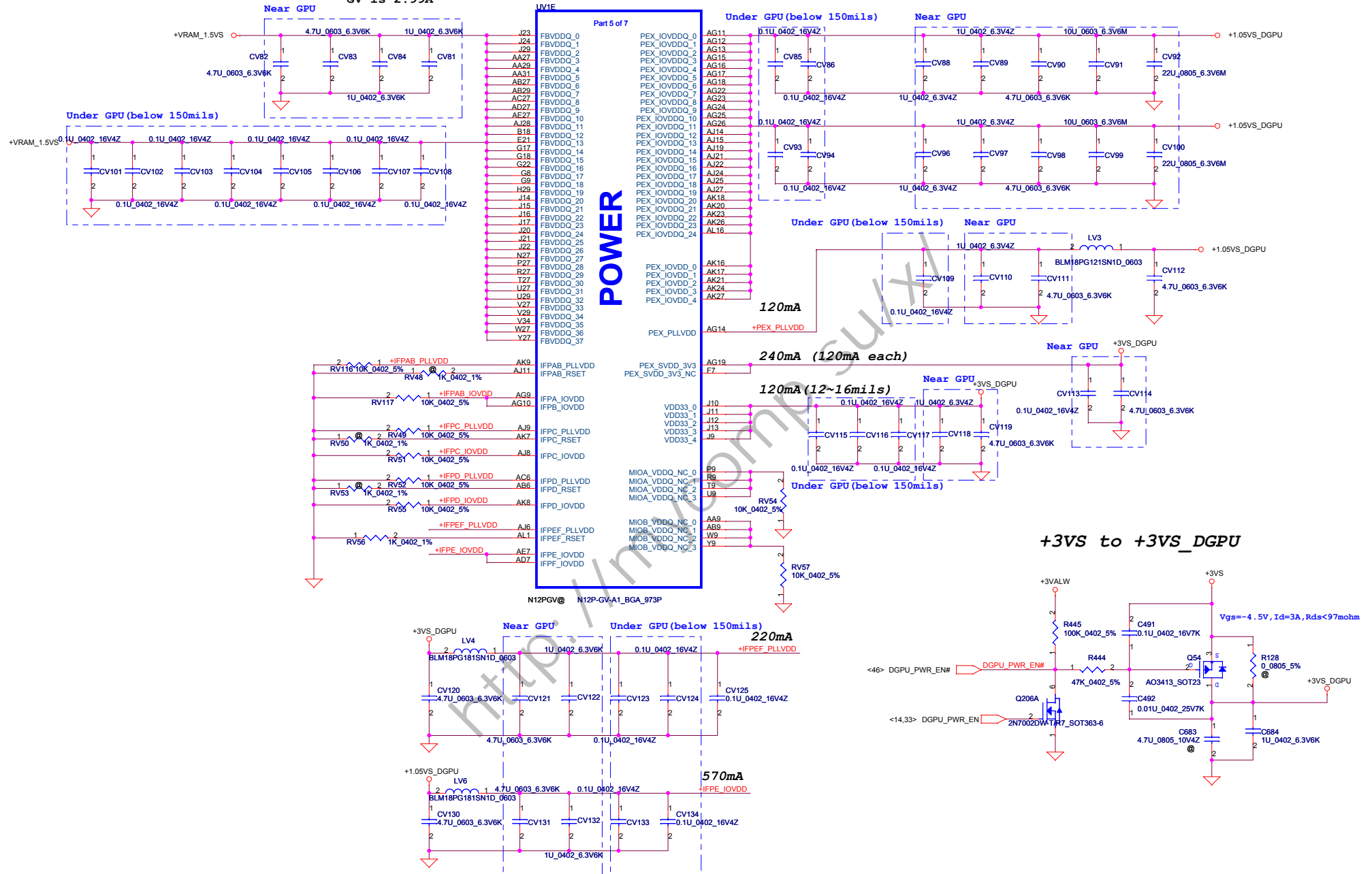
GS EDP Peak is 35.32A
GV EDP Peak is 21.56A



Security Classification		Compal Secret Data		Title		
Issued Date	2010/12/03	Deciphered Date	2011/12/03	VGA(3/12)-VGA CORE		
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					PBL80 LA-7441P M/B	0.1
Date: Friday, January 21, 2011				Sheet	16	of 58

GS is 5.49A
GV is 2.99A

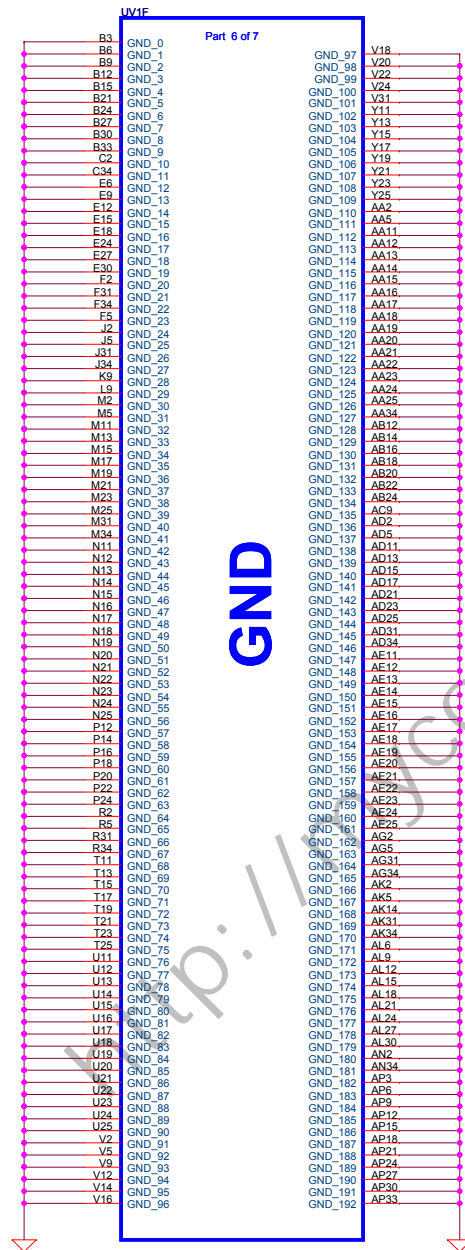
GS is 2.95A
GV is 3.51A



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Title			Compal Electronics, Inc.	
			VGA(4/12)-POWER	
Size	Document Number	Rev		
	PBL80 LA-7441P M/B			0.1
Date:	Friday, January 21, 2011	Sheet	17	of 58



N12P-GV-A1_BGA_973P
N12PGV@

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Issued Date	2010/12/03	Deciphered Date 2011/12/03
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Compal Electronics, Inc.		
VGA(5/12)-GND		
Title	Document Number	Rev
	PBL80 LA-7441P M/B	0.1
Date:	Friday, January 21, 2011	Sheet 18 of 58

<21,22> MDA[0..63] ← MDA[0..63]

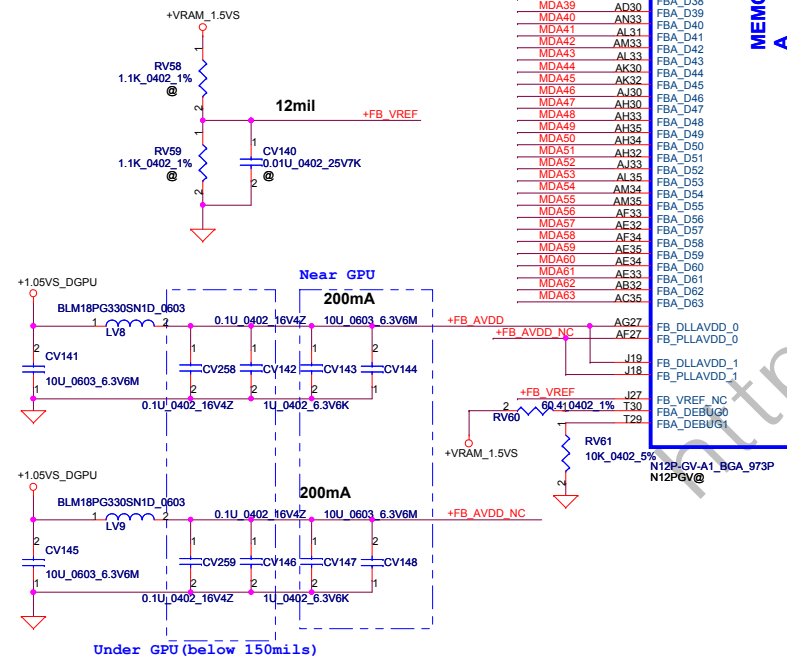
- MDA0 L32 FBA_D0
- MDA1 N33 FBA_D1
- MDA2 L33 FBA_D2
- MDA3 N34 FBA_D3
- MDA4 N35 FBA_D4
- MDA5 P36 FBA_D5
- MDA6 P33 FBA_D6
- MDA7 P34 FBA_D7
- MDA8 K35 FBA_D8
- MDA9 K33 FBA_D9
- MDA10 K34 FBA_D10
- MDA11 H33 FBA_D11
- MDA12 H34 FBA_D12
- MDA13 G33 FBA_D13
- MDA14 E34 FBA_D14
- MDA15 E33 FBA_D15
- MDA16 G31 FBA_D16
- MDA17 F30 FBA_D17
- MDA18 G30 FBA_D18
- MDA19 G32 FBA_D19
- MDA20 K30 FBA_D20
- MDA21 K32 FBA_D21
- MDA22 H30 FBA_D22
- MDA23 K31 FBA_D23
- MDA24 L31 FBA_D24
- MDA25 L30 FBA_D25
- MDA26 M32 FBA_D26
- MDA27 N30 FBA_D27
- MDA28 M30 FBA_D28
- MDA29 P31 FBA_D29
- MDA30 R32 FBA_D30
- MDA31 R30 FBA_D31
- MDA32 AC30 FBA_D32
- MDA33 AC32 FBA_D33
- MDA34 AH31 FBA_D34
- MDA35 AF31 FBA_D35
- MDA36 AF30 FBA_D36
- MDA37 AE30 FBA_D37
- MDA38 AC32 FBA_D38
- MDA39 AD30 FBA_D39
- MDA40 AL31 FBA_D40
- MDA41 AN33 FBA_D41
- MDA42 AM33 FBA_D42
- MDA43 AL33 FBA_D43
- MDA44 AK30 FBA_D44
- MDA45 AK32 FBA_D45
- MDA46 AI30 FBA_D46
- MDA47 AH30 FBA_D47
- MDA48 AH33 FBA_D48
- MDA49 AI35 FBA_D49
- MDA50 AH34 FBA_D50
- MDA51 AH32 FBA_D51
- MDA52 AJ33 FBA_D52
- MDA53 AL35 FBA_D53
- MDA54 AM34 FBA_D54
- MDA55 AM35 FBA_D55
- MDA56 AF33 FBA_D56
- MDA57 AE32 FBA_D57
- MDA58 AE34 FBA_D58
- MDA59 AE35 FBA_D59
- MDA60 AE34 FBA_D60
- MDA61 AE33 FBA_D61
- MDA62 AB32 FBA_D62
- MDA63 AC35 FBA_D63

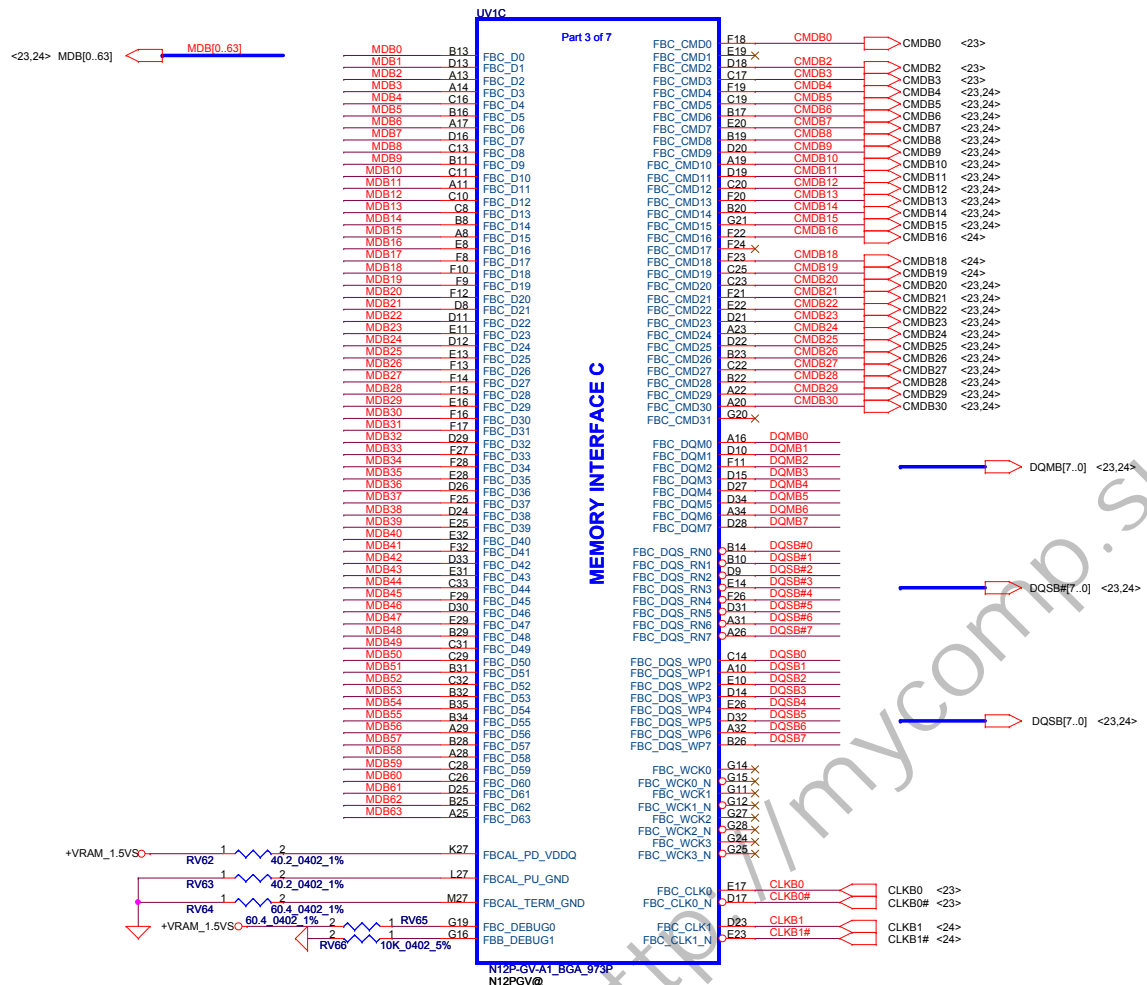
MEMORY INTERFACE

- FBA_CMD0 U30 CMDA0 <21>
- FBA_CMD1 V30 X CMDA1 <21>
- FBA_CMD2 U31 CMDA2 <21>
- FBA_CMD3 V32 CMDA3 <21>
- FBA_CMD4 U33 CMDA4 <21,22>
- FBA_CMD5 W32 CMDA5 <21,22>
- FBA_CMD6 W33 CMDA6 <21,22>
- FBA_CMD7 W33 CMDA7 <21,22>
- FBA_CMD8 W31 CMDA8 <21,22>
- FBA_CMD9 W34 CMDA9 <21,22>
- FBA_CMD10 U34 CMDA10 <21,22>
- FBA_CMD11 U35 CMDA11 <21,22>
- FBA_CMD12 U32 CMDA12 <21,22>
- FBA_CMD13 T32 CMDA13 <21,22>
- FBA_CMD14 T33 CMDA14 <21,22>
- FBA_CMD15 W30 CMDA15 <21,22>
- FBA_CMD16 AB30 CMDA16 <22>
- FBA_CMD17 AA30 X CMDA17 <22>
- FBA_CMD18 AB31 CMDA18 <22>
- FBA_CMD19 AA32 CMDA19 <22>
- FBA_CMD20 AB33 CMDA20 <21,22>
- FBA_CMD21 Y32 CMDA21 <21,22>
- FBA_CMD22 Y33 CMDA22 <21,22>
- FBA_CMD23 AB34 CMDA23 <21,22>
- FBA_CMD24 AB35 CMDA24 <21,22>
- FBA_CMD25 Y35 CMDA25 <21,22>
- FBA_CMD26 W35 CMDA26 <21,22>
- FBA_CMD27 Y34 CMDA27 <21,22>
- FBA_CMD28 Y31 CMDA28 <21,22>
- FBA_CMD29 Y30 CMDA29 <21,22>
- FBA_CMD30 W29 CMDA30 <21,22>
- FBA_CMD31 Y29 X CMDA31 <21,22>
- FBA_DQM0 P32 DOMA0 <21,22>
- FBA_DQM1 H34 DOMA1 <21,22>
- FBA_DQM2 J30 DOMA2 <21,22>
- FBA_DQM3 P30 DOMA3 <21,22>
- FBA_DQM4 AF32 DOMA4 <21,22>
- FBA_DQM5 AL32 DOMA5 <21,22>
- FBA_DQM6 AL34 DOMA6 <21,22>
- FBA_DQM7 AF35 DOMA7 <21,22>
- FBA_DQS_RN0 L35 DOSA0 <21,22>
- FBA_DQS_RN1 G35 DOSA1 <21,22>
- FBA_DQS_RN2 H31 DOSA2 <21,22>
- FBA_DQS_RN3 N32 DOSA3 <21,22>
- FBA_DQS_RN4 AD32 DOSA4 <21,22>
- FBA_DQS_RN5 AJ31 DOSA5 <21,22>
- FBA_DQS_RN6 AJ35 DOSA6 <21,22>
- FBA_DQS_RN7 AC34 DOSA7 <21,22>
- FBA_DQS_WP0 L34 DOSA0 <21,22>
- FBA_DQS_WP1 H35 DOSA1 <21,22>
- FBA_DQS_WP2 J32 DOSA2 <21,22>
- FBA_DQS_WP3 N31 DOSA3 <21,22>
- FBA_DQS_WP4 AE31 DOSA4 <21,22>
- FBA_DQS_WP5 AJ32 DOSA5 <21,22>
- FBA_DQS_WP6 AJ34 DOSA6 <21,22>
- FBA_DQS_WP7 AC33 DOSA7 <21,22>
- FBA_WCK0 P29 X CLKA0 <21>
- FBA_WCK0_N R29 X CLKA0# <21>
- FBA_WCK1 L29 X CLKA1 <22>
- FBA_WCK1_N M29 X CLKA1# <22>
- FBA_WCK2 AG29 X CLKA1 <22>
- FBA_WCK2_N AH29 X CLKA1# <22>
- FBA_WCK3 AD29 X CLKA1 <22>
- FBA_WCK3_N AE29 X CLKA1# <22>
- FBA_CLK0 T32 CLKA0 <21>
- FBA_CLK0# T31 CLKA0# <21>
- FBA_CLK1 AC31 CLKA1 <22>
- FBA_CLK1# AC30 CLKA1# <22>

Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	A8
CMD8	A8	A8
CMD2	CS0#_L	A6
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2





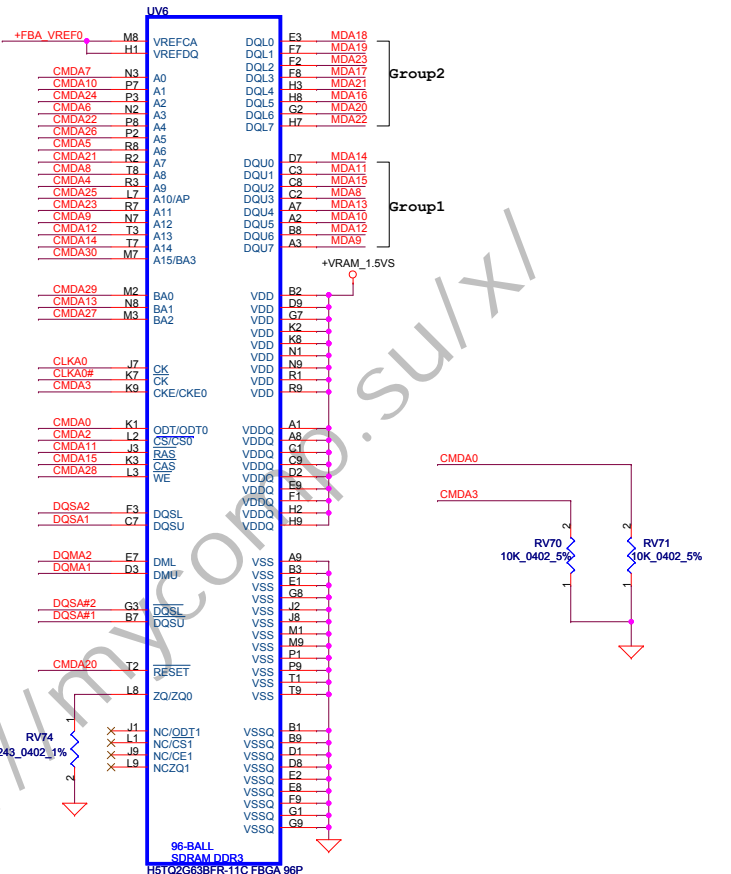
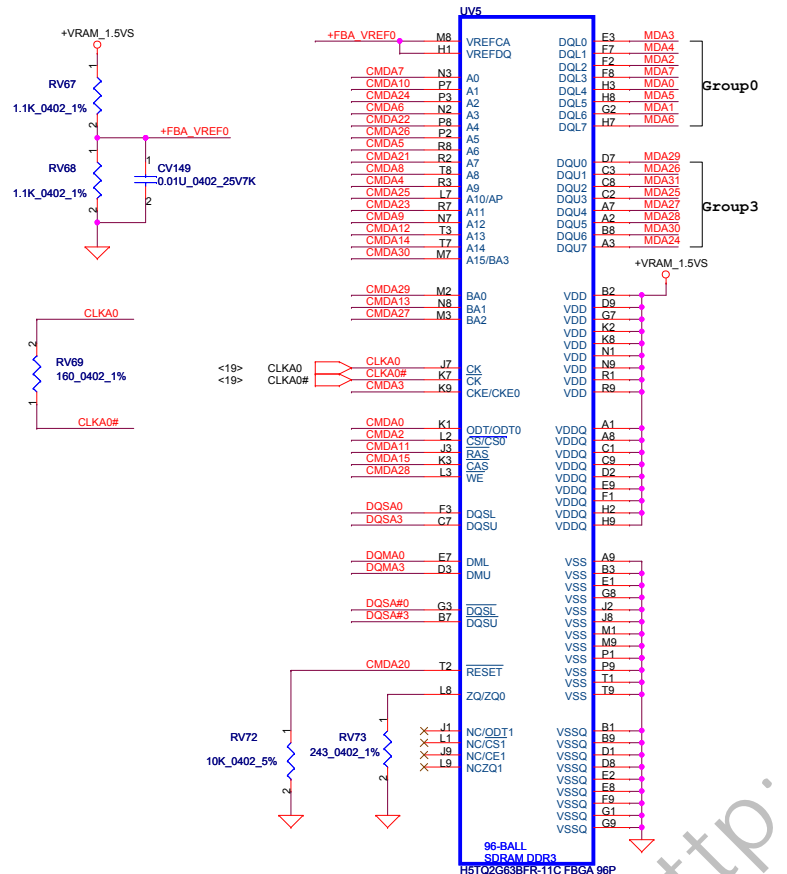
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition A - Lower 32 bits

Support N12P-GV/GS
Support Max VRAM 2G

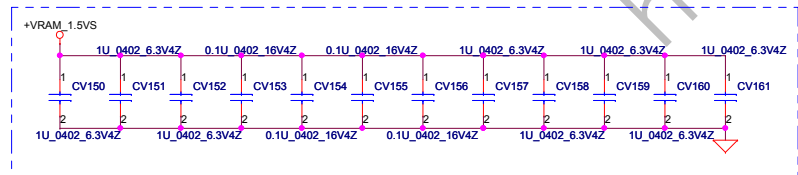
- MDA[0..63] <19..22>
- CMDA[30..0] <19..22>
- DQMA[7..0] <19..22>
- DQSA[7..0] <19..22>
- DQSA# [7..0] <19..22>



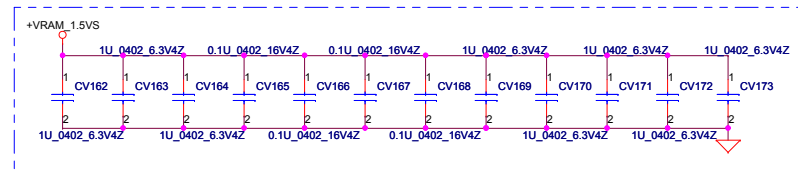
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

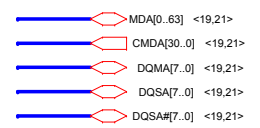
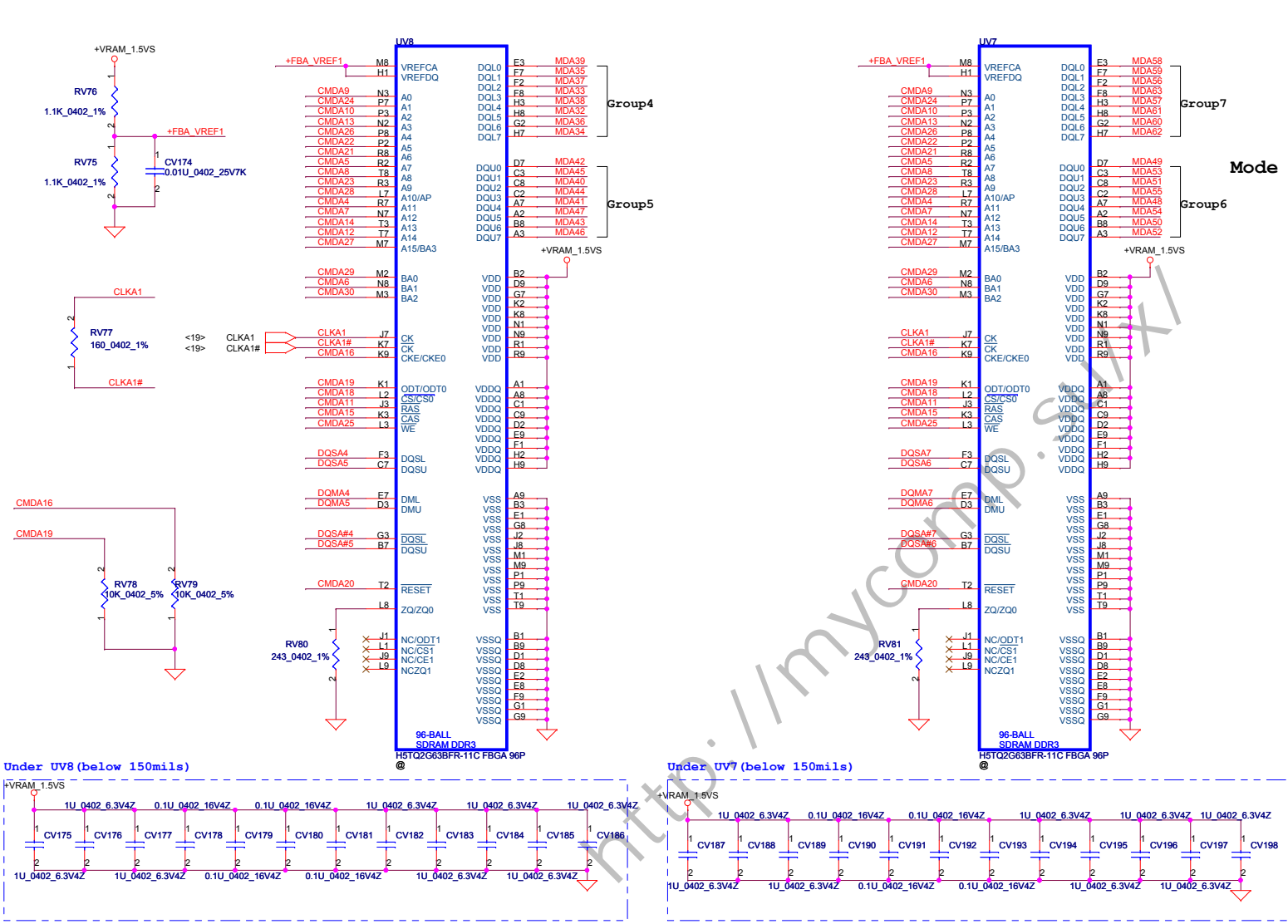
Under UV5 (below 150mils)



Under UV6 (below 150mils)



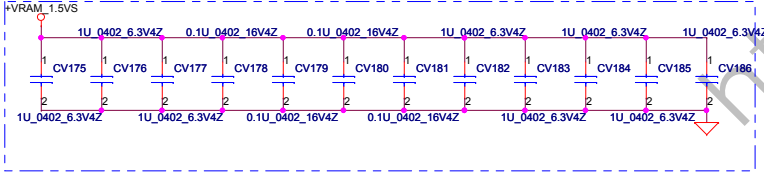
Memory Partition A - Upper 32 bits



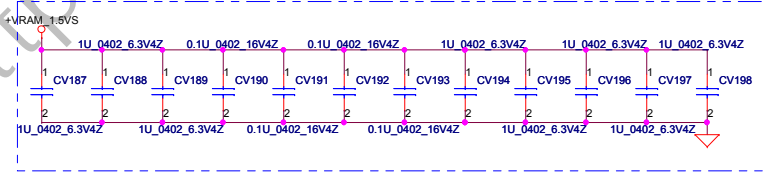
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Under UV8 (below 150mils)



Under UV7 (below 150mils)

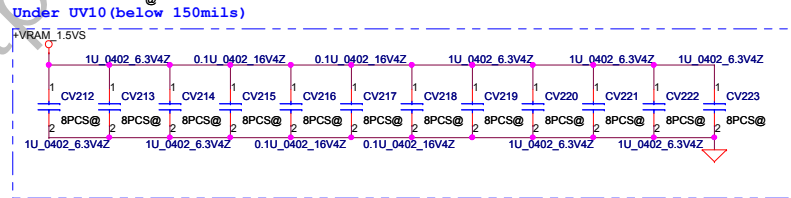
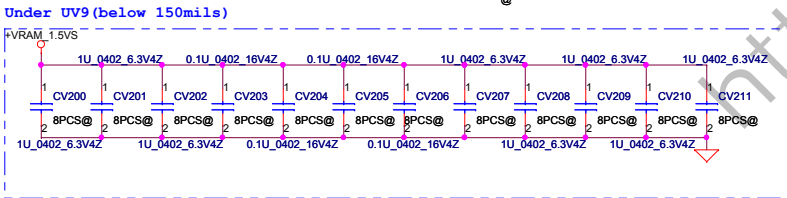
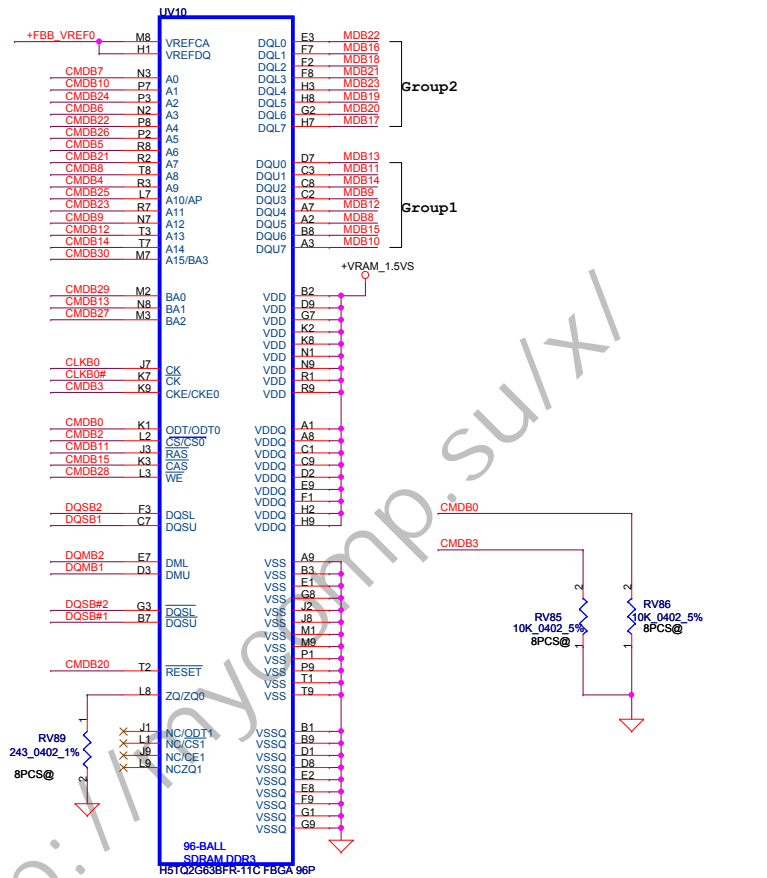
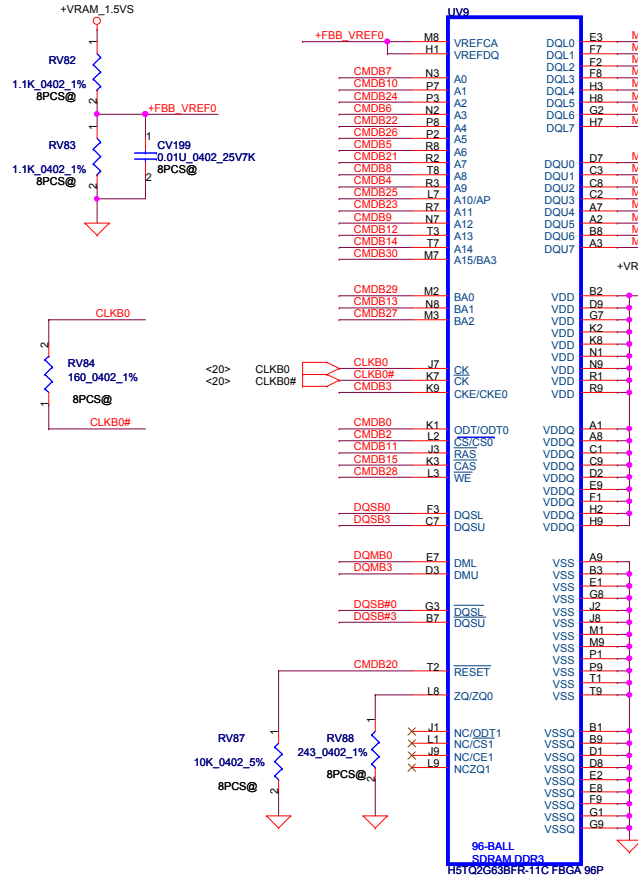


Memory Partition C - Lower 32 bits



Mode E - Mirror Mode Mapping

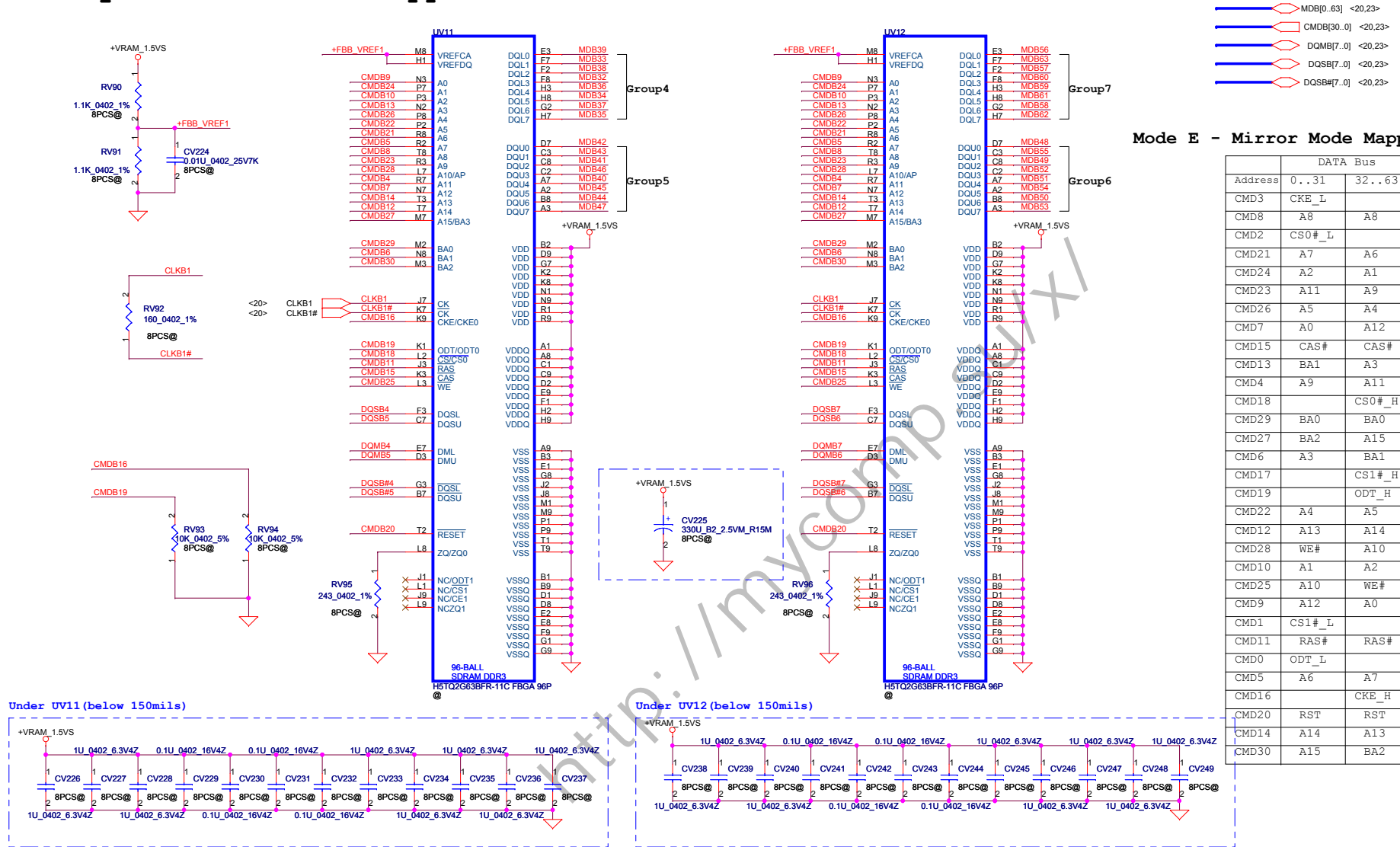
Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



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		2011/12/03
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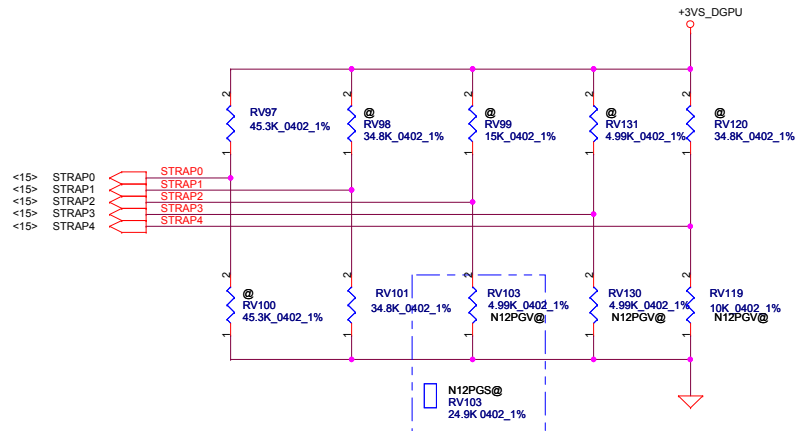
Title		
Compal Electronics, Inc.		
VGA(10/12)-VRAM C Lower		
Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1
Date:	Friday, January 21, 2011	Sheet 23 of 58

Memory Partition C - Upper 32 bits



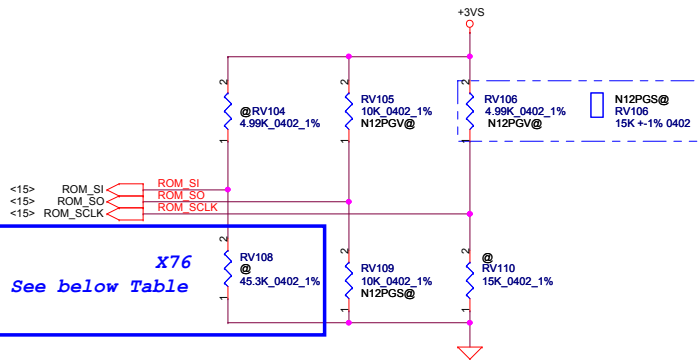
Mode E - Mirror Mode Mapping

Address	DATA Bus	
CMD3	CKE_L	32..63
CMD8	A8	A8
CMD2	CS0#_L	A6
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT#_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



X76
See below Table

GPU	DeviceID	ROM_SI	ROM_SCLK	ROM_SO	STRAP0
N12P-GS	0x0DF4	Below Table	Pull up 15K	Pull down 10K	Pull up 45K
N12P-GV	0x1050	Below Table	Pull up 5K	Pull up 10K	Pull up 45K

GPU	DeviceID	STRAP1	STRAP2	STRAP3	STRAP4
N12P-GS	0x0DF4	Pull down 35K	Pull down 25K		
N12P-GV	0x1050	Pull down 35K	Pull down 5K	Pull down 5K	Pull down 10K

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

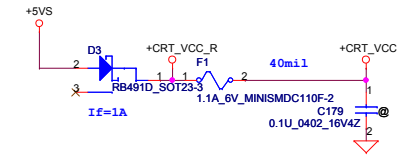
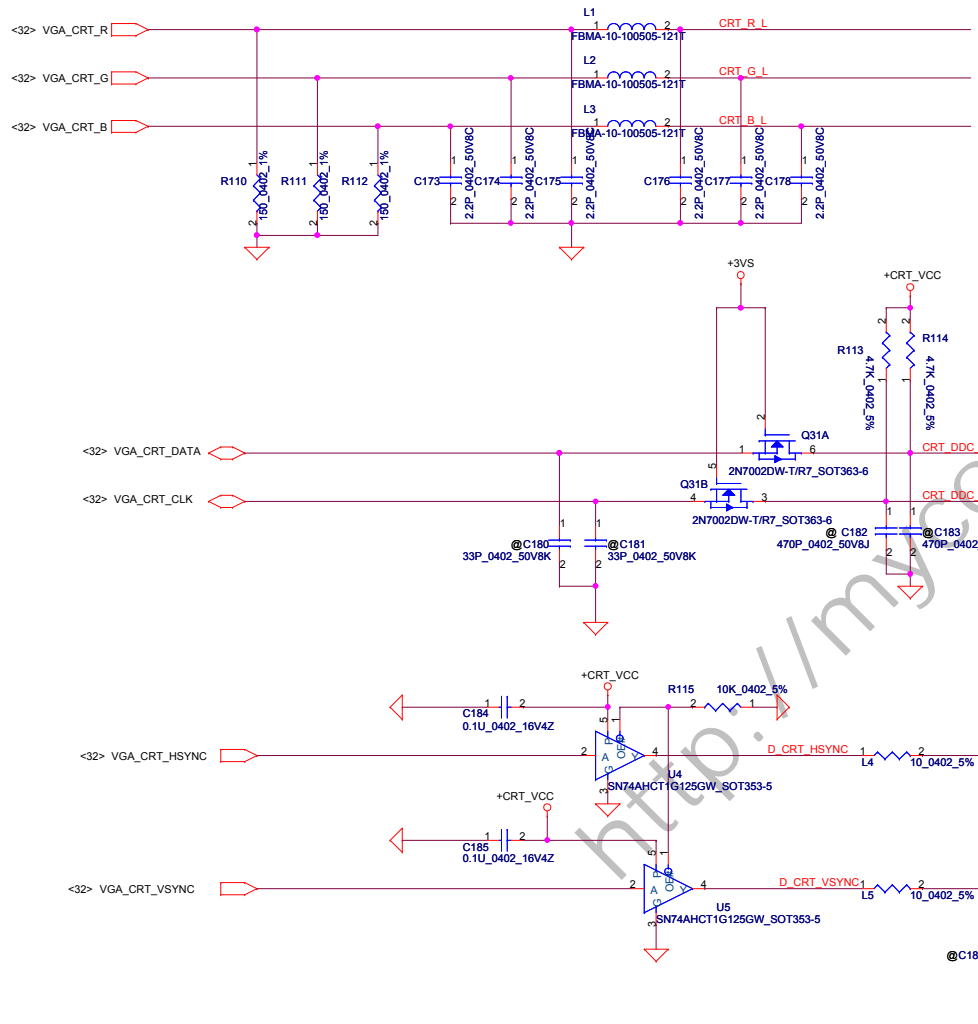
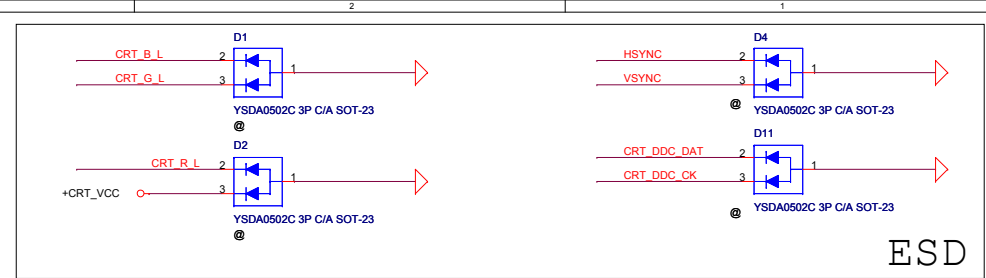
SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

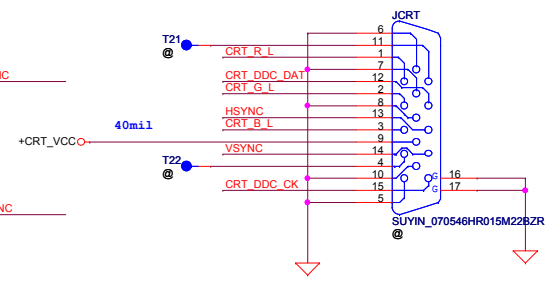
VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

GPU	DDR3 Type	VRAM	RAMCFG[3..0]	RV108
N12P-GS	64M16 900MHz	Hynix H5TQ1G63DFR-11C SA000041S20	512MB 0010 PD 15K	SD034154280
		Samsung K4W1G1646E-HC11 SA000041T00	1GB 0010 PD 15K	SD034200280
	128M16 900MHz	Hynix H5TQ2G63BFR-11C SA00003Y000	512MB 0011 PD 20K	SD034200280
		Samsung K4W2G1646C-HC11 SA000047Q00	1GB 0011 PD 20K	SD034200280
		Hynix H5TQ2G63BFR-11C SA00003Y000	1GB 0110 PD 34.8K	SD034348280
		Samsung K4W2G1646C-HC11 SA00003M400	2GB 0110 PD 34.8K	SD034348280
N12P-GV	64M16 800MHz	Hynix H5TQ1G63DFR-12C SA0000324C0	1GB 0111 PD 45.3K	SD034453280
		Samsung K4W1G1646G-BC12 SA00004HS00	512MB 0010 PD 15K	SD034154280
	128M16 800MHz	Hynix H5TQ2G63BFR-12C SA00003VS00	512MB 0011 PD 20K	SD034200280
		Samsung K4W2G1646C-HC12 SA00003M400	1GB 0110 PD 34.8K	SD034348280
		Hynix H5TQ2G63BFR-12C SA00003VS00	1GB 0111 PD 45.3K	SD034453280
		Samsung K4W2G1646C-HC12 SA00003M400	2GB 0111 PD 45.3K	SD034453280

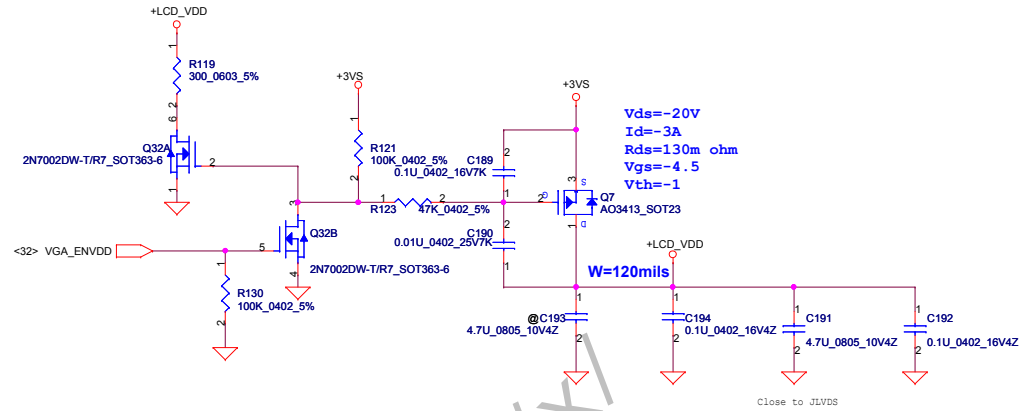
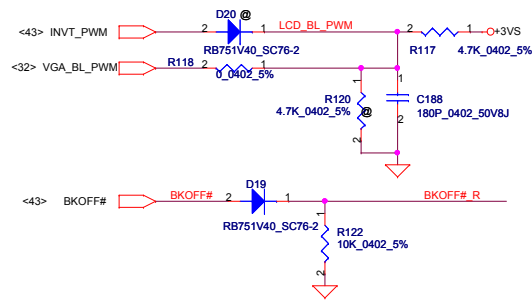
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Size	Document Number	Rev	PBL80 LA-7441P M/B	
Date:	Friday, January 21, 2011	Sheet	25	of 58



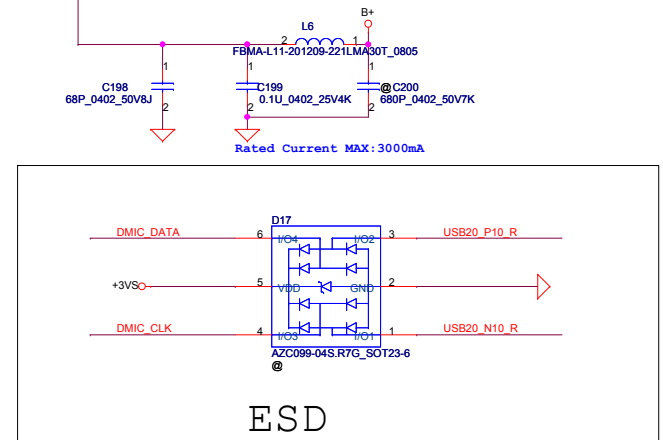
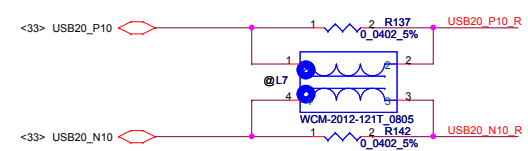
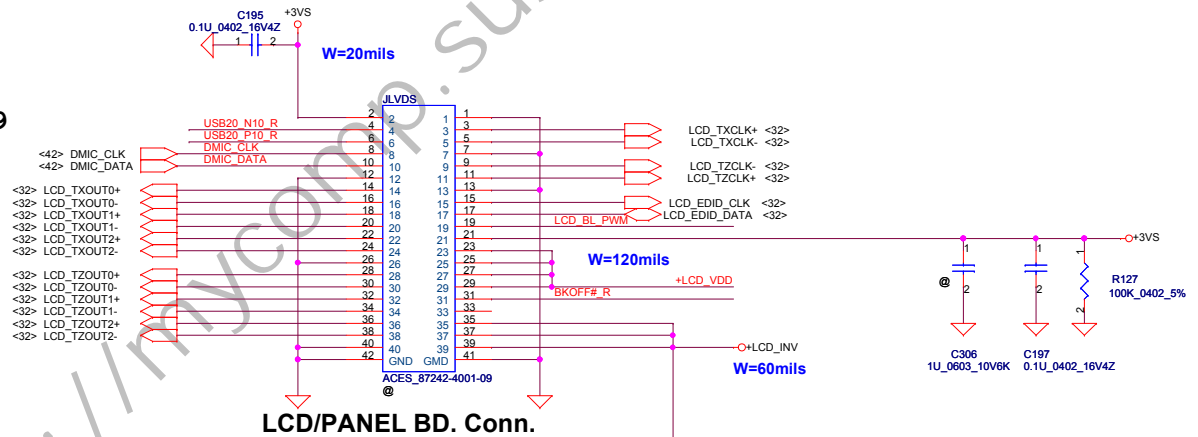
CRT CONNECTOR



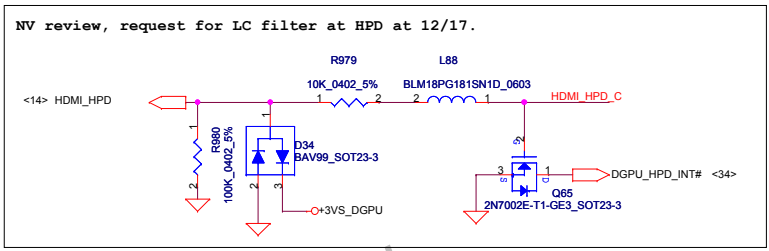
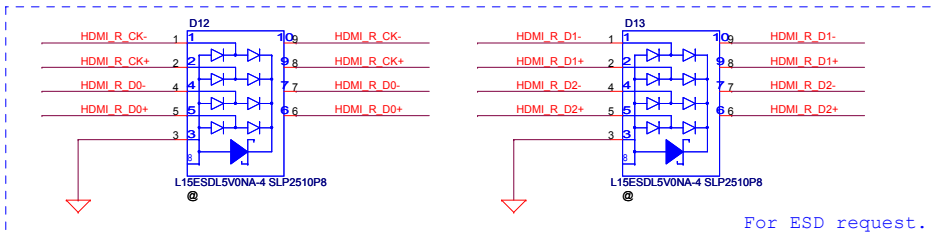
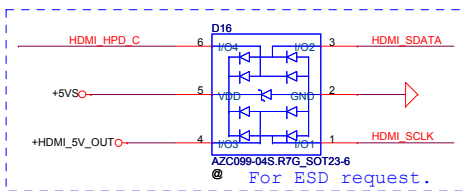
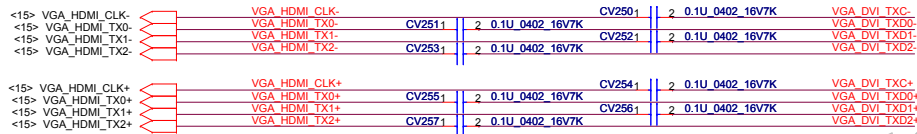
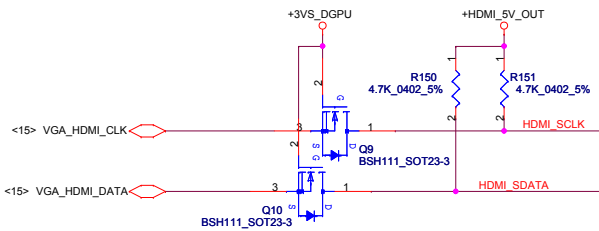
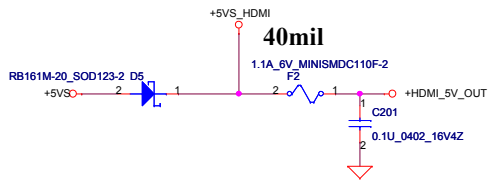
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Date: Friday, January 21, 2011				Sheet 26 of 58



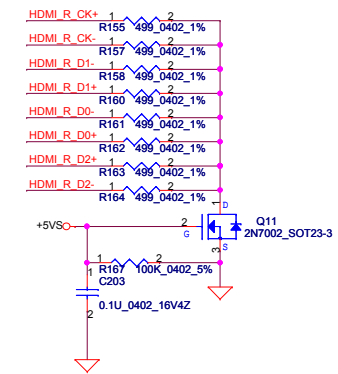
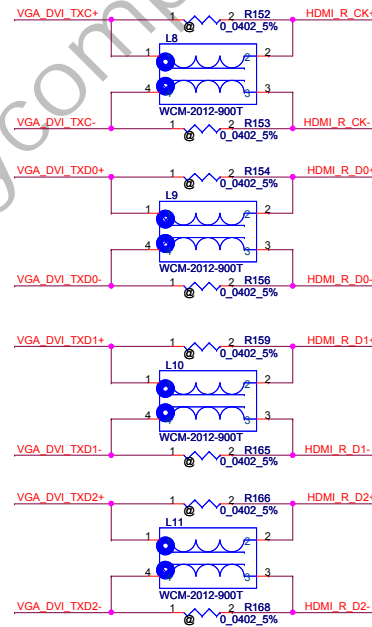
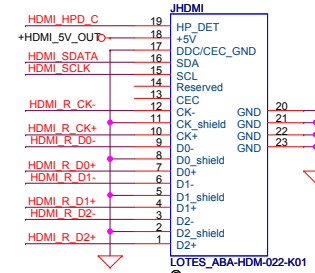
Dual Channel LVDS Support 18.4" HD/FHD 16:9



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				PBL80 LA-7441P M/B	
				Date:	Friday, January 21, 2011
				Sheet	27 of 58

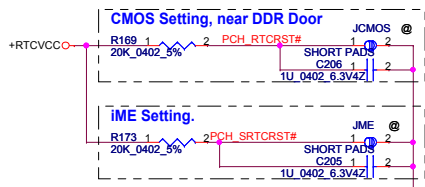


HDMI Connector



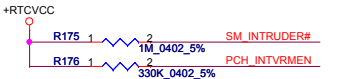
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Issued Date	2010/12/03	Deciphered Date	2011/12/03	Title
				HDMI Connector
				Size Document Number
				PBL80 LA-7441P M/B
				Rev 0.1
				Date: Friday, January 21, 2011 Sheet 28 of 58

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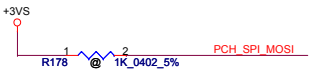


Integrated SUS 1.05V VRM Enable

PCH_INTRVMEN High - Enable Internal VRs (must be always pulled high)



PCH_SPKR High = Enable (No Reboot) Low = Disabled (Default) *



ITPM Enabled Internal: Pull down 20k

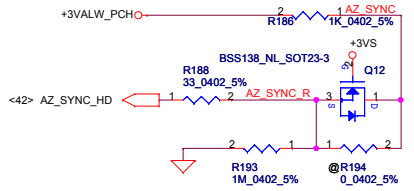
SPI_MOSI High = Enabled Low = Disabled (Default) *

HDA_SYNC

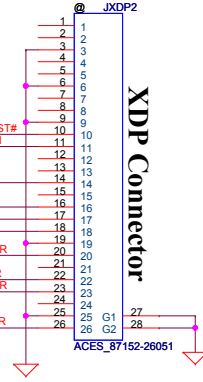
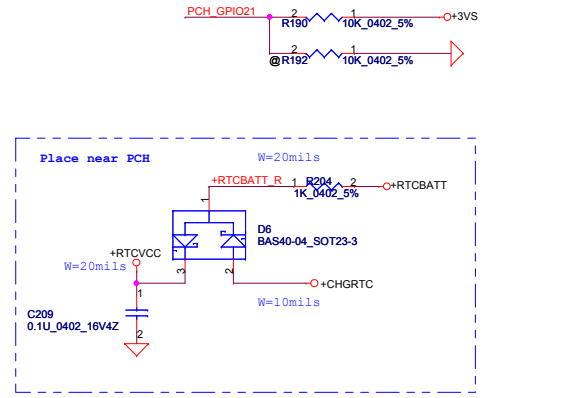
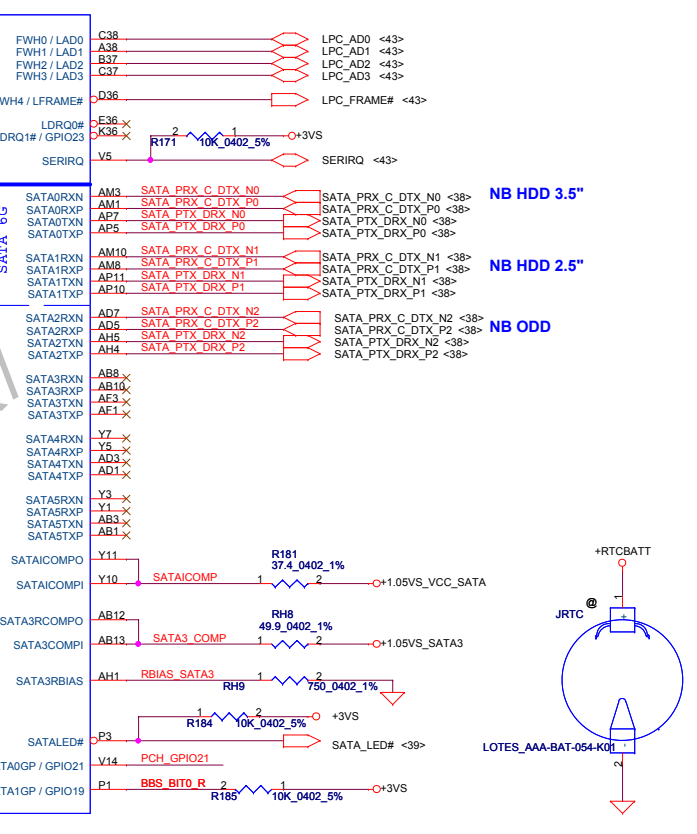
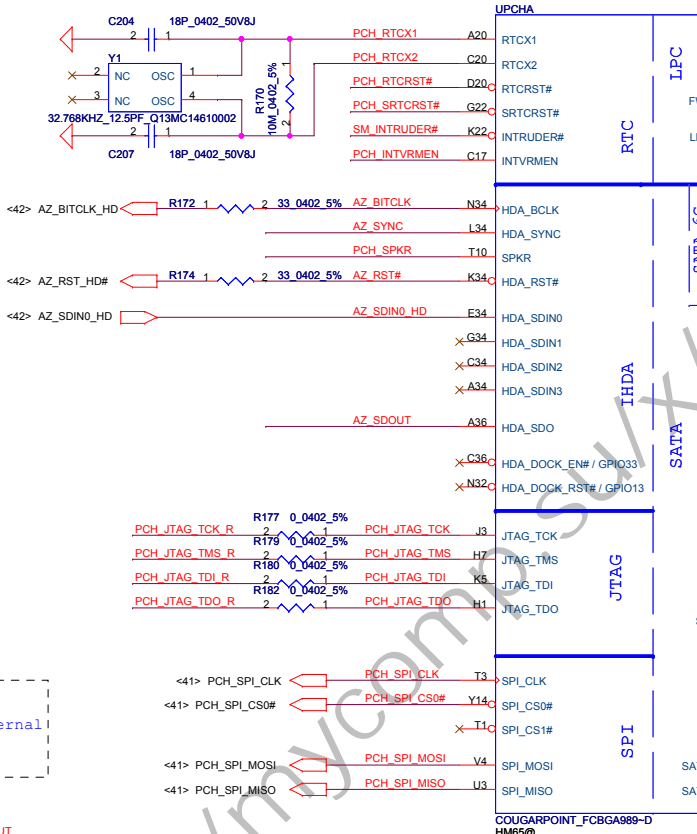
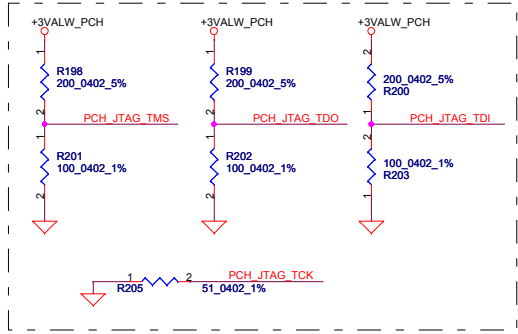
This signal has a weak internal pull down.
 *H=>On Die PLL is supplied by 1.5V
 L=>On Die PLL is supplied by 1.8V

HDA_SDO

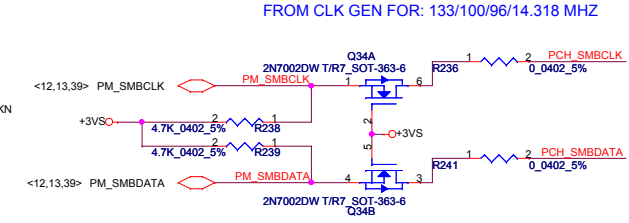
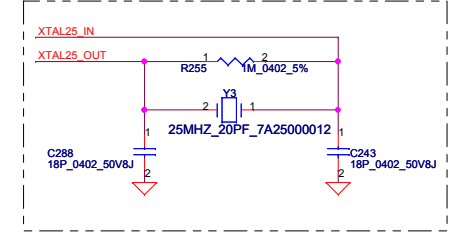
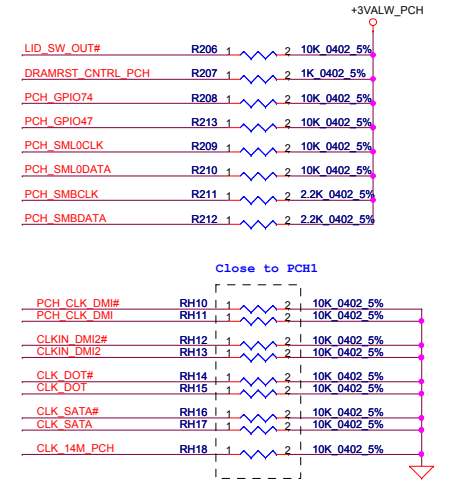
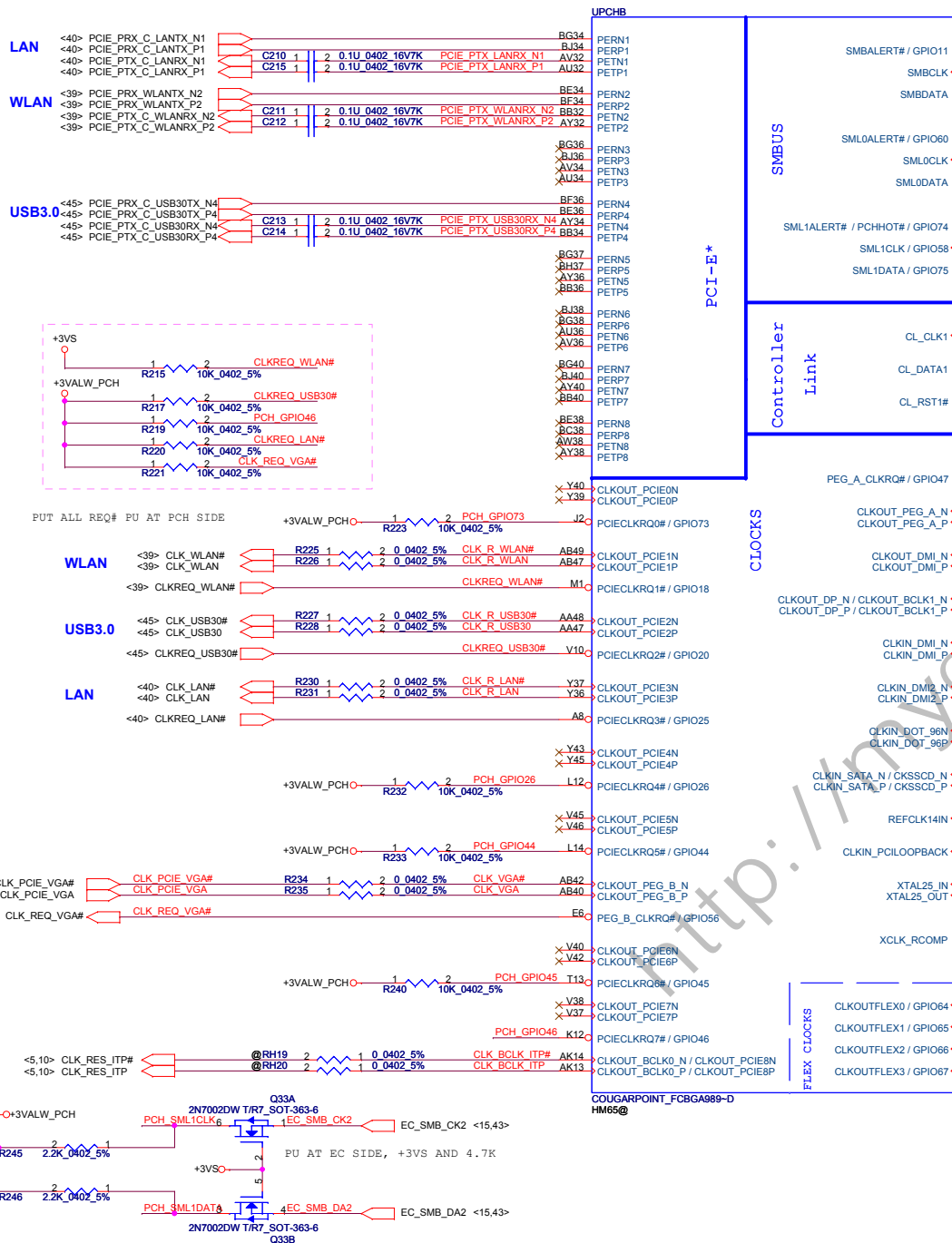
This signal has a weak internal pull down.
 This signal can't PU



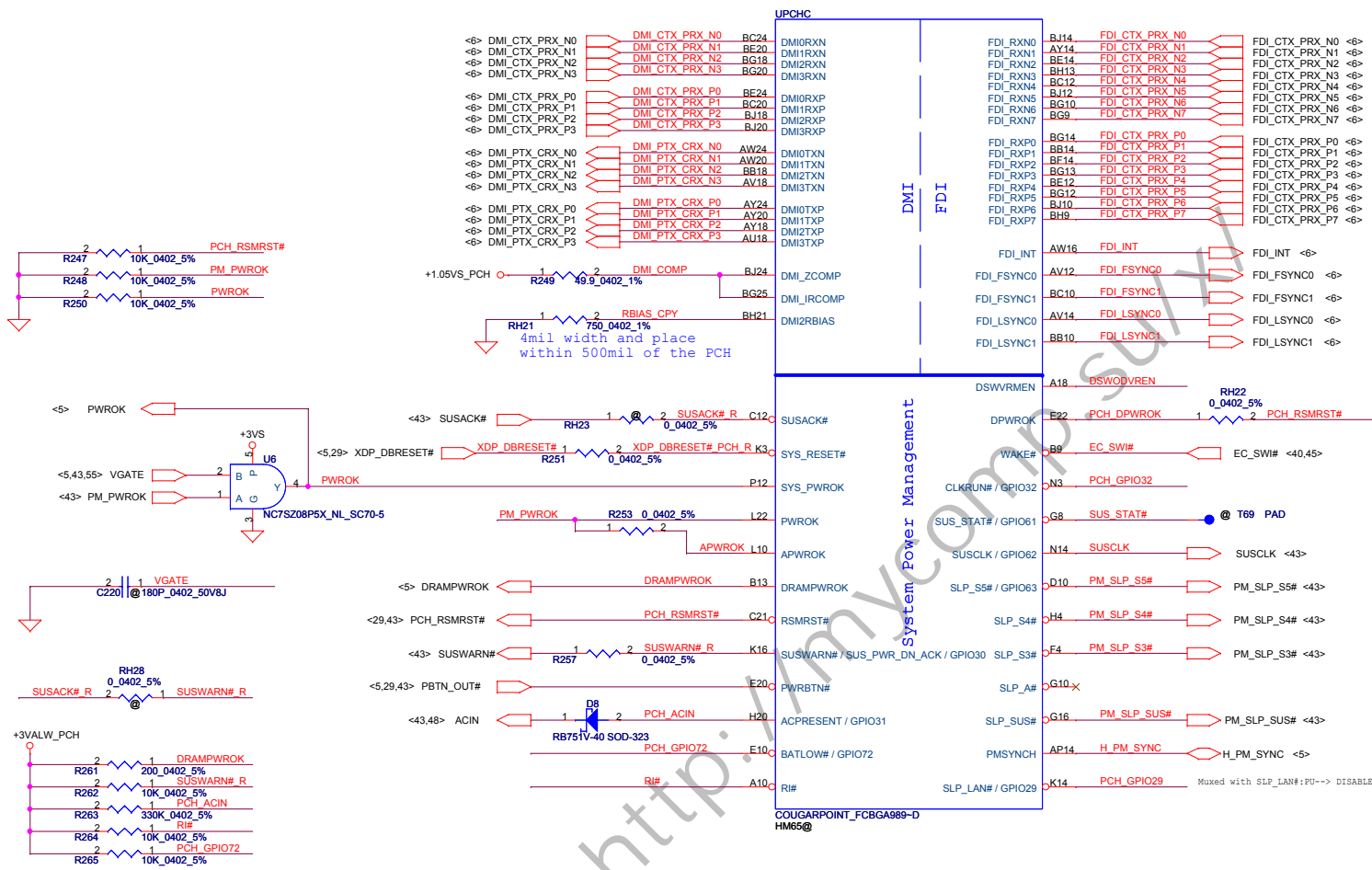
0604 CHANG AZ_SYNC AND AZ_SDOUT TO FIT INTEL SPEC



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		PBL80 LA-7441P M/B	0.1	
Date:	Friday, January 21, 2011	Sheet	29	of 58



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Size	Document Number	PBL80 LA-7441P M/B		Rev
Custom				0.1
Date:	Friday, January 21, 2011	Sheet	30	of 58



If strap is sampled high, the integrated Deep S4/S5 Wall (DSW) On-Die VR mode is enabled.

DSWODVREN - On Die DSW VR Enable
 * H: Enable
 L: Disable

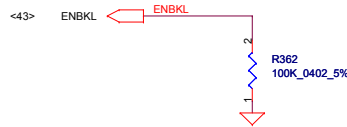
0608 CHANGE PM_CLKRUN# FROM NOT PD OR PU TO PU +3VS

PCH_GPIO32 R256 1 2 8.2K 0.402 5%

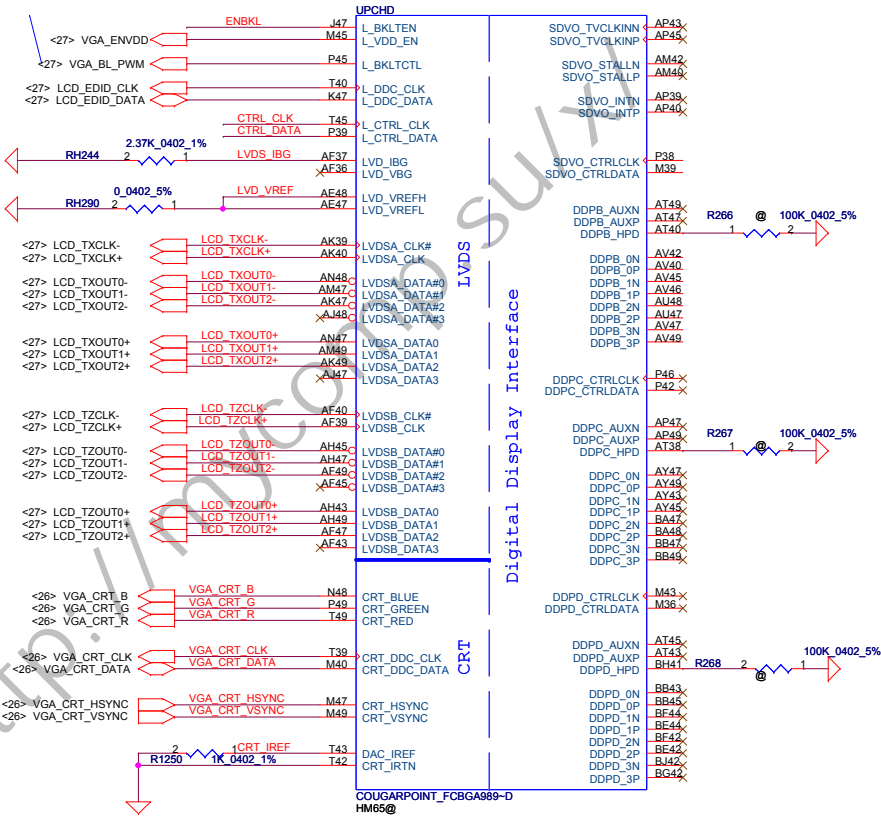
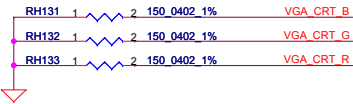
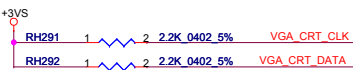
+3VALW_PCH
 EC_SWI# R259 1 2 10K 0.402 5%
 PCH_GPIO29 R260 1 2 10K 0.402 5%

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Cougar Point(3/9)-DMI/FDI/PWM		
Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1
Date:	Friday, January 21, 2011	Sheet 31 of 58



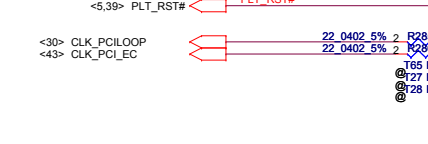
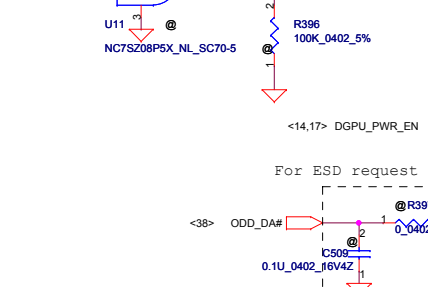
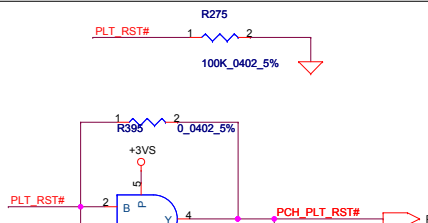
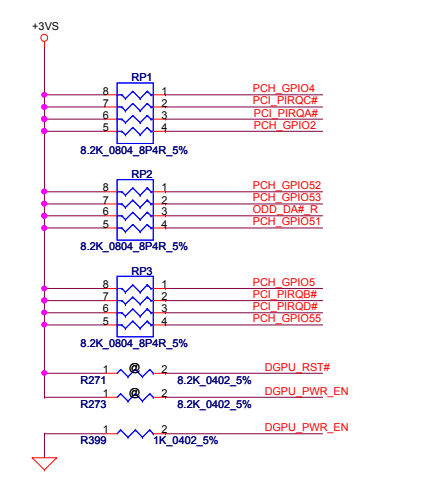
Pull high at LVDS conn side.



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		2011/12/03

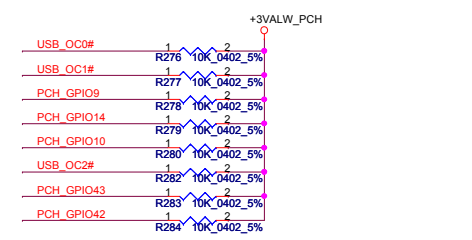
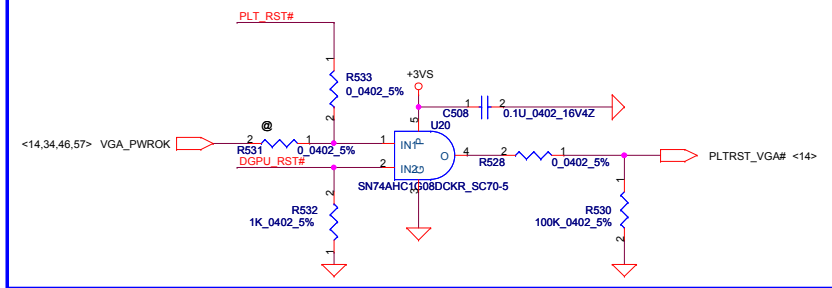
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Cougar Point(4/9)-CRT/LVDS/HDMI/DP		
Size	Document Number	Rev
Custom	PBL80 LA-7441P M/B	0.1
Date:	Friday, January 21, 2011	Sheet 32 of 58



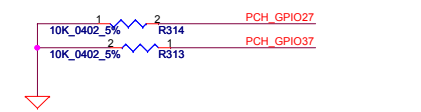
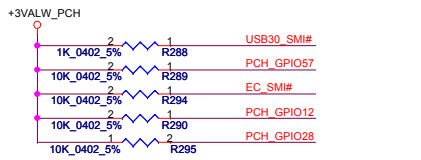
- UPCHE
- TP1
 - TP2
 - TP3
 - TP4
 - TP5
 - TP6
 - TP7
 - TP8
 - TP9
 - TP10
 - TP11
 - TP12
 - TP13
 - TP14
 - TP15
 - TP16
 - TP17
 - TP18
 - TP19
 - TP20
- RSVD
- TP21
 - TP22
 - TP23
 - TP24
 - TP25
 - TP26
 - TP27
 - TP28
 - TP29
 - TP30
 - TP31
 - TP32
 - TP33
 - TP34
 - TP35
 - TP36
 - TP37
 - TP38
 - TP39
 - TP40
- NVRAM
- NV_CE#0
 - NV_CE#1
 - NV_CE#2
 - NV_CE#3
 - NV_DQS0
 - NV_DQS1
 - NV_DQ0 / NV_I00
 - NV_DQ1 / NV_I01
 - NV_DQ2 / NV_I02
 - NV_DQ3 / NV_I03
 - NV_DQ4 / NV_I04
 - NV_DQ5 / NV_I05
 - NV_DQ6 / NV_I06
 - NV_DQ7 / NV_I07
 - NV_DQ8 / NV_I08
 - NV_DQ9 / NV_I09
 - NV_DQ11 / NV_I011
 - NV_DQ12 / NV_I012
 - NV_DQ13 / NV_I013
 - NV_DQ14 / NV_I014
 - NV_DQ15 / NV_I015
- PCI
- PIRQA#
 - PIRQB#
 - PIRQC#
 - PIRQD#
 - REQ1# / GPIO50
 - REQ2# / GPIO52
 - REQ3# / GPIO54
 - GNT1# / GPIO51
 - GNT2# / GPIO53
 - GNT3# / GPIO55
 - PIRQE# / GPIO2
 - PIRQF# / GPIO3
 - PIRQH# / GPIO4
 - PIRQI# / GPIO5
- USB
- USBP0N
 - USBP0P
 - USBP1N
 - USBP1P
 - USBP2N
 - USBP2P
 - USBP3N
 - USBP3P
 - USBP4N
 - USBP4P
 - USBP5N
 - USBP5P
 - USBP6N
 - USBP6P
 - USBP7N
 - USBP7P
 - USBP8N
 - USBP8P
 - USBP9N
 - USBP9P
 - USBP10N
 - USBP10P
 - USBP11N
 - USBP11P
 - USBP12N
 - USBP12P
 - USBP13N
 - USBP13P

- AY7
- AV7
- CAU3
- CG4
- AT10
- BC8
- AU2
- AT4
- AT3
- AT1
- AY3
- AV3
- AV1
- BA3
- BB5
- BB3
- BB7
- BB9
- BD4
- BF6
- AV5
- AY1
- AV10
- AT8
- AV5
- BA2
- AT12
- BF3
- C24
- A24
- C25
- B25
- C26
- A26
- K28
- H28
- E28
- D28
- C28
- A28
- B29
- N28
- M28
- L30
- K30
- G30
- E30
- C30
- A30
- L32
- K32
- C32
- E32
- C32
- A32
- C33
- B33
- A14
- K20
- OC1#
- OC2#
- OC3#
- OC4#
- OC5#
- OC6#
- OC7#
- OC0# / GPIO50
- OC1# / GPIO40
- OC2# / GPIO41
- OC3# / GPIO42
- OC4# / GPIO43
- OC5# / GPIO49
- OC6# / GPIO10
- OC7# / GPIO14
- USB20_N0
- USB20_P0
- USB20_N1
- USB20_P1
- USB20_N2
- USB20_P2
- USB20_N4
- USB20_P4
- USB20_N10
- USB20_P10
- USB20_N11
- USB20_P11
- USB20_N13
- USB20_P13
- USBBIAS
- USBBIAS
- USB_OC0#
- USB_OC1#
- USB_OC2#
- PCH_GPIO42
- PCH_GPIO43
- PCH_GPIO9
- PCH_GPIO10
- PCH_GPIO14



Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Boot BIOS Destination
GNT1# / GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC

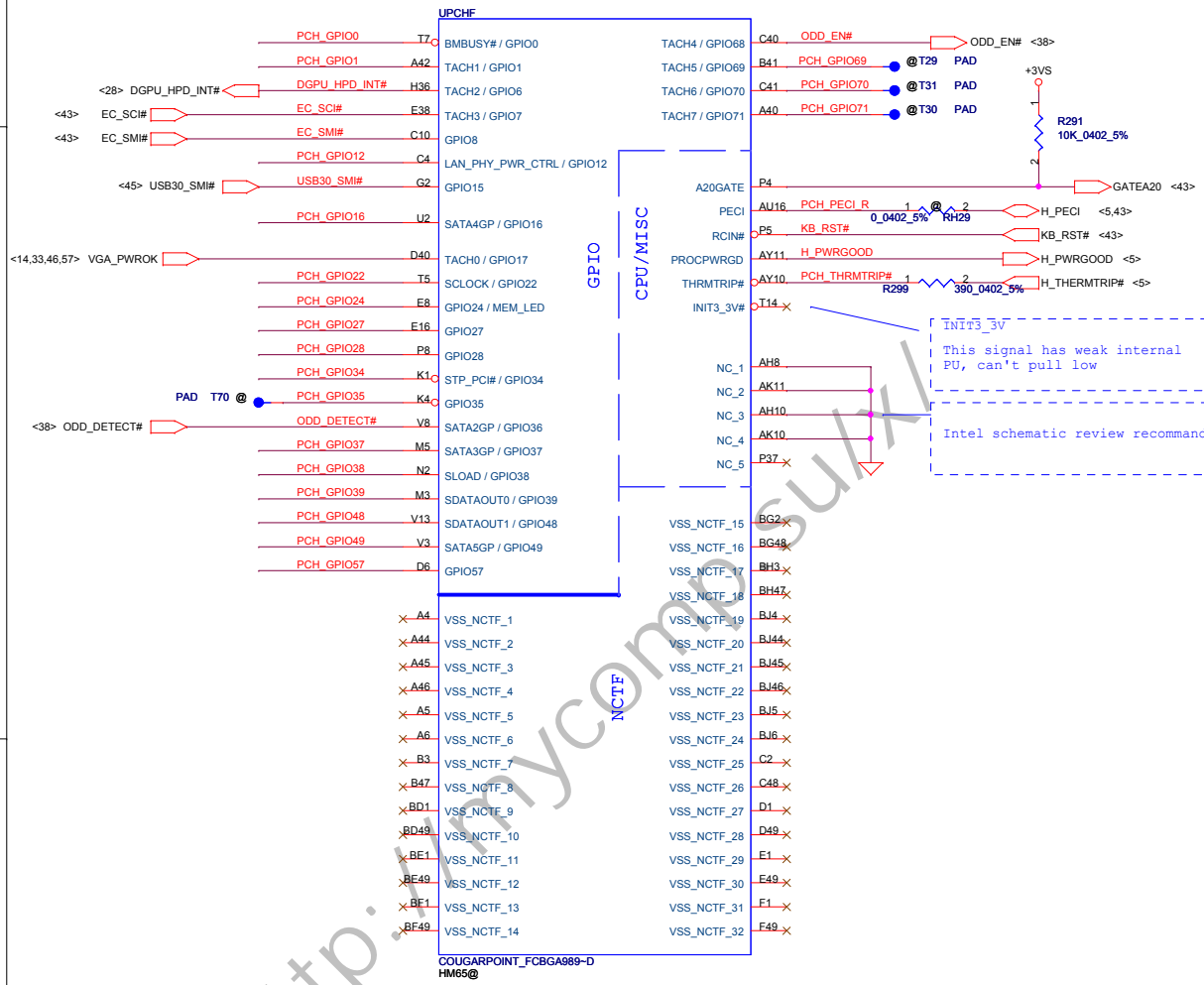
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<p>Compal Electronics, Inc. Cougar Point(5/9)-USB/PCI/NAND/STRAP</p>			Rev 0.1
Size Custom	PBL80 LA-7441P M/B		Date: Friday, January 21, 2011 Sheet 33 of 58



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

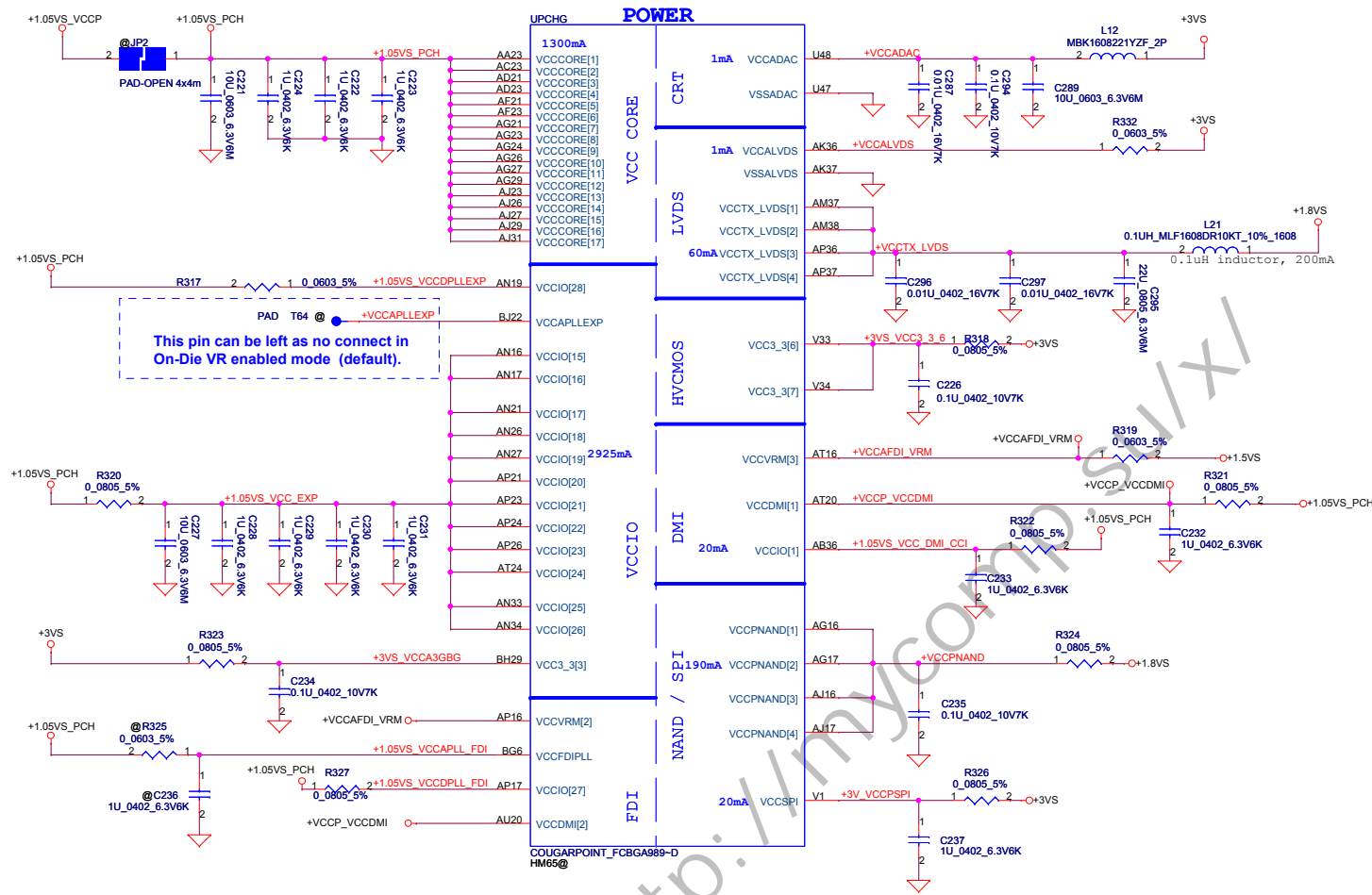
GPIO8
Integrated Clock Chip Enable
H ; Disable
L ; Enable
* L ; Enable

Reserve for ICC enable.



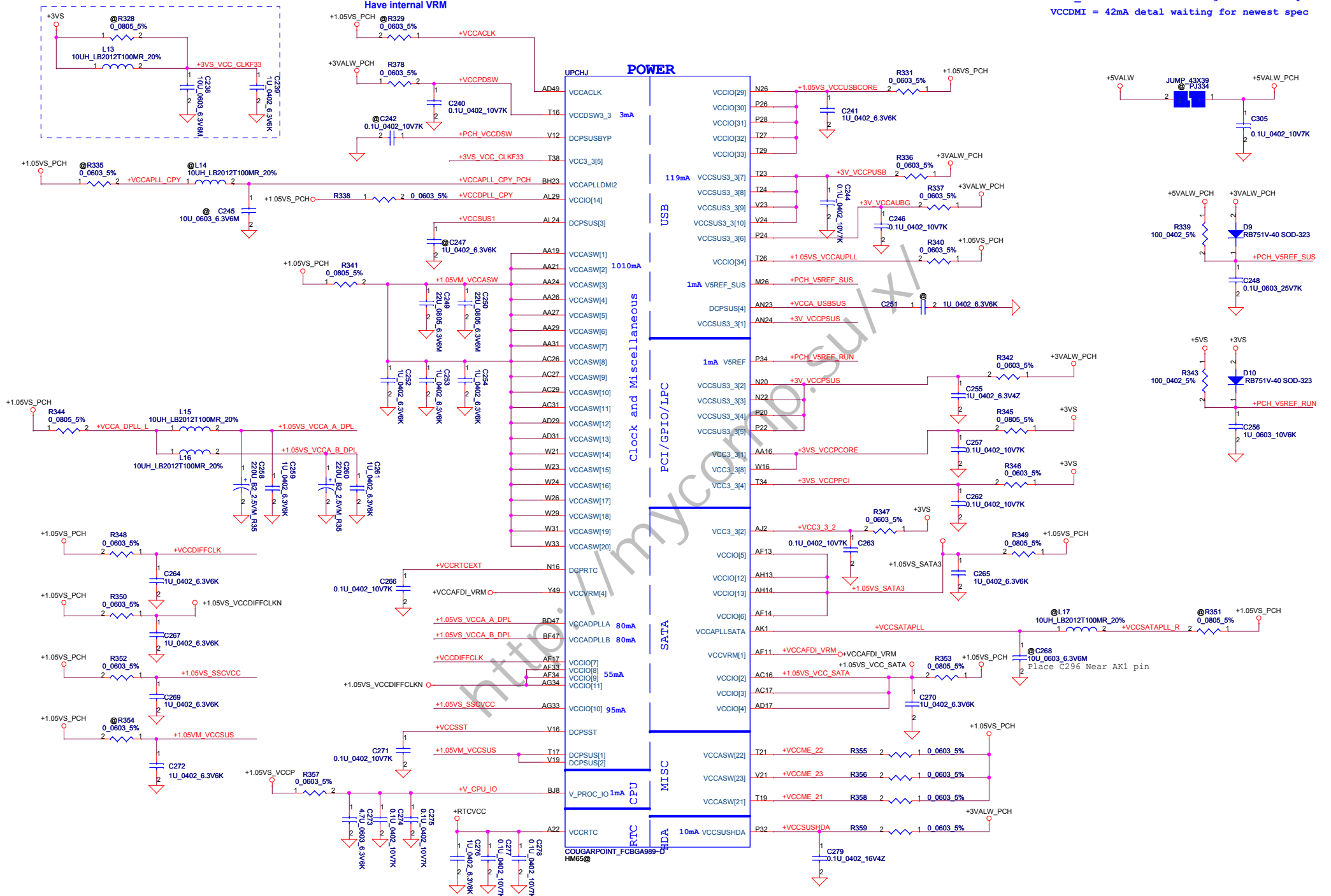
http://www.ycom.com/sux/

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				Custom	0.1
				PBL80 LA-7441P M/B	
				Date:	Friday, January 21, 2011
				Sheet	34 of 58



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSFI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec



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Title Cougar Point(8/9)-PWR2		
Size Custom	Document Number PBL80 LA-7441P M/B	Rev 0.1
Date Friday, January 21, 2011	Sheet 36	of 58

UPCHH		AK38	
H5	VSS[0]		
AA17	VSS[1]	VSS[80]	AK4
AA2	VSS[2]	VSS[81]	AK42
AA3	VSS[3]	VSS[82]	AK46
AA33	VSS[4]	VSS[83]	AK6
AA34	VSS[5]	VSS[84]	AL16
AB11	VSS[6]	VSS[85]	AL17
AB14	VSS[7]	VSS[86]	AL19
AB39	VSS[8]	VSS[87]	AL2
AB4	VSS[9]	VSS[88]	AL21
AB43	VSS[10]	VSS[89]	AL23
AB5	VSS[11]	VSS[90]	AL26
AB7	VSS[12]	VSS[91]	AL27
AC19	VSS[13]	VSS[92]	AL31
AC2	VSS[14]	VSS[93]	AL33
AC21	VSS[15]	VSS[94]	AL34
AC24	VSS[16]	VSS[95]	AL48
AC33	VSS[17]	VSS[96]	AM11
AC34	VSS[18]	VSS[97]	AM14
AC48	VSS[19]	VSS[98]	AM36
AD10	VSS[20]	VSS[99]	AM39
AD11	VSS[21]	VSS[100]	AM43
AD12	VSS[22]	VSS[101]	AM45
AD13	VSS[23]	VSS[102]	AM46
AD19	VSS[24]	VSS[103]	AM7
AD24	VSS[25]	VSS[104]	AN2
AD26	VSS[26]	VSS[105]	AN29
AD27	VSS[27]	VSS[106]	AN3
AD33	VSS[28]	VSS[107]	AN31
AD34	VSS[29]	VSS[108]	AP12
AD36	VSS[30]	VSS[109]	AP19
AD37	VSS[31]	VSS[110]	AP28
AD38	VSS[32]	VSS[111]	AP30
AD39	VSS[33]	VSS[112]	AP38
AD4	VSS[34]	VSS[113]	AP4
AD42	VSS[35]	VSS[114]	AP42
AD43	VSS[36]	VSS[115]	AP46
AD45	VSS[37]	VSS[116]	AR2
AD46	VSS[38]	VSS[117]	AR48
AD8	VSS[39]	VSS[118]	AT11
AE2	VSS[40]	VSS[119]	AT18
AE3	VSS[41]	VSS[120]	AT22
AE3	VSS[42]	VSS[121]	AT26
AF10	VSS[43]	VSS[122]	AT30
AF12	VSS[44]	VSS[123]	AT32
AD14	VSS[45]	VSS[124]	AT34
AD16	VSS[46]	VSS[125]	AT42
AF18	VSS[47]	VSS[126]	AT46
AF19	VSS[48]	VSS[127]	AT7
AF24	VSS[49]	VSS[128]	H10
AF26	VSS[50]	VSS[129]	H17
AF27	VSS[51]	VSS[130]	BH19
AF31	VSS[52]	VSS[131]	H11
AF38	VSS[53]	VSS[132]	H15
AF4	VSS[54]	VSS[133]	BH17
AF4	VSS[55]	VSS[134]	BH19
AF42	VSS[56]	VSS[135]	H10
AF5	VSS[57]	VSS[136]	H17
AF5	VSS[58]	VSS[137]	BH19
AF7	VSS[59]	VSS[138]	H10
AG19	VSS[60]	VSS[139]	H17
AG2	VSS[61]	VSS[140]	AV4
AG31	VSS[62]	VSS[141]	AV43
AG48	VSS[63]	VSS[142]	AV9
AH11	VSS[64]	VSS[143]	AW14
AH3	VSS[65]	VSS[144]	AW18
AH36	VSS[66]	VSS[145]	AW2
AH39	VSS[67]	VSS[146]	AW22
AH40	VSS[68]	VSS[147]	AW26
AH42	VSS[69]	VSS[148]	AW28
AH46	VSS[70]	VSS[149]	AW32
AH7	VSS[71]	VSS[150]	AW34
AJ19	VSS[72]	VSS[151]	AW36
AJ21	VSS[73]	VSS[152]	AW40
AJ24	VSS[74]	VSS[153]	AW48
AJ33	VSS[75]	VSS[154]	AY11
AJ34	VSS[76]	VSS[155]	AY12
AK12	VSS[77]	VSS[156]	AY22
AK3	VSS[78]	VSS[157]	AY28
	VSS[79]	VSS[158]	

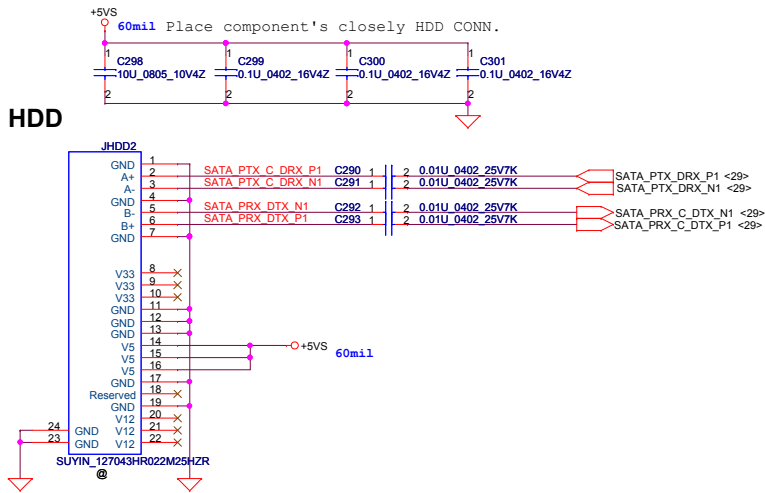
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UPCHI		H46	
AY4	VSS[159]	VSS[259]	H46
AY42	VSS[160]	VSS[260]	K18
AY46	VSS[161]	VSS[261]	K26
AY8	VSS[162]	VSS[262]	K39
B11	VSS[163]	VSS[263]	K46
B15	VSS[164]	VSS[264]	K7
B19	VSS[165]	VSS[265]	L18
B23	VSS[166]	VSS[266]	L2
B27	VSS[167]	VSS[267]	L20
B31	VSS[168]	VSS[268]	L28
B35	VSS[169]	VSS[269]	L28
B39	VSS[170]	VSS[270]	L36
B43	VSS[171]	VSS[271]	L48
F45	VSS[172]	VSS[272]	M12
BB12	VSS[173]	VSS[273]	P16
BB16	VSS[174]	VSS[274]	M18
BB20	VSS[175]	VSS[275]	M22
BB22	VSS[176]	VSS[276]	M24
BB24	VSS[177]	VSS[277]	M30
BB28	VSS[178]	VSS[278]	M32
BB30	VSS[179]	VSS[279]	M34
BB38	VSS[180]	VSS[280]	M38
BB4	VSS[181]	VSS[281]	M4
BB46	VSS[182]	VSS[282]	M42
BC14	VSS[183]	VSS[283]	M46
BC18	VSS[184]	VSS[284]	M8
BC2	VSS[185]	VSS[285]	N18
BC22	VSS[186]	VSS[286]	P30
BC26	VSS[187]	VSS[287]	N47
BC32	VSS[188]	VSS[288]	P11
BC34	VSS[189]	VSS[289]	P18
BC36	VSS[190]	VSS[290]	T33
BC40	VSS[191]	VSS[291]	P40
BC42	VSS[192]	VSS[292]	P45
BC48	VSS[193]	VSS[293]	P47
BD46	VSS[194]	VSS[294]	P7
BD5	VSS[195]	VSS[295]	R48
BF12	VSS[196]	VSS[296]	T12
BF26	VSS[197]	VSS[297]	T31
BF40	VSS[198]	VSS[298]	T37
BF10	VSS[199]	VSS[299]	T4
BF12	VSS[200]	VSS[300]	W34
BF16	VSS[201]	VSS[301]	T46
BF20	VSS[202]	VSS[302]	T47
BF22	VSS[203]	VSS[303]	T8
BF24	VSS[204]	VSS[304]	V11
BF26	VSS[205]	VSS[305]	V17
BF28	VSS[206]	VSS[306]	V26
BD3	VSS[207]	VSS[307]	V27
BF30	VSS[208]	VSS[308]	V29
AT13	VSS[209]	VSS[309]	V31
BF40	VSS[210]	VSS[310]	V36
BF8	VSS[211]	VSS[311]	V39
BG17	VSS[212]	VSS[312]	V43
BG21	VSS[213]	VSS[313]	V7
BG33	VSS[214]	VSS[314]	W17
BG44	VSS[215]	VSS[315]	W19
BG6	VSS[216]	VSS[316]	W2
BH11	VSS[217]	VSS[317]	W27
BH15	VSS[218]	VSS[318]	W48
BH17	VSS[219]	VSS[319]	Y12
BH19	VSS[220]	VSS[320]	Y38
H10	VSS[221]	VSS[321]	Y4
H17	VSS[222]	VSS[322]	Y42
BH31	VSS[223]	VSS[323]	Y46
BH33	VSS[224]	VSS[324]	Y8
BH35	VSS[225]	VSS[325]	BG29
BH39	VSS[226]	VSS[326]	N24
BH43	VSS[227]	VSS[327]	AJ3
BH7	VSS[228]	VSS[328]	AD47
D12	VSS[229]	VSS[329]	B43
D16	VSS[230]	VSS[330]	BE10
D18	VSS[231]	VSS[331]	BG41
D22	VSS[232]	VSS[332]	G14
D24	VSS[233]	VSS[333]	H16
D26	VSS[234]	VSS[334]	H36
D30	VSS[235]	VSS[335]	BG22
D32	VSS[236]	VSS[336]	BG24
D34	VSS[237]	VSS[337]	C22
D38	VSS[238]	VSS[338]	VSS[343]
D42	VSS[239]	VSS[339]	AP13
D48	VSS[240]	VSS[340]	M14
D8	VSS[241]	VSS[341]	AP3
E18	VSS[242]	VSS[342]	AP1
AY12	VSS[243]	VSS[343]	BE16
G18	VSS[244]	VSS[344]	BC16
G20	VSS[245]	VSS[345]	BG28
G26	VSS[246]	VSS[346]	VSS[351]
G28	VSS[247]	VSS[347]	BJ28
G36	VSS[248]	VSS[348]	
G48	VSS[249]	VSS[349]	
H12	VSS[250]	VSS[350]	
H18	VSS[251]	VSS[351]	
H22	VSS[252]	VSS[352]	
H24	VSS[253]	VSS[353]	
H26	VSS[254]	VSS[354]	
H30	VSS[255]	VSS[355]	
H32	VSS[256]	VSS[356]	
H34	VSS[257]	VSS[357]	
F3	VSS[258]	VSS[358]	

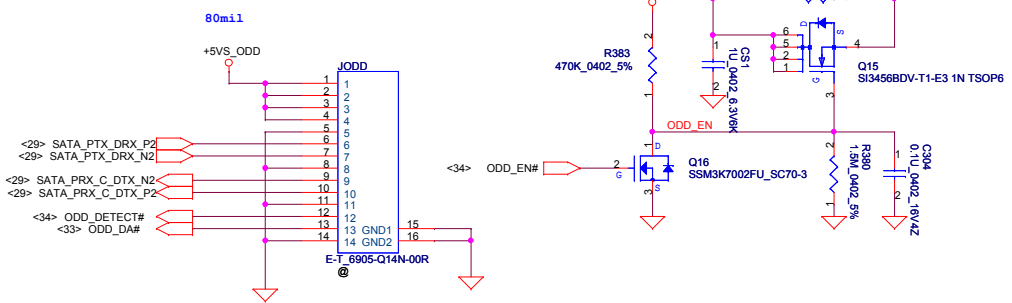
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HM65@

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				Document Number PBL80 LA-7441P M/B
				Rev 0.1
				Date: Friday, January 21, 2011 Sheet 37 of 58

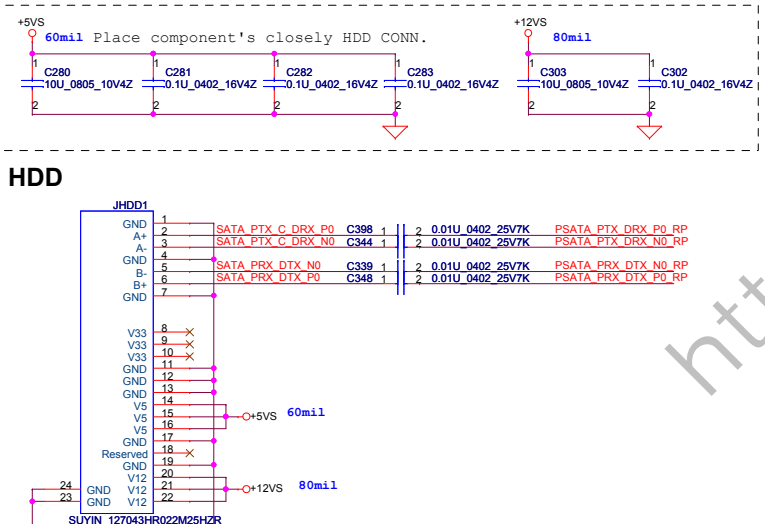
SATA HDD 2.5" Conn.



ODD small board conn

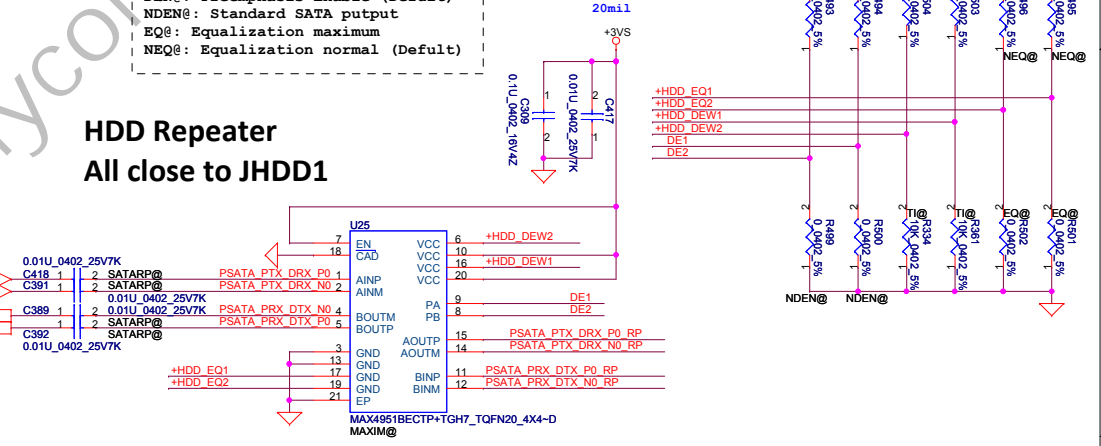


SATA HDD 3.5" Conn.

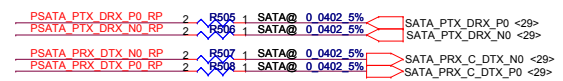


MAXIM@: MAX4951BECTP+TG7 (Default)
 TI@: SN75LVCP601TJR
 DEN@: Preemphasis Enable (Default)
 NDEN@: Standard SATA output
 EQ@: Equalization maximum
 NEQ@: Equalization normal (Default)

HDD Repeater All close to JHDD1

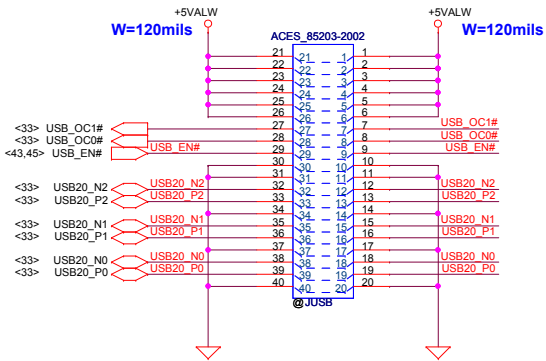


Note: +HDD_DEW1, +HDD_DEW2, +HDD_EQ1, +HDD_EQ2 need to route 10 mils

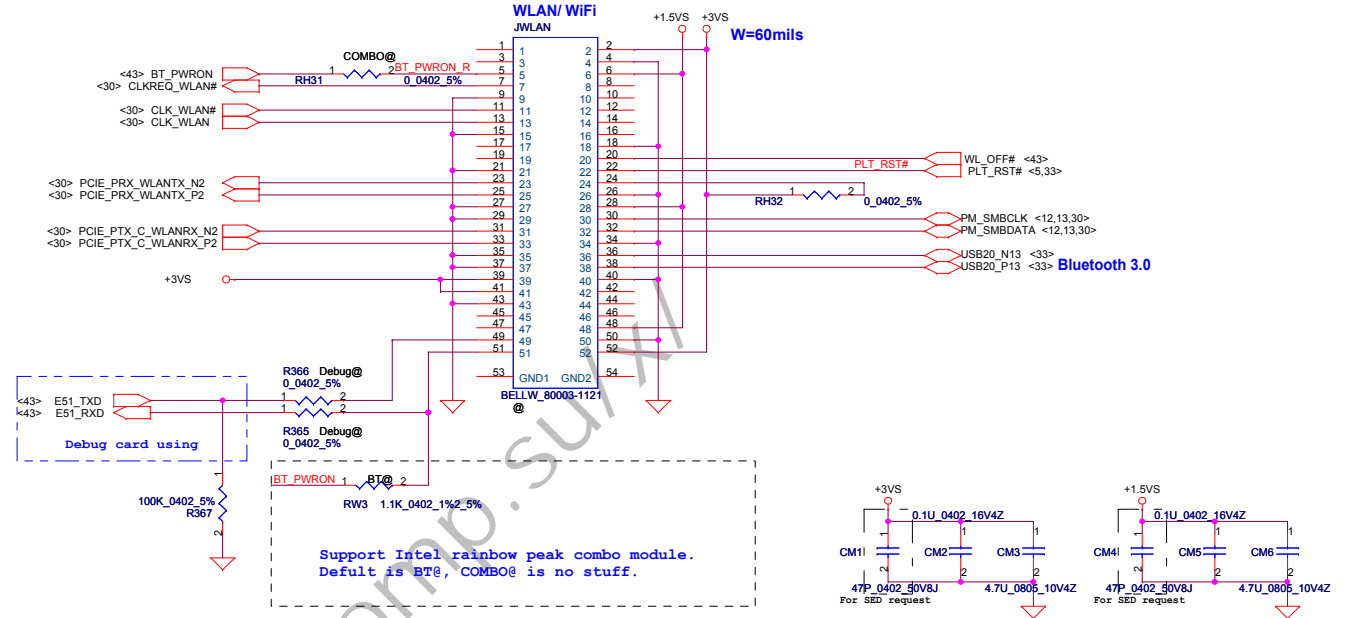


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Issued Date	2010/12/03	Deciphered Date	2011/12/03	SATA-HDD&ODD/B	
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				PBL80 LA-7441P M/B	Rev 0.1
				Date: Friday, January 21, 2011	Sheet 38 of 58

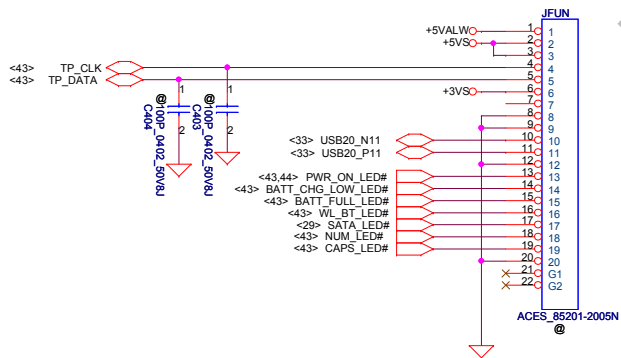
USB/B Right USB X 3



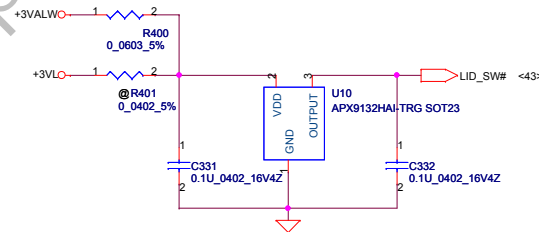
Slot 1 Half PCIe Mini Card-WLAN & BT3.0



Touch pad & LID & Card Reader & LED small board Connector

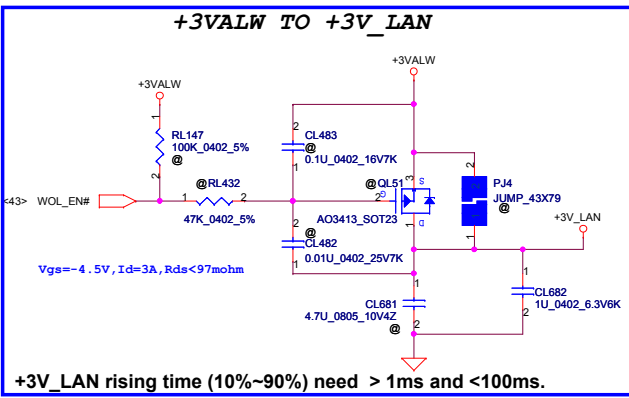
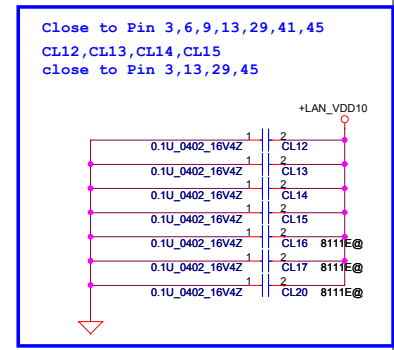
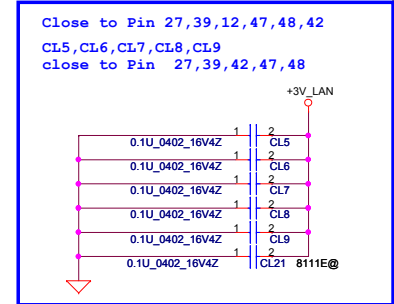
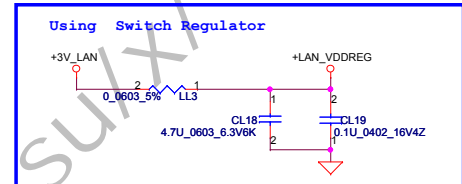
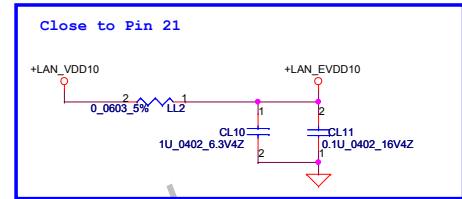
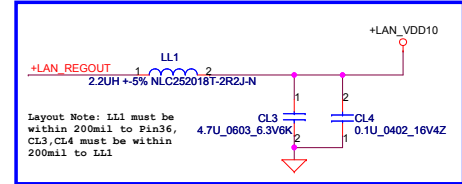
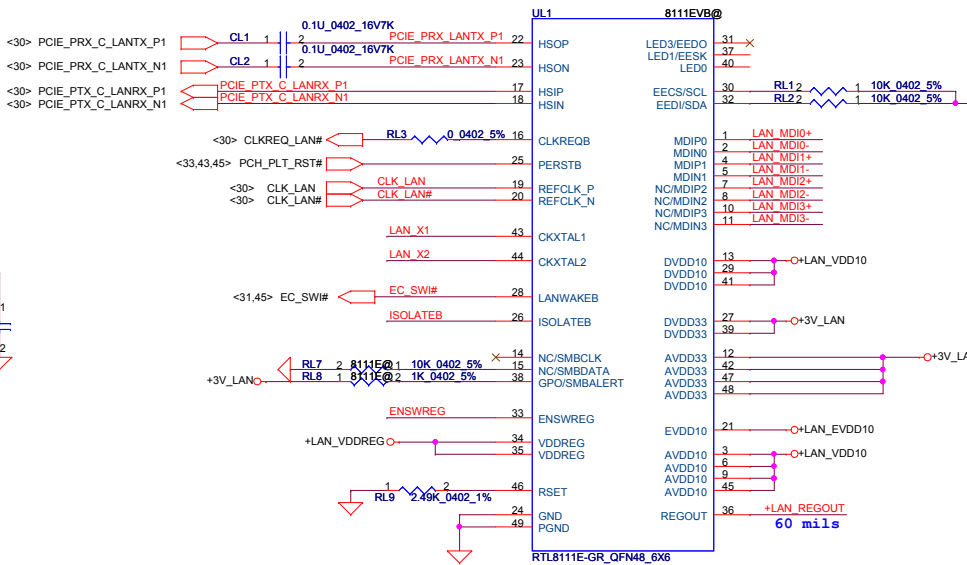
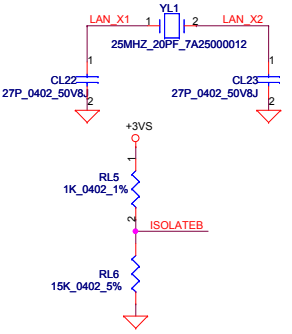


Lid SW

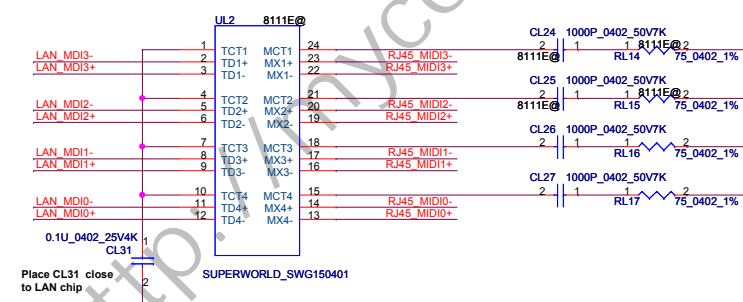


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Title			USB/B&TP/LED/CR/B&LID&PCIe-WLAN	
Size			Document Number	
			PBL80 LA-7441P M/B	
Date			Friday, January 21, 2011	Rev 0.1
			Sheet 39	of 58

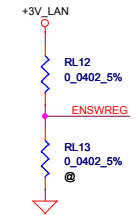
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	



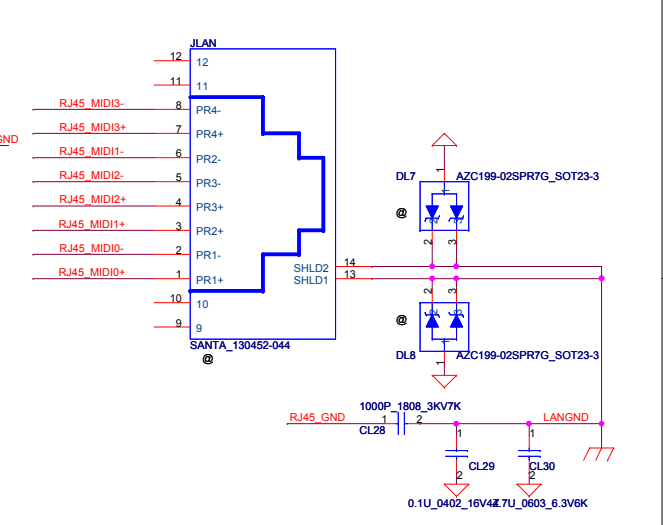
+3V_LAN rising time (10%~90%) need > 1ms and < 100ms.



Place CL31 close to LAN chip

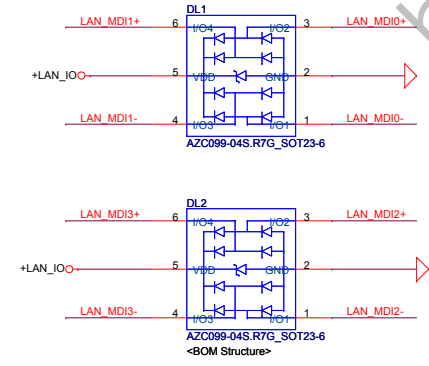


LAN Conn.



For P/N and footprint Please place them to ISPD page

UL1	8111E_VL
UL1	8111EVL@
UL2	8105E 10/100M
UL2	8105E@
UL2	10/100M transformer
UL2	8105E@



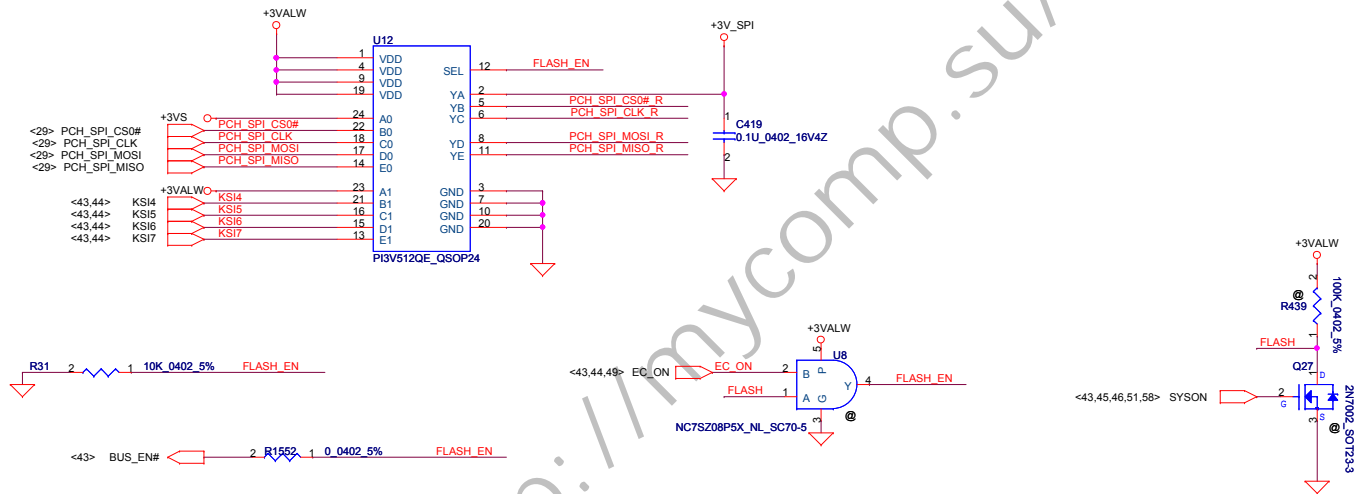
Security Classification	Compal Secret Data	
Issued Date	2010/12/03	Deciphered Date
		2011/12/03
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Title		Compal Electronics, Inc.	
Size		PCIE-LAN-RTL8105E/8111E	
Customer		Document Number	PBL80 LA-7441P M/B
Date	Friday, January 21, 2011	Rev	0.1
Sheet	40	of	58

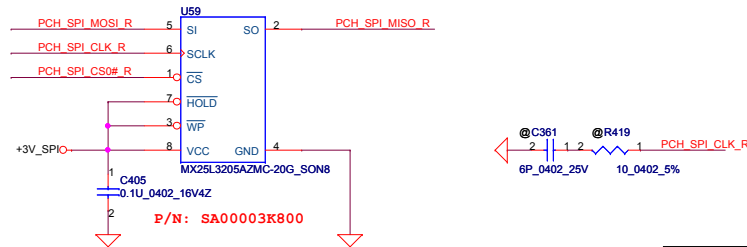
BIOS Bus switch

SPI ROM For Basic ME ROM size 4MByte

- When Flash EC ROM.
 KSO2 to Low (Test mode)
 KSO3 to Low (ISP mode)-----FDA mode
 EC_ON->Low, BUS_EN#->Low
 U11 : Y->A0, PCH to BIOS ROM.
 KSI4,5,6,7 direct to EC_SPI
 - When Flash BIOS ROM.
 KSO2 to High
 KSO3 to Low (ISP mode)
 EC_ON->High, BUS_EN#->High.
 U11 : Y->A1, KSI4,5,6,7 to BIOS ROM.
 +3V_SPI from +3VALW
 Set EC pin KSI4,5,6,7 to HiZ.
 - When normal operation.
 EC_ON->High, BUS_EN#->Low.
 U11 : Y->A0, PCH direct to BIOS ROM.
 +3V_SPI from +3VS.
 - When enter S3,4
 EC_ON->High, BUS_EN#->Low.
 U11 : Y->A1, PCH direct to BIOS ROM.
 But +3V_SPI from +3VS is no power.
- ** BUS_EN# only high when test mode.
 And must make sure it's low when FDA mode.
 Or HW use 10K pull down to GND.

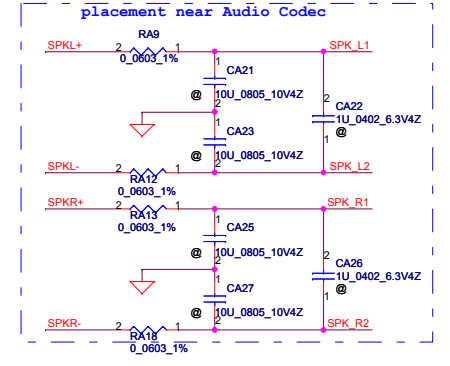
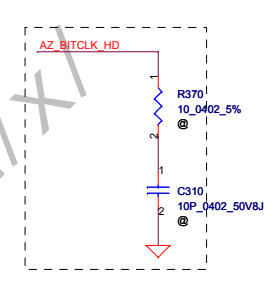
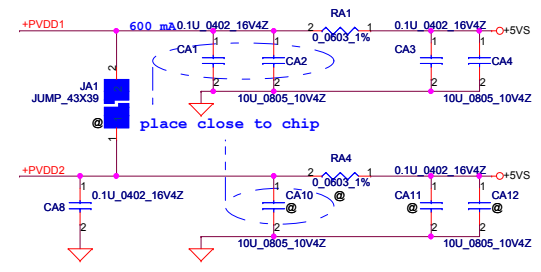
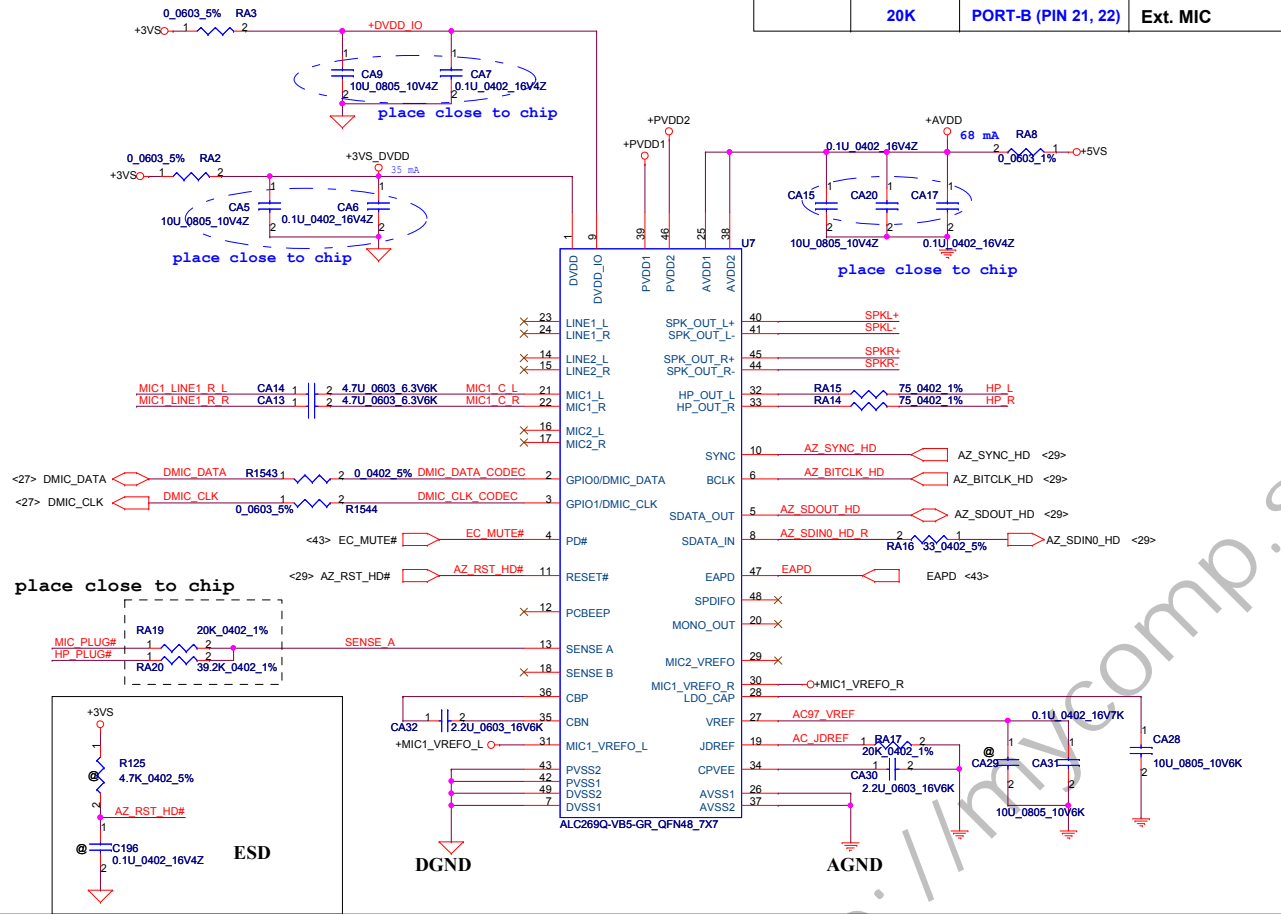


BIOS SPI Flash (4MByte*1)

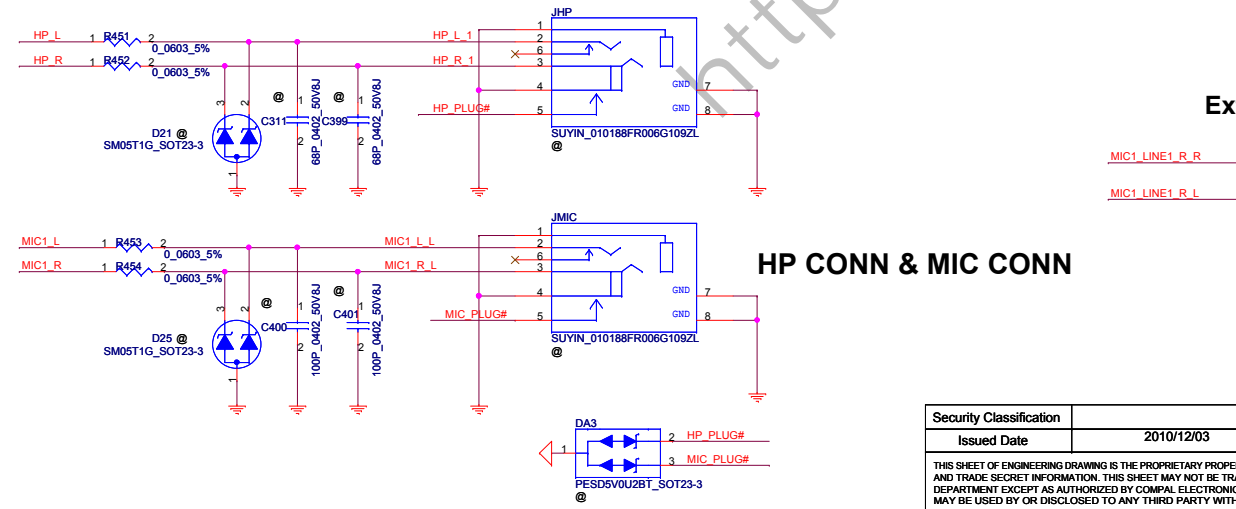
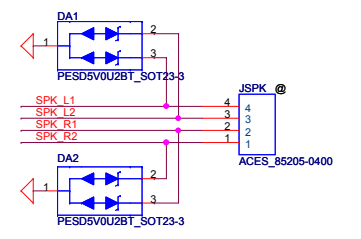


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				Document Number
				PBL80 LA-7441P M/B
				Rev
				0.1
				Date: Friday, January 21, 2011
				Sheet 41 of 58

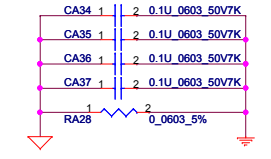
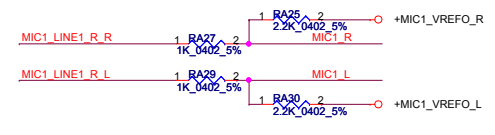
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K 20K	PORT-I (PIN 32, 33) PORT-B (PIN 21, 22)	Headphone out Ext. MIC



SPEAKER CONN



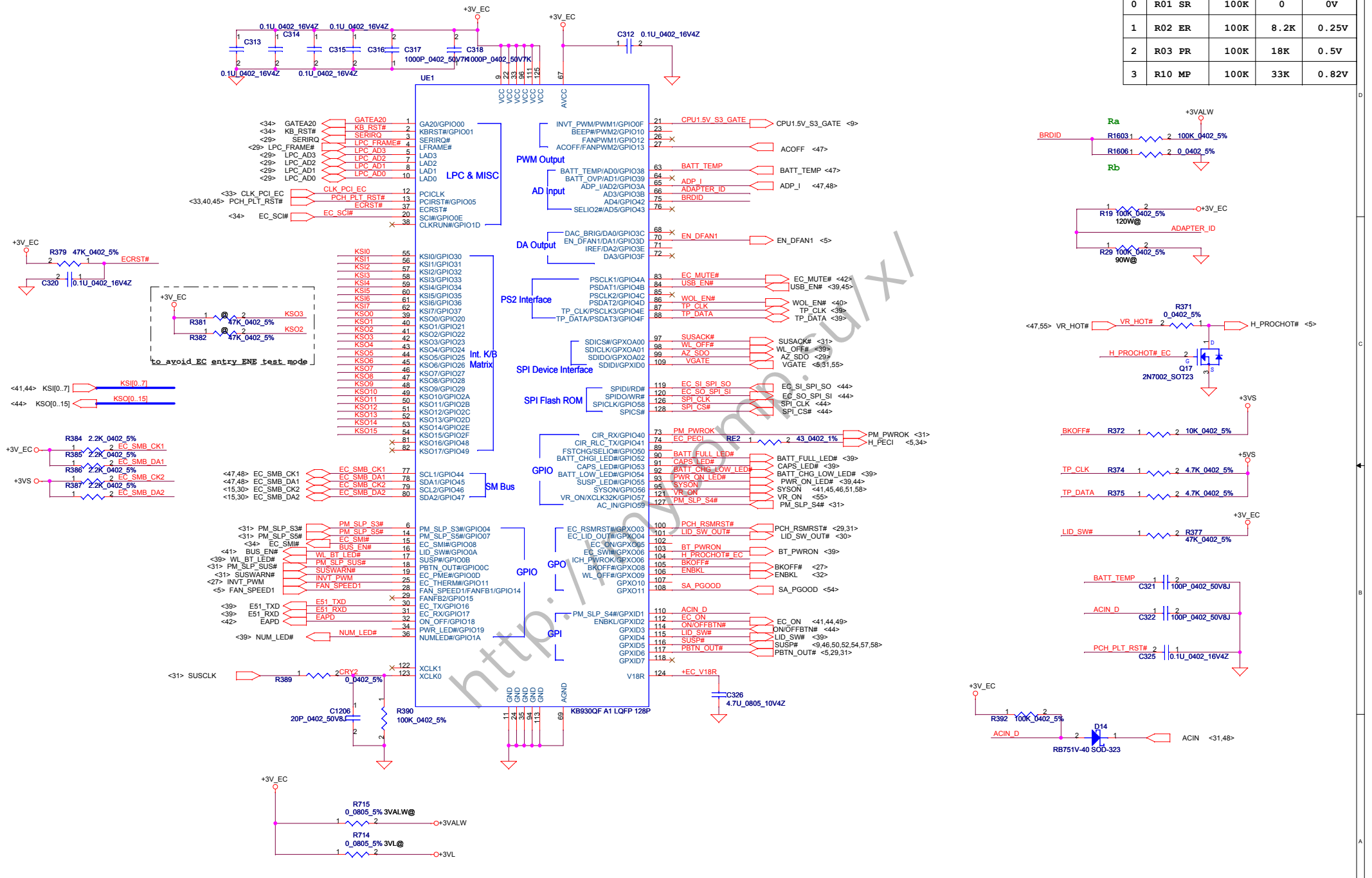
Ext.MIC/LINE IN JACK



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				HD CODEC ALC269
				PBL80 LA-7441P M/B
				Rev 0.1
				Date: Friday, January 21, 2011 Sheet 42 of 58

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ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	0	0V
1	R02 ER	100K	8.2K	0.25V
2	R03 PR	100K	18K	0.5V
3	R10 MP	100K	33K	0.82V



EC Power : +3VALW(default)

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Date:	Friday, January 21, 2011	Sheet	43 of 58	Rev 0.1

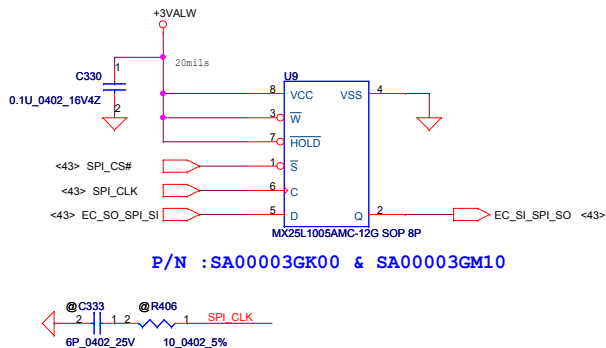
Compal Electronics, Inc.

ENE-KB930

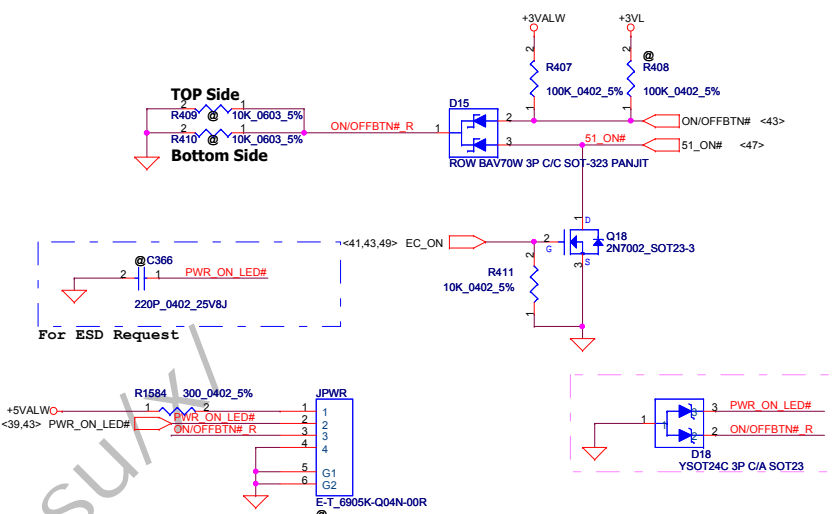
PBL80 LA-7441P M/B

Rev 0.1

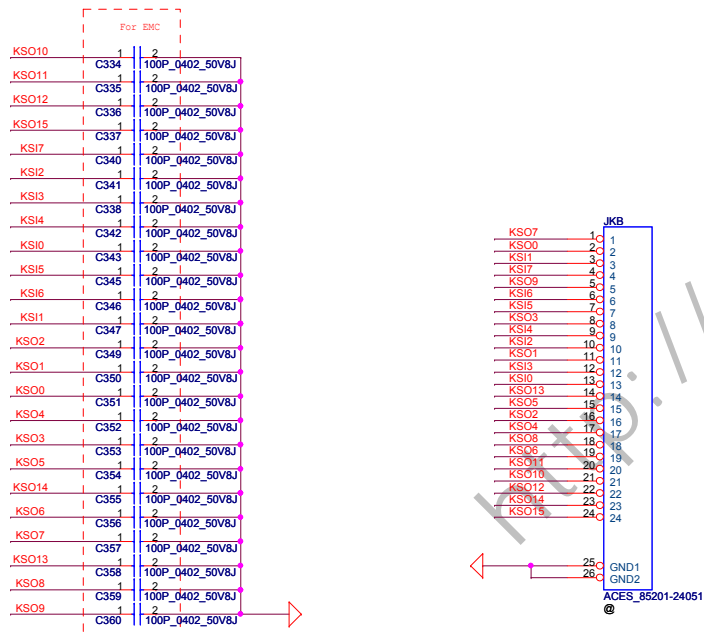
SPI Flash (1MByte*1)



Power Button/ PWR/B

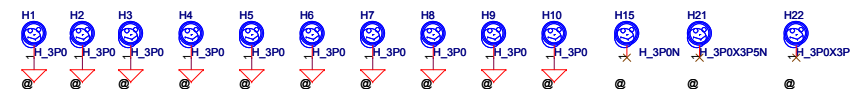


KEYBOARD CONN.

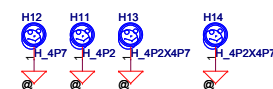


KSIO[.7] <-41,43>
KSIO[.15] <-43>

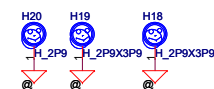
Screw Hole



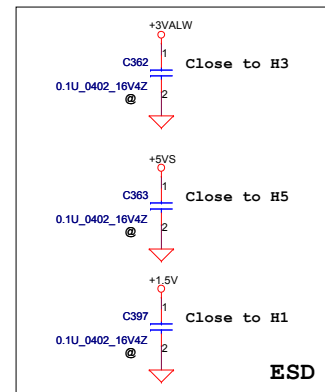
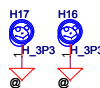
CPU



VGA



WLAN

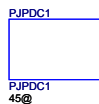


ISPD

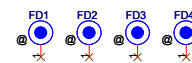


PCB

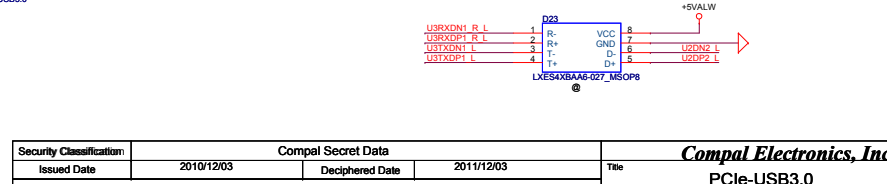
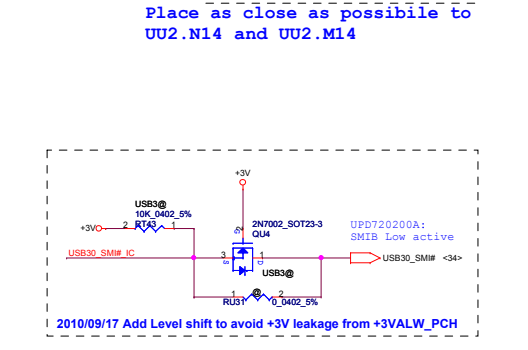
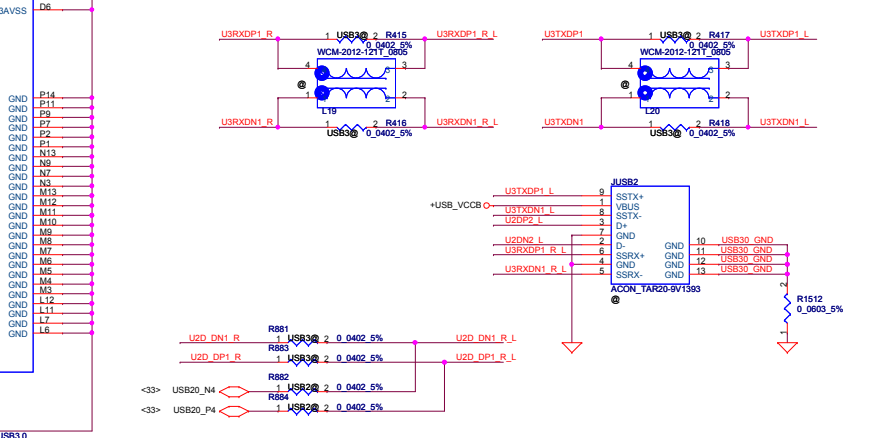
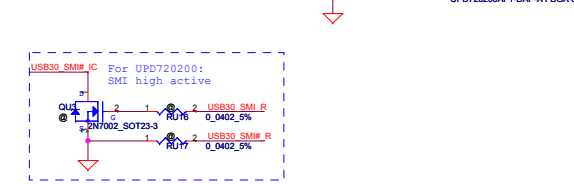
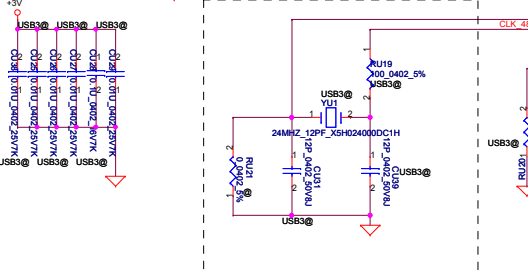
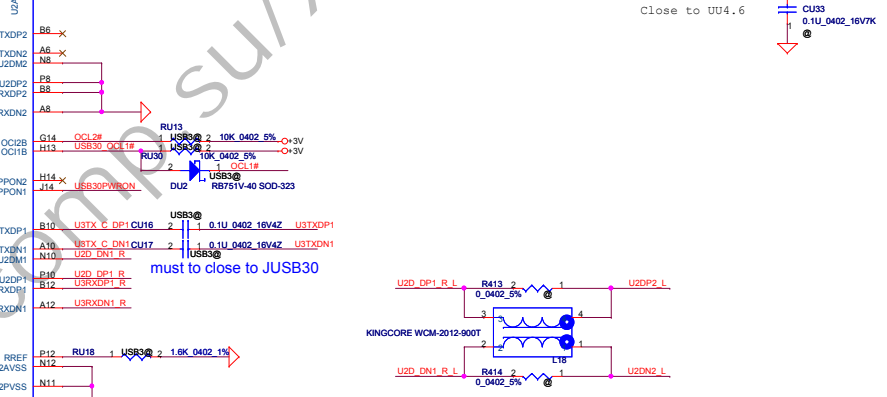
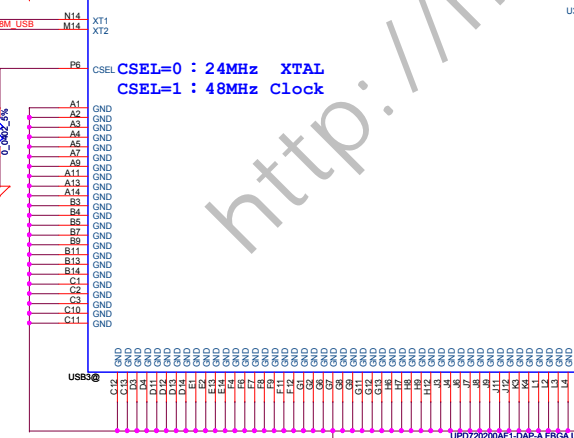
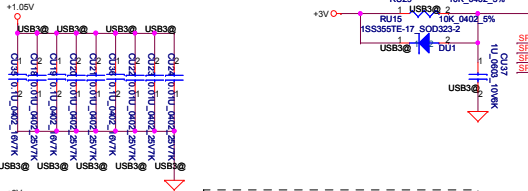
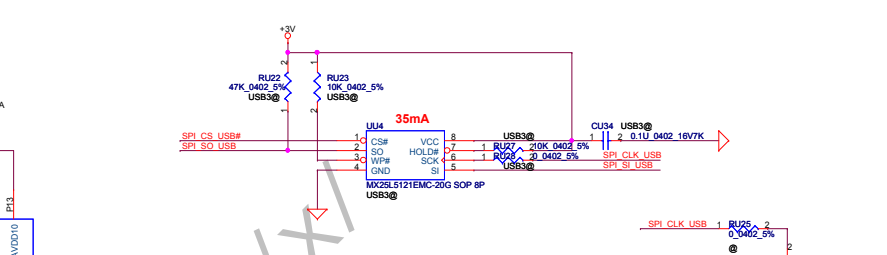
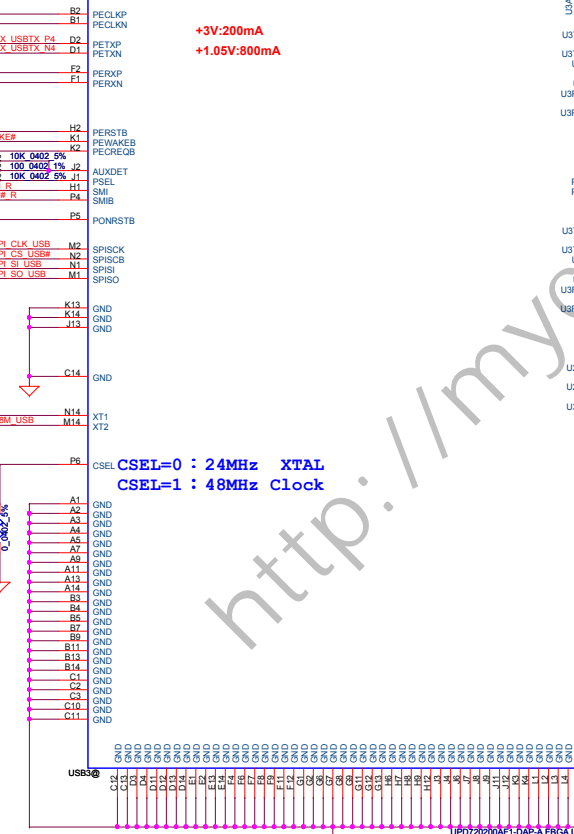
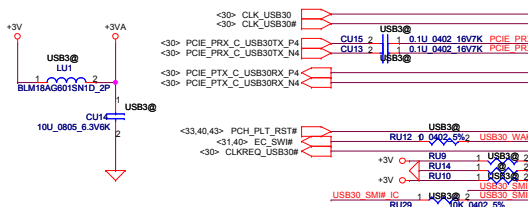
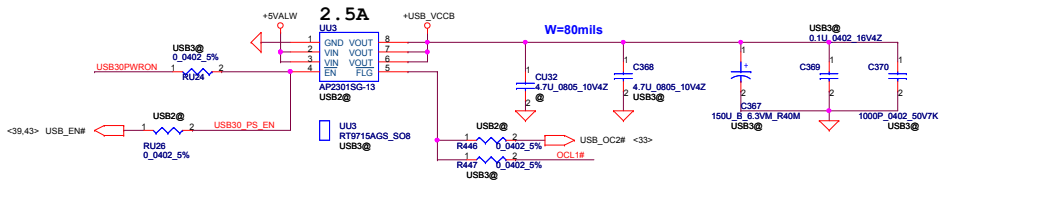
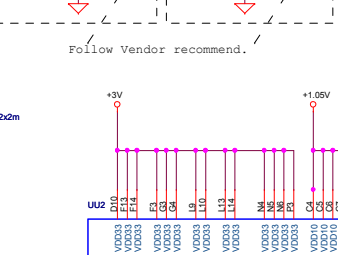
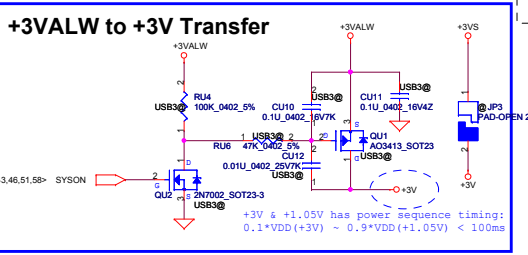
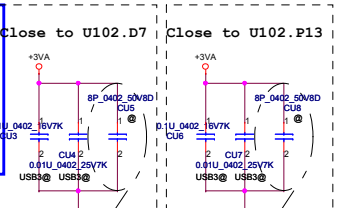
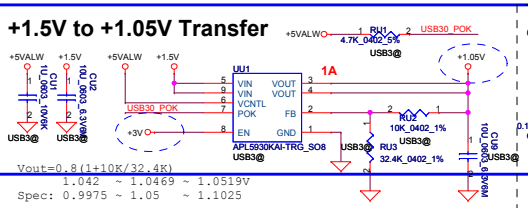
DC-IN



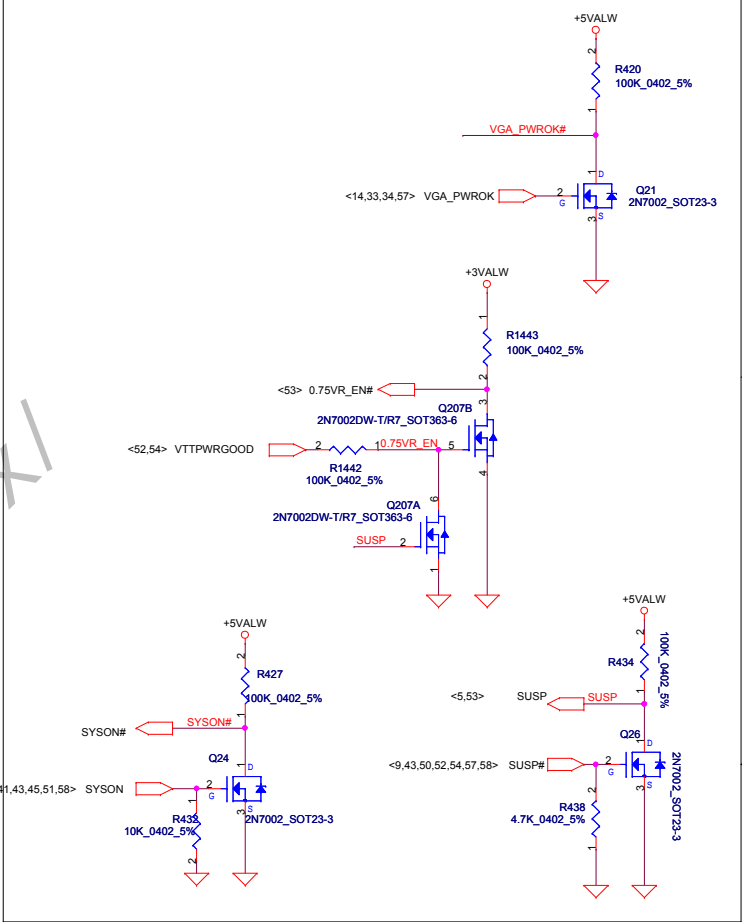
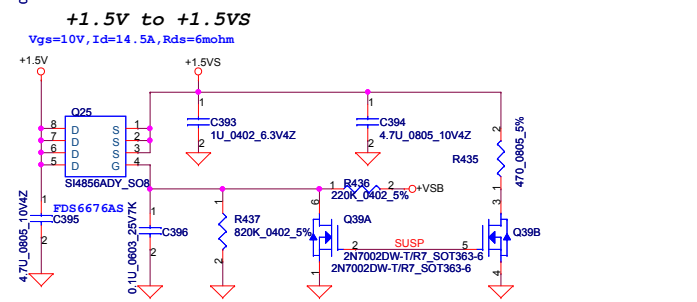
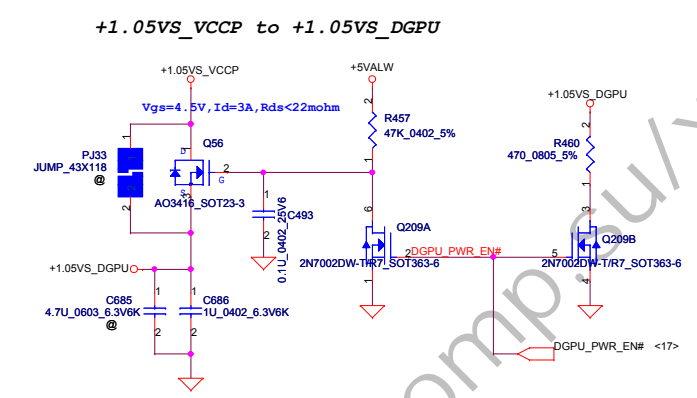
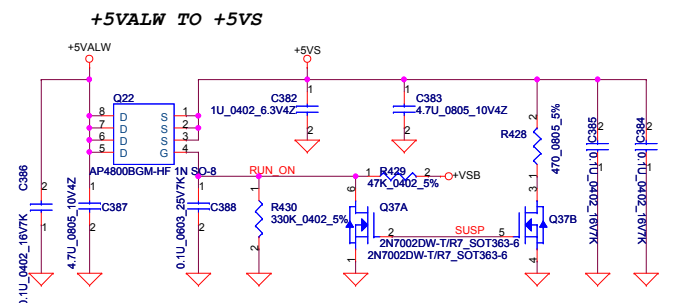
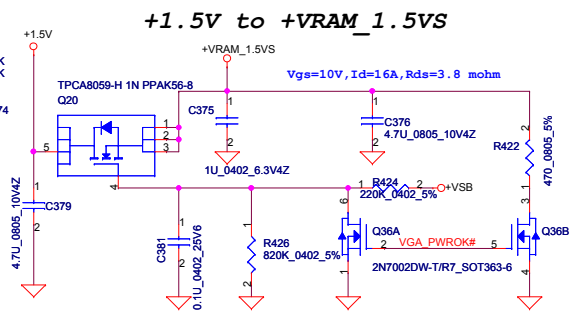
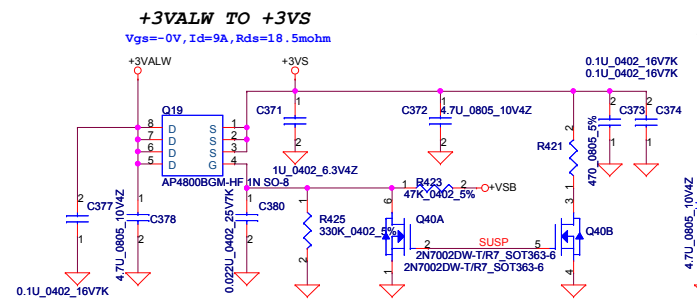
PCB Federal Mark PAD



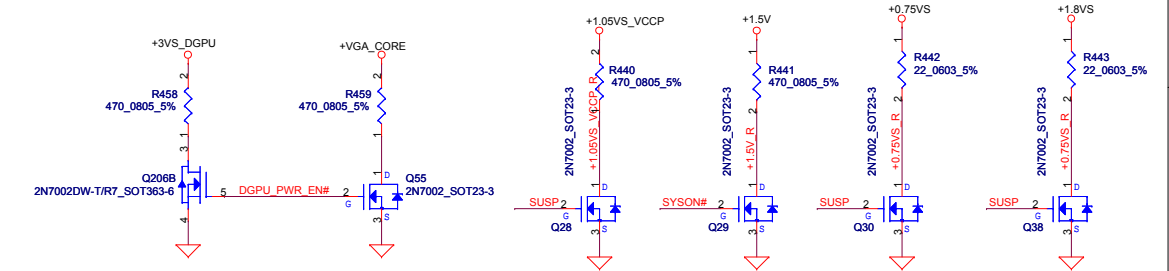
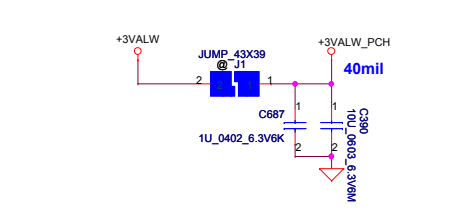
Security Classification	Compal Secret Data		Title	
Issued Date	2010/12/03	Deciphered Date	2011/12/03	ECROM/KB/PWR/B/SCREW
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				PBL80 LA-7441P M/B
				Rev 0.1
Date: Friday, January 21, 2011				Sheet 44 of 58



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Issued Date	2010/12/03	Deciphered Date	2011/12/03	PCIE-USB3.0
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Size	Document Number	PBL80 LA-7441P M/B		Rev 0.1
Date:	Friday, January 21, 2011	Sheet	45	of 58

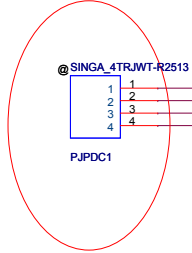


+3VALW TO +3VALW(PCH AUX Power)
 Short J1 for PCH VCCSUS3.3



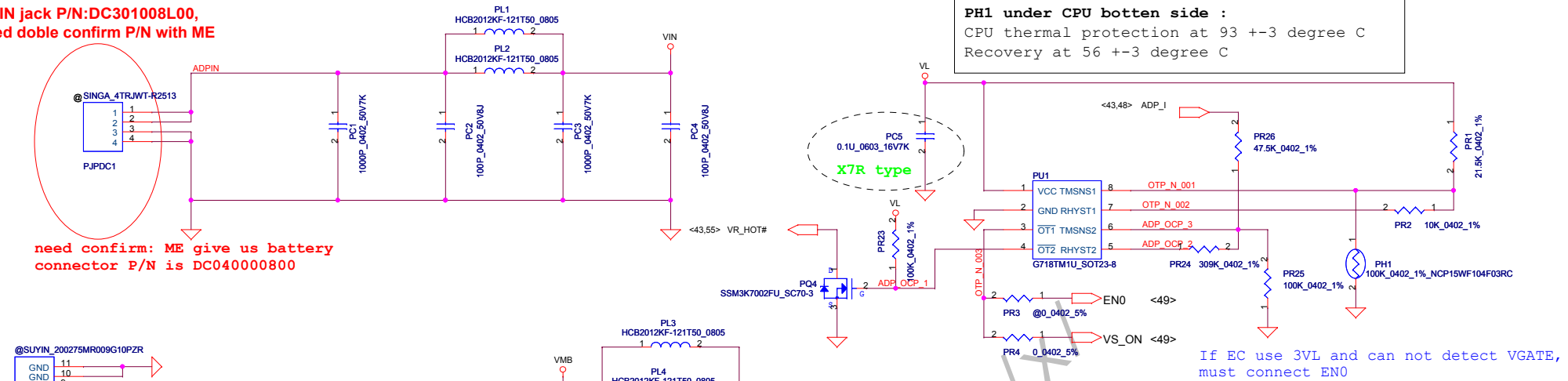
Security Classification		Compal Secret Data		Title	
Issued Date	2010/12/03	Deciphered Date	2011/12/03	DC-DC INTERFACE	
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Date: Friday, January 21, 2011				Sheet	46 of 58

DCIN jack P/N:DC301008L00,
need double confirm P/N with ME

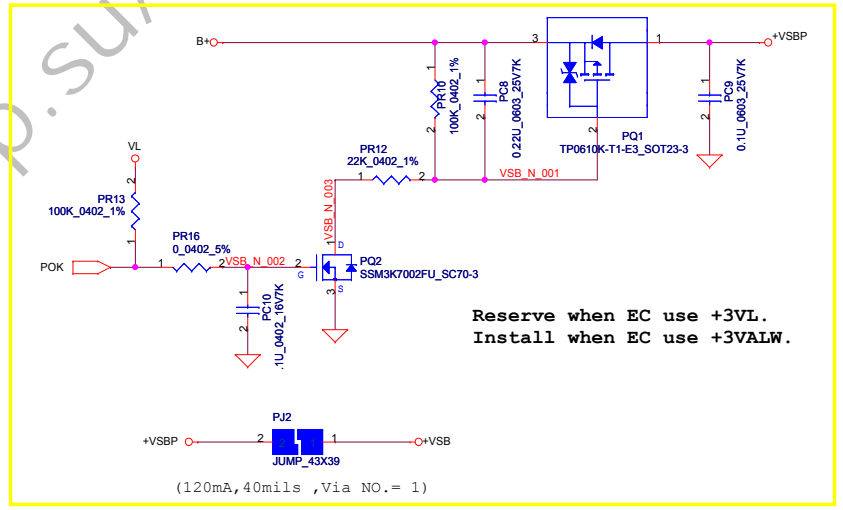
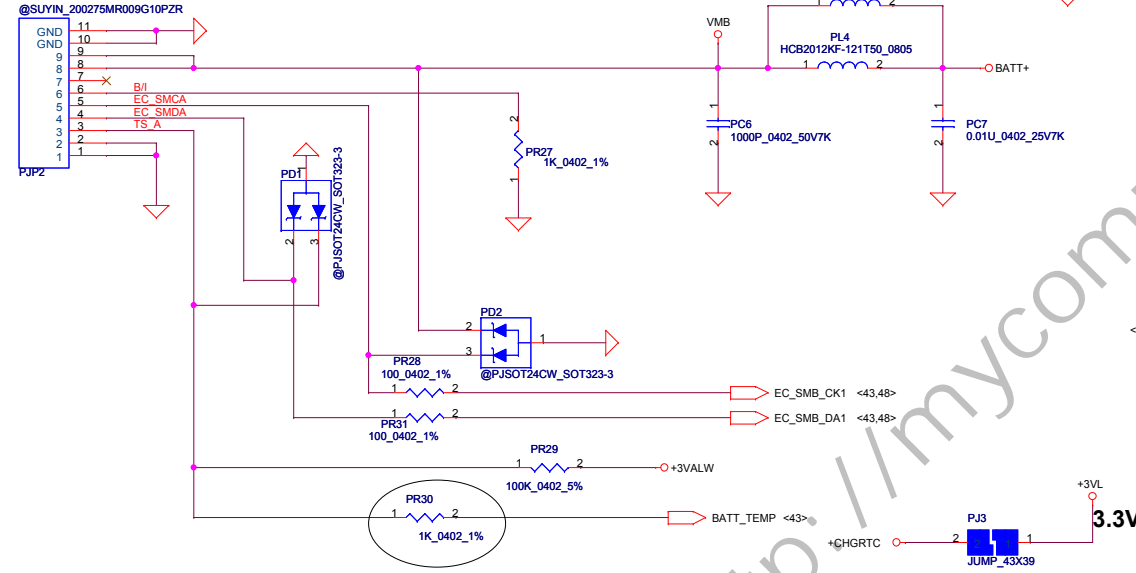


need confirm: ME give us battery
connector P/N is DC040000800

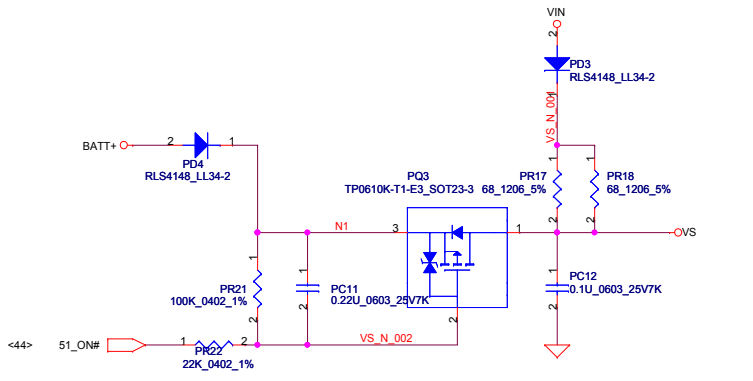
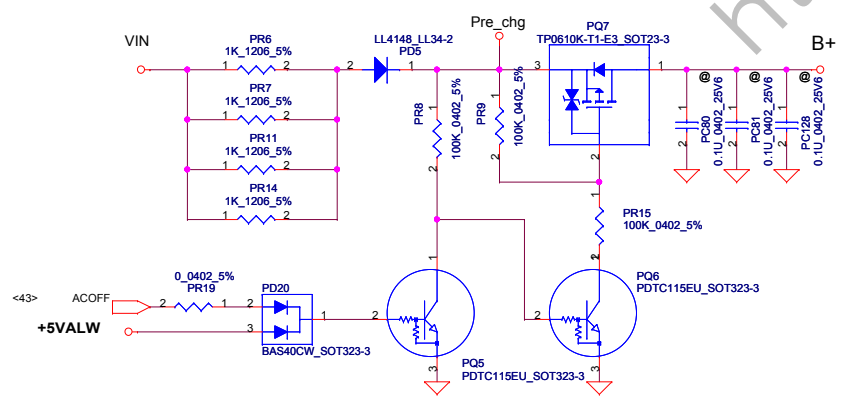
PH1 under CPU botten side :
CPU thermal protection at 93 +/-3 degree C
Recovery at 56 +/-3 degree C



If EC use 3VL and can not detect VGATE,
must connect EN0

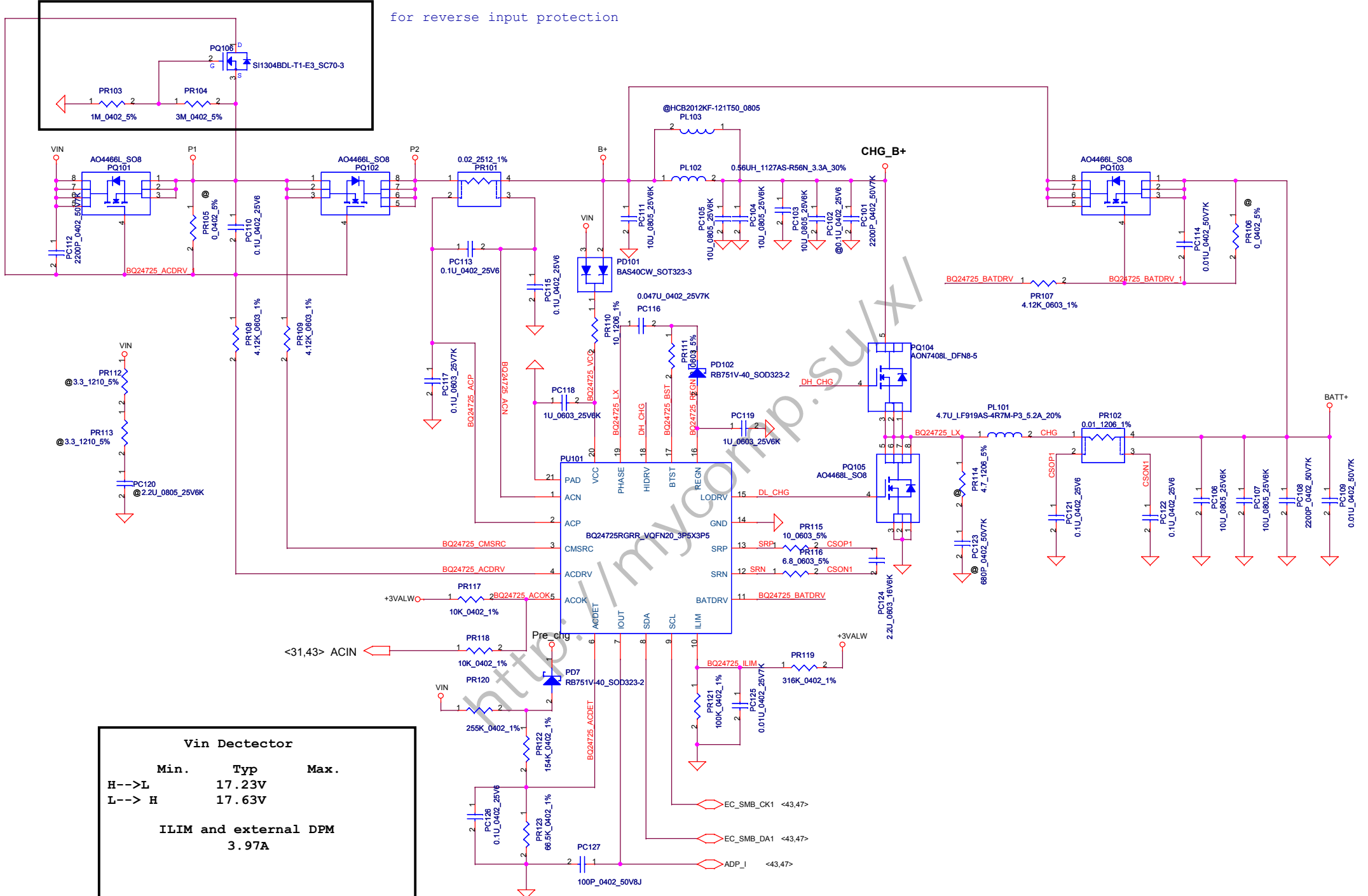


Reserve when EC use +3VL.
Install when EC use +3VALW.

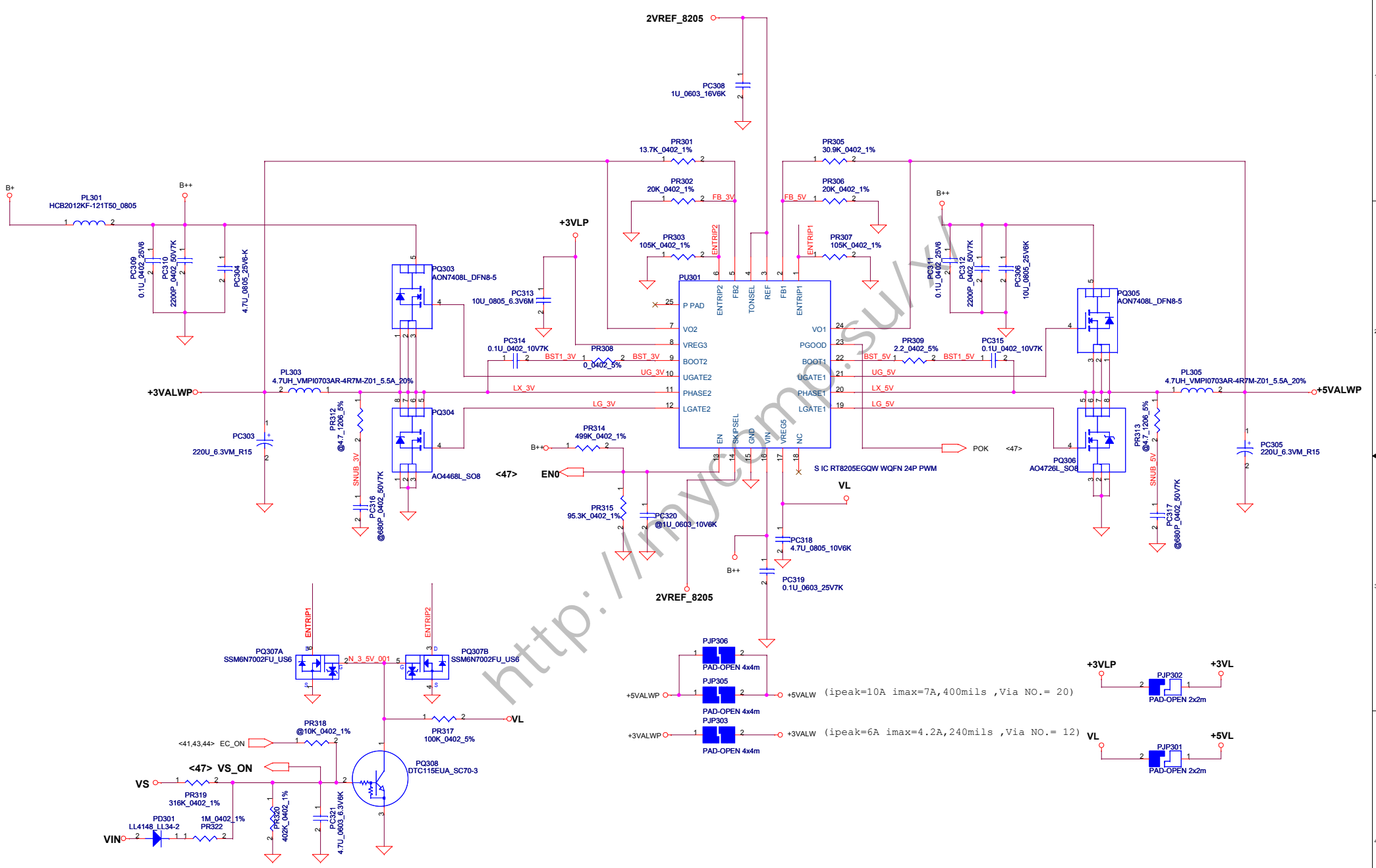


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Date:	Friday, January 21, 2011	Sheet	47	of	58

for reverse input protection



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				Custom	0.1
				Date:	Friday, January 21, 2011
				Sheet	48 of 58
				LA-7221P	

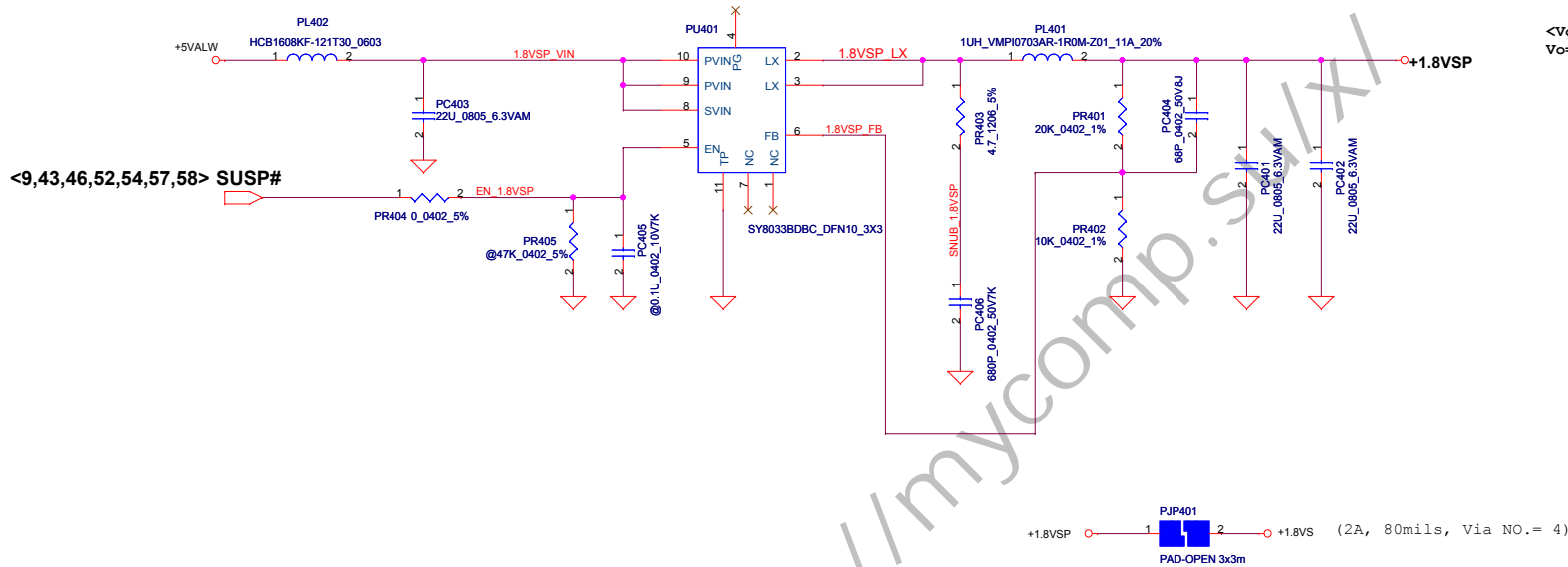


EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

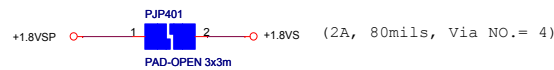
Security Classification	Compal Secret Data	
Issued Date	2007/08/02	Deciphered Date
		2008/08/02

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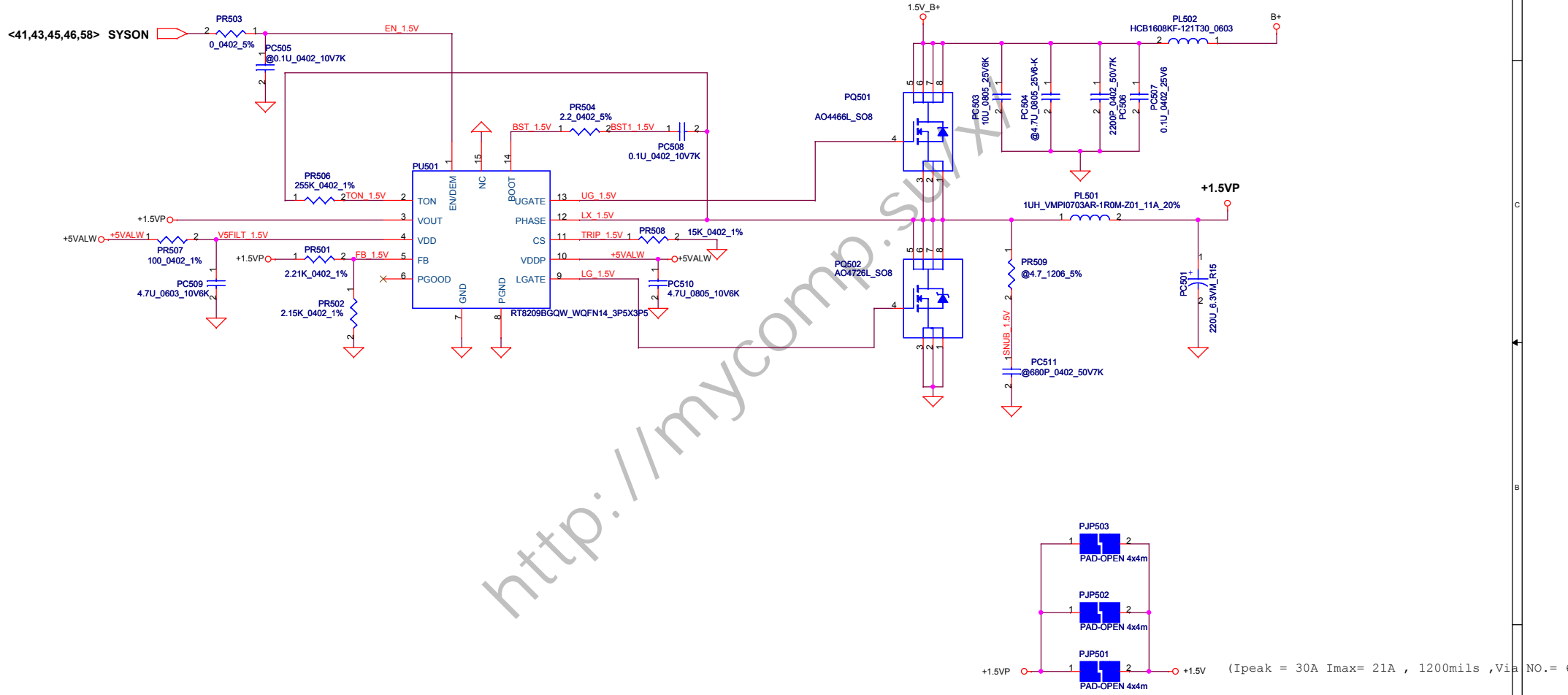
Title		
Compal Electronics, Inc.		
3.3VALWP/5VALWP		
Size	Document Number	Rev
Custom	PBL21 LA671P MB	0.1
Date:	Friday, January 21, 2011	Sheet 49 of 58



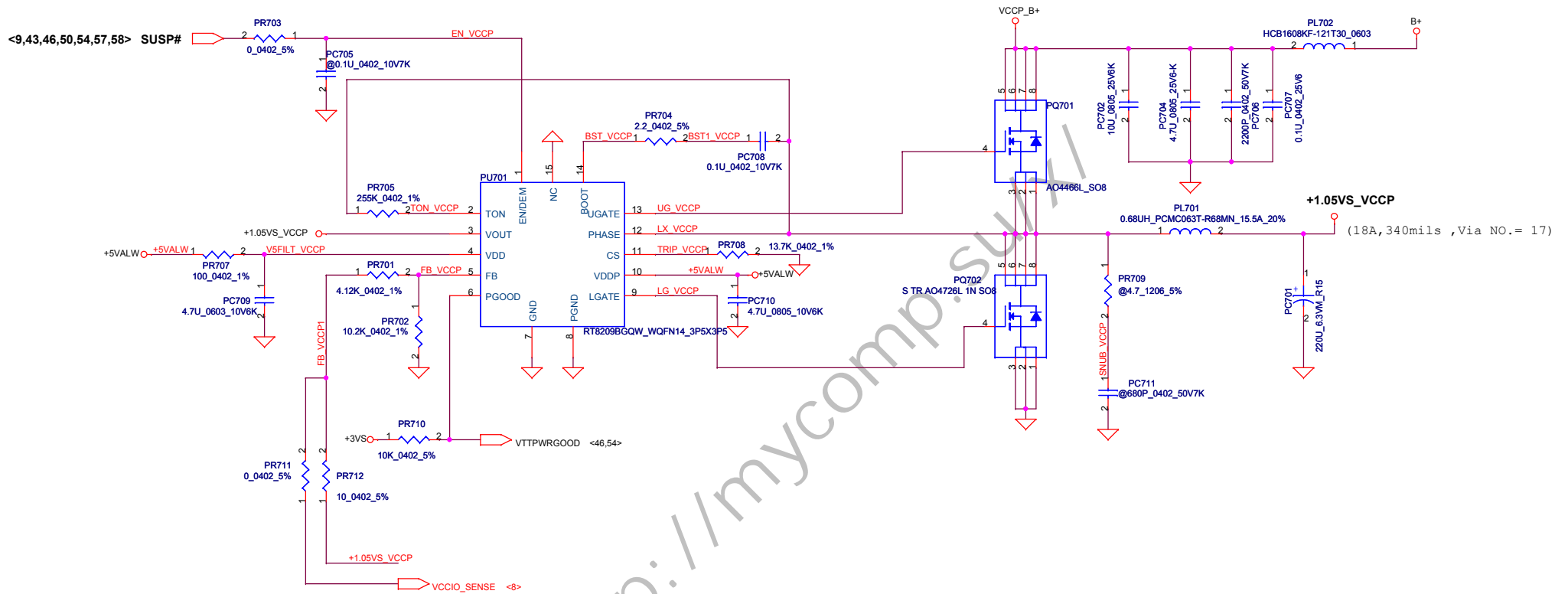
$V_o = 1.8V$ $V_{FB} = 0.6V$
 $V_o = V_{FB} * (1 + PR401 / PR402) = 0.6 * (1 + 20K / 10K) = 1.8V$



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Size	Document Number			Rev	
	NCL61 LA-6321P M/B			0.1	
Date:	Friday, January 21, 2011	Sheet	50	of	58

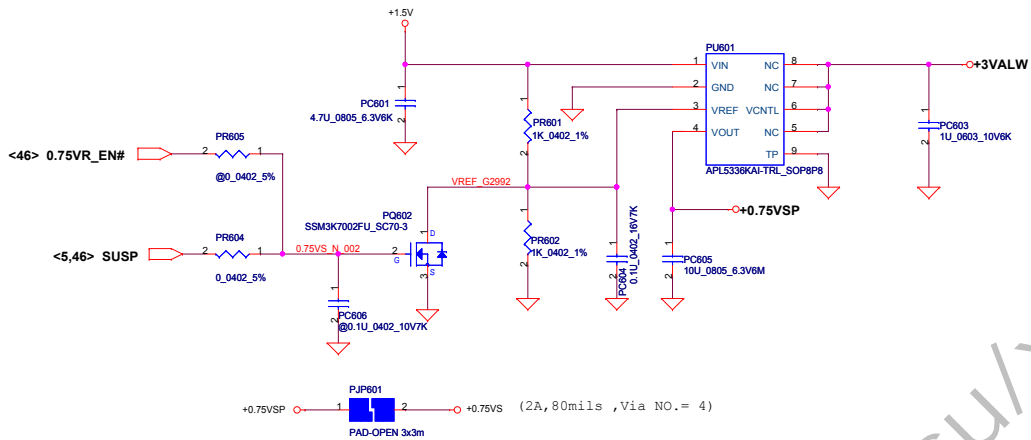


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Date: Friday, January 21, 2011				Sheet 51 of 58	



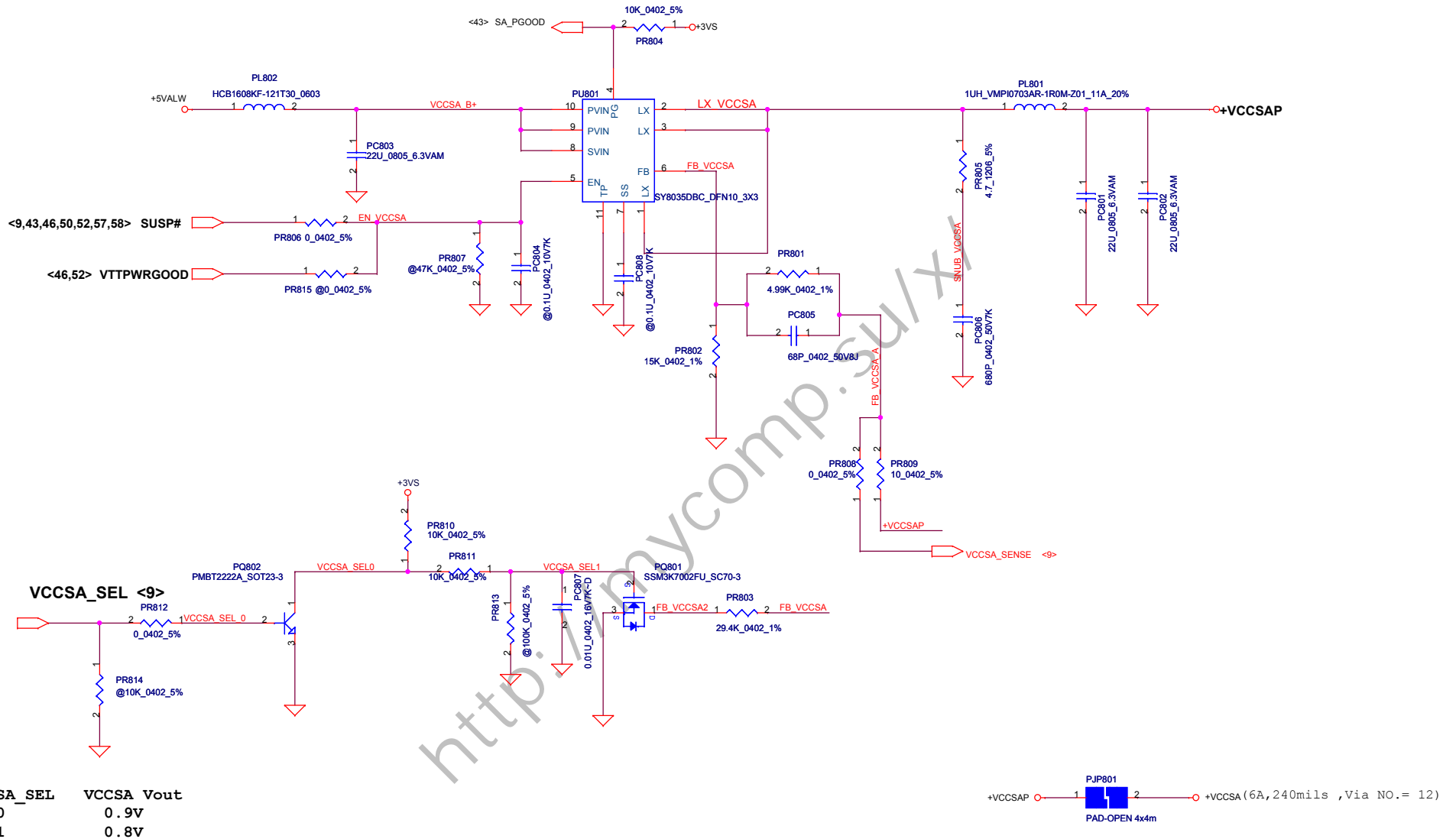
VSSIO_SENSE connect to GND directly.

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Date:	Friday, January 21, 2011	Sheet	52 of 58	Rev	0.1

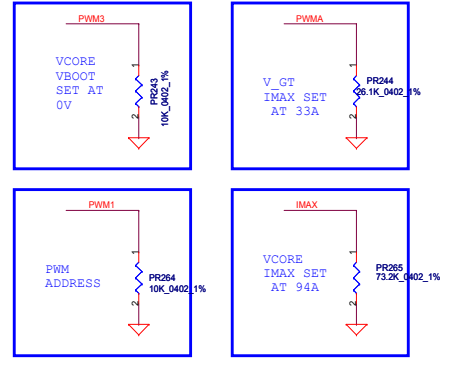
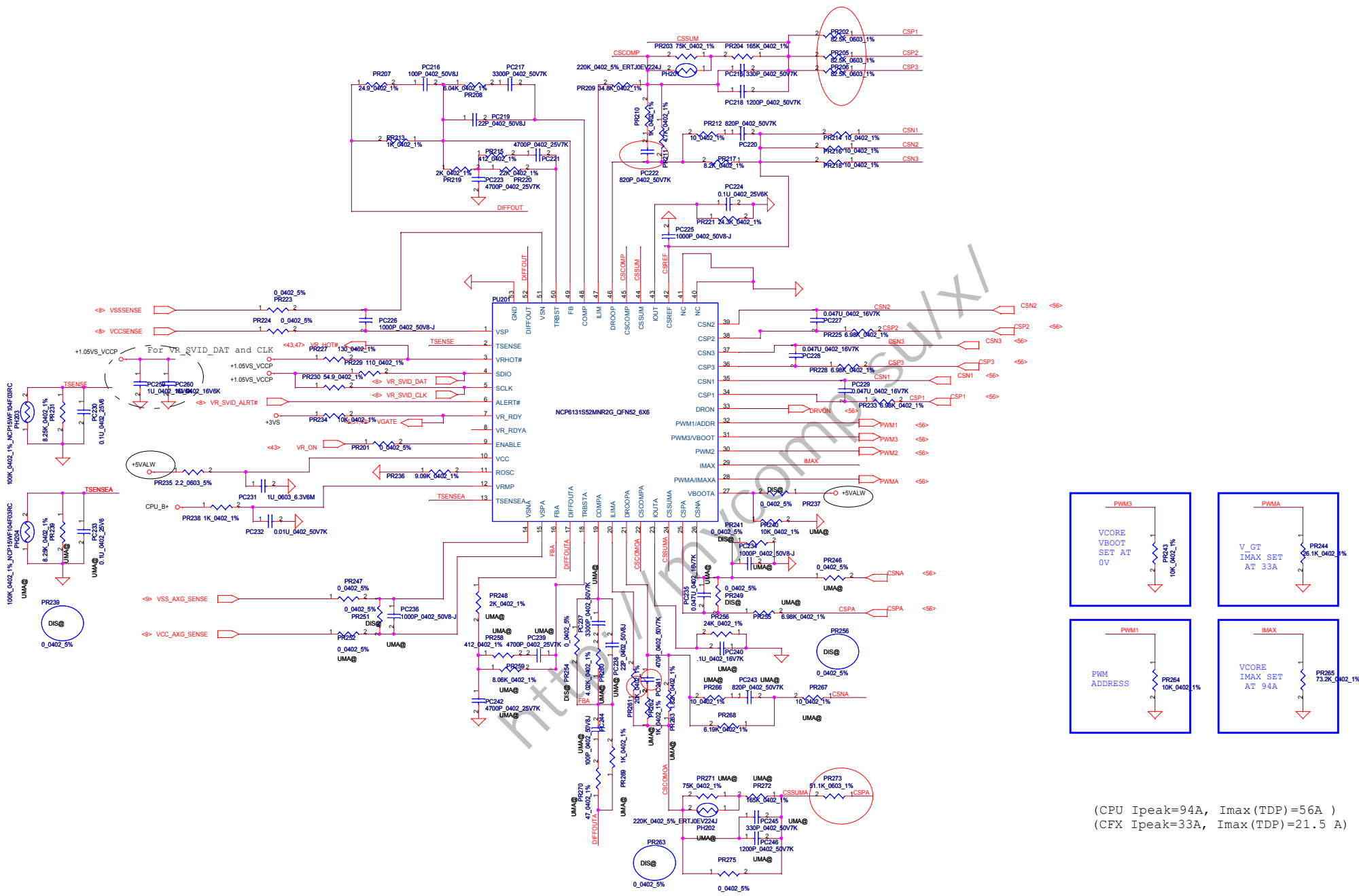


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Size	Document Number			Rev
	PBL21 LA6771P M/B			0.1
Date:	Friday, January 21, 2011	Sheet	53	of 58

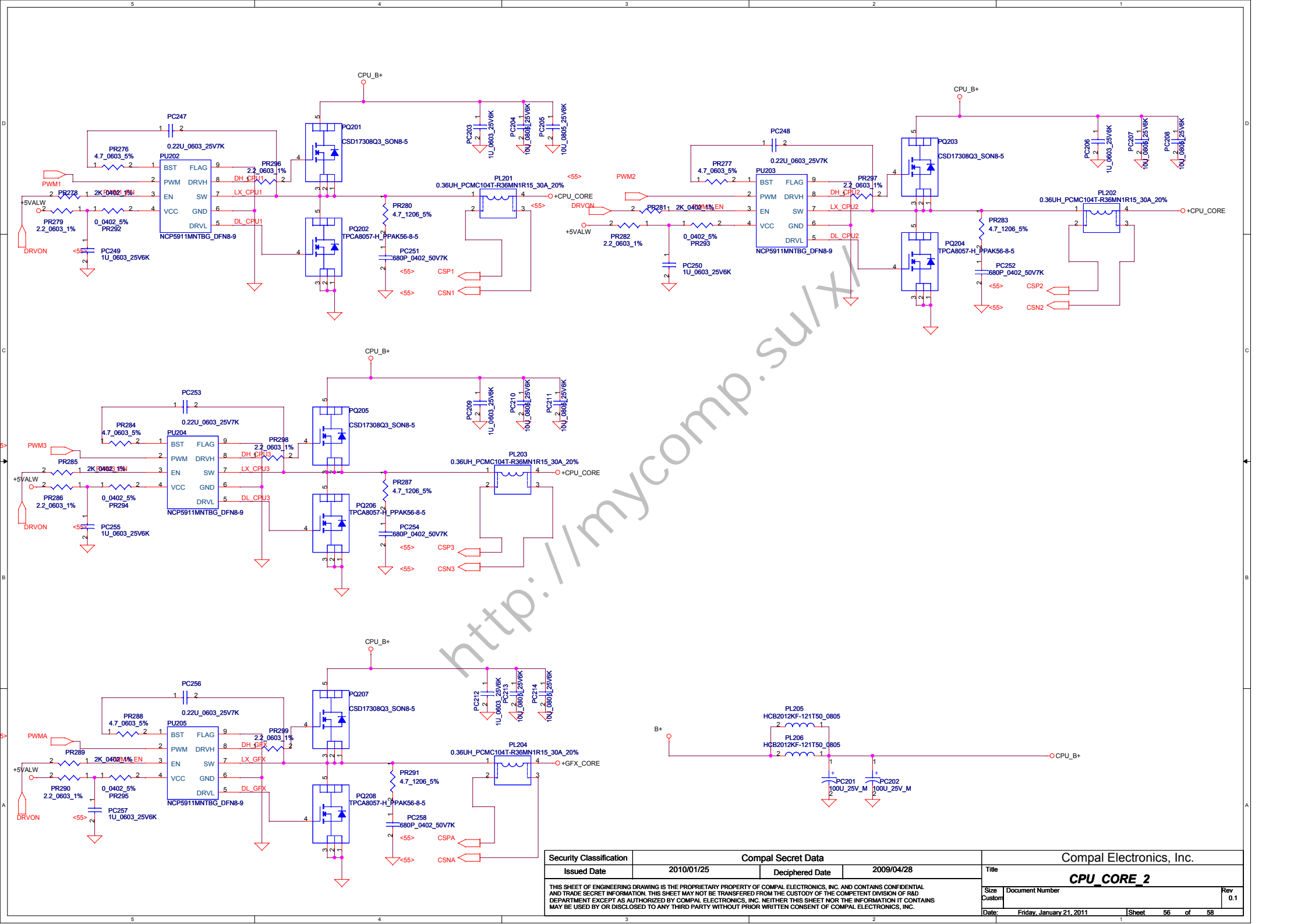


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Date:	Friday, January 21, 2011	Sheet	54	of	58
Rev	0.1				

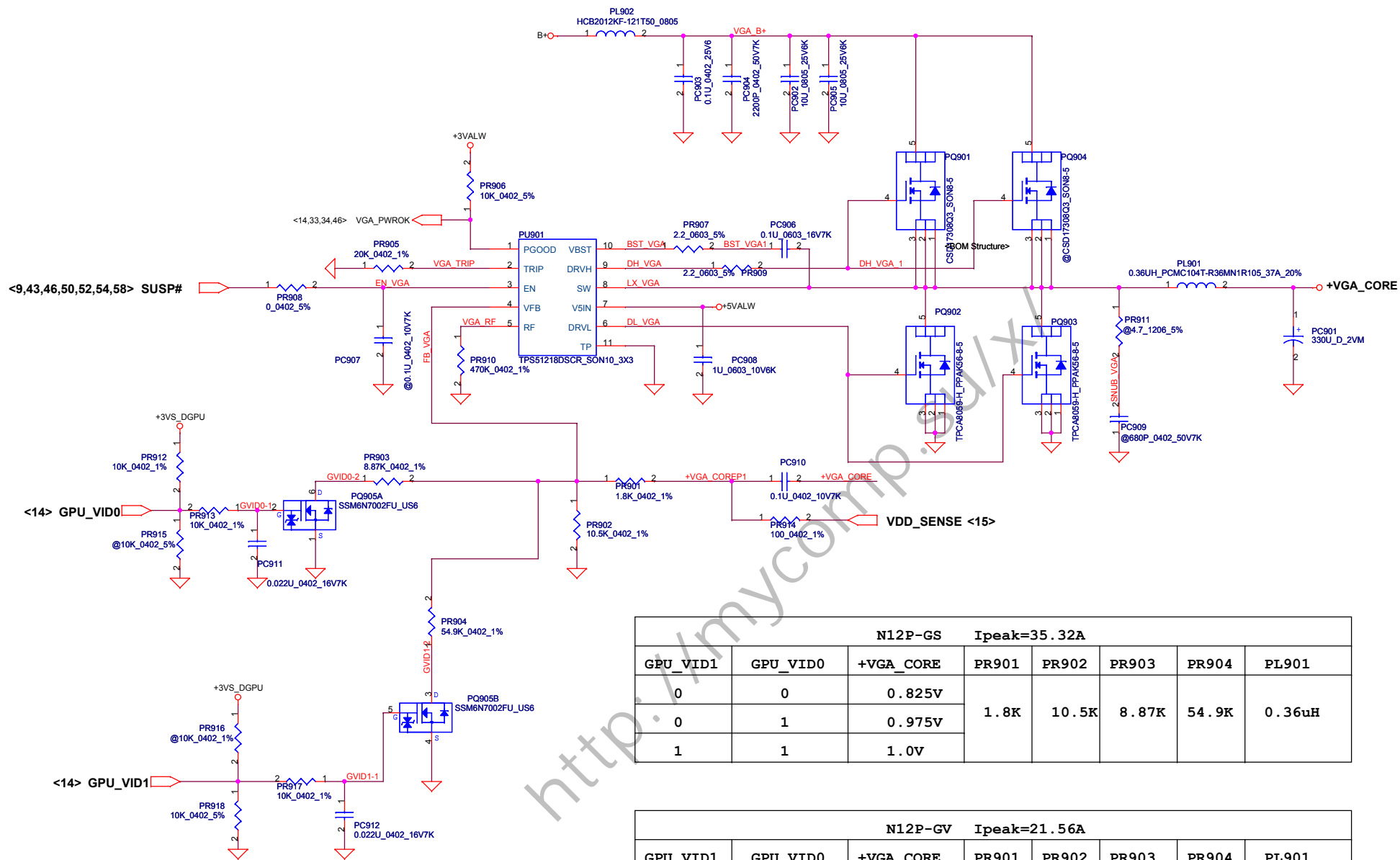


(CPU Ipeak=94A, Imax(TDP)=56A)
 (CFX Ipeak=33A, Imax(TDP)=21.5 A)

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Issued Date	2010/01/25	Deciphered Date	2009/04/28	Title
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Size	C	Sheet	55	Rev
			of	0.1



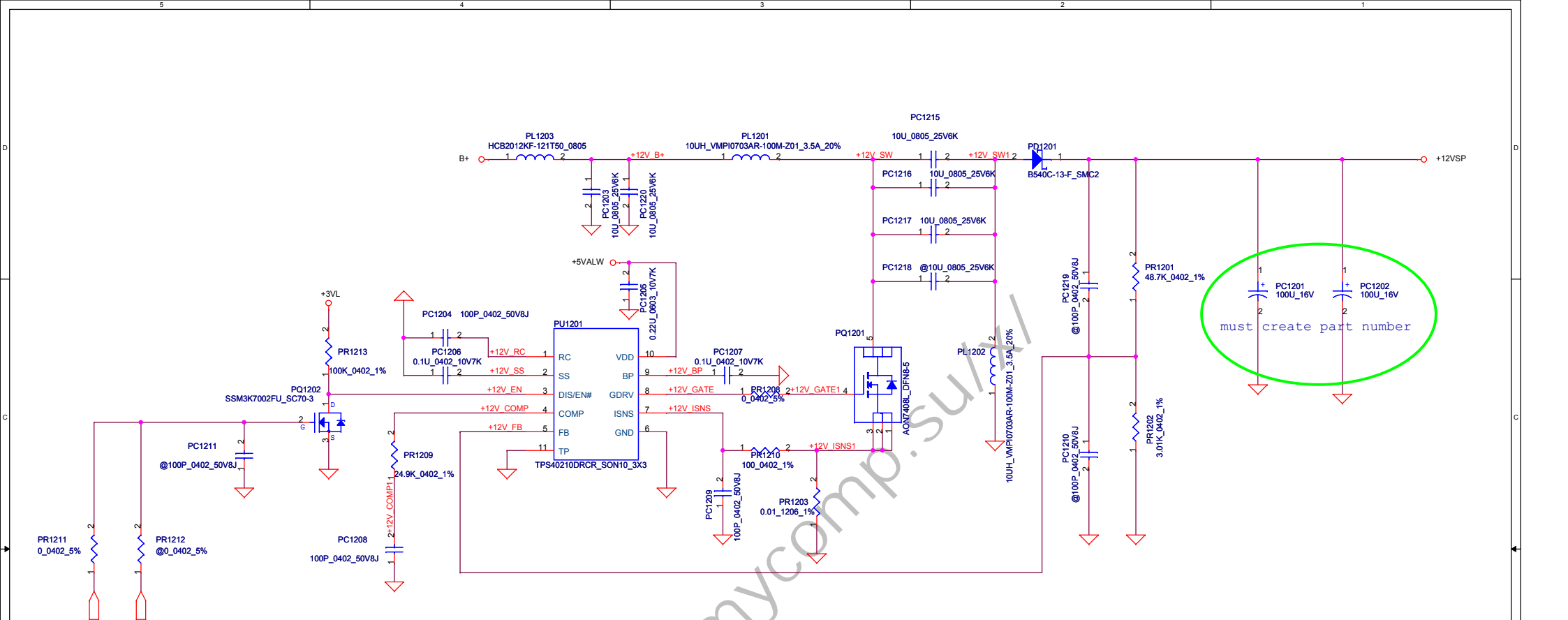
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Size	Custom	Document Number		Rev	0.1
Date:	Friday, January 21, 2011	Sheet	56	of	58



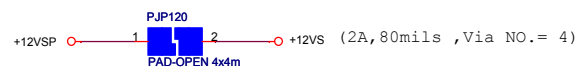
N12P-GS Ipeak=35.32A							
GPU_VID1	GPU_VID0	+VGA_CORE	PR901	PR902	PR903	PR904	PL901
0	0	0.825V	1.8K	10.5K	8.87K	54.9K	0.36uH
0	1	0.975V					
1	1	1.0V					

N12P-GV Ipeak=21.56A							
GPU_VID1	GPU_VID0	+VGA_CORE	PR901	PR902	PR903	PR904	PL901
0	0	0.85V	1.8K	10.5K	8.87K	54.9K	0.36uH
0	1	1.0V					
1	1	1.025V					

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					PBL21 LA671P M/B	0.1	
Date: Friday, January 21, 2011				Sheet	57	of	58



must create part number



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				Document Number	PBL21 LA6771P M/B
Date:	Friday, January 21, 2011	Sheet	58	of	58