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MODEL NAME : *QAL70*

PCB NO : *LA-7741P(DAB00000800)*

BOM P/N : *4619EO31L01 TPM ;4519EO31L02 TPM/TAA*

GPIO MAP: *Rev0.9*

Dalmore 13 UMA

@ *Ivy Bridge + Panther POINT*

2011-06-23

REV : 0.1 (X00)

@ : Nopop Component

CONN@ : Connector Component

MB Type	BOM P/N	
TPM EN/ TCM DIS		1@ 3@
TPM DIS/ TCM EN		2@ 4@
TPM DIS/ TCM DIS		2@ 3@
TAA		@TAA

SPI ON BOARD

@SPI

MB PCB

Part Number	Description
DA800001700	PCB OFH LA-6562P REV0 M/B UMA

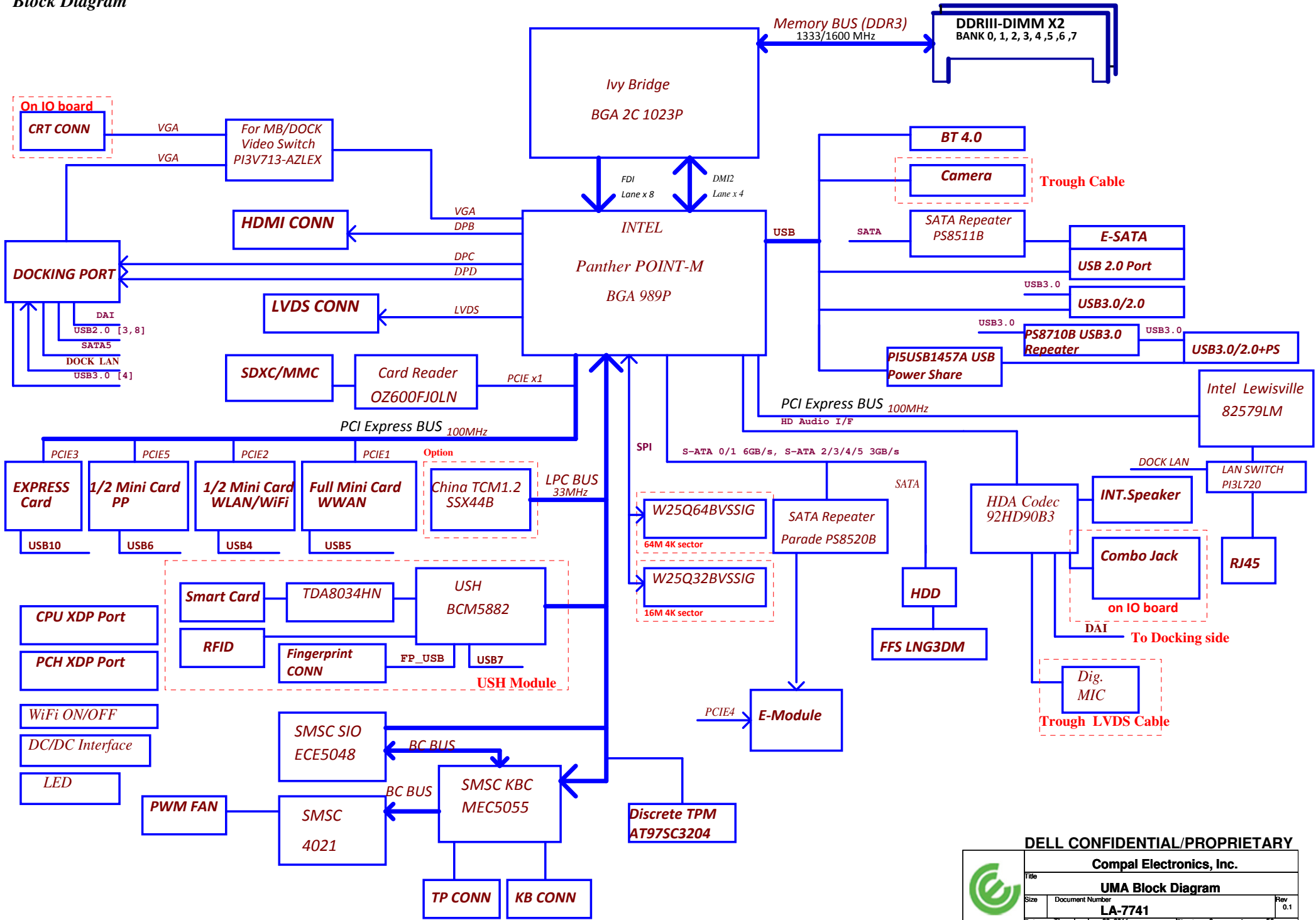
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Block Diagram



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UMA Block Diagram		
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side)
	1	JUSB2 (Rear Left side)
	2	NA
	3	MLK DOCK
	4	WLAN
	5	WWAN
	6	JMINI3(PP)
	7	USH->BIO
	8	DOCKING
	9	JESATA1 (right side)
	10	Express card
	11	Bluetooth
	12	Camera
13	NA	

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

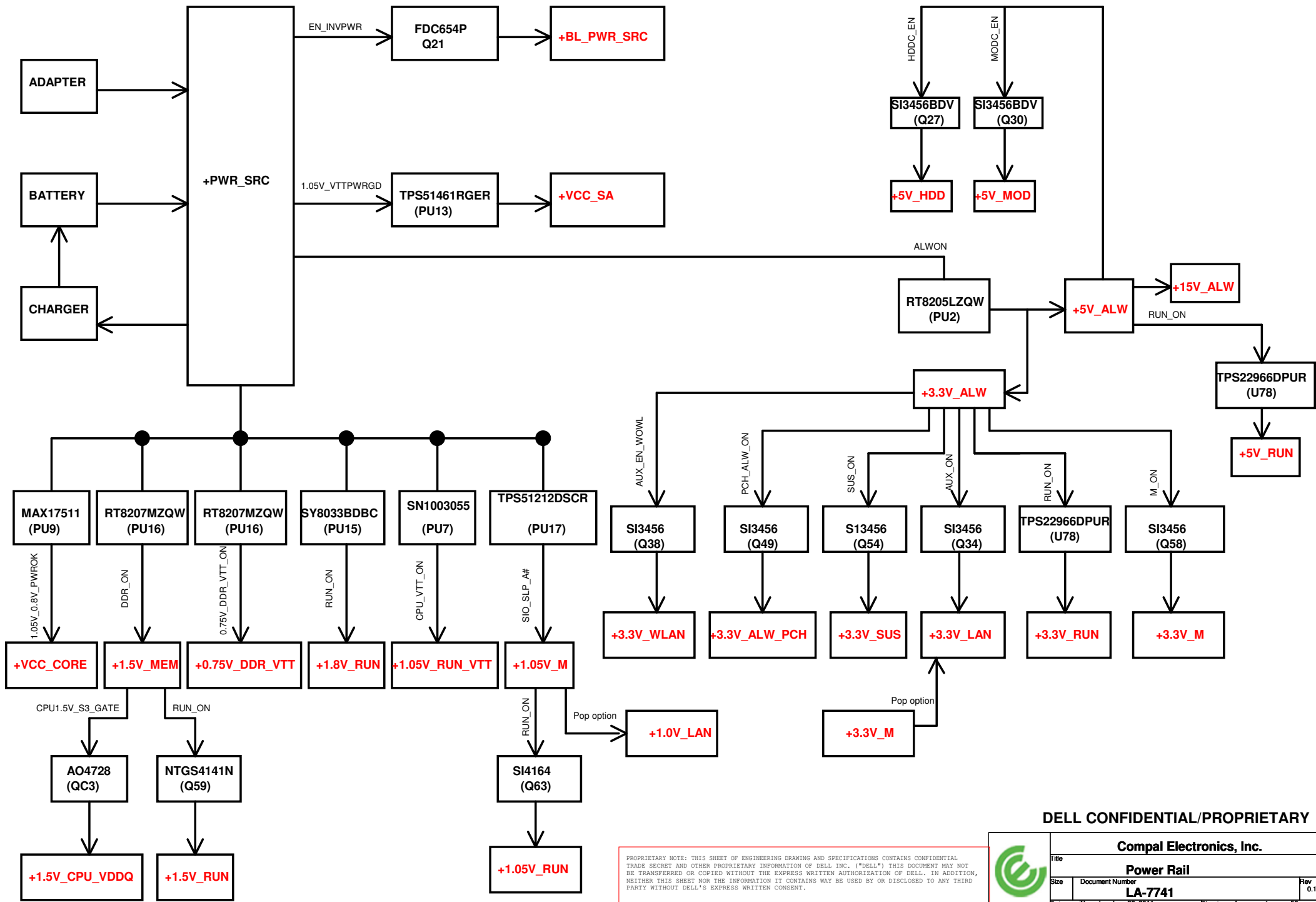
UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

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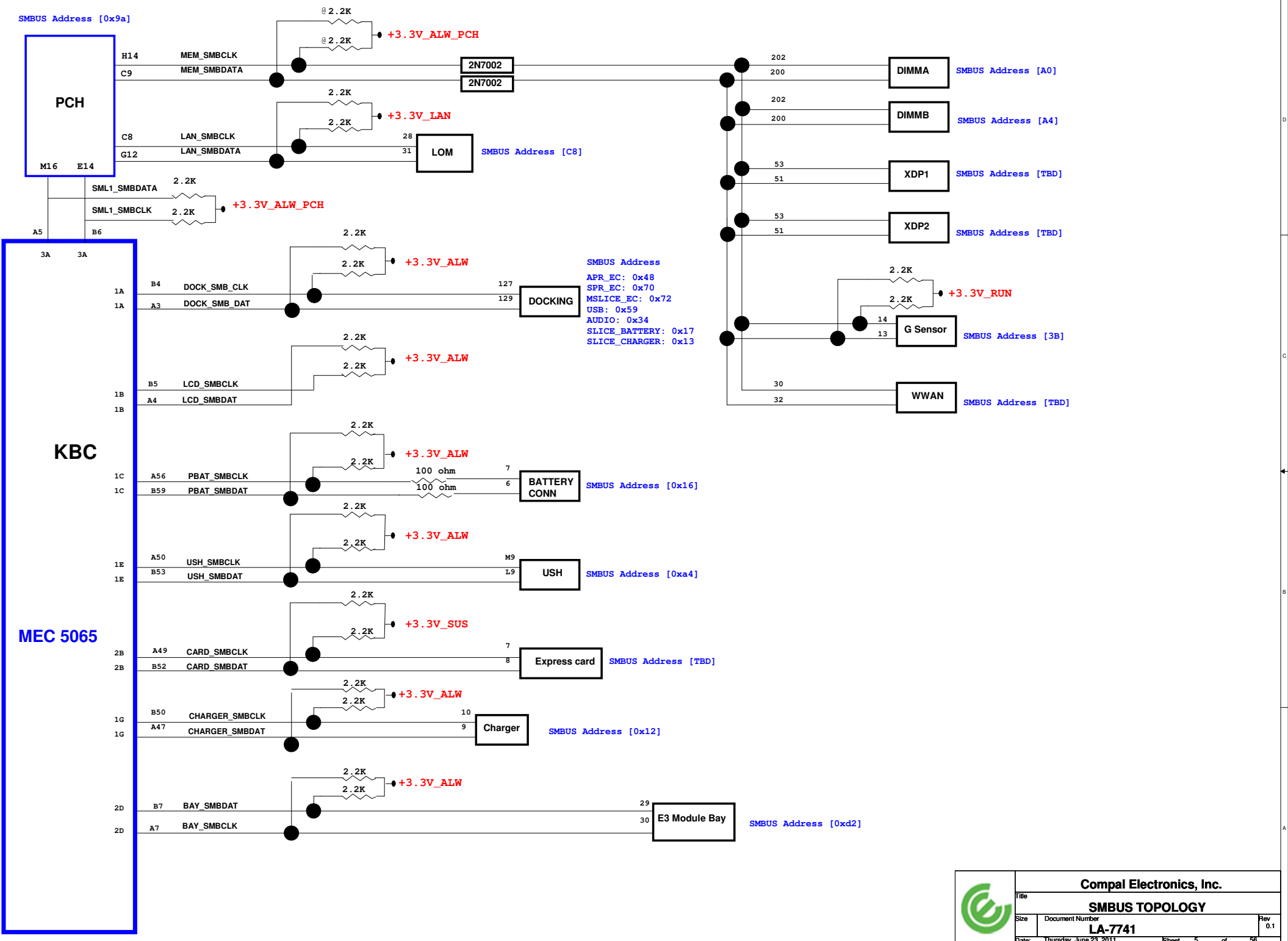




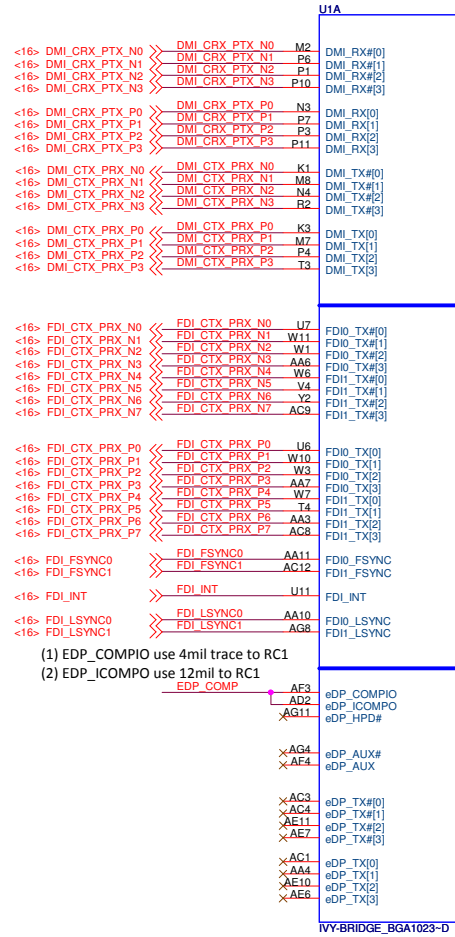
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(1) PEG_RCOMP0 (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
 (2) PEG_ICOMPO use 12mil connect to RC2



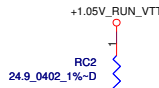
eDP Compensation

+1.05V_RUN_VTT

RC1
24.9_0402_1%-D

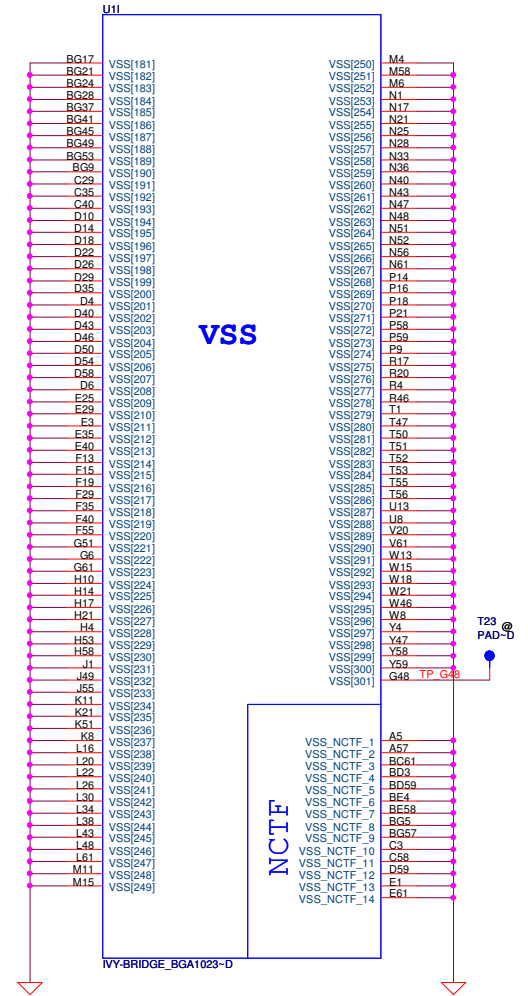
EDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PEG Compensation

PEG_ICOMPI and RCOMP0 signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

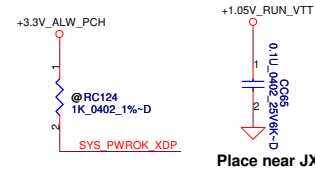
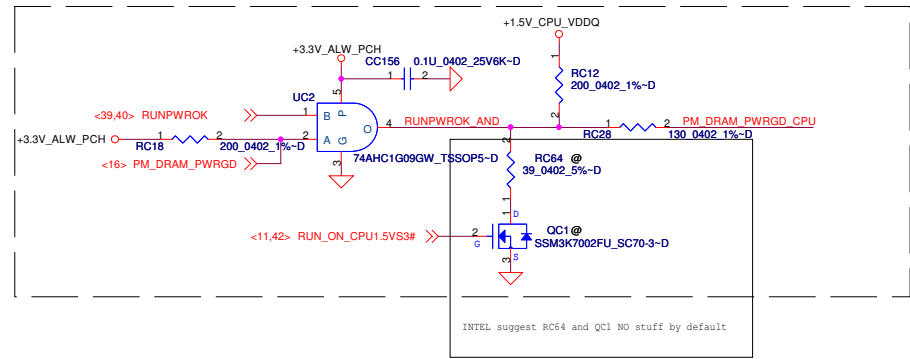


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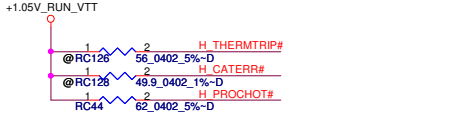
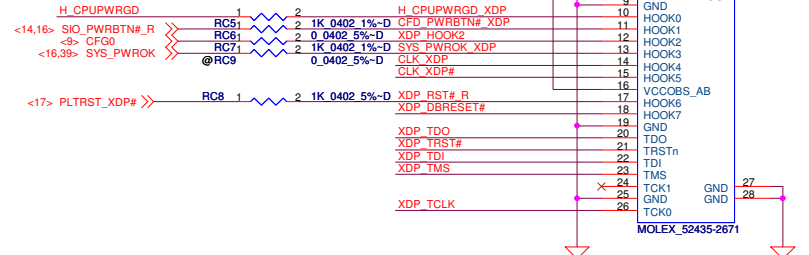
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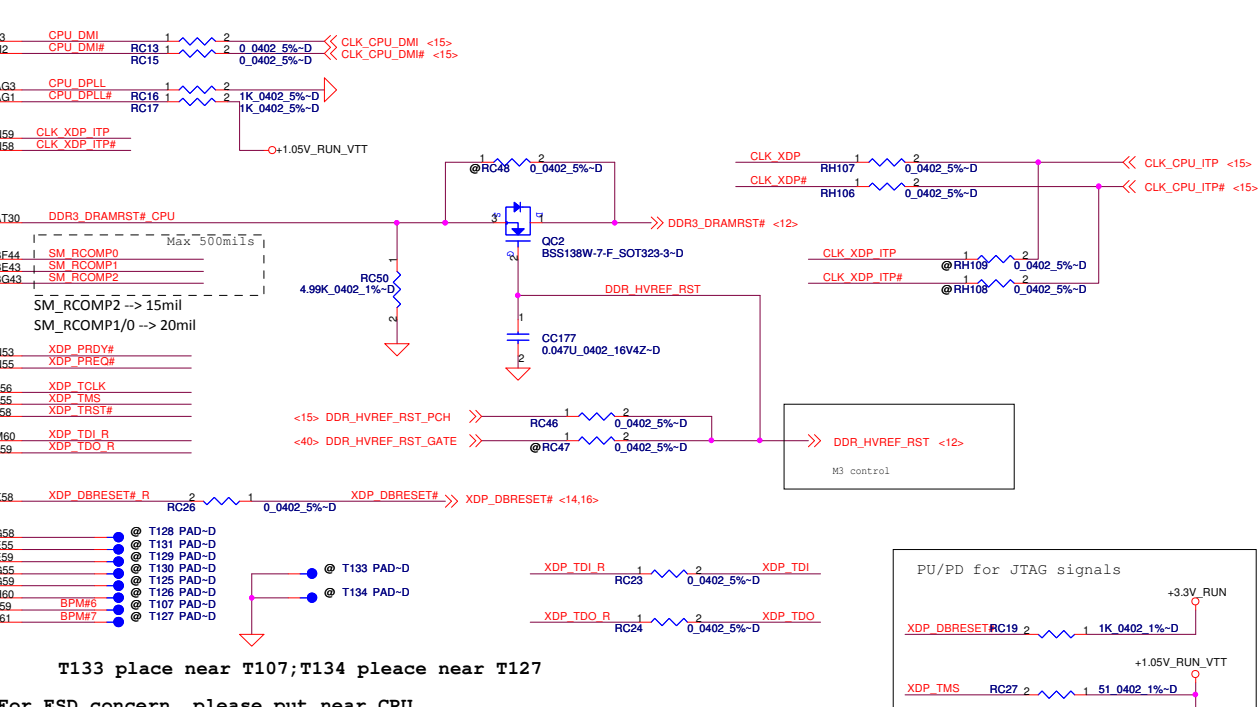
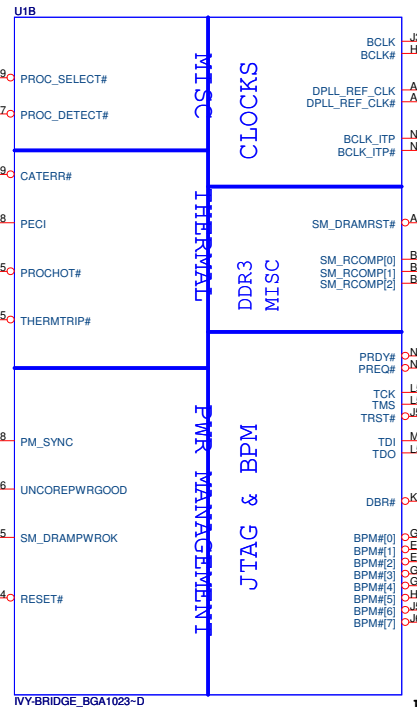
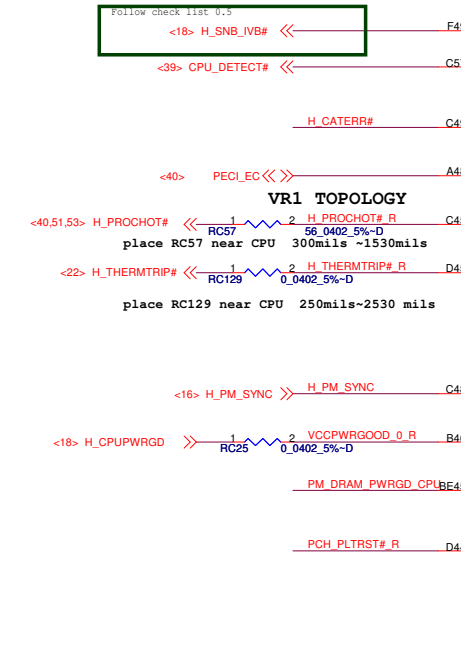
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Place near JXDP1

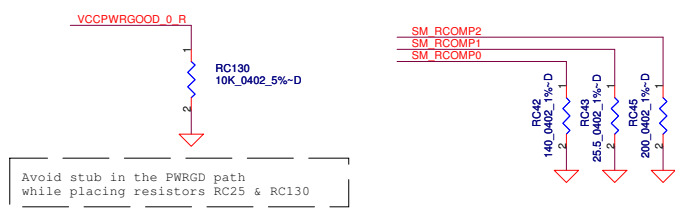
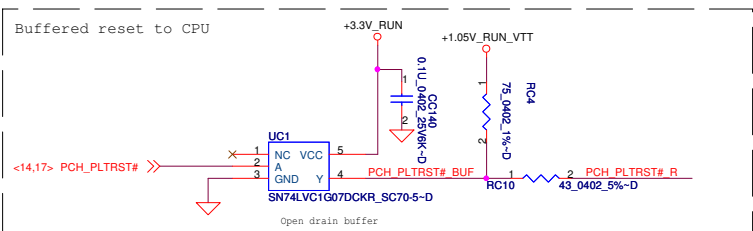


Follow check list U.5
<18> H_SNB_IVB# <<<
<39> CPU_DETECT# <<<

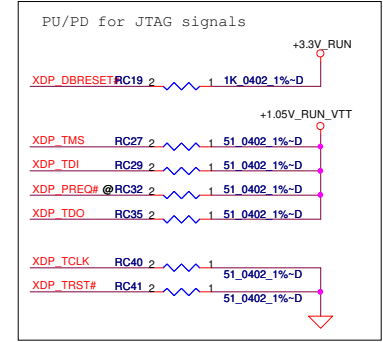


T133 place near T107; T134 place near T127

For ESD concern, please put near CPU



Avoid stub in the PWRGD path while placing resistors RC25 & RC130



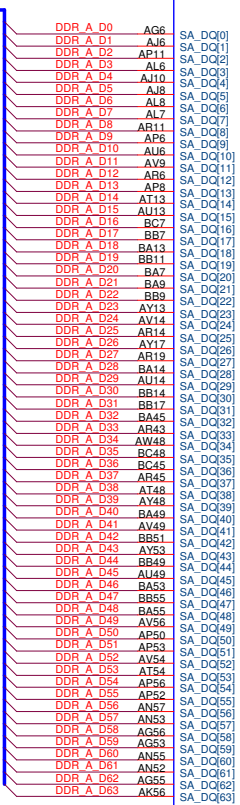
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<12> DDR_A_D[0..63] <<>

UIC

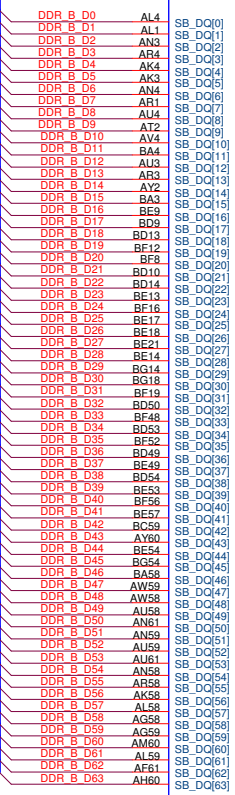


DDR SYSTEM MEMORY A

IVY-BRIDGE_BGA1023-D

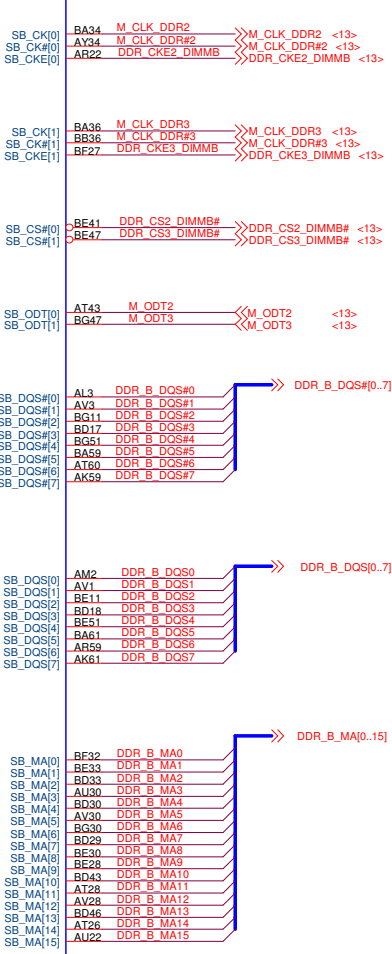
<13> DDR_B_D[0..63] <<>

UID



DDR SYSTEM MEMORY B

IVY-BRIDGE_BGA1023-D



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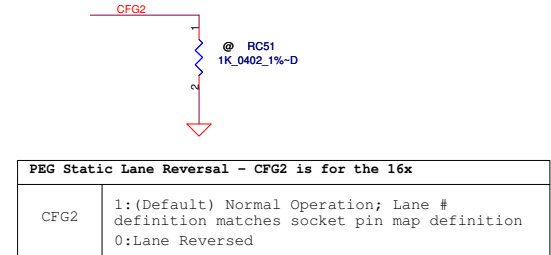
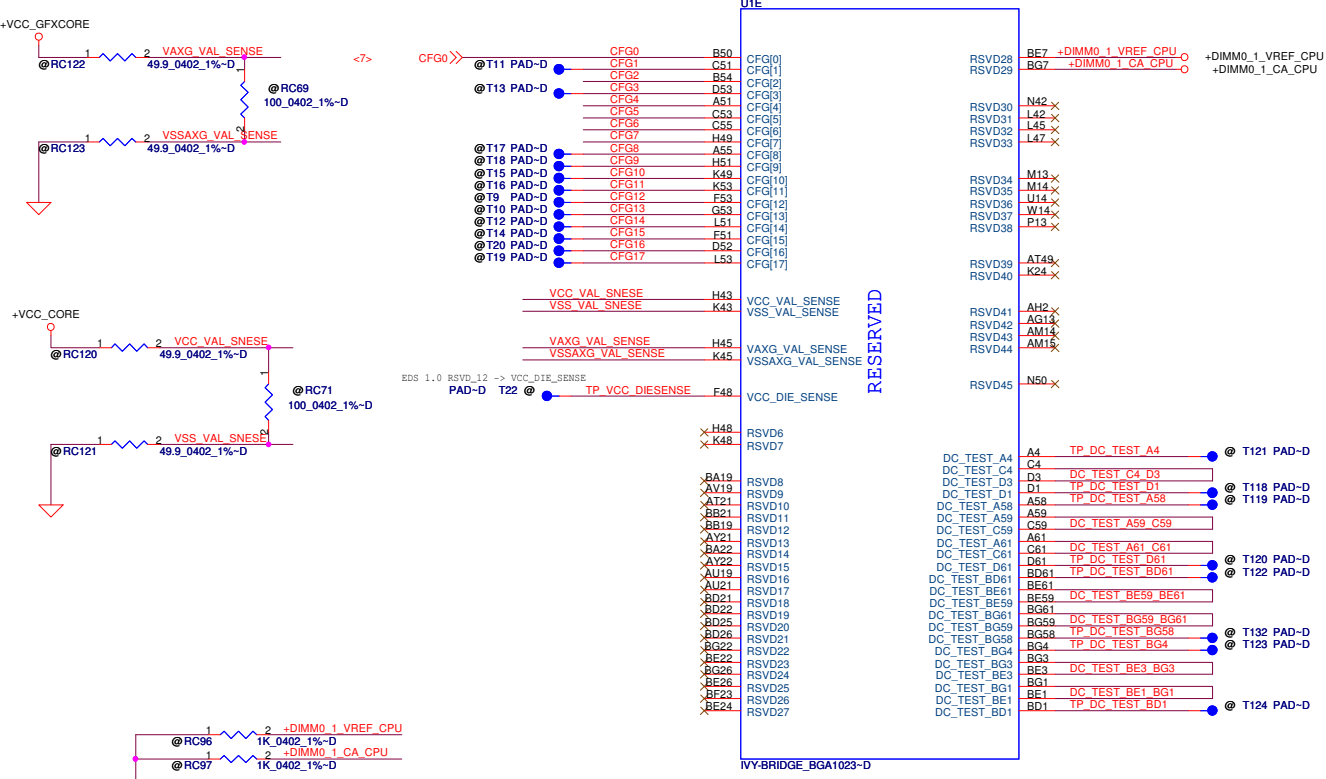
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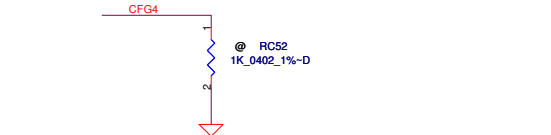
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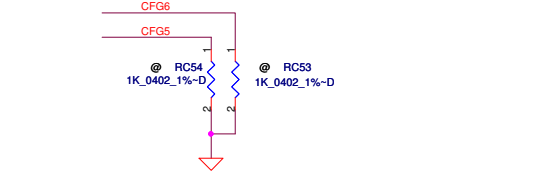
CFG Straps for Processor



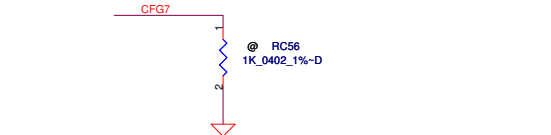
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



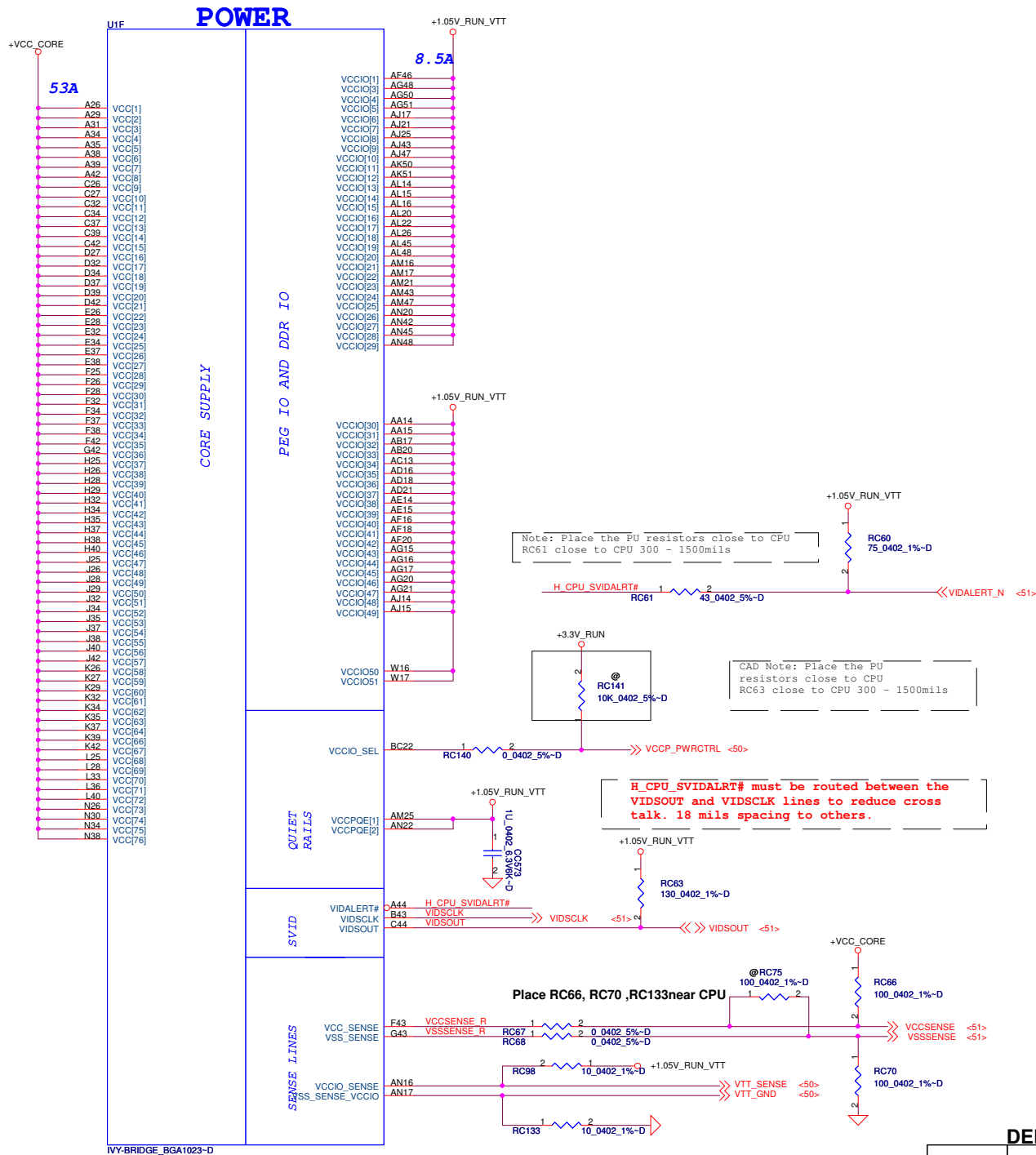
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

*** Description**

5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

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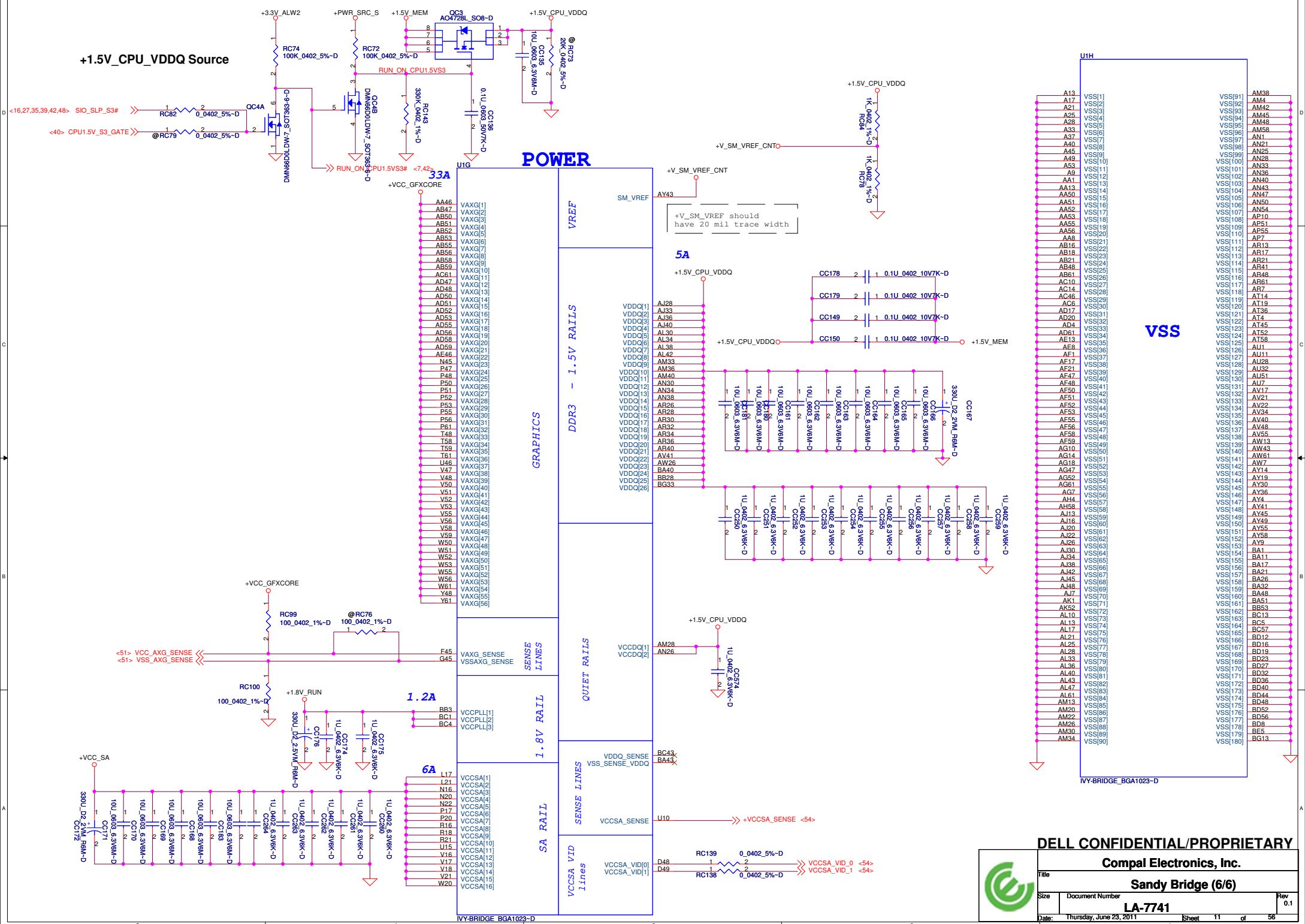
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+1.5V_CPU_VDDQ Source



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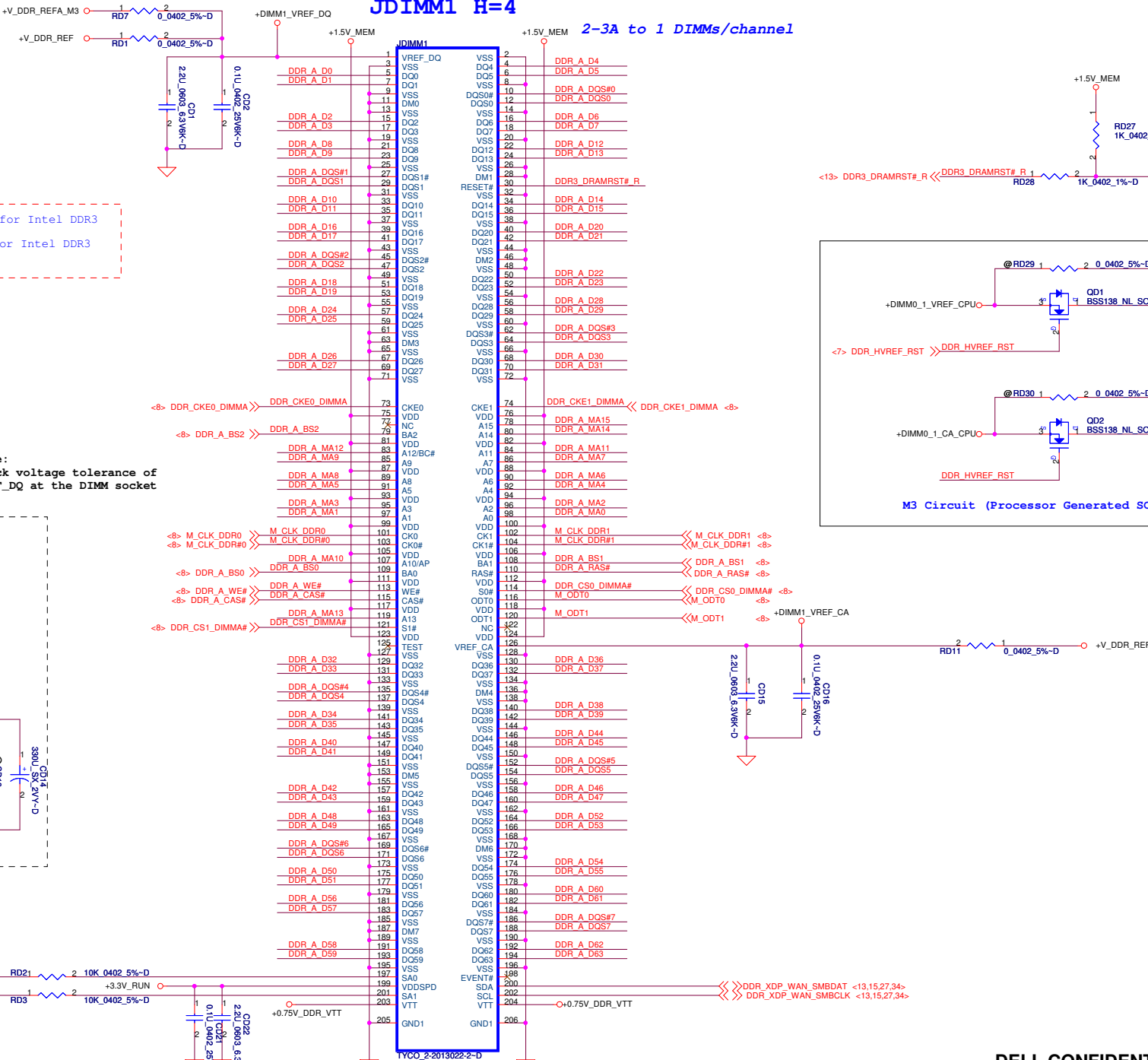
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JDIMM1 H=4

2-3A to 1 DIMMs/channel



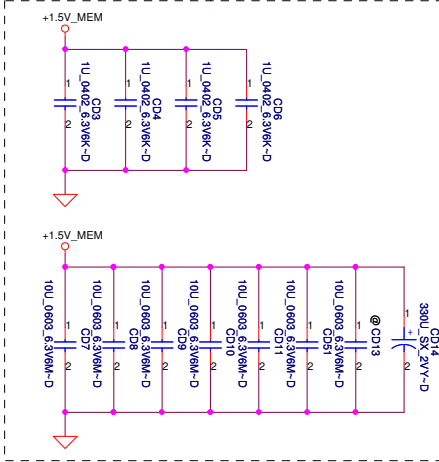
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

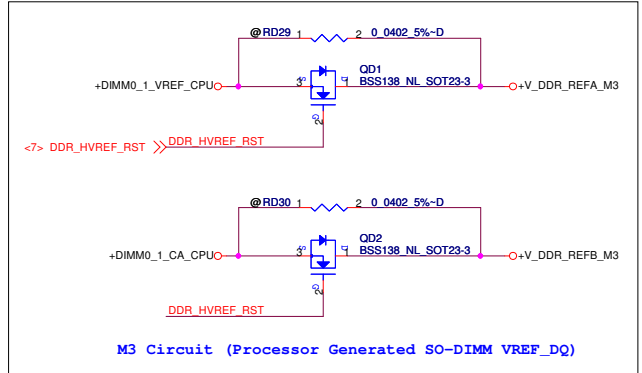
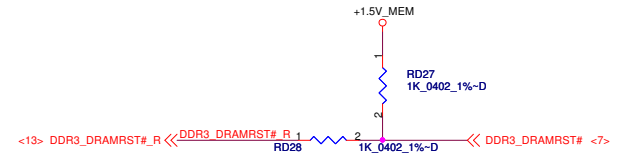
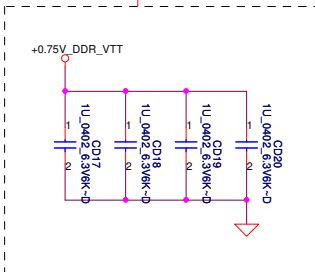
- <8> DDR_A_DOS#0..7
- <8> DDR_A_D0..63
- <8> DDR_A_DQS#0..7
- <8> DDR_A_MA#0..15

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



Layout Note:
Place near JDIMM1.203, 204



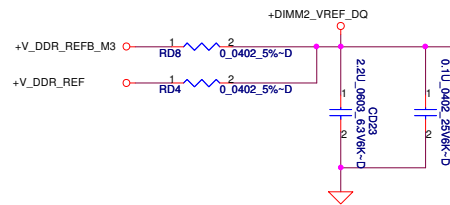
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JDIMMB H=8



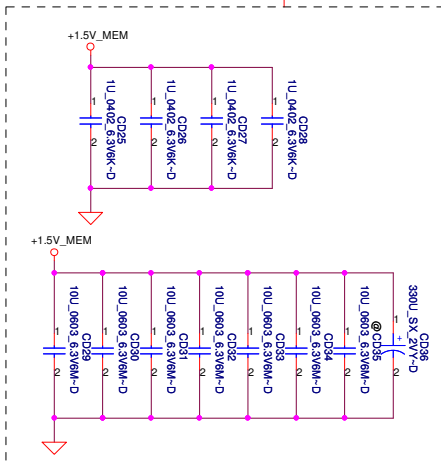
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3

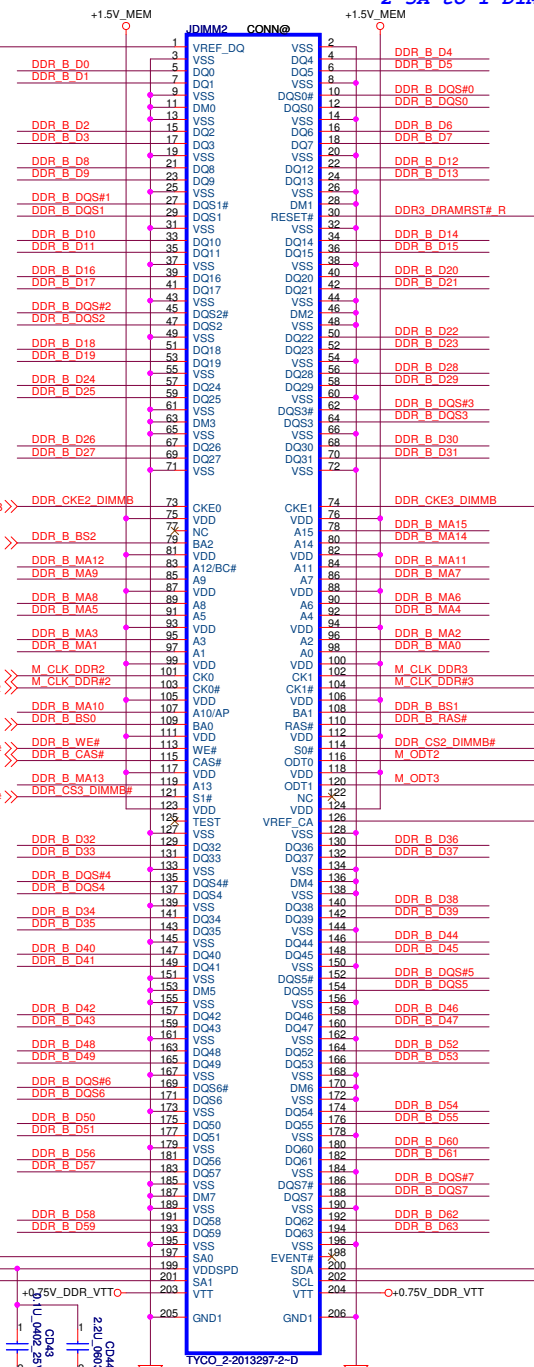
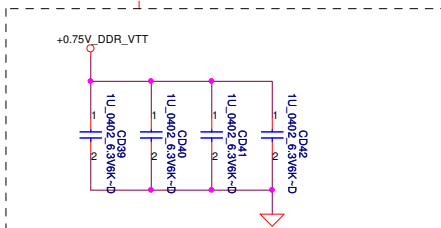
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- <8> DDR_B_DQ[0.63] <<>
- <8> DDR_B_DQS#0[.7] <<>
- <8> DDR_B_MA[0.15] <<>

All VREF traces should
have 10 mil trace width

Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204



- <8> DDR_CKE2_DIMMB >>> DDR_CKE2_DIMMB
- <8> DDR_BS2 >>> DDR_BS2
- <8> M_CLK_DDR2 >>> M_CLK_DDR2
- <8> M_CLK_DDR#2 >>> M_CLK_DDR#2
- <8> DDR_MA10 >>> DDR_MA10
- <8> DDR_BS0 >>> DDR_BS0
- <8> DDR_WE# >>> DDR_WE#
- <8> DDR_CAS# >>> DDR_CAS#
- <8> DDR_CAS# >>> DDR_CAS#
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- <8> DDR_CS3_DIMMB# >>> DDR_CS3_DIMMB#
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- <8> DDR_B_D34 >>> DDR_B_D34
- <8> DDR_B_D35 >>> DDR_B_D35
- <8> DDR_B_D40 >>> DDR_B_D40
- <8> DDR_B_D41 >>> DDR_B_D41
- <8> DDR_B_D42 >>> DDR_B_D42
- <8> DDR_B_D43 >>> DDR_B_D43
- <8> DDR_B_D48 >>> DDR_B_D48
- <8> DDR_B_D49 >>> DDR_B_D49
- <8> DDR_B_DQS#6 >>> DDR_B_DQS#6
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- <8> DDR_B_D50 >>> DDR_B_D50
- <8> DDR_B_D51 >>> DDR_B_D51
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- <8> DDR_B_D57 >>> DDR_B_D57
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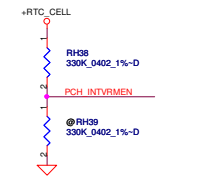
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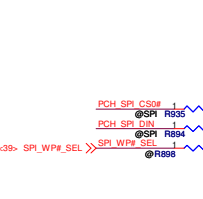
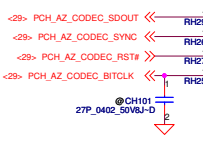
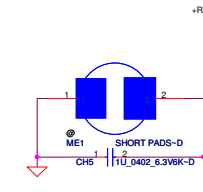
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DDRIII-SODIMM SLOT2	
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CMOS CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

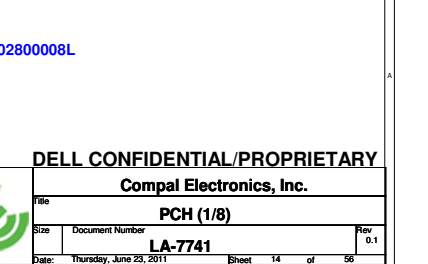
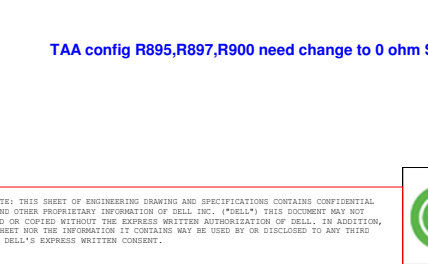
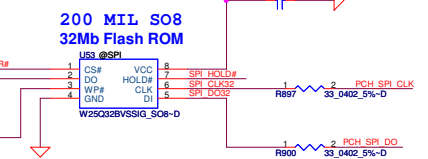
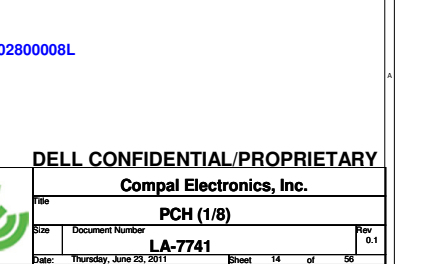
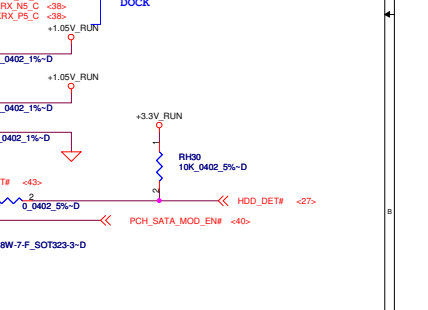
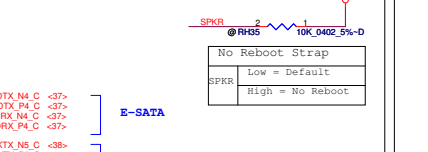
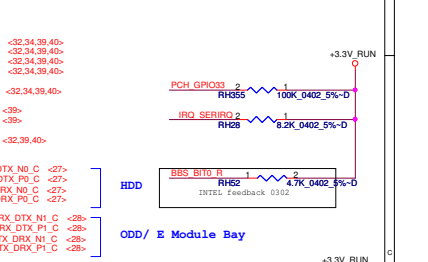
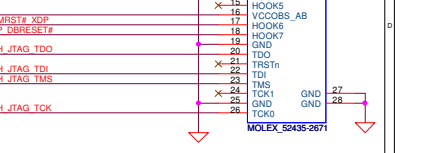
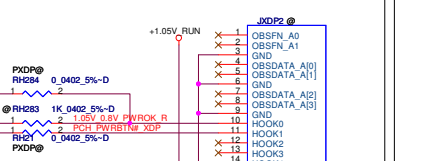
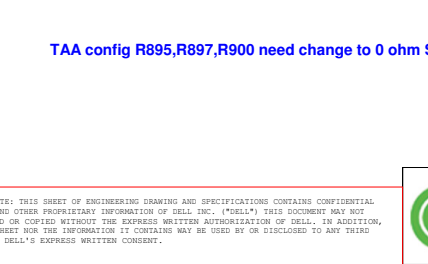
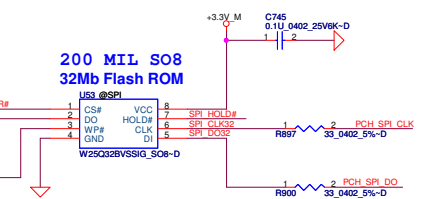
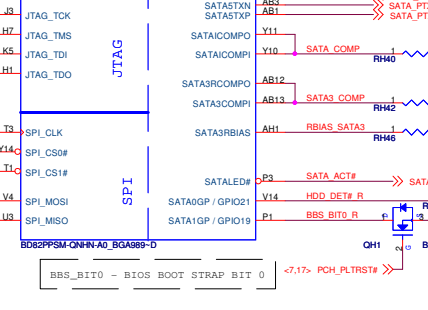
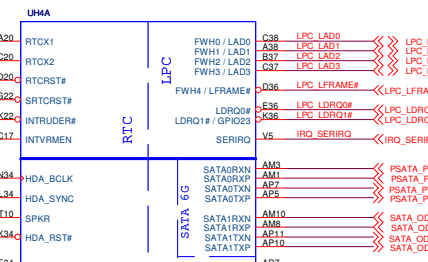
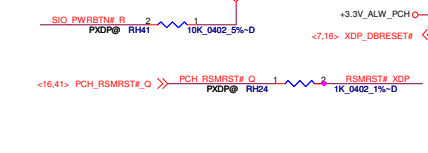
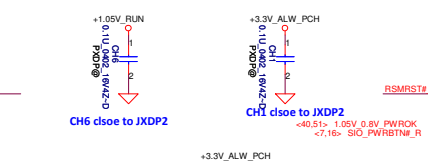
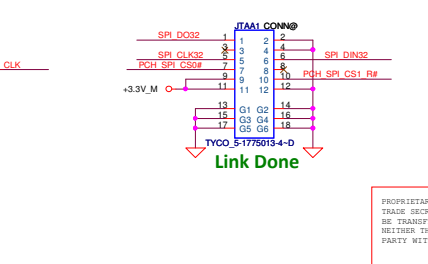
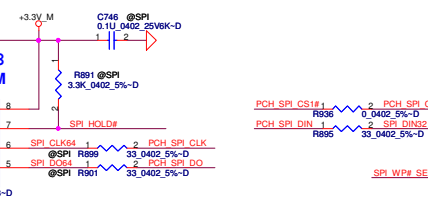
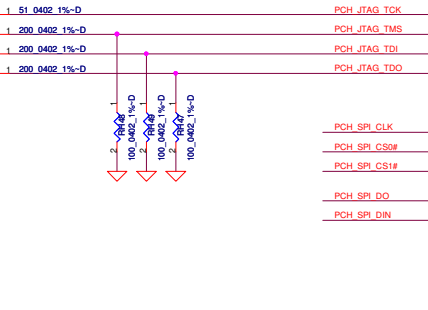
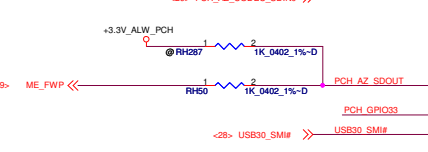
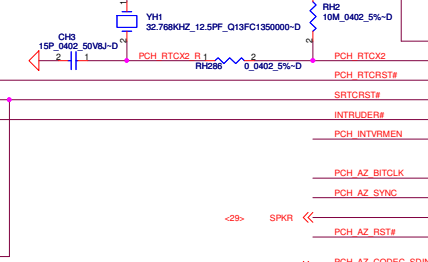
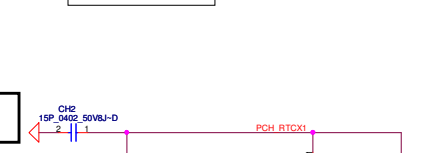
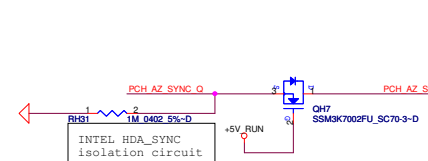
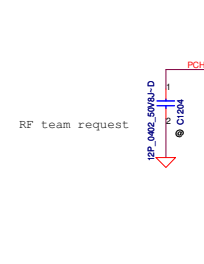
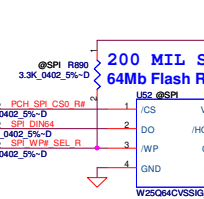
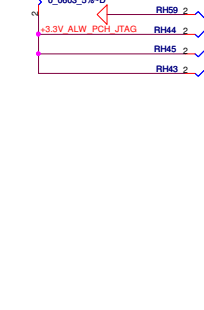
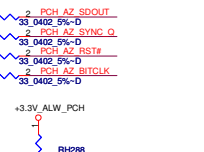
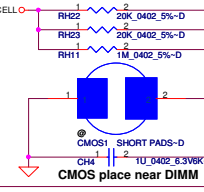


INTVRMEN - Integrated SUS
 1.1V VRM Enable
 High - Enable Internal VRs
 Low - Enable External VRs



Pch_Az_Sync is sampled at the rising edge of PWRBRT# pin. So signal should be P1 to the ADVA5 rail.

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low



TAA config R895,R897,R900 need change to 0 ohm SD02800008L

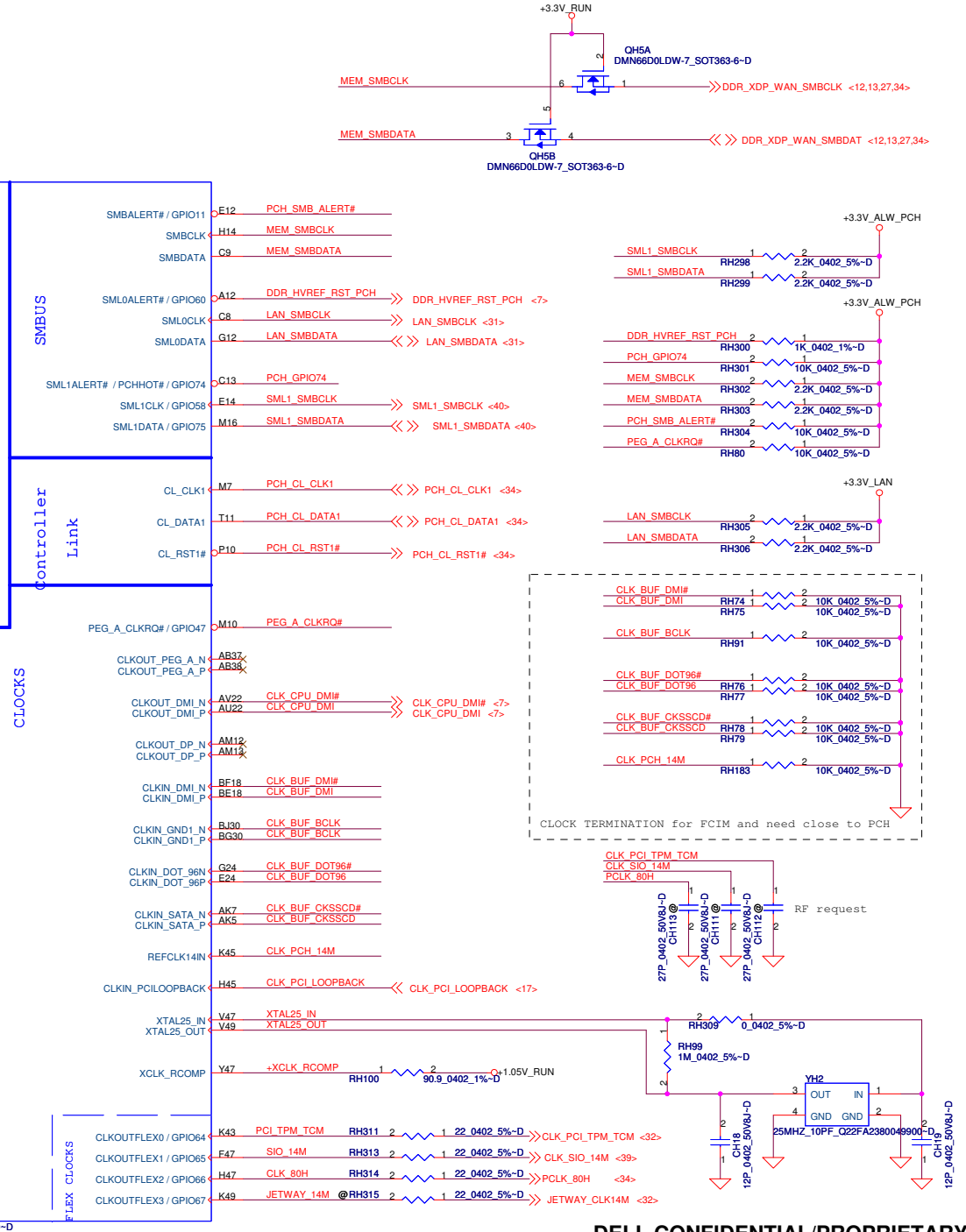
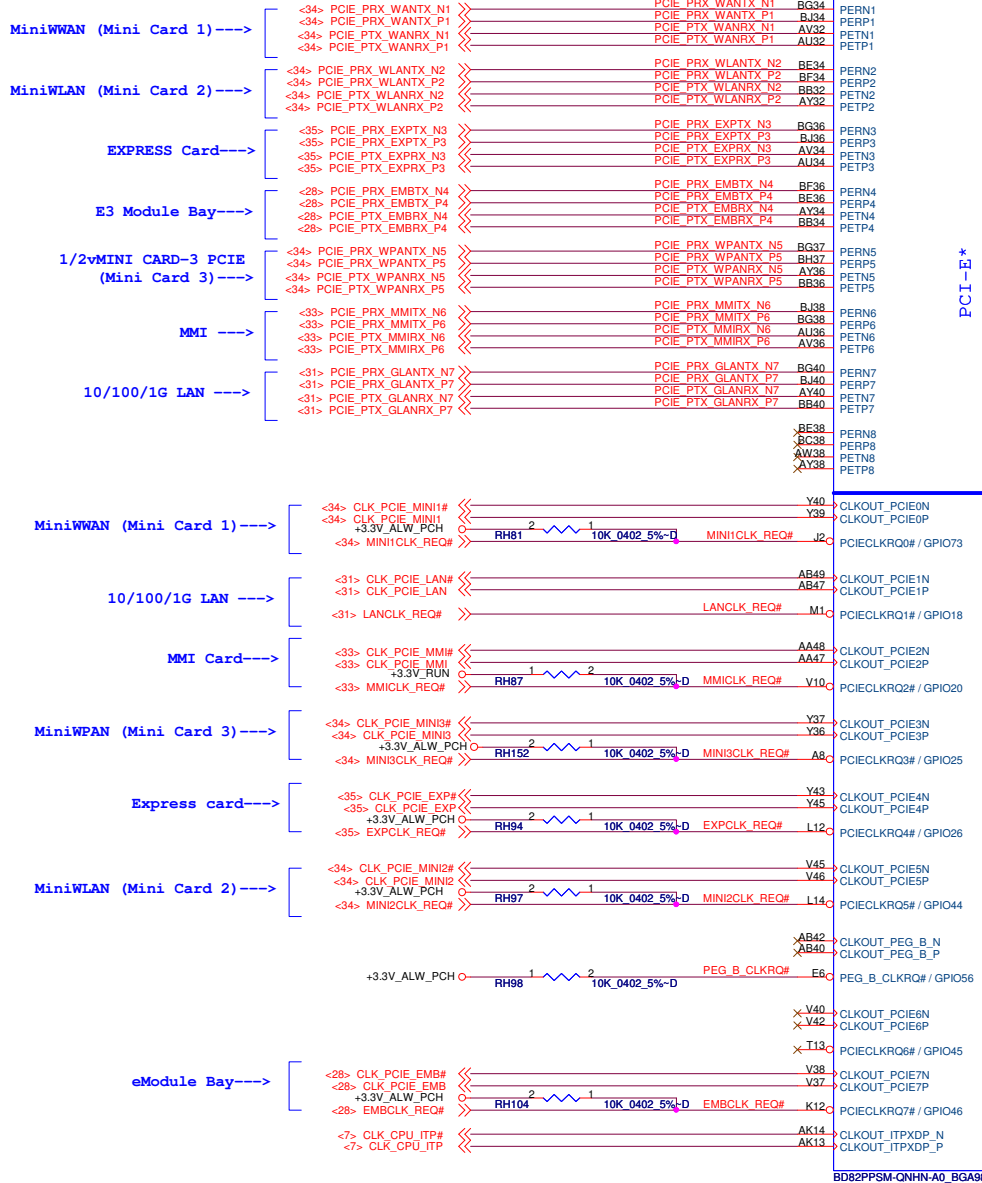
RF team request

Link Done

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 PCH (1/8)
 LA-7741
 Thursday, June 23, 2011

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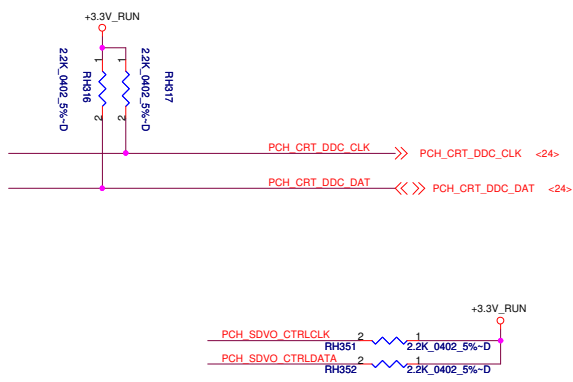
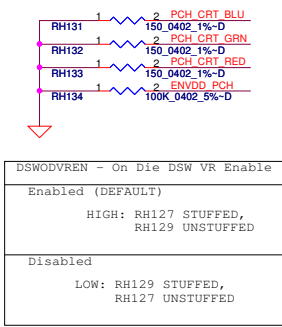
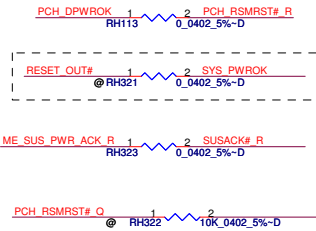
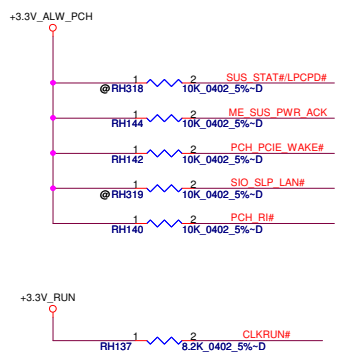
Follow DG0.9 Device down & Express/Mini card topology



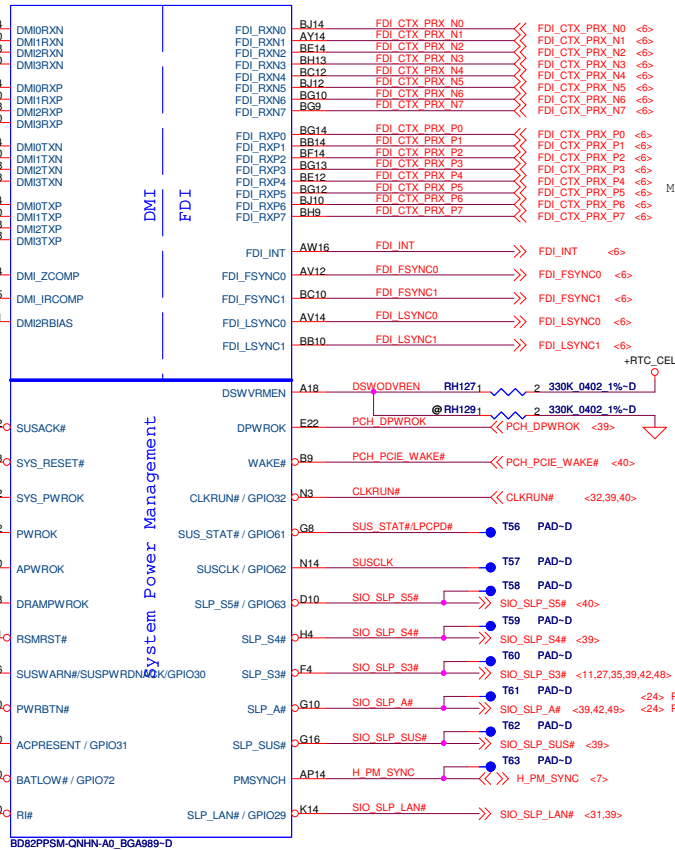
PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

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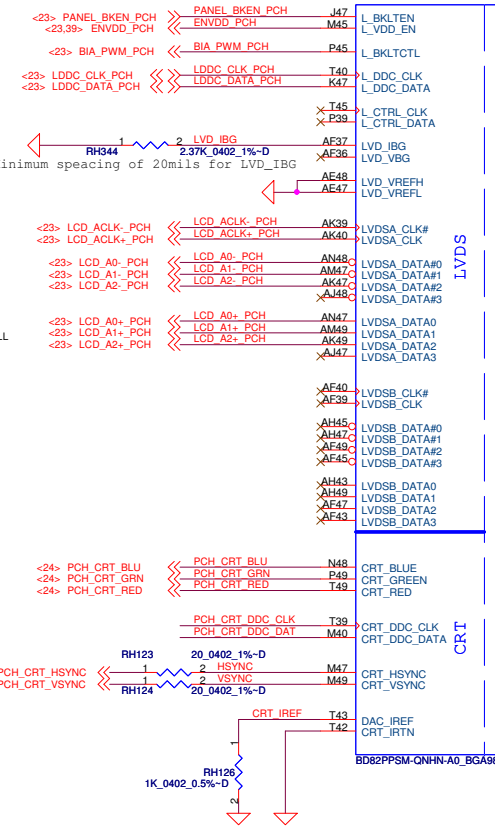
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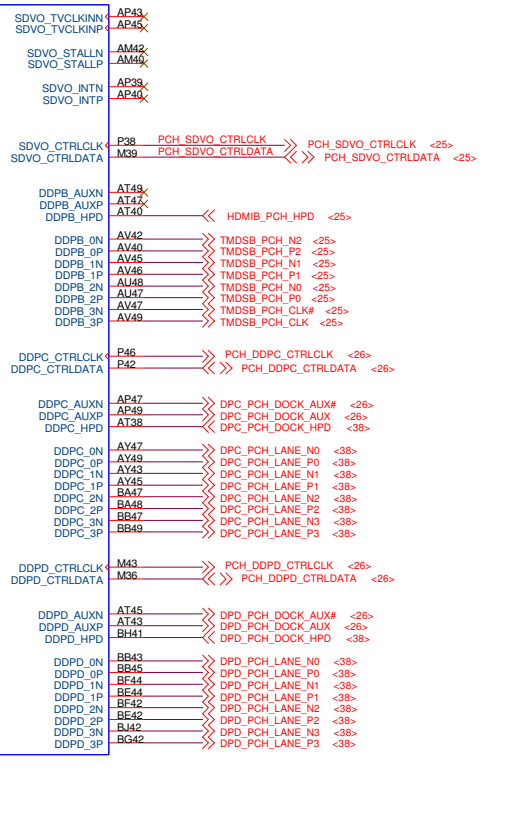
UH4C



UH4D



Digital Display Interface



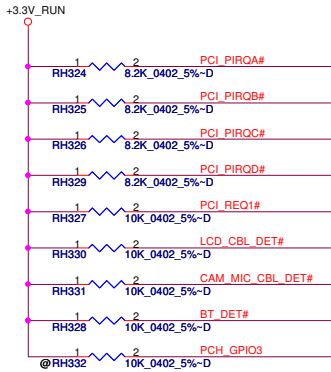
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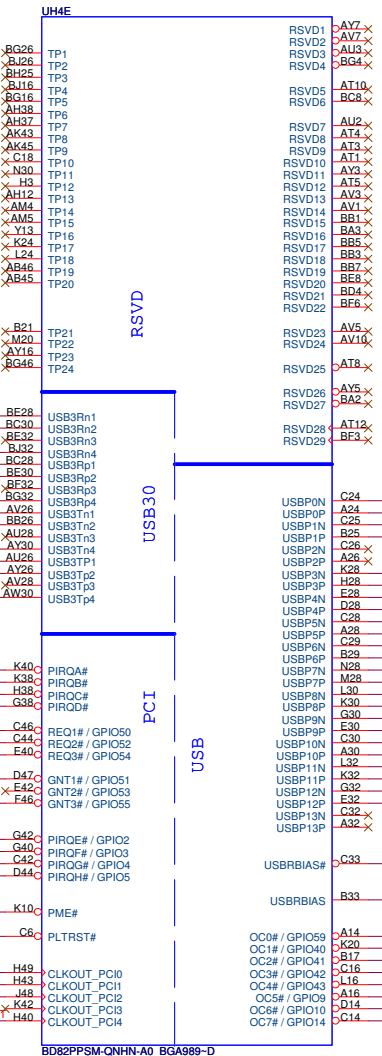
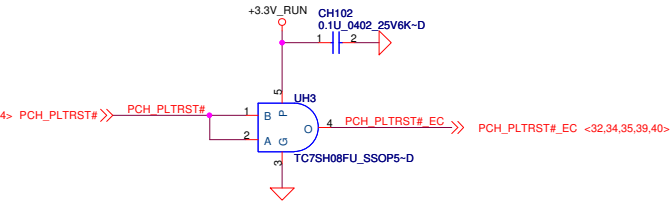
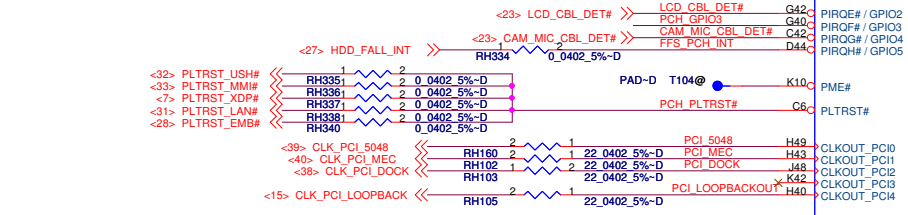
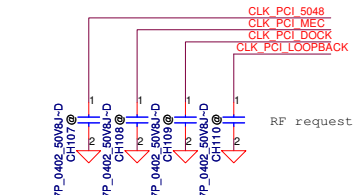
PCH (3/8)

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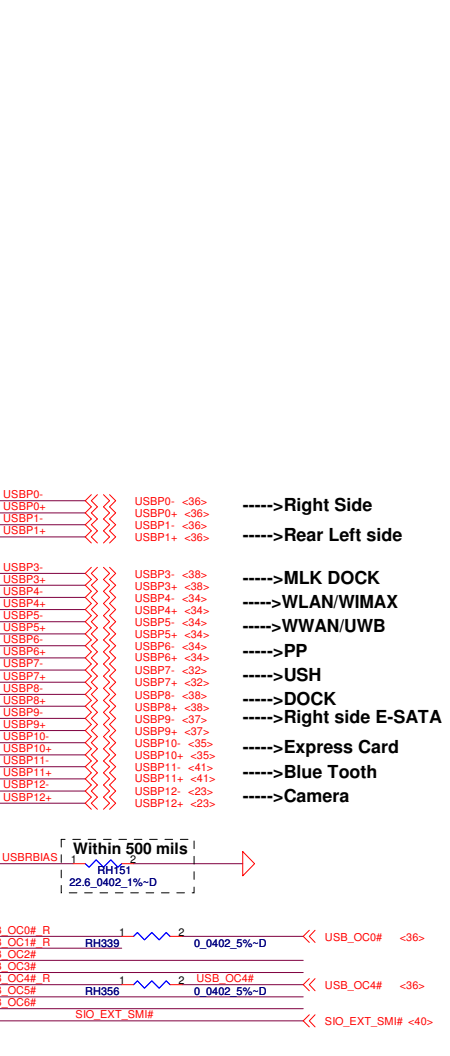
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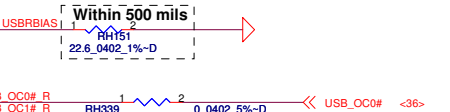
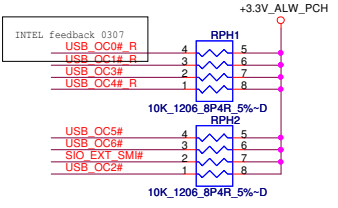
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default



BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



- >Right Side
- >Rear Left side
- >MLK DOCK
- >WLAN/WIMAX
- >WWAN/UWB
- >PP
- >USH
- >DOCK
- >Right side E-SATA
- >Express Card
- >Blue Tooth
- >Camera



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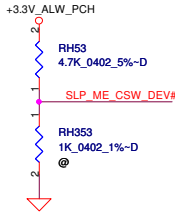
Compal Electronics, Inc.

PCH (4/8)

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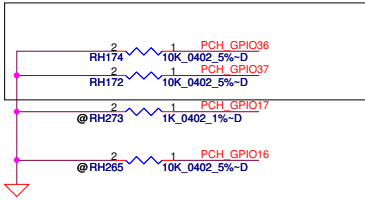
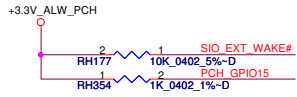
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* B082PPSM-QNHN-A0_BGA989-D

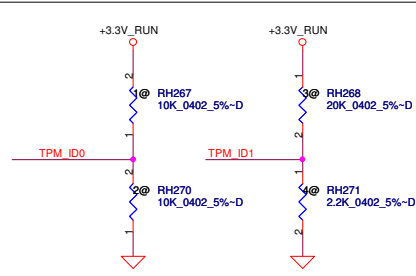
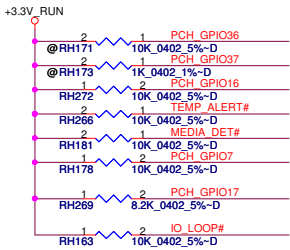
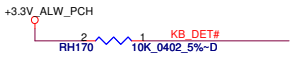


Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

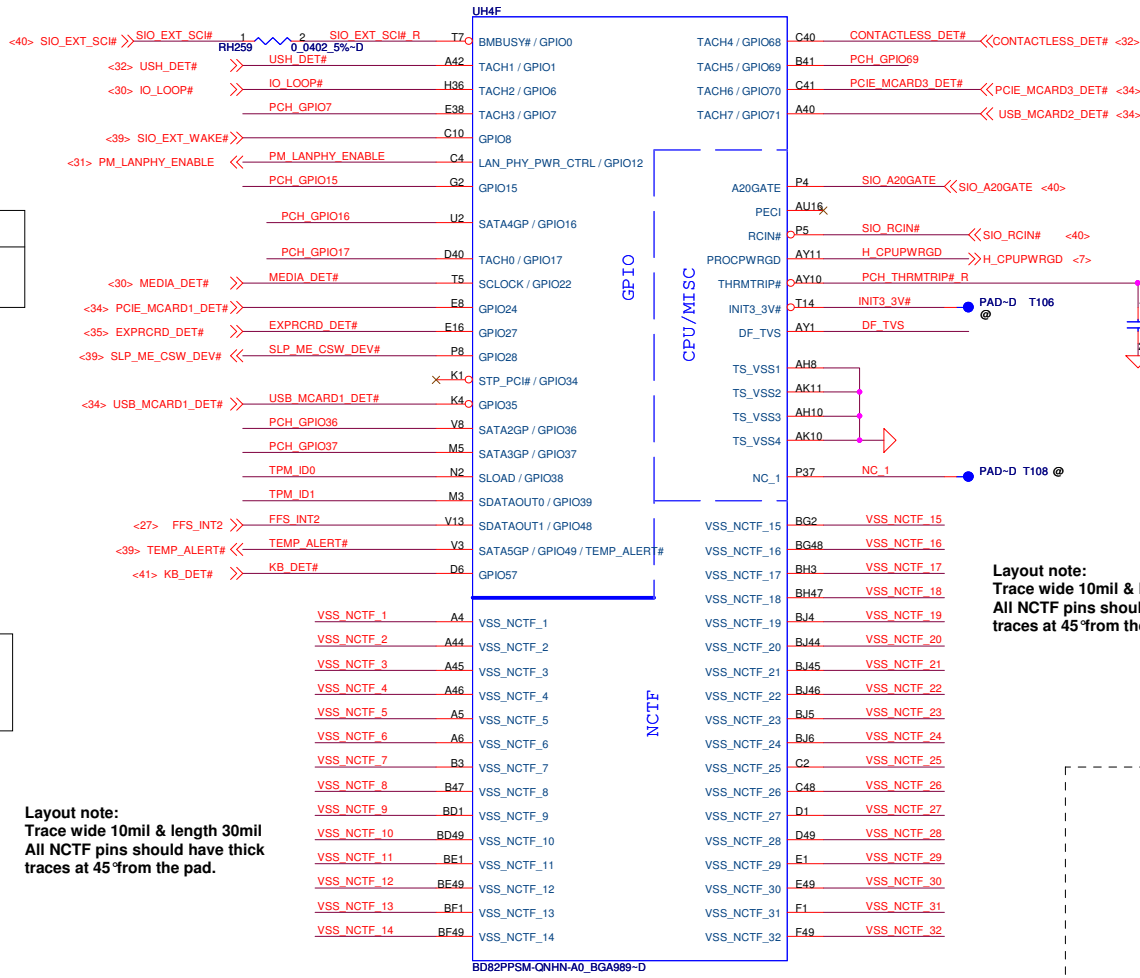
SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT	
DISABLED - LOW	



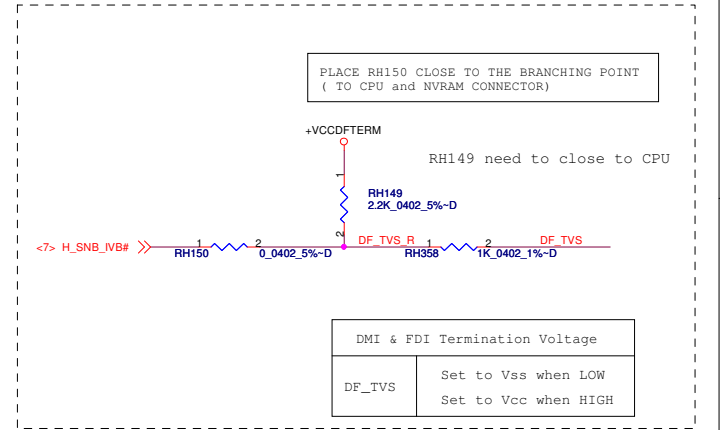
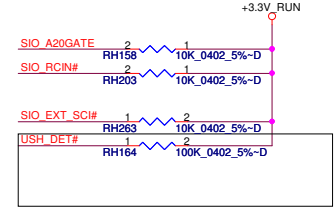
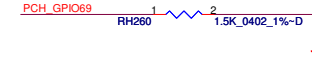
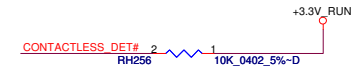
Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH1.0 (For SSI)	1	0
USH2.0	1	1



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



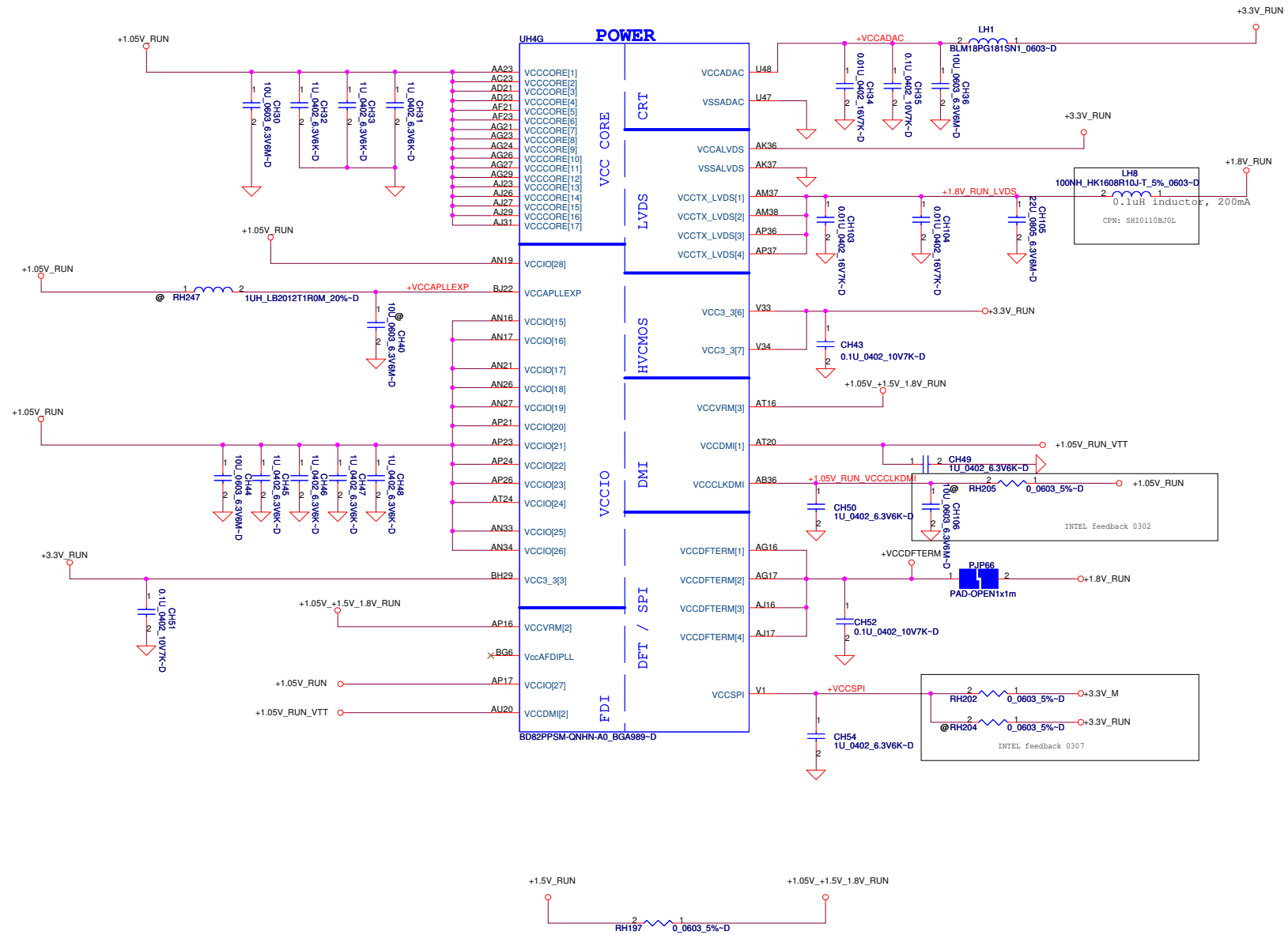
PLACE RH150 CLOSE TO THE BRANCHING POINT (TO CPU and NVRAM CONNECTOR)

RH149 need to close to CPU

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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POWER

USB

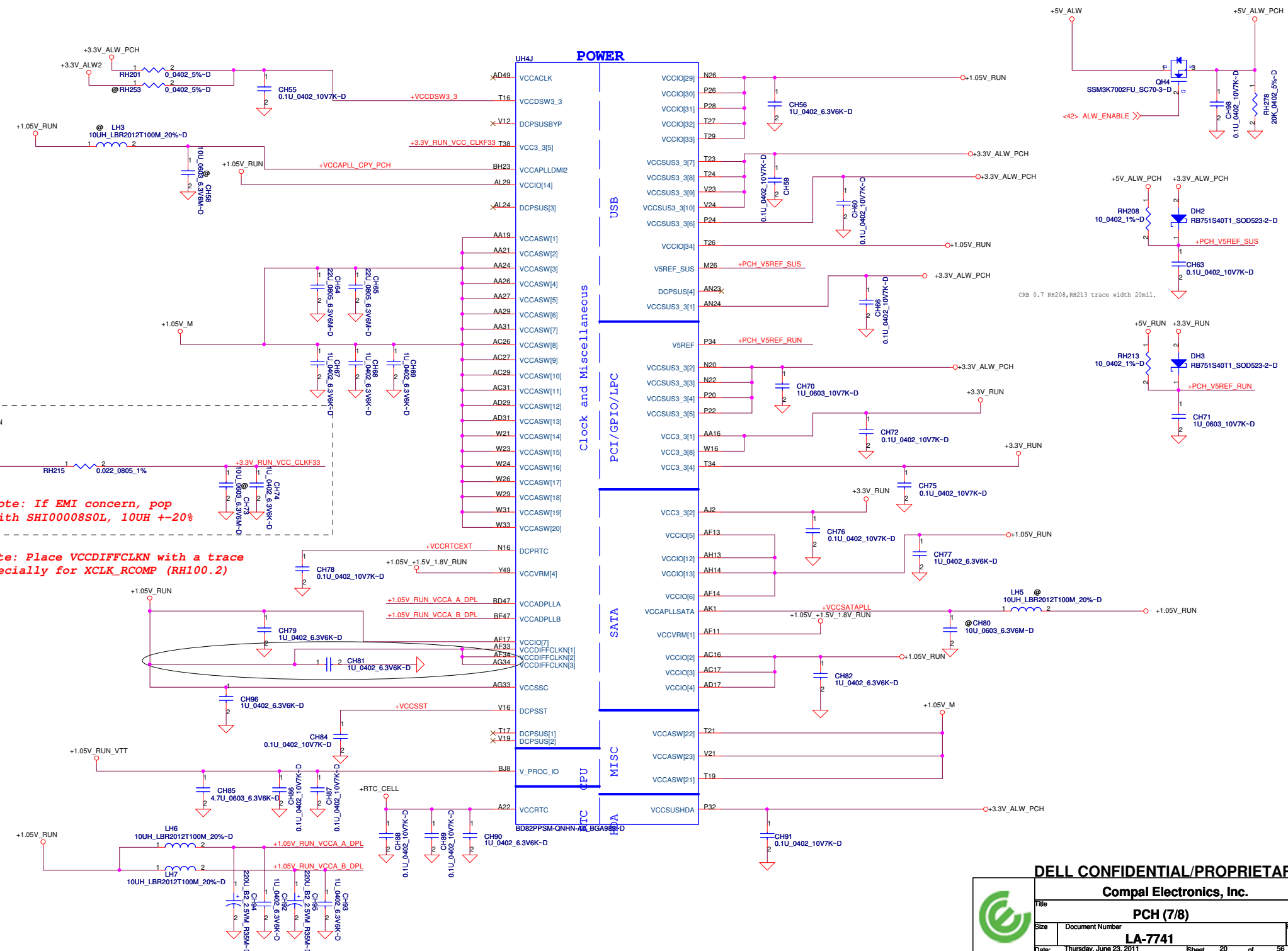
**Clock and Miscellaneous
PCI/GPIO/LPC**

SATA

MISC

ICP CPU

HA



Note: If EMI concern, pop with SHI0008SOL, 10UH +20%

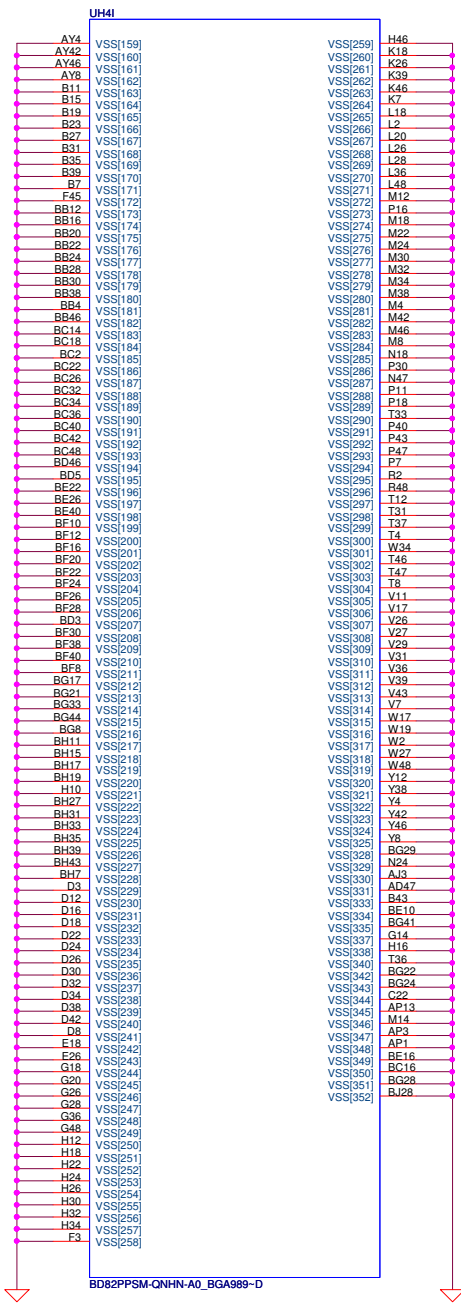
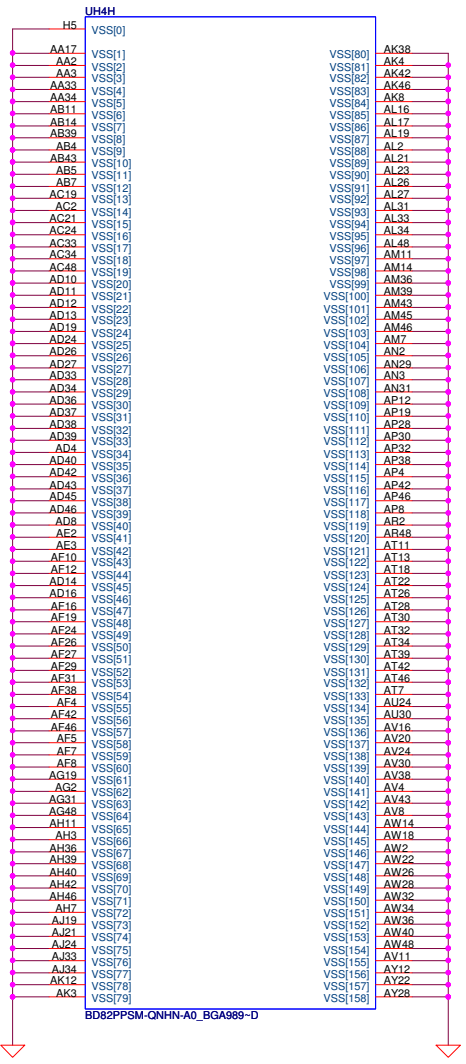
Note: Place VCCDIFFCLKN with a trace specially for XCLK_RCOMP (RH100.2)

CRB 0.7 RH208, RH213 trace width 20mil.

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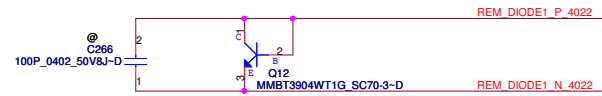
Compal Electronics, Inc.

Title: **PCH (8/8)**

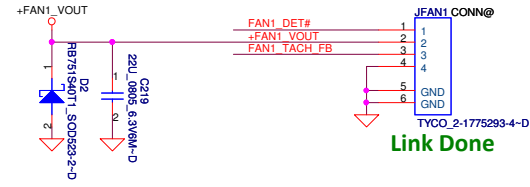
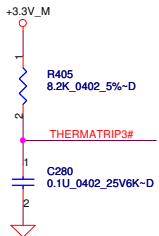
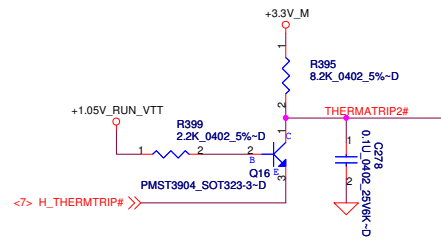
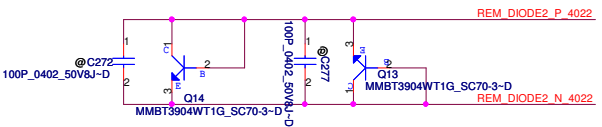
Size: **LA-7741** Rev: **0.1**

Date: **Thursday, June 23, 2011** Sheet: **21** of **56**

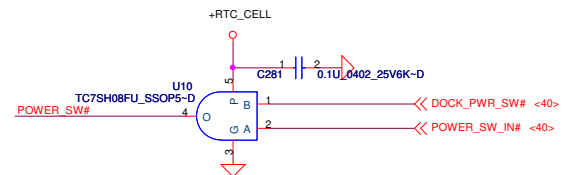
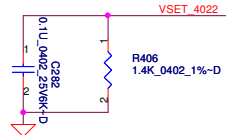
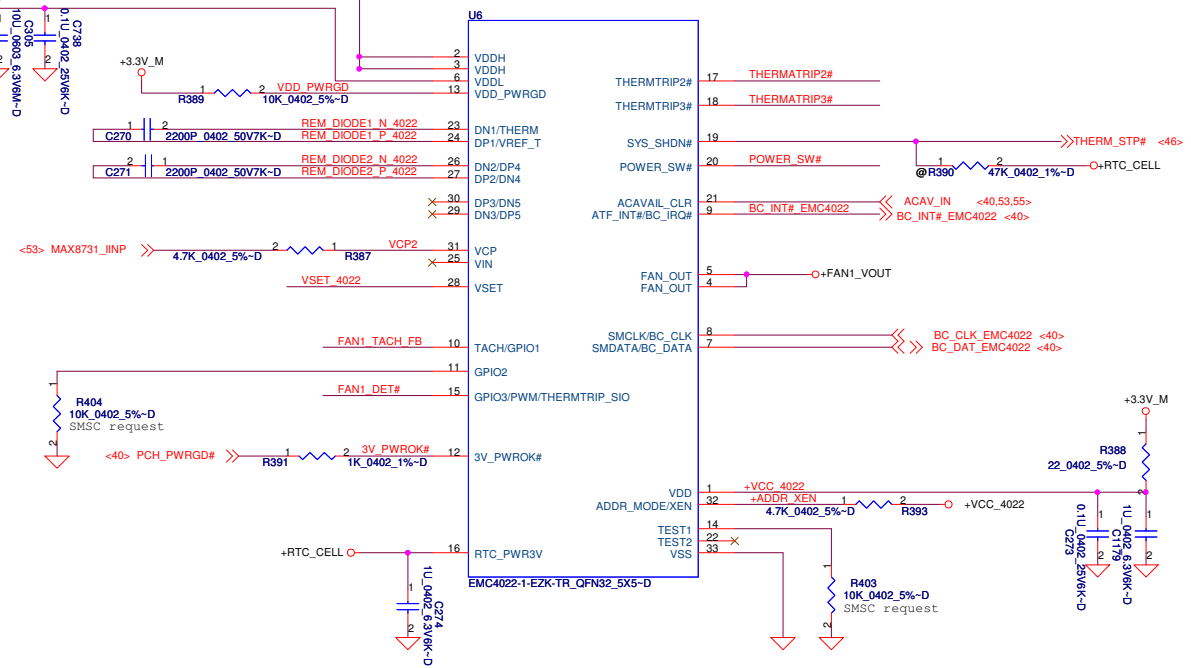
Place under CPU
Place C266 close to the Q12 as possible



(1) DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
(2) DP5/DN5 for Skin on Q13, place Q13 close to Vcore VR choke.



Change to EMC4021 for cost saving

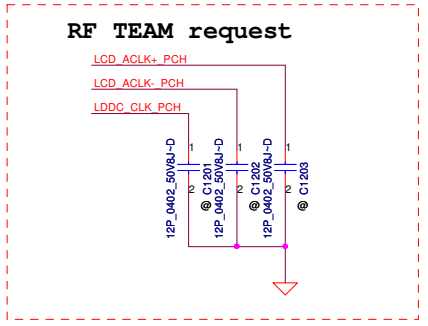
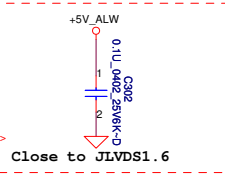
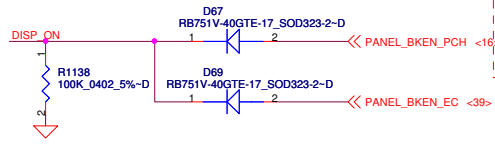
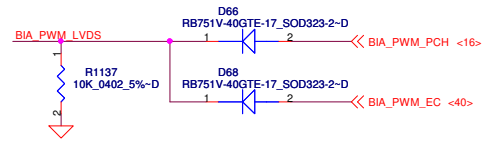
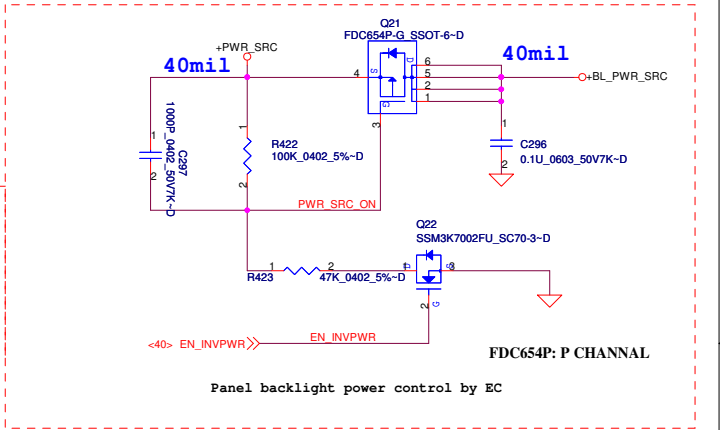
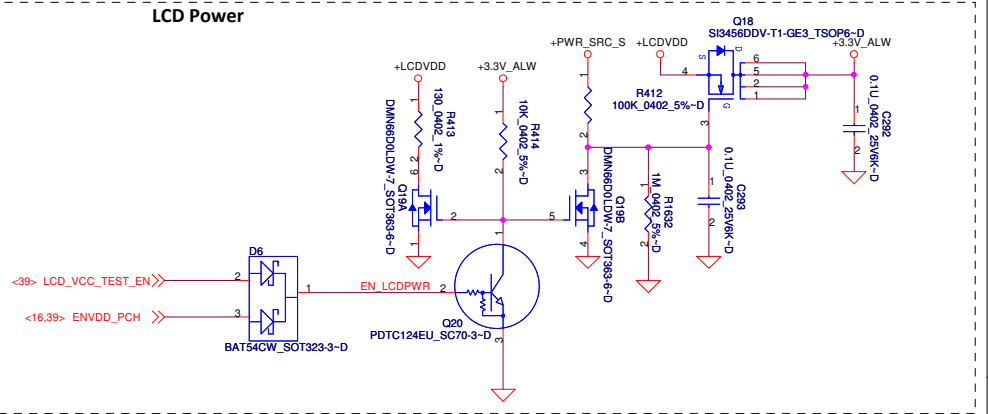
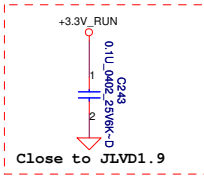
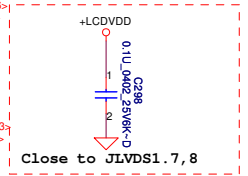
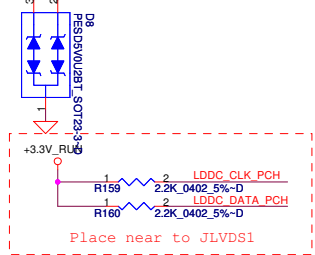
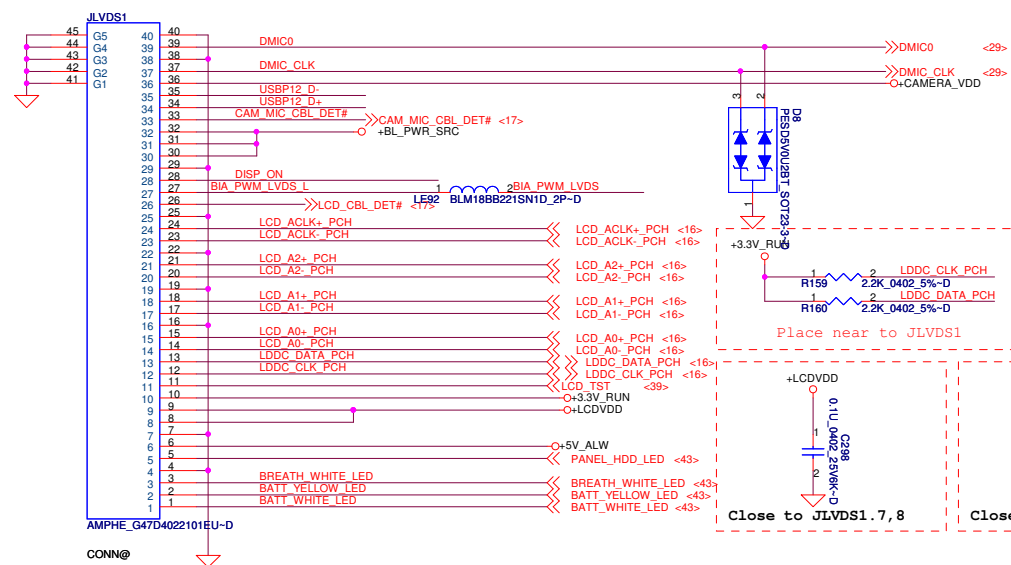


Rest=1400 Tp=94degree

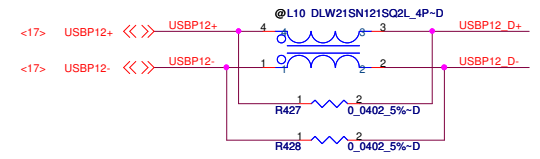
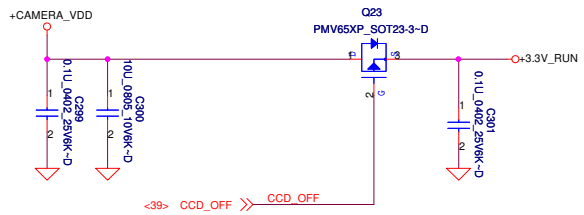
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		Compal Electronics, Inc.	
		FAN & Thermal Sensor	
Size	Document Number	Rev	
	LA-7741	0.1	
Date:	Thursday, June 23, 2011	Sheet	22 of 56

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For Webcam

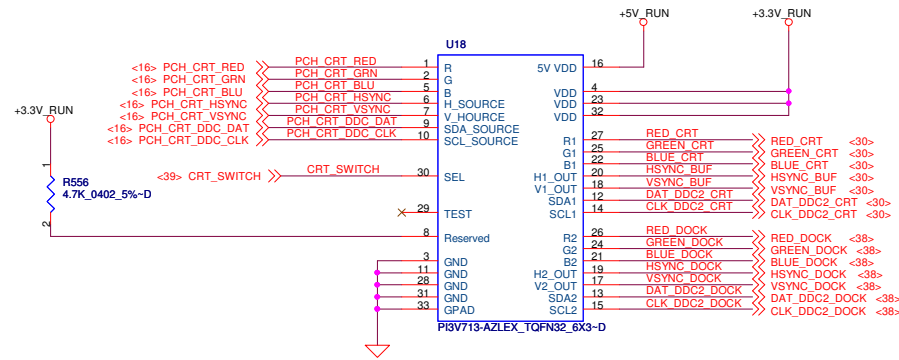


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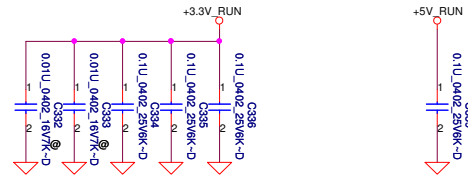
Compal Electronics, Inc.			
LVDS			
Size	Document Number	Rev	
	LA-7741	0.1	
Date:	Thursday, June 23, 2011	Sheet	23 of 56

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SW for MB/DOCK

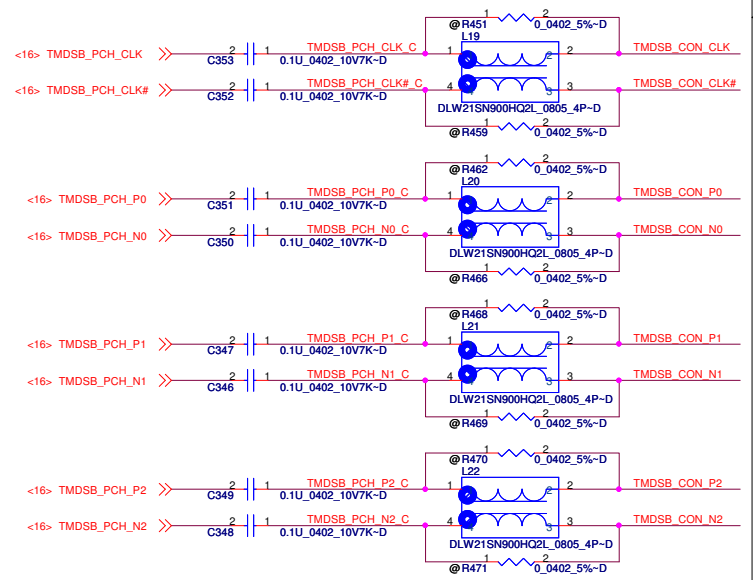
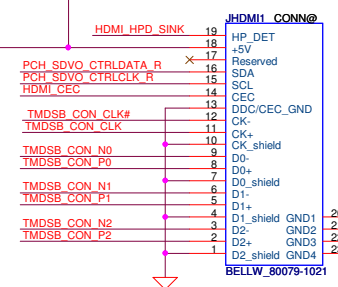
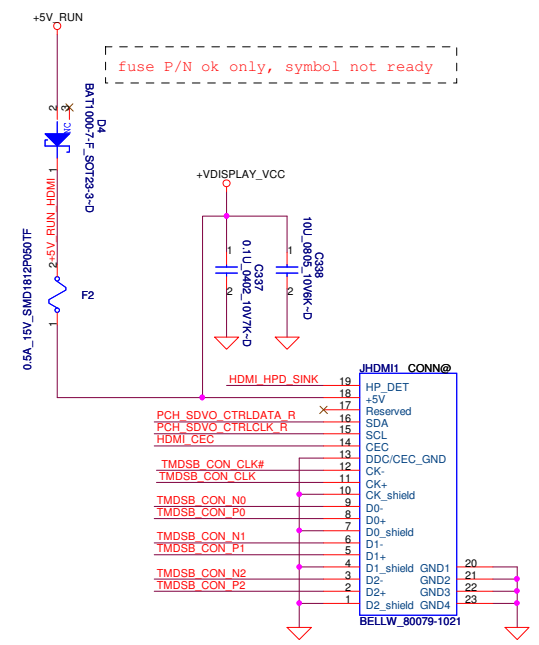
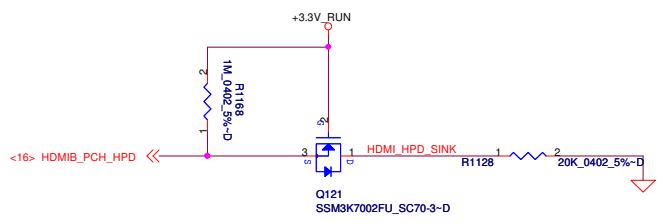
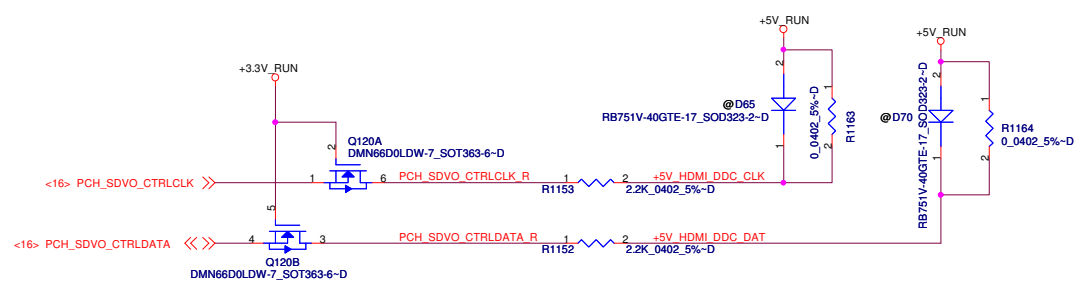
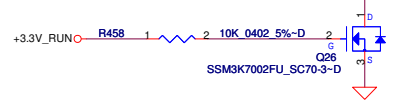
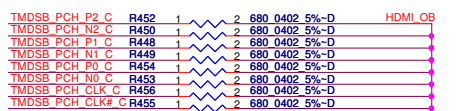
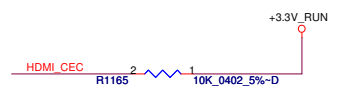


SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



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	CRT/Video switch		
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Compal Electronics, Inc.

HDMI port

LA-7741

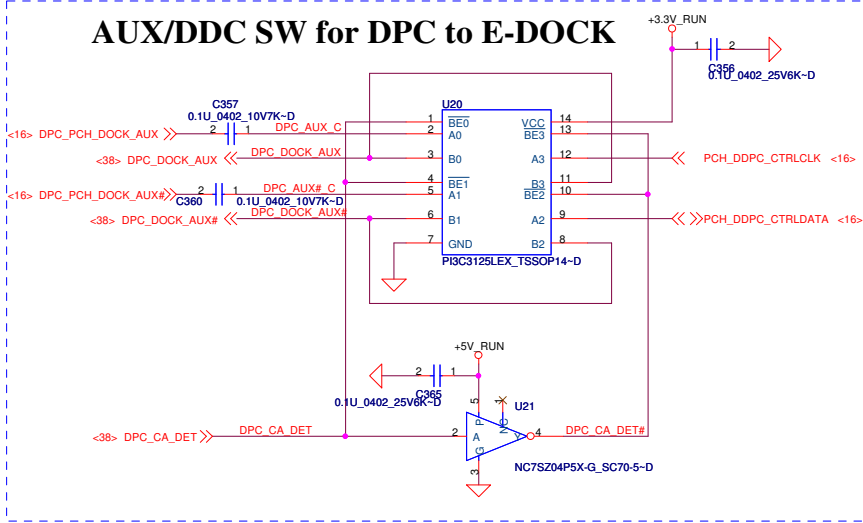
Document Number: LA-7741

Date: Thursday, June 23, 2011

Sheet: 25 of 56

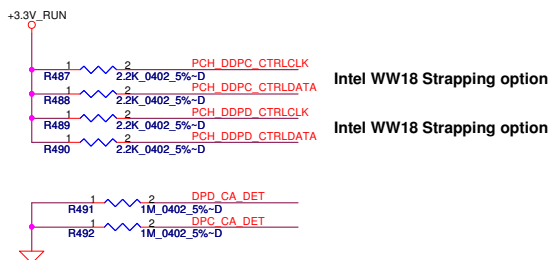
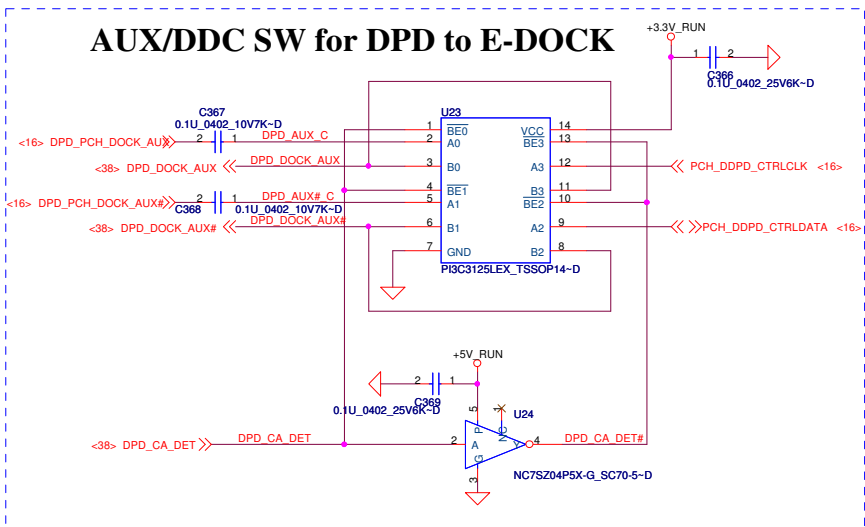
Rev: 0.1

AUX/DDC SW for DPC to E-DOCK



There is a new die for PI3C3125. Sample available on May.

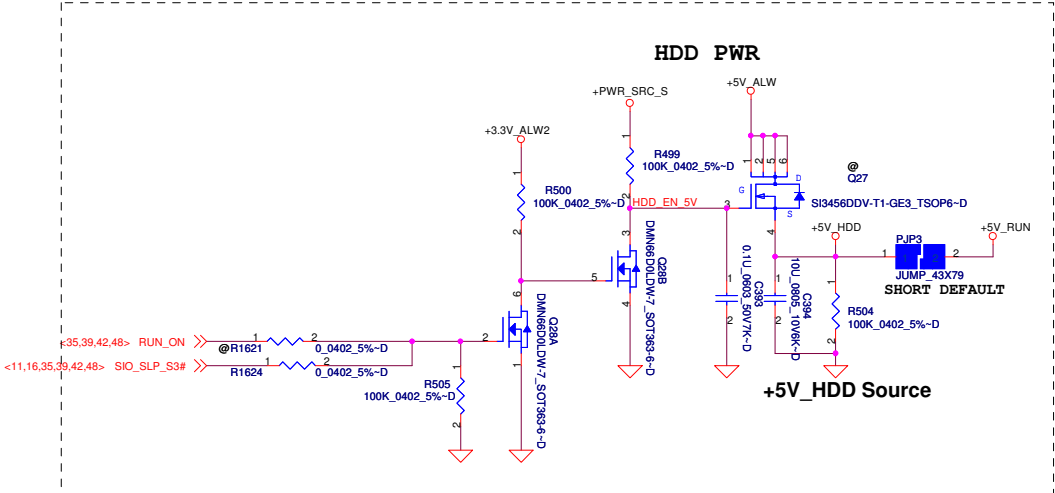
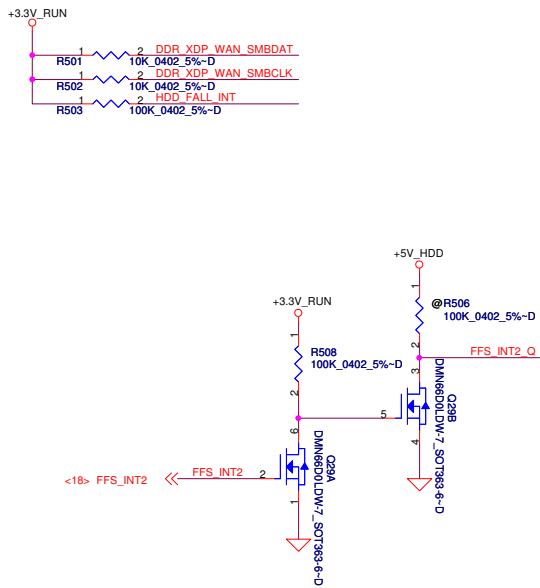
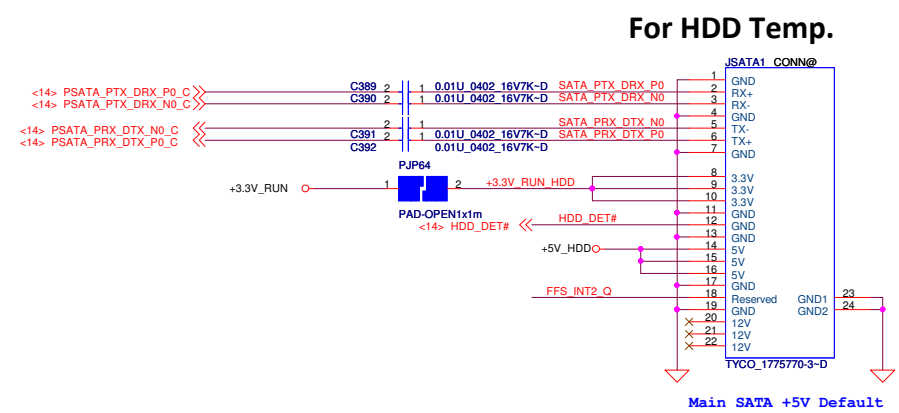
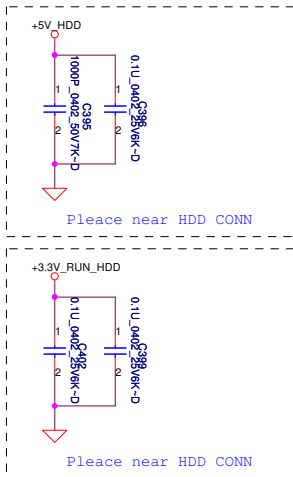
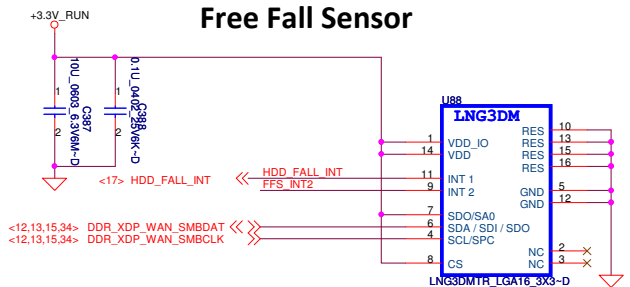
AUX/DDC SW for DPD to E-DOCK



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Title DP125			
Size	Document Number	Rev 0.1	
Date: Thursday, June 23, 2011		Sheet 26 of 56	



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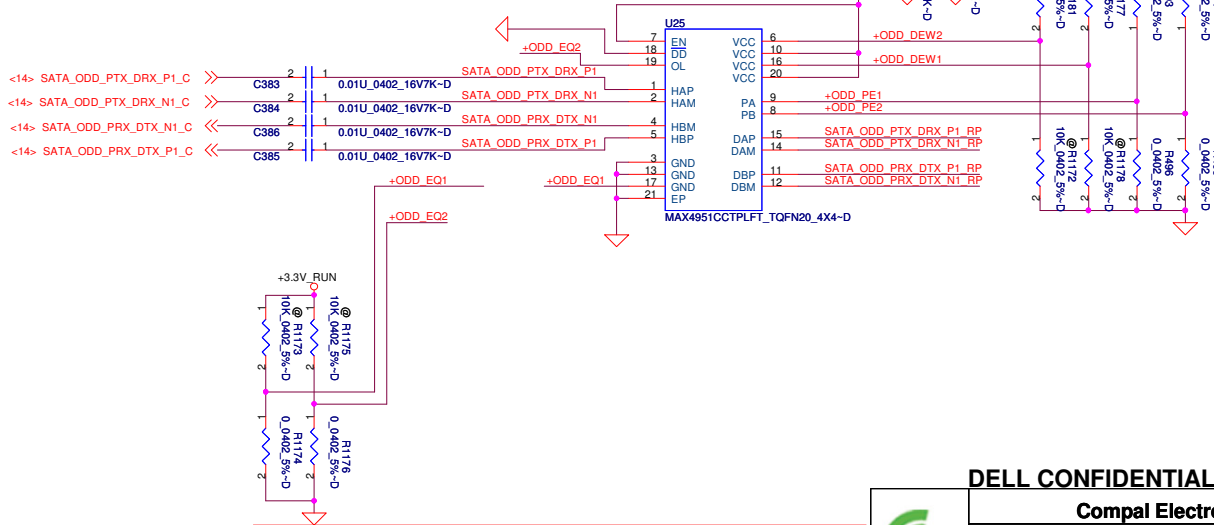
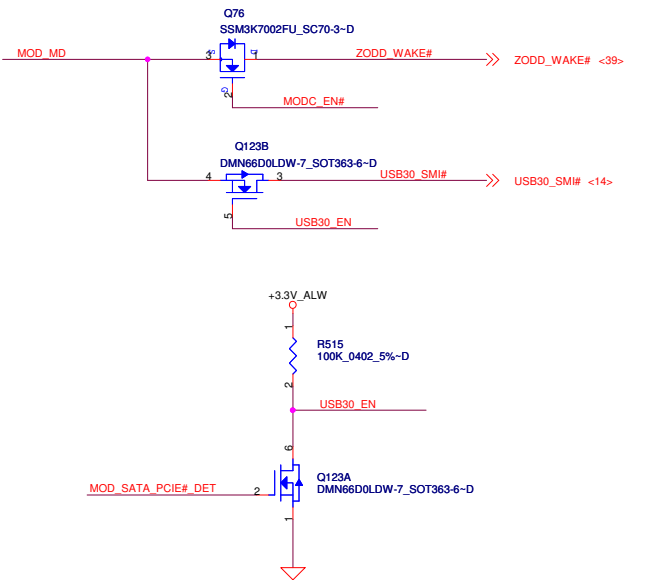
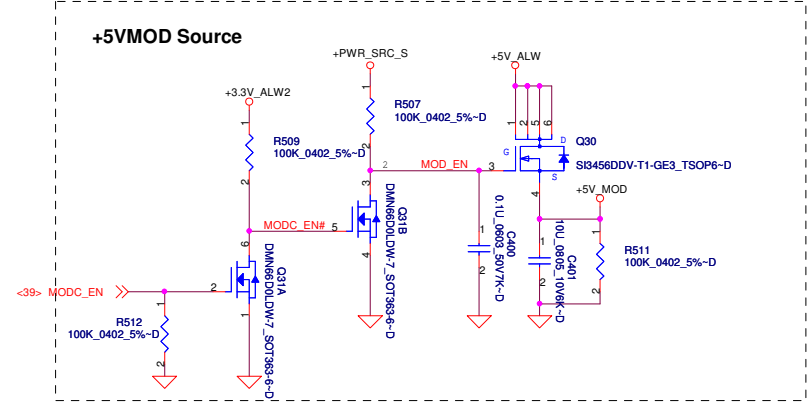
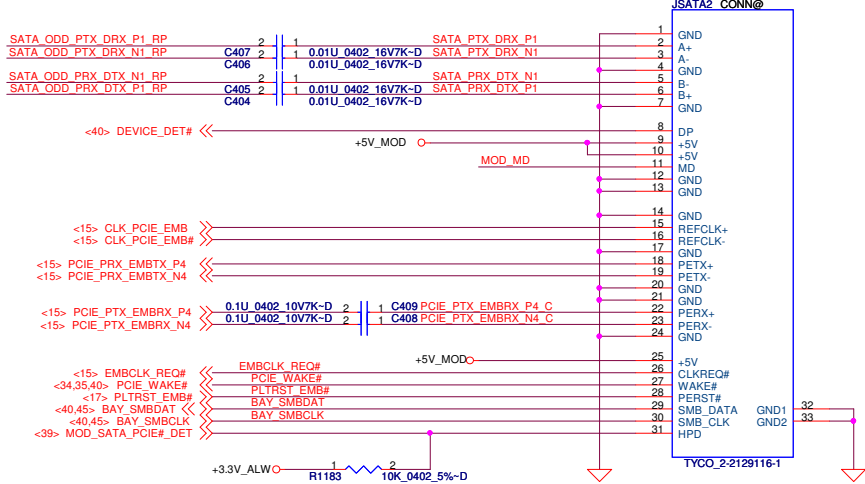
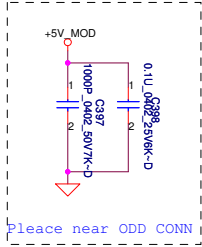
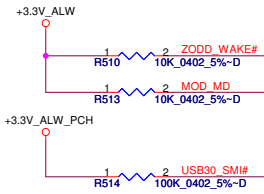
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Size: Document Number **LA-7741** Rev: 0.1

Date: Thursday, June 23, 2011 Sheet: 27 of 56

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For ODD



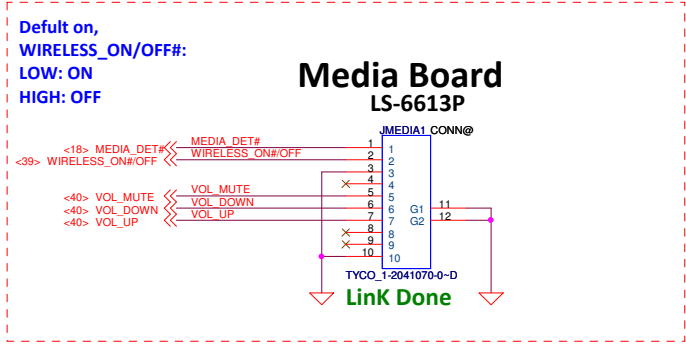
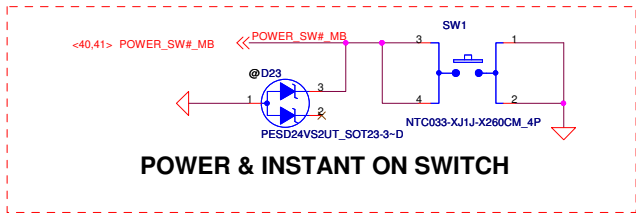
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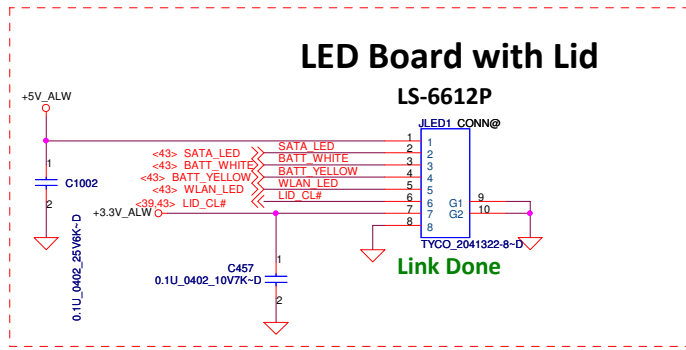
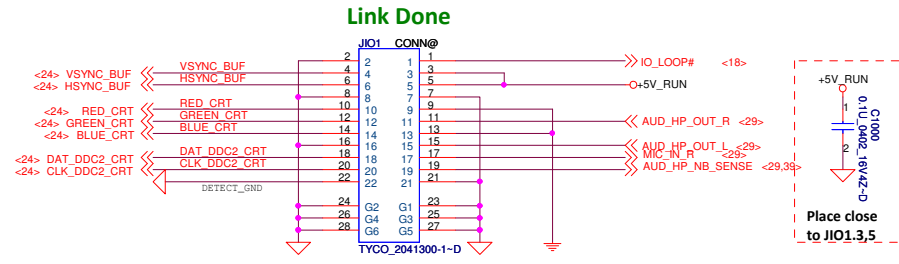
ODD CONNECTOR

LA-7741

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I/O board CONN.



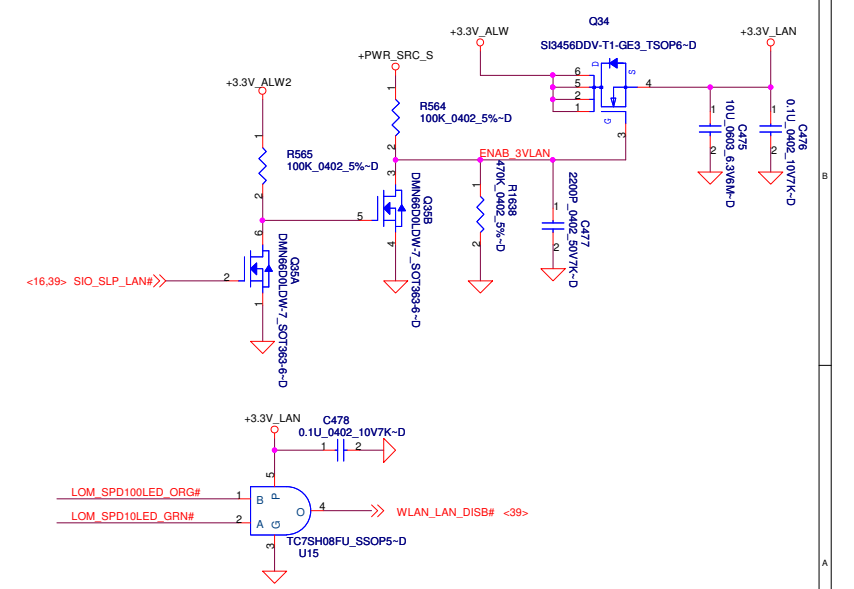
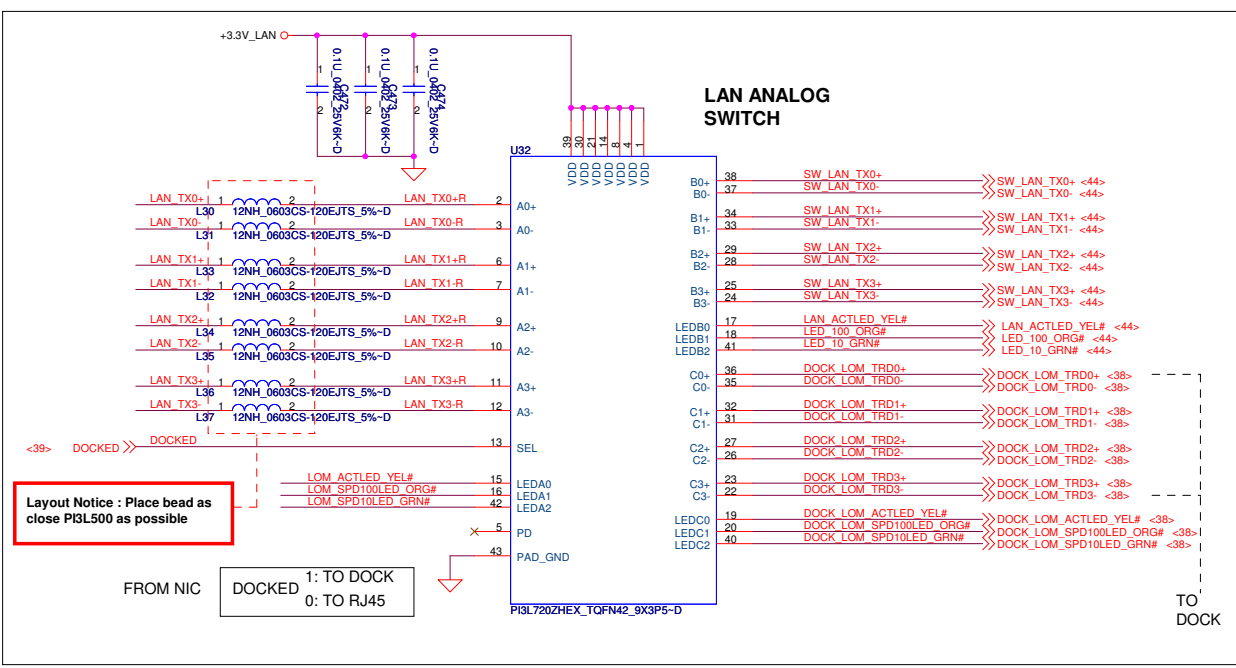
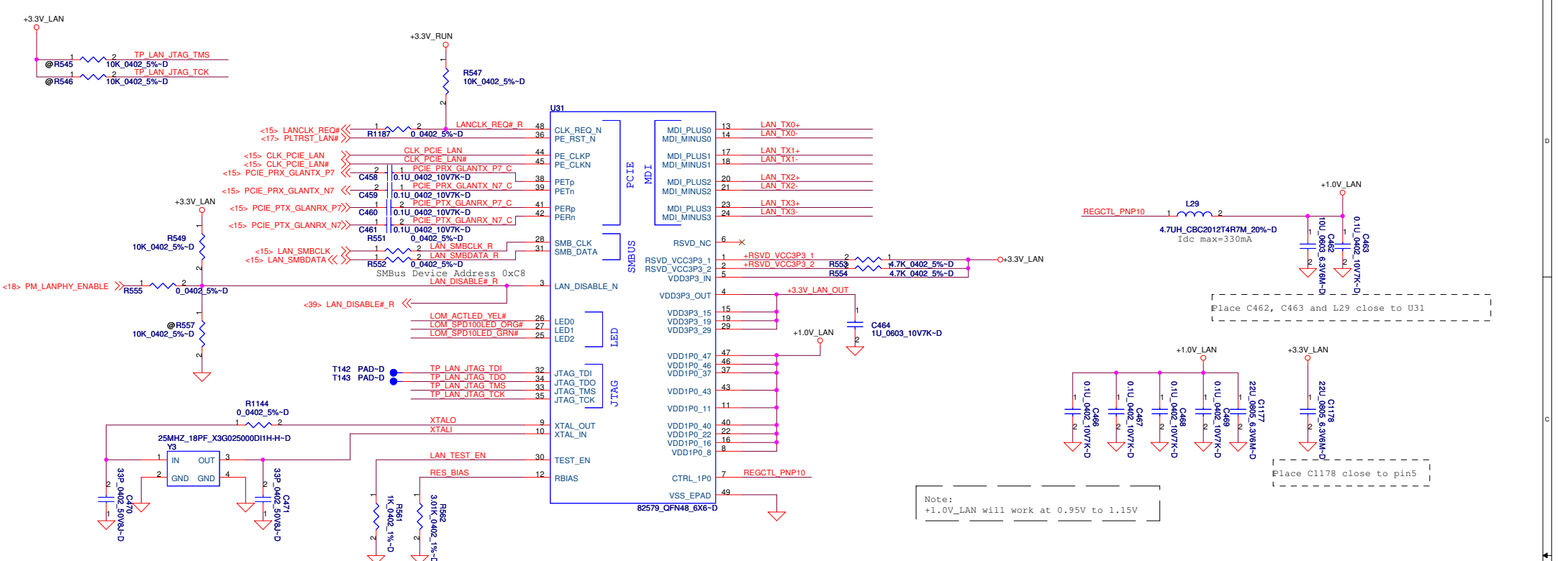
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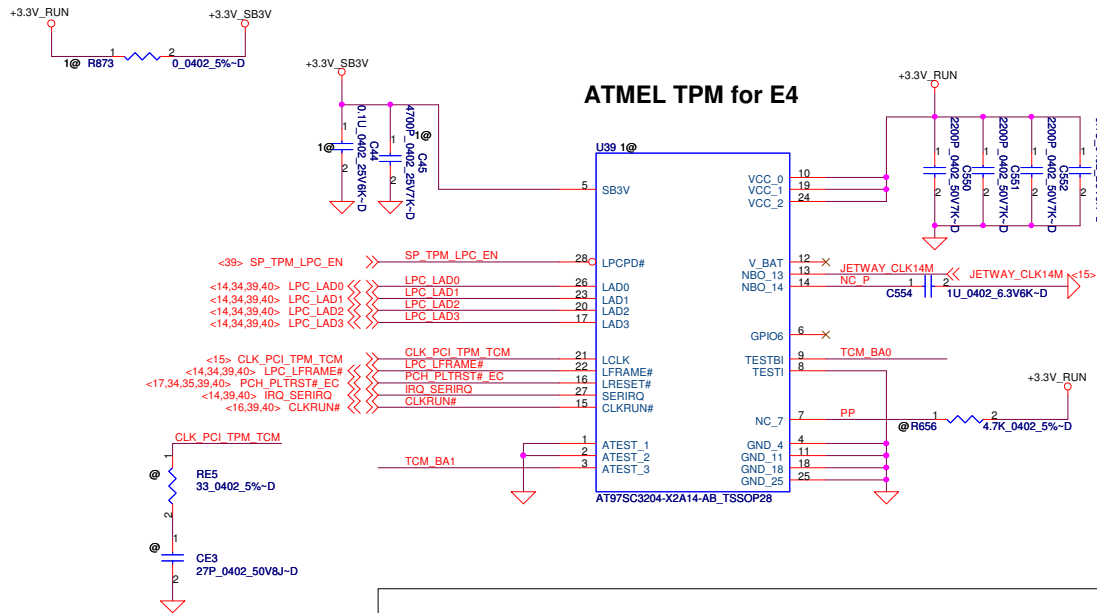
Compal Electronics, Inc.



Title	PWR SW/Sub-board Connector		
Size	Document Number	LA-7741	Rev 0.1
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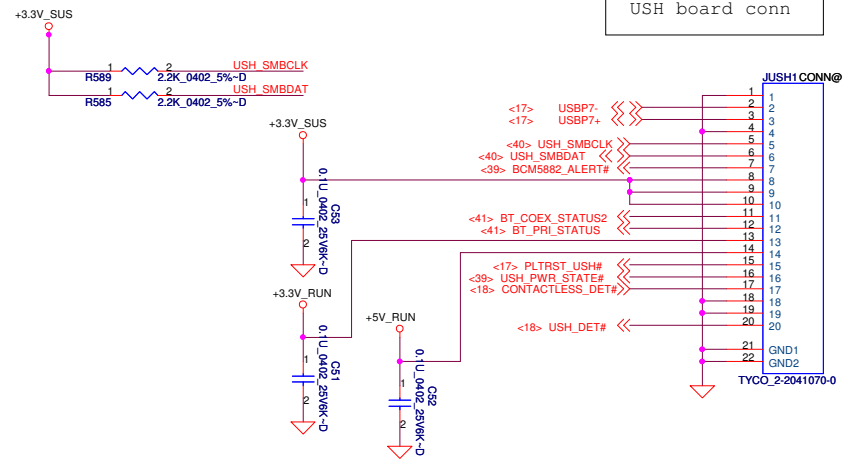
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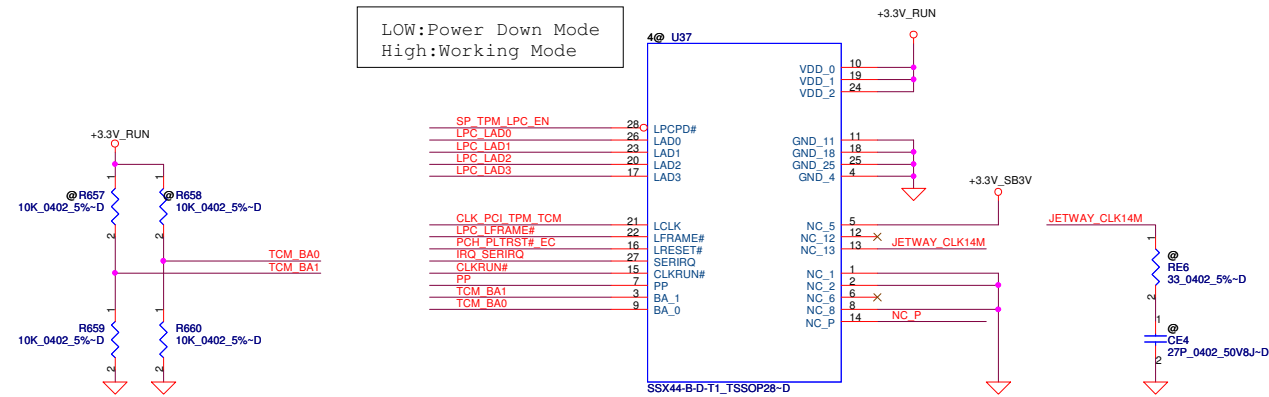
ATMEL TPM for E4

Co-lay U37 and U39
LPC layout: Place TCM first and then end LPC with TPM.



China TCM: NationZ & Jetway co-lay

LOW:Power Down Mode
 High:Working Mode



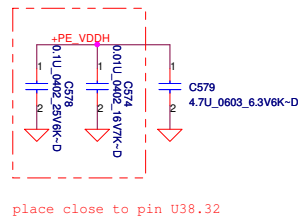
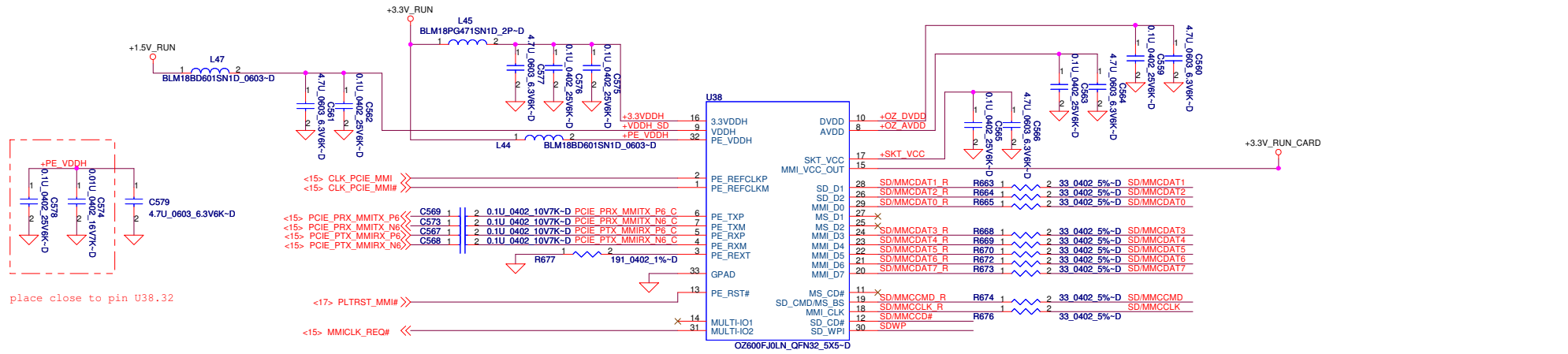
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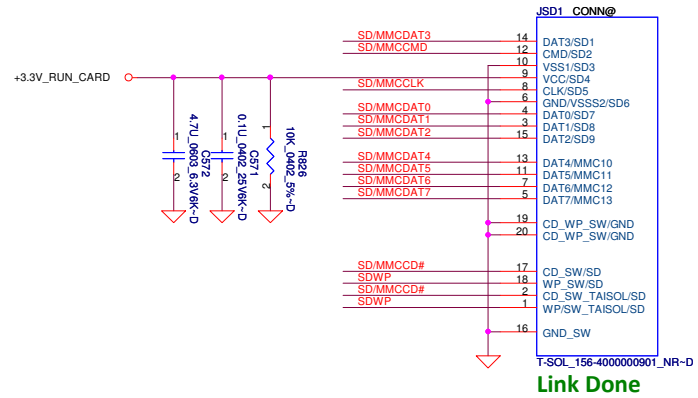
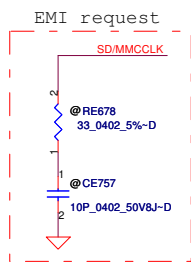


Title			TPM/TCM		
Size	Document Number	Rev			0.1
Date: Thursday, June 23, 2011			Sheet	32	of 56

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place close to pin U38.32



Link Done

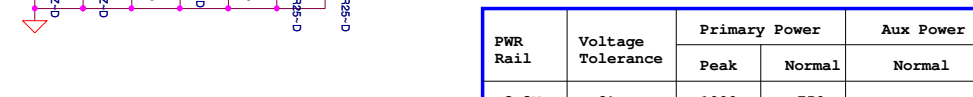
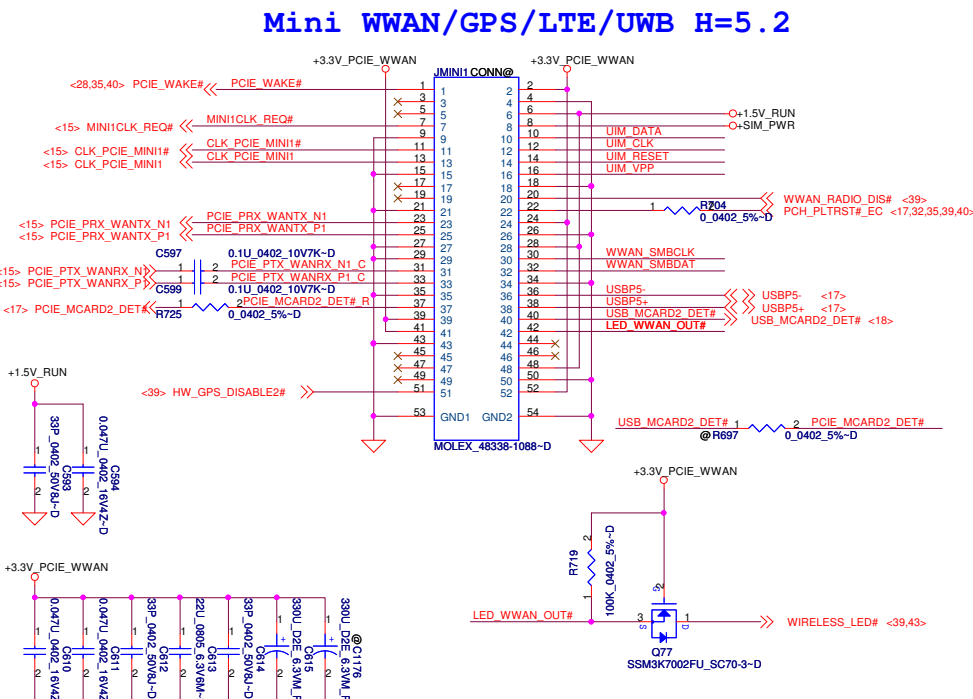
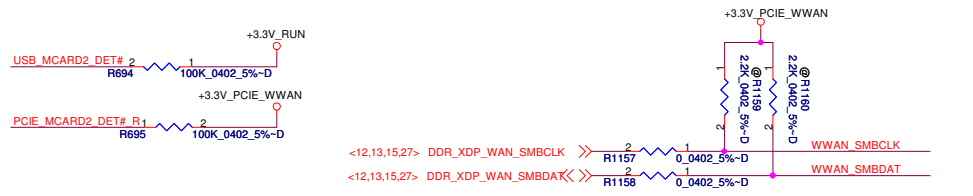
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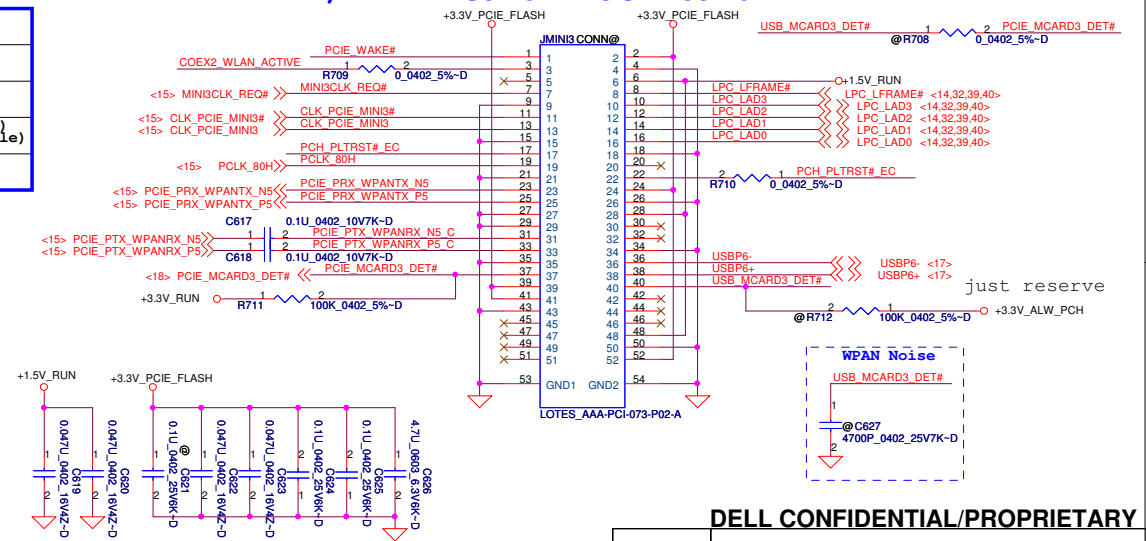
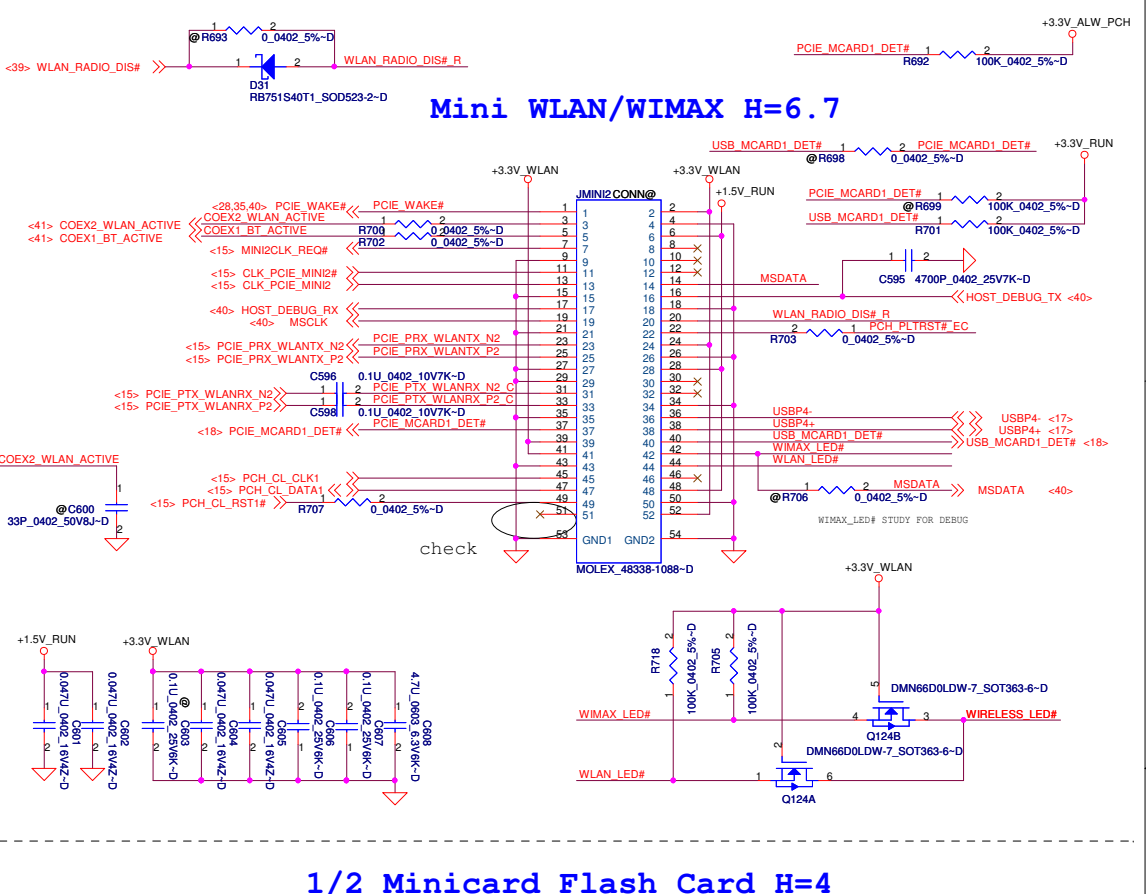


Title			
Card Reader			
Size	Document Number	Rev	
	LA-7741	0.1	
Date	Thursday, June 23, 2011	Sheet	33 of 56

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PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+5%	500	375	NA



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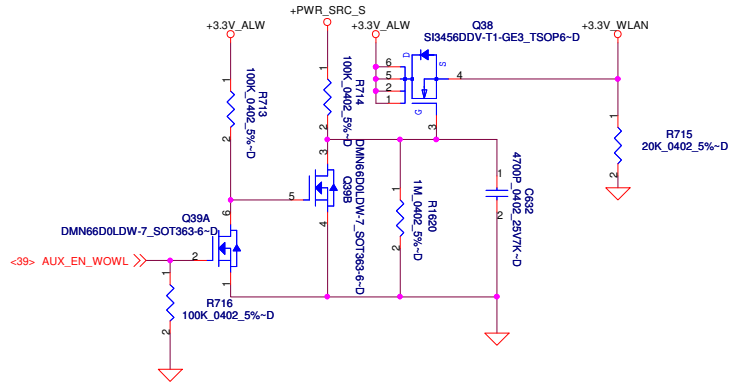
Compal Electronics, Inc.

Mini Card

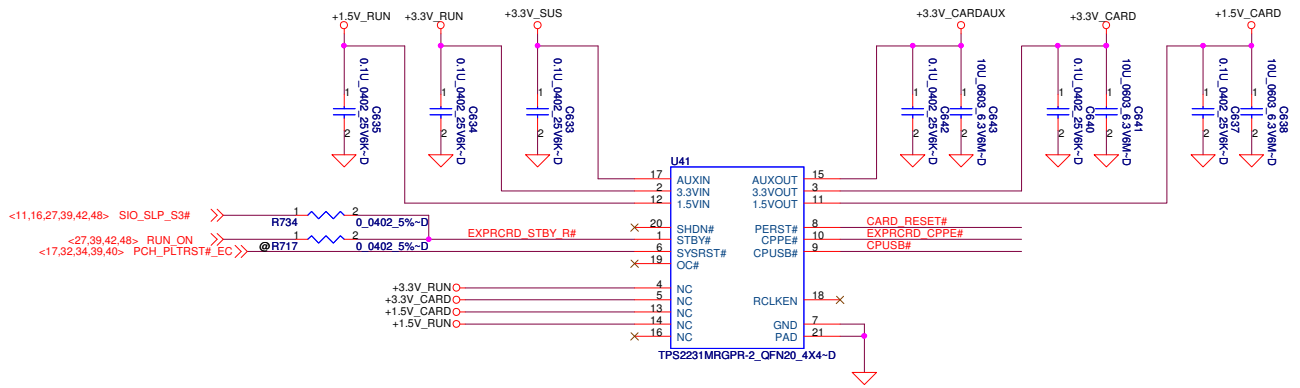
LA-7741

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Power Control for Mini card2

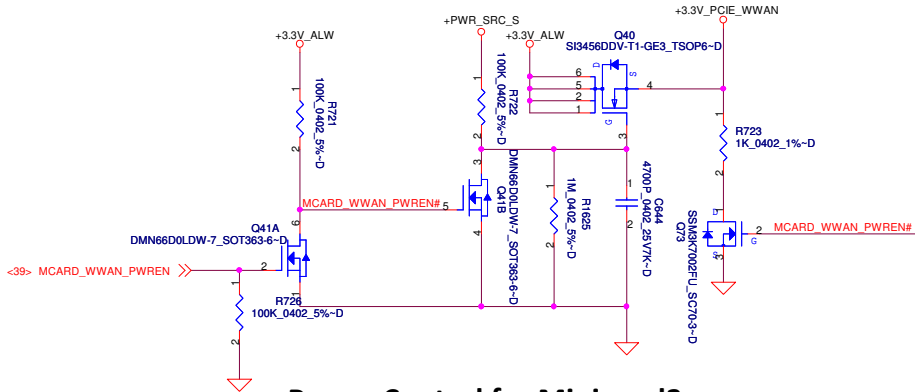


Express Card PWR S/W

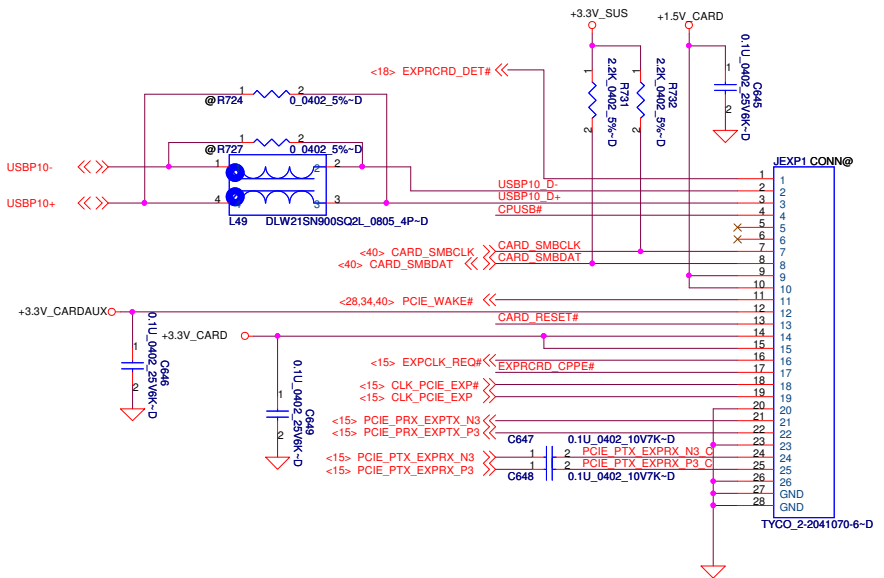


[Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part]

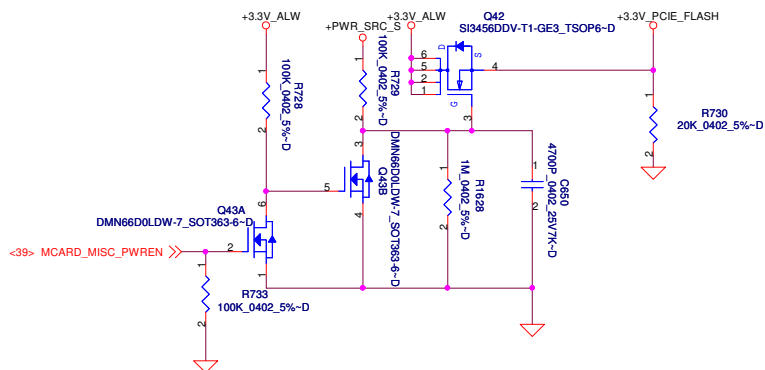
Power Control for Mini card1



Express Card Conn.



Power Control for Mini card3

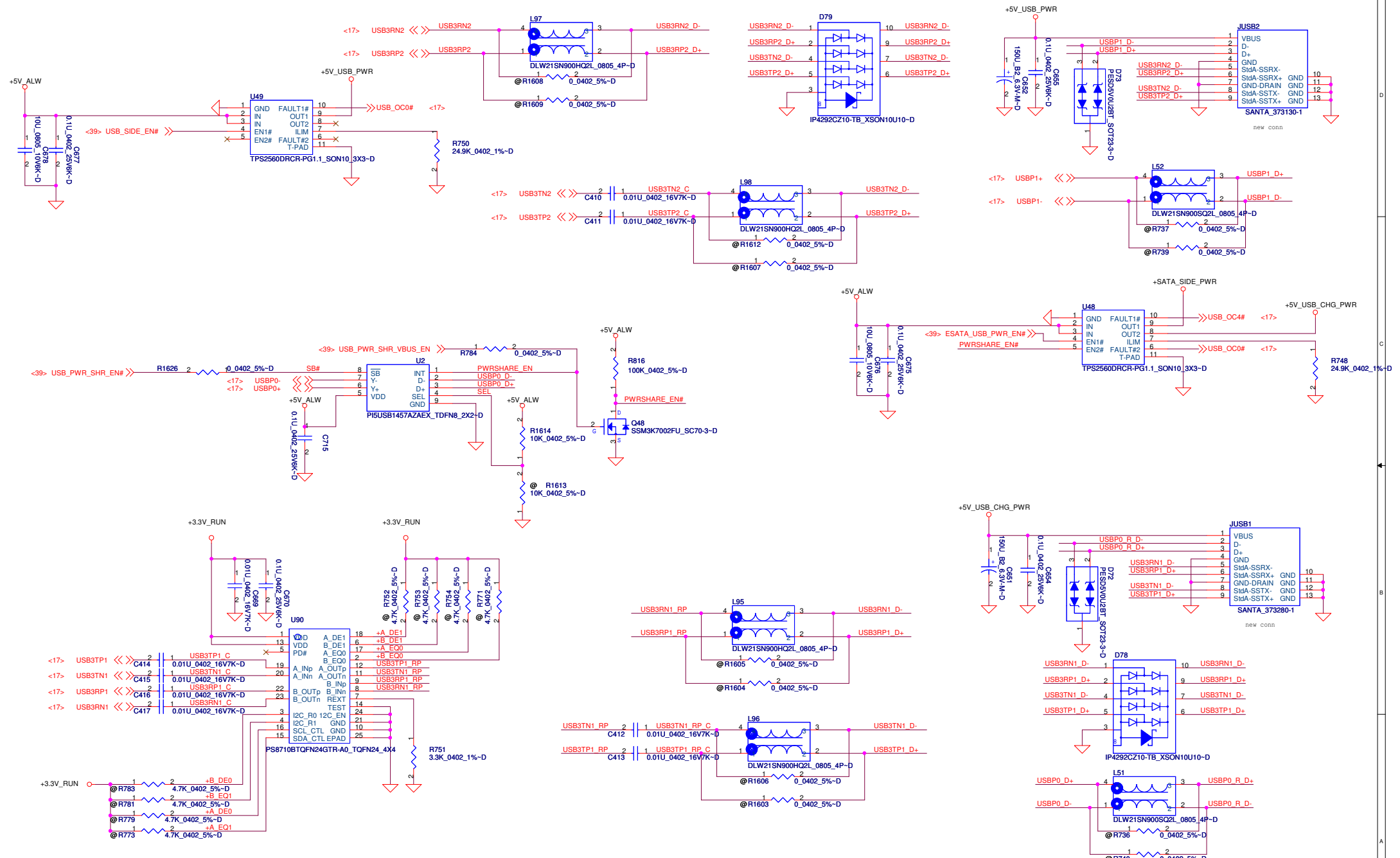


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Title			PCIE-SATA SW / PCIE PWR		
Size	Document Number	LA-7741		Rev	0.1
Date:	Thursday, June 23, 2011	Sheet	35	of	56

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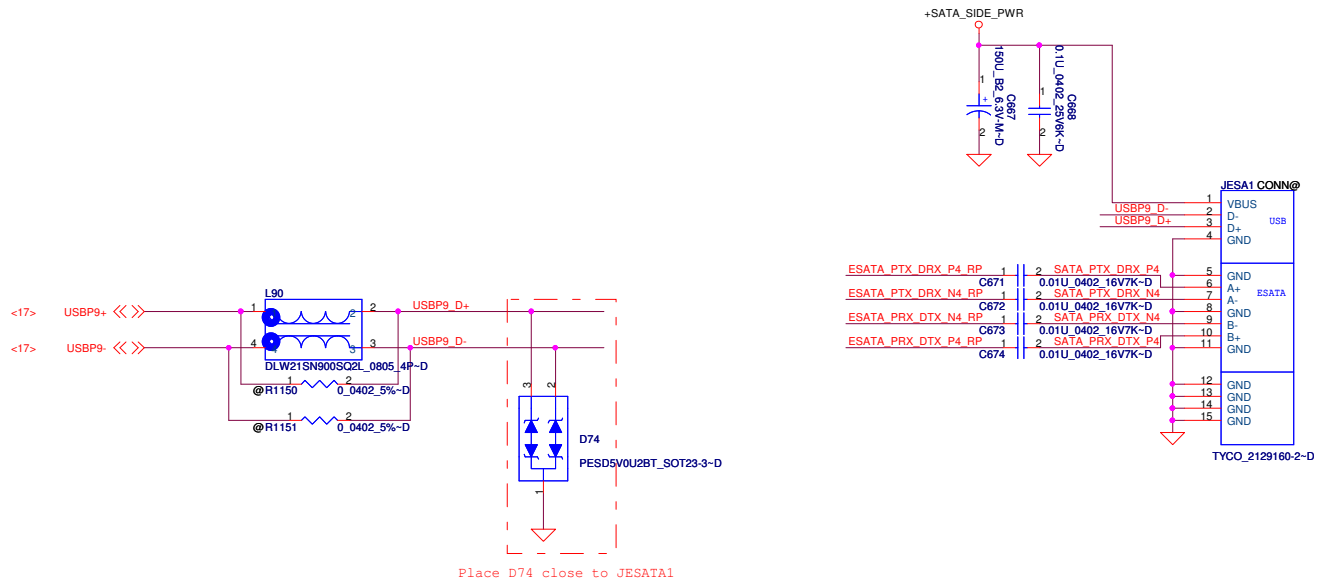
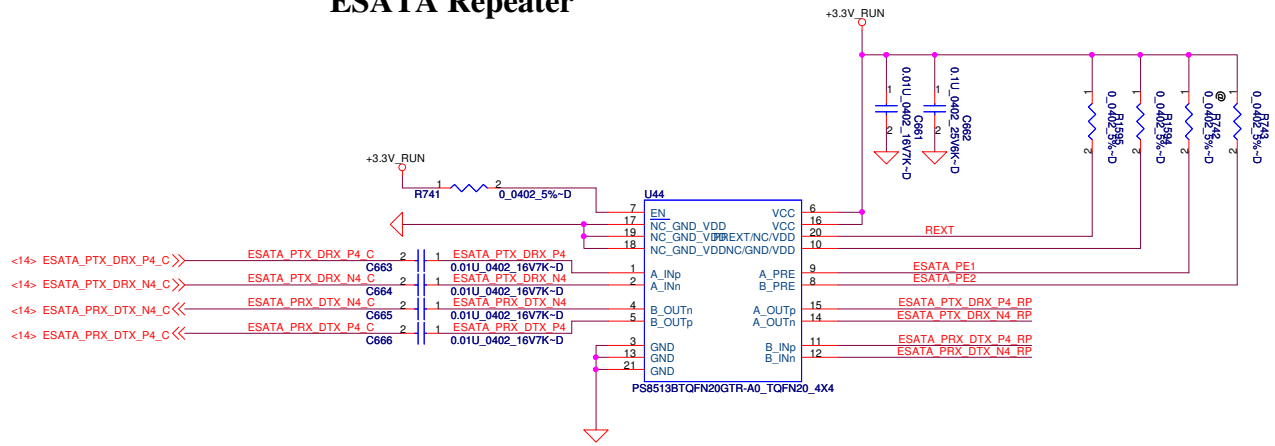


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USB 3.0 x2			
LA-7741			
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ESATA Repeater



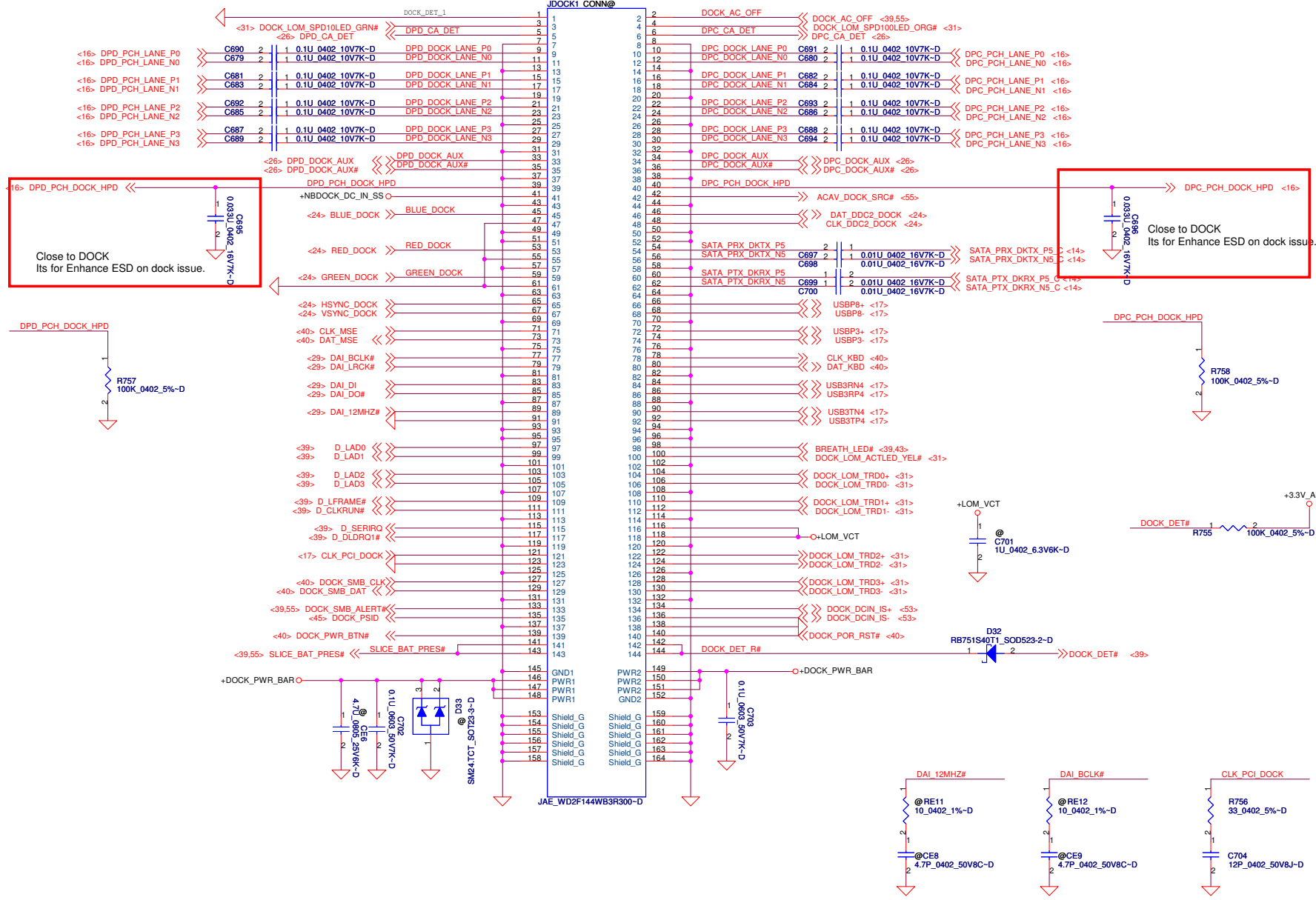
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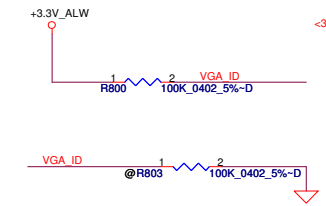
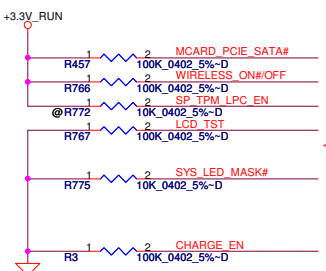
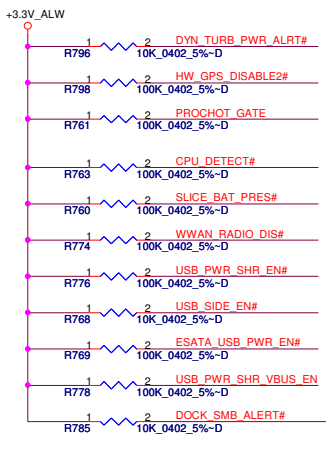
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Size	Document Number	Rev	0.1
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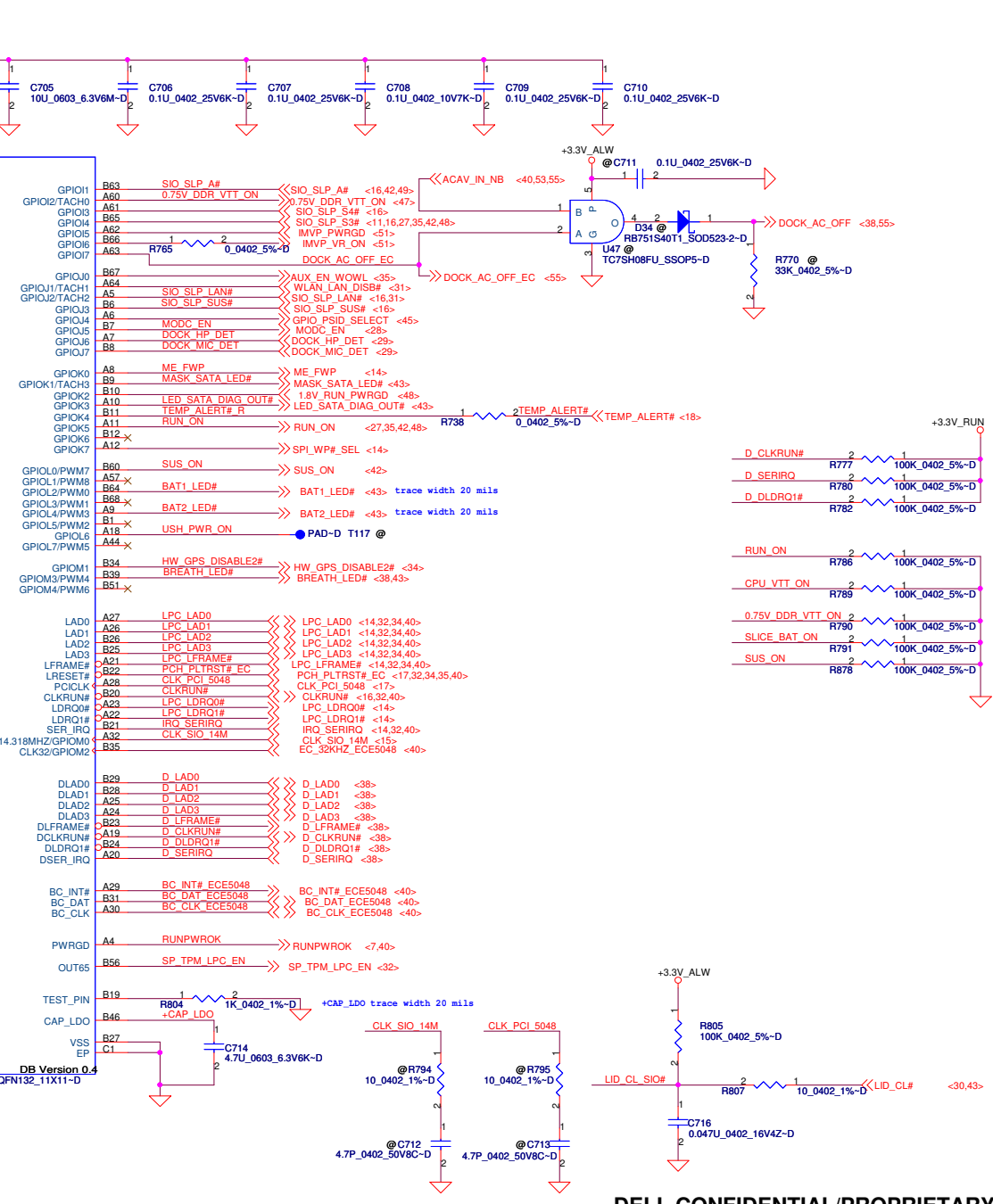
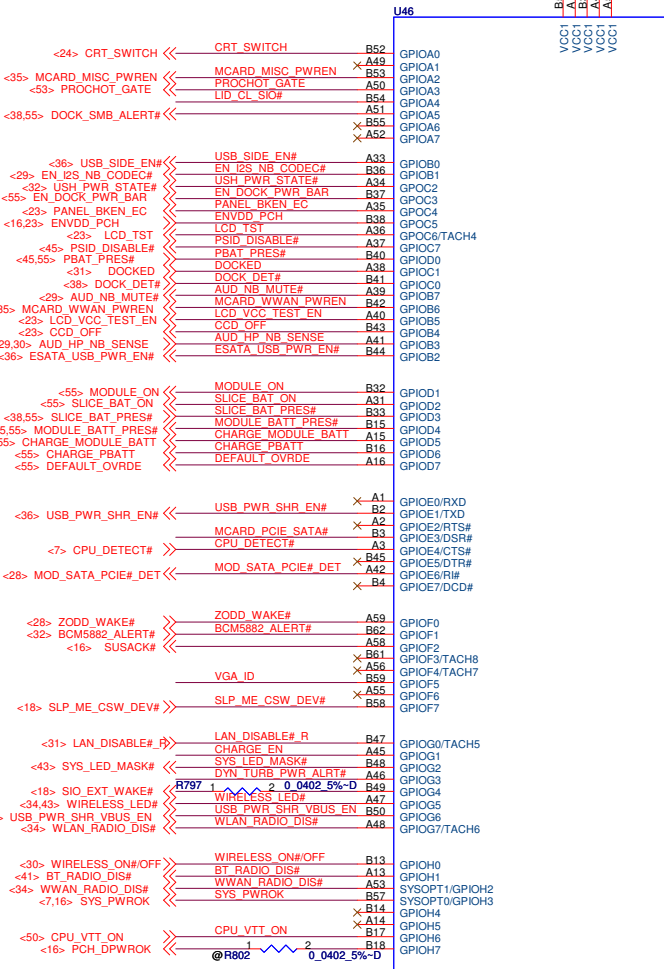
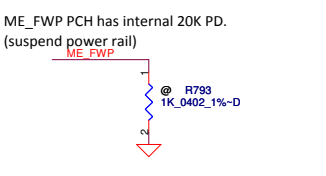


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	VGA_ID0
Discrete	0
UMA	1



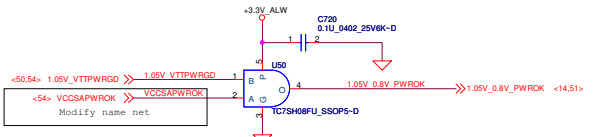
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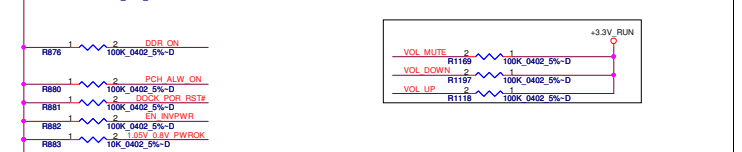
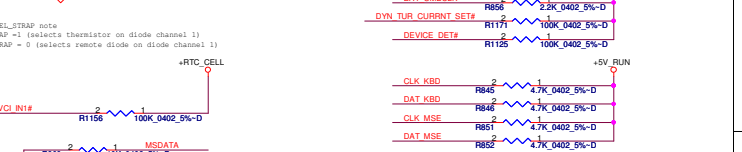
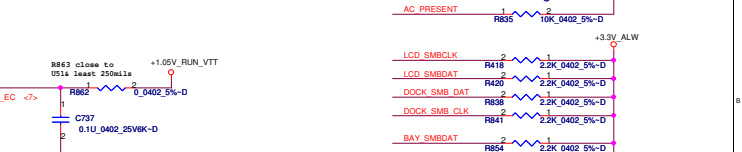
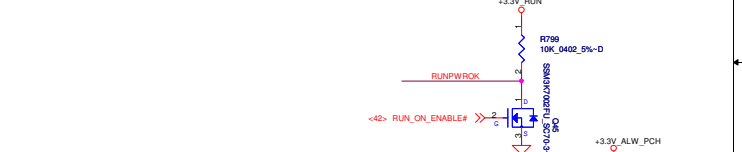
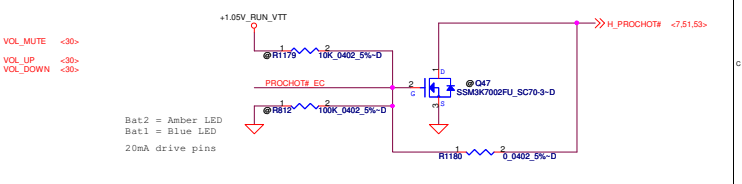
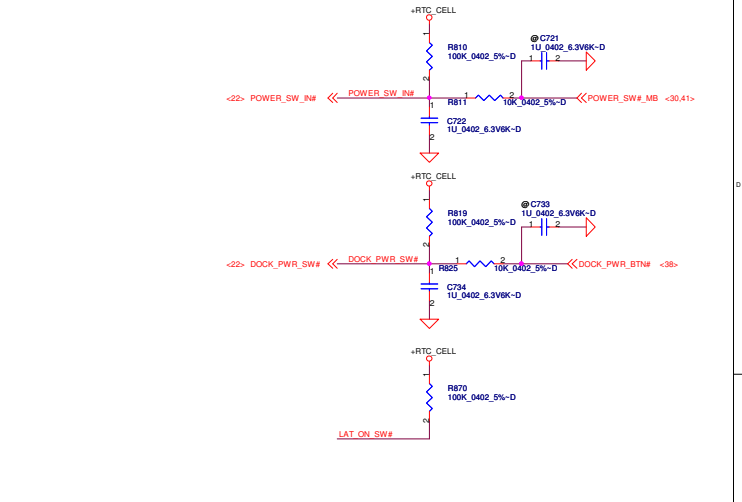
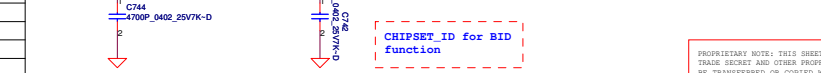
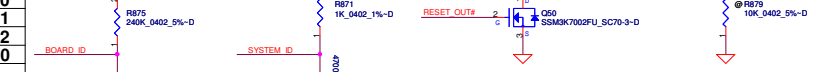
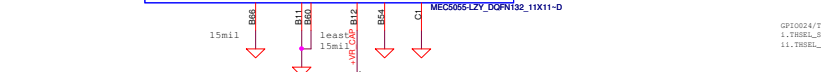
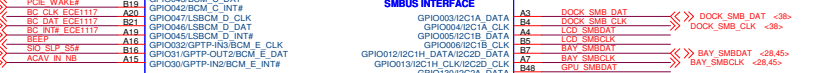
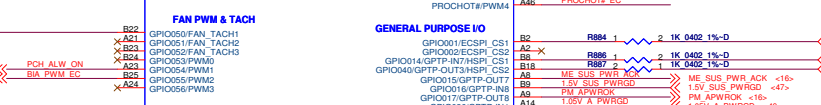
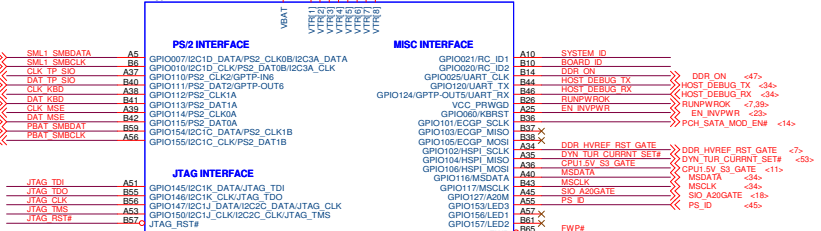
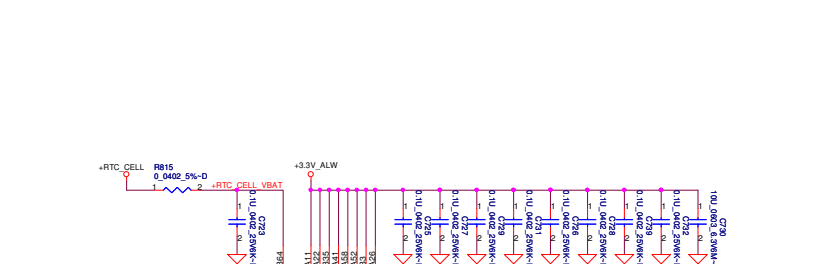
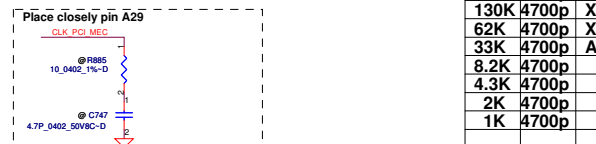
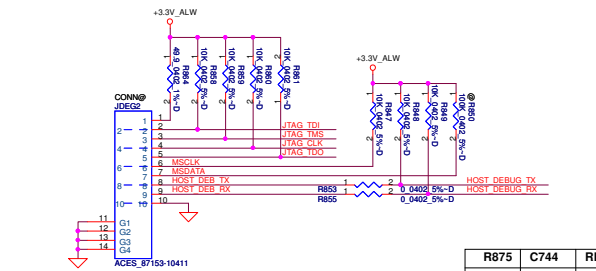
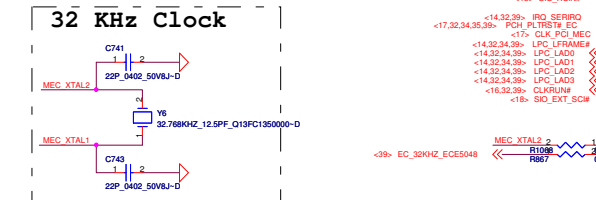
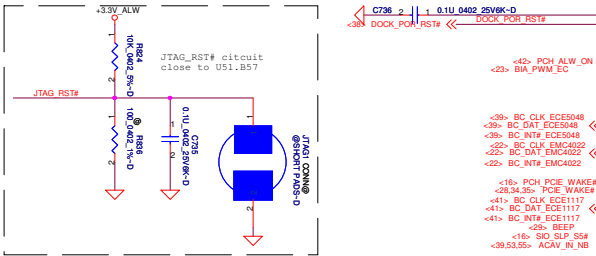


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EC firmware can configure these on-used SMBUS pins as GPIO (Output), then it's OK to leave these on-used pins No-Connect.



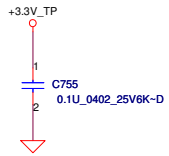
R75	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

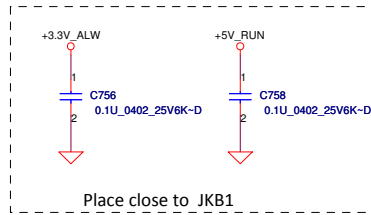
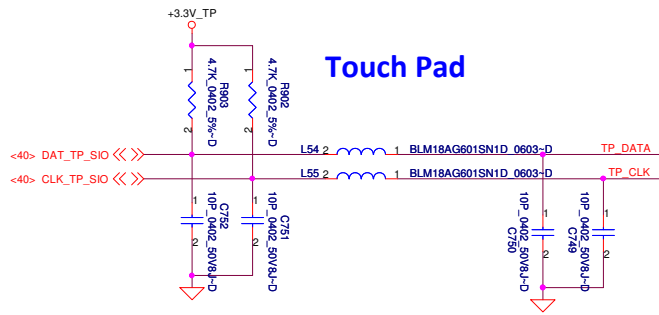
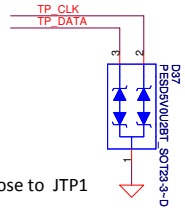
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 File: **MEC5055**
 Size: **LA-7741**
 Date: Thursday, June 23, 2011 Sheet 40 of 55

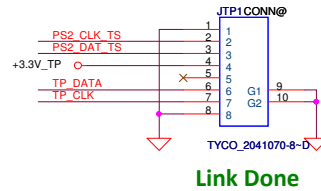
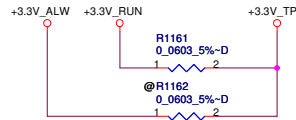
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Place close to JTP1

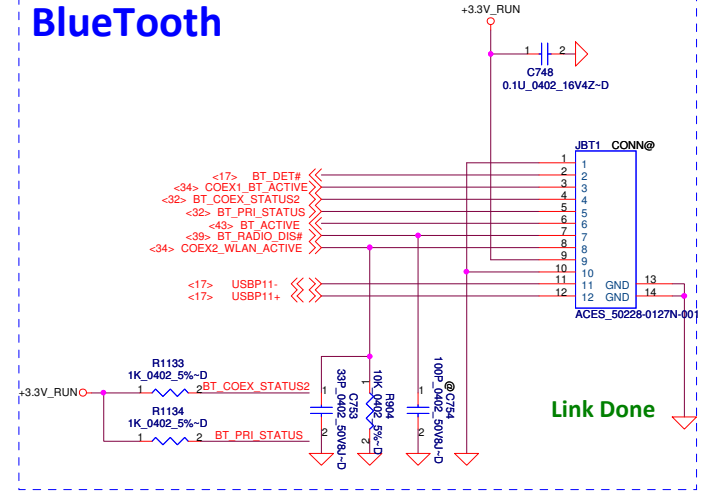


Place close to JKB1



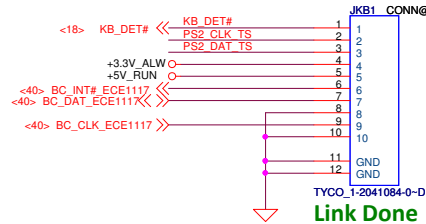
Link Done

BlueTooth



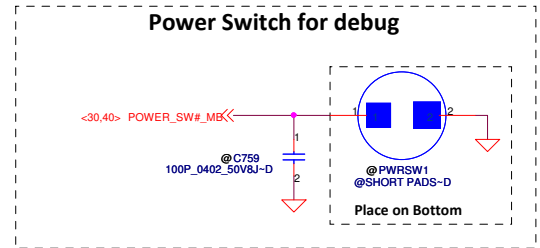
Link Done

KB Conn. Pitch=1.0mm

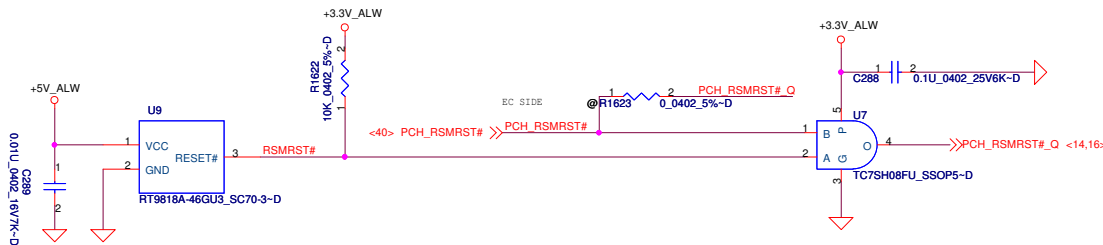


Link Done

Power Switch for debug



Place on Bottom



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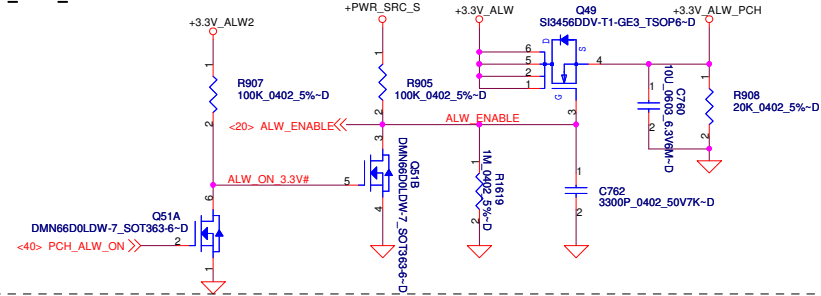
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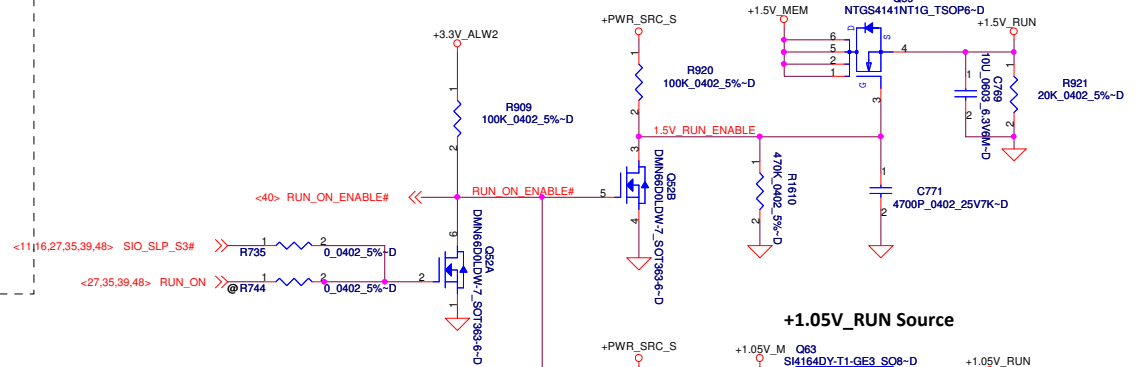
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Size			Document Number		
Date			Rev		
Thursday, June 23, 2011			0.1		
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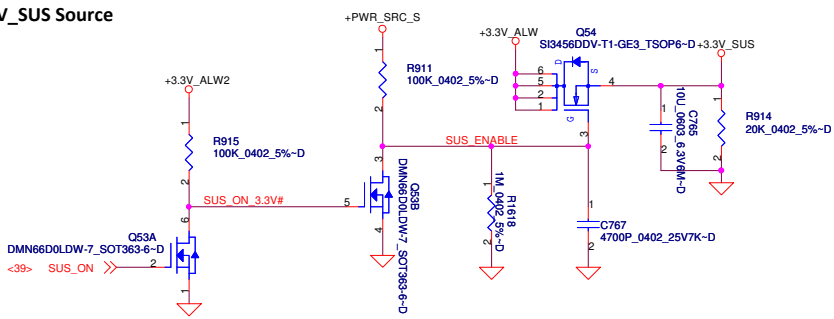
+3.3V_ALW_PCH Source



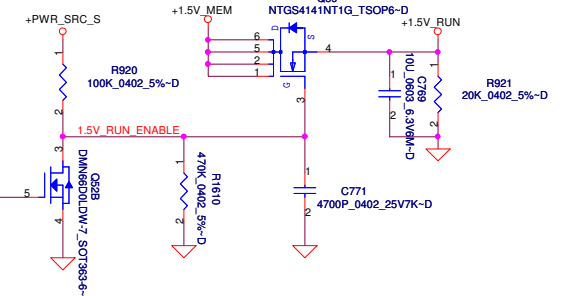
DC/DC Interface



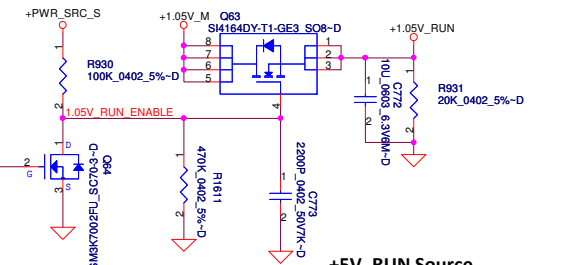
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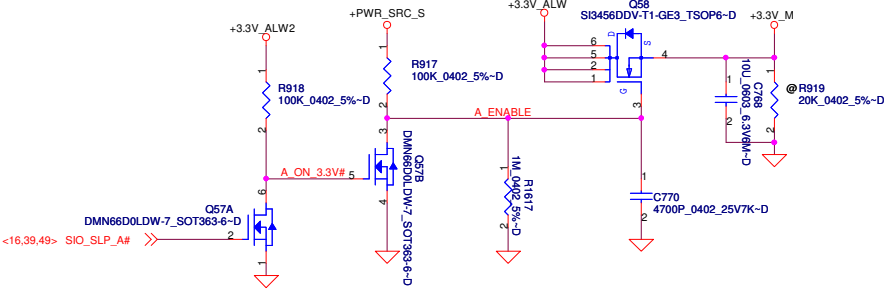
+1.5V_RUN Source



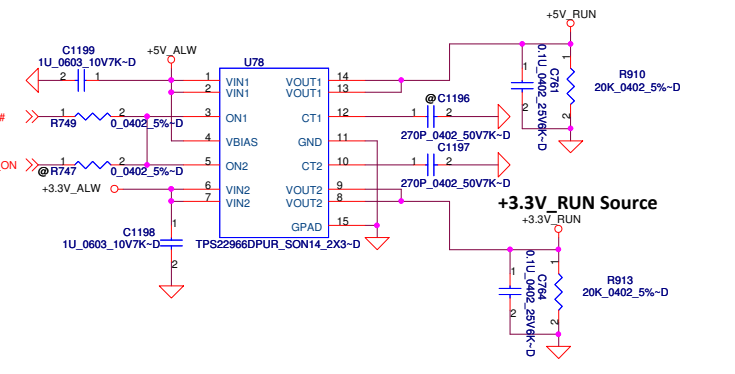
+1.05V_RUN Source



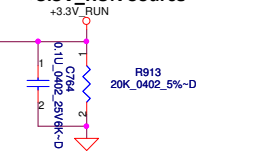
+3.3V_M Source



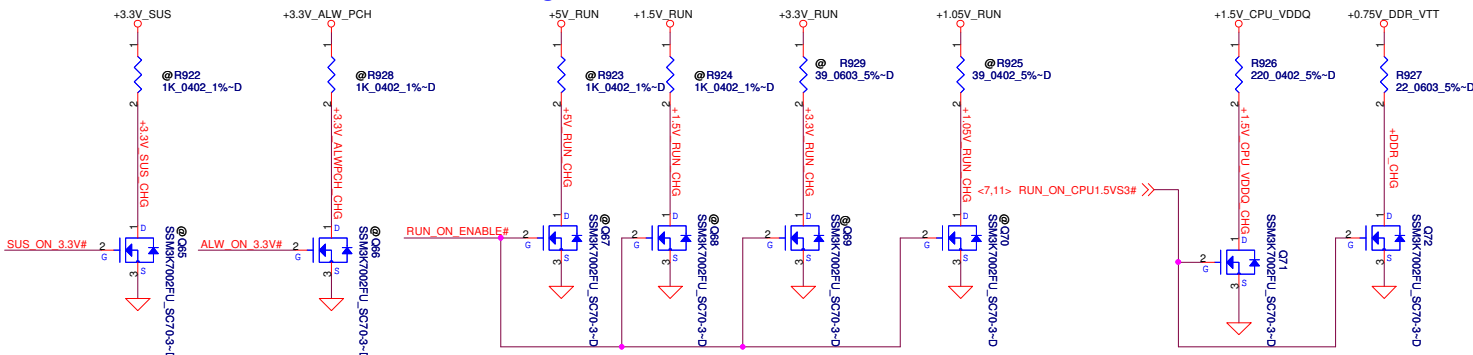
+5V_RUN Source



+3.3V_RUN Source



Discharg Circuit



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POWER CONTROL

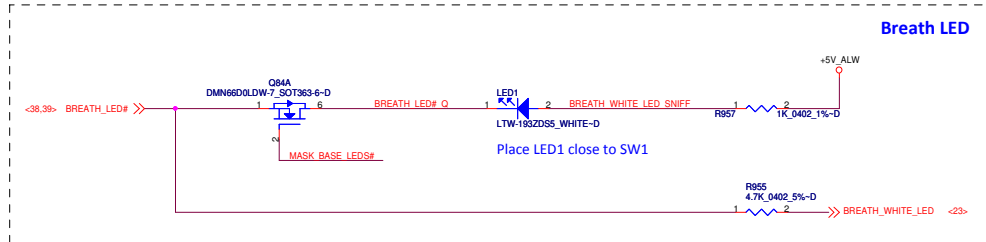
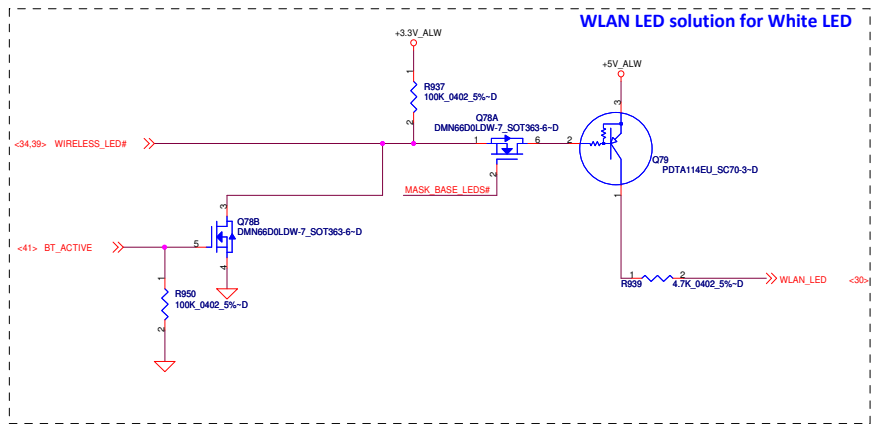
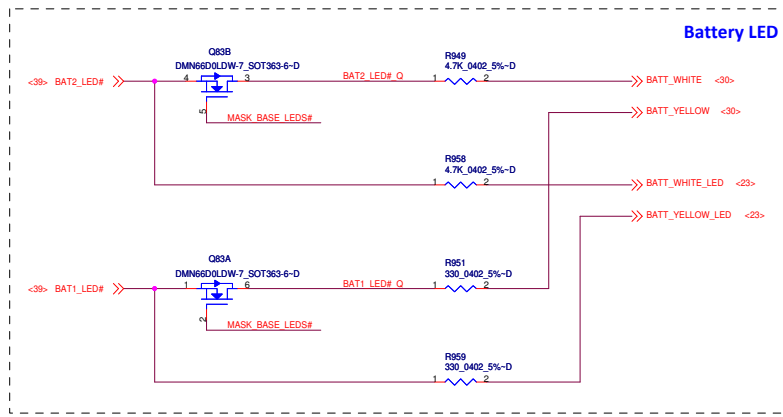
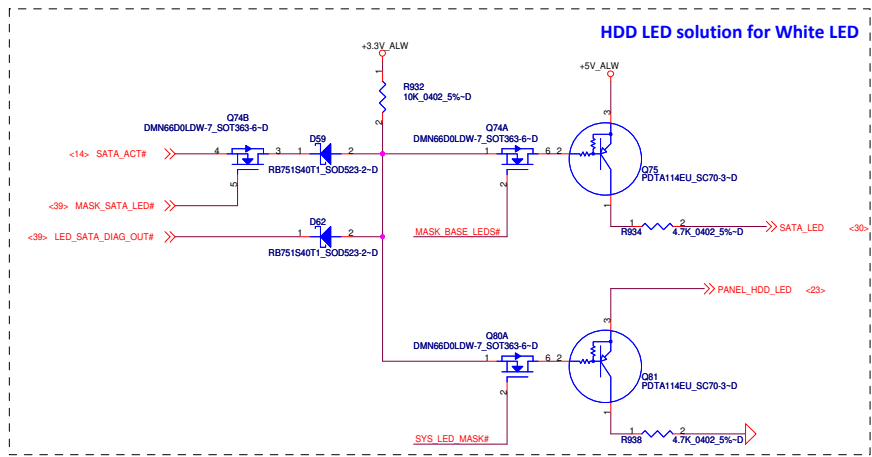
LA-7741

Rev 0.1

Thursday, June 23, 2011

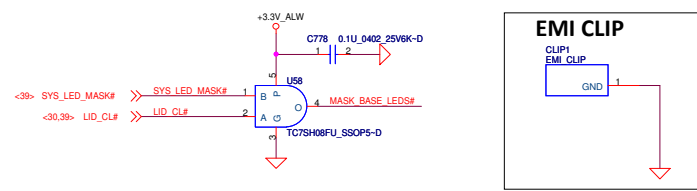
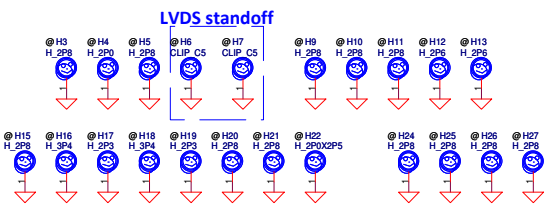
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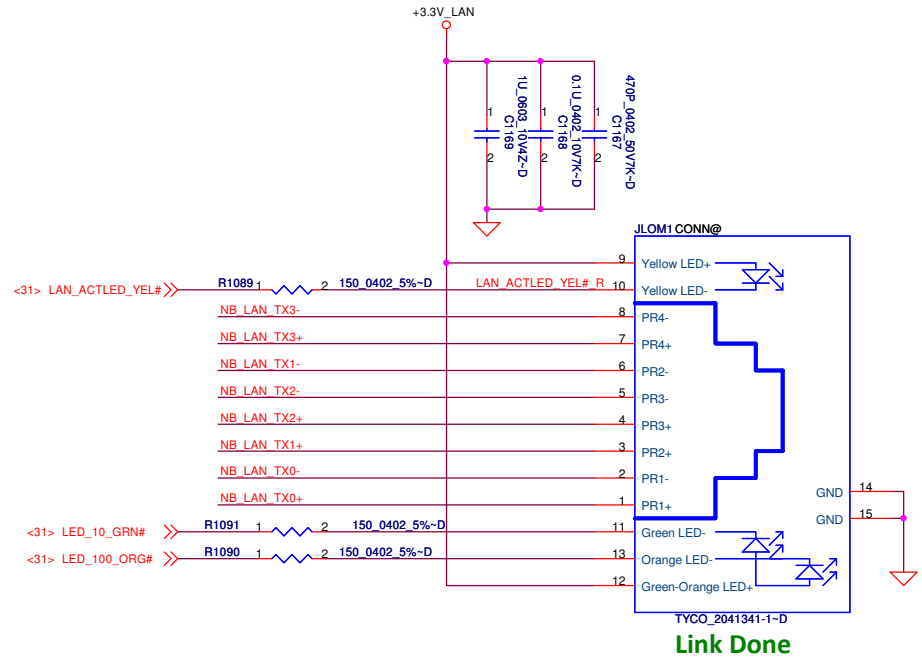
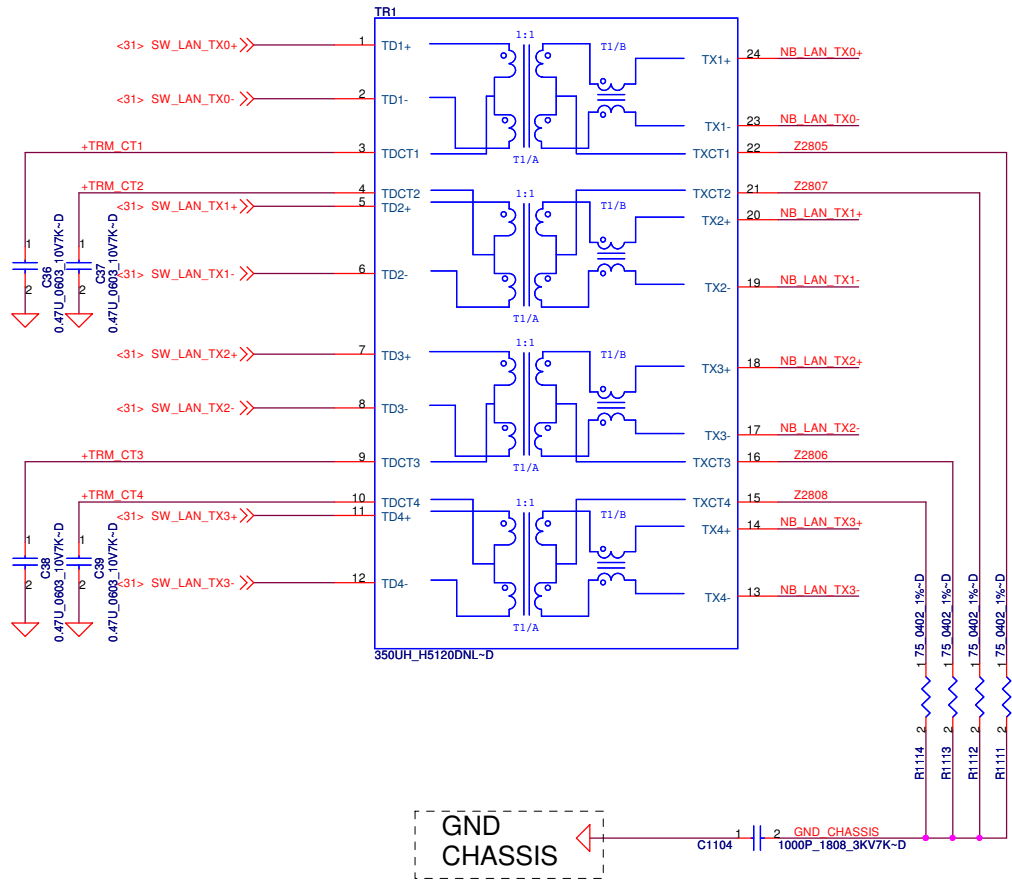
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

- Fiducial Mark**
- FD1
 - FIDUCIAL MARK-D
 - FD2
 - FIDUCIAL MARK-D
 - FD3
 - FIDUCIAL MARK-D
 - FD4
 - FIDUCIAL MARK-D



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Link Done

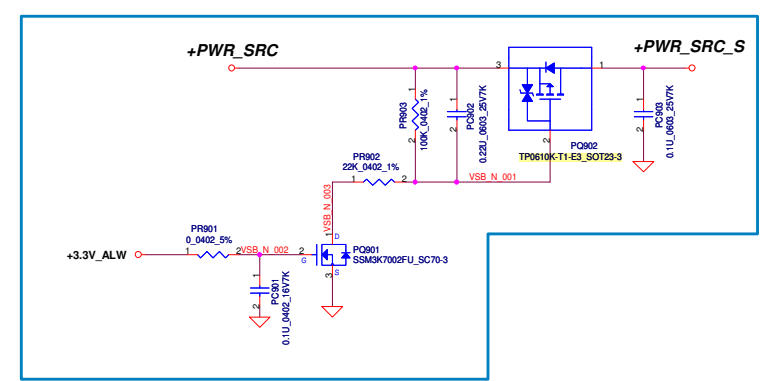
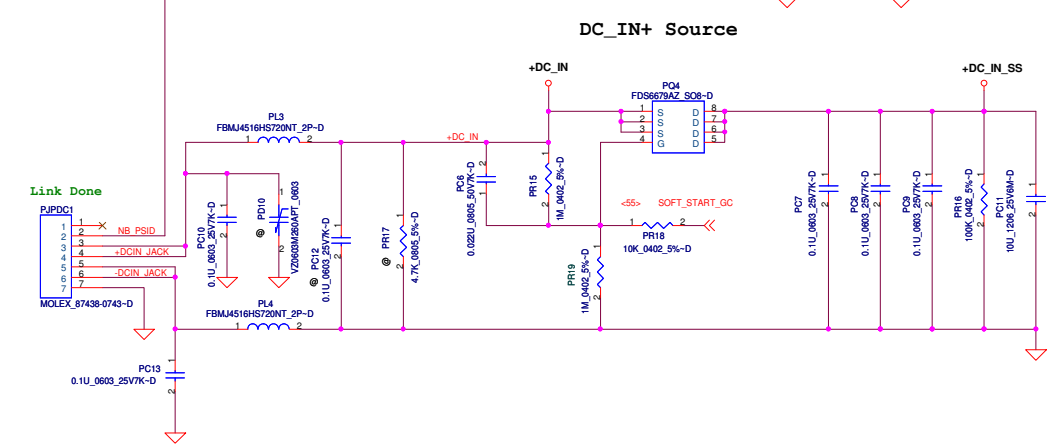
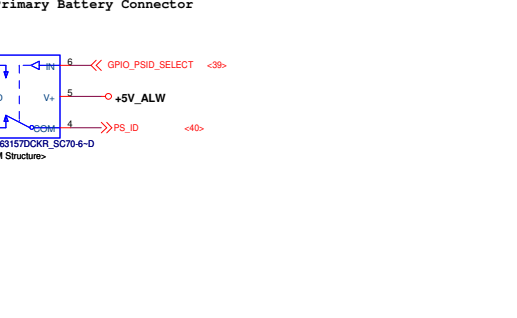
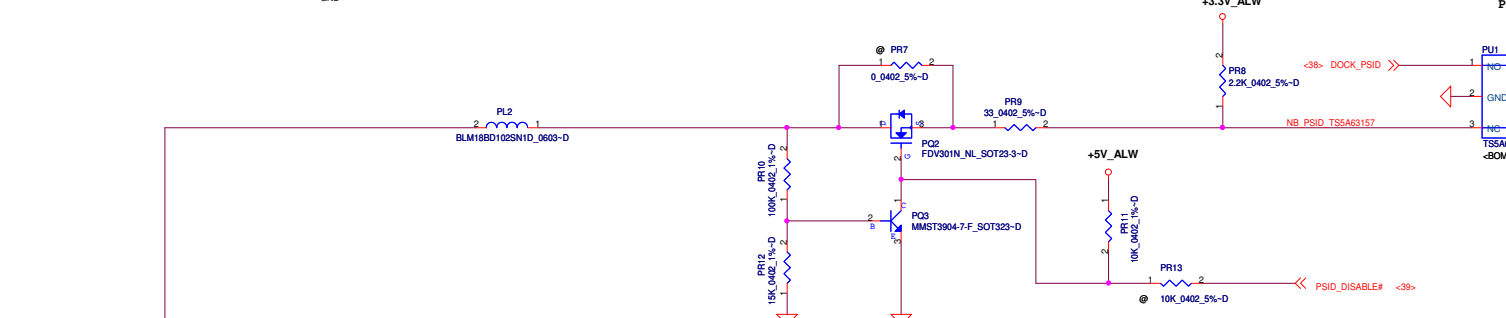
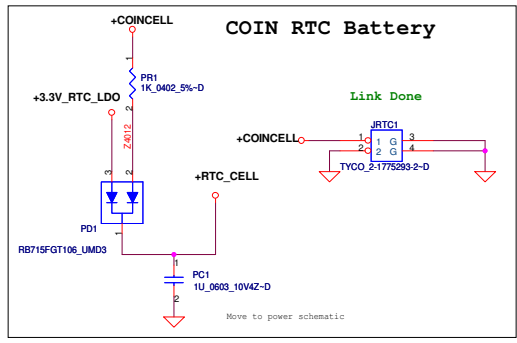
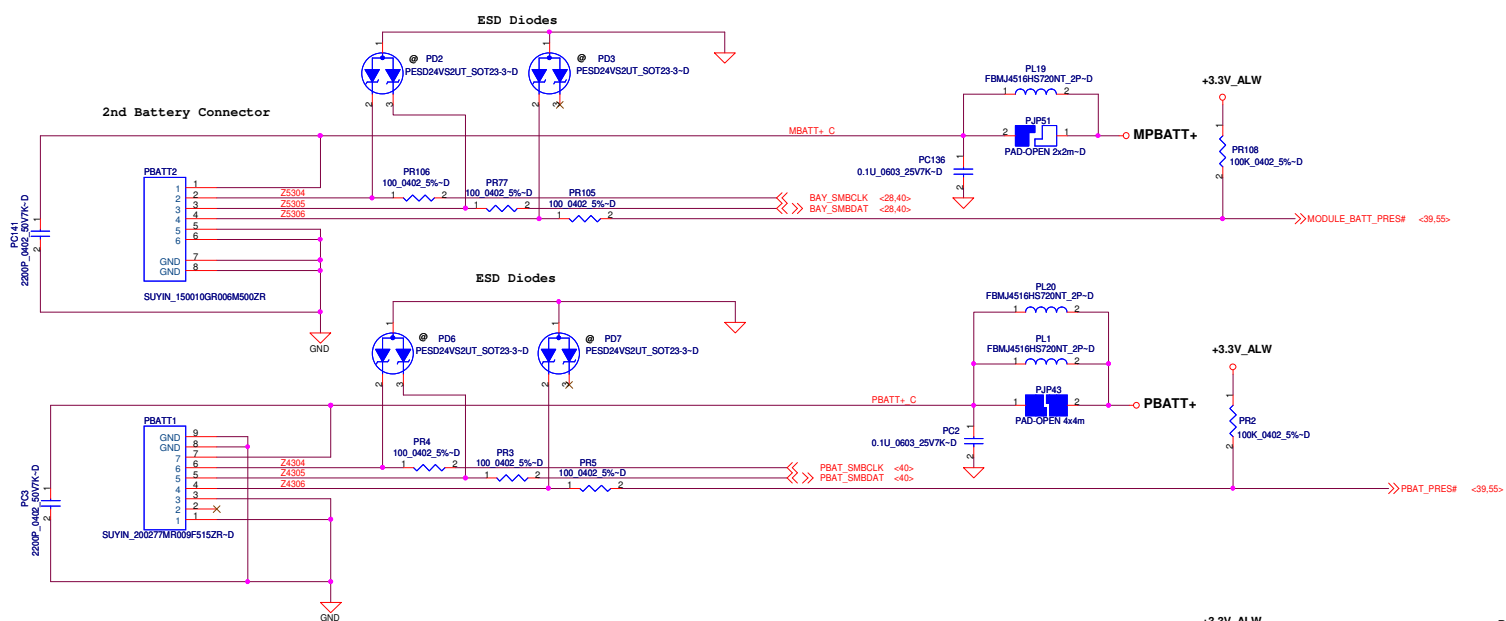
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		+DCIN	
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3.3VALWP +/- 5%
 TDC=5.45A
 Peak Current=7.786A
 OCP min=10.122A
 L/S RDS(on) 14.2m ohm(typ), 17.5m ohm(max)
 FSW=375KHz
 Delta_Iin=1.246A
 Delta_Io=3.3231A

+5V_ALWP / +3.3V_ALWP

Charlie_note :

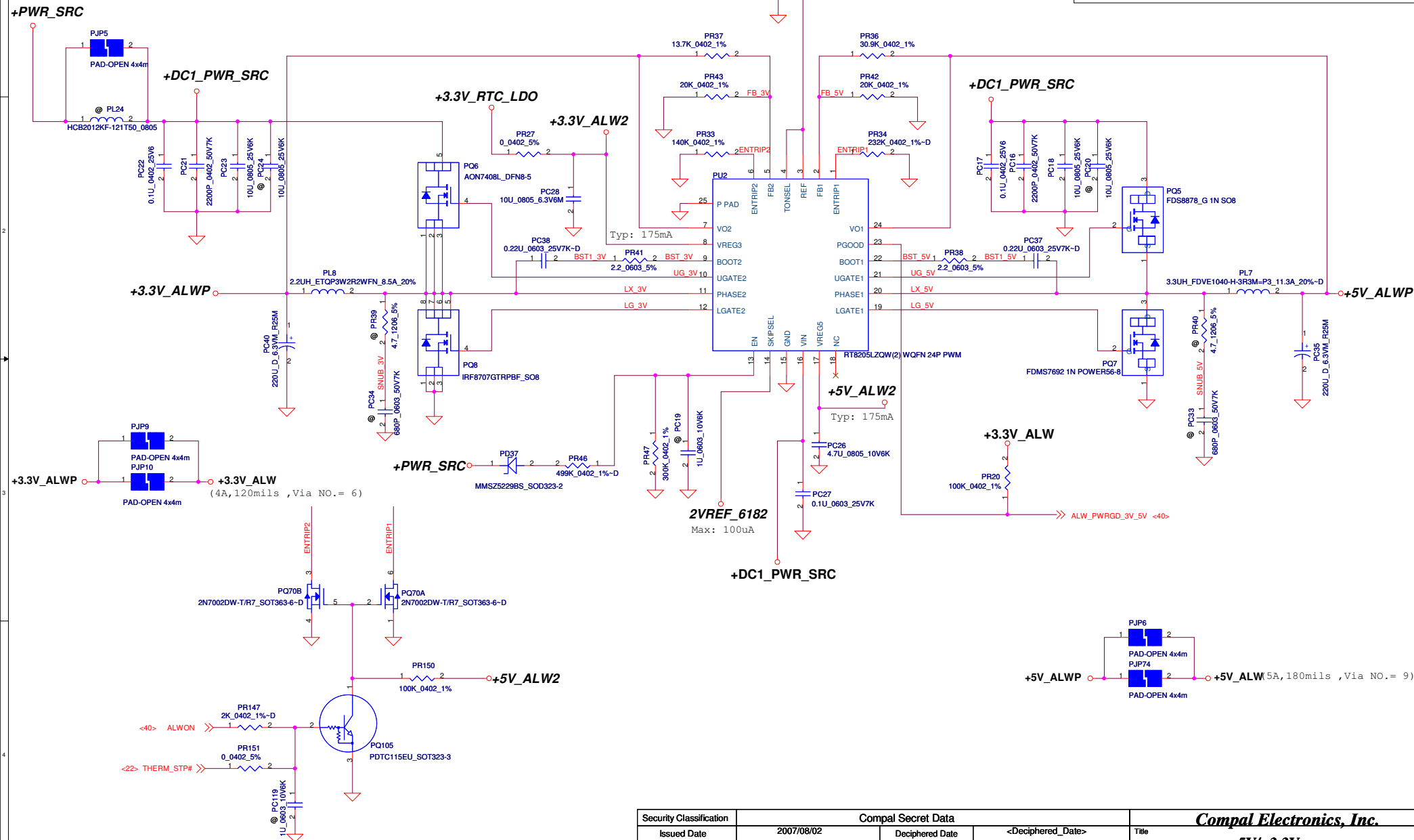
SKIPSEL Connect to REF : DEM Mode

@DEM VFBx=2.0V

TONSEL

Frequency Selectable Input for VOUT1(+5V)/VOUT2(+3.3V) respectively.
 300kHz/375kHz : Connect to REF

5VALWP +/- 5%
 TDC=8.41A
 Peak Current=12.012A
 OCP min=15.62A
 L/S RDS(on) 14.2m ohm(typ), 17.5m ohm(max)
 FSW=300KHz
 Delta_Iin=1.64A
 Delta_Io=3.756A

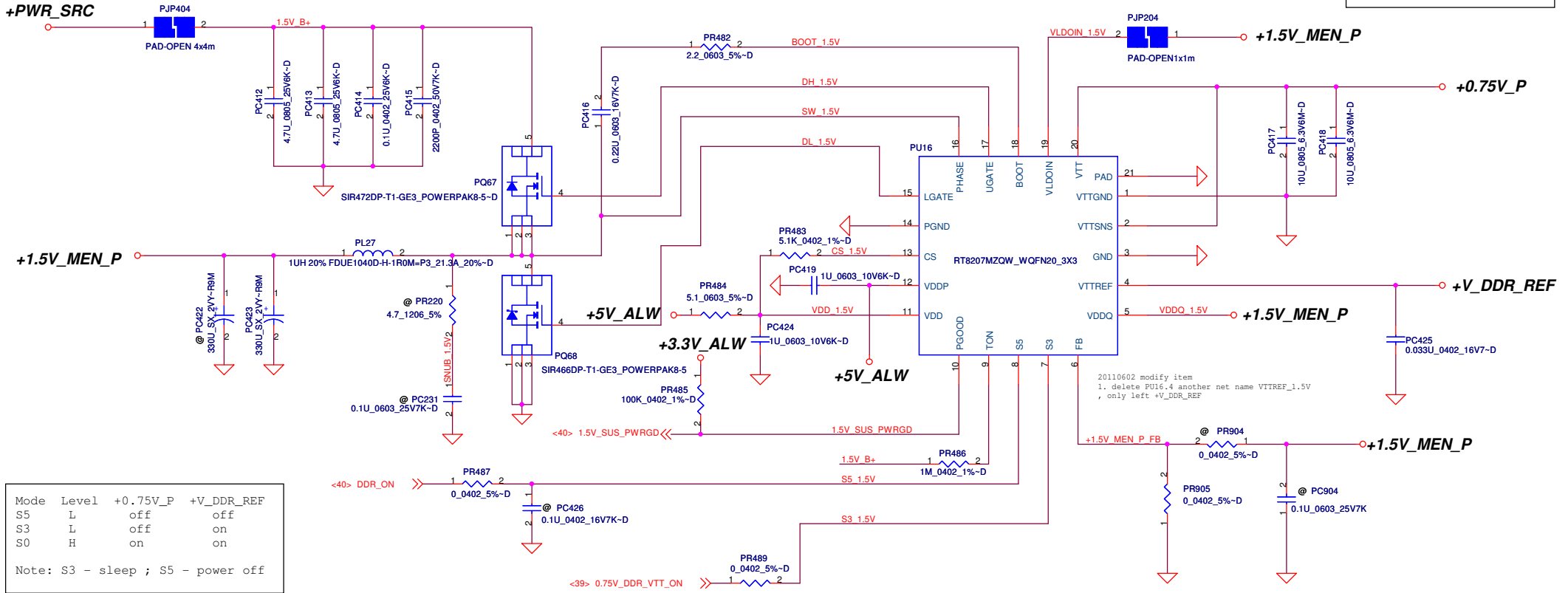


Security Classification	Compal Secret Data			Title		
Issued Date	2007/08/02	Deciphered Date	<Deciphered_Date>	5V/+3.3V		
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1.5Volt +/- 5%
 TDC=7.18A
 Peak Current=10.25A
 OCP min=13.33A
 L/S RDS(on) 3.8m ohm(typ), 4.8m ohm(max)
 FSW=253KHz for RTON=1M ohm, spec. On-Time =303.947ns
 Delta_Iin=1.458A
 Delta_Io=5.4728A

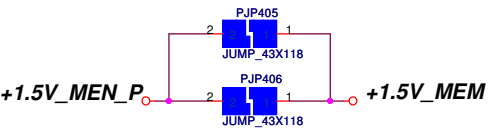
+1.5V_MEN_P/ +0.75V_P

0.75Volt +/- 5%
 TDC=0.525A
 Peak Current=0.75A
 OCP min=0.975A



Mode	Level	+0.75V_P	+V_DDR_REF
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



(2A, 80mils, Via NO. = 4)

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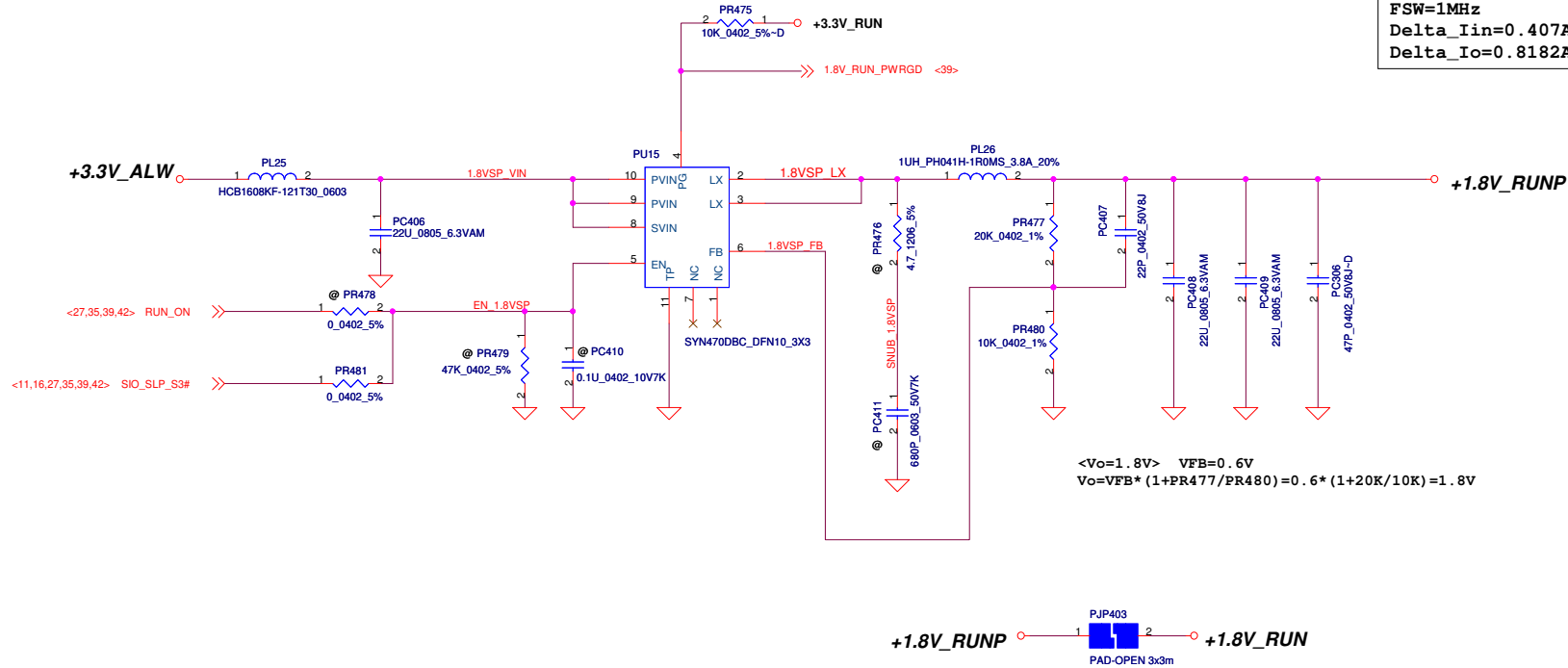
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Title: +1.5V_MEN/+0.75V_DDR_VTT		
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+1.8V_RUNP

1.8Volt +/-5%
 TDC=0.81A
 Peak Current=1.157A
 OCP min=1.5A

FSW=1MHz
 Delta_Iin=0.407A
 Delta_Io=0.8182A



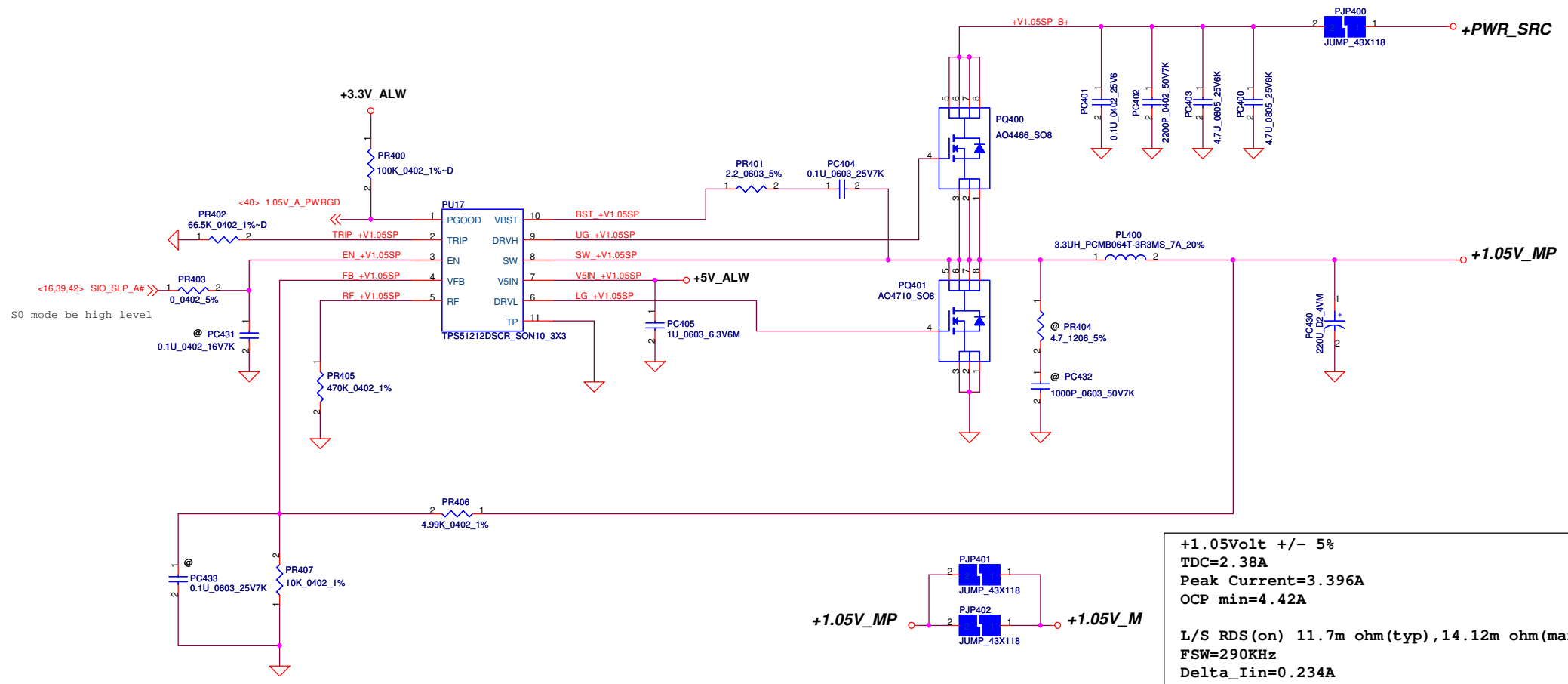
<Vo=1.8V> VFB=0.6V
 $V_o = V_{FB} * (1 + PR477 / PR480) = 0.6 * (1 + 20K / 10K) = 1.8V$

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+1.8V_RUN		
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+1.05V_MP



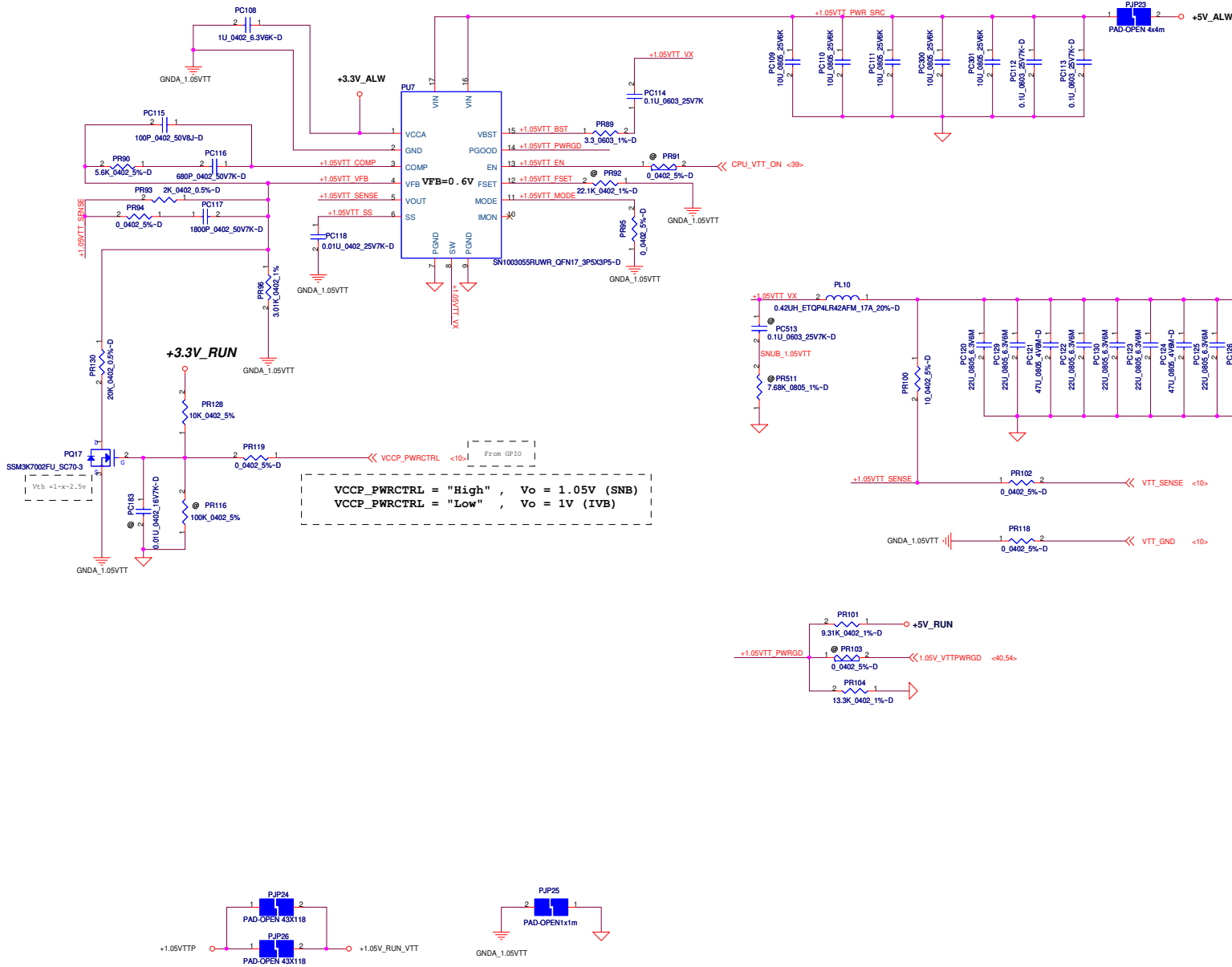
+1.05Volt +/- 5%
TDC=2.38A
Peak Current=3.396A
OCP min=4.42A
L/S RDS(on) 11.7m ohm(typ), 14.12m ohm(max)
FSW=290KHz
Delta_Iin=0.234A
Delta_Io=1.038A

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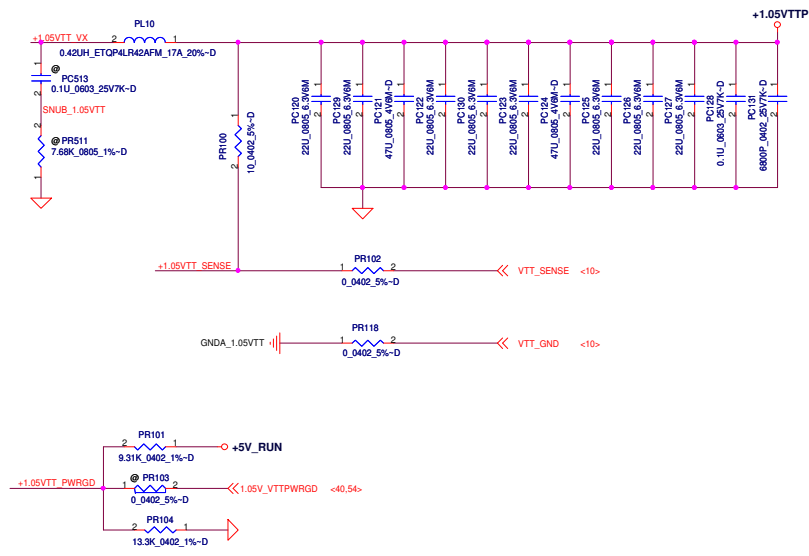
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			+1.05V_M	
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+1.05VTTT



1.05Volt +/-5%
 TDC=4.49A
 Peak Current=6.411A
 OCP min=8.334A
 FSW=1MHz
 Delta_{lin}=0.804A
 Delta_{lo}=1.975A

VCCP_PWRCTRL <10> From GP10
 VCCP_PWRCTRL = "High" , Vo = 1.05V (SNB)
 VCCP_PWRCTRL = "Low" , Vo = 1V (IVB)



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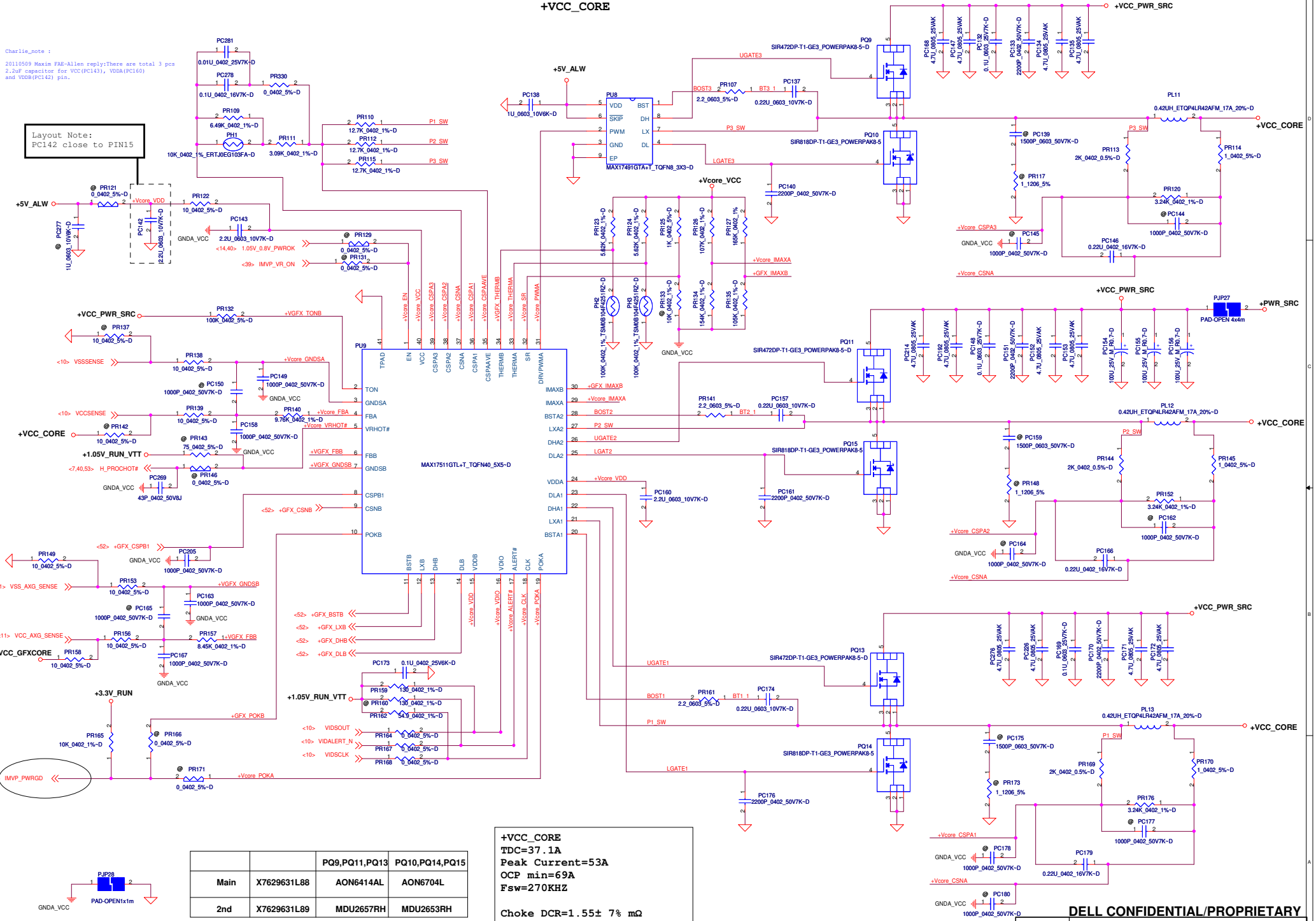
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+VCC_CORE

Charlie_note :
 20110509 Maxin FAB-Allen reply:There are total 3 pcs
 2.2uF capacitor for VCC(PC143), VDDA(PC160)
 and VDDP(PC142) pin.

Layout Note:
 PC142 close to PIN15



		PQ9,PQ11,PQ13	PQ10,PQ14,PQ15
Main	X7629631L88	AON6414AL	AON6704L
2nd	X7629631L89	MDU2657RH	MDU2653RH

+VCC_CORE
TDC=37.1A
Peak Current=53A
OCp min=69A
Fsw=270KHZ
Choke DCR=1.55± 7% mΩ

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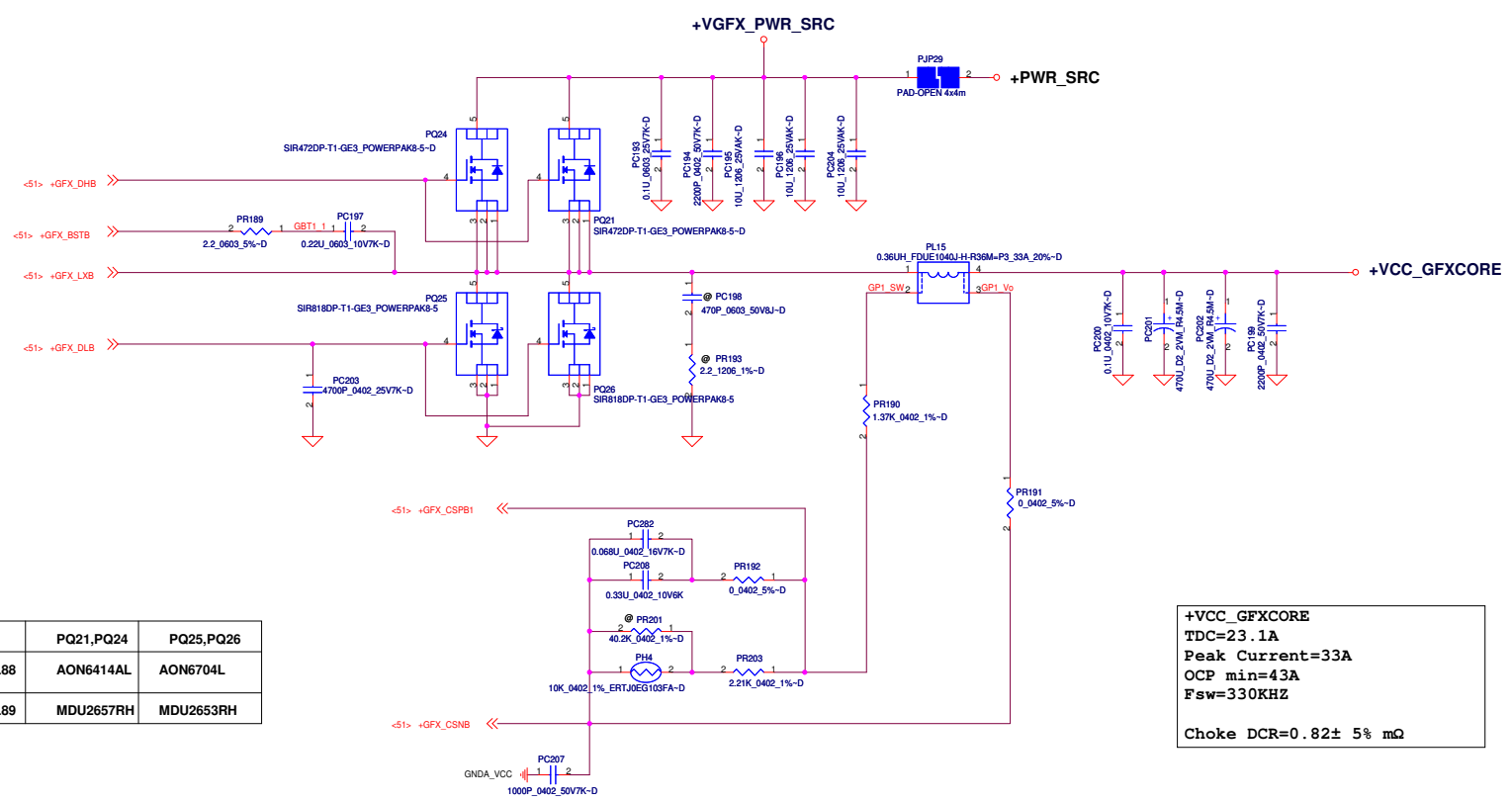
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Vcore

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		PQ21,PQ24	PQ25,PQ26
Main	X7629631L88	AON6414AL	AON6704L
2nd	X7629631L89	MDU2657RH	MDU2653RH

+VCC_GFXCORE
TDC=23.1A
Peak Current=33A
OCp min=43A
Fsw=330KHZ

Choke DCR=0.82± 5% mΩ

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Title: **ISL95870A +1.05V RUN VTT**

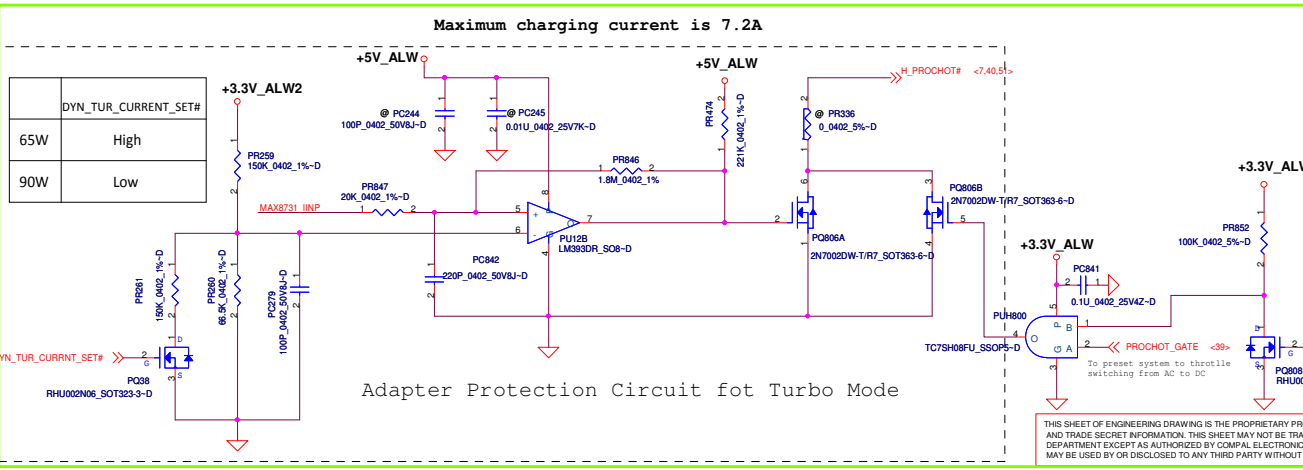
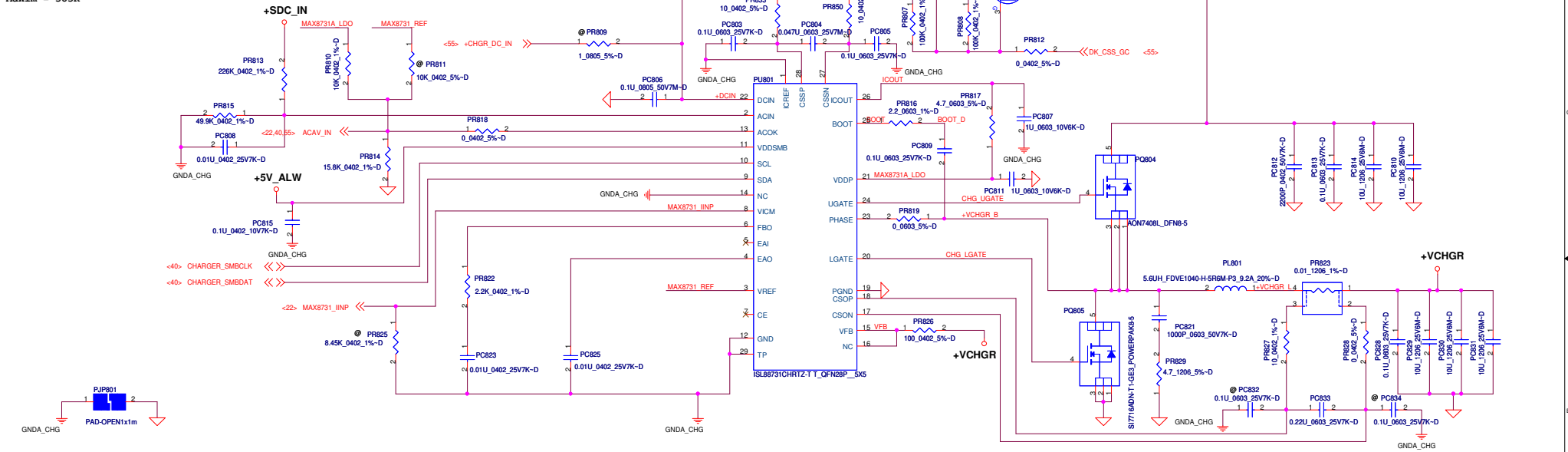
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Adapter Protection Event			
	PR521	PR522	PR510
SW	0 Ohm	@	100k
HW	@	0 Ohm	@

E2 AC_OK=17.7 VoIt

PR813
 TI bq24745 = 316K
 Intersil ISL88731 = 226K
 Maxim = 383K



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Charger

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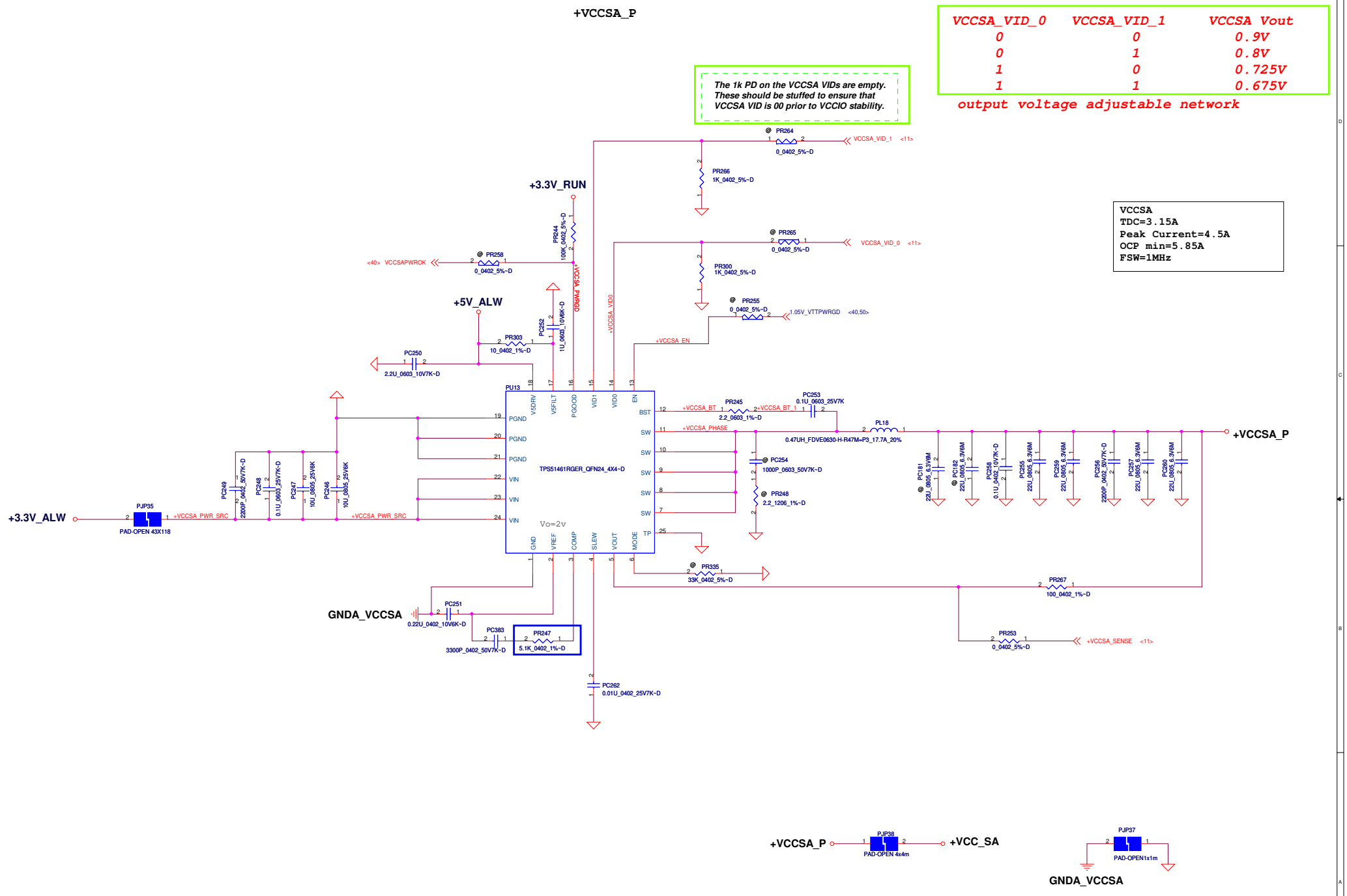
+VCCSA_P

VCCSA_VID_0	VCCSA_VID_1	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VCCSA
TDC=3.15A
Peak Current=4.5A
OCF min=5.85A
FSW=1MHz



+3.3V_ALW

+3.3V_RUN

+5V_ALW

GNDA_VCCSA

+VCCSA_P

GNDA_VCCSA

+VCCSA_P

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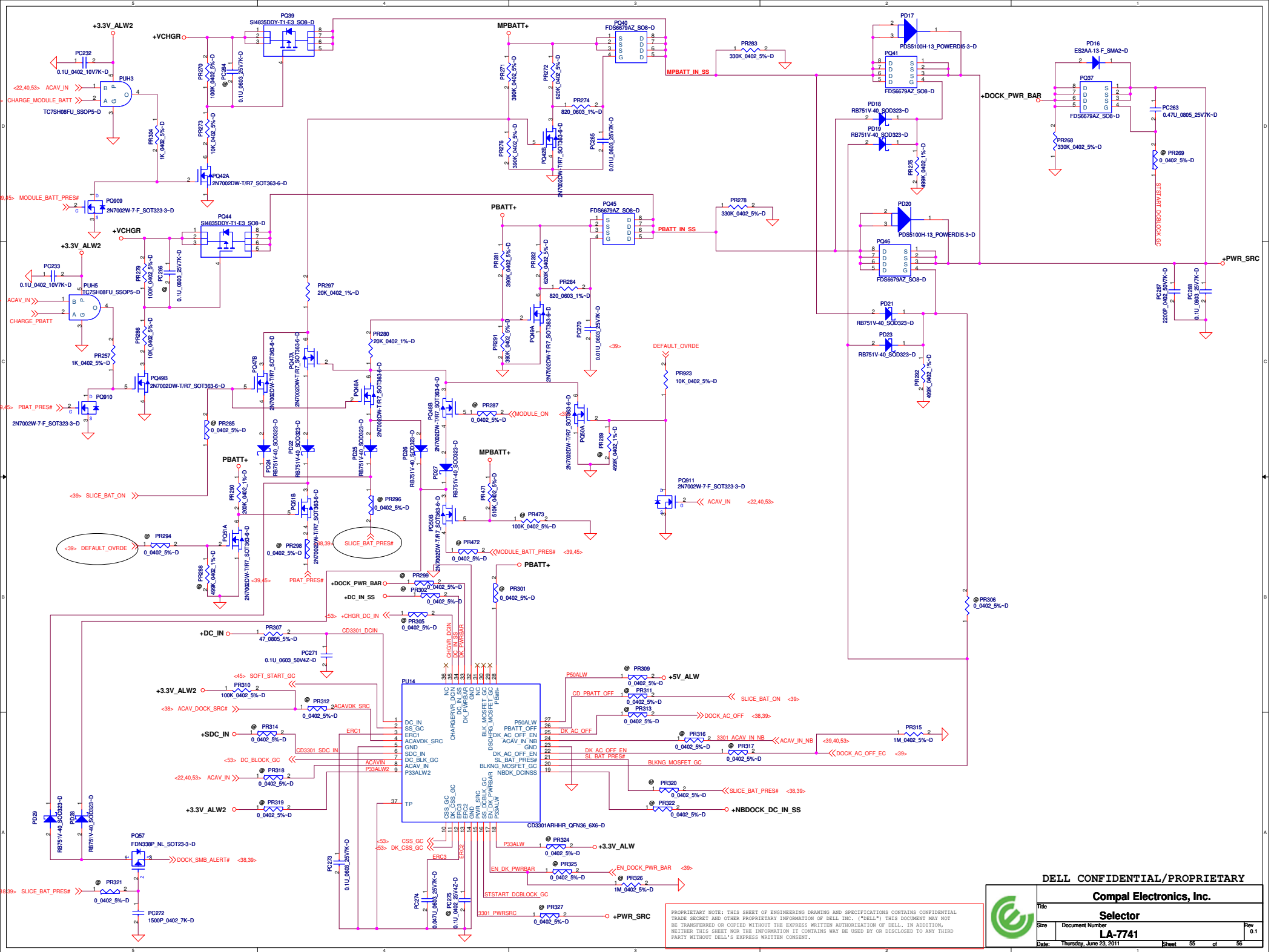
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Title: **ISL95870A 0.8V VCC SA**

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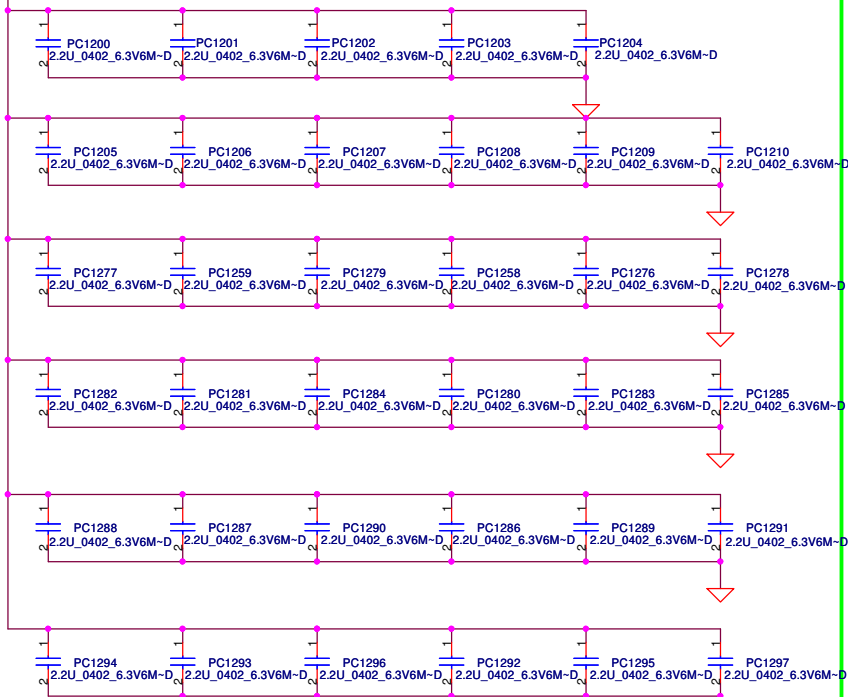
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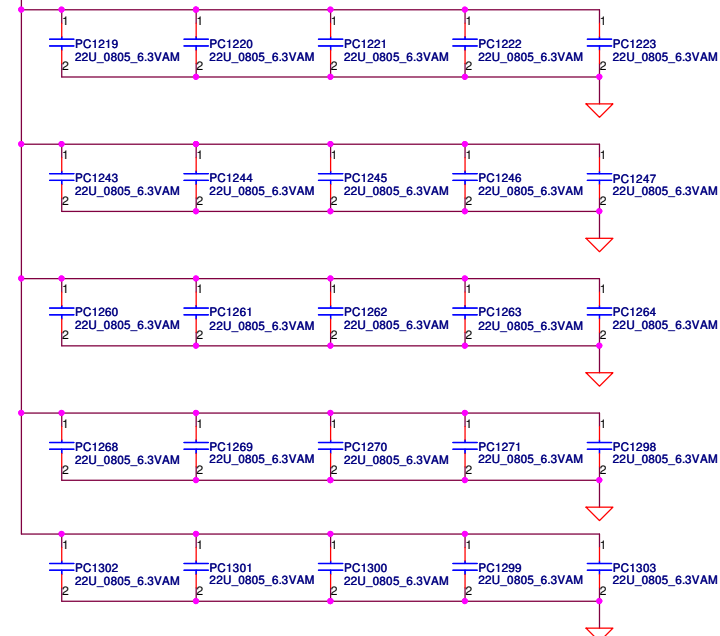
+VCC_CORE

Charlie note:
1.2.2uF*35 (SE00000888L)
2.22uF*25 (SE00000880)
Vcore_Cout2
1.470uF 4.5m *4 (SGA00004X8D)

+VCC_CORE



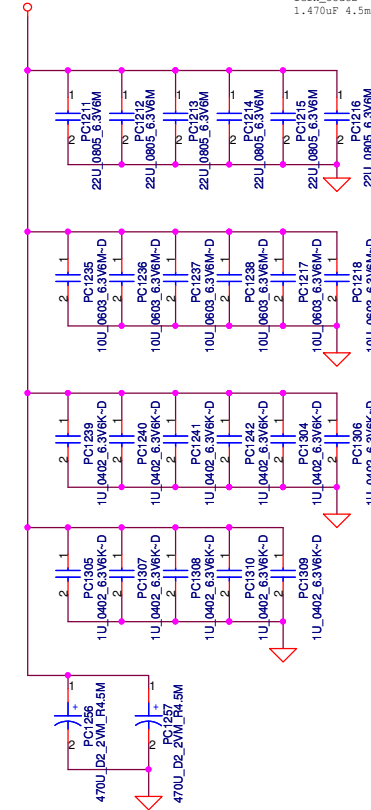
+VCC_CORE



+VCC_GFXCORE

Charlie note:
1.GFX_Cout1
1.22uF*6 (SE000000110)
2.10uF*6 (SE00000578L)
3.11uF*11 (SE00000088L)
iGFX_Cout2
1.470uF 4.5m *2 (SGA00004200)

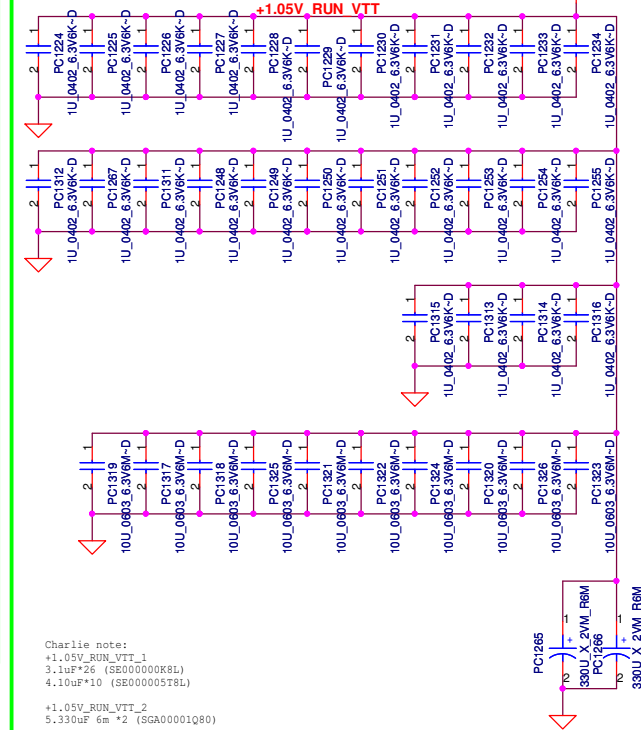
+VCC_GFXCORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

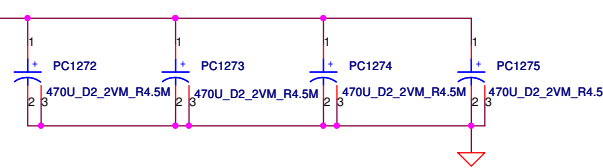
+1.05V_RUN_VTT



Charlie note:
+1.05V_RUN_VTT_1
3.1uF*26 (SE00000088L)
4.10uF*10 (SE00000578L)
+1.05V_RUN_VTT_2
5.330uF 6m *2 (SGA00001Q80)

+VCC_CORE

+VCC_CORE



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PROCESSOR DECOUPLING

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